SERVICE MANUAL FOR

M762

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TESTING TECHNOLOGY DEPARTMENT / TSSC

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MiTAC

M762 N/B Maintenance

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1. Hardware Engineering Specification

1.1 Introduction

1.1.1 General Description

This document describes the system hardware engineer specification for M762 portable notebook computer system. The M762 notebook computer is a new mainstream high performance thin and light notebook in the MiTAC notebook family.

1.1.2 System Overview

CPU	Intel Mobile Tualatin PIII, CuMine-T/Tualatin Celeron CPUs, uFCPGA478 Package
Video	- Dual independent displays (LCD/CRT) - Support Motion Compensation and iDCT - Support Simultaneous display
Memory	One 144pin SO-DIMM, On-Board Memory 128MByte
PCMCIA	- Support one slot of Type II - Non support Zoom Video/Audio Function
IDE	Support 2 IDE channel, up to Ultra DMA100
LCD Display	- Support 65MHz LVDS interface - Support up to XGA (1024*768) Resolution

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Button	5 Easy Start Button (function defined by user), One Email Button
LAN	Support to 10/100 Based T
Modem	56Kbps V.90 MDC Modem
Pointing	Glide PAD with 2 buttons
Keyboard	Internal Key Matrix Keyboard
BIOS	512KB Flash EEPROM (Include System BIOS & VGA BIOS)
Audio	- AC'97 Interface Codec. Sound Blaster Pro Compatible - Built-In One 1W speaker and 1 Mono-Microphone
I/O Port	- External VGA Port (D-SUB 15Pins) - 2 Standard USB 1.1 Port - RJ-11 port for modem - RJ-45 Port for LAN - DC Input Jack - IR port - Battery Connector - SPIDF Jack - Microphone In Jack - VR for Audio Volume Control - Mini IEEE1394 Port
Suspend Mode	POS (S1) , Suspend to RAM (S3) , Suspend to Disk (S4),NO SUPPORT WAKE UP ON TIME
Indicator	HDD/CD-ROM,Num Lock,Caps Lock,Scroll Lock LEDs

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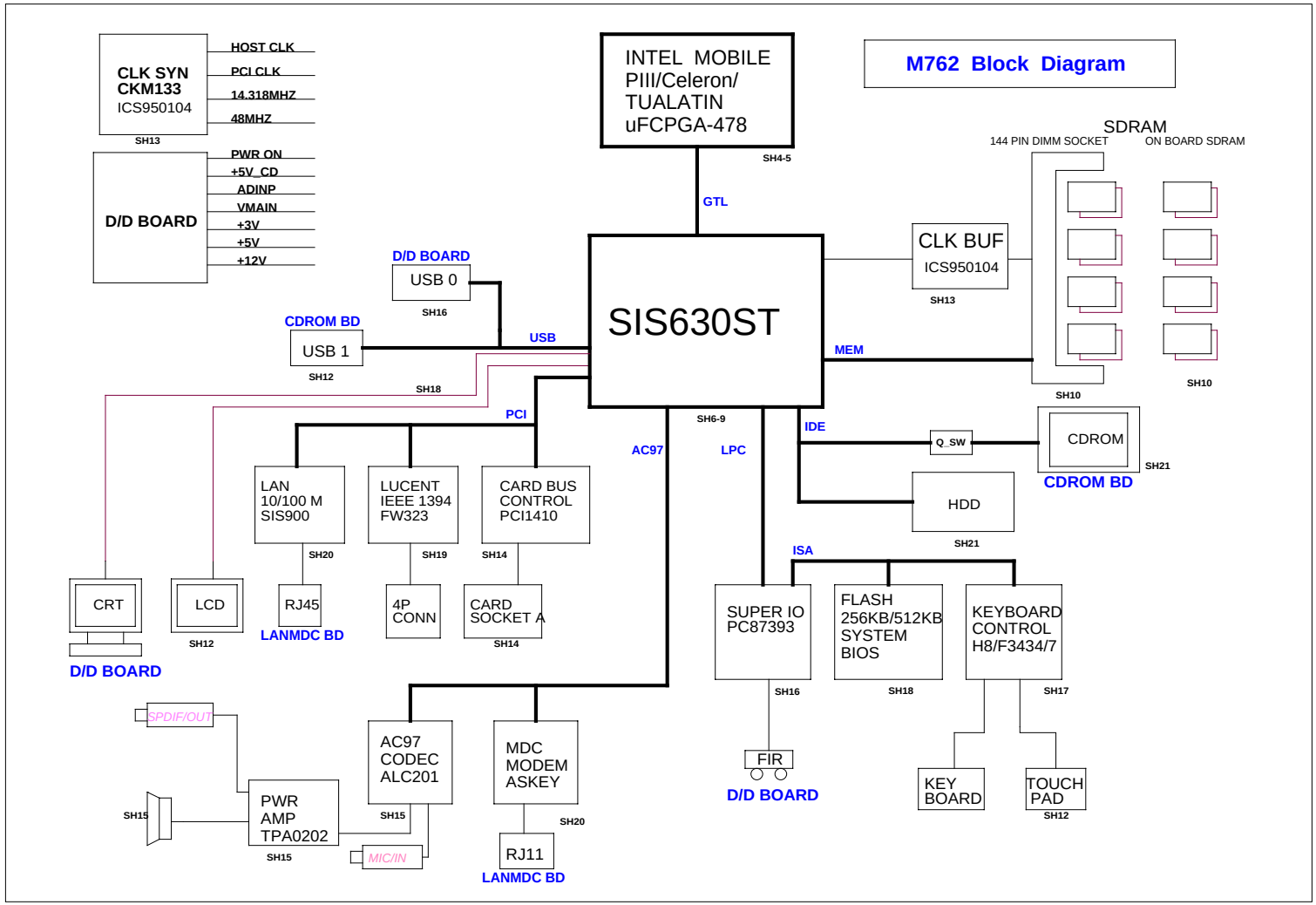
1.2 System Architecture

1.2.1 Block Diagram (without Power System)



1.2.2 Function Description

1.2.2.1 CPU

- Socket able for Intel Mobile Tualatin PIII, CuMine-T/Tualatin Celeron
- Capable of uFCPGA478 processor package
- Supports Enhanced Intel SpeedStep technology (PIII-M)

1.2.2.2 Core Logic

- Integrated Ultra AGP VGA for Hardware 2D/3D Video/Graphics Accelerators
- Integrated DRAM Controller
- Integrated AGP Compliant Target/66MHz Host-to-PCI Bridge
- Low Pin Count Interface
- PCI 2.2 Specification Compliant
- Integrated Host-to-PCI Bridge
- Fast PCI IDE Master/Slave Controller
- Integrated Advanced PCI H/W Audio & V.90 HSP Modem
- Universal Serial Bus Host Controller
- Integrated DMA Controller
- Advanced Power Management
- 672-Balls BGA Package

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1.2.2.3 Memory

- 128MB PC133 SDRAM on board one SO-DIMM slot expandable to 640MB
- Support 3.3V PC100/PC133 SDR SDRAM.

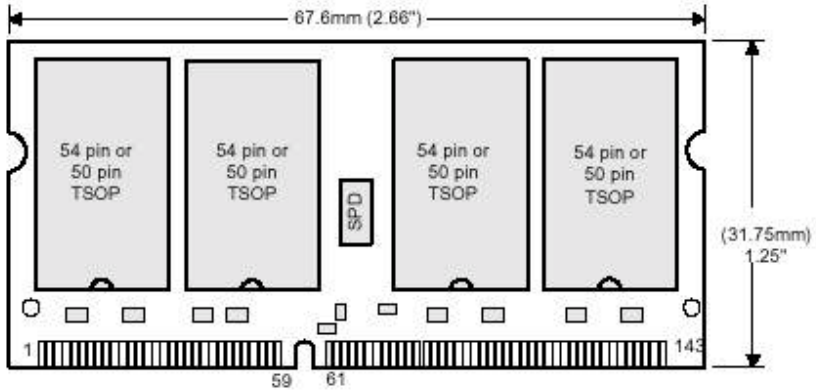

Figure 1. SO-DIMM Module

On board	Slot1	Total
128MB	0	128MB
128MB	64MB	192MB
128MB	128MB	256MB
128MB	256MB	384MB
128MB	512MB	640MB

Table 1. Memory Expansion Capacity

1.2.2.4 I/O Ports

CRT Port

- Standard VGA compatible port
- DDC1 and DDC2B compliant
- Support up 1024*768 resolution(Max1920x1440)

PIN	SIGNAL	DESCRIPTION
1	RED	Red analog video output
2	GREEN	Green analog video output
3	BLUE	Blue analog video output
4	Monitor Sense	Monitor Sense
5	GND	Ground
6	GND	Ground
7	GND	Ground
8	GND	Ground
9	VCC	+5VDC
10	GND	Ground
11	Monitor Sense	Monitor Sense
12	CRT DATA	Data from DDC monitor
13	HSYNC	Horizontal Sync control
14	VSYNC	Vertical Sync control
15	CRT CLK	Clock to DDC monitor

Table 2. CRT Connector

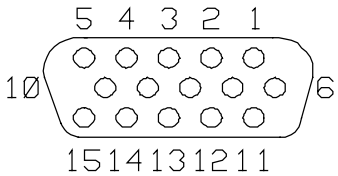

Figure 2. CRT Connector

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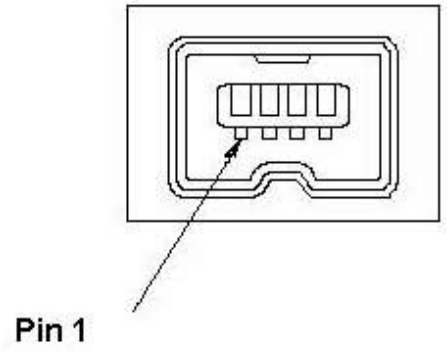
IEEE 1394 Port

- Support IEEE 1394a
- Support Hot-Plug

Pin	Signal Name	Direction
1	TPB-	I/O
2	TPB+	I/O
3	TPA-	I/O
4	TPA+	I/O

Table 3. IEEE 1394 Port



Audio Ports

- SPDIF output
- Microphone in
- Built in one high quality internal speaker (1W)
- Built in 1 mono microphone

RJ-11

- Connection to Modem Daughter Board Connector
- Support Modem RING_UP from S3

Pin	Signal Name	Direction	Description
1	NC	-	No Connect
2	LINE +	I/O	Phone Line Positive
3	LINE -	I/O	Phone Line Negative
4	NC	-	No Connect

Table 4. Modem Port

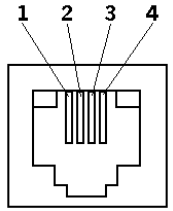


Figure 3. Modem Connector

RJ-45

- Connection to on-board NIC controller

Pin	Signal Name	Direction	Description
1	TX+	Out	Transmit Data Ring
2	TX-	Out	Transmit Data Tip
3	RX+	IN	Receive Data Ring
4	TERM 1	-	Internal termination resistor
5	TERM 2	-	Internal termination resistor
6	RX	IN	Receive Data Tip.
7	TERM 3	-	Internal termination resistor
8	TERM 4	-	Internal termination resistor

Table 5. LAN Port

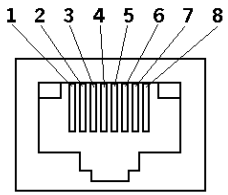


Figure 4. LAN Connector

Infrared interface supporting IRDA format

- Fully compliant IrDA1.1
- Typical Link Distance <=1m

USB Ports

- Two industry standard USB 1.1 ports

Pin	Signal Name	Direction	Description
1	VCC	-	USB Device Power (+5VDC)
2	DATA-	I/O	Balanced Data Negative
3	DATA+	I/O	Balanced Data Positive
4	GND	-	Ground

Table 6. USB Port

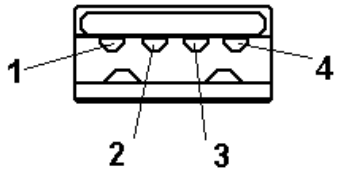


Figure 5. USB Connector

1.2.2.5 PCMCIA Slot

- One Type II slot support full R2 (16-bit) and 32-bit Cardbus data transfer
- TI PCI1410 (PCMCIA Controller) & TI TPS2211 (Power Switch)

1.2.2.6 Graphical Subsystem

- Supports Shared Memory Size from 8MBytes to 64MBytes

1.2.2.7 Display

- Internal LCD Display is 12.1” TFT XGA color (1024 x 768)
- Low driving voltage and low power consumption
- 3.3V power supply
- 1 Channel LVDS Interface
- Single CCFL (Bottom side/Horizontal Direction)
- Data enable signal mode
- Side mounting frame

1.2.2.8 Read Only Memory (BIOS Flash)

- Fully compatible with industry standard software including Windows 2000 & Windows XP
- Fully supports APM V1.2 and latest ACPI specification
- 4MB Flash BIOS
- Insyde BIOS core

1.2.2.9 Power Management Features

- Meets ACPI 1.0 Requirements
- Meets APM 1.2 Requirements
- ACPI Sleep States Include S1orS3,S4,S5
- CPU Power States Include C0, C1, C2
- LED Blinking in S1 and S3 States
- System Power-Up Events Include: Power Button, Hot-Key, RTC Alarm, Modem Ring-In, LAN, PME#
- Software Watchdog Timer
- PCI Bus Power Management Interface Spec. 1.0

1.2.2.10 Keyboard Controller

- Hitachi H8-3434F

1.2.2.11 Super I/O

- NS PC87393F LPC interface Ultra I/O

1.2.2.12 LEDs Indicator

- System has nine status LED indicators to display system activity which include below LCD panel unit and above keyboard:
- Three LED indicators below LCD panel unit:
  From left to right that indicate AC POWER, BATTERY POWER and BATTERY STATUS

POWER LED: This LED lights green when the notebook is being powered by AC, and flash (on 1 second, off 1 second) when suspend to DRAM or standby mode is active using AC power. The LED is off when the notebook is off or powered by batteries, or when suspend to disk.

BATTERY STATUS: During normal operation, this LED stays off as long as the battery is charged. When the the battery charge drops to 10% of capacity, the LED lights red, flashes per 1 second and beeps per 2 second. When AC is connected, this indicator glows green if the battery pack is fully charged, or orange (amber) if the battery is being charged.

Four LED indicators in front of palm rest:
From left to right that indicates CD-ROM/MO/Hard Disk Drive, NUM LOCK, CAPS LOCK and SCROLL LOCK.

Email LED indicators in front of palm rest:
The green LED flashing means new mail coming. Otherwise the Led is always OFF.

1.2.2.13 Buttons

- ACPI Power Button
- ACPI Sleep Button
- ACPI System Button
- Easy Start Button

1.2.2.14 Modem

Pin	Signal Name	Pin	Signal Name
1	MONO_OUT	2	NC
3	GND	4	MODEM_SPK
5	NC	6	NC
7	NC	8	GND
9	NC	10	+5V
11	NC	12	NC
13	NC	14	NC
15	GND	16	Pull Up to +3V
17	+3V	18	+5V
19	GND	20	GND
21	+3V	22	ACSYNC
23	ACSDOUT	24	MSDIN
25	-ACRST	26	MSDIN
27	GND	28	GND
29	GND	30	ACBITCLK

Table 7. Modem Daughter Board Connector

1.3 Appendix 1: GPIO Definitions

Chipset GPIO

Pin Name	Signal Name	Power Plane	Type Define	Original Type	During PCIRST#	Immediately After PCIRST#	S1	S3	S4/S5	Description
GPIO0/REQA#	LCD_ID0	+3V(main)	I	I/O	In	In	Defined	Off	Off	
GPIO1/REQB#/REQ5#	LCD_ID1	+3V(main)	I	I/O	In	In	Defined	Off	Off	
GPIO2/PIRQE#	TP			I/O	In	In	Defined	Off	Off	
GPIO3/PIRQF#	TP			I/O	In	In	Defined	Off	Off	
GPIO4/PIRQG#	CDROM_PLUG#	+3V(resume)	I	I/O	In	In	Defined	Off	Off	
GPIO5/PIRQH#	RST_CDROM	+3V(resume)	O	I/O	In	In	Defined	Off	Off	
GPIO6	EXTSMI#	+3V(resume)	I	I/O	In	In	Defined	Off	Off	
GPIO7	SPDIF	+3V(main)	O	I/O	In	In	Defined	Off	Off	
GPIO8	SPK_OFF#	+3V(resume)	O	I/O	In	In	Defined	Off	Off	
GPIO9	CD_PWR#	+3V(resume)	O	I/O	In	In	Defined	Off	Off	
GPIO10	VR_HI/LO#	+3V(resume)	O	I/O	In	In	Defined	Off	Off	
GPIO11	CPU_LO/HI#	VTT(resume)	O	I/O	In	In	Defined	Off	Off	
GPIO12	VGATE#	+3V(resume)	O	I/O	In	In	Defined	Off	Off	
GPIO13	TP			I/O	In	In	Defined	Off	Off	
GPIO14	CRT_IN#	+5V(resume)	O	I/O	In	In	Defined	Off	Off	
GPIO15	TP			I/O	In	In	Defined	Off	Off	

1.4 Appendix 2: Keyboard Controller Pin Definitions

Pin	Port	Signal Name	Type	Connect To	Description
79~72	P10~P17	KO[0:7]	O	Internal Keyboard	Keyboard Matrix
67~60	P20~P27	KO[8:15]	O	Internal Keyboard	Keyboard Matrix
82~89	P30~P37	SD[0:7]	I/O	Super I/O	ISA data bus
49	P40	H8_PWRON_SIS	O	SiS630ST & CPU	Control system power ON/OFF
50	P41	H8_WAKEUP#	O	SiS630ST	Connect to chipset SiS630ST to wake up system
51	P42	H8_SMI#	O	SiS630ST	Connect to chipset SiS630ST to system management interrupt (Non-ACPI mode)
52	P43	H8_SCI	O	SiS630ST	Connect to chipset SiS630ST to system management interrupt (ACPI mode)
53	P44	IRQ1	O	Super I/O	IRQ for keyboard
54	P45	IRQ12	O	Super I/O	IRQ for mouse
55	P46	BLADJ	O	LCD Connect	Reserve
56	P47	FANON#	O	FAN	Control CPU Core FAN ON/OFF duty
14	P50	H8_PWR_ON	O	DC/DC Connector	Control system power ON/OFF
13	P51	LEARNING	O	DD Board	Control DD Board voltage, negative logic
12	P52	H8_12V	O		No use
26~29	P60~P63	KI[0:3]	I	Internal Keyboard	Keyboard Matrix
30~35	P64~P67	KI[4:7]	I	Internal Keyboard	Keyboard Matrix
38	P70	BAT_TEMP	I	Battery	Report battery thermal
39	P71	BAT_VOLT	I	Battery	Report battery voltage
40	P72	+S3V	I	Power	Detect power level
41	P73	VCC_CORE	I	Power	Detect power level
42	P74	VTT	I	Power	Detect power level
43	P75	+S5V	I	Power	Detect power level
44	P76	CHARGE_I_CTR	O	Charger Circuitry	Control charge battery voltage level
45	P77	BLADJ	O	Inverter	Back/Light adjust control
93	P80	SA2	I	Super I/O	ISA address
94	P81	TP31			No use
95	P82	H8_KBCS#	I	Super I/O	Port 62H/66H chip select
96	P83	IOR#	I	Super I/O	Input/Output read
97	P84	IOW#	I	Super I/O	Input/Output write
98	P85	H8_MCCS#	I	Super I/O	Port 60H/64H chip select
99	P86	BAT_CLK	I/O	Battery	SM_BUS clock for smart battery

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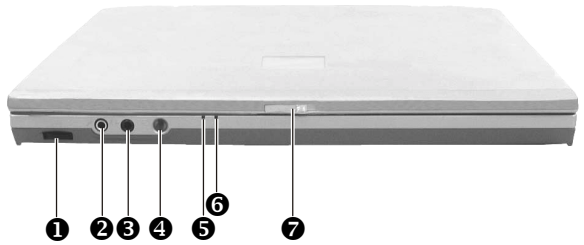
Pin	Port	Signal Name	Type	Connect To	Description
25	P90	H8_SUSC#	I	SiS630SR	System inter S4~S5
24	P91	LID_OPEN#	I	LID Switch	Cover switch, logic low means LCD cover closed
23	P92	POWERBTN#	I	Power Button	System power button
22	P93	H8_THRM#	O	SiS630ST	To SiS630ST, regustang the system power management mode
19	P94	VDD5_SW	O	LP-2951	To Switch VDD5 power source
18	P95	H8_PWROK	I	Vcore Power_Good	Detect Vcore Power_Good
17	P96	H8_GA20	I	SiS630ST	For A20M
16	P97	BAT_DATA	I/O	BAT_H8	SM_BUS data for smart battery
6	MD0	H8_MODE0	I	Pull_Up	H8 mode sSelect
5	MD1	H8_MODE1	I	Pull_Up	H8 mode select
91	PB0	LED_CLK	O	74VHC164	For LED indicate
90	PB1	LED_DATA	O	74VHC164	For LED indicate (Bit 0-7: -SCROLL, -NUM, -CAP, -AC POWER, -BATT POWER, -BATT_R, -BATT_G)
81	PB2	SIS_PWROK	O	SiS630ST & CPU	System Power_Good
80	PB3	VGATE#	I	SiS630ST	For speedstep function to gate VR_POWR_GOOD
69	PB4	CHARGING	O	Charge Circuitry	Indicated charge circuitry to work
68	PB5	D/VADJ_2	O	D/D Connector	Adjust charge battery voltage level
58	PB6	D/VADJ_1	O	D/D Connector	Adjust charge battery voltage level
57	PB7	H8/T_DATA	I/O	Touch Pad	Connect to touch pad data
48	PA0	TP32			No use
47	PA1	BATT_ALARM#	O	D/D Connector	Indicated the battery capacity is not enough to power on system
31	PA2	H8_PME#	I	LAN/Card Bus	If system on suspend mode, then output this signal to wake up system
30	PA3	H8_ADEN#	I	D/D Connector	Adaptor in
21	PA4	FAN_SPD	I	FAN	Return FAN0, FAN1 (CPU Core D/D FAN) speed
20	PA5	H8_PCIRST#	I	PCIRST#	For speedstep function to OR gate VGATE (H8 PB3) for SIS_PWROK (H8 P95)
11	PA6	RI#	I	LAN/Card Bus	If system on suspend mode, then received this signal & system have to wake up
10	PA7	H8/T_CLK	I/O	Touch Pad	Connect to touch pad clock
8	STBY	H8_STBY#	I	Pull_Up	No use
7	/NMI	SUSB#	I	SiS630ST	STR indicator
1	/RES	H8_RESET	I	MAX809	Reset H8-F3437

2. System View and Disassembly

2.1 System View

2.1.1 Front View

❶ Volume Control
❷ Microphone Connector
❸ Audio Output Connector
❹ Mail-Received
❺ Battery Indicator
❻ Power Indicator
❼ Cover Latch

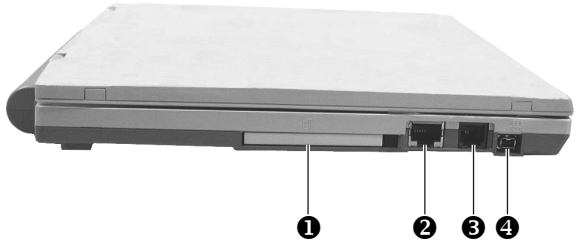


2.1.2 Rear View

❶ VGA Port
❷ Kensington Lock

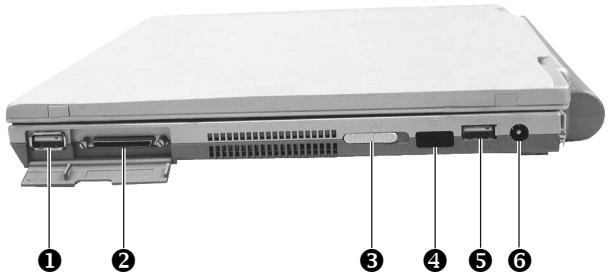
2.1.3 Left Side View

❶ PC Card Slot
❷ RJ-11 Connector
❸ RJ-45 Connector
❹ IEEE1394 Connector



2.1.4 Right Side View

❶ USB Port
❷ CD/DVD-ROM Drive Port
❸ Power Switch
❹ IR Port
❺ USB Port
❻ Power Connector



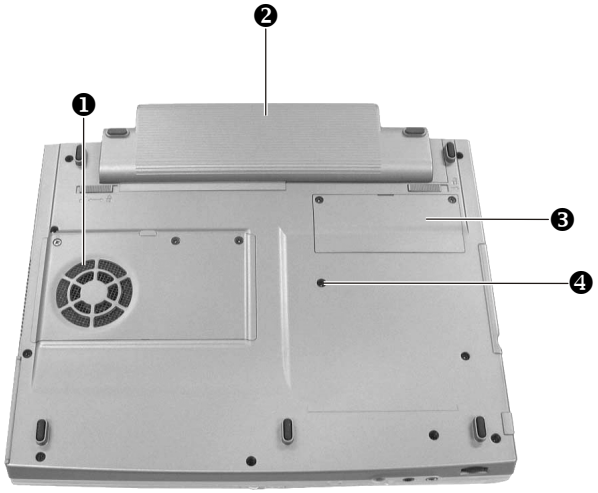
2.1.5 Button View

❶ CPU Cover

❷ Battery Pack

❸ SO-DIMM Cover

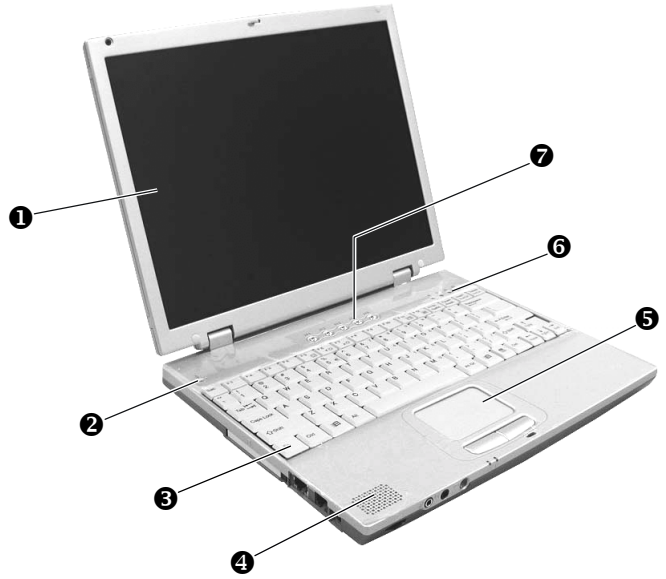
❹ Reset Switch



2.1.6 Top-Open View

To open the cover, press the cover latch toward the right and lift the cover.

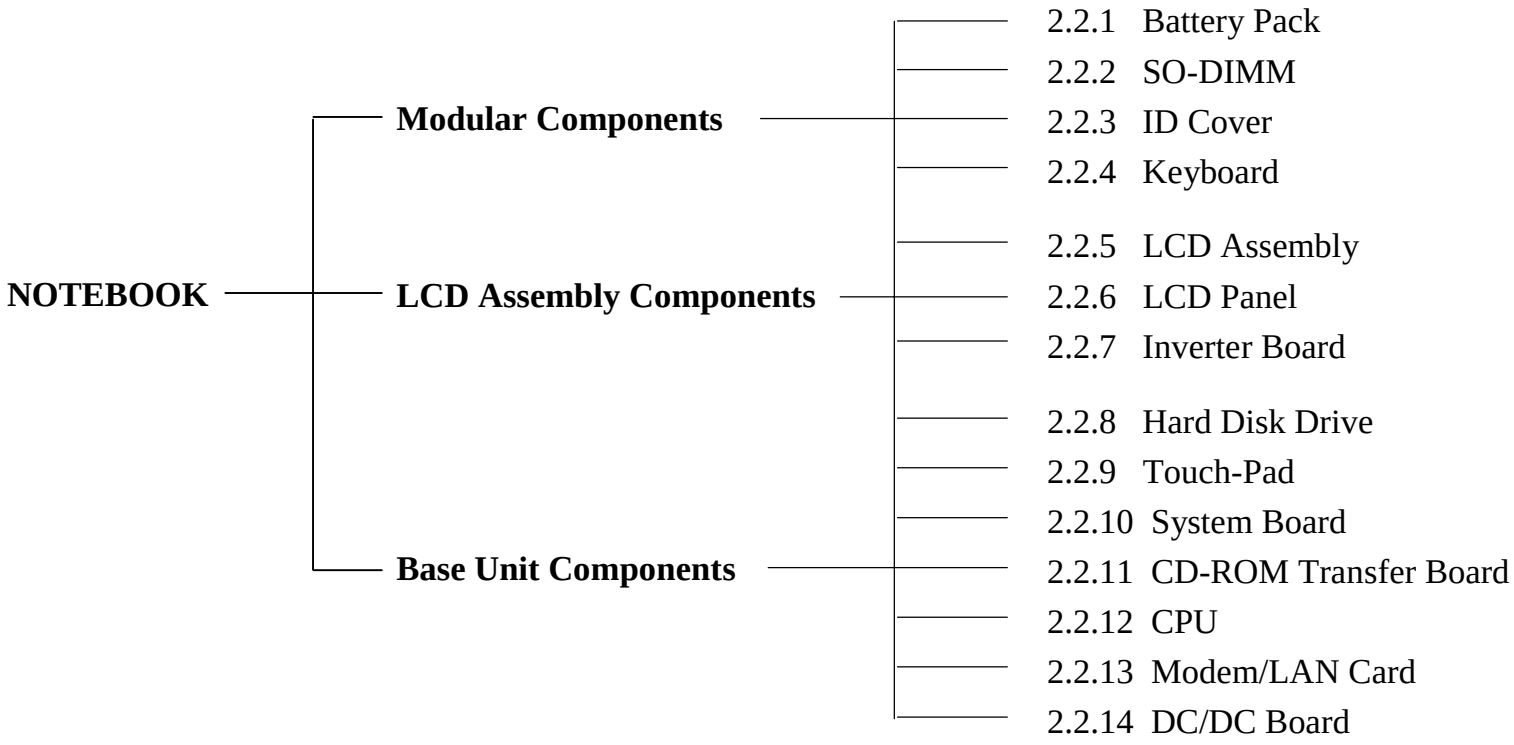
❶ LCD Display
❷ Microphone
❸ Keyboard
❹ Stereo Speaker
❺ Touch-pad
❻ Indicators Panel
❼ Easy Start Buttons



2.2 System Disassembly

This part discusses at length each major component for disassembly/reassembly and show corresponding illustrations. Use the chart below to determine the disassembly sequence for removing components from the notebook.

NOTE : *Before you start to install/replace these modules, disconnect all peripheral devices and make sure the notebook is not turned on or connected to AC power.*



2.2.1 Battery Pack

Disassembly

1. Carefully put the notebook upside down.
2. Slide the right battery lock level outward to the “unlock” ( ) position. (See Figure 2-1)
3. Slide the left battery release level outward to the “unlock” ( ) position and hold it in the unlock position, and then you can remove the battery pack out of its compartment. (See Figure 2-1)

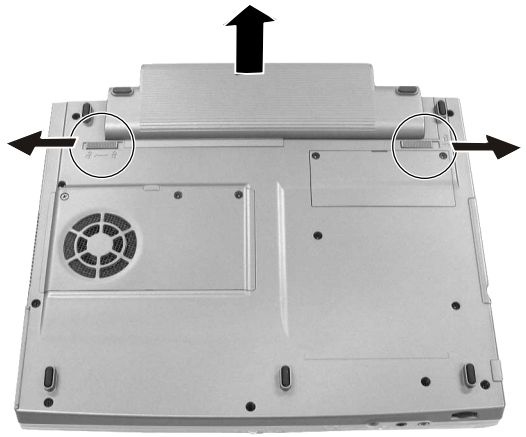


Figure 2-1 Remove the battery Pack

Reassembly

1. Fit the new battery pack into the compartment. The battery release level should click into the locked place.
2. Slide the battery lock inward to the “lock” ( ) position to secure the battery pack in place.

2.2.2 SO-DIMM

Disassembly

1. Carefully put the notebook upside down.
2. Remove the battery pack. (See section 2.2.1 disassembly)
3. Remove two screws to lift the SO-DIMM compartment cover. (See Figure 2-2)

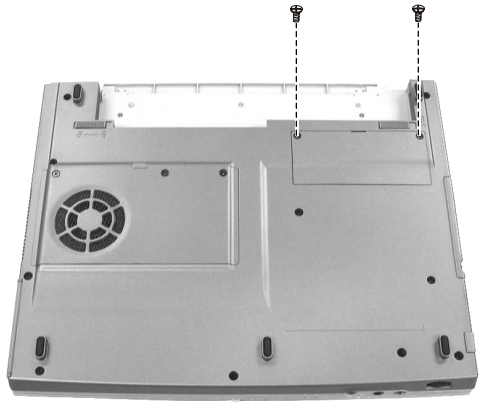


Figure 2-2 Remove the SO-DIMM compartment cover

4. Pull the retaining clips outwards (❶) and remove the SO-DIMM (❷). (See Figure 2-3)

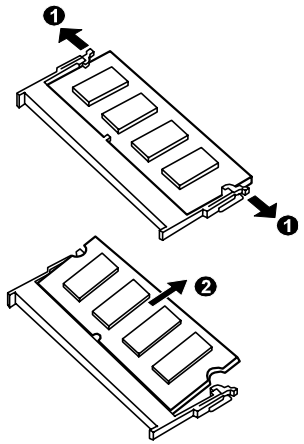


Figure 2-3 Remove the SO-DIMM

Reassembly

1. To install the SO-DIMM, match the SO-DIMM's notched part with the socket's projected part and firmly insert the SO-DIMM into the socket at 20-degree angle. Then push down until the retaining clips lock the SO-DIMM into position.
2. Replace the compartment cover and secure with two screws.
3. Fit the battery pack. (See 2.2.1 reassembly)

2.2.3 ID Cover

Disassembly

1. Remove the battery pack. (See section 2.2.1disassembly)
2. Remove thirteen button screws as shown below. (See Figure 2-4)

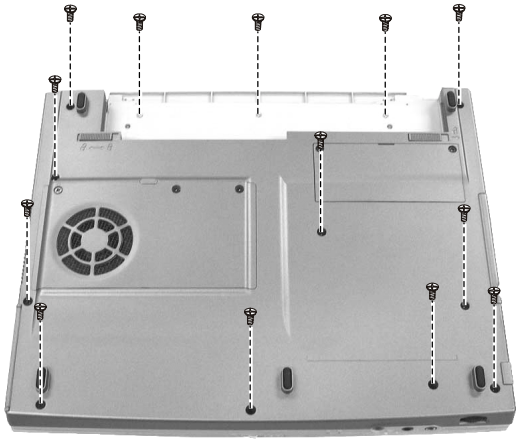


Figure 2-4 Remove screws to loosen the ID Cover

NOTE : *You don't have to remove five other screws that can be found on the bottom.*

3. Put the notebook back to the upright position. Open the top cover and tilt it backward until it lies flat. To detach the ID cover, first slightly lift the upper edge (❶) and then slide it toward the first. (❷) (See Figure 2-5)

Figure 2-5 Slide the ID cover

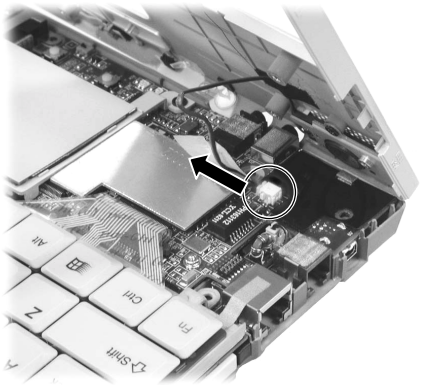


Figure 2-6 Free the ID cover by remove one cable

4. Disconnect the speaker cable from the system board. Now you can separate the ID cover. (See Figure 2-6)

Reassembly

1. Plug the keyboard cable and fit the keyboard back into place.
2. Reconnect the speaker cable, then replace the ID cover and secure with all bottom screws.
3. Replace the battery pack. (See 2.2.1 reassembly)

2.2.4 Keyboard

Disassembly

1. Remove the battery pack. (See section 2.2.1disassembly)
2. Remove the ID cover. (See section 2.2.3 disassembly)
3. Put the notebook upside down. Remove the SO-DIMM compartment cover and then two screws that secure the keyboard (one is in the compartment, the other one is in the central position of the bottom). (See Figure 2-7)

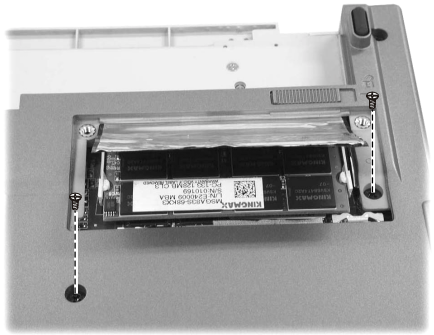


Figure 2-7 Remove two screws

4. Put the notebook back to the upright position. Lift up the keyboard and disconnect the cable to free it from the system board.

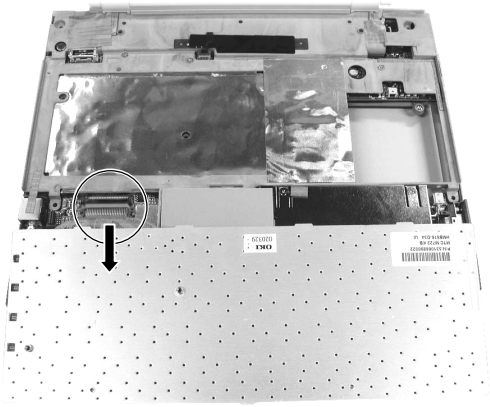


Figure 2-8 Disconnect the cable to remove the keyboard

Reassembly

1. Plug the keyboard cable and fit the keyboard back into place and secure with two screws.
2. Reconnect the speaker cable.
3. Then replace the ID cover and secure with all bottom screws. (See section 2.2.3 reassembly)
3. Replace the battery pack. (See section 2.2.1 reassembly)

2.2.5 LCD Assembly

Disassembly

1. Remove the battery pack. (See section 2.2.1 disassembly)
2. Remove the ID cover. (See section 2.2.3 disassembly)
3. Remove the hinges cover by inserting a flat screwdriver to the rear of the cover and pry the cover out. (See Figure2-9)

Figure 2-9 Remove the hinge covers

4. Open the top cover. Unplug the two cable connectors coming from the LCD assembly, and remove four screws from the hinges. Now you can separate the LCD assembly from the base unit. (See Figure2-10)

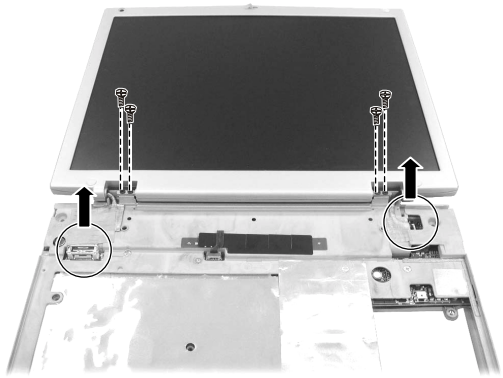


Figure 2-10 Remove the LCD module

Reassembly

1. Attach the LCD assembly to the base unit and secure with four screws on the hinges.
2. Reconnect the LCD cable connectors to system board..
3. Replace the two hinge covers.
4. Reconnect the speaker cable, then replace the ID cover and secure with all bottom screws. (See section 2.2.1 reassembly)
5. Replace the battery pack. (See section 2.2.1 reassembly)

2.2.6 LCD Panel

Disassembly

1. Remove the LCD assembly from the base unit. (See section 2.2.5 disassembly)
2. Remove the four rubber pads and the four screws underneath. Then you can separate the LCD frame from the housing. (See Figure 2-11)

Figure 2-11 Remove the LCD frame

Figure 2-12 Remove the inverter board to free the panel

4.. Remove the four screws on two sides of the LCD panel, and disconnect the cable from the inverter board. Then take out the LCD panel.(See Figure 2-12)

Reassembly

1. Reconnect the cable to the inverter board, then fit the LCD back into place and secure with four screws.
2. Fit the LCD frame back to the housing and secure with four screws and rubbers.
3. Replace the LCD assembly. (See section 2.2.5 reassembly)

2.2.7 Inverter Board

Disassembly

1. Detach the LCD frame. (See steps 1 to 2 in section 2.2.6 disassembly.)
2. To take out the inverter board at the bottom side of the LCD, remover one screw and unplug the cable connected to the LCD panel. (See Figure 2-13)

Figure 2-13 Remove the inverter board

Reassembly

1. Reconnect the cable, then fit the inverter board back into place and secure with one screw.
2. Fit the LCD frame back to the housing and secure with four screws.
3. Replace the LCD assembly. (See section 2.2.5 reassembly)

2.2.8 Hard Driver

Disassembly

1. Remove the battery pack. (See section 2.2.1 disassembly)
2. Remove the ID cover. (See section 2.2.3 disassembly)
3. Lift up the touch-pad board, the remove the screw at the upper right corner of the touchpad holder.(See Figure 2-14)

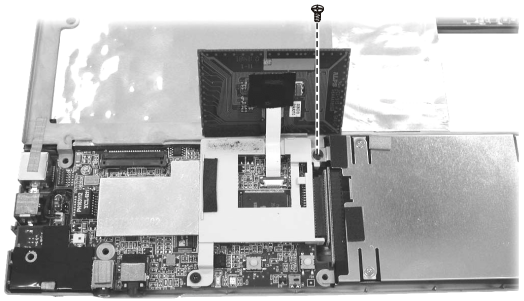


Figure 2-14 Remove one screw

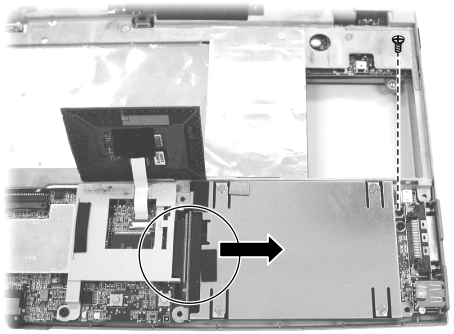


Figure 2-15 Slack the Hard driver

4. Remove the screw at the upper right corner of the hard disk, then slide the hard disk drive outward to unplug the connector and take out the hard disk drive. (See Figure 2-15)

5. Remove four screws to separate the hard disk drive form the metal shield. (See Figure 2-16)

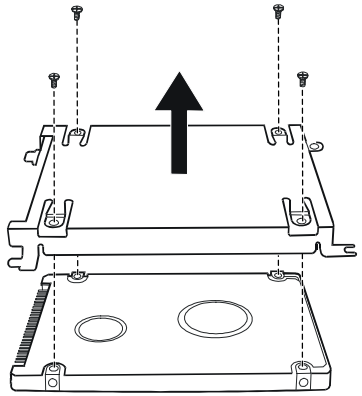


Figure 2-16 Free the Hard driver

Reassembly

1. Attach the metal shield to the hard disk drive and secure with four screws.
2. Fit the hard disk drive into place, connect to the system board, and secure with one screw at the upper right corner.
3. Secure the screw at the upper right corner of the touch-pad holder, then fit the touch-pad board into place and secure with double-stick tape.
4. Reconnect the speaker cable, then replace the ID cover and secure with all bottom screws.
   (See section 2.2.3 reassembly)
5. Replace the battery pack. (See section 2.2.1 reassembly)

2.2.9 Touch-pad

Disassembly

1. Remove the battery pack. (See section 2.2.1 disassembly)
2. Remove the ID cover. (See section 2.2.3 disassembly)
3. Lift up the touch-pad board, and disconnect the cable from the system board. (See Figure 2-17)
4. If you need to remove the touch-pad holder, remove two screws. (See Figure 2-17)

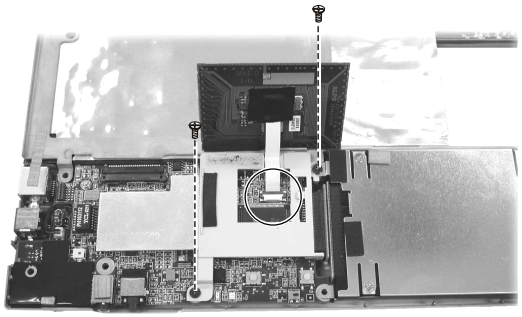


Figure 2-17 Remove the touch-pad and holder

Reassembly

1. Replace the touch-pad holder and secure with two screws.
2. Connect the cable of touch-pad board to the system board, and fit the touch-pad board into place and secure with double-stick tape.
3. Reconnect the speaker cable, then replace the ID cover and secure with all bottom screws.
   (See section 2.2.3 reassembly)
4. Replace the battery pack. (See section 2.2.1 reassembly)

2.2.10 System Board

Disassembly

1. Remove the battery pack. (See section 2.2.1 disassembly)
2. Remove the ID cover. (See section 2.2.3 disassembly)
3. Remove the keyboard. (See section 2.2.4 disassembly)
4. Remove the LCD assembly. (See section 2.2.5 disassembly)
5. Remove the hard disk drive. (See section 2.2.8 disassembly)
6. Remove the touch-pad. (See section 2.2.9 disassembly)
7. Remove three screws fastening the system board and one screw locking the CD-ROM transfer board. (See Figure 2-18)

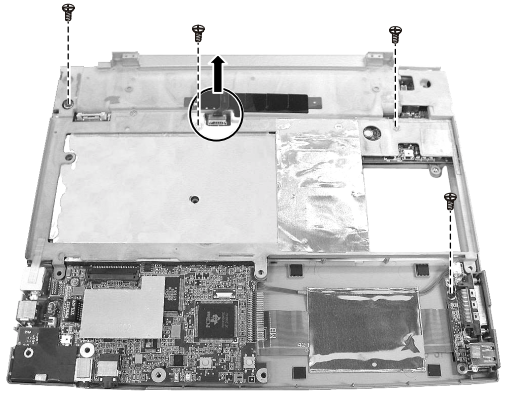


Figure 2-18 Remove system board

8. Unplug one cable from the system board. Then lift the system board free.

Reassembly

1. Fit the system board and CD-ROM transfer board into place and secure with four screws.
2. Replace the touch-pad and the hard disk drive.
3. Attach the LCD assembly to the base unit and secure with four screws and reconnect two cables. Replace the two hinge covers.
4. Plug the keyboard cable and fit the keyboard back into place.
5. Reconnect the speaker cable, then replace the ID cover and secure with all bottom screws.
   (See section 2.2.3 reassembly)
6. Replace the battery pack. (See section 2.2.1 reassembly)

2.2.11 CD-ROM Transfer Board

Disassembly

1. Remove the battery pack, ID cover, keyboard, LCD assembly, hard disk drive. (See section 2.2.1; 2.2.3; 2.2.4; 2.2.5; and 2.2.8 disassembly)
2. Remove one screw fastening the CD-ROM transfer board. (See Figure 2-19)
3. Put the system board upside down.
4. Unplug the two cables from the system board. (See Figure 2-20)

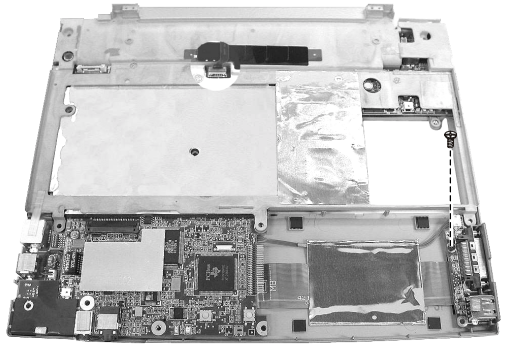


Figure 2-19 Remove the transfer board

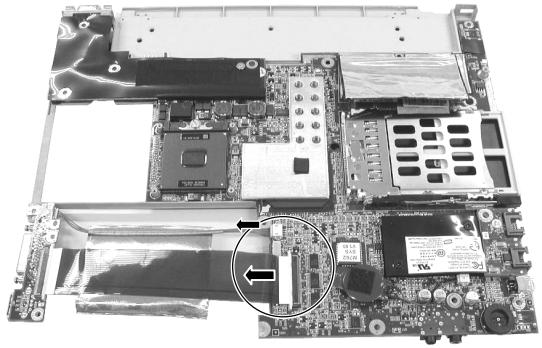


Figure 2-20 Remove the transfer board

Reassembly

1. Reconnect the cables to the system board, then fit the system board and CD-ROM transfer board into place and secure four screws.
2. Replace Replace the hard disk drive, LCD assembly, keyboard, ID cover, battery pack. (See section 2.2.8; 2.2.5; 2.2.4; 2.2.3; 2.2.1 reassembly.)

2.2.12 CPU

Disassembly

1. Remove the battery pack. (See section 2.2.1 disassembly)
2. Put the system board upside down. Remove three screws fastening the CUP cover. (See Figure 2-21)
3. Remove four screws that fastening the heatsink with the spring holder. (See Figure 2-22)

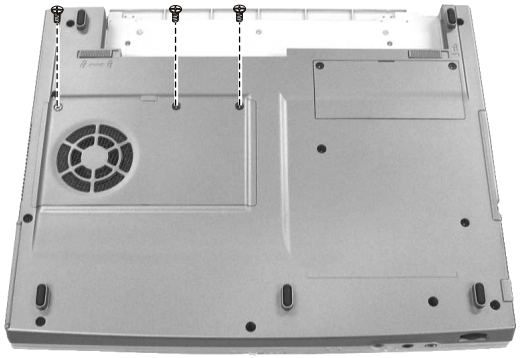


Figure 2-21 Remove the CUP cover

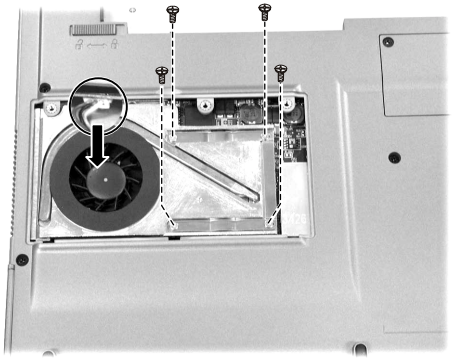


Figure 2-22 Remove the CPU heatsink

4. Unplug the fan assembly's power cord to free the heatsink from the CPU module. (See Figure 2-22)

5. Loosen the screw by a flat screwdriver, upraise the CPU socket to unlock the CPU. (See Figure 2-23)

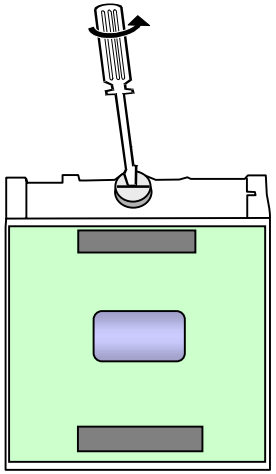


Figure 2-23 Remove the CPU from socket

Reassembly

1. Connect the power cord of the fan assembly to the system board, and fit the heatsink onto the top of the CPU.
2. Fit the spring holder to the heatsink and secure with four screws
3. Replace the battery pack. (See section 2.2.1 reassembly)

NOTE : *When you remove the CPU heatsink, make sure the thermal pad is not damaged. If it is damaged, you have to replace the thermal pad with a new one.*

2.2.13 Modem / LAN Card

Disassembly

1. Remove the battery pack, ID cover, keyboard, LCD assembly, hard disk drive. (See section 2.2.1; 2.2.3; 2.2.4; 2.2.5; and 2.2.8 disassembly)
2. Remove the system board from the base. (See section 2.2.10 disassembly)
3. Put the system board upside down.
4. Remove two screws to lift the Modem/LAN card. (See Figure 2-24 disassembly)

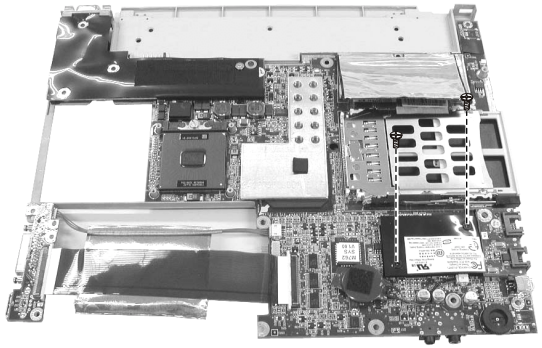


Figure 2-24 Remove the Modem/LAN card

Reassembly

1. Insert the connector of the Modem/LAN card into the headers on the system board, and secure it with two screws.
2. Replace Replace the hard disk drive, LCD assembly, keyboard, ID cover, battery pack. (See section 2.2.8; 2.2.5; 2.2.4; 2.2.3; 2.2.1 reassembly.)

2.2.14 DC/DC Board

Disassembly

1. Remove the battery pack, ID cover, keyboard, LCD assembly, hard disk drive. (See section 2.2.1; 2.2.3; 2.2.4; 2.2.5; and 2.2.8 disassembly)
2. Put the system board upside down.
3. Remove one screw on the board, and two hexnut screws fastening the VGA port. (See Figure 2-24 disassembly)
4. Lift the DC/DC board. (See Figure 2-25)

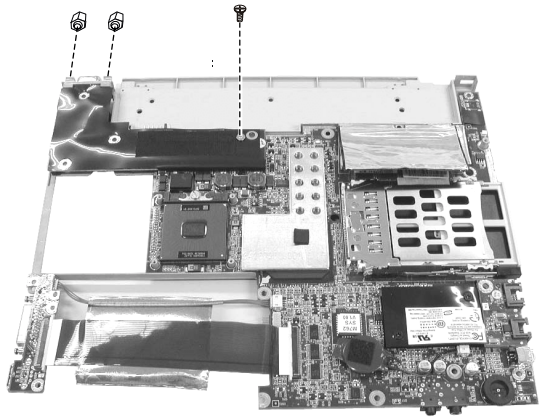


Figure 2-25 Remove the DC/DC board

Reassembly

1. Insert the connector of the DC/DC board into the headers on the system board, and secure it with three screws.
2. Replace Replace the hard disk drive, LCD assembly, keyboard, ID cover, battery pack. (See section 2.2.8; 2.2.5; 2.2.4; 2.2.3; 2.2.1 reassembly.)

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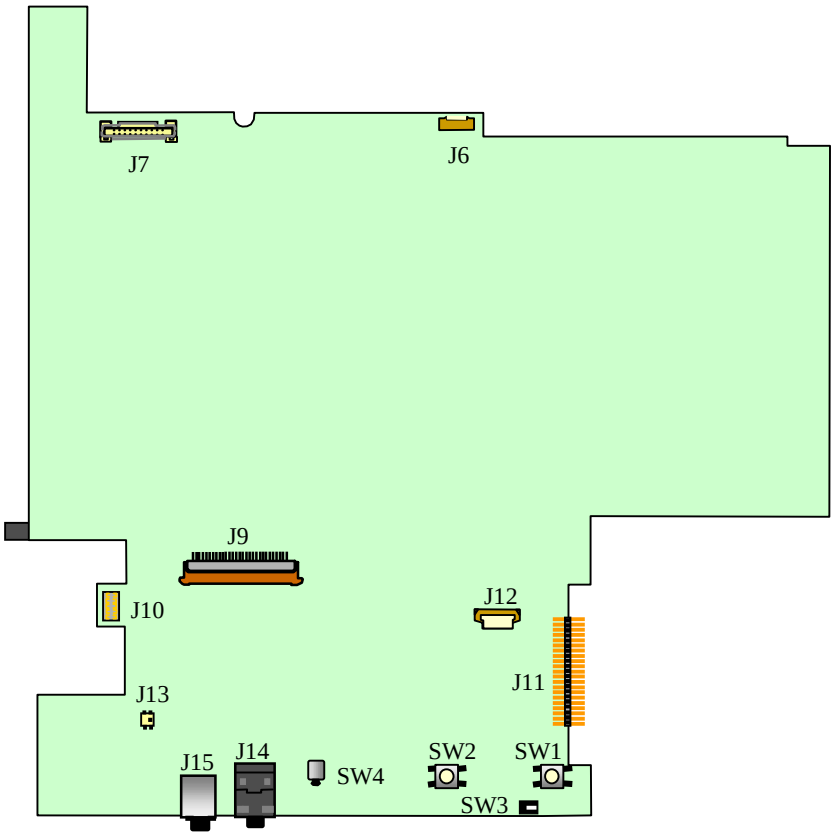
3. Definition & Location of Connectors / Switches

3.1 Mother Board - A



- **J6 : Quick Key Transfer Board Connector**
- **J7 : LCD panel connector**
- **J9 : Internal Keyboard Connector**
- **J10 : LAN Connector**
- **J11 : Hard Disk Drive Connector**
- **J12 : Touch-pad Module Connector**
- **J13 : Internal Speaker Connector**
- **J14 : Line Out Phone Jack**
- **J15 : External Micro Phone Jack**

- **SW1 : Right Button Switch of Touch-pad**
- **SW2 : Left Button Switch of Touch-pad**
- **SW3 : Cover Suspend Switch**
- **SW4 : E-Mail Button**

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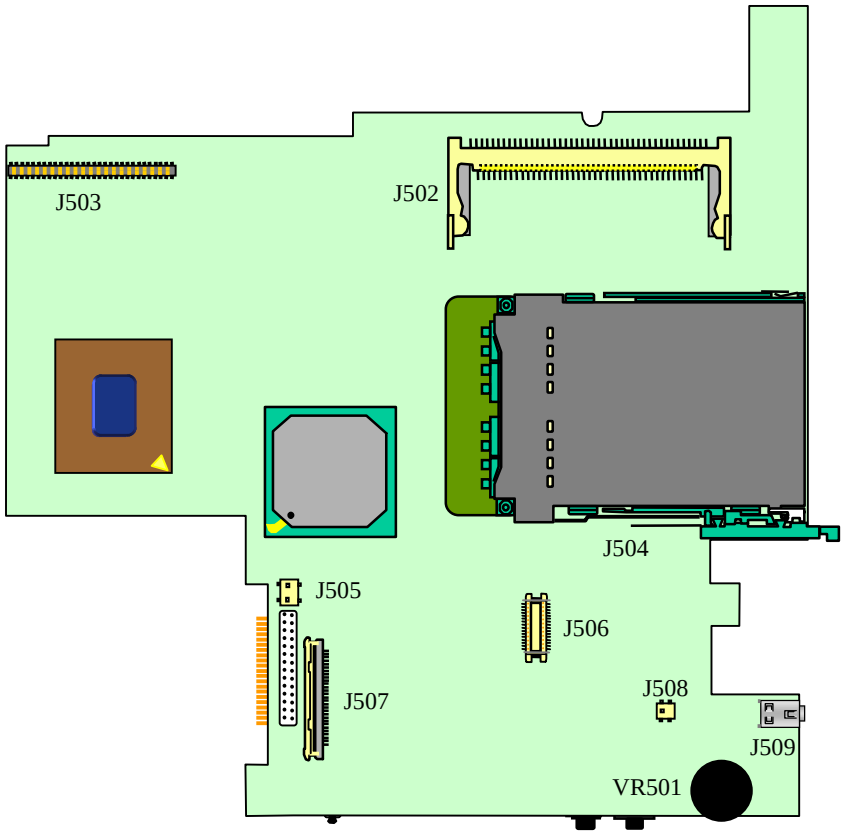
3. Definition & Location of Connectors / Switches

3.1 Mother Board - B



- **J502 : 144 pin SODIMM Slot**
- **J503 : D/D Board Connector.**
- **J504 : PCMCIA Card Slot**
- **J505 : USB Connector**
- **J506 : MDC/LAN Transfer Board Connector**
- **J507 : CD-ROM Transfer Board Connector**
- **J508 : CMOS Battery Connector**
- **J509 : IEEE1394 Connector**

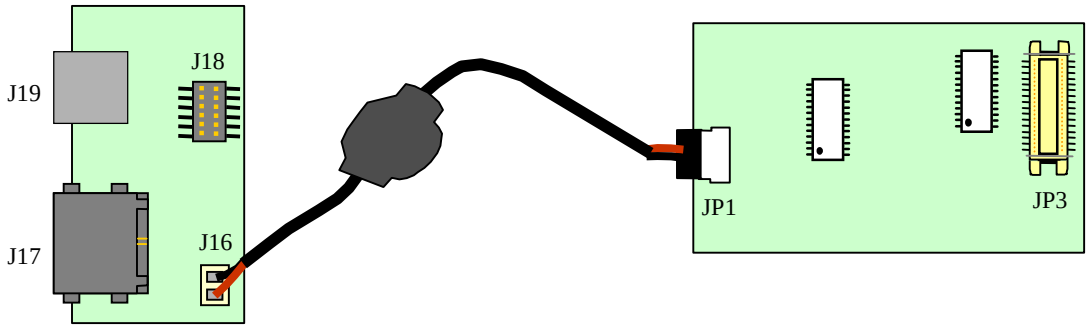
- **VR501: Volume Control**

3. Definition & Location of Connectors / Switches

3.2 Daughter Board

- **J16: MDC Jump Wire Connector**
- **J17 : RJ-11 Phone Jack for Internal Modem**
- **J18 : MDC/LAN Transfer Board to M/B Connector 1**
- **J19 : RJ45 Connector**
- **JP1 : MDC Jump Wire Connector**
- **JP3 : MDC/LAN Transfer Board to M/B Connector 2**

MDC/LAN Transfer Board



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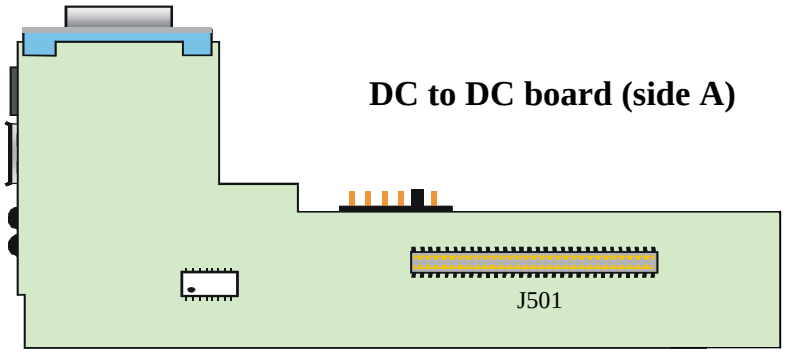
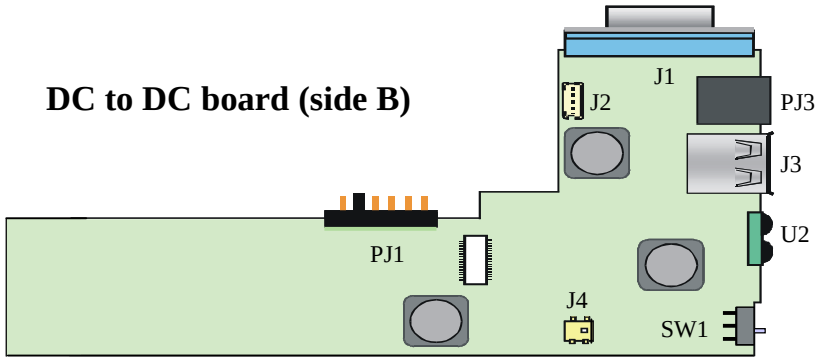
3. Definition & Location of Connectors / Switches

3.3 Charger Board





- **J501 : D/D Board Connector**
- **J1 : External VGA Connector**
- **J2 : Inverter Board Connector**
- **J3 : USB Port**
- **J4 : FAN Connector**
- **PJ1 : Battery Connector**
- **PJ3 : Power Jack (AC adapter)**
- **U2 : HSDL-3600 FIR Module**
- **SW1 : System Power on/off Switch**

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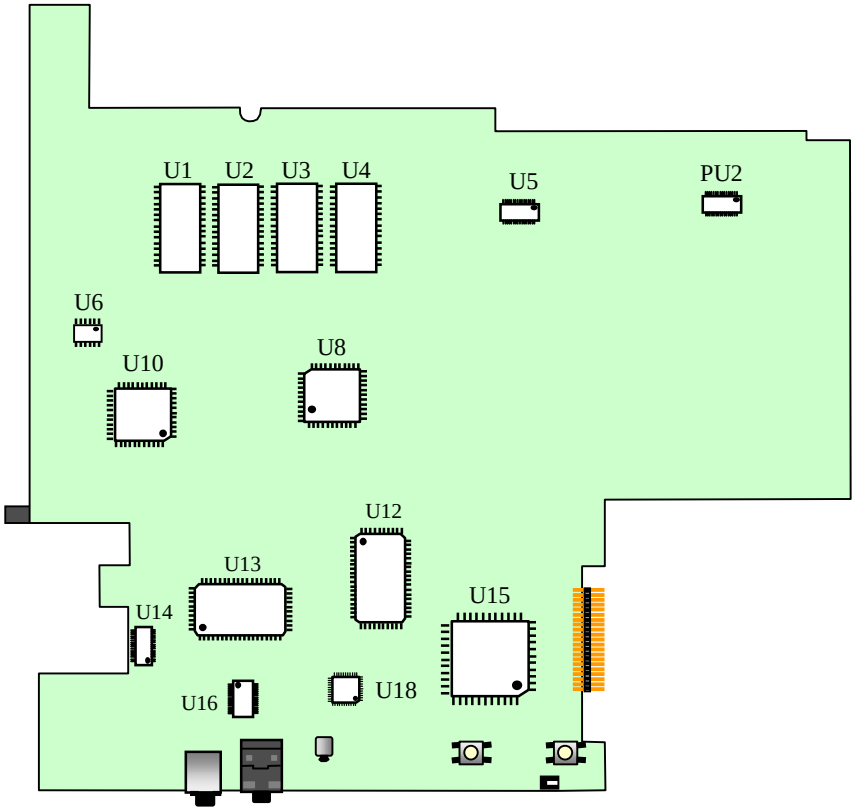
4. Definition & Location of Major Components

4.1 Mother Board - A



- U1~U4 : On board SDRAM_2M*16*4
- U5 : DS90C363MTD VGA LVD controller
- U6 : 74CBTD3384 Level Shift
- U8 : PC87393 Super I/O
- U10 : H8/F3437 KBD Controller
- U12 : SiS900 LAN Controller
- U13 : FW323 IEEE 1394 Controller
- U14 : PH163112 LAN Buffer
- U15 : PCI1410 PCMCIA Controller
- U16 : TA0202 Audio Amplifier
- U18 : ALC201 Audio Codec
- PU2 : CPU Core Voltage Generator

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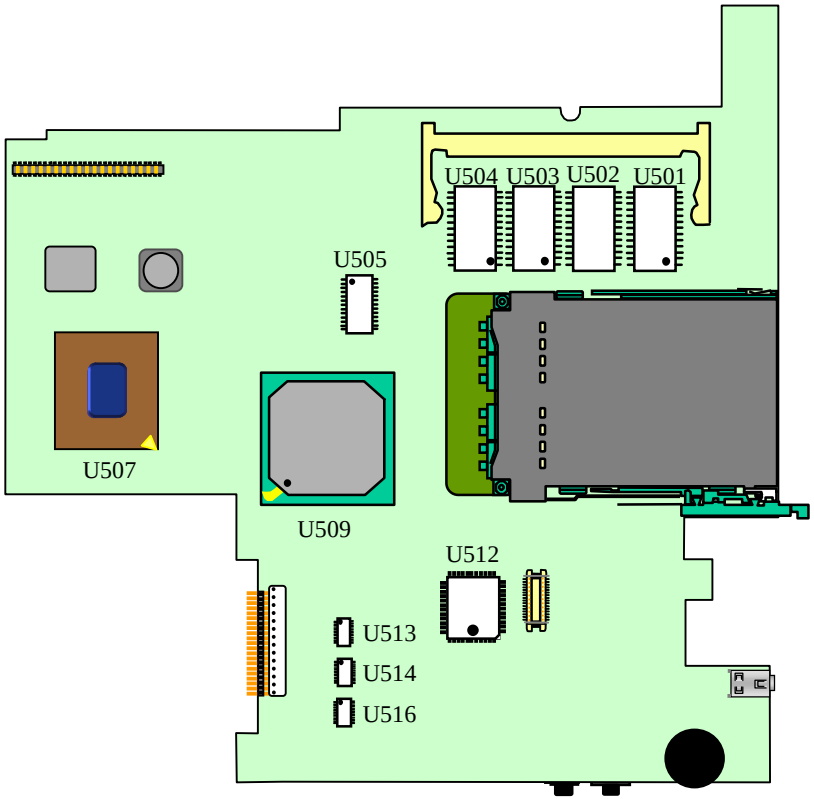
4. Definition & Location of Major Components

4.1 Mother Board - B



- **U50~U504 : On board SDRAM_2M*16*4**
- **U505 : ICS950104 clock generator**
- **U507 : Intel Mobile PIII/Celeron/Tualatin CPU**
- **U509 : SiS630ST single chipset**
- **U512 : System BIOS**
- **U513, U514, U516 : 74CBTD3384**

5. Pin Descriptions of Major Components

5.1 Intel Mobile Pentium III-M uFC-PGA478 Processor

Alphabetical Signal Reference

Signal Name	I/O	Signal Description
BPRI#	I GTL+	The BPRI# (Bus Priority Request) signal is used to arbitrate for ownership of the system bus. It must be connected to the appropriate pins/balls on both agents on the system bus. Observing BPRI# active (as asserted by the priority agent) causes the processor to stop issuing new requests, unless such requests are part of an ongoing locked operation. The priority agent keeps BPRI# asserted until all of its requests are completed and then releases the bus by deasserting BPRI#.
BREQ0#	I/O GTL+	The BREQ0# (Bus Request) signal is a processor Arbitration Bus signal. The processor indicates that it wants ownership of the system bus by asserting the BREQ0# signal. During power-up configuration, the central agent must assert the BREQ0# bus signal. The processor samples BREQ0# on the active-to-inactive transition of RESET#.
BSEL[1:0]	I 1.5V Tolerant	The BSEL[1:0] (Select Processor System Bus Speed) signal is used to configure the processor for the system bus frequency. The following talbe shows the encoding scheme for BSEL[1:0]. The only supported system bus frequency for the mobile Pentium III-M processor is 133 MHz. If another frequency is used or if the BSEL[1:0] signals are not driven with "1" then the processor is not guaranteed to function properly. **BSEL[1:0] Encoding** **BSEL[1:0]** — **System Bus Frequency** 01 — 100 MHz 11 — 133 MHz
CLKREF	Analog	The CLKREF (System Bus Clock Reference) signal provides a reference voltage to define the trip point for the BCLK signal. This signal should be connected to a resistor divider to generate 1.25V from the 2.5-V supply.
CMOSREF	Analog	The CMOSREF (CMOS Reference Voltage) signal provides a DC level reference voltage for the CMOS input buffers. A voltage divider should be used to divide a stable voltage plane (e.g., 2.5V or 3.3V). This signal must be provided with a DC voltage that meets the VCMOSREF specification from Table 13.
D[63:0]#	I/O GTL+	The D[63:0]# (Data) signals are the data signals. These signals provide a 64-bit data path between both system bus agents, and must be connected to the appropriate pins/balls on both agents. The data driver asserts DRDY# to indicate a valid data transfer.

Signal Name	I/O	Signal Description
DBSY#	I/O- GTL+	The DBSY# (Data Bus Busy) signal is asserted by the agent responsible for driving data on the system bus to indicate that the data bus is in use. The data bus is released after DBSY# is deasserted. This signal must be connected to the appropriate pins/balls on both agents on the system bus.
DEFER#	I GTL+	The DEFER# (Defer) signal is asserted by an agent to indicate that the transaction cannot be guaranteed in-order completion. Assertion of DEFER# is normally the responsibility of the addressed memory agent or I/O agent. This signal must be connected to the appropriate pins/balls on both agents on the system bus.
DEP[7:0]#	I/O GTL+	The DEP[7:0]# (Data Bus ECC Protection) signals provide optional ECC protection for the data bus. They are driven by the agent responsible for driving D[63:0]#, and must be connected to the appropriate pins/balls on both agents on the system bus if they are used. During power-on configuration, DEP[7:0]# signals can be enabled for ECC checking or disabled for no checking.
DRDY#	I/O GTL+	The DRDY# (Data Ready) signal is asserted by the data driver on each data transfer, indicating valid data on the data bus. In a multi-cycle data transfer, DRDY# can be deasserted to insert idle clocks. This signal must be connected to the appropriate pins/balls on both agents on the system bus.
EDGCTRLP	Analog	The EDGCTRLP (Edge Rate Control) signal is used to configure the edge rate of the GTL+ output buffers. Connect the signal to VSS with a 110-Ω, 1% resistor.
FERR#	O 1.5V Tolerant Open- drain)	The FERR# (Floating-point Error) signal is asserted when the processor detects an unmasked floating-point error. FERR# is similar to the ERROR# signal on the Intel 387 coprocessor, and it is included for compatibility with systems using DOS-type floating-point error reporting.
FLUSH#	I 1.5V Tolerant	When the FLUSH# (Flush) input signal is asserted, the processor writes back all internal cache lines in the Modified state and invalidates all internal cache lines. At the completion of a flush operation, the processor issues a Flush Acknowledge transaction. The processor stops caching any new data while the FLUSH# signal remains asserted. On the active-to-inactive transition of RESET#, each processor bus agent samples FLUSH# to determine its power-on configuration.

5.1 Intel Mobile Pentium III-M uFC-PGA478 Processor

Alphabetical Signal Reference

Signal Name	I/O	Signal Description
A[35:3]#	I/O GTL+	The A[35:3]# (Address) signals define a 2^{36}-byte physical memory address space. When ADS# is active, these signals transmit the address of a transaction; when ADS# is inactive, these signals transmit transaction information. These signals must be connected to the appropriate pins/balls of both agents on the system bus. The A[35:24]# signals are protected with the AP1# parity signal, and the A[23:3]# signals are protected with the AP0# parity signal. On the active-to-inactive transition of RESET#, each processor bus agent samples A[35:3]# signals to determine its power-on configuration. See Section 4 of this document and the *PentiumII Processor Developer's Manual* for details.
A20M#	I 1.5V Tolerant	If the A20M# (Address-20 Mask) input signal is asserted, the processor masks physical address bit 20 (A20#) before looking up a line in any internal cache and before driving a read/write transaction on the bus. Asserting A20M# emulates the 8086 processor's address wrap-around at the 1-Mbyte boundary. Assertion of A20M# is only supported in Real mode.
ADS#	I/O GTL+	The ADS# (Address Strobe) signal is asserted to indicate the validity of a transaction address on the A[35:3]# signals. Both bus agents observe the ADS# activation to begin parity checking, protocol checking, address decode, internal snoop or deferred reply ID match operations associated with the new transaction. This signal must be connected to the appropriate pins/balls on both agents on the system bus.
AERR#	I/O GTL+	The AERR# (Address Parity Error) signal is observed and driven by both system bus agents, and if used, must be connected to the appropriate pins/balls of both agents on the system bus. AERR# observation is optionally enabled during power-on configuration; if enabled, a valid assertion of AERR# aborts the current transaction. If AERR# observation is disabled during power-on configuration, a central agent may handle an assertion of AERR# as appropriate to the error handling architecture of the system.
AP[1:0]#	I/O GTL+	The AP[1:0]# (Address Parity) signals are driven by the request initiator along with ADS#, A[35:3]#, REQ[4:0]# and RP#. AP1# covers A[35:24]#. AP0# covers A[23:3]#. A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. This allows parity to be high when all the covered signals are high. AP[1:0]# should be connected to the appropriate pins/balls on both agents on the system bus.
BCLK	I 2.5V Tolerant	The BCLK (Bus Clock) signal determines the system bus frequency. Both system bus agents must receive this signal to drive their outputs and latch their inputs on the BCLK rising edge. All external timing parameters are specified with respect to the BCLK signal.

Signal Name	I/O	Signal Description
BERR#	I/O GTL+	The BERR# (Bus Error) signal is asserted to indicate an unrecoverable error without a bus protocol violation. It may be driven by either system bus agent and must be connected to the appropriate pins/balls of both agents, if used. However, the mobile Pentium III processors do not observe assertions of the BERR# signal. BERR# assertion conditions are defined by the system configuration. Configuration options enable the BERR# driver as follows: • Enabled or disabled • Asserted optionally for internal errors along with IERR# • Asserted optionally by the request initiator of a bus transaction after it observes an error • Asserted by any bus agent when it observes an error in a bus transaction
BINIT#	I/O-GTL+	The BINIT# (Bus Initialization) signal may be observed and driven by both system bus agents and must be connected to the appropriate pins/balls of both agents, if used. If the BINIT# driver is enabled during the power-on configuration, BINIT# is asserted to signal any bus condition that prevents reliable future information. If BINIT# is enabled during power-on configuration, and BINIT# is sampled asserted, all bus state machines are reset and any data which was in transit is lost. All agents reset their rotating ID for bus arbitration to the state after reset, and internal count information is lost. The L1 and L2 caches are not affected. If BINIT# is disabled during power-on configuration, a central agent may handle an assertion of BINIT# as appropriate to the Machine Check Architecture (MCA) of the system.
BNR#	I/O-GTL+	The BNR# (Block Next Request) signal is used to assert a bus stall by any bus agent that is unable to accept new bus transactions. During a bus stall, the current bus owner cannot issue any new transactions. Since multiple agents may need to request a bus stall simultaneously, BNR# is a wired-OR signal that must be connected to the appropriate pins/balls of both agents on the system bus. In order to avoid wire-OR glitches associated with simultaneous edge transitions driven by multiple drivers, BNR# is activated on specific clock edges and sampled on specific clock edges.
BP[3:2]#	I/O GTL+	The BP[3:2]# (Breakpoint) signals are the System Support group Breakpoint signals. They are outputs from the processor that indicate the status of breakpoints.
BPM[1:0]#	I/O GTL+	The BPM[1:0]# (Breakpoint Monitor) signals are breakpoint and performance monitor signals. They are outputs from the processor that indicate the status of breakpoints and programmable counters used for monitoring processor performance.

5.1 Intel Mobile Pentium III-M uFC-PGA478 Processor

Alphabetical Signal Reference

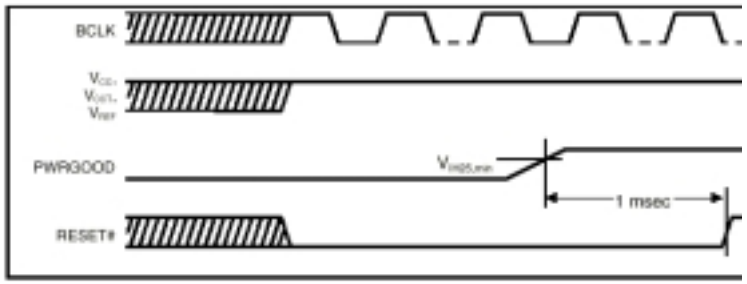
Signal Name	I/O	Signal Description
GHI#	I 1.5V Tolerant	The GHI# signal controls which operating mode bus ratio is selected in a mobile Pentium III processor featuring Intel SpeedStep technology. On the processor featuring Intel SpeedStep technology, this signal is latched when BCLK restarts in Deep Sleep state and determines which of two bus ratios is selected for operation. This signal is ignored when the processor is not in the Deep Sleep state. This signal is a "Don't Care" on processors that do not feature Intel SpeedStep technology. This signal has an on-die pull-up to VccT and should be driven with an Open-drain driver with no external pull-up.
HIT#, HITM#	I/O GTL+	The HIT# (Snoop Hit) and HITM# (Hit Modified) signals convey transaction snoop operation results, and must be connected to the appropriate pins/balls on both agents on the system bus. Either bus agent can assert both HIT# and HITM# together to indicate that it requires a snoop stall, which can be continued by reasserting HIT# and HITM# together.
IERR#	O 1.5V Tolerant Open-drain	The IERR# (Internal Error) signal is asserted by the processor as the result of an internal error.Assertion of IERR# is usually accompanied by a SHUTDOWN transaction on the system bus. This transaction may optionally be converted to an external error signal (e.g., NMI) by system logic. The processor will keep IERR# asserted until it is handled in software or with the assertion of RESET#, BINIT, or INIT#.
IGNNE#	I 1.5V Tolerant	The IGNNE# (Ignore Numeric Error) signal is asserted to force the processor to ignore a numeric error and continue to execute non-control floating-point instructions. If IGNNE# is deasserted, the processor freezes on a non-control floating-point instruction if a previous instruction caused an error. IGNNE# has no affect when the NE bit in control register 0 (CR0) is set.
INIT#	I 1.5V Tolerant	The INIT# (Initialization) signal is asserted to reset integer registers inside the processor without affecting the internal (L1 or L2) caches or the floating-point registers. The processor begins execution at the power-on reset vector configured during power-on configuration. The processor continues to handle snoop requests during INIT# assertion. INIT# is an asynchronous input. If INIT# is sampled active on RESET#'s active-to-inactive transition, then the processor executes its built-in self test (BIST).

Signal Name	I/O	Signal Description
INTR	I 1.5V Tolerant	The INTR (Interrupt) signal indicates that an external interrupt has been generated. INTR becomes the LINT0 signal when the APIC is enabled. The interrupt is maskable using the IF bit in the EFLAGS register. If the IF bit is set, the processor vectors to the interrupt handler after completing the current instruction execution. Upon recognizing the interrupt request, the processor issues a single Interrupt Acknowledge (INTA) bus transaction. INTR must remain active until the INTA bus transaction to guarantee its recognition.
LINT[1:0]	I 1.5V Tolerant	The LINT[1:0] (Local APIC Interrupt) signals must be connected to the appropriate pins/balls of all APIC bus agents, including the processor and the system logic or I/O APIC component. When APIC is disabled, the LINT0 signal becomes INTR, a maskable interrupt request signal, and LINT1 becomes NMI, a non-maskable interrupt. INTR and NMI are backward compatible with the same signals for the Pentium processor. Both signals are asynchronous inputs. Both of these signals must be software configured by programming the APIC register space to be used either as NMI/INTR or LINT[1:0] in the BIOS. If the APIC is enabled at reset, then LINT[1:0] is the default configuration.
LOCK#	I/O GTL+	The LOCK# (Lock) signal indicates to the system that a sequence of transactions must occur atomically. This signal must be connected to the appropriate pins/balls on both agents on the system bus. For a locked sequence of transactions, LOCK# is asserted from the beginning of the first transaction through the end of the last transaction. When the priority agent asserts BPRI# to arbitrate for bus ownership, it waits until it observes LOCK# deasserted. This enables the processor to retain bus ownership throughout the bus locked operation and guarantee the atomicity of lock.
NMI	I 1.5V Tolerant	The NMI (Non-Maskable Interrupt) indicates that an external interrupt has been generated. NMI becomes the LINT1 signal when the APIC is disabled. Asserting NMI causes an interrupt with an internally supplied vector value of 2. An external interrupt-acknowledge transaction is not generated. If NMI is asserted during the execution of an NMI service routine, it remains pending and is recognized after the IRET is executed by the NMI service routine. At most, one assertion of NMI is held pending. NMI is rising edge sensitive.

5.1 Intel Mobile Pentium III-M uFC-PGA478 Processor

Alphabetical Signal Reference

Signal Name	I/O	Signal Description
PICCLK	I 2.5V Tolerant	The PICCLK (APIC Clock) signal is an input clock to the processor and system logic or I/O APIC that is required for operation of the processor, system logic, and I/O APIC components on the APIC bus.
PICD[1:0]	I/O 1.5V Tolerant Open-drain	The PICD[1:0] (APIC Data) signals are used for bi-directional serial message passing on the APIC bus. They must be connected to the appropriate pins/balls of all APIC bus agents, including the processor and the system logic or I/O APIC components. If the PICD0 signal is sampled low on the active-to-inactive transition of the RESET# signal, then the APIC is hardware disabled.
PLL1, PLL2	Analog	The PLL1 and PLL2 signals provide isolated analog decoupling is required for the internal PLL.
PRDY#	O GTL+	The PRDY# (Probe Ready) signal is a processor output used by debug tools to determine processor debug readiness.
PREQ#	I 1.5V Tolerant	The PREQ# (Probe Request) signal is used by debug tools to request debug operation of the processor.
PWRGOOD	I 2.5V Tolerant	PWRGOOD (Power Good) is a 2.5-V tolerant input. The processor requires this signal to be a clean indication that clocks and the power supplies (Vcc, VccT, etc.) are stable and within their specifications. Clean implies that the signal will remain low, (capable of sinking leakage current) and without glitches, from the time that the power supplies are turned on, until they come within specification. The signal will then transition monotonically to a high (2.5V) state. Figure 26 illustrates the relationship of PWRGOOD to other system signals. PWRGOOD can be driven inactive at any time, but clocks and power must again be stable before the rising edge of PWRGOOD.



Signal Name	I/O	Signal Description
REQ[4:0]#	I/O GTL+	The REQ[4:0]# (Request Command) signals must be connected to the appropriate pins/balls on both agents on the system bus. They are asserted by the current bus owner when it drives A[35:3]# to define the currently active transaction type.
RESET#	I GTL+	Asserting the RESET# signal resets the processor to a known state and invalidates the L1 and L2 caches without writing back Modified (M state) lines. For a power-on type reset, RESET# must stay active for at least 1 msec after Vcc and BCLK have reached their proper DC and AC specifications and after PWRGOOD has been asserted. When observing active RESET#, all bus agents will deassert their outputs within two clocks. RESET# is the only GTL+ signal that does not have on-die GTL+ termination. A 56.2Ω 1% terminating resistor connected to VccT is required. A number of bus signals are sampled at the active-to-inactive transition of RESET# for the power-on configuration. Unless its outputs are tri-stated during power-on configuration, after an active-to-inactive transition of RESET#, the processor optionally executes its built-in self-test (BIST) and begins program execution at reset-vector 000FFFF0H or FFFFFFF0H. RESET# must be connected to the appropriate pins/balls on both agents on the system bus.
RP#	I/O GTL+	The RP# (Request Parity) signal is driven by the request initiator and provides parity protection on ADS# and REQ[4:0]#. RP# should be connected to the appropriate pins/balls on both agents on the system bus. A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. This definition allows parity to be high when all covered signals are high.
RS[2:0]#	I GTL+	The RS[2:0]# (Response Status) signals are driven by the response agent (the agent responsible for completion of the current transaction) and must be connected to the appropriate pins/balls on both agents on the system bus.

5.1 Intel Mobile Pentium III-M uFC-PGA478 Processor

PWRGOOD Relationship at Power On

Signal Name	I/O	Signal Description
RSP#	I GTL+	The RSP# (Response Parity) signal is driven by the response agent (the agent responsible for completion of the current transaction) during assertion of RS[2:0]#. RSP# provides parity protection for RS[2:0]#. RSP# should be connected to the appropriate pins/balls on both agents on the system bus. A correct parity signal is high if an even number of covered signals are low, and it is low if an odd number of covered signals are low. During Idle state of RS[2:0]# (RS[2:0]#=000), RSP# is also high since it is not driven by any agent guaranteeing correct parity.
RSVD	TBD	The RSVD (Reserved) signal is currently unimplemented but is reserved for future use. Leave this signal unconnected. Intel recommends that a routing channel for this signal be allocated.
RTTIMPEDP	Analog	The RTTIMPEDP (RTT Impedance/PMOS) signal is used to configure the on-die GTL+ termination. Connect the RTTIMPEDP signal to VSS with a 56.2-Ω, 1% resistor.
SLP#	I 1.5V Tolerant	The SLP# (Sleep) signal, when asserted in the Stop Grant state, causes the processor to enter the Sleep state. During the Sleep state, the processor stops providing internal clock signals to all units, leaving only the Phase-Locked Loop (PLL) still running. The processor will not recognize snoop and interrupts in the Sleep state. The processor will only recognize changes in the SLP#, STPCLK# and RESET# signals while in the Sleep state. If SLP# is deasserted, the processor exits Sleep state and returns to the Stop Grant state in which it restarts its internal clock to the bus and APIC processor units.
SMI#	I 1.5V Tolerant	The SMI# (System Management Interrupt) is asserted asynchronously by system logic. On accepting a System Management Interrupt, the processor saves the current state and enters System Management Mode (SMM). An SMI Acknowledge transaction is issued, and the processor begins program execution from the SMM handler.
STPCLK#	I 1.5V Tolerant	The STPCLK# (Stop Clock) signal, when asserted, causes the processor to enter a low-power Stop Grant state. The processor issues a Stop Grant Acknowledge special transaction and stops providing internal clock signals to all units except the bus and APIC units. The processor continues to snoop bus transactions and service interrupts while in the Stop Grant state. When STPCLK# is deasserted, the processor restarts its internal clock to all units and resumes execution. The assertion of STPCLK# has no affect on the bus clock.
TCK	I 1.5V Tolerant	The TCK (Test Clock) signal provides the clock input for the test bus (also known as the test access port).

Signal Name	I/O	Signal Description
TDI	I 1.5V Tolerant	The TDI (Test Data In) signal transfers serial test data to the processor. TDI provides the serial input needed for JTAG support.
TDO	O 1.5V Tolerant Open-drain	The TDO (Test Data Out) signal transfers serial test data from the processor. TDO provides the serial output needed for JTAG support.
TESTHI	I 1.5V Tolerant	The TESTHI (Test input High) is used during processor test and needs to be pulled high during normal operation.
TESTLO[2:1]	I 1.5V Tolerant	The TESTLO[2:1] (Test input Low) signals are used during processor test and needs to be pulled to ground during normal operation.
TESTP	Analog	The TESTP (Test Point) signals are connected to Vcc and Vss at opposite ends of the die. These signals can be used to monitor the Vcc level on the die. Route the TESTP signals to test points or leave them unconnected. Do not short the TESTP signals together.
THERMDA, THERMDC	Analog	The THERMDA (Thermal Diode Anode) and THERMDC (Thermal Diode Cathode) signals connect to the anode and cathode of the on-die thermal diode.
TMS	I 1.5V Tolerant	The TMS (Test Mode Select) signal is a JTAG support signal used by debug tools.
TRDY#	I GTL+	The TRDY# (Target Ready) signal is asserted by the target to indicate that the target is ready to receive write or implicit write-back data transfer. TRDY# must be connected to the appropriate pins/balls on both agents on the system bus.
TRST#	I 1.5V Tolerant	The TRST# (Test Reset) signal resets the Test Access Port (TAP) logic. The mobile Pentium III processors do not self-reset during power on; therefore, it is necessary to drive this signal low during power-on reset.

5.1 Intel Mobile Pentium III-M uFC-PGA478 Processor

PWRGOOD Relationship at Power On

Signal Name	I/O	Signal Description
VID[4:0]	O - Open-drain	The VID[4:0] (Voltage ID) pins/balls can be used to support automatic selection of power supply voltages. These pins/balls are not signals, they are either an open circuit or a short to VSS on the processor substrate. The combination of opens and shorts encodes the voltage required by the processor. External to pull-ups are required to sense the encoded VID. For processors that have Intel SpeedStep technology enabled, VID[4:0] encode the voltage required in the battery-optimized mode. VID[4:0] are needed to cleanly support voltage specification changes on mobile Pentium III processors. The voltage encoded by VID[4:0] is defined in Table 39. A "1" in this table refers to an open pin/ball and a "0" refers to a short to VSS. The power supply must provide the requested voltage or disable itself. Please note that in order to implement VID on the BGA2 package, some VID[4:0] balls may be depopulated. For the BGA2 package, a "1" in Table 39 implies that the corresponding VID ball is depopulated, while a "0" implies that the corresponding VID ball is not depopulated. But on the Micro-PGA2 package, VID[4:0] pins are not depopulated.

5.2 SiS630ST Slot1/Socket370 2D/3D Ultra AGP™ Single Chipset

Host Bus Interface

Name	Tolerance	Power Plane	Type Attr	Description
CPUCLK	3.3V/5V	MAIN	I	**Host Clock :**
ADS#	1.5V	MAIN	I/O GTL+	**Address Strobe :** Address Strobe is driven by CPU to indicate the start of a CPU bus cycle.
HREQ[4:0]#	1.5V	MAIN	I/O GTL+	**Request Command:** HREQ[4:0]# are used to define each transaction type during the clock when ADS# is asserted and the clock after ADS# is asserted.
BREQ0#	1.5V	MAIN	O GTL+	**Symmetric Agent Bus Request:** BREQ0# is driven by the symmetric agent to request for the bus.
BNR#	1.5V	MAIN	I/O GTL+	**Block Next Request:** This signal can be driven asserted by any bus agent to block further requests being pipelined.
HLOCK#	1.5V	MAIN	I GTL+	**Host Lock :** CPU asserts HLOCK# to indicate the current bus cycle is locked.
HIT#	1.5V	MAIN	I/O GTL+	**Keeping a Non-Modified Cache Line:**
HITM#	1.5V	MAIN	I/O GTL+	**Hits a Modified Cache Line:** Hit Modified indicates the snoop cycle hits a modified line in the L1 cache of CPU.
DEFER#	1.5V	MAIN	O GTL+	**Defer Transaction Completion:** SiS630 will use this signal to indicate a retry response to host bus**.**
RS[2:0]#	1.5V	MAIN	O GTL+	**Response Status:** RS[2:0]# are driven by the response agent to indicate the transaction response type. The following shows the response type. **RS[2:0] Response** 000 Idle State 100 Reserved 001 Retry 101 No data 010 Reserved 110 Implicit Write-back 011 Reserved 111 Normal Data
HTRDY#	1.5V	MAIN	I/O GTL+	**Target Ready:** During write cycles, response agent will drive TRDY# to indicate the agent is ready to accept data.
DRDY#	1.5V	MAIN	I/O GTL+	**Data Ready:** DRDY# is driven by the bus owner whenever the data is valid on the bus.
DBSY#	1.5V	MAIN	I/O GTL+	**Data Bus Busy:** Whenever the data is not valid on the bus with DRDY# is deserted, DBSY# is asserted to hold the bus.

Name	Tolerance	Power Plane	Type Attr	Description
BPRI#	1.5V	MAIN	O GTL+	**Priority Agent Bus Request:** BPRI# is driven by the priority agent that wants to request the bus. BPRI# has higher priority than BREQ0# to access a bus.
CPURST#	1.5V	MAIN	O GTL+	**Host Bus Reset:** CPURST# is used to keep all the bus agents in the same initial state before valid cycles issued.
HA[31:3]#	1.5V	MAIN	I/O GTL+	**Host Address Bus :**
HD[63:0]#	1.5V	MAIN	I/O GTL+	**Host Data Bus :**
FERR#	1.5V~5V	MAIN	I	**Floating Point Error :** CPU will assert this signal upon a floating point error occurring.
IGNE#	1.5V~5V	MAIN	OD	**Ignore Numeric Error :** IGNE# is asserted to inform CPU to ignore a numeric error. **Speed Trap for PII :** This pin will be forced to voltage level according to the input value of MD41 or APC0h.4 during system reset period.
NMI	1.5V~5V	MAIN	OD	**Non-Maskable Interrupt :** A rising edge on NMI will trigger a non-maskable interrupt to CPU. Speed Trap for PII : This pin will be forced to voltage level according to the input value of MD44 or APC0h.7 during system reset period.
INTR	1.5V~5V	MAIN	OD	**Interrupt Request :** High-level voltage of this signal indicates the CPU that there is outstanding interrupt(s) needed to be serviced. **Speed Trap for PII :** This pin will be forced to voltage level according to the input value of MD43 or APC0h.6 during system reset period.
CPUSLP#	1.5V~5V	MAIN	OD	**CPU Sleep :** SiS630 can optionally assert CPUSLP# to force the CPU into deep sleep mode when going to S2 state.
STPCLK#	1.5V~5V	MAIN	OD	**Stop Clock :** STPCLK# will be asserted to inhibit or throttle CPU activities upon a pre-defined power management event occurs.
SMI#	1.5V~5V	MAIN	OD	**System Management Interrupt :** SMI# will be asserted when a pre-defined power management event occurs.

5.2 SiS630ST Slot1/Socket370 2D/3D Ultra AGP™ Single Chipset

Host Bus Interface

Name	Tolerance	Power Plane	Type Attr	Description
INIT#	1.5V~5V	MAIN	OD	**Initialization :** INIT is used to re-start the CPU without flushing its internal caches and registers. In Pentium II platform it is active high. This signal requires an external pull-up resistor tied to 3.3V.
A20M#	1.5V~5V	MAIN	OD	**Address 20 Mask :** When A20M# is asserted, the CPU A20 signal will be forced to "0". **Speed Trap for PII :** This pin will be forced to voltage level according to the input value of MD42 or APC0h.5 during system reset period.

DRAM Controller

Name	Tolerance	Power Plane	Type Attr	Description
SDCLK	3.3V/5V	MAIN	I	SDRAM Clock Input
MD[63:0]	3.3V	MAIN	I/O	System Memory Data Bus
MA[14:0]	3.3V	MAIN	O	System Memory Address Bus
CSA[5:0]#	3.3V	MAIN	O	SDRAM Chip Select
CSB[5:0]#	3.3V	MAIN	O	SDRAM Chip Select Signals (Duplicated Copy)
DQM[7:0]#	3.3V	MAIN	O	SDRAM Input/Output Data Mask
WE#	3.3V	MAIN	O	SDRAM Write Enable
SRAS#	3.3V	MAIN	O	SDRAM Row Address Strobe
SCAS#	3.3V	MAIN	O	SDRAM Column Address Strobe
CKE	3.3V	AUX	O	SDRAM Clock EnableE.

PCI Interface

Name	Tolerance	Power Plane	Type Attr	Description
PCICLK	3.3V/5V	MAIN	I	**PCI Clock :** The PCICLK input provides the fundamental timing and the internal operating frequency for the SiS Chip. It runs at the same frequency and skew of the PCI local bus.
C/BE[3:0]#	3.3V/5V	MAIN	I/O	**PCI Bus Command and Byte Enables:** PCI Bus Command and Byte Enables define the PCI command during the address phase of a PCI cycle, and the PCI byte enables during the data phases. C/BE[3:0]# are outputs when the SiS Chip is a PCI bus master and inputs when it is a PCI slave.
AD[31:0]	3.3V/5V	MAIN	I/O	**PCI Address /Data Bus:** In address phase: 1.When the SiS Chip is a PCI bus master, AD[31:0] are output signals. 2.When the SiS Chip is a PCI target, AD[31:0] are input signals. In data phase: 1.When the SiS Chip is a target of a memory read/write cycle, AD[31:0] are floating. 2.When the SiS Chip is a target of a configuration or an I/O cycle, AD[31:0] are output signals in a read cycle, and input signals in a write cycle.
PAR	3.3V/5V	MAIN	I/O	**Parity :** SiS630 drives out Even Parity covering AD[31:0] and C/BE[3:0]#. It does not check the input parity signal.
FRAME#	3.3V/5V	MAIN	I/O	**Frame#:** FRAME# is an output when the SiS Chip is a PCI bus master. The SiS Chip drives FRAME# to indicate the beginning and duration of an access. When the SiS Chip is a PCI slave device, FRAME# is an input signal.
IRDY#	3.3V/5V	MAIN	I/O	**Initiator Ready :** IRDY# is an output when the SiS Chip is a PCI bus master. The assertion of IRDY# indicates the current PCI bus master's ability to complete the current data phase of the transaction. For a read cycle, IRDY# indicates that the PCI bus master is prepared to accept the read data on the following rising edge of the PCI clock. For a write cycle, IRDY# indicates that the bus master has driven valid data on the PCI bus. When the SiS Chip is a PCI slave, IRDY# is an input pin.
TRDY#	3.3V/5V	MAIN	I/O	**Target Ready :** TRDY# is an output when the SiS Chip is a PCI slave. The assertion of TRDY# indicates the target agent's ability to complete the current data phase of the transaction. For a read cycle, TRDY# indicates that the target has driven valid data onto the PCI bus. For a write cycle, TRDY# indicates that the target is prepared to accept data from the PCI bus. When the SiS Chip is a PCI master, it is an input pin.

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PCI Interface

Name	Tolerance	Power Plane	Type Attr	Description
STOP#	3.3V/5V	MAIN	I/O	**Stop# :** STOP# indicates that the bus master must start terminating its current PCI bus cycle at the next clock edge and release control of the PCI bus. STOP# is used for disconnection, retry, and target-abortion sequences on the PCI bus.
DEVSEL#	3.3V/5V	MAIN	I/O	**Device Select :** As a PCI target, SiS Chip asserts DEVSEL# by doing positive or subtractive decoding. SiS Chip positively asserts DEVSEL# when the DRAM address is being accessed by a PCI master, PCI configuration registers or embedded controllers' registers are being addressed, or the BIOS memory space is being accessed. The low 16K I/O space and low 16M memory space are responded subtractively. The DEVESEL# is an input pin when SiS Chip is acting as a PCI master. It is asserted by the addressed agent to claim the current transaction.
PLOCK#	3.3V/5V	MAIN	I/O	**PCI Lock :** When PLOCK# is sampled asserted at the beginning of a PCI cycle, SiS630 considers itself being locked and remains in the locked state until PLOCK# is sampled and negated at the following PCI cycle.
PREQ[2:0]#	3.3V/5V	MAIN	I	**PCI Bus Request :** PCI Bus Master Request Signals
PGNT[2:0]#	3.3V	MAIN	O	**PCI Bus Grant :** PCI Bus Master Grant Signals
INT[A:D]#	3.3V/5V	MAIN	I	**PCI interrupt A,B,C,D :** The PCI interrupts will be connected to the inputs of the internal Interrupt controller through the rerouting logic associated with each PCI interrupt.
PCIRST#	3.3V	AUX	O	**PCI Bus Reset :** PCIRST# will be asserted during the period when PWROK is low, and will be kept on asserting until about 24ms after PWROK goes high.
SERR#	3.3V/5V	MAIN	I	**System Error :** When sampled active low, a non-maskable interrupt (NMI) can be generated to CPU if enabled.

AGP Interface

Name	Tolerance	Power Plane	Type Attr	Description
AGPCLK	3.3V	MAIN	I	**AGP Clock**
A_FRAME#	3.3V/1.5V	MAIN	I/O	**AGP Frame#**
A_IRDY#	3.3V/1.5V	MAIN	I/O	**AGP Initiator Ready**
A_TRDY#	3.3V/1.5V	MAIN	I/O	**AGP Target Ready**
A_STOP#	3.3V/1.5V	MAIN	I/O	**AGP Stop#**
A_DEVSEL#	3.3V/1.5V	MAIN	I/O	**AGP Device Select**
A_SERR#	3.3V/1.5V	MAIN	I	**AGP System Error**
A_REQ#	3.3V/1.5V	MAIN	I	**AGP Bus Request**
A_GNT#	3.3V/1.5V	MAIN	O	**AGP Bus Grant**
A_AD[31:0]	3.3V/1.5V	MAIN	I/O	**AGP Address/Data Bus**
A_C/BE[3:0]	3.3V/1.5V	MAIN	I/O	**AGP Command/Byte Enable**
A_PAR	3.3V/1.5V	MAIN	I/O	**AGP Parity**
ST[2:0]	3.3V/1.5V	MAIN	O	**AGP Status Bus**
PIPE#	3.3V/1.5V	MAIN	I	**AGP Pipeline Request**
SBA[7:0]	3.3V/1.5V	MAIN	I	**Side Band Address**
RBF#	3.3V/1.5V	MAIN	I	**Read Buffer Full**
WBF#	3.3V/1.5V	MAIN	I	**Write Buffer Full**
AD_STB[1:0]	3.3V/1.5V	MAIN	I/O	**AD Bus Strobe**
AD_STB[1:0]#	3.3V/1.5V	MAIN	I/O	**AD Bus Strobe Compliment**
SB_STB	3.3V/1.5V	MAIN	I	**Side Band Strobe**
SB_STB#	3.3V/1.5V	MAIN	I	**Side Band Strobe Compliment**

PCI IDE Interface

Name	Tolerance	Power Plane	Type Attr	Description
IDA[15:0]	3.3V/5V	MAIN	I/O	Primary Channel Data Bus
IDB[15:0]	3.3V/5V	MAIN	I/O	Secondary Channel Data Bus
IDECSA[1:0]#	3.3V	MAIN	O	Primary Channel CS[1:0]
IDECSB[1:0]#	3.3V	MAIN	O	Secondary Channel CS[1:0]
IIOR[A:B]#	3.3V	MAIN	O	Primary/Secondary Channel IOR# Signals
IIOW[A:B]#	3.3V	MAIN	O	Primary/Secondary Channel IOW# Signals
ICHRDY[A:B]	3.3V/5V	MAIN	I	Primary/Secondary Channel ICHRDY# Signals

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PCI IDE Interface

Name	Tolerance	Power Plane	Type Attr	Description
IDREQ[A:B]	3.3V/5V	MAIN	I	Primary/Secondary Channel DMA Request Signals
IDACK[A:B]#	3.3V	MAIN	O	Primary/Secondary Channel DMACK# Signals
IIRQ[A:B]	3.3V/5V	MAIN	I	Primary/Secondary Channel Interrupt Signals
IDSAA[2:0]	3.3V	MAIN	O	Primary Channel Address [2:0]
IDSAB[2:0]	3.3V	MAIN	O	Secondary Channel Address [2:0]
CBLID[A:B]	3.3V/5V	MAIN	I	Primary/Secondary Ultra-66 Cable ID
IDREQ[A:B]	3.3V/5V	MAIN	I	Primary/Secondary Channel DMA Request Signals
IDACK[A:B]#	3.3V	MAIN	O	Primary/Secondary Channel DMACK# Signals

VGA Interface

Name	Tolerance	Power Plane	Type Attr	Description
HSYNC	3.3V	MAIN	O	Horizontal Sync
VSYNC	3.3V	MAIN	O	Vertical Sync
SSYNC	3.3V	MAIN	O	Stereo Sync
DDCCLK	3.3V/5V	MAIN	I/O	Display Data Channel Clock Line
DDCDATA	3.3V/5V	MAIN	I/O	Display Data Channel Data Line
COMP		MAIN	AI	**Compensation Pin:** Connect this pin to AVDD via a 0.1uF capacitor
RSET		MAIN	AI	**Reference Resistor:** An external resistor is connected between the RSET pin and AGND to control the magnitude of the full-scale current.
VREF		MAIN	AI	**Voltage Reference:** Connect 0.1uF Capacitor to Ground.
VCS#	3.3V	MAIN	I/O	VGA Frame Buffer Cache Chip Select
ROUT		MAIN	AO	Red Signal Output
GOUT		MAIN	AO	Green Signal Output
BOUT		MAIN	AO	Blue Signal Output
VBA1 **VBCLK** **PLPWDN#**	3.3V	MAIN	O I/O O	**Display Memory Bank Select:** When 128bits DRAM interface enable, it represents the Memory Bank Select **Digital Video Clock Input:** When Video Bridge connected, it represents the Digital Video Clock Input **Panel Power Down** When external LCD transmitter connected, it represents power down.
VDQM[7:0]	3.3V	MAIN	O	Display Memory SDRAM Input /Output Mask
OSCI	3.3V/5V	MAIN	I	External 14.318MHz Clock Input
ENTEST	3.3V/5V	MAIN	I	Test Mode Enable
VMD[27:0]	3.3V	MAIN	I/O	Display Memory Data Bus bits [27:0]
VMA11 **VGCLK**	3.3V	MAIN	O O	**Display Memory Address bit 11 :** When 128bits DRAM interface enable, it represents the Memory Address bit 11 **Digital Video Clock Output:** When Video Bridge connected, it represents the Digital Video Clock Output
VMA10 **VBHCLK**	3.3V	MAIN	O O	**Display Memory Address bit 10:** When 128bits DRAM interface enable, it represents the Memory Address bit 10 **Control Clock Output:** When Video Bridge connected, it represents the Control Clock Output
VMD[63:60]	3.3V	MAIN	I/O	Display Memory Data Bus bits [63:60]
VMD[59:52] **VBRGB[7:0]**	3.3V	MAIN	I/O O	Display Memory Data Bus bits [59:52] Digital Video Data bits [7:0]
VMD[51:49] **VBRGB[18:16]**	3.3V	MAIN	I/O O	Display Memory Data Bus bits [51:49] Digital Video Data bits [18:16]
VMD[48:44] **VBRGB[19:23]**	3.3V	MAIN	I/O O	Display Memory Data Bus bits [48:44] Digital Video Data bits [19:23]
VMD[43:42] **VBRGB[10:11]**	3.3V	MAIN	I/O O	Display Memory Data Bus bits [43:42] Digital Video Data bits [10:11]
VMD[41:40] **VBRGB[9:8]]**	3.3V	MAIN	I/O O	Display Memory Data Bus bits [41:40] Digital Video Data bits [9:8]
VMD[39:38] **VBRGB[13:12]**	3.3V	MAIN	I/O O	Display Memory Data Bus bits [39:38] Digital Video Data bits [13:12]
VMD[37:36] **VBRGB[14:15]**	3.3V	MAIN	I/O O	Display Memory Data Bus bits [37:36] Digital Video Data bits [14:15]
VMD35 **VBBLANKN**	3.3V	MAIN	I/O O	Display Memory Data Bus bit 35 Digital Video Display Enable
VMD[34:33] **TVCTL[0:1]**	3.3V	MAIN	I/O O	Display Memory Data Bus bits [34:33] Video Bridge Data Control bits [0:1]
VMD32 **VBCAD**	3.3V	MAIN	I/O I/O	Display Memory Data Bus bit 32 Video Bridge Programming Control
VMD31 **VBHSYNC**	3.3V	MAIN	I/O I/O	Display Memory Data Bus bit 31 Digital Video Horizontal Sync
VMD30 **VBVSYNC**	3.3V	MAIN	I/O I/O	Display Memory Data Bus bit 30 Digital Video Vertical Sync
VMD29 **DDC2CLK**	3.3V	MAIN	I/O I/O	Display Memory Data Bus bit 29 Second Display data channel clock line
VMD28 **DDC2DATA**	3.3V	MAIN	I/O I/O	Display Memory Data Bus bit 28 Second Display data channel data line

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Power management Interface

Name	Tolerance	Power Plane	Type Attr	Description
ACPILED	<=5V	AUX	OD	**ACPILED :** ACPILED can be used to control the blinking of an LED at the frequency of 1Hz to indicate the system is at power saving mode.
EXTSMI#	3.3V/5V	MAIN	I	**External SMI# :** EXTSMI# can be used to generate wakeup event, sleep event, or SCI/SMI#/GPEIRQ event to the ACPI compatible power management unit.
PME#	3.3V/5V	AUX	I/O	**PME# :** When the system is in power-down mode, an active low event on PME# will cause the PSON# to go low and hence turn on the power supply. When the system is in suspend mode, an active PME# event will cause the system wakeup and generate an SCI/SMI#/GPEIRQ.
PSON#	<=5V	AUX	OD	**ATX Power ON/OFF control :** PSON# is used to control the on/off state of the ATX power supply. When the ATX power supply is in the OFF state, an activated power-on event will force the power supply to ON state.
PWRBTN#	3.3V/5V	AUX	I	**Power Button :** This signal is from the power button switch and will be monitored by the ACPI compatible power management unit to switch the system between working and sleeping states.
RING	3.3V/5V	MAIN	I	R**ing Indication :** An active RING pulse and lasting for more than 4ms will cause a wakeup event for system to wake form S1~S5.
THERM#	3.3V/5V	MAIN	I	**Thermal Detect :** THERM# is connected to the internal ACPI compatible power management unit as an indication of outstanding thermal event. An active THERM# event can be used to generate SCI/SMI#/GPEIRQ. If THERM# is activated for more than 2 second, a thermal override event will occur and the system will enter CPU thermal throttling mode automatically.

DAT/CLK Interface

Name	Tolerance	Power Plane	Type Attr	Description
DAT	3.3V/5V	MAIN	I/OD	**DAT :** data input/output pin.
CLK	3.3V/5V	MAIN	I/OD	**CLK :** clock input/output pin.
ALT# **GPIO15** **TXEN**	3.3V/5V	AUX	I/OD I/O/OD O	**Alert :** This pin is used for DAT/CLK device to wake up the system from sleep state or to generate SCI/SMI#/GPEIRQ. **General Purpose Input/Output 15 :** **Transmit Enable :** When set to a 1, and the transmit state machine is idle, then the transmit state machine becomes active. This bit will read back as a 1 whenever the transmit state machine is active. After initial power-up, software must insure that the transmitter has completely reset before setting this bit.

Keyboard controller Interface

Name	Tolerance	Power Plane	Type Attr	Description
KBDAT **GPIO10**	3.3V/5V	AUX	I/OD I/O/OD	**Keyboard Dada :** When the internal keyboard controller is enabled, this pin is used as the keyboard data signal. **General Purpose Input/Output 10 :** Refer to GPIO description.
KBCLK **GPIO11**	3.3V/5V	AUX	I/OD I/O/OD	**Keyboard Clock :** When the internal keyboard controller is enabled, this pin is used as the keyboard clock signal. General Purpose Input/Output 11 : Refer to GPIO description.
PMDAT **GPIO12**	3.3V/5V	AUX	I/OD I/O/OD	**PS2 Mouse Data:** When the internal keyboard and PS2 mouse controllers are enabled, this pin is used as PS2 mouse data signal. **General Purpose Input/Output 12 :**
PMCLK **GPIO13**	3.3V/5V	AUX	I/OD I/O/OD	**PS2 Mouse Clock:** When the internal keyboard and PS2 mouse controllers are enabled, this pin is used as the PS2 mouse clock signal. **General Purpose Input/Output 13 :**
KLOCK# **GPIO14** **TXD[3]**	3.3V/5V	AUX	I I/O/OD O	**Keyboard Lock:** When KLOCK# is tied low, the internal keyboard controller will not respond to any key-strikes. **General Purpose Input/Output 14 :** **Transmit Data[3] :**

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LPC Interface

Name	Tolerance	Power Plane	Type Attr	Description
LAD[3:0]	3.3V/5V	MAIN	I/O	**LPC Address/Data Bus :** LPC controller drives these four pins to transmit LPC command, address, and data to LPC device.
LDRQ#	3.3V/5V	MAIN	I	**LPC DMA Request 0:** This pin is used by LPC device to request DMA cycle.
LFRAME#	3.3V	MAIN	O	**LPC Frame :** This pin is used to notify LPC device that a start or a abort LPC cycle will occur.
SIRQ	3.3V/5V	MAIN	I/OD	**Serial IRQ :** This signal is used as the serial IRQ line signal.

RTC Interface

Name	Tolerance	Power Plane	Type Attr	Description
AUXOK	1.8V	RTC	I	**Auxiliary Power OK :** This signal is supplied from the power source of resume well. It is also used to reset the logic in resume power well. If there is no auxiliary power source on the system, this pin should be tied together with PWROK.
BATOK	1.8V	RTC	I	**Battery Power OK:** When the internal RTC is enabled, this signal is used to indicate that the power of RTC well is stable. It is also used to reset the logic in RTC well. If the internal RTC is disabled, this pin should be tied low.
OSC32KHI	1.8V	RTC	I	**RTC 32.768 KHz Input** : When internal RTC is enabled, this pin provides the 32.768 KHz clock signal from external crystal or oscillator.
OSC32KHO	<1.8V	RTC	O	**RTC 32.768 KHz Output :** When internal RTC is enabled, this pin should be connected with the other end of the 32.768 KHz crystal or left unconnected if an oscillator is used.
PWROK	1.8V	RTC	I	**Main Power OK** : A high-level input to this signal indicates the power being supplied to the system is in stable operating state. During the period of PWROK being low, CPURST and PCIRST# will all be asserted until after PWROK goes high for 24 ms.

AC'97 Interface

Name	Tolerance	Power Plane	Type Attr	Description
AC_BITCLK	3.3V/5V	MAIN	I	**AC'97Bit Clock :** This signal is a 12.288MHz serial data clock, which is generated by primary Codec.
AC_RESET#	3.3V	AUX	O	**AC'97 Reset :** Hardware reset signal for external Codecs.
AC_SDIN[1:0]	3.3V/5V	AUX	I	**AC'97 Serial Data input :** Serial data input from primary Codec and secondary Codec.
AC_SDOUT	3.3V	MAIN	O	**AC'97 Serial Data output :** Serial data output to Codecs.
AC_SYNC	3.3V	MAIN	O	**AC'97 Syncronization :** This is a 48KHz signal, which is used to syncronize the Codecs.
SPDIF **GPIO7**	3.3V/5V	MAIN	O I/O/OD	**S/PDIF Transmitter Output** **General Purpose Input/Output 7 :** Refer to GPIO description.

MAC Interface

Name	Tolerance	Power Plane	Type Attr	Description
GPIO3 **RXER**	3.3V/5V	AUX	I/O/OD I	**General Purpose Input/Output 3:** **RX Packet Error:** This event is signaled after the last receive descriptor in a failed packet reception that has been updated with valid status.
OSC25M **HI**	3.3V	AUX	I	**PHY 25MHz Clock Input: :** This pin is supplied the 25MHz clock signal input from the external crystal or an oscillator.
GPIO8 **MDC**	3.3V/5V	AUX	I/O/OD O	**General Purpose Input/Output 8:** **Management Data Clock:**
GPIO[0] **PREQ3#** **TXD[0]**	3.3V/5V	AUX	I/O/OD O O	**General Purpose Input/Output 1 :** **PCI Bus Grant 3** **Transmit Data[1]**
GPIO[4] **TXCLK**	3.3V/5V	AUX	I/O/OD I	**General Purpose Input/Output 4 :** **Transmit Clock :**
GPIO[5] **COL**	3.3V/5V	AUX	I/O/OD I	**General Purpose Input/Output 5 :** **Collision Detect :**
GPIO[6] **CRS**	3.3V/5V	AUX	I/O/OD I	**General Purpose Input/Output 5 :** **Carrier Sense :**
GPIO[9] **RXCLK**	3.3V/5V	AUX	I/O/OD I	**General Purpose Input/Output 5 :** **Receive Clock :**

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USB Interface

Name	Tolerance	Power Plane	Type Attr	Description
CLK48M	3.3V/5V	MAIN	I	**USB 48 MHz clock input :** This signal provides the fundamental clock for the USB Controller.
OC0# **MDIO#**	3.3V/5V	AUX	I I/O	**USB Port 0 Over Current Detection :** OC0# is used to detect the over current condition of USB Port 0. **MANAGEMENT DATA I/O:**
OC1# **RXDV**	3.3V/5V	AUX	I I	**USB Port 1 Over Current Detection :** OC1# is used to detect the over current condition of USB Port 1. **Receive Data Valid**
LDRQ1# **GPIO2** **TXD[2]**	3.3V/5V	MAIN	I I/O/OD O	**LPC DMA Request 1 :** LDRQ1# is the second LPC DMA request signal used by LPC Device to request DMA cycles. **General Purpose Input/Output 2 :** Refer to GPIO description. **TRANSMIT DATA[2]:**
UV[5:0] +	3.3V	AUX	I/O	USB Port [5:0] Positive Input/Output
UV[5:0]-	3.3V	AUX	I/O	USB Port [5:0] Negative Input/Output

Power and Ground Signals

Name	Tolerance	Power Plane	Type Attr	Description
VSS		GROUND		0V
IVDD		MAIN		1.8V
IVDD (AUX)		AUX		1.8V
OVDD (AUX)		AUX		3.3V
USBVDD		AUX		3.3V
RTCVDD		RTC		1.8V
DCLKAVDD		MAIN		3.3V
ECLKAVDD		MAIN		3.3V
TXAVDD		AUX		3.3V
RXAVDD		AUX		3.3V
DACAVDD		MAIN		3.3V
IDEAVDD		MAIN		1.8V
SDAVDD		MAIN		3.3V
CPUAVDD		MAIN		3.3V
VTTB		MAIN		1.5V
VSSQ		GROUND		0V
VTTA		MAIN		1.5V
VCC3		MAIN		3.3V

Legacy I/o and Miscellaneous Signals

Name	Tolerance	Power Plane	Type Attr	Description
AGPRCOMP	3.3V/1.5V	MAIN	I	**AGP Digital Compensation**
AGPVEREF		MAIN	I	**AGP Reference Voltage:** 3.3V mode – 0.4*VDDQ=1.32V 1.5V mode – 0.5*VDDQ=0.75V
GTLREF		MAIN	I	**GTL Reference Voltage:** 2/3 * Vtt (+/-2%)
SPK	3.3V	MAIN	O	**Speaker output :** The SPK is connected to the system speaker.

5.3 PCI1410 PCMCIA Controller

Power Supply

Name	I/O	Description
GND		Device ground terminals
VCC		Power supply terminal for core logic (3.3V)
VCCCB		Clamp voltage for PC Card interface. Matches card signaling environment, 5 V or 3.3 V.
VCCI		Clamp voltage for interrupt subsystem interface and miscellaneous I/O, 5 V or 3.3 V
VCCP		Clamp voltage for PCI signaling, 5 V or 3.3 V

PC Card Power Switch

Name	I/O	Description
VCCD0 **VCCD1**	O	Logic controls to the TPS2211 PC Card power interface switch to control AVCC.
VPPD0 **VPPD1**	O	Logic controls to the TPS2211 PC Card power interface switch to control AVPP.

PCI System

Name	I/O	Description
GRST#	I	Global reset. When the global reset is asserted, the GRST# signal causes the PCI1410 to place all output buffers in a high-impedance state and reset all internal registers. When GRST# is asserted, the device is completely in its default state. For systems that require wake-up from D3, GRST# will normally be asserted only during initial boot. PRST# should be used following initial boot so that PME context is retained when transitioning from D3 to D0. For systems that do not require wake-up from D3, GRST# should be tied to PRST#. When the SUSPEND# mode is enabled, the device is protected from the GRST#, and the internal registers are preserved. All outputs are placed in a high-impedance state, but the contents of the registers are preserved.
PCLK	I	PCI bus clock. PCLK provides timing for all transactions on the PCI bus. All PCI signals are sampled at the rising edge of PCLK.
PRST#	I	PCI reset. When the PCI bus reset is asserted, PRST# causes the PCI1410 to place all output buffers in a high-impedance state and reset internal registers. When PRST# is asserted, the device is completely nonfunctional. After PRST is deasserted, the PCI1410 is in a default state. When the SUSPEND# mode is enabled, the device is protected from the PRST#, and the internal registers are preserved. All outputs are placed in a high-impedance state, but the contents of the registers are preserved.

PCI Interface Control

Name	I/O	Description
DEVSEL#	I/O	PCI device select. The PCI1410 asserts DEVSEL# to claim a PCI cycle as the target device. As a PCI initiator on the bus, the PCI1410 monitors DEVSEL# until a target responds. If no target responds before timeout occurs, then the PCI1410 terminates the cycle with an initiator abort.
FRAME#	I/O	PCI cycle frame. FRAME# is driven by the initiator of a bus cycle. FRAME# is asserted to indicate that a bus transaction is beginning, and data transfers continue while this signal is asserted. When FRAME# is deasserted, the PCI bus transaction is in the final data phase.
GNT#	I	PCI bus grant. GNT# is driven by the PCI bus arbiter to grant the PCI1410 access to the PCI bus after the current data transaction has completed. GNT# may or may not follow a PCI bus request, depending on the PCI bus parking algorithm.
IDSEL	I	Initialization device select. IDSEL selects the PCI1410 during configuration space accesses. IDSEL can be connected to one of the upper 24 PCI address lines on the PCI bus.
IRDY#	I/O	PCI initiator ready. IRDY# indicates the PCI bus initiator's ability to complete the current data phase of the transaction. A data phase is completed on a rising edge of PCLK where both IRDY# and TRDY# are asserted. Until IRDY# and TRDY# are both sampled asserted, wait states are inserted.
PERR#	I/O	PCI parity error indicator. PERR# is driven by a PCI device to indicate that calculated parity does not match PAR when PERR# is enabled through bit 6 of the command register.
REQ#	O	PCI bus request. REQ# is asserted by the PCI1410 to request access to the PCI bus as an initiator.
SERR#	O	PCI system error. SERR# is an output that is pulsed from the PCI1410 when enabled through bit 8 of the command register indicating a system error has occurred. The PCI1410 need not be the target of the PCI cycle to assert this signal. When SERR# is enabled in the command register, this signal also pulses, indicating that an address parity error has occurred on a CardBus interface.
STOP#	I/O	PCI cycle stop signal. STOP# is driven by a PCI target to request the initiator to stop the current PCI bus transaction. STOP# is used for target disconnects and is commonly asserted by target devices that do not support burst data transfers.
TRDY#	I/O	PCI target ready. TRDY# indicates the primary bus target's ability to complete the current data phase of the transaction. A data phase is completed on a rising edge of PCLK when both IRDY# and TRDY# are asserted. Until both IRDY# and TRDY# are asserted, wait states are inserted.

5.3 PCI1410 PCMCIA Controller

Multifunction and Miscellaneous Pins

Name	I/O	Description
MFUNC0	I/O	Multifunction terminal 0. MFUNC0 can be configured as parallel PCI interrupt INTA#, GPI0, GPO0, socket activity LED output, ZV switching outputs, CardBus audio PWM, GPE#, or a parallel IRQ.
MFUNC1	I/O	Multifunction terminal 1. MFUNC1 can be configured as GPI1, GPO1, socket activity LED output, ZV switching outputs, CardBus audio PWM, GPE#, or a parallel IRQ. Serial data (SDA). When VPPD0 and VPPD1 are high after a PCI reset, the MFUNC1 terminal provides the SDA signaling for the serial bus interface. The two-pin serial interface loads the subsystem identification and other register defaults from an EEPROM after a PCI reset.
MFUNC2	I/O	Multifunction terminal 2. MFUNC2 can be configured as PC/PCI DMA request, GPI2, GPO2, socket activity LED output, ZV switching outputs, CardBus audio PWM, GPE#, RI_OUT#, or a parallel IRQ.
MFUNC3	I/O	Multifunction terminal 3. MFUNC3 can be configured as a parallel IRQ or the serialized interrupt signal IRQSER.
MFUNC4	I/O	Multifunction terminal 4. MFUNC4 can be configured as PCI LOCK#, GPI3, GPO3, socket activity LED output, ZV switching outputs, CardBus audio PWM, GPE#, RI_OUT#, or a parallel IRQ. Serial clock (SCL). When VPPD0 and VPPD1 are high after a PCI reset, the MFUNC4 terminal provides the SCL signaling for the serial bus interface. The two-pin serial interface loads the subsystem identification and other register defaults from an EEPROM after a PCI reset.
MFUNC5	I/O	Multifunction terminal 5. MFUNC5 can be configured as PC/PCI DMA grant, GPI4, GPO4, socket activity LED output, ZV switching outputs, CardBus audio PWM, GPE#, or a parallel IRQ.
MFUNC6	I/O	Multifunction terminal 6. MFUNC6 can be configured as a PCI CLKRUN# or a parallel IRQ.
RI_OUT#/PME#	O	Ring indicate out and power management event output. Terminal provides an output for ring-indicate or PME# signals.
SPKROUT	O	Speaker output. SPKROUT is the output to the host system that can carry SPKR# or CAUDIO through the PCI1410 from the PC Card interface. SPKROUT is driven as the exclusive-OR combination of card SPKR#//CAUDIO inputs.
SUSPEND#	I	Suspend. SUSPEND# protects the internal registers from clearing when the GRST# or PRST# signal is asserted.

PCI Address and Data

Name	I/O	Description
AD[31:0]	I/O	PCI address/data bus. These signals make up the multiplexed PCI address and data bus on the primary interface. During the address phase of a primary bus PCI cycle, AD31–AD0 contain a 32-bit address or other destination information. During the data phase, AD31–AD0 contain data.
C/BE#[3:0]	I/O	PCI bus commands and byte enables. These signals are multiplexed on the same PCI terminals. During the address phase of a primary bus PCI cycle, C/BE#3–C/BE#0 define the bus command. During the data phase, this 4-bit bus is used as byte enables. The byte enables determine which byte paths of the full 32-bit data bus carry meaningful data. C/BE#0 applies to byte 0 (AD7–AD0), C/BE#1 applies to byte 1 (AD15–AD8), C/BE2 applies to byte 2 (AD23–AD16), and C/BE#3 applies to byte 3 (AD31–AD24).
PAR	I/O	PCI bus parity. In all PCI bus read and write cycles, the PCI1410 calculates even parity across the AD31–AD0 and C/BE#3–C/BE#0 buses. As an initiator during PCI cycles, the PCI1410 outputs this parity indicator with a one-PCLK delay. As a target during PCI cycles, the calculated parity is compared to the initiator's parity indicator. A compare error results in the assertion of a parity error (PERR#).

16-Bit PC Card Address and Data (Slots A and B)

Name	I/O	Description
ADDR[25:0]	O	PC Card address. 16-bit PC Card address lines. ADDR25 is the most significant bit.
DATA[15:0]	I/O	PC Card data. 16-bit PC Card data lines. DATA15 is the most significant bit.

5.3 PCI1410 PCMCIA Controller

16-Bit PC Card Interface Control (Slots A and B)

Name	I/O	Description
BVD1 (STSCHG#/RI#)	I	Battery voltage detect 1. BVD1 is generated by 16-bit memory PC Cards that include batteries. BVD1 is used with BVD2 as an indication of the condition of the batteries on a memory PC Card. Both BVD1 and BVD2 are high when the battery is good. When BVD2 is low and BVD1 is high, the battery is weak and should be replaced. When BVD1 is low, the battery is no longer serviceable and the data in the memory PC Card is lost. Status change. STSCHG# is used to alert the system to a change in the READY, write protect, or battery voltage dead condition of a 16-bit I/O PC Card. Ring indicate. RI is used by 16-bit modem cards to indicate a ring detection.
BVD2 (SPKR#)	I	Battery voltage detect 2. BVD2 is generated by 16-bit memory PC Cards that include batteries. BVD2 is used with BVD1 as an indication of the condition of the batteries on a memory PC Card. Both BVD1 and BVD2 are high when the battery is good. When BVD2 is low and BVD1 is high, the battery is weak and should be replaced. When BVD1 is low, the battery is no longer serviceable and the data in the memory PC Card is lost. Speaker. SPKR# is an optional binary audio signal available only when the card and socket have been configured for the 16-bit I/O interface. The audio signals from cards A and B are combined by the PCI1410 and are output on SPKROUT. DMA request. BVD2 can be used as the DMA request signal during DMA operations to a 16-bit PC Card that supports DMA. The PC Card asserts BVD2 to indicate a request for a DMA operation.
CD1# CD2#	I	Card detect 1 and Card detect 2. CD1# and CD2# are internally connected to ground on the PC Card. When a PC Card is inserted into a socket, CD1# and CD2# are pulled low.
CE1# CE2#	O	Card enable 1 and card enable 2. CE1# and CE2# enable even- and odd-numbered address bytes. CE1# enables even-numbered address bytes, and CE2# enables odd-numbered address bytes.
INPACK#	I	Input acknowledge. INPACK# is asserted by the PC Card when it can respond to an I/O read cycle at the current address. DMA request. INPACK# can be used as the DMA request signal during DMA operations from a 16-bit PC Card that supports DMA. If it is used as a strobe, then the PC Card asserts this signal to indicate a request for a DMA operation.
IORD#	O	I/O read. IORD# is asserted by the PCI1410 to enable 16-bit I/O PC Card data output during host I/O read cycles. DMA write. IORD# is used as the DMA write strobe during DMA operations from a 16-bit PC Card that supports DMA. The PCI1410 asserts IORD# during DMA transfers from the PC Card to host memory.
IOWR#	O	I/O write. IOWR# is driven low by the PCI1410 to strobe write data into 16-bit I/O PC Cards during host I/O write cycles. DMA read. IOWR# is used as the DMA write strobe during DMA operations from a 16-bit PC Card that supports DMA. The PCI1410 asserts IOWR# during transfers from host memory to the PC Card.
OE#	O	Output enable. OE# is driven low by the PCI1410 to enable 16-bit memory PC Card data output during host memory read cycles. DMA terminal count. OE# is used as terminal count (TC) during DMA operations to a 16-bit PC Card that supports DMA. The PCI1410 asserts OE# to indicate TC for a DMA write operation.
READY (IREQ#)	I	Ready. The ready function is provided by READY when the 16-bit PC Card and the host socket are configured for the memory-only interface. READY is driven low by the 16-bit memory PC Cards to indicate that the memory card circuits are busy processing a previous write command. READY is driven high when the 16-bit memory PC Card is ready to accept a new data transfer command. Interrupt request. IREQ# is asserted by a 16-bit I/O PC Card to indicate to the host that a device on the 16-bit I /O PC Card requires service by the host software. IREQ# is high (deasserted) when no interrupt is requested.
REG#	O	Attribute memory select. REG# remains high for all common memory accesses. When REG# is asserted, access is limited to attribute memory (OE# or WE# active) and to the I/O space (IORD# or IOWR# active). Attribute memory is a separately accessed section of card memory and is generally used to record card capacity and other configuration and attribute information. DMA acknowledge. REG# is used as a DMA acknowledge (DACK#) during DMA operations to a 16-bit PC Card that supports DMA. The PCI1410 asserts REG to indicate a DMA operation. REG# is used in conjunction with the DMA read (IOWR#) or DMA write (IORD#) strobes to transfer data.
RESET	O	PC Card reset. RESET forces a hard reset to a 16-bit PC Card.
WAIT#	I	Bus cycle wait. WAIT# is driven by a 16-bit PC Card to extend the completion of the memory or I/O cycle in progress.
WE#	O	Write enable. WE# is used to strobe memory write data into 16-bit memory PC Cards. WE# is also used for memory PC Cards that employ programmable memory technologies. DMA terminal count. WE# is used as TC# during DMA operations to a 16-bit PC Card that supports DMA. The PCI1410 asserts WE# to indicate TC# for a DMA read operation.
WP (IOIS16#)	I	Write protect. WP applies to 16-bit memory PC Cards. WP reflects the status of the write-protect switch on 16-bit memory PC Cards. For 16-bit I/O cards, WP is used for the 16-bit port (IOIS16#) function. I/O is 16 bits. IOIS16# applies to 16-bit I/O PC Cards. IOIS16# is asserted by the 16-bit PC Card when the address on the bus corresponds to an address to which the 16-bit PC Card responds, and the I/O port that is addressed is capable of 16-bit accesses. DMA request. WP can be used as the DMA request signal during DMA operations to a 16-bit PC Card that supports DMA. If used, then the PC Card asserts WP to indicate a request for a DMA operation.
VS1# VS2#	I/O	Voltage sense 1 and voltage sense 2. VS1# and VS2#, when used in conjunction with each other, determine the operating voltage of the PC Card.

5.3 PCI1410 PCMCIA Controller

CardBus PC Card Interface System (Slots A and B)

Name	I/O	Description
CCLK	O	CardBus clock. CCLK provides synchronous timing for all transactions on the CardBus interface. All signals except CRST#, CCLKRUN#, CINT#, CSTSCHG, CAUDIO, CCD2#, CCD1#, CVS2, and CVS1 are sampled on the rising edge of CCLK, and all timing parameters are defined with the rising edge of this signal. CCLK operates at the PCI bus clock frequency, but it can be stopped in the low state or slowed down for power savings.
CCLKRUN#	I/O	CardBus clock run. CCLKRUN# is used by a CardBus PC Card to request an increase in the CCLK frequency, and by the PCI1410 to indicate that the CCLK frequency is going to be decreased.
CRST#	O	CardBus reset. CRST# brings CardBus PC Card-specific registers, sequencers, and signals to a known state. When CRST# is asserted, all CardBus PC Card signals are placed in a high-impedance state, and the PCI1410 drives these signals to a valid logic level. Assertion can be asynchronous to CCLK, but deassertion must be synchronous to CCLK.

CardBus PC Card Address and Data (Slots A and B)

Name	I/O	Description
CAD[31:0]	I/O	CardBus address and data. These signals make up the multiplexed CardBus address and data bus on the CardBus interface. During the address phase of a CardBus cycle, CAD31–CAD0 contain a 32-bit address. During the data phase of a CardBus cycle, CAD31–CAD0 contain data. CAD31 is the most significant bit.
CC/BE#[3:0]	I/O	CardBus bus commands and byte enables. CC/BE#3–CC/BE#0 are multiplexed on the same CardBus terminals. During the address phase of a CardBus cycle, CC/BE#3–CC/BE#0 define the bus command. During the data phase, this 4-bit bus is used as byte enables. The byte enables determine which byte paths of the full 32-bit data bus carry meaningful data. CC/BE#0 applies to byte 0 (CAD7–CAD0), CC/BE#1 applies to byte 1 (CAD15–CAD8), CC/BE#2 applies to byte 2 (CAD23–CAD8), and CC/BE#3 applies to byte 3 (CAD31–CAD24).
CPAR	I/O	CardBus parity. In all CardBus read and write cycles, the PCI1410 calculates even parity across the CAD and CC/BE# buses. As an initiator during CardBus cycles, the PCI1410 outputs CPAR with a one-CCLK delay. As a target during CardBus cycles, the calculated parity is compared to the initiator's parity indicator; a compare error results in a parity error assertion.

CardBua PC Card Interface Control (Slots A and B)

Name	I/O	Description
CAUDIO	I	CardBus audio. CAUDIO is a digital input signal from a PC Card to the system speaker. The PCI1410 supports the binary audio mode and outputs a binary signal from the card to SPKROUT.
CBLOCK#	I/O	CardBus lock. CBLOCK# is used to gain exclusive access to a target.
CCD1# **CCD2#**	I	CardBus detect 1 and CardBus detect 2. CCD1# and CCD2# are used in conjunction with CVS1 and CVS2 to identify card insertion and interrogate cards to determine the operating voltage and card type.
CE1# **CE2#**	O	Card enable 1 and card enable 2. CE1# and CE2# enable even- and odd-numbered address bytes. CE1# enables even-numbered address bytes, and CE2# enables odd-numbered address bytes.
CDEVSEL#	I/O	CardBus device select. The PCI1410 asserts CDEVSEL# to claim a CardBus cycle as the target device. As a CardBus initiator on the bus, the PCI1410 monitors CDEVSEL# until a target responds. If no target responds before timeout occurs, then the PCI1410 terminates the cycle with an initiator abort.
CFRAME#	I/O	CardBus cycle frame. CFRAME# is driven by the initiator of a CardBus bus cycle. CFRAME# is asserted to indicate that a bus transaction is beginning, and data transfers continue while this signal is asserted. When CFRAME# is deasserted, the CardBus bus transaction is in the final data phase.
CGNT#	O	CardBus bus grant. CGNT# is driven by the PCI1410 to grant a CardBus PC Card access to the CardBus bus after the current data transaction has been completed.
CINT#	I	CardBus interrupt. CINT# is asserted low by a CardBus PC Card to request interrupt servicing from the host.
CIRDY#	I/O	CardBus initiator ready. CIRDY# indicates the CardBus initiator's ability to complete the current data phase of the transaction. A data phase is completed on a rising edge of CCLK when both CIRDY# and CTRDY# are asserted. Until CIRDY# and CTRDY# are both sampled asserted, wait states are inserted.

5.3 PCI1410 PCMCIA Controller

CardBua PC Card Interface Control (Slots A and B) (Continued)

Name	I/O	Description
CPERR#	I/O	CardBus parity error. CPERR# reports parity errors during CardBus transactions, except during special cycles. It is driven low by a target two clocks following that data when a parity error is detected.
CREQ#	I	CardBus request. CREQ# indicates to the arbiter that the CardBus PC Card desires use of the CardBus bus as an initiator.
CSERR#	I	CardBus system error. CSERR# reports address parity errors and other system errors that could lead to catastrophic results. CSERR# is driven by the card synchronous to CCLK, but deasserted by a weak pullup, and may take several CCLK periods. The PCI1410 can report CSERR# to the system by assertion of SERR# on the PCI interface.
CSTOP#	I/O	CardBus stop. CSTOP# is driven by a CardBus target to request the initiator to stop the current CardBus transaction. CSTOP# is used for target disconnects, and is commonly asserted by target devices that do not support burst data transfers.
CSTSCHG	I	CardBus status change. CSTSCHG alerts the system to a change in the card's status, and is used as a wake-up mechanism.
CTRDY#	I/O	CardBus target ready. CTRDY# indicates the CardBus target's ability to complete the current data phase of the transaction. A data phase is completed on a rising edge of CCLK, when both CIRDY# and CTRDY# are asserted; until this time, wait states are inserted.
CVS1 **CVS2**	I/O	CardBus voltage sense 1 and CardBus voltage sense 2. CVS1 and CVS2 are used in conjunction with CCD1# and CCD2# to identify card insertion and interrogate cards to determine the operating voltage and card type.

5.4 FW323 IEEE 1394 Controller

Pin	Type	Symbol	Description
1	-	**VDD**	**Power.**
2	-	**VSS**	**Ground.**
3	I	**CARDBUS**	**CardBus (Active-Low).** Selects mode of operation for PCI output Buffers. Tie low for cardbus operation, high for PCI operation. An internal pull-up is provided to force buffers to PCI mode, if no connection is made to this pin.
4	-	**NC**	**No Connect.**
5	O	**CAN**	**Cable Not Active.** CAN output is provided for use in legacy power management systems.
6	O	**NANDTREE**	**Nand Tree Test Output.** When the chip is placed into the NAND tree test mode, the pin is the output of the NAND tree logic. This pin is not used during functional operation.
7	I	**TEST1**	**Test.** Used for device testing. Tie to VSS.
8	I/O	**ROM_CLK**	**ROM Clock.**
9	I/O	**ROM_AD**	**ROM Address/Data.**
10	I	**TEST0**	**Test.** Used for device testing. Tie to VSS.
11	-	**VDD**	**Power**
12	-	**VSS**	**Ground.**
13	I/O	**CLKRUNN**	**CLKRUNN (Active-Low).** Optional signal for PCI mobile environment. If not used, CLKRUNN pin needs to be pulled down to VSS for correct operation.
14	O	**CPI_INTAN**	**PCI Interrupt (Active-Low).**
15	I	**PCI_RSTN**	**PCI Reset (Active-Low).**
16	I	**PCI_GNTN**	**PCI Grant Signal (Active-Low).**
17	O	**PCI_REQN**	**PCI Request Signal (Active-Low).**
18	O	**PCI_PMEN**	**PCI Power Management Event (Active-Low).**
19	-	**VDD**	**Power.**
20	I	**PCI)CLK**	**PCI Clock Input.** 33MHz.
21	-	**VSS**	**Ground.**
22	I/O	**PCI_AD[31]**	**PCI Address/Data Bit.**
23	I/O	**PCI_AD[30]**	**PCI Address/Data Bit.**
24	I/O	**PCI_AD[29]**	**PCI Address/Data Bit.**
25	I/O	**PCI_AD[28]**	**PCI Address/Data Bit.**
26	-	**VDD**	**Power.**
27	-	**VSS**	**Ground.**
28	I/O	**PCI_AD[27]**	**PCI Address/Data Bit.**
29	I/O	**PCI_AD[26]**	**PCI Address/Data Bit.**
30	I/O	**PCI_AD[25]**	**PCI Address/Data Bit.**
31	I/O	**PCI_AD[24]**	**PCI Address/Data Bit.**
32	-	**VSS**	**Ground.**

Pin	Type	Symbol	Description
33	I/O	**PCI_CBEN[3]**	**PCI Command/Byte Enable (Active-Low).**
34	I	**PCI_IDSEL**	**PCI ID Select.**
35	I/O	**PCI_AD[23]**	**PCI Address/Data Bit.**
36	I/O	**PCI_AD[22]**	**PCI Address/Data Bit.**
37	-	**VDD**	**Power.**
38	-	**VSS**	**Ground.**
39	I/O	**PCI_AD[21]**	**PCI Address/Data Bit.**
40	I/O	**PCI_AD[20]**	**PCI Address/Data Bit.**
41	I/O	**PCI_AD[19]**	**PCI Address/Data Bit.**
42	I/O	**PCI_AD[18]**	**PCI Address/Data Bit.**
43	-	**VDD**	**Power.**
44	-	**VSS**	**Ground.**
45	I/O	**PCI_AD[17]**	**PCI Address/Data Bit.**
46	I/O	**PCI_AD[16]**	**PCI Address/Data Bit.**
47	I/O	**PCI_CBEN[2]**	**PCI Command/Byte Enable (Active-Low).**
48	I/O	**PCI_FRAMEN**	**PCI Frame Signal (Active-Low).**
49	-	**VDD**	**Power**
50	-	**VSS**	**Ground.**
51	I/O	**PCI_IRDYN**	**PCI Initiator Ready Signal (Active-Low).**
52	I/O	**PCI_TRDYN**	**PCI Target Ready Signal (Active-Low).**
53	I/O	**PCI_DEVSELN**	**PCI Device Select Signal (Active-Low).**
54	I/O	**PCI_STOPN**	**PCI Stop Signal (Active-Low).**
55	-	**VDD**	**Power.**
56	-	**VSS**	**Ground.**
57	I/O	**PCI_PERRN**	**PCI Parity Error Signal (Active-Low).**
58	I/O	**PCI_SERRN**	**PCI System Error Signal (Active-Low).**
59	I/O	**PCI_PAR**	**PCI Parity Signal.**
60	I/O	**PCI_CBEN[1]**	**PCI Command/Byte Enable Signal (Active-Low).**
61	-	**VSS**	**Ground.**
62	I/O	**PCI_AD[15]**	**PCI Address/Data Bit.**

5.4 FW323 IEEE 1394 Controller

Pin	Type	Symbol	Description
63	I/O	**PCI_AD[14]**	**PCI Address/Data Bit.**
64	I/O	**PCI_AD[13]**	**PCI Address/Data Bit.**
65	I/O	**PCI_AD[12]**	**PCI Address/Data Bit.**
66	-	**VSS**	**Ground.**
67	I/O	**PCI_AD[11]**	**PCI Address/Data Bit.**
68	I/O	**PCI_AD[10]**	**PCI Address/Data Bit.**
69	I/O	**PCI_AD[9]**	**PCI Address/Data Bit.**
70	I/O	**PCI_AD[8]**	**PCI Address/Data Bit.**
71	-	**VSS**	**Ground.**
72	-	**VDD**	**Power.**
73	I/O	**PCI_CBEN[0]**	**PCI Command/Byte Enable Signal (Active-Low).**
74	I/O	**PCI_AD[7]**	**PCI Address/Data Bit.**
75	I/O	**PCI_AD[6]**	**PCI Address/Data Bit.**
76	I/O	**PCI_AD[5]**	**PCI Address/Data Bit.**
77	-	**VSS**	**Ground.**
78	I/O	**PCI_AD[4]**	**PCI Address/Data Bit.**
79	I/O	**PCI_AD[3]**	**PCI Address/Data Bit.**
80	I/O	**CPI_AD[2]**	**PCI Address/Data Bit.**
81	-	**VSS**	**Ground.**
82	-	**VDD**	**Power.**
83	I/O	**PCI_AD[1]**	**PCI Address/Data Bit.**
84	I/O	**PCI_AD[0]**	**PCI Address/Data Bit.**
85	-	**PCI_VIOS**	**PCI Signaling Indicator.** (5V or 3.3V)
86	I	**CONTENDER**	**Contender.** On hardware reset, this input sets the default value of the CONTERDER bit indicated during self-ID. This bit can be programmed by tying the signal to VDD (high) or to ground (low).
87	I	**PC2`**	**Power-Class Indicators.** On hardware rest, these inputs set the default value of the power class indicated during self-ID. These bits can be programmed by tying these signals to VDD (high) or to ground (low).
88		**PC1**	
89		**PC0**	
90	O	**LKON**	**Link On.** Signal from the internal PHY core to the internal link core. This signal is provided as an output for use in legacy power management systems.
91	O	**LPS**	**Link Power Status.** Signal from the internal link core to the internal PHY core. LPS is provided as an output for use in legacy power management systems.
92	-	**NC**	**No Connect.**
93	-	**VDD**	**Power.**

Pin	Type	Symbol	Description
94	I	**CPS**	**Cable Power Status.** CPS is normally connected to the cable power through a 400K resistor. This circuit drives an internal comparator that detects the presence of cable power. This information is maintained in one internal register and is available to the LLC by way of a register read.
95	-	**VSSA**	**Analog Circuit Ground.** All VSSA signals should be tied together to a low-impedance ground plane.
96	-	**VDDA**	**Analog Circuit Power.** VDDA supplies power to the analog portion of the device.
97	Analog I/O	**TPB2-**	**Port 2, Port Cable Pair B.** TPB2± is the port B connection to the twisted-pair cable. Board traces from each pair of positive and negative differential signal pins should be kept matched and as short as possible to the external load resistors and to the cable connector.
98		**TPB2+**	
99	Analog I/O	**TPA2-**	**Port 2, Port Cable Pair A.** TPA2± is the port A connection to the twisted-pair cable. Board traces from each pair of positive and negative differential signal pins should be kept matched and as short as possible to the external load resistors and to the cable connector.
100		**TPA2+**	
101	Analog I/O	**TPBIAS2**	**Port2, Twisted-Pair Bias.** TPBIAS2 provides the 1.86V nominal bias voltage needed for proper operation of the twisted-pair cable drivers and receivers and for sending a valid cable connection signal to the remote nodes.
102	-	**VSSA**	**Analog Circuit Ground.** All VSSA signals should be tied together to a low-impedance ground plane.
103	-	**VSSA**	**Analog Circuit Ground.** All VSSA signals should be tied together to a low-impedance ground plane.
104	-	**VDDA**	**Analog Circuit Power.** VDDA supplies power to the analog portion of the device.
105	Analog I/O	**TPB1-**	**Port 1, Port Cable Pair B.** TPB1± is the port B connection to the twisted-pair cable. Board traces from each pair of positive and negative differential signal pins should be kept matched and as short as possible to the external load resistors and to the cable connector.
106		**TTPB1+**	
107	Analog I/O	**TPA1-**	**Port 1, Port Cable Pair A.** TPA1± is the port A connection to the twisted-pair cable. Board traces from each pair of positive and negative differential signal pins should be kept matched and as short as possible to the external load resistors and to the cable connector.
108		**TPA1+**	

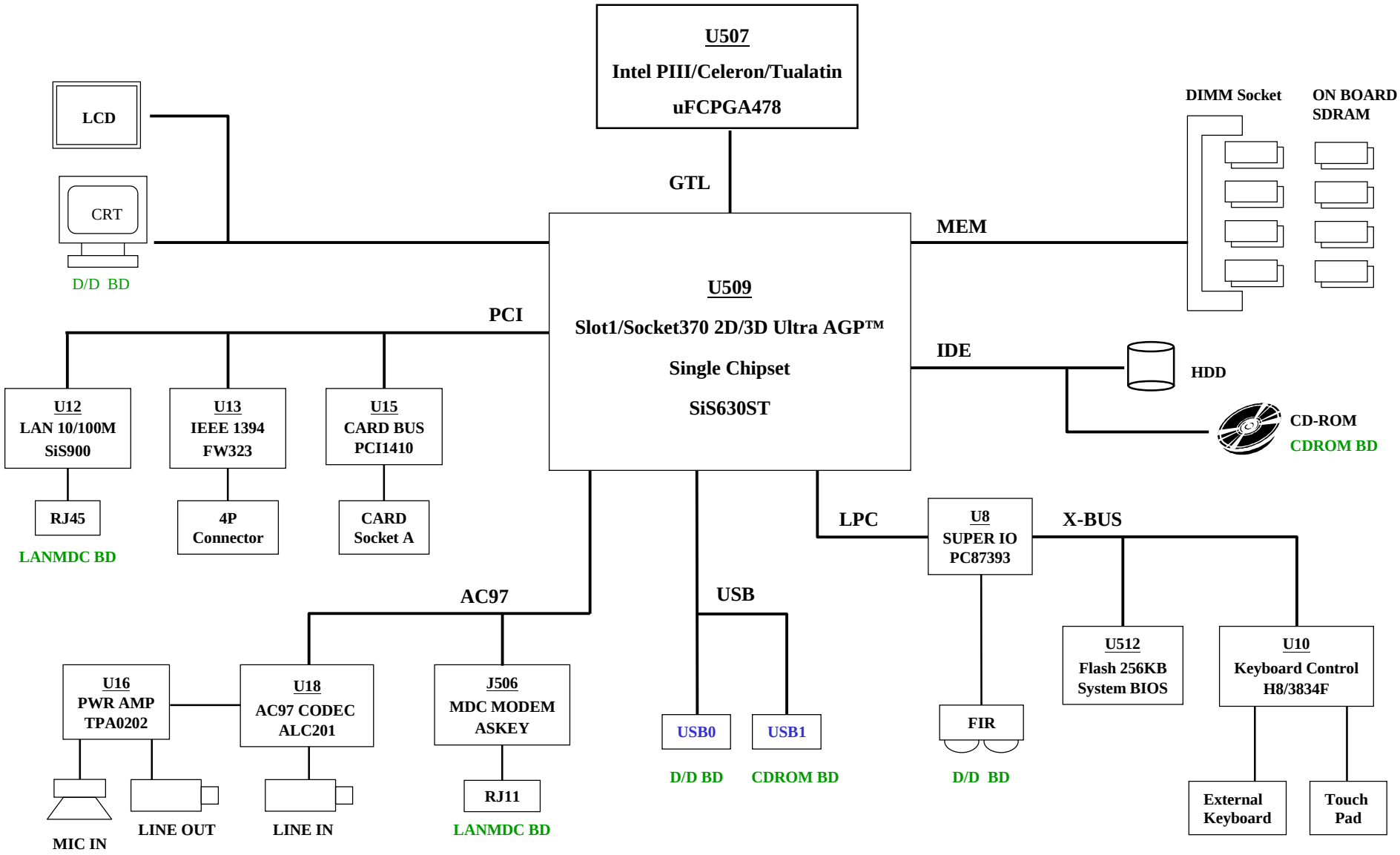
5.4 FW323 IEEE 1394 Controller

Pin	Type	Symbol	Description
109	Analog I/O	**TPBIAS1**	**Port1, Twisted-Pair Bias.** TPBIAS1 provides the 1.86V nominal bias voltage needed for proper operation of the twisted-pair cable drivers and receivers and for sending a valid cable connection signal to the remote nodes.
110	Analog I/O	**TPB0-**	**Port 0, Port Cable Pair B.** TPB0± is the port B connection to the twisted-pair cable. Board traces from each pair of positive and negative differential signal pins should be kept matched and as short as possible to the external load resistors and to the cable connector.
111		**TPB0+**	
112	Analog I/O	**TPA0-**	**Port 0, Port Cable Pair A.** TPA0± is the port A connection to the twisted-pair cable. Board traces from each pair of positive and negative differential signal pins should be kept matched and as short as possible to the external load resistors and to the cable connector.
113		**TPA0+**	
114	Analog I/O	**TPBIAS0**	**Port0, Twisted-Pair Bias.** TPBIAS0 provides the 1.86V nominal bias voltage needed for proper operation of the twisted-pair cable drivers and receivers and for sending a valid cable connection signal to the remote nodes
115	-	**VSSA**	**Analog Circuit Ground.** All VSSA signals should be tied together to a low-impedance ground plane.
116	-	**VDDA**	**Analog Circuit Power.** VDDA supplies power to the analog portion of the device.
117	I	**R0**	**Current Setting Resistor.** An internal reference voltage is applied to a resistor connected between R0 and R1 to set the operating current and the cable driver output current. A low temperature-coefficient resistor (TCR) with a value of 2.49K±1% should be used to meet the IEEE 1394-1995 standard requirements for output voltage limits.
118		**R1**	

Pin	Type	Symbol	Description
119	-	**PLLVDD**	**Power for PLL Circuit.** PLLVDD supplies power to the PLL circuitry portion of the device.
120	-	**PLLVSS**	**Ground for PLL Circuit.** PLLVSS is tied to a low impedance ground plane.
121	-	**XI**	**Crystal Oscillator.** XI and XO connect to a 24.576 MHz parallel resonant fundamental mode crystal. Although when a 24.576 MHz clock source is used, it can be connected to XI with XO left unconnected. The optimum values for the external shunt capacitors are dependent on the specifications of the crystal used. The suggested values of 12 pF are appropriate for crystal with 7 pF specified loads.
122		**XO**	
123	I	**RESETN**	**Reset (Active-Low).** When RESETN is asserted low (active), a bus reset condition is set on the active cable ports and the internal PHY core logic is reset to the reset start state. An internal pull-up resistor, which is connected to VDD, is provided, so only an external delay capacitor and resistor are required. This input is a standard logic buffer and can also be driven by an open-drain logic output buffer.
124	I	**PTEST**	**Test.** Used for device testing. Tie to VSS.
125	I	**SM**	**Test Mode Control.** SM is used during the manufacturing test and should be tied to VSS.
126	I	**SE**	**Test Mode Control.** SE is used during the manufacturing test and should be tied to VSS.
127	-	**NC**	**No Connect.**
118	-	**NC**	**No Connect.**

M762 N/B Maintenance

6. System Block Diagram



7. Maintenance Diagnostics

7.1 Introduction

Each time the computer is turned on ,the system BIOS runs a series of internal checks on the hardware. This power-on self test (post) allows the computer to detect problems as early as the power-on stage. Error messages of post can alert you to the problems of your computer.

If an error is detected during these tests, you will see an error message displayed on the screen. If the error occurs before the display, then the screen cannot display the error message. Error codes or system beeps are used to identify a post error that occurs when the screen is not available.

The value for the diagnostic port (3F8H) is written at the beginning of the test. Therefore , if the test fail, the user can determine where the problem occurs by reading the last value written to post 3F8H by the especial debug card plug at SIO port. But for the model which does not support SIO port , considering designing for mechanism, as M762, debug card could not directly be used. User must connect the each pin of the especial debug card to the appropriate COM1 signal by using cable, and then get the proper message from debug card to identify a post error.

7.2 Error Codes

Following is a list of error codes in sequent display on the PIO debug board.

Code	POST Routine Description
10h	Some type of long reset
11h	Turn off FAST A20 for POST
12h	Signal power on reset
13h	Initialize the chipset
14h	Search for ISA Bus VGA adapter
15h	Reset counter / Timer 1
16h	User register config through CMOS
17h	Sizememory
18h	Dispatch to RAM test
19h	Check sum the ROM
1Ah	Reset PIC's
1Bh	Initialize video adapter(s)
1Ch	Initialize video (6845Regs)
1Dh	Initialize color adapter
1Eh	Initialize monochrome adapter
1Fh	Test 8237A page registers

Code	POST Routine Description
20h	Test keyboard
21h	Test keyboard controller
22h	Check if CMOS RAM valid
23h	Test battery fail & CMOS X-SUM
24h	Test the DMA controller
25h	Initialize 8237A controller
26h	Initialize int vectors
27h	RAM quick sizing
28h	Protected mode entered safely
29h	RAM test completed
2Ah	Protected mode exit successful
2Bh	Setup shadow
2Ch	Going to initialize video
2Dh	Search for monochrome adapter
2Eh	Search for color adapter
2Fh	Signon messages displayed

7.2 Error Codes

Following is a list of error codes in sequent display on the PIO debug board.

Code	POST Routine Description
30h	Special init of keyboard ctlr
31h	Test if keyboard Present
32h	Test keyboard Interrupt
33h	Test keyboard command byte
34h	Test, blank and count all RAM
35h	Protected mode entered safely(2)
36h	RAM test complete
37h	Protected mode exit successful
38h	Update output port
39h	Setup cache controller
3Ah	Test if 18.2Hz periodic working
3Bh	Test for RTC ticking
3Ch	Initialize the hardware vectors
3Dh	Search and init the mouse
3Eh	Update NUMLOCK status
3Fh	Special init of COMM and LPT ports

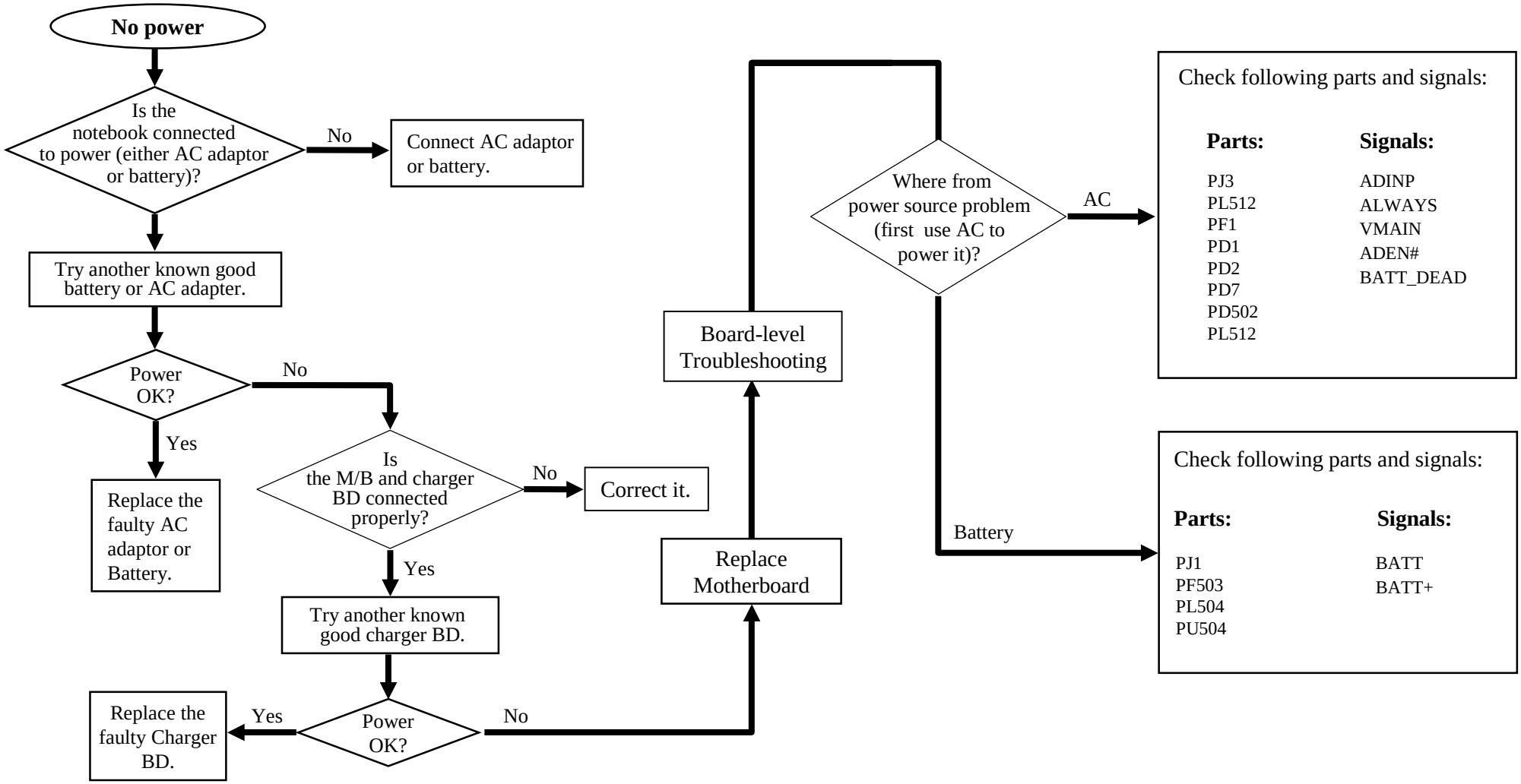
Code	POST Routine Description
40h	Configure the COMM and LPT ports
41h	Initialize the floppies
42h	Initialize the hard disk
43h	Initialize option ROMs
44h	OEM’s init of power management
45h	Update NUMLOCK status
46h	Test for coprocessor installed
47h	OEM functions before boot
48h	Dispatch to operate system boot
49h	Jump into bootstrap code
50h	ACPI init
51h	PM init & Geyserville
52h	USB HC init

8. Trouble Shooting

- 8.1 No Power
- 8.2 No Display
- 8.3 VGA Controller Failure LCD No Display
- 8.4 External Monitor No Display
- 8.5 Memory Test Error
- 8.6 Keyboard (K/B) Touch-Pad (T/P) Test Error
- 8.7 Hard Disk Driver Test Error
- 8.8 CD-ROM Driver Test Error
- 8.9 USB Port Test Error
- 8.10 Audio Failure
- 8.11 LAN Test Error
- 8.12 PC Card Slot Failure
- 8.13 IEEEE 1394 Failure

8.1 No Power

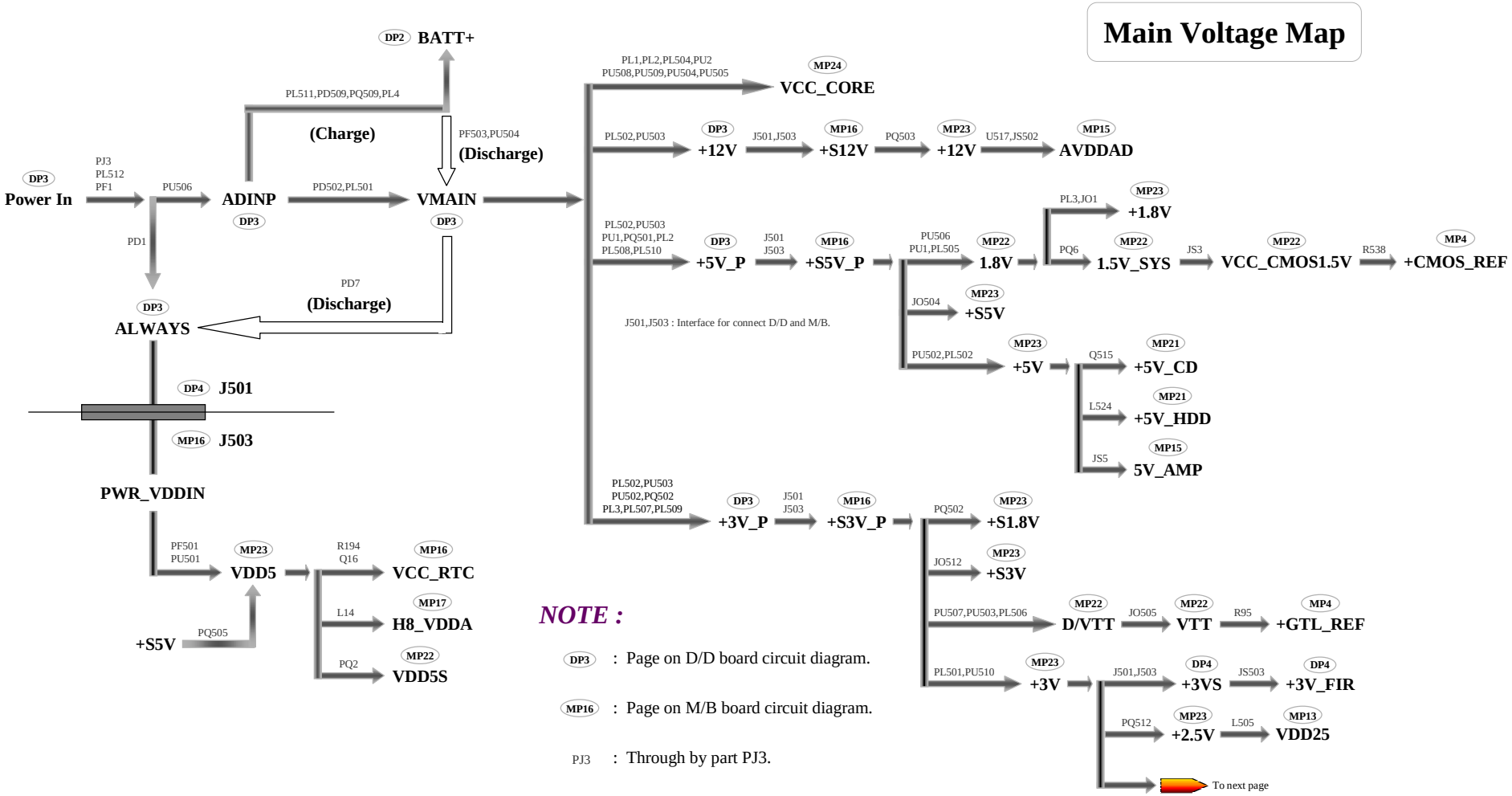
When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.



M762 N/B Maintenance

8.1 No Power

When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.

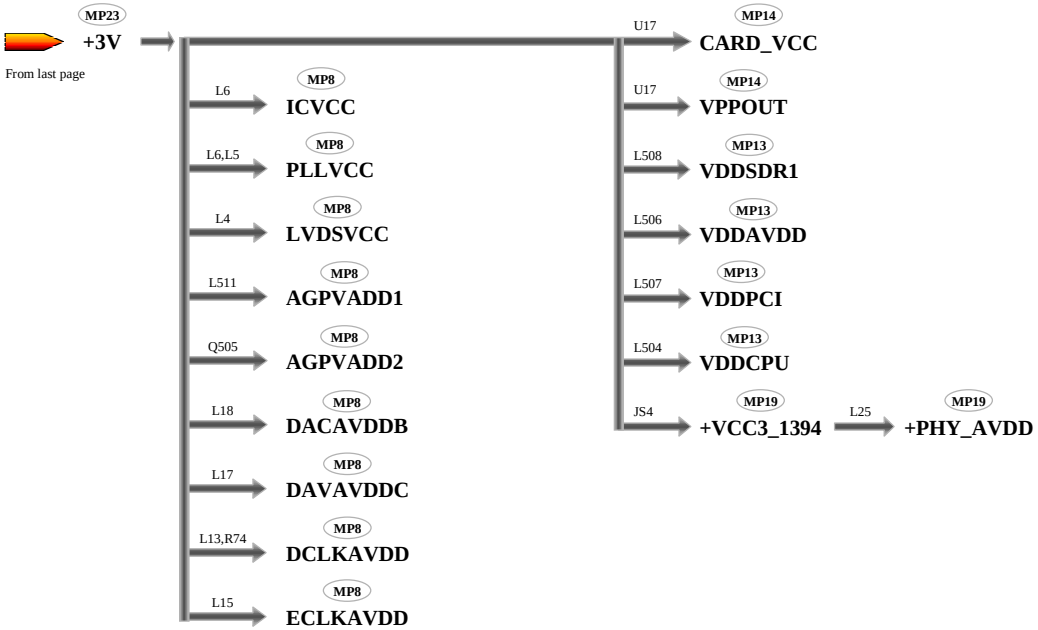


M762 N/B Maintenance

8.1 No Power

When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.

Main Voltage Map



M762 N/B Maintenance

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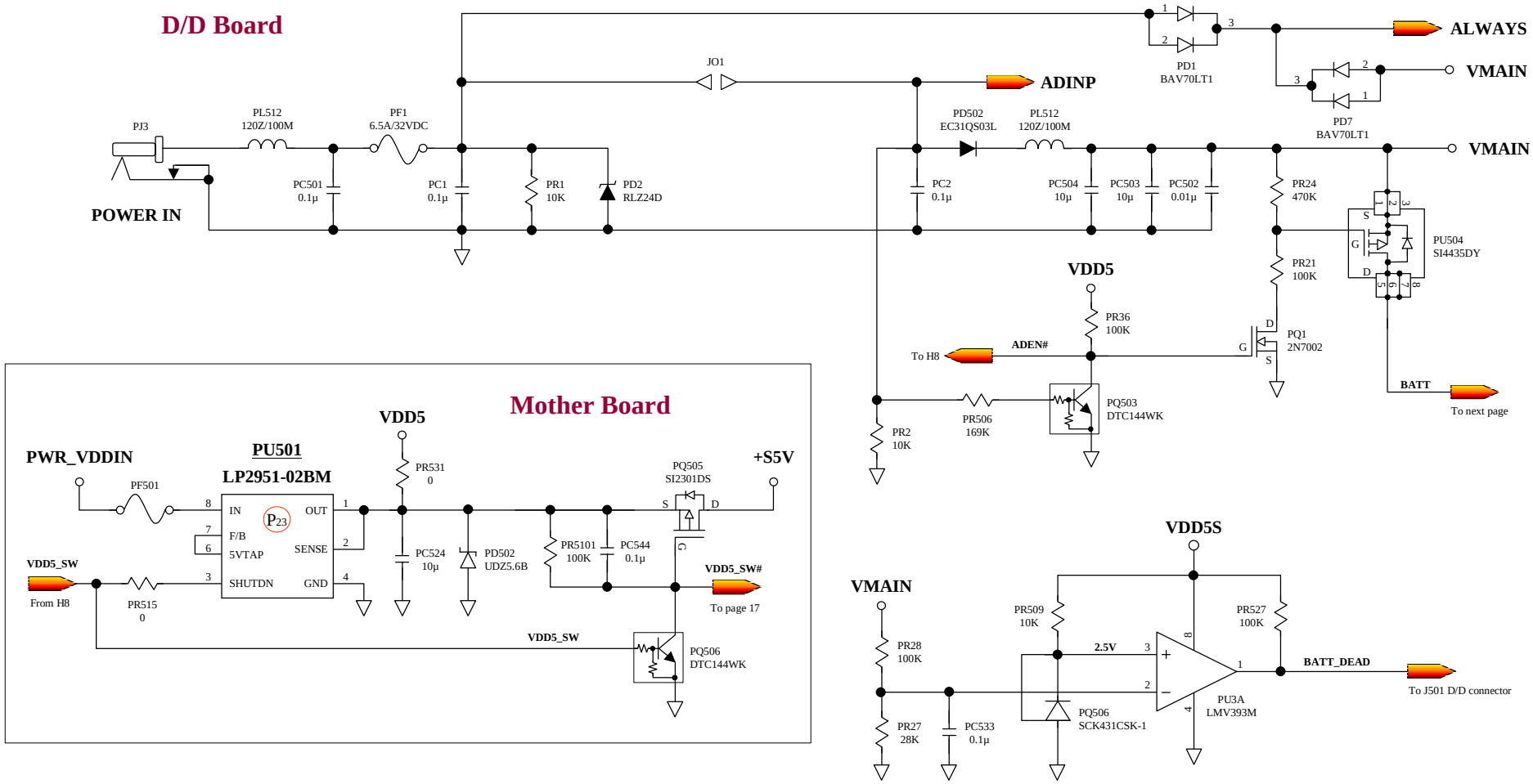
When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.



M762 N/B Maintenance

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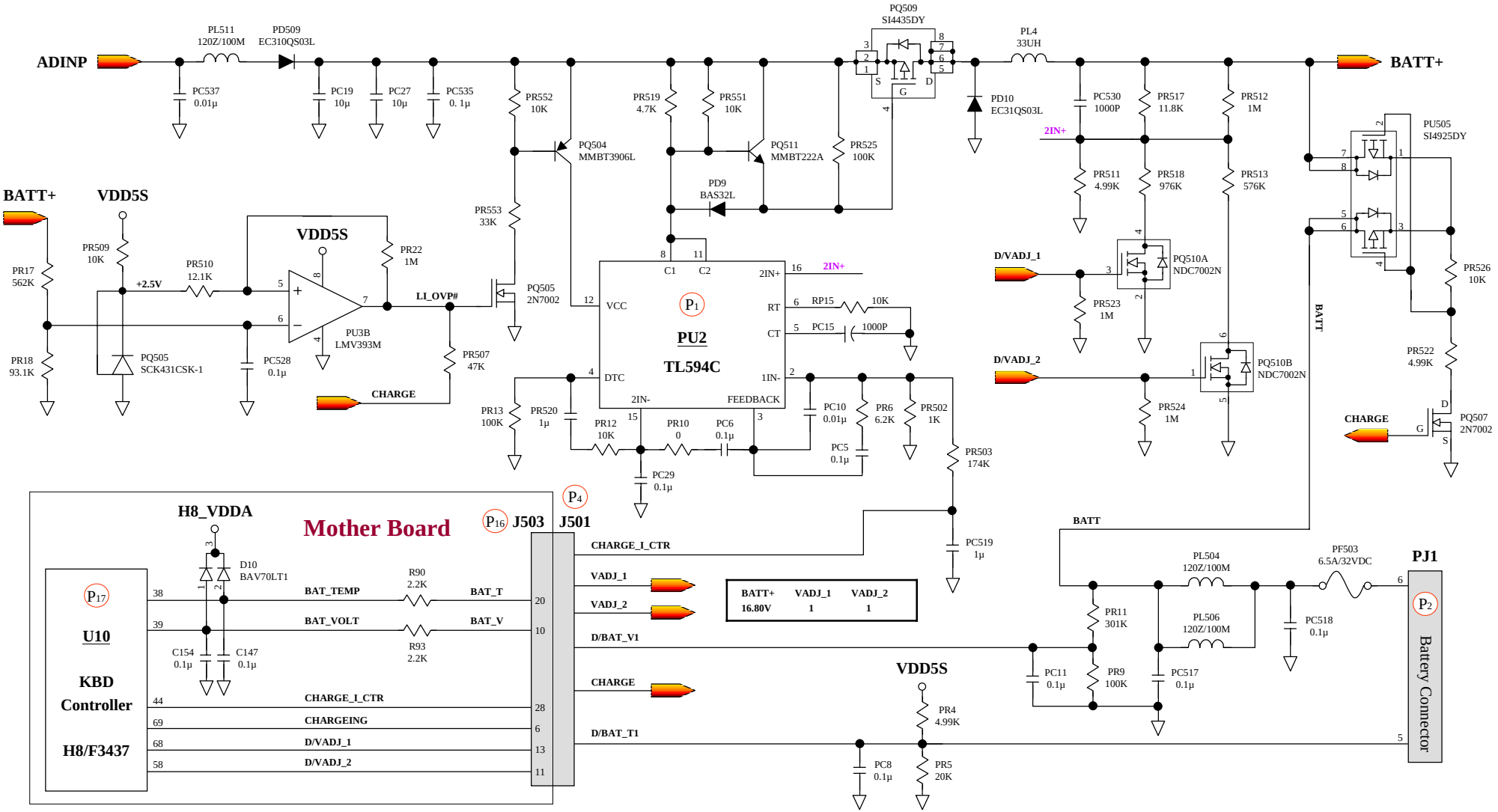
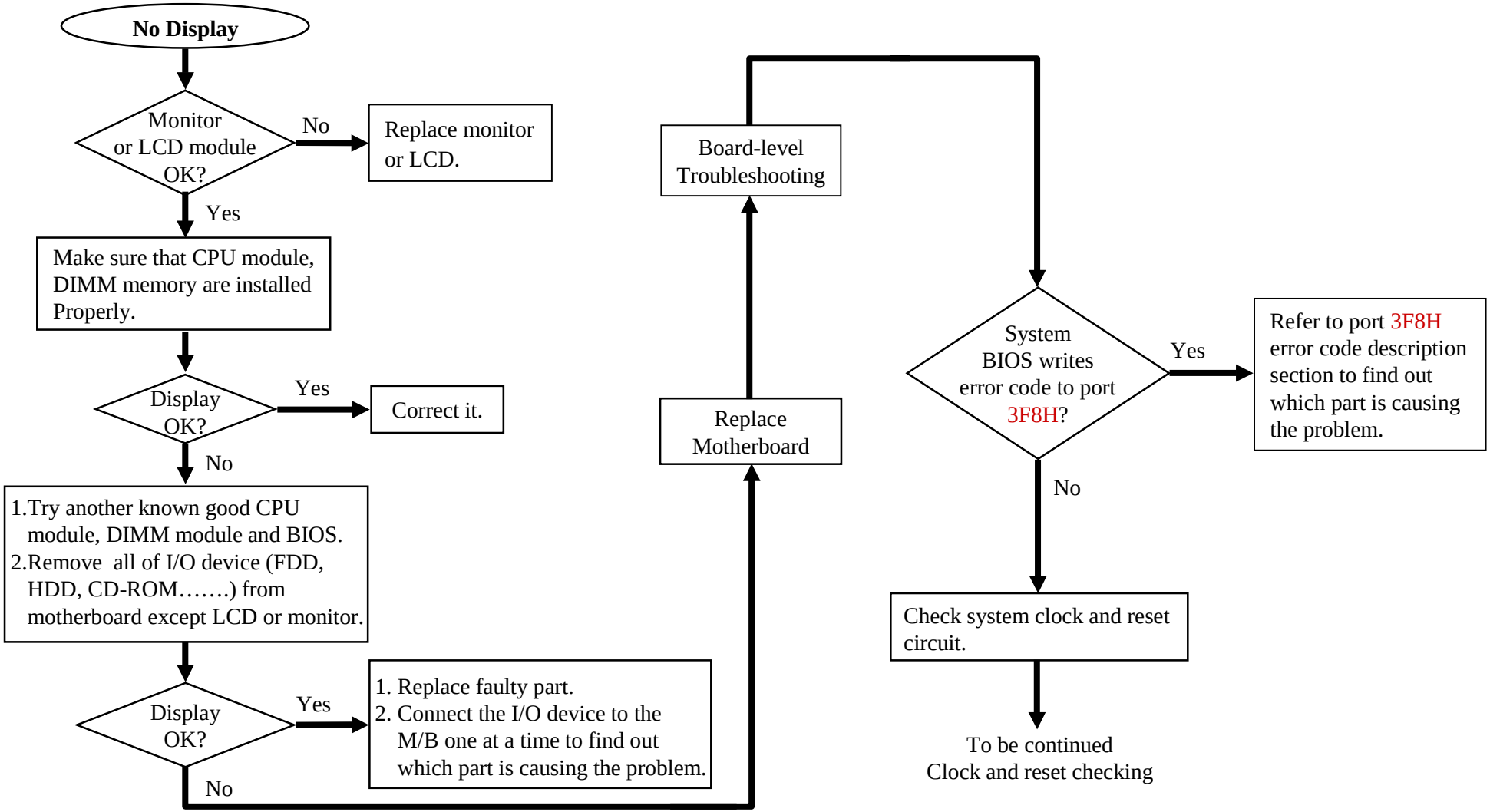
When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.



8.2 No Display

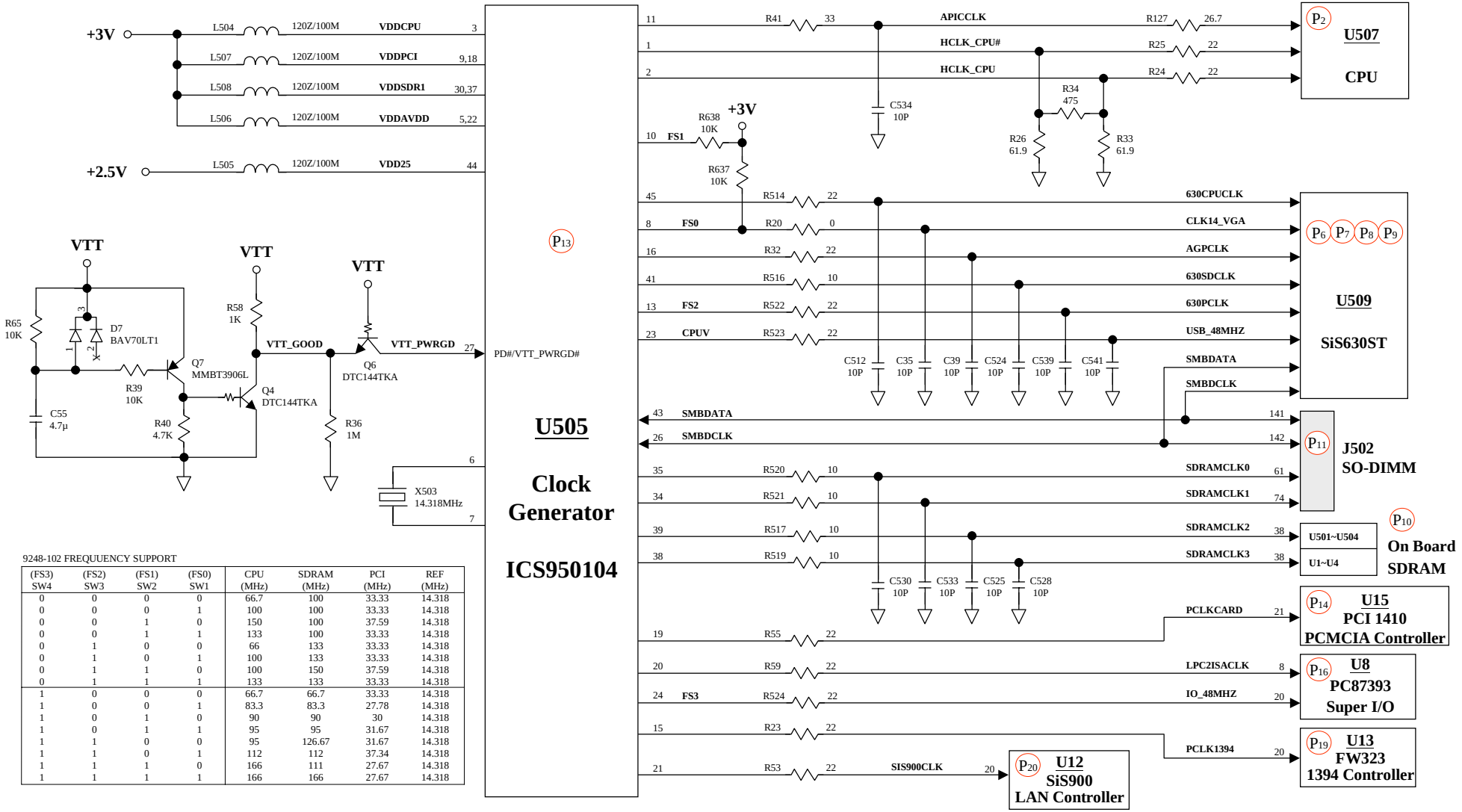
There is no display on both LCD and VGA monitor after power on although the LCD and monitor is known-good.



M762 N/B Maintenance

8.2 No Display

****** System Clock Check ******



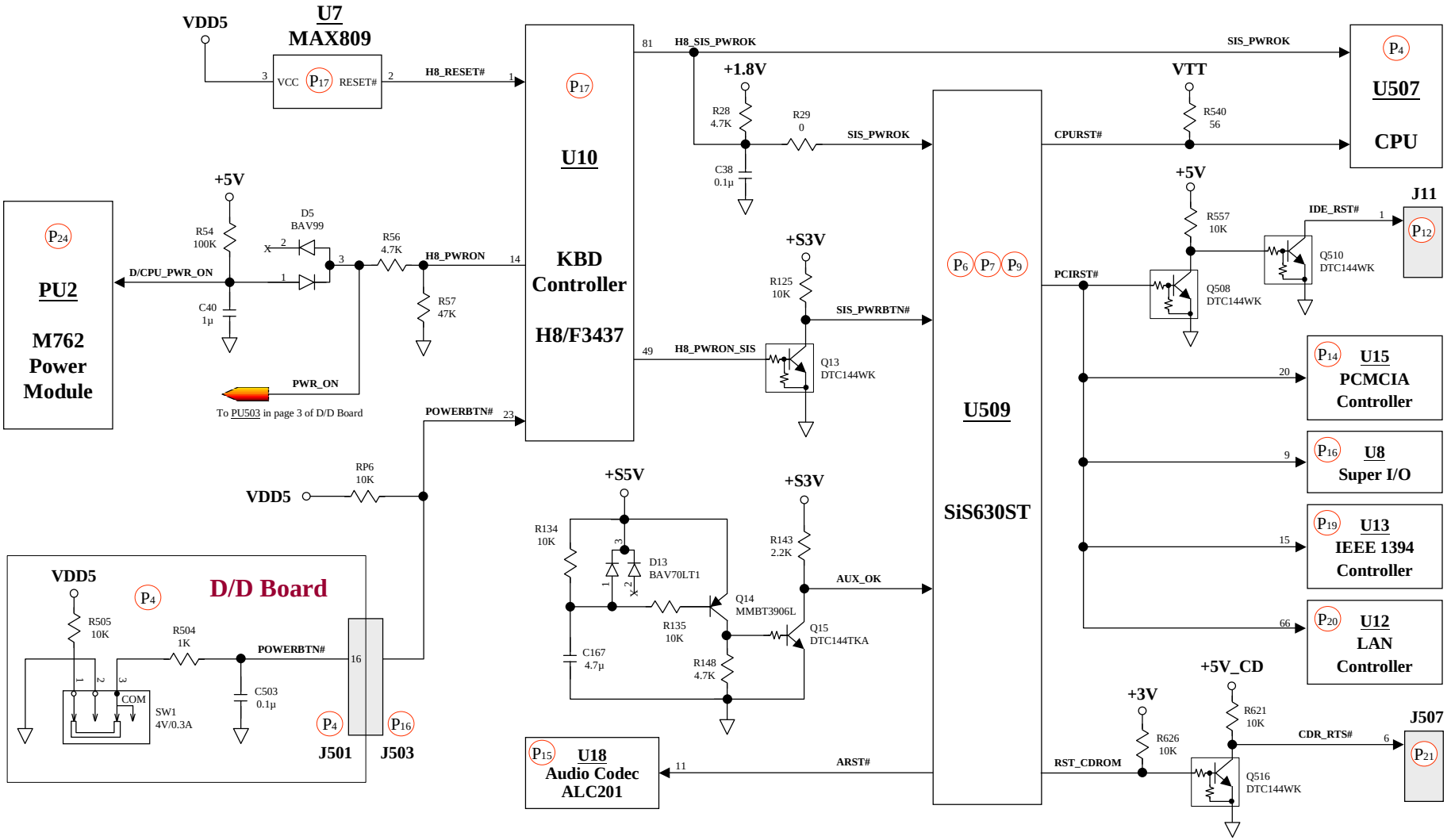
9248-102 FREQUUENCY SUPPORT

(FS3) SW4	(FS2) SW3	(FS1) SW2	(FS0) SW1	CPU (MHz)	SDRAM (MHz)	PCI (MHz)	REF (MHz)
0	0	0	0	66.7	100	33.33	14.318
0	0	0	1	100	100	33.33	14.318
0	0	1	0	150	100	37.59	14.318
0	0	1	1	133	100	33.33	14.318
0	1	0	0	66	133	33.33	14.318
0	1	0	1	100	133	33.33	14.318
0	1	1	0	100	150	37.59	14.318
0	1	1	1	133	133	33.33	14.318
1	0	0	0	66.7	66.7	33.33	14.318
1	0	0	1	83.3	83.3	27.78	14.318
1	0	1	0	90	90	30	14.318
1	0	1	1	95	95	31.67	14.318
1	1	0	0	95	126.67	31.67	14.318
1	1	0	1	112	112	37.34	14.318
1	1	1	0	166	111	27.67	14.318
1	1	1	1	166	166	27.67	14.318

M762 N/B Maintenance

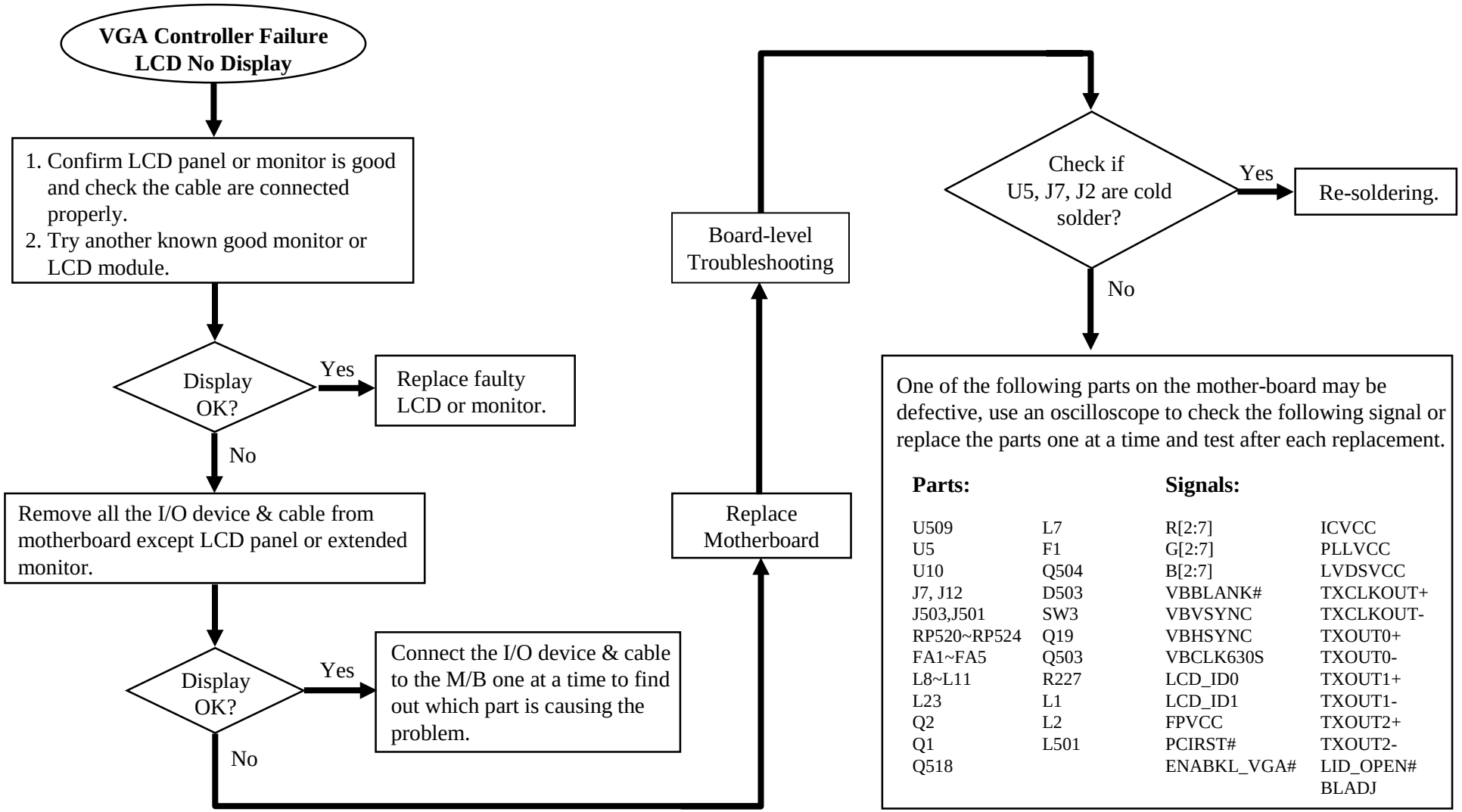
8.2 No Display

****** Power Good & Reset Circuit Check ******



8.3 VGA Controller Failure LCD No Display

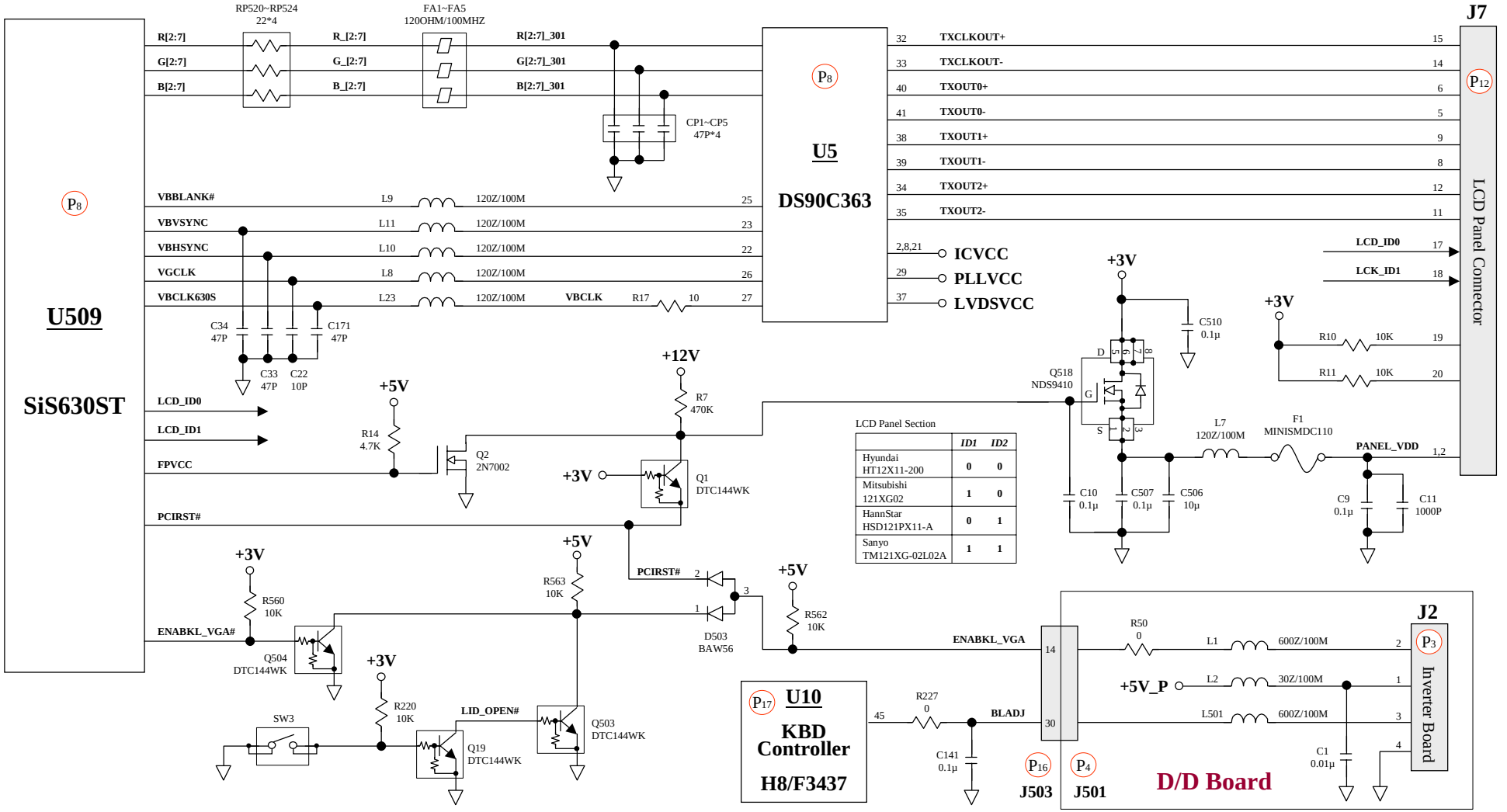
There is no display or picture abnormal on LCD although power-on-self-test is passed.



M762 N/B Maintenance

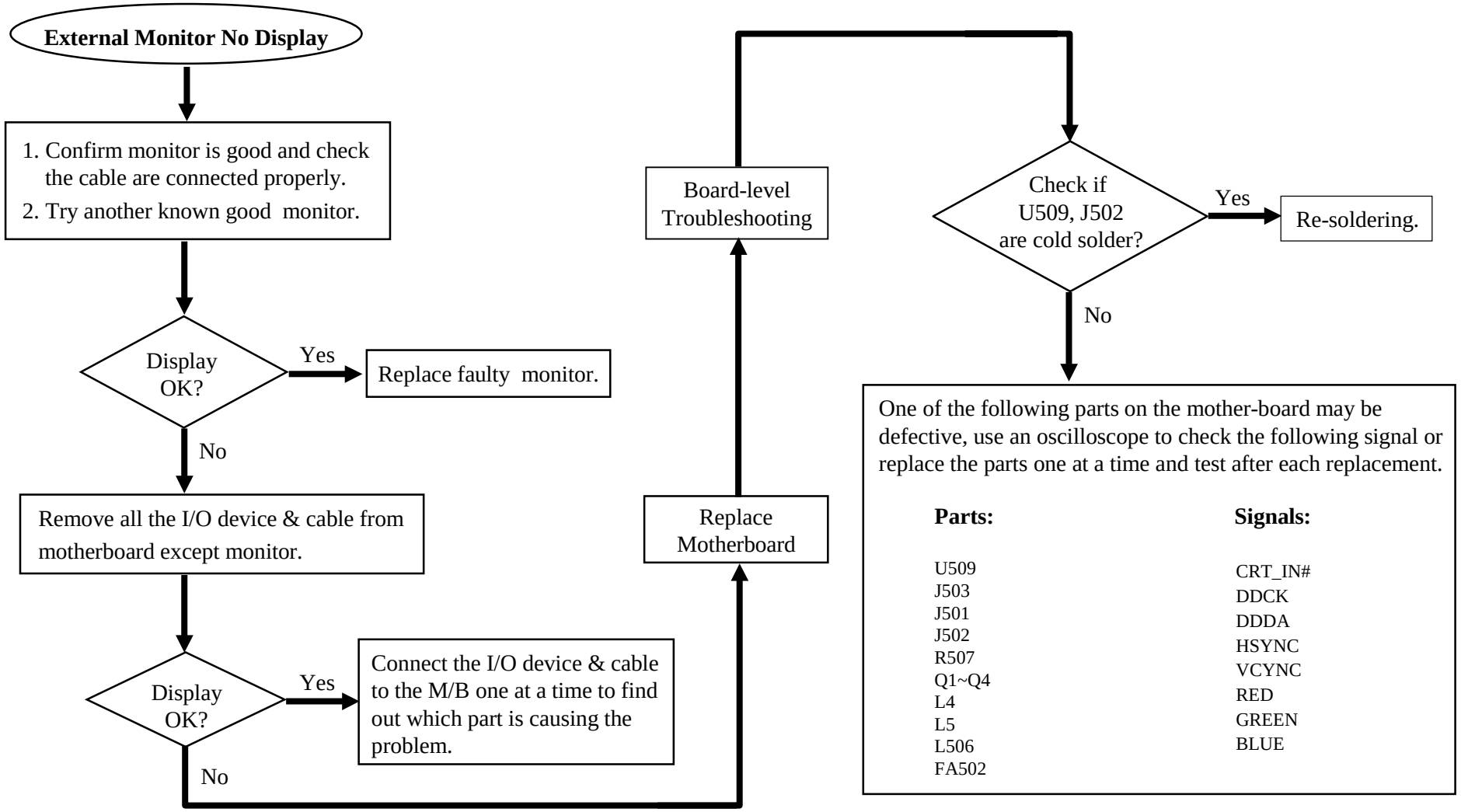
8.3 VGA Controller Failure LCD No Display

There is no display or picture abnormal on LCD although power-on-self-test is passed.



8.4 External Monitor No Display

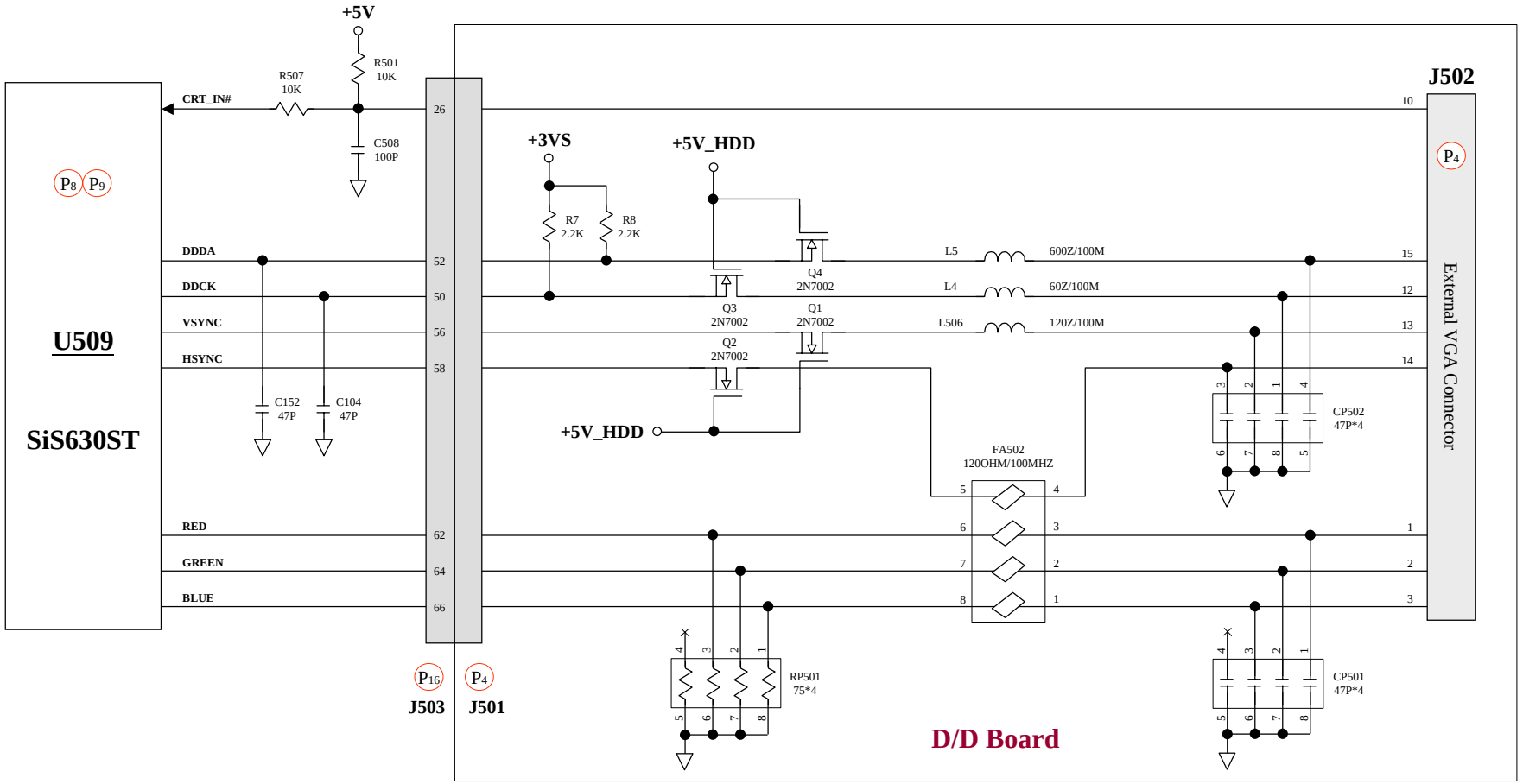
There is no display or picture abnormal on CRT monitor, but it is OK for LCD.



M762 N/B Maintenance

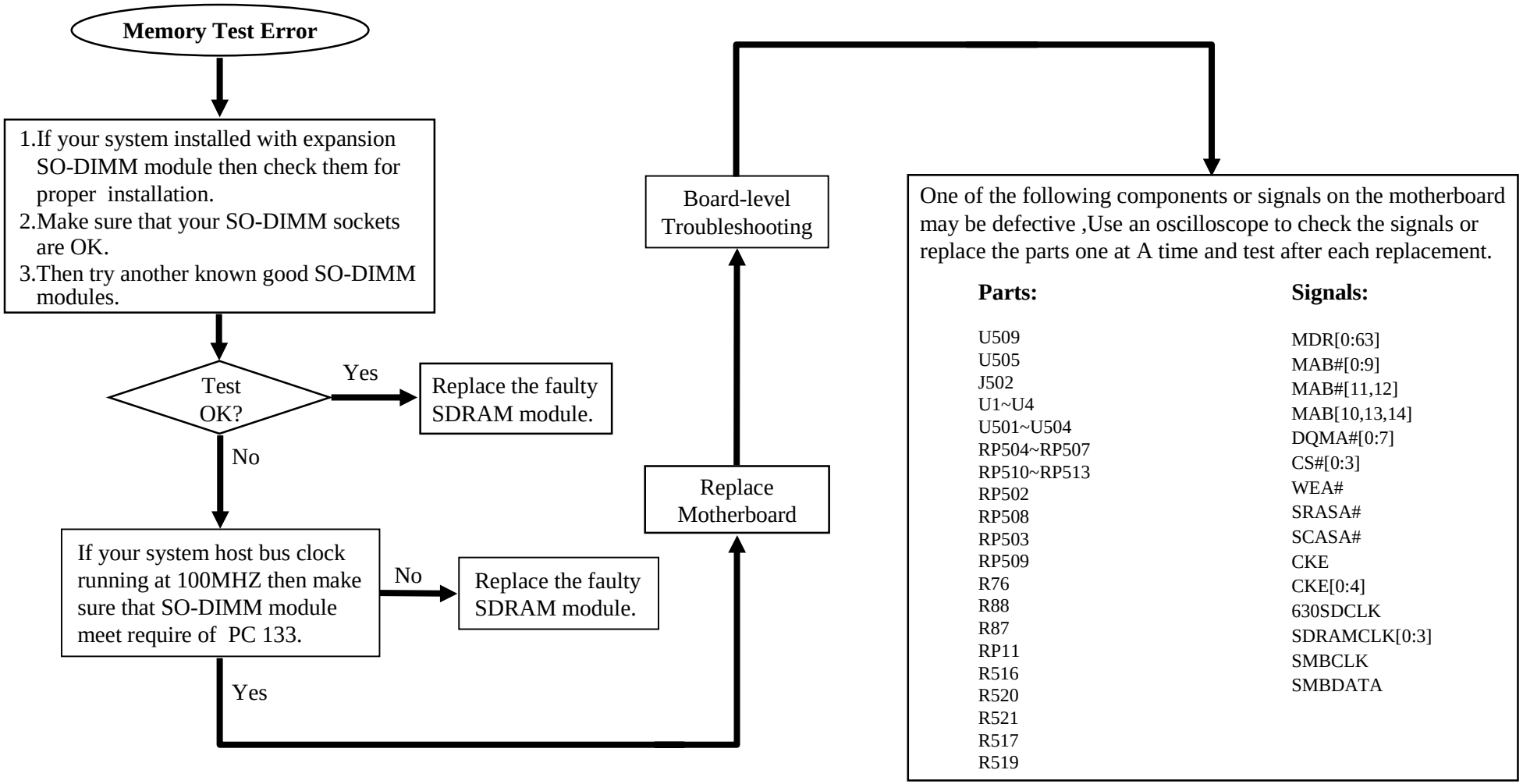
8.4 External Monitor No Display

There is no display or picture abnormal on CRT monitor, but it is OK for LCD.



8.5 Memory Test Error

Either on board or extend SDRAM is failure or system hangs up.



M762 N/B Maintenance

8.5 Memory Test Error

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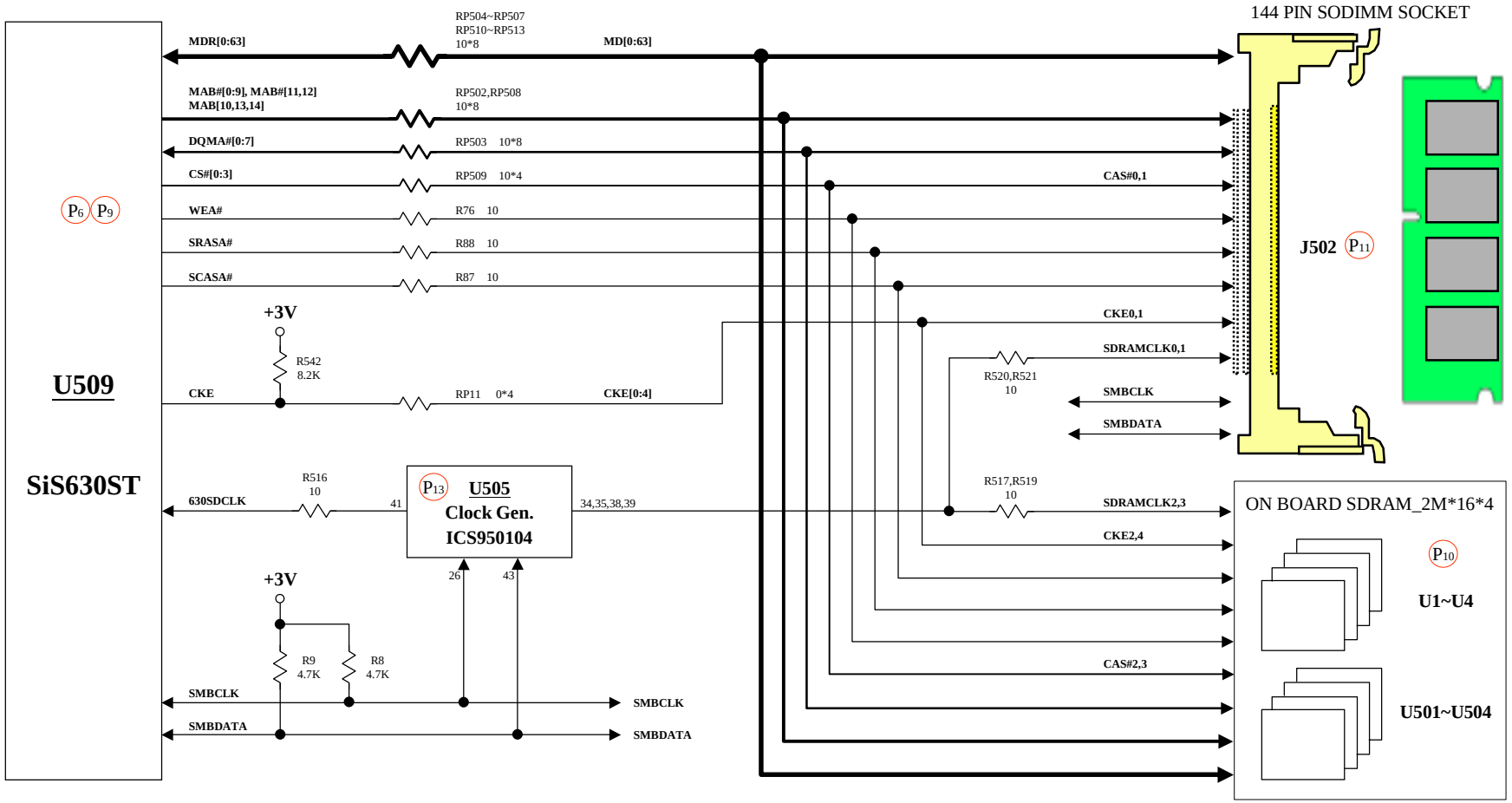
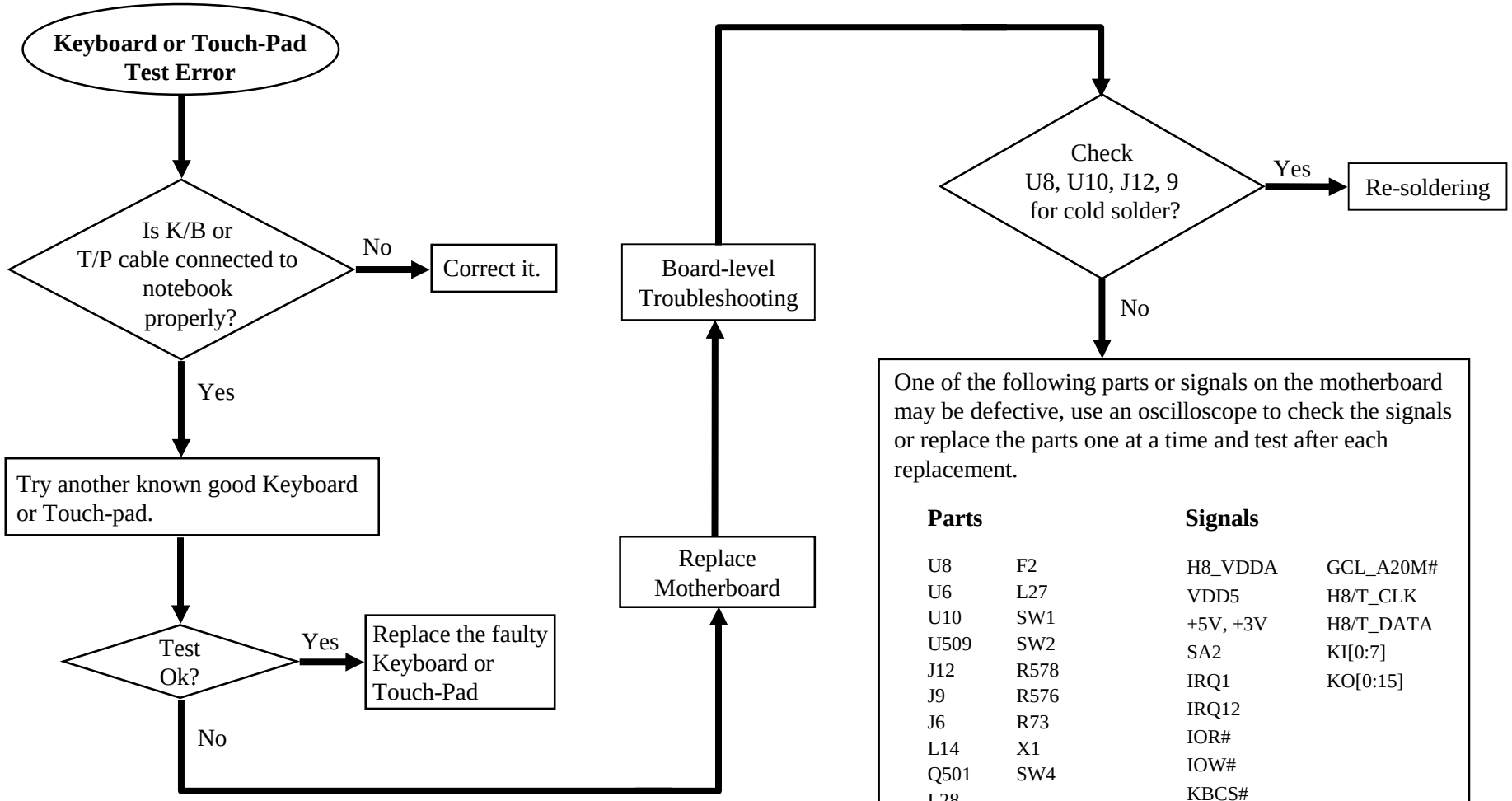


8.6 Keyboard (K/B) Touch-Pad (T/P) Test Error

Error message of keyboard or touch-pad failure is shown or any key does not work.



M762 N/B Maintenance

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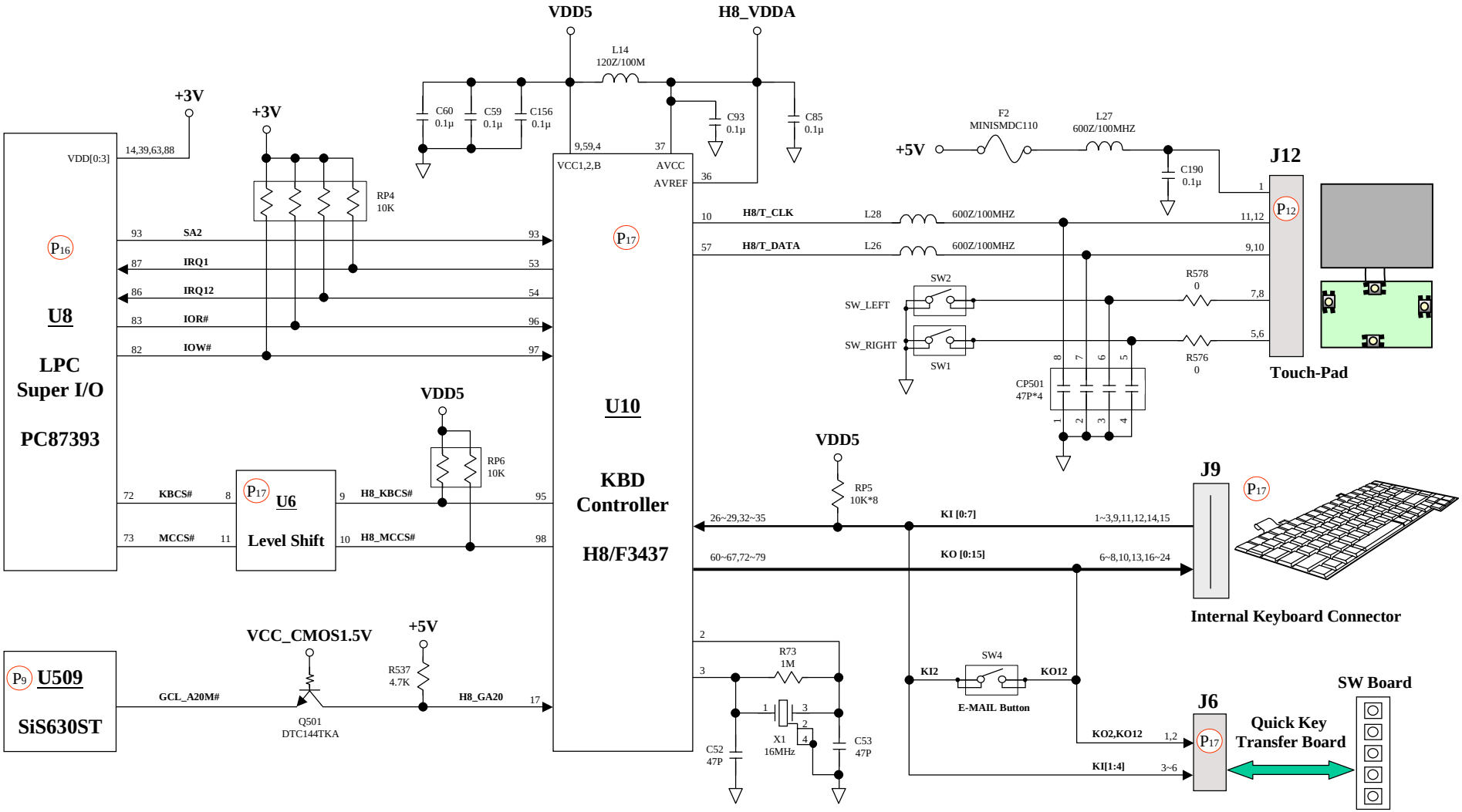
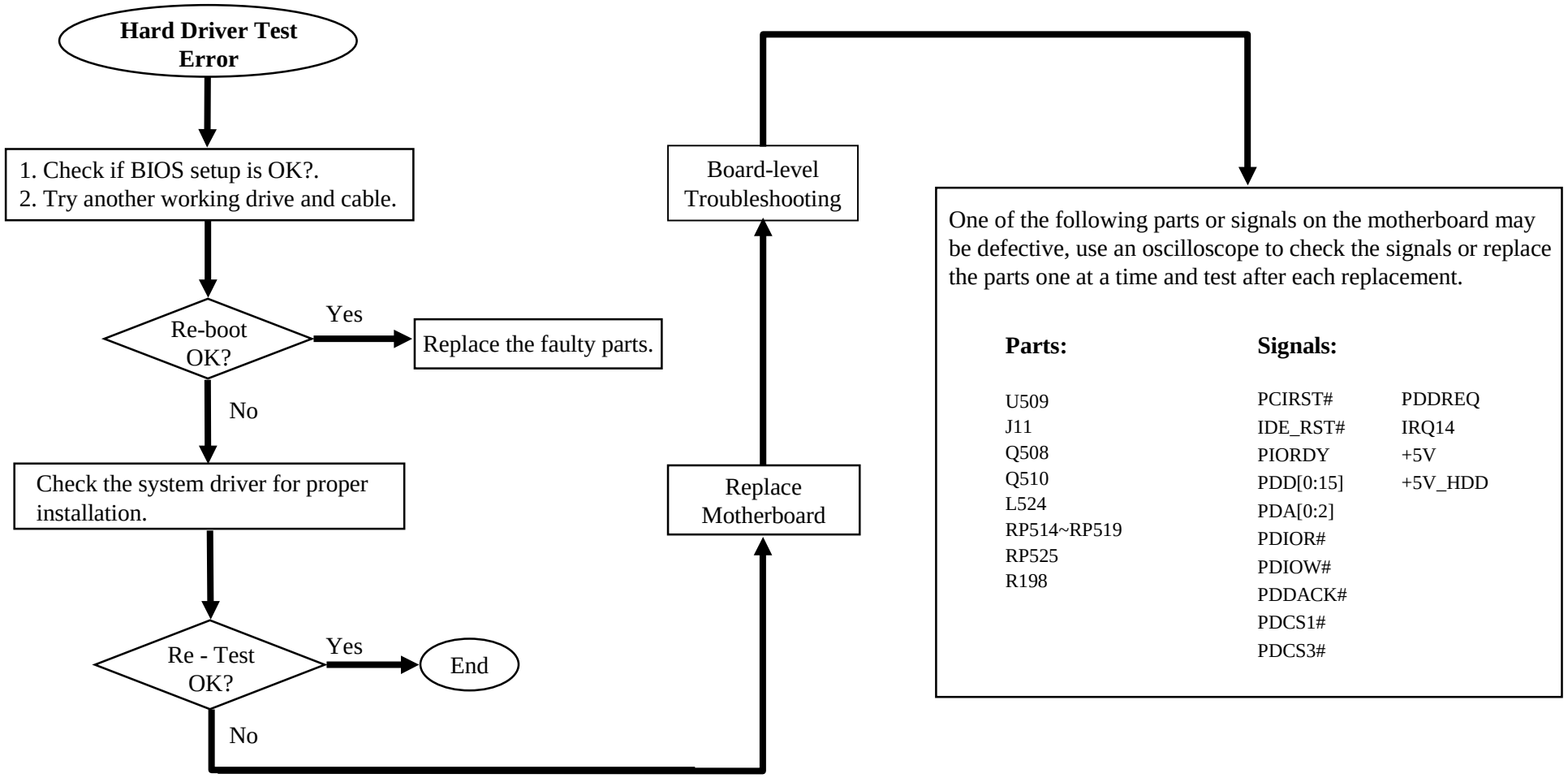
Error message of keyboard or touch-pad failure is shown or any key does not work.



8.7 Hard Disk Drive Test Error

Either an error message is shown, or the drive motor spins non-stop, while reading data from or writing data to hard disk.



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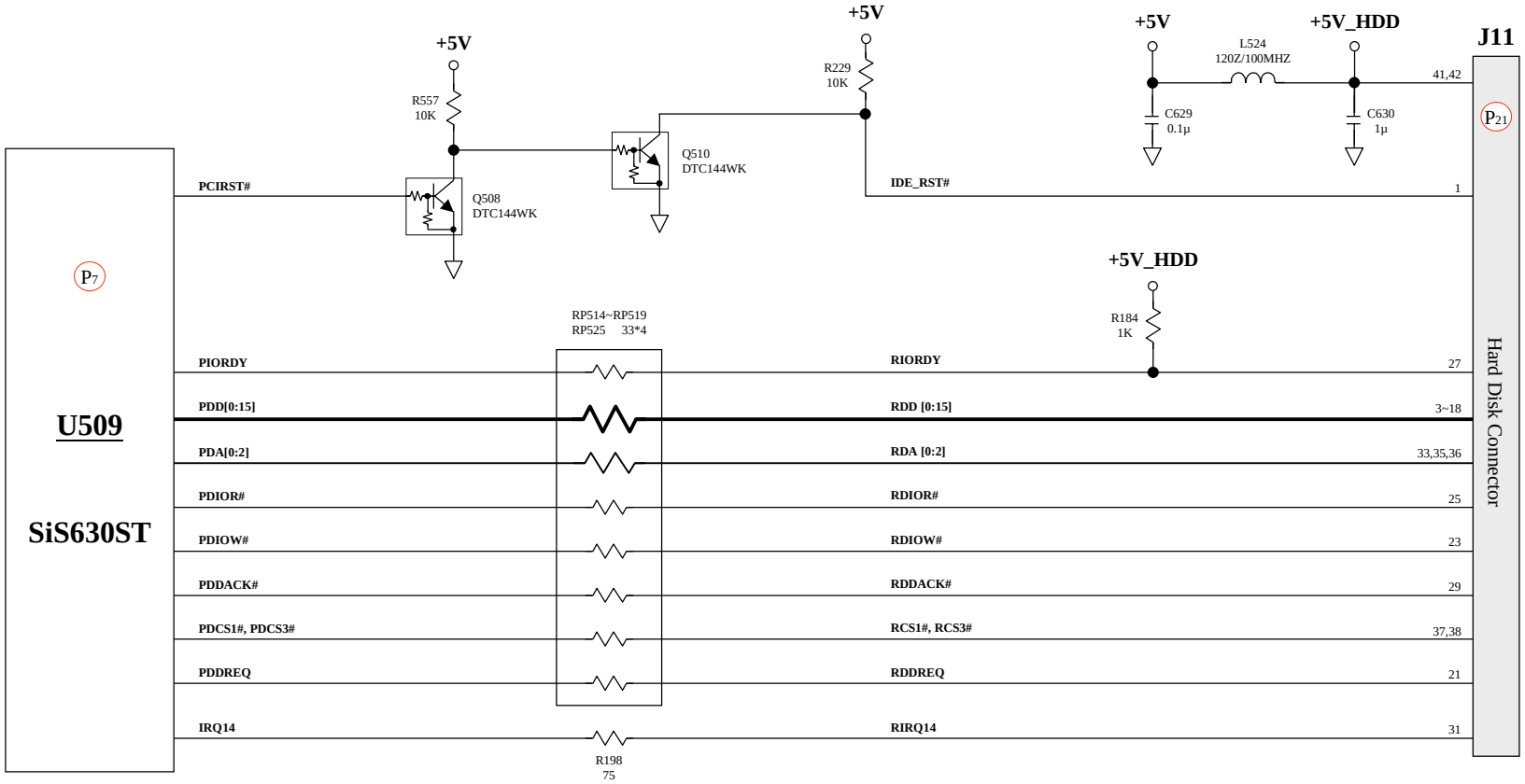
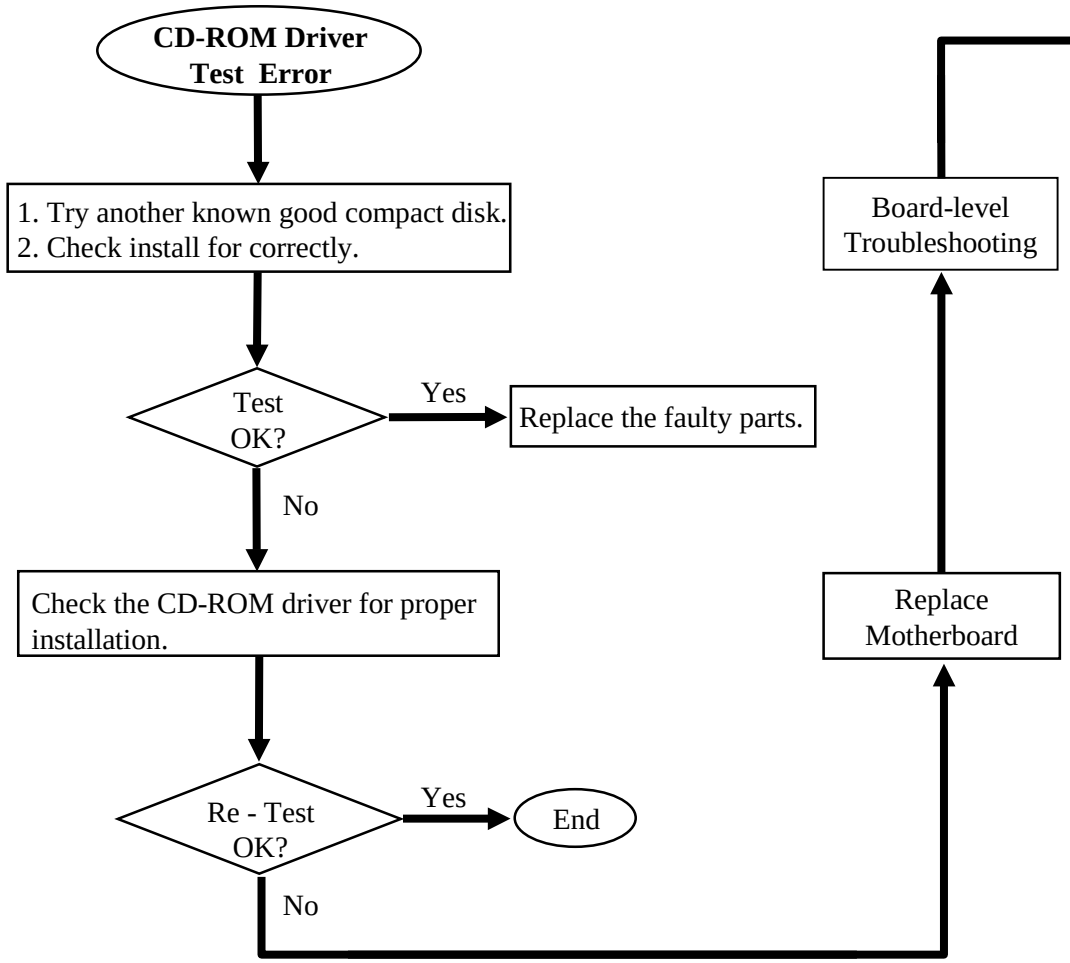
8.7 Hard Disk Drive Test Error

Either an error message is shown, or the drive motor spins non-stop, while reading data from or writing data to hard disk.



8.8 CD-ROM Drive Test Error

An error message is shown when reading data from CD-ROM drive.



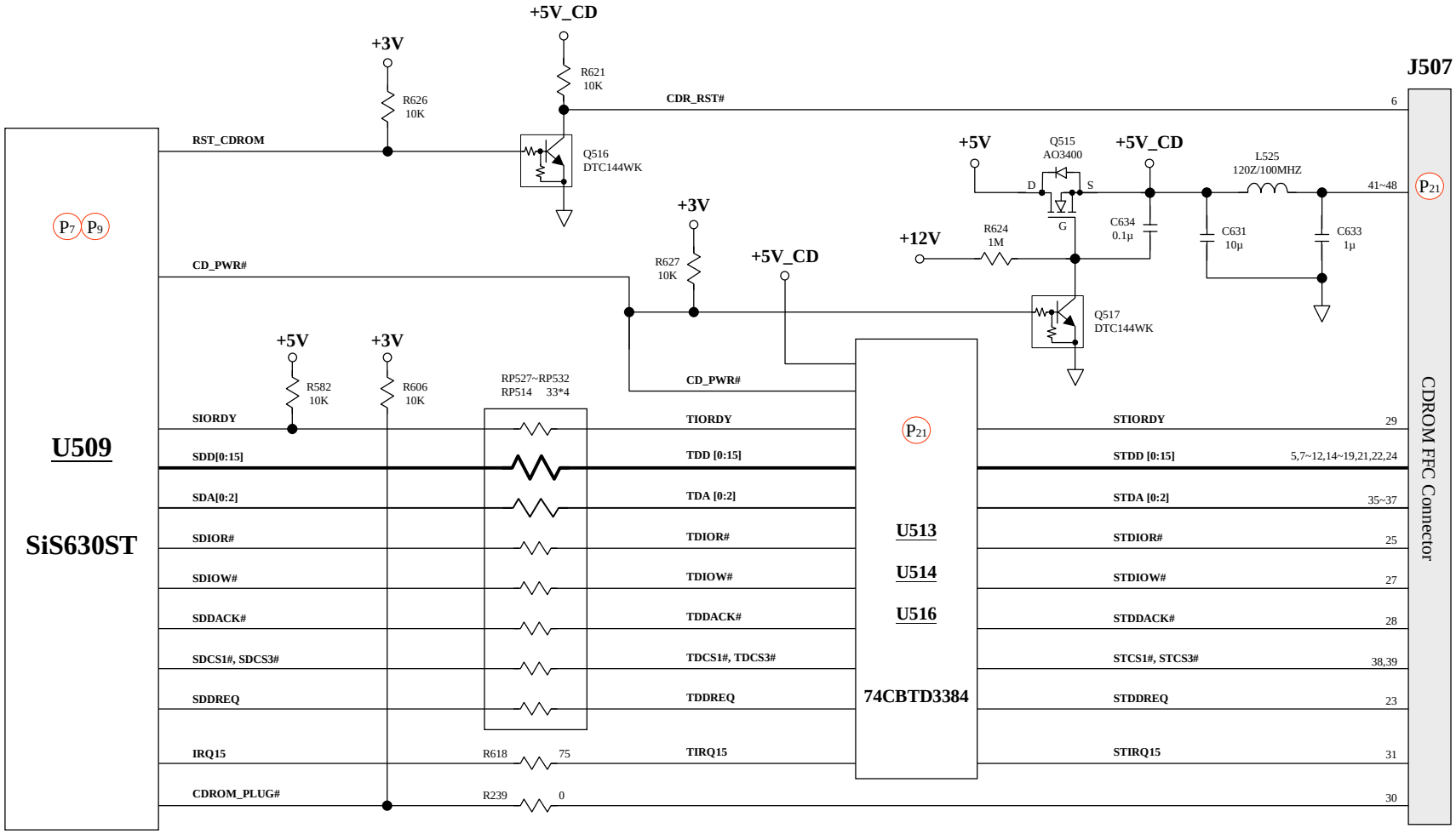
One of the following parts or signals on the motherboard may be defective, use an oscilloscope to check the signals or replace the parts one at a time and test after each replacement.

Parts:	**Signals:**
U509	RST_CDROM
J507	CDR_RST#
Q516	SIORDY
U513	SDD[0:15]
U514	SDA[0:2]
U516	SDIOR#
Q515	SDIOW#
Q517	SDDACK#
L525	SDCS1#
R624	SDCS3#
RP527~RP532	SDDREQ
RP514	IRQ15
R618	CDROM_PLUG#
R239	CD_PWR#
	+5V
	+5V_CD

M762 N/B Maintenance

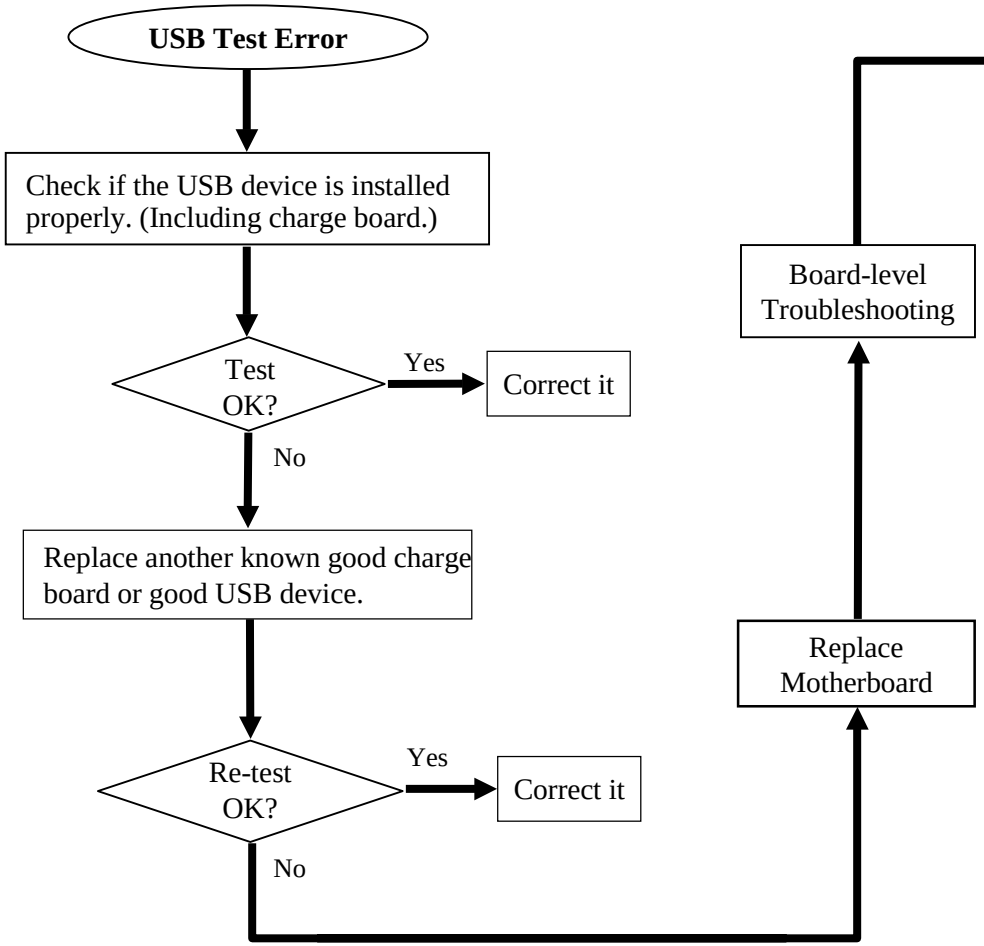
8.8 CD-ROM Drive Test Error

An error message is shown when reading data from CD-ROM drive.



8.9 USB Test Error

An error occurs when a USB I/O device is installed.



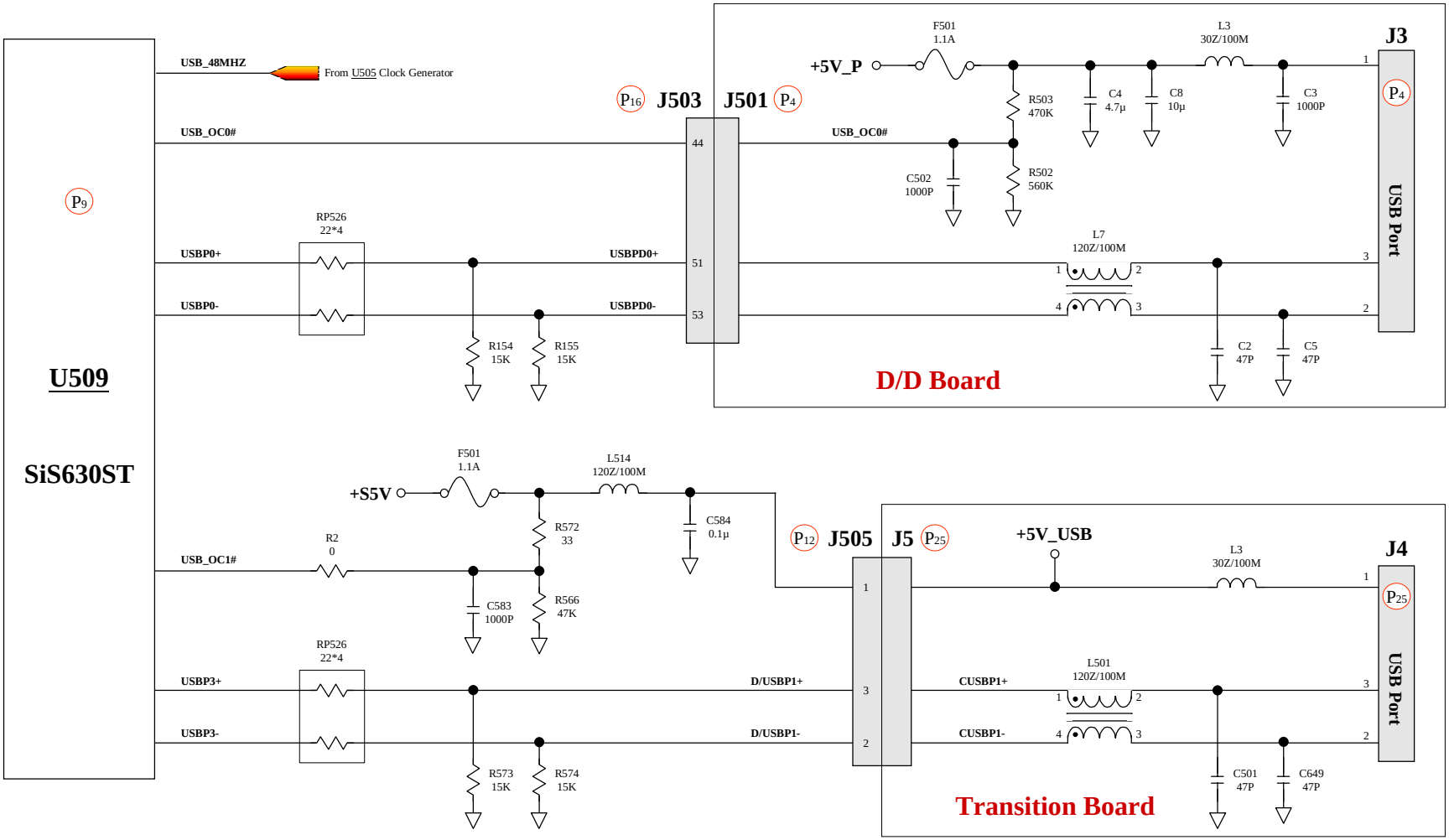
Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:		**Signals:**
U509	J501	+S5V
J503	F501	USB_48MHZ
RP526	L3	USB_OC0#
F501	L7	USB_P0+
L514	J3	USB_P0-
R2	J5	USB_OC1#
J505	L3	USB_P3+
	L501	USB_P3-
	J4	

M762 N/B Maintenance

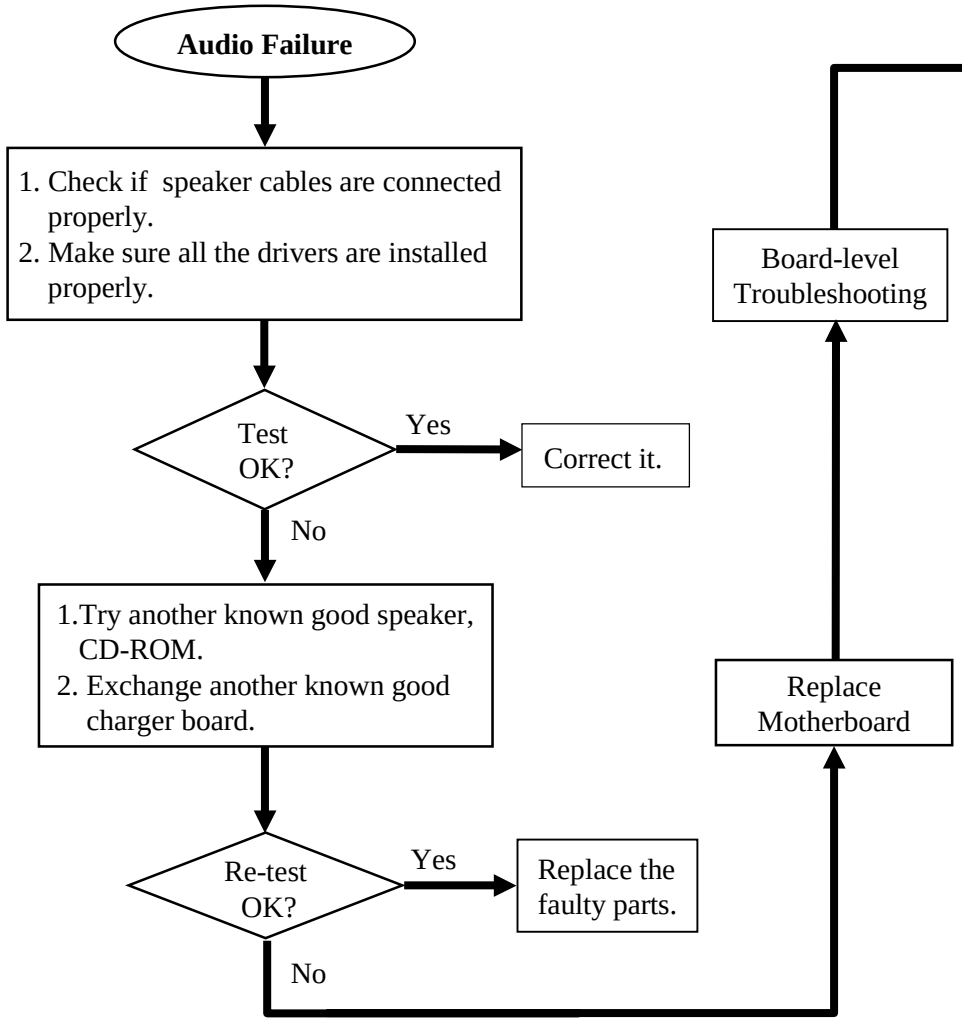
8.9 USB Test Error

An error occurs when a USB I/O device is installed.



8.10 Audio Failure

No sound from speaker after audio driver is installed.



Check the following parts for cold solder or one of the following parts on the motherboard may be defective,use an oscilloscope to check the following signal or replace parts one at a time and test after each replacement.

1.If no sound cause of line out, check the following parts & signals:

Parts:	Signals:
U509	AOUT_R
U15	AOUT_L
U515	5V_AMP
U18	SPK_OFF
U16	SPDIFOUT
J14	
L33	
L32	
L529	
L42	
L39	
L519	
L523	

2. If no sound cause of MIC, check the following parts & signals:

Parts:	Signals:
U509	AVDDAD
U15	MIC1
U515	
U18	
C608	
R225	
R727	
L37	
J15	
MIC1	

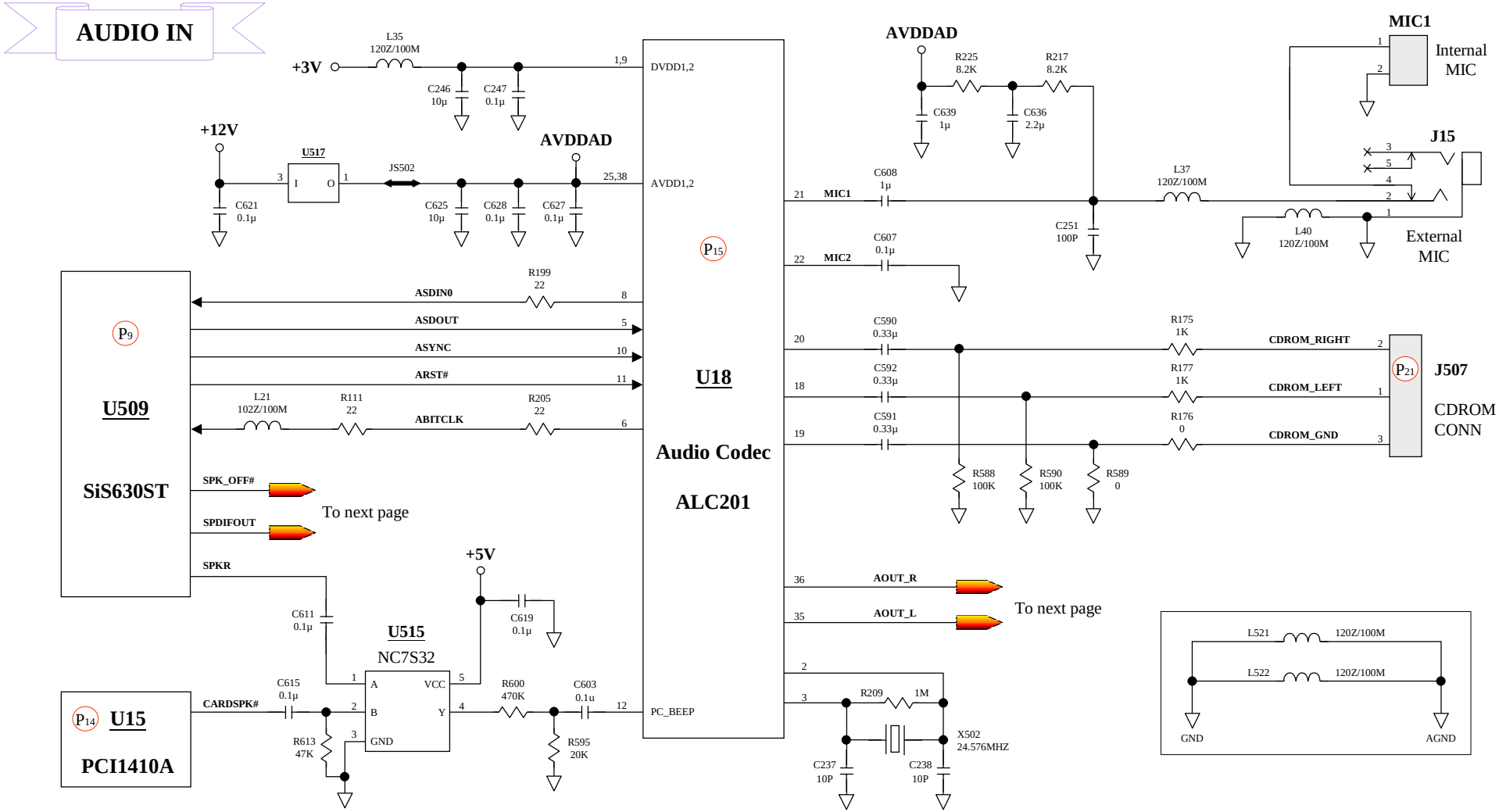
3. If no sound cause of CD-ROM, check the following parts & signals:

Parts:	Signals:
U509	CDROM_LEFT
U15	CDROM_RIGHT
U515	CDROM_GND
U18	
C590	
C591	
C592	
R175	
R176	
R177	
J507	

M762 N/B Maintenance

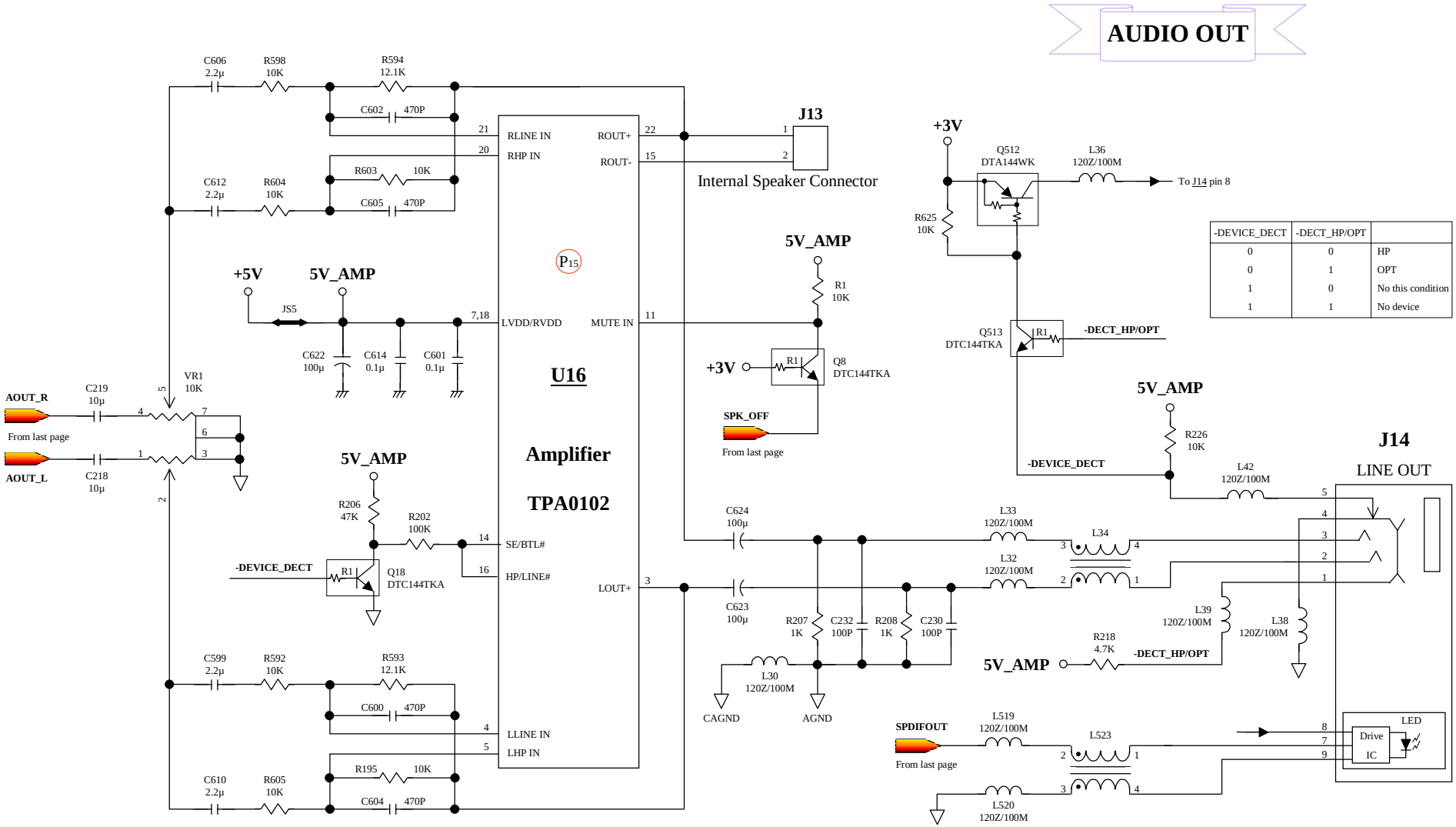
8.10 Audio Failure

No sound from speaker after audio driver is installed.



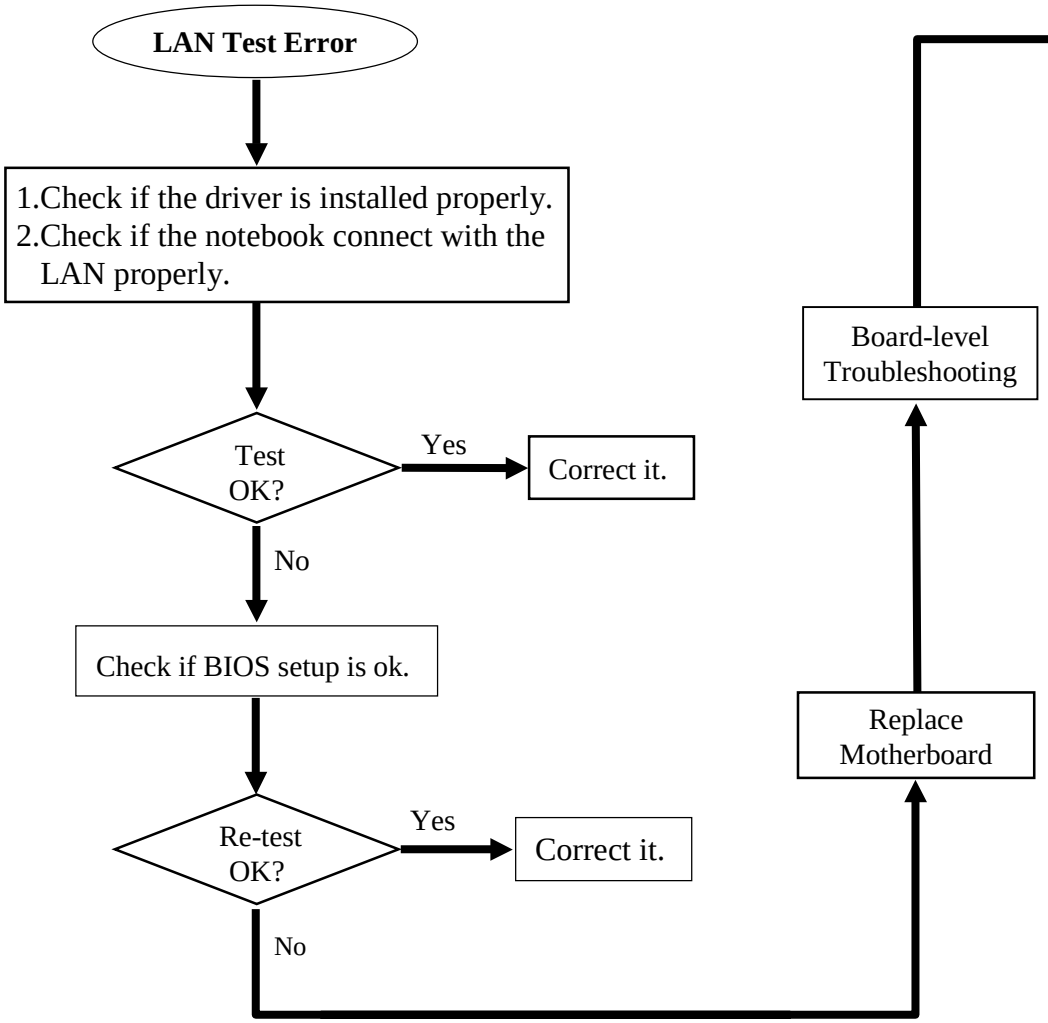
8.10 Audio Failure

No sound from speaker after audio driver is installed.



8.11 LAN Test Error

An error occurs when a LAN device is installed.



Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:

U509	R178
U12	R236
U11	L55
U14	L29
J10	R165
Q3	R160
RP13	R159
RP15	R152
RP16	
R167	
L57	
X3	
C213	
R190	
R185	
L56	
R237	
R238	

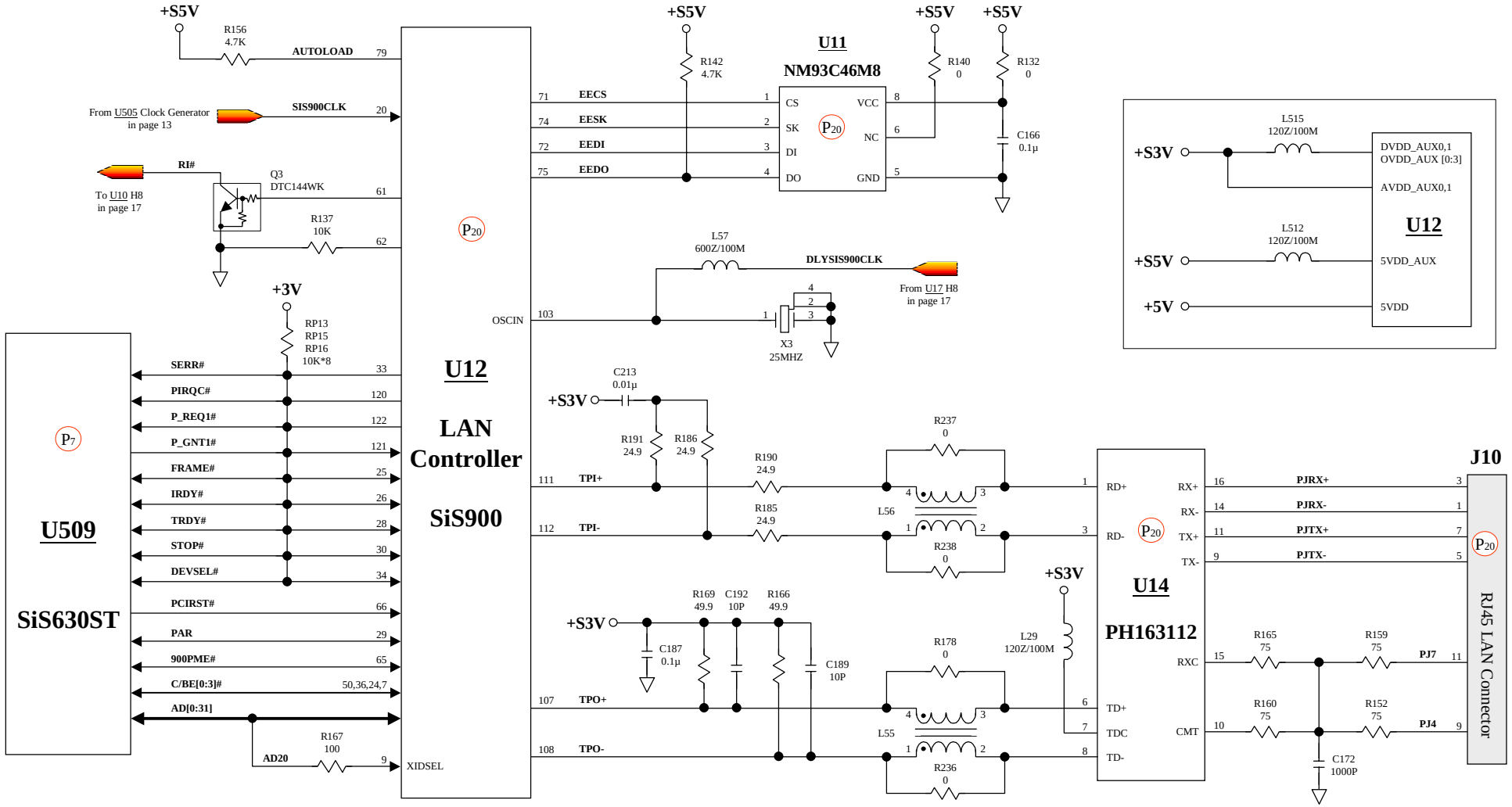
Signals:

AUTOLOAD	EECS
SIS900CLK	EESK
RI#	EEDI
SERR#	EEDO
PIRQC#	DLYSIS900CLK
P_REQ1#	TPI+
P_GNT1#	TPI-
PCIRST#	IPO+
FRAME#	TPO-
IRDY#	PJRX+
TRDY#	PJRX-
STOP#	PJTX+
PAR	PJTX-
DEVSEL#	PJ7
900PME#	PJ4
C_BE[0:3]#	
AD[0:31]	

M762 N/B Maintenance

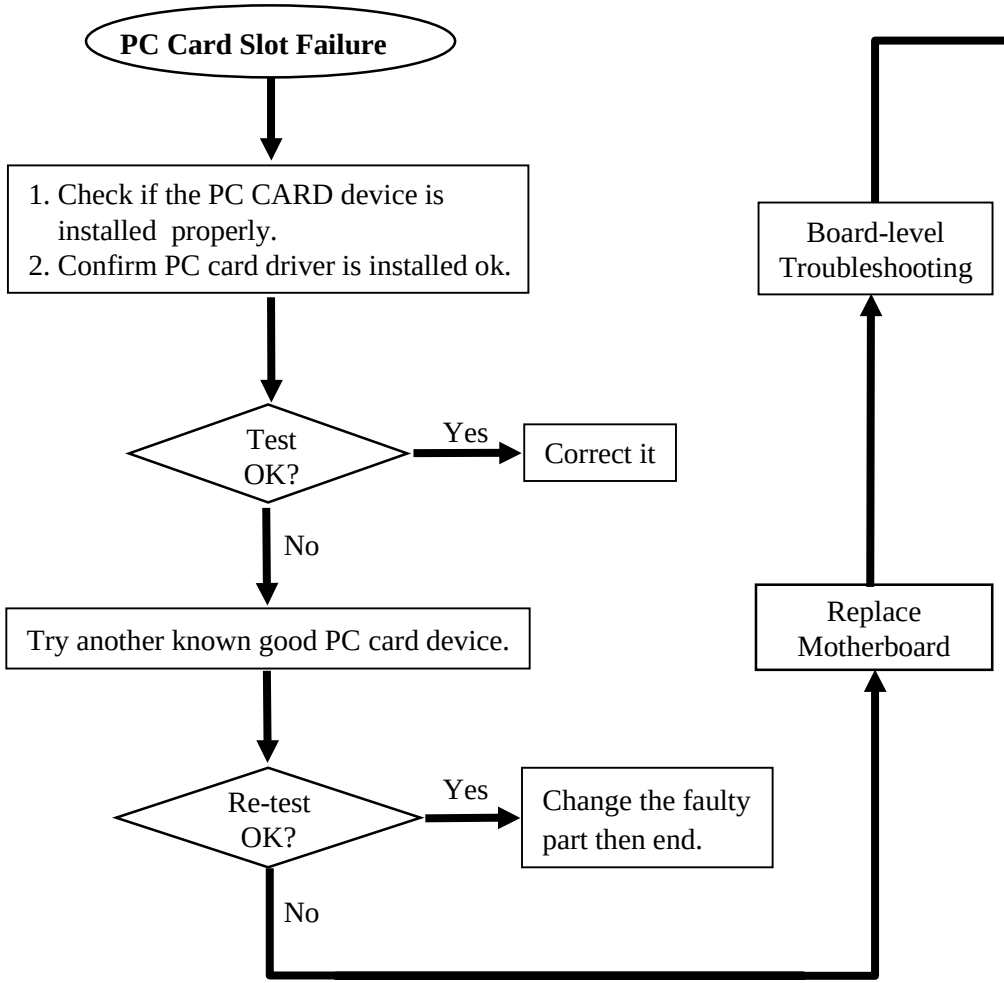
8.11 LAN Test Error

An error occurs when a LAN device is installed.



8.12 PC Card Slot Failure

An error occurs when a PC card device is installed.



Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:

U509
U15
U17
J504
Q509
R157
R192
R164

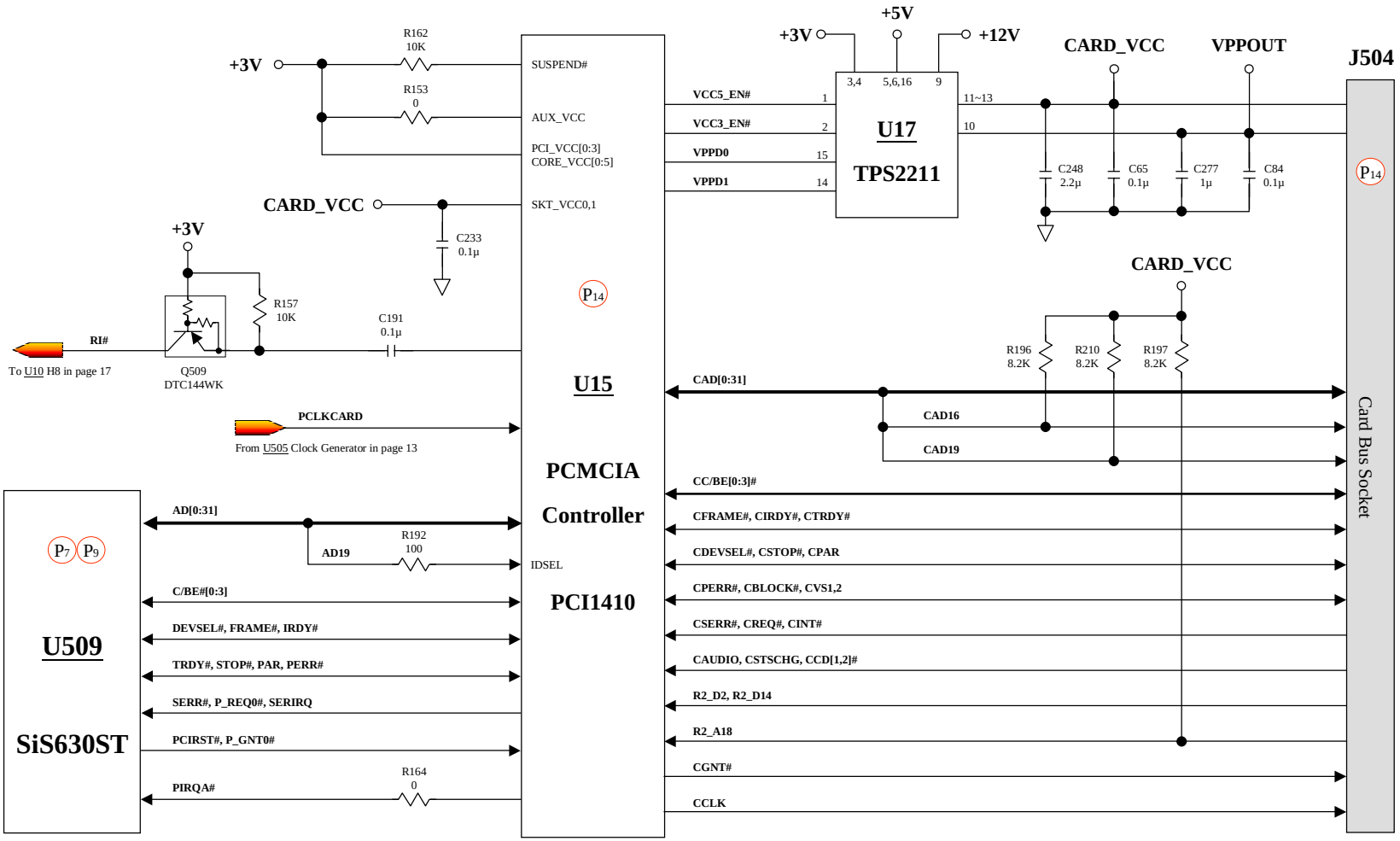
Signals

AD[0:31]
C/BE# [0:3]
DEVSEL#
FRAME#
IRDY#
TRDY#
STOP#
PAR
PERR#
SERR#
P_REQ0#
SERIRQ
PCIRST#
P_GNT0#
PIRQA#
CARD_VCC
RI#
PCLKCARD
VCC5_EN#
VCC3_EN#
VPPD0
VPPD1
CARD_VCC
VPPOUT
+3V

M762 N/B Maintenance

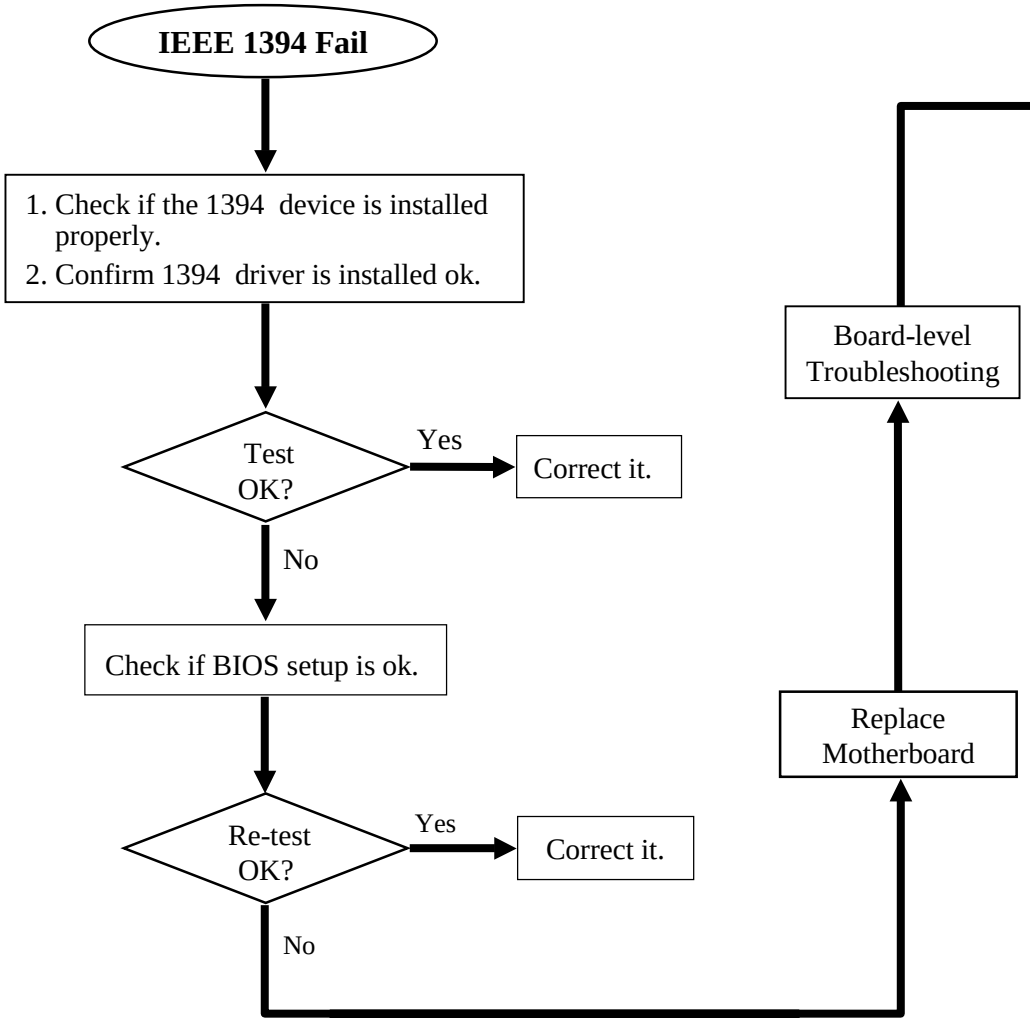
8.12 PC Card Slot Failure

An error occurs when a PC card device is installed.



8.13 IEEE 1394 Failure

An error occurs when a IEEE 1394 device is installed.



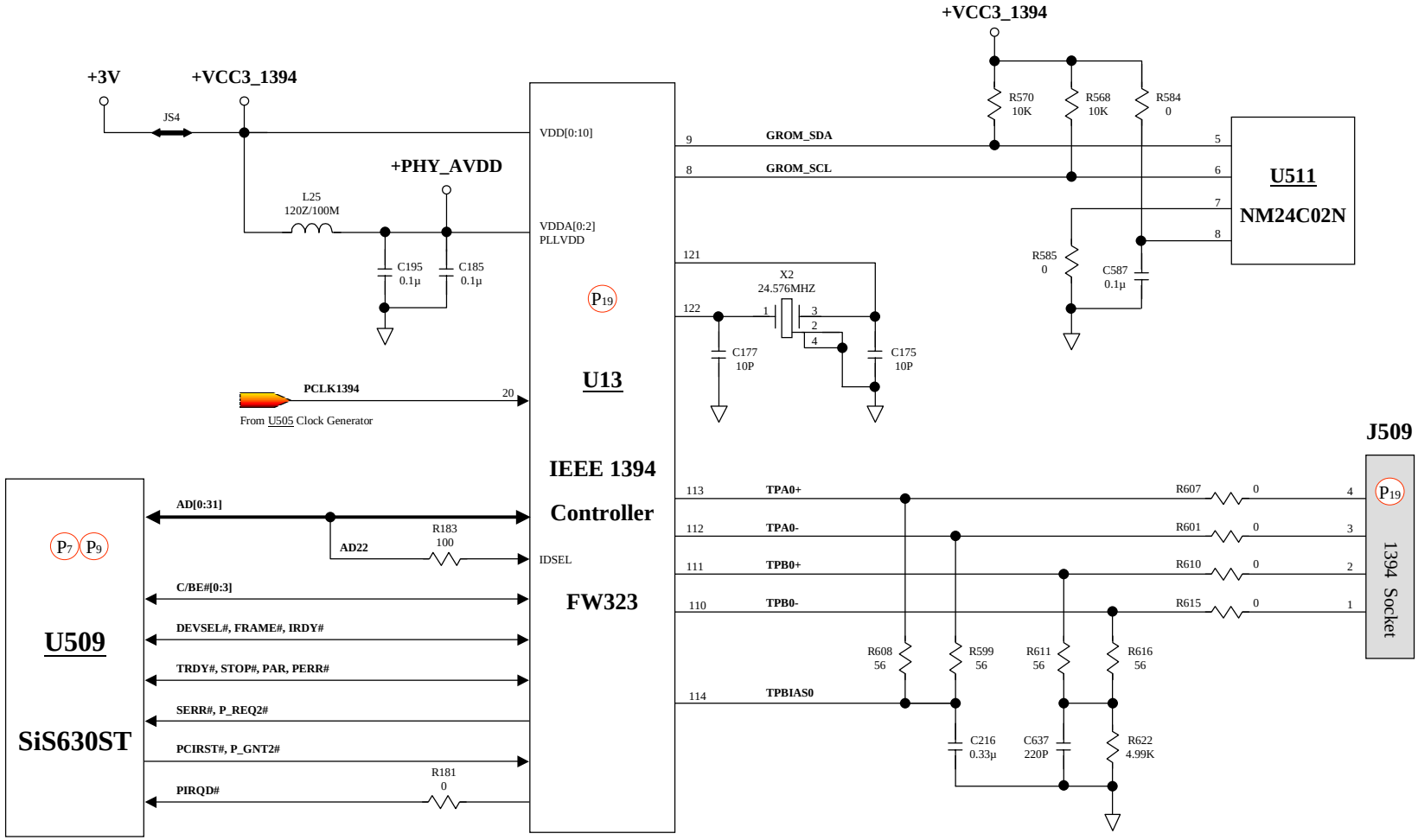
Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:	**Signals**	
U509	AD[0:31]	PCIRST#
U13	C/BE# [0:3]	P_GNT2#
U511	DEVSEL#	PIRQD#
JS4	FRAME#	PCLK1394
L25	IRDY#	GROM_SDA
R183	TRDY#	GROM_SCL
R181	STOP#	TPA0+
X2	PAR	TPA0-
R607	PERR#	TPB0+
R601	SERR#	TPB0-
R610	P_REQ2#	TPBIAS0
R615		+3V
J509		+VCC3_1394
		+PHY_AVDD

M762 N/B Maintenance

8.13 IEEE 1394 Failure

An error occurs when a IEEE 1394 device is installed.



9. Spare Parts List - 1

Part Number	Description	Location(s)
441999900201	AC ADPT ASSY OPTION;M722	
442051200001	AC ADPT ASSY;19V/3.16A,DELTA	
541667200031	AK;BOX,LEGEND,M762	
346672000008	AL-FOIL;CD-ROM WIRE,M762	
346672000007	AL-FOIL;K/B REAR COVER,M762	
340672000011	AL-PLATE ASSY;SIS630,M762	
340672000012	AL-PLATE ASSY;SIS900,M762	
441999900061	BATT ASSY OPTION;LI-ION,1650MAH,	
442672000001	BATT,ASSY;14.8V/3.3AH,LI-MOLICEL	
242670800113	BFM-WORLD MARK;WINXP,7521N	
221668940001	BOX;INNER AK,M722	
340668300022	BRACKET ASSY;HDD-2,HOPE	
342668900002	BRACKET;SPEAKER,2ND ID,M722	
421672000001	CABLE ASSY;LCD,HYUNDAI,M762	
421015560001	CABLE ASSY;PHONE LINE,6P2C,W/Z C	
272075103702	CAP;.01U ,50V,+80-20%,0603,SMT	C7
272075103702	CAP;.01U ,50V,+80-20%,0603,SMT	C1,PC537,,PC502,509,10
272075103702	CAP;.01U ,50V,+80-20%,0603,SMT	C12,C122,C13,C138,C144,C1
272075104701	CAP;.1U ,50V,+80-20%,0603,SMT	PC501,506,514,515,,PC517,5
272075104701	CAP;.1U ,50V,+80-20%,0603,SMT	C10,C103,C111,C112,C113,C
272072224701	CAP;.22U ,16V ,+80-20%,0603,Y5V,	C102,C105,C106,C108,C109,(
272072334701	CAP;.33U ,CR,16V ,+80-20%,0603,Y	C216,C590,C591,C592
272075102701	CAP;1000P,50V ,+/-20%,0603,X7R,S	PC16,PC3,PC516,PC525,PC6
272030102405	CAP;1000P,CR,3KV,10%,1808,X7R,TU	C640,C641
272030102405	CAP;1000P,CR,3KV,10%,1808,X7R,TU	C172

Part Number	Description	Location(s)
272075102403	CAP;1000P,CR,50V,10%,0603,X7R,SM	C3,502,PC15,530
272075102403	CAP;1000P,CR,50V,10%,0603,X7R,SM	C11,C114,C148,C161,C186,C
272075101701	CAP;100P ,50V ,+ -10%,0603,NPO,S	C230,C232,C251,C508,PC24
272431107509	CAP;100U,2V,20%,7343,SDK-CAP	PC534,PC535,PC536,PC537,P
272075100701	CAP;10P ,50V ,+-10%,0603,NPO,SM	C145,C173,C175,C177,C189,(
272011106701	CAP;10U ,10V,+80-20%,1206,Y5V,S	C8
272011106701	CAP;10U ,10V,+80-20%,1206,Y5V,S	C8
272011106701	CAP;10U ,10V,+80-20%,1206,Y5V,S	C100,C116,C120,C14,C142,C
272012106701	CAP;10U ,16V ,+80-20%,1206,Y5U,	PC30,PC525,PC526
272023106701	CAP;10U ,25V ,+80-20%,1210,Y5U,	PC522,PC523,PC527,PC532
272023106501	CAP;10U ,25V ,20%,1210,Y5U,SMT	PC19,27,503-505,508,,PC529
272075121401	CAP;120P ,CR,50V ,10%,0603,NPO,S	PC513,PC8
272431227503	CAP;150U ,POLY,6.3V,20%,7243,SMT	PC13,9
272001105403	CAP;1U ,10%,10V ,0805,X7R,SMT	PC14,PC501,PC503,PC504,PC
272071105701	CAP;1U ,CR,10V ,80-20%,0603,Y5	PC507,519
272071105701	CAP;1U ,CR,10V ,80-20%,0603,Y5	C101,C107,C117,C129,C130,(
272002105701	CAP;1U ,CR,16V ,-20+80%,0805,Y5	PC520
272002225701	CAP;2.2U ,CR,16V ,+80-20%,0805,Y	C210,C211,C248,C546,C599,(
272075221401	CAP;220P ,CR,50V ,10%,0603,X7R,S	C637
272431227504	CAP;220U ,4V ,20%,7343,POSCAP,SM	PC24-26
272431227516	CAP;220U,2V,20%,7343,SDK-CAP	PC539,PC540,PC541
272075220701	CAP;22P ,50V ,+ -10%,0603,NPO,S	C2,5
272021226701	CAP;22U ,10V,+80-20%,1210,Y5V,S	C184,PC502
272041226501	CAP;22U ,CR,10V ,20%,1812,X7R,S	C654
272043226501	CAP;22U ,25V ,+-20%,1812,Y5U,SMT	PC521

9. Spare Parts List - 2

Part Number	Description	Location(s)
272075271401	CAP;270P ,50V,+-10%,0603,X7R,SMT	C243,C547
272075331401	CAP;330P ,CR,50V,10%,0603,X7R,SM	PC25
272011475401	CAP;4.7U ,10%,10V ,1206,X7R,SMT	C4,PC12
272012475701	CAP;4.7U ,CR,16V ,+80-20%,1206,Y	C167,C169,C17,C18,C55,PC1
272075471401	CAP;470P ,50V,10%,0603,X7R,SMT	PC10,PC518,PC530,PC9
272075470701	CAP;47P ,50V ,+ -10%,0603,NPO,S	C501,C649
272075470701	CAP;47P ,50V ,+ -10%,0603,NPO,S	C104,C152,C155,C171,C33,C
221668950010	CARD BOARD,BTM,PALLET,M722	
221668950007	CARD BOARD;FRAME,PALLET,M722	
221668950006	CARD BOARD;TOP,PALLET,M722	
221668920017	CARTON;NON-BRAND,MSL,M722	
431672000003	CASE KIT;LEGEND,M762	
273000500068	CHOKE COIL;0.6UH,26A	PL504
273000500019	CHOKE COIL;10UH,4.5A,4.5MM,CDRH1	PL3
273000111002	CHOKE COIL;120OHM/100MHZ,20%,321	L501
273000111002	CHOKE COIL;120OHM/100MHZ,20%,321	L7
273000111002	CHOKE COIL;120OHM/100MHZ,20%,321	L34,L523,L55,L56
273000500057	CHOKE COIL;4.7UH,16mOHM,30%,5.7A	PL505,PL506
273000500015	CHOKE COIL;50UH(REF),D.4*2,5.5T,	L43
331000006008	CON;BATT,6P,MA,2.5MM,R/A,25063A	PJ1
331720015035	CON;D,FM,15P,2.29MM,R/A,3 ROW,73	J1
291000725001	CON;D,MA,50P,0.8MM,R/A,SMT	J2
291000151201	CON;FPC/FFC,12P,0.5MM,R/A,SMT	J12
291000153006	CON;FPC/FFC,15P*2,.8MM,BD/BD,ST,	J506
291000152401	CON;FPC/FFC,24P,1MM,R/A,ELCO	J9

Part Number	Description	Location(s)
291000155001	CON;FPC/FFC,50P,0.5MM,R/A,ZIF,SM	J501
291000155001	CON;FPC/FFC,50P,0.5MM,R/A,ZIF,SM	J507
291000150806	CON;FPC/FFC,8P,0.5MM,R/A,SMT	J6
291000021203	CON;HDR,FM,12P,1.27MM,R/A,SMT	J10
291000026601	CON;HDR,FM,33P*2,1.27MM,R/A,SMT	J501
291000021204	CON;HDR,MA,12P,1.27MM,R/A,SMT	J18
331040044012	CON;HDR,MA,22P*2,1.27,R/A,H3.45,	J11
291000020202	CON;HDR,MA,2P*1,1.25,R/A,SMT,HIR	J13,J508
291000026602	CON;HDR,MA,33P*2,1.27MM,R/A,SMT	J503
331040004014	CON;HDR,MA,4P*1,2.5MM,R/A,USB	J4
331040004014	CON;HDR,MA,4P*1,2.5MM,R/A,USB	J3
291000010404	CON;HDR,MA,4P,1.25MM,H=3.6,ST,SM	J5
291000010404	CON;HDR,MA,4P,1.25MM,H=3.6,ST,SM	J505
331040004016	CON;HDR,MA,4P,1.25MM,R/A	J2
291000020303	CON;HDR,SHROUD,MA,3P,1.25MM,R/A,	J4
291000256808	CON;IC CARD,68P,.635MM,SMT,FCI62	J504
331000004009	CON;IEEE1394,MA,4P*1,0.8MM,R/A	J509
331810006044	CON;PHONE JACK,6P2C,H11.5,RJ11,T	J17
291000810802	CON;PHONE JACK,8P,H=12.59,R/A,RJ	J19
331840010005	CON;POF MINI JACK,10P,W/SPDIF,2F	J14
331910003024	CON;POWER JACK,3P,D=2.5,H=7,W=9.	PJ3
291000032001	CON;RECT,FM,20P,0.5MM,ST,SMT	J7
331840005007	CON;STEREO JACK,5P,R/A,W9.1,LGY2	J15
291000410201	CON;WFR,MA,2P,1.25,ST,SMT/MB	J16
225672000009	CONDUCTIVE TAPE:MODEM,M762	

9. Spare Parts List - 3

Part Number	Description	Location(s)
225672000010	CONDUCTIVE TAPE:TOP RJ11-RT45,M7	
225668300002	CONDUCTIVE TAPE;DIMM COVER,HOPE	
225672000006	CONDUCTIVE TAPE;INVERTER WIRE,20	
225672000005	CONDUCTIVE TAPE;LCD CABLE,30X30,	
340672000017	COVER ASSY;CPU,M762	
340672000016	COVER ASSY;DIMM,M762	
340672000003	COVER ASSY;REAR,M762	
340672000014	COVER ASSY;TOP,LEGEND,M762	
344672000034	COVER;HINGE,M762	
344668340001	COVER;LAN&MODEM,B-200,HOPE2	
344672000032	COVER;LCD,M762	
344668900031	COVER;VGA(NEW),M722	
272625470401	CP;47P*4 ,8P,50V ,10%,1206,NPO,S	CP501,502
272625470401	CP;47P*4 ,8P,50V ,10%,1206,NPO,S	CP1,CP2,CP3,CP4,CP5,CP50
291000621445	DIMM SOCKET;144P,.8MM,GOLD,SMT	J502
288100032013	DIODE;BAS32L,VRRM75V,MELF,SOD-80	PD9
288100701002	DIODE;BAV70LT1,70V,225MW,SOT-23	PD1,7
288100701002	DIODE;BAV70LT1,70V,225MW,SOT-23	D10,D13,D7
288100099001	DIODE;BAV99,70V,450MA,SOT-23	D14,D5,D505
288100056003	DIODE;BAW56,70V,215MA,SOT-23	PD6
288100056003	DIODE;BAW56,70V,215MA,SOT-23	D11,D503,D506,PD504
288100112003	DIODE;EC11FS2-TE12L,SCHOTTKY,200	PD3
288103103001	DIODE;EC31QS03L,30V,3A,SMT	PD10,502,509
288103103001	DIODE;EC31QS03L,30V,3A,SMT	PD501,PD506,PD507
288104148001	DIODE;RLS4148,200MA,500MW,MELF,S	D12,D8,D9,PD503,PD505,PD

Part Number	Description	Location(s)
288100024002	DIODE;RLZ24D,ZENER,23.63V,5%,SMT	PD2
288100036001	DIODE;RLZ3.6B,ZENER,3.45V,5%,SMT	PD503
288100056001	DIODE;RLZ5.6B,ZENER,5.6V,5%,LL34	PD5
288100056005	DIODE;UDZ5.6B,ZENER,5.6V,UMD2,SM	PD4,511
288100056005	DIODE;UDZ5.6B,ZENER,5.6V,UMD2,SM	PD502
344668900013	DOOR;CD-ROM,M722	
344668900053	DUMMY-CARD;PCMCIA,M722	
272602107501	EC;100U,16V,M,6.3*5.5,-55+85'C,S	C622,C623,C624
312272205359	EC;22U ,20V,20%,RA,D6.3*5,OS-CO	PC14
272603226504	EC;22U ,25V,M,3.6*6.3,85'PETITC	PC23
227668900005	END CAP;CD-ROM,M722	
227668900006	END CAP;FDD,M722	
227672000001	END CAP;FRAME,M762	
227672000003	END CAP;M762	
227672000002	END CAP;TOP,AK,M762	
481672000002	F/W ASSY;KBD CTRL,M762	U10
481672000004	F/W ASSY;SYS/VGA BIOS,LEGENDS,M7	U512
273000610008	FERRITE ARRAY;120OHM/100MHZ,TKIN	FA502
273000610008	FERRITE ARRAY;120OHM/100MHZ,TKIN	FA1,FA2,FA3,FA4,FA5
273000130019	FERRITE CHIP;120OHM/+-10%/100MHZ	L10,L11,L14,L17,L18,L19,L21
273000130001	FERRITE CHIP;120OHM/100MHZ,1608,	L506
273000150013	FERRITE CHIP;120OHM/100MHZ,2012,	L526,L528
273000150013	FERRITE CHIP;120OHM/100MHZ,2012,	PL501,502,504,,PL506-512
273000150013	FERRITE CHIP;120OHM/100MHZ,2012,	L13,L15,L20,L25,L4,L5,L510,
273000150009	FERRITE CHIP;30OHM/100MHZ,2012,S	L2,L3

9. Spare Parts List - 4

Part Number	Description	Location(s)
273000150009	FERRITE CHIP;30OHM/100MHZ,2012,S	L3,2
273000130006	FERRITE CHIP;600OHM/100MHZ,.2A,1	L1,4,5,501
273000130006	FERRITE CHIP;600OHM/100MHZ,.2A,1	L26,L27,L28,L32,L33,L36,L37
422666200001	FFC ASSY;TOUCH PAD,CASE KIT,NV	
341669900011	FINGER;EMI GROUND SMD FINGER,H=3	E501,E502,E503
288003600001	FIR;HSDL3600#007,FRONT VIEW,10P,	U2
421668300034	FPC ASSY;HDD,HOPE	
421668300032	FPC ASSY;QUICK KEY TO M BD,HOPE	
421668900051	FPC;CD-ROM/MB,M722	
346668300029	FR4;PCB,HDD-CONN.44P,HOPE	
295000010008	FUSE;1.1A,POLY SWITCH,1812,SMT	F501
295000010044	FUSE;1.1A/6V,POLY SWITCH,1210,SM	F502
295000010044	FUSE;1.1A/6V,POLY SWITCH,1210,SM	F1,F2,F501
295000010105	FUSE;1A,NORMAL,1206,SMT	PF501
295000010016	FUSE;NORMAL,6.5A/32VDC,3216,SMT	PF1,503
345666700002	GASKET;345665400028,6133S	
345668300031	GASKET;BOTTOM-SIDE/HEATSINK,HOPE	
345668300028	GASKET;BRACKET-HDD,HOPE	
345672000014	GASKET;MB-TOP,VR,M762	
345668300024	GASKET;MINI-USB,HOPE	
345668300029	GASKET;MINI-USB2,HOPE	
345672000007	GASKET;QSB CONN,M/B,M762	
345672000009	GASKET;REAR COVER,K/B,M762	
345668300019	GASKET;USB,HOPE	
340672000004	HEATSINK ASSY;MFCPGA,M762	

Part Number	Description	Location(s)
340668900003	HINGE;L,12.1",M722	
340668900004	HINGER;R,12.1"M722	
344668900039	HOLDER;TOUCH-PAD,2ND ID,M722	
340672000002	HOUSING ASSY;BOTTOM,M762	
451672000033	HOUSING KIT;LEGEND,M762	
343672000002	HOUSING;LCD,HYUNDAI,M762	
344600000388	IC CARD CON PART;68P*1,CARD BUS	
331650047901	IC SOCKET;479P,ZIF,UFCPGA,AMP	U507
282574373004	IC;74AHC373,OCT D-TRAN,TSSOP,20P	U9
282074338402	IC;74CBTD3384,10 BIT BUS SW,TSOP	U513,U514,U516,U6
282574164002	IC;74VHC164,SIPO REGISTER,TSSOP,	U518
284501032001	IC;ADM1032,TEMPERATURE MTR,SO8	U506
286300809003	IC;ADM809M,RESET CIRCUIT,4.38V,S	U7
284500201002	IC;ALC201,AC97 CODEC,TQFP,48P	U18
284590363001	IC;DS90C363,LVDS,18BIT,SSOP,48P	U5
283466570001	IC;EEPROM,9346,64*16 BITS,SO8,SM	U11
283400000003	IC;EEPROM,NM24C02N,2K,SO,8P	U511
283450083002	IC;FLASH,512K*8-70,PLCC32,ST39SF	
284500323001	IC;FW323,IEEE1394,HOST BRGE TQFP	U13
284583437003	IC;H8/F3437S,KBD CTRL,TQFP,100P,	
284595010401	IC;ICS950104,CLOCK GEN,SSOP,48P	U505
286100393004	IC;LMV393,DUAL COMPARTOR,SSOP,8P	PU3
286302951015	IC;LP2951ACM,VOLTAGE REGULATOR,S	PU501
286301622001	IC;LTC1622,PWM,SO8P	PU1,PU503
286301632002	IC;MAX1632CAI,PWM CTRL,SSOP,28P	PU503

9. Spare Parts List - 5

Part Number	Description	Location(s)
286301718002	IC;MAX1718,PWM,QSOP,28P	PU2
281300732001	IC;NC7S32,SINGLE OR GATE,SC70-5	U515
286307805010	IC;NJM78L05UA,VOL REGULATOR,SOT,	U517
284587393002	IC;PC87393F,TQFP,100P	U8
284501410007	IC;PCI1410A,PCI/CARDBUS,PQFP,144	U15
286300431010	IC;SC431CSK-1,1%,ADJ REG,SOT23	PQ506
286300431010	IC;SC431CSK-1,1%,ADJ REG,SOT23	Q17
286300431014	IC;SC431LCSK-.5,.5%,ADJ REG,SOT2	PQ5,PQ504,PQ511
283767200002	IC;SDRAM,2M*16*4,PC133,HY57V2816	U1,U2,U3,U4,U501,U502,U5
284500630013	IC;SIS630ST,PCI/AGP/LPC,VGA,BGA,	U509
284500900001	IC;SIS900,LAN CONTROLLER,PQFP,12	U12
286300594001	IC;TL594C,PWM CONTROL,SO,16P	PU2
286100202001	IC;TPA0202,AUDIO AMP,2W,TSSOP,24	U16
286302211001	IC;TPS2211,POWER DISTRI SW,SSOP1	U17
273000990031	INDUCTOR;10UH,CDRH127B,SUMIDA,SM	PL2
273000990021	INDUCTOR;33uH,CDRH124,SMT	PL4
273000150106	INDUCTOR;4.7UH,10%,2012,SMT	L12
346668300007	INSULATOR;COVER,REAR,USB,HOPE	
346668300024	INSULATOR;DIMM P/N MB TOP,HOPE	
346672000011	INSULATOR;DIMM,M/B,8X30,M762	
346672000009	INSULATOR;DIMM,M/B,M762	
346668300046	INSULATOR;INVERTER,SXGA,2,HOPE	
346668300025	INSULATOR;LCD,WIRE,HOPE	
346668300008	INSULATOR;M/B,PCMCIA,HOPE	
346672000013	INSULATOR;MB-TOP,VR,M762	

Part Number	Description	Location(s)
346668300040	INSULATOR;MDC MB,94V0,HOPE	
346668300020	INSULATOR;MIC-BTM-MB,HOPE	
346668300020	INSULATOR;MIC-BTM-MB,HOPE	
346668300041	INSULATOR;QSB,REAR COVER,HOPE	
346672000012	INSULATOR;TOP-REAR COVER,M762	
451672000006	LABEL KIT;LEGEND,M762	
242600000145	LABEL;10*10,BLANK,COMMON	
242600000145	LABEL;10*10,BLANK,COMMON	
242662300009	LABEL;25*10MM,3020F	
242600000385	LABEL;27*10,LAN ID BAR CODE	
242668300028	LABEL;32*7MM,POLYESTER FILM,HOPE	
242668300017	LABEL;4*3MM,HI-TEMP,260'C,HOPE	
242672000003	LABEL;AGENCY-GLOBAL,MSL,M762	
242600000157	LABEL;BAR CODE,125*65,COMMON	
242600000433	LABEL;BLANK,11*5MM,COMMON	
242664800013	LABEL;CAUTION,INVERT BD,PITCHING	
242600000099	LABEL;MODEL,5M,MITAC	
242600000099	LABEL;MODEL,5M,MITAC	
242600000195	LABEL;SOFTWARE,INSYDE BIOS-M	
340672000013	LATCH ASSY;LCD,M762	
441672000001	LCD ASSY;HYUN,XGA,12.1,DIST/LEG,	
451672000051	LCD ME KIT;HYUN,XGA,12.1,DIST/LE	
413000020264	LCD;HT12X12-100,TFT,12.1",XGA,HY	
294011200121	LED;BLUE,H1.1,1206,LTST-C150TBKT	D1,D2,D3,D4
294011200016	LED;GREEN,H0.8,0603,CL-190G,SMT	D15

9. Spare Parts List - 6

Part Number	Description	Location(s)
294011200001	LED;GRN,H1.5,0805,PG1102W,SMT	D17
294011200021	LED;ORG,H0.8,0603,CL-190D,SMT	D16
294011200006	LED;RE/GR,H1.5,L3,W2.5,BRPG1201W	D18
344668300002	LENS;IR,HOUSING KIT,HOPE	
526267200020	LTXNX;M762/T2XA/XXX7/XXX/L3D3A/X	
339115000038	MICROPHONE;-60+-3dB,1KOHM,4.5V	MIC1
412999900037	MODEM OPTION;UNIVERSEL,MDC,M722	
416267200903	NB PF OPTION;XGA,12.1,LEGEND,M76	
416267200007	NB PF;HYUNDAI,LEGEND,M762	
375102030010	NUT-HEX;M2,2,NIW	
461668900018	PACKING KIT;N-B,M722 MSL	
221668950008	PARTITION;A,PALLET,M722	
221672050001	PARTITION;AK,M762	
221668950009	PARTITION;B,PALLET,M722	
412668900004	PCB ASSY;INVERTER BD,12.1",M722,	
412668900002	PCB ASSY;MDM,56K,UNIV,W/O Y-CAP,	
316672000002	PCB;PWA-M762/CDROM TRANS BD	R01
316672000006	PCB;PWA-M762/DD BD	R01
316672000004	PCB;PWA-M762/LAN MDC BD	R01
316672000001	PCB;PWA-M762/M BD	R01
222600020049	PE BAG;50*70MM,W/SEAL,COMMON	
222668320002	PE BAG;90*280,HOPE	
222668900001	PE BAG;LCD,280x220,M722	
222668320001	PE BAG;N/B,T.08,HOPE	
222600020009	PE BUBBLE BAG;10"*8",COMMON	

Part Number	Description	Location(s)
222668330002	PROTECTING COLTH;LCD,HOPE	
222668330001	PROTECTING COLTH;NB,HOPE	
411672000005	PWA;PWA-M762,CD ROM TRANS BD	
411672000009	PWA;PWA-M762,D/D BD,SMT	
411672000008	PWA;PWA-M762,D/D BD,T/U	
411672000014	PWA;PWA-M762,LEGENDS,MOTHER BD	
411672000016	PWA;PWA-M762,LEGENDS,MOTHER BD,S	
411672000015	PWA;PWA-M762,LEGENDS,MOTHER BD,T	
411672000004	PWA;PWA-M762,MDCLAN TRANS BD	
332810000102	PWR CORD;250V10A,2P,BLK,CHINA,15	
271045047101	RES;.004,1W,1%,2512,SMT	PR31,PR39
271045107101	RES;.01 ,1W ,1% ,2512,SMT	PR521
271045157101	RES;.015 ,1W ,1% ,2512,SMT	PR508,501
271045207101	RES;.02 ,1W ,1% ,2512,SMT	PR525,PR526
271071000002	RES;0 ,1/16W,0603,SMT	PR515,PR10,PR505,PR560,R
271071000002	RES;0 ,1/16W,0603,SMT	PR10,PR21,PR28,PR30,PR52
271071152101	RES;1.5K ,1/16W,1% ,0603,SMT	R526,R530,R532
271071100302	RES;10 ,1/16W,5% ,0603,SMT	PR531
271071100302	RES;10 ,1/16W,5% ,0603,SMT	PR13,PR17,PR29,PR38,PR4,P
271071101301	RES;100 ,1/16W,5% ,0603,SMT	PR11,PR25,R167,R183,R192
271071104101	RES;100K ,1/16W,1% ,0603,SMT	PR13,PR28,PR525,PR9
271071104302	RES;100K ,1/16W,5% ,0603,SMT	PR21,PR36,PR527
271071104302	RES;100K ,1/16W,5% ,0603,SMT	PR22,PR23,PR24,PR501,PR5
271071103101	RES;10K ,1/16W,1% ,0603,SMT	PR12,15
271071103101	RES;10K ,1/16W,1% ,0603,SMT	PR34,PR40,PR507,PR528,PR

9. Spare Parts List - 7

Part Number	Description	Location(s)
271071103302	RES;10K ,1/16W,5% ,0603,SMT	R505,509,517,518,PR1,PR2,5
271071103302	RES;10K ,1/16W,5% ,0603,SMT	PR19,PR513,PR8,R1,R10,R10
271071106301	RES;10M ,1/16W,5% ,0603,SMT	R555
271071118211	RES;11.8K,1/16W,1% ,0603,SMT	PR517
271071111101	RES;110 ,1/16W,1% ,0603,SMT	R546
271071121211	RES;12.1K,1/16W,1% ,0603,SMT	PR510
271071121211	RES;12.1K,1/16W,1% ,0603,SMT	R593,R594
271071137011	RES;137 ,1/16W,1% ,0603,SMT	R128
271071140101	RES;14,1/16W,1%,0603,SMT	R92
271071141102	RES;140 ,1/16W,1% ,0603,SMT	R108
271071151101	RES;150 ,1/16W,1% ,0603,SMT	R535,R539,R545,R83
271071153301	RES;15K ,1/16W,5% ,0603,SMT	R126,R129,R130,R131,R154,I
271071169311	RES;169K ,1/16W,1% ,0603,SMT	PR506,528
271071174311	RES;174K ,1/16W,1% ,0603,SMT	PR503
271071102102	RES;1K ,1/16W,1% ,0603,SMT	PR502
271071102102	RES;1K ,1/16W,1% ,0603,SMT	PR26,R538,R95
271071102302	RES;1K ,1/16W,5% ,0603,SMT	PR554,PR556,R504
271071102302	RES;1K ,1/16W,5% ,0603,SMT	PR33,PR36,PR508,PR524,R1
271071105101	RES;1M ,1/16W,1% ,0603,SMT	PR22,512,523,524,R521,PR3
271071105301	RES;1M ,1/16W,5% ,0603,SMT	PR20,PR519,PR527,PR6,R20
271071222302	RES;2.2K ,1/16W,5% ,0603,SMT	R7,R8
271071222302	RES;2.2K ,1/16W,5% ,0603,SMT	R143,R224,R529,R90,R93
271071249111	RES;2.49K,1/16W,1% ,0603,SMT	R172
271034278301	RES;2.7 ,1/2W ,5% ,2010,SMT	R515
271071200101	RES;20 ,1/16W,1% ,0603,SMT	PR520

Part Number	Description	Location(s)
271071203101	RES;20K ,1/16W,1% ,0603,SMT	PR5
271071203101	RES;20K ,1/16W,1% ,0603,SMT	PR533,R194,R595
271071221302	RES;22 ,1/16W,5% ,0603,SMT	R111,R145,R199,R205,R23,R
271071221012	RES;221 ,1/16W,1% ,0603,SMT	R515
271071249811	RES;24.9 ,1/16W,1% ,0603,SMT	R185,R186,R190,R191
271071267811	RES;26.7 ,1/16W,1% ,0603,SMT	R127
271071202102	RES;2K ,1/16W,1% ,0603,SMT	PR35,R102,R536
271071301311	RES;301K ,1/16W,1% ,0603,SMT	PR11
271071330302	RES;33 ,1/16W,5% ,0603,SMT	R507
271071330302	RES;33 ,1/16W,5% ,0603,SMT	PR512,PR517,R117,R41,R45,
271071331301	RES;330 ,1/16W,5% ,0603,SMT	R1-R4
271071331301	RES;330 ,1/16W,5% ,0603,SMT	R219,R43,R531,R547
271071333101	RES;33K ,1/16W,1% ,0603,SMT	PR27
271071333301	RES;33K ,1/16W,5% ,0603,SMT	PR553
271071333301	RES;33K ,1/16W,5% ,0603,SMT	R572
271071453111	RES;4.53K,1/16W,1% ,0603,SMT	PR502
271071472302	RES;4.7K ,1/16W,5% ,0603,SMT	R106,R109,R138,R14,R142,R
271071499111	RES;4.99K,1/16W,1% ,0603,SMT	PR4,511,522
271071499111	RES;4.99K,1/16W,1% ,0603,SMT	R622
271071432112	RES;43K,1/16W,1%,0603,SMT	PR530
271071471302	RES;470 ,1/16W,5% ,0603,SMT	R103,R214,R221,R222,R223,I
271071474301	RES;470K ,1/16W,5% ,0603,SMT	R503,PR24,516
271071474301	RES;470K ,1/16W,5% ,0603,SMT	PR1,R600,R7
271071475011	RES;475 ,1/16W,1% ,0603,SMT	R34
271071473301	RES;47K ,1/16W,5% ,0603,SMT	PR507

9. Spare Parts List - 8

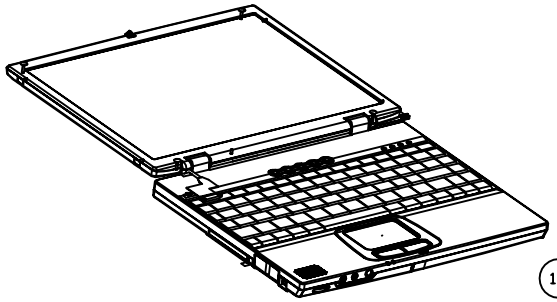
Part Number	Description	Location(s)
271071473301	RES;47K ,1/16W,5% ,0603,SMT	R147,R206,R566,R57,R613
271071499811	RES;49.9 ,1/16W,1% ,0603,SMT	R166,R169
271071562301	RES;5.6K ,1/16W,5% ,0603,SMT	R110,R558
271071513301	RES;51K ,1/16W,5% ,0603,SMT	PR18
271071560301	RES;56 ,1/16W,5% ,0603,SMT	R540,R543,R550,R599,R608,I
271071564301	RES;560K ,1/16W,5% ,0603,SMT	R502
271071562311	RES;562K ,1/16W,1% ,0603,SMT	PR17
271071576311	RES;576K ,1/16W,1% ,0603,SMT	PR513
271071622301	RES;6.2K ,1/16W,5% ,0603,SMT	PR6
271071682301	RES;6.8K ,1/16W,5% ,0603,SMT	R174,R188
271071619811	RES;61.9 ,1/16W,1% ,0603,SMT	R26,R33,R556
271071750101	RES;75 ,1/16W,1% ,0603,SMT	R152,R159,R160,R165,R198,I
271071753101	RES;75K ,1/16W,1% ,0603,SMT	PR16,PR522
271071822301	RES;8.2K ,1/16W,5% ,0603,SMT	R196,R197,R210,R217,R225,I
271071931211	RES;93.1K,1/16W,1% ,0603,SMT	PR18
271071976211	RES;97.6K,1/16W,1% ,0603,SMT	PR32
271071976311	RES;976K ,1/16W,1% ,0603,SMT	PR518
271611000301	RP;0*4 ,8P ,1/16W,5% ,0612,SMT	RP11,RP501
271611100301	RP;10*4 ,8P ,1/16W,5% ,0612,SMT	RP14,RP509
271571100301	RP;10*8 ,16P ,1/16W,5% ,1606,SM	RP502,RP503,RP504,RP505,I
271611103301	RP;10K*4 ,8P ,1/16W,5% ,0612,SMT	RP10,RP12,RP2
271621103303	RP;10K*8 ,10P,1/16W,5% ,1206,SMT	RP13,RP15,RP16,RP4,RP5,RI
271611102301	RP;1K*4 ,8P ,1/16W,5% ,0612,SMT	PRP1
271611220301	RP;22*4 ,8P ,1/16W,5% ,0612,SMT	RP520,RP521,RP522,RP523,I
271611330301	RP;33*4 ,8P ,1/16W,5% ,0612,SMT	RP514,RP515,RP516,RP517,I

Part Number	Description	Location(s)
271611750301	RP;75*4 ,8P ,1/16W,5% ,0612,SMT	RP501
345668300006	RUBBER;LCD,HOPE	
371102610406	SCREW;M2.6L4,K-HEAD(+),NIB	
371102610606	SCREW;M2.6L6,FLT(+),NIW/NLK	
344668900030	SLIDE;VGA COVER,M722	
370102610602	SPC-SCREW;M2.6 L6,NIB,K-HD,t0.8,	
370102610901	SPC-SCREW;M2.6*L9,FLT(+),NIW,NYL	
370102611001	SPC-SCREW;M2.6L10,NIB,K-HD,NY	
370102610302	SPC-SCREW;M2.6L3,NIB,K-HD,NYLOK	
370102610401	SPC-SCREW;M2.6L4,K-HD,t0.8,NIB/N	
370102610603	SPC-SCREW;M2.6L6,K-HD,NIB/NLK	
370102610802	SPC-SCREW;M2.6L8,FLT(+),NIW/NLK	
370102011006	SPC-SCREW;M2L10.2,NUF-HEX,HD(D3.	
370102010281	SPC-SCREW;M2L2.8,FLT,NIW/NLK	
370102010303	SPC-SCREW;M2L3,NIW,K-HD(+),NYLOK	
370102010407	SPC-SCREW;M2L4,K-HD,NIB/NLK	
370102010407	SPC-SCREW;M2L4,K-HD,NIB/NLK	
370102010604	SPC-SCREW;M2L6,K-HD(+),NIB/NLK,H	
370103010405	SPC-SCREW;M3L4,NIW,K-HD,T0.3	
340672000010	SPEAKER ASSY;M762	
345668900006	SPONG;LCD,HOUSING,M722	
345668300018	SPONGE;BAT.BIOS,HOPE	
345668900016	SPONGE;BIOS BATT,M722	
345668900017	SPONGE;SPEAKER BRACKET,M722	
345668900010	SPONGE;TOUCH-PAD-HOLDER,M722	

9. Spare Parts List - 9

Part Number	Description	Location(s)
341668300003	SPRING;HEATSINK,CPU,HOPE	
342668900001	STANDOFF;4-40L5.8,NIW FOR VGA CO	
343668300006	STANDOFF;M/B-D/D,HOPE	
341668300008	STANDOFF;MDC MODEM,NLK,HOPE	
297040200001	SW;PUSH BUTTON,DPDT,4P,12V/50MA	SW4
297040102002	SW;PUSH BUTTON,SPST,15V/20MA,H3.	SW1,SW2
297150200003	SW;SLIDE,DPDT,3P,POM,4V/0.3A	SW1
297030105003	SW;TOGGLE,SPST,5V/1mA,MPU-101-80	SW3
225665500001	TAPE;INSULATION,AC04,25M*6MM,503	
442668900031	TOUCH PAD MODULE;KGDDFR950A-1;AP	
288227002001	TRANS;2N7002LT1,N-CHANNEL FET	PQ1,505,Q1-3,502,PQ507,Q4
288227002001	TRANS;2N7002LT1,N-CHANNEL FET	PQ3,PQ4,PQ501,PQ507,PQ5
288206400001	TRANS;AO6400,N-MOSFET,SO6	PU502,PU510
288206401001	TRANS;AO6401,P-MOSFET,SO6	PU506,PU507
288200144002	TRANS;DTA144WK,PNP,SMT	Q512
288200144003	TRANS;DTC144TKA,N-MOSFET,SOT-23	PQ1,Q18,Q20,Q4,Q501,Q502
288200144001	TRANS;DTC144WK,NPN,SOT-23,SMT	PQ503
288200144001	TRANS;DTC144WK,NPN,SOT-23,SMT	PQ506,Q1,Q11,Q12,Q13,Q15
288202222001	TRANS;MMBT2222AL,NPN,TO236AB	PQ511
288203904010	TRANS;MMBT3904L,NPN,Tr35NS,TO236	Q10,Q16
288203906018	TRANS;MMBT3906L,PNP,Tr35NS,TO236	PQ504
288203906018	TRANS;MMBT3906L,PNP,Tr35NS,TO236	Q14,Q7
288207002001	TRANS;NDC7002N,N-MOSFET,SSOT-6	PQ510
288202301001	TRANS;SI2301DS,P-MOSFET,SOT-23	Q501
288202301001	TRANS;SI2301DS,P-MOSFET,SOT-23	PQ2,PQ503,PQ505,Q511

Part Number	Description	Location(s)
288202302001	TRANS;SI2302DS,N-MOSFET,SOT-23	PQ502,PQ512,PQ6,Q515
288104362001	TRANS;SI4362DY,N-HOSFET,S08	PU504,PU505
288204800001	TRANS;SI4800DY,N-MOS,.0185OHM,SO	PU502,1
288204800001	TRANS;SI4800DY,N-MOS,.0185OHM,SO	Q518
288204832001	TRANS;SI4832DY,N-MOSFET,.028OHM,	PQ501,502
288204835001	TRANS;SI4835DY,PMOS,6A/30V,.035,	PU506,504,PQ509
288204892001	TRANS;SI4892DY,N-MOSFET,SO8	PU508,PU509
288204925001	TRANS;SI4925DY,P-MOSFET,SO-8	PU505
273001050022	TRANSFORMER;10/100 BASE,PH163112	U14
270140000003	VARISTOR;280V,5.6X3.8MM,TVB280-0	S501
311821002101	VR;10K,CF,.02W,30%,RVR16H-013-B1	VR501
421668300002	WIRE ASSY;BACKLIGHT,HOPE	
421668300005	WIRE ASSY;BIOS,BATTERY,HOPE	
421668300003	WIRE ASSY;CD-ROM,HOPE	
274011431409	XTAL;14.318MHZ,16PF,50PPM,8*4.5,	X503
274011600407	XTAL;16MHZ,30PPM,16PF,7*5,4P,SMT	X1
274012457405	XTAL;24.576M,30PPM,16PF,7*5,4P,S	X2
274012457406	XTAL;24.576MHZ,16PF,50PPM,8*4.5,	X502
274012500401	XTAL;25MHZ,30PPM,18PF,4P,SMT	X3
274013276114	XTAL;32.768KHZ,10PPM,12.5PF	X501
	P/N:526267200020	



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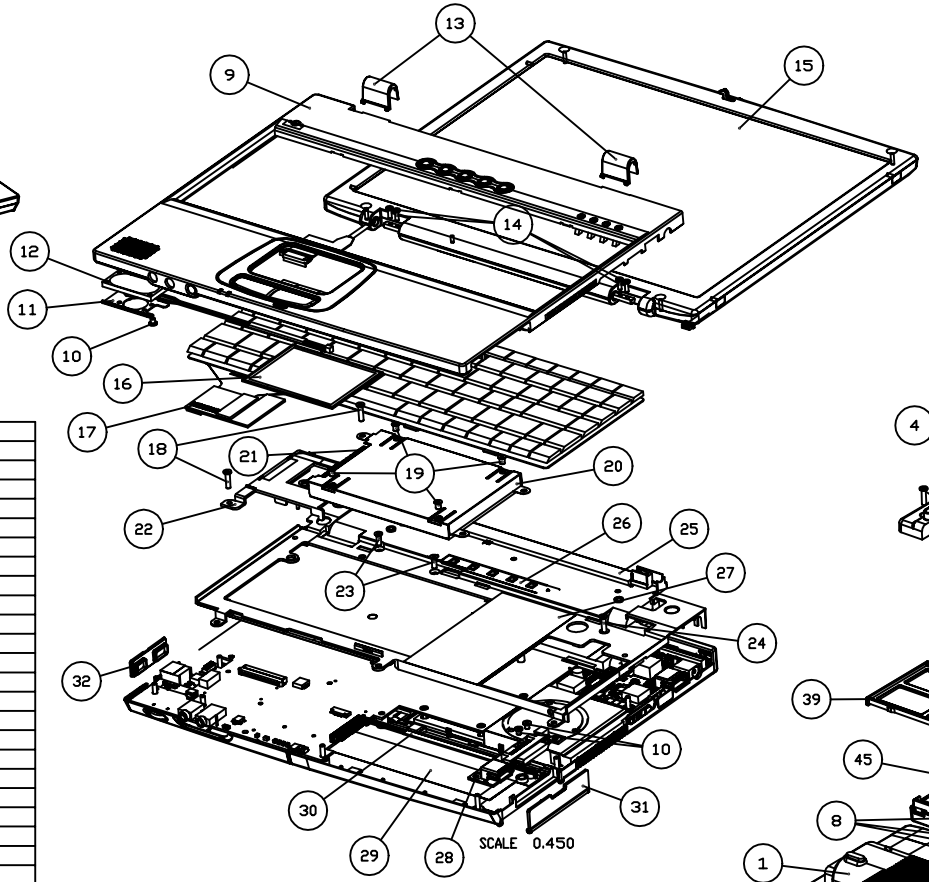

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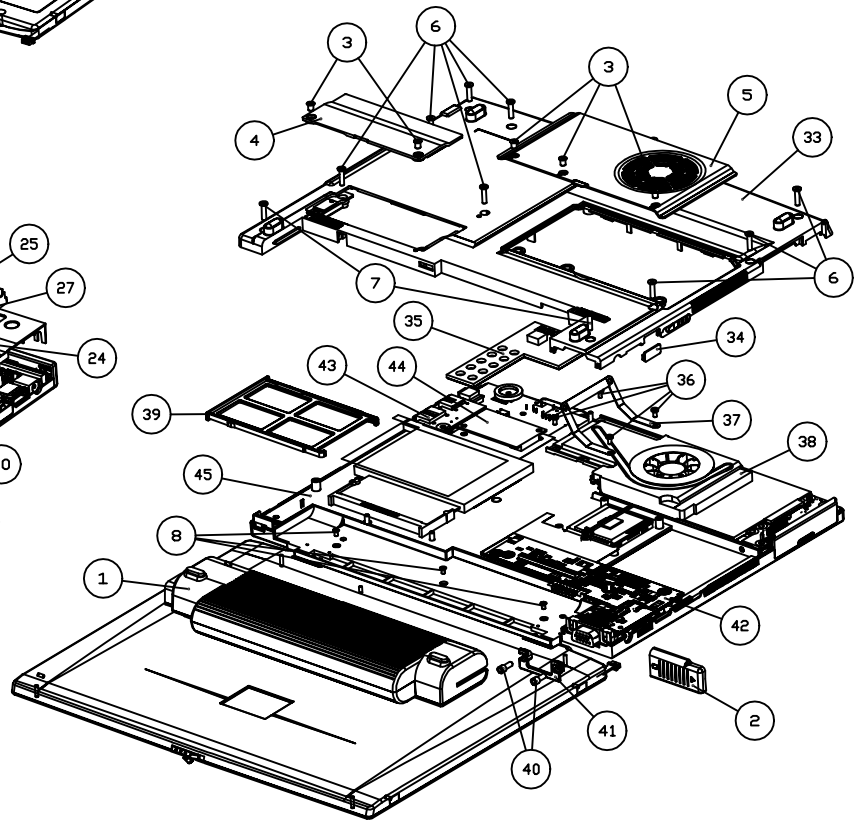


SCALE 0.450

ITEM	PART NUMBER	DESCRIPTION	QTY	REMARK
45	411672000001	PWA;PWA-M762,MOTHER,BD	1	
44	412999900037	MODEM OPTION;UNIVERSEL,MDC,M722	1	
43	411672000004	PWA;PWA-M762,MDCLAN TRANS BD	1	
42	411672000008	PWA;PWA-M762,D/D BD,T/U	1	
41	344668900030	SLIDE;VGA COVER,M722	1	
40	342668900001	STANDOFF;4-40L5.8,NIW FOR VGA CONN	2	
39	344668900053	DUMMY-CARD;PCMCIA,M722	1	
38	340672000004	HEATSINK ASSY;MFCPGA,M762	1	
37	341668300003	SPRING;HEATSINK,CPU,HOPE	1	
36	370102010303	SPC-SCREW;M2L3,NIW,K-HD(+),NYLOK	4	
35	340672000011	AL-PLATE ASSY;SIS630,M762	1	
34	344668300002	LENS;IR,HOUSING KIT;HOPE	1	
33	340672000002	HOUSING ASSY;BOTTOM,M762	1	
32	344668340001	COVER;LAN & MODEM,B-200,HOPE 2	1	
31	344668900013	DOOR;CD-ROM,M722	1	
30	421668300003	WIRE ASSY;CD-ROM,HOPE	1	
29	421668900051	FPC;CD-ROM/MB,M722	1	
28	411672000005	PWA;PWA-M762,CD-ROM TRANS BD	1	
27	346672000007	AL-FOIL;K/B REAR COVER,M762	1	
26	421668300032	FPC ASSY;QUICK KEY TO M BD,HOPE	1	
25	340672000003	COVER ASSY;REAR,M762	1	
24	370102610901	SPC-SCREW;M2.6L9,FLT(+)NIW,NYLOK	1	
23	371102610606	SCREW;M2.6L6,FLT(+),NIW/NLK,HEAT	2	
22	344668900039	HOLDER;TOUCH-PAD,2ND ID,M722	1	
21	421668300034	FPC ASSY;HDD,HOPE	1	
20	340668300022	BRACKET ASSY;HDD-2,HOPE	1	
19	370103010405	SPC-SCREW;M3L4,NIW,K-HD,T0.3	4	
18	370102610603	SPC-SCREW;M2.6L6,K-HD,NIB/NLK	2	
17	340672000012	AL-PLATE ASSY;SIS900,M762	1	
16	442668900031	TOUCH PAD MODULE;KGDDFR950A-1,APLS	1	
15	441672000001	LCD ASSY;HYUN,XGA,12.1,DIST/LEG,M762	1	
14	370102610901	SPC-SCREW;M2.6L9,FLT(+)NIW,NYLOK	4	
13	344672000034	COVER;HINGE,M762	2	
12	340672000010	SPEAKER ASSY;M762	1	
11	342668900002	BRACKET;SPEAKER,2ND ID,M722	1	
10	370102610302	SPC-SCREW;M2.6L3,NIB	3	
9	340672000001	COVER ASSY;TOP CASE,M762	1	
8	370102010281	SPC-SCREW;M2L2.8,FLT,NIW/NLK	3	
7	370102611001	SPC-SCREW;M2.6L10,NIB,K-HD,NY	2	
6	370102610602	SPC-SCREW;M2.6L6,NIB,K-HD,T0.8,NLK	9	
5	340672000017	COVER ASSY;CPU,M762	1	
4	340672000016	COVER ASSY;DIMM,M762	1	
3	371102610406	SCREW;M2.6L4,K-HEAD(+),NIB	5	
2	344668900031	COVER;VGA(NEW),M722	1	
1	442672000001	BATT ASSY;14.8V/3.3AH,LI-MOLICEL,MOLICEL,M762	1	

ITEM	CONTENTS OF CHANGE	RVS	CHK	APV	M/D/Y
					/ /
					/ /
					/ /
					/ /
					/ /

TOL± RANGE	M1	M2	S1	S2	P1	P2	C	B
0~6	.05	0.1	.15	0.2	.05	0.1	0.5	.15
6~30	0.1	0.2	.15	.25	0.1	.15	1	.15
30~80	.15	.25	0.2	0.3	0.2	0.4	2	.25
80~180	.15	0.3	.25	.45	0.4	0.8	3	.25
180~315	0.2	0.5	0.4	0.6	0.6	1.2	3	0.3
315~800	0.3	0.8	0.7	1.1	0.8	1.5	4	0.5

DATE	05/30/02	MATERIAL	SEE NOTES	TREATMENT		REMARK	
UNIT	MM	SCALE	0.45	DRAWING NAME	NB,HYUNDAI,XGA,12.1,M762		
DRAWN	DESIGNED	CHECKED	APPROVED	MATERIAL NO.	4162672000002	R00	

MiTAC International Corp.

SHEET NO. 1 OF 1

MODEL :M762 Revision 0A

Contexts

DRAWN	DESIGN	CHECK	ISSUES

History of Schematics

Rerision 00

1.Component is too high;Change C44(22uF) to C654(22uF),C623.C624 form (220uF) to (100uF)
2.No VTT_GOOD signal;Change Q4 form (DTA144WK) to (DTC144TKA),R58 form (2.2K) to (1K)
3.Improve Vcore voltage ripple;Add C644~C647.C651~C653(10uF)
4.X501(32.768KHZ) can't oscillate ;Add R555(10M)
5.Add two USB port;Add RP533(22*4),R503~R506(15K),J510.J511(USB/4P),U19.U20(NC7S08),F501.F3.F4(1.1A/6V),C280.C285(1000P),R233.R231(47K),R230.R232(33K),L46.L527(120Z/100M),L49.L53(120Z/100M),C283.C284.C288.C289(47P)C282.C648(0.1uF),Delete R131.R126.R551.R552,U510(RT9701)
6.BOM error;Change SDRAM form PC100 to PC133
7.Speedstep no function;Delete R52(10K),RP501(10K*4),Add Q20(DTC144TKA),R637~R640(10K)
8.No VTTPWRGD signal;Change R36 form (10K) to (1M)
9.Card bus can't transmission;Delete R211(10K),RP17.RP19(10K*8)
10.Prevent card can't detect;Add C547.C243(270P)
11.Cost down and shortage;Change J14 form SHARP to FOXCONN
12.Prevent audio gi noise;Change C218.C219 form (4.7uF) to (10uF),Add R634(10K),Q519(DTC144TKA),Delete R614(0)
13.No use so delete;Delete R38(10K),Q8(DTC144TKA),R68(1M),R506.R504.R507.R510.R513(10K),L509(120Z/100M),C554(0.1uF),C555(0.01uF)
14.Sometime no screen;Delect RP3.RP7.RP9 (10K*8) ,RP1 (10K*4)
15.IEEE 1394 can't transmission;Change R172 form (4.7K) to (2.49K),Delete R180(470K)
16.Sometime can't detect HDD.CD-ROM;Add R229(10K),Delete R619(0)
17.Sometime can't detect USB print port;Delete CP500(47P*4),Add C500.C501(47P)
18.MSL no H8/3434;Change H8 form (3434) to (3437),Delete R51(10K),R61(4.7K),Q9(DTC144WK),Q5(2N3906),D6(BAT54C)
19.Leakage Current ;Delete L503(120Z/100M),C509(0.1uF),D1~D4.D501.D502.D507(BAV99)
20.Cost down;Delete OSC1(25MHZ),R178(22),C201(47P),C224(10uF),L31(120Z/100M),C229(0.01uF),Add X3(25MHZ)
21.Spdif no function;Change Q512 (DTC144WK) to (DTA144WK)
22.For EMI function;Add EC20~EC23(0.1uF),E501~E504(Touchpad_metal3)
23.Spdif over specification;Change R593.R594 from 15K to 12.1K
24.Power add function;Delect PC539 ~PC541.PC545~PC547(100uF),Add PC539~PC541(220uF)
25.Cost math;Delect R50(2.7K),Change R529 from 3K to 2.2K,RP10.RP12 from (4.7K*4) to(10K*4),C52.C53 from (22P) to (47P),C540 from (2200P) to(1000P),C244.C245 from (560P) to (1000P),D7.D13 from (DAN212K) to (BAV70LT1)
R02 Modify: Replace LAN 25MHz Crystal to OSC for cann't autoload LAN's eeprom

Power Status

STATE / SIGNAL	VOTAGE	FULL ON	STR	STD	MEC-OFF	REMARK
-SUSB	+5V	HIGH	LOW	LOW	LOW	
-SUSC	+5V	HIGH	HIGH	LOW	LOW	
ADP	+19V	O	O	O	O	
BATTERY	+12V	O	O	O	O	
RTC_VCC	+1.8V	O	O	O	O	1.6V - 1.8V
CPU_CORE	+1.4(1.15)V +1.7V +1.15V	O	X	X	X	PIIIM Celeron CeleronT
VCC_CMOS15V	+1.5V	O	X	X	X	
+S1.8V	+1.8V	O	X	X	X	
+5V	+5V	O	O	X	X	
+3V	+3.3V	O	X	X	X	
+S3V	+3.3V	O	O	X	X	
VTT	+1.25V	O	X	X	X	
+5V	+5V	O	X	X	X	
+S5V	+5V	O	O	X	X	
VDDA	+5V	O	O	0	0	
+2.5V	+2.5V	O	X	X	X	
+12V	+12V	O	X	X	X	

IDSEL

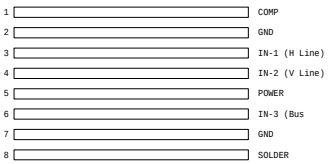
IDSEL	CHIP
AD11	VGA(N.B.)
AD12	VIA(S.B.)
AD13	SIS630(PCI Bridge)
AD19	PCMCIA
AD20	LAN
AD22	1394

BUSMASTER

REQ	CHIP
REQ0	PCMCIA
REQ1	LAN
REQ2	1394

PCIINT

PCIINT	CHIP
INTA	PCMCIA
INTB	N.B.(VGA)
INTC	LAN
INTD	1394



MiTAC

Title: COVER SHEET
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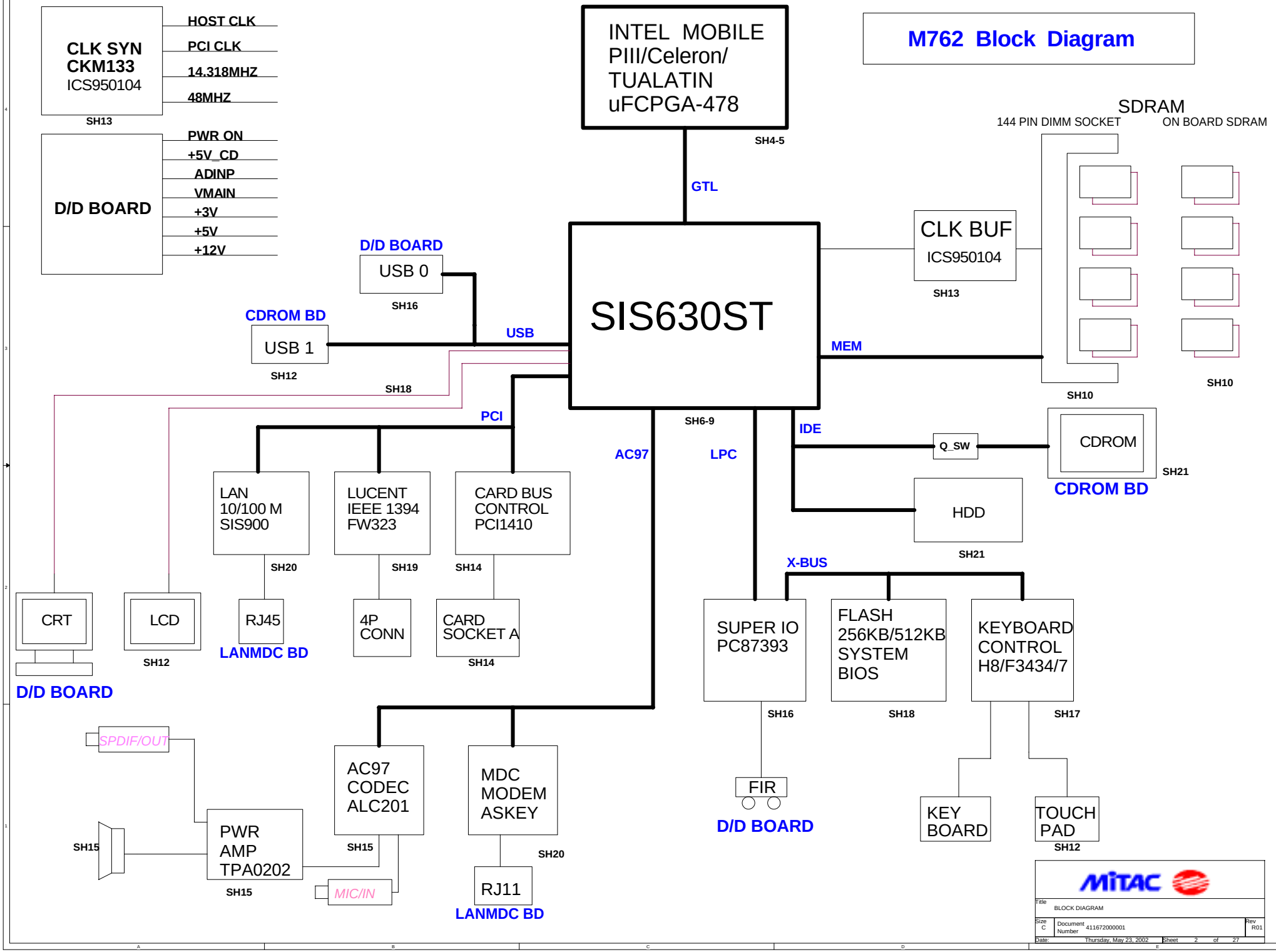
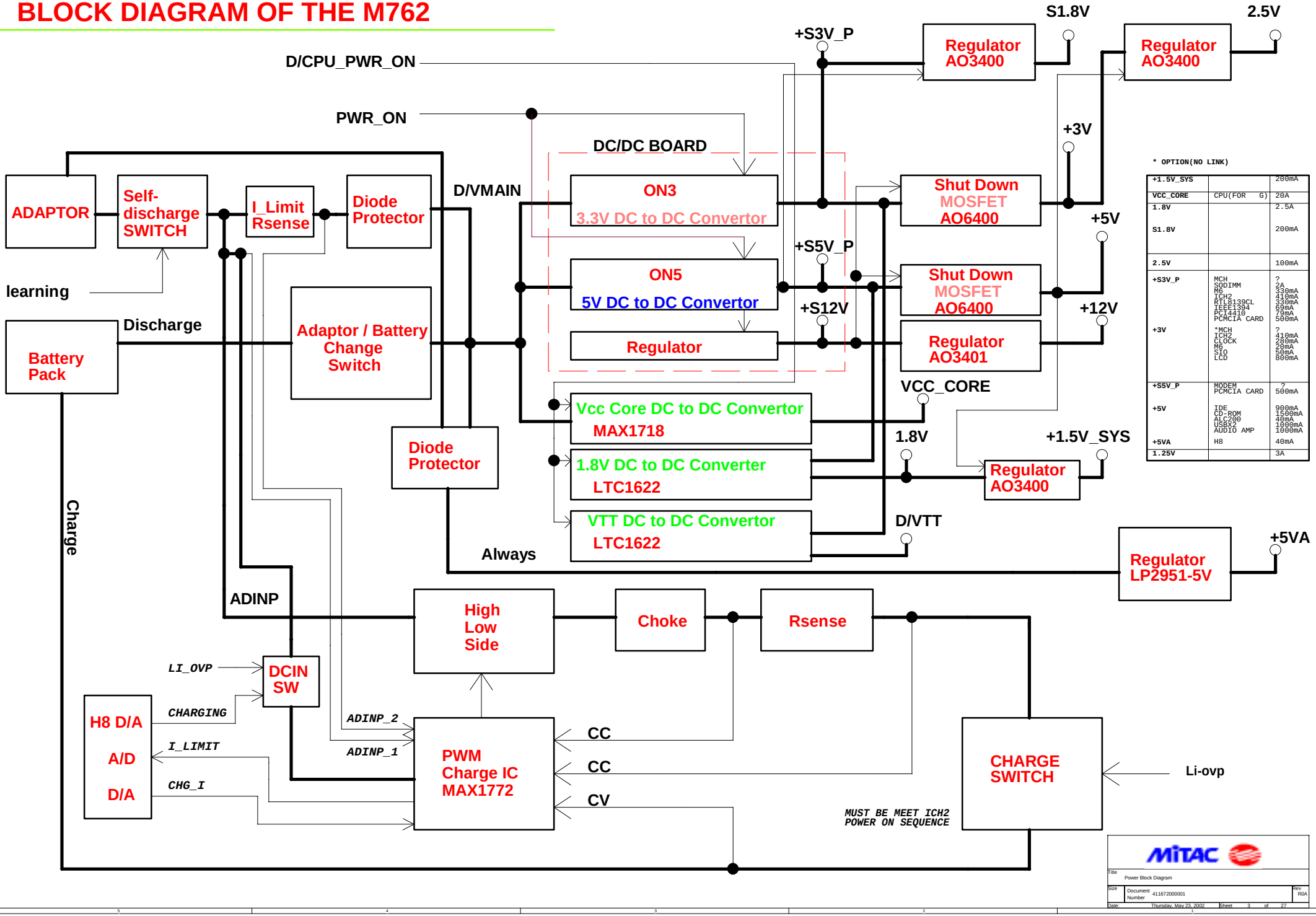
M762 Block Diagram



BLOCK DIAGRAM OF THE M762



* OPTION(NO LINK)

+1.5V_SYS		200mA
VCC_CORE	CPU(FOR G)	20A
1.8V		2.5A
S1.8V		200mA
2.5V		100mA
+S3V_P	MCH	?
	SODIMM	2A
	M6	330mA
	ICH2	410mA
	RTL8139CL	330mA
	IEEE1394	60mA
	PCI4410	79mA
	PCMCIA CARD	500mA
+3V	*MCH	?
	ICH2	410mA
	CLOCK	280mA
	M6	20mA
	SIO	50mA
	LCD	800mA
+S5V_P	MODEM	?
	PCMCIA CARD	500mA
+5V	IDE	900mA
	CD-ROM	1500mA
	ALC200	40mA
	USBX2	1000mA
	AUDIO AMP	1000mA
+5VA	H8	40mA
1.25V		3A

MiTAC

Title: Power Block Diagram

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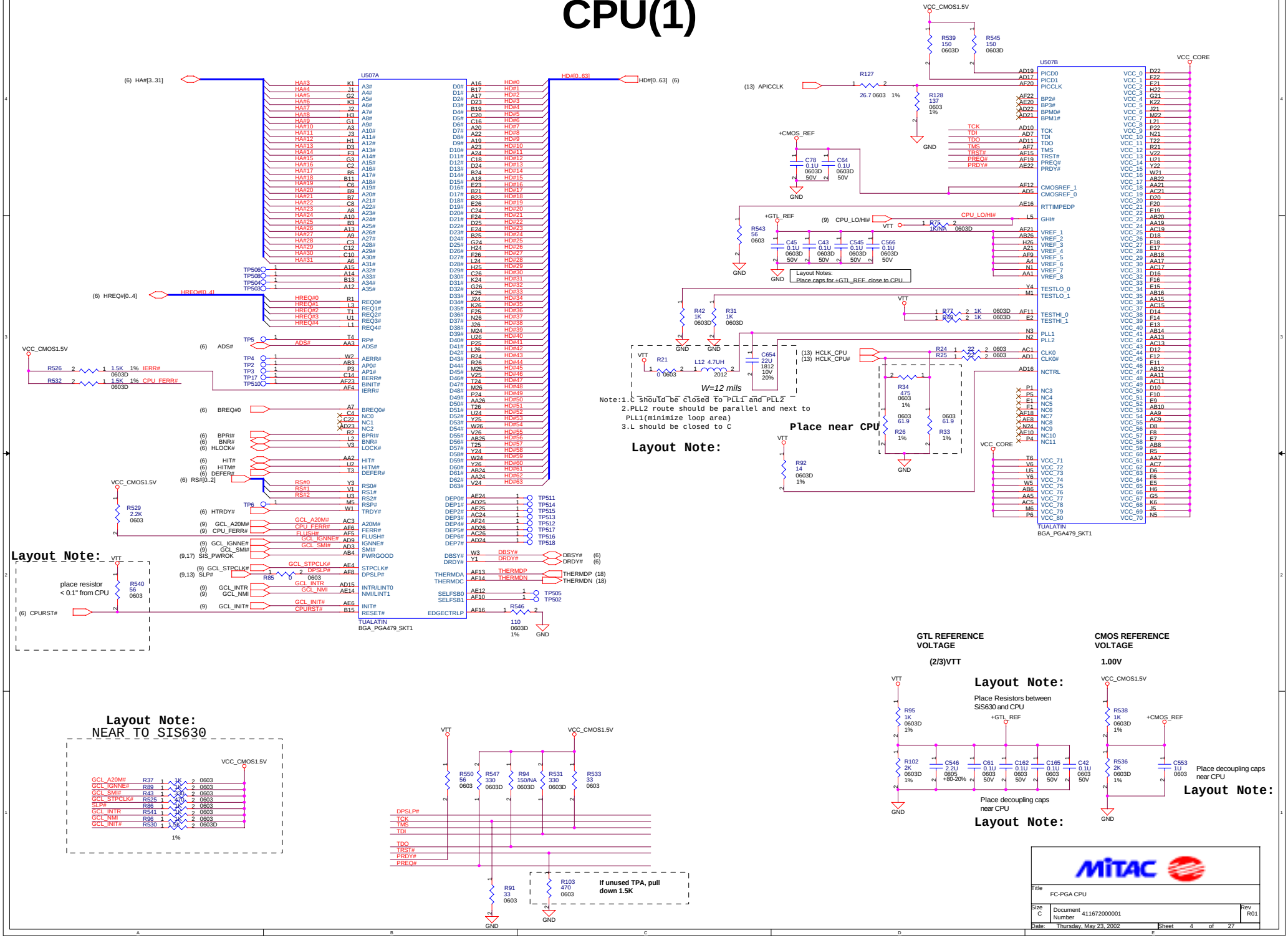
CPU(1)


U507A
TUALATIN
BGA_PGA479_SKT1
U507B
TUALATIN
BGA_PGA479_SKT1
Layout Note:
Note:1.C should be closed to PLL1 and PLL2
2.PLL2 route should be parallel and next to PLL1(minimize loop area)
3.L should be closed to C
W=12 mils
Place near CPU
Layout Note:
place resistor < 0.1" from CPU
Layout Note:
NEAR TO SIS630
GTL REFERENCE VOLTAGE
(2/3)VTT
CMOS REFERENCE VOLTAGE
1.00V
Layout Note:
Place Resistors between SiS630 and CPU
Place decoupling caps near CPU
Layout Note:
Place decoupling caps near CPU
Layout Note:
If unused TPA, pull down 1.5K
Layout Notes:
Place caps for +GTL_REF close to CPU
MiTAC
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FC-PGA CPU
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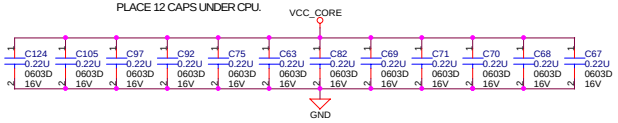
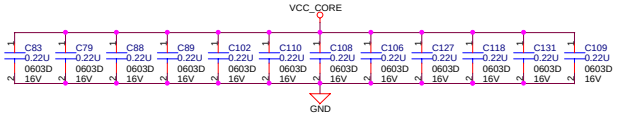
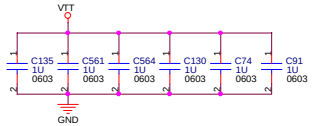
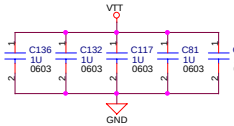
CPU(2)

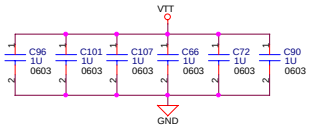
Layout Note:
PLACE CLOSE TO CPU;
PLACE 12 CAPS UNDER CPU.



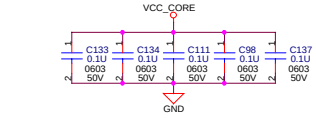


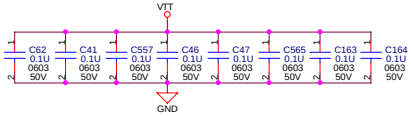


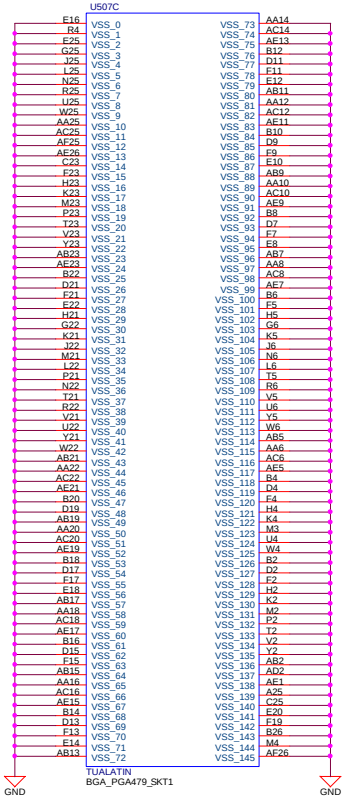


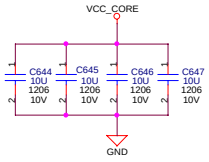


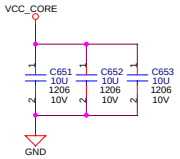
FOR EMI REQUEST.



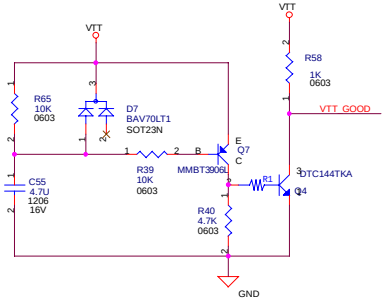


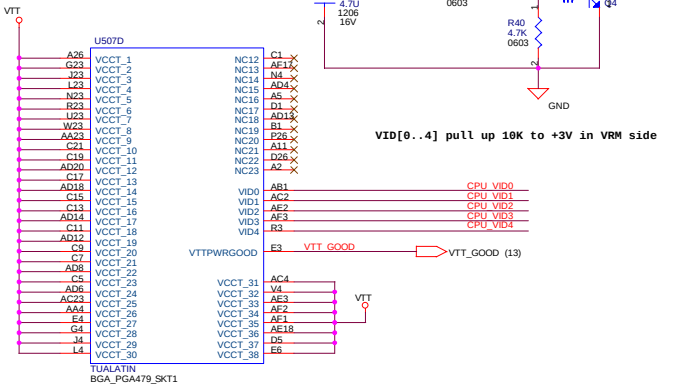




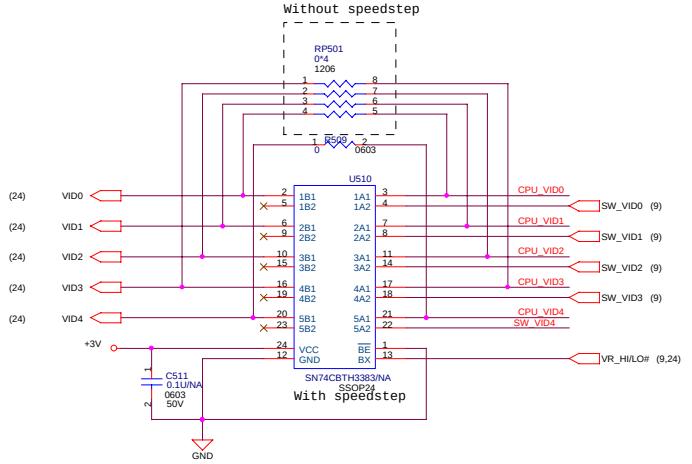


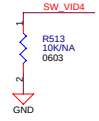
time delay for VTT_PWRGOOD
after VTT 1mS





Without speedstep





VID4	VID3	VID2	VID1	VID0	VOLT.
0	0	0	0	0	1.75
0	0	0	0	1	1.70
0	0	0	1	0	1.65
0	0	0	1	1	1.60
0	0	1	0	0	1.55
0	0	1	0	1	1.50
0	0	1	1	0	1.45
0	0	1	1	1	1.40
0	1	0	0	0	1.35
0	1	0	0	1	1.30
0	1	0	1	0	1.25
0	1	0	1	1	1.200
0	1	1	0	0	1.15
0	1	1	0	1	1.100
0	1	1	1	0	1.050
0	1	1	1	1	1.000
1	0	0	0	0	0.975
1	0	0	0	1	0.950
1	0	0	1	0	0.925
1	0	0	1	1	0.9
1	0	1	0	0	0.875
1	0	1	0	1	0.85
1	0	1	1	0	0.825
1	0	1	1	1	0.8
1	1	0	0	0	0.775
1	1	0	0	1	0.75
1	1	0	1	0	0.725
1	1	0	1	1	0.7
1	1	1	0	0	0.675
1	1	1	0	1	0.65
1	1	1	1	0	0.625
1	1	1	1	1	0.6

MiTAC

Title: FC-PGA CPU

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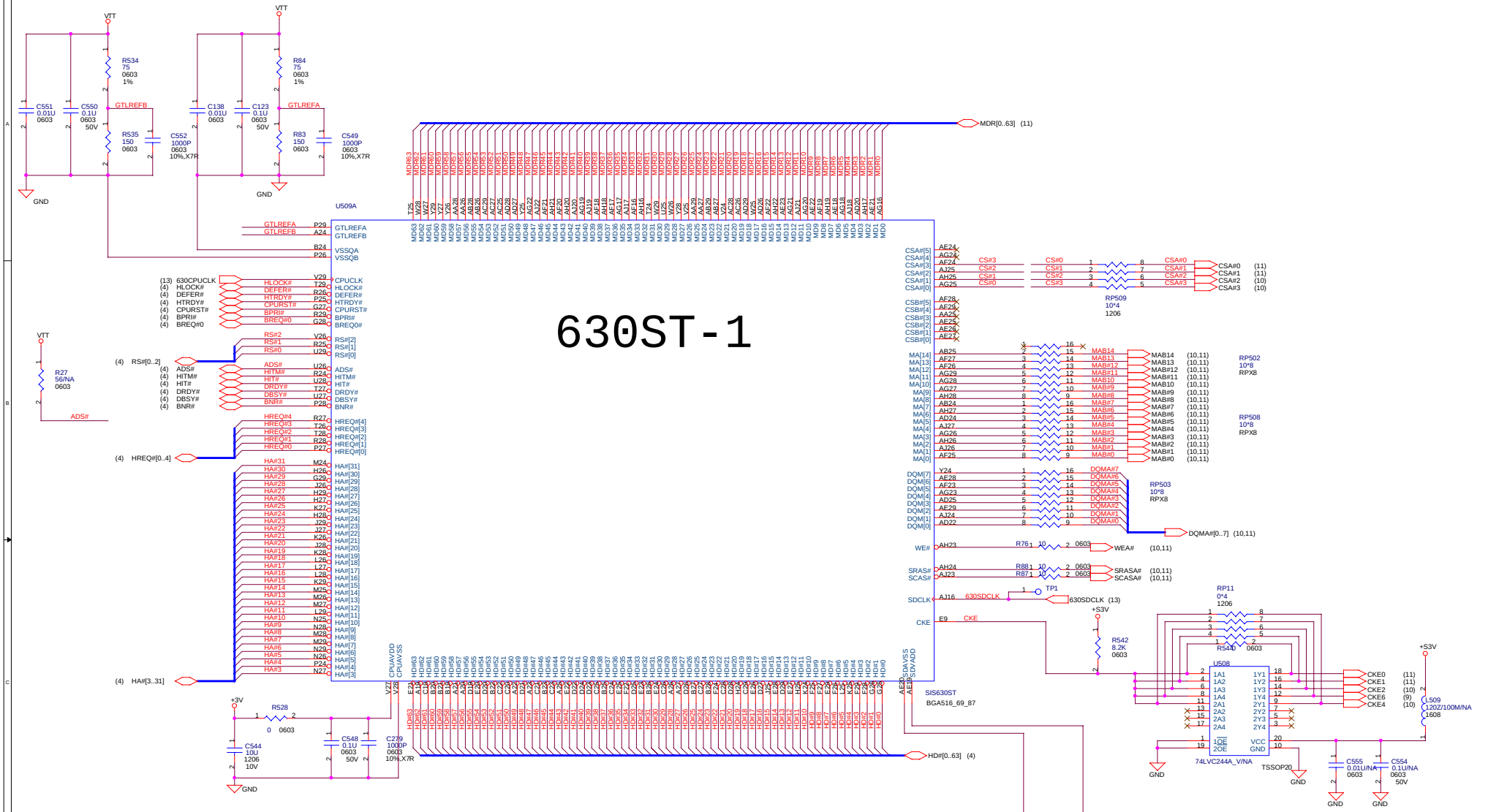
630ST-1



Title	SIS 630ST	
Size C	Document Number 411672000001	Rev R0A
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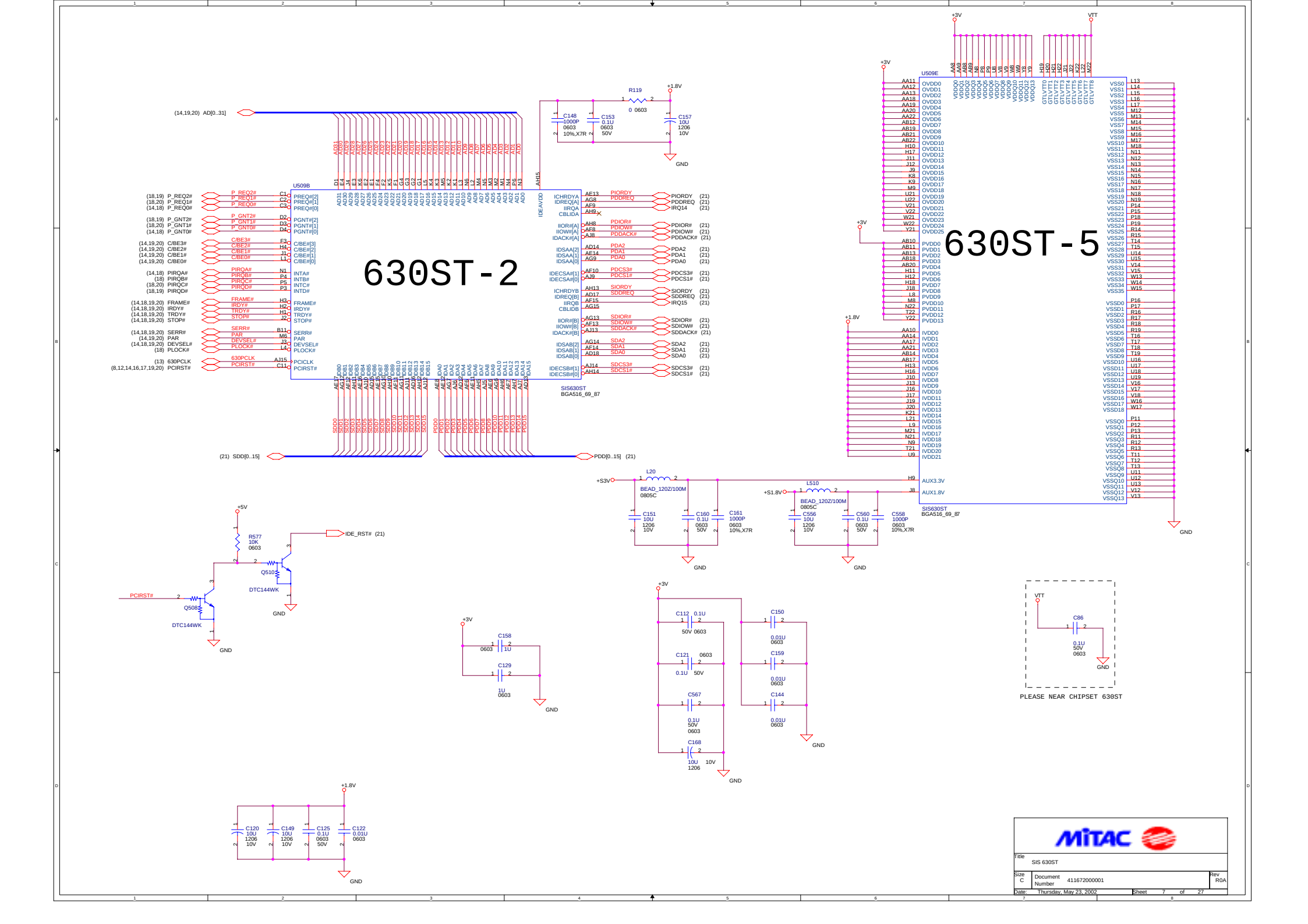
630ST-2
630ST-5
U509B
U509E
SIS630ST
BGA516_69_87
(14,19,20) AD[0..31]
(21) SDD[0..15]
PDD[0..15] (21)
P_REQ2#
P_REQ1#
P_REQ0#
P_GNT2#
P_GNT1#
P_GNT0#
C/BE3#
C/BE2#
C/BE1#
C/BE0#
PIRQA#
PIRQB#
PIRQC#
PIRQD#
FRAME#
IRDY#
TRDY#
STOP#
SERR#
PAR
DEVSEL#
PLOCK#
630PCLK
PCIRST#
PCICLK
IDE_RST# (21)
PLEASE NEAR CHIPSET 630ST
Title
SIS 630ST
Size
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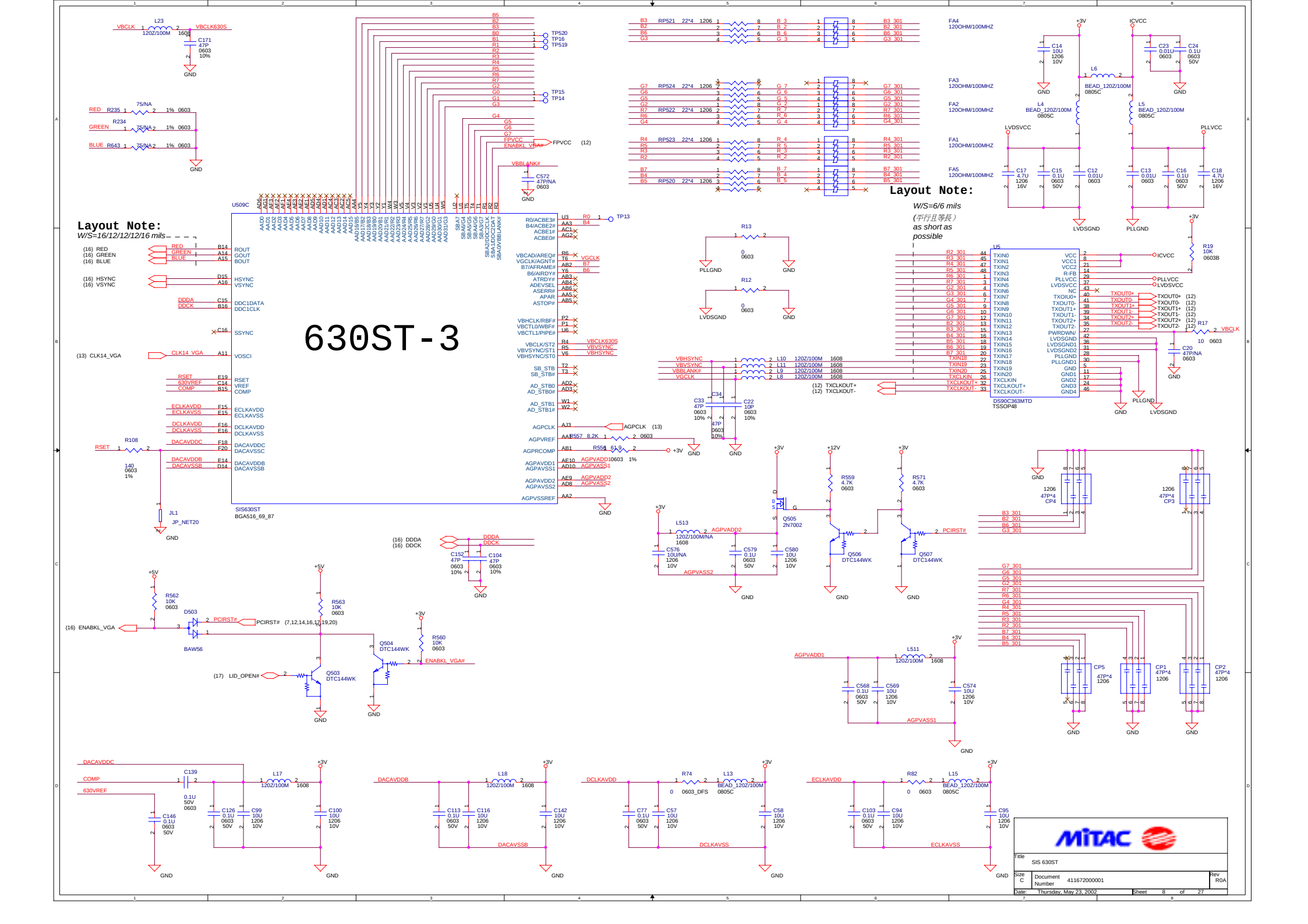
630ST-3
Layout Note:
W/S=16/12/12/12/16 mils
Layout Note:
W/S=6/6 mils
(平行且等長)
as short as possible
SIS630ST
BGA516_69_87
U509C
U5
DS90C363MTD
TSSOP48
U3
BAW56
Q503 DTC144WK
Q504 DTC144WK
Q505 2N7002
Q506 DTC144WK
Q507 DTC144WK
JL1 JP_NET20
L23 120Z/100M 1608
L4 BEAD_120Z/100M 0805C
L5 BEAD_120Z/100M 0805C
L6 BEAD_120Z/100M 0805C
L17 120Z/100M 1608
L18 120Z/100M 1608
L511 120Z/100M 1608
L513 120Z/100M/NA 1608
L10 120Z/100M 1608
L11 120Z/100M 1608
L9 120Z/100M 1608
L8 120Z/100M 1608
L13 BEAD_120Z/100M 0805C
L15 BEAD_120Z/100M 0805C
RP521 22*4 1206
RP524 22*4 1206
RP522 22*4 1206
RP523 22*4 1206
RP520 22*4 1206
FA1 120OHM/100MHZ
FA2 120OHM/100MHZ
FA3 120OHM/100MHZ
FA4 120OHM/100MHZ
FA5 120OHM/100MHZ
TP520
TP16
TP519
TP15
TP14
TP13
C171 47P 0603 10%
C572 47P/NA 0603
C139 0.1U 50V 0603
C146 0.1U 0603 50V
C126 0.1U 0603 50V
C99 10U 1206 10V
C100 10U 1206 10V
C113 0.1U 0603 50V
C116 10U 1206 10V
C142 10U 1206 10V
C77 0.1U 0603 50V
C57 10U 1206 10V
C58 10U 1206 10V
C103 0.1U 0603 50V
C94 10U 1206 10V
C95 10U 1206 10V
C568 0.1U 0603 50V
C569 10U 1206 10V
C574 10U 1206 10V
C576 10U/NA 1206 10V
C579 0.1U 0603 50V
C580 10U 1206 10V
C33 47P 0603 10%
C22 10P 0603 10%
C34 47P 0603 10%
C152 47P 0603 10%
C104 47P 0603 10%
C14 10U 1206 10V
C23 0.01U 0603
C24 0.1U 0603 50V
C17 4.7U 1206 16V
C15 0.1U 0603 50V
C12 0.01U 0603
C13 0.01U 0603
C16 0.1U 0603 50V
C18 4.7U 1206 16V
C20 47P/NA 0603
R235 75/NA 1% 0603
R234 75/NA 1% 0603
R643 75/NA 1% 0603
R108 140 0603 1%
R562 10K 0603
R563 10K 0603
R560 10K 0603
R559 4.7K 0603
R571 4.7K 0603
R13 0 0603
R12 0 0603
R19 10K 0603B
R17 10 0603
R557 8.2K 0603
R554 61.9 0603 1%
CP1 47P*4 1206
CP2 47P*4 1206
CP3 47P*4 1206
CP4 47P*4 1206
CP5 47P*4 1206
GND
+3V
+5V
+12V
LVDSVCC
PLLVCC
LVDSGND
PLLGND
ICVCC
VBCLK630S
RED
GREEN
BLUE
HSYNC
VSYNC
DDCA
DDCK
SSYNC
CLK14_VGA
RSET
COMP
630VREF
ECLKAVDD
ECLKAVSS
DCLKAVDD
DCLKAVSS
DACAVDDC
DACAVSSC
DACAVDDB
DACAVSSB
AGPCLK
AGPVREF
AGPRCOMP
AGPAVDD1
AGPAVSS1
AGPAVDD2
AGPAVSS2
AGPVSSREF
VBHSYNC
VBVSYNC
VBBLANK#
VGCLK
VBLANK#
FPVCC
ENABKL_VGA#
PCIRST#
LID_OPEN#
ENABKL_VGA
TXOUT0+
TXOUT0-
TXOUT1+
TXOUT1-
TXOUT2+
TXOUT2-
TXCLKOUT+
TXCLKOUT-
MiTAC
Title
SIS 630ST
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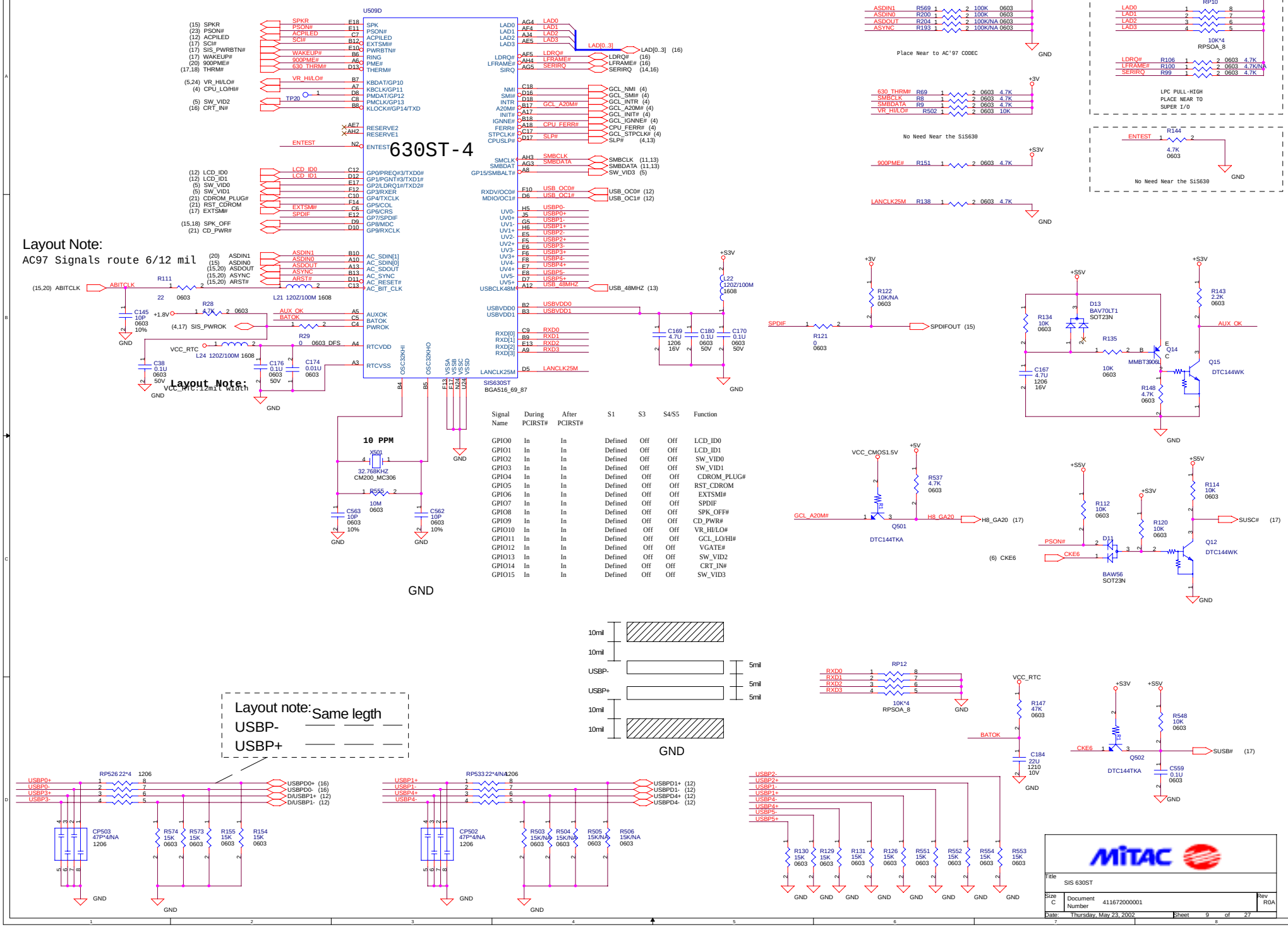
U509D
630ST-4
SIS630ST
BGA516_69_87
Layout Note:
AC97 Signals route 6/12 mil
Layout Note:
VCC_RTC:12mil width
10 PPM
32.768KHZ
CM200_MC306
GND
Signal Name | During PCIRST# | After PCIRST# | S1 | S3 | S4/S5 | Function
GPIO0 In In Defined Off Off LCD_ID0
GPIO1 In In Defined Off Off LCD_ID1
GPIO2 In In Defined Off Off SW_VID0
GPIO3 In In Defined Off Off SW_VID1
GPIO4 In In Defined Off Off CDROM_PLUG#
GPIO5 In In Defined Off Off RST_CDROM
GPIO6 In In Defined Off Off EXTSMI#
GPIO7 In In Defined Off Off SPDIF
GPIO8 In In Defined Off Off SPK_OFF#
GPIO9 In In Defined Off Off CD_PWR#
GPIO10 In In Defined Off Off VR_HI/LO#
GPIO11 In In Defined Off Off GCL_LO/HI#
GPIO12 In In Defined Off Off VGATE#
GPIO13 In In Defined Off Off SW_VID2
GPIO14 In In Defined Off Off CRT_IN#
GPIO15 In In Defined Off Off SW_VID3
Layout note: Same legth
USBP-
USBP+
10mil
5mil
Place Near to AC'97 CODEC
No Need Near the SiS630
LPC PULL-HIGH
PLACE NEAR TO
SUPER I/O
MiTAC
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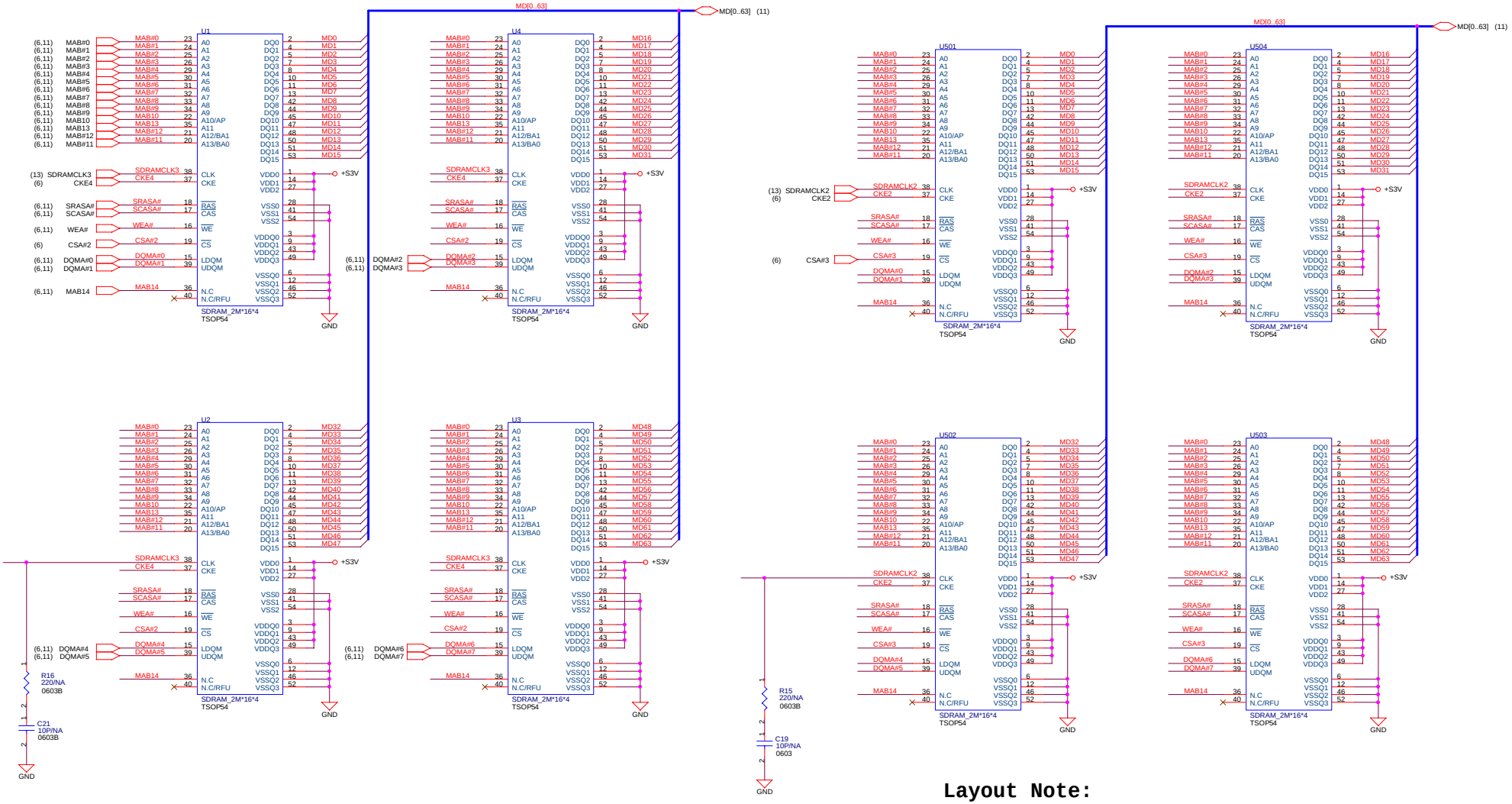
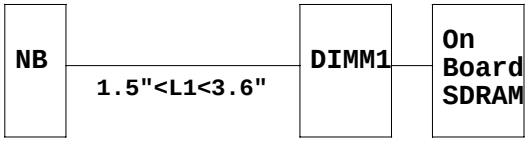
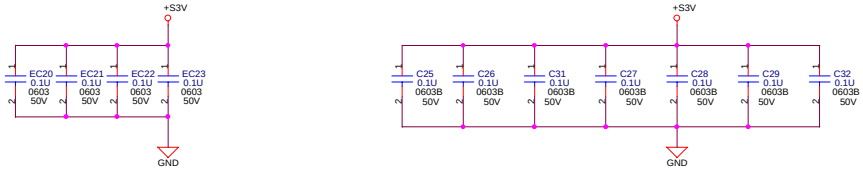
2M X 16 BITS X 4 BANK X 8 = 128M BYTES



Layout Note:





MiTAC

Title	ON BOARD 128MB SDRAM	
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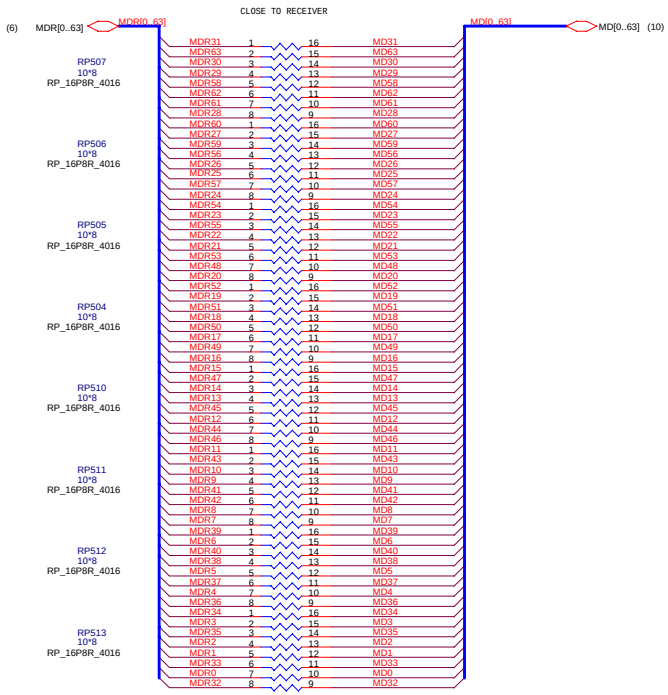
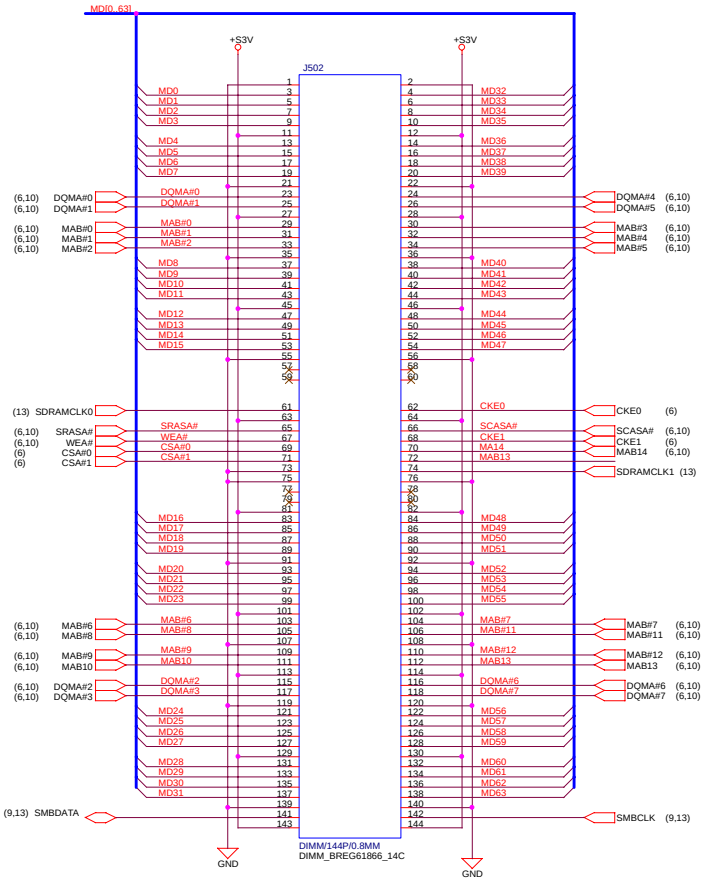
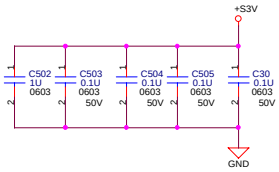
144 PIN SODIMM SOCKET







Title	SO-DIMM SOCKET	
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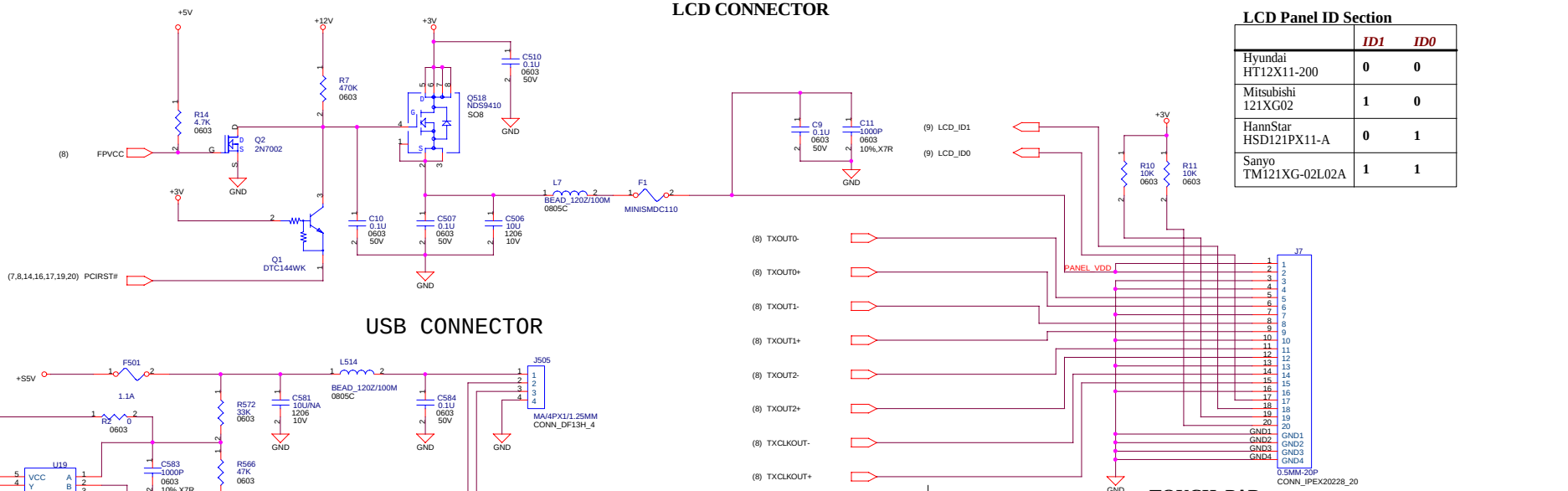
LCD CONNECTOR

LCD Panel ID Section

	ID1	ID0
Hyundai HT12X11-200	0	0
Mitsubishi 121XG02	1	0
HannStar HSD121PX11-A	0	1
Sanyo TM121XG-02L02A	1	1

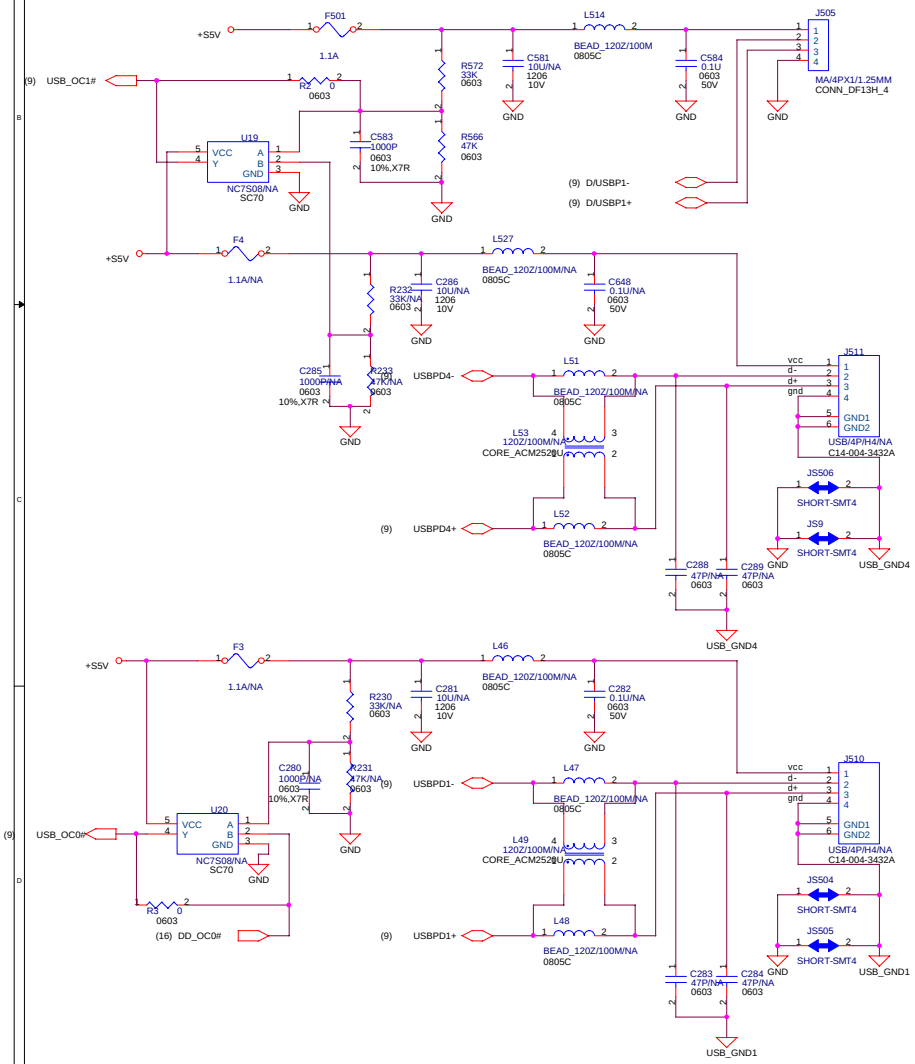


Layout Note:

S/W/W/S=12/6/6/12 mils as short as possible

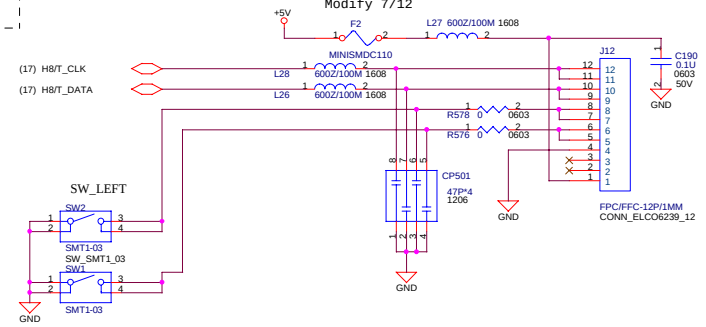
四組各自平行走線等長

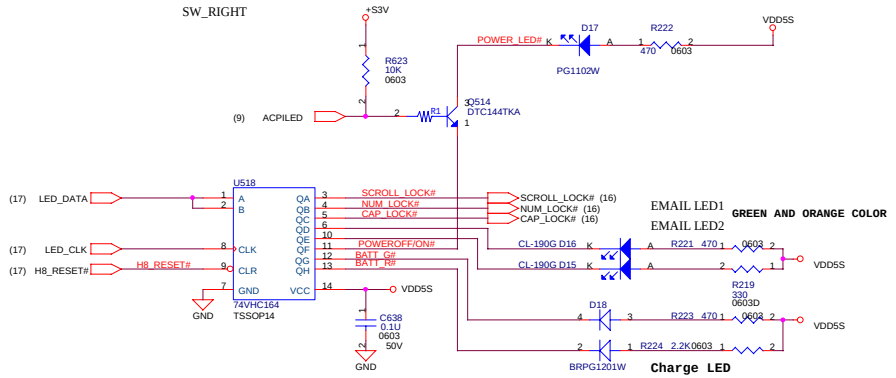
USB CONNECTOR



TOUCH_PAD

Modify 7/12





MiTAC	Title: DISPLAY INTERFACE		
	Size: C	Document Number: 411672000001	Rev: R0A
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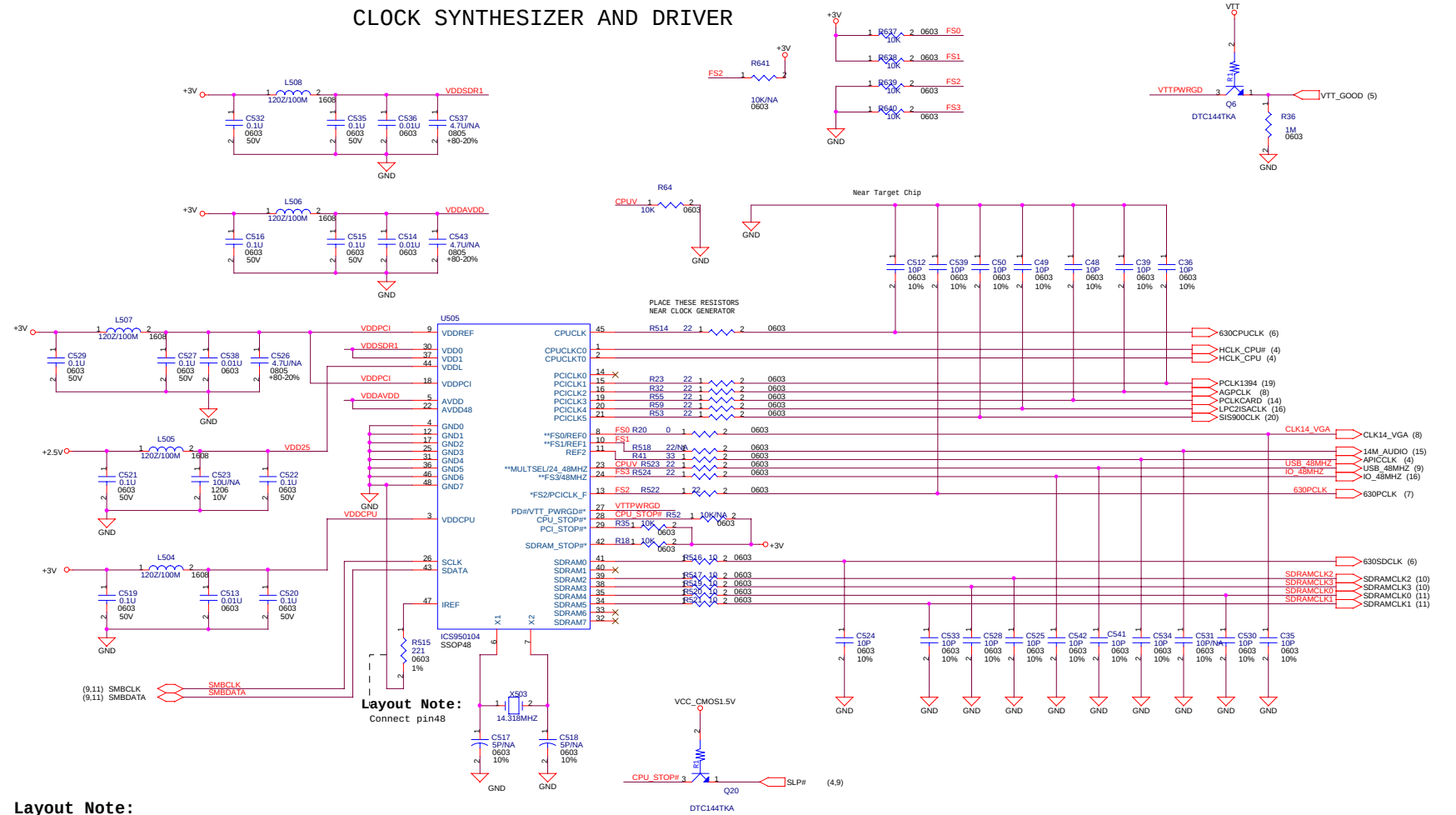
CLOCK SYNTHESIZER AND DRIVER



Layout Note:

Signal Name	Trace Length	Limit	W/S
CPUCLK	Lsd+5.0"	6" -`10"	6/12
HCLKCPU/#	Lsd+3.8"	4.8" -8.8"	6/12
630SDCLK	Lsd+5.0"	6" -`10"	6/12
SDRAMCLK0	Lsd	1" - 5"	6/12
SDRAMCLK1	Lsd	1" - 5"	6/12
SDRAMCLK2	Lsd+1.7"	1.7" -6.7"	6/12
SDRAMCLK3	Lsd+1.7"	1.7" -6.7"	6/12
630PCLK	Lpci	4" -15"	6/12
PCLKCARD	Lpci	4" -15"	6/12
PCLK1394	Lpci"	1" -12"	6/12
AGPPCLK	Lpci	4" -15"	6/12
LPC2ISACLK	Lpci	4" -15"	6/12
SIS900CLK	Lpci	4" -15"	6/12
IO_48MHZ			6/12
USB_48MHZ			6/12
CLK14_VGA			6/12
14M_GCL			6/12
APICCLK1			6/12

愈短愈好

9248-102 FREQUENCY SUPPORT

(FS3) SW4	(FS2) SW3	(FS1) SW2	(FS0) SW1	CPU (MHz)	SDRAM (MHz)	PCI (MHz)	REF (MHz)
0	0	0	0	66.7	100	33.33	14.318
0	0	0	1	100	100	33.33	14.318
0	0	1	0	150	100	37.59	14.318
0	0	1	1	133	100	33.33	14.318
0	1	0	0	66	133	33.33	14.318
0	1	0	1	100	133	33.33	14.318
0	1	1	0	100	150	37.59	14.318
0	1	1	1	133	133	33.33	14.318
1	0	0	0	66.7	66.7	33.33	14.318
1	0	0	1	83.3	83.3	27.78	14.318
1	0	1	0	90	90	30	14.318
1	0	1	1	95	95	31.67	14.318
1	1	0	0	95	126.67	31.67	14.318
1	1	0	1	112	112	37.34	14.318
1	1	1	0	166	111	27.67	14.318
1	1	1	1	166	166	27.67	14.318

0:OFF
1:ON

MiTAC

Title	CLOCK GENERATOR-ICS	
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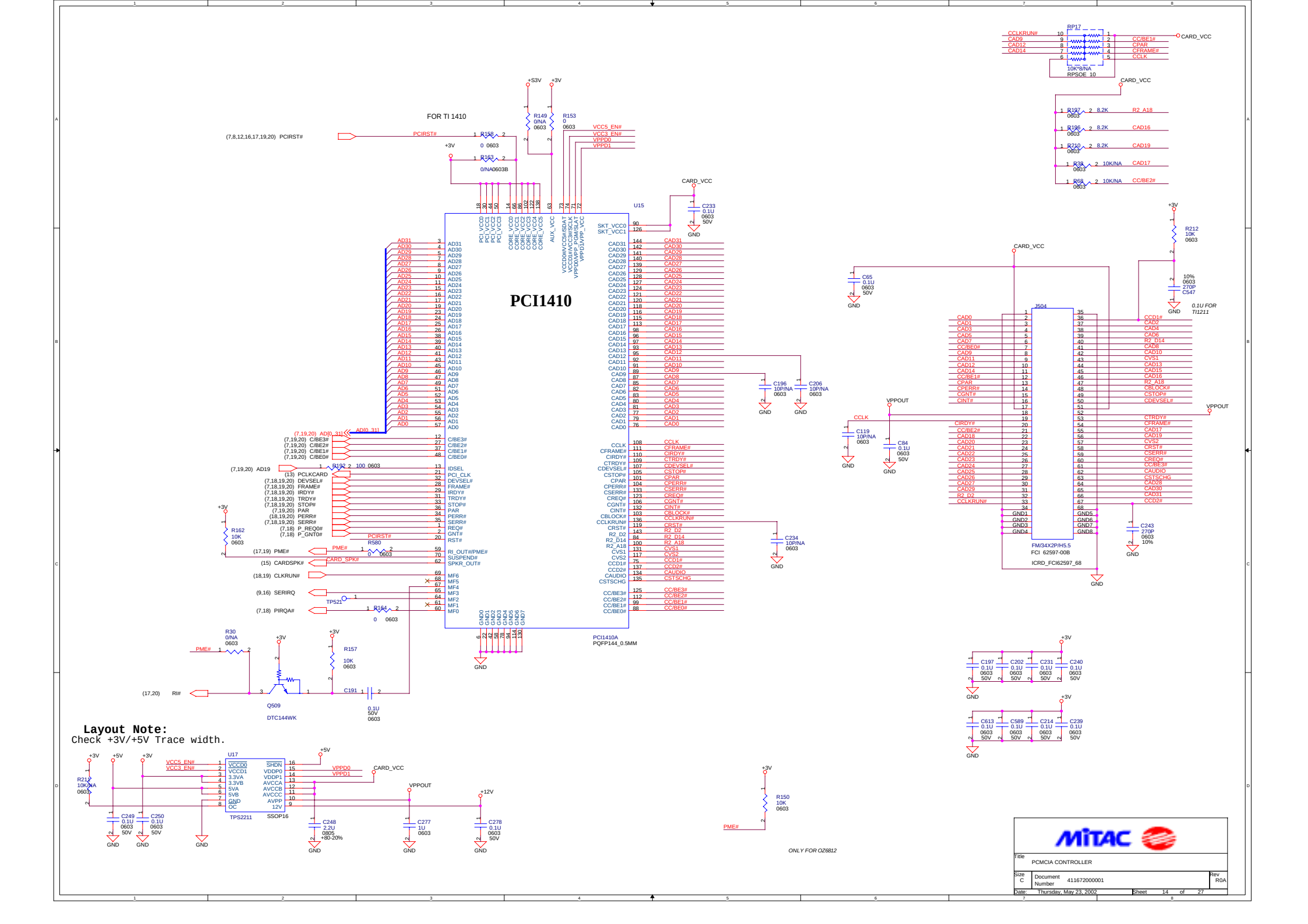
PCI1410
FOR TI 1410
U15
PCI1410A
PQFP144_0.5MM
Layout Note:
Check +3V/+5V Trace width.
U17
TPS2211
SSOP16
ONLY FOR OZ6812
J504
FM/34X2P/H5.5
FCI 62597-00B
ICRD_FCI62597_68
0.1U FOR TI1211
RP17
RPSOE_10
10K*8/NA
CARD_VCC
VPPOUT
Q509
DTC144WK
TPS521
PCIRST#
PME#
CARD_SPK#
CCLK
SERIRQ
PIRQA#
CLKRUN#
RI#
Title
PCMCIA CONTROLLER
Size
C
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411672000001
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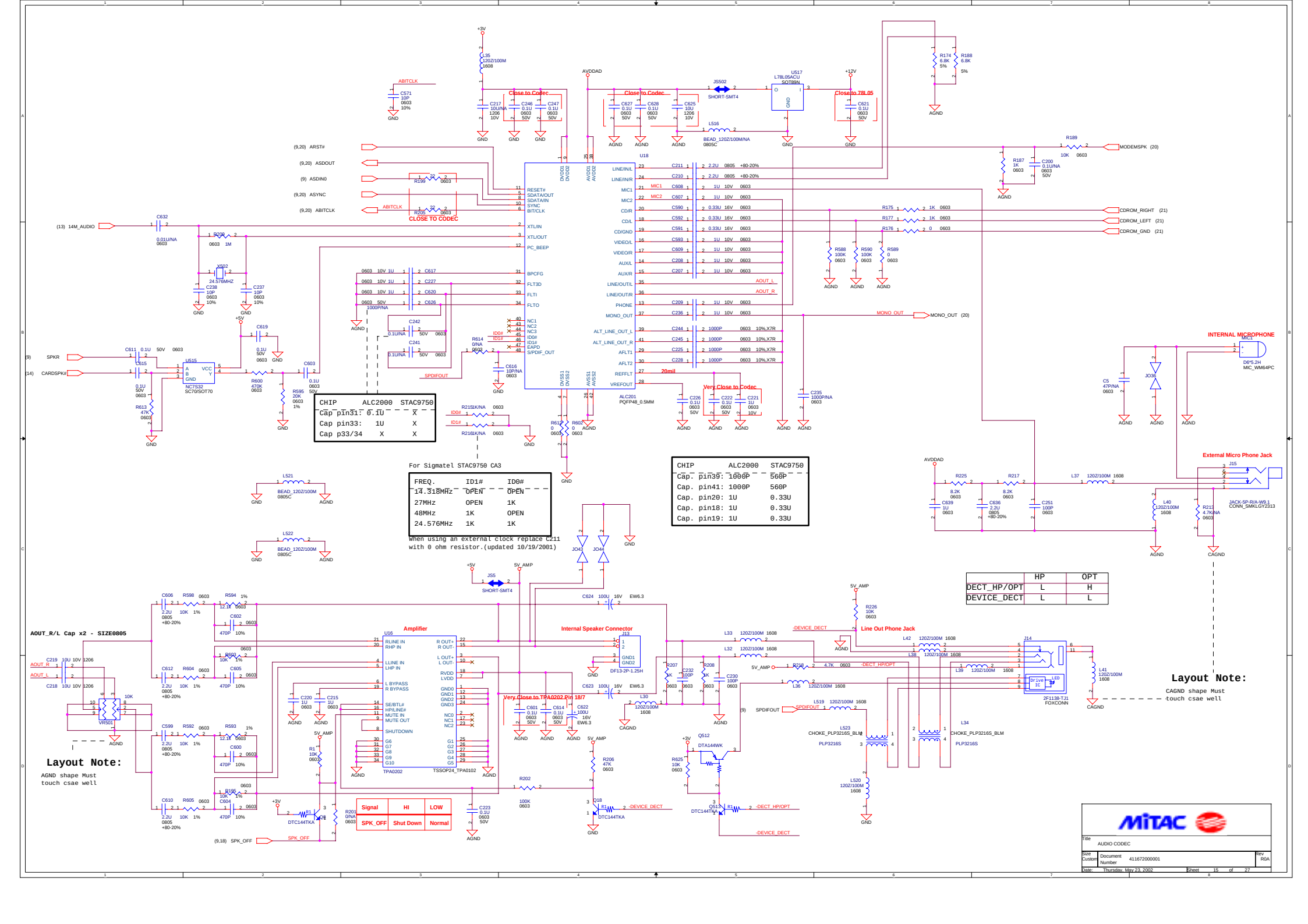
27


CHIP ALC2000 STAC9750
Cap pin31: 0.1U X
Cap pin33: 1U X
Cap p33/34 X X
For Sigmatel STAC9750 CA3
FREQ. ID1# ID0#
14.318MHz OPEN OPEN
27MHz OPEN 1K
48MHz 1K OPEN
24.576MHz 1K 1K
When using an external clock replace C211 with 0 ohm resistor.(updated 10/19/2001)
CHIP ALC2000 STAC9750
Cap. pin39: 1000P 560P
Cap. pin41: 1000P 560P
Cap. pin20: 1U 0.33U
Cap. pin18: 1U 0.33U
Cap. pin19: 1U 0.33U
HP OPT
DECT_HP/OPT L H
DEVICE_DECT L L
Signal HI LOW
SPK_OFF Shut Down Normal
Layout Note:
AGND shape Must
touch csae well
Layout Note:
CAGND shape Must
touch csae well
AOUT_R/L Cap x2 - SIZE0805
INTERNAL MICROPHONE
External Micro Phone Jack
Line Out Phone Jack
Internal Speaker Connector
Amplifier
CLOSE TO CODEC
Close to Codec
Close to 78L05
Very Close to Codec
20mil
ALC201 PQFP48_0.5MM
TPA0202
TSSOP24_TPA0102
MIC_WM64PC
JACK-5P-R/A-W9.1
CONN_SMKLGY2313
2F1138-TJ1 FOXCONN
MITAC
AUDIO CODEC
Document Number 411672000001
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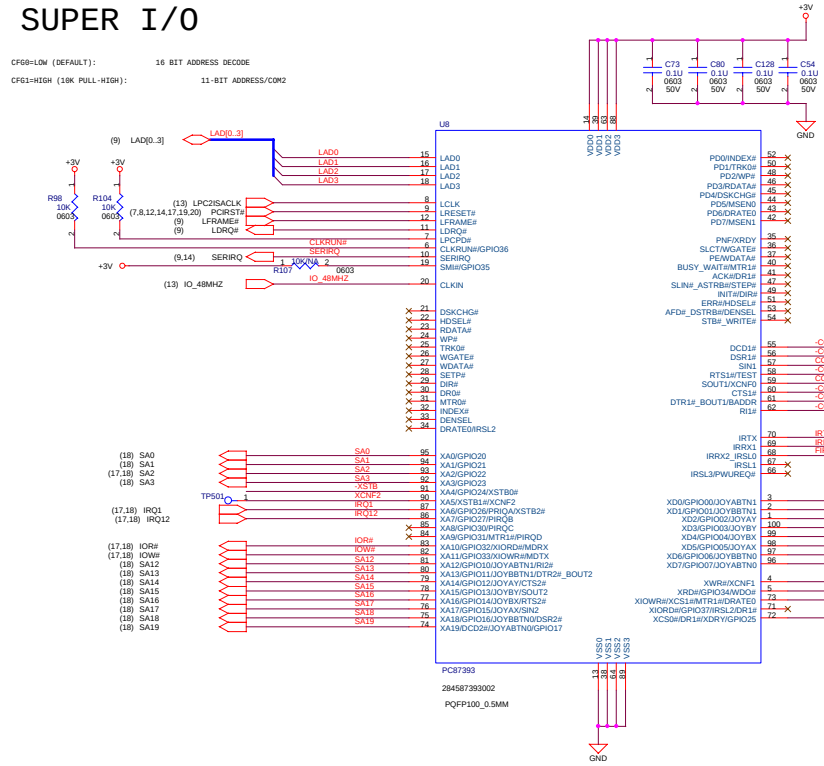
SUPER I/O

CFG0=LOW (DEFAULT): 16 BIT ADDRESS DECODE

CFG1=HIGH (10K PULL-HIGH): 11-BIT ADDRESS/COM2



STRAP OPTION

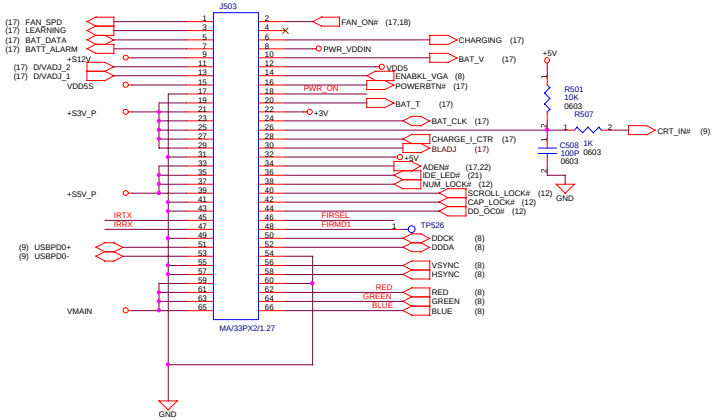
XCNF2	XCNF1	XCNF0	FUNCTIONALITY
X	0	0	NO BIOS
X	0	1	NORMAL MODE , XRDY DISABLE
0	1	0	LATCH MODE ,XA12-19, XRDY ENABLE
1	1	0	LATCH MODE , GPIO 10-17 , XRDY ENABLE
0	1	1	LATCH MODE , XA12-19, XRDY DISABLE
1	1	1	LATCH MODE , GPIO 10-17 ,XRDY DISABLE

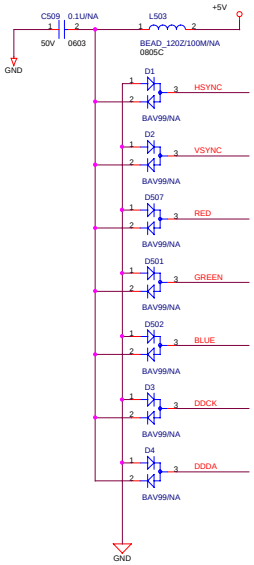
BASE ADDRESS SELECT

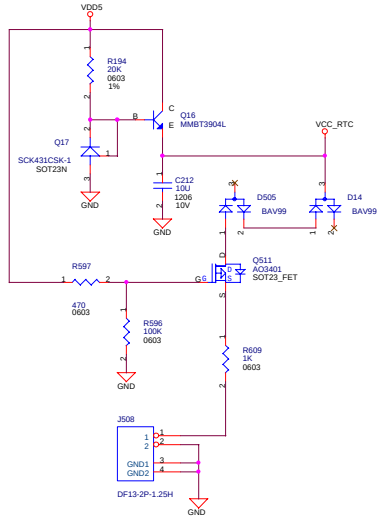
R303	INDEX REGISTER	DATA REGISTER
MOUNTED	4EH	4FH
OPEN	2EH	2FH

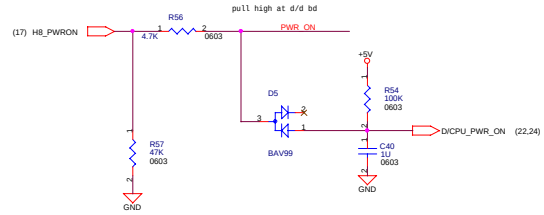
D/D CONNECTOR

Layout Note:
J503 pin23 and
J503 pin32 trace 40 mil









MiTAC

Title: SUPER I/O&D/D CONNECTOR

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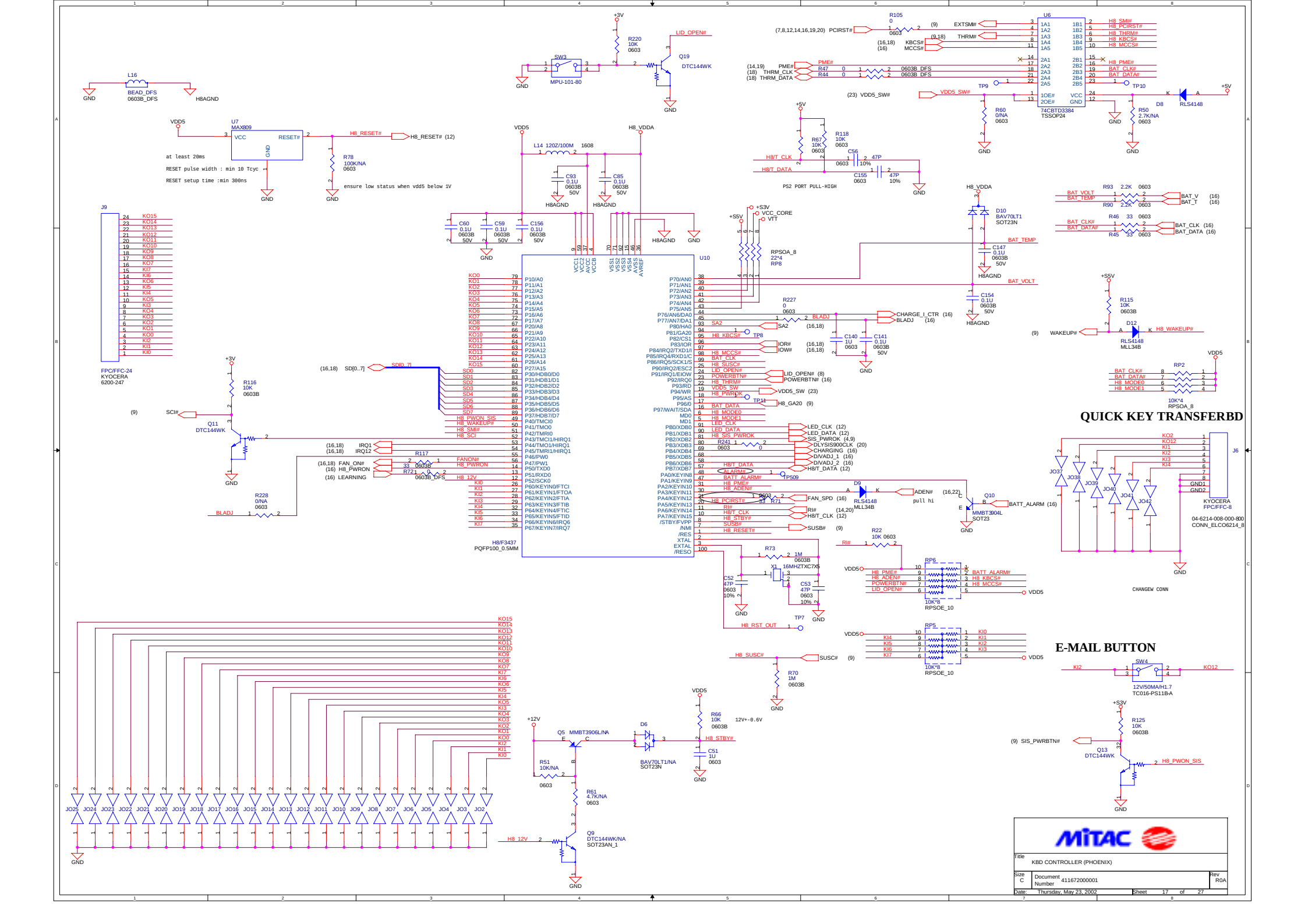
QUICK KEY TRANSFERBD
E-MAIL BUTTON
CHANGEW CONN
MiTAC
Title
KBD CONTROLLER (PHOENIX)
Size C
Document Number 411672000001
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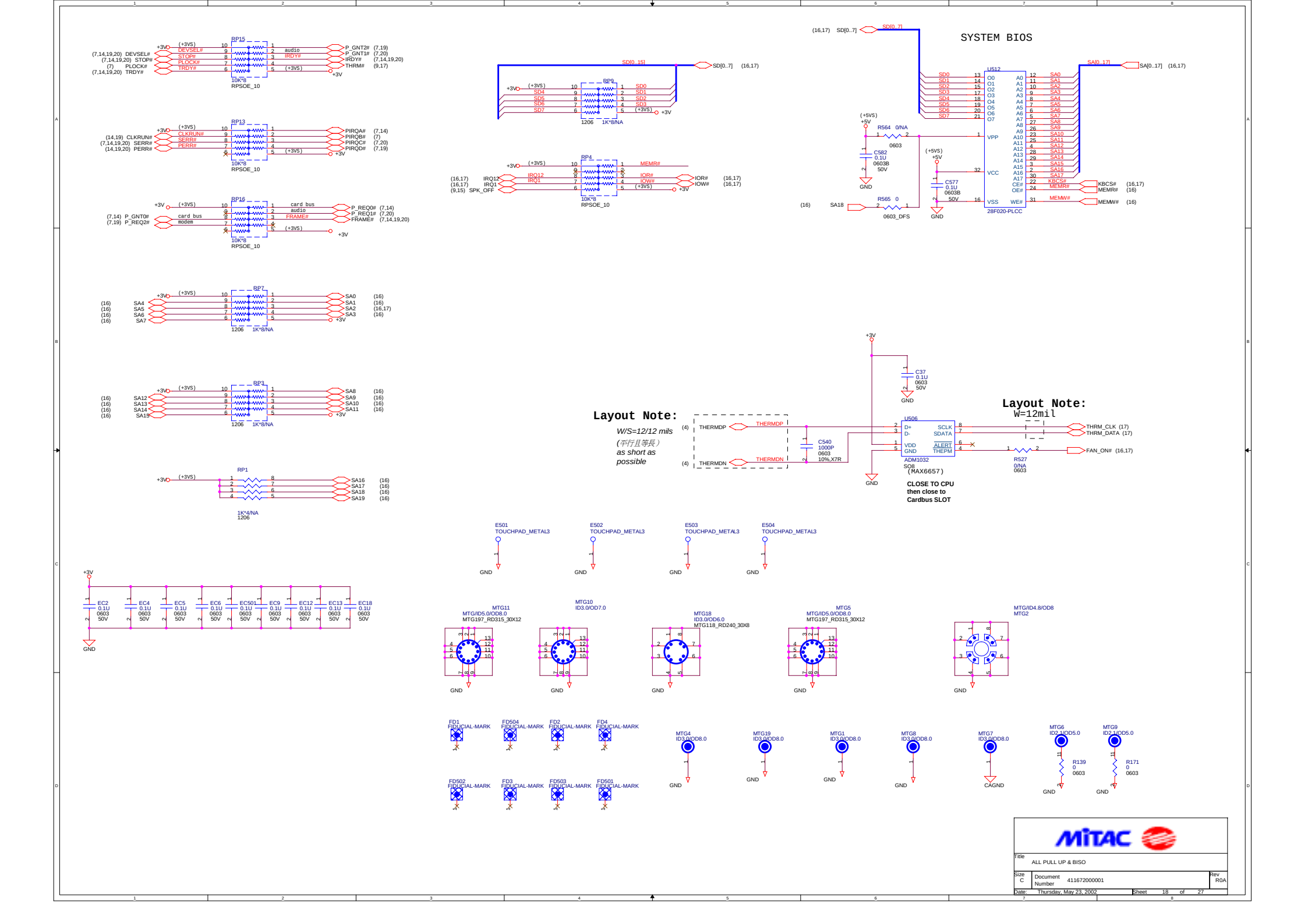
SYSTEM BIOS
Layout Note:
W/S=12/12 mils
(平行且等長)
as short as
possible
Layout Note:
W=12mil
CLOSE TO CPU
then close to
Cardbus SLOT
RP15
RP13
RP16
RP7
RP3
RP1
RP9
RP4
U12
28F020-PLCC
U506
ADM1032
SO8
(MAX6657)
RPSOE_10
1206 1K*8/NA
1K*4/NA
MITAC
Title
ALL PULL UP & BISO
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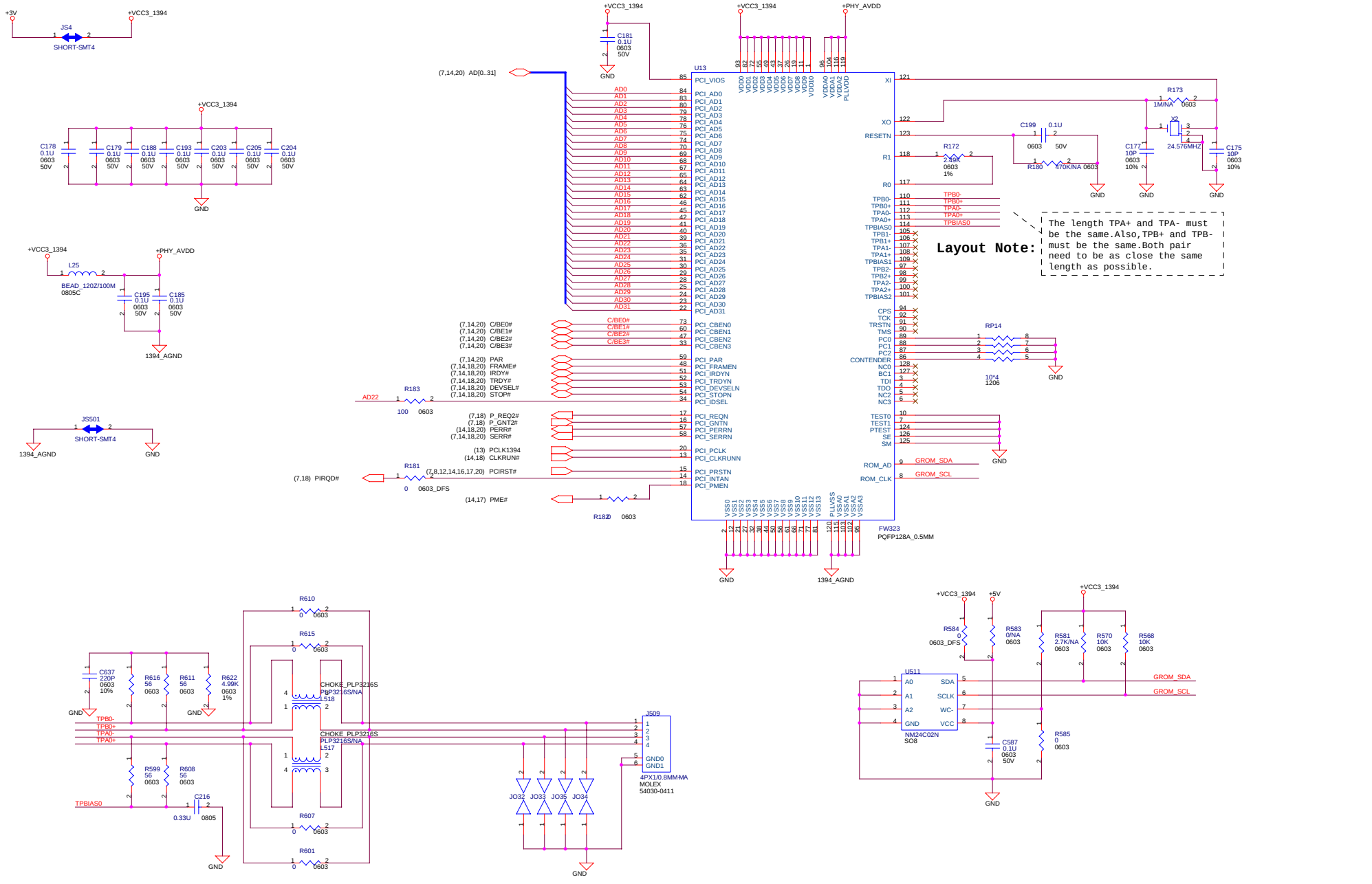
U13
FW323
PQFP128A_0.5MM
Layout Note:
The length TPA+ and TPA- must be the same.Also,TPB+ and TPB- must be the same.Both pair need to be as close the same length as possible.
U511
NM24C02N
SO8
J509
4PX1/0.8MM-MA
MOLEX
54030-0411
JS4
SHORT-SMT4
JS501
SHORT-SMT4
L25
BEAD_120Z/100M
0805C
X2
24.576MHZ
CHOKE_PLP3216S
PLP3216S/NA
L518
L517
MiTAC
Title
1394.SCH
Size C
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Layout Note:

二組各自平行走線等長
二組中間須絕緣,
EX: GND SHIELDING
S/W/W/S=12/6/6/12 mils
as short as possible

Layout Note:
GND Shape must touch CASE well.

MDC+/- LINK TO GOLDEN FINGER

FA SPEED-7426-9751-121
MA SPEED-BO6B-3100-126

MDC

Layout Note:
W/S=6/12 mils

Layout Note:
CLOSE TO MDC

Layout Note:

IDSEL:AD20

Title	LAN & MDC
Size	C
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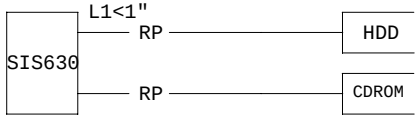
CDROM FFC CONNECTOR

Layout Note:

W/S=16/12/12/16 mils

Layout Note:

All RP on this page must near SIS630ST



CDROM DIAG AND IDE ACTIVE LED

HARD DISK CONNECTOR

Title	HDD & CD_ROM CONNECTOR
Size	C
Document Number	411672000001
Rev	R01
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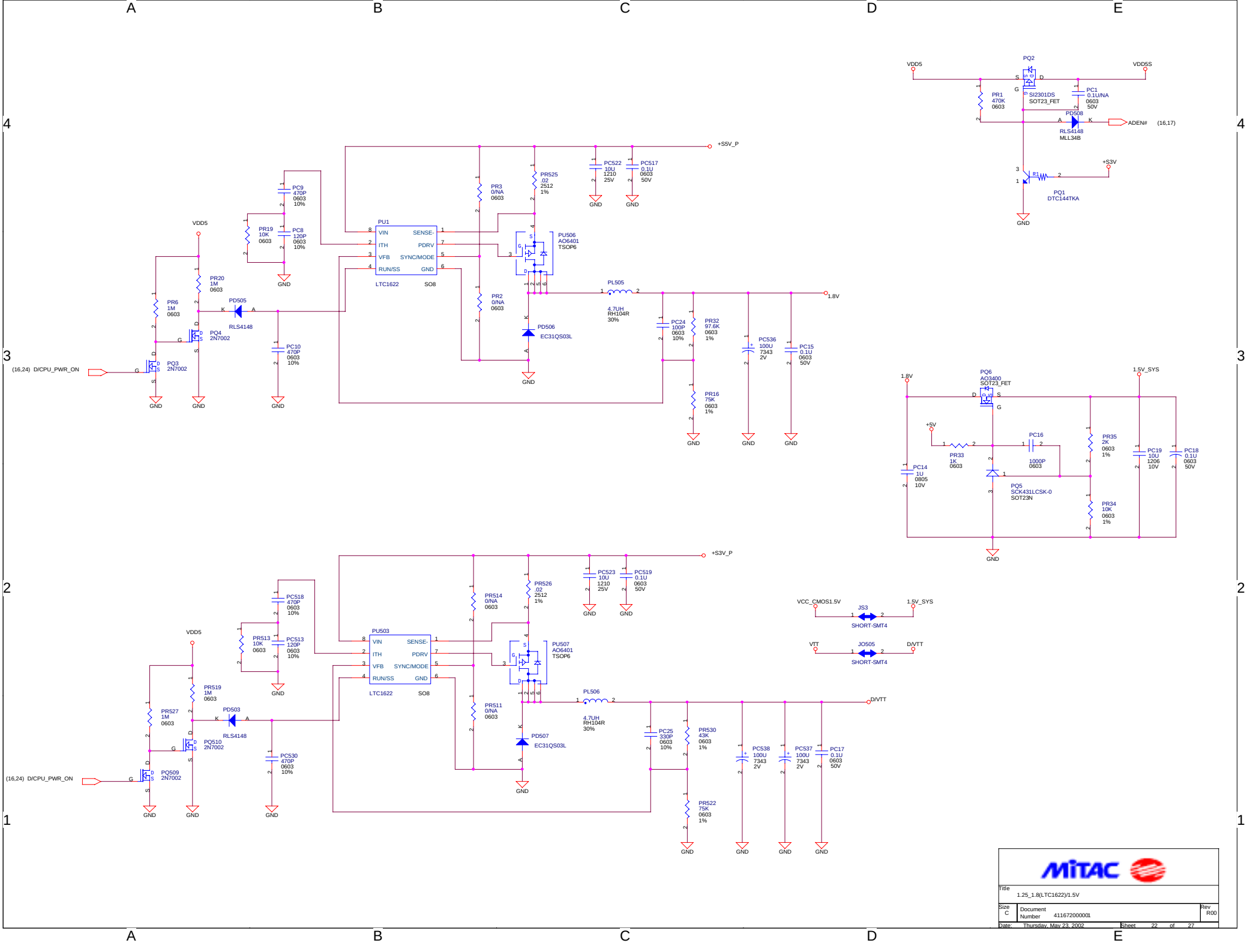
VDD5
PQ2
SI2301DS
SOT23_FET
PC1
0.1U/NA
0603
50V
PR1
470K
0603
PD508
RLS4148
MLL34B
ADEN#
(16,17)
+S3V
R1
PQ1
DTC144TKA
GND
+S5V_P
PU1
LTC1622
SO8
VIN
ITH
VFB
RUN/SS
SENSE-
PDRV
SYNC/MODE
GND
PR525
.02
2512
1%
PC522
10U
1210
25V
PC517
0.1U
0603
50V
PR3
0/NA
0603
PU506
AO6401
TSOP6
PR2
0/NA
0603
PL505
4.7UH
RH104R
30%
1.8V
PD506
EC31QS03L
PC9
470P
0603
10%
PR19
10K
0603
PC8
120P
0603
10%
PR20
1M
0603
PR6
1M
0603
PD505
RLS4148
PQ4
2N7002
PC10
470P
0603
10%
PQ3
2N7002
(16,24) D/CPU_PWR_ON
PC24
100P
0603
10%
PR32
97.6K
0603
1%
PR16
75K
0603
1%
PC536
100U
7343
2V
PC15
0.1U
0603
50V
PQ6
AO3400
SOT23_FET
1.5V_SYS
+5V
PR33
1K
0603
PC16
1000P
0603
PC14
1U
0805
10V
PR35
2K
0603
1%
PC19
10U
1206
10V
PC18
0.1U
0603
50V
PQ5
SCK431LCSK-0
SOT23N
PR34
10K
0603
1%
+S3V_P
PU503
LTC1622
SO8
PR526
.02
2512
1%
PC523
10U
1210
25V
PC519
0.1U
0603
50V
PR514
0/NA
0603
PU507
AO6401
TSOP6
PR511
0/NA
0603
PL506
4.7UH
RH104R
30%
D/VTT
PD507
EC31QS03L
VCC_CMOS1.5V
JS3
SHORT-SMT4
VTT
JO505
SHORT-SMT4
PC518
470P
0603
10%
PR513
10K
0603
PC513
120P
0603
10%
PR519
1M
0603
PR527
1M
0603
PD503
RLS4148
PQ510
2N7002
PC530
470P
0603
10%
PQ509
2N7002
(16,24) D/CPU_PWR_ON
PC25
330P
0603
10%
PR530
43K
0603
1%
PC538
100U
7343
2V
PC537
100U
7343
2V
PC17
0.1U
0603
50V
PR522
75K
0603
1%
MiTAC
Title
1.25_1.8(LTC1622)/1.5V
Size
C
Document
Number
411672000001
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R00
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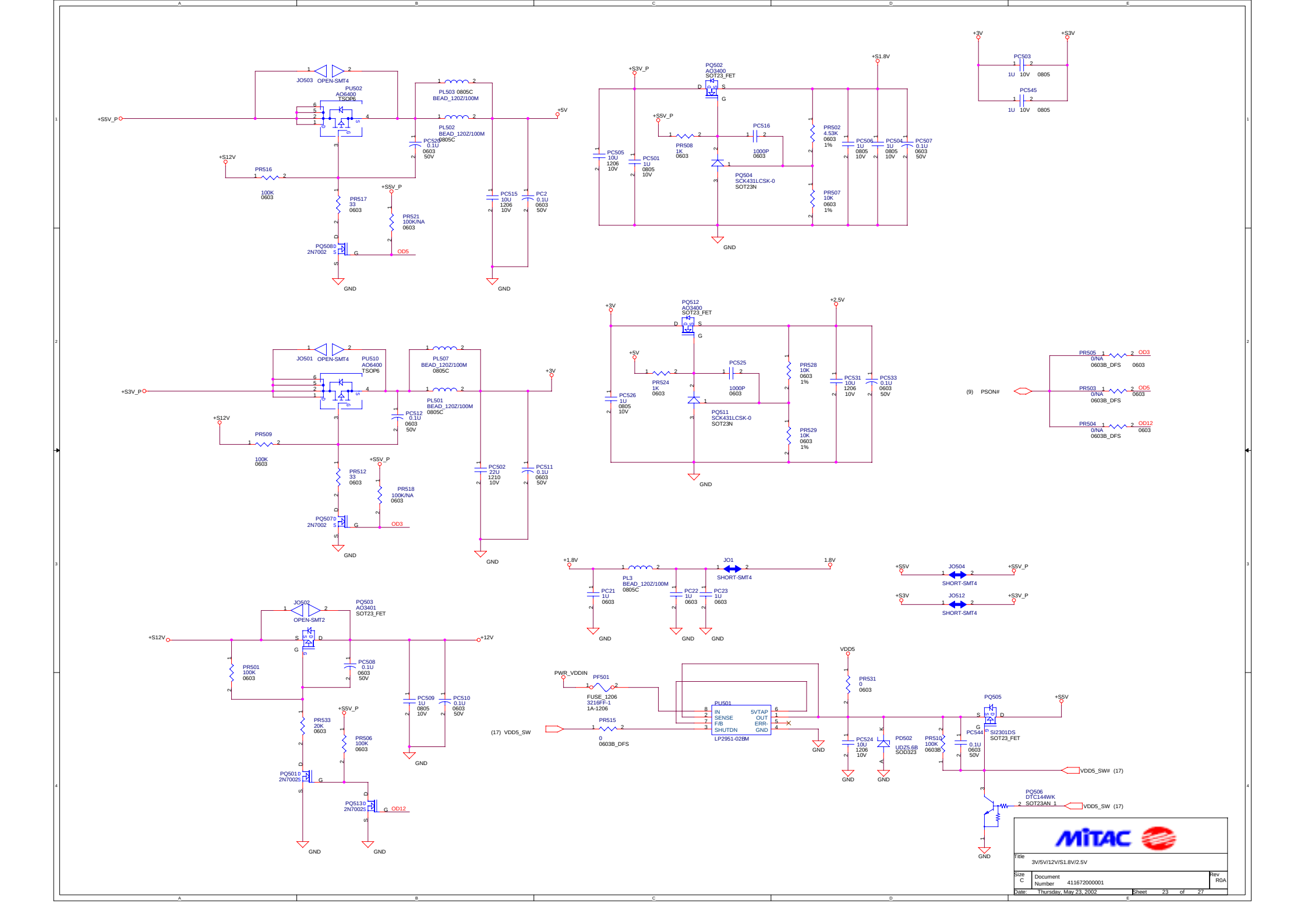
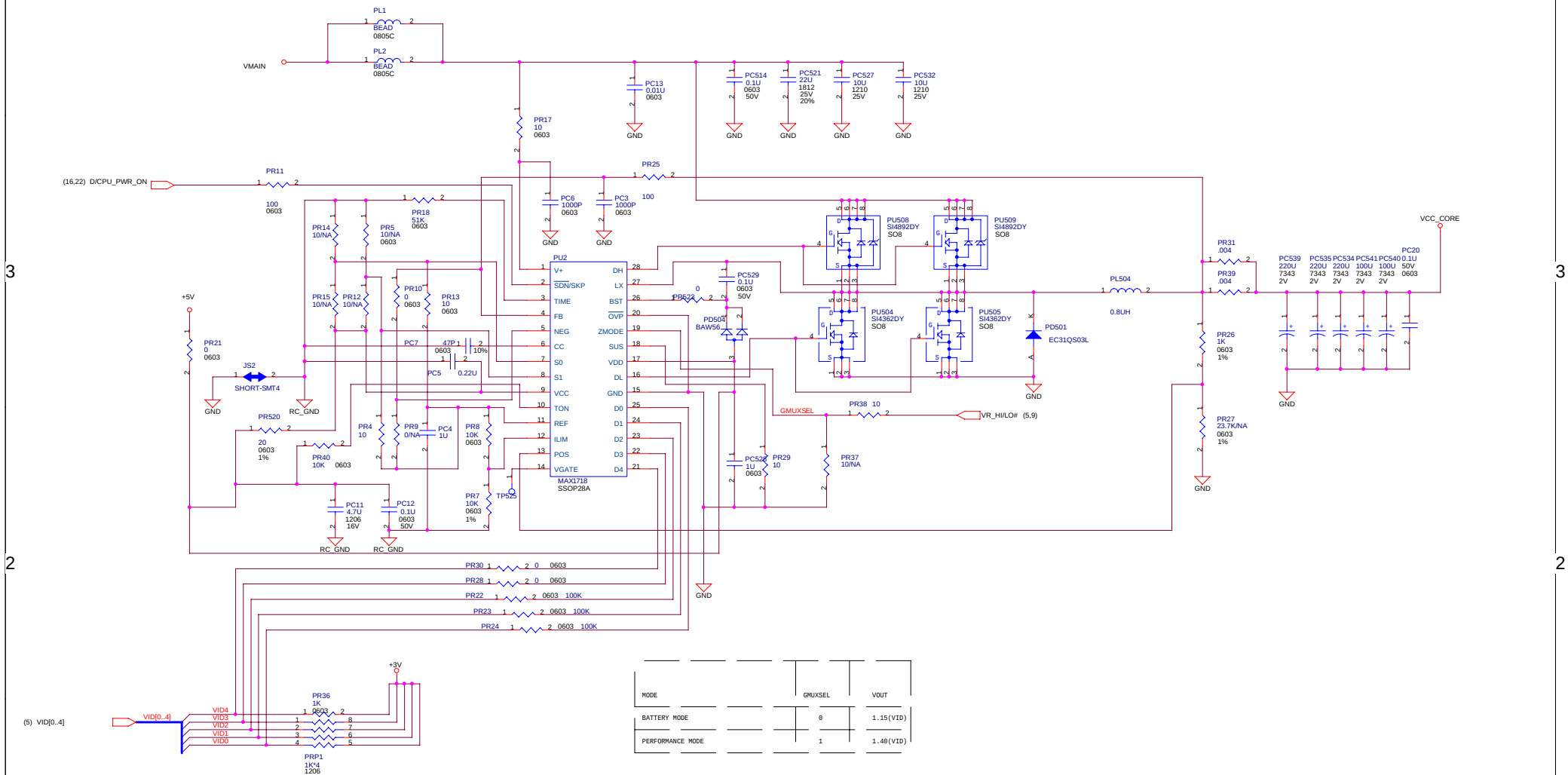
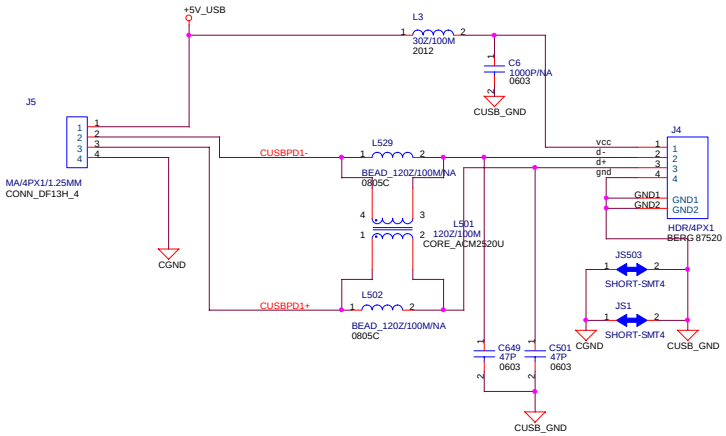

JO503 OPEN-SMT4
PU502 AO6400 TSOP6
PL503 0805C BEAD_120Z/100M
PL502 BEAD_120Z/100M 0805C
+S5V_P
+5V
+S12V
PR516 100K 0603
PR517 33 0603
PR521 100K/NA 0603
PC520 0.1U 0603 50V
PC515 10U 1206 10V
PC2 0.1U 0603 50V
PQ508 2N7002
OD5
GND
+S3V_P
PQ502 AO3400 SOT23_FET
+S1.8V
PR508 1K 0603
PC516 1000P 0603
PR502 4.53K 0603 1%
PR507 10K 0603 1%
PC505 10U 1206 10V
PC501 1U 0805 10V
PC506 1U 0805 10V
PC504 1U 0805 10V
PC507 0.1U 0603 50V
PQ504 SCK431LCSK-0 SOT23N
+3V
+S3V
PC503 1U 10V 0805
PC545 1U 10V 0805
JO501 OPEN-SMT4
PU510 AO6400 TSOP6
PL507 BEAD_120Z/100M 0805C
PL501 BEAD_120Z/100M 0805C
PR509 100K 0603
PR512 33 0603
PR518 100K/NA 0603
PC512 0.1U 0603 50V
PC502 22U 1210 10V
PC511 0.1U 0603 50V
PQ507 2N7002
OD3
PQ512 AO3400 SOT23_FET
+2.5V
PR524 1K 0603
PC525 1000P 0603
PR528 10K 0603 1%
PR529 10K 0603 1%
PC526 1U 0805 10V
PC531 10U 1206 10V
PC533 0.1U 0603 50V
PQ511 SCK431LCSK-0 SOT23N
(9) PSON#
PR505 0/NA 0603B_DFS
PR503 0/NA 0603B_DFS
PR504 0/NA 0603B_DFS
OD3
OD5
OD12
JO502 OPEN-SMT2
PQ503 AO3401 SOT23_FET
+S12V
+12V
PR501 100K 0603
PR533 20K 0603
PR506 100K 0603
PC508 0.1U 0603 50V
PC509 1U 0805 10V
PC510 0.1U 0603 50V
PQ501 2N7002
PQ513 2N7002
OD12
+1.8V
1.8V
JO1 SHORT-SMT4
PL3 BEAD_120Z/100M 0805C
PC21 1U 0603
PC22 1U 0603
PC23 1U 0603
JO504 SHORT-SMT4
JO512 SHORT-SMT4
+S5V
+S3V
PWR_VDDIN
PF501 FUSE_1206 3216FF-1 1A-1206
PR515 0 0603B_DFS
(17) VDD5_SW
PU501 LP2951-02BM
IN
SENSE
F/B
SHUTDN
5VTAP
OUT
ERR-
VDD5
PR531 0 0603
PC524 10U 1206 10V
PD502 UDZ5.6B SOD323
PR510 100K 0603B
PC544 0.1U 0603 50V
PQ505 SI2301DS SOT23_FET
VDD5_SW# (17)
PQ506 DTC144WK SOT23AN
VDD5_SW (17)
MiTAC
Title
3V/5V/12V/S1.8V/2.5V
Size C
Document Number 411672000001
Rev R0A
Date: Thursday, May 23, 2002
Sheet 23 of 27

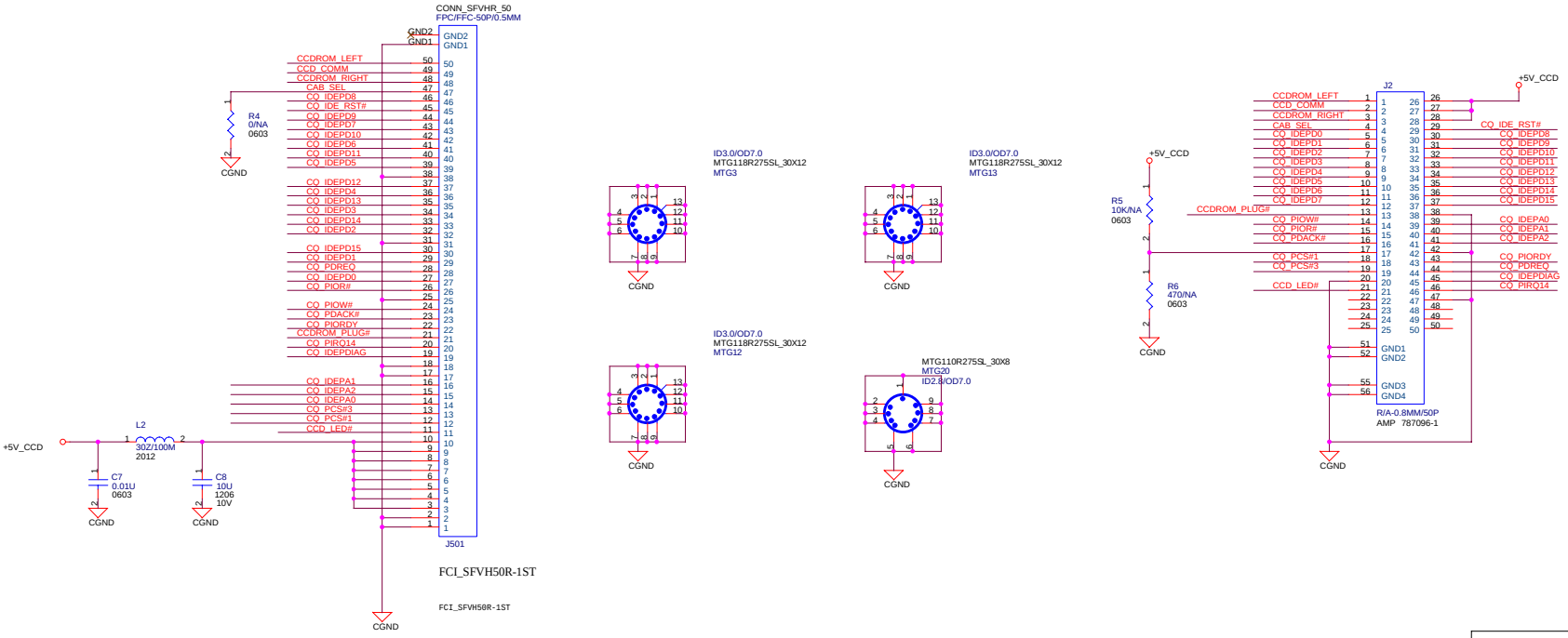


Title	CPU_CORE(MAX1718)	
Size C	Document Number 411672000001	Rev R0A
Date: Thursday, May 23, 2002	Sheet 24 of 27	

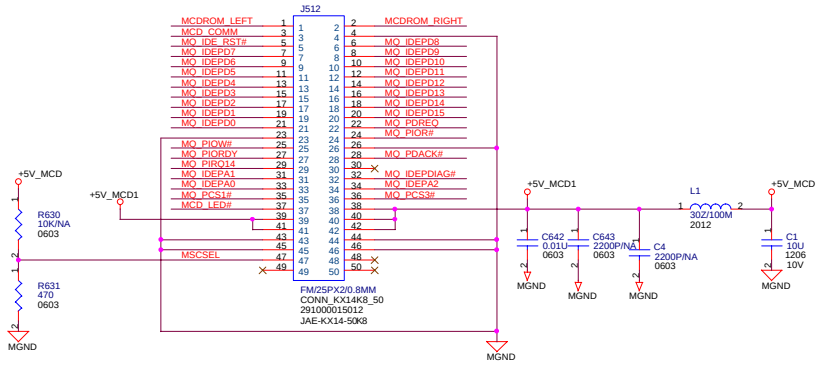
USB

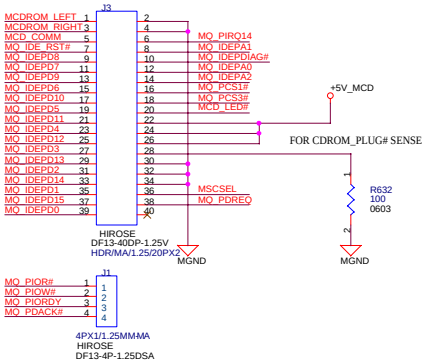


CDROM FFC CONNECTOR



Title	CD/USB_TRANS_BD		
Size C	Document Number 411672000005		Rev R0A
Date: Thursday, May 23, 2002	Sheet 25 of 27		





MiTAC			
Title	CDROM_MODULE		
Size C	Document Number 411672000006		Rev R0A
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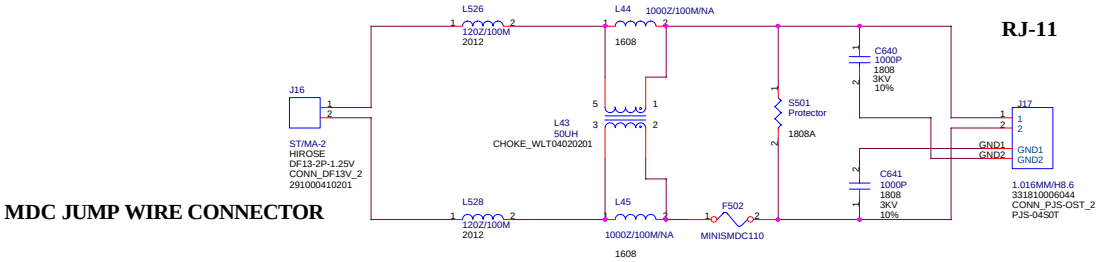
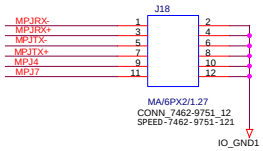
M762 MDC/ LAN TRANSFER BD



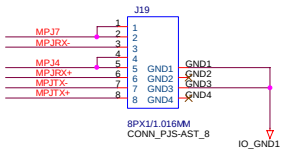
RJ-11

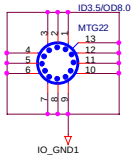
MDC JUMP WIRE CONNECTOR

MDC/ LAN TRANS BD



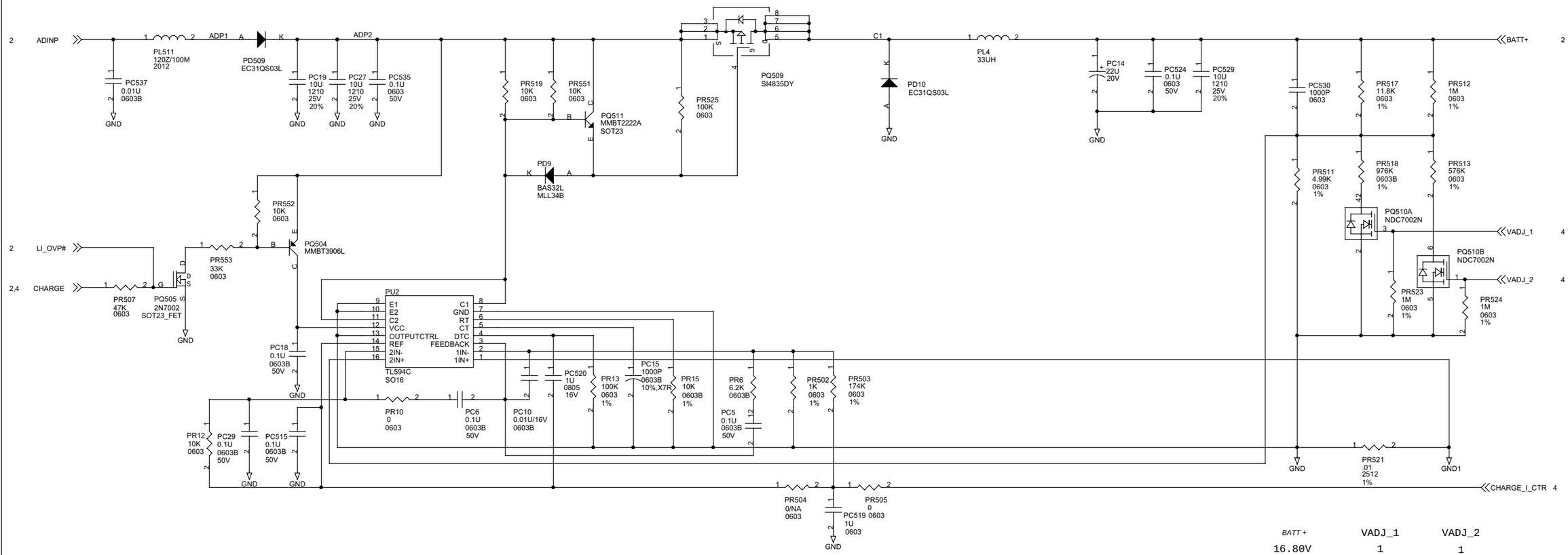
RJ-45





Title	MDC/LAN TRANSFER BD	
Size C	Document Number 411672000004	Rev R01
Date: Thursday, May 23, 2002	Sheet 27 of 27	

M722 D/D BOARD



BATT+	VADJ_1	VADJ_2
16.80V	1	1

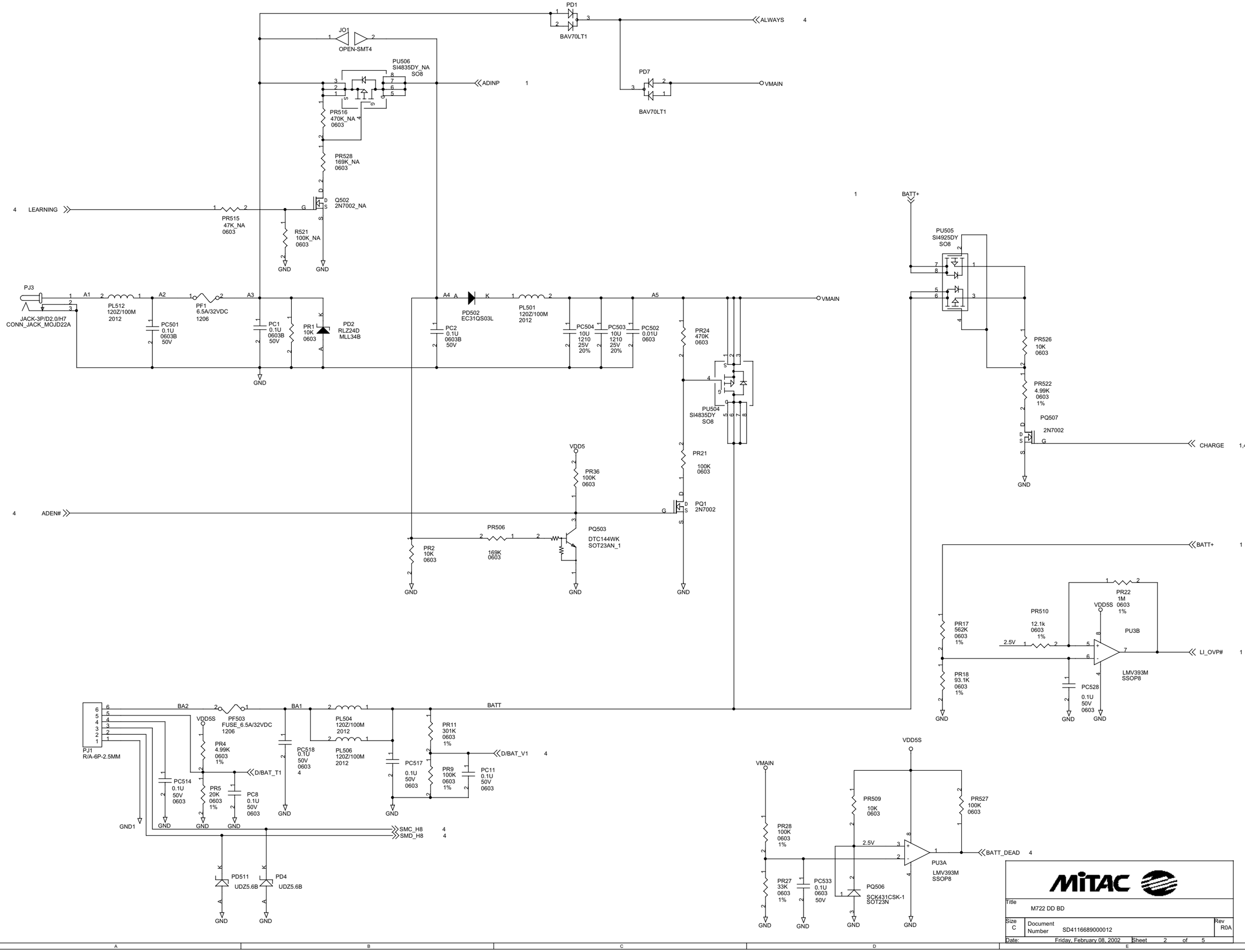
DRAWN	DESIGN	CHECK	ISSUES

MITAC INTERNATIONAL CORP.

Title: M722 DD BD

Size	Document Number	Rev
C	SD411668900012	R0A

Date: Friday, February 08, 2002 Sheet 1 of 5


PD1
BAV70LT1
ALWAYS
JO1
OPEN-SMT4
PU506
SI4835DY_NA
SO8
ADINP
PD7
BAV70LT1
VMAIN
PR516
470K_NA
0603
PR528
169K_NA
0603
LEARNING
PR515
47K_NA
0603
Q502
2N7002_NA
R521
100K_NA
0603
GND
PJ3
JACK-3P/D2.0/H7
CONN_JACK_MOJD22A
PL512
120Z/100M
2012
PF1
6.5A/32VDC
1206
PC501
0.1U
0603B
50V
PC1
0.1U
0603B
50V
PR1
10K
0603
PD2
RLZ24D
MLL34B
PD502
EC31QS03L
PL501
120Z/100M
2012
PC2
0.1U
0603B
50V
PC504
10U
1210
25V
20%
PC503
10U
1210
25V
20%
PC502
0.01U
0603
PR24
470K
0603
PU504
SI4835DY
SO8
VDD5
PR36
100K
0603
PR21
100K
0603
PQ1
2N7002
ADEN#
PR506
PQ503
DTC144WK
SOT23AN_1
PR2
10K
0603
169K
0603
BATT+
PU505
SI4925DY
SO8
PR526
10K
0603
PR522
4.99K
0603
1%
PQ507
2N7002
CHARGE
BATT+
PR22
1M
0603
1%
VDD5S
PR510
12.1k
0603
1%
PR17
562K
0603
1%
PU3B
2.5V
LI_OVP#
LMV393M
SSOP8
PR18
93.1K
0603
1%
PC528
0.1U
50V
0603
PJ1
R/A-6P-2.5MM
BA2
BA1
BATT
VDD5S
PF503
FUSE_6.5A/32VDC
1206
PL504
120Z/100M
2012
PL506
120Z/100M
2012
PR4
4.99K
0603
1%
PC518
0.1U
50V
0603
PR11
301K
0603
1%
D/BAT_V1
PC517
0.1U
50V
0603
PR9
100K
0603
1%
PC11
0.1U
50V
0603
D/BAT_T1
PC514
0.1U
50V
0603
PR5
20K
0603
1%
PC8
0.1U
50V
0603
GND1
SMC_H8
SMD_H8
PD511
UDZ5.6B
PD4
UDZ5.6B
VDD5S
VMAIN
PR509
10K
0603
PR527
100K
0603
PR28
100K
0603
1%
2.5V
PU3A
LMV393M
SSOP8
BATT_DEAD
PR27
33K
0603
1%
PC533
0.1U
0603
50V
PQ506
SCK431CSK-1
SOT23N
MiTAC
Title
M722 DD BD
Size
C
Document
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R0A
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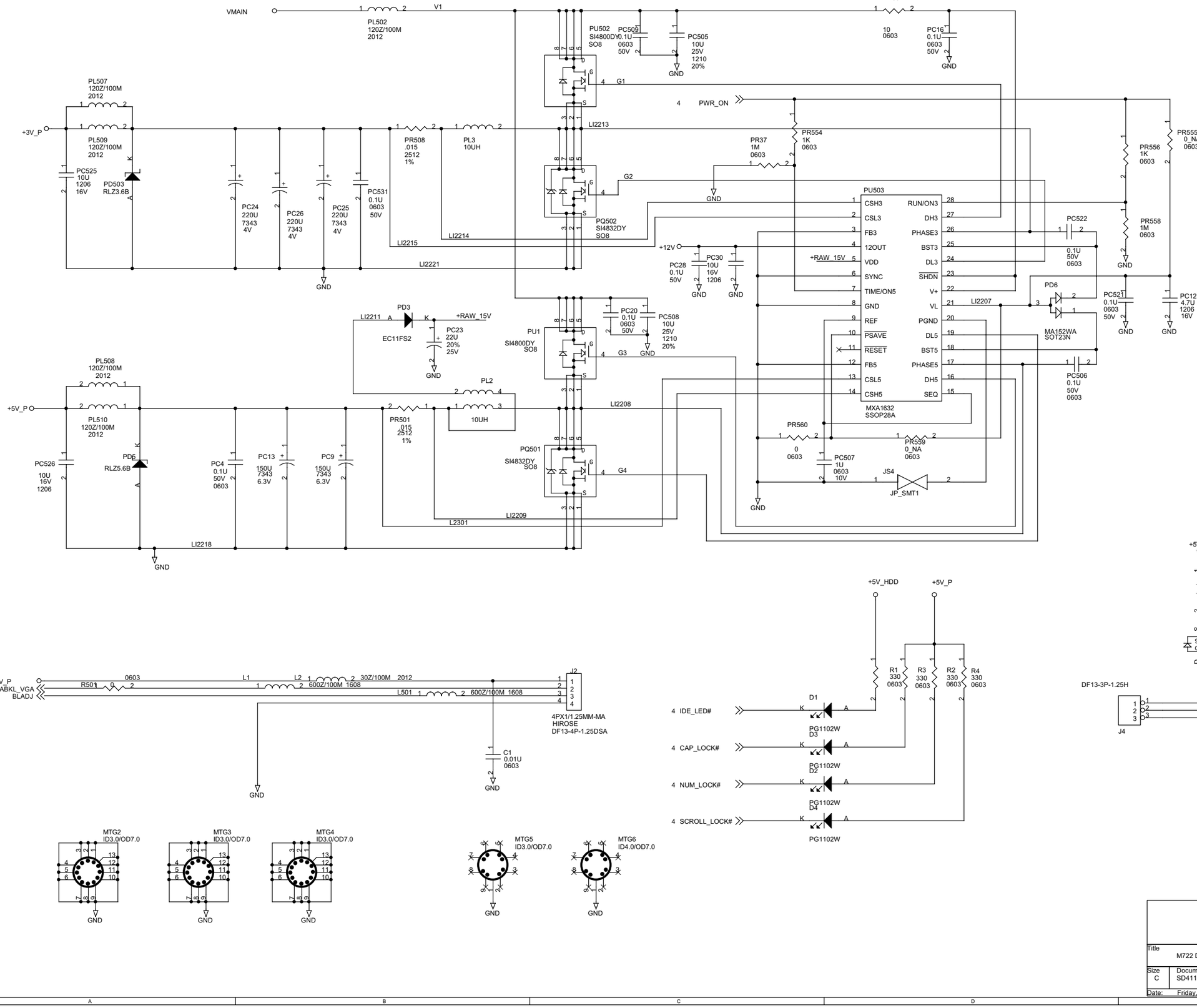
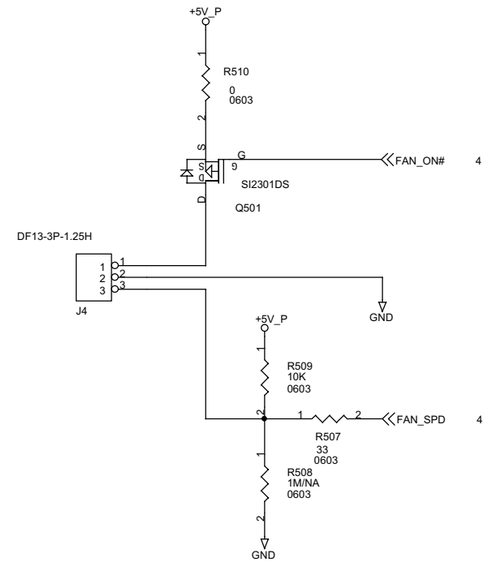
5





MiTAC

Title: M722 DD BD		
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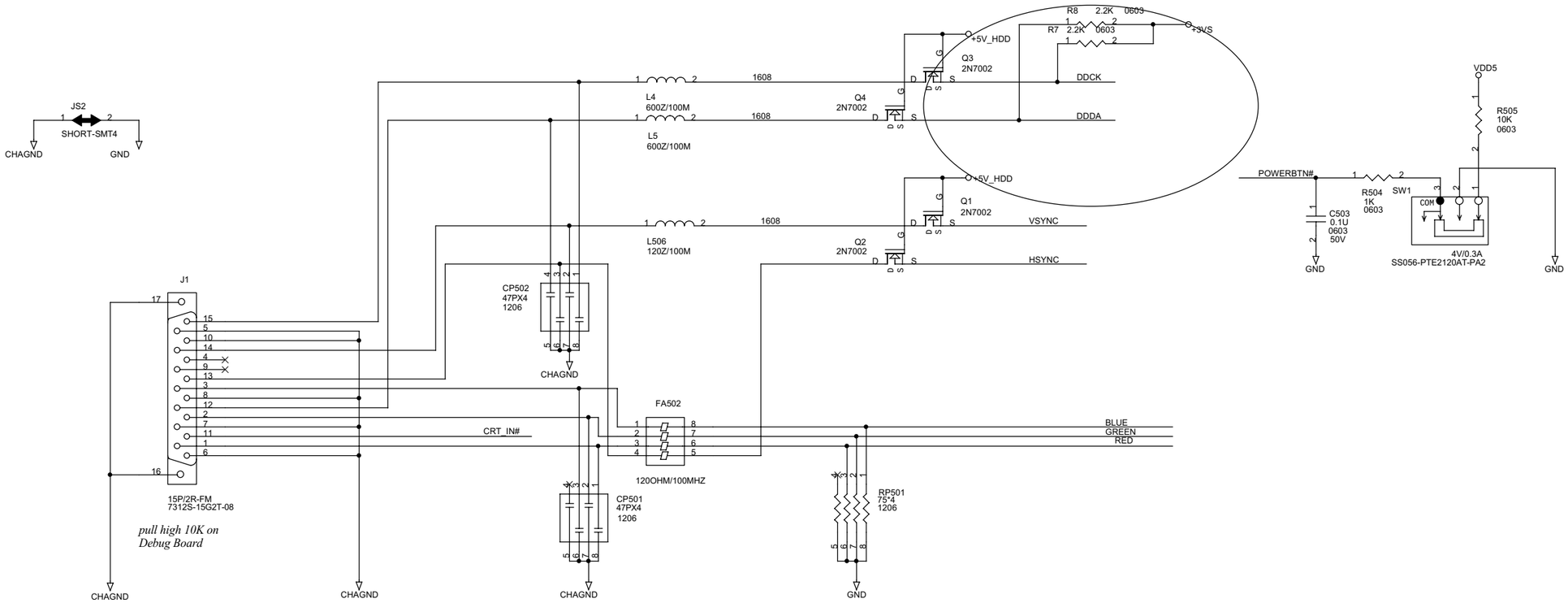

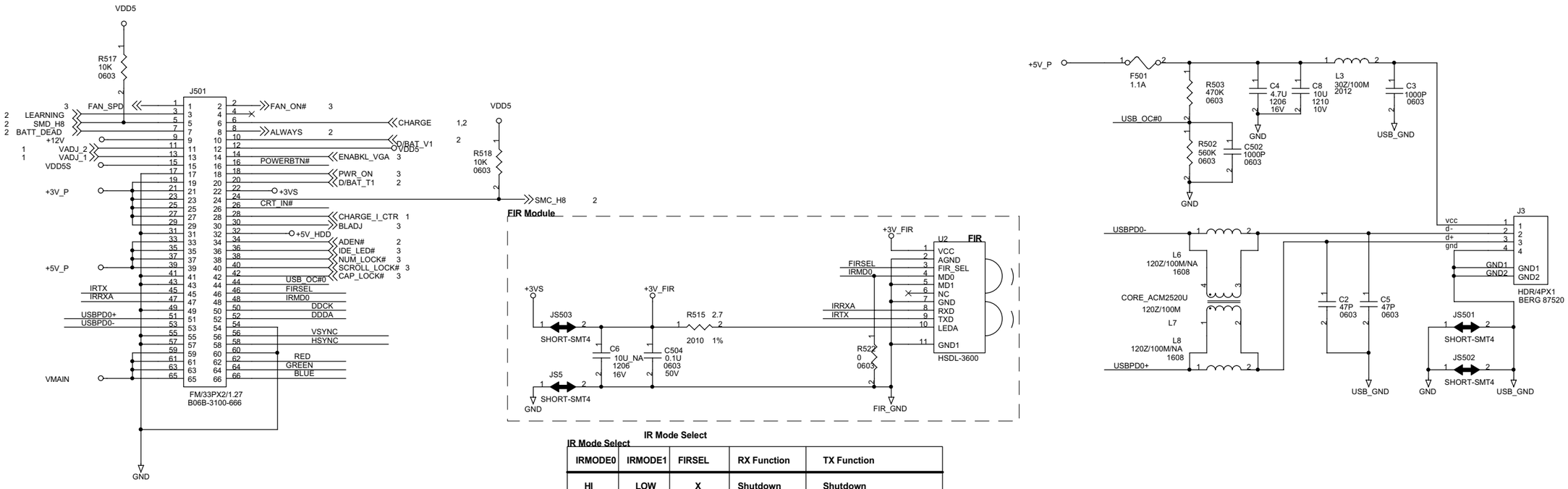

IR Mode Select

IRMODE0	IRMODE1	FIRSEL	RX Function	TX Function
HI	LOW	X	Shutdown	Shutdown
LOW	LOW	LOW		Full Distance Power
LOW	HI	LOW	SIR	2/3 Distance Power
HI	HI	LOW	SIR	1/3 Distance Power
LOW	LOW	HI	MIR/FIR	Full Distance Power
LOW	HI	HI	MIR/FIR	2/3 Distance Power
HI	HI	HI	MIR/FIR	1/3 Distance Power

Title	M722 DD BD
Size: C	Document Number: SD411668900012
Rev: R0A	
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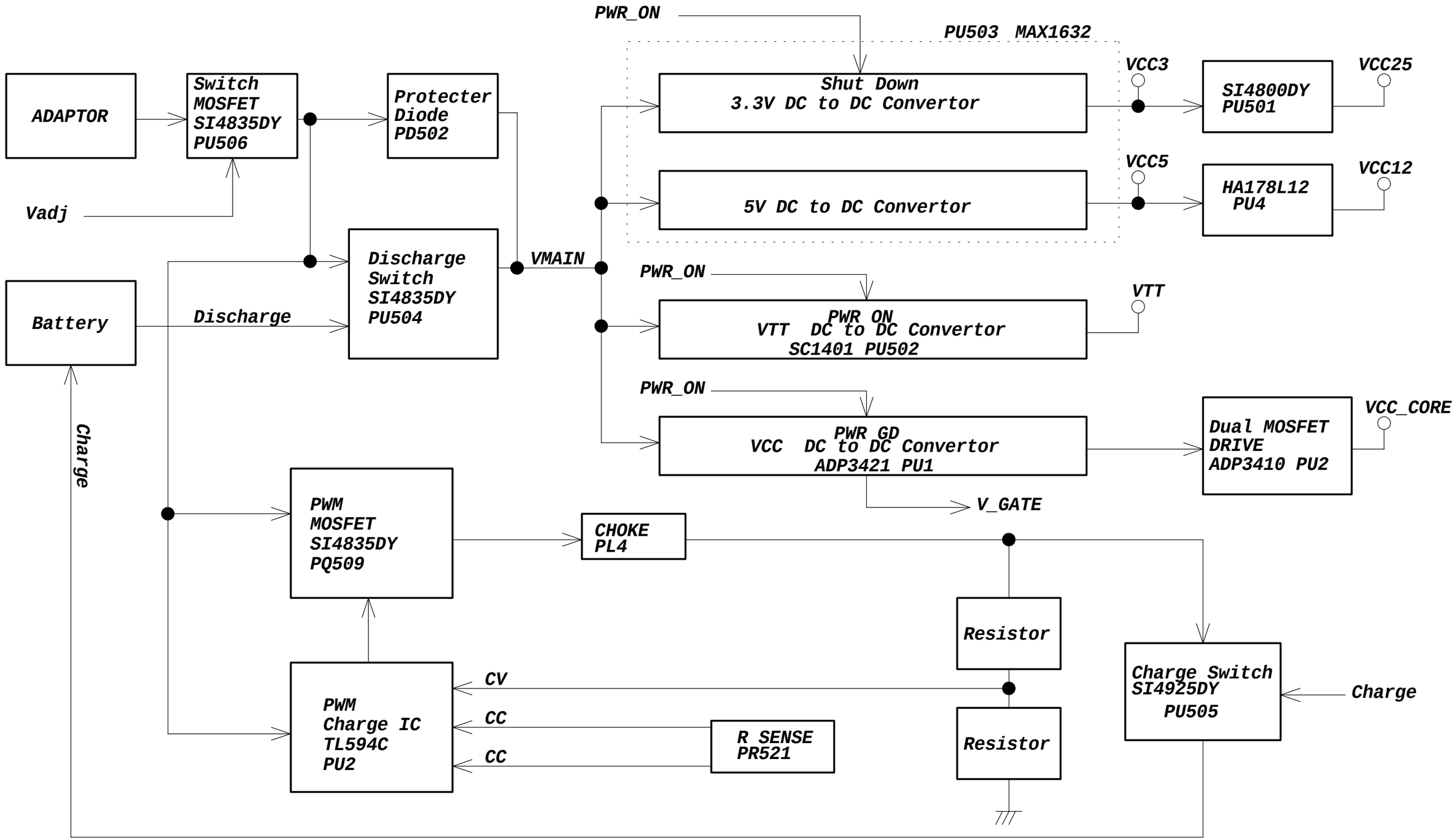
POWER DIAGRAM OF THE M722



MiTAC		
Title	Power Diagram	
Size	Document Number 411668900012	Rev R0A
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Reference Material

❖ Intel Mobile Pentium III-M uFC-PGA478 Processor	Intel, INC
❖ SiS630ST Slot1/Socket370 2D/3D Ultra AGP™ Single Chipset	SiS, INC
❖ PCI1410 PCMCIA Controller	TI, INC
❖ FW323 IEEE1394 Controller	NEC, INC
❖ M762 Hardware Engineering Specification	*Technology Corp.*/MiTAC

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