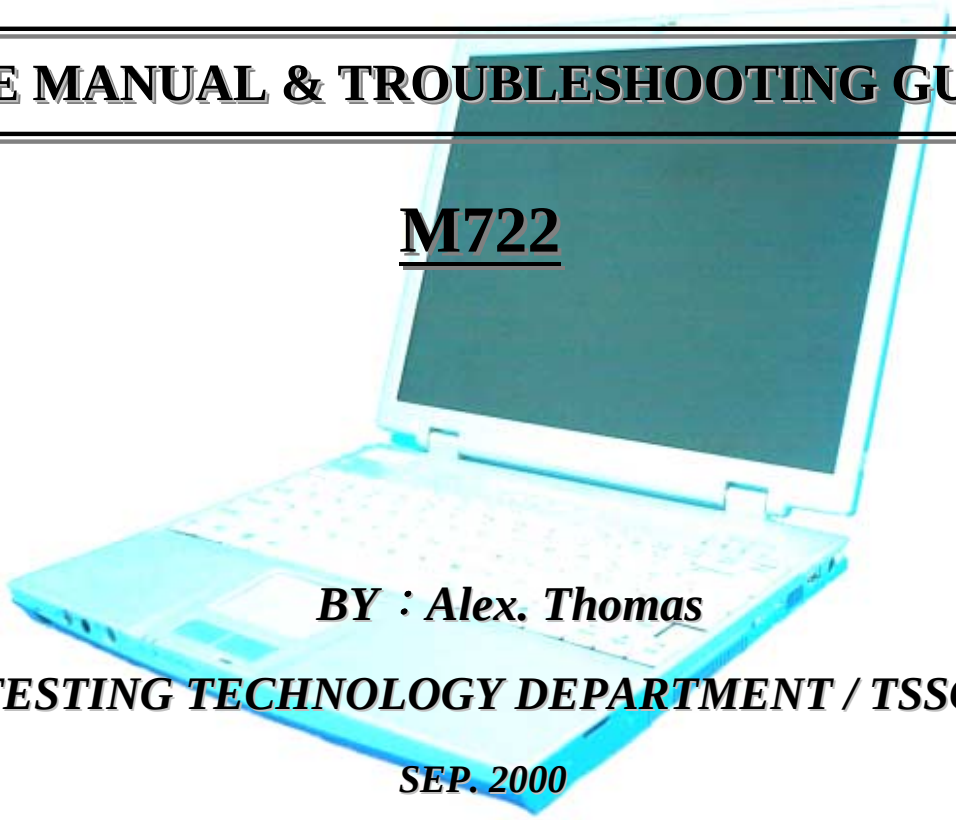
SERVICE MANUAL & TROUBLESHOOTING GUIDE FOR

M722



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SEP. 2000

MiTAC

M722 N/B MAINTENANCE

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0. HARDWARE ENGINEERING SPECIFICATION

M 722 Hardware Engineering Specification

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0.1. INTRODUCTION

The M722 model motherboard would support the Mobile Pentium III processor at 500/600*/650* /700*/750*/800*MHz uPGA2 package on board and Celeron 450/500/550/600/650/700MHz uPGA2 package .(*Enabled with IST,Intel Speedstep technology)

This system is based on PCI architecture and is fully compatible with IBM PC/AT specification, which have standard hardware peripheral interface and support Intel Mobile Pentium III/Celeron (uPGA2) family. The power management complies with Advanced Configuration and Power Interface (ACPI) 1.0. It also provides easy configuration through CMOS setup, which is built in system BIOS software and can be pop-up by pressing F2 at system start up or warm reset. System also provides icon LEDs to display system status, such as Power indicator, LAN, HDD/CDROM, NUM LOCK, CAP LOCK, SCROLL LOCK, SUSPEND MODE and Battery charging status. It also equipped with Zoom Video capture port, FIR, 4 USB ports, and 3D stereo audio functions.

The memory subsystem supports 64MB SDRAM on board and one 144pin DIMM socket for upgrading up to 192MB or 256 MB of DRAM using PC-100 SDRAM DIMM module.

The 82440MX Chipset integrated the North Bridge chipset (without AGP) and the South Bridge chipset while adding a two channel, digital AC'97.2 links feature. 82440MX Chipset brings second important firsts to the mobile PC environment: (1) Concurrent PCI (PCI 2.1) reduces CPU latencies for smoother video and more realistic audio; (2) Universal Serial Bus (USB) technology makes Plug and Play peripheral connections a reality. The Intel 82440MX Chipset also contains an integrated PCI Bus Mastering IDE controller with one high performance IDE interfaces and supports "Ultra 33" synchronous DMA mode which transfers up to 33 Mbytes per second. In addition, the 440MX Chipset supports Intel's new Dynamic Power Management Architecture (DPMA) for consuming less power consumption than earlier PCIset designs and supports Advanced Configuration and Power Interface (ACPI) 1.0 for longer battery life in mobile systems.

The ATI 3D RAGE Mobility-M VGA controller integrated with 4Mbyte SDRAM provides LCD, and CRT simultaneously and supports 2D and 3D acceleration, ZV port, DVD, ACPI power management, integrated LVDS…etc. The TI 1410 CARDBUS controller supports PCMCIA and CARDBUS. The National Semiconductor PC97338 Super I/O controller integrates an IrDA 1.1, 1.0 and sharp ASK compatible infrared interface To provide for the increasing number of multimedia applications, the AC97 CODEC CS4299 is integrated onto the motherboard which contain 3D digital audio output.

A full set of software drivers and utilities are available to allow advanced operating systems such as Windows 98 to take full advantage of the hardware capabilities such as bus mastering IDE, Windows 95-ready Plug & Play, Advanced Power Management (APM) and Advance configuration and power interface (ACPI).

Following chapters will have more detail description for each individual sub-systems and functions.

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0.2. SYSTEM HARDWARE PARTS

Central Processing Unit: Intel Mobile Pentium III microprocessor (uPGA2) operating at 500/600/650/700/750/800MHz and Celeron microprocessor (uPGA2) operating at 450/500/600/650/700MH
Synthesizer and SDRAM buffer: ICS9248-101
CPU/PCI bridge with memory controller and PCI/ISA bridge with IDE/USB/PMU controller: Intel82440MX-100 -BANISTER
PCI Video Controller: ATI 3D RAGE Mobility-M
Super I/O Controller: NS PC97338VJG
Cardbus Controller: TI 1410
Keyboard System: Hitachi H8 (3434) universal keyboard controller
AC97 CODEC: Crystal CS4299
FIR port: VISHAY TFDU6101E FIR module
FAX/MODEM: ASKEY 56Kbps MDC Software Modem
LAN100M/10Mbits: RTL8139CL
IEEE1394 :NEC UPD72870A

0.2.1 CPU – INTEL MOBILE Celeron/Pentium III PROCESSOR IN uPGA2 PACKAGE

Exceptional value and improved performance over existing mobile processors
- Supports the Intel Architecture with Dynamic Execution
- Supports the Intel Architecture MMX technology
- Support for Streaming SIMD Extensions for enhanced video,sound and 3D performance
- Support Intel Speedstep Technology
- Integrated Intel Floating-Point Unit compatible with the IEEE Std 754

Integrated on die primary (L1) instruction and data caches
- 4-way set associative, 32-byte line size, 1 line per sector
- 16-Kbyte instruction cache and 16-Kbyte writeback data cache
- Cacheable range programmable by processor programmable registers

Integrated second level (L2) cache
- 4-way set associative, 32-byte line size,1 line per sector
- Operates at full core speed
- 128-Kbyte for Celeron
- 256-Kbyte for Pentium III, ECC protected cache data array
- 4 G Bytes cacheable range

Low Power GTL+ system bus interface
- 64-bit data bus, 100-MHz operation
- Uniprocessor, two loads only (processor and I/O bridge/memory controller)
- Integrated termination

Voltage reduction technology
Advanced Pentium III processor clock control
- Quick Start for low power, low exit latency clock “throttling”
- Deep Sleep mode for extremely low power dissipation

Thermal diode for measuring processor temperature

0.2.2 Intel 82440MX-100 Chipset Host Bridge

64-bit GTL+ based Host Bus Interface
32-bit Host address Support
64-bit Main Memory Interface with optimized support for SDRAM at 100 MHz
32-bit Primary PCI Bus Interface (PCI) with integrated PCI arbiter
Extensive Data Buffering between all interfaces for high throughput and concurrent operations.
Mobile and *“Deep Green”* Desktop power management support.
Host bridge for translation from CPU bus cycle to PCI bus cycle
Integrated IDE controller with Ultra DMA/33 support.
Processor/Host bus support
- Optimized for mobile Celeron processors or Pentium III processors at 100MHz host bus frequency
- Supports 32-bit mobile Celeron processor / Pentium III processor bus addressing.
- 4 or 1 deep in-order queue; 4 or 1 deep request queue
- Supports uni-processor systems only
- In-order transaction and dynamic deferred transaction support
- GTL+ bus driver technology (gated GTL+ receivers for reduced power)

Integrated DRAM controller
- 8 to 512 Mbytes .
- Supports up to 2 double-sided SO-DIMMs (4-row memory).
- 64-bit data interface without ECC support.
- Unbuffered SDRAM Support (x-1-1-1 access @ 100 MHz).
- Support only 3.3v DIMM DRAM configuration.
- Enhanced SDRAM Open Page Architecture Support for 16- and 64-Mbit DRAM devices with 2k, 4k and 8k page sizes
- Max address decode A0..A11, BA0, BA1

PCI bus interface
- PCI Rev. 2.2, 3.3V, 33MHz interface compliant.
- 4 PCI bus masters support for combination of Graphic, LAN, Card Bus, and IEEE1394
- PCI Parity Generation Support.
- Data streaming support from PCI to DRAM.
- Delayed Transaction supports for PCI-DRAM Reads.
- Supports concurrent CPU, and PCI transactions to main memory.

Power Management Functions

- Stop Clock Grant and Halt special cycle translation (host to PCI Bus).
- Mobile and “deep Green” Desktop support for system suspend/resume (i.e., DRAM and power-on suspend).
- Dynamic power down idle DRAM rows.
- SDRAM self-refresh power down support in suspend mode.
- Independent, internal dynamic clock gating reduces average power dissipation.
- Static STOP CLOCK support.
- Power-on Suspend mode.
- Suspend to DRAM.
- ACPI compliant power management.

AC’97. 2 link controller (2 channels)
- Interface to AC’97x AUDIO CODEC
- Interface to MDC modem

GPIO pins (31)

Supporting I/O Bridge.
- System Management Bus (SMB) with support for DIMM Serial Presence Detect (SPD).
- Power Management Support.
- 3.3V core and mixed 5V, 3.3V I/O and interface to the 2.5V CPU

PCI-to-ISA/EIO bridge (south bridge) for passing the cycles accessing ISA (w/EIO)

Multifunction PCI to ISA Bridge
- Supports PCI at 30 MHz and 33 MHz
- Supports PCI Rev 2.2 Specification
- Supports Full ISA or Extended I/O (EIO) Bus
- Supports Full Positive Decode or Subtractive Decode of PCI
- Supports ISA and EIO at 1/4 of PCI Frequency

Supports both Mobile and Desktop Deep Green Environments
- 3.3V Operation with 5V Tolerant Buffers
- Ultra-low Power for Mobile Environments Support
- Power-On Suspend, Suspend to RAM, Suspend to Disk, and Soft-OFF System States
- All Registers Readable and Restorable for Proper Resume from 0.V Suspend

Power Management Logic
- Global and Local Device Management
- Suspend and Resume Logic
- Supports Thermal Alarm
- Support for External Micro controller
- Full Support for Advanced Configuration and Power Interface (ACPI) Revision 1.0 Specification and OS Directed Power Management

1 channel bus master IDE support ultra DMA33

Enhanced DMA Controller
- Two 82C37 DMA Controllers
- Supports PCI DMA with 1 PC/PCI Channels and Distributed DMA Protocols (Simultaneously)

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Interrupt Controller Based on Two 82C59
- 15 Interrupt Support
- Independently Programmable for Edge/Level Sensitivity
- Supports Optional I/O APIC
- Serial Interrupt Input

Timers Based on 82C54
- System Timer, Refresh Request, Speaker Tone Output

USB
- Two USB 1.1 Ports for Serial Transfers at 12 Mbor 1.5 MB/sec
- Supports Legacy Keyboard and Mouse Software with USB-based Keyboard and Mouse.
- Supports UHCI Design Guide

SMBus
- Host Interface Allows CPU to Communicate Via SMBus
- Slave Interface Allows External SMBus Master to Control Resume Events

Real-Time Clock
- 256-byte Battery-Back CMOS SRAM
- Includes Date Alarm
- Two 8-byte Lockout Ranges

Packaging/Voltage
- 492 Pin BGA

3.3V core and mixed 3.3V and GTL I/O.

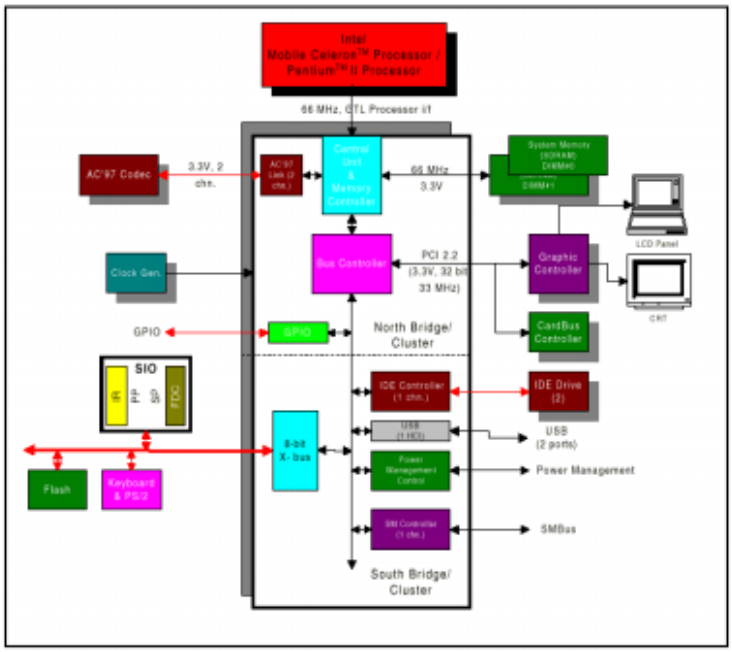

Figure 1: Intel 82440MX Simplified Block Diagram.

0.2.3 System frequency synthesizer and SDRAM buffer : ICS9148-101

Maximized EMI suppression using ICS spread spectrum technology.
Two copies of CPU output, output to output skew between them within 175ps and six copies of PCI output, output to output skew within 500ps.
One 48MHz output for USB and selectable 24/48MHz output (pin 27).
Two buffer copies of 14.318MHz input reference signal.
Supports 100MHz or 66MHz CPU operation.

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Power management control pins.
Spread spectrum function can be disabled.
Low voltage, 8 skew controlled CMOS output clock buffers (SDRAM 0:7)
Supports two SDRAM DIMMS.
Ideal for high performance systems designed around Intel's latest mobile chip set.
I2C serial configuration interface.
Skew between any two SDRAM output is less than 250ps
1 to 5ns propagation delay.
Dc to 133mhz operation.
Singles 3.3V supply voltage.
Low power CMOS design packaged in a 48-pin, SSOP(Shrink small package).

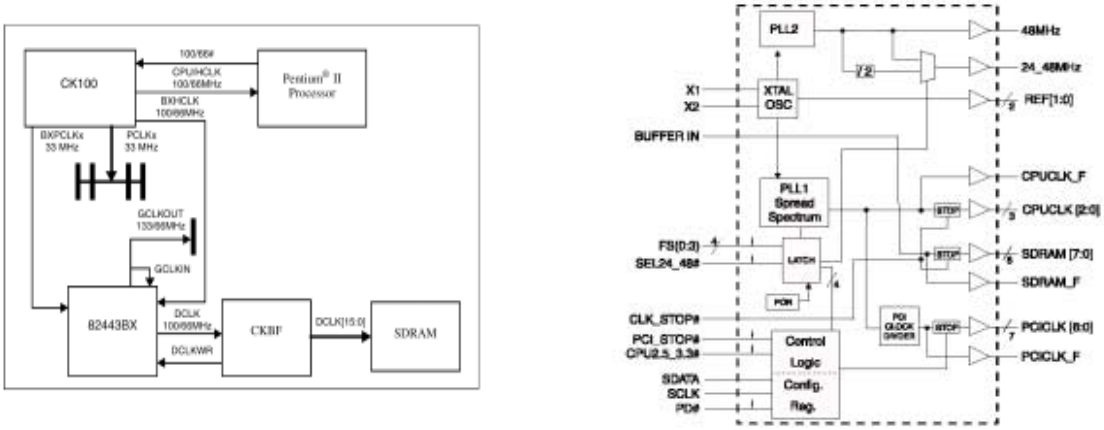

Figure 2 : System clock structure and ICS 9148-101 block diagram

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0.2.4 VGA Controller: ATI 3D Rage Mobility-M Integrated 4MB SDRAM

Supports PCI 33Mhz
Support dual view controller. Dual independent displays (LCD/CRT) and the resolutions, refresh rates and display data can be completely independent.
Primary display path supports:
- VGA and accelerated modes
- Video overlay
- Hardware cursor and hardware icon
- Palette gamma correction.

Supports both independent displays at 1024 x 768, 24bpp.
Secondary display path supports:
- Accelerated modes
- YUV422 video data
- 24-bit palette

Integrated dual 65MHz LVDS interface
- Up to 10 LVDS channels for power and EMI reduction.
- Dual pixel SXGA resolution TFT panels
- XGA resolution DSTN panels.
- 24bpp TFT (SGA/XGA) using dual pixel LVDS (versus 18 bpp using direct digital interface).
- 455 Mbps/channel with 65 MHz pixel clock rate.
- 3 pairs (+1 clock) and 4 pairs (+1 clock) modes for both single and dual pixel LVDS.
- FPDI-2 compliant; compatible with receivers from National Semiconductor and Texas Instruments.
- LVDS eye pattern to improve testability of LVDS module.

Flat panel power management:
- Automatic power down panel by programmable internal timer
- Standby/Suspend pins for hardware Power Management support.
- Standby/Suspend registers for software Power Management support.

Flat panel support:
- Color STN/DSTN/CSTN LCD panels up to XGA (1024 x 768) resolution, up to 160Hz-refresh rate, up to 256k colors on an 8-color panel.
- Color TFT panel up to 1600 x 1280 resolution, up to 24-bit per pixel, single/double pixel per clock.
- 2/4 levels of frame modulation can be done on 9-bit, 12-bit and 18-bit TFT panels.
- Hardware Z-buffer supports with both DSTN and TFT panels.
- Integrated LVDS interface support.
- Support for Panel Link Interface.
- Support external Panel Link transmitter.

- Panel ID to allow multiple panels support without swapping BIOS.
- Five bits allocated for panel ID.
- DDC support for LCD monitors.
- General-purpose I/O pins available to support DDC on LCD monitor applications.

Integrated a floating-point set-up engine
- Processing up to 1.2 million triangles per send.

Supports 100 MHz SGRAM:
- 64-bit, 100MHz SGRAM interface
- 800 MB/s of low-latency frame buffer bandwidth

ZV Port (PCMCIA compliant with CCIR601 timing)
- Allows transfer of video data directly into frame buffer without loading down PCI bus.
- Dedicated video port guarantees video frame rates (30 frames per second)
- Maximum 40 MHz, 16bpp YUV422 (PCMCIA specs 16 MHz maximum)

DVD and Video Support
- Enhanced motion compensation acceleration
- 4-tap horizontal and 2-tap vertical high quality DVD video scalar.
- De-interlacing filter, Video on graphics overlay, Multi-stream video
- Color-space conversion, Scatter-gather bus-master, Planar YUV mode
- ATI Multimedia Channel (AMC) video input port
- Zoom Video input port (ZV-port)
- Improves software DVD/MPEG-2 frame rate by 20 to 30%.
- Provides full motion MPEG-2 playback on Pentium III processors

Supports 3D Acceleration
- integrated 1 million triangle/s set-up engine
- 4K on-chip texture cache.
- Full screen or window double buffering for smooth animation
- Hidden surface removal using 16-bit Z-buffering
- Edge anti-aliasing
- Sub-pixel and sub-texel accuracy
- Gouraud and specular shaded polygons
- Prospectively correct mip-mapped texturing with chroma-key support.
- Full support of Direct3D texture lighting.

Extensive 3D mode support:
- Draw in RGBA32, RGBA16, and RGB16.
- Texture map modes: RGBA32, RGBA16,RGB8,ARGB4444, YUV444.
- Compressed texture mode: YUV422, CLUT4 (CI4), CLUT8(CI8), VQ

Mobile PCI 1.0 support.
Pin, Register and Timer modes for hardware and software power management.
Dynamic clock switching.

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Panel bias voltage and digital power control.
Self-refresh SDRAM in Suspend mode
Enhanced line buffer allows vertical filtering of native MPEG-2 size (720 x 480) images.
DVD/MPEG-2 decode assist provides dramatically improved frame rate
Hardware mirroring for flipping video images in video images in video conferencing systems.
Smooth video scaling and enhanced YUV to RGB color space conversion
Front and back end scalars support multi-stream video for video conferencing
Filtered horizontal/vertical, up/down, scaling enhances playback quality.

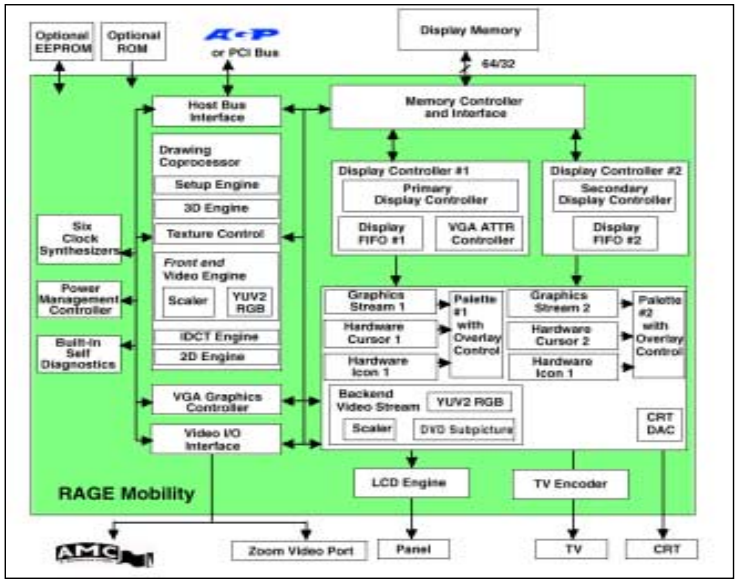

Figure 3: ATI Rage Mobility-M

0.2.5 PC Card Interface Controller: TI1410

ACPI 1.0 Compliance
PCI Power Management interface specification 1.0 Compliance
Supports distributed DMA (DDMA) and PC/PCI DMA
Advanced submicron, low-power CMOS technology.
Supports two I/O windows and two memory windows available to cardbus socket.
Supports five PCI memory windows and two I/O windows available to PC CARD16 socket.
Supports Burst Transfers To Maximize Data Throughput On Both PCI Buses
Provides Serial Interface To TI TPS2211 Single Slot PC CARD Power Interface Switch
Supports up to 5 general purpose I/O
Supports Distributed DMA(DDMA)
Pipelined architecture allows greater than 130Mbps second throughput from cardbus to PCI and from PCI to cardbus.
Support PCI Bus Lock (/LOCK)
3.3-V core logic with universal PCI interface
PCI Local Bus Specification Revision 2.2 compliant
1998 PC Card Standard compliant
Supports one 16-bit PC card or Cardbus card ;sockets powered at 3.3V or 5V with hot insertion and removal
ExCA compatible Registers mapped in memory or I/O space.
Supports ring indicate output, SUSPEND#, and programmable output select for CLKRUN#.
Provides socket activity LED signals.
Provides zoom video support signals.
144-Pin LQFP package

0.2.6 Single-Slot PC Card Power Interface Switch: TPS2211

Fully Integrated Vcc and Vpp Switching for Single-Slot PC Card Interface
3.3 V Low-Voltage Mode
Meets PC Card Standards
RESET for System Initialization of PC Cards
12-V Supply Can Be Disabled Except During 12-V Flash Programming
Short Circuit and Thermal Protection
16-Pin SSOP (DB)
Compatible With 3.3-V, 5-V and 12-V PC Cards
Low $Rds_{(on)}$ (140-mOHM 5-V Vcc Switch; 110-mOHM3.3-V Vcc Switch)
Break-Before-Make Switching

0.2.7 AC'97 AUDIO SYSTEM: CRYSTAL CS 4299

82440MX is an AC'97 2.1 compliant controller that communicates with companion codecs via a digital serial link called the AC-link.
The AC'97 CODEC provides a complete high quality audio solution, feature include:
20-bit Stereo Digital-to-Analog Converter and 18-bit Stereo Analog to Digital Converter with Sample Rate Conversion
Four Analog Line-level Stereo Inputs for Connection from LINE IN, CD, VIDEO, and AUX
Two Analog Line-level Mono Inputs for Modem Sub-system and Internal PC Beeper
Mono Microphone Input Switch able from Two External Sources
High Quality Pseudo Differential CD Input
Dual Stereo Line-level Outputs
CrystalClear 3D Stereo Enhancement

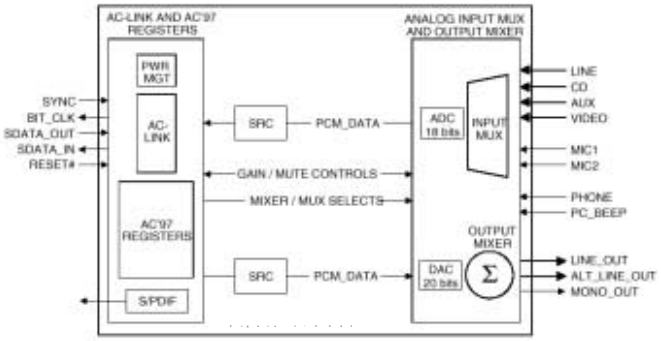

Figure 4:CS4299

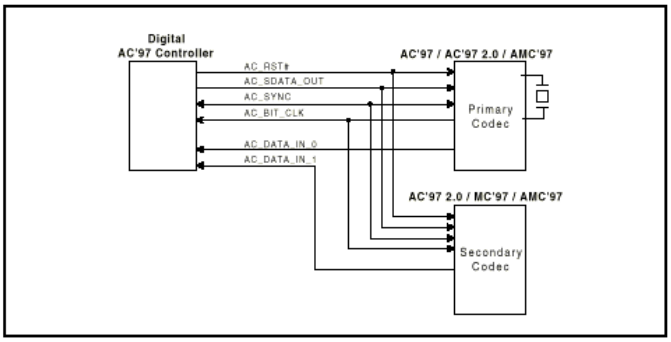

Figure5:AC links

0.2.8 MDC: PCTel MODEM DAUGHTER CARD

ITU-T V.90 (56Kbps), V.34 (4.8Kbps TO 33.6 Kbps), V.32 bis (4.8Kbps to 14.4Kbps), V.22 bis (1.2 bps to 2.4 Kbps), V.21 and Bell 103 and 212A(300 to 1200 bps) modulation protocol.
Automode
Virtual com port with a DTE throughout up to 460.8Kbps.
G3 Fax compatible
Auto dial and auto answer
Ring detection
Support AC-link primary and secondary operating modes
Support ACPI power management
Operating temperature range from 0 to 60 degree c
Power consumption less than 100Mw
Support PCTel, Modem driver on demand

0.2.9 Super IO: NS PC 97338VJG

High speed PC16550A compatible UART with receive/transmit 16 Bytes FIFO programmable serial baud rate generator
Multi-mode parallel port support including standard port, EPP/ECP (IEEE1284 compliant, 2 interrupt pins)
Plug and Play module
FDC, 100% IBM compatible, S/W & register compatible to 82077 with 16Bytes data FIFO
Support 3-Mode FDD
FIR/MIR/SIR/SHARP ASK for Infrared application.
COM2

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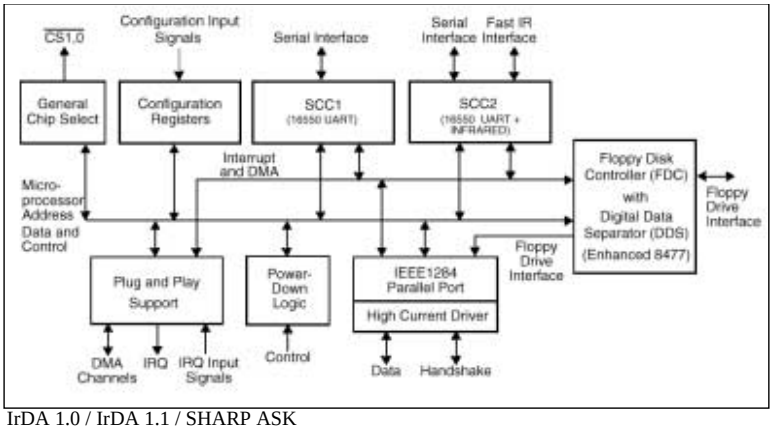
High speed PC16550A compatible UART with receive/transmit 16 Bytes FIFO programmable serial baud rate generator
Multi-mode parallel port support including standard port, EPP/ECP (IEEE1284 compliant, 2 interrupt pins)
Plug and Play module
FDC, 100% IBM compatible, S/W & register compatible to 82077 with 16Bytes data FIFO
Support 3-Mode FDD
FIR/MIR/SIR/SHARP ASK for Infrared application.
COM2



IrDA 1.0 / IrDA 1.1 / SHARP ASK
Baud rate: max. 4Mb
Link distance: 0.01 to 1 m
Half angle: ±15°
Bit Error Rate (BER) : 10^{-9}
Peak wavelength: 0.85 - 0.90 µm
TQFP 100 pins
Standby mode: control by software

Figure 6: NS PC97338VJG

	IO address	IRQx	DRQx
COM1	3F8-3FF	4	-
FIR/MIR/SIR/ SHARP ASK (COM2)	278-27F	3	-
PIO	378-37F	7	-
FDD	3F0-3FF	6	2

Table 1: 97338 IO address.

0.2.10 IR MODULE: VISHAY TFDU6101E

Compliant to IrDA 1.1 (Up to 4 Mbit/s) HP-SIR, Sharp ASK and TV Remote Wide Operating Voltage Range 2.6 V to 5.5 V
Small Module Size 4.0 x 9.9 x 4.7 mm (HxWxD)
Low Power Sonsumption (3mA Supply Current).
Power Shutdown Mode (1uA Shutdown Current).
Built-in EMI protection
Edge Detection Input Prevents the LED from long turn-on time
Directly Interface with various Super I/O and Controller Devices
Few External Components Required

0.2.11 Keyboard System: H8(3434) Universal Keyboard Controller

CPU: Two-way general register configuration
Eight 16-bit registers or Sixteen 8-bit registers
High-speed operation
Maximum clock rate : 16Mhz at 5V
Memory
include 32KB ROM and 1KB RAM
16-bit free-running timer
One 16-bit free-running counter
Two output-compare lines
Four input capture lines

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8-bit timer (2 channels)
- Each channel has one 8-bit up-counter , two time constant registers

PWM timer (2 channels)
- resolution :1/250
- Duty cycle can be set from 0 to 100%

I^2C bus interface (one channel)
- include single master mode and slave mode

Host interface (HIF)
- 8-bit host interface port
- Three host interrupt requests (HIRQ1,11,12)
- Regular and fast A20 gate output

Keyboard controller
- Controls a matrix-scan keyboard by providing a keyboard scan function with wake-up Interrupts and sense ports

A/D converter
- 10-bit resolution
- 8 channels : single or scan mode (selectable)

D/A converter
- 8-bit resolution
- 2 channels

Interrupts
- nine external interrupt lines : NMI# , IRQ0 to 7# 26 on-chip interrupt sources

Power-down modes
- Sleep mode
- Software standby mode

Hardware standby mode
A single chip microcomputer
On-chip flash memory
Maximum 64-kbyte address space
Support three PS/2 port for external keyboard, mouse and internal track pad.
Support SMI,SCI trigger input:
Cover switch
Battery charging control
Smart Battery monitoring
Control D/D system on/off
Fan control and LED indicator serial interface
100pin TQFP

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0.2.12 System Flash Memory (BIOS)

2 M bit Flash memory
Flashed by 5V only
User can upgrade the system BIOS in the future just running flash program.

0.2.13 Memory System

0.2.13.1 On Board Main Memory

PC100 SDRAM on board

Config 1: memory size: 4Mx16bit SDRAM x8 pcs. Total 64Mbyte
Config 2: memory size: 8Mx16bit SDRAM x4 pcs. Total 64Mbyte
Config 3: memory size: 8Mx16bit SDRAM x8 pcs. Total 128Mbyte

Standard 54 pin TSOP package.
Power supply: 3.3V±0.3V
Memory bus bandwidth: 64 bits

0.2.13.2 JEDEC 144-pin SO DIMM sockets

Supports one JEDEC 144-pin SO DIMM sockets on Mother Board for expansion Supports 3.3V SDRAM
2 banks on one socket
PC-100 DIMM Module uses only.
Max Address line: A0.. A11, BA0 BA1

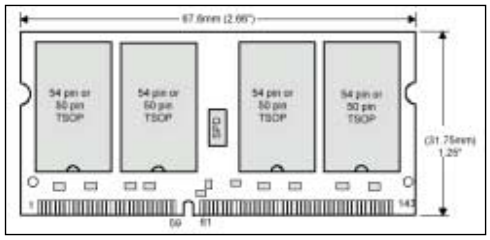

Figure 7: SO-Dimm Module.

0.2.14 LAN : Realtek RTL8139CL

128 pins TQFP
Integrated Fast Ethernet MAC, Physical chip and transceiver in one chip
10 Mb/s and 100 Mb/s operation
PCI local bus single-chip Fast Ethernet controller
Compliant to PCI Revision 2.2
Supports PCI clock 16.75MHz-40MHz
Supports PCI target fast back-to-back transaction
Supports ACPI, PCI power management
Supports LAN WAKE-UP function (Magic packet only)
Provides PCI bus master data transfers and PCI memory space or I/O space mapped data transfers of RTL8139A's operational registers.
Support 10 Mb/s and 100 Mb/s N-way Auto-negotiation operation
Support up to 128K bytes Boot ROM interface
Allow remote wake-up(Magic packet and Microsoft wake-up frame)
Include a programmable, PCI burst size and early tx/rx threshold
Support a 32-bit general-purpose timer, referenced by the external PCI clock source, and timer-interrupt
Contain two large (2Kbyte) independent receive and transmit FIFOs
Use 9346 (64*16-bit EEPROM) to store resource configuration and ID parameter
Support LED pins for various network activity indications
Support digital and analog loopback capability on both ports
Half/Full duplex capability
Support Full Duplex Flow Control (IEEE 802.3x)

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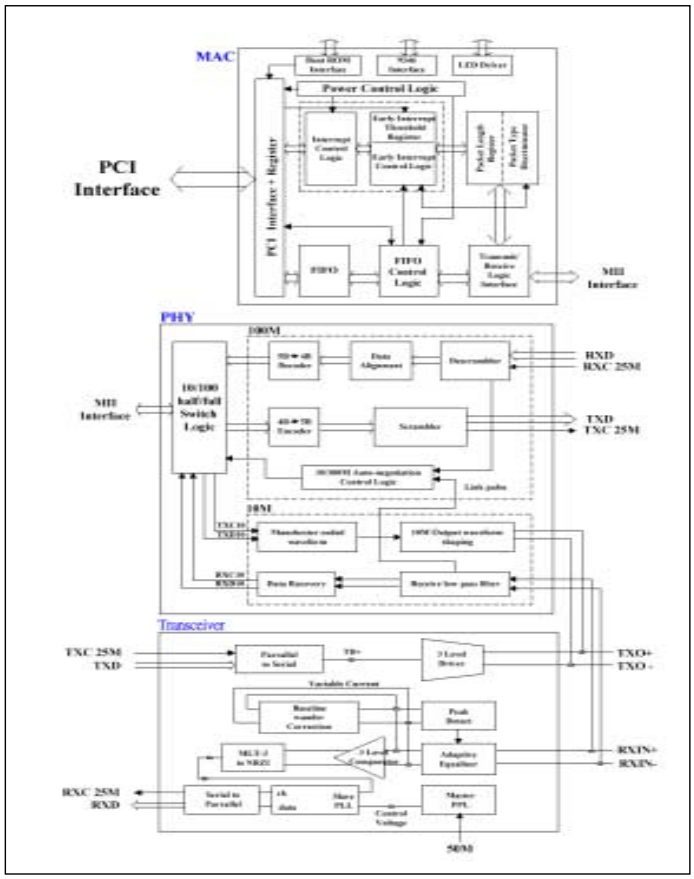


Figure 8:RTL8139CL Block Diagram

0.2-15 IEEE 1394 : NEC uPD72870A

-The μPD72870A is the LSIs which integrated OHCI-Link and PHY function into a single chip.
-The μPD72870A comply with the P1394a draft 2.0 specifications and the OpenHCI IEEE1394 1.0 and work up to 400 Mbps.
-Compliant with Link Layer Services as defined in 1394 Open Host Controller Interface specification release 1.0
-Compliant with Physical Layer Services as defined in P1394a draft 2.0 (Data Rate 100/200/400 Mbps)
-Compliant with protocol enhancement as defined in P1394a draft 2.0
-Modular 32-bit host interface compliant to PCI Specification release 2.1
-Support PCI-Bus Power Management Interface Specification release 1.0
-Modular 32-bit host interface compliant to Card Bus Specification
-Cycle Master and Isochronous Resource Manager capable
-Built-in FIFOs for isochronous transmit (1024 bytes), asynchronous transmit (1024 bytes), and receive (2048bytes)
-32-bit CRC generation and checking for receive/transmit packets
-4 isochronous transmit DMAs and 4 isochronous receive DMAs supported
-32-bit DMA channels for physical memory read/write
-Clock generation by 24.576 MHz Xtal
-Internal control and operational registers direct-mapped to PCI configuration space
-2-wire Serial EEPROM TM interface supported
-Separate power supply Link and PHY

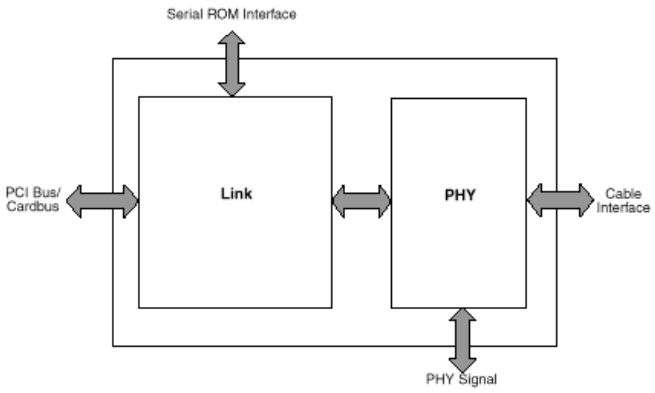
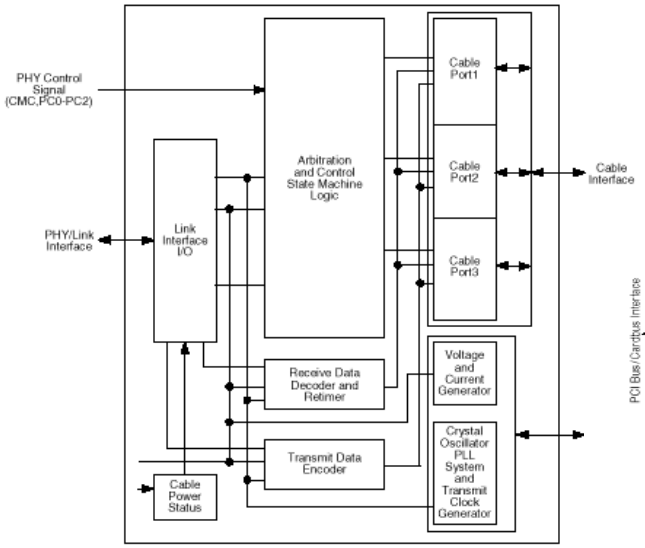


Figure 9 :Block Diagrams

M722 N/B MAINTENANCE



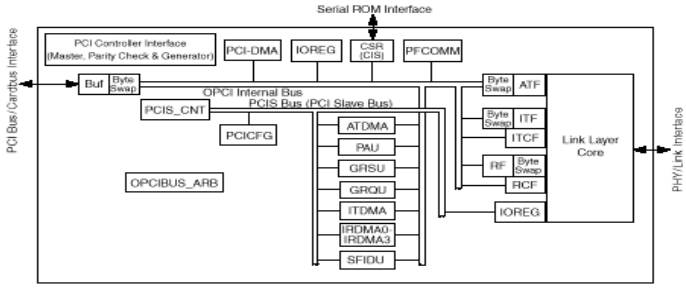


Figure 11:Link Block Daigrams

Remark Cable Port:

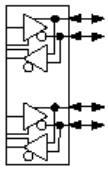


Figure 10:PHY Block Daigrams

M722 N/B MAINTENANCE

0.3. I/O PORT

One Power Supply Jack.
One External CRT Connector For CRT Display
IRDA SIR /MIR/FIR
Supports four USB port for all USB devices (Std x2+Min x2)
One Mini IEEE 1394 port for all IEEE 1394 Device
One MODEM RJ-11 phone jack for PSTN line
One RJ-45 for LAN.
S/PDIF Digital Audio output
Microphone Input Jack.
One Cardbus Socket for extension
One IDE extended port for IDE CDROM/DVD

0.4.PERIPHERAL COMPONENTS

0.4.1LCD PANEL

Brand	model mane
HITACHI	TX31D70VC1CAA/XGA(P)
HYUNDAI	HT12X11-100(P)
SANYO	TM121XG-02L02A

0.4.2 Floppy Disk Drive(USB)

Mitsumi: D353GU (3.5” 1.44MB/1.2MB/720KB FDD)

0.4.3 HDD

IBM (2.5” 9.5mmH): 6.0GB – DARA-206000
12GB – DARA-212000
Hitachi (2.5” 9.5mmH): 6.0GB – DK23AA-60 (P)
12GB – DK23AA-12 (P)

0.4.4 24X CD-ROM Drive

Brand	*model mane*
Quanta	SCR-242E
Matsushita	UJDA150

0.4.5 8X DVD-ROM drive

Brand	*model mane*
QUANTA	SDR-081E

0.4.6 Keyboard

OKI

0.4.7 Touch Pad

ALPS

0.4.8 Fan

0.5. APPENDIX 1: BANISTER GPIO DEFINITIONS

Signal Name	POWER PLANE	Input	Output/OD	Device Activity Monitor	Default Function Value	GPIO_DIR Defaults	M722 GPIO Setting	
GPIO0	Resume	PME#			PME#,1	Input	I	SCI#
GPIO1	Resume	GPI(1)			GPIO1	Input	O	GCL_LO/HI#
GPI02					GPIO2	Input	O	SPK_OFF
GPIO3			GNTA#		GPIO3	Output	O	IDE_RST#
GPIO4	Resume			Generic0	Generic 0	Input	O	HDD_PWR#
GPIO5				Pide1	PIDE1	Input	I	CRTIN#
GPIO6	Resume	IRQ8#			GPIO6	Input	O	CD_PWR
GPIO7		SERIRQ	SERIRQ		GPIO7	Input	I/O	SERIRQ
GPIO8	Core	THERM#			THERM#,1	Input	I	THERM#
GPIO9	Resume					Input	I	KBD_US/JP
GPIO10	Resume	LID			LID,0	Input	O	CDROM_PLUG#
GPIO11	Resume	BATLOW#			BATLOW#,1	Input	O	H8_12V
GPIO12	Resume	RI#			RI#,1	Input	I	WAKE_UP#
GPIO13				AUDIO	AUDIO	Input	I	IDEDASP_ON
GPIO14			SPKR	FDD	SPKR,0	Output	O	SPKR
GPIO15				SERIAL A	SERIAL A	Input	I	CCD1#
GPIO16			PCS1#	SERIAL B	PCS1#,1	Output	I	HUB_SUSPEND#
GPIO17	Resume			LPT	LPT	Input	O	MD/ID0
GPIO18	Resume			GENERIC 1	GENERIC 1	Input	O	MD/ID1#
GPIO19			PCS0#	GFX	PCS0#,1	Output	O	LAN_IN#
GPIO20	Resume			CARDBUS 0	CARDBUS 0	Input	O	IRMD0
GPIO21		ZEROWS#		CARDBUS2	ZEROWS#,1	Input	I	ZER0WS#
GPIO22		PIRQC#	PIRQC#		PIRQC#,1	Input	I	PIRQC#
GPIO23		PIRQD#	PIRQD#		PIRQD#,1	Input	I	PIRQD#
GPIO24	Resume	EXTSMI#	EXTSMI#		EXTSMI#,1	Input	I	EXTSMI#
GPIO25			MSSS#		MSSS#,1	Output	O	MCCS#
GPIO26			KBCCS#		KBCCS#,1	Output	O	KBCS#
GPIO27		DREQ3			DREQ3,0	Input	I	DREQ3
GPIO28			DACK3#		DACK3#,1	Output	O	DACK3#
GPIO29		PREQ3				Input	I	PREQ3#
GPIO30			PGNT3#			Output	O	PGNT3#

Table 2: GPIO definitions.

M722 N/B MAINTENANCE

0.6.M722 External Specifications R0.4

CPU	- Mobile Pentium Ⅲ 600/650/700/750/800/850MHz with Intel SpeedStep Technology, uPGA2 package. - Celeron 450/500/550/600/650/700MHz, uPGA2 pkg.
Chipset	Intel 440MX, support 100MHz FSB
L2 Cache	256KB On-Die (P Ⅲ), 128KB On-Die (Celeron)
System BIOS	Flash EPROM - Include System BIOS and VGA BIOS - ACPI 1.0 - DMI 2.X
Memory	- 64MB SDRAM onboard - 144-pin SDRAM SO-DIMM Memory Module x1 (64-bit data bandwidth) - Expandable to 192MB (user upgaradable)
ROM Drive	- Support External 24X CD-ROM/8X DVD ROM Drive (IDE I/F, support boot-up) - CD-RW support for future models (Factory option)
FDD	- 3.5" Format for 720KB/1.2MB/1.44MB - External USB I/F - Support USB FDD boot
HDD	- 2.5" 8.45/9.5 mm height: 5/6/10/12/15GB - support Ultra DMA33/66
Display	- 12.1" XGA TFT display - AGAR (Anti-Glare & Anti-Reflection) - 16M colors in LCD - Resolution: 1024x768 XGA
Video Controller	- ATI Mobility-M (4MB SDRAM integrated) - Support Multi Monitor
Keyboard & Button	- 18mm pitch/2.5mm stroke - 5X QUICK Start BUTTONs: functions defined by user - 1X Mail Checking Button - support Windows98 system start & Application start/user friendly interface
Pointing Device	- Two buttons; GlidePad (a touch-sensitive controlpad)
PCMCIA	- Type II x 1 - CardBus support - ZV Port Support
Memory slot	Support Security Digital card slot for next products

M722 N/B MAINTENANCE

Audio System	- Built-in sound board - Sound Blaster Pro compatible, 16-bit sampling and playback - Full duplex supported - Built-in mono microphone and monaural speaker - S/PDIF Digital Audio Output
I/O Port	- USB port with Rubber cover and Strap x 4 (Mini × 2) - FIR port x 1; complies with ASK and IrDA (4Mbps and 115Kbps) - RJ-11 port x 1 - RJ-45 port x 1 (LAN & Modem w/z rubber cover x 1) - DC input x 1 - VGA monitor port with door x 1 (P.P or Niron detachable) - Audio-out (Optical with Copy protect) x 1 - Mic-in x 1 - Hardware volume control - IEEE1394 x 1 - CD-ROM drive port (IDE)
LAN	10Base-T/100Base-TX (Built-in)
FAX modem	56kbps MDC modem (K56Flex & V.90)
Power Supply	- 4-cell Li-ion Battery standard, optional battery (12-cell Li-ion) - User swappable - BATT Life: 1.5hrs with standard battery (4-cell Li-ion; 20.7W) , 4.5hrs with optional battery (12-cell Li-ion; 62.2W)
AC adapter	Universal AC adapter 60W; Input:100-240V, 50/60Hz AC
Dimensions	Main unit: 269x218x24.4(Min.)/28.3 (Max.) mm
Weight	Main System: 1.575Kg (incl. HDD & CPU; w/o CD-ROM Drive & FDD)
Accessories	Power Cord, AC Adapter, Modem Bitware software, Phone Cord with RJ-11 Jack, Modem Driver, Modem & LAN Port Cover, Manual, Driver CD-Title, Heatsink
Architecture	Support PC99 Specification, support WfM2.0
Options	32/64/128MB SDRAM, Li-ION BATT (12-cell), External CD-ROM/DVD-ROM Drive w/z IDE I/F, External FDD w/z USB I/F, AC Adapter w/o Power Cord, Carry Bag, USB-Parallel Cable, USB-Serial Cable, USB Lead-Bus, Mini USB-Standard USB, USB-Combo Parallel & Serial Port

0.7. Output Power

The LCD backlight inverter shall provide AC outputs as specified below.

0.7.1 Inverter Output Characteristics

AC Output Parameters

The follow specification is used for single lamp of LCD panel.

Parameter	Minimum	Nominal	Maximum	Units
Lamp ignition voltage (Vs)	----	----	1450	Volts-rms.
Lamp discharging voltage (VL)	----	650	----	Volts-rms.
Lamp discharging current (IL)	2.2	4.5	6.0	mA-rms.
Lamp discharging frequency	50	55	60	KHz

0.7.2 AC Load Characteristics

The inverter shall be one LCD of either type listed below :

ITEM	Vendor(Inverter)	Vendor(LCD Panel)
1	INN-SU N 23A9S-01E(412219300045)	SANYO (TM121XG-02L02)
2	INN-SU N 23A9S-01E(412219300045)	SAMSUNG (LTM121X1-L01)
3	INN-SU N 23A9S-01E(412219300045)	HITACHI (TX31D70VC1CAA)

M722 N/B MAINTENANCE

0.8. Electronic Specification

0.8.1Input Section

A) Adapter

Input Power : 60W
Input Voltage : 19V
Input Current : 0 – 3.16A

B) Battery pack

Specifications :

Battery pack (Li-ION)

Vendor	**Panasonic**	**Panasonic**
Type	**Li-Ion**	**Li-Ion**
Size	**10.3x34.0x49.8**	**10.3x34.0x49.8**
Pieces per Pack	**4cells**	**12 cells**
Nominal Voltage/Pack	**14.8 V**	**14.8 V**
Capacity	**1400 mAh**	**4200mAh**
Supply Power	**20.72W**	**62.16W**
Part P/N	**44268900001**	**442668900002**

Protection：Timer, Thermal Breaker, Temperature Sensor.

Service Life：>300 charge/discharge cycles, 85% capacity

Charging Time：(4S1P) Li-Ion 2hrs Full Charge by system OFF.
3.6 hrs Slow Full Charge by system ON.
(4S3P) Li-Ion 3hrs Full Charge by system OFF.
11 hrs Slow Full Charge by system ON.

0.8.2 Output Section

The power module have following output:

A) Vcc3 +3.3V 4.5A
B) Vcc5 +5.0V 4.5A
C) Vcc_core Adi. For cpu select 14A
D)Vcc12 +12.0V 0.1A
E) VTT +1.5V 2.7A
F) +2.5V +2.5V 1A
G) VDD5 +5V 80mA
There are limits in following table:

OUTPUT CHARACTERISTICS

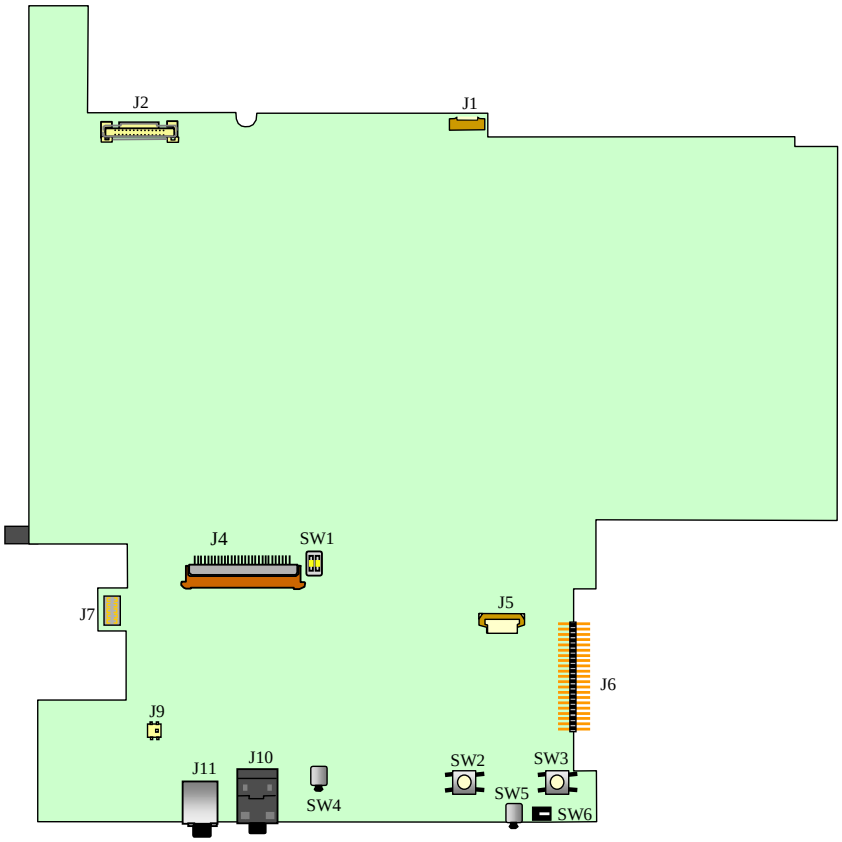
OUTPUT	Vcc5	Vcc3	V cc_core	VTT
Tolerance	+/-5%	+/-5%	+/-5%	+/-5%
MIN. CURRENT	0.5A	0.5A	0.5	0.5A
MAX. CURRENT	4.5A	4.5A	14A	2.7A
PEAK CURRENT	5A	5A	18A	3A
RIPPLE AND NOISE	100mV	100mV	100mV	100mV
O.V.P.	5.6V	3.6V	-	-
SHORT PROTECT	v	v	v	-
OVER SHOOT	100mV	100mV	115mV	115mV
EFFICIENCY	85%	85%	80%	85%

OUTPUT	VDD5	+2.5V	Vcc12	
Tolerance	+/-5%	+/-5%	+/-5%	
MIN. CURRENT	0A	0.5A	0A	
MAX. CURRENT	80mA	1A	80mA	
PEAK CURRENT	100mA	1.5A	100mA	
RIPPLE AND NOISE	120mA	100mV	120mV	
O.V.P.	-	-	-	
SHORT PROTECT	-	-	v	
OVER SHOOT	200mA	100mV	200mV	
EFFICIENCY	-	-	-	

M722 N/B MAINTENANCE

1. DEFINITION & LOCATION OF CONNECTORS/SWITCHES

1.1 Mother Board-A



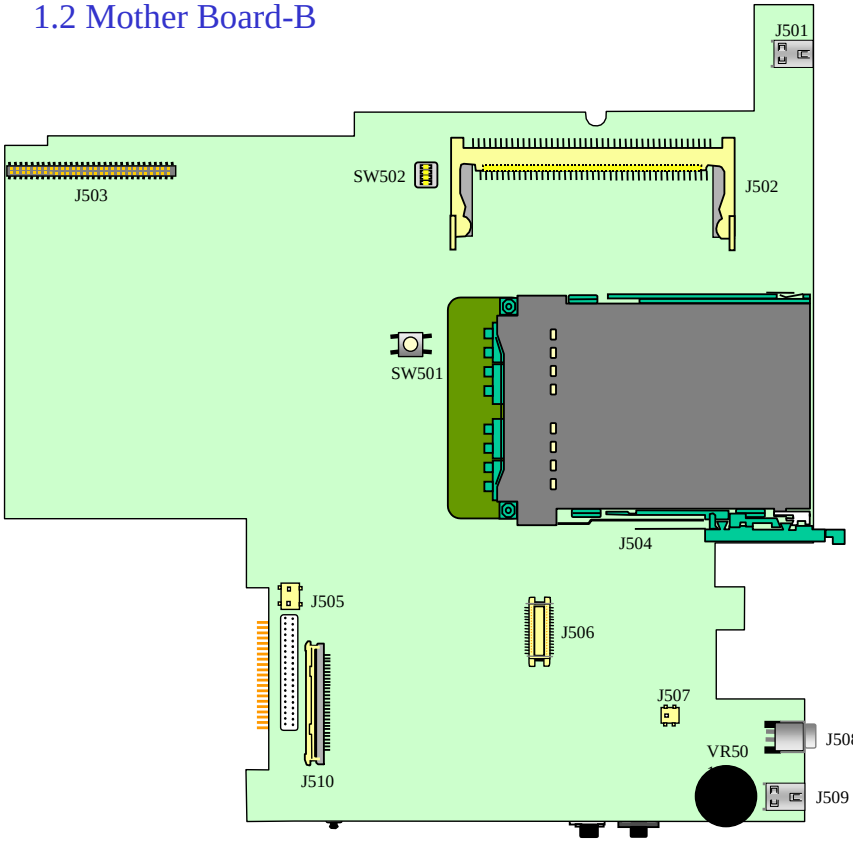
- J1: Quick key transfer BD connector.
- J2: LCD panel connector.
- J4: Internal keyboard connector.
- J5: Touch_pad module connector
- J6: Hard disk drive connector.
- J7: MDC/LAN transfer board connector.
- J9: Internal left channel speaker connector.
- J10: External speaker connector .
- J11: External MIC-in connector.

- SW1: Country selection for keyboard
- SW2: Left button switch of touch-pad.
- SW3: Right button switch of touch-pad.
- SW4: E-Mail button.
- SW5: Battery Capacity button.
- SW6: Cover Suspend SW.

M722 N/B MAINTENANCE

1. DEFINITION & LOCATION OF CONNECTORS/SWITCHES

1.2 Mother Board-B



- J501: USB connector.
- J502 : 144 pins expansion SDRAM socket.
- J503: DC/DC board connector.
- J504: PC card socket.
- J505: USB connector
- J506: MDC/LAN transfer board connector
- J507: CMOS Battery connector.
- J508: 1394 connector.
- J509: USB connector.
- J510: CD-ROM drive connector.
- SW501: System reset button.
- SW502: LCD Panel ID Section.

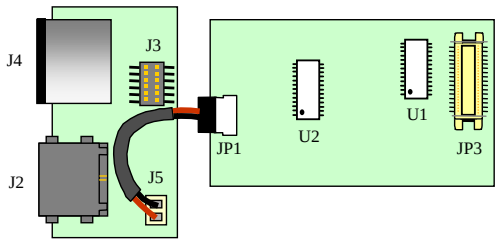
M722 N/B MAINTENANCE

1. DEFINITION & LOCATION OF CONNECTORS/SWITCHES

1.3 Daughter Board

MDC/LAN transfer board

- J2: RJ-11 phone jack for internal modem.
- J3: Connector 1 for connected MDC/LAN transfer board to M/B.
- J4: RJ-45 internal LAN connector.
- J5: MDC jump wire connector.

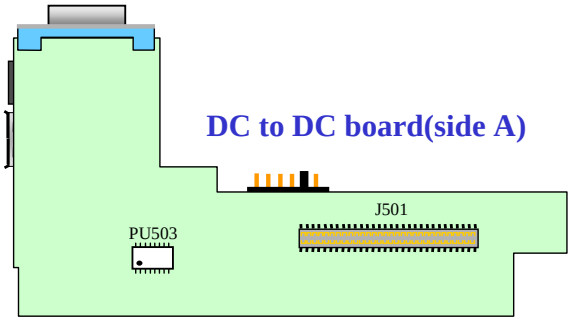


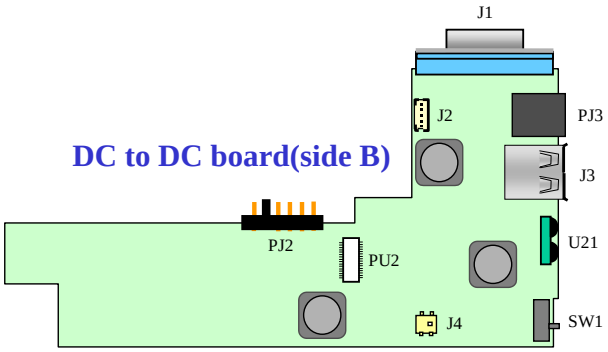
- JP1: MDC jump wire connector.
- JP3: Connector 2 for connected MDC/LAN transfer board to M/B.

M722 N/B MAINTENANCE

1. DEFINITION & LOCATION OF CONNECTORS/SWITCHES

1.3 Daughter Board



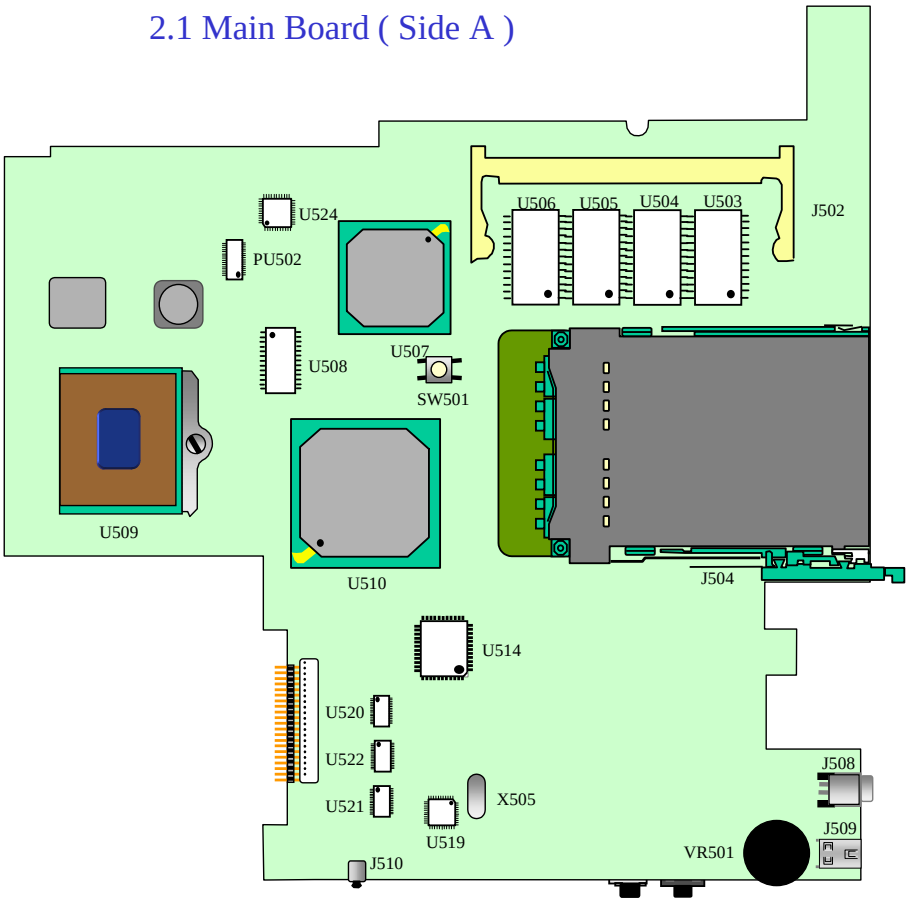


- J501: Connector for connected the DC/DC BD to M/B.

- J1: External VGA monitor connector.
- J2: Backlight connector for LCD panel.
- J3: USB Connector.
- J4: FAN Connector.
- PJ3: Power jack (AC adapter).
- PJ2: Battery pack connector.
- SW1: System power on/off switch.

2. DEFINITION & LOCATION OF MAJOR COMPONENTS

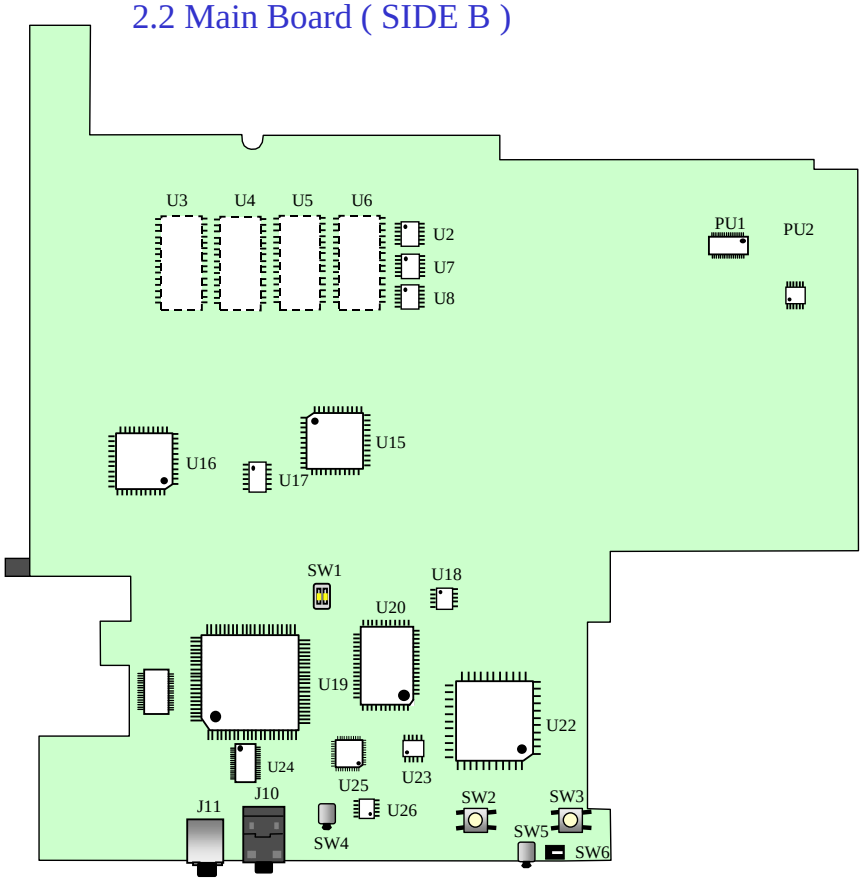
2.1 Main Board (Side A)



- U524: GCL W/GEYSERVILLE.
- U507: RAGE MOBILITY-M VGA controller.
- U508: ICS9248-101 Clock syntheriser.
- U503~U506: On board 64MB main memory.
- U509: CPU INTEL PIII/Celeron µPGA2-495.
- U510: Banister.
- U514: System BIOS.
- U520~U522: 74CBTD3384.
- U519: TUSB2036 USB HUB.
- VR501: Volume Up & Down.
- J502: Ext SDRAM socket.
- J504: PC Card socket.
- J508:1394 connector.
- J509: USB connector.
- J510: E-mail switch.

2. DEFINITION & LOCATION OF MAJOR COMPONENTS

2.2 Main Board (SIDE B)

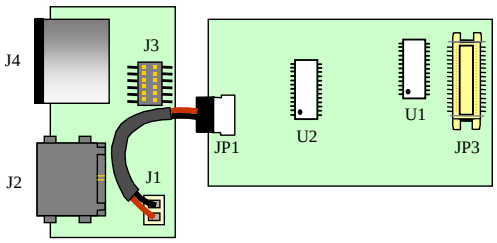


- PU1: ADP3421.
- U3~U6: On board memory(N/A) (option).
- U2, U7, U8: 74AC244 signals buffer.
- U15: Super IO PC93338VJG.
- U16: H8/F3434.
- U20: RTL 8139 PCI BL PCI LAN.
- U19: IEEE 1397 UPD72870.
- U22: PCI1410 Card bus controller.
- U24: LM4834 AUDIO AMP.
- SW1: Country selection for keyboard.
- SW2: Left button switch of touch-pad.
- SW3: Right button switch of touch-pad.
- SW4: E-Mail button.
- SW5: Battery Capacity button.
- SW6: Cover Suspend SW.

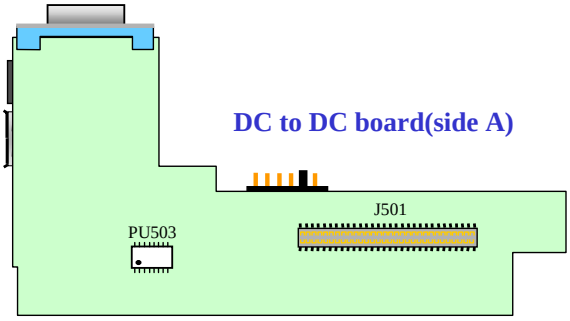
2. DEFINITION & LOCATION OF MAJOR COMPONENTS

2.3 Definition Of Daughter Board

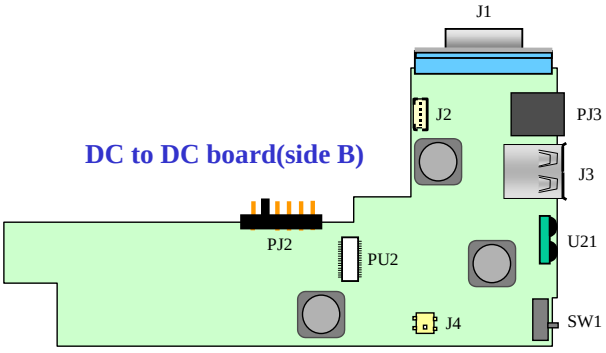
MDC/LAN transfer board



DC to DC board(side A)



DC to DC board(side B)



IR module

3. PIN DESCRIPTIONS OF MAJOR COMPONENTS

3.1 Pentium III/Celeron µPGA2 CPU

Alphabetical Signal Reference

Signal Name	I/O	Signal Description
A[35:3]#	I/O GTL+	The A[35:3]# (Address) signals define a 2^{36}-byte physical memory address space. When ADS# is active, these signals transmit the address of a transaction; when ADS# is inactive, these signals transmit transaction information. These signals must be connected to the appropriate pins/balls of both agents on the system bus. The A[35:24]# signals are protected with the AP1# parity signal, and the A[23:3]# signals are protected with the AP0# parity signal. On the active-to-inactive transition of RESET#, each processor bus agent samples A[35:3]# signals to determine its power-on configuration. See Section 4 of this document and the *PentiumII Processor Developer's Manual* for details.
A20M#	I 1.5V Tolerant	If the A20M# (Address-20 Mask) input signal is asserted, the processor masks physical address bit 20 (A20#) before looking up a line in any internal cache and before driving a read/write transaction on the bus. Asserting A20M# emulates the 8086 processor's address wrap-around at the 1-Mbyte boundary. Assertion of A20M# is only supported in Real mode.
ADS#	I/O GTL+	The ADS# (Address Strobe) signal is asserted to indicate the validity of a transaction address on the A[35:3]# signals. Both bus agents observe the ADS# activation to begin parity checking, protocol checking, address decode, internal snoop or deferred reply ID match operations associated with the new transaction. This signal must be connected to the appropriate pins/balls on both agents on the system bus.
AERR#	I/O GTL+	The AERR# (Address Parity Error) signal is observed and driven by both system bus agents, and if used, must be connected to the appropriate pins/balls of both agents on the system bus. AERR# observation is optionally enabled during power-on configuration; if enabled, a valid assertion of AERR# aborts the current transaction. If AERR# observation is disabled during power-on configuration, a central agent may handle an assertion of AERR# as appropriate to the error handling architecture of the system.
AP[1:0]#	I/O GTL+	The AP[1:0]# (Address Parity) signals are driven by the request initiator along with ADS#, A[35:3]#, REQ[4:0]# and RP#. AP1# covers A[35:24]#. AP0# covers A[23:3]#. A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. This allows parity to be high when all the covered signals are high. AP[1:0]# should be connected to the appropriate pins/balls on both agents on the system bus.
BCLK	I 2.5V Tolerant	The BCLK (Bus Clock) signal determines the system bus frequency. Both system bus agents must receive this signal to drive their outputs and latch their inputs on the BCLK rising edge. All external timing parameters are specified with respect to the BCLK signal.

Signal Name	I/O	Signal Description
BERR#	I/O GTL+	The BERR# (Bus Error) signal is asserted to indicate an unrecoverable error without a bus protocol violation. It may be driven by either system bus agent and must be connected to the appropriate pins/balls of both agents, if used. However, the mobile Pentium III processors do not observe assertions of the BERR# signal. BERR# assertion conditions are defined by the system configuration. Configuration options enable the BERR# driver as follows: • Enabled or disabled • Asserted optionally for internal errors along with IERR# • Asserted optionally by the request initiator of a bus transaction after it observes an error • Asserted by any bus agent when it observes an error in a bus transaction
BINIT#	I/O-GTL+	The BINIT# (Bus Initialization) signal may be observed and driven by both system bus agents and must be connected to the appropriate pins/balls of both agents, if used. If the BINIT# driver is enabled during the power-on configuration, BINIT# is asserted to signal any bus condition that prevents reliable future information. If BINIT# is enabled during power-on configuration, and BINIT# is sampled asserted, all bus state machines are reset and any data which was in transit is lost. All agents reset their rotating ID for bus arbitration to the state after reset, and internal count information is lost. The L1 and L2 caches are not affected. If BINIT# is disabled during power-on configuration, a central agent may handle an assertion of BINIT# as appropriate to the Machine Check Architecture (MCA) of the system.
BNR#	I/O-GTL+	The BNR# (Block Next Request) signal is used to assert a bus stall by any bus agent that is unable to accept new bus transactions. During a bus stall, the current bus owner cannot issue any new transactions. Since multiple agents may need to request a bus stall simultaneously, BNR# is a wired-OR signal that must be connected to the appropriate pins/balls of both agents on the system bus. In order to avoid wire-OR glitches associated with simultaneous edge transitions driven by multiple drivers, BNR# is activated on specific clock edges and sampled on specific clock edges.
BP[3:2]#	I/O GTL+	The BP[3:2]# (Breakpoint) signals are the System Support group Breakpoint signals. They are outputs from the processor that indicate the status of breakpoints.
BPM[1:0]#	I/O GTL+	The BPM[1:0]# (Breakpoint Monitor) signals are breakpoint and performance monitor signals. They are outputs from the processor that indicate the status of breakpoints and programmable counters used for monitoring processor performance.

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3.1 Pentium III/Celeron µPGA2 CPU

Alphabetical Signal Reference

Signal Name	I/O	Signal Description
BPRI#	I GTL+	The BPRI# (Bus Priority Request) signal is used to arbitrate for ownership of the system bus. It must be connected to the appropriate pins/balls on both agents on the system bus. Observing BPRI# active (as asserted by the priority agent) causes the processor to stop issuing new requests, unless such requests are part of an ongoing locked operation. The priority agent keeps BPRI# asserted until all of its requests are completed and then releases the bus by deasserting BPRI#.
BREQ0#	I/O GTL+	The BREQ0# (Bus Request) signal is a processor Arbitration Bus signal. The processor indicates that it wants ownership of the system bus by asserting the BREQ0# signal. During power-up configuration, the central agent must assert the BREQ0# bus signal. The processor samples BREQ0# on the active-to-inactive transition of RESET#.
BSEL[1:0]	I 1.5V Tolerant	The BSEL[1:0] (Select Processor System Bus Speed) signal is used to configure the processor for the system bus frequency. Table 38 shows the encoding scheme for BSEL[1:0]. The only supported system bus frequency for the mobile Pentium III processor is 100 MHz. If another frequency is used or if the BSEL[1:0] signals are not driven with "1" then the processor is not guaranteed to function properly. **BSEL[1:0] Encoding** **BSEL[1:0] — System Bus Frequency** 00 — 66 MHz 01 — 100 MHz 10 — Reserved 11 — 133 MHz
CLKREF	Analog	The CLKREF (System Bus Clock Reference) signal provides a reference voltage to define the trip point for the BCLK signal. This signal should be connected to a resistor divider to generate 1.25V from the 2.5-V supply.
CMOSREF	Analog	The CMOSREF (CMOS Reference Voltage) signal provides a DC level reference voltage for the CMOS input buffers. A voltage divider should be used to divide a stable voltage plane (e.g., 2.5V or 3.3V). This signal must be provided with a DC voltage that meets the VCMOSREF specification from Table 13.
D[63:0]#	I/O GTL+	The D[63:0]# (Data) signals are the data signals. These signals provide a 64-bit data path between both system bus agents, and must be connected to the appropriate pins/balls on both agents. The data driver asserts DRDY# to indicate a valid data transfer.

Signal Name	I/O	Signal Description
DBSY#	I/O-GTL+	The DBSY# (Data Bus Busy) signal is asserted by the agent responsible for driving data on the system bus to indicate that the data bus is in use. The data bus is released after DBSY# is deasserted. This signal must be connected to the appropriate pins/balls on both agents on the system bus.
DEFER#	I GTL+	The DEFER# (Defer) signal is asserted by an agent to indicate that the transaction cannot be guaranteed in-order completion. Assertion of DEFER# is normally the responsibility of the addressed memory agent or I/O agent. This signal must be connected to the appropriate pins/balls on both agents on the system bus.
DEP[7:0]#	I/O GTL+	The DEP[7:0]# (Data Bus ECC Protection) signals provide optional ECC protection for the data bus. They are driven by the agent responsible for driving D[63:0]#, and must be connected to the appropriate pins/balls on both agents on the system bus if they are used. During power-on configuration, DEP[7:0]# signals can be enabled for ECC checking or disabled for no checking.
DRDY#	I/O GTL+	The DRDY# (Data Ready) signal is asserted by the data driver on each data transfer, indicating valid data on the data bus. In a multi-cycle data transfer, DRDY# can be deasserted to insert idle clocks. This signal must be connected to the appropriate pins/balls on both agents on the system bus.
EDGCTRLP	Analog	The EDGCTRLP (Edge Rate Control) signal is used to configure the edge rate of the GTL+ output buffers. Connect the signal to VSS with a 110-Ω, 1% resistor.
FERR#	O 1.5V Tolerant Open-drain)	The FERR# (Floating-point Error) signal is asserted when the processor detects an unmasked floating-point error. FERR# is similar to the ERROR# signal on the Intel 387 coprocessor, and it is included for compatibility with systems using DOS-type floating-point error reporting.
FLUSH#	I 1.5V Tolerant	When the FLUSH# (Flush) input signal is asserted, the processor writes back all internal cache lines in the Modified state and invalidates all internal cache lines. At the completion of a flush operation, the processor issues a Flush Acknowledge transaction. The processor stops caching any new data while the FLUSH# signal remains asserted. On the active-to-inactive transition of RESET#, each processor bus agent samples FLUSH# to determine its power-on configuration.

3.1 Pentium III/Celeron µPGA2 CPU

Alphabetical Signal Reference

Signal Name	I/O	Signal Description
GHI#	I 1.5V Tolerant	The GHI# signal controls which operating mode bus ratio is selected in a mobile Pentium III processor featuring Intel SpeedStep technology. On the processor featuring Intel SpeedStep technology, this signal is latched when BCLK restarts in Deep Sleep state and determines which of two bus ratios is selected for operation. This signal is ignored when the processor is not in the Deep Sleep state. This signal is a "Don't Care" on processors that do not feature Intel SpeedStep technology. This signal has an on-die pull-up to VccT and should be driven with an Open-drain driver with no external pull-up.
HIT#, HITM#	I/O GTL+	The HIT# (Snoop Hit) and HITM# (Hit Modified) signals convey transaction snoop operation results, and must be connected to the appropriate pins/balls on both agents on the system bus. Either bus agent can assert both HIT# and HITM# together to indicate that it requires a snoop stall, which can be continued by reasserting HIT# and HITM# together.
IERR#	O 1.5V Tolerant Open-drain	The IERR# (Internal Error) signal is asserted by the processor as the result of an internal error.Assertion of IERR# is usually accompanied by a SHUTDOWN transaction on the system bus. This transaction may optionally be converted to an external error signal (e.g., NMI) by system logic. The processor will keep IERR# asserted until it is handled in software or with the assertion of RESET#, BINIT, or INIT#.
IGNNE#	I 1.5V Tolerant	The IGNNE# (Ignore Numeric Error) signal is asserted to force the processor to ignore a numeric error and continue to execute non-control floating-point instructions. If IGNNE# is deasserted, the processor freezes on a non-control floating-point instruction if a previous instruction caused an error. IGNNE# has no affect when the NE bit in control register 0 (CR0) is set.
INIT#	I 1.5V Tolerant	The INIT# (Initialization) signal is asserted to reset integer registers inside the processor without affecting the internal (L1 or L2) caches or the floating-point registers. The processor begins execution at the power-on reset vector configured during power-on configuration. The processor continues to handle snoop requests during INIT# assertion. INIT# is an asynchronous input. If INIT# is sampled active on RESET#'s active-to-inactive transition, then the processor executes its built-in self test (BIST).

Signal Name	I/O	Signal Description
INTR	I 1.5V Tolerant	The INTR (Interrupt) signal indicates that an external interrupt has been generated. INTR becomes the LINT0 signal when the APIC is enabled. The interrupt is maskable using the IF bit in the EFLAGS register. If the IF bit is set, the processor vectors to the interrupt handler after completing the current instruction execution. Upon recognizing the interrupt request, the processor issues a single Interrupt Acknowledge (INTA) bus transaction. INTR must remain active until the INTA bus transaction to guarantee its recognition.
LINT[1:0]	I 1.5V Tolerant	The LINT[1:0] (Local APIC Interrupt) signals must be connected to the appropriate pins/balls of all APIC bus agents, including the processor and the system logic or I/O APIC component. When APIC is disabled, the LINT0 signal becomes INTR, a maskable interrupt request signal, and LINT1 becomes NMI, a non-maskable interrupt. INTR and NMI are backward compatible with the same signals for the Pentium processor. Both signals are asynchronous inputs. Both of these signals must be software configured by programming the APIC register space to be used either as NMI/INTR or LINT[1:0] in the BIOS. If the APIC is enabled at reset, then LINT[1:0] is the default configuration.
LOCK#	I/O GTL+	The LOCK# (Lock) signal indicates to the system that a sequence of transactions must occur atomically. This signal must be connected to the appropriate pins/balls on both agents on the system bus. For a locked sequence of transactions, LOCK# is asserted from the beginning of the first transaction through the end of the last transaction. When the priority agent asserts BPRI# to arbitrate for bus ownership, it waits until it observes LOCK# deasserted. This enables the processor to retain bus ownership throughout the bus locked operation and guarantee the atomicity of lock.
NMI	I 1.5V Tolerant	The NMI (Non-Maskable Interrupt) indicates that an external interrupt has been generated. NMI becomes the LINT1 signal when the APIC is disabled. Asserting NMI causes an interrupt with an internally supplied vector value of 2. An external interrupt-acknowledge transaction is not generated. If NMI is asserted during the execution of an NMI service routine, it remains pending and is recognized after the IRET is executed by the NMI service routine. At most, one assertion of NMI is held pending. NMI is rising edge sensitive.

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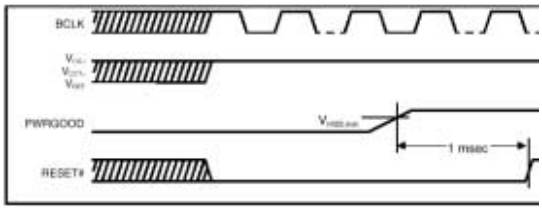
3.1 Pentium III/Celeron µPGA2 CPU

Alphabetical Signal Reference

Signal Name	I/O	Signal Description
PICCLK	I 2.5V Tolerant	The PICCLK (APIC Clock) signal is an input clock to the processor and system logic or I/O APIC that is required for operation of the processor, system logic, and I/O APIC components on the APIC bus.
PICD[1:0]	I/O 1.5V Tolerant Open-drain	The PICD[1:0] (APIC Data) signals are used for bi-directional serial message passing on the APIC bus. They must be connected to the appropriate pins/balls of all APIC bus agents, including the processor and the system logic or I/O APIC components. If the PICD0 signal is sampled low on the active-to-inactive transition of the RESET# signal, then the APIC is hardware disabled.
PLL1, PLL2	Analog	The PLL1 and PLL2 signals provide isolated analog decoupling is required for the internal PLL. See Section 3.2.2 for a description of the analog decoupling circuit.
PRDY#	O GTL+	The PRDY# (Probe Ready) signal is a processor output used by debug tools to determine processor debug readiness.
PREQ#	I 1.5V Tolerant	The PREQ# (Probe Request) signal is used by debug tools to request debug operation of the processor.
PWRGOOD	I 2.5V Tolerant	PWRGOOD (Power Good) is a 2.5-V tolerant input. The processor requires this signal to be a clean indication that clocks and the power supplies (Vcc, VccT, etc.) are stable and within their specifications. Clean implies that the signal will remain low, (capable of sinking leakage current) and without glitches, from the time that the power supplies are turned on, until they come within specification. The signal will then transition monotonically to a high (2.5V) state. Figure 26 illustrates the relationship of PWRGOOD to other system signals. PWRGOOD can be driven inactive at any time, but clocks and power must again be stable before the rising edge of PWRGOOD. It must also meet the minimum pulse width specified in Table 17 (Section 3.7) and be followed by a 1 ms RESET# pulse.

PWRGOOD Relationship at Power On



Signal Name	I/O	Signal Description
REQ[4:0]#	I/O GTL+	The REQ[4:0]# (Request Command) signals must be connected to the appropriate pins/balls on both agents on the system bus. They are asserted by the current bus owner when it drives A[35:3]# to define the currently active transaction type.
RESET#	I GTL+	Asserting the RESET# signal resets the processor to a known state and invalidates the L1 and L2 caches without writing back Modified (M state) lines. For a power-on type reset, RESET# must stay active for at least 1 msec after Vcc and BCLK have reached their proper DC and AC specifications and after PWRGOOD has been asserted. When observing active RESET#, all bus agents will deassert their outputs within two clocks. RESET# is the only GTL+ signal that does not have on-die GTL+ termination. A 56.2Ω1% terminating resistor connected to VccT is required. A number of bus signals are sampled at the active-to-inactive transition of RESET# for the power-on configuration. The configuration options are described in Section 4 and in the *Pentium II Processor Developer's Manual*. Unless its outputs are tri-stated during power-on configuration, after an active-to-inactive transition of RESET#, the processor optionally executes its built-in self-test (BIST) and begins program execution at reset-vector 000FFFF0H or FFFFFFF0H. RESET# must be connected to the appropriate pins/balls on both agents on the system bus.
RP#	I/O GTL+	The RP# (Request Parity) signal is driven by the request initiator and provides parity protection on ADS# and REQ[4:0]#. RP# should be connected to the appropriate pins/balls on both agents on the system bus. A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. This definition allows parity to be high when all covered signals are high.
RS[2:0]#	I GTL+	The RS[2:0]# (Response Status) signals are driven by the response agent (the agent responsible for completion of the current transaction) and must be connected to the appropriate pins/balls on both agents on the system bus.

3.1 Pentium III/Celeron µPGA2 CPU

PWRGOOD Relationship at Power On

Signal Name	I/O	Signal Description
RSP#	I GTL+	The RSP# (Response Parity) signal is driven by the response agent (the agent responsible for completion of the current transaction) during assertion of RS[2:0]#. RSP# provides parity protection for RS[2:0]#. RSP# should be connected to the appropriate pins/balls on both agents on the system bus. A correct parity signal is high if an even number of covered signals are low, and it is low if an odd number of covered signals are low. During Idle state of RS[2:0]# (RS[2:0]#=000), RSP# is also high since it is not driven by any agent guaranteeing correct parity.
RSVD	TBD	The RSVD (Reserved) signal is currently unimplemented but is reserved for future use. Leave this signal unconnected. Intel recommends that a routing channel for this signal be allocated.
RTTIMPEDP	Analog	The RTTIMPEDP (RTT Impedance/PMOS) signal is used to configure the on-die GTL+ termination. Connect the RTTIMPEDP signal to VSS with a 56.2-Ω, 1% resistor.
SLP#	I 1.5V Tolerant	The SLP# (Sleep) signal, when asserted in the Stop Grant state, causes the processor to enter the Sleep state. During the Sleep state, the processor stops providing internal clock signals to all units, leaving only the Phase-Locked Loop (PLL) still running. The processor will not recognize snoop and interrupts in the Sleep state. The processor will only recognize changes in the SLP#, STPCLK# and RESET# signals while in the Sleep state. If SLP# is deasserted, the processor exits Sleep state and returns to the Stop Grant state in which it restarts its internal clock to the bus and APIC processor units.
SMI#	I 1.5V Tolerant	The SMI# (System Management Interrupt) is asserted asynchronously by system logic. On accepting a System Management Interrupt, the processor saves the current state and enters System Management Mode (SMM). An SMI Acknowledge transaction is issued, and the processor begins program execution from the SMM handler.
STPCLK#	I 1.5V Tolerant	The STPCLK# (Stop Clock) signal, when asserted, causes the processor to enter a low-power Stop Grant state. The processor issues a Stop Grant Acknowledge special transaction and stops providing internal clock signals to all units except the bus and APIC units. The processor continues to snoop bus transactions and service interrupts while in the Stop Grant state. When STPCLK# is deasserted, the processor restarts its internal clock to all units and resumes execution. The assertion of STPCLK# has no affect on the bus clock.
TCK	I 1.5V Tolerant	The TCK (Test Clock) signal provides the clock input for the test bus (also known as the test access port).

Signal Name	I/O	Signal Description
TDI	I 1.5V Tolerant	The TDI (Test Data In) signal transfers serial test data to the processor. TDI provides the serial input needed for JTAG support.
TDO	O 1.5V Tolerant Open-drain	The TDO (Test Data Out) signal transfers serial test data from the processor. TDO provides the serial output needed for JTAG support.
TESTHI	I 1.5V Tolerant	The TESTHI (Test input High) is used during processor test and needs to be pulled high during normal operation.
TESTLO[2:1]	I 1.5V Tolerant	The TESTLO[2:1] (Test input Low) signals are used during processor test and needs to be pulled to ground during normal operation.
TESTP	Analog	The TESTP (Test Point) signals are connected to Vcc and Vss at opposite ends of the die. These signals can be used to monitor the Vcc level on the die. Route the TESTP signals to test points or leave them unconnected. Do not short the TESTP signals together.
THERMDA, THERMDC	Analog	The THERMDA (Thermal Diode Anode) and THERMDC (Thermal Diode Cathode) signals connect to the anode and cathode of the on-die thermal diode.
TMS	I 1.5V Tolerant	The TMS (Test Mode Select) signal is a JTAG support signal used by debug tools.
TRDY#	I GTL+	The TRDY# (Target Ready) signal is asserted by the target to indicate that the target is ready to receive write or implicit write-back data transfer. TRDY# must be connected to the appropriate pins/balls on both agents on the system bus.
TRST#	I 1.5V Tolerant	The TRST# (Test Reset) signal resets the Test Access Port (TAP) logic. The mobile Pentium III processors do not self-reset during power on; therefore, it is necessary to drive this signal low during power-on reset.

3.1 Pentium III/Celeron µPGA2 CPU

PWRGOOD Relationship at Power On

Signal Name	I/O	Signal Description
VID[4:0]	O - Open-drain	The VID[4:0] (Voltage ID) pins/balls can be used to support automatic selection of power supply voltages. These pins/balls are not signals, they are either an open circuit or a short to VSS on the processor substrate. The combination of opens and shorts encodes the voltage required by the processor. External to pull-ups are required to sense the encoded VID. For processors that have Intel SpeedStep technology enabled, VID[4:0] encode the voltage required in the battery-optimized mode. VID[4:0] are needed to cleanly support voltage specification changes on mobile Pentium III processors. The voltage encoded by VID[4:0] is defined in Table 39. A "1" in this table refers to an open pin/ball and a "0" refers to a short to VSS. The power supply must provide the requested voltage or disable itself. Please note that in order to implement VID on the BGA2 package, some VID[4:0] balls may be depopulated. For the BGA2 package, a "1" in Table 39 implies that the corresponding VID ball is depopulated, while a "0" implies that the corresponding VID ball is not depopulated. But on the Micro-PGA2 package, VID[4:0] pins are not depopulated.

3.2 Intel 82443MX Host Bridge Controller

SIGNAL DESCRIPTION

Host Interface Signal Description (1 of 3)

Signal	Type	Description
A20GATE	I	**Address 20 Gat**e. This input from the keyboard controller is logically combined with a bit in Port 92h which is then output via the A20M# signal. A20GATE saves the external OR gate needed with various other chipsets.
A20M#	OD	**Address 20 Mas**k. A20M# goes active by either setting the appropriate bit in the Port 92h Register, or by the A20GATE input signal.
ADS#	I/O	**Address Strob**e. The processor bus owner asserts ADS# to indicate the first of two cycles of a request phase.
BNR#	I/O	**Block Next Request**. Used to block the current request bus owner from issuing a new request. This signal is used to dynamically control the processor bus pipeline depth.
BPRI#	I/O	**Priority Agent Bus Request**. The 440MX is the only Priority Agent on the processor bus. The 440MX asserts this signal to obtain the ownership of the address bus. This signal has priority over symmetric bus requests and will cause the current symmetric owner to stop issuing new transactions unless the HLOCK# signal was asserted.
BREQ0#	I/O	**Symmetric Agent Bus Request**. BREQ0# is asserted during CPURST# to configure the symmetric bus agents and is negated two host clocks after CPURST# is negated.
CPURST#	I/O	**CPU Rese**t. The CPURST# pin is an output from the 440MX. The 440MX generates this signal based on the PCIRST# signal (generated internally from the South Bridge/Cluster) and the SUS_STAT# pin. CPURST# allows the processor to begin execution in a known state.
DBSY#	I/O	**Data Bus Bus**y. Used by the data bus owner to hold the data bus for transfers requiring more than one cycle.
DEFER#	I/O	**Defe**r. The 440MX generates a deferred response as defined by the 440MX's dynamic defer policy. The 440MX also uses the DEFER# signal to indicate a processor retry response.
DRDY#	I/O	**Data Read**y. Asserted for each cycle that data is transferred.
FERR#	I	**Numeric Coprocessor Erro**r. This signal is tied to the coprocessor error signal on the processor. If FERR# is asserted, the 440MX generates an internal IRQ13 to its interrupt controller unit. It is also used to gate the IGNNE# signal to ensure that IGNNE# is not asserted to the processor unless FERR# is active.
HA[31:3]#	I/O	**Address Bu**s. HA[31:3]# connects to the processor address bus. During processor cycles the HA[31:3]# are inputs. Note that the address bus is inverted on the processor bus.

Host Interface Signal Description (2 of 3)

Signal	Type	Description
HD[63:0]#	I/O	**Host Dat**a. These signals are connected to the processor data bus. Note that the data signals are inverted on the processor bus.
HIT#	I/O	**Hi**t. Indicates that a caching agent holds an unmodified version of the requested line. Also driven in conjunction with HITM# by the target to extend the snoop window.
HITM#	I/O	**Hit Modifie**d. Indicates that a caching agent holds a modified version of the equested line and that this agent assumes responsibility for providing the line. Also, driven in conjunction with HIT# to extend the snoop window.
HLOCK#	I/O	**Host Loc**k. All processor cycles sampled with the assertion of HLOCK# and ADS#, until the negation of HLOCK# must be atomic, i.e., no PCI snoopable access to DRAM is allowed when HLOCK# is asserted by the processor.
HREQ(4:0)#	I/O	**Request Comman**d. Asserted during both clocks of a request phase. In the first clock, the signals define the transaction type to a level of detail that is sufficient to begin a snoop request. In the second clock, the signals carry additional information to define the complete transaction type. The transactions supported by the 440MX Host Bridge are defined in Section 7.1.
HTRDY#	I/O	**Host Target Read**y. Indicates that the target of the processor transaction is ready to enter the data transfer phase.
IGNNE#	OD	**Ignore Numeric Erro**r. This signal is connected to the ignore error pin on the processor. IGNNE# is only used if the 440MX coprocessor error reporting function is enabled in the XBCSA Register (bit 5=1). If FERR# is active, indicating a coprocessor error, a write to the Coprocessor Error Register (F0h) causes the IGNNE# to be asserted. IGNNE# remains asserted until FERR# is negated. If FERR# is not asserted when the Coprocessor Error Register is written, the IGNNE# signal is not asserted.
INIT#	OD	**Initialization.** INIT# is asserted in response to any one of the following conditions: When the System Reset bit in the Reset Control Register is reset to 0 and the Reset CPU bit toggles from 0 to 1, the 440MX initiates a soft reset by asserting INIT#. * If a Shut Down Special cycle is decoded on the PCI Bus. * If the RCIN# signal is asserted. * If a write occurs to Port 92h, bit 0. When asserted, INIT# remains asserted for approximately 64 PCI clocks before being negated. **Mobile Celeron processor / Pentium II Processor:** **During Reset:** High **After Reset:** High **During POS:** High

3.2 Intel 82443MX Host Bridge Controller

Host Interface Signal Description (3 of 3)

Signal	Type	Description
INTR	OD	CPU Interrupt. INTR is driven by the 440MX to signal the CPU that an interrupt request is pending and needs to be serviced. It is asynchronous with respect to SYSCLK or PCICLK and is always an output. The interrupt controller must be programmed following PCIRST# to ensure that INTR is at a known state. **During Reset:** Low **After Reset:** Low **During POS:** Low
NMI	OD	**Non-Maskable Interrup**t. NMI is used to force a non-maskable interrupt to the processor. The 440MX can generate an NMI when either SERR# or IOCHK# is asserted. The processor detects an NMI on a rising edge. NMI is reset by setting the corresponding NMI source enable/disable bit in the NMI Status and Control Register.
RCIN#	I	**Keyboard Controller Reset processo**r. This pin from the keyboard controller saves the external OR gate needed. This is called RESET processor, because it uses the KBC terminology. However, the signal is mainly used to generate INIT#. RS(2:0)# I/O **Respons**e. Indicates type of response according to the following: RS[2:0] Response Type 000 Idle state 001 Retry response 010 Deferred response 011 Reserved (Not driven by the 440MX) 100 Hard failure (Not driven by the 440MX) 101 No data response 110 Implicit writeback 111 Normal data response
SMI#	OD	**System Management Interrup**t. SMI# is an active low output synchronous to PCICLK that is asserted by the 440MX in response to one of many enabled hardware or software events. **Not**e: The 440MX allows synchronous SMI events to generate SMI# even after STPCLK# has occurred.
STPCLK#	OD	**Stop Clock Request**. STPCLK# is an active low synchronous output synchronous to PCICLK that is asserted by the 440MX in response to one of many hardware or software events. When the processor samples STPCLK# asserted, it responds by stopping its internal clock.

Memory I/F Signal Description (1 of 1)

Signal	Type	Description
CKE(3:0)#	O	**Clock Enable (SDRAM**). Clock Enable is used to signal a self-refresh or power-down command to an SDRAM array when entering system Suspend. CKE is also used to dynamically power down inactive SDRAM rows.
CS(3:0)#	O	**Chip Select (SDRAM).** For memory rows configured with SDRAM these pins select the particular SDRAM components during the active state.
DQM(7:0)	O	**Input/Output Data Mask (SDRAM).** These pins act as synchronized output enables during read cycles and as a byte enables during write cycles. The read cycles require Tdqz clock latency before the functions are performed. In the case of write cycles, byte-masking functions are performed during the same clock when write data is driven (i.e., 0 clock latency).
MA(13,12#, 11#, 10, (9:0)#)	O	**Memory Address (SDRAM).** MA(13,12#:11#,10,(9:0)#) signals provide the multiplexed row and column address to DRAM. Each Memory address line has a programmable buffer strength to optimize for different signal loading conditions.
MD(63:0)	I/O	**Memory Data (SDRAM).** These signals interface to the DRAM data bus.
SCAS#	O	**SDRAM Column Address Strobe (SDRAM).** The SCAS# signal generates SDRAM commands encoded on SRAS#/SCAS#/WE# signals.
SRAS#	O	**SDRAM Row Address Strobe (SDRAM).** The SRAS# signal generates SDRAM commands encoded on SRAS#/SCAS#/WE# signals.
WE#	O	**Write Enable Signal (SDRAM).** WE# is asserted during writes to DRAM. The WE# lines have a programmable buffer strength that can be optimized for different signal loading conditions.

IDE Signal Description (1 of 2)

Signal	Type	Description
PDA[2:0]	O	**IDE Device Address**. These output signals are connected to the corresponding signals on the IDE connectors. They are used to indicate which byte in either the ATA command block or control block is being addressed.
PDCS1#	O	**IDE Device Chip Selects for 100 Rang**e. For ATA Command Register block. This output signal is connected to the corresponding signal on the IDE connector.
PDCS3#	O	**IDE Device Chip Select for 300 Rang**e. For ATA Control Register block. This output signal is connected to the corresponding signal on the IDE connector.

3.2 Intel 82443MX Host Bridge Controller

IDE Signal Description (2 of 2)

Signal	Type	Description
PDD[15:0]	I/O	**IDE Device Dat**a. These signals directly drive the corresponding signals on the IDE connector.
PDDAK#	O	**IDE Device DMA Acknowledg**e. This signal directly drives the DAK# signal on the IDE connectors. It is asserted by the 440MX to indicate to IDE DMA slave devices that a given data transfer cycle (assertion of PDIOR# or PDIOW#) is a DMA data transfer cycle. This signal is used in conjunction with the PCI bus master IDE function and is not associated with any AT-compatible DMA channel.
PDDRQ	I	**IDE Device DMA Request**. This input signal is directly driven from the DREQ signal on the IDE connector. It is asserted by the IDE device to request a data transfer. This signal is used in conjunction with the PCI bus master IDE function and is not associated with any AT-compatible DMA channel.
PDIOR# (PDWSTB / PRDMARDY#)	O	**Disk I/O Read (PIO and Non-Ultra33 DMA)**. This is the command to the IDE device that it may drive data onto the PDD lines. Data is latched by the 440MX on the de-assertion edge of PDIOR#. The IDE device is selected either by the ATA Register file chip selects (PDCS1#, PDCS3#) and the PDA lines, or the IDE DMA acknowledge (PDDAK#). Disk Write Strobe (Ultra33 DMA Writes to Disk). This is the data write strobe for writes to disk. When writing to disk, the 440MX drives valid data on rising and falling edges of PDWSTB. Disk DMA Ready (Ultra33 DMA Reads from Disk). This is the DMA ready for reads from disk. When reading from disk, the 440MX de-asserts PRDMARDY# to pause burst data transfers.
PDIOW# (PDSTOP)	O	**Disk I/O Write (PIO and Non-Ultra33 DMA)**. This is the command to the IDE device that it may latch data from the PDD lines. The IDE device latches data on the de-assertion edge of PDIOW#. The IDE device is selected either by the ATA Register file chip selects (PDCS1#, PDCS3#) and the PDA lines, or the IDE DMA acknowledge (PDDAK#). Disk Stop (Ultra33 DMA). The 440MX asserts this signal to terminate a burst.
PIORDY	I	**I/O Channel Ready (PIO)**. This signal keeps the strobe active (PDIOR# on reads, PDIOW# on writes) longer than the minimum width. It adds wait states to PIO transfers. Disk Read Strobe (Ultra33 DMA Reads from Disk). When reading from disk, the 440MX latches data on rising and falling edges of this signal. Disk DMA Ready (Ultra33 DMA Writes to Disk). When writing to disk, this signal is de-asserted by the disk to pause burst data transfers.

Other System/Test Signal Description

Signal	Type	Description
SPKR / GPIO(14)	O / I/O	**Speake**r. The SPKR signal is the output of counter 2 and is internally "ANDed" with Port 61h bit 1 to provide Speaker Data Enable. This signal drives an external speaker driver device. Upon PCIRST#, its output state is 0. This signal is muxed with GPIO(14). Refer to Section 4.2 for the pin count.
TEST#	I	Intel Reserved signal. This signal must be strapped to an external pull-up resistor.

PCI I/F Signal Description (1 of 3)

Signal	Type	Description
AD[31:0]	I/O	**PCI Address/Dat**a. AD[31:0] is a multiplexed address and data bus. During the first clock of a transaction, AD[31:0] contain a physical byte address (32 bits). During subsequent clocks, AD[31:0] contain data.
C/BE[3:0]#	I/O	**Bus Command and Byte Enable**s. The command and byte enable signals are multiplexed on the same PCI pins. During the address phase of a transaction, C/BE[3:0]# define the bus command. During the data phase C/BE[3:0]# are used as Byte Enables. C/BE[3:0]# Command Type 0 0 0 0 Interrupt Acknowledge 0 0 0 1 Special Cycle 0 0 1 0 I/O Read 0 0 1 1 I/O Write 0 1 1 0 Memory Read 0 1 1 1 Memory Write 1 0 1 0 Configuration Read 1 0 1 1 Configuration Write 1 1 0 0 Memory Read Multiple 1 1 1 0 Memory Read Line 1 1 1 1 Memory Write and Invalidate All command encodings not shown here are Reserved. The 440MX does not use reserved values, and does not respond if a PCI master generates a cycle using one of the reserved values.
CLKRUN#	I/OD	**PCI Clock Ru**n. CLKRUN# uses a protocol between the 440MX and various peripherals for dynamic starting and stopping of the PCI clock.
DEVSEL#	I/O	**Device Selec**t. The 440MX asserts DEVSEL# to claim a PCI transaction. As an output, the 440MX asserts DEVSEL# when it claims a PCI cycle. As an input, DEVSEL# indicates the response to a the 440MX-initiated transaction on the PCI bus. DEVSEL# is three-stated from the leading edge of PCIRST# and remains three-stated by the 440MX until driven as a target.

3.2 Intel 82443MX Host Bridge Controller

PCI I/F Signal Description (2 of 3)

Signal	Type	Description
FRAME#	I/O	**Cycle Fram**e. FRAME# is driven by the current Initiator to indicate the beginning and duration of an access. While FRAME# is asserted data transfers continue. When FRAME# is negated the transaction is in the final data phase. FRAME# is an input to the 440MX when it is the target. FRAME# is an output when the 440MX is the initiator and remains three-stated by the 440MX until driven as an initiator.
GNTA# / GPIO(3)	O / IO	**PC/PCI DMA Acknowledg**e. See Section 7.7 for a description. If the PC/PCI request is not needed, these can be used as general-purpose inputs.
IRDY#	I/O	**Initiator Read**y. IRDY# indicates the 440MX's ability, as an Initiator, to complete the current data phase of the transaction. It is used in conjunction with TRDY#. A data phase is completed on any clock when both IRDY# and TRDY# are sampled asserted. During a write, IRDY# indicates the 440MX has valid data present on AD[31:0]. During a read, it indicates the 440MX is prepared to latch data. IRDY# is an input to the 440MX when the 440MX is the Target and an output when the 440MX is an Initiator. IRDY# remains three-stated by the 440MX until driven as an initiator.
PAR	I/O	**Calculated Parit**y. PAR is "even" parity and is calculated on 36 bits — AD[31:0] plus C/BE[3:0]#. "Even" parity means that the number of "1"s within the 36 bits plus PAR is counted and the sum is always even. PAR is always calculated on 36 bits regardless of the valid byte enables. PAR is generated for address and data phases and is only guaranteed to be valid one PCI clock after the corresponding address or data phase. PAR is driven and three-stated identically to the AD[31:0] lines except that PAR is delayed by exactly one PCI clock. PAR is an output during the address phase (delayed one clock) for all 440MX-initiated transactions. It is also an output during the data phase (delayed one clock) when the 440MX is the Initiator of a PCI write transaction, and when it is the Target of a read transaction.
PCIRST#	O	**PCI Rese**t. The 440MX asserts PCIRST# to reset devices that reside on the PCI bus. The 440MX asserts PCIRST# during power-up and when a hard Reset sequence is initiated through the RC (CF9h) Register. PCIRST# is driven inactive a minimum of 1 ms after PWROK is driven active. PCIRST# is driven for a minimum of 1 ms when initiated through the RC Register. PCIRST# is asserted after PWROK is de-asserted in the STR state.
PGNT[3]# / GPIO(30) PGNT[2:0]#	I/O	**PCI Grant**s. 4 channels of bus master on the PCI bus. PGNT[3]# is multiplexed with GPIO.
PIRQ(A-B)#, PIRQ(C-D)# / GPIO(22:23)	I/OD	**PCI Interrupt Request**s. The PIRQx# signals can be routed to interrupts 3, 4, 5, 6, 7, 9, 10, 11, 12, 14 or 15 as described in Section 7.10.1.8. Each PIRQx# line has a separate Route Control Register. PIRQC# and PIRQD# are multiplexed with GPIO.

PCI I/F Signal Description (3 of 3)

Signal	Type	Description
PLOCK#	I/O	**PCI Loc**k. Indicates an exclusive bus operation and may require multiple transactions to complete. The 440MX asserts PLOCK# when it is doing non-exclusive transactions on PCI. PLOCK# is ignored when PCI masters are granted the bus.
PME# / GPIO(0)	I / I/O	**PCI Power Management Even**t. Driven by PCI peripherals to wake the system from low-power states S1-S5. Now included in the PCI specification.
PREQ[3]# / GPIO(29) PREQ[2:0]#	I/O	**PCI Request**s. 4 channels of bus master on the PCI bus.
REQA# / GPIO(2)	I	**PC/PCI DMA Reques**t. See Section 7.7 for a description. If the PC/PCI request is not needed, this signal can be used as a GPIO.
SERR#	I/OD	**System Erro**r. SERR# can be pulsed active by any PCI device that detects a system error condition. Upon sampling SERR# active, the 440MX can be programmed to generate an NMI, SMI#, or interrupt. Some internal conditions can also cause the 440MX to drive SERR# active.
STOP#	I/O	**Sto**p. STOP# indicates that the 440MX, as a Target, is requesting an initiator to stop the current transaction. As an Initiator, STOP# causes the 440MX to stop the current transaction. STOP# is an output when the 440MX is a Target and an input when the 440MX is an Initiator. STOP# is three-stated from the leading edge of PCIRST#. STOP# remains three-stated until driven by the 440MX as a slave.
TRDY#	I/O	**Target Read**y. TRDY# indicates the 440MX's ability to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#. A data phase is completed when both TRDY# and IRDY# are sampled asserted. During a read, TRDY# indicates that the 440MX, as a Target, has placed valid data on AD[31:0]. During a write, it indicates the 440MX, as a Target is prepared to latch data. TRDY# is an input to the 440MX when the 440MX is the Initiator and an output when the 440MX is a Target. TRDY# is three-stated from the leading edge of PCIRST#. TRDY# remains three-stated by the 440MX until driven as a target.

AC'97 Signal Description (1 of 2)

Signal	Type	Description
AC_BIT_CLK	I	**AC'97 Bit Cloc**k. 12.288 MHz serial data clock
AC_RST#	O	**AC'97 Rese**t. Master H/W Reset
AC_SDATA_IN(0)	I	**AC'97 Serial Data I**n. Serial TDM data input

3.2 Intel 82443MX Host Bridge Controller

AC'97 Signal Description (2 of 2)

Signal	Type	Description
AC_SDATA_IN(1)	I	**AC'97 Serial Data In**. Serial TDM data input
AC_SDATA_	O	**AC'97 Serial Data Out**. Serial TDM data output OUT
AC_SYNC	O	**AC'97 Sync**. 48 KHz fixed rate sample sync

Interrupt Signal Description

Signal	Type	Description
IRQ(14)	I	**Interrupt Request 14**. This interrupt input is connected to the IDE drive.
SERIRQ / GPIO(7)	I/OD	**Serial Interrupt Request**. This pin conveys the serial interrupt protocol. This signal is muxed with GPIO(7).

RTC Signal Description

Signal	Type	Description
RTCX1	Special	**32 KHz crystal**. Connected to the 32.768 KHz crystal. If no external crystal is used, then RTCX1 can be driven with the desired clock rate.
RTCX2	Special	**32 KHz crystal**. Connected to the 32.768 KHz crystal. If no external crystal is used, then RTCX2 should remain floating.

Clocks, Reset, PLLs and Miscellaneous Signal Description (1 of 2)

Signal	Type	Description
CLK48	I	**48 MHz Clock**. This signal runs the USB controller.
DCLK	I	**SDRAM Clock**. Feedback reference from the external zero-delay SDRAM clock buffer. The 440MX uses this clock when accessing an SDRAM array.
DCLKO	O	**SDRAM Clock Out**. 66 MHz SDRAM clock reference generated internally by the 440MX onboard PLL. It feeds an external buffer that produces multiple copies for the DIMMs.

Clocks, Reset, PLLs and Miscellaneous Signal Description (2 of 2)

Signal	Type	Description
HCLKIN	I	**Host Clock In**. This pin receives a buffered host clock. This clock is used by all of the 440MX's logic that resides is in the Host clock domain. This clock is used by an internal PLL to generate clock references for 66 MHz operations. During POS/STR HCLKIN must be low. This is the same or identical clock that goes to processor.
OSC	I	**Oscillator Clock**. Used for 8254 timers. Runs at 14.31818 MHz.
PCICLK	I	**PCI Clock**. This is a buffered PCI clock reference that is synchronously derived by an external clock synthesizer component from the host clock. This clock is used by all of the 440MX's logic that resides in the PCI clock domain. During POS/STR PCLKIN must be low.

USB Signal Description

Signal	Type	Description
OC[1:0]#	I	**Overcurrent Indicators**. These signals set corresponding bits in the USB controller to indicate that an overcurrent condition has occurred.
USBPRT[0]+, USBPRT[0]-	I/O	**Universal Serial Bus Port 0 Differential**. Bus Data/Address/Command Bus.
USBPRT[1]+, USBPRT[1]-	I/O	**Universal Serial Bus Port 1 Differential**. Bus Data/Address/Command Bus.

SMBus Signal Description

Signal	Type	Description
SMBCLK	I/OD	**SMBus Clock**. SMBus Clock Pin. External pull-up required.
SMBDATA	I/OD	**SMBus Data**. SMBus Data Pin. External pull-up required.

Power Management Signal Description (1 of 2)

Signal	Type	Description
BATLOW# / GPIO(11)	I / I/O	**Battery Low**. This signal is on the Resume plane. If the Battery Low function is not needed, then this signal is used as a general-purpose I/O pin.
CPUSTP#	O	**Stop CPU Clock**. This signal is an output to the external clock generator to turn off the processor and memory clocks. This is done prior to entering the C3 state, as well as the S1 and S2 states.

3.2 Intel 82443MX Host Bridge Controller

Power Management Signal Description (2 of 3)

Signal	Type	Description
EXSMI# / GPIO(24)	I / I/O	**External System Management Interrup**t. EXSMI# is a falling edge-triggered input to the 440MX indicating that an external device is requesting the system to enter SMM mode. When enabled, a falling edge on EXSMI# results in the assertion of SMI# to the processor. EXSMI# is an asynchronous input to the 440MX. However, when the setup and hold times are met it is only required to be asserted for one PCICLK. Once de-asserted it must remain de-asserted for at least four PCICLKs to allow the edge detect logic to PCIRST#. An external pullup should be placed on this signal if it is not used; otherwise it is not always guaranteed to be driven. EXSMI# can cause an SERR# (if enabled). This signal resides on the RESUME plane. If EXSMI# is not used, this signal can be used as a GPIO.
LID / GPIO(10)	I / I/O	**Li**d. Input from the lid button/switch. This signal can be used to generate wake events or interrupts. This signal is muxed with GPIO(10).
PCISTP#	O	**Stop PCI Cloc**k. This signal is an output to the external clock generator to turn off the PCI clock.
PWRBTN#	I	**Power Butto**n. This signal causes the SMI# or SCI to request that the system enter a Sleep state. If already in a Sleep state, it causes a wake event. If PWRBTN# is pressed for four seconds, it causes an unconditional transition (power button override) to the S5 state with only the PWRBTN# available as a wake event. An override occurs even if the system is in the S1-S4 states.
PWROK	I	**Power O**K. When asserted, PWROK is an indication to the 440MX that STR (Suspend-to-RAM) power plane and PCICLK has been stable for at least 1 ms. PWROK can be driven asynchronously. When PWROK is negated, the 440MX asserts PCIRST# and RSTDRV. It also resets the processor.
RI# / GPIO(12)	I / I/O	**Ring Indicat**e. When asserted, this signal indicates that a telephone ringing signal has been received by the modem and that the 440MX should wake up the system to accept data from the call. This signal is muxed with GPIO(12).
RSMRST#	I	**Resume Well Rese**t. Used for resetting the Resume well. If using a PS'98 power supply, then no external RC circuit is required. Otherwise, a 1 ms delay is needed.
SUS_STAT#	O	**Suspend Statu**s. This signal is asserted by the 440MX to indicate that the system will be entering a low-power state soon. It can be used by peripherals as an indication that they should isolate their outputs that may be going to powered-off planes.
SUSA#	O	**Power plane control.** Shuts off power to all non-critical systems when in the S1 (Power-On Suspend) or S2 (Power-On Suspend w/ full Reset) state. This signal goes low to turn off the power.

Power Management Signal Description (3 of 3)

Signal	Type	Description
SUSB#	O	**Power plane contro**l. Shuts off power to all non-critical systems when in the S3 (Suspend-to-RAM) state. This signal goes low to turn off the power.
SUSC#	O	**Power plane contro**l. Shuts power to all non-critical systems when in the S4 (Suspend-to-Disk) or S5 (Soft Off) states. This signal goes low to turn off the power.
SUSCLK	O	**Suspend Cloc**k. 32.768 KHz. This output signal from the Real Time Clock generator circuit is used as the Refresh clock for the 440MX. This signal is always running, except in the Suspend-to-Disk or Soft-Off states. During Reset: Running After Reset: Running During POS, STR: Running
THRM# / GPIO(8)	I / I/O	**Thermal Alar**m. Active low signal generated by external hardware to start the Hardware clock throttling mode. This signal can also generate an SMI# or an SCI. This signal is muxed with GPIO(8).

GPIO Signal Description

Signal	Default Type*	Description
GPIO[0,1,2,4,5, 6,7,8,9,10,11, 12,13,15,17,18, 20,21,22,23,24, 27,29,30]	Input	**General Purpose I/**O. Handled by system processor. Some of the 31 GPIO signals are muxed with other functions. (See Section 4.1.2 for the GPIO definition.) 3.3V only or 3.3/5V (3.3V drive with 5V tolerant). See Table 24 for details.
GPIO[3,14,16, 19,25,26,28]	Output	**General Purpose I/**O. Handled by system processor. Some of the 31 GPIO signals are muxed with other functions. (See Section 4.1.2 for the GPIO definition.) 3.3V only or 3.3/5V (3.3V drive with 5V tolerant). See Table 24 for details.

Note: *This table specifies the default direction of the pins selected as GPIOs (GPIO_DIR Register Dev #7, Function 3, Power Management I/O Space).

3.2 Intel 82443MX Host Bridge Controller

X-bus Signal Description (1 of 4)

Signal	Type	Description
BIOSCS#	O	**ROM BIOS Chip Selec**t. This chip select is driven active during read or write accesses to enabled BIOS memory ranges.
DACK(3)# / GPIO(28)	I/O	**DMA Acknowledg**e. The DACK output lines indicate that a request for DMA service has been granted by the 440MX. These lines should be used to decode the DMA slave device with the IOR# or IOW# line to indicate selection. Upon PCIRST#, these lines are set inactive (high). DACK3# is muxed with GPIO(28).
DACK(2:0)#	O	**DMA Acknowledg**e. The DACK output lines indicate that a request for DMA service has been granted by the 440MX. These lines should be used to decode the DMA slave device with the IOR# or IOW# line to indicate selection. Upon PCIRST#, these lines are set inactive (high).
DREQ(3) / GPIO(27)	I/O	**DMA Reques**t. The DREQ lines are used to request DMA service from the 440MX's DMA controller. All inactive to active edges of DREQ are assumed to be asynchronous. The request must remain active until the appropriate DACKx# signal is asserted. DREQ3 is muxed with GPIO(27).
DREQ(2:0)	I	**DMA Reques**t. The DREQ lines are used to request DMA service from the 440MX's DMA controller. All inactive to active edges of DREQ are assumed to be asynchronous. The request must remain active until the appropriate DACKx# signal is asserted.
IOCHRDY	I/O	**I/O Channel Read**y. Resources on the X-bus de-assert IOCHRDY to indicate that additional time (wait states) is required to complete the cycle. This signal is normally high on the X-bus.
IOR#	I/O	**I/O Rea**d. IOR# is the command to an X-bus I/O slave device that the slave may drive data on to the X-bus data bus (SD[15:0]). The I/O slave device must hold the data valid until after IOR# is negated. IOR# is driven high upon PCIRST#. During Reset: High-Z After Reset: High During POS: High
IOW#	I/O	**I/O Writ**e. IOW# is the command to an X-bus I/O slave device that the slave may latch data from the X-bus data bus (SD[7:0]). IOW# is driven high upon PCIRST#. During Reset: High-Z After Reset: High During POS: High
IRQ12 (Mouse IRQ)	I	**Interrupt Request 12/ Mouse Interrup**t. This pin provides a mouse interrupt function. Config Dev #7, offset 4e :bit 4 in the X-bus Chip Select Register determines the functionality of IRQ12. When bit 4=0, the standard interrupt function is provided and this pin can be tied to the X-bus connector. When bit

X-bus Signal Description (2 of 4)

Signal	Type	Description
		4=1, the mouse interrupt function is provided and this pin can be tied to the IRQ12 output of the keyboard controller. When the mouse interrupt function is selected, a low-to-high transition on this signal is latched by the 440MX and an INT is generated to the processor as IRQ12. An internal IRQ12 interrupt will continue to be generated until a Reset or an I/O read access to address 60h (falling edge of IOR#) is detected. After Reset, this pin provides the standard IRQ12 function (as an input).
IRQ8# / GPIO(6)	I / I/O	**IRQ8#** is always an active low edge-triggered interrupt input (i.e., this interrupt cannot be modified by software). Upon PCIRST#, IRQ8# is placed in active-low edge-sensitive mode. This signal is muxed with GPIO(6). During Reset: High-Z After Reset: High-Z During Power-down: High-Z
IRQ[3:7]	I	**Interrupt Requests [3:7**]. The IRQ signals provide both system board components and X-bus I/O devices with a mechanism for asynchronously interrupting the processor. The assertion mode of these inputs depends on the programming of the two ELCR Registers. When an ELCR bit is programmed to a 0, a low-to-high transition on the corresponding IRQ line is recognized as an interrupt request. This "edge-triggered" mode is the 440MX default. When an ELCR bit is programmed to a 1, a high level on the corresponding IRQ line is recognized as an interrupt request. This mode is "level-triggered" mode.
IRQ1 (KBC IRQ)	I	**Keyboard Interrup**t. This is the interrupt from the keyboard controller. An internal flip-flop is placed between the pin and the 8259 to be compatible with keyboard controllers which only pulse IRQ1 to signal an interrupt. A low-to-high transition on IRQ1 can be latched by the 440MX. Reads to port 60h clear the internal flip flop, at which time the flip-flop is armed for another low-to-high transition.
KBCCS# /	O / I/O	**Keyboard Chip Selec**t. KBCCS# is asserted during I/O Read or Write accesses
GPIO(26)		to KBC. This signal is muxed with GPIO(26).
MCCS# / GPIO(25)	O / I/O	**Microcontroller Chip Selec**t. Dedicated chip select for an external microcontroller. The I/O registers for the microcontroller are hard coded to I/O locations 62h and 66h. During Reset: High After Reset: High During POS: High This signal is muxed with GPIO(25).
MEMR#	I/O	**Memory Rea**d. MEMR# is the command to a memory slave that it may drive data onto the X-bus data bus. During Reset: High-Z After Reset: High During POS: High

3.2 Intel 82443MX Host Bridge Controller

X-bus Signal Description (3 of 4)

Signal	Type	Description
MEMW#	I/O	**Memory Writ**e. MEMW# is the command to a memory slave that it may latch data from the X-bus data bus. During Reset: High-Z After Reset: High During POS: High
PCS(1)# / GPIO(16) PCS(0)# / GPIO(19)	O / I/O	**Programmable Chip Select**s. This active low chip select is asserted for ISA I/O cycles that hit the range programmed into the Device Monitors[9,10] Function 3, PM I/O space. It is assumed that the peripheral selected via this pin resides on the X-bus. NOTE: PCS(1:0)# pins are included in the GPIO section (Section 4.1.2).
RSTDRV	O	**Reset Driv**e. The 440MX asserts RSTDRV to reset devices that reside on the X-bus. The 440MX asserts this signal during a hard Reset and during power-up. RSTDRV is asserted during power-up and de-asserted after PWROK is driven active. RSTDRV is also driven active for a minimum of 1 ms if a hard Reset has been programmed in the RC Register. During Reset: High After Reset: Low During POS: Low
SA[18:0]	I/O	**System Address Bu**s. These address lines define the selection with the granularity of one byte within the 512KB section of memory. For I/O accesses, only SA(15:0) are used. The 440MX always owns the X-bus during slave and legacy DMA cycles. SA[18:0] are at an unknown state upon PCIRST#. **DURING A DMA I/O CYCLE, THE ADDRESS BUS WILL BE DRIVEN TO 00H TO PREVENT OTHER I/O DEVICES FROM FALSELY DECODING THE CYCLE.** During Reset: High-Z After Reset: Undefined During POS: Last Address
SD[7:0]	I/O	**System Data Bu**s. SD[7:0] provide the 8-bit data path for devices residing on the X-bus. The 440MX three-states SD[7:0] during PCIRST#.
SYSCLK	O	**X-Bus System Cloc**k. SYSCLK is the reference clock for the X-bus. It drives the X-bus directly. The SYSCLK is generated by dividing PCICLK by four. During Reset: Running After Reset: Running During POS: Low NOTE: This clock is needed for external IR.

X-bus Signal Description (4 of 4)

Signal	Type	Description
TC	O	**Terminal Coun**t. The 440MX asserts TC to DMA slaves as a terminal count indicator. The 440MX asserts TC after a new address has been output, if the byte count expires with that transfer. When all the DMA channels are not in use, TC is negated (low). Upon PCIRST#, TC is inactive. During Reset: High After Reset: Low During POS: High
ZEROWS#	I	**Zero Wait State**s. An ISA slave asserts ZEROWS# after its address and command signals have been decoded to indicate that the current cycle can be shortened. A 16-bit ISA memory cycle can be reduced to two SYSCLKs. An 8-bit memory or I/O cycle can be reduced to three SYSCLKs. ZEROWS# has no effect during 16-bit I/O cycles. If IOCHRDY is negated and ZEROWS# is asserted during the same clock, then ZEROWS# is ignored and wait states are added as a function of IOCHRDY.

Notes:
1. X-bus signals are 5V tolerant.
2. Since the 440MX does not support the Secondary IDE Channel, IRQ15 is no longer available. However, SERIRQ and PCI interrupts can be steered to generate Interrupt 15 to the Interrupt controller.

POWER AND GROUND PINS

Core Power Pins

Name	Description
V CC	3.3V for Core. This power is shut off during some low-power states.
V SS	V SS Core.

Host I/F Power Pins

Name	Description
GTLREF	GTL+ Buffer Voltage Reference input for the mobile Celeron processor or Pentium II processor I/F.
VTT[B:A]	GTL+ termination voltage used for early clamps.

3.2 Intel 82443MX Host Bridge Controller

RTC Power Pins

Name	Description
V CCRTC	Power for RTC Well. 2.0V-3.3V. This power is not expected to be shut off unless the RTC battery is removed or drained, or unless an external RTC is used.

USB Power Pins

Name	Description
V CC USB	Power for USB Logic. 3.3V. This power will not be shut off in low-power states except for Mechanical Off.
V SS USB	Ground for USB.

Note: V CC SUS and V CC USB should both be on simultaneously.

Resume Power Pins

Name	Description
V CC SUS	3.3V for Resume Well. This power is not expected to be shut off unless the system is unplugged or the main battery is completely drained for a mobile system.

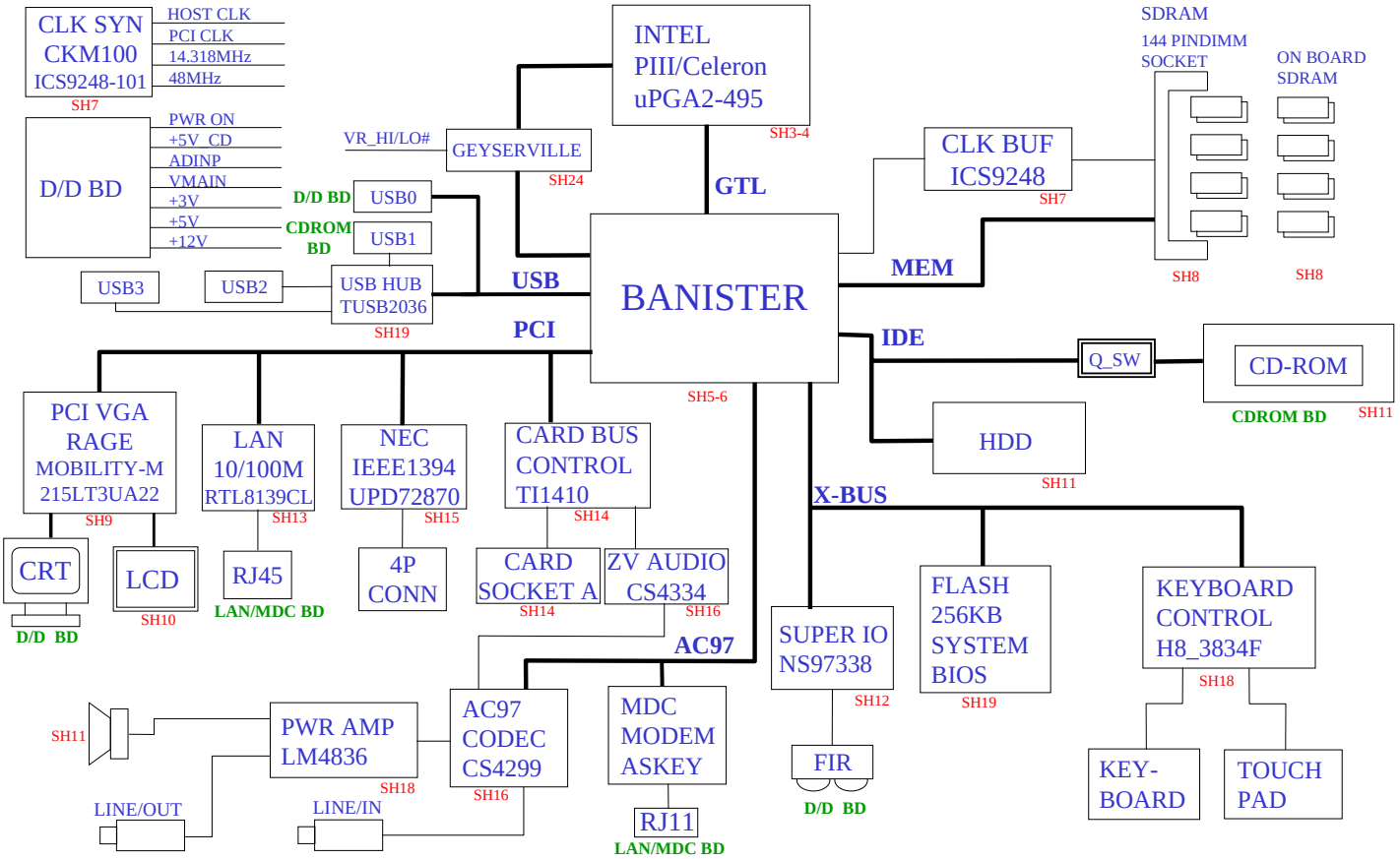
Note: V CC SUS and V CC USB should both be on simultaneously.

VREF Power Pins

Name	Description
REFV CC	Reference for 5V tolerance on inputs. This power is shut off in some low-power states.

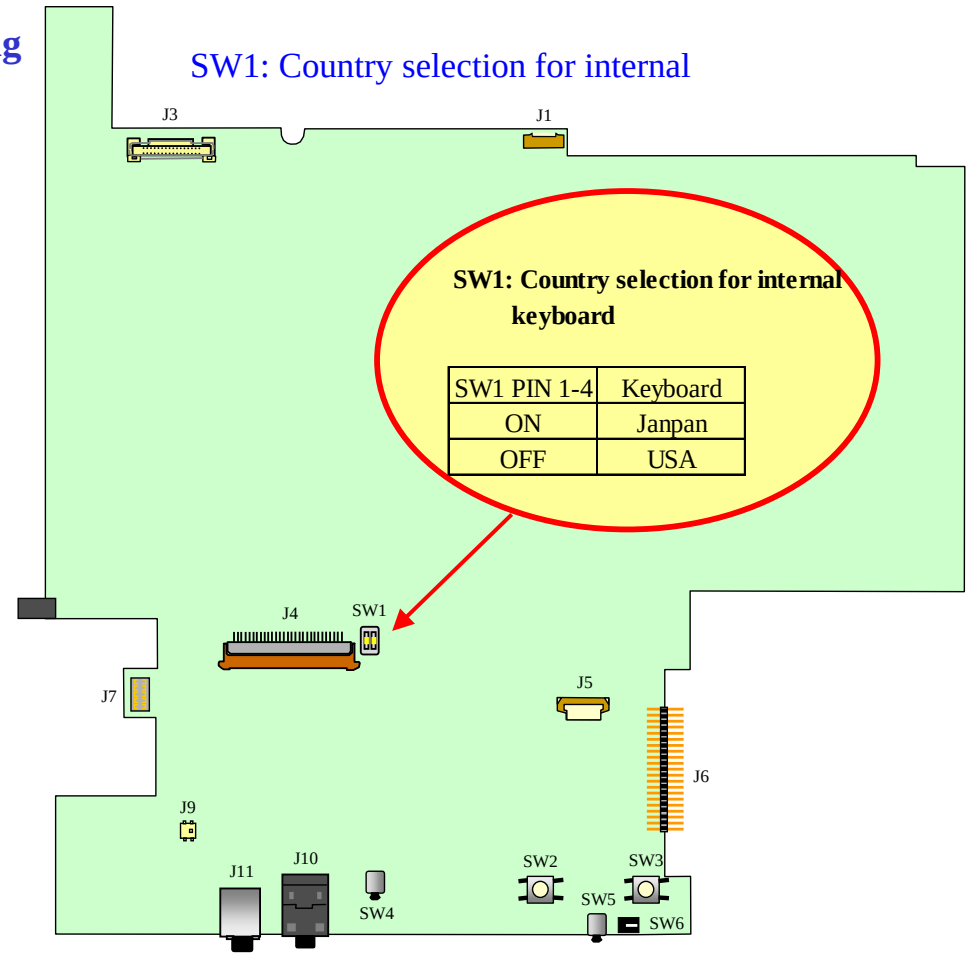
M722 N/B MAINTENANCE

4.M722 Block Diagram



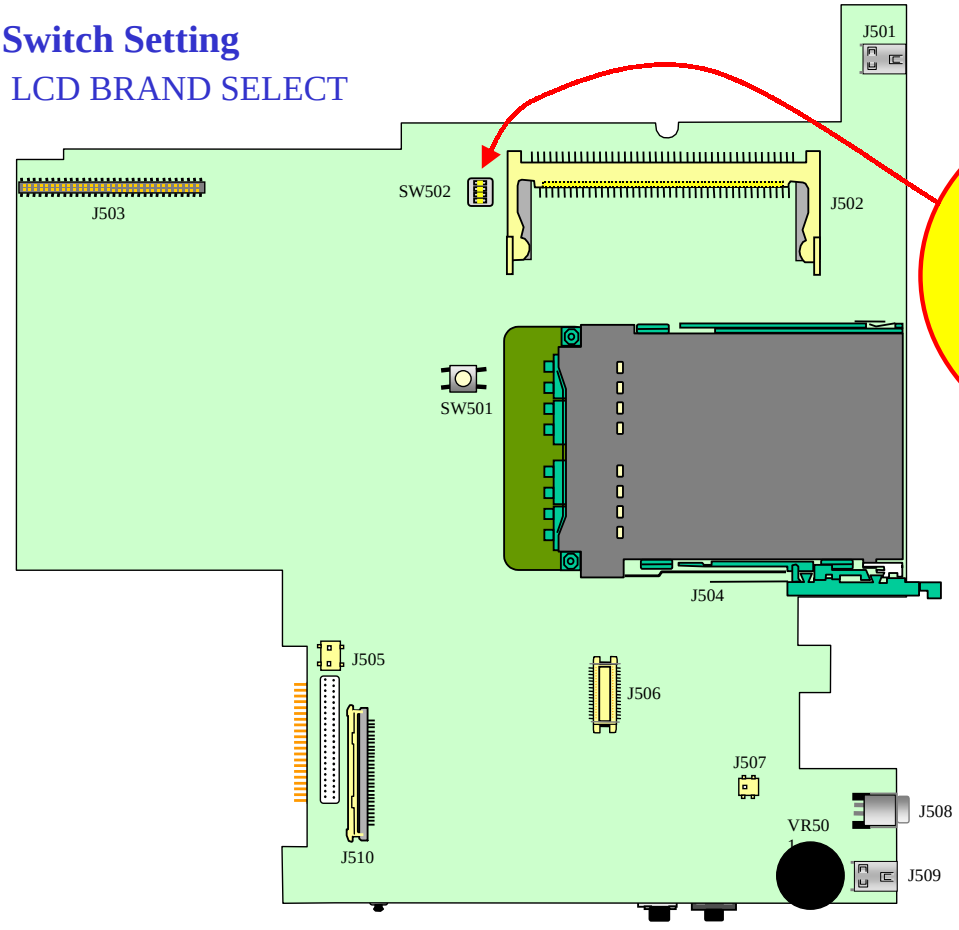
4. Switch Setting

SW1: Country selection for internal



4. Switch Setting

LCD BRAND SELECT

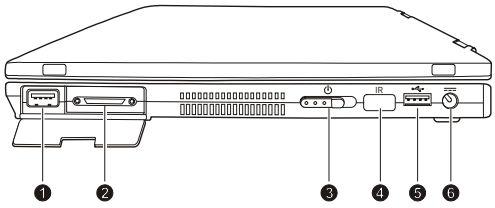


	SW1-8	SW2-7	SW3-6	SW4-5
HYUNDAI HT12X11-100	OFF	ON	ON	X
SAMSUNG LTN121X1-L01	ON	OFF	ON	X
HITACHI TX31D70VC1CAA	OFF	OFF	ON	X
SANYO TM121XG-02L02	ON	ON	OFF	X

5 System View and Disassembly

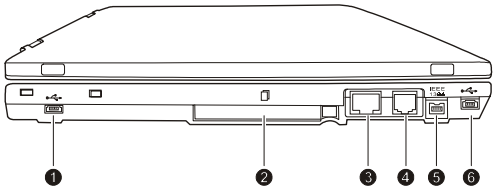
5.1 System View

5.1.1 Right-Side View



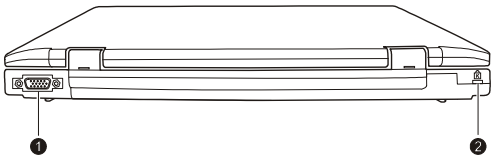
❶ USB Port
❷ CD/DVD-ROM Drive Port
❸ Power Switch
❹ IR Port
❺ USB Port
❻ Power Connector

5.1.2 Left-Side View



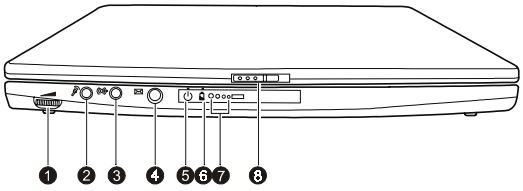
❶ Mini USB Port
❷ PC Card Slot
❸ RJ-45 connector
❹ RJ-11 connector
❺ IEEE 1394 Port
❻ Mini USB Port

5.1.3 Rear View



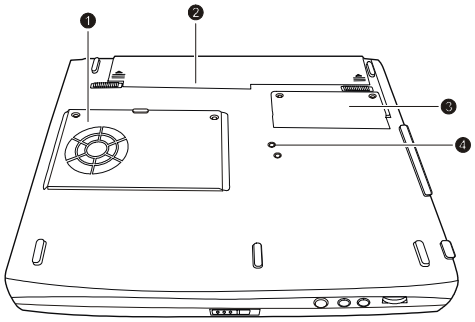
❶ VGA Port
❷ Kensington Lock

5.1.4 Front View



❶ Volume Control
❷ Microphone Connector
❸ Audio Output Connector
❹ Mail-Received Button/Indicator
❺ Power Indicator
❻ Battery Charge Indicator
❼ Battery Indicators
❽ Cover Latch

51.5 Bottom View

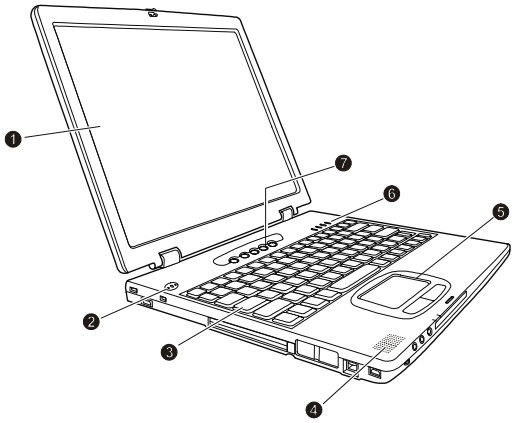


❶ CPU Cover
❷ Battery Pack
❸ RAM Board Slot Cover
❹ Reset Switch

5.1.6 Top-Open View

To open the cover, press the cover latch toward the right and lift the cover.

M722 N/B MAINTENANCE



❶ LCD Display
❷ Microphone
❸ Keyboard
❹ Stereo Speaker
❺ Touchpad
❻ Indicators Panel
❼ Easy Start Buttons

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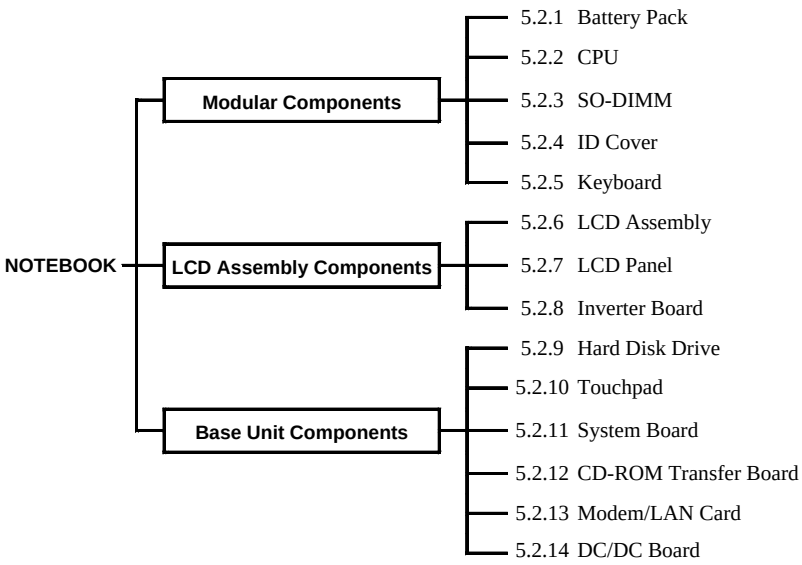
5.2 System Disassembly

This part discusses at length each major component for disassembly/reassembly and show corresponding illustrations. Use the chart below to determine the disassembly sequence for removing components from the notebook.

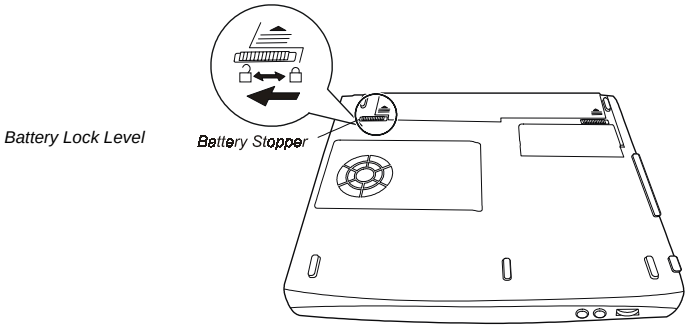
NOTE: *Before you start to install/replace these modules, disconnect all peripheral devices and make sure the notebook is not turned on or connected to AC power.*



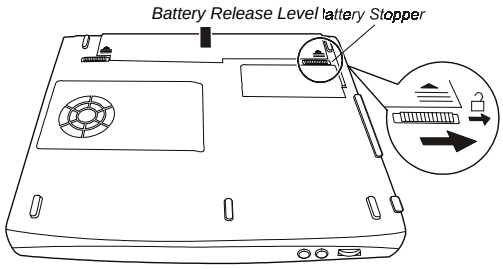
5.2.1 Battery Pack

Disassembly

1. Carefully put the notebook upside down.
2. Slide the battery lock level outward to the "unlock" ( ) position.



3. Slide the battery release level outward to the "unlock" ( ) position and hold it in the unlock position, and then you can remove the battery pack out of its compartment.



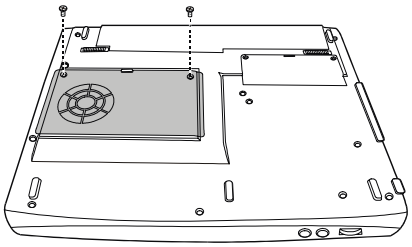
Reassembly

1. Fit the new battery pack into the compartment. The battery release level should click into the locked place.
2. Slide the battery lock inward to the "lock" ( ) position to secure the battery pack in place.

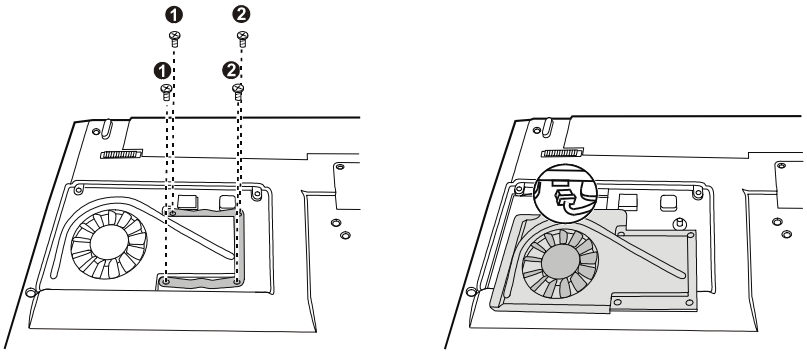
5.2.2 CPU

Disassembly

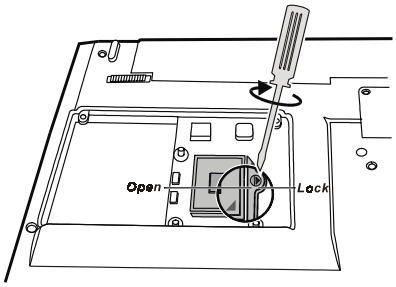
1. Carefully put the notebook upside down.
2. Remove two screws to lift the CPU compartment cover.



3. Remove four screws that locking the spring holder, then unplug the fan assembly's power cord to free the heatsink from the CPU module.



4. Use a flat screwdriver to rotate the screw on the socket from "L" (lock) position to "O" (open) position and then take out the CPU.



Reassembly

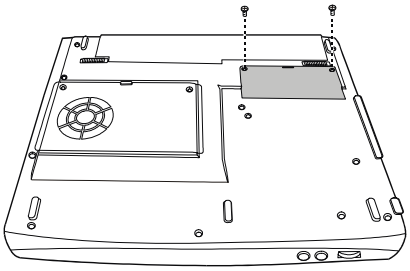
1. Align the arrowhead of the CPU with the arrowhead of the socket, and insert the CPU pins into the holes. Then, use a flat screwdriver to rotate the screw on the socket, from “O” position to “L” position, to lock the CPU.
2. Connect the power cord of the fan assembly to the system board, and fit the heatsink onto the top of the CPU.
3. Fit the spring holder to the heatsink and secure with four screws in this order: two center screws (❶) first and then two outer screws (❷).
4. Replace the CPU compartment cover and secure with two screws.

***NOTE**: When you remove the CPU heatsink, make sure the thermal pad is not damaged. If it is damaged, you have to replace the thermal pad with a new one.*

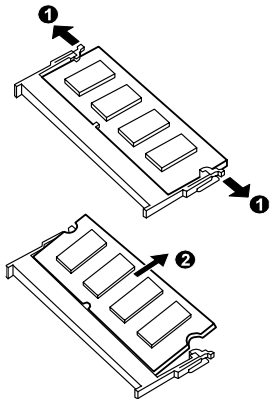
5.2.3 SO-DIMM

Disassembly

1. Carefully put the notebook upside down.
2. Remove two screws to lift the SO-DIMM compartment cover.



3. Pull the retaining clips outwards (❶) and remove the SO-DIMM (❷).



Reassembly

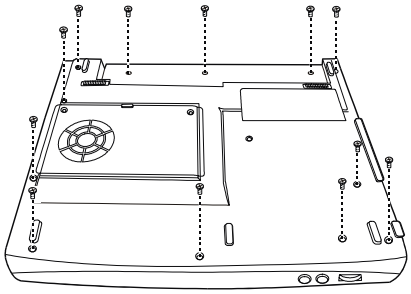
1. To install the SO-DIMM, match the SO-DIMM's notched part with the socket's projected part and firmly insert the SO-DIMM into the socket at 20-degree angle. Then push down until the retaining clips lock the SO-DIMM into position.
2. Replace the compartment cover and secure with two screws.

5.2.4 ID Cover

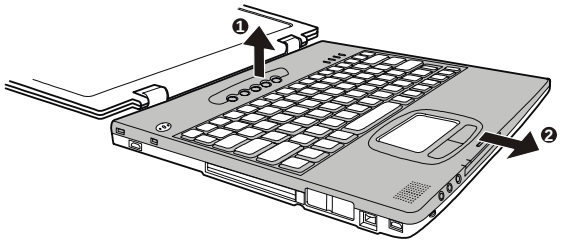
Disassembly

1. Remove the battery pack. (See section 5.2.1.)
2. Remove twelve bottom screws as shown below.

NOTE: *You don't have to remove five other screws that can be found on the bottom. To avoid mistakes, these holes are identified by a "dot" beside the screw hole.*



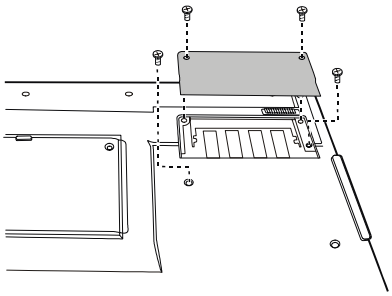
3. Put the notebook back to the upright position. Open the top cover and tilt it backward until it lies flat. To detach the ID cover, first slightly lift the upper edge (❶) and then slide it toward the front (❷).



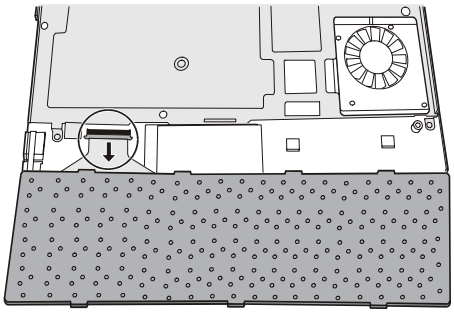
4. Disconnect the speaker cable from the system board.

5.2.5 Keyboard

1. Remove the battery pack. (See section 5.2.1.)
2. Remove the ID cover. (See section 5.2.4.)
3. Put the notebook upside down. Remove the SO-DIMM compartment cover and then two screws that secure the keyboard (one is in the compartment, the other one is in the central position of the bottom).



4. Put the notebook back to the upright position. Lift up the keyboard and disconnect the cable to free it from the system board.



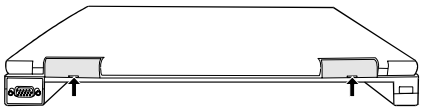
Reassembly

1. Plug the keyboard cable and fit the keyboard back into place.
2. Reconnect the speaker cable, then replace the ID cover and secure with all bottom screws.
3. Replace the battery pack.

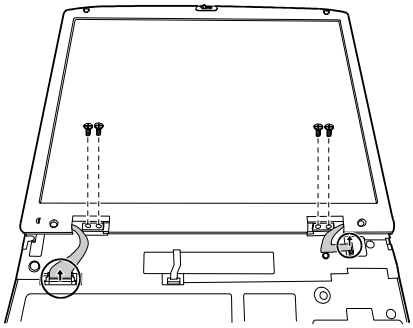
5.2.6 LCD Assembly

Disassembly.

1. Remove the battery pack. (See section 5.2.1.)
2. Remove the ID cover. (See section 5.2.4.)
3. Remove the hinge cover by inserting a flat screwdriver to the rear of the cover and pry the cover out.



4. Open the top cover. Unplug the two cable connectors coming from the LCD assembly, and remove four screws from the hinges. Now you can separate the LCD assembly from the base unit.



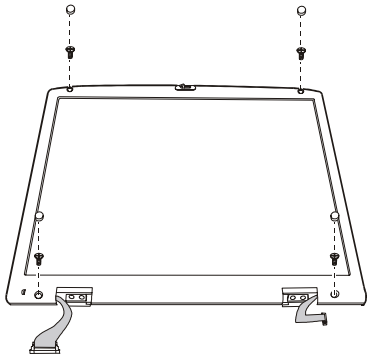
Reassembly

1. Attach the LCD assembly to the base unit and secure with four screws on the hinges.
2. Reconnect the LCD cable connectors to the system board.
3. Replace the two hinge covers.
4. Reconnect the speaker cable, then replace the ID cover and secure with all bottom screws.
5. Replace the battery pack.

5.2.7 LCD Panel

Disassembly

1. Remove the LCD assembly from the base unit. (See section 5.2.6.)
2. Remove the four rubber pads and the four screws underneath. Then you can separate the LCD frame from the housing.



3. To take out the LCD panel, remove four screws and unplug the cable from the inverter board.

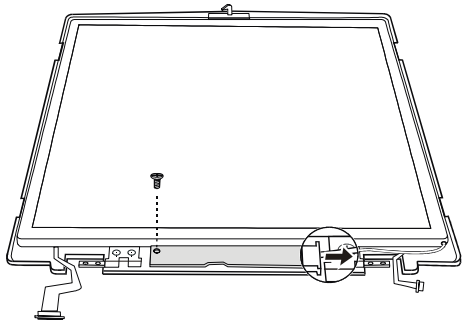
Reassembly

1. Reconnect the cable to the inverter board, then fit the LCD back into place and secure with four screws.
2. Fit the LCD frame back to the housing and secure with four screws.
3. Replace the LCD assembly.

5.2.8 Inverter Board

Disassembly

1. Detach the LCD frame. (See steps 1 to 2 in section 5.2.7 Disassembly.)
2. To take out the inverter board at the bottom side of the LCD, remove one screw and unplug the cable connected to the LCD panel.



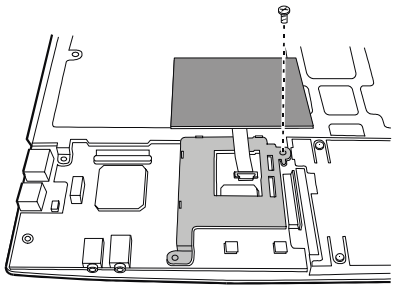
Reassembly

1. Reconnect the cable, then fit the inverter board back into place and secure with one screw.
2. Fit the LCD frame back to the housing and secure with four screws.

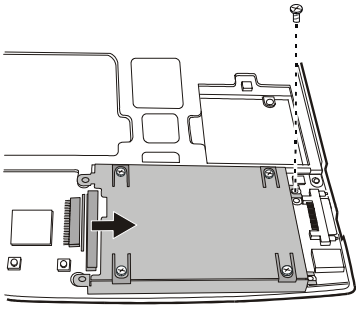
5.2.9 Hard Disk Drive

Disassembly

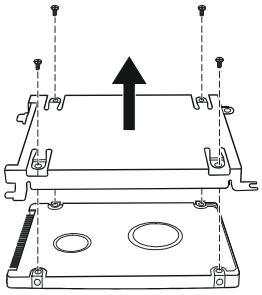
1. Remove the battery pack. (See section 5.2.1.)
2. Remove the ID cover. (See section 5.2.4.)
3. Lift up the touchpad board, then remove the screw at the upper right corner of the touchpad holder.



Remove the screw at the upper right corner of the hard disk, then slide the hard disk drive outward to unplug the connector and take out the hard disk drive.



5. Remove four screws to separate the hard disk drive from the metal shield.



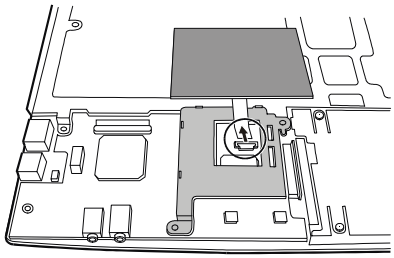
Reassembly

1. Attach the metal shield to the hard disk drive and secure with four screws.
2. Fit the hard disk drive into place, connect to the system board, and secure with one screw at the upper right corner.
3. Secure the screw at the upper right corner of the touchpad holder, then fit the touchpad board into place and secure with double-stick tape.
4. Reconnect the speaker cable, then replace the ID cover and secure with all bottom screws.
5. Replace the battery pack.

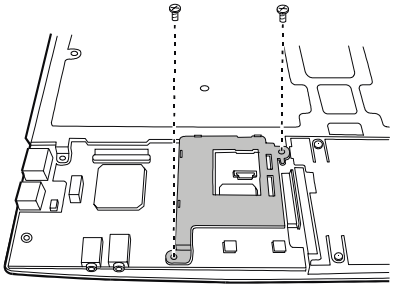
5.2.10 Touchpad

Disassembly

1. Remove the battery pack. (See section 5.2.1.)
2. Remove the ID cover. (See section 5.2.4.)
3. Lift up the touchpad board, and disconnect the cable from the system board.



4. If you need to remove the touchpad holder, remove two screws.



Reassembly

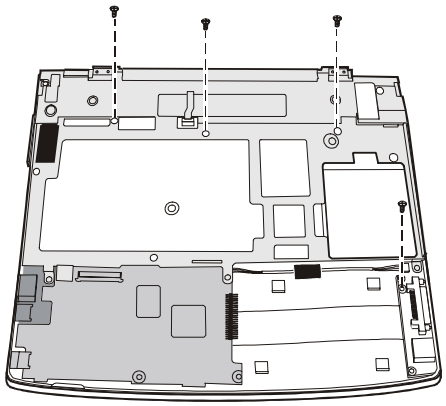
1. Replace the touchpad holder and secure with two screws.
2. Connect the cable of touchpad board to the system board, and fit the touchpad board into place and secure with double-stick tape.
3. Reconnect the speaker cable, then replace the ID cover and secure with all bottom screws.
4. Replace the battery pack.

5.2.11 System Board

Disassembly

1. Remove the battery pack. (See section 5.2.1.)
2. Remove the heatsink. (See steps 1 to 3 in section 5.2.2 Disassembly.)
3. Remove the ID cover. (See section 5.2.4.)
4. Remove the keyboard. (See section 5.2.5.)
5. Remove the LCD assembly. (See section 5.2.6.)
6. Remove the hard disk drive. (See section 5.2.7.)
7. Remove the touchpad. (See section 5.2.8.)

8. Remove three screws locking the system board and one screw locking the CD-ROM transfer board.



9. Lift the system board free.

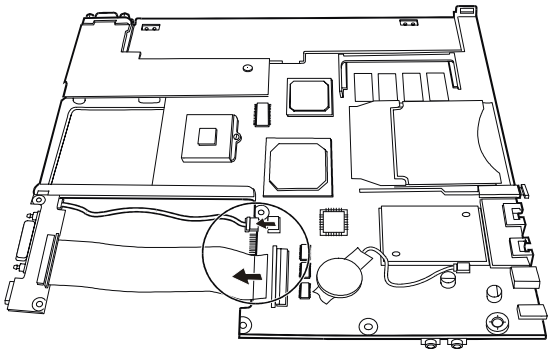
Reassembly

1. Fit the system board and CD-ROM transfer board into place and secure with four screws.
2. Replace the touchpad and the hard disk drive.
3. Attach the LCD assembly to the base unit and secure with four screws. Replace the two hinge covers.
4. Plug the keyboard cable and fit the keyboard back into place.
5. Replace the heatsink.
6. Reconnect the speaker cable, then replace the ID cover and secure with all bottom screws.
7. Replace the battery pack.

5.2.12 CD-ROM Transfer Board

Disassembly

1. Remove the system board and CD-ROM transfer board from the base. (See section 5.2.11.)
2. Put the system board upside down.
3. Unplug the cables from the system board.



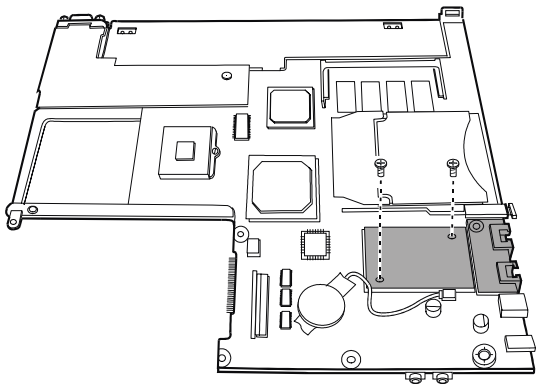
Reassembly

1. Reconnect the cables to the system board, then fit the system board and CD-ROM transfer board into place and secure with four screws.
2. Replace the system board. (See section 5.2.11 Reassembly.)

5.2.13 Modem/LAN Card

Disassembly

1. Remove the system board from the base. (See section 5.2.11.)
2. Put the system board upside down.
3. Remove two screws to lift the Modem/LAN card.



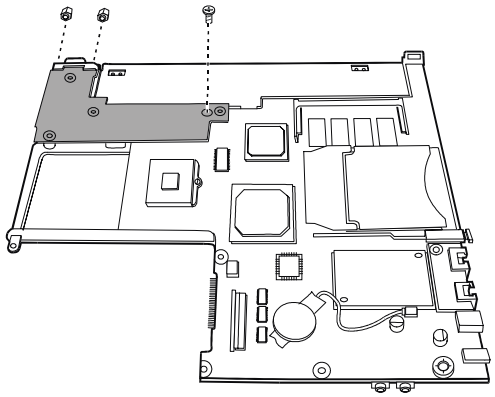
Reassembly

1. Insert the connector of the Modem/LAN card into the headers on the system board, and secure it with two screws.
2. Replace the system board. (See section 5.2.11 Reassembly.)

5.2.14 DC/DC Board

Disassembly

1. Remove the system board from the base. (See section 5.2.11.)
2. Put the system board upside down.
3. Remove one screw on the board, and two hexnut screws fastening the VGA port.
4. Lift the DC/DC board.



Reassembly

1. Insert the connector of the DC/DC board into the header on the system board, and secure it with three screws.
2. Replace the system board. (See section 5.2.11 Reassembly.)

M722 N/B MAINTENANCE

5.A Maintenance Diagnostics

5.A.1 Introduction

Each time the computer is turned on, the system bios runs a series of internal checks on the hardware. This power-on self test (post) allows the computer to detect problems as early as the power-on stage. Error messages of post can alert you to the problems of your computer.

If an error is detected during these tests, you will see an error message displayed on the screen. If the error occurs before the display is initialized,then the screen cannot display the error message. Error codes or system beeps are used to identify a post error that occurs when the screen is not available.

The value for the diagnostic port (3F8H) is written at the beginning of the test. Therefore, if the test failed, the user can determine where the problem occurred by reading the last value written to port 3F8H by the M722 debug board plug at CD-ROM CONNECTOR.

M722 N/B MAINTENANCE

5.A Maintenance Diagnostics

5.A.2 Error Codes : Following is a list of error codes in sequent display on the m722 Debug board.

SYSTEM SOFT BIOS:

CODE	DESCRIPTION
01h	Start of boot loader sequence.
02h	Initialize chipset.
03h	Memory Sizing.
04h	Perform conventional RAM(1st 640K) test with crossed-pattern R/W
05h	Move boot loader to the RAM.
06h	Start point of execution of boot loader in RAM.
07h	Shadow system BIOS.
08h	Initialize clock synthesizer
09h	Initialize audio controller.
0Ah	Detect internal ISA MODEM
0Bh	Proceed with normal boot
0Ch	Proceed with crisis boot
0Fh	DRAM sizing
10h	Initial L1,L2 cache, make stack and diagnose CMOS.
11h	Turn off fast A20 for post. Reset GDT's, 8259s quickly.
12h	Signal power on reset at COMS.
13h	Initialize the chipset, (SDRAM).
14h	Search for ISA bus VGA adapter
15h	Reset counter/timer 1, exite the RAM.
16h	User register config through CMOS
18h	Dispatch to 1st 64K RAM test
19h	Checksum the ROM
1Ah	Reset PIC's(8259s)
1Bh	Initialize video adapter(s)
1Ch	Initialize video (6845 regs)

CODE	DESCRIPTION
1Dh	Initialize color adapter
1Eh	Initialize monochrome adapter
1Fh	Test 8237A page registers
20h	Perform keyboard self test
21h	Test & initialize keyboard controller
22h	Check if CMOS RAM valid
23h	Test battery fail & CMOS X-SUM
24h	Test the DMA controllers
25h	Initialize 8237A controller
26h	Initialize interrupt vectors table.
27h	RAM quick sizing
28h	Protected mode entered safely
29h	RAM test completed
2Ah	Protected mode exit successful
2Bh	Setup shadow
2Ch	Prepare to initialize video
2Dh	Search for monochrome adapter
2Eh	Search for color adapter, VGA initialize.
2Fh	Signon messages displayed
30h	Special init of keyboard ctlr
31h	Test if keyboard present
32h	Test keyboard interrupt
33h	Test keyboard command Byte
34h	Test, blank and count all RAM
35h	Protected mode entered safely (2).
36h	RAM test complete

5.A. Maintenance Diagnostics

5.A.2 Error Codes : Following is a list of error codes in sequent display on the PIO debug board. SYSTEM SOFT BIOS:

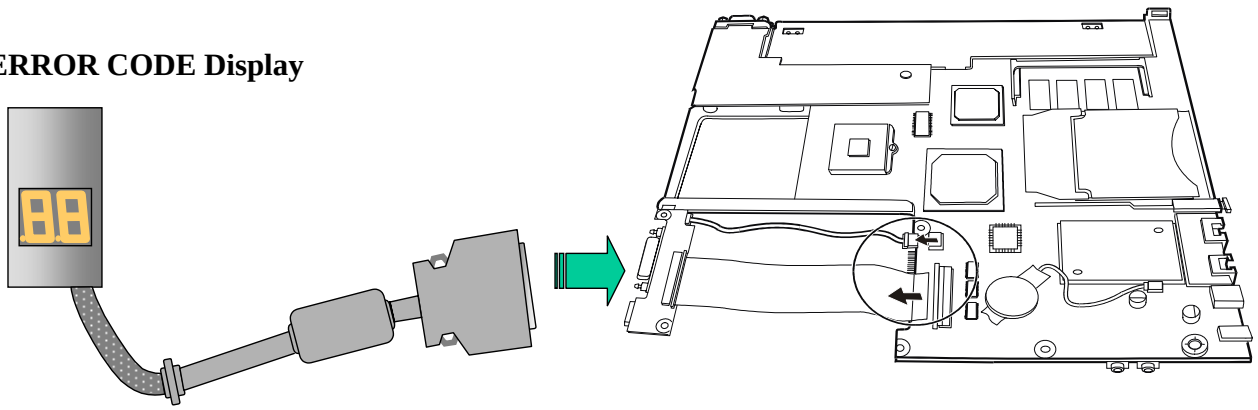
CODE	DESCRIPTION
37h	Protected mode exit successful
38h	Update keyboard output port to disable gate of A20
39h	Setup cache controller
3Ah	Test if 18.2Hz periodic working
3Bh	Initialize BIOS data area at 40:0.
3Ch	Initialize the hardware interrupt vector tabl
3Dh	Search and init the Mouse
3Eh	Update num lock status
3Fh	OEM initialization of COMM and LPT ports
40h	Configure the COMM and LPT ports
41h	Initialize the floppies
42h	Initialize the hard disk
43h	OEM's init of PM with USB
44h	Initialize additional ROMs
45h	Update NUMLOCK status
46h	Test for coprocessor installed
47h	OEM's init of power management, (check SMI)
48h	OEM functions before boot (PCMCIA, CardBus)
49h	Dispatch to operation system boot
4Ah	Jump into bootstrap code

M722 N/B MAINTENANCE

5.A. Maintenance Diagnostics

5.A.3. M722 Debug B'D

ERROR CODE Display



M722 DEBUG B'D

M722 Motherboard

Note:The M722 Debug B'D provide by Mitac/Tssc If need please contact us .

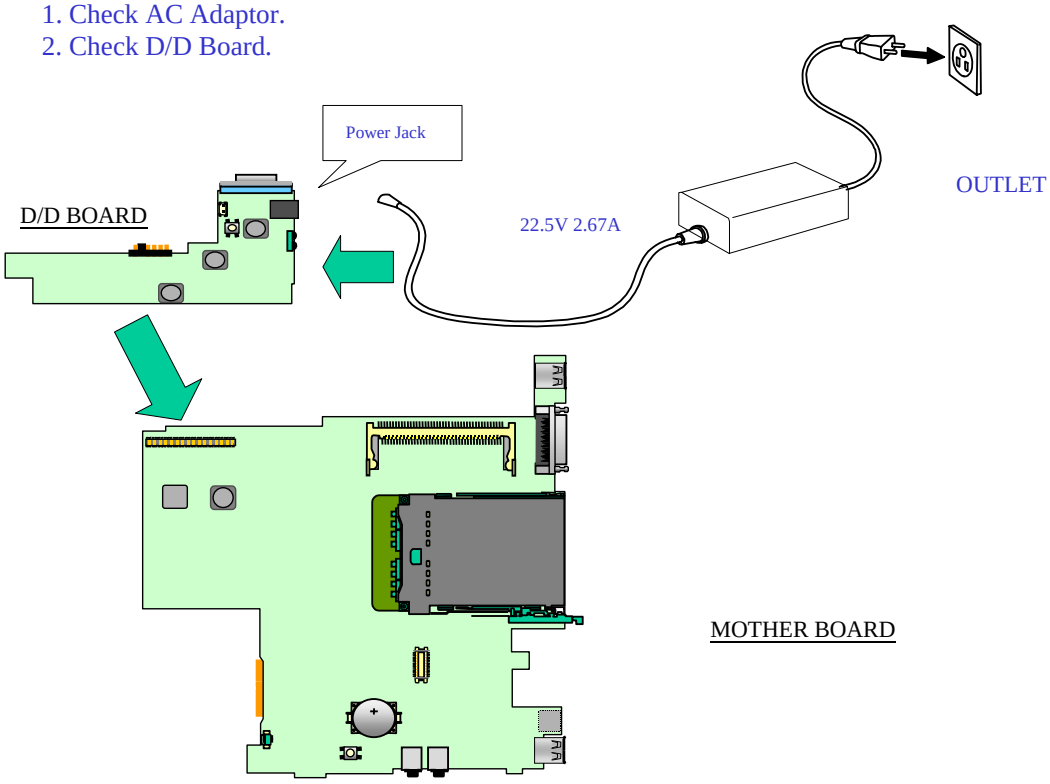
6. TROUBLE SHOOTING

M722 N/B MAINTENANCE

6.1 NO POWER:

When the power button is pressed, nothing happens ,power indicator does not light up.

1. Check AC Adaptor.
2. Check D/D Board.

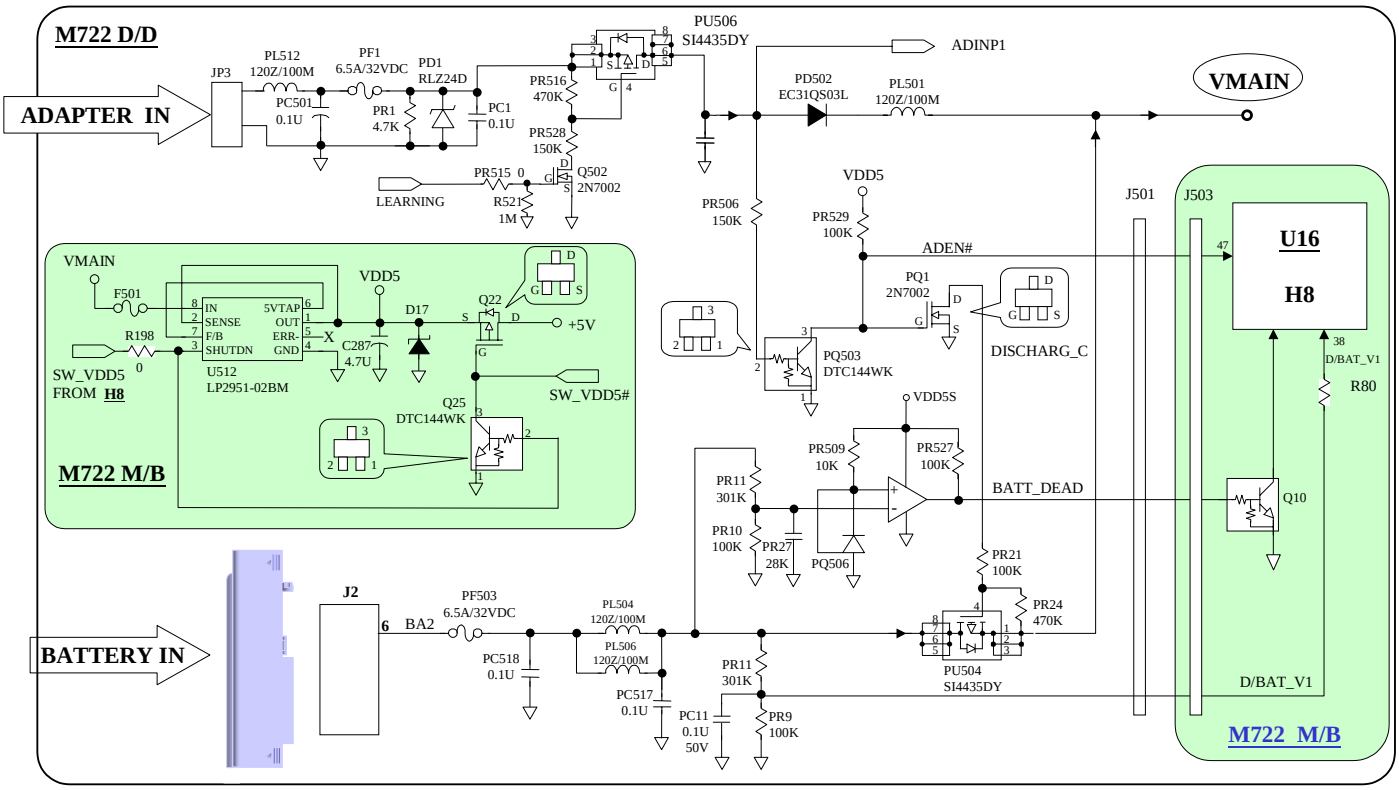


M722 N/B MAINTENANCE

6.1 NO POWER:

Symptom:

When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.

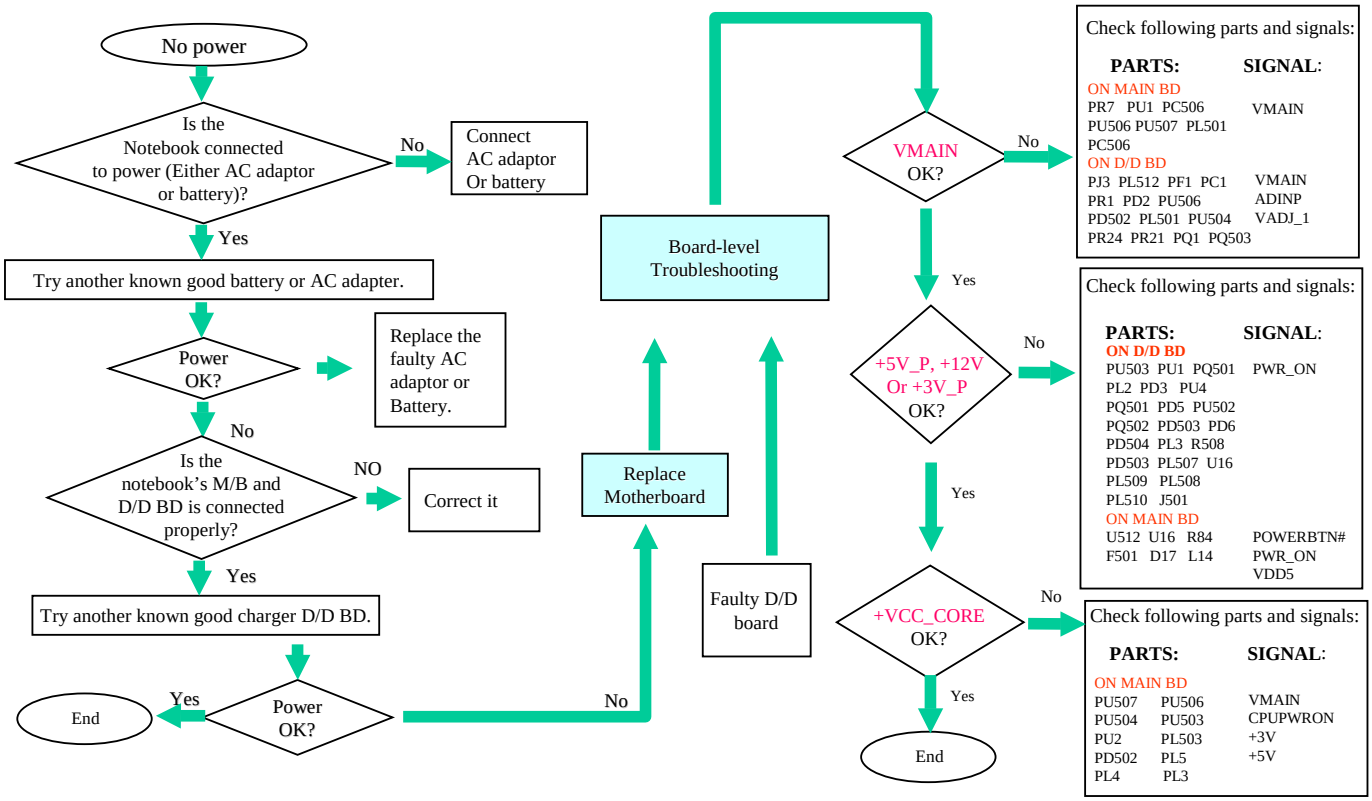


M722 N/B MAINTENANCE

6.1 NO POWER:

Symptom:

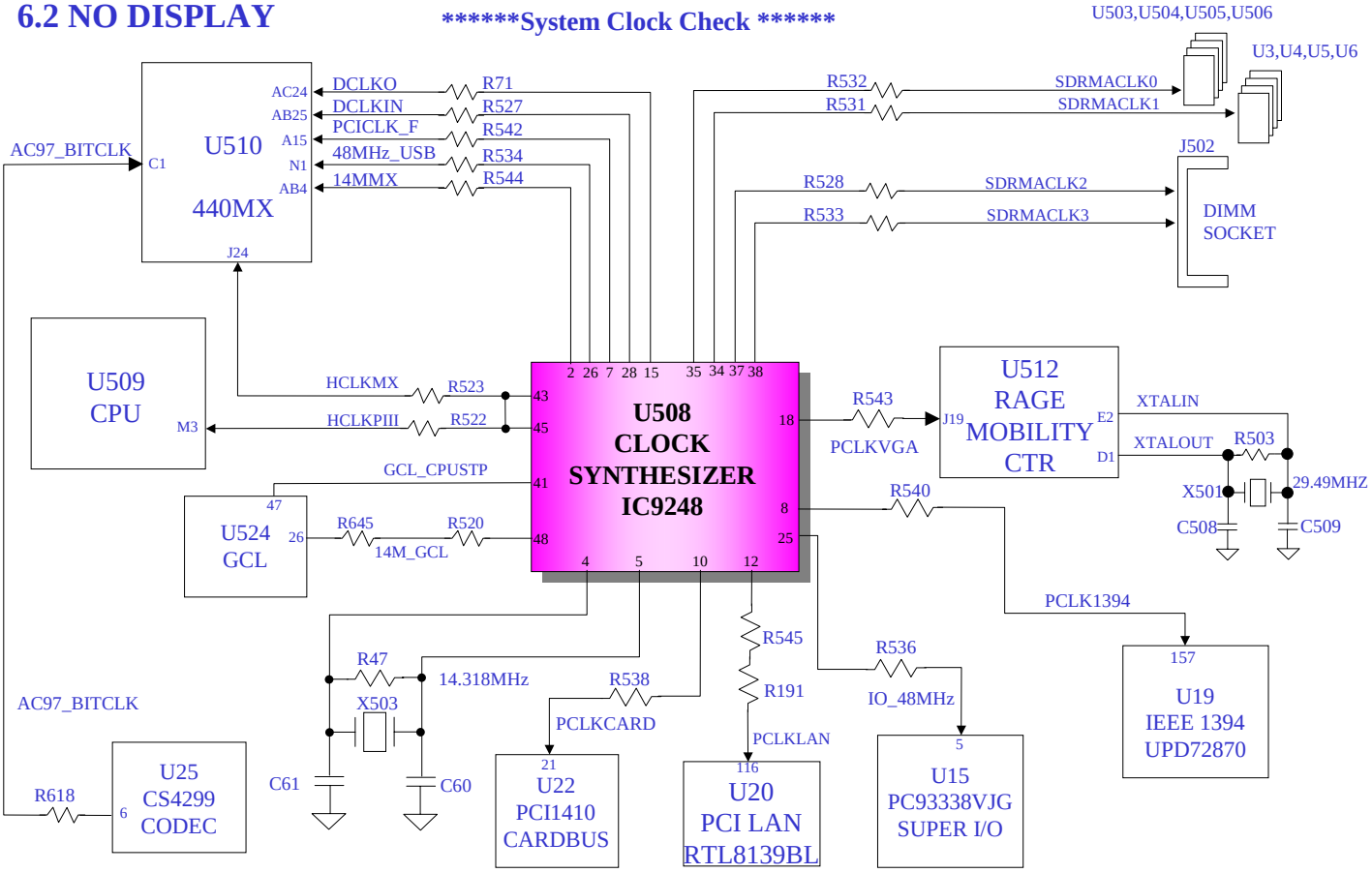
When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.



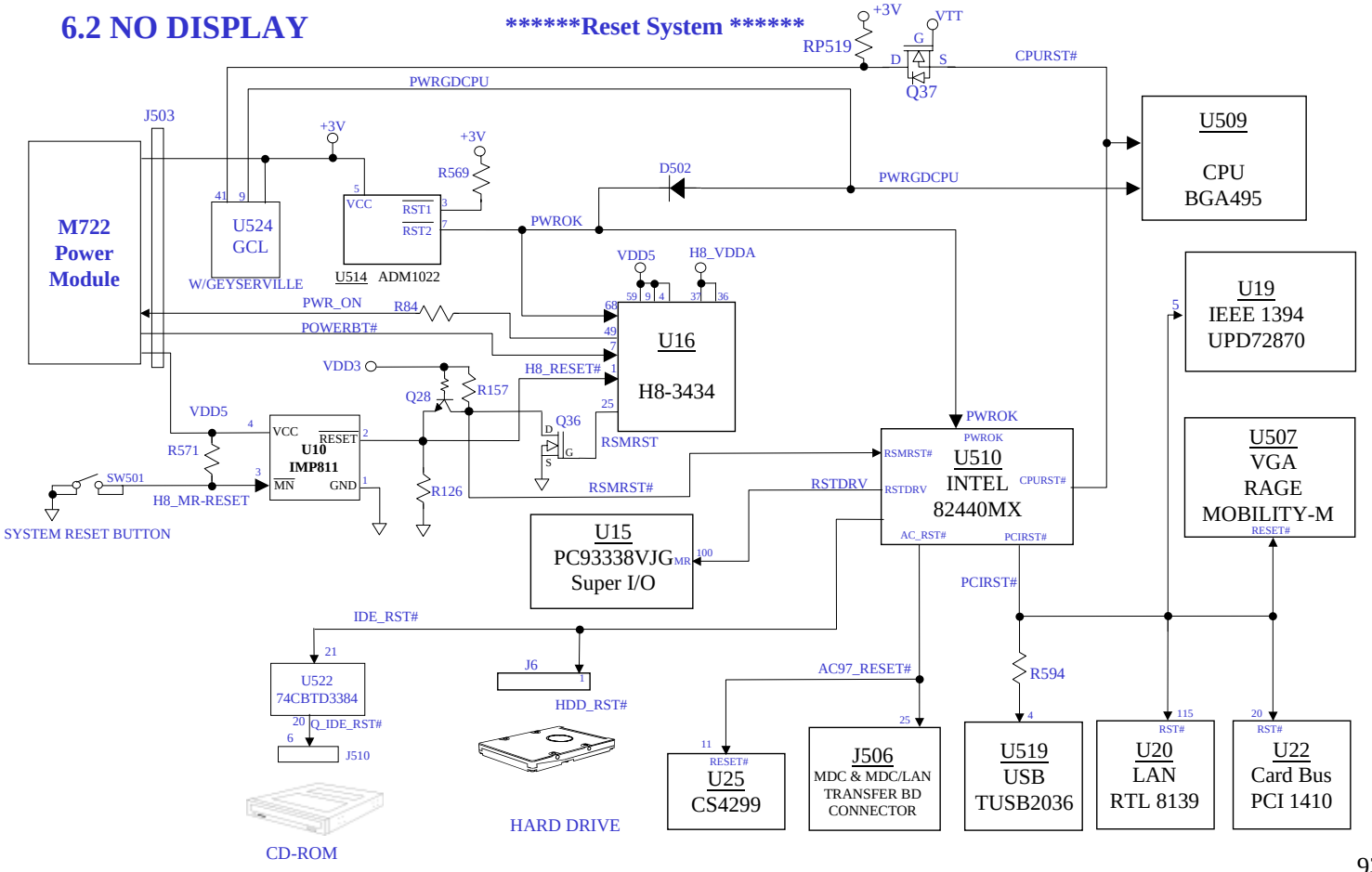
M722 N/B MAINTENANCE

6.2 NO DISPLAY

********System Clock Check ********

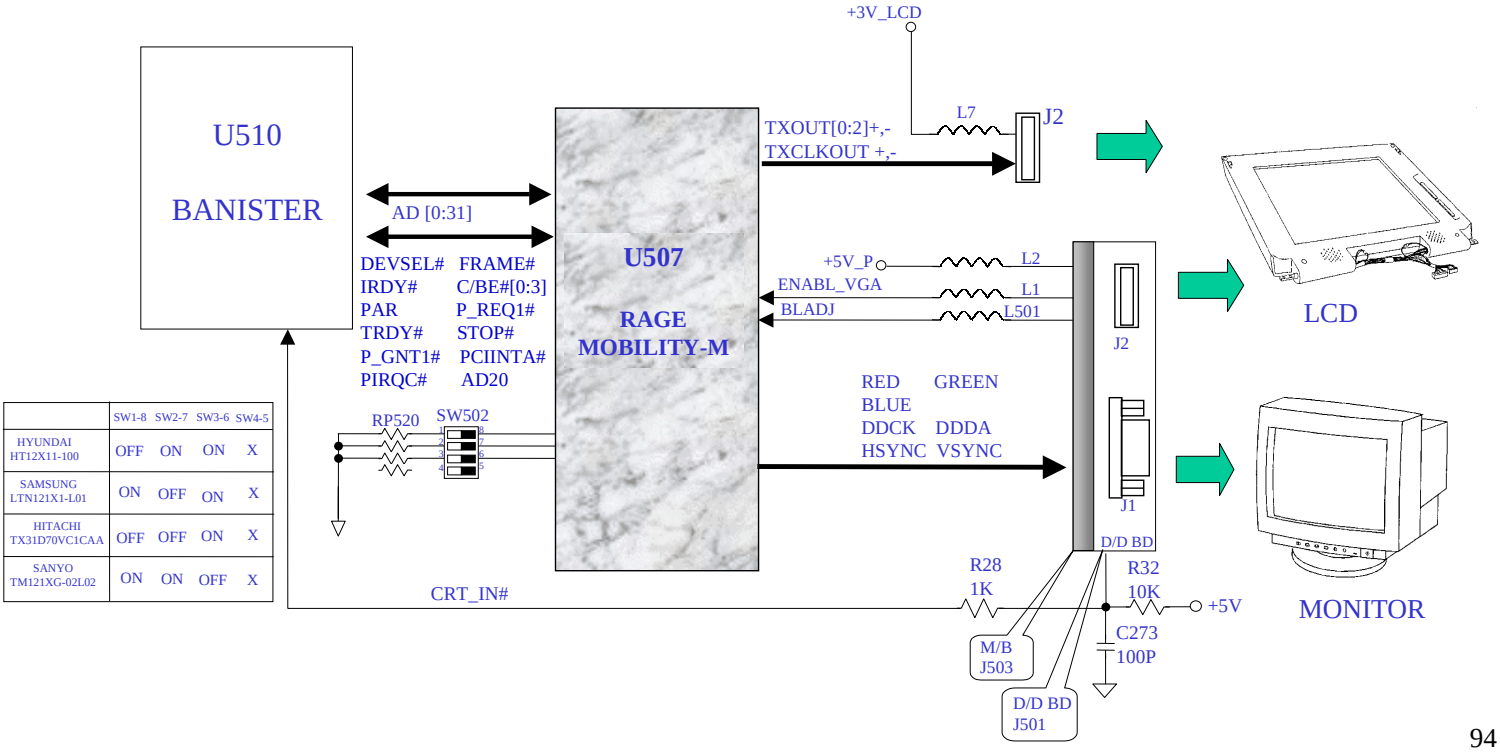


6.2 NO DISPLAY



6.3 VGA CONTROLLER FAILURE

There is no display or picture abnormal on LCD or monitor.



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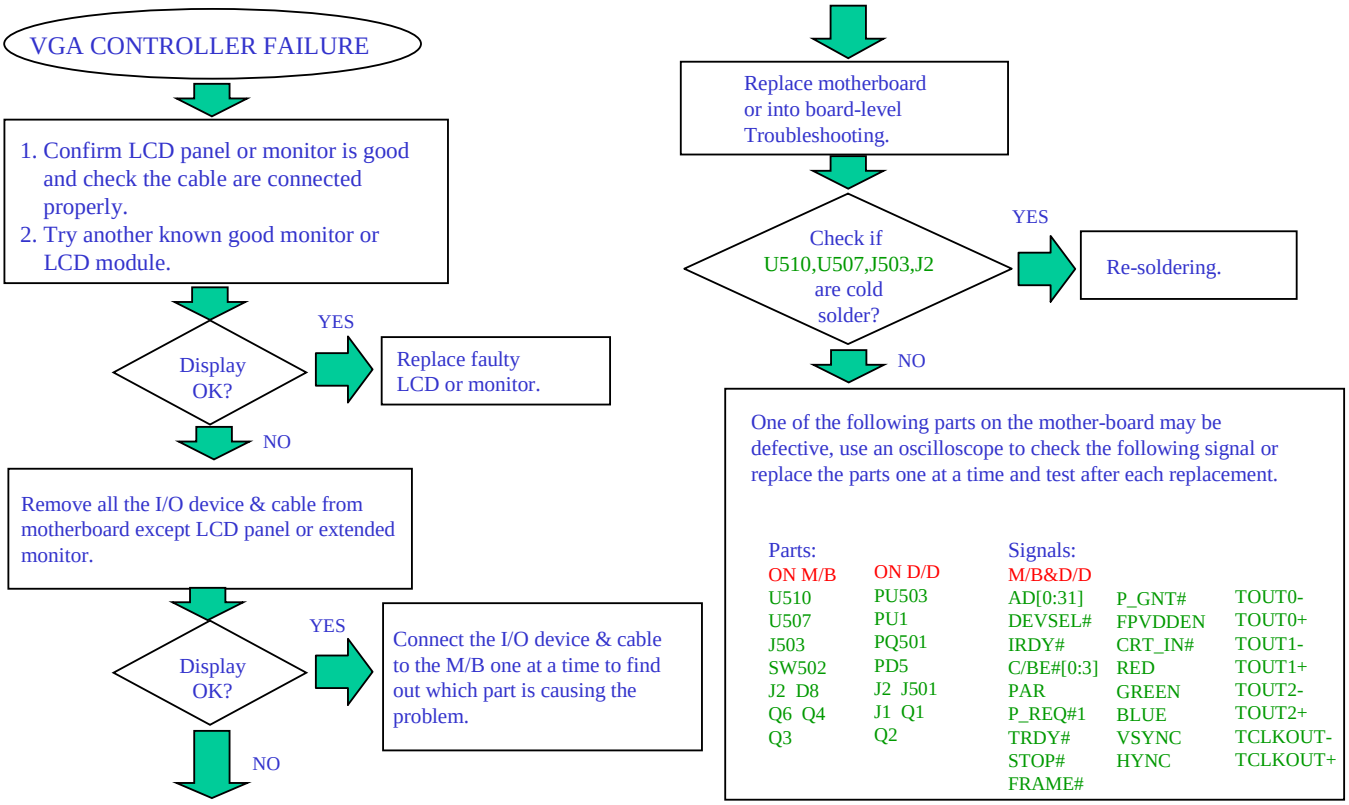
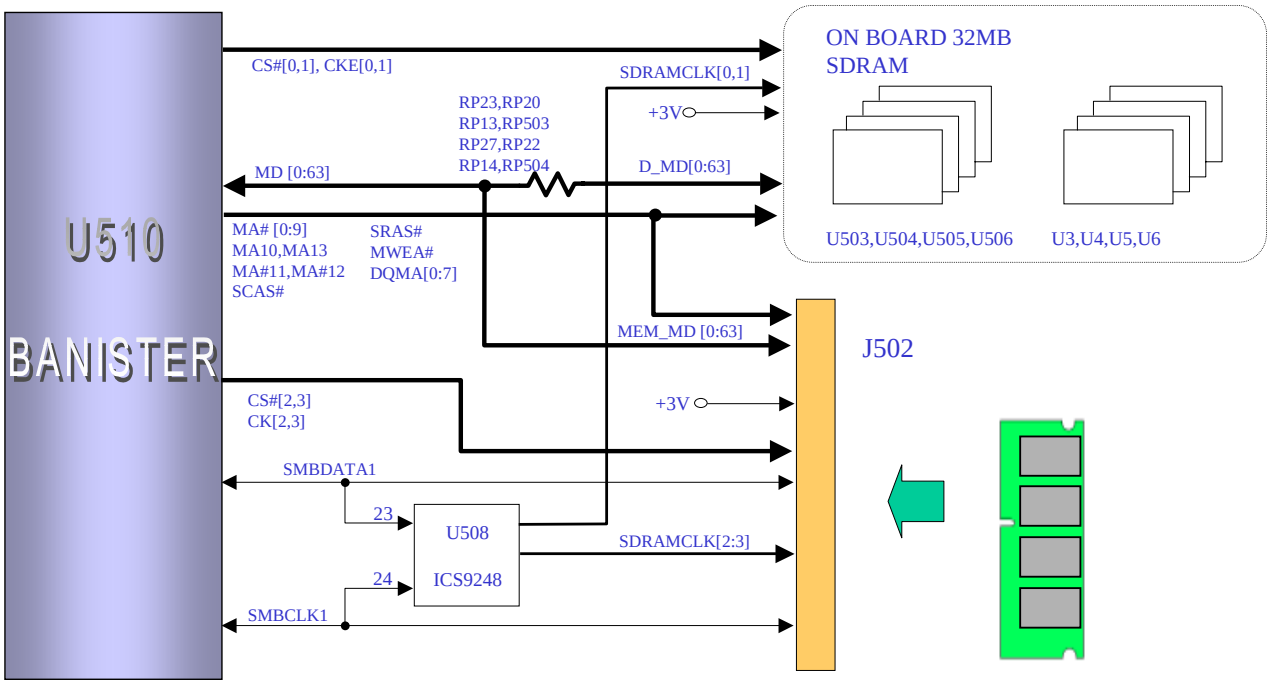
There is no display or picture abnormal on LCD or monitor.



6.4 MEMORY TEST ERROR

Either on board or extend SDRAM is failure or system hangs up.



6.4 MEMORY TEST ERROR

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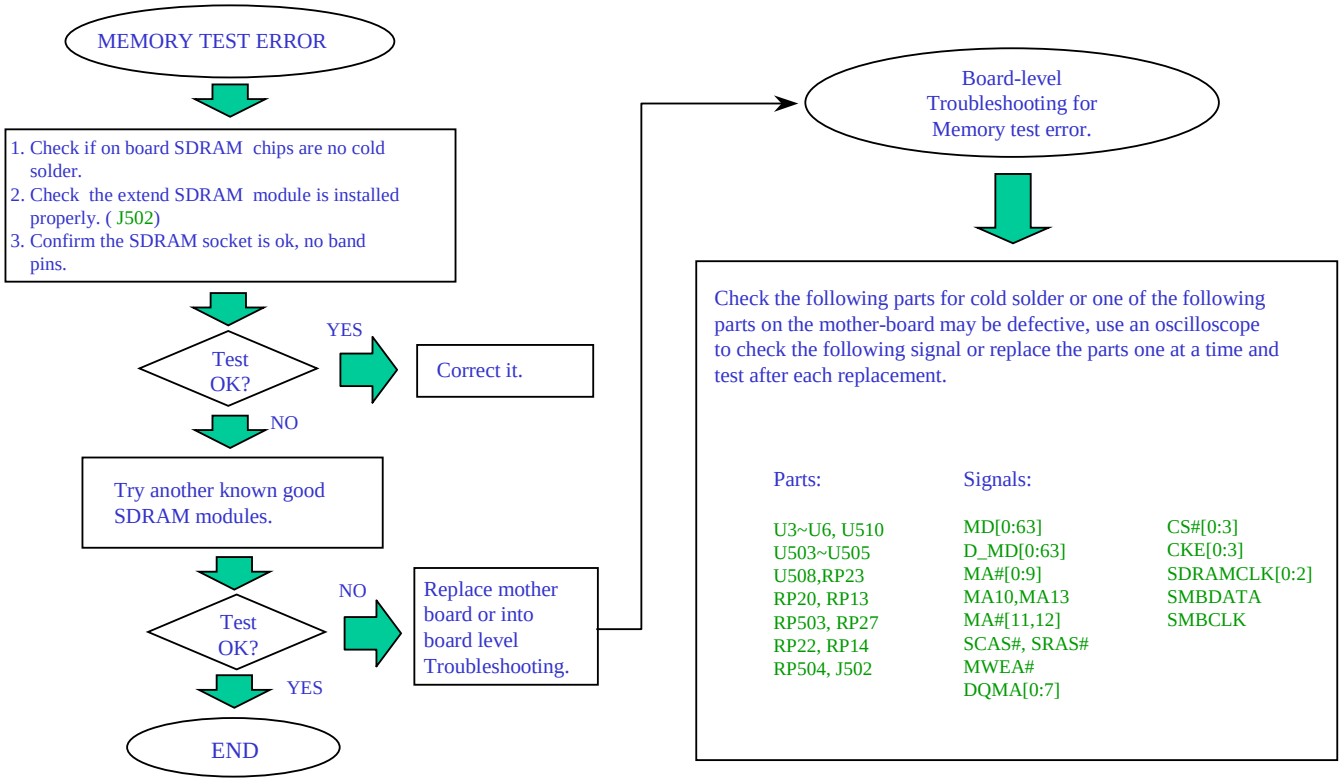
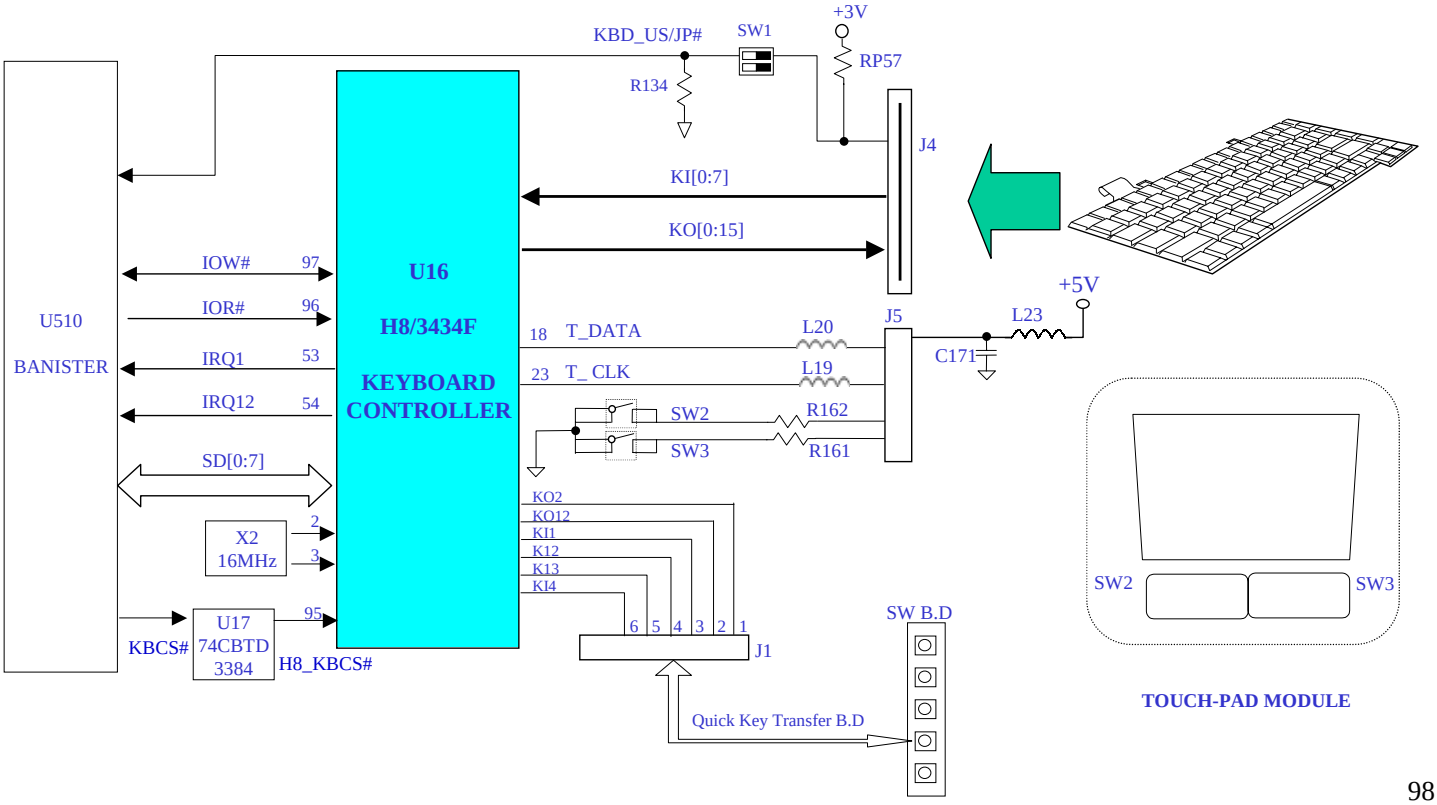


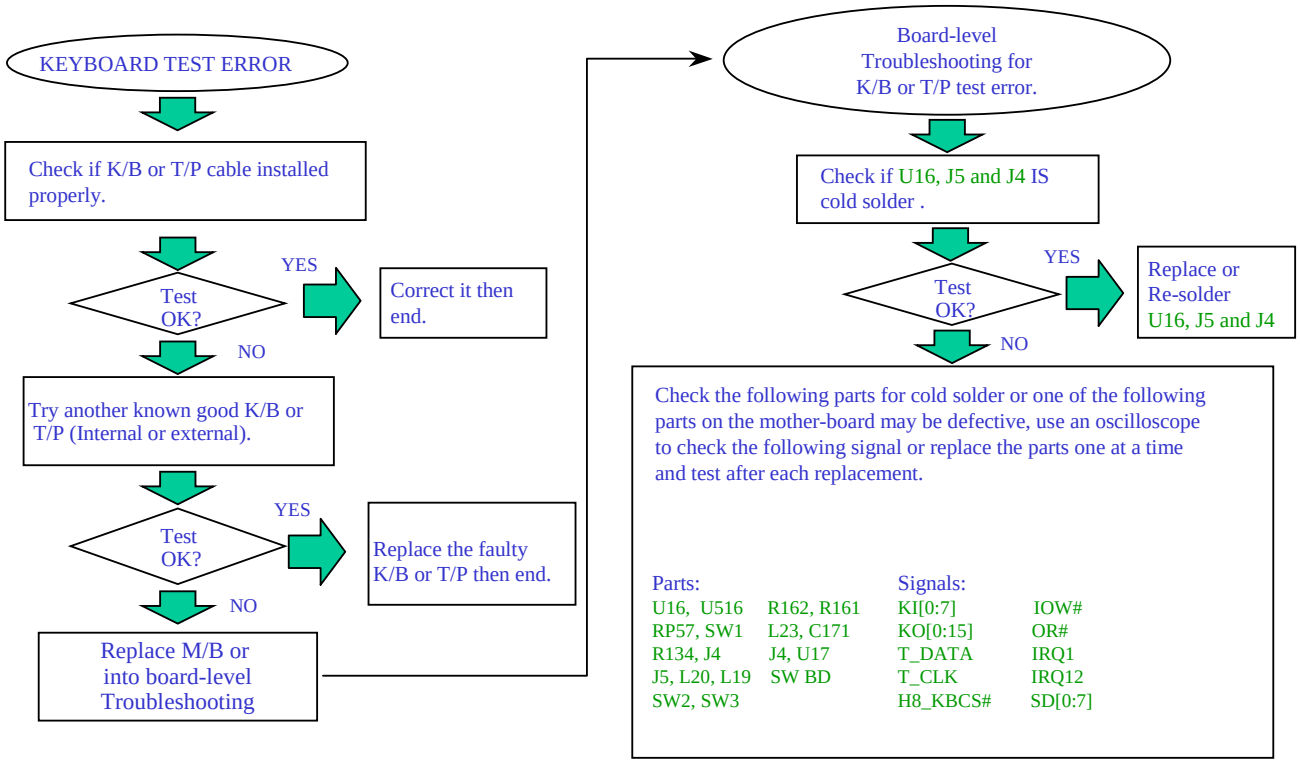
6.5 KEYBOARD(K/B) TOUCH-PAD(T/P) TEST ERROR

Error message of keyboard failure is shown or any key doesn't work.



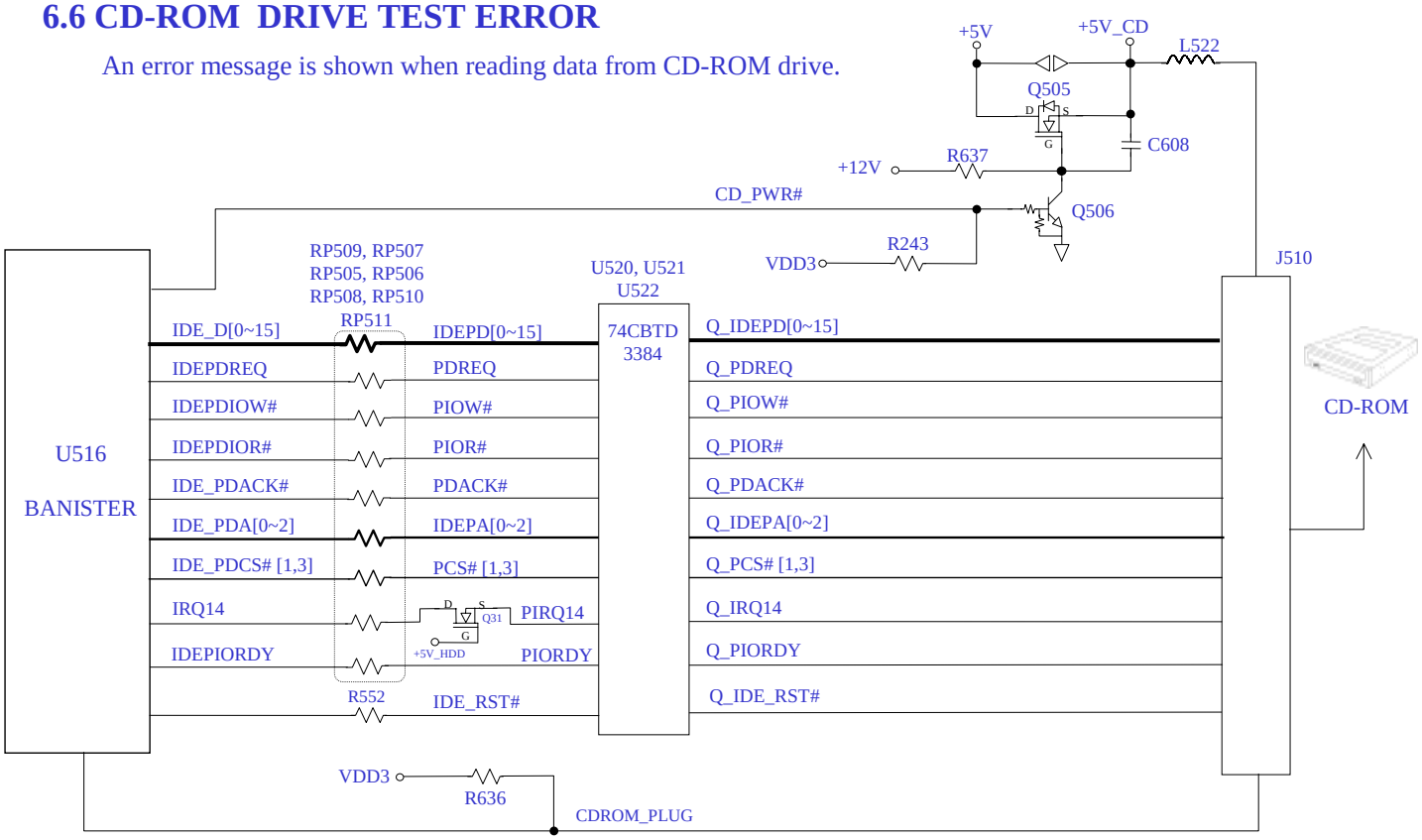
6.5 KEYBOARD(K/B) TOUCH-PAD(T/P) TEST ERROR

Error message of keyboard or touch pad failure is shown or any key doesn't work.



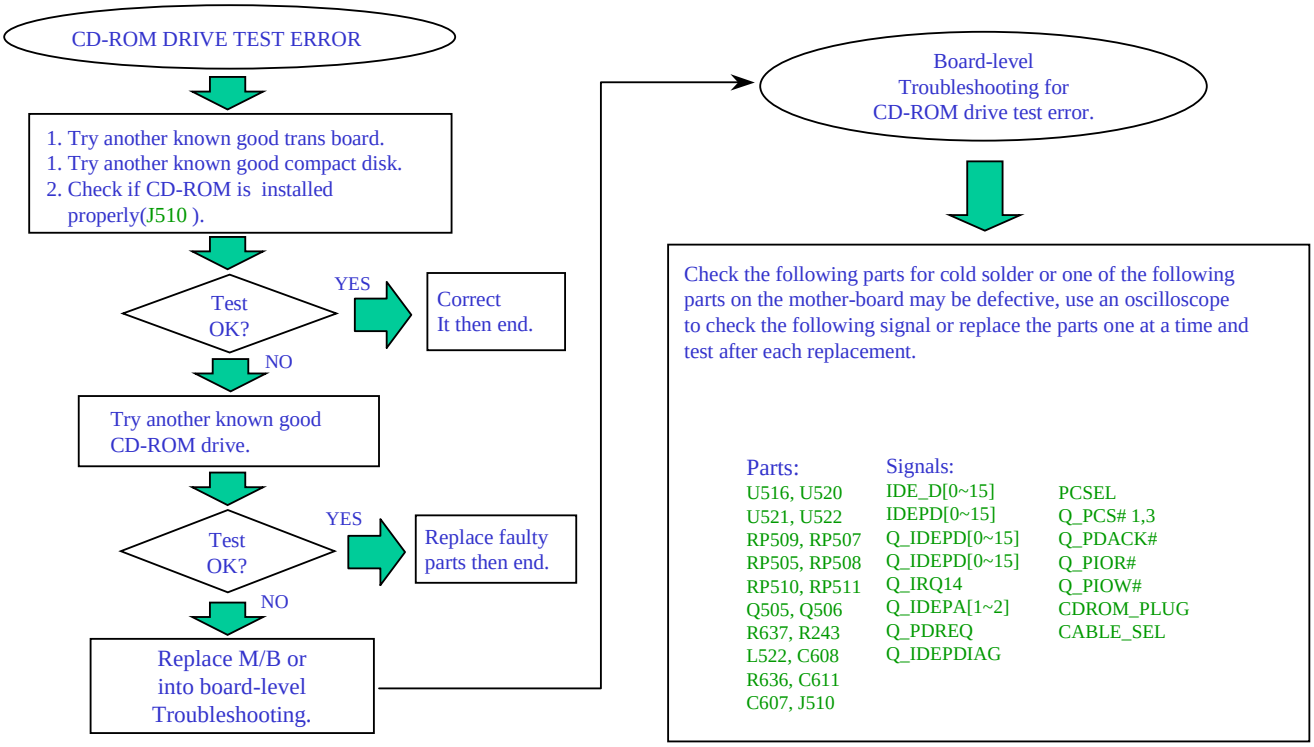
6.6 CD-ROM DRIVE TEST ERROR

An error message is shown when reading data from CD-ROM drive.



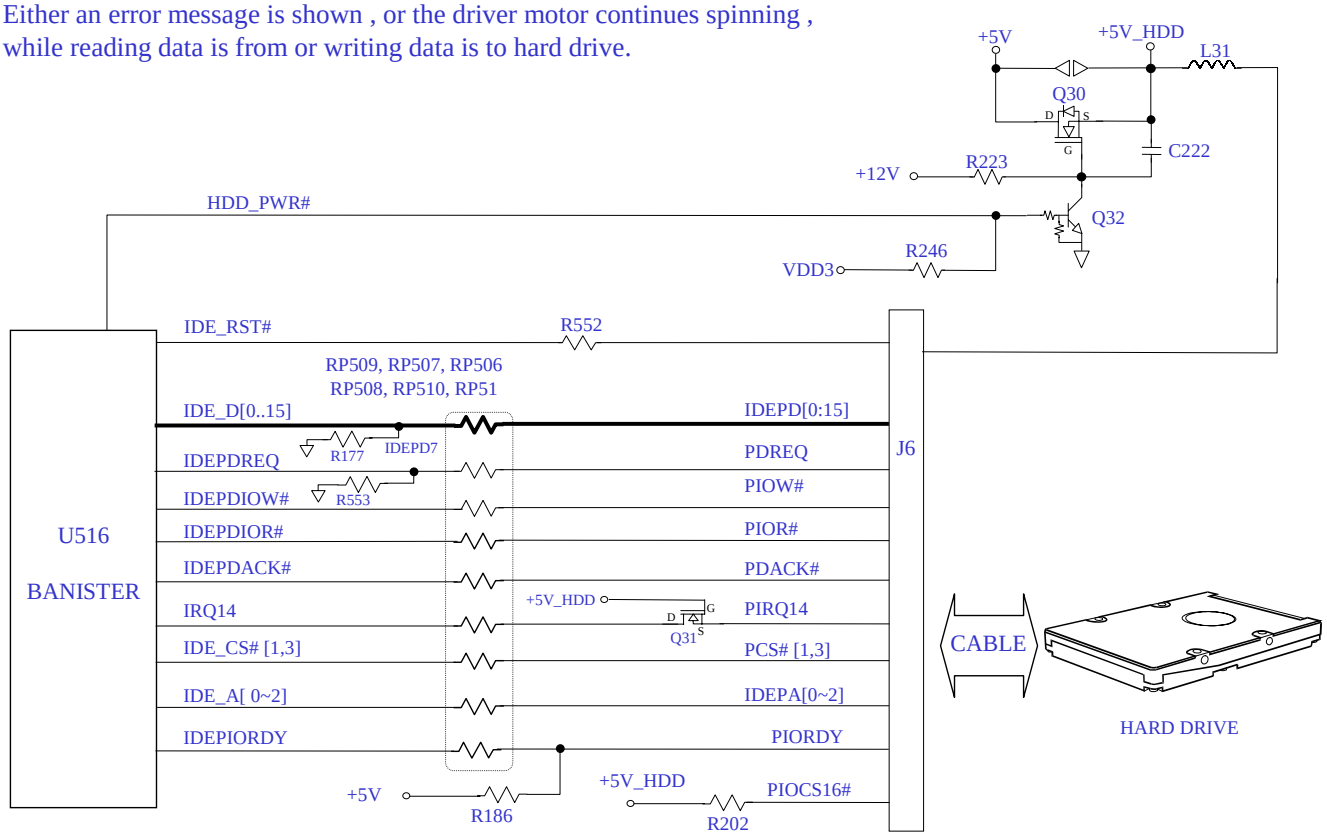
6.6 CD-ROM DRIVE TEST ERROR

An error message is shown when reading data from CD-ROM drive.



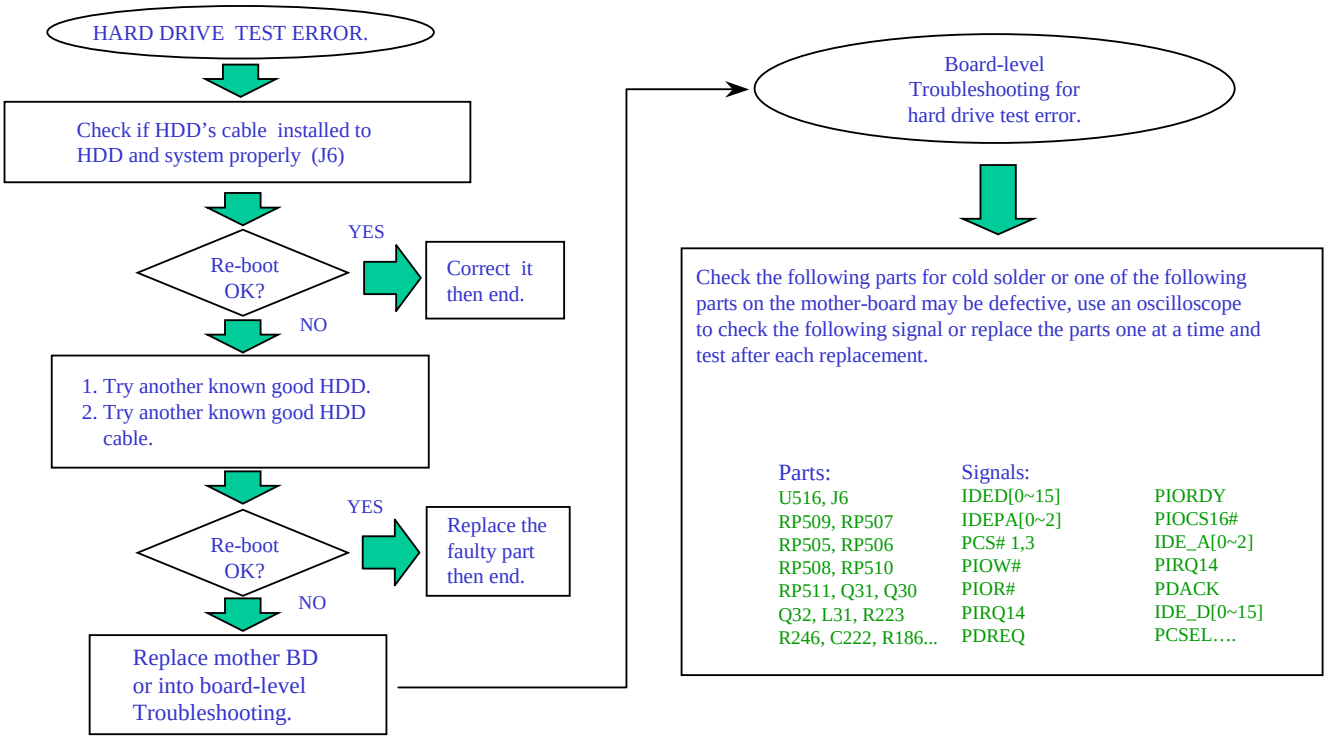
6.7 HARD DRIVE TEST ERROR

Either an error message is shown , or the driver motor continues spinning , while reading data is from or writing data is to hard drive.



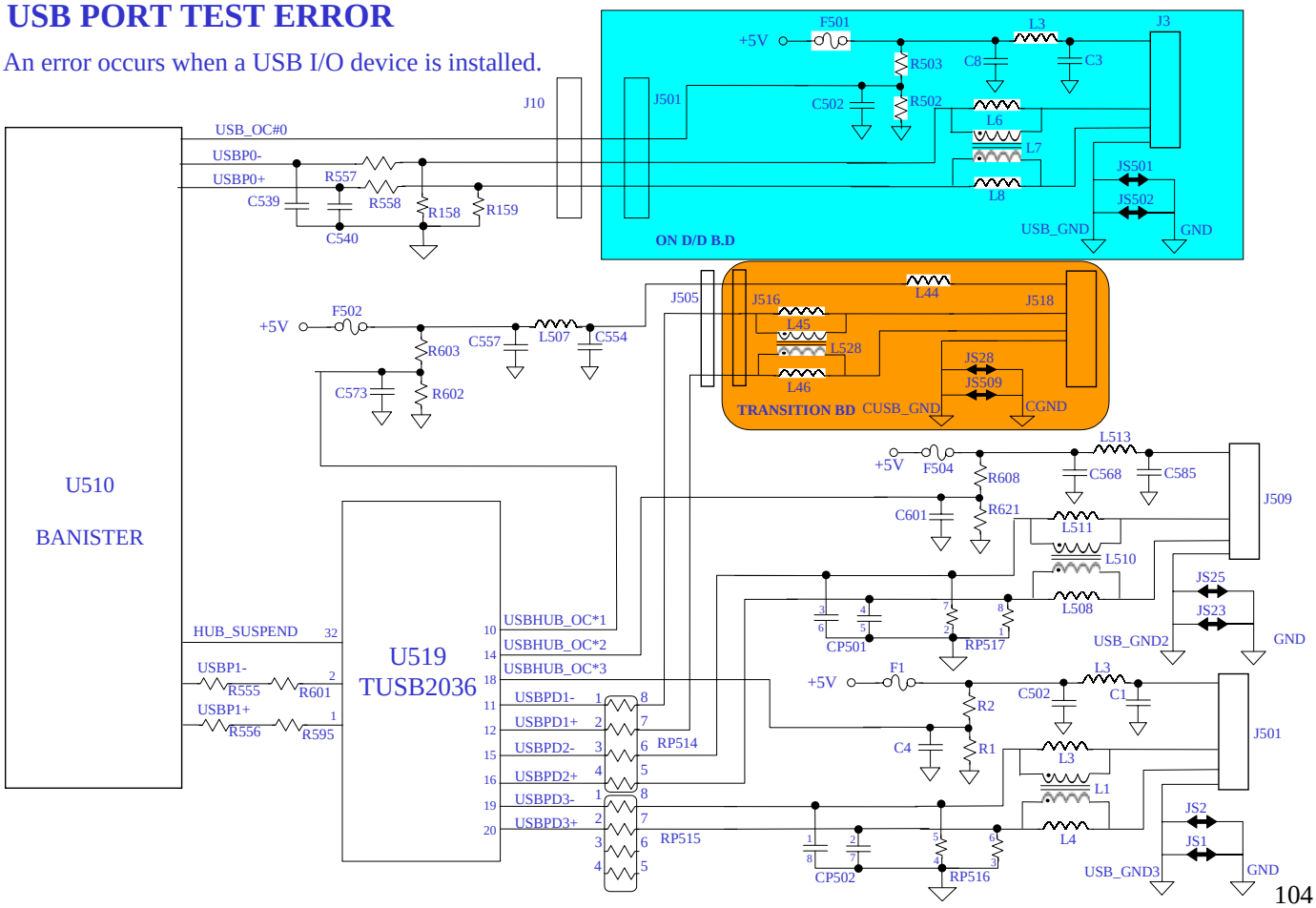
6.7 HARD DRIVE TEST ERROR

Either an error message is shown , or the driver motor continues spinning , while reading data is from or writing data is to hard drive.



6.8 USB PORT TEST ERROR

An error occurs when a USB I/O device is installed.



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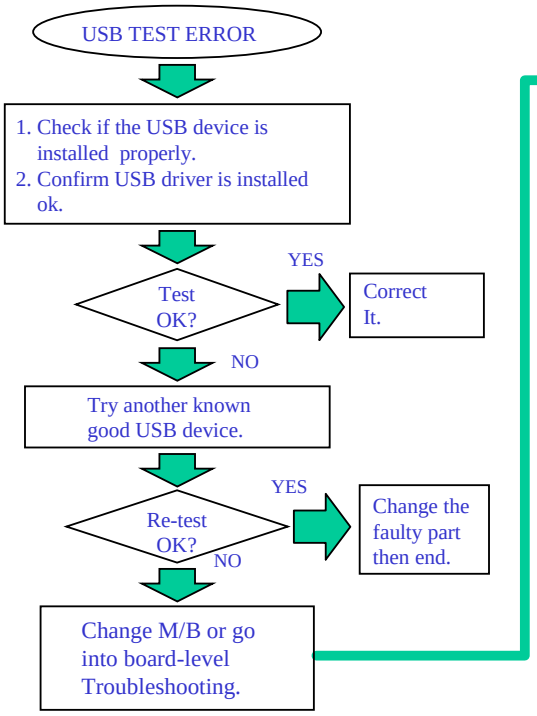


Board-level Troubleshooting for USB test error

Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

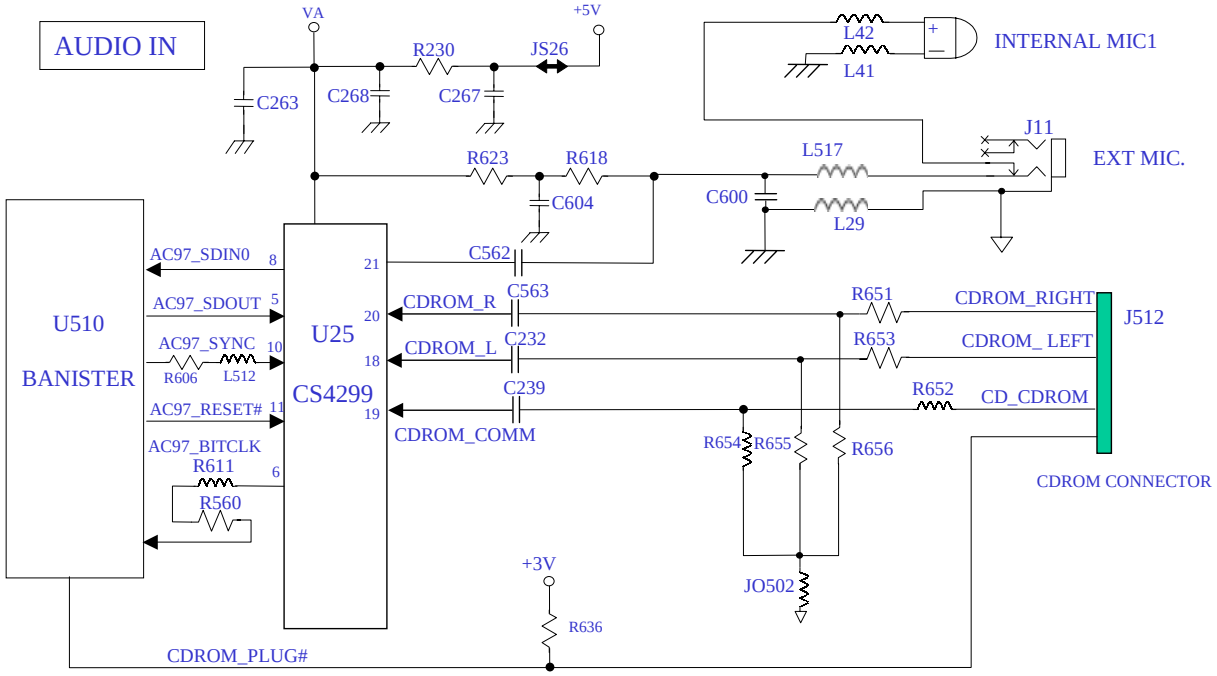
Parts:
ON M.B
U510, U519, R555
R556, R567, R568
R601, R595, RP514
RP515, X505, R701
C701, C702, CP502
CP501, RP516, RP517
F504, L513, R608
R621, C568, C585
L511, L510, L508
C581, C575, L509
F1, L2, R2, R1, C4
C502, C1, L3, L4

Parts:
ON M.B
L1, C3, C2, J501
R557, R558, C539
C540, R159, R158
ON D/D B.D
F501, R503, R502
C4, C8, L3, C3, L6
L7, L8, C2, C5, J3
J501
ON TRANSITION BD
L44, L45, L528, L46
J516, J518

Signals:
ON M.B
USBP1-
USBP1+
USBP0-
USBP0+
USBPD2-
USBPD2+
USBPD3-
USBPD3+
USBHUB_OC#[1~3]
ON D/D B.D
USBPD0-
USBPD0+
USB_OC#0
ON TRANS BD
CUSBPD1-
CUSBPD1+

6.9 AUDIO FAILURE

No sound from speaker after audio driver is installed.



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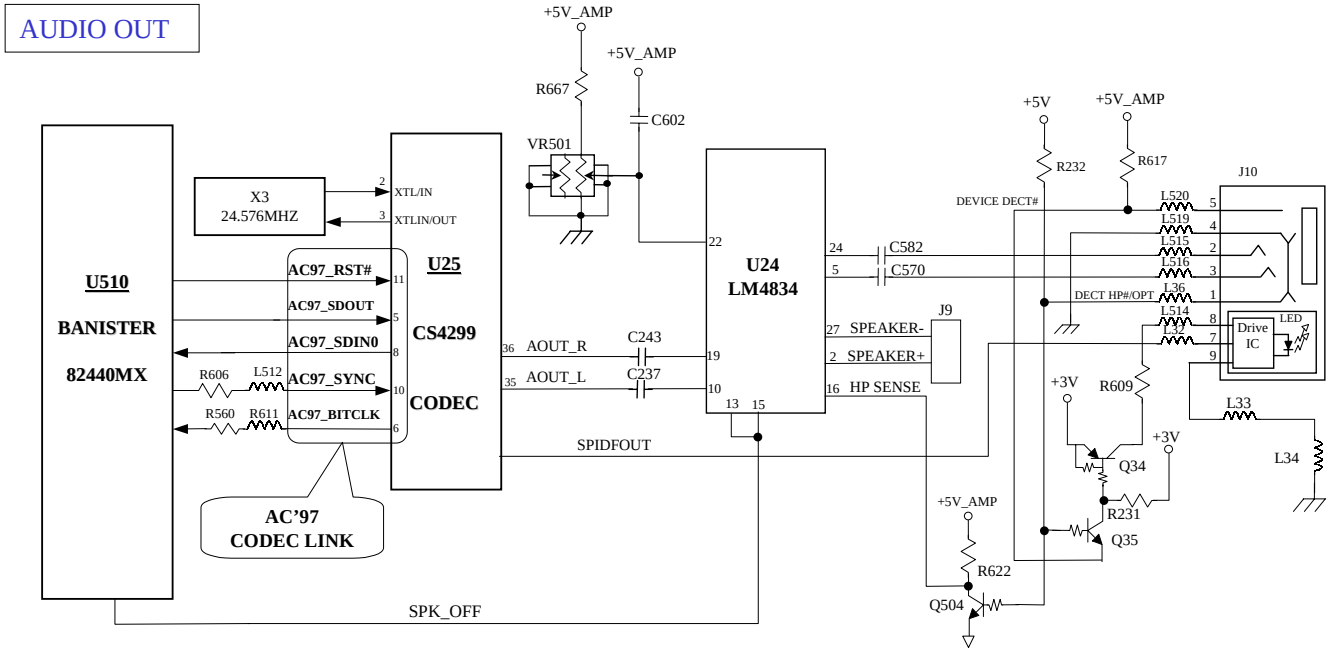
No sound from speaker after audio driver is installed.



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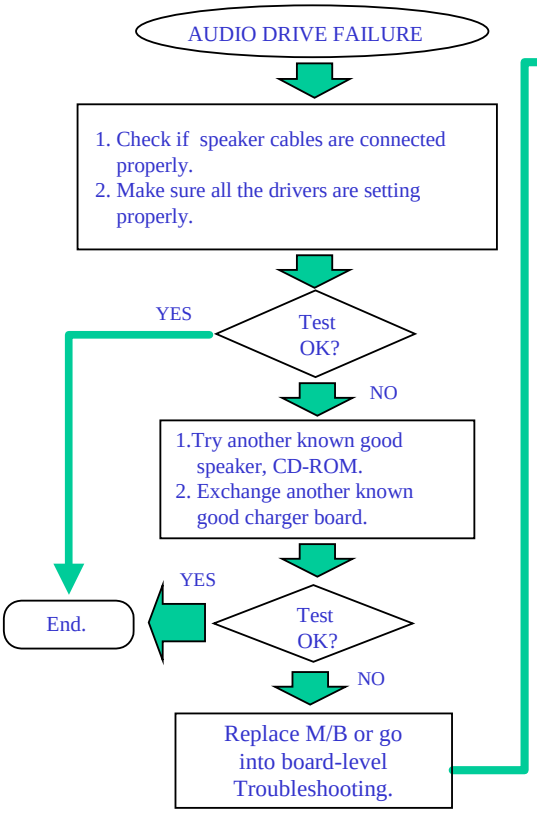


Board-level Troubleshooting for audio test error.

Check the following parts for cold solder or one of the following parts on the motherboard may be defective,use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

1. If no sound cause of line out, check the following parts & signals:

Parts:	Signals:
U510, U25	AOUT_R
C592,C256	AOUT_L
U24,VR501	SPEAKER+
C243, C237	SPEAKER-
C570, L582	LINE-HP_RIGHT
L516, L515	LINE-HP_LEFT
J10, J9	SPK_OFF

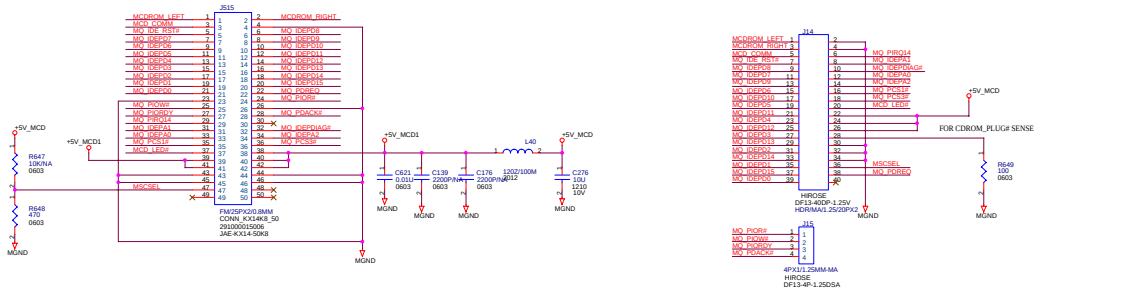
2. If no sound cause of MIC, check the following parts & signals:

Parts:	Signals:
U25, C562	MIC1
L517, C600	
C599, L29	
MIC1, J11	
L42, C277	

3. If no sound cause of CD-ROM, check the following parts & signals:

Parts:	Signals:
U25, C563	CDROM_L
C232, C239	CDROM_R
J510	CDROM_COMM

M722 CDROM MODULE TRANSITION BOARD



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SERVICE MANUAL & TROUBLESHOOTING GUIDE FOR M722

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