SERVICE MANUAL FOR

8375

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TESTING TECHNOLOGY DEPARTMENT / TSSC

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CONTENTS

1. Hardware Engineering Specification 4

1.1 Introduction 4
1.2 System Hardware Parts 5
1.3 Other Functions 48
1.4 Peripheral Components 53
1.5 Power Management 58
1.6 Appendix 1: GPIO definitions 60
1.7 Appendix 2: KBC Pins Definitions 61
1.8 Appendix 3: 8375 product spec 55

2. System View and Disassembly 67

2.1 System View 67
2.2 System Disassembly 70

3. Definition & Location of Connectors / Switches 92

3.1 Mother Board 92
3.2 DC Power Board 95
3.3 Touch-pad 96
3.4 Daughter Board 96

4. Definition & Location of Major Component 97

4.1 Mother Board 97

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8375 N/B Maintenance

CONTENTS

5. Pin Description of Major Component 99

5.1 Athlon XP Processor OPG462 Pin 99
5.2 VIA VT8372 North Bridge 102
5.3 VIA VT8235 South Bridge 107

6. System Block Diagram 116

7. Maintenance Diagnostics 117

7.1 Introduction 117
7.2 Error Codes 118
7.3 Maintenance Diagnostics 120

8. Trouble Shooting 121

8.1 No Power 122
8.2 No Display 127
8.3 VGA Controller Failure LCD No Display 132
8.4 External Monitor No Display 134
8.5 Memory Test Error 136
8.6 Keyboard (K/B) Touch-Pad (T/P) Test Error 138
8.7 Hard Disk Drive Test Error 140
8.8 CD-ROM Driver Test Error 142
8.9 USB Test Error 144

MiTac Secret Confidential Document

CONTENTS

8.10 PIO Port Test Error 147
8.11 Audio Failure 149
8.12 LAN Test Error 152
8.13 PC Card Socket Failure 154
8.14 IEEE 1394 Failure 156
8.15 TV Test Error 158

9. Spare Parts List 160

10. System Exploded Views 175

11. Circuit Diagram 176

12. Reference Material 211

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8375 N/B Maintenance

1. Hardware Engineering Specification

1.1 Introduction

The 8375 motherboard would support the Mobile AMD Athlon XP/ Athlon 4/ Duron Processors with OPGA/ CPGA, 462 Socket, which will support different speeds up to Mobile 45W 512K Cache Athlon XP 2800+.

This system is based on PCI architecture, which have standard hardware peripheral interface. The power management complies with Advanced Configuration and Power Interface (ACPI) 1.0. It also provides easy configuration through CMOS setup, which is built in system BIOS software and can be pop-up by pressing F2 at system start up or warm reset. System also provides icon LEDs to display system status, such as Power indicator, HDD/CDROM, NUM LOCK, CAP LOCK, SCROLL LOCK, SUSPEND MODE and Battery charging status. It also equipped 4 USB ports.

The memory subsystem supports 0MB on board memory,Two JEDEC-standard 200-pin, small-outline, dual in-line memory module (SODIMM) ,support PC2100.

Integrated VIA Apollo KT266 and S3 Graphics, ProSavage8 128-bit 2D/3D graphics controller with equivalent 8x AGP performance in a single chip, 64-bit Advanced Memory controller supporting PC2100/PC1600 DDR SDRAM. Combines with VIA VT8235 Vlink-LPC South Bridge with integrated audio, 4 USB ports, ATA100 IDE and LAN.

To provide for the increasing number of multimedia applications, the AC97 CODEC VT1612A is integrated onto the motherboard.

A full set of software drivers and utilities are available to allow advanced operating systems such as Windows Me and Windows 2000 to take full advantage of the hardware capabilities such as bus mastering IDE, Windows 95-ready Plug & Play, Advanced Power Management (APM) and Advance configuration and power interface (ACPI).

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Following chapters will have more detail description for each individual sub-systems and functions.

1.2 System Hardware Parts

CPU	- Mobile AMD Athlon XP/ Athlon 4/ Duron Processors with OPGA/ CPGA, 462 Socket, - Support up to Mobile 45W 512K Cache Athlon XP 2800+ - FSB 266MHz
Core logic	VIA KN266 + VIA VT8235
VGA Control	Pro Savage 8 GFX Integrated in KN266
System BIOS	256KB Flash EPROM Inside -Includes System BIOS, VGA BIOS, and plug & Play capability, ACPI
Memory	- 0MB on board memory; Expandable to 2.0GB of 200MHz or 266MHz DDR SDRAM - Two JEDEC-standard 200-pin, DDR SODIMMs - Support PC2100
Video Memory	8/16/32 MB
Clock Generator	ICS 950902
Embedded controller	Winbond W83L950D
PCMCIA+	Card Bus Controller: ENE CP1410 One type II slot/Card Bus support/no ZV port support
Audio System	AC97 CODEC: Advance Logic, Inc, VT1612A Power Amplifier: APA2020
Super I/O	VIA VT1211
Modem	56Kbps(V.90, worldwide) MDC Modem
LAN	MAC + PHY(VIA VT6103)
USB	Support USB2.0
TV-OUT	VIA VT1622M
IEEE1394	VIA VT6306L

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1.2.1 The AMD Athlon™ XP Processor Model 8

❑ Overview

The AMD Athlon™ XP processor model 8 is the latest member of the AMD Athlon family of processors designed to meet the computation-intensive requirements of cutting-edge software applications running on high-performance desktop systems. Delivered in an OPGA package, the AMD Athlon XP processor model 8 delivers the integer, floating-point, and 3D multimedia performance for highly demanding applications running on x86 system platforms.

The AMD Athlon XP processor model 8 delivers compelling performance for cutting-edge software applications that include high-speed Internet capability, digital content creation, digital photo editing, digital video, image compression, video encoding for streaming over the Internet, soft DVD, commercial 3D modeling, workstation-class Computer-Aided Design (CAD), commercial desktop publishing, and speech recognition. The AMD Athlon XP processor model 8 also offers the scalability and reliability that IT managers and business users require for enterprise computing.

The AMD Athlon XP processor model 8 features a seventh-generation micro architecture with an integrated, exclusive L2 cache, which supports the growing processor and system bandwidth requirements of emerging software, graphics, I/O, and memory technologies. The high-speed execution core of the AMD Athlon XP processor model 8 includes multiple x86 instruction decoders, a dual-ported 128-Kbyte split level-one (L1) cache, an exclusive 256-Kbyte L2 cache, three independent integer pipelines, three address calculation pipelines, and a superscalar, fully pipelined, out-of-order, three-way floating-point engine. The floating-point engine is capable of delivering outstanding performance on numerically complex applications.

The features of the AMD Athlon XP processor model 8 are QuantiSpeed™ architecture, a high-performance full-speed cache, a 266-MHz, 2.1-Gigabyte per second system bus, and 3DNow!™ Professional technology. The AMD Athlon system bus combines the latest technological advances, such as point-to-point topology, source-synchronous packet-

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-based transfers, and low-voltage signaling to provide an extremely powerful, scalable bus for an x86 processor.

The AMD Athlon XP processor model 8 is binary-compatible with existing x86 software and backwards compatible with applications optimized for MMX™, SSE, and 3DNow! technology. Using a data format and Single-Instruction Multiple-Data (SIMD) operations based on the MMX instruction model, the AMD Athlon XP processor model 8 can produce as many as four, 32-bit, single-precision floating-point results per clock cycle. The 3DNow! Professional technology implemented in the AMD Athlon XP processor model 8 includes new integer multimedia instructions and software-directed data movement instructions for optimizing such applications as digital content creation and streaming video for the internet, as well as new instructions for Digital Signal Processing (DSP) and communications applications.

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❑ QuantiSpeed™ Architecture Summary

The following features summarize the AMD Athlon XP processor model 8 QuantiSpeed architecture:

- An advanced nine-issue, superpipelined, superscalar x86 processor microarchitecture designed for increased Instructions Per Cycle (IPC) and high clock frequencies
- Fully pipelined floating-point unit that executes all x87(floating-point), MMX, SSE and 3DNow! Instructions
- Hardware data pre-fetch that increases and optimizes performance on high-end software applications utilizing high-bandwidth system capabilities

- An advanced nine-issue, superpipelined, superscalar x86 processor microarchitecture designed for increased Instructions Per Cycle (IPC) and high clock frequencies
- Fully pipelined floating-point unit that executes all x87(floating-point), MMX, SSE and 3DNow! Instructions
- Hardware data pre-fetch that increases and optimizes performance on high-end software applications utilizing high-bandwidth system capabilities

- Advanced two-level Translation Look-aside Buffer (TLB) structures for both enhanced data and instruction address translation. The AMD Athlon XP processor model 8 with QuantiSpeed architecture incorporates three TLB optimizations: the L1 DTLB increases from 32 to 40 entries, the L2 ITLB and L2 DTLB both use exclusive architecture, and the TLB entries can be speculatively loaded.

The AMD Athlon XP processor model 8 delivers excellent system performance in a cost-effective, industry-standard form factor. The AMD Athlon XP processor model 8 is compatible with motherboards based on Socket A.

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1.2.2 System frequency

System frequency synthesizer_ICS950902

Pin Configuration Recommended Application:

VIA P4X/P4M266 chipset with PC133 or DDR memory.

Output Features:

- 1 - Pair of differential CPU clocks @ 3.3V (CK408)/ 1 - Pair of differential open drain CPU clocks (K7)
- 1 - Pair of differential push pull CPU_PP clocks @ 2.5V
- 3 - AGP @ 3.3V
- 7 - PCI @ 3.3V
- 1 - 48MHz @ 3.3V fixed
- 1 - 24_48MHz @ 3.3V
- 2 - REF @ 3.3V, 14.318MHz

Features/Benefits:

- Programmable output frequency.
- Programmable output divider ratios.
- Programmable output rise/fall time.
- Programmable output skew.
- Programmable spread percentage for EMI control.
- Watchdog timer technology to reset system if system malfunctions.
- Programmable watch dog safe frequency.
- Support I 2 C Index read/write and block read/write operations.
- Uses external 14.318MHz crystal.

Key Specifications:

- CPU_CS - CPUT/C: <±250ps
- CPU_CS - AGP: <±250ps
- CPU - DDR/SD: <±250ps
- PCI - PCI: <500ps

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1.2.3 Core Logic VIA KN266+ VIA 8235

1.2.3.1 VIA KN266 Chipset

❑ **Feature List**

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- High Performance CPU Interface

- Socket-A support for AMD_ Athlon. Processors
- 266 or 200 MHz CPU Front Side Bus (FSB)
- Built-in Phase Lock Loop circuitry for optimal skew control within and between clocking regions
- Five outstanding transactions (four In-Order Queue (IOQ) plus one output latch)
- Dynamic deferred transaction support

- High Bandwidth 266MB/sec 8-bit V-Link Host Controller

- Supports 66 MHz V-Link Host interface with peak bandwidth of 266MB/sec
- V-Link operates at 2X or 4X modes
- Full-duplex commands with separate strobe / command
- Request / Data split transaction
- Configurable outstanding transaction queue for Host to V-Link Client accesses
- Supports Defer / Defer-Reply transactions
- Transaction assurance for V-Link Host to Client access (eliminates V-Link Host-Client Retry cycles)
- Intelligent V-Link transaction protocol to eliminate data wait-state / throttle transfer latency. All V-Link transactions (both Host and Client) have a consistent view of transaction data depthand buffer size to avoid data overflow.
- Highly efficient V-Link arbitration with minimum overhead. All V-Link transactions have predictable cycle length with known Command / Data duration.

❑ **Additional Features**

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- 250 MHz RAMDAC with Gamma Correction
- 12-bit interface to external TV encoder
- I2C Serial Bus and DDC Monitor Communications
- 2.5V Core and Mixed 3.3V/5V Tolerant and GTL+ I/O
- 35 x 35mm HSBGA (Ball Grid Array with Heat Spreader) package with 552 balls

❑ **Advanced High-Performance SDR / DDR DRAM Controller**

- DRAM interface synchronous with host CPU (100/133 MHz) for most flexible configuration
- DRAM interface may be faster than CPU by 33 MHz to allow use of 133 MHz memory with 100 MHz FSB
- DRAM interface may be slower than CPU by 33 MHz to allow use of 100 MHz memory with 133 MHz FSB
- Concurrent CPU, AGP, and V-Link access
- Supports SDR and DDR SDRAM memory types
- Clock Enable (CKE) control for SDRAM power reduction in high speed systems
- Mixed 1M / 2M / 4M / 8M / 16M / 32M / 64MxN DRAMs
- Supports 8 banks up to 4 GB DRAMs (512Mb x8/x16 DRAM technology) for registered SDR/DDR modules
- Supports 6 banks up to 3 GB DRAMs (512Mb x8/x16 DRAM technology) for unbuffered SDR/DDR modules
- Flexible row and column addresses. 64-bit data width only
- LVTTL 3.3V DRAM interface with 5V-tolerant inputs for SDR SDRAM and 2.5V SSTL-2 DRAM interface for DDR SDRAM
- Programmable I/O drive capability for MA, command, and MD signals
- Dual copies of control signals for improved drive

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- Two-bank interleaving for 16Mbit SDRAM support
- Two-bank and four bank interleaving for 64Mbit SDRAM support
- Supports maximum 8-bank interleave (i.e., 8 pages open simultaneously); banks are allocated based on LRU
- Seamless DRAM command scheduling for maximum DRAM bus utilization
- Four cache lines (16 quadwords) of CPU to DRAM write buffers
- Four cache lines of CPU to DRAM read prefetch buffers
- Read around write capability for non-stalled CPU read
- Speculative DRAM read before snoop result
- Burst read and write operation
- x-1-1-1-1-1-1-1 back-to-back accesses for SDR SDRAM
- x-1/2-1/2-1/2-1-1/2-1/2-1/2 back-to-back accesses for DDR SDRAM
- Supports DDR SDRAM CL 2/2.5/3 and 1T per command
- Decoupled and burst DRAM refresh with staggered RAS timing (CAS before RAS or self refresh)

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❑ **Integrated ProSavage8 2D/3D/Video Accelerator**

- Optimized Shared Memory Architecture (SMA)
- Equivalent 8x AGP internal performance
- 8 / 16 / 32 MB frame buffer using system memory
- Floating point triangle setup engine
- Single cycle 128-bit 3D architecture
- 8M triangles/second setup engine

- 140M pixels/second trilinear fill rate
- Microsoft DirectX texture compression
- Next generation, 128-bit 2D graphics engine
- High quality DVD video playback
- Flat panel monitor support
- 2D/3D resolutions up to 1920x1440

❑ **3D Rendering Features**

- Single-pass multiple textures
- Anisotropic filtering
- 8-bit stencil buffer
- 32-bit true color rendering
- Specular lighting and diffuse shading
- Alpha blending modes
- Massive 2K x 2K textures
- MPEG-2 video textures
- Vertex and table fog
- 16 or 24-bit Z-buffering
- Reflection mapping, texture morphing, shadows, procedural textures and atmospheric effects

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❑ 2D Hardware Acceleration Features

- ROP3 Ternary Raster Operation BitBLTs
- 8, 16, and 32 bpp mode acceleration

❑ Motion Video Architecture

- High quality up/down scaler
- Planar to packed format conversion
- Motion compensation for full speed DVD playback
- Hardware subpicture blending and highlights
- Multiple video windows for video conferencing
- Contrast, hue, saturation, brightness and gamma controls
- Digital port for NTSC/PAL TV encoders

❑ Extensive LCD Support

- Integrated 2-channel 110 MHz LVDS interface with 4-bit data path per channel
- Support for all resolutions up to 1600x1200
- Panel power sequencing
- Hardware Suspend/Standby control

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❑ **Flat Panel Monitor Support**

- 12-bit TFT flat panel interface to TMDS encoders
- Digital Visual Interface (DVI) 1.0 compliant

❑ **Advanced System Power Management Support**

- Power down of SDRAM (CKE)
- Independent clock stop controls for CPU / SDRAM and on-chip AGP bus
- Clock run and clock generator control for on-chip AGP bus
- VTT suspend power plane preserves memory data
- Suspend-to-DRAM and self-refresh power down
- Low-leakage I/O pads
- ACPI1.0B and PCIB us Power Management 1.1 compliant

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1.2.3.2 VIA VT8235 V-Link Client Highly Integrated South Bridge

❑ **High Bandwidth 533 MB/s 8-bit V-Link Client Controller**

- Supports 66 MHz V-Link Client interface with peak bandwidth of 533 MB/sec
- V-Link operates in 2x, 4x, and 8x modes
- Full duplex commands with separate Strobe / Command

- Request / Data split transaction
- Configurable outstanding transaction queue for V-Link Client accesses
- Auto Client Retry to eliminate V-Link Host-Client Retry cycles
- Auto connect / reconnect capability and dynamic stop for minimum power consumption
- Parity checking to insure correct data transfers

❑ Integrated Peripheral Controllers

- Integrated Fast Ethernet Controller with 1 / 10 / 100 Mbit capability
- Integrated USB 2.0 Controller with three root hubs and six function ports
- Dual channel UltraDMA-133 / 100 / 66 / 33 master mode EIDE controller
- AC-link interface for AC-97 audio codec and modem codec
- HSP modem support
- Integrated DirectSound compatible digital audio controller
- LPC interface for Low Pin Count interface to Super-I/O or ROM

❑ Integrated Legacy Functions

- Integrated Keyboard Controller with PS2 mouse support
- Integrated DS12885-style Real Time Clock with extended 256 byte CMOS RAM and Day/Month Alarm for ACPI
- Integrated DMA, timer, and interrupt controller
- Serial IRQ for docking and non-docking applications

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- Fast reset and Gate A20 operation

❑ Concurrent PCI Bus Controller

- 33 MHz operation
- Supports up to six PCI masters
- Peer concurrency
- Concurrent multiple PCI master transactions; i.e., allow PCI masters from both PCI buses active at the same time
- Zero wait state PCI master and slave burst transfer rate
- PCI to system memory data streaming up to 132Mbyte/sec (data sent to north bridge via high speed V-Link Interface)
- PCI master snoop ahead and snoop filtering
- Eight DW of CPU to PCI posted write buffers
- Byte merging in the write buffers to reduce the number of PCI cycles and to create further PCI bursting possibilities
- Enhanced PCI command optimization (MRL, MRM, MWI, etc.)
- Four lines of post write buffers from PCI masters to DRAM
- Sixteen levels (double-words) of prefetch buffers from DRAM for access by PCI masters
- Delay transaction from PCI master accessing DRAM
- Transaction timer for fair arbitration between PCI masters (granularity of two PCI clocks)
- Symmetric arbitration between Host/PCI bus for optimized system performance
- Complete steerable PCI interrupts
- PCI-2.2 compliant, 32 bit 3.3V PCI interface with 5V tolerant inputs

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❑ Plug and Play Controller

- PCI interrupts steerable to any interrupt channel
- Steerable interrupts for integrated peripheral controllers: USB, floppy, serial, parallel, and audio
- Microsoft Windows XPTM, Windows NTTM, Windows 2000TM, Windows 98TM and plug and play BIOS compliant
- Built-in NAND-tree pin scan test capability
- 22um, 2.5V, low power CMOS process
- Single chip 27 x 27 mm, 1.0 mm ball pitch, 487 pin BGA

❑ Fast Ethernet Controller

- High performance PCI master interface with scatter / gather and bursting capability
- Standard MII interface to external PHYceiver
- 1 / 10 / 100 MHz full and half duplex operation
- Independent 2K byte FIFOs for receive and transmit
- Flexible dynamically loadable EEPROM algorithm
- Physical, Broadcast, and Multicast address filtering using hashing function
- Magic packet and wake-on-address filtering
- Software controllable power down

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❑ UltraDMA-133 / 100 / 66 / 33 Master Mode EIDE Controller

- Dual channel master mode hard disk controller supporting four Enhanced IDE devices
- Transfer rate up to 133MB/sec to cover PIO mode 4, multi-word DMA mode 2 drives, and UltraDMA-133 interface
- Increased reliability using UltraDMA-133/100/66 transfer protocols
- Thirty-two levels (doublewords) of prefetch and write buffers
- Dual DMA engine for concurrent dual channel operation
- Bus master programming interface for SFF-8038i rev.1.0 and Windows-95com pliant
- Full scatter gather capability
- Support ATAPI compliant devices including DVD devices
- Support PCI native and ATA compatibility modes
- Complete software driver support

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❑ Direct Sound Ready AC97 Digital Audio Controller

- AC-Link access to 4 CODECs (AC97 + AMC97 + MC97)
- Multichannel Audio
- Bus Master Scatter / Gather DMA
- Dedicated read and write channels supporting simultaneous stereo playback and record
- Dedicated read and write channels supporting simultaneous modem receive and transmit
- 1 stereo DirectSound channel with source / volume control / mixer
- 1 shared FM / SPDIF PCM read channel

- 1 dedicated channel supporting multi-channel audio
- 32-byte line-bufers for each SGD channel
- Programmable 8bit / 16bit mono / stereo PCM data format support
- AC97 2.1 compliant

❑ System Management Bus Interface

- Host interface for processor communications
- Slave interface for external SMBus masters

❑ Universal Serial Bus Controller

- USB v2.0 and Enhanced Host Controller Interface (EHCI) v1.0 compatible
- USB v1.1 and Universal Host Controller Interface (UHCI) v1.1 compatible
- Eighteen level (doublewords) data FIFO with full scatter and gather capability
- Three root hubs and six function ports
- Integrated physical layer transceivers with optional over-current detection status on USB inputs
- Legacy keyboard and PS/2 mouse support

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❑ Sophisticated PC2001-Compatible Mobile Power Management

- Supports both ACPI (Advanced Configuration and Power Interface) and legacy (APM) power management
- ACPI v1.0 Compliant
- APM v1.2 Compliant
- CPU clock throttling and clock stop control for complete ACPI C0 to C3 state support
- PCI bus clock run, Power Management Enable (PME) control, and PCI/CPU clock generator stop control
- Supports multiple system suspend types: power-on suspends with flexible CPU/PCI bus reset options, suspend to DRAM, and suspend to disk (soft-off), all with hardware automatic wake-up
- Multiple suspend power plane controls and suspend status indicators
- One idle timer, one peripheral timer and one general purpose timer, plus 24/32-bit ACPI compliant timer
- Normal, doze, sleep, suspend and conserve modes
- Global and local device power control
- System event monitoring with two event classes
- Primary and secondary interrupt differentiation for individual channels
- Dedicated input pins for power and sleep buttons, external modem ring indicator, and notebook lid open/close for system wake-up
- 32 general purpose input ports and 32 output ports
- Multiple internal and external SMI sources for flexible power management models
- Enhanced integrated real time clock (RTC) with date alarm, month alarm, and century field
- Thermal alarm on external temperature sensing circuit
- I/O pad leakage control

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1.2.4 VIA VT1622M SDTV Encoder

Features

❑ **Input Format**

- Support digital RGB (15/16 or 24-bit) or YCrCb (CCIR601 or CCIR656) 16 bit 4:2:2 input video data in both interlaced or non-interlaced formats

❑ **Output Format**

- S-Video, composite, YCbCr, and SCART(RGB) with interlaced and non-interlaced scan output support
- YPbPr or RGB progressive scan output support
- NTSC (M and J) or PAL (B, D, G, H, I, M, N and Nc) TV output standards are support
- SDTV output mode (525p or 625p) compliant with EIA770-1 and EIA770-2

❑ **High quality 4 x 10-bit video DAC**

- Simultaneous 2 s-video or 1 s-video with 2 composite outputs support
- Simultaneous RGB or YCbCr component output with 1 composite output support
- One progressive scan channel with YPbPr or RGB component output support

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❑ Macrovision

- Support Macrovision 7.1 anti-copy protection
- Support Macrovision 1.0 AGC copy protection with 525p progressive scan output

❑ Other features

- Serial bus programming interface
- Graphic resolution up to 1024x768
- Programmable CRTC can support any vertical or horizontal scaling ratio minimum
- Down to 0.5
- Programmable power management
- Master or slave video timing operation
- P:P2 clocking mode for full TV screen
- Adaptive deflicker filter
- 64-pin LQFP package
- Automatic detection of TV presence

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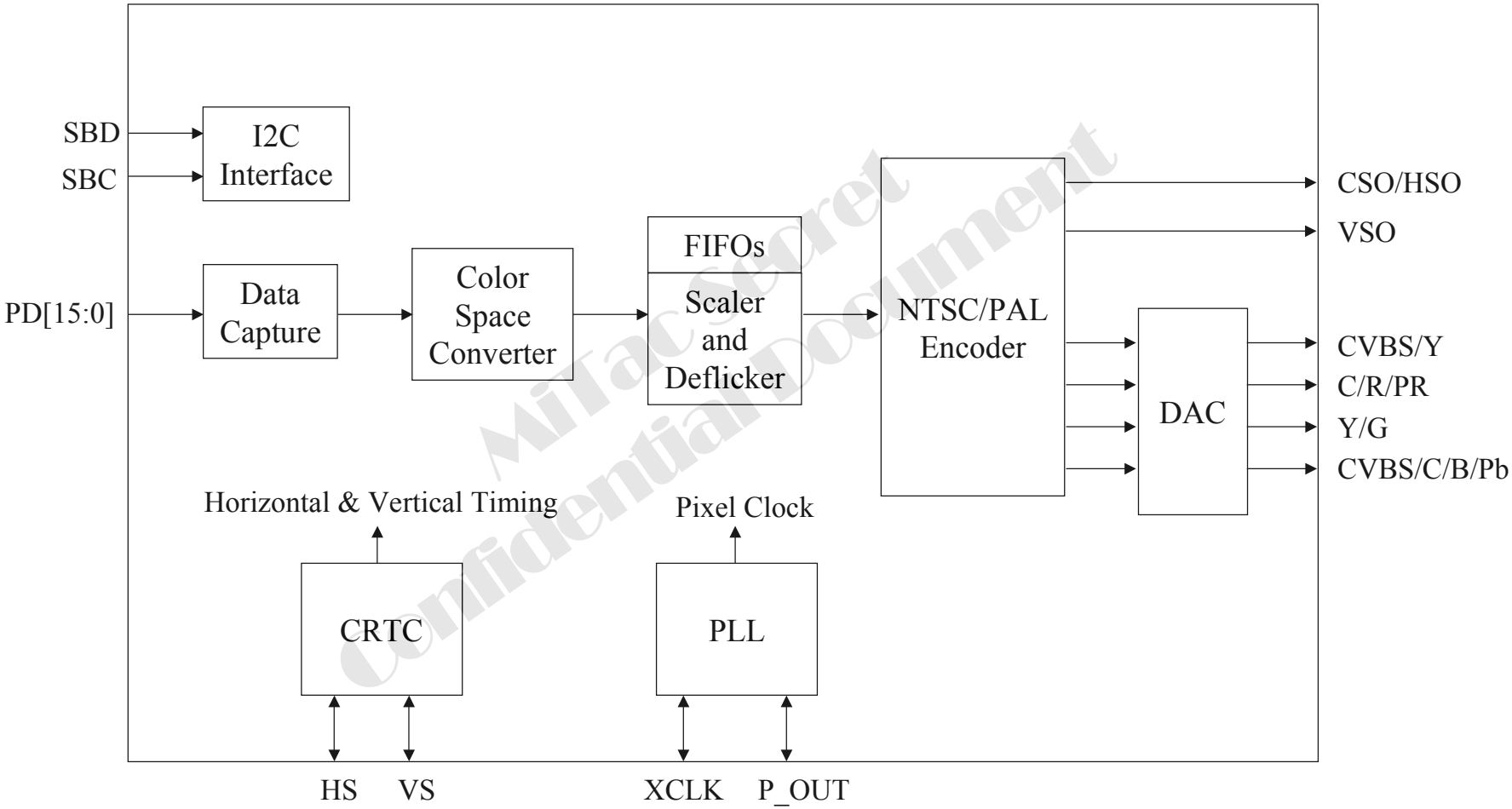
TV Encoder Block Diagram



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1.2.5 VIA VT6306L PCI 1394A Integrated Host Controller

❑ **Embedded 1394 Link Core**

- 32 bit CRC generator and checker for receive and transmit data
- On-chip isochronous and asynchronous receive and transmit FIFOs for packets (2K for general receive plus 2K for isochronous transmit plus 2K for asynchronous transmit)
- 8 isochronous transmit / receive contexts
- 3-deep physical post-write queue
- 2-deep physical response queue
- Dual buffer mode enhancements
- Skip Processing enhancements
- Block Read Request handling
- Ack_tardy processing

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❑ **OHCI Compliant Programming Interface**

- Compliant with 1394 Open HCI Specifications v1.0 and v1.1
- Descriptor based isochronous and asynchronous DMA channels for receive / transmit packets

❑ **32-Bit Power-Managed PCI Bus Interface**

- Compliant with PCI specification v2.2

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- High-performance bus mastering support
- Byte alignment to run in little-endian (x86/PCI) environment
- Compliant with PCI Bus Power Management Specification v1.1
- Supports power states D0, D1, D2, D3hot, and D3cold
- Supports CardBus interface

❑ **Supports I2C EEPROM and 4-Wire Serial ROM with GUID PROM Shadow to EEPROM Integrated 400 Mbit 3-Port PHY**

- Supports provisions of IEEE 1394-1995 Standard for High Performance Serial Bus and the P1394a Supplement 4.0.
- Fully interoperable with IEEE Std 1394-1995 devices
- Full P1394a Supplement Support includes:
- Arbitrated short reset,
- Enhanced priority arbitration,
- Connection debounce,
- Multispeed packet concatenation,
- Ack accelerated arbitration,
- Fly-by concatenation,
- Per port disable, suspend, resume, through register write and remote command packet,
- Remote access packet
- Boundary node short reset

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- No phy_ID wrap past 63
- Provides three 1394a fully compliant cable ports at 100/200/400 Mbit per second
- Host notification of PHY LinkOn events
- Logic performs bus initialization and arbitration functions
- Encode and decode functions included for data-strobe bit-level encoding
- Incoming data resynchronized to local clock.
- 24.576 MHz crystal oscillator and PLL provide TX/RX data at 100/200/400 Mbps and Link-Layer Controller clock at 49.152 MHz.
- Cable power presence monitoring.
- Programmable node power class information for system power management
- Fully Compliant P1394a 4.0 PHY register map
- Separate TPBIAS for each port
- Cable ports monitor line conditions for active connection to remote node
- Automatic power down inactive circuit and logic for low power application
- Self power up reset and pinless PLL to reduce passive component counts on system
- Automatic configuration to single-port, two-port, and three-port applications; unused ports power down automatically
- Dedicated power supply pins separate from link core
- 2KV ESD protection

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❑ **3.3V Power Supply with 5V Tolerant Inputs**

- **35um, Low Power CMOS Process**
- **128-Pin PQFP Package (VT6306) and 128-Pin LQFP Package (VT6306L) Available**

1.2.6 AC'97 Audio System: VIA VT1612A

Features

- AC'97 2.2 S/PDIF extension compliant codec
- 18-bit stereo full duplex SD codec
- 1Hz resolution VSR (Variable Sampling Rate)
- Integrated IEC958 line driver for S/PDIF
- S/PDIF compressed digital or LPCM audio out
- 3D stereo expansion for simulated surround
- 18-bit independent rate stereo ADC/DAC
- Hardware VU peak meters for PCM streams
- 4 stereo, 2 mono analog line-level inputs
- Alt. line-level output with volume control, or
- Headphone Amplifier with Thermal Protection
- Low Power consumption mode
- Exceeds Microsoft® WHQL logo requirements

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- 3V digital, 3.3 or 5V analog power supply
- 48-pin LQFP small footprint package

1.2.7 VIA VT1211 Low PIN Count Super I/O

Features

❑ **LPC (Low Pin Count) Interface**

- Complies with Intel Low Pin Count Interface Specification Revision 1.0
- Supports LDRQ#, SERIRQ protocols

❑ **Hardware Monitor Controller**

- Built-in 8-bit Analog to Digital Converter
- One thermal input for Pentium II type thermal diode
- 1 intrinsic Vcc voltage monitor input
- 5 external Universal Channels for monitor inputs
- Monitors 2 fan tachometer inputs
- 1 chassis open detection input

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- 1 chassis open detection input
- WatchDog comparison of all monitored values
- Provides VID0 - VID4 support for P6 class CPU
- Over temperature indicator output
- Over limit of fan and voltage indicator output
- Provides beep tone warning
- Serial Bus slave mode supported

❑ Fan Speed Controller

- Provides fan on-off and speed control
- Supports 2 programmable Pulse Width Modulation (PWM) outputs
- Duty cycle resolution of 1/256

❑ Flash-ROM Interface

- Supports up to 4MB flash ROM

❑ SmartGuardian Controller

- Provides automatic temperature to fan speed control

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8375 N/B Maintenance

- Provides automatic temperature to fan speed control
- Supports mix-and-match for temperature inputs and fan speed control outputs
- Overrides fan speed controller during catastrophic situations
- Provides over-temperature beep tone warning

❑ **Two 16C550 UARTs**

- Supports two standard Serial Ports
- Each port supports Serial Port

❑ **Floppy Disk Controller**

- Supports two 360K / 720K / 1.2M / 1.44M / 2.88M floppy disk drives
- Enhanced digital data separator
- 3-Mode drives supported

❑ **IEEE1284 Parallel Port**

- Standard mode -- Bi-directional SPP
- Enhanced mode -- EPP V1.7 and 1.9 compliant
- High speed mode -- ECP, IEEE1284 compliant

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- High speed mode -- ECP, IEEE1284 compliant
- Backdrive current reduction
- Printer power-on damage reduction

❑ **Game Port**

- Built-in 558 quad timers and buffer chips
- Supports direct connection to two joysticks

❑ **Dedicated MIDI Interface**

- UART implementation
- Supports direct connect to MPU-401 MIDI

❑ **56 General Purpose I/O Pins**

- Input mode supports switch de-bounce
- Output mode supports one set of programmable LED blinking periods

❑ **Watch Dog Timer**

- Times out the system, based on a user-programmable time-out period

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- Time resolution 1 minute, maximum 255 minutes

❑ **Dedicated Infrared pins**

- Compliant with IrDA 1.4 for VFIR

❑**Single 48MHz Clock Input**

❑**Single 3.3V Power Supply**

❑**128-pin LPQF**

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1.2.8 MDC: PCTEL Modem Daughter Card PCT2303W

The PCT2303W chipset is designed to meet the demand of this emerging worldwide AMR/MDC market. The combination of PC-TEL's well proven PCT2303W chipset and the HSP56TM MR software modem driver allows systems manufactures to implement modem functions in PCs at a lower bill of materials (BOM) while maintaining higher system performance.

PC-TEL has streamlined the traditional modem into the Host Signal Processing (HSP) solution. Operating with the Pentium class processors, HSP becomes part of the host computer's system software. It requires less power to operate and less physical space than standard modem solutions. PC-TEL's HSP modem is an easily integrated, cost-effective communications solution that is flexible enough to carry you into the future.

The PCT2303W chip set is an integrated direct access arrangement (DAA) and Codec that provides a programmable line interface to meet international telephone line requirements. The PCT2303W chip set is available in two 16-pin small outline packages (AC'97 interface on PCT303A and phone-line interface on PCT303W). The chip set eliminates the need for an AFE, an isolation transformer, relays, opto-isolators, and 2-to 4-wire hybrid. The PCT2303W chip set dramatically reduces the number of discrete components and cost required to achieve compliance with international regulatory requirements. The PCT2303W complies with AC'97 Interface specification Rev. 2.1. The chip set is fully programmable to meet worldwide telephone line interface requirements including those described by CTR21, NET4, JATE, FCC, and various country-specific PTT specifications. The programmable parameters of the PCT2303W chip set include AC termination, DC termination, ringer impedance, and ringer threshold. The PCT2303W chip set has been designed to meet stringent worldwide requirements for out-of-band energy, billing-tone immunity, lightning surges, and safety requirements.

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❑ **Operating System Compatibility**

✧ Windows 98 / NT4.0 /Win 2K /Win XP

❑ **Compatibility**

✧ ITU-T V.90	56000,54667,53333,52000,50667,49333,48000,46667,45333, 42667,41333 40000,38667,37333,36000,34667,33333,32000, 30667,29333, 28000bps

✧ K56Flex	56000,54000,52000,50000,48000,46000,44000,42000,40000, 38000,36000, 32000bps
✧ ITU-T V.34Annex	33600,31200 bps.
✧ ITU-T V.34	28800 bps
✧ ITU-T V.32bis	14400 bps
✧ ITU-T V.32	9600,4800 bps
✧ ITU-T V.22bis	2400 bps
✧ITU-T V.22	1200 bps
✧ ITU-T V.21	300 bps
✧ ITU-T V.23	1200/75 bps
✧ ITU-T V.17	14400,12000,9600,7200 bps
✧ ITU-T V.29	9600,7200 bps
✧ ITU-T V.27ter	4800,2400 bps
✧ Bell 212A	1200 bps
✧ Bell 103	300 bps

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❑ **Modulation**

✧ 56000bps(V90&K56Flex)	PCM
✧ 33600 bps (V.34Annex)	TCM

✧ 28800 bps (V.34)	TCM
✧ 14400 bps (V.32bis)	TCM
✧ 12000 bps (V.32bis)	TCM
✧ 9600 bps (V.32bis)	TCM
✧ 7200 bps (V.32bis)	QAM
✧ 9600 bps (V.32)	TCM, QAM
✧ 4800 bps (V.32)	QAM
✧ 14400 bps (V.17)	TCM
✧ 12000 bps (V.17)	TCM
✧ 9600 bps (V.29)	QAM
✧ 7200 bps (V.29)	QAM
✧ 4800 bps (V.27ter)	DPSK
✧ 2400 bps (V.27ter)	DPSK
✧2400 bps (V.22bis)	QAM
✧ ✧ 1200/75bps (V.23)	FSK
✧ 1200bps(V.22/Bell 212A)	DPSK
✧ 300bps(V.21/Bell 103)	FSK

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❑ **Data Compression**

✧ V.42bis, MNP5

❑ **Error Correction**

✧ V.42 LAPM, MNP 2-4

❑ **DTE interface**

✧ AC-Link

❑ **DTMF Tone Frequency**

✧ Low Group Frequency (Hz)

		697	770	852	941
High Group	1209	1	4	7	*
Frequency	1336	2	5	8	0
(Hz)	1477	3	6	9	#
	1633	A	B	C	D

❑ **DTMF signal level**

✧ High group -10+/-2dBm

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✧ Low group	-12+/-2dBm
✧ Dialing Type	Tone or pulse dialing
✧ Telephone Line interface	RJ-11
✧ Return Loss	300HZ - 3400HZ >= 10db
✧ Flow Control	XOFF/XON or RTS/CTS
✧ Receive Level	-35 +/- 2dBm
✧ Transmit Level	>-15 dBm

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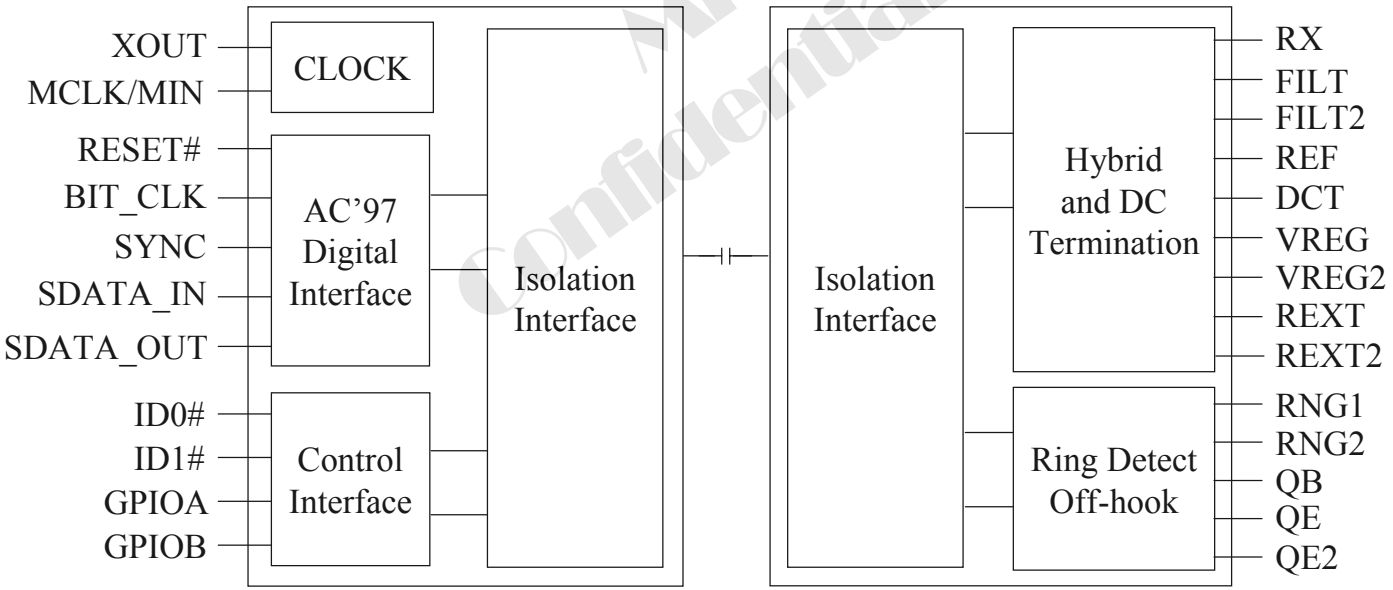
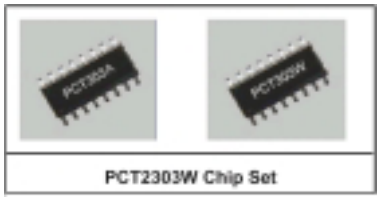
Specification and features subject to change without notice!





1.2.9 Keyboard System: WINBOND W83L950D Keyboard Controller

Features

- Pin –to-Pin compatible with Mitsubishi M3886 family
- 8051 uC based
- Keyboard Controller Embedded Controller (MTP version)
- Software optional with ISA and LPC interface
- Support either Parallel IRQ or SERIRQ (in LPC interface)
- Supply embedded programmable flash memory (internal ROM size: 40KB) and RAM size is 2 KB
- Support 2 SMBus interface for master and slave, for Smart Battery System communication.
- Support 4 Timer (8 bit) signal with 3 prescalers.
- Support 2 PWM channels, 2 D-A and 8 A-D converters.
- Reduce Firmware burden by Hardware PS/2 decoding
- Support 72 useful GPIOs totally
- Support Flash utility for on board re-flash
- Support ACPI
- Hardware fast Gate A20 with software programmable
- 80-pin LQFP

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1.2.10 System Flash Memory (BIOS)

- 2 M bit Flash memory
- Flashed by 3.3V only
- User can upgrade the system BIOS in the future just running flash program.

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1.2.11 System Memory

1.2.11.1 128MB, 256MB, 512MB (x64) 200-Pin DDR SDRAM SODIMMs

- JEDEC-standard 200-pin, small-outline, dual in-line memory module (SODIMM)
- Utilizes 200 Mb/s and 266 Mb/s DDR SDRAM components
- 128MB (16 Meg x 64, [H] and [HD]); 256MB (32 Meg x 64 [HD]); 512MB (64 Meg x 64 [HD])
- VDD= VDDQ= +2.5V ±0.2V
- VDDSPD = +2.2V to +5.5V
- 5V I/O (SSTL_2 compatible)
- Commands entered on each positive CK edge
- DQS edge-aligned with data for READs; center-aligned with data for WRITEs
- Internal, pipelined double data rate (DDR) architecture; two data accesses per clock cycle

- Bi-directional data strobe (DQS) transmitted/received with data— i.e., source-synchronous data capture
- Differential clock inputs (CK and CK# - can be multiple clocks, CK0/CK0#, CK1/CK1#, etc.)
- Four internal device banks for concurrent operation
- Selectable burst lengths: 2, 4, or 8
- Auto pre-charge option
- Auto Refresh and Self Refresh Modes
- 15.6µs (MT4VDDT864H, MT8VDDT1664HD), 7.8125µs (MT4VDDT1664H, MT8VDDT3264HD, MT8VDDT6464HD) maximum average periodic refresh interval
- Serial Presence Detect (SPD) with EEPROM
- Fast data transfer rates PC2100 or PC1600
- Selectable READ CAS latency for maximum compatibility
- Gold-plated edge contacts

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1.2.12 VIA VT6103 Fast Ethernet 10/100 1-Port PHY / Transceiver

Features

- Single Chip 100Base-TX / 10Base-T Physical Layer Solution
- Dual Speed – 100 / 10 Mbps

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- Half and Full Duplex
- MII Interface to Ethernet Controller
- MII Interface to Configuration & Status
- Optional Repeater Interface
- Auto Negotiation: 10 / 100, Full / Half Duplex
- Meet All Applicable IEEE 802.3, 10Base-T and 100Base-Tx Standards
- On Chip Wave Shaping – No External Filters Required
- Adaptive Equalizer
- Baseline Wander Correction
- LED Outputs
- Link Status
- Duplex status
- Speed Status
- Collision
- 48 Pin SSOP Package

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1.2.13 PC Card Interface Controller: CP1410

The ene CP1410 is a high-performance PCI-to-CardBus controller that support a single PC Card socket compliant with the 1997 PC Card Standard. The CP1410 provides features that make it the best choice for bridging between PCI and PCI Cards in both notebook and desktop computers. The 1997 PC Card Standard retains the 16-bit PC Card specification defined in PCI Local Bus Specification and defines the 32-bit PC Cards, powered at 5V or 3.3V, as required.

The CP1410 is compliant with the PCI Local Bus Specification, and its PCI interface can act as either a PCI master device or a PCI slave device. The PCI bus mastering is initiated during 16-bit PC Card DMA transfers or CardBus PC Card bridging transactions. The CP1410 is also compliant with the latest PCI Bus Power Management Interface Specification and PCI Bus Power Management Interface Specification for PCI to CardBus Bridges.

A card signals are internally buffered to allow hot insertion and removal without external buffering. The CP1410 is register compatible with the Intel 82365SL-DF and 82365SL ExCA controls. The CP1410 internal data path logic allows the host to access 8-, 16-, and 32-bit cards using full 32-bit PCI cycles for maximum performance. Independent buffering and a pipeline architecture provide an unsurpassed performance level with sustained bursting. The CP1410 can also be programmed to accept fast posted wires to improve system-bus utilization.

Multiple system-interrupt signaling options are provided, including: parallel PCI, parallel ISA, serialized ISA, and serialized PCI. Furthermore, general-purpose inputs and outputs are provided for the board designer to implement sideband functions. Many other features designed into the CP1410, such as socket activity light-emitting diode(LED) outputs, are discussed in detail throughout the design specification.

An advanced complementary metal-oxide semiconductor (CMOS) process achieves low system power consumption

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while operating at PCI click rates up to 33 MHz. Several low-power modes enable the host power management system to further reduce power consumption.

The CP1410 supports the following features:

- ability to wake from D3hot and D3cold
- 144-Pin Low-Profile QFP (PGE), 144-ball MicroStar Ball Grid Array (GGU) package, or 209-Pin MicroStar Ball Grid Array (GHK) package
- 3.3-V core logic with universal PCI interfaces compatible with 3.3-V and 5-V PCI signaling environments
- mix-and-match 5-V/3.3-V 16-bit PC Cards and 3.3-V CardBus Cards
- Single PC Card or CardBus slots with hot insertion and removal
- burst transfers to maximize data throughput on the PCI bus and CardBus Cards
- Parallel PCI interrupts, parallel ISA IRQ and parallel PCI interrupts, serial ISA IRQ with parallel PCI interrupts, and serial ISA IRQ and PCI interrupts
- Serial EEPROM interface for loading subsystem ID and subsystem vendor ID
- Pipelined architecture allows greater than 130M bps throughput from CardBus-to-PCI and from PCI-to-CardBus
- Interface to parallel single-slot PC Card power interface switches like the TI TPS2211
- Up to five general-purpose I/Os
- Programmable output select for CLKRUN
- Five PCI memory windows and two I/O windows available to the 16-bit PC Card socket
- Two I/O windows and two memory windows available to each CardBus socket
- Exchangeable Card Architecture (ExCA) compatible registers are mapped in memory and I/O space

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- Distributed DMA (DDMA) and PC/PCI DMA
- 16-Bit DMA on both PC Card sockets
- Ring indicate, SUSPEND, PCI CLKRUN, and CardBus CCLKRUN
- Socket activity LED pins
- PCI Bus Lock (LOCK)
- Advanced Submicron, Low-Power CMOS Technology
- Internal Ring Oscillator

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1.2.14 Audio Power Amplifier : APA2020A

Features

- Low Supply Current , IDD= 8mA at Stereo BTL
- Low Shutdown Current , IDD= 0.5 £gA
- Depop Circuitry Integrated
- Low Supply Voltage
- Thermal Shutdown Circuitry Integrated
- Output Power at 1% THD+N , VDD=5V

  - 1.8 W/Ch (typ) into a 4 Ω Load
  - 1.2 W/Ch (typ) into a 8 Ω Load

- Bridge-Tied Load (BTL) or Single-Ended (SE) Modes Operation
- Various 24-Pin Power Packages Available SOP , TSSOP-P
- High Supply Voltage Ripple Rejection
- Applications General Description

  The APA2020A is a stereo bridge-tied audio power amplifier in various 24-pin power packages , including SOP , TSSOP-P. When connecting to a 5V voltage supply , the APA2020A is capable of delivering 1.8W/1.2W of continuous RMS power per channel into 4Ω/8Ω loads with less than 1% THD+N, respectively. The APA2020A simplifies design and frees up board space for other features .

- Stereo Audio Power Amplifier for Notebook Computer

  The APA2020A also served well in low-voltage applications , which provides 800-mW per channel into 4Ω loads with a 3.3V supply voltage . Both of the depop circuitry and the thermal shutdown protection circuitry are integrated in the APA2020A , that reduces pops and clicks noise during power up and when using the shutdown or mute modes and protects the chip from being destroyed by over-temperature failure. To simplify the audio system design in notebook computer applications , the APA2020A combines a stereo bridge-tied loads (BTL) mode for speaker drive and a stereo single-end (SE) mode for headphone drive into a single chip , where both modes are easily switched by the SE/BTL input control pin signal . For power sensitive applications , the APA2020A also features a shutdown function which keeps the supply current only 0.5 £gA (typ)

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1.2.15 Single-Slot PC Card Power Interface Switch: TPS2211

TPS2211 is a single slot PCMCIA and CardBus power switch. It integrates control logic, low switching resistance MOSFET, over current alarm and over temperature auto shutdown circuits. It can deliver 3.3V or 5V to PC Card xVCCOUT and 3.3V, 5V or 12V to PC Card xVPPOUT. The output current is up to 1A for xVCCOUT and 250mA for xVPPOUT. The power is controlled by 4-wire parallel data interface VCCD0Z, VCCD1Z, VPPD0 and VPPD1.

- Fully integrated Vcc and Vpp Switching for Single-Slot PC Card Interface
- Low Rds(on)(90-mohm 5-V Vcc Switch and 3.3-V Vcc Switch)
- Compatible with controllers from cirrus , Ricoh ,O2Micro , and Texas Instruments
- 3.3 –V Low –voltage Mode
- Meets PC Card Standards
- 12-V Supply Can BE Disable Except During 12-V Flash programming
- Short –Circuit and Thermal Protection
- Spacing-Saving 16-Pin SSOP(DB)
- Copatible with 3.3-V ,5-V and 12-v PC Cards
- Break-Before-Make Switching

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1.3 Other Functions

1.3.1 Hot Key Function

Keys Combination	Feature	Meaning
Fn + F1	Reserve	
Fn + F2	Reserve	
Fn + F3	Reserve	
Fn + F4	Reserve	
Fn + F5	LCD/CRT Switching	Switch display mode of LCD only, CRT only, and simultaneously display.
Fn + F6	Brightness Down	Decreases LCD brightness
Fn + F7	Brightness Up	Increases LCD brightness
Fn + F8	Reserve	
Fn + F9	Reserve	
Fn + F10	Reserve	
Fn + F11	Panel Off/On	Toggle Panel on/off
Fn + F12	Suspend	Force system into either Suspend to DRAM (S3) or Suspend to HDD (S4) mode based on BIOS Setting

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1.3.2 Power on/off/suspend/resume button

- **APM mode**

  At APM mode, Power button is on/off system power.

- **ACPI mode**

At ACPI mode. Windows power management control panel set power button behavior.

You could set “standby”, “power off” or “hibernate”(must enable hibernate function in power Management) to power button function.

Continue pushing power button over 4 seconds will force system off at ACPI mode

1.3.3 Cover Switch

System automatically provides power saving by monitoring Cover Switch. It will save battery power and prolong the usage time when user closes the notebook cover.

At ACPI mode there are four functions to be chosen at windows power management control panel.

1. None
2. Standby
3. Off

Hibernate (must enable hibernate function in power management)

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1.3.4 LED Indicators

System has eight status LED indicators to display system activity, which include three at front side and five above keyboard.

❑ **Three LED indicators at the lower side of LCD Panel:**

From left to right that indicate, AC power, battery power and battery status

- *AC POWER* : This LED lights green when AC is powering the notebook, and flash (on 1 second, off 1 second) when Suspend to DRAM is active using AC power. The LED is off when the notebook is off or powered by batteries.
- *BATTERY POWER* : This LED lights green when the notebook is being powered by Battery, and flash (on 1 second, off 1second) when Suspend to DRAM is active using Battery power. The LED is off when the notebook is off or powered by batteries, or when Suspend to Disk
- *BATTERY STATUS*: During normal operation, this LED stays off as long as the battery is charged. When the battery charge drops to 10% of capacity, the LED lights red, flashes per 1 second and beeps per 2 second. When AC is connected, this indicator glows green if the battery pack is fully charged or orange (amber) if the battery is being charged

❑ **Six LED indicators at front side of system:**

- From left to right that indicates CD-ROM activity, HARD DRIVE activity, NUM LOCK, CAPS LOCK, SCROL LOCK and Wireless LAN status.

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1.3.5 Battery status

❑ **Battery Warning**

- System also provides Battery capacity monitoring and gives user a warning so that users have chance to save his data before battery dead. Also, this function protects system from mal-function while battery capacity is low
- Battery Warning: Capacity below 10%, Battery Capacity LED flashes per second, system beeps per 2 seconds
- System will suspend to HDD after 2 Minutes to protect users data

❑ **Battery Low State**

- After Battery Warning State, and battery capacity is below 4%, system will generate beep for twice per second.

❑ **Battery Dead State**

- When the battery voltage level reaches 7.4 volts, system will shut down automatically in order to extend the battery packs' life

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1.3.6 Fan power on/off management

FAN is controlled by H8 embedded controller-using AD1032 to sense CPU temperature and PWM control fan speed. Fan speed is depended on CPU temperature. Higher CPU temperature faster Fan Speed.

1.3.7 CMOS Battery

CR2032 3V 220mAh lithium battery. When AC in or system main battery inside, CMOS battery will consume no power. AC or main battery not exists, CMOS battery life at less (220mAh/5.8uA) 4 years. Battery was put in battery holder, can be replaced.

1.3.8 I/O Port

- One Power Supply Jack.
- One External CRT Connector For CRT Display
- Supports four USB ports for all USB devices.
- One MODEM RJ-11 phone jack for PSTN line
- One RJ-45 for LAN.
- Headphone Out Jack.
- Microphone Input Jack.
- Line in Jack
- One Card Bus Sockets for one type II PC card extension
- One Parallel Port for Print

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1.3.9 Battery current limit and learning.

Implanted H/W current limit and battery learning circuit to enhance protection of battery

1.4 Peripheral Components

1.4.1 LCD PANEL

- 14” TFT XGA : 1.QDI:QD141X1LH03-MP01
- 2.CHI-mei : N141X6-L01
- 3.AU : B141XN04-2(UB141X03)
- 15” TFT XGA : 1.Samsung: LTN150X3-L01-M00
  2.Hannstar:HDS150PX11-B
- 15” TFT SXGA+ : Samsung: lt150p1-L04

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1.4.2 Ext.Floppy Disk Drive

- Mitsumi D353FUE(3.5” 1.44MB /1.2 MB/720KB FDD)

1.4.3 HDD

- FujitsuI : 20GB MHR2020AT
  30GB MHR2030AT
  40GB MHR2040AT

- HITACHI : 20GB DK23DA-20
  30GB DK23DA-30
  40GB DK23DA-40
- IBM : 20GB IC25N020ATCS04-0
  30GB IC25N030ATCS04-0
  40GB IC25N040ATCS04-0

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1.4.4 24X CD-ROM Drive

- TEAC :CD-224E-C93(24X)
- QSI:SCR-242-BS(24X)

1.4.5 DVD-ROM

- QSI:SDR-083(8X)
- MKE:SR-8177-BS(8X)
- TEAC:DV-28E-B93(8X)

1.4.6 Combo Driver

- QSI: SBW-161 (16X12X8X24)
- KME: UJDA730MT (16 X 10 X 8 X 24)
- TEAC: DW-224E-B93

1.4.7 CD-RW

- MKE: UJDA-340 (8X8X24)

1.4.8 Keyboard

- JME 300 type, 19mm pitch/3.0mm stroke
- Zippy 300 type, 19mm pitch/3.0mm stroke

1.4.9 Track Pad Synaptics

- Accurate positioning
- Low fatigue pointing action
- Low profile

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- No moving part, high reliability
- Low power consumption
- Environmentally sealed
- Compact size.
- Software configurable
- Low weight
- Operating temperature: 0 to 60 degree C
- Operating humidity: 5%-95% relative humidity, non condensing
- Storage temperature: -40 to +65 degree C
- ESD: 15KV applied to front surface SEE ESD Testing specification PN 520-000270-01
- Power supply voltage: 5.0Voltage ± 10%
- Power supply current: 4.0mA max operating.

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1.4.10 Fan

- HY45J05-001

1.4.11 Memory

DDR SO-DIMM module 128/256 MB support PC2100 specification

1. Kingmax: MSDB62D-68KX2-MAA(256M), MSDA82D-68KX2-MAA (128M)
2. Apacer:77.10321.460 (128MB) ,77.10521.460 (128MB), 77.10620.110 (256MB)

1.4.12 Wireless LAN

- MiTAC Askey WLL030 Ambit

1.4.13 Modem MDC

- AC97 Link :56Kbps MDC
- Askey: V1456VQL-P1(INT)
- Castlenet: (2nd source)

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1.5 Power Management

The 8375 system has built in several power saving modes to prolong the battery usage. User can enable and configure different degrees of power management modes via ROM CMOS setup (booting by pressing F2 key). Following are the descriptions of the power management modes supported.

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1.5.1 System Management Mode

- **Full on mode**

  In this mode, each device is running with the maximal speed. CPU clock is up to its maximum.

- **Doze Mode**

  In this mode, CPU will be toggling between on & stop grant mode either. The technology is clock throttling. This can save battery power without loosing much computing capability.The CPU power consumption and temperature is lower in this mode.

- **Standby mode**

  For more power saving, it turns of the peripheral components. In this mode, the following is the status of each device:

  -- CPU: Stop grant

  -- LCD: backlight off

  -- HDD: spin down

- **Suspend to DRAM**

  The most chipset of the system is entering power down mode for more power saving. In this mode, the following is the status of each device:

  -- CPU: off

  -- Twister K: Partial off

  -- VGA: Suspend

  -- PCMCIA: Suspend

  -- Audio: off

  -- SDRAM: self refresh

- **Suspend to HDD**

  -- All devices are stopped clock and power-down

  -- System status is saved in HDD

  -- All system status will be restored when powered on again

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1.5.2 Other power management functions

- **HDD & Video access**

  System has the ability to monitor video and hard disk activity. User can enable monitoring function for video and/or hard disk individually. When there is no video and/or hard disk activity, system will enter next PMU state depending on the application. When the VGA activity monitoring is enabled, the performance of the system will have some impact.

1.6 Appendix 1: GPIO definitions

VT8235	Input/Output	Default Value	Definition
GPO0	Output		
GPO1/SUSA#			SUSA#
GPO2/SUSB #			SUSB#
GPO3/SUSST1#			SUSST#
GPO4/ SUSCLK			SUSCLK-
GPO5/CPUSTP#			CPUSTP#
GPO6/PCISTP#			PCI_STP#
GPO7/SLP#			SLP#
GPI0	Input		Reserved
GPI1	Input		Reserved
GPI2/EXTSMI#			EXTSMI#
GPI3/RING#			WAKEUP#
GPI4/LID#	Input		PME#
GPI5/BATLOW#	Input		-CARD_RI#
GPI6/PME#			SCI#
GPI7/SMBALRT#	Input		SMBALRT#
GPIO8	Input		CD_RST
GPIO9/ VRDPSLP			
GPIO10	Output	High	EN_BL
GPIO11	Output	High	SPK_OFF
GPIO12	Input		MB_ID0
GPIO13	Input		MB_ID1
GPIO14	Output	Low	MB_ID2
GPIO15	Output	Low	MPCIACT#
GPI16/ INTRUDER#	Input		
GPI17/ CPUMISS	Input		CPUMISS
GPI18/ THRM#			THRM#
GPI19/ IORDY	Input		IOCHRDY
GPIO20/ VGATE			
GPIO21/AGPBZ#	Output		
GPIO22/IOR#	Output	Low	
GPIO23/IOW#	Output	Low	
GPIO24/GPIOA	Input		
GPIO25/GPIOC	Input		

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Continue

VT8235	Input/Output	Default Value	Definition
APICD0/GPIO28	Input		
APICD1/GPIO29	Input		LCD_ID0
#GHI/GPIO30			LCD_ID1
VIDSEL/GPIO31			LCD_ID2

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1.7 Appendix 2: KBC Pins Definitions

Name	Pin	W83950D Pin Definitions	During RESET	After RESET/ OFF		ON		STANDBY		Function
CNVSS	24	GND								
Xin	28	KBC_X+	I	I		I		I		Crystal 8M
Xout	29	KBC_X-	I	I		I		I		
Vref	72	Voltage Reference								Reference voltage of AD/DA
Vss	30	GND								
AVss	73	GND								
Vcc	71	3.3v								W83950D power

8375 N/B Maintenance

PCIreset gate

Pin	W83950D Pin Definitions	During RESET	After RESET/OFF		ON		STANDBY		Function
54	KB OUT0	L	O	L	O	LH	O	Keep L	Key matrix scan output 0
53	KB OUT1	L	O	L	O	LH	O	Keep L	Key matrix scan output 1
52	KB OUT2	L	O	L	O	LH	O	Keep L	Key matrix scan output 2
51	KB OUT3	L	O	L	O	LH	O	Keep L	Key matrix scan output 3
50	KB OUT4	L	O	L	O	LH	O	Keep L	Key matrix scan output 4
49	KB OUT5	L	O	L	O	LH	O	Keep L	Key matrix scan output 5
48	KB OUT6	T	O	L	O	LH	O	Keep L	Key matrix scan output 6
47	KB OUT7	T	O	L	O	LH	O	Keep L	Key matrix scan output 7
46	KB OUT8	L	O	L	O	LH	O	Keep L	Key matrix scan output 8
45	KB OUT9	L	O	L	O	LH	O	Keep L	Key matrix scan output 9
44	KB OUT10	L	O	L	O	LH	O	Keep L	Key matrix scan output 10
43	KB OUT11	L	O	0	O	LH	O	Keep L	Key matrix scan output 11
42	KB OUT12	L	O	0	O	LH	O	Keep L	Key matrix scan output 12
41	KB OUT13	L	O	0	O	LH	O	Keep L	Key matrix scan output 13
40	KB OUT14	L	O	0	O	LH	O	Keep L	Key matrix scan output 14
39	KB OUT15	L	O	0	O	LH	O	Keep L	Key matrix scan output 15
38	THRM#	T ↑	I	H	I		I	H	Throttle on
37	WAKEUP#	T ↑	I	H/L	I		I	H/L	Wake up signal for Chipset
36	WAKEEUP#	T ↑	I	H	I		I	H	Battery LED Green
35	BATT_R#	T ↑	I	H	I		I	H	Battery LED Red
34	EXTSMI#	T ↑	I	H	I		I	L	SMI signal for chipset
33	CAP#	T ↑	I	L	I		I	H	Indicate CAPS LOCK status
32	NUM#	T ↑	I	L	I	L	I	H	Indicate NUM LOCK status
31	SCROLL#	T	I/O		I/O		I	H	Indicate SCROLL LOCK status
62	KEYIN0	T	I/O		I/O		I/O	Keep	Key matrix intput0
61	KEYIN	T	I/O		I/O		I/O	Keep	Key matrix intput1
60	KEYIN2	T	I/O		I/O		I/O	Keep	Key matrix intput2
59	KEYIN3	T	O		I/O		I/O	Keep	Key matrix intput3

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Pin	W83950D Pin Definitions	During RESET	After RESET/OFF		ON		STANDBY		Function
58	KEYIN4	T	I/O		I/O		I/O	Keep	Key matrix input 4
57	KEYIN5	T	I/O		I/O		I/O	Keep	Key matrix input 5
56	KEYIN6	T	I/O		I/O		I/O	Keep	Key matrix input 6
55	KEYIN7	T	I/O		I/O		I/O	Keep	Key matrix input 7
27	FAN ON#	T	O	L		LHL	O	Keep H	Fan control signal
26	BATT_PWR_G#	T	O	H	O		O	Keep H	Battery power Green for system on in battery mode
25	KBC_RESET#								
22	Charging	T	O	L	O		O	Keep H	Turn on Charger
23	Learning	T	O	L	O		O	Keep	Auto-learning for disable ADEN input
21	KBRESETCPU								
20	KBA20GATE	T	O	L	O	H	O	Keep	GATE 20 function
19	SCI#	T	0	L	O	H	O	Keep	SCI signal for ACPI mode
18	KBC_PWRON	T	O	L	O	LH	O	Keep H	KBC_PWRON
17	VDD3_SW#	T	O		O		O	Keep	VDD3v switch
16	LID_SW#	T	O		O		O	Keep	Cover switch
15	BATT_DEAD#	T	O		O		O	Keep	Battery Low Alarm
14	ADEN#	T	O		O		O	Keep	AC in signal
13	FAN_SPEED1	T	O		O		O	Keep	Fan speed feed back
79	AC_POWER#	T	O		O		O	Keep	Indicated LED for AC power
11	BADJ	T	O		O		O	Keep	Adjustment of Charging Voltage
10	I_CTRL	T	O		O		O	Keep	Charging current control
1	MPWRBTN	T ↑	I		I		I	Keep	Power button
80	3V	T ↑	I		I		I	Keep	System 3v
12	FAN_SPEED2	T ↑	I		I		I	Keep	Fan 2 speed feed back
78	BAT_V	T ↑	I		I		I	Keep	Battery voltage
77	BAT_TEMP	T ↑	I		I		I	Keep	Battery temperature voltage
76	I_LIMITE	T ↑	I		I		I	Keep	Current measurement
75	BUKREST	T ↑	I		I		I	Keep	Card bus reset
74	CPU_CORE_V	T ↑	I		I		I	Keep	CPU core voltage
9	T_DATA	T	I		I		I	T	Touch pad data line

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8375 N/B Maintenance

Pin	W83950D Pin Definitions	During RESET	After RESET/OFF		ON		STANDBY		Function
8	RSMRST	T	I		I		I	T	I-Limit Function
7	SB_PWRBTN	T	I		I		I	T	SB power connect to South bridge Power Button
6	T_CLK	T	I		I		I	T	Touch Pad clock line
5	SUSB#	T	I		I		I	T	System suspend signal (S3)
4	SUSC#	T	I		I		I	T	System off signal (S4,S5)
3	BAT_DAT	T	O		O		O	T	I2C data line
2	BAT_CLK	T	O		O		O	T	I2C clock line
70	LCLK	T	I		I		I	Keep	PCI clock
69	SERIRQ	T	O		O		O	Keep	Serial IRQ
68	LAD3	T	I		I		I	Keep	LPC bus bit 3
67	LAD2	T	I		I		I	Keep	LPC bus bit 2
66	LAD1	T	I		I		I	Keep	LPC bus bit 1
65	LAD0	T	I		I		I	Keep	LPC bus bit 0
64	NC	T	I		I		I	Keep	NO function
63	LFRAME	T	I/O		I/O		I/O	Keep	Start of a new LPC frame or termination of a premature frame

↑ Pull High，↓ Pull Low，5→3V Level shift

(*1): If support second fan, must have another pin to select which fan speed we want detect.

Please use south bridge GPIO to do this function.

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1.8 Appendix 3: 8375 product SPEC

1.8.1 8375 External Specifications, R0B

CPU	Mobile AMD Athlon XP/ Athlon 4/ Duron Processors with OPGA/ CPGA, 462 Socket, Support up to Mobile 45W 512K Cache Athlon XP **2800+** FSB 266MHz
Chipset	VIA VT8237(KN266) + VIA VT8235
L2 Cache	According to CPU
System BIOS	Flash EPROM (Include System BIOS and VGA BIOS) ACPI 1.0b; DMI 2.3.1 compliant
Memory	0MB SDRAM on board; Expandable to 2G B Expandable with combination of optional 128MB/256MB/512MB memory Two 200-pin DDR SDRAM Memory Module, PC 2100/1600 specifications
ROM Drive	12.7mm Height 24X CD ROM Drive 8X DVD ROM Drive 8X8x24 CD-RW or above 16X12X8X24 Combo or above
HDD	2.5" 9.5 mm height: 20/30/40GB; Support Ultra DMA 66/100 Reseller Exchangeable
Ext. FDD	Support External FDD w/z USB I/F; 3.5" Format for 720KB/1.2MB/1.44MB
Display	14.1"/ 15" XGA TFT display; Resolution: 1024x768 14.1"/15" SXGA+ TFT display; Resolution: 1280x1024 (P)
Video Controller	Pro Savage 8 GFX Integrated in KN266
Keyboard	19mm pitch/3.0mm stroke Windows Logo Key x 1; Application Key x 1
Pointing Device	Glide pad with 2x buttons and 1x scroll button
PCMCIA	Type I/II CardBus Support
Audio System	Sound Blaster Pro compatible Built-in mono microphone Support AC97 2.1 2X Speakers (1Watt each)

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I/O Port	Bi-directional Parallel Port (EPP/ECP) x 1 Standard USB2.0 port x 4 RJ-11 port x 1 RJ-45 port x 1 IR port x1, complies with IrDA 1.1 DC input x 1 VGA monitor port x1 Audio-out x 1 (SPIDF) Mic-in x 1 Hardware Volume Control IEEE1394a Port x 1 S-Video Out Port x 1 (NTSC/PAL)
Communication	Built-in 56Kbps V.90 MDC modem Built-in 10/100 based-T LAN
Power Supply	9-cell Li-ion (2000mAH/3.7V) User swappable Battery Life: 1.5 hrs Support Power off charge : 3hr ,80% in 1.6Hrs Support Power on charge : 4hr~5.5hr,
AC adapter	Universal AC adapter 90W ; Input: 100-240V, 50/60Hz AC
Dimensions	328X274X46~37(P)
Weight	3.8(P)
Accessories	Power Cord, AC Adapter, RJ-11 Phone Cable, Manual, System Driver CD-Title
Architecture	Support PC2001 Specification, Designed for Windows ME, Windows 2000 & Windows XP
Options	128MB/256MB/512MB DDR SDRAM, 9-cell Li-ION Battery Pack, AC Adapter w/o Power Cord, Notebook Carry Bag

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2. System View and Disassembly

2.1 System View

2.1.1 Front View

❶ Stereo Speaker Set
❷ Mini IEEE1394 Connector
❸ External Microphone Jack
❹ Line Out Phone Jack
❺ Volume Control
❻ Top Cover Latch

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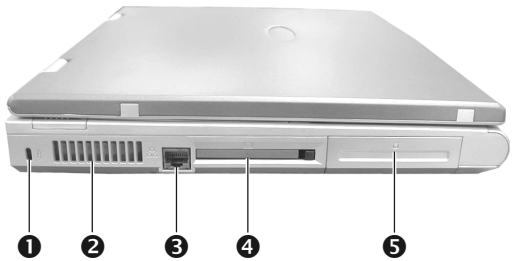
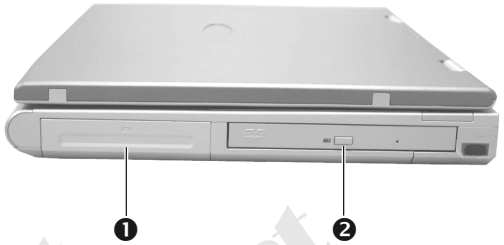
2.1.2 Left-side View

❶ Kensington Lock
❷ Ventilation Openings
❸ RJ-45 Connector
❹ PC Card Slot
❺ Hard Disk Drive



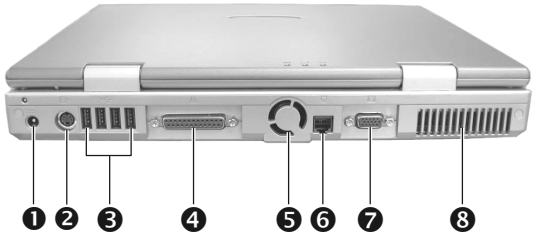
2.1.3 Right-side View

❶ Battery Pack
❷ CD-ROM/DVD-ROM Drive



2.1.4 Rear View

❶ Power Connector
❷ S-Video Output Connector
❸ USB Ports
❹ Parallel Port
❺ D/D Fan
❻ RJ-11 Connector
❼ VGA Port
❽ Ventilation Openings



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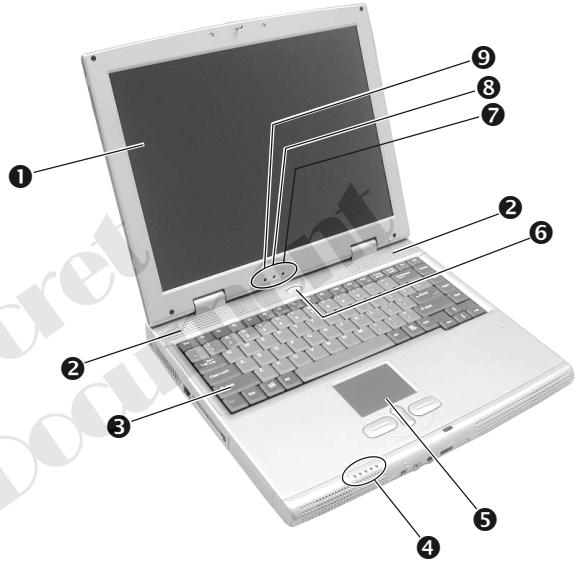
2.1.5 Top-open View

❶ LCD Screen
❷ Microphone
❸ Keyboard
❹ Device Indicators
❺ Touch Pad
❻ Power Button
❼ Battery Charge Indicator
❽ Battery Power Indicator
❾ AC Power Indicator



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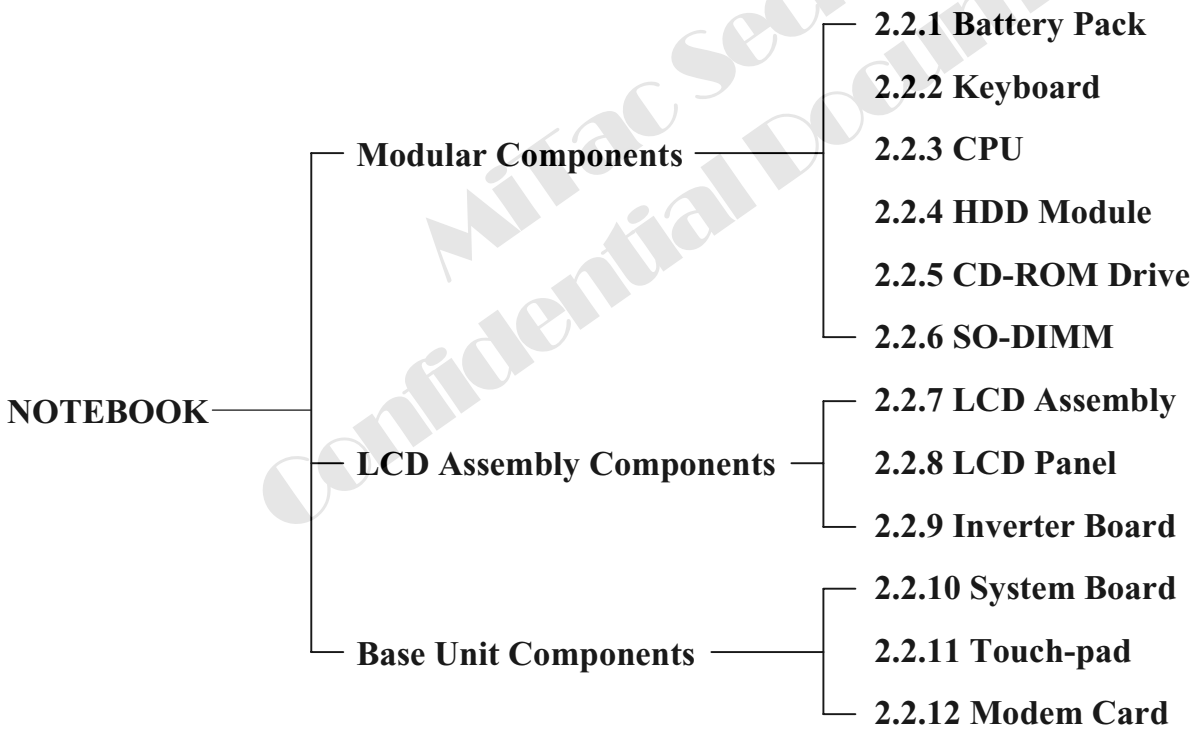
2.2 System Disassembly

The section discusses at length each major component for disassembly/reassembly and show corresponding illustrations. Use the chart below to determine the disassembly sequence for removing components from the notebook.

NOTE: *Before you start to install/replace these modules, disconnect all peripheral devices and make sure the notebook is not turned on or connected to AC power.*



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2.2.1 Battery Pack

Disassembly

1. Carefully put the notebook upside down.
2. Slide the release lever to the "unlock" ( ) position (❶), then sliding and holding the release lever outwards while pull the battery pack out of the compartment (❷). (Figure 2-1)

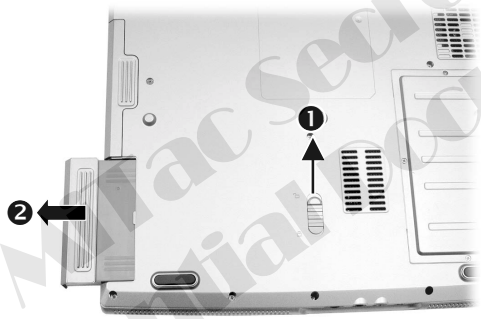

Figure 2-1 Remove the battery pack

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Reassembly

1. Push the battery pack into the compartment. The battery pack should be correctly connected when you hear a clicking sound.
2. Slide the release lever to the "lock" ( ) position.

2.2.2 Keyboard

Disassembly

1. Remove the battery pack. (See section 2.2.1disassembly)
2. Open the top cover.
3. Insert a small rod, such as a straightened paper clip, into the eject hole near the power connector of the notebook. (Figure 2-2)

Figure 2-2 Insert a rod into the hole

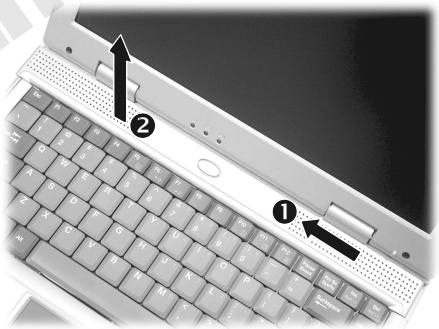

Figure 2-3 Remove Keyboard cover

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4. Push the rod firmly and slide the keyboard cover toward left (❶). Then lift the keyboard cover up (❷). (Figure 2-3)

5. Remove three screws fastening the keyboard. (Figure 2-4)
6. To detach the keyboard, slightly lift up the keyboard and disconnect the cable from the system board. (Figure 2-5)

Figure 2-4 Remove three screws

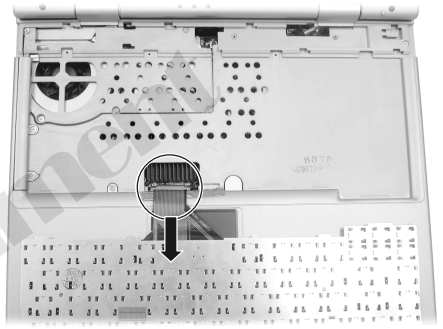

Figure 2-5 Remove keyboard

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Reassembly

1. Reconnect the keyboard cable and fit the keyboard back into place with three screws.
2. Turn the three screws to the right to tighten the keyboard.
3. Replace the keyboard cover.
4. Replace the battery pack. (See section 2.2.1 reassembly)

2.2.3 CPU

Disassembly

1. Remove the battery pack. (See section 2.2.1disassembly)
2. Remove the keyboard cover and keyboard to access the CPU compartment. (See section 2.2.2 Disassembly)
3. Remove two screws fastening the rail (Dummy cover). (Figure 2-6)

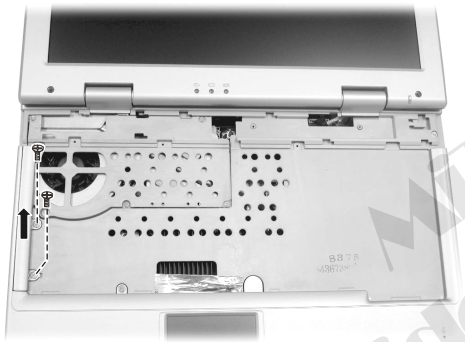

Figure 2-6 Remove the rail

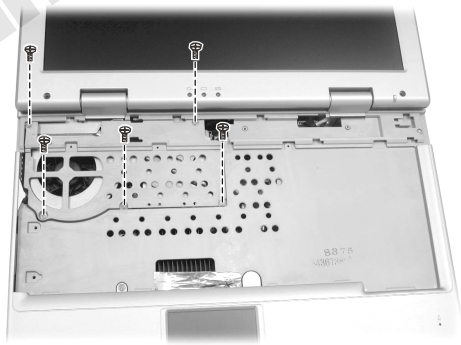

Figure 2-7 Remove the heatsink cover

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4. Remove five screws fastening the heatsink cover (KB Plate). (Figure 2-7)

5. Remove four screws fastening the headsink. (Figure 2-8)

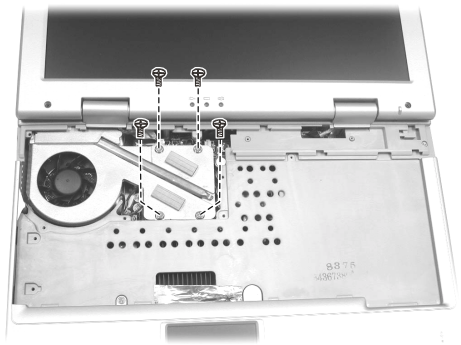

Figure 2-8 Remove the fan's power cord

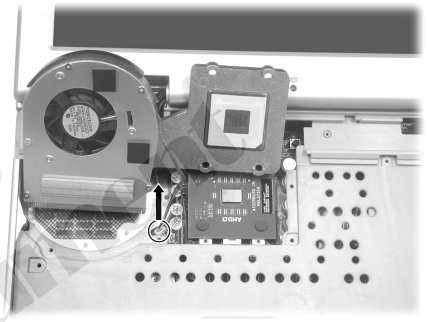

Figure 2-9 Remove the CPU

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6. Disconnect the fan's power cord from the system board, then take the heatsink away. (Figure 2-9)

7. Loosen the screw by a flat screwdriver,upraise the CPU socket to unlock the CPU. (Figure 2-10)

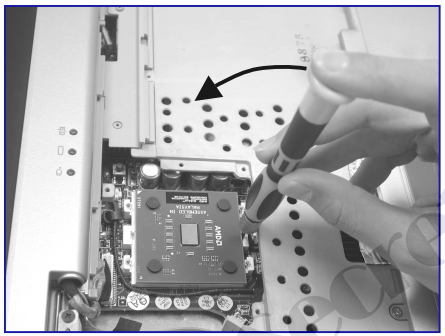

Figure 2-10 Remove the CPU

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Reassembly

1. Carefully, align the arrowhead corner of the CPU with the beveled corner of the socket, then insert CPU pins into the holes. Tighten the screw by a flat screwdriver to locking the CPU.
2. Connect the fan's power cord to the system board, fit the heatsink onto the top of the CPU and secure with four screws.
3. Replace the keyboard and battery pack. (See section 2.2.2 and 2.2.1 reassembly))

2.2.4 HDD Module

Disassembly

1. Carefully put the notebook upside down.
2. Remove the battery pack. (See section 2.2.1 disassembly)
3. Remove one screw and slide the HDD module out of the compartment. (Figure 2-11)
4. Remove six screws to separate the hard disk drive from the metal bracket. (Figure 2-12)

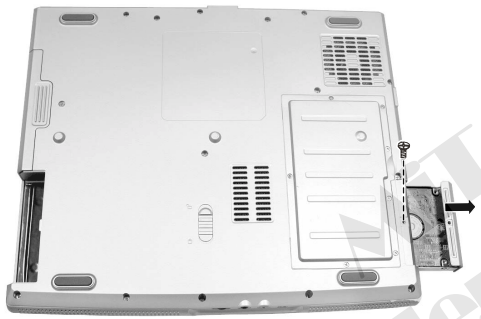

Figure 2-11 Remove HDD module

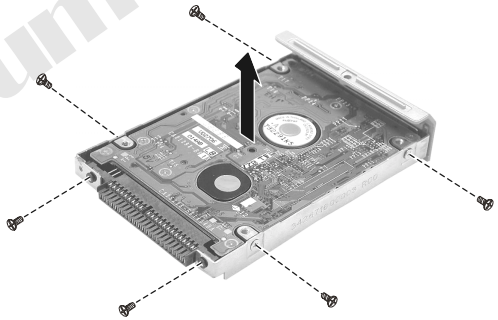

Figure 2-12 Disassemble the hard disk

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Reassembly

1. To install the hard disk drive, place it in the bracket and secure with six screws.
2. Slide the HDD module into the compartment and secure with one screw.
3. Replace the battery pack. (See section 2.2.1 reassembly)

2.2.5 CD/DVD-ROM Drive

Disassembly

1. Carefully put the notebook upside down.
2. Remove the battery pack. (See section 2.2.1disassembly)
3. Remove one screw fastening the CD/DVD-ROM drive. Then hold the CD/DVD-ROM drive and slide it outwards carefully. (Figure 2-13)

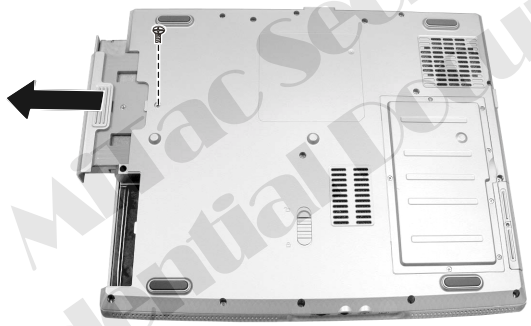

Figure 2-13 the CD/DVD-ROM drive

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Reassembly

1. Slide the CD/DVD-ROM drive back into the compartment.
2. Secure the CD/DVD-ROM drive with one screw.
3. Replace the battery pack. (See section 2.2.1 reassembly)

2.2.6 SO-DIMM

Disassembly

1. Carefully put the notebook upside down. And then remove the battery pack. (See section 2.2.1disassembly)
2. Remove seven screws to access the SO-DIMM socket. (Figure 2-14)
3. Full the retaining clips outwards (❶) and remove the SO-DIMM (❷). (Figure 2-15)

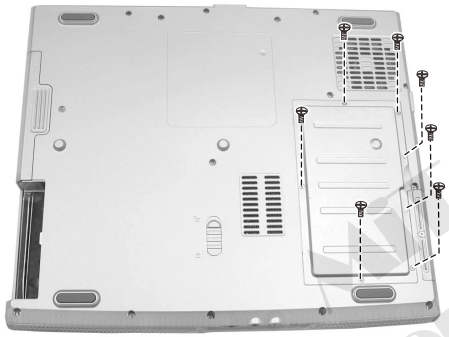

Figure 2-14 Remove the SO-DIMM cover

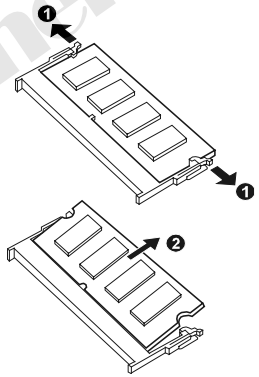

Figure 2-15 Remove the SO-DIMM

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Reassembly

1. To install the SO-DIMM, match the SO-DIMM's notched part with the socket's projected part and firmly insert the SO-DIMM into the socket at 20-degree angle. Then push down until the retaining clips lock the SO-DIMM into cover.
2. Replace the SO-DIMM socket cover and secure with seven screws.
3. Replace the battery pack. (See section 2.2.1 reassembly)

2.2.7 LCD

Disassembly

1. Remove the battery pack, keyboard and headsink. (See section 2.2.1 to 2.2.3 disassembly)
2. Carefully put the notebook upside down and remove seven screws to access the SO-DIMM socket.
3. Rip the insulating tape off to free the antenna that near the Mini-PCI socket.(Figure 2-16)

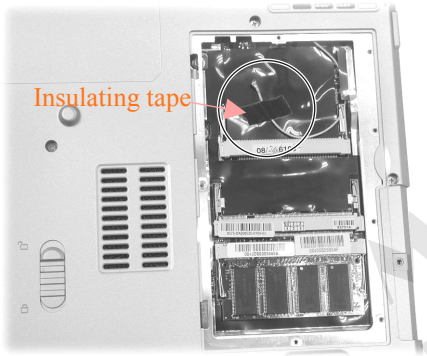

Figure 2-16 Peel of the insulating tape

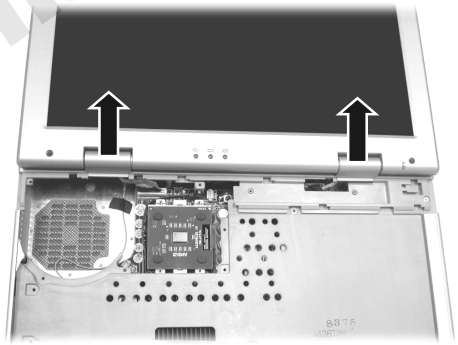

Figure 2-17 Remove the LCD hinge covers

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4. Open the top cover.
5. Remove the two hinge covers. (Figure 2-17)

6. Disconnect the two LCD cables from the system board, and remove four screws of the hinges. (Figure 2-18)
7. Rip the insulating tape off and pull out the antenna. Now you can detach the LCD assembly from the base unit. (Figure 2-18)

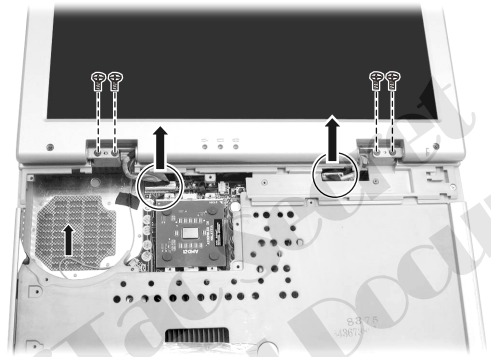

Figure 2-18 Remove the LCD ASSY

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Reassembly

1. Attach the LCD assembly and secure with four screws on the hinges.
2. Reconnect the LCD cables to the system board.
3. Insert the antenna through the CPU compartment to the SO-DIMM compartment and cling the antenna by insulating tape.
4. Replace two hinge covers.
5. Replace the heatsink, keyboard and battery pack. (See sections 2.2.3 to 2.2.1 reassembly)

2.2.8 LCD Panel

Disassembly

1. Remove the battery, keyboard, headsink and LCD assembly. (See sections 2.2.1 to 2.2.3 and 2.2.7 Disassembly)
2. Remove the four rubber pads and two screws on the lower part of the panel. (figure 2-19)
3. Insert a flat screwdriver to the lower part of the LCD cover and gently pry the cover out. Repeat the process until the cover is completely separated from the housing.
4. Remove the two screws on two sides and two screws on the lower part of the LCD panel, and disconnect the cable from the inverter board. (figure 2-20)

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Figure 2-19 Remove LCD frame

Figure 2-20 Remove LCD panel

Reassembly

1. Fit the LCD panel back into place and secure with four screws, and reconnect the cable to the inverter board.
2. Fit the LCD cover back into the housing and replace the four screws and four rubber pads.
3. Replace the LCD assembly, headsink, keyboard and battery pack. (See sections 2.2.7, 2.2.3 to 2.2.1 reassembly)

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2.2.9 Inverter Board

Disassembly

1. Remove the battery pack, keyboard, headsink. (See sections 2.2.1 to 2.2.3 disassembly)
2. Remove the LCD assembly and detach the LCD cover. (See instructions in previous two sections)
3. To remove the inverter board on the bottom side of the LCD assembly, disconnect the cable and remove one screw. (figure 2-21)

Figure 2-21 Remove the inverter board

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Reassembly

1. Fit the inverter board back into place and secure with one screw.
2. Reconnect the cable.
3. Replace the LCD cover. (See the step 1– 3 of section 2.2.8 Reassembly)
4. Replace the LCD assembly, headsink, keyboard and battery pack. (See sections 2.2.7, 2.2.3 to 2.2.1 reassembly)

2.2.10 System Board

Disassembly

1. Remove the battery pack, keyboard, CPU, HDD module, CD/DVD-ROM drive and LCD assembly. (See instructions in previous sections)
2. Remove seven screws fastening the cover Assy. (Figure 2-22)

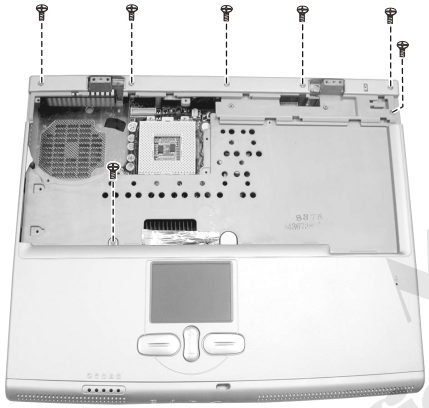

Figure 2-22 Remove the bottom

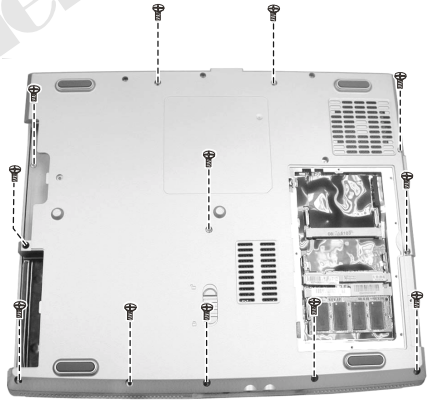

Figure 2-23 Remove the twelve screws

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3. Remove twelve screws also fastening the cover Assy on the bottom of housing. (figure 2-23)

4. Lift up the cover Assy and disconnect the touch pad cord. (Figure 2-24)

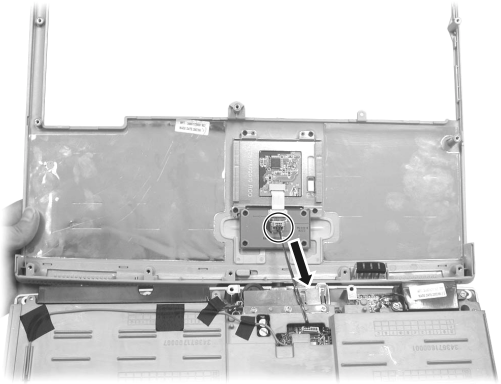

Figure 2-24 Remove the base unit cover

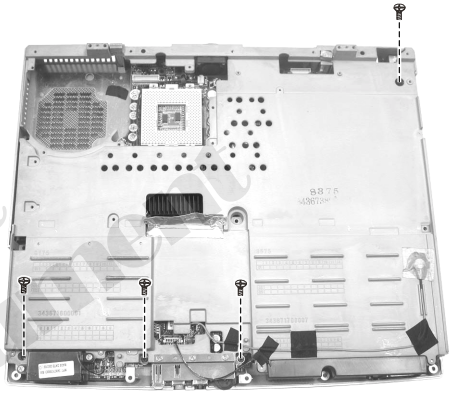

Figure 2-25 Remove the four screws

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5. Remove four screws fastening the gasket with system board in the housing. (Figure 2-25)

6. Remove two screws fastening the gasket with system board too. Now separate the housing. (Figure 2-26)

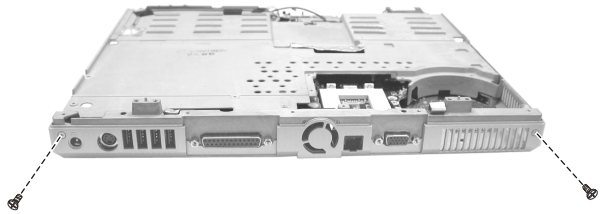

Figure 2-26 Remove two screws

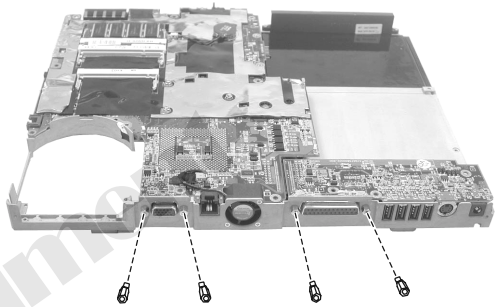

Figure 2-27 Remove the system board

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7. Remove four hex nuts on the rear of the notebook. (Figure 2-27)

8. Carefully turnover it. To detach the audio shielding , remove the three screws fastening it. (Figure 2-28)

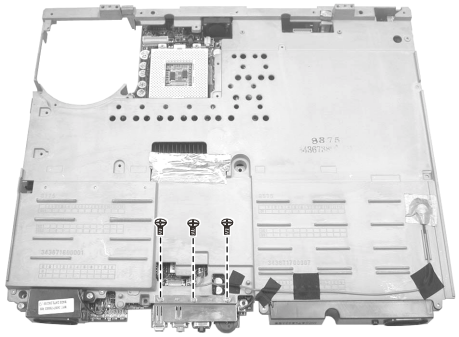

Figure 2-28 Remove the audio shielding

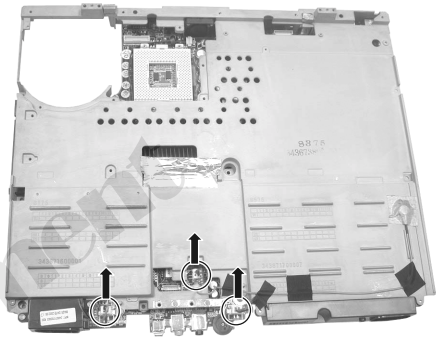

Figure 2-29 Disconnect three wires

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9. Disconnect three wires from system board. (Figure 2-29)

10. Carefully turnover it again. Remove four screws fastening the system on the gasket. (Figure 2-30)

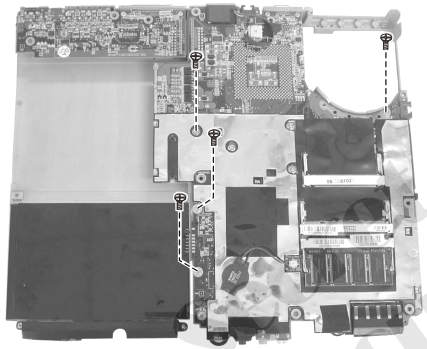

Figure 2-30 Remove the system board

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Reassembly

1. Replace the system board and secure with four screws.
2. Reconnect three wires to system board. Then secure the audio shielding by three screws.
3. Replace the housing , Turn the two screws and four hex nuts to the right to tighten the system board and gasket.
4. Replace the four screws. Then hold the cover Assy and reconnect the cord to touchpad board.
5. Replace the cover Assy and secure with seven screws.
8. Carefully put the notebook upside down. Secure the base unit by twelve screws.
9. Replace the battery pack, keyboard, CPU, HDD module, CD/DVD-ROM drive and LCD assembly. (See instructions in previous sections reassembly)

2.2.11 Touch-pad

Disassembly

1. Remove the battery pack, keyboard, CPU, CD/DVD-ROM drive and LCD assembly. (See sections 2.2.1 to 2.2.3, 2.2.5 and 2.2.7 disassembly)
2. Remove the cover Assy. (See steps 1-4 in section 2.2.10 Disassembly.)
3. Remove the eight screws to lift up the touch pad holder and touch pad panel. (Figure 2-31)

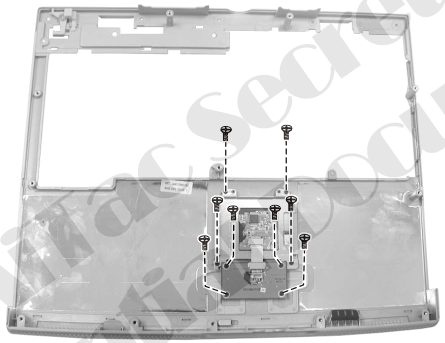

Figure 2-31 Remove the touch-pad

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Reassembly

1. Replace the touch-pad holder and touch-pad panel, and secure with eight screws.
2. Assemble the cover Assy. (See section 2.2.10 Reassembly)
3. Replace the LCD assembly, CD/DVD-ROM drive, CPU, keyboard, battery pack. (See instructions in previous sections reassembly)

2.2.12 Modem Card

Disassembly

1. Remove the battery pack, keyboard, CPU, HDD module, CD/DVD-ROM drive, and LCD assembly. (See section 2.2.1 to 2.2.5 and 2.2.7 Disassembly)
2. Disassemble the notebook to access the system board. (See section 2.2.10 Disassembly)
3. Remove the two screws fastening the modem card,and then disconnect the cable from system board. (Figure 2-32)

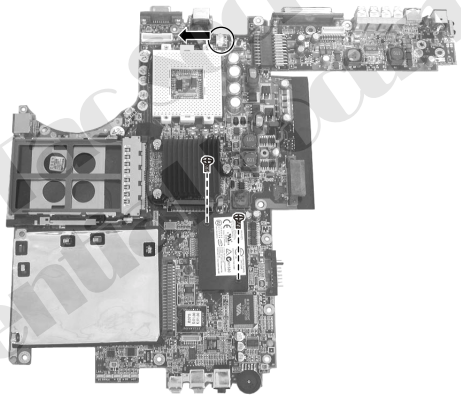

Figure 2-32 Remove the Modem card

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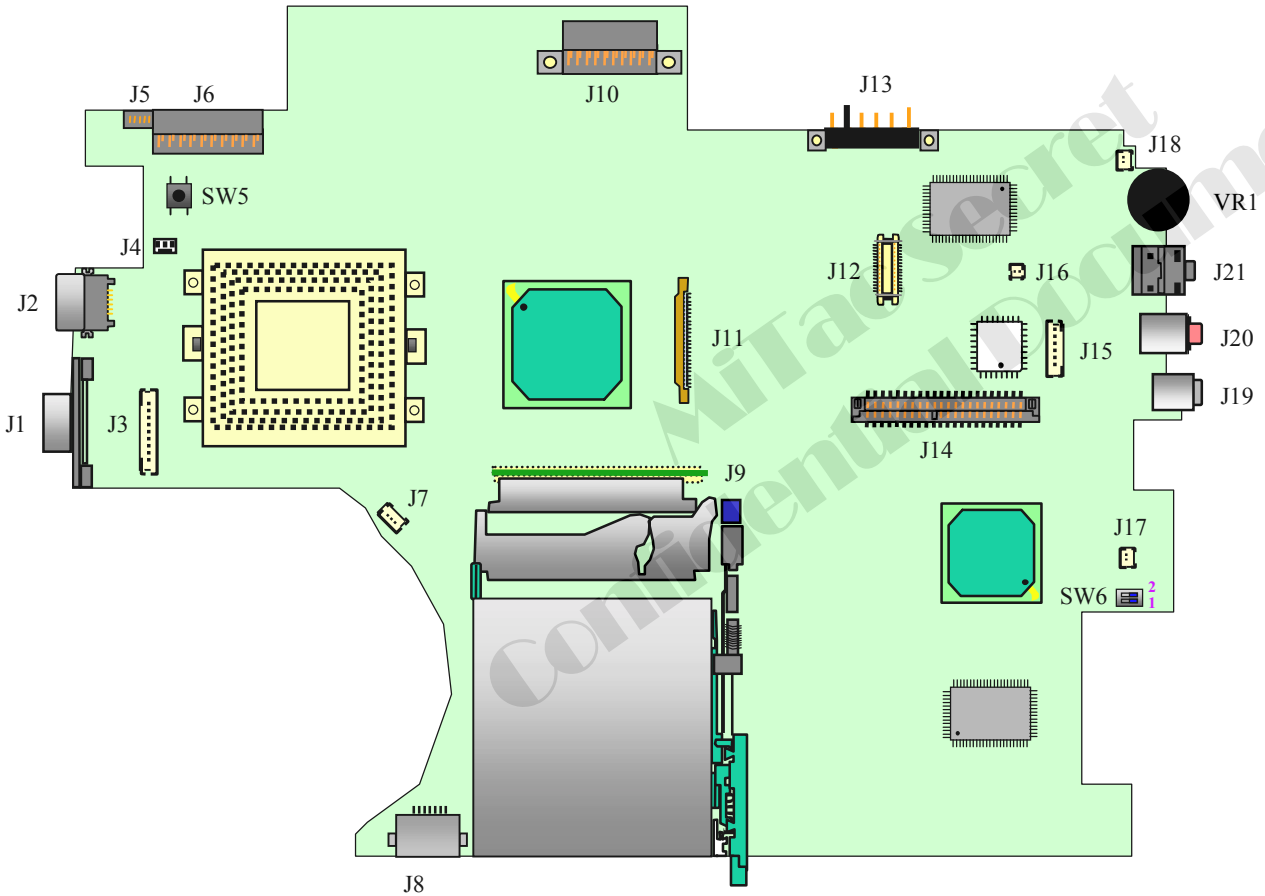
Reassembly

1. Reconnect the cable to the modem card and secure the modem card with two screws.
2. Assemble the notebook. (See section 2.2.10 Reassembly)

3. Definition & Location of Components / Switches

3.1 Mother Board (Side A-1)



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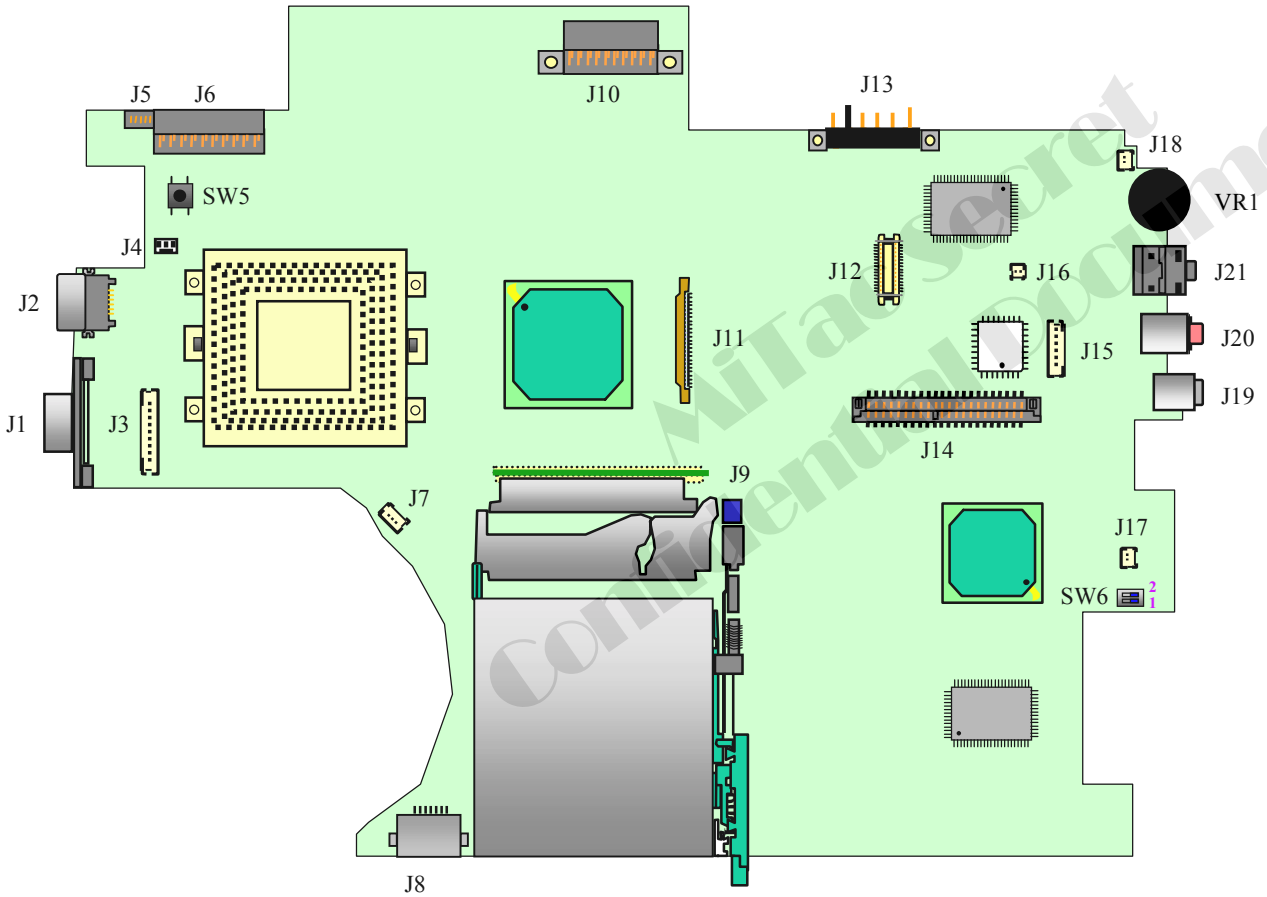
- J1: External VGA Connector
- J2 : Modem Connector (RJ11)
- J3 : LCD Connector
- J4 : MDC Jump Wire Connector
- J5 : MISC Connector
- J6 : D/D Board Connector
- J7 : CPU Fan Connector
- J8 : LAN Connector (RJ45)
- J9 : PC Card Socket
- J10 : Secondary IDE Connector
- J11 : Internal Keyboard Connector
- J12 : MDC Connector
- J13 : External Battery Connector
- J14 : Primary IDE Connector
- J15 : Touch-pad Connector

Continue to the next page

3. Definition & Location of Components / Switches

3.1 Mother Board (Side A-2)



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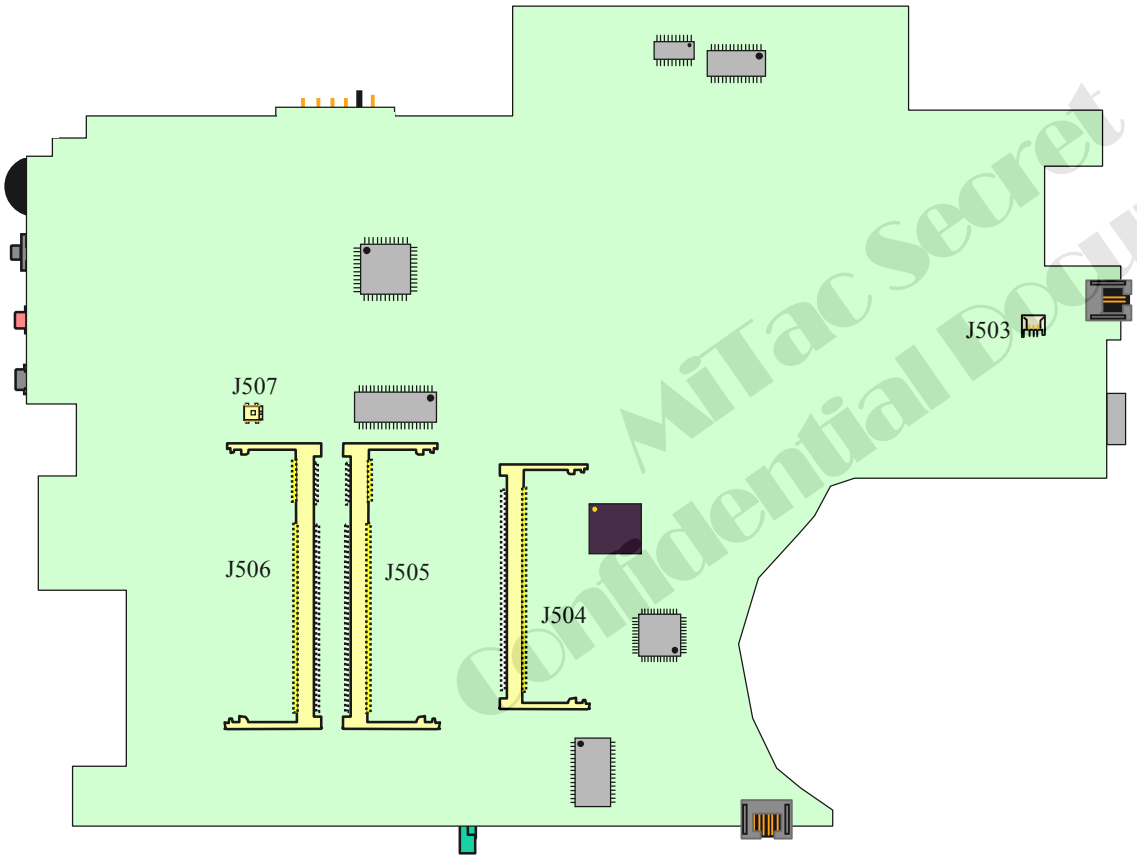
Continue from previous page

- J16 : Internal Micro Phone Jack
- J17 : L Speaker Connector
- J18 : R Speaker Connector
- J19 : IEEE1394 Port
- J20 : External Microphone Jack
- J21 : Line Out Phone Jack

- VR1 : Volume Control
- SW5 : Power Button
- SW6 : System CLK Frequency Select Jump

3. Definition & Location of Connectors / Switches

3.1 Mother Board (Side B)



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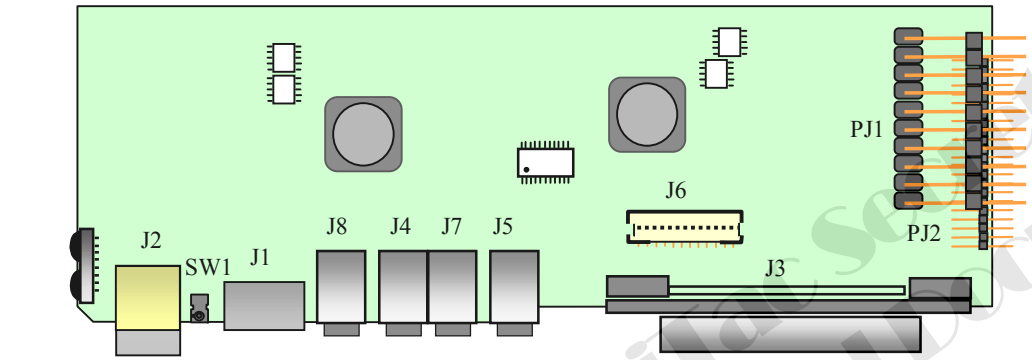
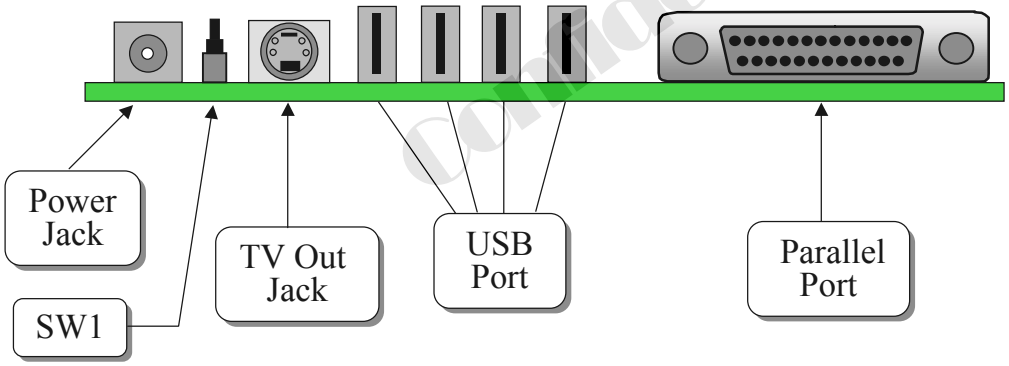
- J503 : Fan Connector
- J504 : Mini PCI Socket
- J505 : 200-pin Expansion DDR SDRAM Socket
- J506 : 200-pin Expansion DDR SDRAM Socket
- J507 : CMOS Battery Connector

3. Definition & Location of Connectors / Switches

3.2 DC Power Board





- J1 : TV Out Jack
- J2 : Power Jack (AC Adapter)
- J3 : Parallel Port Connector
- J4 : USB Port Connector
- J5 : USB Port Connector
- J6 : Invert Board Connector
- J7 : USB Port Connector
- J8 : USB Port Connector
- PJ1 : D/D Connector
- PJ2 : MISC Connector

- SW1 : Cover Switch

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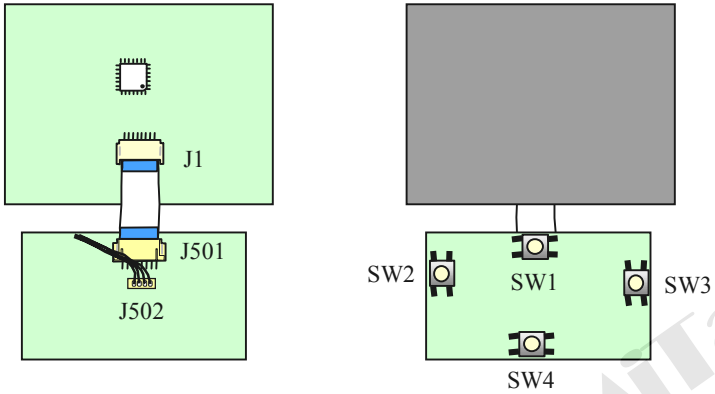
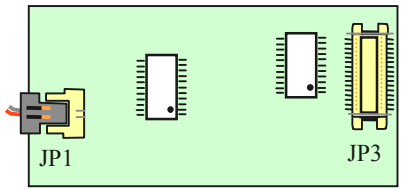
3. Definition & Location of Connectors / Switches

3.3 Touch-pad – A,B



- J1 : Touch-pad to Touch-pad Board Connector
- J501 : Touch-pad Board to Touch-pad Connector
- J502 : Touch-pad Board to Main Board Connector
- SW1 : Scroll Up Button Switch
- SW2 : Left Button Switch
- SW3 : Right Button Switch
- SW4 : Scroll Down Button Switch

3.4 Daughter Board



- JP1 : MDC Jump Wire Connector
- JP3 : MDC/LAN Transfer Board to M/B Connector

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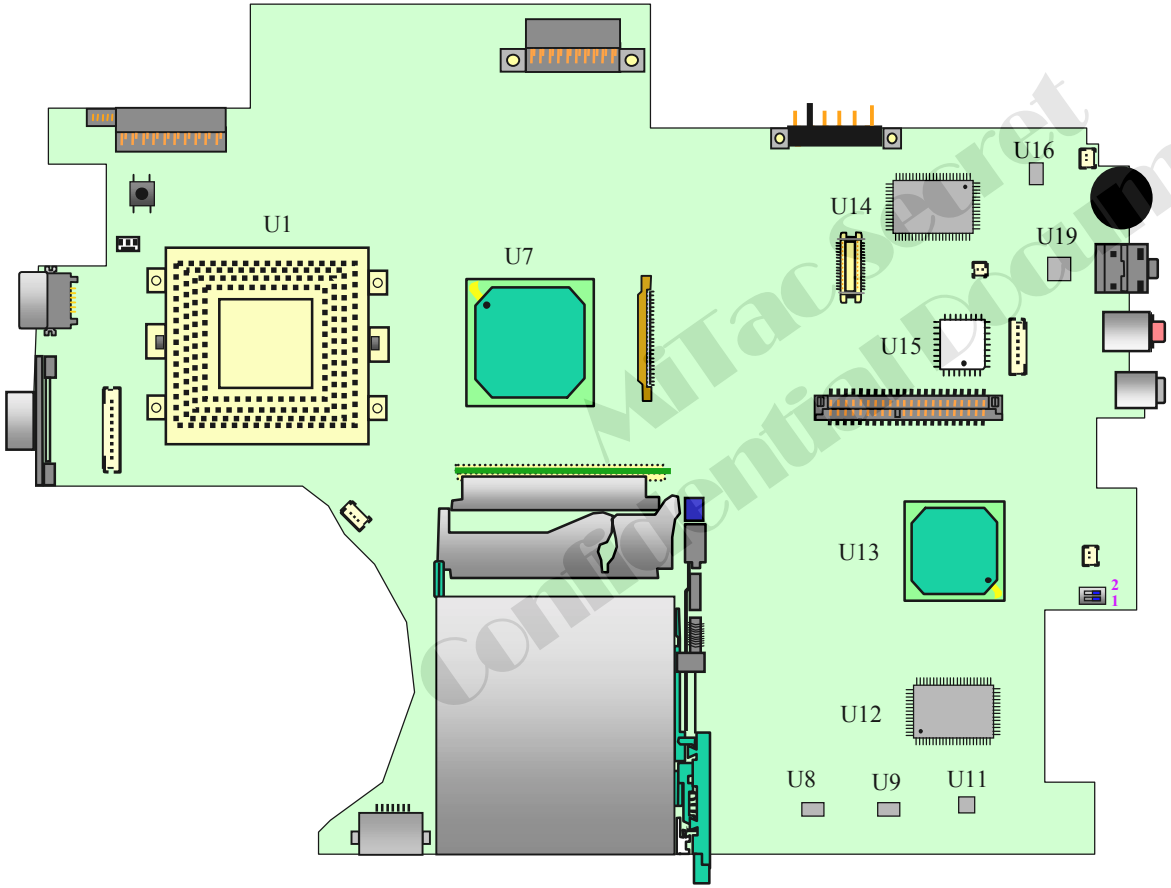
4. Definition & Location of Major Components

4.1 Mother Board –(Side A)



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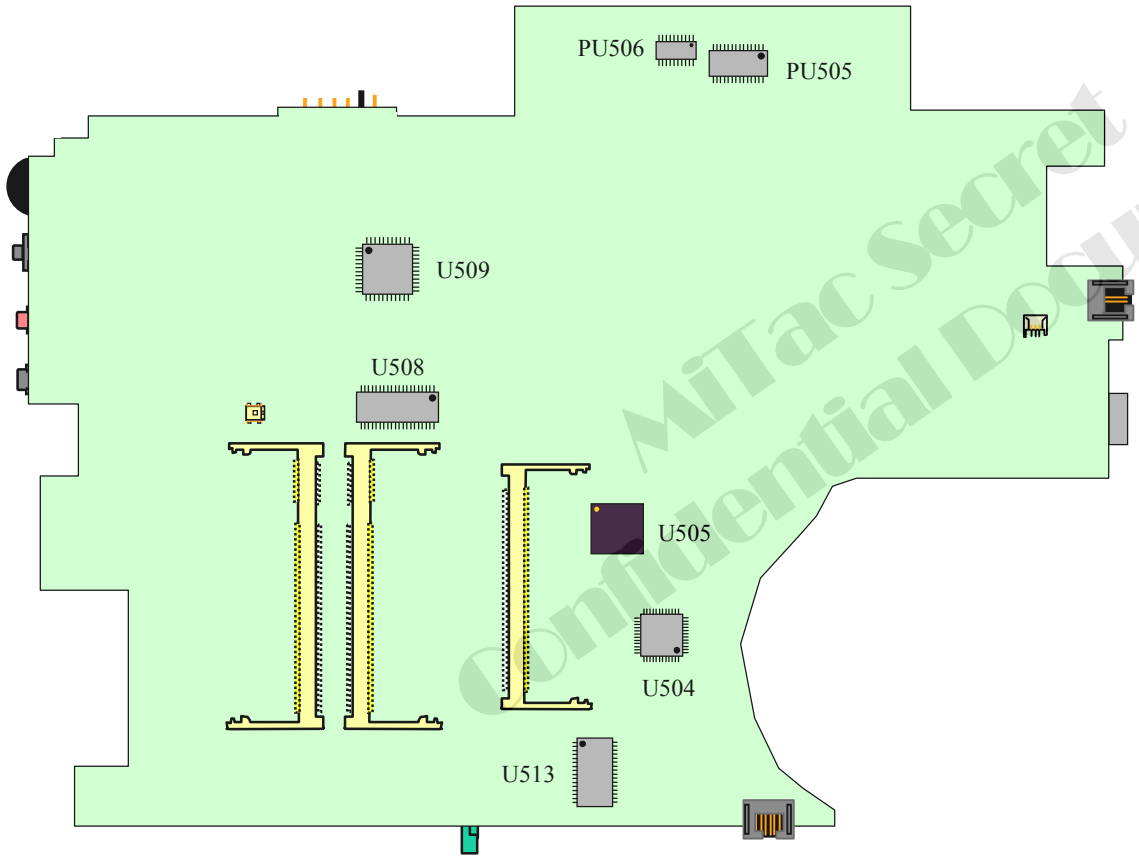
- U1: CPU Socket
- U7 : VT8372 North Bridge
- U8 : 7408_V SO14
- U9 : 7404_V1 SO14
- U11 : NM93C46 SO8
- U12 : VT6306L IEEE1394 Controller
- U13 : VT8235 South Bridge
- U14 : VT1211 Super I/O Controller
- U15 : Flash ROM
- U16 : APA2020A Audio Amplifier
- U19 : VT1612A Audio CODEC

4. Definition & Location of Major Components

4.1 Mother Board (Side B)



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- U504 : VT1622 TV ENCODER
- U505 : CB-1410 PCMCIA Controller
- U508 : Clock Generator
- U509 : W83L950D Keyboard Controller
- U513 : VT6103 LAN Controller
- PU506 : LTC3707 2.5V Generator
- PU505 : 1709EG-7 CPU_CORE Generator

5. Pin Descriptions of Major Components

5.1 AMD Athlon™ XP Processor Model 8 OPGA462Pin

Detailed Pin Descriptions

Name	Description
A20M# Pin	A20M# is an input from the system used to simulate address wrap-around in the 20-bit 8086.
AMD Pin	AMD Socket A processors do not implement a pin at location AH6. All Socket A designs must have a top plate or cover that blocks this pin location. When the cover plate blocks this location, a non-AMD part (e.g., PGA370) does not fit into the socket. However, socket manufacturers are allowed to have a contact loaded in the AH6 position. Therefore, motherboard socket design should account for the possibility that a contact could be loaded in this position.
AMD Athlon™ System Bus Pins	See the *AMD Athlon™ System Bus Specification*, order# 21902 for information about the system bus pins—PROCRDY, PWROK, RESET#, SADDIN[14:2]#, SADDINCLK#, SADDOUT[14:2]#, SADDOUTCLK#, SDATA[63:0]#, SDATAINCLK[3:0]#, SDATAINVALID#, SDATAOUTCLK[3:0]#, SDATAOUTVALID#, SFILLVALID#.
Analog Pin	Treat this pin as a NC.
APIC Pins, PICCLK, PICD[1:0]#	The Advanced Programmable Interrupt Controller (APIC) is a feature that provides a flexible and expandable means of delivering interrupts in a system using an AMD processor. The pins, PICD[1:0], are the bi-directional message-passing signals used for the APIC and are driven to the Southbridge or a dedicated I/O APIC. The pin, PICCLK, must be driven with a valid clock input.
CLKFWDRST Pin	CLKFWDRST resets clock-forward circuitry for both the system and processor.
CLKIN, RSTCLK (SYSCLK) Pins	Connect CLKIN with RSTCLK and name it SYSCLK. Connect CLKIN# with RSTCLK# and name it SYSCLK#. Length match the clocks from the clock generator to the Northbridge and processor.
CONNECT Pin	CONNECT is an input from the system used for power management and clock-forward initialization at reset.
COREFB and COREFB# Pins	COREFB and COREFB# are outputs to the system that provide processor core voltage feedback to the system.
CPU_PRESENCE# Pin	CPU_PRESENCE# is connected to VSS on the processor package. If pulled-up on the motherboard, CPU_PRESENCE# may be used to detect the presence or absence of a processor in the Socket A-style socket.
DBRDY and DBREQ# Pins	DBRDY and DBREQ# are routed to the debug connector. DBREQ# is tied to VCC_CORE with a pullup resistor.
FERR Pin	FERR is an output to the system that is asserted for any unmasked numerical exception independent of the NE bit in CR0. FERR is a push-pull active High signal that must be inverted and level shifted to an active Low signal. For more information about FERR and FERR#, see the "Required Circuits" chapter of the *AMD Athlon™ Processor-Based Motherboard Design Guide*, order# 24363.

Detailed Pin Descriptions Cotinue

Name	Description
FLUSH# Pin	FLUSH# must be tied to VCC_CORE with a pullup resistor. If a debug connector is implemented, FLUSH# is routed to the debug connector.
IGNNE# Pin	IGNNE# is an input from the system that tells the processor to ignore numeric errors.
INIT# Pin	INIT# is an input from the system that resets the integer registers without affecting the floating-point registers or the internal caches. Execution starts at 0_FFFF_FFF0h.
INTR Pin	INTR is an input from the system that causes the processor to start an interrupt acknowledge transaction that fetches the 8-bit interrupt vector and starts execution at that location.
JTAG Pins	TCK, TMS, TDI, TRST#, and TDO are the JTAG interface. Connect these pins directly to the motherboard debug connector. Pull TDI, TCK, TMS, and TRST# up to VCC_CORE with pullup resistors.
K7CLKOUT and K7CLKOUT# Pins	K7CLKOUT and K7CLKOUT# are each run for two to three inches and then terminated with a resistor pair: 100 ohms to VCC_CORE and 100 ohms to VSS. The effective termination resistance and voltage are 50 ohms and VCC_CORE/2.
Key Pins	These 16 locations are for processor type keying for forwards and backwards compatibility (G7, G9, G15, G17, G23, G25, N7, Q7, Y7, AA7, AG7, AG9, AG15, AG17, AG27, and AG29). Motherboard designers should treat key pins like NC (No Connect) pins. A socket designer has the option of creating a top mold piece that allows PGA key pins only where designated. However, sockets that populate all 16 key pins must be allowed, so the motherboard must always provide for pins at all key pin locations.
NC Pins	The motherboard should provide a plated hole for an NC pin. The pin hole should not be electrically connected to anything.
NMI Pin	NMI is an input from the system that causes a non-maskable interrupt.
PGA Orientation Pins	No pin is present at pin locations A1 and AN1. Motherboard designers should not allow for a PGA socket pin at these locations. For more information, see the *AMD Athlon™ Processor-Based Motherboard Design Guide*, order# 24363.
PLL Bypass and Test Pins	PLLTEST#, PLLBYPASS#, PLLMON1, PLLMON2, PLLBYPASSCLK, and PLLBYPASSCLK# are the PLL bypass and test interface. This interface is tied disabled on the motherboard. All six pin signals are routed to the debug connector. All four processor inputs (PLLTEST#, PLLBYPASS#, PLLMON1, and PLLMON2) are tied to VCC_CORE with pullup resistors.

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5.1 AMD Athlon™ XP Processor Model 8 OPGA462Pin

Detailed Pin Descriptions Cotinue

Name	Description
FID[3:0] Pins	FID[3] (Y3), FID[2] (Y1), FID[1] (W3), and FID[0] (W1) are the 4-bit processor clock-to-SYSCLK ratio. **FID[3:0] Clock Multiplier Encodings** **FID[3:0]**[2] / **Processor Clock to SYSCLK Frequency Ratio** 0000 — 11 0001 — 11.5 0010 — 12 0011 — ≥12.5[1] 0100 — 5 0101 — 5.5 0110 — 6 0111 — 6.5 1000 — 7 1001 — 7.5 1010 — 8 1011 — 8.5 1100 — 9 1101 — 9.5 1110 — 10 1111 — 10.5 ***Notes:*** *1. All ratios greater than or equal to 12.5x have the same FID[3:0] code of 0011b, which causesthe SIP configuration for all ratios of 12.5x or greater to be the same.* *2. BIOS initializes the CLK_Ctl MSR during the POST routine. This CLK_Ctl setting is used with all FID combinations and selects a Halt disconnect divisor and a Stop Grant disconnect divisor. For more information, refer to the* AMD Athlon™ and AMD Duron™ Processors BIOS, Software, and Debug Developers Guide*, order# 21656.* The FID[3:0] signals are open-drain processor outputs that are pulled High on the motherboard and sampled by the chipset to determine the SIP (Serialization Initialization Packet) that is sent to the processor. The FID[3:0] signals are valid after PWROK is asserted. The FID[3:0]signals must not be sampled until they become valid. See the *AMD Athlon™ System Bus Specification*, order# 21902 for more information about Serialization Initialization Packets and SIP protocol. The processor FID[3:0] outputs are open-drain and 2.5 V tolerant. To prevent damage to the processor, if these signals are pulled High to above 2.5 V, they must be electrically isolated from the processor. For information about the FID[3:0] isolation circuit, see the *AMD Athlon™ Processor-Based Motherboard Design Guide*, order# 24363.

Detailed Pin Descriptions Cotinue

Name	Description
PLL Bypass and Test Pins	PLLTEST#, PLLBYPASS#, PLLMON1, PLLMON2, PLLBYPASSCLK, and PLLBYPASSCLK# are the PLL bypass and test interface. This interface is tied disabled on the motherboard. All six pin signals are routed to the debug connector. All four processor inputs (PLLTEST#, PLLBYPASS#, PLLMON1, and PLLMON2) are tied to VCC_CORE with pullup resistors.
PWROK Pin	The PWROK input to the processor must not be asserted until all voltage planes in the system are within specification and all system clocks are running within specification.
SADDIN[1:0]# and SADDOUT[1:0]# Pins	The AMD Athlon XP processor model 8 does not support SADDIN[1:0]# or SADDOUT[1:0]#. SADDIN[1]# is tied to VCC with pullup resistors, if this bit is not supported by the Northbridge (future models can support SADDIN[1]#). SADDOUT[1:0]# are tied to VCC with pullup resistors if these pins are supported by the Northbridge. For more information, see the *AMD Athlon™ System Bus Specification*, order# 21902.
Scan Pins	SCANSHIFTEN, SCANCLK1, SCANINTEVAL, and SCANCLK2 are the scan interface. This interface is AMD internal and is tied disabled with pulldown resistors to ground on the motherboard.
SMI# Pin	SMI# is an input that causes the processor to enter the system management mode.
STPCLK# Pin	STPCLK# is an input that causes the processor to enter a lower power mode and issue a Stop Grant special cycle.
SYSCLK and SYSCLK#	SYSCLK and SYSCLK# are differential input clock signals provided to the PLL of the processor from a system-clock generator.
THERMDA and THERMDC Pins	Thermal Diode anode and cathode pins are used to monitor the actual temperature of the processor die, providing more accurate temperature control to the system.
VCCA Pin	VCCA is the processor PLL supply.
VREFSYS Pin	VREFSYS (W5) drives the threshold voltage for the system bus input receivers. The value of VREFSYS is system specific. In addition, to minimize VCC_CORE noise rejection from VREFSYS, include decoupling capacitors. For more information, see the *AMD Athlon™ Processor-Based Motherboard Design Guide*, order# 24363.
ZN and ZP Pins	ZN (AC5) and ZP (AE5) are the push-pull compensation circuit pins. In Push-Pull mode (selected by the SIP parameter SysPushPull asserted), ZN is tied to VCC_CORE with a resistor that has a resistance matching the impedance Z0 of the transmission line. ZP is tied to VSS with a resistor that has a resistance matching the impedance Z0 of the transmission line.

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5.1 AMD Athlon™ XP Processor Model 8 OPGA462Pin

Detailed Pin Descriptions Cotinue

<table>
<tr><th>Name</th><th>Description</th></tr>
<tr><td>VID[4:0] Pins</td><td>The VID[4:0] (Voltage Identification) outputs are used to dictate the VCC_CORE voltage level. The VID[4:0] pins are strapped to ground or left unconnected on the processor package. The VID[4:0] pins are pulled-up on the motherboard and used by the VCC_CORE DC/DC converter.
VID[4:0] Code to Voltage Definition
<table>
<tr><th>VID[4:0]</th><th>VCC_CORE (V)</th><th>VID[4:0]</th><th>VCC_CORE (V)</th></tr>
<tr><td>00000</td><td>1.850</td><td>10000</td><td>1.450</td></tr>
<tr><td>00001</td><td>1.825</td><td>10001</td><td>1.425</td></tr>
<tr><td>00010</td><td>1.800</td><td>10010</td><td>1.400</td></tr>
<tr><td>00011</td><td>1.775</td><td>10011</td><td>1.375</td></tr>
<tr><td>00100</td><td>1.750</td><td>10100</td><td>1.350</td></tr>
<tr><td>11101</td><td>1.725</td><td>10101</td><td>1.325</td></tr>
<tr><td>00111</td><td>1.675</td><td>10111</td><td>1.275</td></tr>
<tr><td>01000</td><td>1.650</td><td>11000</td><td>1.250</td></tr>
<tr><td>01001</td><td>1.625</td><td>11001</td><td>1.225</td></tr>
<tr><td>01010</td><td>1.600</td><td>11010</td><td>1.200</td></tr>
<tr><td>01011</td><td>1.575</td><td>11011</td><td>1.175</td></tr>
<tr><td>01100</td><td>1.550</td><td>11100</td><td>1.150</td></tr>
<tr><td>01101</td><td>1.525</td><td>11101</td><td>1.125</td></tr>
<tr><td>01110</td><td>1.500</td><td>11110</td><td>1.100</td></tr>
<tr><td>01111</td><td>1.475</td><td>11111</td><td>NO CPU</td></tr>
</table>
For more information, see the “Required Circuits” chapter of the AMD Athlon™ Processor-Based Motherboard Design Guide, order# 24363.</td></tr>
</table>

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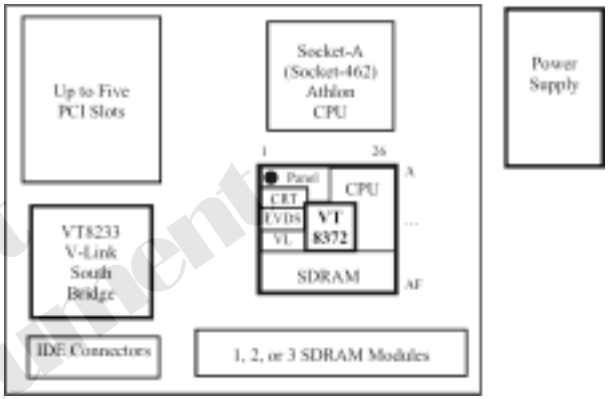
5.2 VIA VT8372 North Bridge

CPU Interface

Signal Name	Pin #	I/O	Signal Description
CFWDRST	D14	O	CLK Forward Reset.Reset the clock forward circuitry for the Athlon .interface.
CONNECT	C14	O	Connect.Used for power anagement and CLK-forward initialization at reset.
PROCRDY	E14	I	Processor Ready.Used for power anagement and clock-forward initialization at reset.
AIN[14-2]#	(see pin list)	O	Host CPU Address /Command Output.Unidirectional syste address /com and interface to the processor from the system controller.It is used to transfer probes or data ovement com ands into the processor during PCI-to-DRAM cycles to snoop the CPU internal Cache. AIN[14:2]#is skew-aligned with the forward clock,AINCLK#
AINCLK#	B15	O	Host CPU Address Output Clock.Single-ended forwarded clock for the AIN[14:2]# bus that is driven by the syste controller.Both rising and falling edges are used to transfer addresses or com ands to the processor.
AOUT[14-2]#	(see pin list)	I	Host CPU Address Input.Unidirectional system address /command interface from the processor to the system controller.It is used to transfer processor com ands or probes responses to the syste controller.AOUT[14:2]# is skew-aligned with the forward clock, AOUTCLK#
AOUTCLK#	R25	I	Host CPU Address Input Clock.Single-ended forwarded clock for the AOUT[14:bus that is driven by the processor.Both rising and falling edges are used to transfer com ands or probe responses.
D[63-0]#	see pin list)	IO	Host CPU Data.Bi-directional interface between the processor and the system controller for data movement. D[63:0]#bus is skew-aligned with either the DICLK[3:0]#or DOCLK[3:0]#forward clocks.
DICLK[3-0]#	L24,G23 , A24,A1 9	O	Host CPU Data Input Clock. Single-ended forwarded clocks for the D[63:0]#bus, driven by the syste controller to the processor.Each 16-bit data word is skew-aligned with one of these clocks.Both rising and falling edges are used to transfer data to the pocessor.
DOCLK[3-0] #	L22,F23 , B24,C19	I	Host CPU Data Output Clock.Single-ended forwarded clocks for the D[63:0]#bus, driven by the processor to the system controller.Each 16-bit data word is skew-aligned with one of these clocks.Both rising and falling edges are used to transfer data to the system controller.
DINVAL#	E13	O	HostCPUDataReadInVald.Driven by the syste controller to control the flow of data into the processor.DINVAL#can be used to introduce an arbitrary number of cycles between octawords into the processor.

The pinouts were defined assuming the ATX PCB layout model shown below (and general pin layout shown) as a guide for PCB component placement. Other PCB layouts (AT, LPX, and NLX) were also considered and can typically follow the same general component placement.



V-Link Interface

Signal Name	Pin #	I/O	Signal Description				
VAD7,	AC1	IO	Address/Data Bus.				SB
			Strap	Function	Setting (L=strap low,H=strap high)	Register	Pin
VAD6 /strap	AB4	IO	VAD6	Auto-Configure	L=Disable (use on-chip defaults) H=Enable (get from ROM)		SDA2
VAD5 /strap,	Y2	IO	VAD5	CPU Clock Divide Bit-3	(see register description)	Rx97[6]	SDA1
VAD4 /strap,	AC2	IO	VAD4	CPU Clock Divide Bit-2	(see register description)	Rx97[5]	SDA0
VAD3 /strap,	Y1	IO	VAD3	CPU Clock Divide Bit-1	(see register description)	Rx97[4]	SA19
VAD2 /strap,	AA4	IO	VAD2	CPU Clock Divide Bit-0	(see register description)	Rx97[3]	SA18
VAD1 /strap,	W5	IO	VAD1	FSB Clock Speed Msb	LL=66,LH=100,		SA17
VAD0 /strap	W4	IO	VAD0	FSB Clock Speed Lsb	HL=HH=133 MHz		SA16
VBE#	Y3	IO	Byte Enable.				
VUPCMD	Y4	I	Command from Client-to-Host.				
VUPSTB	AA1	I	Strobe from Client-to-Host.				
VUPSTB#	AA2	I	Complement Strobe from Client-to-Host.				
VDNCMD	AB3	O	Command from Host-to-Client.				
VDNSTB	AB1	O	Strobe from Host-to-Client.				
VDNSTB#	AB2	O	Complement Strobe from Host-to-Client.				

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5.2 VIA VT8372 North Bridge

DRAM Interface

Signal Name	Pin #	I/O	Signal Description
MD[63:0]	(see pinout tables)	IO	Memory Data.These signals are connected to the DRAM data bus. Output drive strength ay be set by Device 0 Rx6D[1-0].
MA[14:0]	AB19,AB18,AF17, AC9,AB10,AC17,A E17,AC18,AB15,AB 17,AB16,AB14,AC1 2,AB12,AC11	O	Memory Address.DRAM address lines.Output drive strength may be set by Device 0 Rx6C[7-6].
CS[5:0]#	AD5,AB7,AB6, AC6,AC5,AD6	O	Chip Select.Chip select of each bank.Output drive strength aybe set by Device 0 Rx6D[3-2].
DQM[7:0]	AF4,AB8,AF12, AE15,AF19,AD22,A D25,Y26	O	Data Mask.Data ask of each byte lane.Output drive strength may be set by Device 0 Rx6D[5-4].
DQS[7:0]#	AD4,AC8,AE12, AF15,AD19,AF22,A D26,Y24	IO	DDR Data Strobe.Data strobe of each byte lane.Output drive strength ay be set by Device 0 Rx6C[3-2].
SRASA#, SRASB#/CK E5, SRASC#/CK E4	AB11 AF24 AB20	O	Row Address Command Indicator.Output drive strength ay be set by Device 0 Rx6C[7-4].
SCASA#, SCASB#/CK E3, SCASC#/CK E1	AD7 AC24 AD24	O	Column Address Command Indicator.Output drive strength ay be set by Device 0 Rx6C[7-4].
SWEA#, SWEB#/CKE 2, SWEC#/CKE 0	AB9 AB22 AC21	O	Write Enable Command Indicator.Output drive strength ay be set by Device 0 Rx6C[7-4].
CKE5 /SRASB#, CKE4 /SRASC#, CKE3 /SCASB#, CKE2 /SWEB#, CKE1 /SCASC#, CKE0 /SWEC#	AF24 AB20 AC24 AB22 AD24 AC21	O	Clock Enables.Clock enables for each DRAM bank for powering down the SDRAM or clock control for reducing power usage and for reducing heat /temperature in high-speed e ory systems. See Device 0 Rx6B[4].

Clocks, Resets, Power Control, General Purpose I/O, Interrupts and Test

Signal Name	Pin #	I/O	Signal Description
HCLK	G21	I	Host Clock. This pin receives the host CPU clock (100 /133 MHz).This clock is used by all TwisterK-DDR logic that is in the host CPU domain.
HCLK#	F22	I	Host Clock Complement. HCLK inverted. Used for Quad Data Transfer on host CPU bus.
MCLK	Y22	O	Memory (SDRAM)Clock. Output from internal clock generator to the external clock buffer.
MCLKFB	AA23	I	Memory (SDRAM)Clock Feedback. Input from the external clock buffer.
DCLKI	D5	I	Dot Clock (Pixel Clock)In. Used for external EMI reduction circuit if used. Loop back from DCLKO if external EMI reduction circuit not implemented.
DCLKO	C5	O	Dot Clock (Pixel Clock)Out. Used for external EMI reduction circuit if used. Loop back to DCLKI if external EMI reduction circuit not implemented.
GCLK	V5	I	Graphics Clock.
XIN	E6	I	Reference Frequency Input. An external 14.31818 MHz clock source is normally connected to this pin. All internal graphics controller clocks are synthesized on chip using this frequency as a reference.
RESET#	AE1	I	Reset. Input from the South Bridge chip. When asserted, this signal resets Twister K-DDR and sets all register bits to the default value. The rising edge of this signal is used to sample all power-up strap options
PWROK	AD1	I	Power OK. Connect to South Bridge and Power Good circuitry.
SUSST#	AD2	I	Suspend Status. For implementation of the Suspend-to-DRAM feature. Connect to an external pull up to disable.
SUSPEND	B1	I	Suspend. Used to put the integrated graphics controller into suspend state.
STNDBY	E4	I	Standby. Used to put the integrated graphics controller into standby state.
GPOUT /STRW	E7	O	General Purpose Output. This pin reflects the state of SRD[0].
GOP0	D10	O	General Output Port. When SR1A[4]is cleared, this pin reflects the state of CR5C[0].
STRW /GPOUT	E7	O	
INTA#	F6	O	Interrupt. PCI interrupt output (handled by the interrupt controller in the South Bridge)

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5.2 VIA VT8372 North Bridge

Clocks, Resets, Power Control, General Purpose I/O, Interrupts and Test Continue

Signal Name	Pin #	I/O	Signal Description
BISTIN	A5	I	BIST In. This pin is used for testing and must be left unconnected or tied high on all board designs.
TESTIN	F12	I	Test In.
TEST[7:0]	E2,E1,D3,D2, D1,C2,C1,E3		Test Data.

LCD Panel /Flat Panel Monitor (DVI) Interface

Signal Name	Pin #	I/O	Signal Description
FPD11 /TVBL#, FPD10 /TVD10, FPD9 /TVD9, FPD8 /TVD8, FPD7/TVD7/strap, FPD6 /TVD6/strap, FPD5 /TVD5/strap, FPD4 /TVD4/strap, FPD3 /TVD3/strap, FPD2 /TVD2/strap, FPD1 /TVD1/strap, FPD0 /TVD0/strap	A7 B7 C7 C8 A8 B8 E8 E9 A9 B9 C9 D9	O	Panel Data.Default output drive is 8 a.16 a ay be selected via SR3D[6]=1. Panel data is selected for output on these pins when SR31[4]=1.TV Encoder outputs are uxed on the FPD[11:0]pins (see the TV Encoder Interface pin list for details). FPD[7:0]are also used for power-up /reset straps for the internal graphics controller logic (see Table 10 in the Functional Description section of this data sheet for details). Internally pulled down during reset for strap default of 0. FPD0 /strap PCI Interrupt CR36[0] 1 =Enable FPD1 /strap IO Disable CR36[4] 1 =Enable FPD2 /strap PCI Base Address Mapping CRB0[7] 0 =Map1, 1 =Map0 FPD3 /strap -reserved- FPD4 /strap OEM Defined Panel Type bit-0 CRF0[0] FPD5 /strap OEM Defined Panel Type bit-1 CRF0[1] FPD6 /strap OEM Defined Panel Type bit- 2 CRF0[2] FPD7 /strap OEM Defined Panel Type bit-3 CRF0[3]
FPVS /TVVS	B11	O	Panel VSYNC. Internally pulled down.
FPHS /TVHS	B10	O	Panel HSYNC. Internally pulled down.
FPDE /TVCLKI	A10	O	Panel Data enable. Internally pulled down.
FPCLK /TVCLKO	D8	O	Panel Clock. Internally pulled down during reset.8Ma is the default.16Ma ay also be selected.
FPDET /TV11	A11	I	Panel Detect. If SR30[1]=0,SR30[2]will read 1 if a Flat Panel is appropriately connected. Must be tied to GND if not used.
ENVDD	F3	O	Enable VDD. This signal is driven high to external logic to initiate a flat panel power up sequence.
ENVEE	F1	O	Enable VEE. This signal is driven high to a program able time after ENVDD is driven high during a flat panel power up sequence.

CRT Interface

Signal Name	Pin #	I/O	Signal Description
AR	A3	A	Analog Red.Analog red output to the CRT onitor.
AB	B3	A	Analog Blue.Analog blue output to the CRT onitor.
AG	A2	A	Analog Green.Analog green output to the CRT onitor.
HSYNC	B6	O	Horizontal Sync.Output to CRT.
VSYNC	A6	O	Vertical Sync.Output to CRT.
RSET	B5	A	Reference Resistor.Tie to GNDRGB through an external 140 .resistor to control the RAMDAC full-scale current value.

TV Encoder Interface

Signal Name	Pin #	I/O	Signal Description
TVD11 /FPDET, TVD10 /FPD10, TVD9 /FPD9, TVD8 /FPD8, TVD7 /FPD7 /strap, TVD6 /FPD6 /strap, TVD5 /FPD5 /strap, TVD4 /FPD4 /strap, TVD3 /FPD3 /strap, TVD2 /FPD2 /strap, TVD1 /FPD1 /strap, TVD0 /FPD0 /strap	A11 B7 C7 C8 A8 B8 E8 E9 A9 B9 C9 D9	O	TV Encoder Data.Internally pulled down during reset
TVCLKI /FPDE	A10	I	TV Encoder Clock In. Input clock from encoder. Internally pulled down.
TVCLKO /FPCLK	D8	O	TV Encoder Clock Out. Output clock to TV encoder. Internally pulled down.
TVHS /FPHS	B10	O	TV Encoder HSYNC. Internally pulled down during reset
TVVS /FPVS	B11	O	TV Encoder VSYNC. Internally pulled down during reset
TVBL#/FPD11	A7	O	TV Encoder Blanking. Internally pulled down during reset

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5.2 VIA VT8372 North Bridge

Power,Ground,and Test

Signal Name	Pin #	I/O	Signal Description
VTT	J13-J18,K18,L18, M18,N18,P18,R18	P	Power for CPU I/O Interface Logic. Voltage is CPU dependent. See also VID (Voltage ID)pin.
VID#	E10v	I	Voltage ID.CPU FSB interface voltage select.0 =desktop,1=mobile.
VCCS2K	M21	P	S2K Bus Interface Power.(2.5V ±5%)
GNDS2K	K21	P	S2K Bus Ground. Connect to main ground plane.
S2KCOMP	L21	I	S2K Bus Compensation. Connect to 70 ？1%resistor to ground.
S2KVREF	F17,N21	P	S2K Bus Voltage Reference.碾TT derived using 100 ？1%+100 ？1% resistive voltage divider. See TwisterK-DDR Design Guide.
VCCM	T18,U18,V9-V18, AA7,AA17,AA21	P	Power for Memory I/O Interface Logic (2.5 ±5%).
MEMVREF	AA10,AA18	P	Memory Voltage Reference.
VCCVL	T9,U9,Y6,AA6	P	Power for V-Link I/O Interface Logic (2.5V ±5%).
VLCOMP	AB5	I	Vlink P-Channel Compensation. Connect 70 ？1%resistor to ground.
VLVREF	Y5	P	V-Link Voltage Reference.1.0V derived using a resistive voltage divider between VCC25 and ground (see Design Guide for details).
VCC33	(see pin list)	P	Power for Internal Logic (3.3V ±5%).
VCC25	(see pin list)	P	Power for Internal Logic (2.5V ±5%).
VSUS25	AD3	P	Suspend Power (2.5V ±5%).
VCCHCK	G22	P	Power for Host CPU Clock DLL (2.5V ±5%)
VCCMCK	AA22	P	Power for Memory Clock DLL (2.5V ±5%)
VCCMDLL	AA14	P	Power for Memory Strobe DLL (2.5V ±5%)
VCCFP	J10-J12	P	Power for Flat Panel /DVI Interface (3.3V ±5%).
VCCRGB	C3	P	Power for CRT RGB Outputs (2.5V ±5%).
VCCDAC	C4	P	Power for DAC Digital Logic (2.5V ±5%)
VCCPLL1	B4	P	Power for Graphics Controller PLL1 (2.5V ±5%).
VCCPLL2	A4	P	Power for Graphics Controller PLL2 (2.5V ±5%).
VCCLVDS	H1,W3	P	Digital Power for LVDS Circuitry (2.5V ±5%).
VCCALVDS	K2,N5,U4	P	Analog Power for LVDS Circuitry (3.3V ±5%).
VCCALPLL	H3	P	Analog Power for LVDS PLL (2.5V ±5%).
GND	(see pin table)	P	Ground. Connect to main ground plane.

Power,Ground,and Test Continue

Signal Name	Pin #	I/O	Signal Description
GNDHCK	F21	P	Ground for Host CPU Clock Circuitry. Connect to main ground plane through a ferrite bead.
GNDMCK	Y21	P	Ground for Memory Clock Circuitry. Connect to main ground plane through a ferrite bead.
GNDMDLL	AA13	P	Ground for Memory Strobe DLL Circuitry. Connect to main ground plane through a ferrite bead.
GNDRGB	A1	P	Connection Point for RGB Load Resistors.
GNDDAC	A1	P	Connection Point for RGB Load Resistors.
GNDDAC	B2	P	Ground for DAC Analog Circuitry.
GNDPLL1	E5	P	Ground for Graphics Controller PLL1.
GNDPLL2	D4	P	Ground for Graphics Controller PLL2.
GNDALPLL	H4,J3	P	Ground for LVDS PLL.
GNDALVDS	M5,R5,U5	P	Ground for LVDS Analog Circuitry.
GNDLVDS	H2,J1,J5,W2	P	Ground for LVDS Digital Circuitry.
NC	(see pin table)		No Connect.

LVDS Interface

Signal Name	Pin #	I/O	Signal Description
Y[3:0]+ Y[3:0] -	N4,T1,U3,U1 P3,T2,U2,V1	A A	LVDS Data Positive Output. LVDS Data Negative Output.
YC+ YC -	P4 P5	A A	LVDS Clock Posit ve Output. LVDS Clock Negative Output.nd
Z[3:0]+ Z[3:0] -	K3,L1,L4,N1 K1,L2,L3,N2	A A	2nd LVDS Data Positive Output. 2nd LVDS Data Negative Output.
ZC+ ZC -	K4 K5	A A	2nd LVDS Clock Positive Output. 2nd LVDS Clock Negative Output.

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5.2 VIA VT8372 North Bridge

SMB /I2C Interface

Signal Name	Pin #	I/O	Signal Description
SPCLK[2:1]	C6,F7	IO	Serial Port (SMB/I2C)Clocks.These are the clocks for serial data transfer. SPCLK1 is typically used for I 2 C com unications.As an output,it is program ed via CRA0[0]. As an input,its status is read via CRA0[2].In either case the serial port ust be enabled by CRA0[4]=1.SPCLK2 is typically used for DDC onitor com unications.As an output,it is program ed via CRB1[0].As an input,its status is read via CRB1[2].The port is enabled via CRB1[4]=1.
SPDAT[2 :1]	D6,D7	IO	Serial Port (SMB/I2C)Data.These are the data signals used for serial data transfer.SPDAT1 is typically used for I^2C com unications.As an output,it is program ed via CRA0[1].As an input,its status is read via CRA0[3].In either case the serial port ust be enabled by CRA0[4]=1. SPDAT2 is typically used for DDC monitor communications. As an output,it is program ed via CRB1[1]. As an input,its status is read via CRB1[3].The port is enabled via CRB1[4]=1.

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5.3 VIA VT8235 South Bridge

V-Link Interface

Signal Name	Pin #	I/O	Signal Description
VAD[15:0]	K22,J22,G24,H22, G22,G23,F23,D25, K26,K24,E24,E26, J25,J26,F26,F25	IO	Address /Data Bus. Bits 0-7 are implemented and bits 8-15 are reserved for future use. VAD[6:0]are used to send strap information o he chipset north bridge. A power up VAD[6:4]reflect he state of straps on pins SDA[2:0] and VAD[3:0]reflect the state of straps on pins SA[19:16].The specific interpretation of these straps is north bridge chip design dependent.
VPAR	D26	IO	Parity. If the VPAR function is implemented in a compatible manner on the north bridge, this pin should be connected to the north bridge VPAR pin (P4X333, P4X400, P4X800,KT400).If VPAR is not implemented in the north bridge chip or is incompatible with he 8235 (4x V-Link north bridges) connect this pin to an 8.2K pull up to 2.5V (Pro266,Pro266T,KT266, KT266A, KT333, P4X266, PN266,KN266,KM266, P4M266, P4N266).See app note AN222 for details.
VBE[1:0]#	L26,F24	IO	Byte Enables.VBE0#is used with VAD[7-0]and VBE1# is used with VAD[15-8](VBE1#and VAD[15-8]are reserved for future use).
VCLK	L24	I	V-Link Clock.
UPCMD	K25	O	Command from Client-to-Host.
DNCMD	J24	I	Command from Host-to-Client.
UPSTB	H24	O	Strobe from Client-to-Host.
UPSTB#	H26	O	Complement Strobe from Client-to-Host.
DNSTB	G25	I	Strobe from Host-to-Client.
DNSTB#	G26	I	Complement Strobe from Host-to-Client.
VLVREF	J23	I	Voltage Reference.
VLCOMP	K23	I	V-Link Compensation.
VCCVK	(see pin list)	P	V-Link VK Power.

Advanced Programmable Interrupt Controller (APIC)Interface

Signal Name	Pin #	I/O	Signal Description
APICD1	V23	O	Internal APIC Data 1.Function 0 Rx58[6]=1
APICD0	T22	O	Internal APIC Data 0.Function 0 Rx58[6]=1
APICCLK	U23	I	APIC Clock.

Straps

Signal Name	Pin #	I/O	Signal Description
Strap /SDCS3#	AD23	I	Strap. State reflected on VAD[7]at powerup. No internal function.
Strap /SDA2	AF23	I	Strap. State reflected on VAD[6]at powerup. No internal function.
Strap /SDA1	AC22	I	Strap. State reflected on VAD[5]at powerup. No internal function.
Strap /SDA0	AE23	I	Strap. State reflected on VAD[4]at powerup. No internal function.
Strap /SA19	AC11	I	Strap. State reflected on VAD[3]at powerup. No internal function.
Strap /SA18	AD11	I	Strap. State reflected on VAD[2]at powerup. No internal function.
Strap /SA17	AE11	I	Strap. State reflected on VAD[1]at powerup. No internal function.
Strap /SA16	AF11	I	Strap. State reflected on VAD[0]at powerup. No internal function.
Strap /SOE#	AD12	I	Strap. Strap low o enable (high o disable)auto reboot.
Strap /SPKR	AE9	I	Strap. Strap low o enable (high o disable)CPU frequency s rapping
Strap /ROMCS#/KBCS#	AF12	I	Strap. Strap high to enable LPCBIOSROM

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5.3 VIA VT8235 South Bridge

CPU Speed Control Interface

Signal Name	Pin #	I/O	Signal Description
VGATE /GPIO8 /PCREQA	C8	I	Voltage Gate. Signal from he CPU voltage regulator. High indicates he voltage regulator output is stable. This pin performs he VGATE function if Device 17 Function 0 Rx53[7]=0,E5[4]=1 and E4[3]=0.
VIDSEL /GPIO28	P25	OD	Voltage Regulator ID Select. Connected o he CPU voltage regulator. Low selects the voltage ID from the CPU; high selects a different fixed voltage ID (the lower voltage used for CPU deep sleep mode). This pin performs the VIDSEL function if Function 0 RxE5[3]=0.
VRDSLP /GPIO29	P24	OD	Voltage Regulator Deep Sleep. Connected to the CPU voltage regulator. High selects the proper voltage for deep sleep mode. This pin performs he VRDPSLP function if Function 0 RxE5[3]=0.
GHI#/GPIO22	R24	OD	CPU Speed Select. Connected o he CPU voltage regulator, used to select high speed (L) or low speed (H).This pin performs the GHI# function if Function 0 RxE5[3]=0.
DPSLP#/GPIO23	P26	OD	CPU Deep Sleep.
CPUMISS /GPI17	Y1	I	CPU Missing. Used to detect the physical presence of the CPU chip in its socket. High indicates no CPU present. Connect to the CPUMISS pin of he CPU socket. The state of this pin may be read in the SMBus 2 registers. This pin may be used as CPUMISS and GPI17 at the same time.
AGPBZ#/GPI6	A8	I	AGP Busy. Low indicates that an AGP master cycle is in progress (CPU speed transitions will be postponed if his input is asserted low).Connected to the AGP Bus AGPBZ# pin.

Summary of Internal Pull-Up /Pull-Down Resistor Implementation Internal Pullups are present on pins KBCK,KBDT,MSCK,MSDT,SERIRQ,LAD [3:0]Internal Pulldowns are present on pins SA [19-16] and all LAN pins

Low Pin Count (LPC)Interface

Signal Name	Pin #	I/O	PU	Signal Description
LFRM#	AE7	IO		LPC Frame.
LREQ#	AD7	IO		LPC DMA /Bus Master Request.
LAD[3-0]	AF7,AD8,AE8, AF8	IO	PU	LPC Address /Data.

Note: Connect the LPC interface LPCRST#(LPC Reset)signal to PCIRST#

CPU Interface

Signal Name	Pin #	I/O	Signal Description
A20M#	T25	OD	A20 Mask. Connect to A20 mask input of he CPU to control address bi -20 generation. Logical combination of the A20GATE input (from internal or external keyboard controller) and Port 92 bit -1 (Fast_A20).
FERR#	U26	I	Numerical Coprocessor Error. This signal is tied o he coprocessor error signal on the CPU. Internally generates interrupt 13 if active. Output voltage swing is programmable tot 1.5V or 2.5V by Device 17 Function 0 Rx67[2].
IGNNE#	T26	OD	Ignore Numeric Error. This pin is connected to the CPU "ignore error" pin.
INIT#	R25	OD	Initialization. The VT8235 asserts INIT# if it detects a shut-down special cycle on he PCI bus or if a soft reset is initiated by he register
INTR	T23	OD	CPU Interrupt. INTR is driven by he VT8235 to signal he CPU hat an interrupt request is pending and needs service.
NMI	R23	OD	Non-Maskable Interrupt. NMI is used o force a non-maskable interrupt to the CPU. The VT8235 generates an NMI when PCI bus SERR# is asserted.
SLP#	U25	OD	Sleep. Used to put the CPU to sleep.
SMI#	T24	OD	System Management Interrupt. SMI# is asserted by he VT8235 o he CPU in response to different Power-Management events.
STPCLK#	R26	OD	Stop Clock. STPCLK# is asserted by he VT8235 to the CPU to throttle the processor clock.

Note: Connect each of the above signals to 150 .pullup resistors to VCC_CMOS (see Design Guide).

Serial EEPROM Interface

Signal Name	Pin #	I/O	PU	Signal Description
EECS#	A13	O		Serial EEPROM Chip Select.
EECK	C14	O		Serial EEPROM Clock.
EEDO	A14	O		Serial EEPROM Data Output.
EEDI	B14	I		Serial EEPROM Data Input.

These pins are disabled if the SDCS1#pin is strapped low to enable serial EEPROM connection via the MII interface.

Confidential Document

5.3 VIA VT8235 South Bridge

PCI Bus Interface

Signal Name	Pin #	I/O	Signal Description
AD[31:0]	see pin list)	IO	Address /Data Bus. Multiplexed address and data. The address is driven with FRAME# assertion and data is driven or received in following cycles.
CBE[3:0]#	L1,A4, D1,F4	IO	Command /Byte Enable. The command is driven with FRAME# assertion. Byte enables corresponding to supplied or requested data are driven on following clocks.
DEVSEL#	B3	IO	Device Select. The VT8235 asserts his signal o claim PCI transactions through positive or subtractive decoding. As an input, DEVSEL# indicates the response to a VT8235-initiated transaction and is also sampled when decoding whether to subtractively decode the cycle.
FRAME#	B4	IO	Frame. Assertion indicates the address phase of a PCI transfer. Negation indicates that one more data transfer is desired by the cycle initiator.
IRDY#	C4	IO	Initiator Ready. Asserted when the initiator is ready for data transfer.
TRDY#	A3	IO	Target Ready. Asserted when the target is ready for data transfer.
STOP#	C3	IO	Stop. Asserted by the target to request the master to stop the current transaction.
SERR#	C1	I	System Error. SERR# can be pulsed active by any PCI device that detects a system error condition. Upon sampling SERR# active, the VT8235 can be programmed o generate an NMI to the CPU.
PAR	D3	IO	Parity. A single parity bi is provided over AD[31:0]and C/BE[3:0]#.
INTA# INTB# INTC# INTD# INTE# /GPIO12 /PCGNTA, INTF# /GPIO13 /PCGNTB, INTG# /GPIO14, INTH# /GPIO15	P1, P2, P3, R1 A7, B8, D8, C7	I	PCI Interrupt Request .The INTA# through INTD# pins are typically connected to the PCI bus INTA#-INTD# pins per the able below. INTE-H# are enabled by setting Device 17,Function 0 Rx5B[1]=1. BIOS settings must match the physical connection method. INTA# INTB# INTC# INTD# PCI Slot 1 INTA# INTB# INTC# INTD# PCI Slot 2 INTB# INTC# INTD# INTE# PCI Slot 3 INTC# INTD# INTE# INTF# PCI Slot 4 INTD# INTE# INTF# INTG# PCI Slot 5 INTE# INTF# INTG# INTH# PCI Slot 6 INTF# INTG# INTH# INTA#

PCI Bus Interface Continue

Signal Name	Pin #	I/O	Signal Description
REQ5#/GPI7, REQ4#, REQ3#, REQ2#, REQ1#, REQ0#	N4 L4 H4 D4 C5 D6	I	PCI Request. These signals connect to the VT8235 from each PCI slot (or each PCI master)o request he PCI bus. To use pin N4 as REQ5#, Function 0 RxE4 must be set to 1 otherwise his pin will function as General Purpose Input 7.
GNT5#/GPO 7, GNT4#, GNT3#, GNT2#, GNT1#, GNT0#	P4 M4 J4 E4 D5 E6	O	PCI Grant. These signals are driven by he VT8235 to grant PCI access to a specific PCI master. To use pin P4 as GNT5#,Function 0 RxE4 must be set to 1 otherwise this pin will function as General Purpose Output 7.
PCIRST#	R2	O	PCI Reset. This signal is used o reset devices attached to the PCI bus.
PCICLK	R22	I	PCI Clock. This signal provides timing for all transactions on the PCI Bus.
PCKRUN#	AF5	IO	PCI Bus Clock Run. This signal indicates whether he PCI clock is or will be stopped high) or running (low).The VT8235 drives his signal low when he PCI clock is running default on reset)and releases it when it stops the PCI clock. External devices may assert this signal low o request hat he PCI clock be restarted or prevent it from stopping. Connect his pin o ground using a 100 .resistor if he function is not used. Refer to the “PCI Mobile Design Guide” and he VIA “VT8633 Apollo Pro266 Design Guide” for more details.

PC /PCI DMA

Signal Name	Pin #	I/O	PU	Signal Description
PCREQA/GPIO8/VGATE	C8	I		PC /PCI Request A. Device 17 Function 0 Rx53[7]=1
PCREQB /GPIO9	B7	I		PC /PCI Request B. Device 17 Function 0 Rx53[7]=1
PCGNTA /GPIO12	A7	O		PC /PCI Grant A. Device 17 Function 0 Rx53[7]=1
PCGNTB /GPIO13	B8	O		PC /PCI Grant B. Device 17 Function 0 Rx53[7]=1

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5.3 VIA VT8235 South Bridge

LAN Controller -Media Independent Interface (MII)

Signal Name	Pin #	I/O	PU	Signal Description
MCOL	C13	I	*PD*	MII Collision Detect. From he external PHY.
MCRS	B13	I	*PD*	MII Carrier Sense. Asserted by the external PHY when the media is active.
MDCK	C9	O	*PD*	MII Management Data Clock. Sent to the external PHY as a timing reference for MDIO
MDIO	B9	IO	*PD*	MII Management Data I/O. Read from he MDI bit or written to the MDO bit.
MRXCLK	B10	I	*PD*	MII Receive Clock.2.5 or 25 MHz clock recovered by the PHY.
MRXD[3-0]	A9,D9,D10,E10	I	*PD*	MII Receive Data. Parallel receive data lines driven by the external PHY synchronous with MRXCLK.
MRXDV	C10	I	*PD*	MII Receive Data Valid.
MRXERR	A10	I	*PD*	MII Receive Error. Asserted by the PHY when it detects a data decoding error.
MTXCLK	A12	I	*PD*	MII Transmit Clock. Always active 2.5 or 25 MHz clock supplied by the PHY.
MTXD[3-0]	C11,B11,A11,C12	O	*PD*	MII Transmit Data. Parallel transmit data lines synchronized to MTXCLK.
MTXENA	B12	O	*PD*	MII Transmit Enable. Signals that transmit is active from the MII port to the PHY.
MIIVCC	D11,D12,E11,E12	Power		MII Interface Power.3.3V ±5%.
MIIVCC25	D13,E13	Power		MII Suspend Power.2.5V ±5%.
RAMVCC	E7	Power		Power For Internal LAN RAM.2.5V ±5%.
RAMGND	E8	Power		Ground For Internal LAN RAM.

General Purpose I/O

Signal Name	Pin #	I/O	Signal Description
GPIOA /GPI24/GPO24	AE5	IO	**General Purpose I/O A /24**. RxE6[0]=1
GPIOC /GPI25/GPO25	AE6	IO	**General Purpose I/O C /25**.
GPIOD /GPI30/GPO30	AD6	IO	**General Purpose I/O D /30.**
GPIOE /GPI31/GPO31	AC6	IO	**General Purpose I/O E /31.**

The output type of he above pins may be selected as either OD or TTL (see Device 17 Function 0 RxE7)

Universal Serial Bus 2.0 Interface

Signal Name	Pin #	I/O	Signal Description
USBP0+	A21	IO	USB 2.0 Port 0 Data +
USBP0 –	B21	IO	USB 2.0 Port 0 Data –
USBP1+	E21	IO	USB 2.0 Port 1 Data +
USBP1 –	D21	IO	USB 2.0 Port 1 Data –
USBP2+	A19	IO	USB 2.0 Port 2 Data +
USBP2 –	B19	IO	USB 2.0 Port 2 Data –
USBP3+	E19	IO	USB 2.0 Port 3 Data +
USBP3 –	D19	IO	USB 2.0 Port 3 Data –
USBP4+	A17	IO	USB 2.0 Port 4 Data +
USBP4 –	B17	IO	USB 2.0 Port 4 Data –
USBP5+	E17	IO	USB 2.0 Port 5 Data +
USBP5 –	D17	IO	USB 2.0 Port 5 Data –
USBCLK	D23	I	USB 2.0 Clock.48MHz clock input for he USB interface
USBOC0#	A15	I	USB 2.0 Port 0 Over Current Detect. Port 0isdisablediflow.
USBOC1#	B15	I	USB 2.0 Port 1 Over Current Detect. Port1isdisablediflow.
USBOC2#	C15	I	USB 2.0 Port 2 Over Current Detect. Port2isdisablediflow.
USBOC3#	E15	I	USB 2.0 Port 3 Over Current Detect. Port 3isdisablediflow.
USBOC4#	D14	I	USB 2.0 Port 4 Over Current Detect. Port 4isdisablediflow.
USBOC5#	E14	I	USB 2.0 Port 5 Over Current Detect. Port 5isdisablediflow.
USBVCC	(see pin list)	Power	USB 2.0 Port Differential Output Interface Logic Voltage.3.3V
USBGND	(see pin list)	Power	USB 2.0 Port Differential Output Interface Logic Ground.
VSUSUSB	D15	Power	USB 2.0 Suspend Power.2.5V ±5%.
VCCUPLL	A23,D22	Power	USB 2.0 PLL Analog Voltage.2.5V ±5%.
GNDUPLL	B23,E22	Power	USB 2.0 PLL Analog Ground.

Programmable Chip Selects

Signal Name	Pin #	I/O	Signal Description
PCS0#/GPIO20 /ACSDIN2	U2	O	Programmable Chip Select 0.RxE4[6]=1,E5[1]=1
PCS1#/GPIO21/ACSDIN3 /SLPBTN#	V1	O	Programmable Chip Select 1.RxE4[6]=1,E5[2]=1

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5.3 VIA VT8235 South Bridge

UltraDMA-133 /100 /66 /33 Enhanced IDE Interface

Signal Name	Pin #	I/O	Signal Description
PDRDY / PDDMARDY / PDSTROBE	Y26	I	EIDE Mode: **Primary I/O Channel Ready.**Device read indicator UltraDMA Mode:**Primary Device DMA Ready** .Output flow control. The device may assert DDMARDY o pause output transfers **Primary Device Strobe** .Input data strobe (both edges).The device may s op DSTROBE to pause input data transfers
SDRDY / SDDMARDY / SDSTROBE	AD15	I	EIDE Mode: **Secondary I/O Channel Ready.** Device ready indicator UltraDMA Mode: **Secondary Device DMA Ready** .Output flow control. The device may assert DDMARDY to pause output transfers Secondary Device Strobe .Input data strobe (both edges).The device may stop DSTROBE o pause input data transfers
PDIOR#/ PHDMARDY / PHSTROBE	Y24	O	EIDE Mode: Primary Device I/O Read. Device read strobe UltraDMA Mode: Primary Host DMA Ready .Primary channel input flow control .The host may assert HDMARDY o pause input transfers Primary Host Strobe .Output data strobe (both edges).The host may stop HSTROBE o pause output data transfers
SDIOR#/ SHDMARDY / SHSTROBE	AF22	O	EIDE Mode: Secondary Device I/O Read. Device read strobe UltraDMA Mode: Secondary Host DMA Ready .Input flow control. The host may assert HDMARDY to pause input transfers Host Strobe B .Output strobe (both edges).The host may stop HSTROBE to pause output data transfers
PDIOW#/ PSTOP	Y25	O	EIDE Mode: **Primary Device I/O Write.** Device wri te strobe UltraDMA Mode: **Primary Stop.**Stop transfer: Asserted by the host prior to initiation an UltraDMA burst; negated by the host before data is transferred an UltraDMA burst. Assertion of STOP by he host during or after transfer in UltraDMA mode signals the nation of the burst
SDIOW#/ SSTOP	AC21		EIDE Mode: **Secondary Device I/O Write.**Device writ strobe UltraDMA Mode: **Secondary Stop** .Stop transfer Asserted by the host prior to initiation of an UltraDMA burst;negated by the host before data is transferted in an ULtraDMA burst Assert of Stop by the host during or after data transfer in ULtraDMA mode signals the termination of the burst

UltraDMA-133 /100 /66 /33 Enhanced IDE Interface Continue

Signal Name	Pin #	I/O	Signal Description
PDDRQ	Y22	I	Primary Device DMA Request.Primary channel DMA request
SDDRQ	AE15	I	Secondary Device DMA Request.Secondary channel DMA request
PDDACK#	W26	O	Primary Device DMA Acknowledge.Primary channel DMA acknowledge
SDDACK#	AD22	O	Secondary Device DMA Acknowledge.Secondary channel DMA acknowledge
IRQ14	AE24	I	Primary Channel Interrupt Request.
IRQ15	AF24	I	Secondary Channel Interrupt Request.
PDCS1#	V24		Primary Master Chip Select.This signal corresponds toCS1FX#on the primary IDM connector
PDCS3#	W24		Primary Slave Chip Select.This signal corresponds to CS3FX# on the primary IDE connector.
SDCS1#/srap	AC23		Secondary Master Chip Select.This signal corresponds o CS17X# on he secondary IDE connector.S rap low (resistor o ground) to enable serial EEPROM interface via he MII bus (this disables the EExx pins).This pin has an internal pullup to default to serial EEPROM interface via the EEPROM interface via the Eexx pine
SDCS3#/s rap	AD23		Secondary Slave Chip Select. This signal corresponds toCS37X#on the secondary IDE connector. Strap information is communicated to the north bridge via VAD[7].
PDA[2-0]	V26,V25,Y23		Primary Disk Address. PDA[2:0]are used o indicate which by e in either the ATA command block or control block is being accessed.
SDA[2-0]/srap	AF23,AC22,AE23		Secondary Disk Address. SDA[2:0]are used o indicate which byte in either the ATA command block or control block is being accessed. Strap information is communicated to the north bridge via VAD[6:4].
PDD[15-0]	(see pin list)		Primary Disk Data.
SDD[15-0]/SA[15-0]	(see pin list)		Secondary Disk Data.
PDCOMP	W23		Primary Disk Compensation.
SDCOMP	AC15		Secondary Disk Compensation.

Serial IRQ

Signal Name	Pin #	I/O	Signal Description
SERIRQ	AE10	I	Serial IRQ. This pin has an internal pull-up resistor.

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5.3 VIA VT8235 South Bridge

General Purpose Inputs

Signal Name	Pin #	I/O	Signal Description
GPI0 *(VBAT)*	AE3	I	**General Purpose Input 0**.Status on PMIO Rx20[0]
GPI1 *(VSUS33)*	AC3	I	**General Purpose Input 1**.Status on PMIO Rx20[1]
GPI2 /EXTSMI#*(VSUS33)*	AA1	I	**General Purpose Input 2**.Status on PMIO Rx20[4]
GPI3 /RING#*(VSUS33)*	Y2	I	**General Purpose Input 3**.Status on PMIO Rx20[8]
GPI4 /LID#*(VSUS33)*	AC1	I	**General Purpose Input 4**.Status on PMIO Rx20[11]
GPI5 /BATLOW#*(VSUS33)*	W4	I	**General Purpose Input 5**.Status on PMIO Rx20[12]
GPI6 /AGPBZ#	A8	I	**General Purpose Input 6**.Status on PMIO Rx20[5]
GPI7 /REQ5#	N4	I	**General Purpose Input 7**.RxE4[2]=0
GPI8 /GPO8 /PDREQA /VGATE	C8	I	**General Purpose Input8**. RxE4[3]=0, E5[4]=0, 53[7]=0
GPI9 /GPO9 /PDREQB	B7	I	**General Purpose Input 9**. RxE4[3]=0,53[7]=0
GPI10 /GPO10	D7	I	**General Purpose Input 10**.RxE4[3]=0
GPI11 /GPO11	A6	I	**General Purpose Input 11**.RxE4[3]=0
GPI12 /GPO12 /INTE#/PDGNTA	A7	I	**General Purpose Input 12**. RxE4[4]=0,5B[1]=0, 53[7]=0
GPI13 /GPO13 /INTF#/PDGNTB	B8	I	**General Purpose Input 13**. RxE4[4]=0,5B[1]=0, 53[7]=0
GPI14 /GPO14 /INTG#	D8	I	**General Purpose Input 14**.RxE4[4]=0,5B[1]=0
GPI15 /GPO15/INTH#	C7	I	**General Purpose Input 15**.RxE4[4]=0,5B[1]=0
GPI16 /INTRUDER#*(VBAT)*	AD3	I	**General Purpose Input 16**.Status on PMIO Rx20[6]
GPI17 /CPUMISS	Y1	I	**General Purpose Input 17**.Status on PMIO Rx20[5]
GPI18 /THRM#/AOLGPI	Y4	I	**General Purpose Input 18**.Rx8C[3]=0
GPI19 /IORDY	AD10	I	**General Purpose Input 19**.RxE5[0]=1
GPI20 /GPO20/ACSDIN2/PCS0#	U2	I	**General Purpose Input 20**.RxE4[6]=1,E5[1]=0, PMIO 4C[20]=1
GPI21 /GPO21/ACSDIN3/PCS1#/SLP BTN#	V1	I	**General Purpose Input 21**.RxE4[6]=1,E5[2]=0 PMIO 4C[21]=1
GPI22 /GPO22 /GHI#	R24	I	**General Purpose Input 22**.RxE5[3]=1,PMIO 4C[22]=1
GPI23 /GPO23 /DPSLP#	P26	I	**General Purpose Input 23**.RxE5[3]=1,PMIO 4C[23]=1
GPI24 /GPO24/GPIOA	AE5	I	**General Purpose Input 24**.RxE6[0]=0
GPI25 /GPO25/GPIOC	AE6	I	**General Purpose Input 25**.RxE6[1]=0
GPI26 /GPO26/SMBDT2 *(VSUS33)*	AD1	I	**General Purpose Input 26**.Rx95[2]=1,95[3]=0

General Purpose Inputs Continue

Signal Name	Pin #	I/O	Signal Description
GPI27 /GPO27 /SMBCK2 *(VSUS33)*	AE1	I	**General Purpose Input 27**.Rx95[2]=1,95[3]=0
GPI28 /GPO28 /VIDSEL	P25	I	**General Purpose Input 28**.RxE5[3]=1,PMIO 4C[28]=1
GPI29 /GPO29/VRDSLP	P24	I	**General Purpose Input 29**.RxE5[3]=1,PMIO 4C[29]=1
GPI30 /GPO30 /GPIOD	AD6	I	**General Purpose Input 30**.RxE6[6]=0
GPI31 /GPO31/GPIOE	AC6	I	**General Purpose Input 31**.RxE6[7]=0

Note:Defaul pin function is underlined in he signal name column above.
Note:Input pin s a us for he above GPI pins 31-0 is also available on PMIO Rx4B-48 [31-0]
Note:See also Power Management I/O register Rx50 for input pin change status for GPI16-19 and 24-27
Note:See also Power Management I/O register Rx52 for SCI/SMI select for GPI16-19 and 24-27
Note:See also Power Management I/O register Rx4C.General purpose input pins 20-31 are shared with OD (open drain)general purpose output functions,so to use one of these pins as an input pin,a one must be written to the corresponding bit of PMIO Rx4C.

Resets,Clocks,and Power Status

Signal Name	Pin #	I/O	Signal Description
PWRGD	AF4	I	**Power Good.** Connected o he Power Good signal on he Power Supply. Internal logic powered by VBAT.
PWROK#	AE2	O	**Power OK.** Internal logic powered by VSUS33.
PCIRST#	R2	O	**PCI Reset.** Active low reset signal for he PCI bus. The VT8235 will assert his pin during power-up or from he control register.
OSC	AC12	I	**Oscillator.**14.31818 MHz clock signal used by he in ernal Timer.
RTCX1	AD4	I	**RTC Crystal Input :**32.768 KHz crystal or oscilla or input. This input is used for the internal RTC and power-well power management logic and is powered by VBAT.
RTCX2	AF3	O	**RTC Crystal Output :**32.768 KHz crystal output. Internal logic powered by VBAT.
TEST	AF9	I	Test.
TPO	U24	O	**Test Pin Output.** Output pin for est mode.
NC	W22,AD17	-	**No Connect.** Reserved for future use,do not connect.

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5.3 VIA VT8235 South Bridge

Power Management and Event Detection

Signal Name	Pin #	I/O	Signal Description
PWRBTN#	AD2	I	**Power Button.**Used by the Power Management subsystem to monitor an external system on/off but on or switch. Internal logic powered by VSUS33.
SLPBTN#/GPIO21 /ACSDIN3 /PCS1#	V1	I	**Sleep Button.** Used by he Power Management subsystem to monitor an external sleep but on or switch.RxE4[6]=1,80[6]=1,E5[2]=0 and PMIO Rx4C[21]=1
RSMRST#	AD5	I	**Resume Reset.** Resets he internal logic connected o he VSUS33 power plane and also resets portions of he internal RTC logic. Internal logic powered by VBAT.
EXTSMI#/GPI2	AA1	IOD	**External System Management Interrupt.** When enabled o allow it ,a falling edge on this input causes an SMI# to be generated o he CPU o enter SMI mode.(10K PU to VSUS33 if not used)(3.3V only)
PME#	W3	I	**Power Management Event.**(10K PU o VSUS33 if not used)
SMBALRT#	AB2	I	**SMB Alert** .When programmed to allow it (SMB I/O Rx8[3]=1),assertion generates an IRQ, SMI,or power management event.(10K PU o VSUS33 if not used)
LID#/GPI4	AC1	I	**Notebook Computer Display Lid Open /Closed Monitor.** Used by he Power Management subsystem to monitor he opening and closing of the display lid of notebook computers. Can be used o detect either low-to-high or high-to-low transitions o generate an SMI#.(10K PU o VSUS33 if not used)
INTRUDER#/GPI16	AD3	I	Intrusion Indicator. The value of his bi may be read at PMIO Rx20[6]
THRM#/GPI18 /AOLGPI	Y4	I	**Thermal Alarm Monitor.**Rx8C[3]=1.Rising or falling edges (selectable by PMIO Rx2C[6])may be detected to status at used a PMIO Rx20[10].Setting of this status bit may then be used to generate an SCI or SMI. THRM# may also be used to enable duty cycle control of stop-clock (STPCLK#)o automatically limit maximum temperature (see Device 17 Function 0 Rx8C[7-3]).
RING#/GPI3	Y2	I	**Ring Indicator.** May be connected to external modem circuitry to allow he system to be re-activated by a received phone call.(10K PU to VSUS33 if not used)
BATLOW#/GPI5	W4	I	**Battery Low Indicator.** (10K PU to VSUS33 if not used)(3.3V only)

Power Management and Event Detection Continue

Signal Name	Pin #	I/O	Signal Description
CPUSTP#/GPO5	AC7	O	**CPU Clock Stop** (RxE4[0]=0).Signals the system clock generator to disable the CPU clock outputs. Not connected if not used.
PCISTP#/GPO6	AF6	O	**PCI Clock Stop** (RxE4[1]=0).Signals the system clock generator o disable he PCI clock outputs. Not connected if not used.
SUSA#/GPO1	AA2	O	**Suspend Plane A Control** (Rx94[2]=0).Asserted during power management POS, STR, and STD suspend states. Used to control the primary power plane.(10K PU to VSUS33 if not used)
SUSB#/GPO2	AF2	O	**Suspend Plane B Control** (Rx94[3]=0).Asserted during power management STR and STD suspend states. Used o control he secondary power plane.(10K PU o VSUS33 if not used)
SUSC#	AF1	O	**Suspend Plane C Control**. Asserted during power management STD suspend state. Used to control he tertiary power plane. Also connected to ATX power-on circuitry. (10K PU o VSUS33 if not used)
SUSST1#/GPO3	Y3	O	**Suspend Status 1** (Rx94[4]=0).Typically connected to the North Bridge to provide information on host clock status. Asserted when the system may stop the host clock, such as Stop Clock or during POS, STR, or STD suspend statues. Connect 10K PU to VSUS33.
SUSCLK	AB1	O	**Suspend Clock.**32.768 KHz output clock for use by the North Bridge (e.g.,VT8633 or VT8366)for DRAM refresh purposes. Stopped during Suspend-to-Disk and Soft-Off modes. Connect 10K PU to VSUS33.
CPUMISS /GPI17	Y1	I	**CPU Missing.** Used to detect the physical presence of the CPU chip in its socket. High indicates no CPU present. Connect to he CPUMISS pin of the CPU socket.The state of his pin may be read in the SMBus 2 registers.This pin may be used as CPUMISS and GPI17 a the same time.
AOLGPI /GPI18 /THRM#	R2	I	**Alert On LAN.** The state of this pin may be read in the SMBus 2 registers. This pin may be used as AOLGPI, GPI18andTHRM#alla the same time.

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5.3 VIA VT8235 South Bridge

Internal Keyboard Controller

Signal Name	Pin #	I/O	PU	Signal Description
MSCK /IRQ1	W2	IO/I	PU	**MultiFunction Pin** (Internal mouse controller enabled by Rx51[1]) Rx51[1]=1 **Mouse Clock**. From internal mouse controller. Rx51[1]=0 **Interrupt Request 1** .Interrupt input 1.
MSDT /IRQ12	W1	IO/I	PU	**MultiFunction Pin** (Internal mouse controller enabled by Rx51[1]) Rx51[1]=1 **Mouse Data**. From internal mouse controller. Rx51[1]=0 **Interrupt Request 12**. Interrupt input 12.
KBCK /KA20G	V3	IO /I	PU	**MultiFunction Pin** (Internal keyboard controller enabled by Rx51[0]) Rx51[0]=1 Keyboard Clock. From internal keyboard controller Rx51[0]=0 Gate A20.Input from external keyboard controller.
KBDT /KBRC	V2	IO/I	PU	**MultiFunction Pin** (Internal keyboard controller enabled by Rx51[0]) Rx51[0]=1 **Keyboard Data**. From internal keyboard controller. Rx51[0]=0 **Keyboard Rese**t. From external keyboard controller (KBC)for CPURST# generation
KBCS#/ROMCS#/srap	AF12	O/O		**Keyboard Chip Select** (Rx51[0]=0).To external keyboard controller chip. Strap high o enable LPC ROM:

Note: KBCK,KBDT,MSCK,and MSDT are powered by the VSUS33 suspend voltage plane.

AC97 Audio /Modem Interface

Signal Name	Pin #	I/O	Signal Description
ACRST#	R3	O	AC97 Reset.
ACBTCK	T3	I	AC97 Bit Clock.
ACSYNC	T1	O	AC97 Sync.
ACSDO	U1	O	AC97 Serial Data Out.
ACSDIN0 (VSUS33)	T2	I	AC97 Serial Data In 0.
ACSDIN1 (VSUS33)	U3	I	AC97 Serial Data In 1.
ACSDIN2 /GPIO20 /PCS0#	U2	I	AC97 Serial Data In2.RxE4[6]=0,E5[1]=0,PMIO Rx4C[20]=1
ACSDIN3/GPIO21 /PCS1#/SLPBTN#	V1	I	AC97 Serial Data In 3.RxE4[6]=0,E5[2]=0,PMIO Rx4C[21]=1

The supply voltage for ACSDIN0-1 is VSUS33 so these inputs can support wake-up on modem ring

Power and Ground

Signal Name	Pin #	I/O	Signal Description
VCC33	(see pin list)v	P	**I/O Power.**3.3V ±5%
VCC	(see pin list)	P	**Core Power.**2.5V ±5%.This supply is turned on only when he mechanical switch on the power supply is turned on and he PWRON signal is conditioned high . Note: The VT8235L core voltage is 2.5V so board designs that are intended t all w use of either VT8235 or VT8235L should take this difference into account and allow the core voltage to be selected as either 2.5V (for the VT8235)or 3.3V (for the VT8235L).
GND	(see pin list)	P	Ground. Connect o primary motherboard ground plane.
VSUS33	AA4,AB4, AC4,AC5	P	**Suspend Power.**3.3V ±5%.Always available unless the mechanical switch of the power supply is turned off. If the "soft-off" state is not implemented, then this pin can be Connected to VCC33.Signals powered by or referenced o this plane are:PWRGD, RSMRST#,PWRBTN#,SMBCK1/2, SMBDT1/2,GPO0,SUSA#/GPO1,SUSB#/ GPO2,SUSC#, SUSST1#/GPO3,SUSCLK /GPO4,GPI1,GPI2/EXTSMI#,GPI3 /RING#,GPI4 /LID,GPI5 /BATLOW#,GPI6 /PME#, SMBALRT#
VSUS25	T4,U4	P	**Suspend Power.**2.5V ±5%.
VSUSUSB	D15	P	**USB Suspend Power**.2.5V ±5%.
VBAT	AE4	P	**RTC Battery.** Battery input for internal RTC (RTCX1,RTCX2)
VLVREF	J23	P	**V-Link Voltage Reference.**0.9V ±5%.0.34 xVCC25to0.38 xVCC25.
VCCVK	(see pin list)	P	V-Link Compensation Circuit Voltage.2.5V ±5%
MIIVCC	D11,D12, E11,E12	P	**LAN MII Power.**3.3V ±5%.Power for LAN Media Independent Interface (interface to external PHY).Connect o VCC33 through a ferrite bead.
MIIVCC25	D13,E13	P	**LAN MII Suspend Power.**2.5V ±5%.
RAMVCC	E7	P	**LAN RAM Power.**2.5V ±5%.Power for LAN internal RAM. Connect to VCC through a ferrite bead.
RAMGND	E8	P	**LAN RAM Ground.** Connect o GND through a ferrite bead.
USBVCC	(see pin list)	P	**USB 2.0 Differential Output Power.**3.3V ±5%.Power for USB differential outputs (USBP0+,P0 – ,P1+,P1 – ,P2+, P2 – , P3+, P3 – ,P4+,P4 – ,P5+,P5 –).Connect o VSUS33 through a ferrite bead.
USBGND	(see pin list)	P	**USB 2.0 Differential Output Ground.** Connect to GND through a ferrite bead.

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5.3 VIA VT8235 South Bridge

Power and Ground Continue

Signal Name	Pin #	I/O	Signal Description
VCCUPLL	A23,D22	P	**USB 2.0 PLL Analog Voltage**.2.5V ±5%.Connect to VCC through a ferrite bead.
GNDU PLL	B23,E22	P	**USB 2.0 PLL Analog Ground.** Connect to GND through a ferrite bead.
PLLVCC	P22	P	**PLL Analog Power.**2.5V ±5%.Connect to VCC through a ferrite bead.
PLLGND	P23	P	**PLL Analog Ground.** Connect o GND through a ferrite bead.

System Management Bus (SMB)Interface (I 2 CBus)

Signal Name	Pin #	I/O	Signal Description
SMBCK1	AB3	IO	SMB /I^2 C Channel 1 Clock.
SMBCK2 /GPI27/GPO27	AE1	IO	SMB /I^2 C Channel 2 Clock.Rx95[2]=0
SMBDT1	AC2	IO	SMB /I^2C Channel 1 Data.
SMBDT2 /GPI26/GPO26	AD1	IO	SMB /I^3C Channel 2 Data.Rx95[2]=0
SMBALRT#	AB2	I	SMB Alert.(enabled by System Management Bus I/O space Rx08[1]When the chip is enabled to allow it, assertion generates an IRQ SMI interrupt or a power management resume event. Connect o a ohm pull up to VSUS33 if not used.

ISA Subset /Parallel BIOS ROM Interface

Signal Name	Pin #	I/O	PU	Signal Description
ROMCS#/KBCS#/ strap	AF12	O		**ROM Chip Select** (Rx51[0]=1).Chip Select o the BIOS ROM. Strap high to enable LPCROM.
SPKR /srap	AE9	O		**Speaker**. Strap low to enable (high o disable)CPU frequency strapping.
MEMR#	AE12	O		**Memory Read.**
MEMW#	AF10	O		**Memory Write.**
IOR#	AC10	O		**I/O Read.**
IOW#	AD9	O		**I/O Write.**
IORDY /GPI19	AD10	I		**I/O Ready**. Used to insert wait states in I/O or memory cycles. RxE5[0]=0
SOE#/s rap	AD12	O		**XD Bus Tranceiver Output Enable**. Strap low to enable auto reboot.
XD[7-0]	AD13,AE13, AF13,AD14, AE14,AF14, AC13,AC14	IO		**XD Bus**. For input of BIOS ROM data or data from to her on-board I/O or memory devices.
SA[19-16]/GPO[19-16] /sraps	AC11,AD11, AE11,AF11	O	*PD*	**System Address 19-16**.Strap states are passed to North Bridge via VAD[3-0].Functions as SA[19-16]if RxE4[5]=0.
SA[15-0]/SDD[15-0]	(see pin lis)	O		**System Address 15-0**.

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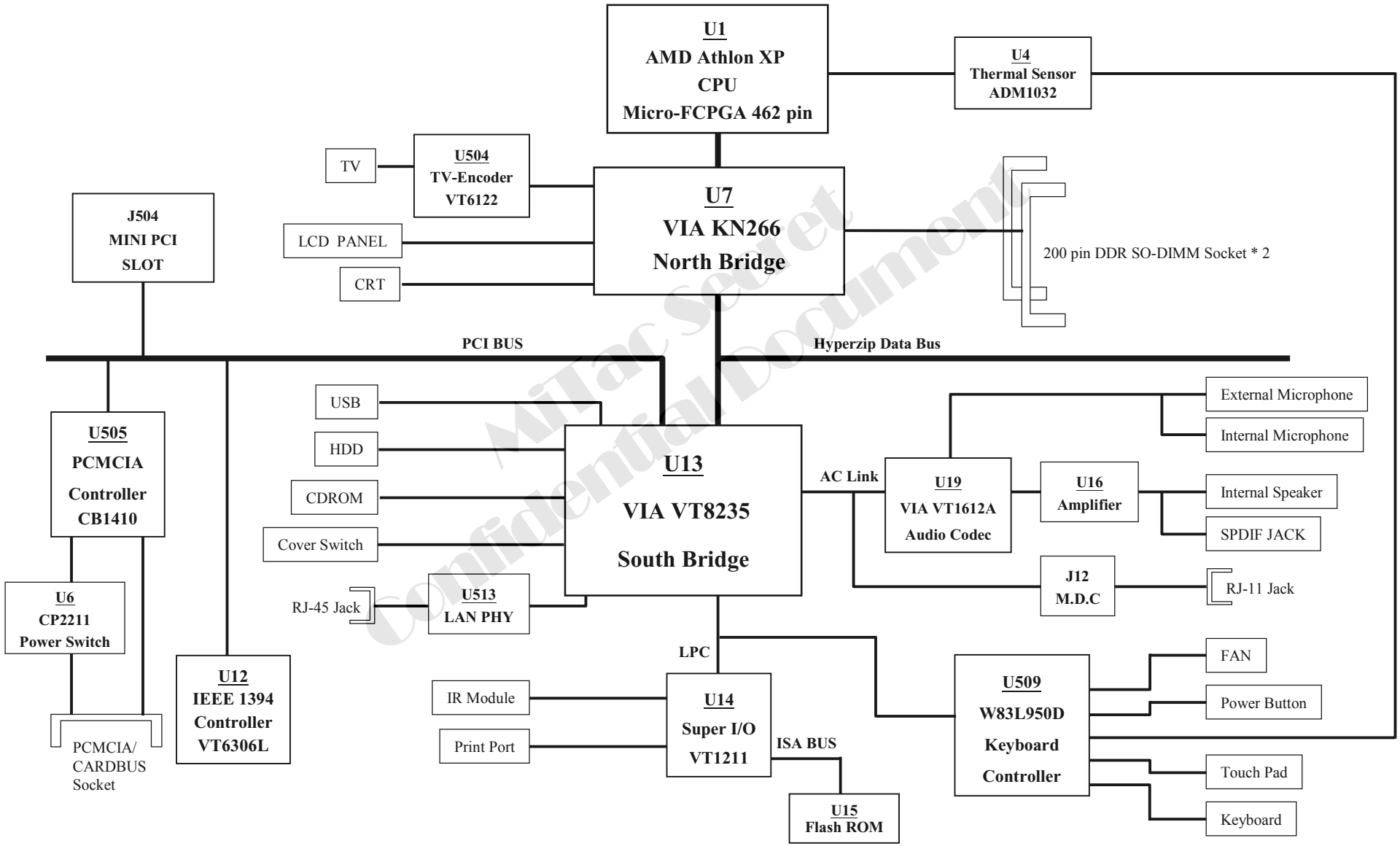
6. System Block Diagram



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7. Maintenance Diagnostics

7.1 Introduction

Each time the computer is turned on, the system BIOS runs a series of internal checks on the hardware. This power-on self test (post) allows the computer to detect problems as early as the power-on stage. Error messages of post can alert you to the problems of your computer.

If an error is detected during these tests, you will see an error message displayed on the screen. If the error occurs before the display is initialized,then the screen cannot display the error message. Error codes or system beeps are used to identify a post error that occurs when the screen is not available.

The value for the diagnostic port (378H) is written at the beginning of the test. Therefore, if the test failed, the user can determine where the problem occurred by reading the last value written to port 378H by the 378H port debug board plug at PIO PORT.

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7.2 Error Codes

Following is a list of error codes in sequent display on the PIO debug board.

Code	POST Routine Description
10h	Some type of lone reset
11h	Turn off FAST A20 for POST
12h	Signal power on reset
13h	Initialize the chipset
14h	Search for ISA Bus VGA adapter
15h	Reset counter / Timer 1
16h	User register config through CMOS
17h	Sizememory
18h	Dispatch to RAM test
19h	Check sum the ROM
1Ah	Reset PIC's
1Bh	Initialize video adapter(s)
1Ch	Initialize video (6845Regs)
1Dh	Initialize color adapter
1Eh	Initialize monochrome adapter
1Fh	Test 8237A page registers

Code	POST Routine Description
20h	Test keyboard
21h	Test keyboard controller
22h	Check if CMOS RAM valid
23h	Test battery fail & CMOS X-SUM
24h	Test the DMA controller
25h	Initialize 8237A controller
26h	Initialize int vectors
27h	RAM quick sizing
28h	Protected mode entered safely
29h	RAM test completed
2Ah	Protected mode exit successful
2Bh	Setup shadow
2Ch	Going to initialize video
2Dh	Search for monochrome adapter
2Eh	Search for color adapter
2Fh	Signon messages displayed

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7.2 Error Codes

Following is a list of error codes in sequent display on the PIO debug board.

Code	POST Routine Description
30h	Special init of keyboard ctlr
31h	Test if keyboard Present
32h	Test keyboard Interrupt
33h	Test keyboard command byte
34h	Test, blank and count all RAM
35h	Protected mode entered safely(2)
36h	RAM test complete
37h	Protected mode exit successful
38h	Update output port
39h	Setup cache controller
3Ah	Test if 18.2Hz periodic working
3Bh	Test for RTC ticking
3Ch	Initialize the hardware vectors
3Dh	Search and init the mouse
3Eh	Update NUMLOCK status
3Fh	Special init of COMM and LPT ports

Code	POST Routine Description
40h	Configure the COMM and LPT ports
41h	Initialize the floppies
42h	Initialize the hard disk
43h	Initialize option ROMs
44h	OEM's init of power management
45h	Update NUMLOCK status
46h	Test for coprocessor installed
47h	OEM functions before boot
48h	Dispatch to operate system boot
49h	Jump into bootstrap code
50h	ACPI init
51h	PM init & Geyserville
52h	USB HC init

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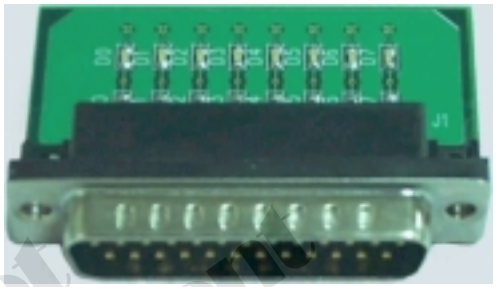
7.3 Maintenance Diagnostics

7.3.1 Diagnostic Tools :

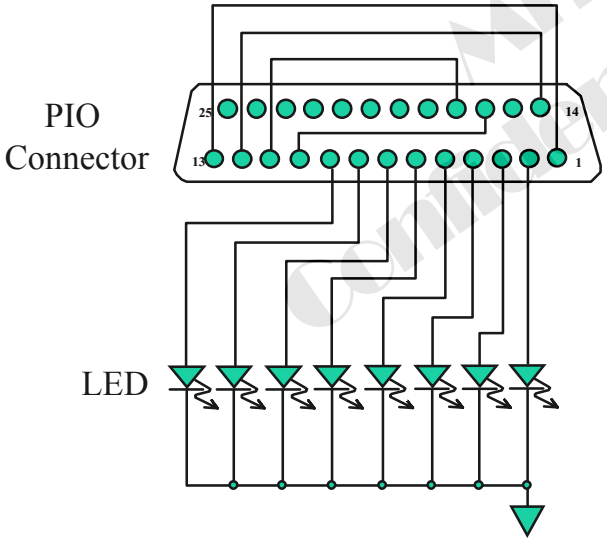
- **LED * 8**
- **PIO CONNECTOR * 1**

OR



P/N:411904800001
Description: PWA; PWA-378Port Debug BD
Note: Order it from MIC/TSSC

7.3.2 Circuit:



PIN1 : STROBE ⟷ PIN 13 : SLCT

PIN10: ACK# ⟷ PIN 16 : INT#

PIN11: BUSY ⟷ PIN 17 : SELIN#

PIN12: PTERR ⟷ PIN 14 : AUTOFD#

PIN{9:2}: PD{7:0}

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8. Trouble Shooting

- 8.1 No Power
- 8.2 No Display
- 8.3 VGA Controller Failure LCD No Display
- 8.4 External Monitor No Display
- 8.5 Memory Test Error
- 8.6 Keyboard (K/B) Touch-Pad (T/P) Test Error
- 8.7 Hard Drive Test Error
- 8.8 CD-ROM Drive Test Error
- 8.9 USB Port Test Error
- 8.10 PIO Port Test Error
- 8.11 Audio Failure
- 8.12 LAN Test Error
- 8.13 PC-Card Socket Failure
- 8.14 IEEE1394 Failure
- 8.15 TV Test Error

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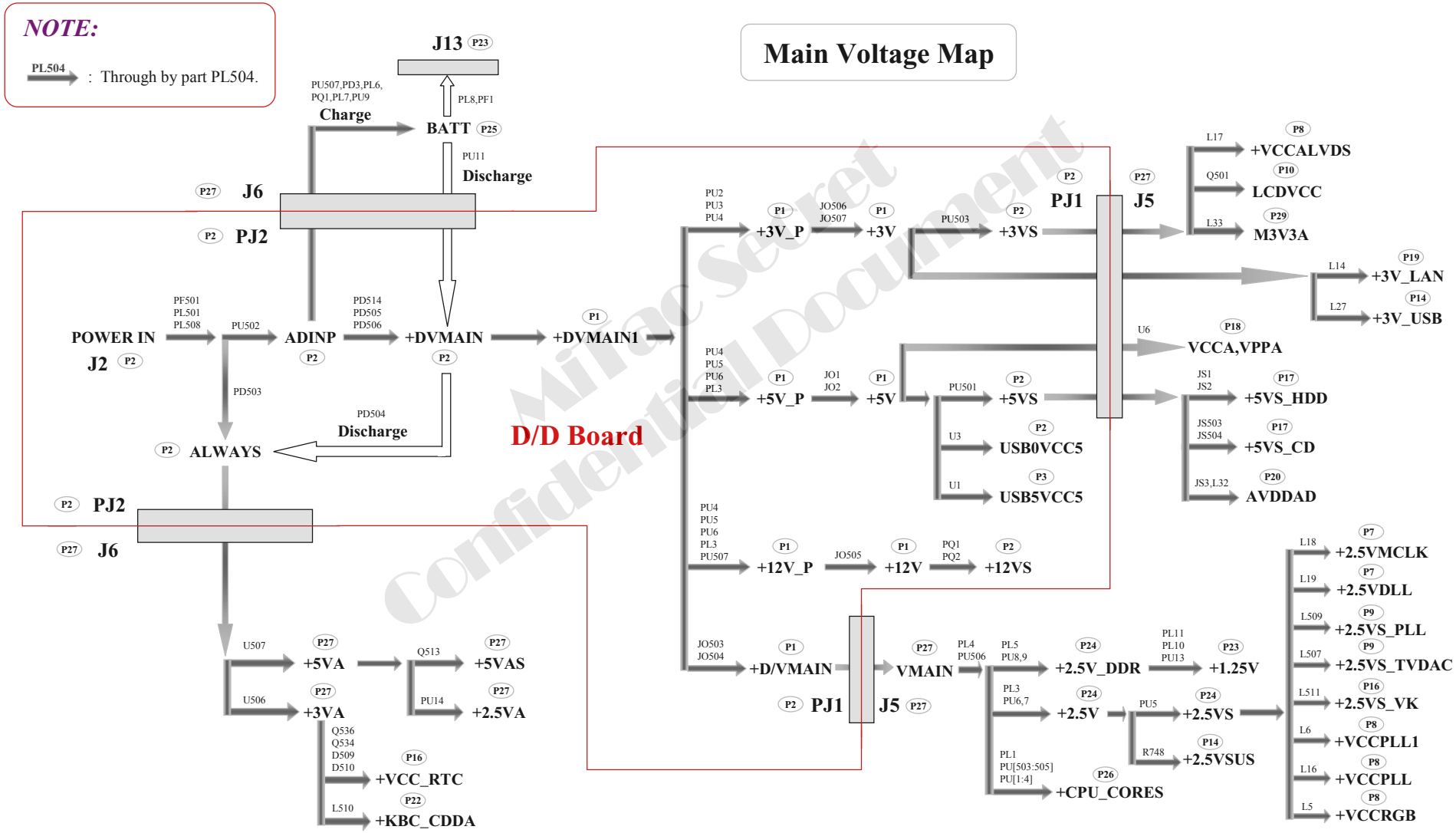
8.1 No Power

When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.



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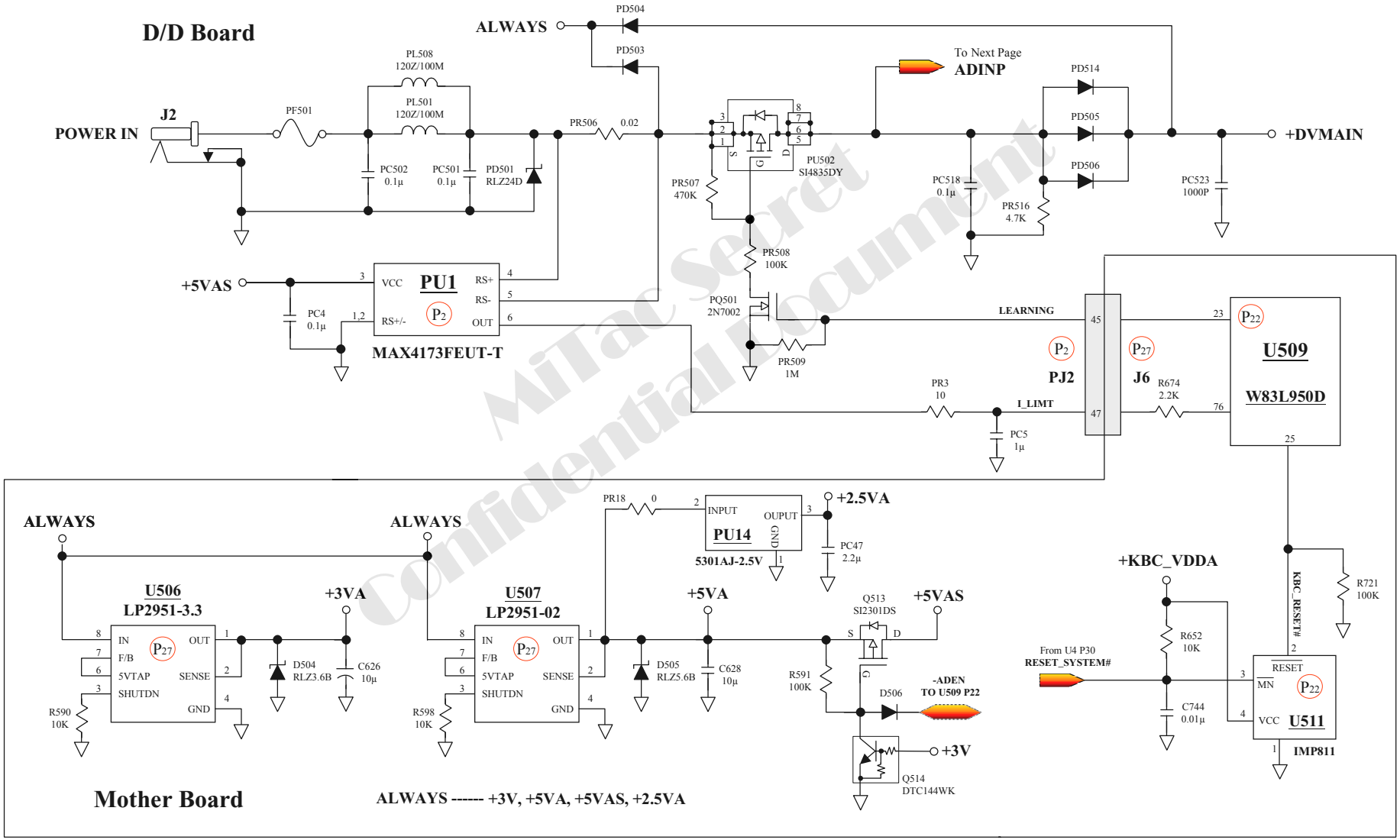

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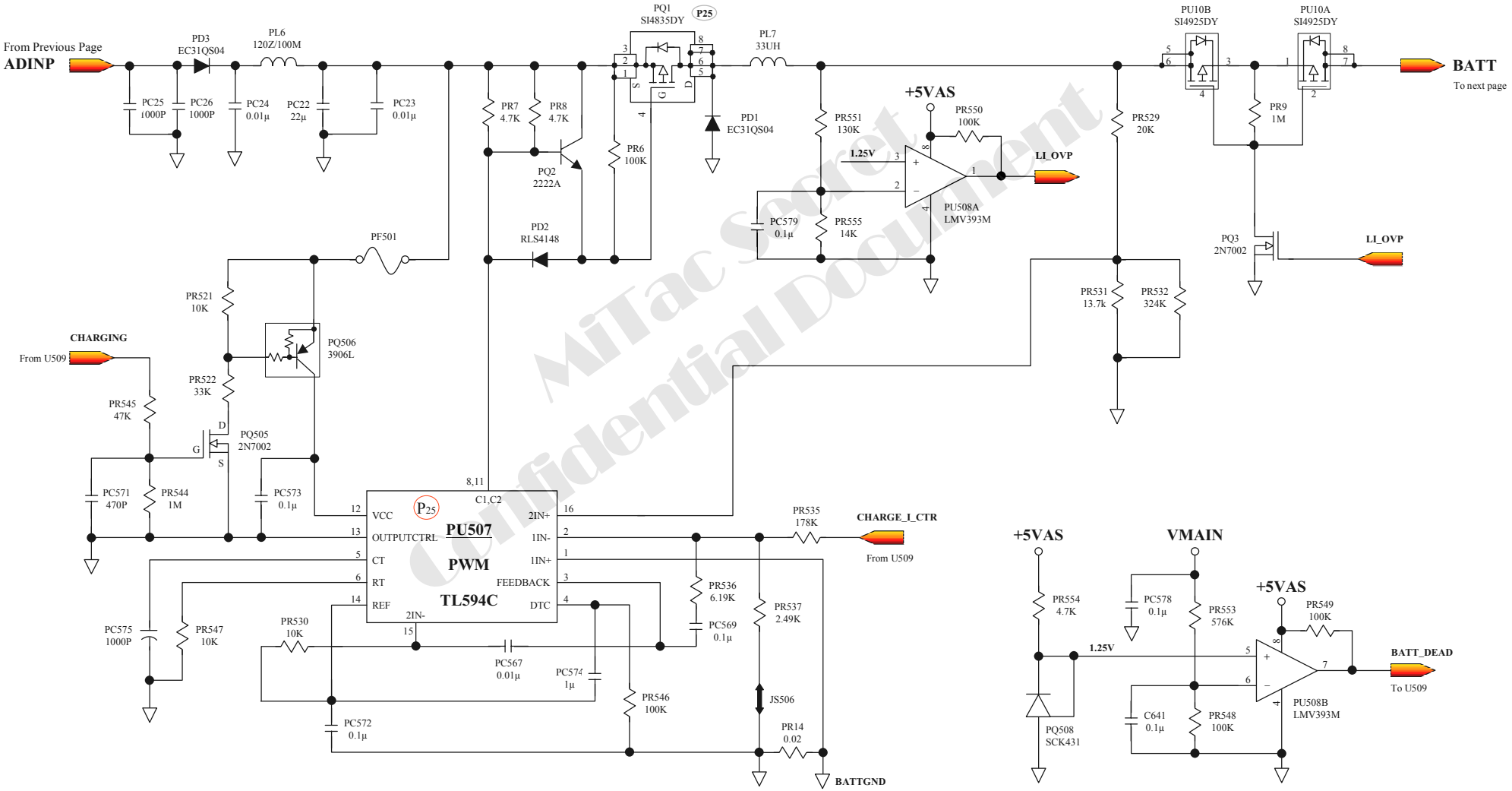
8.1 No Power – Battery Charge

When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.



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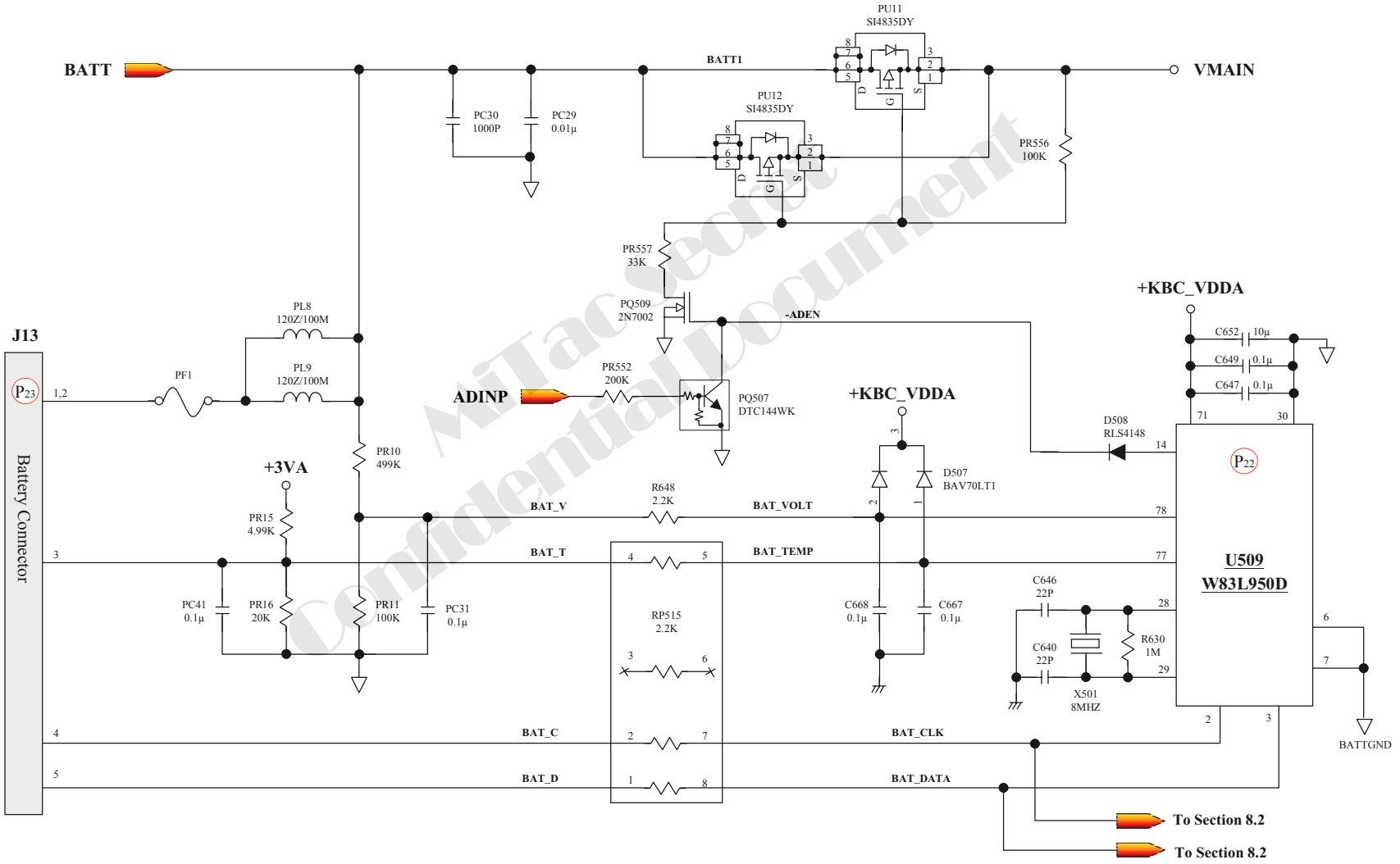
8.1 No Power – Battery Discharge

When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.



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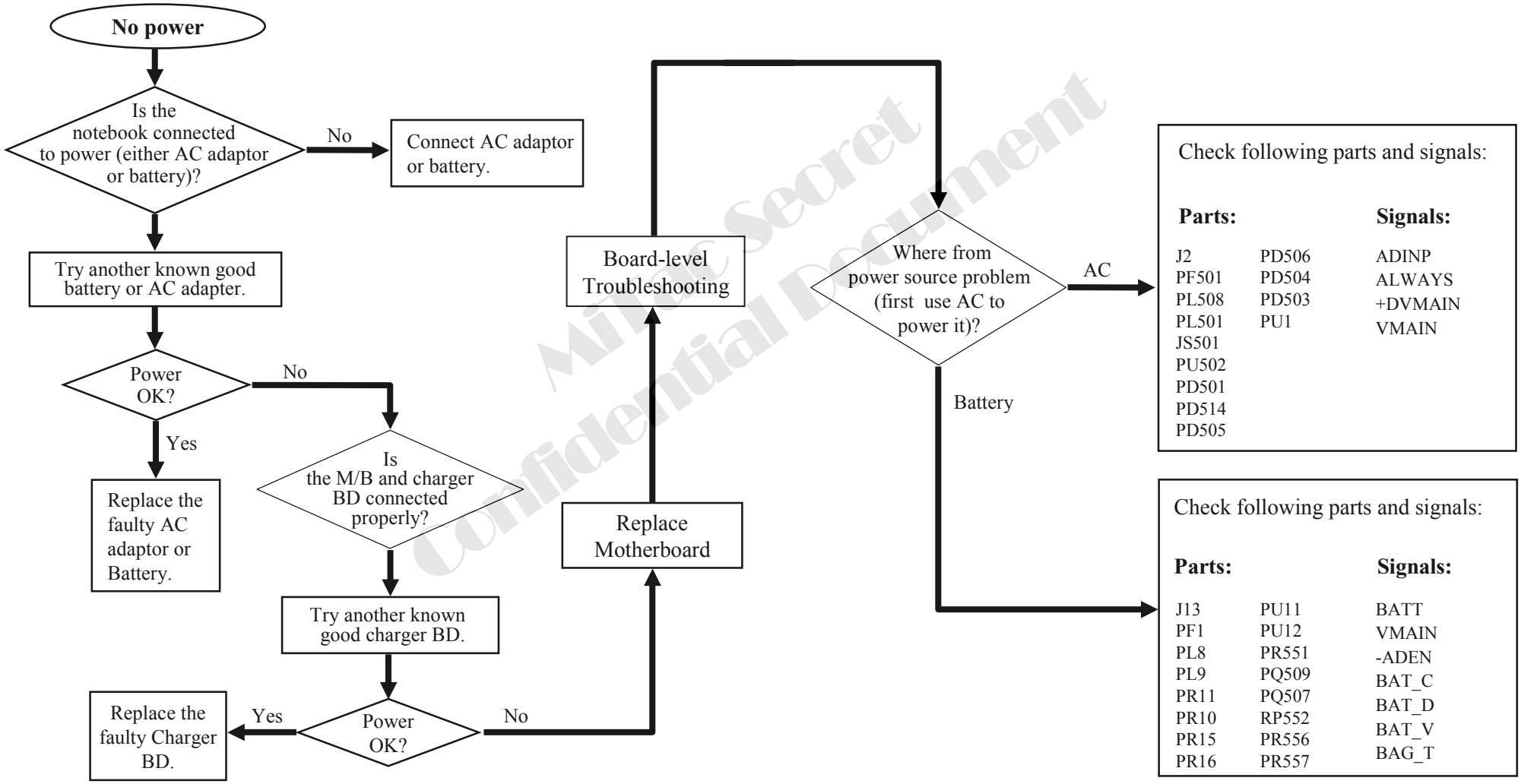
8.1 No Power

When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.



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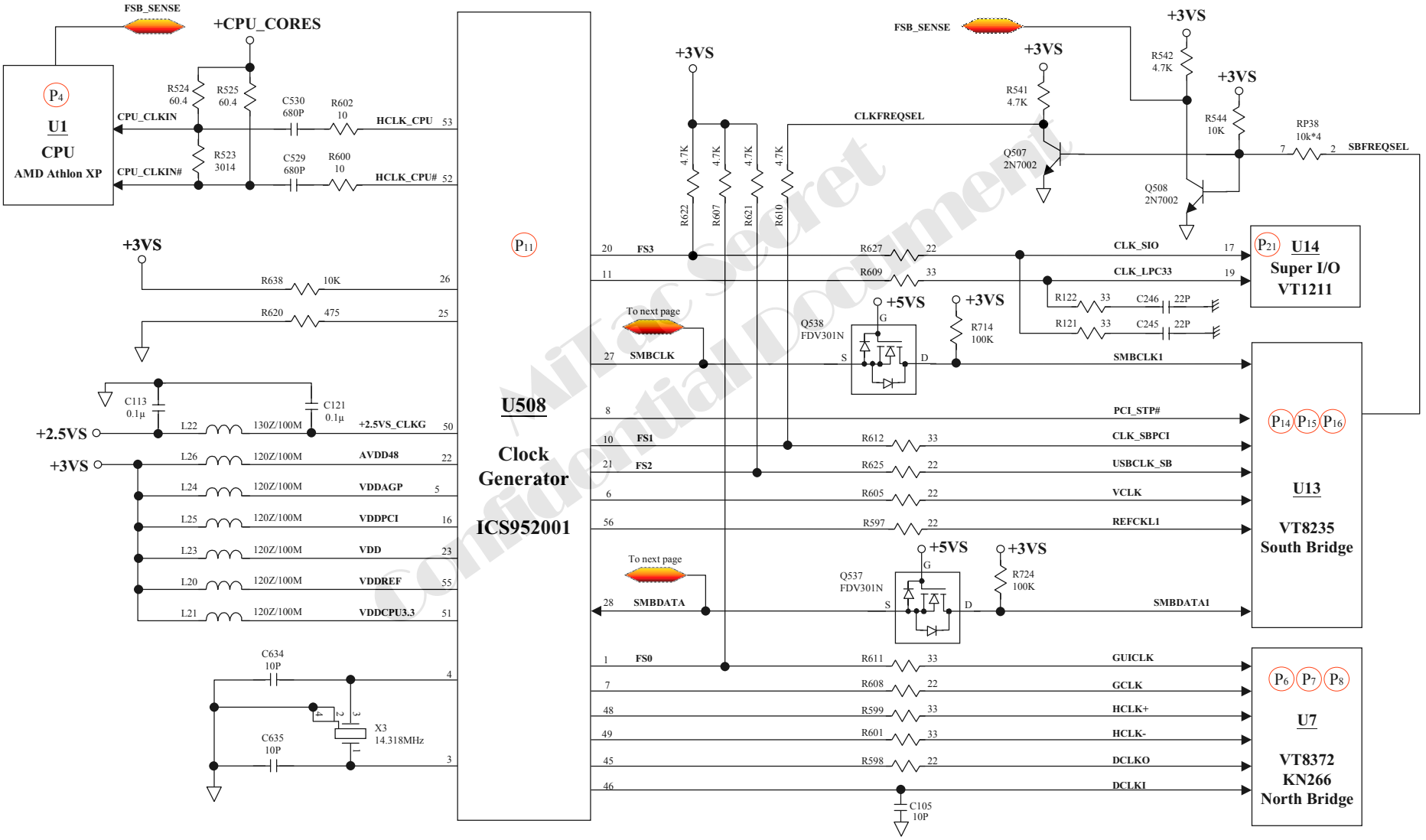
8.2 No Display

****** System Clock Check ******



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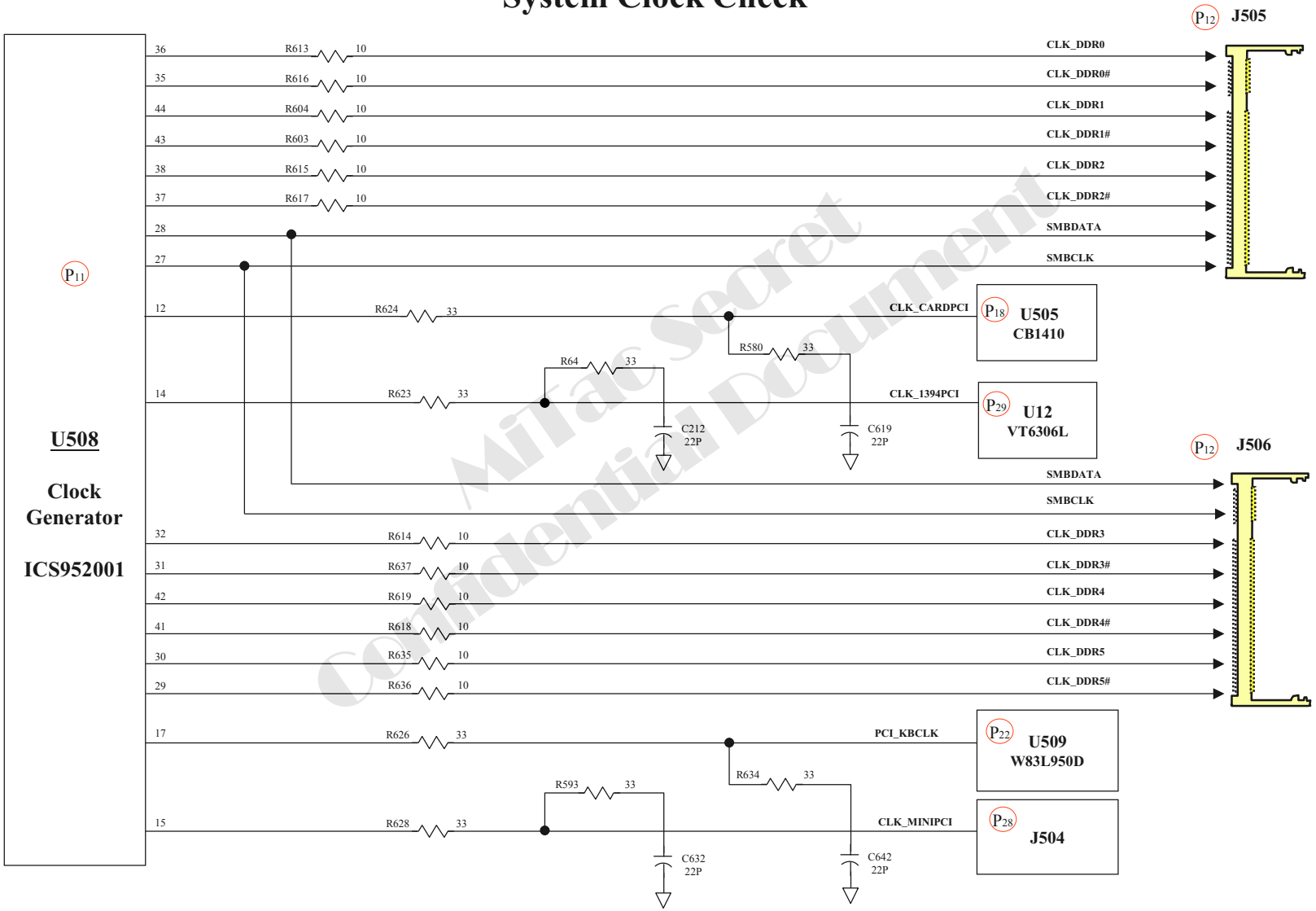
8.2 No Display

****** System Clock Check ******



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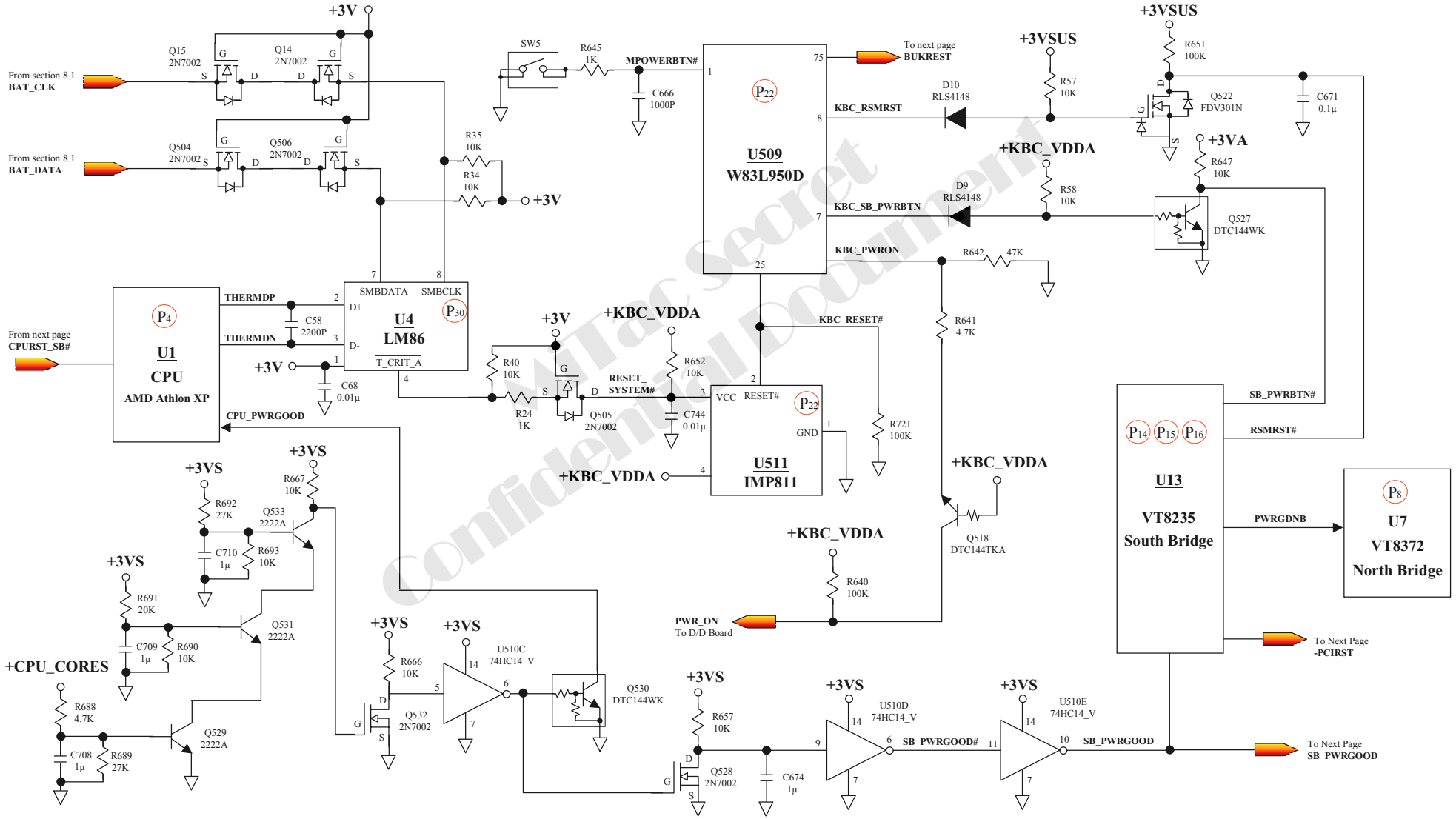
8.2 No Display

****** Power Good & Reset Circuit Check (1)******



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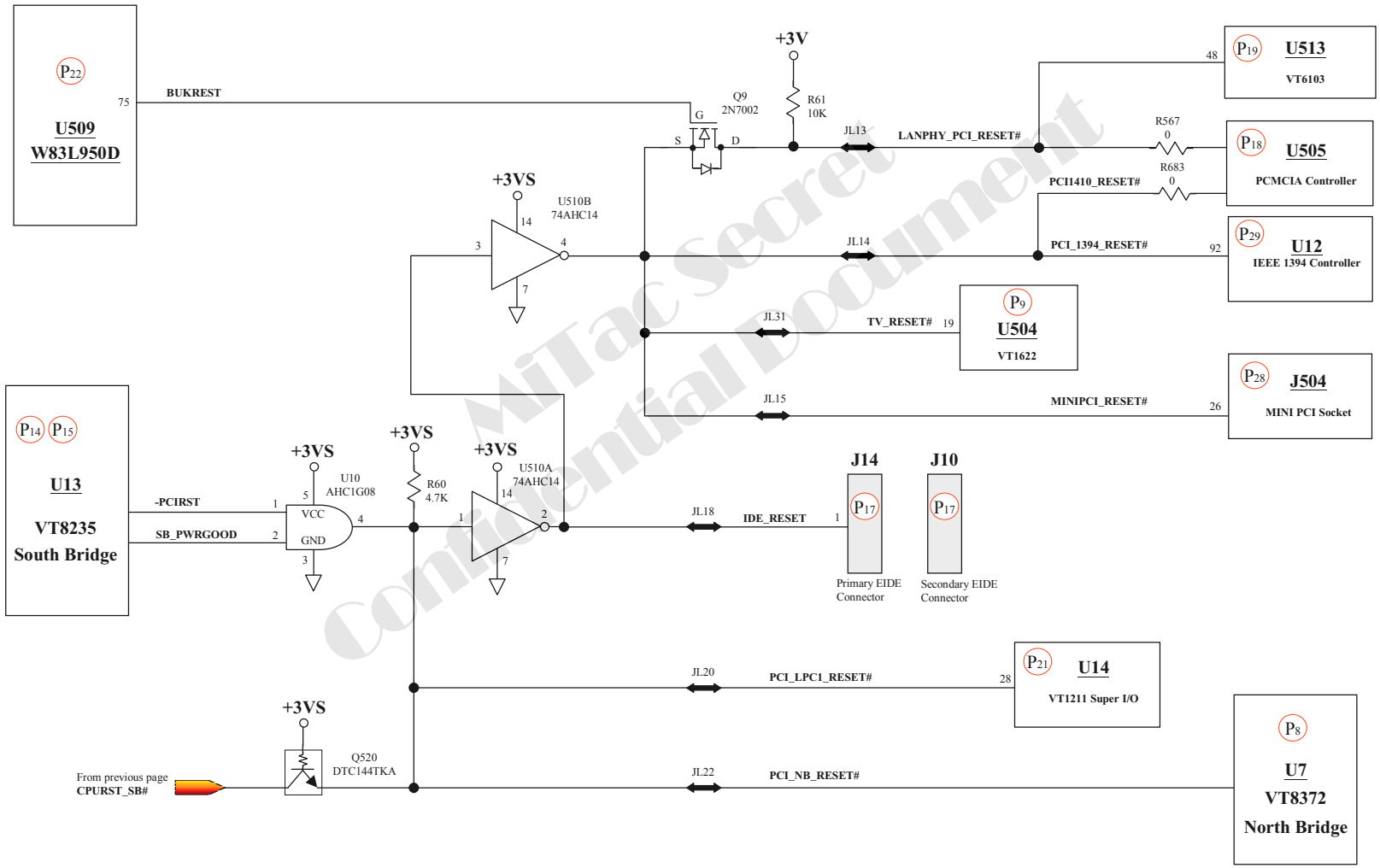
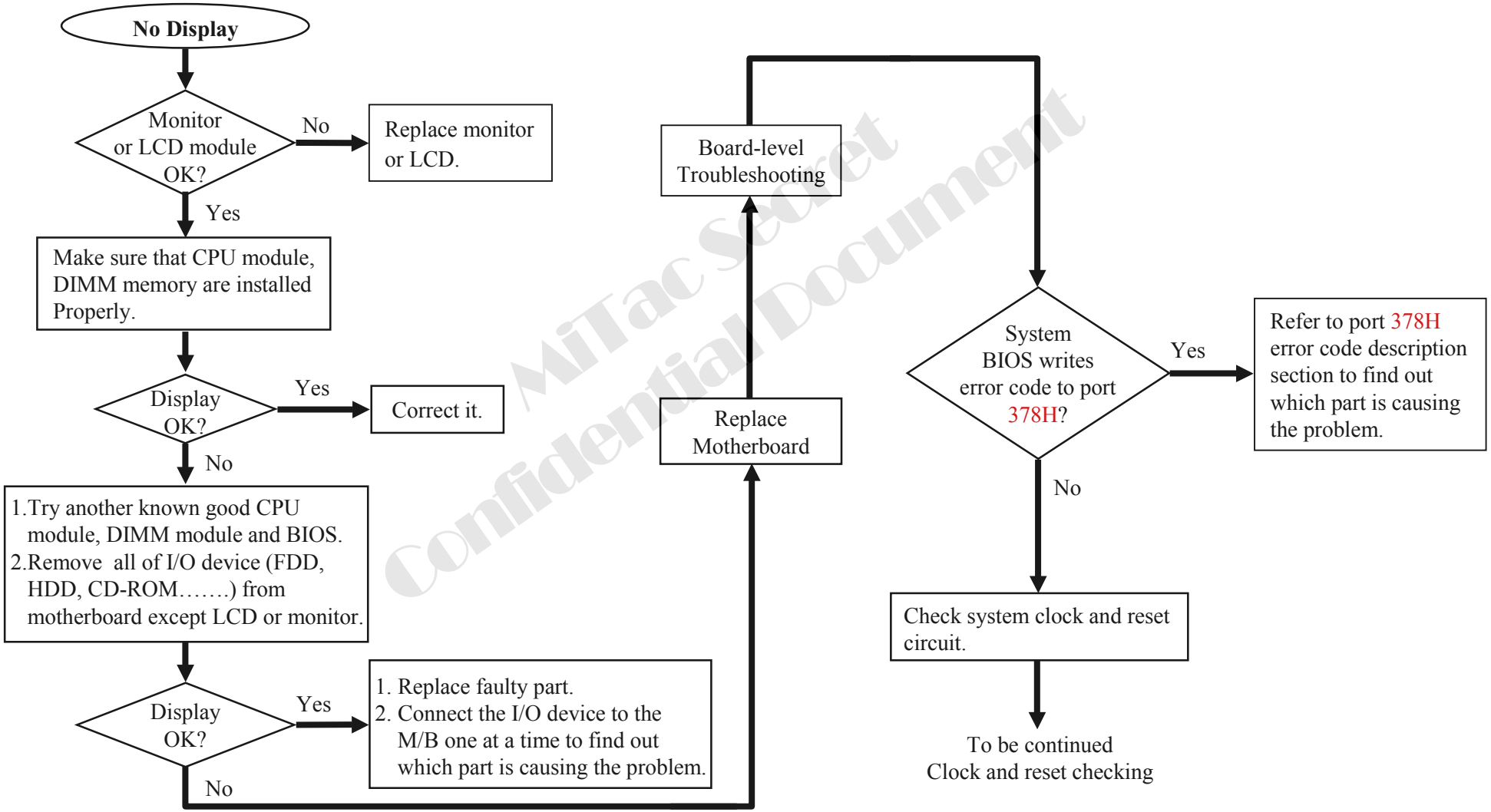
8.2 No Display

****** Power Good & Reset Circuit Check (2) ******



8.2 No Display

There is no display on both LCD and VGA monitor after power on although the LCD and monitor is known-good.



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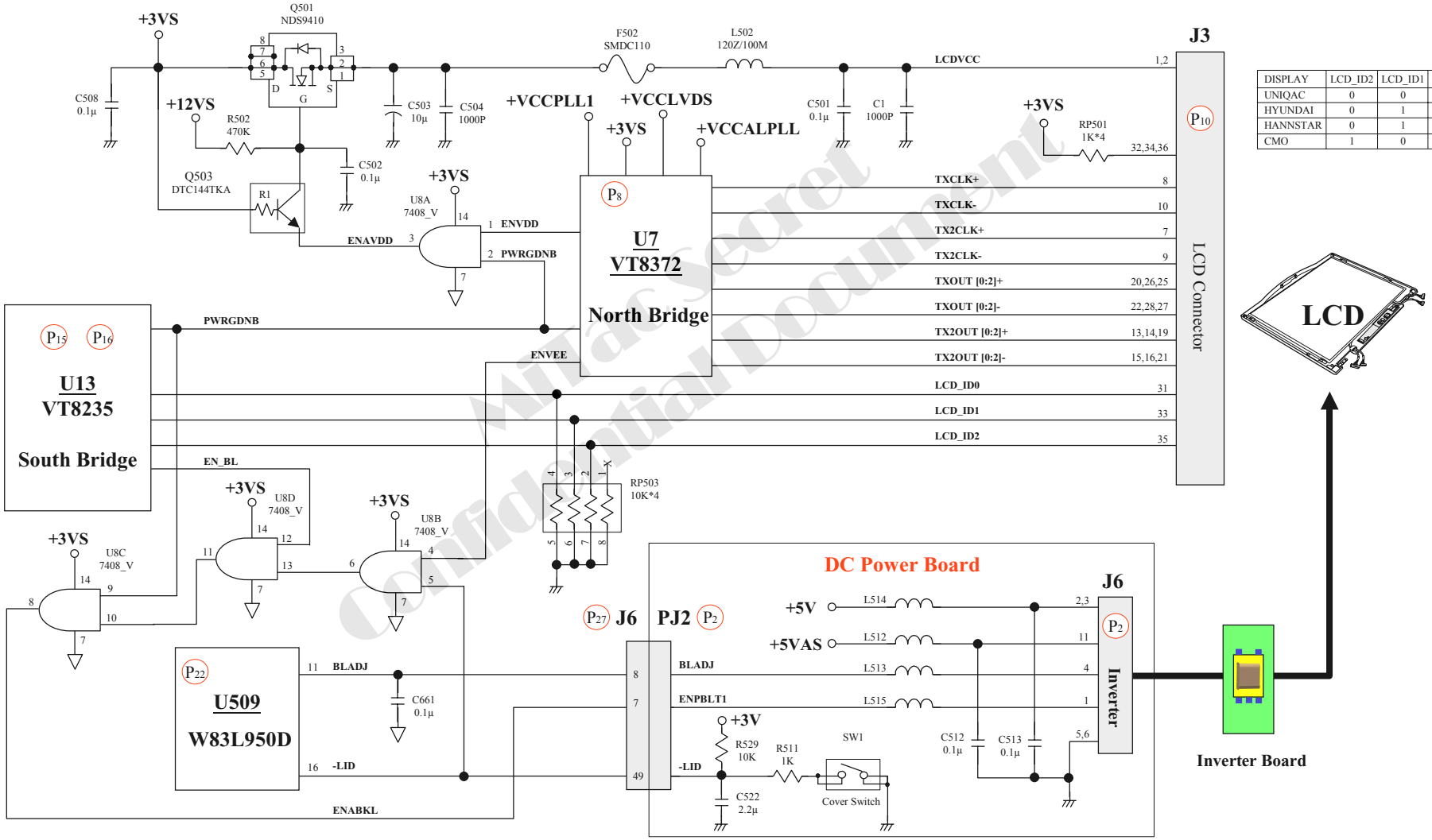
8.3 VGA Controller Failure LCD No Display

There is no display or picture abnormal on LCD although power-on-self-test is passed.



DISPLAY	LCD_ID2	LCD_ID1	LCD_ID0
UNIQAC	0	0	1
HYUNDAI	0	1	0
HANNSTAR	0	1	1
CMO	1	0	0

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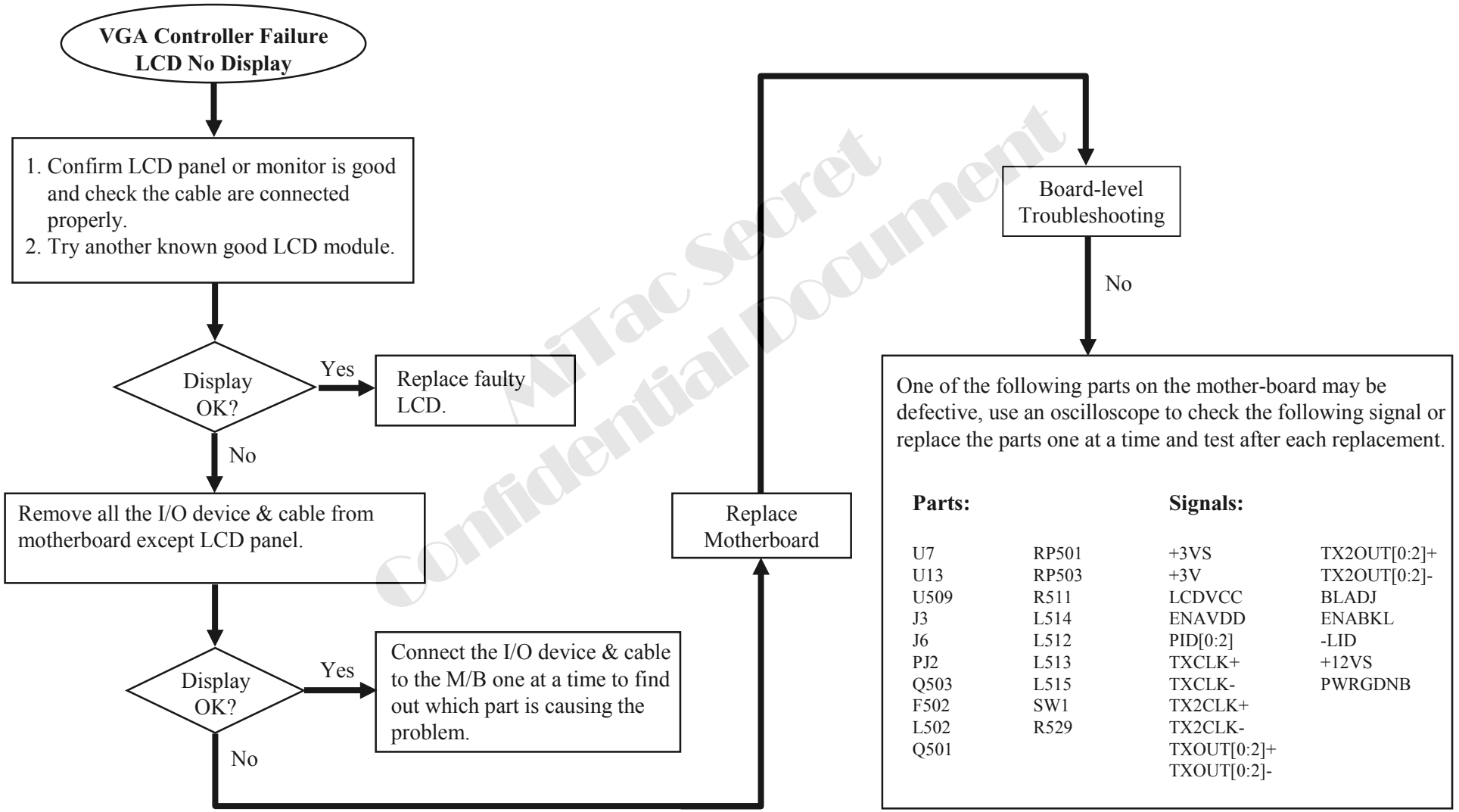
8.3 VGA Controller Failure LCD No Display

There is no display or picture abnormal on LCD although power-on-self-test is passed.



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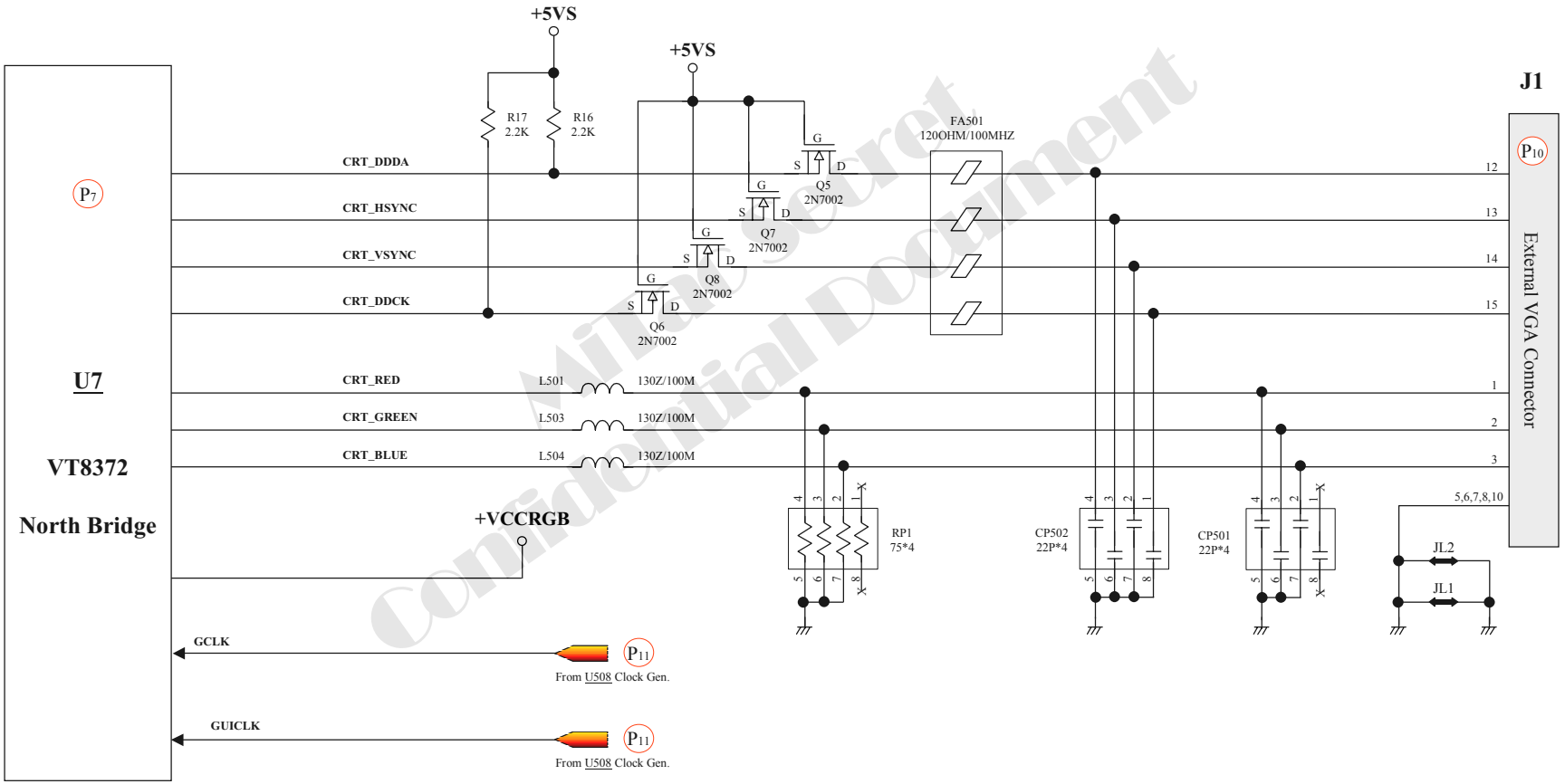
8.4 External Monitor No Display

There is no display or picture abnormal on CRT monitor, but it is OK for LCD.



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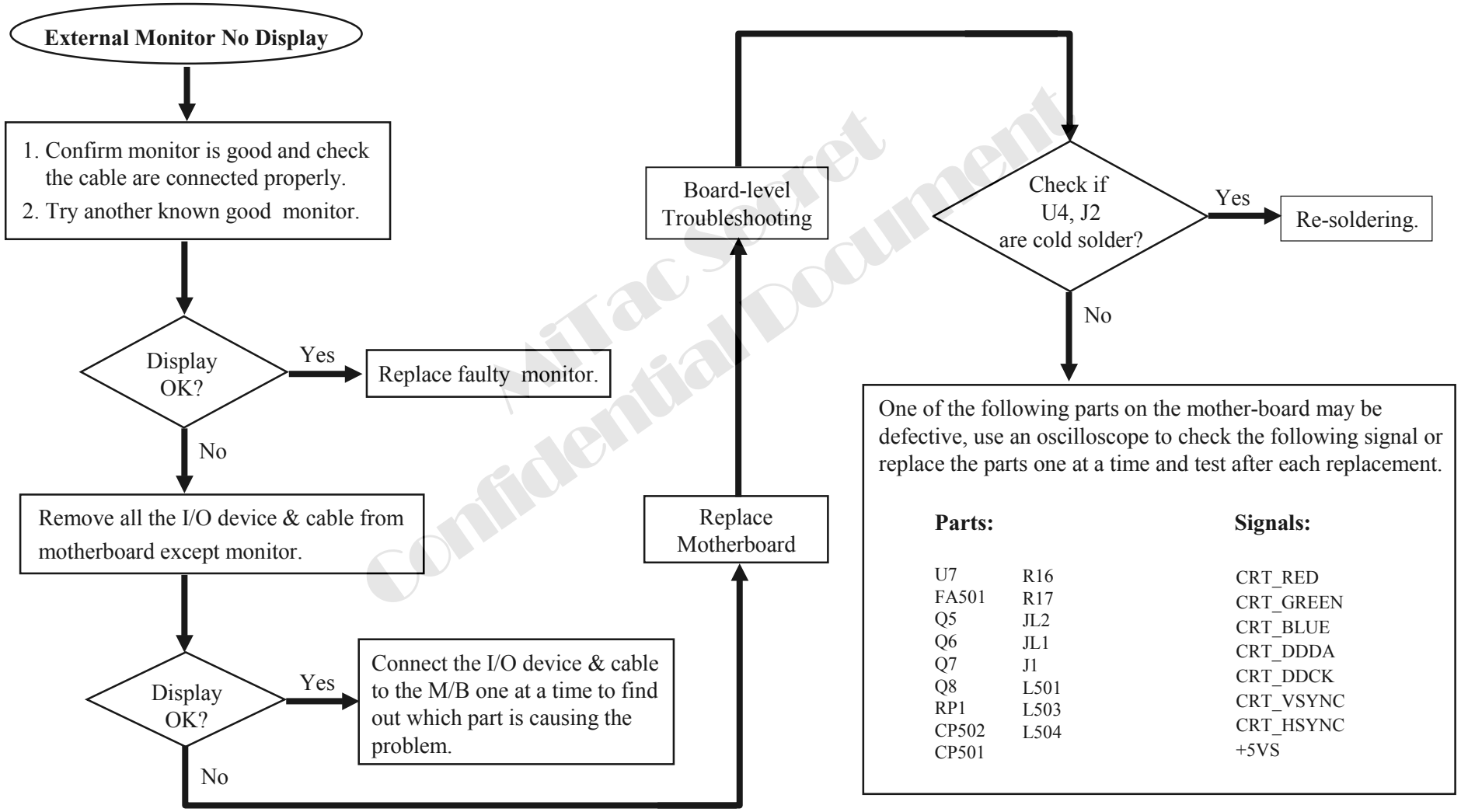
8.4 External Monitor No Display

There is no display or picture abnormal on CRT monitor, but it is OK for LCD.



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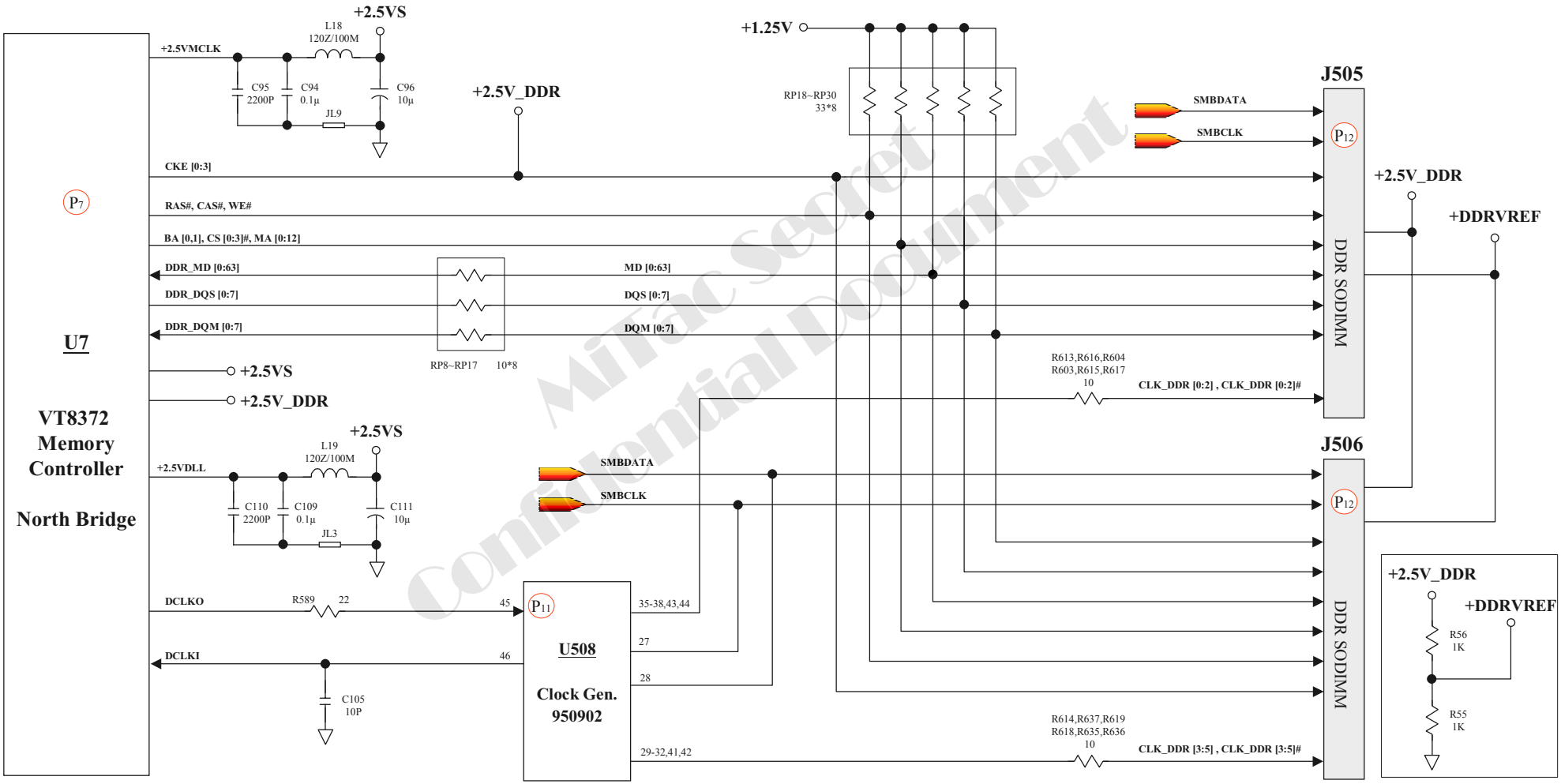
8.5 Memory Test Error

Extend SDRAM is failure or system hangs up.



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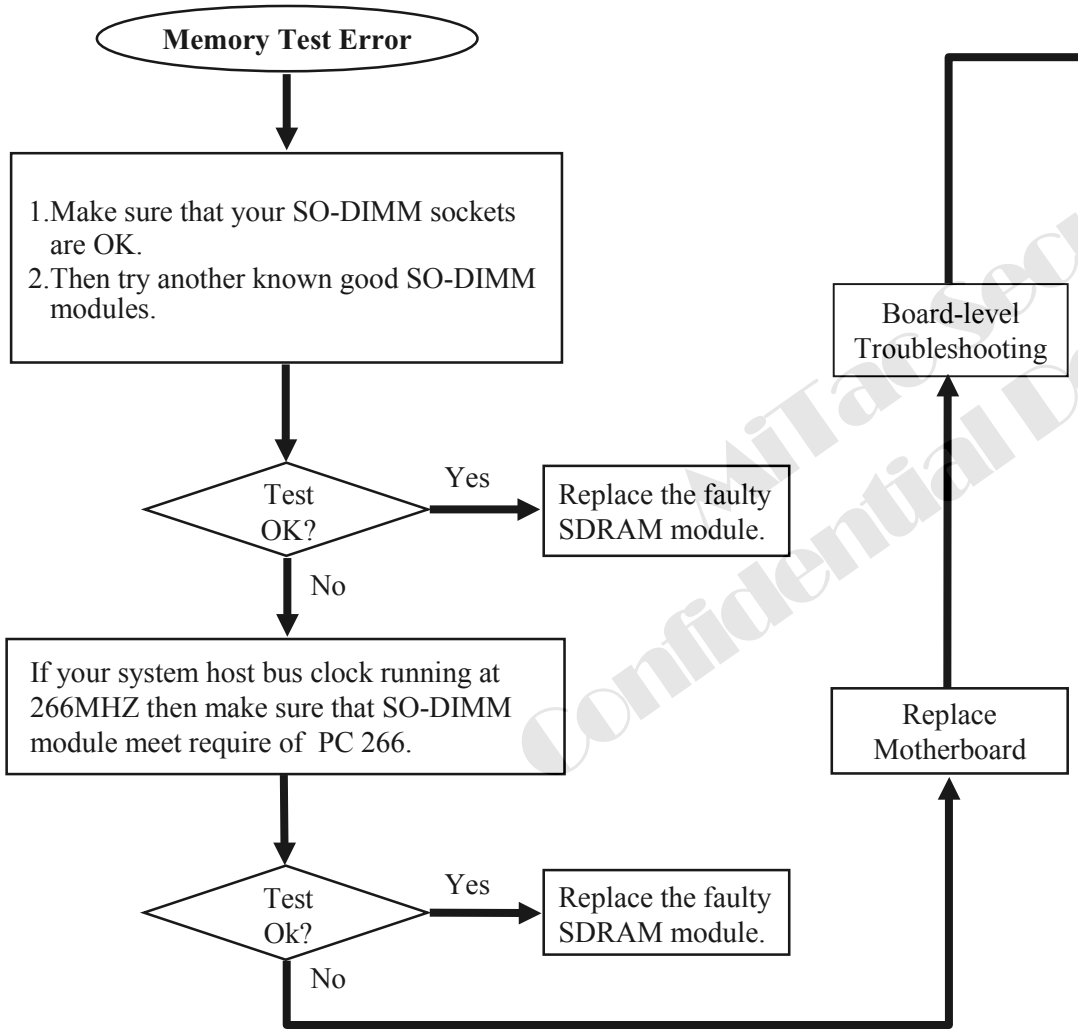

One of the following components or signals on the motherboard may be defective ,Use an oscilloscope to check the signals or replace the parts one at A time and test after each replacement.

Parts:		**Signals:**
U7	R637	+2.5V_DDR
U508	R589	+DDRVREF
J505	L19	CKE[0:3]
J506	L18	DDR_DQM[0:7]
RP18~RP30		DDR_MD[0:63]
R603		BA [0,1]
R604		CS[0:3]#
R615		MA[0:12]
R616		DDR_DQS[0:7]
R617		RAS#
R618		CAS#
R119		WE#
R614		+1.25V
R635		+2.5VS
R636		SMBDATA
		SMBCLK
		CLK_DDR[0:5]
		CLK_DDR[0:5]#

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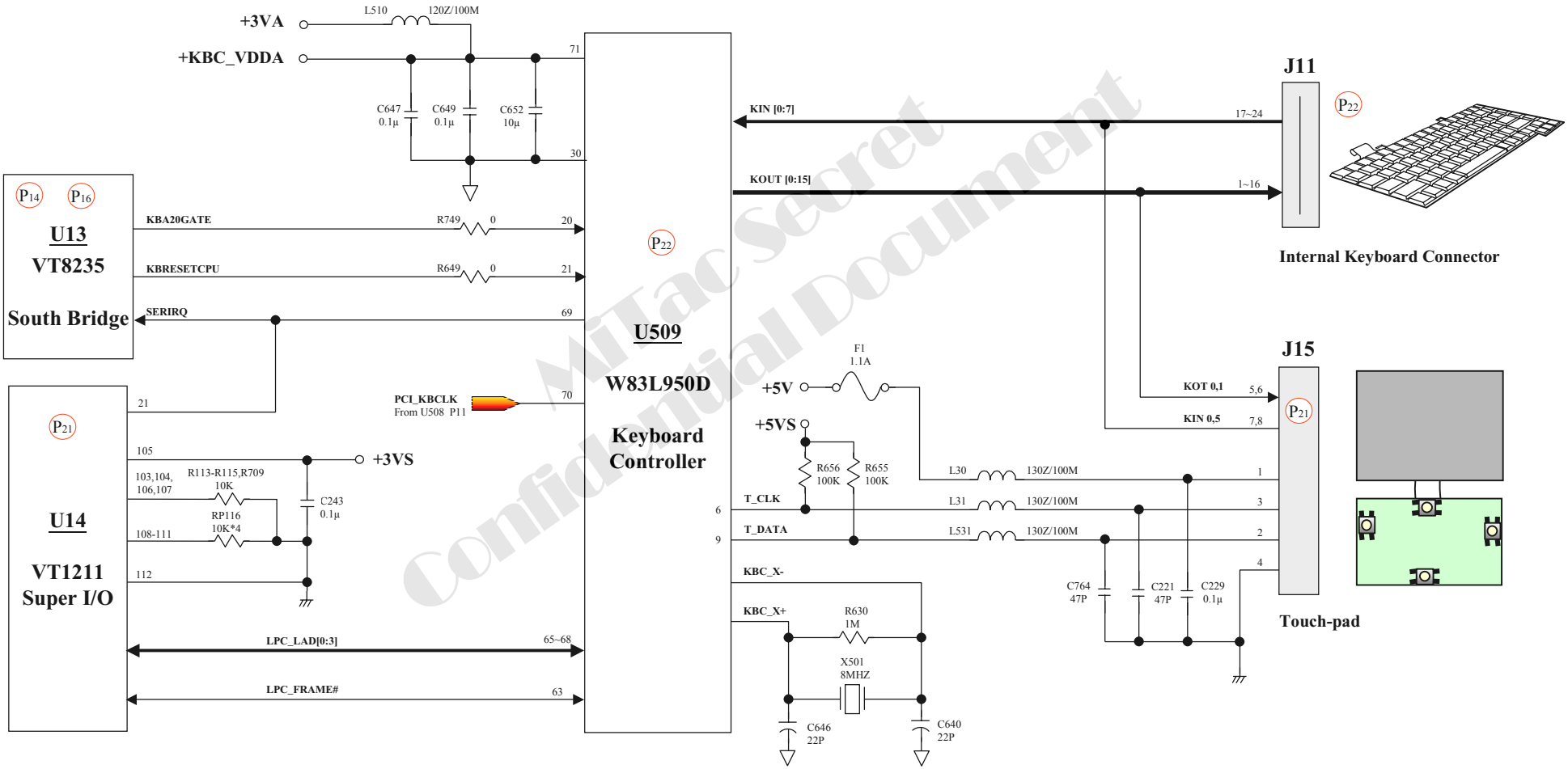
8.6 Keyboard (K/B) Touch-Pad (T/P) Test Error

Error message of keyboard or touch-pad failure is shown or any key does not work.



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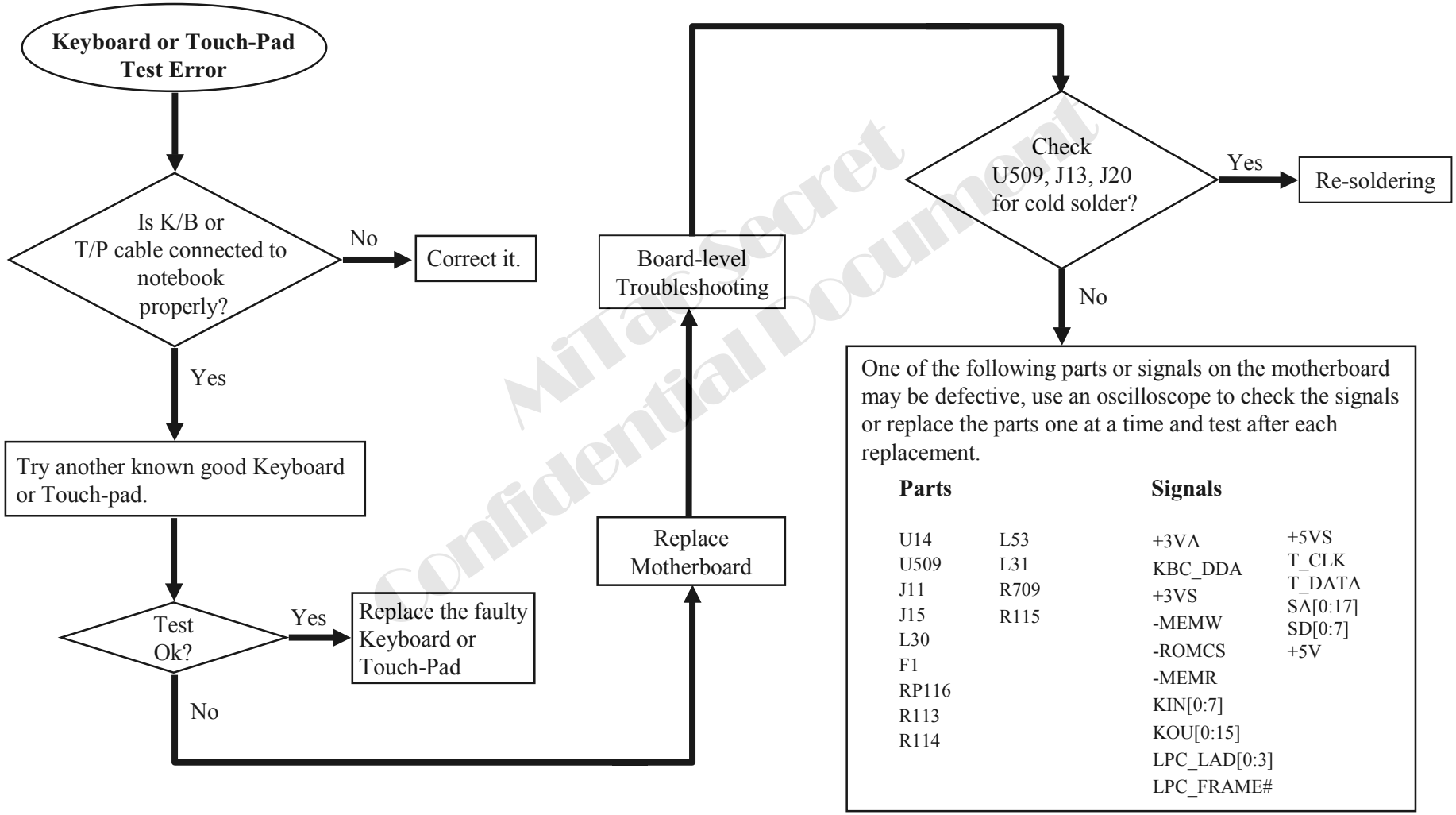

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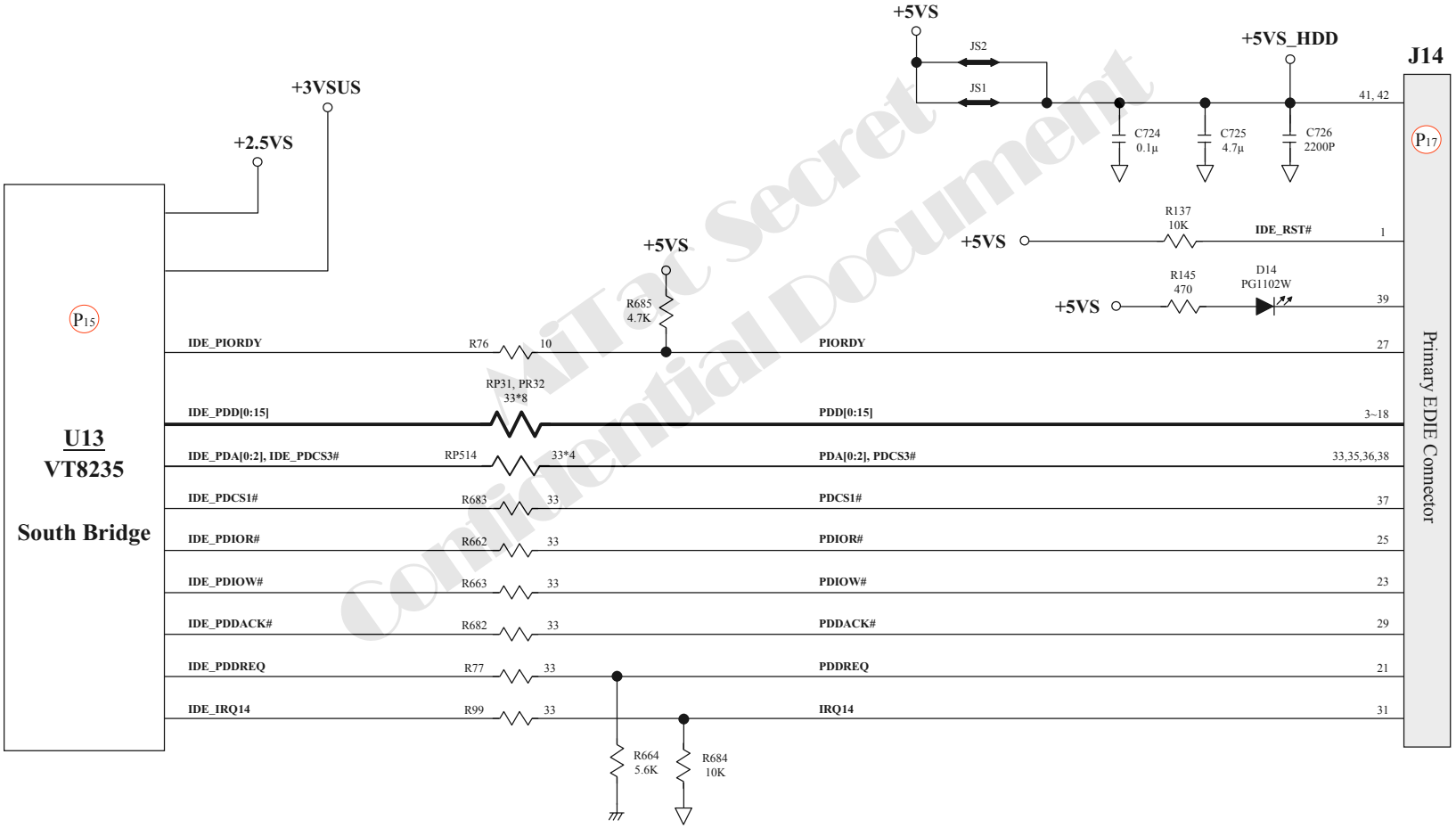
8.7 Hard Drive Test Error

Either an error message is shown, or the drive motor spins non-stop, while reading data from or writing data to hard disk.



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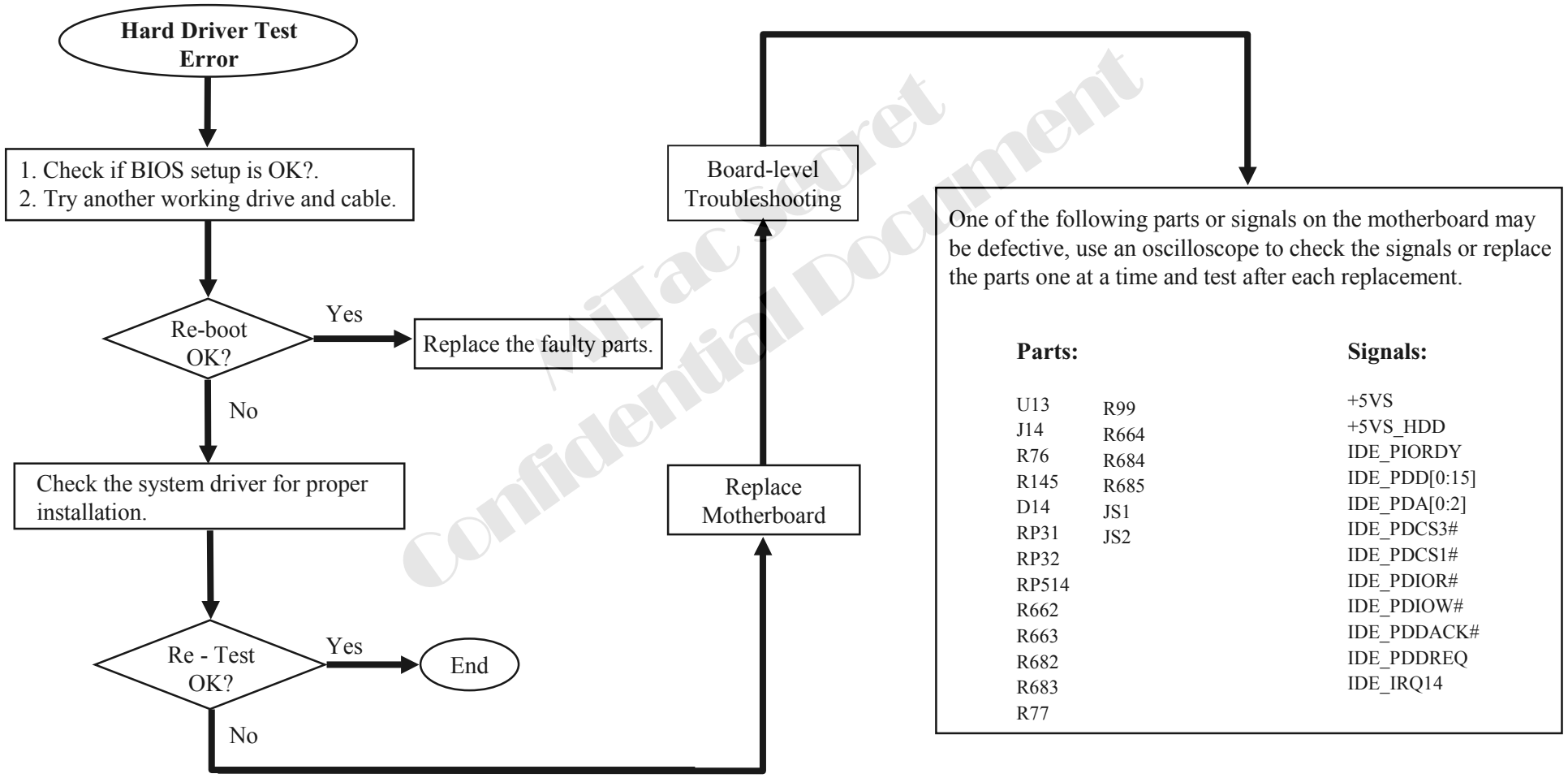

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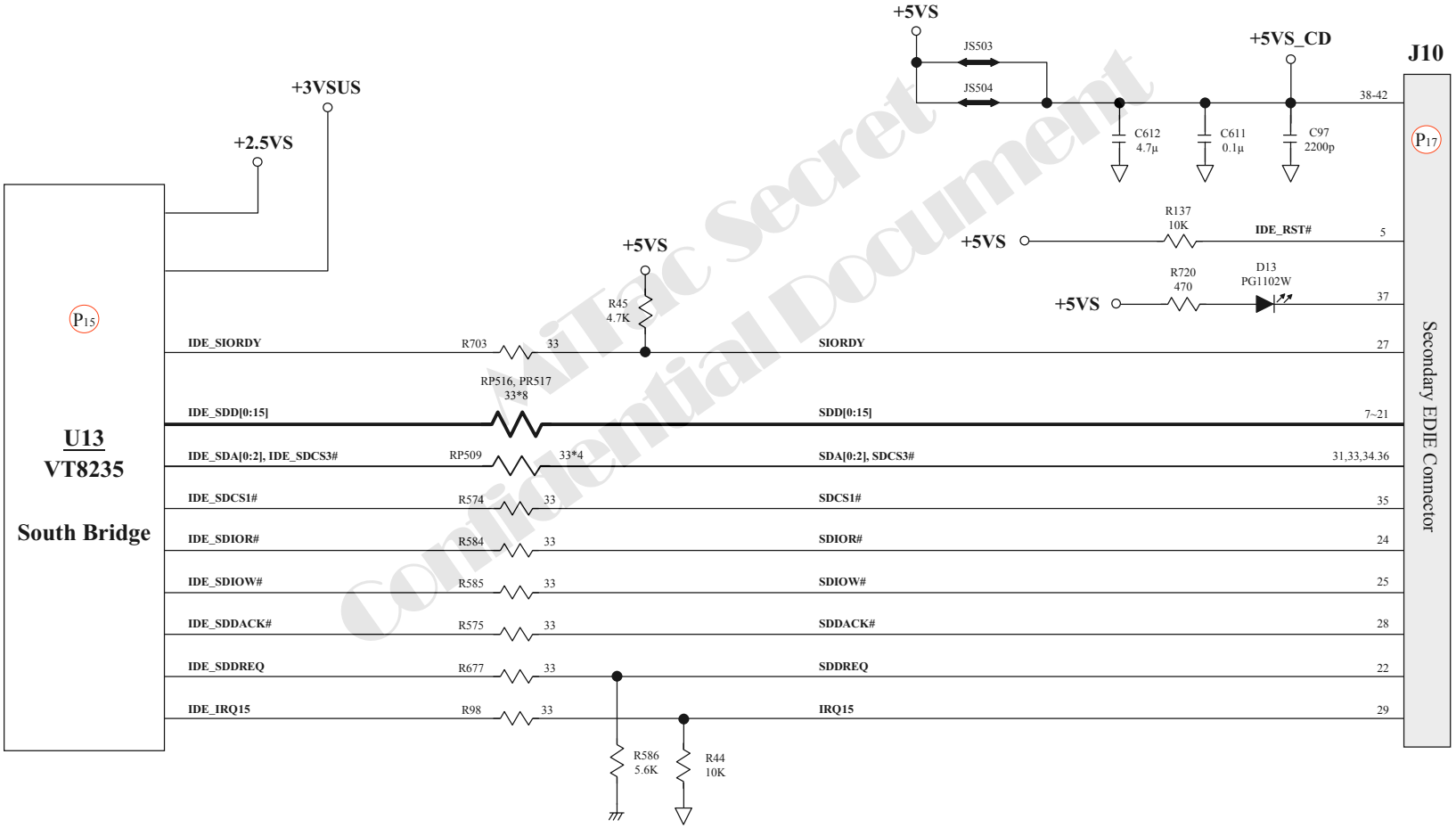
8.8 CD-ROM Drive Test Error

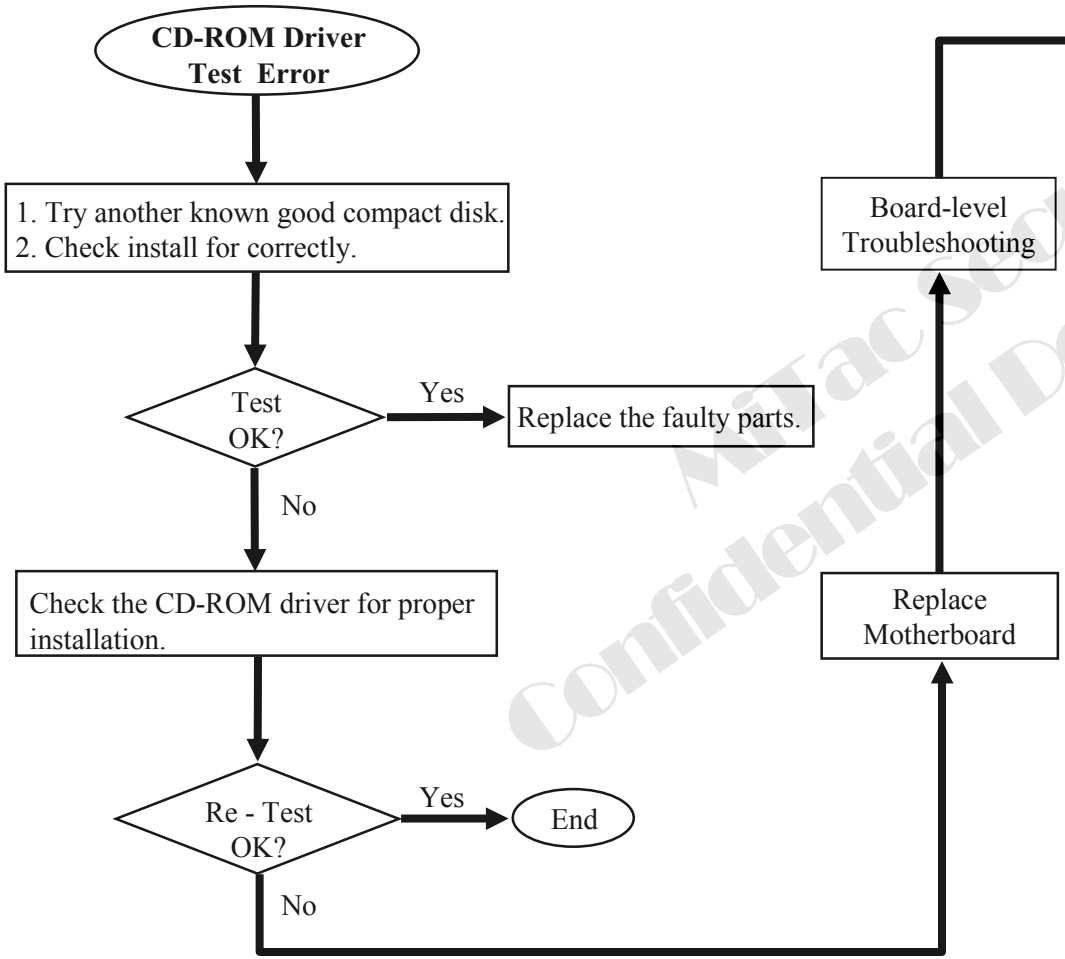
An error message is shown when reading data from CD-ROM drive.



AIPC Secret Confidential Document

8.8 CD-ROM Drive Test Error

An error message is shown when reading data from CD-ROM drive.



One of the following parts or signals on the motherboard may be defective, use an oscilloscope to check the signals or replace the parts one at a time and test after each replacement.

Parts:		**Signals:**
U13	R44	+5VS
J10	R720	+5VS_CD
R703	JS503	+3VSUS
RP516	JS504	+2.5VS
RP517	R45	IDE_SIORDY
RP509		IDE_SDD[0:15]
R574		IDE_SDA[0:2]
R584		IDE_SDCS3#
R585		IDE_SDCS1#
R575		IDE_SDIOR#
R677		IDE_SDIOW#
R98		IDE_SDDACK#
R586		IDE_SDDREQ
		IDE_IRQ15

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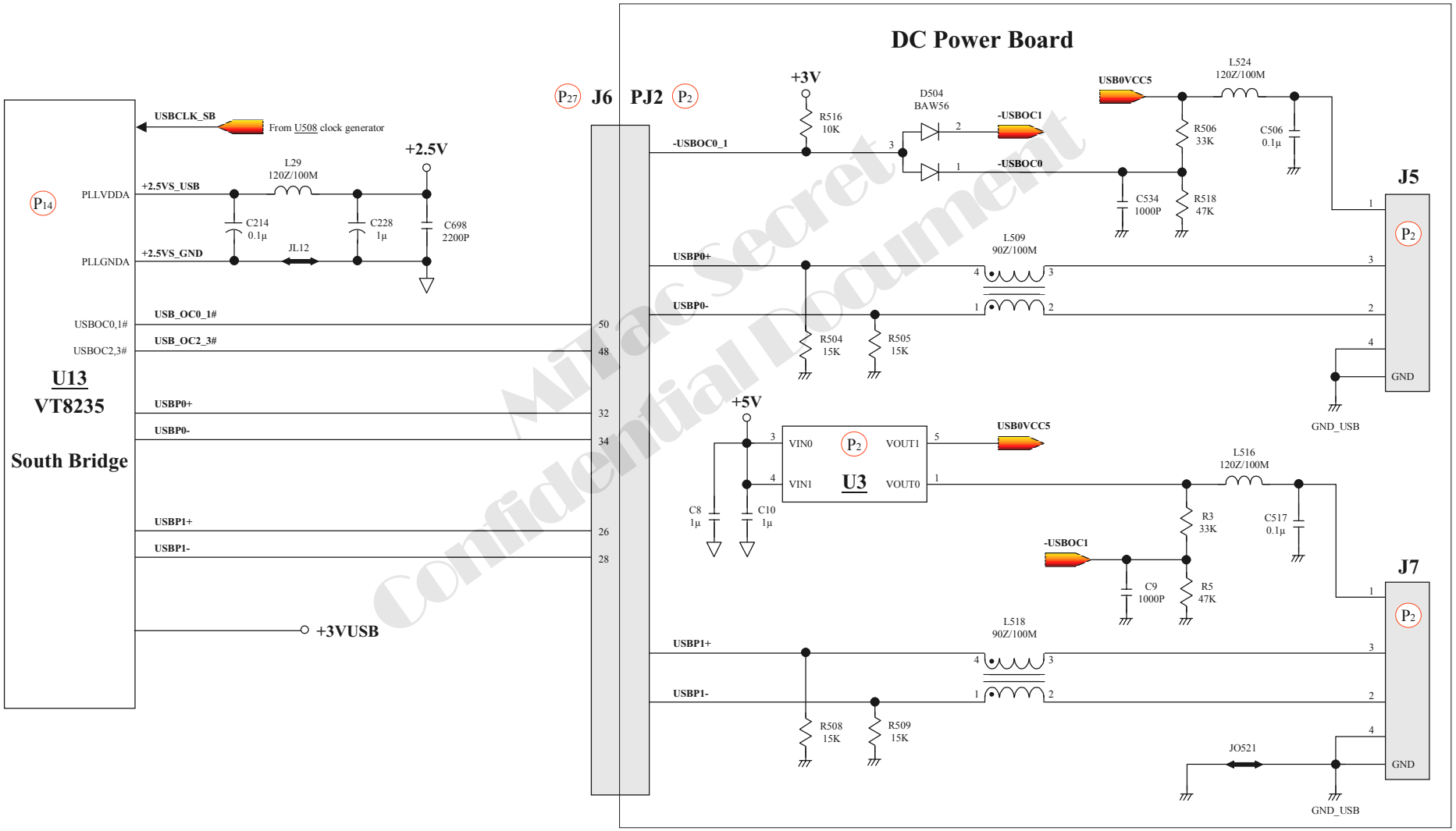
8.9 USB Test Error - 1

An error occurs when a USB I/O device is installed.



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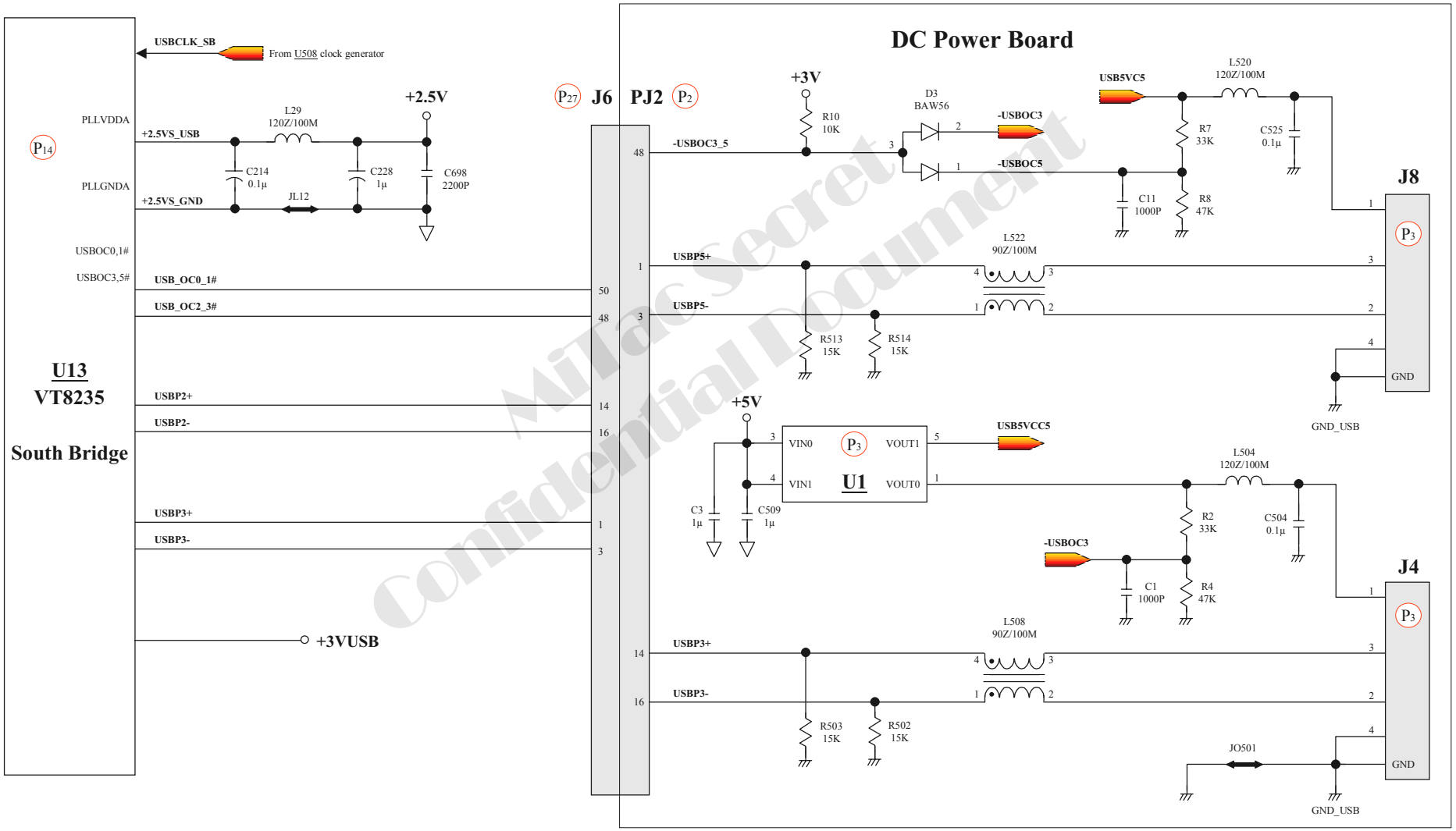
8.9 USB Test Error - 2

An error occurs when a USB I/O device is installed.



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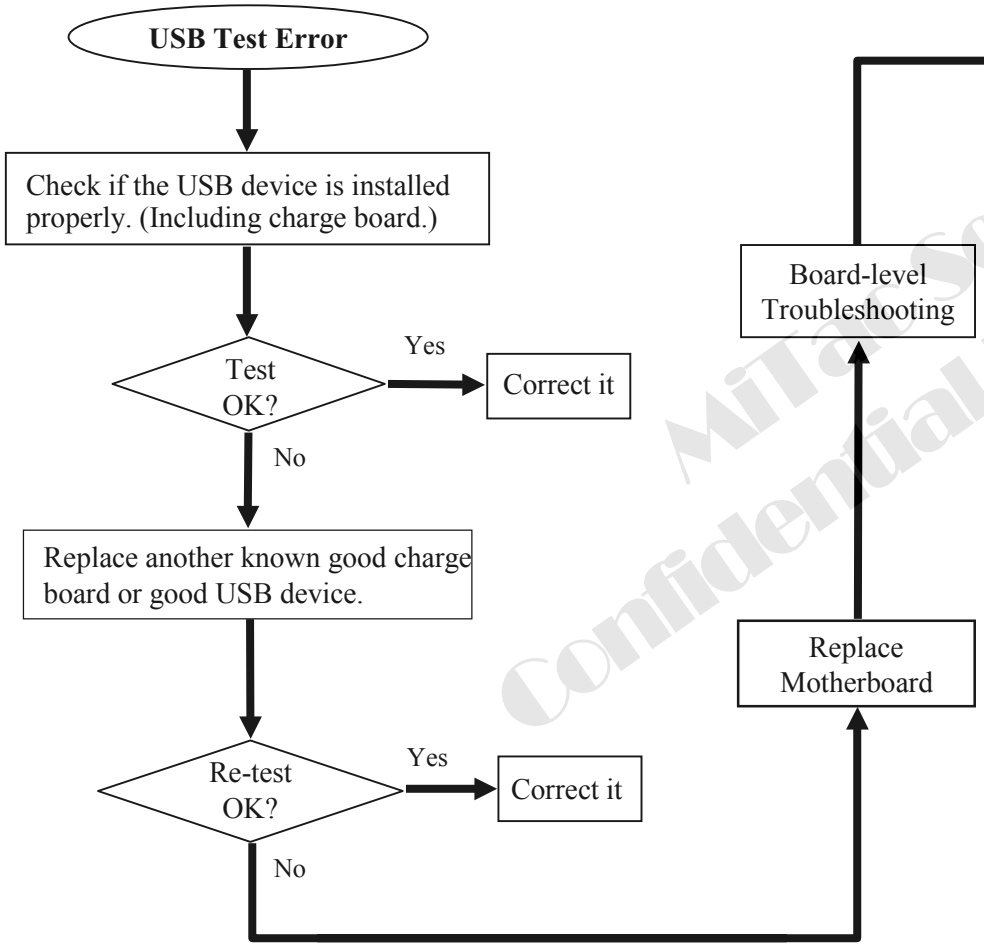
8.9 USB Test Error

An error occurs when a USB I/O device is installed.



Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:

M/B	D/D	
U13	U1	U3
J6	PJ2	J8
L29	J4	JO501
R49	J5	JO521
R51	J7	D3
R669	D504	L520
R670	L524	L522
C214	L509	L504
C228	L516	L508
C698	L518	

Signals:

+3V	-USBOC2_3
USBCLK_SB	USBP2+
-USBOC0_1	USBP2-
USBP0+	USB5VCC5
USBP0-	USBP3+
USB0VCC5	USBP3-
USBP1+	
USBP1-	

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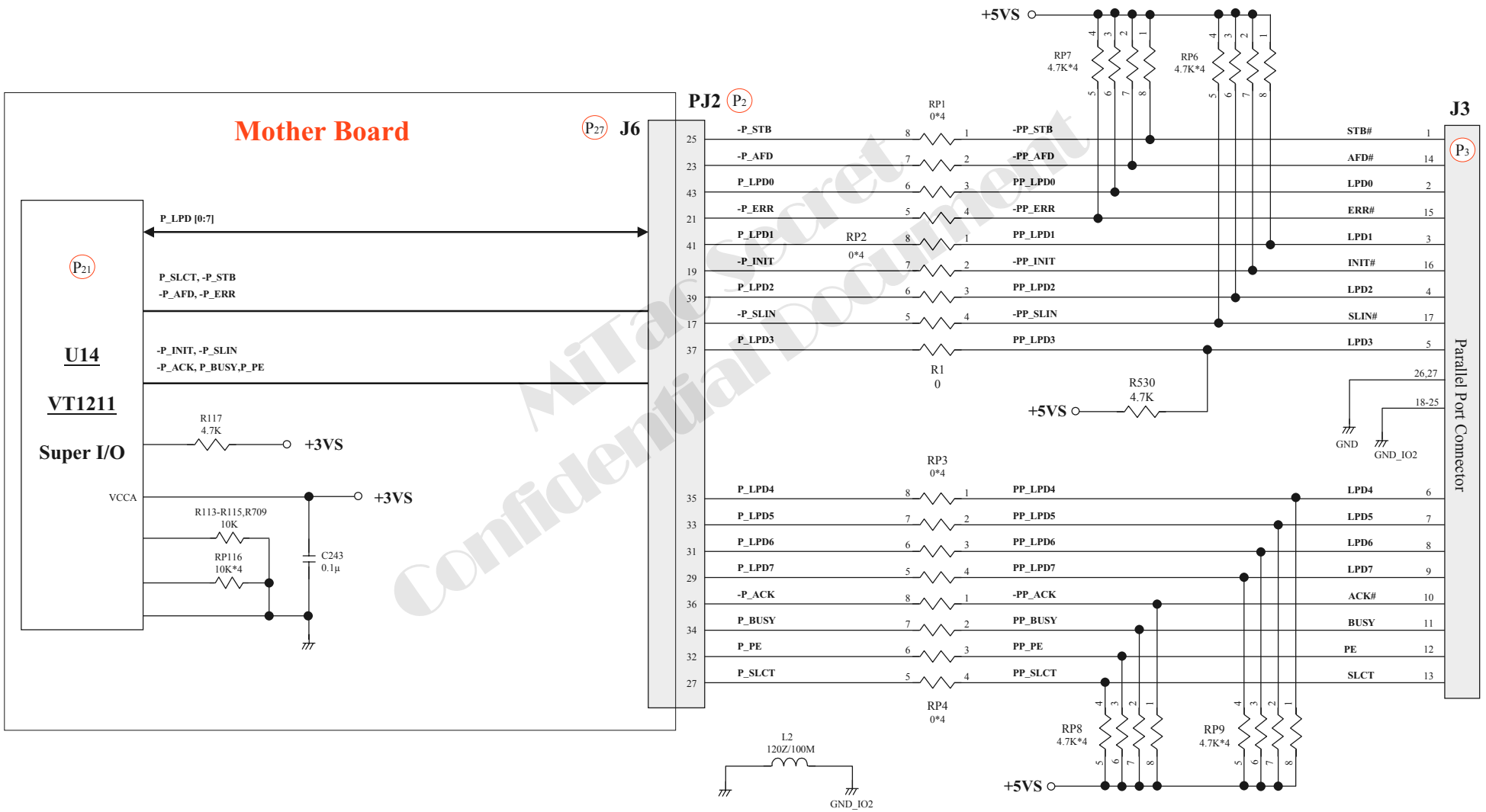
8.10 PIO Port Test Error

When a print command is issued, printer prints nothing or garbage.



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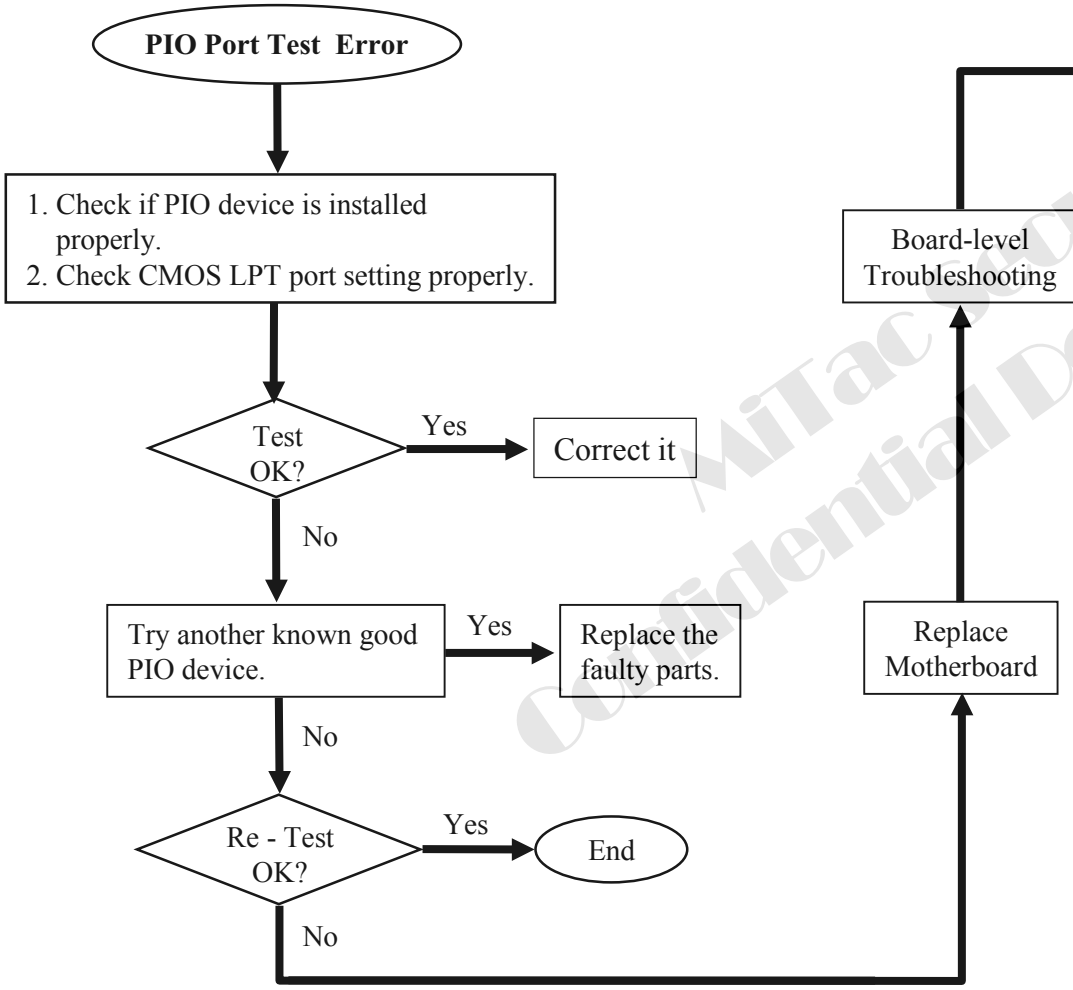
8.10 PIO Port Test Error

When a print command is issued, printer prints nothing or garbage.



One of the following parts or signals on the motherboard may be defective, use an oscilloscope to check the signals or replace the parts one at a time and test after each replacement.

Parts:		**Signals:**	
M/B	D/D		
U14	PJ2	+3VS	-P_STB
J6	RP6	P_LPD0	-P_AFD
R117	RP7	P_LPD1	-P_ERR
R[113:115]	RP8	P_LPD2	-P_INIT
R709	RP9	P_LPD3	-P_SLIN
RP116	J3	P_LPD4	-P_ACK
C243	RP1	P_LPD5	P_BUSY
	RP2	P_LPD6	P_PE
	R1	P_LPD7	P_SLCT
	RP3		
	RP4		
	D1		

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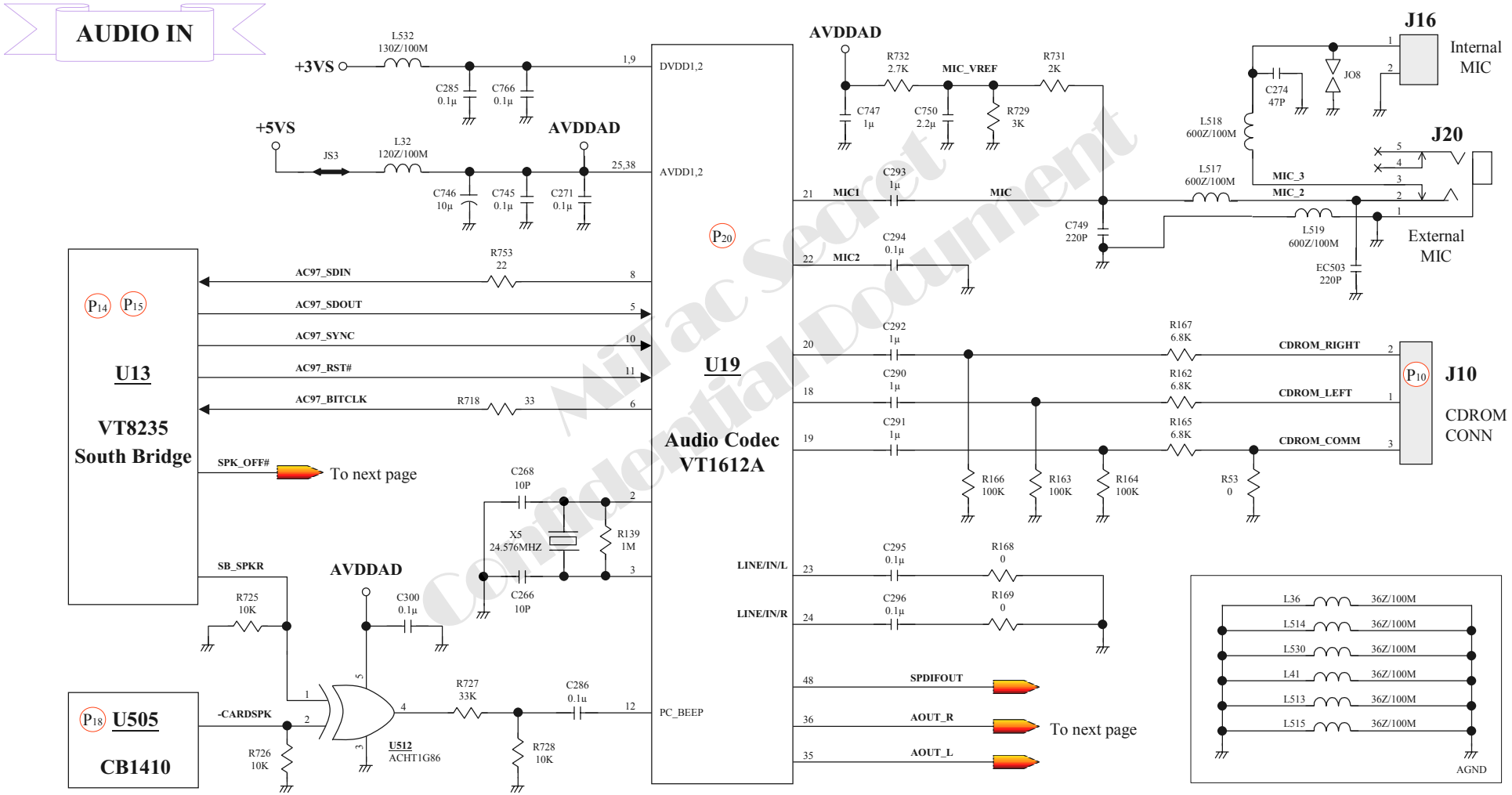
8.11 Audio Failure

No sound from speaker after audio driver is installed.



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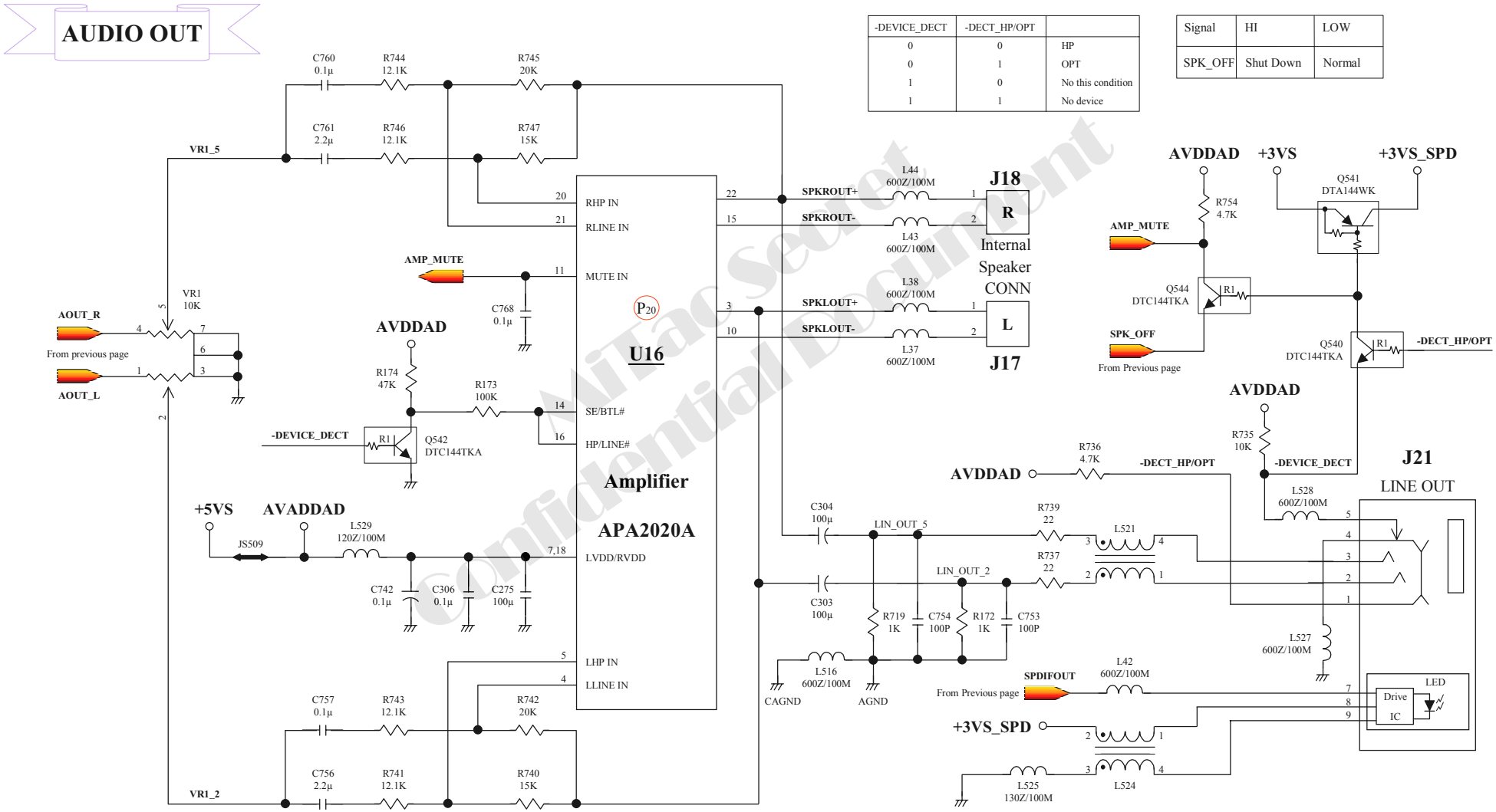
8.11 Audio Failure

No sound from speaker after audio driver is installed.



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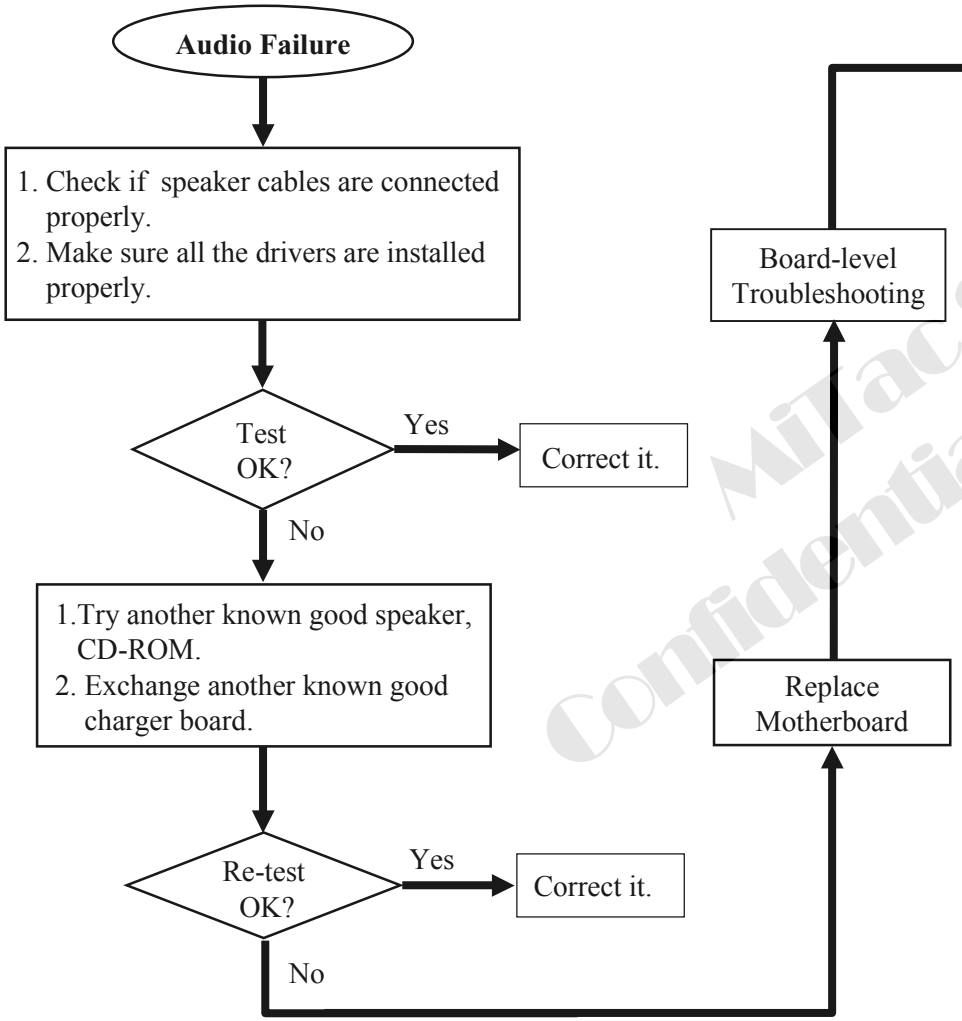
8.11 Audio Failure

No sound from speaker after audio driver is installed.



Check the following parts for cold solder or one of the following parts on the motherboard may be defective,use an oscilloscope to check the following signal or replace parts one at a time and test after each replacement.

1.If no sound cause of line out, check the following parts & signals:

Parts:	Signals:
U16	AOUT_R
U13	AOUT_L
U19	+3VS
VR1	AVDDAD
L516	+3VS_SPD
L524	SPK_OFF
L525	SPDIFOUT
Q540	
Q544	
J21	

2. If no sound cause of MIC, check the following parts & signals:

Parts:	Signals:
U13	+5VS
U19	+3VS
J16	AVDDAD
J20	MIC
L517	MIC1
L518	MIC2
L519	

3. If no sound cause of CD-ROM, check the following parts & signals:

Parts:	Signals:
U13	CDROM_LEFT
U19	CDROM_RIGHT
J10	CDROM_COMM
R167	
R162	
R165	

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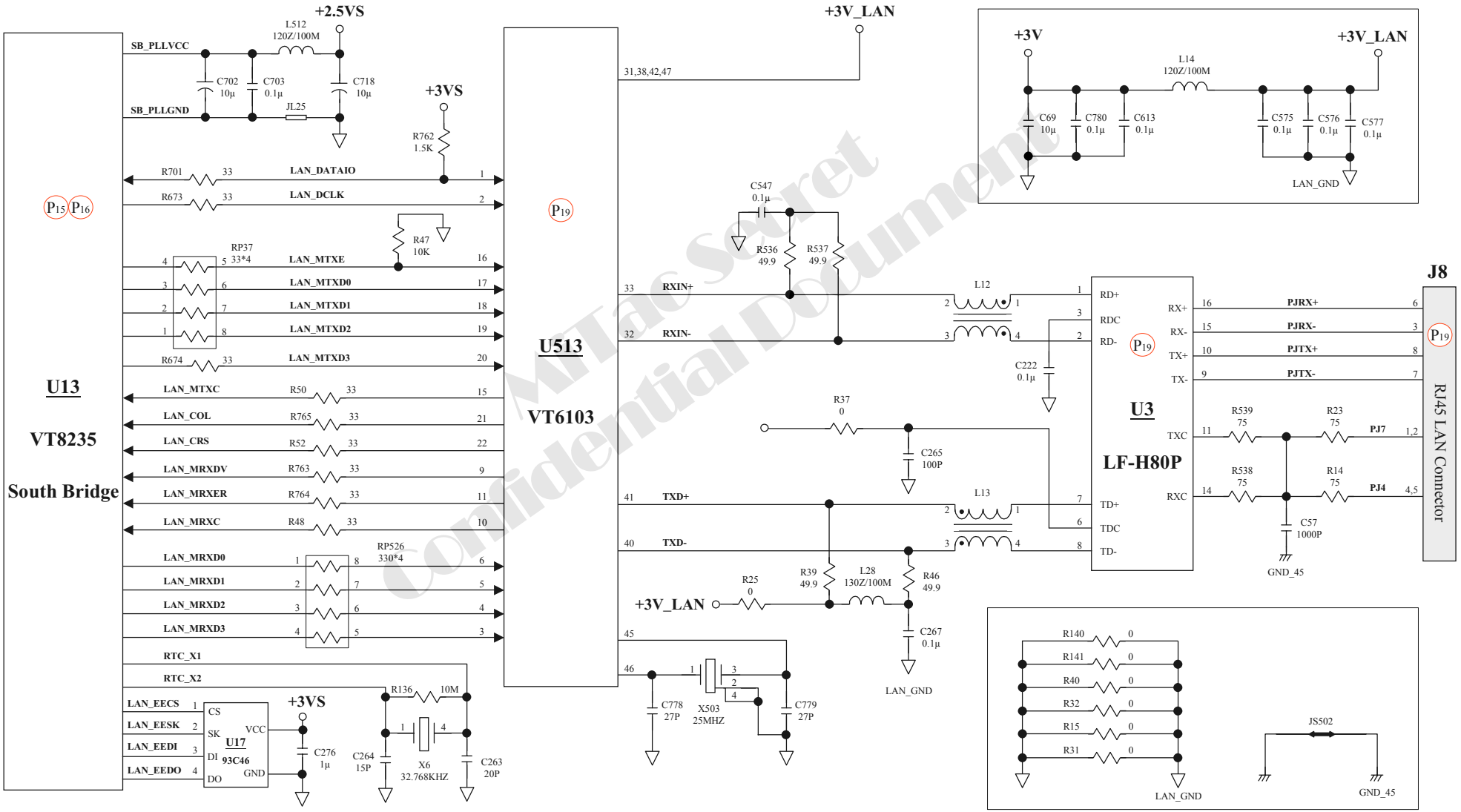
8.12 LAN Test Error

An error occurs when a LAN device is installed.



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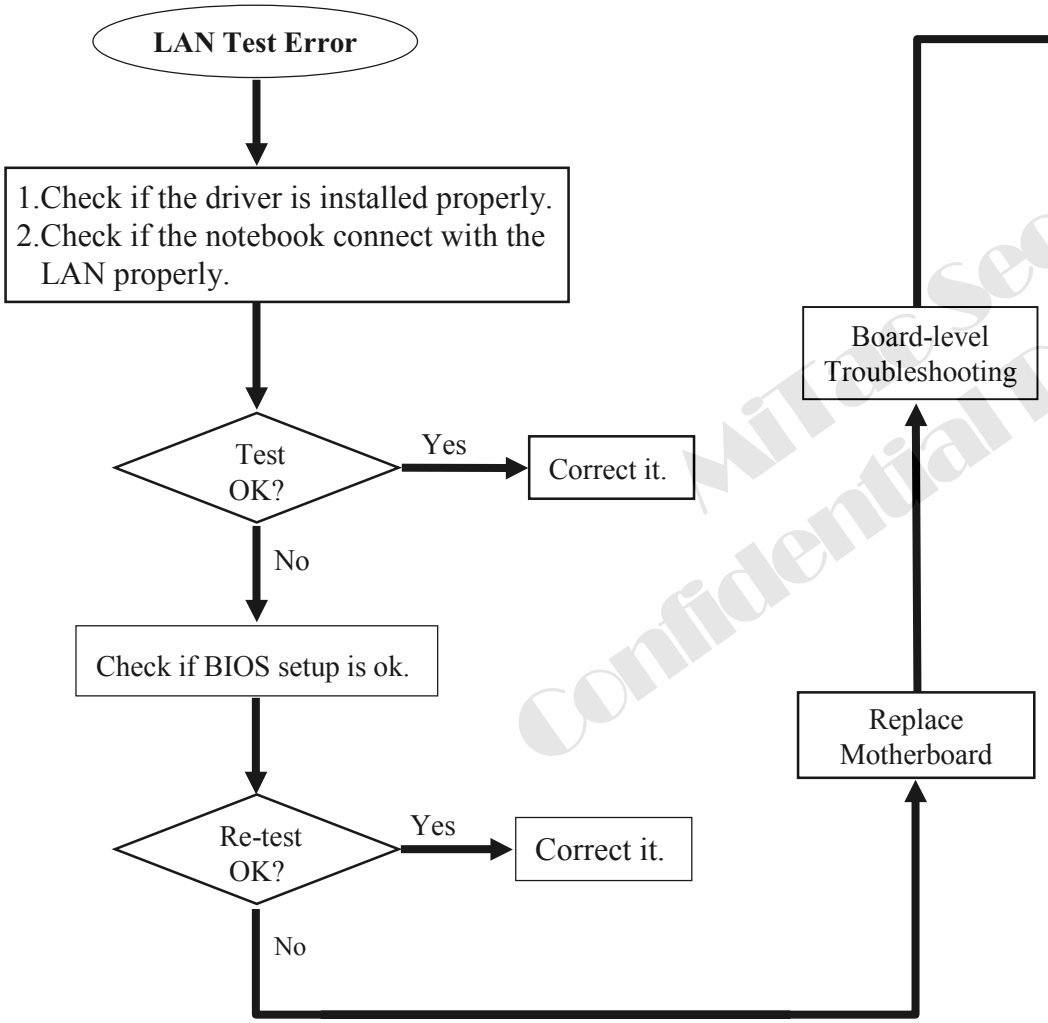
8.12 LAN Test Error

An error occurs when a LAN device is installed.



Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:		**Signals:**	
U14	R50	+3VS	RXIN+
U513	R765	+3V_LAN	RXIN-
U3	R52	LAN_DATAIO	+2.5VS
J8	R763	LAN_DCLK	TXD+
L12	R764	LAN_MTXD[0:3]	TXD-
L13	R46	LAN_MTXE	PJRX+
L28	R136	LAN_MTXC	PJRX-
L14	R25	LAN_COL	PJTX+
X6	R539	LAN_CRS	PJTX-
X503	R23	LAN_MRXDV	PJ7
RP37	R538	LAN_MRXER	PJ4
L512	R39	LAN_MRXC	+3V
RP526	R37	LAN_MRXD[0:3]	
R701	R536	RTC_X1	
R673	R537	RTC_X2	
R674	U17		

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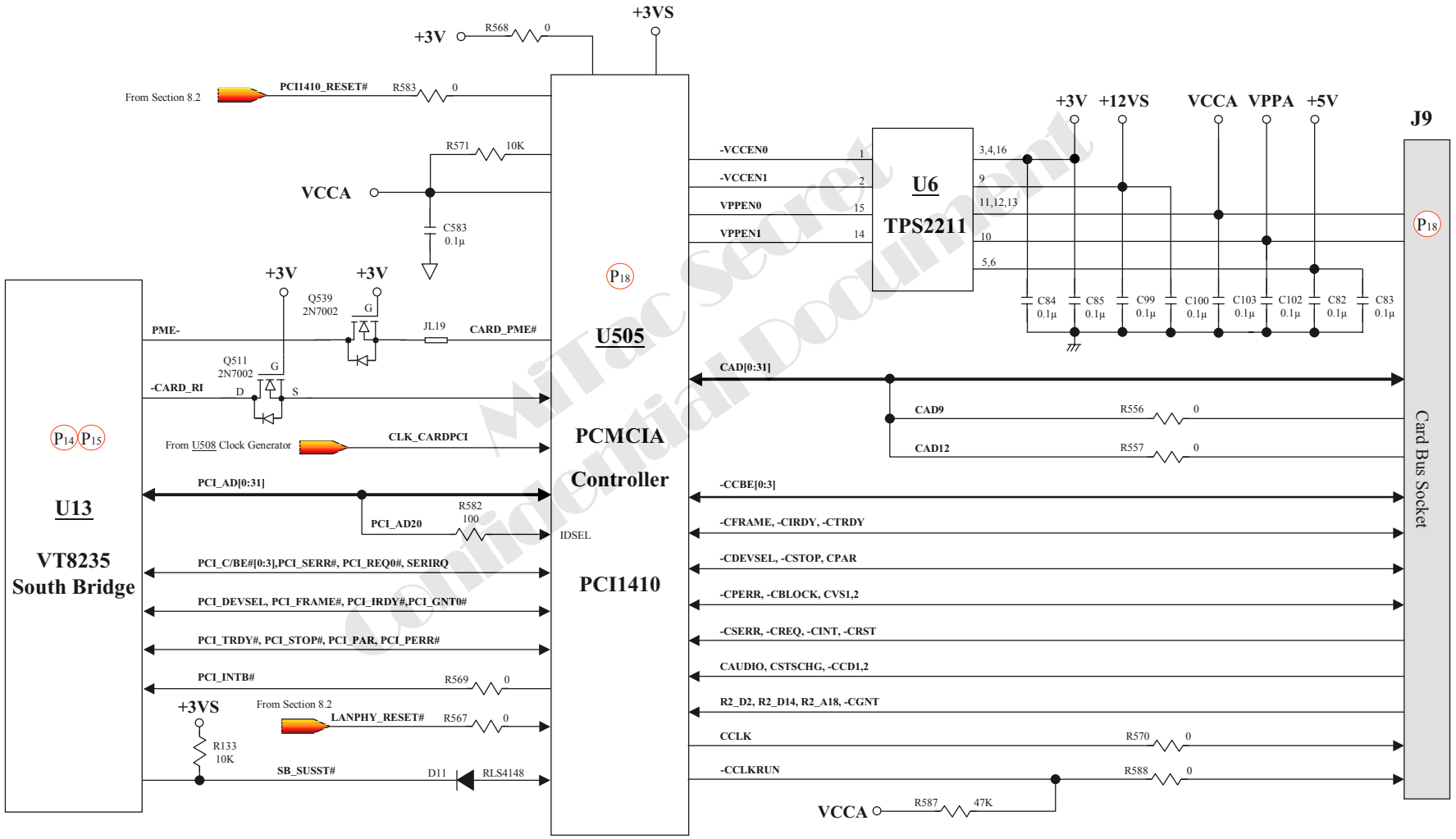
8.13 PC Card Socket Failure

An error occurs when a PC card device is installed.



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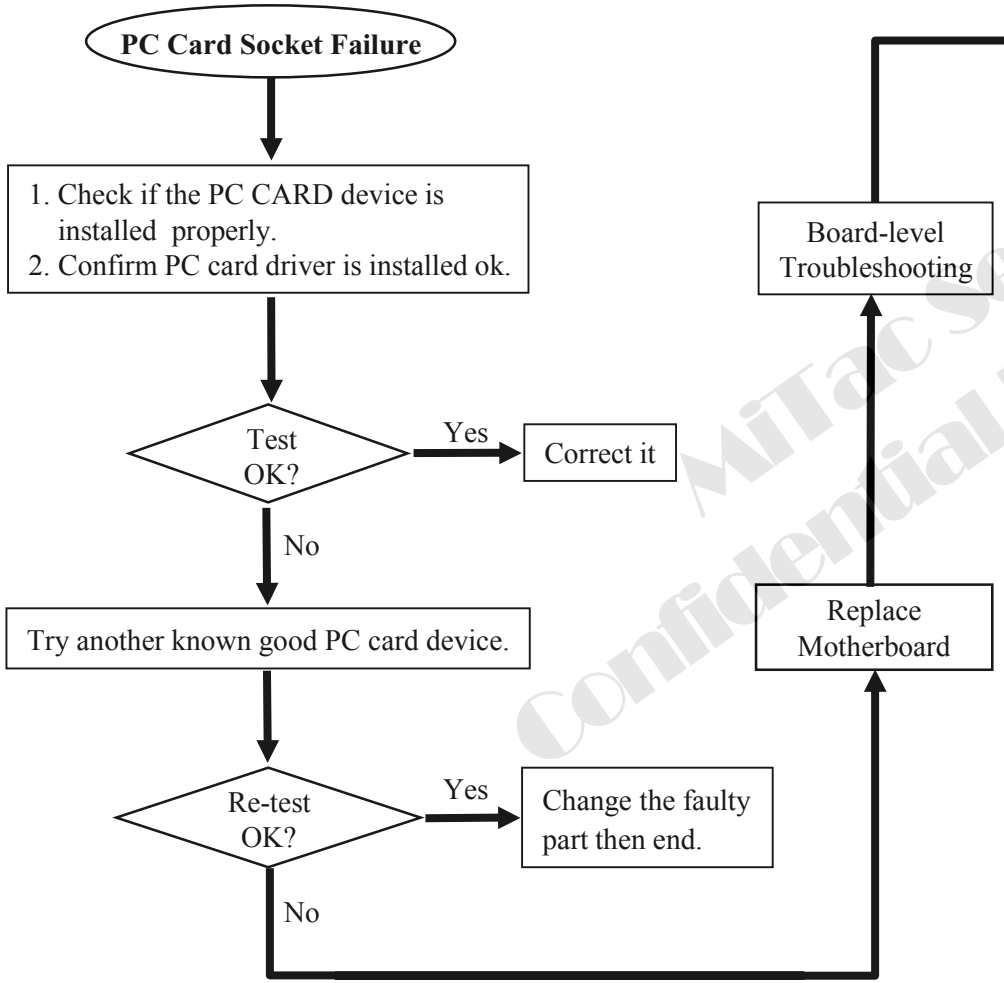
8.13 PC Card Socket Failure

An error occurs when a PC card device is installed.



Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:	Signals	
U13	PCI_AD[0:31]	PCI_SERR#
U505	PCI_C/BE# [0:3]	CARD_PME#
U6	PCI_REQ0#	SERIRQ
U505	PCI_FRAME#	-CARD_RI
J9	PCI_IRDY#	CLK_CARDPCI
Q511	PCI_TRDY#	-VCCEN0
D11	PCI_DEVSEL#	-VCCEN1
U508	PCI_STOP#	-VPPEN0
R570	PCI_INTC#	-VPPEN1
R587	CLK_CARDPCI	+3VS
R588	PCI_GNT0#	VCCA
R557	PCI_PAR	VPPA
R556	PCI_PERR#	+12VS
R569		+3V
		+5V

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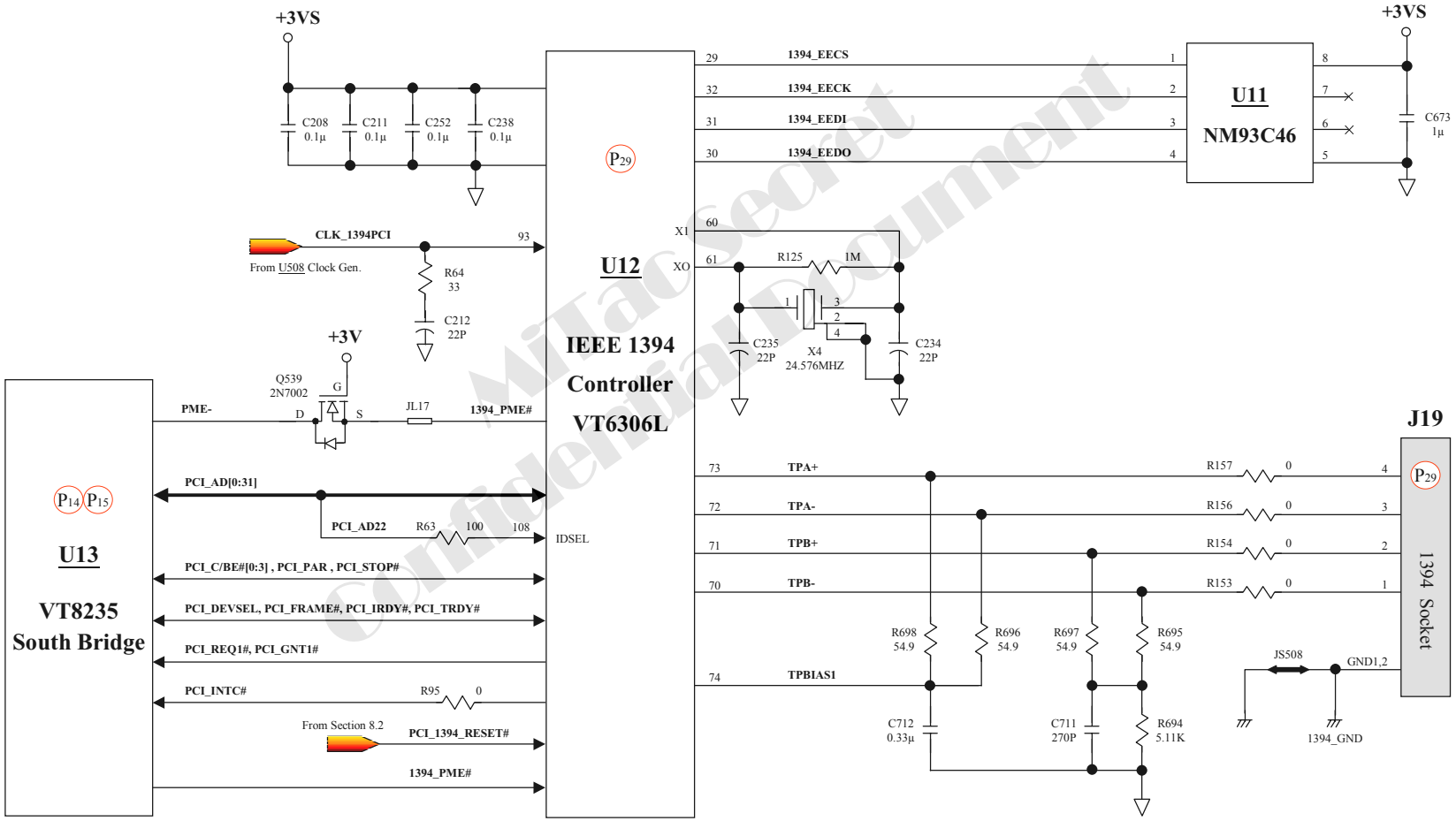
8.14 IEEE 1394 Failure

An error occurs when a IEEE 1394 device is installed.



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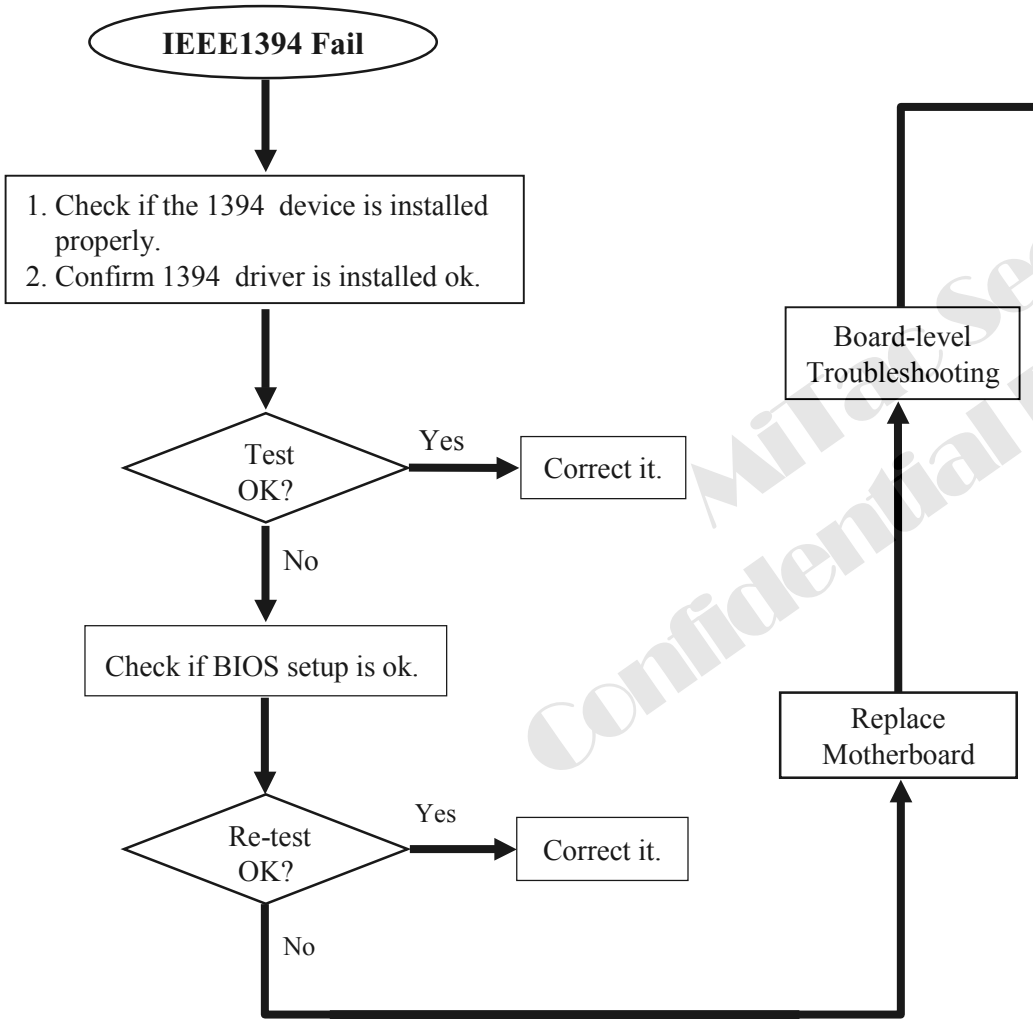
8.14 IEEE 1394 Failure

An error occurs when a IEEE 1394 device is installed.



Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:	**Signals**	
U13	PCI_AD[0:31]	1394_PME#
U12	PCI_C/BE# [0:3]	CLK_1394PCI
U11	PCI_REQ1#	1394_EECS
U508	PCI_FRAME#	1394_EECK
J19	PCI_IRDY#	1394_EEDI
X4	PCI_TRDY#	1394_EEDO
Q539	PCI_DEVSEL#	TPA+
R695	PCI_STOP#	TPA-
R696	PCI_INTC#	TPB+
R697	PCI_1394_RESET#	TPB-
R698	PCI_GNT1#	TPBIAS1
R153	PCI_PAR	+3VS
R154		
R156		
R157		

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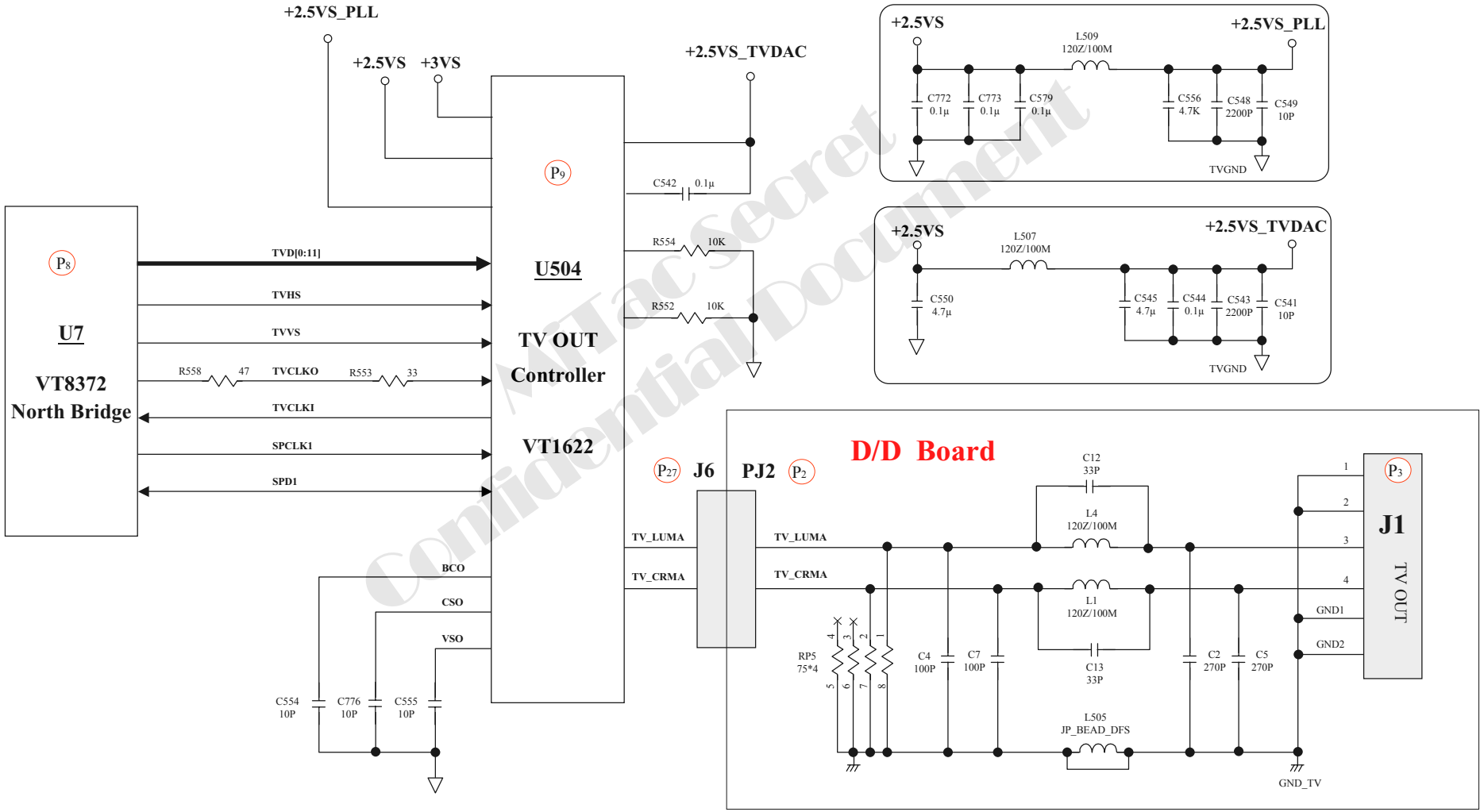
8.15 TV Test Error

An error occurs when a TV device is connected.



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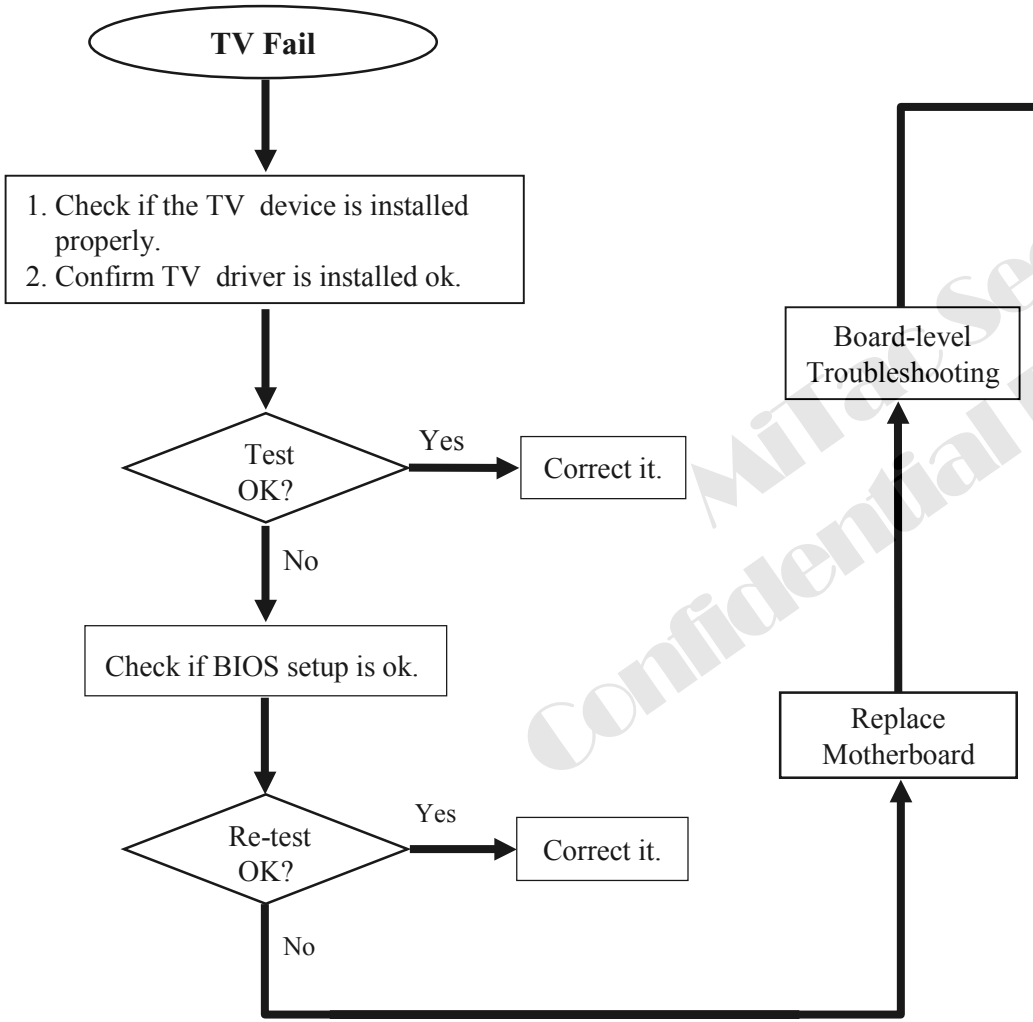
8.15 TV Test Error

An error occurs when a TV device is Connected.



Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:	**Signals**	
U7	TVD[0:11]	+2.5VS_PLL
U504	TVHS	+2.5VS_TVDAC
J6	TVVS	+2.5VS
R553	TVCLKO	+3VS
R558	TVCLKI	
L507	SPCLK1	
L509	SPD1	
D/D:	BCO	
PJ2	CSO	
J1	VSO	
L1	TV_LUMA	
L4	TV_CRMA	
L505		
RP5		

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9. Spare Part List (1)

Part Number	Description	Location(s)
441999900205	AC ADPT ASSY OPTION;8575	
442671200004	AC ADPT ASSY;19V/4.74A,DELTA,817	
361400003030	ADHESIVE;ABS+PC PACK,G485,CEMIDA	
361400003005	ADHESIVE;HEAT,TRANSFER,HTA-48(W)	
541667380011	AK;10-UK,BOX,8375	
541667380032	AK;31-LEMEL,MBAG,8375	
346600000531	AL-FOIL/ADHESIVE;T=0.1,W=220,PRC	
346673800005	AL-FOIL;AUDIO,JACK,8375	
346671700016	AL-FOIL;HDD,M/B,8575	
441999900062	BATT ASSY OPTION;LI,9-CELL,8575	
442671700002	BATT ASSY;11.1V/6AH,LI,MSL,8575	
441503900001	BATT ASSY;Li,9CELLS/6AH,8575	
541350390001	BATT KIT;8575/11.1V,6AH,Li	
338536010006	BATTERY;LI,3.6V/2.0AH,18650,PANA	
346673800004	BE-CU;SHIELDING,AUDIO,8375	
340673800004	BEZEL ASSY;DVD-COMBO,QSI,ID5,837	
344671600020	BEZEL;BATTERY,8175	
242670800113	BFM-WORLD MARK;WINXP,7521N	
221671640001	BOX;AK,8175	
340671600010	BRACKET ASSY;T/P,8175	
340671600028	BRACKET ASSY;T/P,INSULATOR,8175	
342671600003	BRACKET;HDD,8175	
342671600007	BRACKET;LCD,14",8175	
342671600005	BRACKET;LCD,R,14",8175	
421673800003	CABLE ASSY;MDC,8375	

Part Number	Description	Location(s)
421015560001	CABLE ASSY;PHONE LINE,6P2C,W/Z C	
272072153401	CAP;.015U ,CR,16V,10%,0603,X7R,S	C190,C191,C204,C205
272075103403	CAP;.01U ,50V,10%,0603,X7R,SMT	C3,C16
272075103702	CAP;.01U ,50V,+80-20%,0603,Y5V,S	C68,C728,C744,PC23,PC24,P
272075103401	CAP;.01U ,CR,50V ,10%,0603,X7R,S	PC550,PC560
272075103401	CAP;.01U ,CR,50V ,10%,0603,X7R,S	PC10,PC16,PC20,PC27,PC54
272005103401	CAP;.01U ,CR,50V,10%,0805,X7R	PC34,PC4
272005103401	CAP;.01U ,CR,50V,10%,0805,X7R	PC519
272072473401	CAP;.047U,16V ,10%,0603,X7R,SMT	C7
272072104702	CAP;.1U ,16V,+80-20%,0603,Y5V,S	C149,C150,C153,C167,C168,
272073104703	CAP;.1U ,25V,+80-20%,0603,X7R,S	C1,C4,C8
272075104701	CAP;.1U ,50V,+80-20%,0603,Y5V,S	C100,C102,C103,C106,C109,
272075104701	CAP;.1U ,50V,+80-20%,0603,Y5V,S	C504,C506,C512,C513,C517,
272075104703	CAP;.1U ,50V,+80-20%,0603,Y5V,S	
272075104703	CAP;.1U ,50V,+80-20%,0603,Y5V,S	
272072104402	CAP;.1U ,CR,16V,10%,0603,X7R,SM	PC529,PC569
272003104701	CAP;.1U ,CR,25V ,+80-20%,0805,Y	C757,C760,PC39,PC43,PC44
272072224701	CAP;.22U ,16V ,+80-20%,0603,Y5V,	C11,C13,C21,C22,C23,C24,C
272072334701	CAP;.33U ,CR,16V ,+80-20%,0603,Y	C712
272072334701	CAP;.33U ,CR,16V ,+80-20%,0603,Y	C9
272072474701	CAP;.47U ,16V,+80-20%,0603,Y5V,S	
272072474701	CAP;.47U ,16V,+80-20%,0603,Y5V,S	
272002474401	CAP;.47U ,CR,16V ,10%,0805,X7R,S	
272075103707	CAP;0.033U,50V,10%,0603,X7R,SMT	PC524
272075102701	CAP;1000P,50V ,+/-20%,0603,X7R,S	C1,C128,C163,C164,C165,C1

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9. Spare Part List (2)

Part Number	Description	Location(s)
627207510241	CAP;1000P,50V ,10%,0603,X7R,SMT	
272030102405	CAP;1000P,CR,3KV,10%,1808,X7R,TU	C3,C4,C727
272075102403	CAP;1000P,CR,50V,10%,0603,X7R,SM	C666,PC20,PC25,PC26,PC37
272075102403	CAP;1000P,CR,50V,10%,0603,X7R,SM	C1,C11,C534,C9,PC13,PC23,
272075101701	CAP;100P ,50V ,+ -10%,0603,NPO,S	C753,C754
272075101701	CAP;100P ,50V ,+ -10%,0603,NPO,S	PC22
272075101401	CAP;100P ,50V ,10%,0603,COG,SMT	C265
272075101401	CAP;100P ,50V ,10%,0603,COG,SMT	C4,C7
272075100701	CAP;10P ,50V ,+-10%,0603,NPO,SM	C137,C151,C155,C159,C217,
272075100302	CAP;10P ,CR,50V ,5%,0603,NPO,SM	C105,C112,C114,C115,C116,
272021106501	CAP;10U ,10V ,20%,1210,X7R,SMT	C127,C148,C207
272021106501	CAP;10U ,10V ,20%,1210,X7R,SMT	PC21,PC31,PC535
272011106703	CAP;10U ,10V,+80-20%,1206,Y5V,1	C107,C108,C111,C213,C214,
272012106701	CAP;10U ,16V ,+80-20%,1206,Y5U,	C501,C516,C524,C531,C533
272023106501	CAP;10U ,25V ,20%,1210,Y5U,SMT	PC539,PC557,PC576
272011106404	CAP;10U,6.3V,10%,1206,X7R,SMT	C27,C28,C5
272011106406	CAP;10U,CR,6.3V,+-10%,1206,X7R,S	
272073151301	CAP;150P ,CR,25V,5% ,0603,NPO,SM	PC9
272431157507	CAP;150U ,TPC,6.3V,20%,H1.9,7343	C57,C670,PC527,PC537,PC5
272431157507	CAP;150U ,TPC,6.3V,20%,H1.9,7343	PC11,PC12,PC29,PC30
272075150701	CAP;15P ,50V ,+ -10%,0603,NPO,S	C51,C53,C54,C56
272075150301	CAP;15P ,CR,50V ,5% ,0603,NPO,S	C263,C264
272071105701	CAP;1U ,CR,10V ,80-20%,0603,Y5	C154,C157,C160,C223,C261,
272071105701	CAP;1U ,CR,10V ,80-20%,0603,Y5	C10,C3,C509,C8
272001105402	CAP;1U ,CR,10V,10%,0805,X5R,SM	PC5

Part Number	Description	Location(s)
272002105402	CAP;1U ,CR,16V,+80-20%,0805,Y5	C12,C19,C20,C30,C36
272002105403	CAP;1U ,CR,16V,10%,0805,X7R,SM	C6
272003105701	CAP;1U ,CR,25V ,+80%-20%,0805,	PC574,PC578
272003105701	CAP;1U ,CR,25V ,+80%-20%,0805,	PC550
272001225401	CAP;2.2U ,CR,10V ,10%,0805,X7R,S	C5
272002225701	CAP;2.2U ,CR,16V ,+80-20%,0805,Y	C538,C750,C756,C761,PC47
272012225702	CAP;2.2U ,CR,16V ,+80-20%,1206,Y	C522
272075222701	CAP;2200P,50V ,+/-20%,0603,X7R,S	C110,C136,C152,C156,C158,
272075221302	CAP;220P ,50V ,5% ,0603,NPO,SMT	PC18,PC28
272075221401	CAP;220P ,CR,50V ,10%,0603,X7R,S	C749,EC503,EC504,EC55
272075220701	CAP;22P ,50V ,+ -10%,0603,NPO,S	C212,C234,C235,C245,C246,
272075220701	CAP;22P ,50V ,+ -10%,0603,NPO,S	C11
272021226701	CAP;22U ,10V,+80-20%,1210,Y5V,S	C620,PC1,PC3
272043226501	CAP;22U ,25V ,+-20%,1812,Y5U,SMT	PC12,PC13,PC15,PC16,PC22
272075271401	CAP;270P ,50V,+-10%,0603,X7R,SMT	C299,C301,C551,C623,C711
272075271401	CAP;270P ,50V,+-10%,0603,X7R,SMT	C2,C5
272075270302	CAP;27P ,50V ,5%,0603,COG,SMT	C553,C770,C778,C779
272075209001	CAP;2P ,CR,50V ,+-0.25PF,0603,	C13
272431337506	CAP;330U,4V,20%,7343,SMT	PC33
272073330701	CAP;33P ,25V ,+/-10%,0603,NPO,S	C12,C13
272075390301	CAP;39P ,50V ,5% ,0603,NPO,SMT	C10,C14,C15,C16,C17,C18,C
272001475701	CAP;4.7U ,CR,10V ,+80-20%,0805,Y	C147,C278,C545,C550,C556,
272012475701	CAP;4.7U ,CR,16V ,+80-20%,1206,Y	C612,C725
272012475502	CAP;4.7U ,CR,16V,20%,1206,Y5U,SM	C14
272013475701	CAP;4.7U ,CR,25V ,+80-20%,1206,Y	

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9. Spare Part List (3)

Part Number	Description	Location(s)
272075471401	CAP;470P ,50V,10%,0603,X7R,SMT	PC519,PC532,PC533,PC534,
272075471401	CAP;470P ,50V,10%,0603,X7R,SMT	PC19
272072471301	CAP;470P ,CR,16V ,5% ,0603,NPO,P	C12
272075470701	CAP;47P ,50V ,+ -10%,0603,NPO,S	C221,C274,C764
272075470401	CAP;47P ,50V ,10%,0603,COG,SMT	C662,C672
272075470302	CAP;47P ,CR,50V ,5%,0603,NPO,SM	C240
272431476502	CAP;47U ,6.3V,20%,SP-CON,7343,S	C2
272075681401	CAP;680P ,50V ,10%,0603,X7R,SMT	C529,C530
272030680402	CAP;68P ,3KV,10%,1808,NPO,SMT,P	C15
272431826501	CAP;82U ,2.5V,20%,SP-CON,7343,S	PC504,PC506,PC7,PC8
221669950008	CARD BOARD;FRAME,PALLET,7170	
221669950006	CARD BOARD;TOP,PALLET,7170	
221671620001	CARTION;BATTERY,20IN1	
221600020128	CARTON;380MM*320MM*320MM,BC FLUT	
221671220002	CARTON;NON-BRAND,MSL,8170	
431673850002	CASE KIT;ID5,8375	
451671600031	CD ROM ME KIT;8175	
335152000044	CFM-BAT;FUSE THERMAL 98'C	
313000020360	CHOKE COIL;1.25uH,+30-0%,4.5Ts,D	PL1,PL2
273000111002	CHOKE COIL;120OHM/100MHZ,20%,321	L12,L13,L505,L521,L524
273000111004	CHOKE COIL;160OHM/100MHZ,25%,321	
273000150313	CHOKE COIL;90OHM/100MHZ,20%,2012	L508,L509,L518,L522
331000008038	CON;BAT,8P,2.5MM,SUYIN	J13
291000001001	CON;BATTERY,10P,FM,2MM,R/A,SMT	
331000007015	CON;BATTERY,FM,7P,R/A,8175,PRC	

Part Number	Description	Location(s)
331720015006	CON;D,FM,15P,2.29,R/A,3ROW	J1
331720025005	CON;D,FM,25P,2.775,R/A	J3
291000143001	CON;FPC/FFC,15P*2,.8MM,BD/BD,QTC	J12
291000142404	CON;FPC/FFC,24P,1MM,H8.2,ST,ACES	J11
291000150804	CON;FPC/FFC,8P,1MM,R/A,2CONTAC,E	J501
291000144004	CON;HDR,20P*2,1.0MM,H=4.6,ST,SMT	J3
331040020004	CON;HDR,FM,10P*2,2.54MM,R/A,H8,4	J5
331030044013	CON;HDR,FM,22*2,2MM,ST,C16805	
331040050013	CON;HDR,FM,25P*2,1.27X1.27MM,D/R	J6
331040020005	CON;HDR,MA,10P*2,2.54MM,R/A,H8.4	PJ1
291000021101	CON;HDR,MA,11P*1,1.25,R/A,DF13-1	J1
291000011209	CON;HDR,MA,12P*1,1.25,ST,SMT	J6
291000024409	CON;HDR,MA,22P*2,2MM,R/A,SMT,ALL	J14
331040050012	CON;HDR,MA,25P*2,1.27X1.27MM,D/R	PJ2
291000020202	CON;HDR,MA,2P*1,1.25,R/A,SMT,HIR	J507
291000020204	CON;HDR,MA,2P*1,3.5MM,R/A,SMT,SM	J2
291000020408	CON;HDR,MA,4P,1.25MM,H3.5MM,R/A,	J4
331040050010	CON;HDR,MA,50P,0.8MM,R/A,H1.1	J10
291000020303	CON;HDR,SHROUD,MA,3P,1.25MM,R/A,	J503
291000256823	CON;IC CARD PART;68P,0.635,H5,SM	J9
331000004009	CON;IEEE1394,MA,4P*1,0.8MM,R/A	J19
331870004017	CON;MINI DIN,4P,R/A,W/GROND,C108	J1
331810006014	CON;MODULAR JACK,FM,6P4C,R/A,UK	
291000810404	CON;PHONE JACK,4P,H=8.5,R/A,SMT,	J2
291000810808	CON;PHONE JACK,8P,H=12.59,R/A,RJ	J8

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9. Spare Part List (4)

Part Number	Description	Location(s)
331840010005	CON;POF MINI JACK,10P,W/SPDIF,2F	J21
331910002006	CON;POWER JACK,2P,20VDC,5A,DIP	J2
331840005041	CON;STEREO JACK,5P,R/A,MITAC	J20
331000004029	CON;USB,MA,R/A,4P*1,2551A-04G5T-	J4,J5,J7,J8
291000410201	CON;WFR,MA,2P,1.25,ST,SMT/MB	J16,J17,J18
291000410301	CON;WFR,MA,3P,1.25,ST,SMT/MB	J7
291000410401	CON;WFR,MA,4P,1.25MM,ST,SMT	J502
291000410801	CON;WFR,MA,8P*1,1.25MM,ST,SMT	J15
346600000040	CONDUCTIVE TAPE;10MM,UCTP,PRC	
346600000059	CONDUCTIVE TAPE;15MM,UCTP,PRC	
346600000060	CONDUCTIVE TAPE;25MM,UCTP,PRC	
346600000039	CONDUCTIVE TAPE;5MM,UCTP/8269H,P	
346673800009	CONDUCTIVE TAPE;CONNECTOR,LCD,83	
225600000290	CONDUCTIVE TAPE;U-TEK/UCTP,W=10M	
225600000292	CONDUCTIVE TAPE;U-TEK/UCTP,W=20M	
342503400302	CONTACT PLATE;W5L135T0.13,8170LI	
342503400005	CONTACT PLATE;W5L24T0.13,7170LI,	
342503400004	CONTACT PLATE;W5L45T0.13,7170LI,	
342503400006	CONTACT PLATE;W5L45T0.13,7170LI,	
342503400303	CONTACT PLATE;W5L75T0.13,8170LI,	
342503400301	CONTACT PLATE;W5L92T0.15,8170LI,	
342503400002	CONTACT PLATE;W5L9T0.13,7170LI,P	
342503400003	CONTACT PLATE;W7L7T0.13,7170LI,P	
313000150093	CORE;LAN CORE,230OHM/100MHZ,LF-1	
340673840004	COVER ASSY;DIMM,ID4,8375	

Part Number	Description	Location(s)
340671600029	COVER ASSY;HDD,8175	
340671740006	COVER ASSY;ID5,8575	
340673850001	COVER ASSY;KB,ID5,8375	
340671740004	COVER ASSY;LCD,14",ID5,8575	
344671600018	COVER;BATTERY,8175	
344671740107	COVER;DUMMY,ID5,8575	
344671600016	COVER;HDD,8175	
344671740106	COVER;HINGE,ID5,8575	
272625220401	CP;22P*4 ,8P,50V ,10%,1206,NPO,S	CP501,CP502
346600000142	DIALAMY;T=0.1,W=113,WHITE,PRC	
331660020004	DIMM SOCKET;DDR SODIMM 200P, CA0	J505
331660020005	DIMM SOCKET;DDR SODIMM 200P, CA0	J506
288100032013	DIODE;BAS32L,VRRM75V,MELF,SOD-80	PD2,PD3,PD515,PD516
288100701002	DIODE;BAV70LT1,70V,225MW,SOT-23	D507,D514
288100099001	DIODE;BAV99,70V,450MA,SOT-23	D1,D3,D4,D6
288100099001	DIODE;BAV99,70V,450MA,SOT-23	D1
288100056003	DIODE;BAW56,70V,215mA,SOT-23	PD503,PD505,PD506
288100056003	DIODE;BAW56,70V,215mA,SOT-23	D3,D504
288100084002	DIODE;BZX84C5V6,5.2~6V,350mA,SOT	
288101004024	DIODE;EC10QS04,RECT,40V,1A,CHIP,	PD504,PD507
288101004024	DIODE;EC10QS04,RECT,40V,1A,CHIP,	PD1,PD4
288100112003	DIODE;EC11FS2-TE12L,SCHOTTKY,200	PD503,PD504,PD511
288103104001	DIODE;EC31QS04-TE12L,40V,3A,SMT	PD1,PD3,PD501,PD502
288103104001	DIODE;EC31QS04-TE12L,40V,3A,SMT	PD505,PD506,PD514
288104148001	DIODE;RLS4148,200MA,500MW,MELF,S	D10,D11,D501,D502,D506,D

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9. Spare Part List (5)

Part Number	Description	Location(s)
288100024002	DIODE;RLZ24D,ZENER,23.63V,5%,SMT	PD501
288100056005	DIODE;UDZ5.6B,ZENER,5.6V,UMD2,SM	D505
288100018003	DIODE;UDZS18B,ZENER,18V,SOD-323,	
288100036002	DIODE;UDZS3.6B,ZENER,3.6 V,UMD2,	D504
344671600043	DUMMY CARD;PCMCIA,8175	
523499991026	DVD COMBO ASSY OPTION;16X10X8X24	
523430061906	DVD COMBO DRIVE;16X8X8X24,SBW-16	
523467384001	DVD-COMBO ASSY;SBW-161,ID4/5,837	
272601107501	EC;100U ,6.3V,20%,D6.3,-40+85'C,	C303,C304
272602107501	EC;100U,16V,M,6.3*5.5,-55+85'C,S	C275
312271006358	EC;100U,25V,RA,M,D6.3*7,SGX,SANY	PC27,PC28
312271006358	EC;100U,25V,RA,M,D6.3*7,SGX,SANY	PC25
312271005357	EC;10U,25V,20%,RA,6.3*6.8,+105℃	PC10,PC18,PC21
312271005357	EC;10U,25V,20%,RA,6.3*6.8,+105℃	PC2,PC3
312273361501	EC;330U ,6.3V ,RA,M,6.3*7,+105C	PC1,PC6
312008206151	EC;820U,4V,+-20%,10X10.5,M-VIP,F	PC11,PC14,PC6,PC9
227671600001	END CAP;14.1",8175	
227671600008	END CAP;BATTERY,AK BOX,8175	
227671600009	END CAP;FDD,AK BOX,8175	
481673800002	F/W ASSY;KBD CTRL,8375	U509
481673800001	F/W ASSY;SYS/VGA BIOS,8375	U15
340671200020	FAN ASSY;8170	
273000150002	FERRIET CHIP;120OHM/100MHZ,2012,	L11,L14,L15,L16,L17,L18,L1
273000610019	FERRITE ARRAY;130OHM/100MHZ,3216	FA501
273000610019	FERRITE ARRAY;130OHM/100MHZ,3216	FA501

Part Number	Description	Location(s)
273000130009	FERRITE CHIP;120OHM/100MHZ,1608,	L507,L509
273000130019	FERRITE CHIP;120OHM/100MHZ,1608,	L30,L31,L531
273000150013	FERRITE CHIP;120OHM/100MHZ,2012,	L502,L510,PL11,PL4,PL501,
273000150013	FERRITE CHIP;120OHM/100MHZ,2012,	L504,L512,L514,L516,L520,L
273000130039	FERRITE CHIP;130OHM/100MHZ,1608,	L22,L33,L501,L503,L504,L52
273000130039	FERRITE CHIP;130OHM/100MHZ,1608,	L1,L4,L513,L515
273000150001	FERRITE CHIP;220OHM/100MHZ,2012,	
273000150036	FERRITE CHIP;32OHM/100MHZ,2012,S	L36,L41,L513,L514,L515,L53
273000130006	FERRITE CHIP;600OHM/100MHZ,.2A,1	L37,L38,L42,L43,L44,L46,L5
273000130038	FERRITE CHIP;600OHM/100MHZ,1608,	L516,L518
422665400002	FFC ASSY;TOUCH PAD,CASE KIT,VENU	
341671200010	FINGER;EMI GROUND SMD FINGER,H=4	E501,E502
342672400007	FINGER;EMI GROUNDING SMD FINGER	E10,E11,E508,E509,E510,TP
288003600001	FIR;HSDL3600#007,FRONT VIEW,10P,	U2
245600010030	FLOW CARD;SPS,PINK,100MM*30MM,PR	
295000010028	FUSE;0.14A/60V,POLY SWITCH,PTC,S	F501
295000010105	FUSE;1A,NORMAL,1206,SMT	F1,F502,PF501
295000010057	FUSE;228R,139C',5A/250V,SMT,PRC	
295000010116	FUSE;FAST, 10A, 86VDC, 6125,SMT	PF1
295000010116	FUSE;FAST, 10A, 86VDC, 6125,SMT	PF501
295000010126	FUSE;FAST,2A,63VDC,1206,SMT,PRC	F1
335152000062	FUSE;LR4-730,POLY SWITCH,PRC	
345673500018	GASKET;6x6x10,WEASEL	
345671700009	GASKET;BRACKET T/P,8575	
345673800006	GASKET;ESD-2,SHIELDING,8375	

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9. Spare Part List (6)

Part Number	Description	Location(s)
345671600018	GASKET;HEATSINK,K/B_PLATE,8175	
345671700010	GASKET;KB PLATE,8575	
345671700011	GASKET;KB PLATE-1,8575	
345671700019	GASKET;MIC,8575	
345671700004	GASKET;USB,8575	
230000010004	GLUE;9001B,BLACK,PRC	
230000010003	GULE;9001A,BLACK,PRC	
451671600051	HDD ME KIT;8175	
340673800001	HEATSINK ASSY;8375	
340671700006	HEATSINK ASSY;N/B,8575	
340671600020	HINGE;L,14",8175	
340671600018	HINGE;R,14",8175	
340671600039	HOUSING ASSY;CDROM,8175	
340673840002	HOUSING ASSY;ID4,8375	
340673830004	HOUSING ASSY;LCD,ID5,8375	
451673850001	HOUSING KIT;ID5,8375	
344671600019	HOUSING;BATTERY,8175	
344600000425	HOUSING;HIROSE/DF13-4S-1.25C,PRC	
344600000842	HOUSING;HRS/DF13-11S-1.25C,PRC	
344600000843	HOUSING;HRS/DF13-12S-1.25C,PRC	
344600000889	HOUSING;HRS/DF13-8S-1.25C,PRC	
344600000577	HOUSING;JAE/F1-S20S,PRC	
344600000863	HOUSING;JST//SHDR-40V-S-B,PRC	
344600000824	IC CARD CON PART;68P,IC11SA-BD-P	
291000614621	IC SOCKET;462P,ZIF,FOXCONN,PZ462	U1

Part Number	Description	Location(s)
282574014004	IC;74AHC14,HEX INVERTER,TSSOP,14	U18,U510
282574186002	IC;74AHCT1G86,SINGLE,XOR,SOT23,S	U512
282074338405	IC;74CBT3384,10 BIT BUS SW,TSOP-	U502
286308800001	IC;AME8800,0.3A,1.5%,LDO,SOT89	U503
286308800003	IC;AME8800,0.3A,3.3V,REG,SOT89	U514
286302020001	IC;APA2020ARI,AUDIO AMP,2W,TSSOP	U16
286305301002	IC;APL5301-25AC-TR,LDO REGULATOR	PU14
286002040001	IC;BQ2040,GAS GAUGE,SO,16P,SMT	
284501410009	IC;CB1410,PCI/CARDBUS,LFBGA,144L	U505
284508500002	IC;CM8500,3A BUS TERMINATOR,PTSS	PU13
283466570001	IC;EEPROM,9346,64*16 BITS,SO8,SM	U11,U17
283400000003	IC;EEPROM,NM24C02N,2K,SO,8P	
283460000002	IC;FLASH,256K*8-70,PLCC32,EN29F0	
286300680001	IC;G680,RESET CIRCUIT,ADJ,SOT23-	
286317812001	IC;HA178L12UA,VOLT REGULATOR,SC-	PU507
284595090202	IC;ICS950902,CLOCK GEN,SSOP56,56	U508
286300811001	IC;IM811,MICROPWR VOL,SOT23-4	U511
284500086001	IC;LM86,TEMPERATURE MTR,SO8	U4
286100393004	IC;LMV393,DUAL COMPARTOR,SSOP,8P	PU508
286302951015	IC;LP2951ACM,VOLTAGE REGULATOR,S	U507
286329510001	IC;LP2951CM-3.3,VOLTAGE REGULATO	U506
286317097001	IC;LTC1709EG-7,PWM CTRL,SSOP ,36	PU505
286303707001	IC;LTC3707,PWM SWITCH REG,SOOP,2	PU506
286303707001	IC;LTC3707,PWM SWITCH REG,SOOP,2	PU4
286104173001	IC;MAX4173F,I-SENSE AMP,SOT23,6P	PU1

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9. Spare Part List (7)

Part Number	Description	Location(s)
286301414001	IC;MM1414,PROTECTION,TSOP-20A,PR	
281307085001	IC;NC7SZ08P5,2-INPUT & GATE,SC70	U10
286300965001	IC;OZ965R,CCFL CTRL,TSSOP16,O2	U1
286309701001	IC;RT9701,POWER DISTRI SW,SOT23-	U1,U3
286381250001	IC;S-81250,DECECTOR,SOT-89,PRC	
286300431014	IC;SC431LCSK-.5,.5%,ADJ REG,SOT2	PQ508
282007404003	IC;SN74LVC04ADR,HEX INVERTERS,SO	U9
282007408002	IC;SN74LVC08ADR,2 I/P,AND GATE,S	U8
286300594001	IC;TL594C,PWM CONTROL,SO,16P	PU507
286302211004	IC;TPS2211A,POWER INTERFACE SW,S	U6
284501211004	IC;VT1211,LPC2SUPERIO,PQFP,128,S	U14
284501612002	IC;VT1612A,AC97 CODEC,TQFP,48P,S	U19
284501622001	IC;VT1622,TV ENCODER,PQFP,64P,SM	U504
284506103002	IC;VT6103,LAN-PHY,SSOP,48P,SMT	U513
284506307001	IC;VT6307L,PCI-1394,2PORT,LQFP,1	U12
284508235002	IC;VT8235,SOUTH BRIDGE,BGA,487P,	U13
284508372001	IC;VT8372,NORTH BRIDGE,HSBGA,552	U7
284583950001	IC;W83L950D,LPC_KBC,LQFP,80P,SMT	
273000120128	INDUCTOR;10nH,10%,0805,SMT	L1,L10,L2,L3,L4,L7,L8,L9
273000990012	INDUCTOR;10UH,CDRH127,SUMIDA,SMT	PL3,PL5
273000990012	INDUCTOR;10UH,CDRH127,SUMIDA,SMT	PL2
273000990031	INDUCTOR;10UH,CDRH127B,SUMIDA,SM	PL3
273000990115	INDUCTOR;3.3uH,3A,CSS054D,SMT	PL10
273000990021	INDUCTOR;33uH,CDRH124,SUMIDA,SMT	PL7
346671200036	INSULATOR,MDC,8170	

Part Number	Description	Location(s)
346600000464	INSULATOR/2ADHESIVE;FIBER/W204,T	
346600000517	INSULATOR/2ADHESIVE;FIBER/W204,T	
346600000481	INSULATOR/2ADHESIVE;FIBER/W204,T	
346600000414	INSULATOR/ADHESIVE;FIBER/W204,T=	
346600000463	INSULATOR/ADHESIVE;FIBER/W204,T=	
346600000515	INSULATOR/ADHESIVE;FIBER/W204,T=	
346503100005	INSULATOR;5,BATTERY ASSY,7521Li	
346671700001	INSULATOR;AL-FOIL,M/B BOTTOM,857	
346503400504	INSULATOR;BATT ASSY,L125,8175	
346503400502	INSULATOR;BATT ASSY,L22R9.2,8175	
346503200006	INSULATOR;BATT ASSY,ONE ROUND,GR	
346503400503	INSULATOR;BATT ASSY,W7L13,8175	
346671700006	INSULATOR;CD-ROM,M-B,8575	
346503400301	INSULATOR;FOR 3 CELLS,DOUBLE-FA,	
346503400501	INSULATOR;FOR 4 CELL,DOUBLE-FACE	
346503200002	INSULATOR;FOR 4 CELLS,GRAMPUS	
346669900004	INSULATOR;INVERTER,7170	
346673800001	INSULATOR;MINIPCI,8375	
346503400203	INSULATOR;ONE ROUND,STINGRAY	
346503900001	INSULATOR;PCB ASSY,W15L52,8575	
346671600015	INSULATOR;PCMCIA,8175	
346671700021	INSULATOR;REAR,SCREW,8575	
346671600009	INSULATOR;T/P,BRACKET,8175	
346600000403	INSULATOR;TWO DIALAMY,T=0.1,W=60	
346503400303	INSULATOR;W13MML52MM,8170Li,PRC	

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9. Spare Part List (8)

Part Number	Description	Location(s)
541150340202	INVERTER BD;STINGRAY (FOR 8640)	
531099990129	KBD OPTION;87,UK,8175	
531020237348	KBD;87,UK,K000918J1,8175	
451673840052	LABEL KIT;N-B,ID4/5,8375	
242600000145	LABEL;10*10,BLANK,COMMON	
242600000145	LABEL;10*10,BLANK,COMMON	
242600000457	LABEL;20*7MM,COMMON,PRC	
242662300009	LABEL;25*10MM,3020F	
242662300009	LABEL;25*10MM,3020F	
242662300009	LABEL;25*10MM,3020F	
242600000434	LABEL;25*6MM,COMMON	
242600000378	LABEL;27*7MM,HI-TEMP 260'C	
242668300017	LABEL;4*3MM,HI-TE	
624200010140	LABEL;5*20,BLANK,COMMON	
624200010140	LABEL;5*20,BLANK,COMMON	
242673840001	LABEL;AGENCY-GLOBAL,ID4/5,8375	
242600000157	LABEL;BAR CODE & S/N,13.5*75,COM	
242671700002	LABEL;BATT 11.1V/6AH,LI,PANASONI	
242669900009	LABEL;BLANK,60*80MM,7170	
242664800013	LABEL;CAUTION,INVERT BD,PITCHING	
242600000315	LABEL;RED ARROW HEAD,PRC	
242600000315	LABEL;RED ARROW HEAD,PRC	
242600000195	LABEL;SOFTWARE,INSYDE BIOS-M	
441673850003	LCD ASSY;QDI,XGA,14.1",ID5,8375	
451673850031	LCD ME KIT;14.1",ID5,8375	

Part Number	Description	Location(s)
413000020322	LCD;QD141X1LH03,TFT,14",LCDS,XGA	
294011200069	LED;GREEN,19-21VGC/TR8,LED_CL190	LED1,2,3,4
294011200001	LED;GRN,H1.5,0805,PG1102W,SMT	D13,D14,D15,D16,D17,D18
294011200070	LED;RED/GREEN,19-22SRVGC/TR8,LED	LED5,6
416267385901	LT PF OPTION;XGA,14.1",ID5,8375	
416267385002	LT PF;QDI,XGA,14.1",ID5,8375	
526267385011	LTXNX;8375/T4XX/XXL/4UK1/L3D3C/X	
561567380001	MANUAL KIT;EN,8375,N-B	
561567380013	MANUAL;USER'S,EN,8375,N-B	
421671600051	MICROPHONE ASSY;8175	
291000001203	MINIPCI SOCKET;124P,0.8MM,H=6,SM	J504
346600000446	MYLAR/3M-467;T=0.1,W=46,BLACK,PR	
346600000465	MYLAR/ADHESVIE;MYLAR/W204,T=0.1,	
346600000074	MYLAR;T=0.1,W=110,BLACK,PRC	
346600000226	MYLAR;T=0.1,W=113,BLACK,PRC	
346600000574	MYLAR;T=0.1,W=220,BLACK,PRC	
346600000321	MYLAR;T=0.2,W=72.4,BLACK,PRC	
375102030010	NUT-HEX;M2,2,NIW	
375120262008	NUT-HEX;M2.6,NCG	
461503900001	PACKING KIT;8575,BATT,Li	
461671600002	PACKING KIT;N-B,14.1",8175	
227671600003	PAD;LCD/KB,ANIT-STATIC,8175	
224670830002	PALLET;1250*1080*130,7521N	
221671650014	PARTITION;AK BOX,8175	
221671650009	PARTITION;BATTERY,8575N	

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9. Spare Part List (9)

Part Number	Description	Location(s)
221671650004	PARTITION;FDD,AK BOX,8175	
221600050113	PARTITION;FLAT,320MM*290MM,BC FL	
221671250005	PARTITION;HDD CASE,8170	
221671250003	PARTITION;PALLET,8170	
221671650010	PARTITION;TOP/BTM,8575N	
412155600047	PCB ASSY;MDM,56K,UNIV,F-PACK,WO/	
316503400501	PCB;PWA-8175/BATT GAUGE BD	
316503400502	PCB;PWA-8175/BATT PROTECTION BD	
316673800002	PCB;PWA-8375/DD BD	
316673800001	PCB;PWA-8375/MOTHER BD	R0B
316671700003	PCB;PWA-8575/TOUCHPAD BD	R00
316000000019	PCB;PWA-STINGRAY/INVERTER BD (FO	
222600020049	PE BAG;50*70MM,W/SEAL,COMMON	
222600020310	PE BAG;70X100MM,W/SEAL,COMMON	
222668820001	PE BAG;ANTI-STATIC,170x270MM,ORC	
222667220003	PE BAG;L560XW345,CERES	
222670000001	PE BUBBLE BAG;BATTERY,7521	
222503220001	PE BUBBLE BAG;BATTERY,GRAMPUS	
222671620001	PE BUBBLE BAG;CD-ROM HOUSING,817	
230000000003	PEN;OIL,BLUE,PRC	
343673800003	PLATE;K/B,8375	
411673800005	PWA;PWA-8375,D/D BD,SMT	
411673800004	PWA;PWA-8375,D/D BD,T/U	
411673800001	PWA;PWA-8375,MOTHER BD	
411673800003	PWA;PWA-8375,MOTHER BD,SMT	

Part Number	Description	Location(s)
411673800002	PWA;PWA-8375,MOTHER BD,T/U	
411671700009	PWA;PWA-8575,T/P BD	
411503900003	PWA;PWA-8575/BATT GAUGE BD,LI	
411503900001	PWA;PWA-8575/BATT PROTECTION BD,	
411503900002	PWA;PWA-8575/BATT PROTECTION BD,	
411503400205	PWA;PWA-STINGRAY/INVERTER BD,MSL	
411503400206	PWA;PWA-STINGRAY/INVERTER BD,SMT	
332810000043	PWR CORD;250V/3A,2P,BLACK,UK	
271045047101	RES;.004,1W,1%,2512,SMT	PR1,PR2,PR501,PR502
271045087101	RES;.008 ,1W ,1% ,2512,SMT	PR16
271045107101	RES;.01 ,1W ,1% ,2512,SMT	PR4,PR5
271045107101	RES;.01 ,1W ,1% ,2512,SMT	PR4,PR506
271045207101	RES;.02 ,1W ,1% ,2512,SMT	PR14
271046257101	RES;.025 ,2W ,1% ,2512,SMT,PRC	
271002000301	RES;0 ,1/10W,5% ,0805,SMT	R152,R748
271002000301	RES;0 ,1/10W,5% ,0805,SMT	L2
271071000002	RES;0 ,1/16W,5% ,0603,SMT	L28,PR18,PR512,PR524,R11
271071000002	RES;0 ,1/16W,5% ,0603,SMT	PR17,PR522,PR523,R1,R511
271071102172	RES;1.02K,1/16W,1% ,0603,SMT	R20,R22,R65
271071113113	RES;1.13K,1/16W,1%,0603,SMT	R43,R658
271071152101	RES;1.5K ,1/16W,1% ,0603,SMT	R25,R26
271071152302	RES;1.5K ,1/16W,5% ,0603,SMT	R503,R762
271071100302	RES;10 ,1/16W,5% ,0603,SMT	PR507,PR515,R600,R602,R6
271071100302	RES;10 ,1/16W,5% ,0603,SMT	PR3
271071100302	RES;10 ,1/16W,5% ,0603,SMT	R9

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9. Spare Part List (10)

Part Number	Description	Location(s)
271071102211	RES;10.2K,1/16W,1% ,0603,SMT	R26,R734
271071102211	RES;10.2K,1/16W,1% ,0603,SMT	R5
271071101101	RES;100 ,1/16W,1% ,0603,SMT	R11,R12,R516,R519,R520,R5
271071101301	RES;100 ,1/16W,5% ,0603,SMT	
271071101301	RES;100 ,1/16W,5% ,0603,SMT	
271071104101	RES;100K ,1/16W,1% ,0603,SMT	PR11,PR548
271071104101	RES;100K ,1/16W,1% ,0603,SMT	R16,R17
271071104101	RES;100K ,1/16W,1% ,0603,SMT	
271071104101	RES;100K ,1/16W,1% ,0603,SMT	
271071104302	RES;100K ,1/16W,5% ,0603,SMT	PR505,PR516,PR542,PR546,
271071104302	RES;100K ,1/16W,5% ,0603,SMT	PR518
271071104302	RES;100K ,1/16W,5% ,0603,SMT	
271071104302	RES;100K ,1/16W,5% ,0603,SMT	
271071103101	RES;10K ,1/16W,1% ,0603,SMT	PR509,PR530,PR538,PR540,
271071103101	RES;10K ,1/16W,1% ,0603,SMT	PR12,PR19
271071103101	RES;10K ,1/16W,1% ,0603,SMT	R18
271071103302	RES;10K ,1/16W,5% ,0603,SMT	PR521,R1,R107,R108,R109,F
271071103302	RES;10K ,1/16W,5% ,0603,SMT	R10,R516,R529
271071103302	RES;10K ,1/16W,5% ,0603,SMT	
271071106301	RES;10M ,1/16W,5% ,0603,SMT	R136
271071113101	RES;11K ,1/16W,1% ,0603,SMT	PR526
271071113101	RES;11K ,1/16W,1% ,0603,SMT	PR8
271071121211	RES;12.1K,1/16W,1% ,0603,SMT	R741,R743,R744,R746
271071121301	RES;120 ,1/16W,5% ,0603,SMT	R505,R506,R507,R508
271071123301	RES;12K ,1/16W,5% ,0603,SMT	R170

Part Number	Description	Location(s)
271071137271	RES;13.7K,1/16W,.1%,0603,SMT	PR531
271071134701	RES;130K ,1/16W,0.1% ,0603,SMT	PR551
271071147011	RES;147 ,1/16W,1% ,0603,SMT	R18
271071143701	RES;14K ,1/16W,0.1% ,0603,SMT	PR555
271071154101	RES;150K ,1/16W,1% ,0603,SMT	R1
271071154301	RES;150K ,1/16W,5% ,0603,SMT	R140
271071153101	RES;15K ,1/16W,1% ,0603,SMT	PR520,PR527,R49,R51,R669
271071153101	RES;15K ,1/16W,1% ,0603,SMT	PR13,PR14
271071153101	RES;15K ,1/16W,1% ,0603,SMT	R3,R4
271071153301	RES;15K ,1/16W,5% ,0603,SMT	R502,R503,R504,R505,R508,
271071164301	RES;160K ,1/16W,5% ,0603,SMT	
271071178311	RES;178K ,1/16W,1% ,0603,SMT	PR535
271071102102	RES;1K ,1/16W,1% ,0603,SMT	PR13,R55,R56
271071102102	RES;1K ,1/16W,1% ,0603,SMT	R8,R15,R19
271071102302	RES;1K ,1/16W,5% ,0603,SMT	PR508,PR528,R118,R119,R1
271071102302	RES;1K ,1/16W,5% ,0603,SMT	PR517
271071105101	RES;1M ,1/16W,1% ,0603,SMT	R13
271071105301	RES;1M ,1/16W,5% ,0603,SMT	PR3,PR506,PR543,PR544,PR
271071105301	RES;1M ,1/16W,5% ,0603,SMT	PR509,PR521,PR6,PR7,R9
271071221111	RES;2.21K,1/16W,1% ,0603,SMT	R92
271071222302	RES;2.2K ,1/16W,5% ,0603,SMT	R16,R17,R648
271071225301	RES;2.2M,1/16W,5% ,0603,SMT	
271071249111	RES;2.49K,1/16W,1% ,0603,SMT	PR537
271012278101	RES;2.7 ,1/8W,1% ,1206,SMT	R14
271071272101	RES;2.7K ,1/16W,1% ,0603,SMT	PR513,PR525,R59,R80,R81,F

MiTac Secret
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9. Spare Part List (11)

Part Number	Description	Location(s)
271071272101	RES;2.7K ,1/16W,1% ,0603,SMT	PR9
271071201301	RES;200 ,1/16W,5% ,0603,SMT	
271071204101	RES;200K ,1/16W,1% ,0603,SMT	PR12,PR552
271071203701	RES;20K ,1/16W,.1%,0603,SMT	PR529
271071203101	RES;20K ,1/16W,1% ,0603,SMT	PR16,PR519,R691,R742,R74
271071203101	RES;20K ,1/16W,1% ,0603,SMT	R2
271071221302	RES;22 ,1/16W,5% ,0603,SMT	R589,R605,R608,R625,R627,
271071221211	RES;22.1K,1/16W,1% ,0603,SMT	PR539,PR541
271071224301	RES;220K ,1/16W,5% ,0603,SMT	R148
271071244301	RES;240K ,1/16W,5% ,0603,SMT	
271071273301	RES;27K ,1/16W,5% ,0603,SMT	R689,R692
271071202102	RES;2K ,1/16W,1% ,0603,SMT	R126,R42,R659,R731,R732,R
271071205101	RES;2M ,1/16W,1% ,0603,SMT	R11
271071392301	RES;3.9K ,1/16W,5% ,0603,SMT	R511,R512,R513,R514,R515,
271071301011	RES;301 ,1/16W,1% ,0603,SMT	R523
271071324211	RES;32.4K,1/16W,1% ,0603,SMT	PR5
271071324012	RES;324K ,1/16W,1% ,0603,SMT	PR532
271071330302	RES;33 ,1/16W,5% ,0603,SMT	R121,R122,R48,R50,R52,R55
271071333301	RES;33K ,1/16W,5% ,0603,SMT	PR522,PR557,R727
271071333301	RES;33K ,1/16W,5% ,0603,SMT	R2,R3,R506,R7
271071361101	RES;360 ,1/16W,1% ,0603,SMT	R675,R676
271002383011	RES;383 ,1/10W,1% ,0805,SMT	R678,R79
271072302301	RES;3K ,1/10W,5% ,0603,SMT	R729
271071442112	RES;4.42K,1/16W,1% ,0603,SMT	R534
271071475112	RES;4.75K,1/16W,1% ,0603,SMT	R29,R30,R564,R565,R566

Part Number	Description	Location(s)
271002472301	RES;4.7K ,1/10W,5% ,0805,SMT	PR516
271071472101	RES;4.7K ,1/16W,1% ,0603,SMT	R606
271071472302	RES;4.7K ,1/16W,5% ,0603,SMT	PR554,PR7,PR8,R100,R101,I
271071499111	RES;4.99K,1/16W,1% ,0603,SMT	PR15
271071402811	RES;40.2 ,1/16W,1% ,0603,SMT	R10,R9
271071470301	RES;47 ,1/16W,5% ,0603,SMT	R558
271071471101	RES;470 ,1/16W,1% ,0603,SMT	R21,23,27
271071471302	RES;470 ,1/16W,5% ,0603,SMT	,R681,R720
271071474301	RES;470K ,1/16W,5% ,0603,SMT	R502,R639
271071474301	RES;470K ,1/16W,5% ,0603,SMT	PR507,PR508,PR510
271071475011	RES;475 ,1/16W,1% ,0603,SMT	R620
271071473301	RES;47K ,1/16W,5% ,0603,SMT	PR545,R174,R587,R642,R71
271071473301	RES;47K ,1/16W,5% ,0603,SMT	R4,R5,R518,R8
271071487211	RES;48.7K,1/16W,1% ,0603,SMT	R7
271071499811	RES;49.9 ,1/16W,1% ,0603,SMT	R39,R46,R536,R537
271071499311	RES;499K ,1/16W,1% ,0603,SMT	PR10
271071518301	RES;5.1 ,1/16W,5% ,0603,SMT	PR17
271071511111	RES;5.11K,1/16W,1% ,0603,SMT	R694
271071512101	RES;5.1K ,1/16W,1% ,0603,SMT	R66
271002515302	RES;5.1M ,1/8W ,5% ,0805,SMT,PRC	R10
271071562301	RES;5.6K ,1/16W,5% ,0603,SMT	R586,R664
271071536211	RES;53.6K,1/16W,1% ,0603,SMT	PR18
271071549811	RES;54.9 ,1/16W,1% ,0603,SMT	R695,R696,R697,R698
271071560301	RES;56 ,1/16W,5% ,0603,SMT	R517,R518
271071561101	RES;560 ,1/16W,1% ,0603,SMT	R22,24,28

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9. Spare Part List (12)

Part Number	Description	Location(s)
271071576311	RES;576K ,1/16W,1% ,0603,SMT	PR553
271071619111	RES;6.19K,1/16W,1% ,0603,SMT	PR536
271071634111	RES;6.34K,1/16W,1% ,0603,SMT	R104
271071649111	RES;6.49K,1/16W,1% ,0603,SMT	R756
271071682301	RES;6.8K ,1/16W,5% ,0603,SMT	PR514,R162,R165,R167
271071604811	RES;60.4 ,1/16W,1% ,0603,SMT	R524,R525
271071681301	RES;680 ,1/16W,5% ,0603,SMT	R592
271071683101	RES;68K ,1/16W,1% ,0603,SMT	R12
271071690101	RES;69.8,1/16W,1%,0603,SMT	R54,R68
271071698311	RES;698K ,1/16W,1% ,0603,SMT	
271071750302	RES;75 ,1/16W,5% ,0603,SMT	R538,R539,R547,R548
271071822301	RES;8.2K ,1/16W,5% ,0603,SMT	R19,R67
271071806211	RES;80.6K,1/16W,1% ,0603,SMT	PR518
271071820301	RES;82 ,1/16W,5% ,0603,SMT	R562
271071887211	RES;88.7K,1/16W,1% ,0603,SMT	R6
271071909011	RES;909 ,1/16W,1% ,0603,SMT	R14
271611000301	RP;0*4 ,8P ,1/16W,5% ,0612,SMT	RP1,RP2,RP3,RP4
271611152301	RP;1.5K*4,8P ,1/16W,5% ,0612,SMT	RP507
271571100301	RP;10*8 ,16P ,1/16W,5% ,1606,SM	RP10,RP11,RP12,RP13,RP14
271611103301	RP;10K*4 ,8P ,1/16W,5% ,0612,SMT	R116,RP34,RP35,RP38,RP50
271621103302	RP;10K*8 ,10P,1/32W,5% ,1206,SMT	RP513
271611102301	RP;1K*4 ,8P ,1/16W,5% ,0612,SMT	RP5,RP501,RP504,RP508
271621102302	RP;1K*8 ,10P,1/32W,5% ,1206,SMT	RP505,RP506
271611222301	RP;2.2K*4,8P ,1/16W,5% ,0612,SMT	RP518,RP521,RP522
271611220301	RP;22*4 ,8P ,1/16W,5% ,0612,SMT	RP515

Part Number	Description	Location(s)
271611392311	RP;3.9K*4,8P,1/16W,5%,0612,SMT	RP2,RP3
271611330301	RP;33*4 ,8P ,1/16W,5% ,0612,SMT	RP37,RP509,RP514
271571330301	RP;33*8 ,16P ,1/16W,5% ,1606,SM	RP18,RP19,RP20,RP21,RP22
271611331301	RP;330*4 ,8P ,1/16W,5% ,0612,SMT	RP526
271611472301	RP;4.7K*4,8P ,1/16W,5% ,0612,SMT	RP33,RP36,RP39,RP4,RP502
271621472302	RP;4.7K*8,10P,1/32W,5% ,1206,SMT	RP512
271611750301	RP;75*4 ,8P ,1/16W,5% ,0612,SMT	RP1
271611750301	RP;75*4 ,8P ,1/16W,5% ,0612,SMT	RP5
345671600002	RUBBER PAD;LCD,LOWER,8175	
345671600001	RUBBER PAD;LCD,UPPER,8175	
345503400001	RUBBER;2MM,ROUND,STINGRAY	
565167380001	S/W;CD ROM,SYSTEM DRIVER,8375	
565180626001	S/W;CD*1,DVD,WIN-DVD,INTERVIDEO	
565167000013	S/W;CD-ROM,B'S RECORDER GOLD2.0	
340671200014	SCREW ASSY;IC,82845,8170	
371102011502	SCREW;M2L15,FLT(+),NIW/NLK	
340673800003	SHIELDING ASSY; TOP,8375	
341671700001	SHIELDING;AUDIO,8575	
333050000119	SHRINK TUBE;600V,105'C,D0.8*6MM,	
333050000120	SHRINK TUBE;600V,105'C,D0.8*9MM,	
333050000107	SHRINK TUBE;UL,600V,105'C,ID2.5*	
333050000117	SHRINK TUBE;UL,600V,105'C,ID2.5*	
333050000116	SHRINK TUBE;UL,600V,105'C,ID3.5*	
333050000098	SHRINK TUBE;ULCSA,125'C,D0.7MM,B	
561860000022	SINGLE PAGE;GN,NOTE FOR BATTERY&	

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9. Spare Part List (13)

Part Number	Description	Location(s)
361400003021	SOLDER CREAM;NOCLEAN,P4020870980	
600100010010	SOLDER WIRE;63/37,0.5,CM,N/C,PRC	
370102610302	SPC-SCREW;M2.6L3,NIB,K-HD,NYLOK	
370102610401	SPC-SCREW;M2.6L4,K-HD,t0.8,NIB/N	
370102610401	SPC-SCREW;M2.6L4,K-HD,t0.8,NIB/N	
370102610603	SPC-SCREW;M2.6L6,K-HD,NIB/NLK	
370102610603	SPC-SCREW;M2.6L6,K-HD,NIB/NLK	
370102610801	SPC-SCREW;M2.6L8,NIB,K-HD,t=1.1,	
370102030301	SPC-SCREW;M2L3,K-HD,1,NIB/NLK	
370102030301	SPC-SCREW;M2L3,K-HD,1,NIB/NLK	
370102030301	SPC-SCREW;M2L3,K-HD,1,NIB/NLK	
370102030301	SPC-SCREW;M2L3,K-HD,1,NIB/NLK	
370102010407	SPC-SCREW;M2L4,K-HD,NIB/NLK	
370102010407	SPC-SCREW;M2L4,K-HD,NIB/NLK	
370102010401	SPC-SCREW;M2L4,NIB,FLT(+),NL,731	
370102010606	SPC-SCREW;M2L6,K-HD(t0.2),NIB/NL	
370103010405	SPC-SCREW;M3L4,NIW,K-HD,T0.3	
370103010604	SPC-SCREW;M3L6,NIB,K-HD,t0.8,NYL	
340671700003	SPEAKER ASSY,L,8575	
340671700008	SPEAKER ASSY;R,8575	
226600030149	SPONGE/2ADHESIVE;CR-RUBBER/G9000	
226600030058	SPONGE;CR,T=1.5MM,W=8MM,PRC	
377244010002	STANDOFF;#4-40DP3.5H5L5.5,NIW	
341670400006	STANDOFF;HEATSINK,GRAMPUS	
341668300008	STANDOFF;MDC MODEM,NLK,HOPE	

Part Number	Description	Location(s)
297120101007	SW;DIP,SPST,4P,24VDC,.025A,SMT	SW6
297040105010	SW;PUSH BUTTOM,5P,SPST,12V/50MA,	SW1,SW2,SW3,SW4
297120100009	SW;SPST,4P,24VDC,50MA,STS-KD5,HC	SW5
297030102001	SW;TOGGLE,SPST,5V/0.2mA,H10.7MM,	SW1
225600000309	TAPE;3M-467/DOUBLE RELEASE PAPER	
225600000032	TAPE;ACETURM ADHESTIVE,W=4mm,BLK	
225600000032	TAPE;ACETURM ADHESTIVE,W=4mm,BLK	
225600000034	TAPE;ACETURN ADHESI,W=10mm,PRC	
225600000061	TAPE;ADHENSIVE,DOUBLE-FACE,W20,U	
225600000310	TAPE;ADHENSIVE,DOUBLE-FACE,W8,UL	
225671700002	TAPE;BRACKET,LCD,8575	
622200000008	TAPE;CARTON,2.5"W,30M/RL,PRC	
225600000375	TAPE;CONDUCTIVE/DOUBLE RELEASE P	
225600000004	TAPE;DOUBLE SIDE,12MM*15M	
225600000237	TAPE;G9000,W=110,PRC	
225600000312	TAPE;G9000,W=113,PRC	
225600000344	TAPE;G9000,W=220,PRC	
225600000268	TAPE;G9000,W=72,PRC	
225600000054	TAPE;INSULATING,POLYESTER FILM,1	
225600000027	TAPE;INSULATOR,W10T0.06,UL-510	
225600000143	TAPE;SONY G9000,W=10,T=0.15,PRC	
225600000177	TAPE;T=0.05MM,W=7MM,KAPTON/ADHES	
333334000046	TERMINAL;HRS/DF13-2630SCF,PRC	
333334000046	TERMINAL;HRS/DF13-2630SCF,PRC	
333334000084	TERMINAL;JAE/FI-C3-A1-15000,PRC	

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9. Spare Part List (14)

Part Number	Description	Location(s)
333334000099	TERMINAL;JST/SSH-003T-P0.2,PRC	
346673800010	THERMAL PAD;DDR,8375	
345671700002	THERMAL PAD;MOS,8575	
310111103013	THERMISTOR;10K,1%,RA,DISK,103AT-	
442164900010	TOUCH PAD MODULE;TM41PD-350	
288227002001	TRANS;2N7002LT1,N-CHANNEL FET,SO	PQ3,PQ501,PQ502,PQ503,P
288227002001	TRANS;2N7002LT1,N-CHANNEL FET,SO	PQ2,PQ501,PQ502,PQ503
628820014401	TRANS;DTA144EKA,PNP,100MA,50V,SO	
288200144002	TRANS;DTA144WK,PNP,SMT	Q541
288200144003	TRANS;DTC144TKA,N-MOSFET,SOT-23	Q11,Q12,Q13,Q503,Q517,Q5
288200144001	TRANS;DTC144WK,NPN,SOT-23,SMT	PQ507,Q514,Q521,Q524,Q52
288206612003	TRANS;FDD6612A,30V,30A,.028hm,N-	PU501,PU502,PU503,PU504
288206676004	TRANS;FDD6676,30V,78A,.0085hm,N-	PU1,PU2,PU3,PU4
288200301001	TRANS;FDV301N,N-CHANNEL,SOT23	Q522,Q537,Q538
288202222001	TRANS;MMBT2222AL,NPN,TO236AB	PQ2,Q507,Q508,Q529,Q531,
288203904010	TRANS;MMBT3904L,NPN,Tr35NS,TO236	Q502,Q519
288203906002	TRANS;MMBT3906L,40V,200mA,SOT23,	Q1
288203906018	TRANS;MMBT3906L,PNP,Tr35NS,TO236	PQ506
288202301001	TRANS;SI2301DS,P-MOSFET,SOT-23	Q18,Q513,Q516
288202301001	TRANS;SI2301DS,P-MOSFET,SOT-23	PQ1
288202302001	TRANS;SI2302DS,N-MOSFET,SOT-23	Q512
288204416001	TRANS;Si4416DY,N-MOSFET,.028OHM,	PU2,PU5
288204425002	TRANS;SI4425DY,PMOS,8.5A/30V,0.0	PU502
288204425002	TRANS;SI4425DY,PMOS,8.5A/30V,0.0	
288204532001	TRANS;SI4532DY,N&P-MOSFET,SO8,PR	U2

Part Number	Description	Location(s)
288204800001	TRANS;SI4800DY,N-MOS,.0185OHM,SO	PU5,PU7,PU9
288204810001	TRANS;SI4810DY,N-MOS,.0155OHM,SO	PU3,PU6
288204832001	TRANS;SI4832DY,N-MOSFET,.028OHM,	PU6,PU8
288204835001	TRANS;SI4835DY,PMOS,6A/30V,.035,	PQ1,PU11,PU12
288204925001	TRANS;SI4925DY,P-MOSFET,SO-8	PU10
288209410001	TRANS;SI9410DY,N-MOSFET,.04OHM,S	Q501
270140000003	VARISTOR;280V,5.6X3.8MM,TVB280-0	S501
271911103906	VR;10K,20%,0.05W,RN101GAC10KPGJ-	VR1
421673800001	WIRE ASSY;ANTENNA;8375	
421668300005	WIRE ASSY;BIOS,BATTERY,HOPE	
421671600010	WIRE ASSY;INVERT,8175	
421671600006	WIRE ASSY;LCD,UNIPAC,14",XGA,817	
421671700001	WIRE ASSY;TOUCHPAD,8575	
332110020057	WIRE;#20,UL1007,122MM,RED,PRC	
332110020028	WIRE;#20,UL1007,50MM,RED,PRC	
332110020050	WIRE;#20,UL1007,55MM,BLK,PRC	
332110020020	WIRE;#20,UL1007,BLK,PRC	
332110020019	WIRE;#20,UL1007,RED,PRC	
332110020019	WIRE;#20,UL1007,RED,PRC	
332110026096	WIRE;#26,UL1007,165MM,WHITE,PRC	
332110026097	WIRE;#26,UL1007,55MM,BLACK,PRC	
332110026099	WIRE;#26,UL1007,93MM,YELLOW,PRC	
332110026008	WIRE;#26,UL1007,BLACK,PRC	
332110026016	WIRE;#26,UL1007,WHITE,PRC	
332110026013	WIRE;#26,UL1007,YELLOW,PRC	

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9. Spare Part List (15)

Part Number	Description	Location(s)
332110030058	WIRE;#30,UL1571,OD0.6mm,BLACK,PR	
332110030052	WIRE;#30,UL1571,OD0.6mm,BLUE,PRC	
332110030059	WIRE;#30,UL1571,OD0.6mm,BROWN,PR	
332110030055	WIRE;#30,UL1571,OD0.6mm,GREEN,PR	
332110030050	WIRE;#30,UL1571,OD0.6mm,GREY,PRC	
332110030057	WIRE;#30,UL1571,OD0.6mm,ORANGE,P	
332110030060	WIRE;#30,UL1571,OD0.6mm,ORANGE/B	
332110030053	WIRE;#30,UL1571,OD0.6mm,PURPLE,P	
332110030056	WIRE;#30,UL1571,OD0.6mm,RED,PRC	
332110030051	WIRE;#30,UL1571,OD0.6mm,WHITE,PR	
332110030054	WIRE;#30,UL1571,OD0.6mm,YELLOW,P	
332110032036	WIRE;#32,1571,BLACK/RED/#28,DRAI	
332110032014	WIRE;#32,UL1571,BLK,PRC	
332110032006	WIRE;#32,UL1571,BLK/WHT,PRC	
332110032005	WIRE;#32,UL1571,BROWN/WHT,PRC	
332110032002	WIRE;#32,UL1571,GRAY,PRC	
332110032003	WIRE;#32,UL1571,ORANGE/BLK,PRC	
332110032004	WIRE;#32,UL1571,RED/WHT,PRC	
332110032001	WIRE;#32,UL1571,WHT,PRC	
273001050039	XSFORMER;10/100 BASE,LF-H80P,SMT	U3
273001050062	XSFORMER;CI8.5,SIT16260,16/2600T	T1
274011431408	XTAL;14.318M,50PPM,32PF,7*5,4P,S	X3
274011431409	XTAL;14.318MHZ,16PF,50PPM,8*4.5,	X502
274012457405	XTAL;24.576M,50PPM,16PF,7*5,4P,S	X4
274012457406	XTAL;24.576MHZ,16PF,50PPM,8*4.5,	X5

Part Number	Description	Location(s)
274012500401	XTAL;25MHZ,30PPM,18PF,4P,SMT	X503
274013276103	XTAL;32.768KHZ,20PPM,12.5PF,CM20	X6
274010800405	XTAL;8Mhz,30PPM,16PF,8*4.5,2P,SM	X501
		P/N:526267385011

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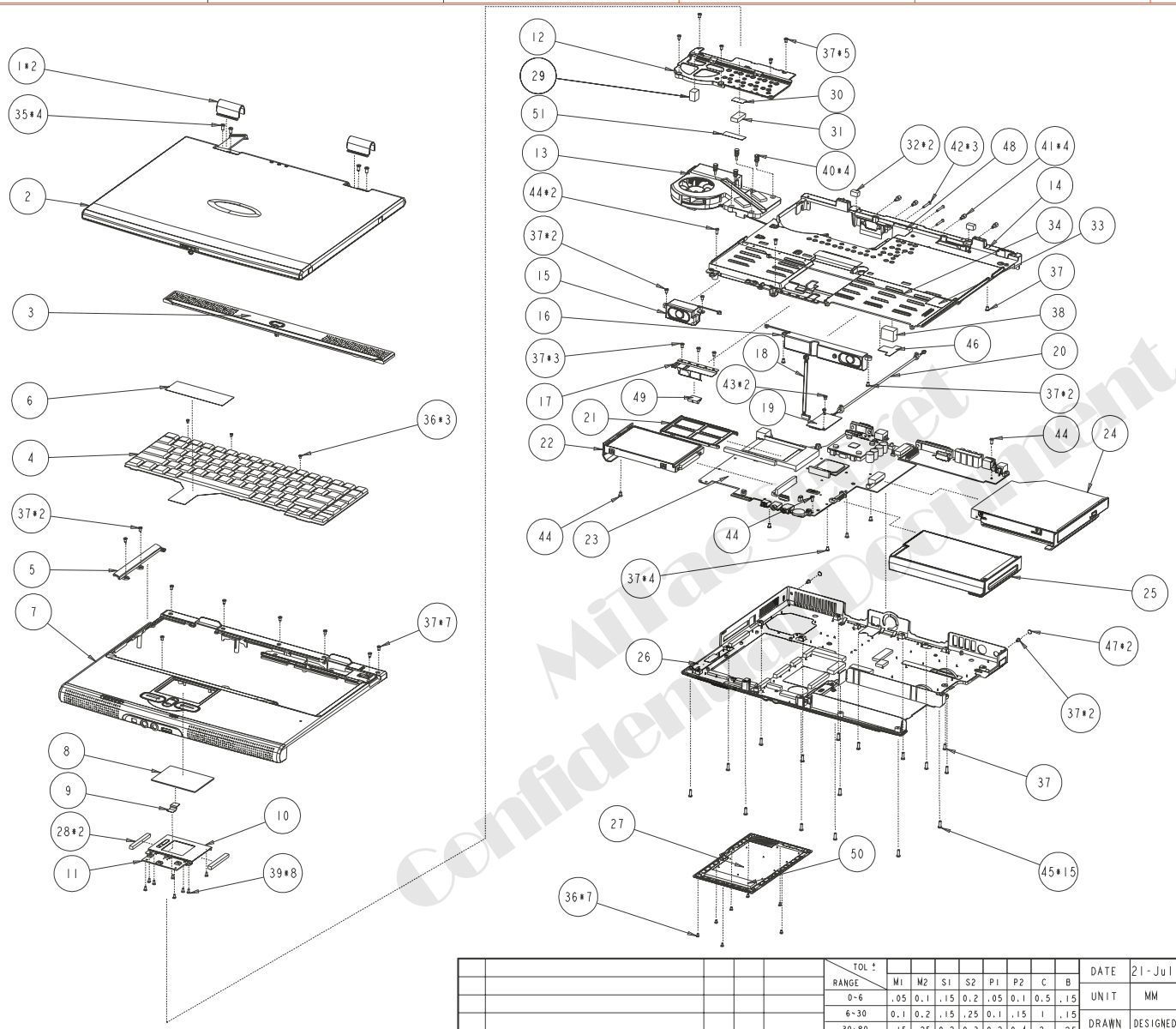

ITEM	PART NO.	DESCRIPTION	Q'TY	REMARK
1	344671720023	COVER;HINGE,1D3,8575	2	
2	441673800001	LCD ASSY;QD1,XGA,14.1",1D3,8375	1	OPTION
3	340673800002	COVER ASSY;K/B,8375	1	
4	5310999901 28	KBD OPTION;86,US,8175	1	OPTION
5	344671720002	COVER;DUMMY,1D3,8575	1	
6	225671700007	TAPE;CONDUCTIVE,KB,ESD,8575	1	
7	340671720001	COVER ASSY;1D3,8575	1	
8	442164900010	TOUCH PAD MODULE;TM41PD-350	1	
9	422665400002	FFC ASSY;TOUCH PAD,CASE KIT,VENUS	1	
10	340671600028	BRACKET ASSY;T/P,INSULATOR,8175	1	
11	411671700009	PWA;PWA-8575,T/P BD	1	
12	343673800003	PLATE;KB,8375	1	
13	340673800001	HEATSINK ASSY;8375	1	
14	340673800003	SHIELDING ASSY;TOP,8375	1	
15	340671700003	SPEAKER ASSY;L,8575	1	
16	340671700008	SPEAKER ASSY;R,8575	1	
17	341671700001	SHIELDING;AUDIO,8575	1	
18	421671700001	WIRE ASSY;TOUCH PAD,8575	1	
19	412155600047	PCB ASSY;MDM,56K,UNIV,F-PACK,WO/KIT	1	
20	421673800003	CABLE ASSY;MDC,8375	1	
21	344670500042	DUMMY CARD;PCMCIA,TETRA	1	
22	523467380004	HDD ASSY;MHR2020AT,FUJITSU,8375	1	OPTION
23	411673800001	PWA;PWA-8375,MOTHER BD	1	
24	523467380002	DVD ROM ASSY;8X,SDR-083,QUANTA,1D3,8375	1	OPTION
25	441999900065	BATT ASSY OPTION;LI-ION,2000mAH,8575 1D3	1	OPTION
26	340673800006	HOUSING ASSY;8375	1	
27	340673830001	COVER ASSY;DIMM,1D3,8375	1	
28	345671700009	GASKET;BRACKET T/P,8575	2	
29	345671600018	GASKET;HEATSINK,K/B PLATE,8175	1	
30	345671700010	GASKET;KB PLATE,8575	1	
31	345671700011	GASKET;KB PLATE-1,8575	1	
32	345673500018	GASKET;6x6x10,WEASEL	2	
33	345671700019	GASKET;MIC,8575	1	
34	421671600051	MICROPHONE ASSY;8175	1	
35	370103010604	SPC-SCREW;M3L6,NIB,K-HD,±0.8,NYLOK	4	
36	371102030303	SCREW;M2L3,,K-HEAD(+),NIW/NLK	10	
37	370102610405	SPC-SCREW;M2.6L4,NIW,K-HD,±0.8,NLK	30	
38	345673800006	GASKET;ESD-2,SHIELDING,8375	1	
39	370102010407	SPC-SCREW;M2L4,K-HD,NIB/NLK	8	
40	341670400006	STANDOFF;HEATSINK,GRAMPUS	4	
41	377240410002	STANDOFF;#4-40DP3.5H5L5.5,NIW	4	
42	371102011502	SCREW;M2L15,FLT(+),NIW/NLK	3	
43	370102610302	SPC-SCREW;M2.6L3,NIB,K-HD,NYLOK	2	
44	370102610603	SPC-SCREW;M2.6L6,K-HD,NIB/NLK	4	
45	370102610805	SPC-SCREW;M2.6L8,K-HD,NIW/NLK	15	
46	345671700002	THERMAL PAD;MOS,8575	1	
47	346671720002	INSULATOR;REAR,SCREW,1D3,8575	2	
48	340671200020	FAN ASSY;8170	1	
49	346673800004	BE-CU;SHIELDING,AUDIO,8375	1	
50	346673800010	THERMAL PAD;DDR,8375	1	
51	346673800012	CONDUCTIVE TAPE;PLATE,8375	1	

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ITEM	CONTENTS OF CHANGE	CHK	APV	MM/DD/YY

TOL ± RANGE	M1	M2	S1	S2	P1	P2	C	B
0~6	.05	0.1	.15	0.2	.05	0.1	0.5	.15
6~30	0.1	0.2	.15	.25	0.1	.15	1	.15
30~80	.15	.25	0.2	0.3	0.2	0.4	2	.25
80~180	.15	0.3	.25	.45	0.4	0.8	3	.25
180~315	0.2	0.5	0.4	0.6	0.6	1.2	3	0.3
315~800	0.3	0.8	0.7	1.1	0.8	1.5	4	0.5

DATE	21-Jul-02	MATERIAL	SEE NOTES	TREATMENT		REMARK
UNIT	MM	SCALE	0.260	DRAWING NAME	LT PF;QD1,XGA,14.1",1D3,8375	
DRAWN	DESIGNED	CHECKED	APPROVED	MATERIAL NO.	AD	416267380001 R00

MiTAC International Corp.

SHEET NO.1 OF 1

Model name:MAIN-ASSY-8575 File name:MAIN-ASSY-1D3-8375

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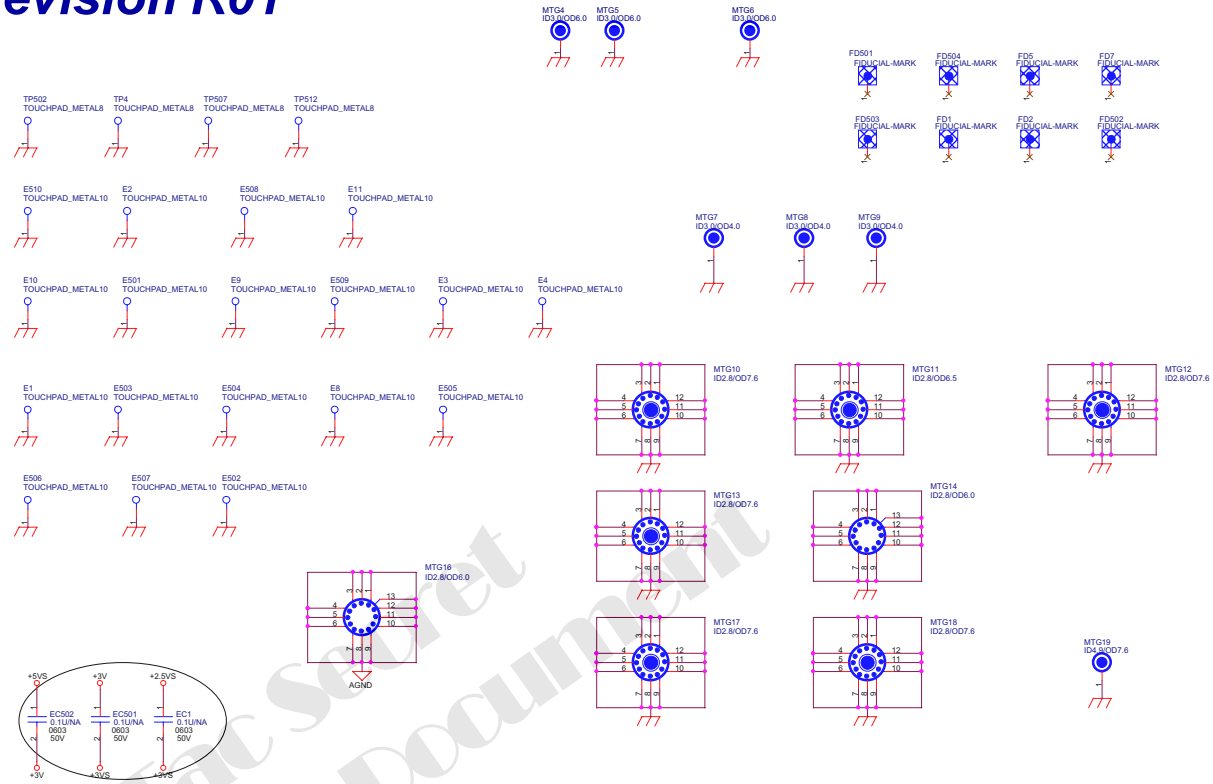
MODEL:8375

Revision R01

Contexts

Title	Page
COVER SHEET & SCREW HOLE	1
System Block Diagram	2
Power Block Diagram	3
AMD K7 (1/2)	4
AMD K7 (2/2)	5
VIA KN266(1/3)	6
VIA KN266(2/3)	7
VIA KN266(3/3)	8
TV/LVDS ENCODER (VT6122)	9
LCD/VGA INTERFACE & LEDs	10
MAIN CLOCK (ICS950902)	11
DDR SODIMMs	12
DDR TERMINATION	13
VIA VT8235(1/3)	14
VIA VT8235(2/3)	15
VIA VT8235(3/3)	16
IDE INETRFACE	17
PCI 1410 / PU2211	18
LAN PHY (VIA VT6103) & MDC	19
AUDIO CODEC (VIA VT1612A) & AUDIO AMP	20
SUPER I/O, T/P & BUTTON	21
MICROCONTROLLER(W83L950D)	22
BATTERY CONNECT AND +1.25V	23
2.5v_DDR	24
CHARGER	25
CPU CORE	26
D/D CONNECTOR	27
MINI PCI SLOT	28
VIA VT6306 IEEE1394	29
THERMAL IC	30



POWER STATES

STATE / SIGNAL	VOTAGE	FULL ON	STR	STD	MEC-OFF	REMARK
-SUSB	-	HIGH	LOW	LOW	LOW	
-SUSC	-	HIGH	HIGH	LOW	LOW	
ADP	+19V	0	0	0	0	
BATTERY	+12V	0	0	0	0	
+VCC_RTC	+3.3V	0	0	0	0	
+VCC_CORE	+1.75V	0	0	X	X	
+2.5VS	+2.5V	0	X	X	X	
+2.5V	+2.5V	0	0	X	X	
+2.5V_DDR	+2.5V	0	0	X	X	
+3VS	+3.3V	0	X	X	X	
+3V	+3.3V	0	0	X	X	
+3VA	+3.3V	0	0	0	0	
+5VS	+5V	0	X	X	X	
+5V	+5V	0	0	X	X	
+5VA	+5V	0	0	0	0	
+12VS	+12V	0	X	X	X	
+12V	+12V	0	0	X	X	

IDSEL

IDSEL	CHIP
AD20	TI1410
AD22	1394(VIA VT6306)

BUS MASTER

REQ/GNT	CHIP
-REQ0/-GNT0	TI1410
-REQ1/-GNT1	1394(VIA VT6306)

PCIINT

PCIINT	CHIP
INTA#	VIA KN266
INTB#	PCMCIA (TI1410)
INTC#	1394 (VIA VT6306)

DRAW	DESIGN	CHECK	ISSUED

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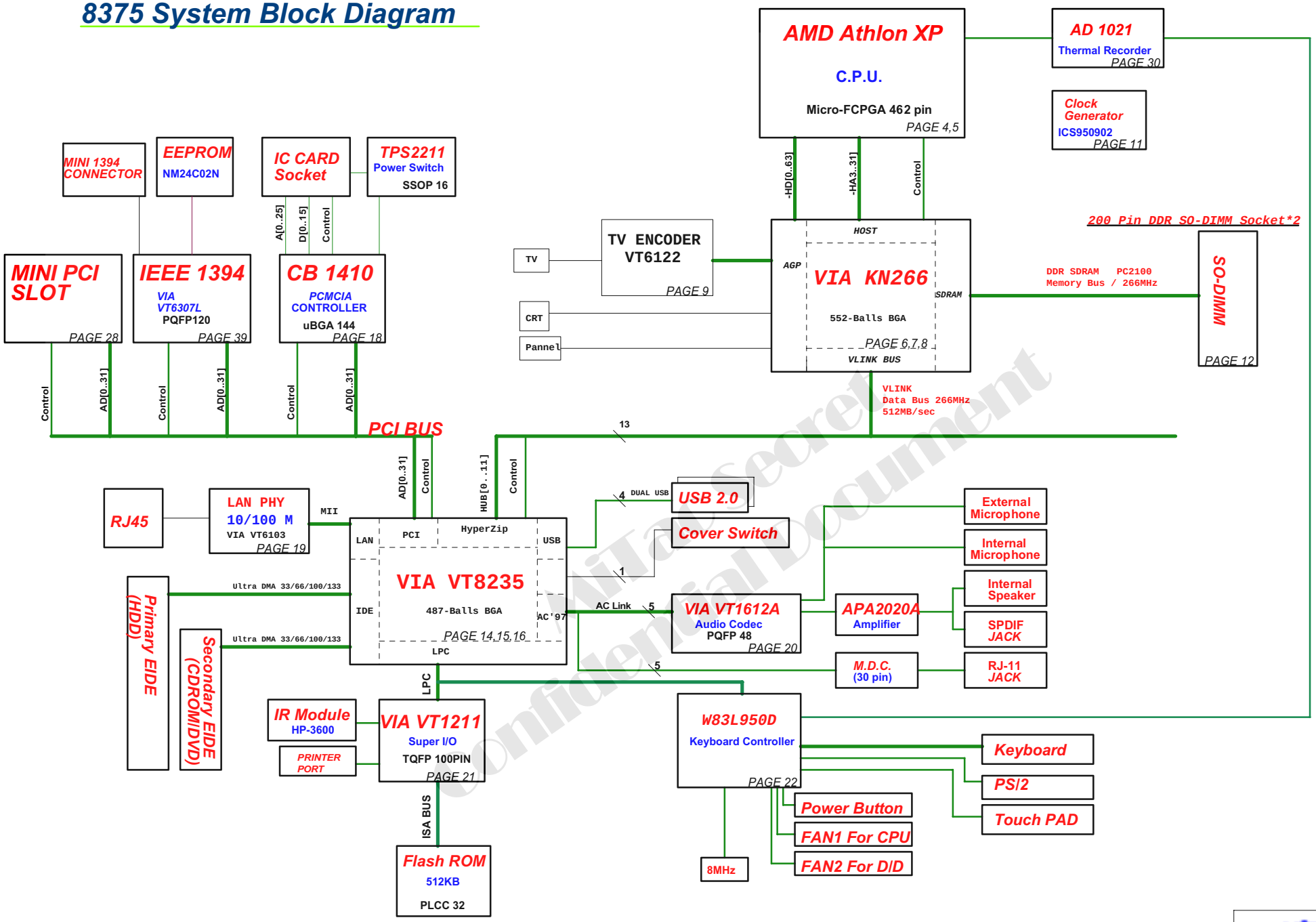
Title: 8375 COVER SHEET & SCREW HOLE

Size: C | Document Number: BD 316673800001 & TU 411673800001 | Rev: 01

Date: Monday, August 12, 2002 | Sheet 1 of 31

8375 System Block Diagram



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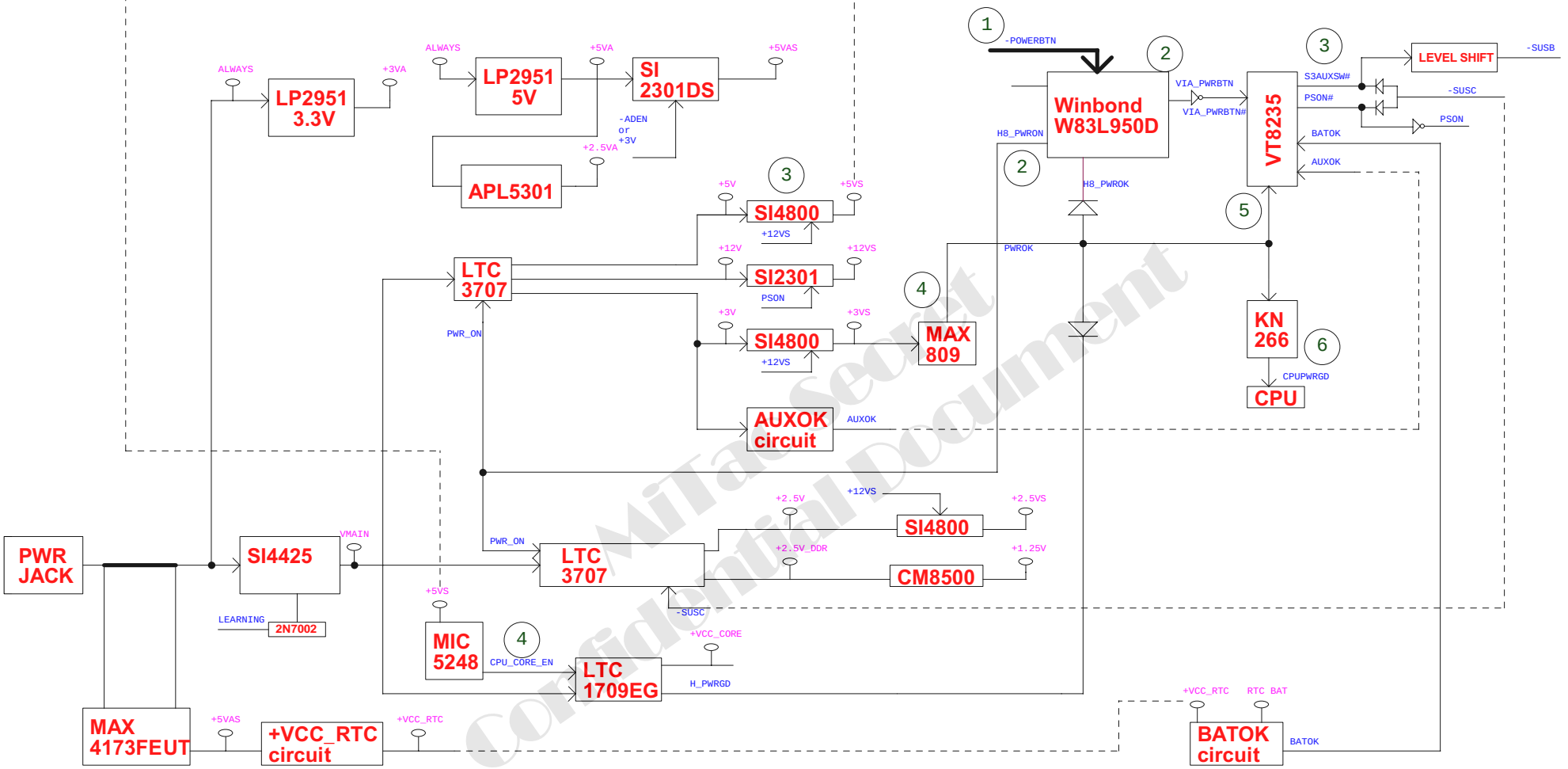
Title	8375 SYSTEM BLOCK DIAGRAM	
Size	Document Number: BD 316673800001 & TU 411673800001	Rev 01
Date: Monday, August 12, 2002	Sheet 2 of 31	

POWER BLOCK DIAGRAM OF THE 8375 PROJECT



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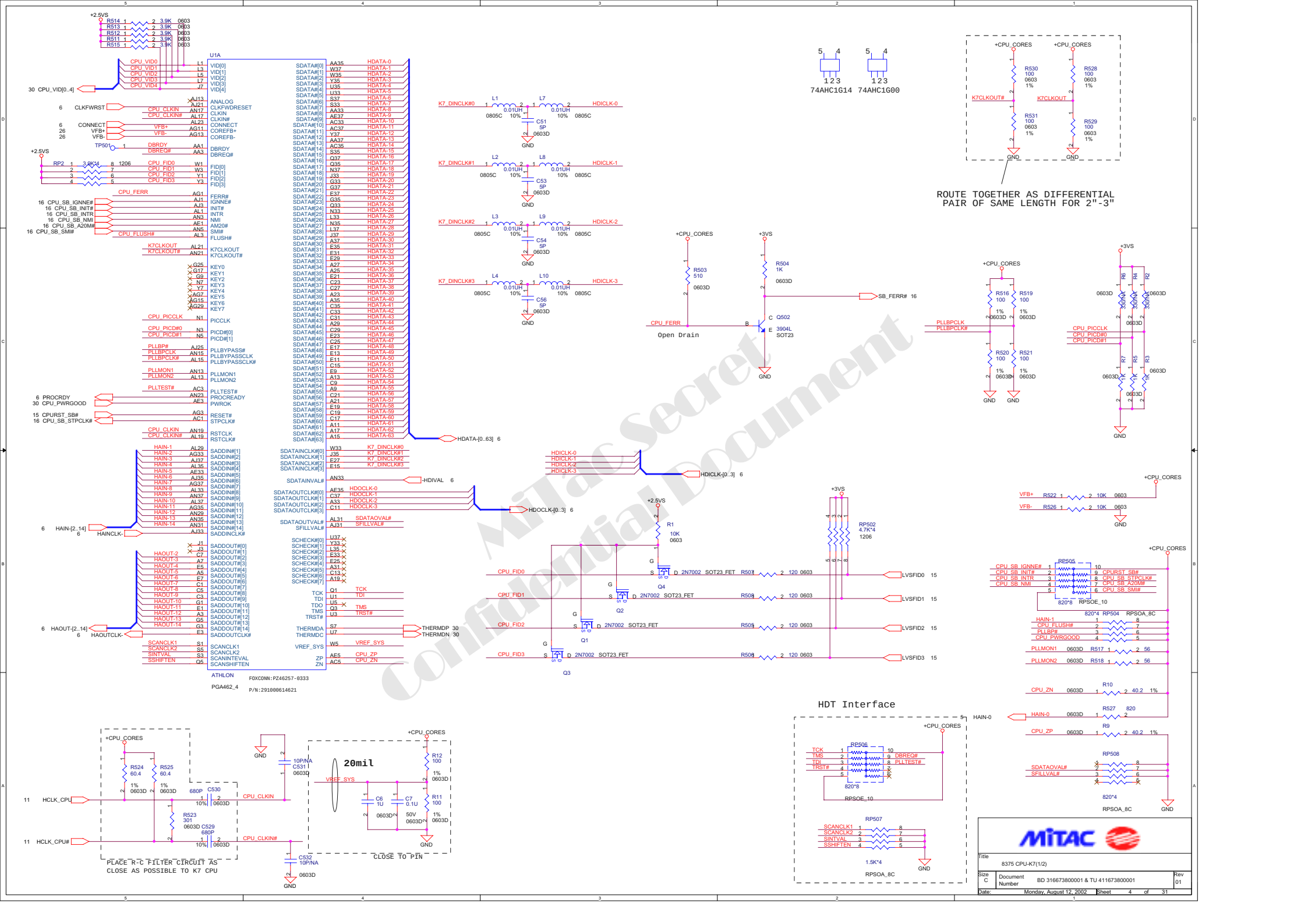
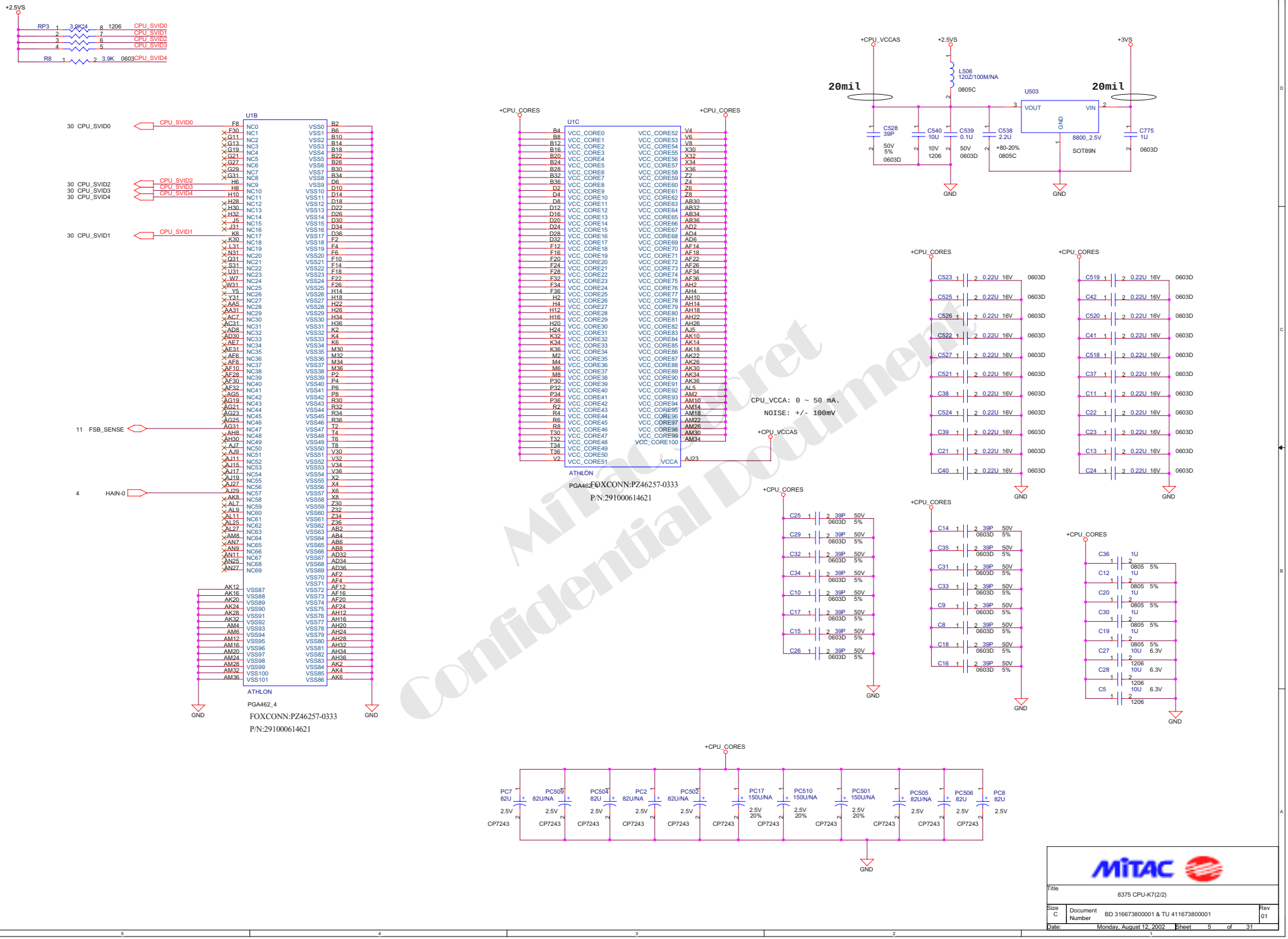
電子訊號線

視線輔助線

MiTAC

Title	8375 POWER BLOCK DIAGRAM	
Size	Document Number BD 316673800001 & TU 411673800001	Rev 01
Date: Monday, August 12, 2002	Sheet 3 of 31	


U1A
ATHLON
PGA462_4
FOXCONN:PZ46257-0333
P/N:291000614621
74AHC1G14 74AHC1G00
ROUTE TOGETHER AS DIFFERENTIAL PAIR OF SAME LENGTH FOR 2"-3"
Open Drain
HDT Interface
PLACE R-C FILTER CIRCUIT AS CLOSE AS POSSIBLE TO K7 CPU
CLOSE TO PIN
20mil
MiTAC Secret Confidential Document
Title
8375 CPU-K7(1/2)
Size C
Document Number
BD 316673800001 & TU 411673800001
Rev 01
Date: Monday, August 12, 2002
Sheet 4 of 31



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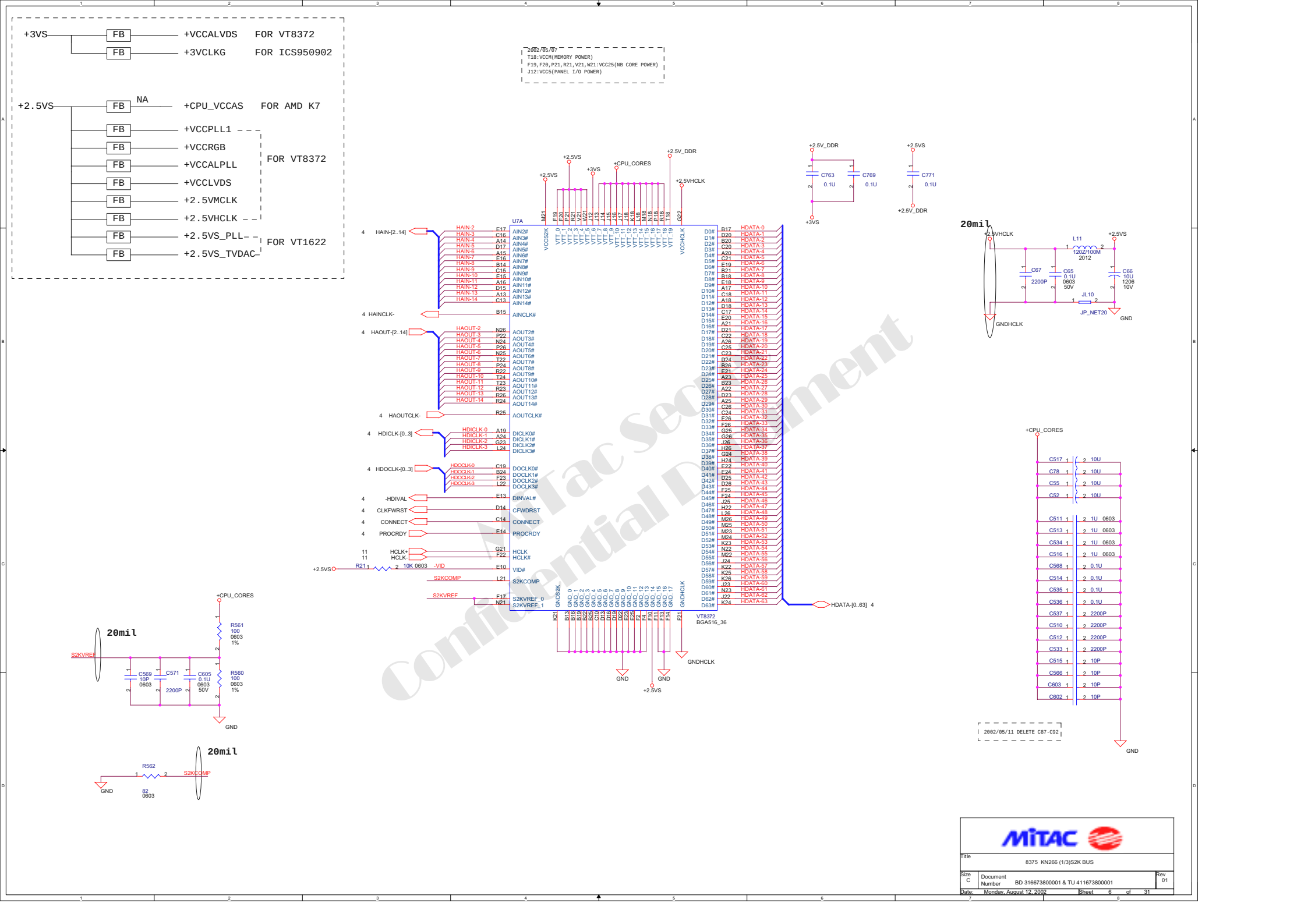
Title	8375 CPU-K7(2/2)		
Size C	Document Number	BD 316673800001 & TU 411673800001	Rev 01
Date: Monday, August 12, 2002	Sheet 5	of 31	



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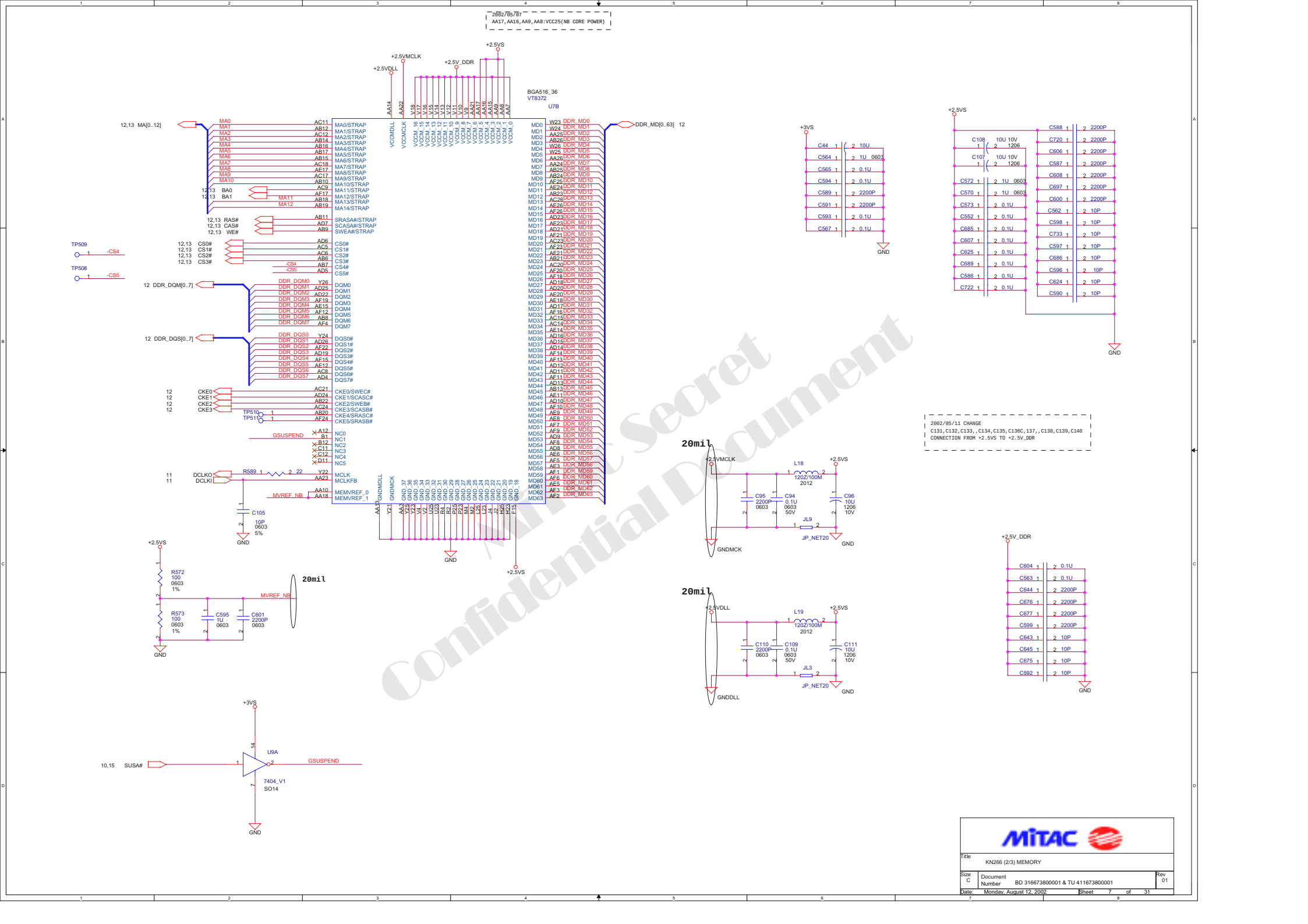
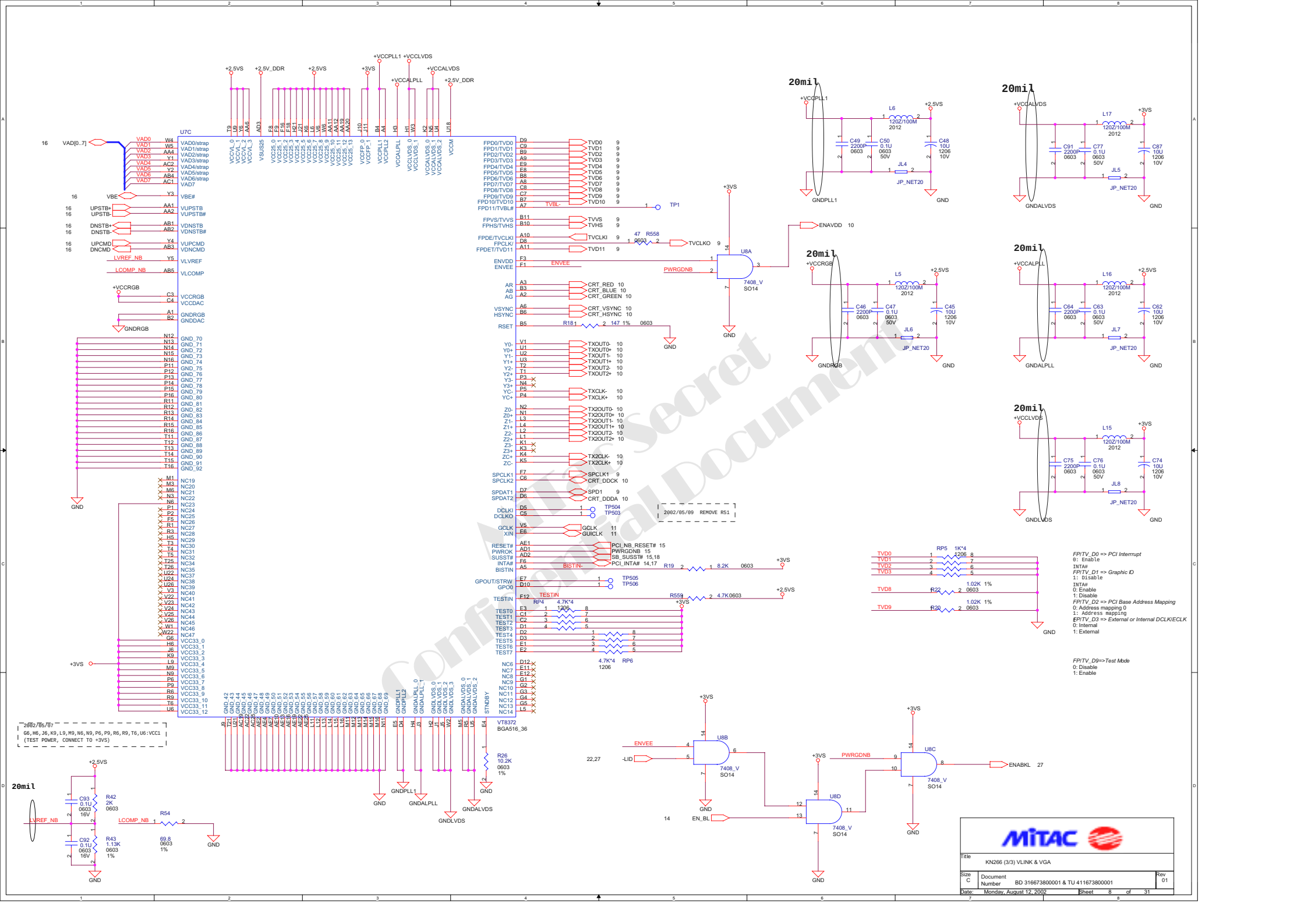
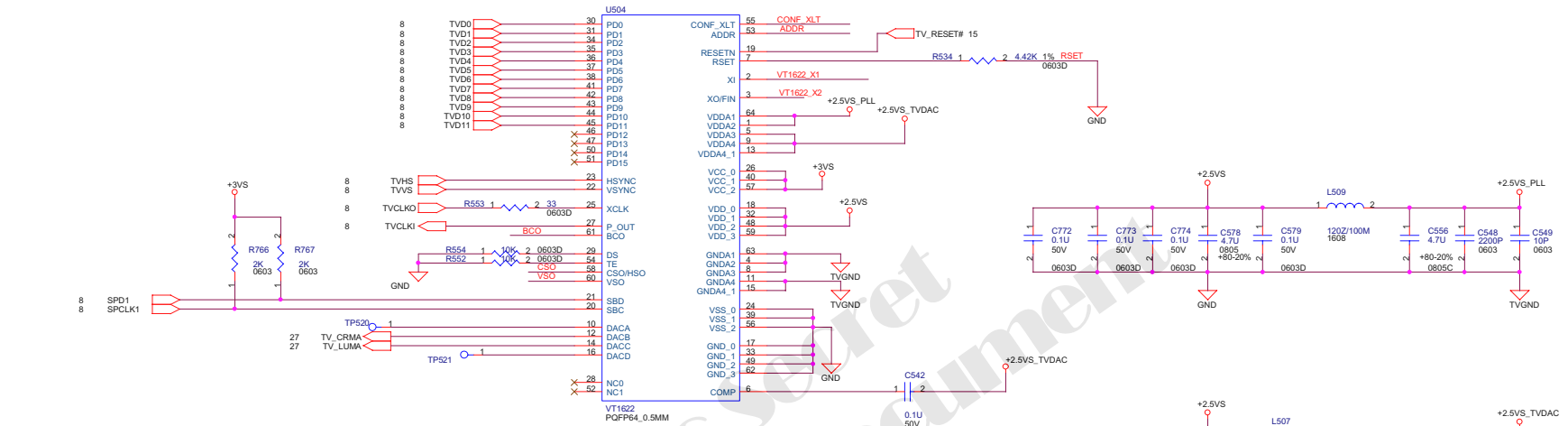
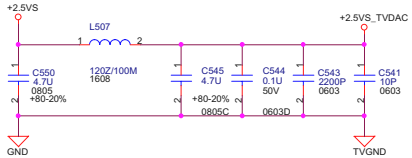
Title	8375 KN266 (1/3)S2K BUS	
Size C	Document Number BD 316673800001 & TU 411673800001	Rev 01
Date: Monday, August 12, 2002	Sheet 6 of 31	

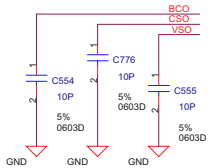

2002/05/07
AA17,AA16,AA9,AA8:VCC25(NB CORE POWER)
BGA516_36
VT8372
U7B
+2.5VS
+2.5VMCLK
+2.5VDLL
+2.5V_DDR
12,13 MA[0..12]
DDR_MD[0..63] 12
12,13 BA0
12,13 BA1
12,13 RAS#
12,13 CAS#
12,13 WE#
12,13 CS0#
12,13 CS1#
12,13 CS2#
12,13 CS3#
TP509
TP508
12 DDR_DQM[0..7]
12 DDR_DQS[0..7]
12 CKE0
12 CKE1
12 CKE2
12 CKE3
TP510
TP511
GSUSPEND
11 DCLKO
11 DCLKI
R589
C105
10P
0603
5%
GND
MVREF_NB
R572
100
0603
1%
R573
100
0603
1%
C595
1U
0603
C601
2200P
0603
20mil
+3VS
U9A
7404_V1
SO14
10,15 SUSA#
GSUSPEND
C44 10U
C564 1U 0603
C565 0.1U
C594 0.1U
C589 2200P
C591 2200P
C593 0.1U
C567 0.1U
C108 10U 10V 1206
C107 10U 10V 1206
C572 1U 0603
C570 1U 0603
C573 0.1U
C552 0.1U
C685 0.1U
C607 0.1U
C625 0.1U
C689 0.1U
C586 0.1U
C722 0.1U
C588 2200P
C720 2200P
C606 2200P
C587 2200P
C608 2200P
C697 2200P
C600 2200P
C562 10P
C598 10P
C733 10P
C597 10P
C686 10P
C596 10P
C624 10P
C590 10P
2002/05/11 CHANGE
C131,C132,C133,,C134,C135,C136C,137,,C138,C139,C140
CONNECTION FROM +2.5VS TO +2.5V_DDR
20mil
+2.5VMCLK
L18
120Z/100M
2012
C95
2200P
0603
C94
0.1U
0603
50V
C96
10U
1206
10V
JL9
JP_NET20
GNDMCK
20mil
+2.5VDLL
L19
120Z/100M
2012
C110
2200P
0603
C109
0.1U
0603
50V
C111
10U
1206
10V
JL3
JP_NET20
GNDDLL
+2.5V_DDR
C604 0.1U
C563 0.1U
C644 2200P
C676 2200P
C677 2200P
C599 2200P
C643 10P
C645 10P
C675 10P
C592 10P
MiTAC Secret
Confidential Document
MiTAC
Title
KN266 (2/3) MEMORY
Size
C
Document Number
BD 316673800001 & TU 411673800001
Rev
01
Date: Monday, August 12, 2002
Sheet 7 of 31

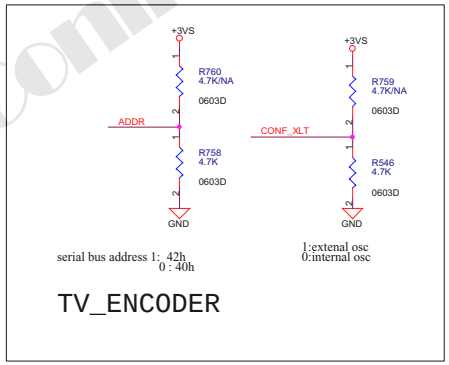

U7C
VT8372
BGA516_36
U8A
U8B
U8C
U8D
7408_V
SO14
+VCCPLL1
+VCCCLVDS
+VCCALVDS
+VCCALPLL
+2.5VS
+2.5V_DDR
+3VS
+VCCRGB
+VCCVLDS
GNDRGB
GNDPLL1
GNDALPLL
GNDLVDS
GNDALVDS
20mil
L6
L5
L15
L16
L17
120Z/100M
2012
JP_NET20
TP1
TP504
TP503
TP505
TP506
2002/05/09 REMOVE R51
RP5 1K*4 1206
RP4 4.7K*4 1206
RP6 4.7K*4 1206
R26 10.2K 0603 1%
R42 2K 0603
R43 1.13K 0603 1%
R54 69.8 0603 1%
R181 147 1% 0603
R19 8.2K 0603
R559 4.7K 0603
R22 1.02K 1% 0603
R20 1.02K 1% 0603
ENVEE
ENVDD
PWRGDNB
ENABKL
-LID
EN_BL
LVREF_NB
LCOMP_NB
TESTIN
BISTIN-
FP/TV_D0 => PCI Interrupt
0: Enable
1: Disable
FP/TV_D1 => Graphic ID
0: Disable
1: Enable
FP/TV_D2 => PCI Base Address Mapping
0: Address mapping 0
1: Address mapping
FP/TV_D3 => External or Internal DCLK/ECLK
0: Internal
1: External
FP/TV_D9=>Test Mode
0: Disable
1: Enable
MiTAC
KN266 (3/3) VLINK & VGA
BD 316673800001 & TU 411673800001
Monday, August 12, 2002
Sheet 8 of 31
Rev 01
Size C
Document Number
Date:
Title
MiTAC Secret Confidential Document

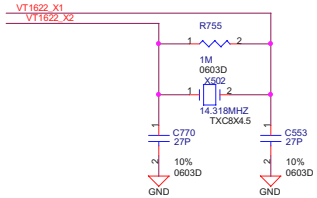
2002/05/09 DELETE
R637,R638,R639,R640,R641,R642,R643,R644,C734,U39
TV CLOCK SPREAD SPECTRUM CIRCUIT

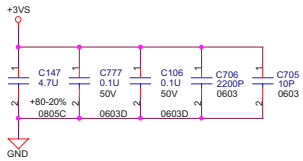












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MiTAC

Title	TV ENCODER (VT1622)	
Size C	Document Number BD 316673800001 & TU 411673800001	Rev 01
Date: Monday, August 12, 2002	Sheet 9 of 31	

LCD & CRT INTERFACE

LED INDICATOR

D16	D15	D13	D14	D15
CDROM	HDD	NUM	CAP	SCROLL

(NA D10,D8,D9,D11,D15,R586 ,R211,R212,R213,R96, For LCD 15")

C280 1U 0603, C277 1U 0603, C279 1U 0603

+5VS

R150 470 0603, R146 470 0603, R149 470 0603

D17 PG1102W, D15 PG1102W, D16 PG1102W

22 -SCROLL, 22 -NUM, 22 -CAP

-SCROLL, -NUM, -CAP

R147 1M 0603D

+3V

U18A, U18B, U18C — 74AHC14_V TSSOP14

GND

C276 4.7U +80-20% 0805C

R148 220K 0603D

-BATT_LED

Q11 DTC114TKA SOT23AN_1

-BATT_LED 27

SUSA# 7,15

Q12 DTC114TKA SOT23AN_1

BATT_POWER# 22

NEW PART

DTC114TKA;10K,20mA,P/N:288200114001

DTC124TKA;22K,10mA,P/N:288200124003

DTC144TKA;47K,5mA,P/N:288200144003

R723 10K 0603

D18 PG1102W

MPCI_PD 15,28

Q13 DTC114TKA SOT23AN_1

R151 470 0603

LCD CONNECTOR

LCD 14" 330mA,15"800mA

80mil or Power Plane

LCDVCC

J3 MA/20PX2/ST ACES 87216-4000

TX2CLK+, TX2CLK-, TX2OUT0+, TX2OUT0-, TX2OUT2+, TX2OUT2-, TXOUT2+, TXOUT2-

LCD_ID0, LCD_ID1, LCD_ID2

RP503 10K*4 1206

RP501 1K*4 1206

GND1, GND2

L502 120Z/100M 2012, F502 SMDC110

Q501 NDS9410 SO8

C1 1000P 0603, C501 0.1U 0603 50V, C504 1000P 0603, C503 10U 1206 10V

Close to LCD Connector

C502 0.1U 0603 50V

+12VS

R502 470K 0603

Q503 DTC144TKA

ENAVDD

CLOSE TO NDS9410

C508 0.1U 0603 50V, C509 10U_NA 1206 10V

Layout Note:

S/W/W/S=12/6/6/12 mils as short as possible

四組各自平行走線等長

W/S=16/12/12/12/16 mils

CRT_RED, CRT_GREEN, CRT_BLUE, CRT_DDDA, CRT_HSYNC, CRT_VSYNC, CRT_DDCK

R16 2.2K 0603, R17 2.2K 0603

Q5, Q6, Q7, Q8 2N7002

Close to VGA Connector

L501130Z/100M 1608, L503130Z/100M 1608, L504130Z/100M 1608

FA501 130OHM/100MHZ

CP1 22P*4/NA 1206, RP1 75*4 1206, CP502 22P*4 1206, CP501 22P*4 1206, C2 10U_NA 1206 10V

JL2 SHORT-SMT3, JL1 SHORT-SMT3

U501 PACDN006/NA SSOP8

F503 SMDC110/NA

D503 EC11FS2/NA, D3 BAV99/NA

DDC2B

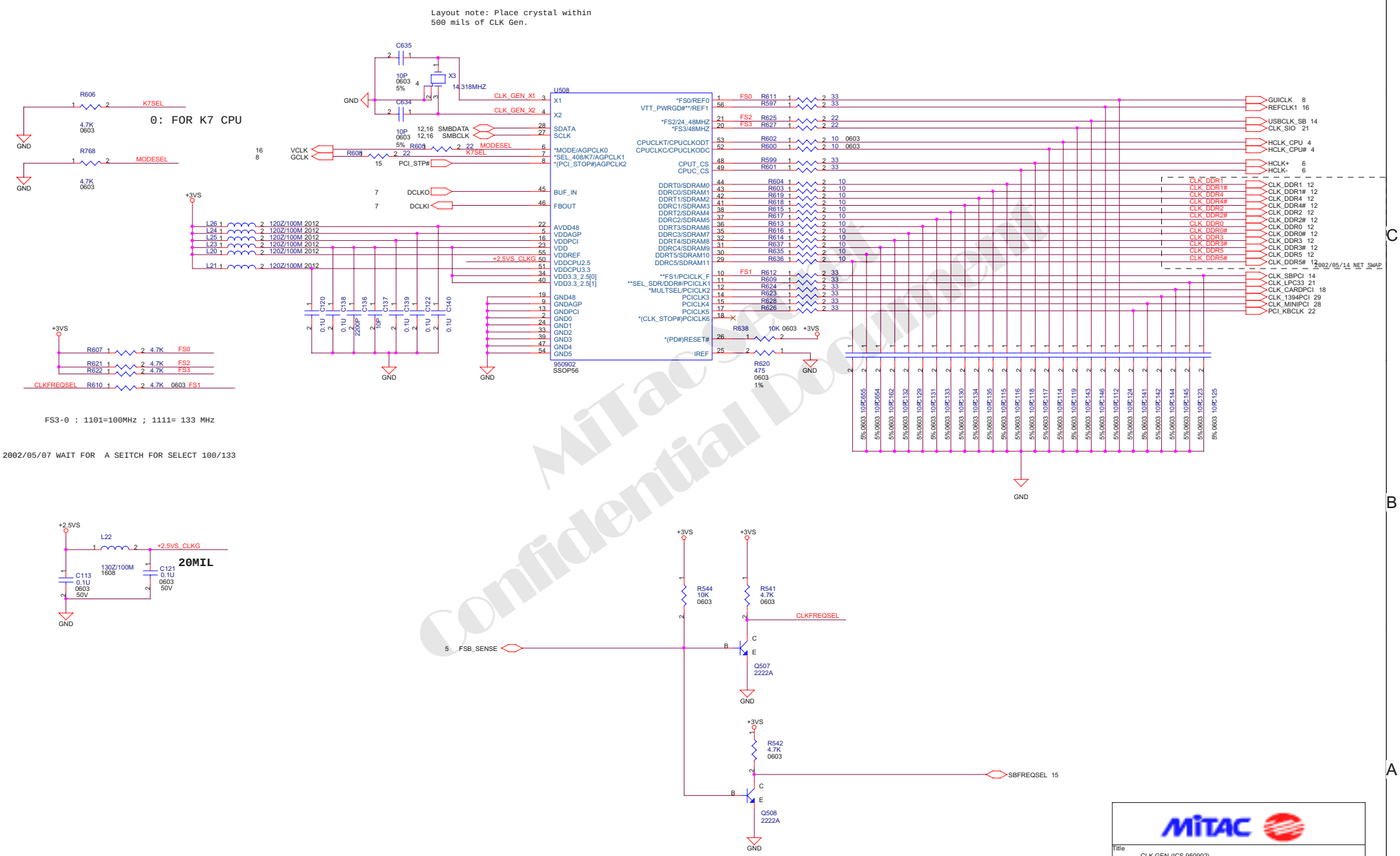
GNDRGB

J1 VGA SUYIN 7535S-15G2T-05 External VGA Connector

MiTac Secret Confidential Document

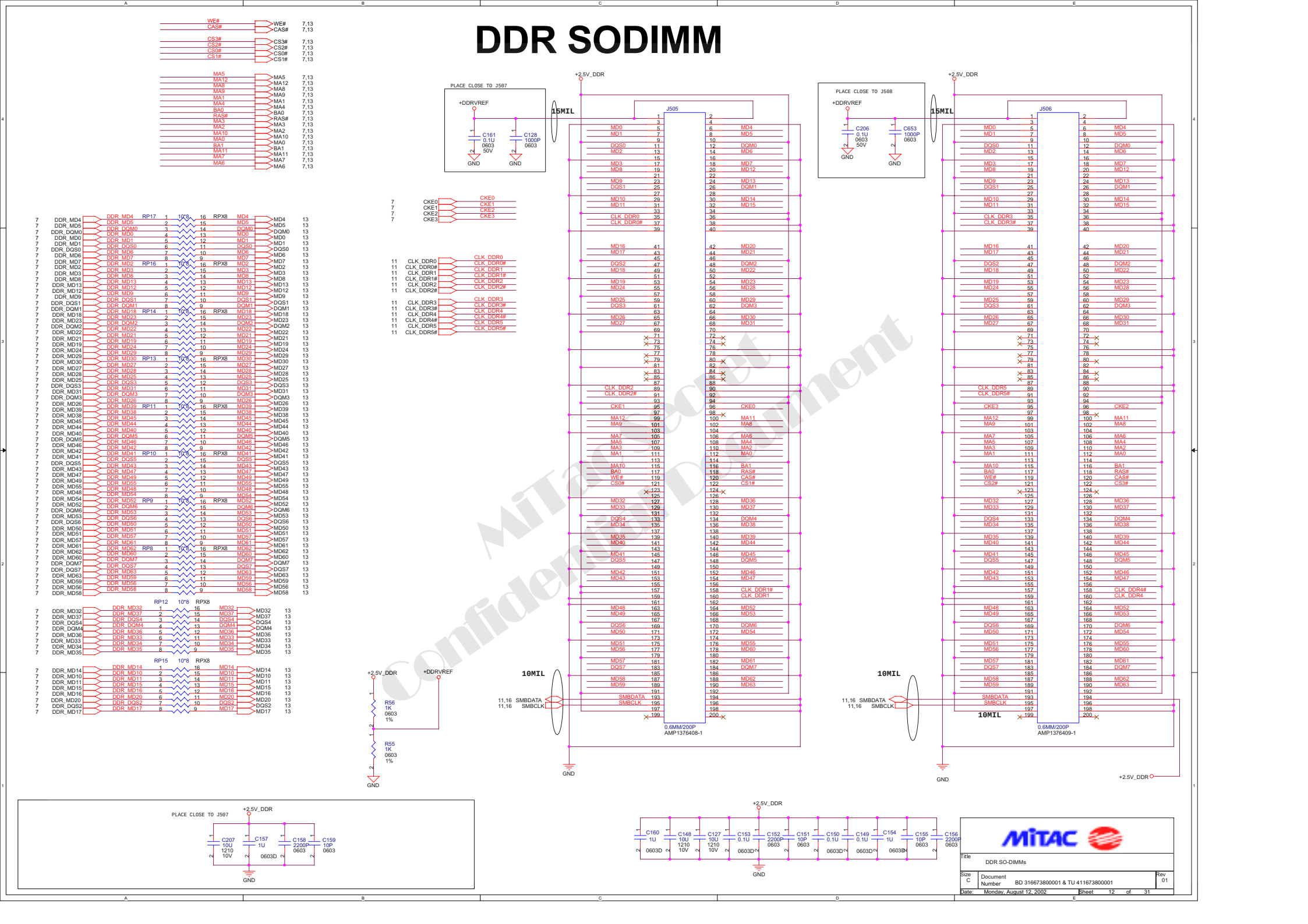
MiTAC

Title	LCD/VGA INTERFACE	
Size	Document Number: BD 316673800001 & TU 411673800001	Rev: 01
Date: Monday, August 12, 2002	Sheet 10 of 31	



Title	CLK GEN (ICS 950902)
Size	Document Number: BD 316673800001 & TU 411673800001
Rev	01
Date:	Monday, August 12, 2002
Sheet	11 of 31

DDR SODIMM



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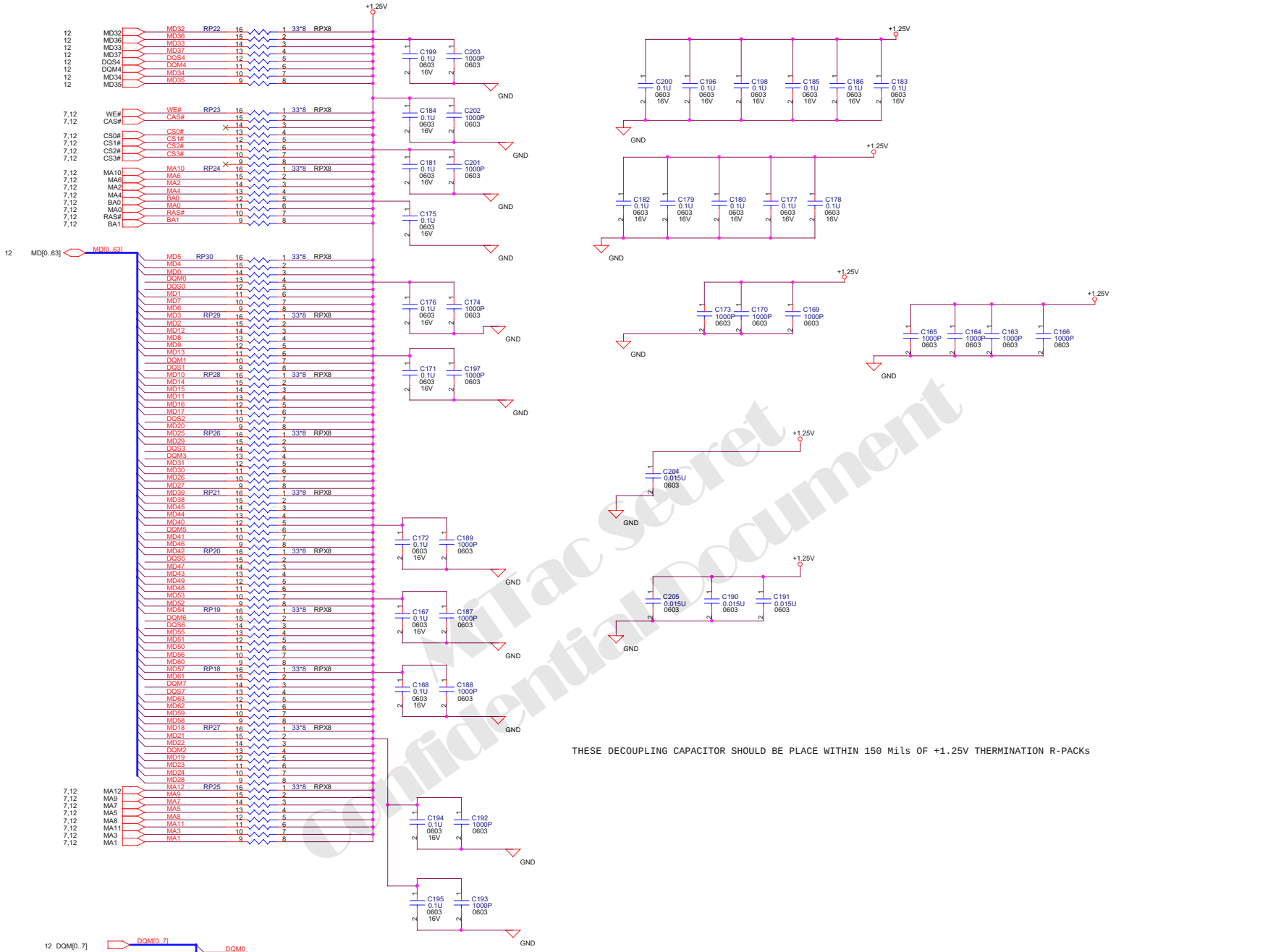
Confidential Document

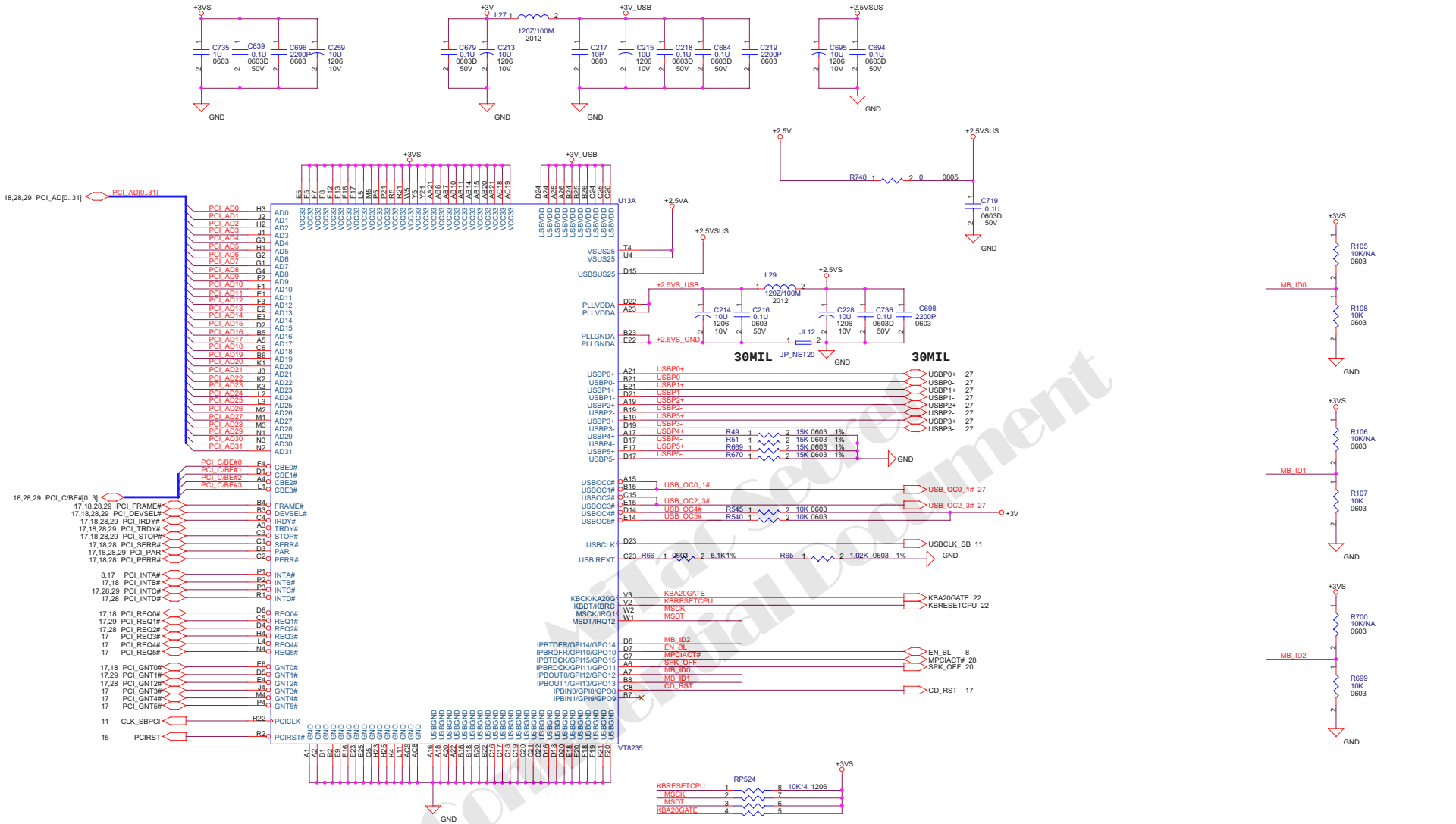
Title	DDR SO-DIMMs
Size	C
Document Number	BD 316673800001 & TU 411673800001
Rev	01
Date:	Monday, August 12, 2002
Sheet	12 of 31



THESE DECOUPLING CAPACITOR SHOULD BE PLACE WITHIN 150 Mils OF +1.25V THERMINATION R-PACKs

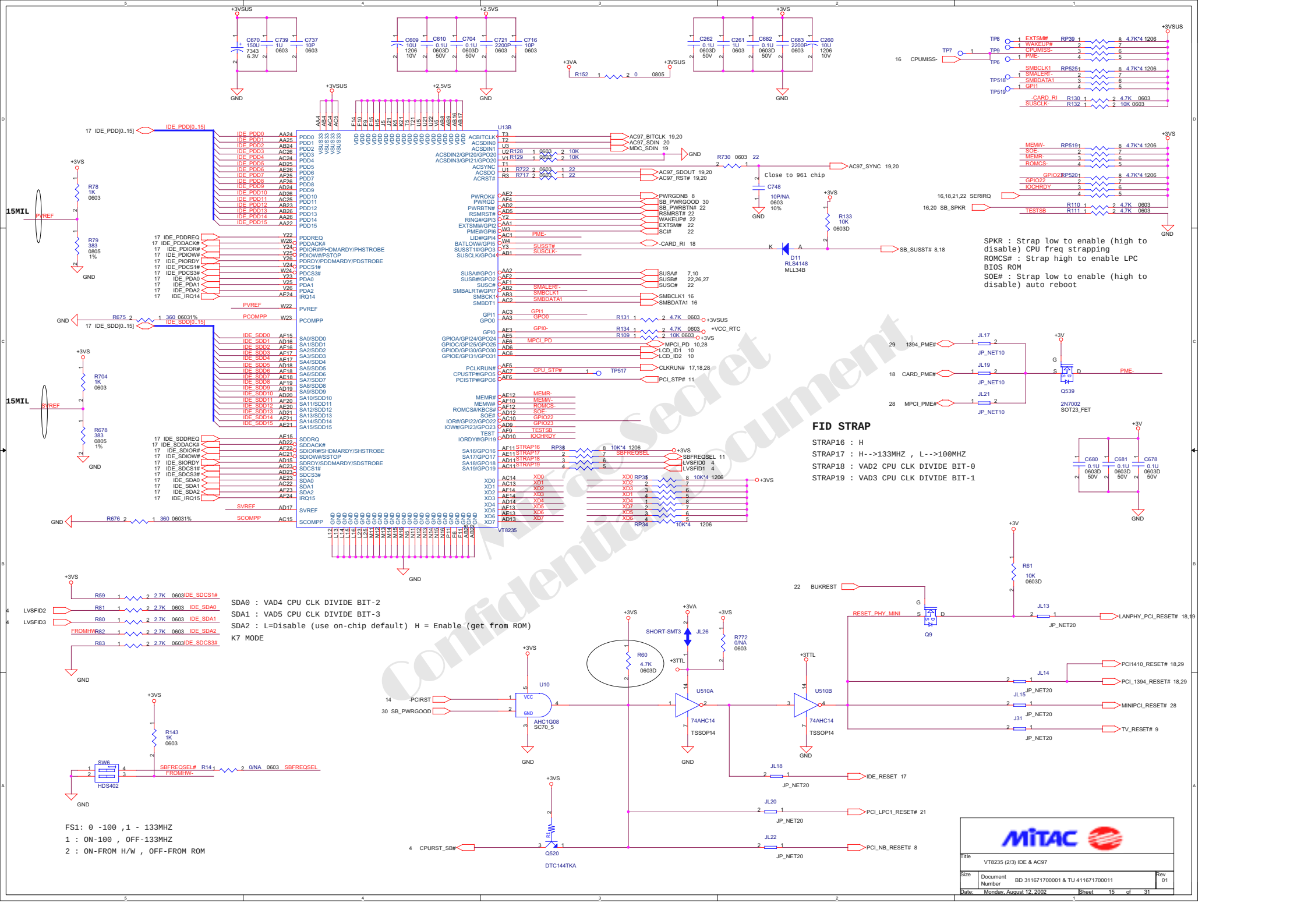
MiTac secret
Confidential Document

Title	DDR TERMINATION		
Size C	Document Number BD 316673800001 & TU 411673800001		Rev 01
Date: Monday, August 12, 2002	Sheet 13 of 31		



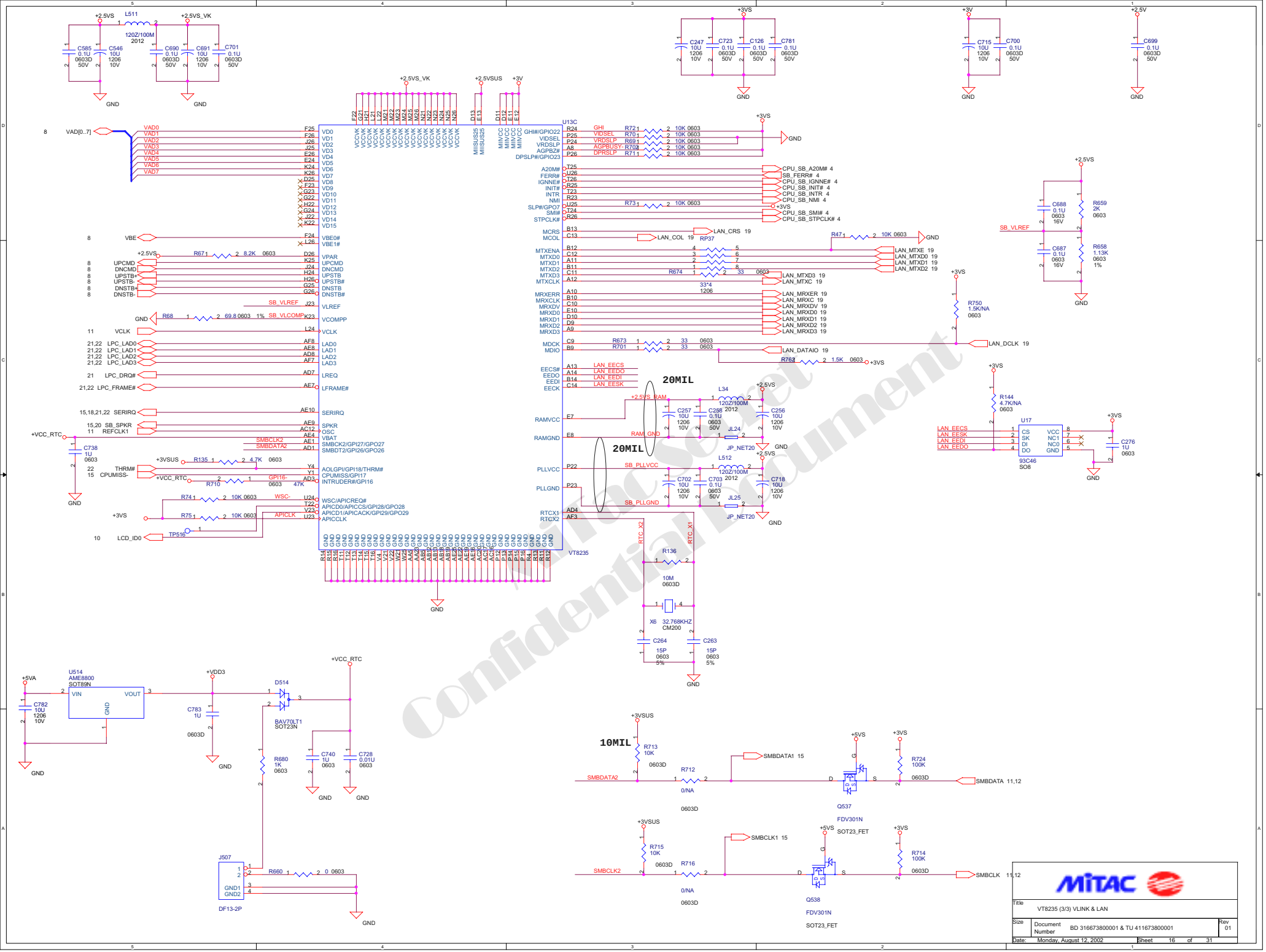
Wistron Secret Confidential Document

Title	VT8235 (1/3)PCI&USB	
Size	Document Number: BD 316673800001 & TU 411673800001	Rev 01
Date: Monday, August 12, 2002	Sheet 14 of 31	



Confidential Document
MiTAC Secret

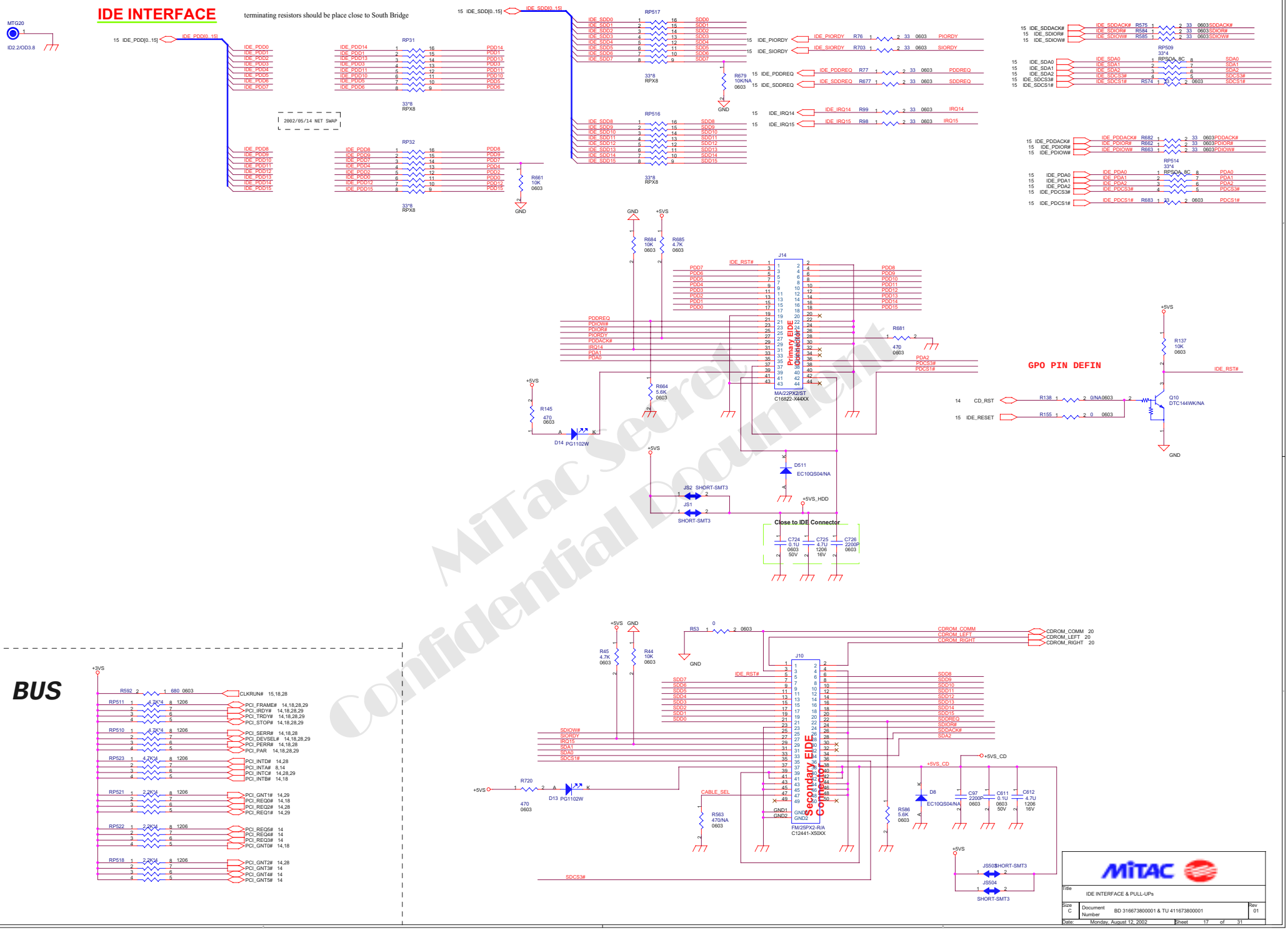
Title	VT8235 (2/3) IDE & AC97
Size	Document Number: BD 311671700001 & TU 411671700011 — Rev 01
Date:	Monday, August 12, 2002 — Sheet 15 of 31



Title	VT8235 (3/3) VLINK & LAN
Size	Document Number: BD 316673800001 & TU 411673800001
Rev	01
Date:	Monday, August 12, 2002
Sheet	16 of 31

IDE INTERFACE

terminating resistors should be place close to South Bridge



PCI BUS

MiTac Secret Confidential Document

Title	IDE INTERFACE & PULL-UPs		
Size C	Document Number BD 316673800001 & TU 411673800001		Rev 01
Date: Monday, August 12, 2002	Sheet 17 of 31		

PCMCIA CONTROLLER & CARDBUS SCOKET

PCI1410

AD20

PCI_INTB#

REQ0#/GNT0#

FOR TI 1410

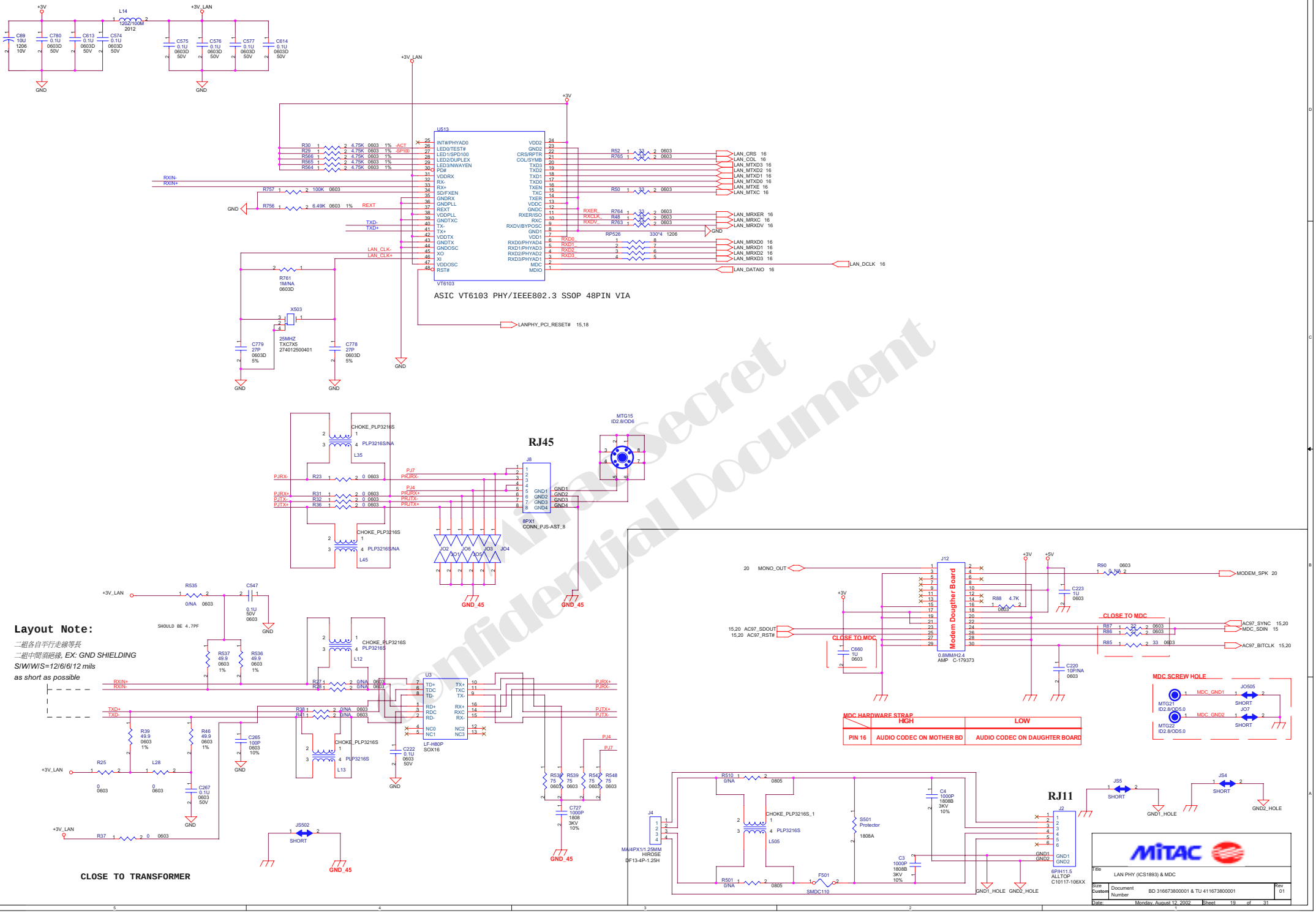
SIGNAL	PC CARD PULL UP	VOLT
CCD#1	+3V	
CCD#2	+3V	
CBLOCK#	CARD_VCC	
CSTOP#	CARD_VCC	
CDEVSEL#	CARD_VCC	
CTRDY#	CARD_VCC	
CVS1	+3V	
CVS2	+3V	
CRST#	CARD_VCC	
CSERR#	CARD_VCC	
CPERR#	CARD_VCC	
CINT#	CARD_VCC	
CIRDY#	CARD_VCC	
CREQ#	CARD_VCC	
CSTSCHG#	CARD_VCC	
CAUDIO	CARD_VCC	

PCI1410 HAVE INTEGRATED ALL PULL UP RES ABOVE

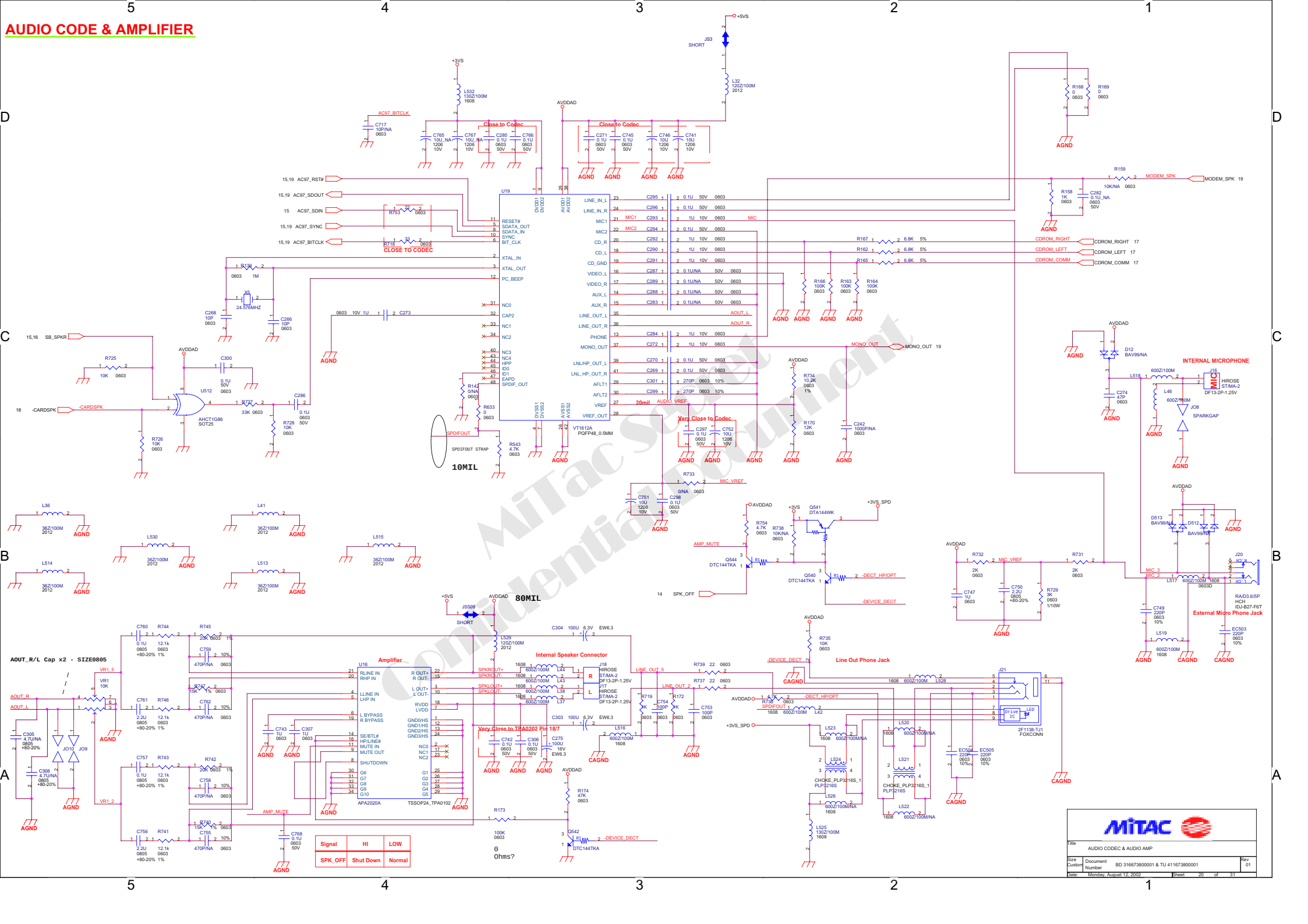
Card Bus Socket

MiTac Secret Confidential Document

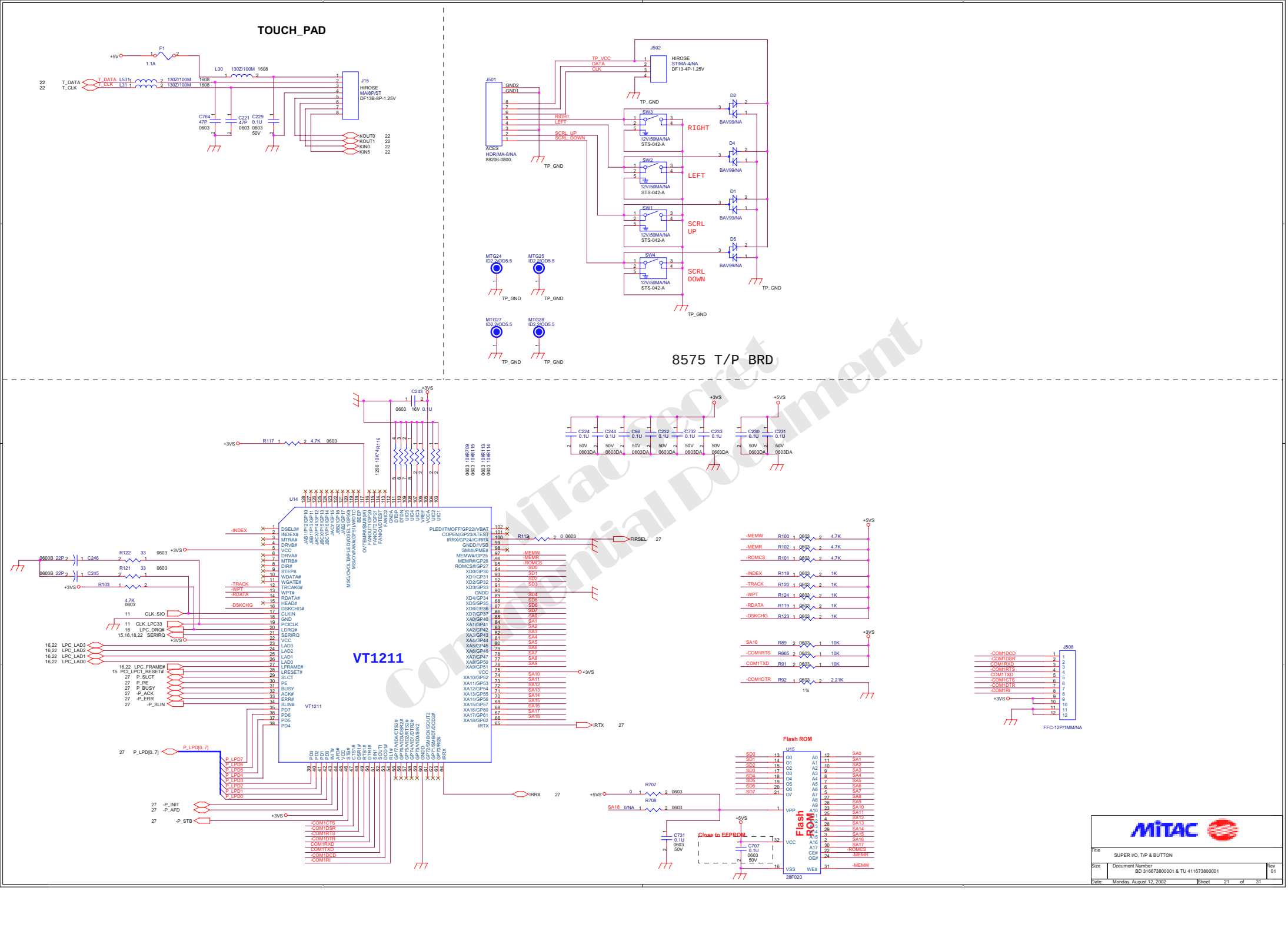
Title	PCI410 & CARDBUS SOCKET
Size	Document Number: BD 316673800001 & TU 411673800001 Rev 01
Date:	Monday, August 12, 2002 Sheet 18 of 31

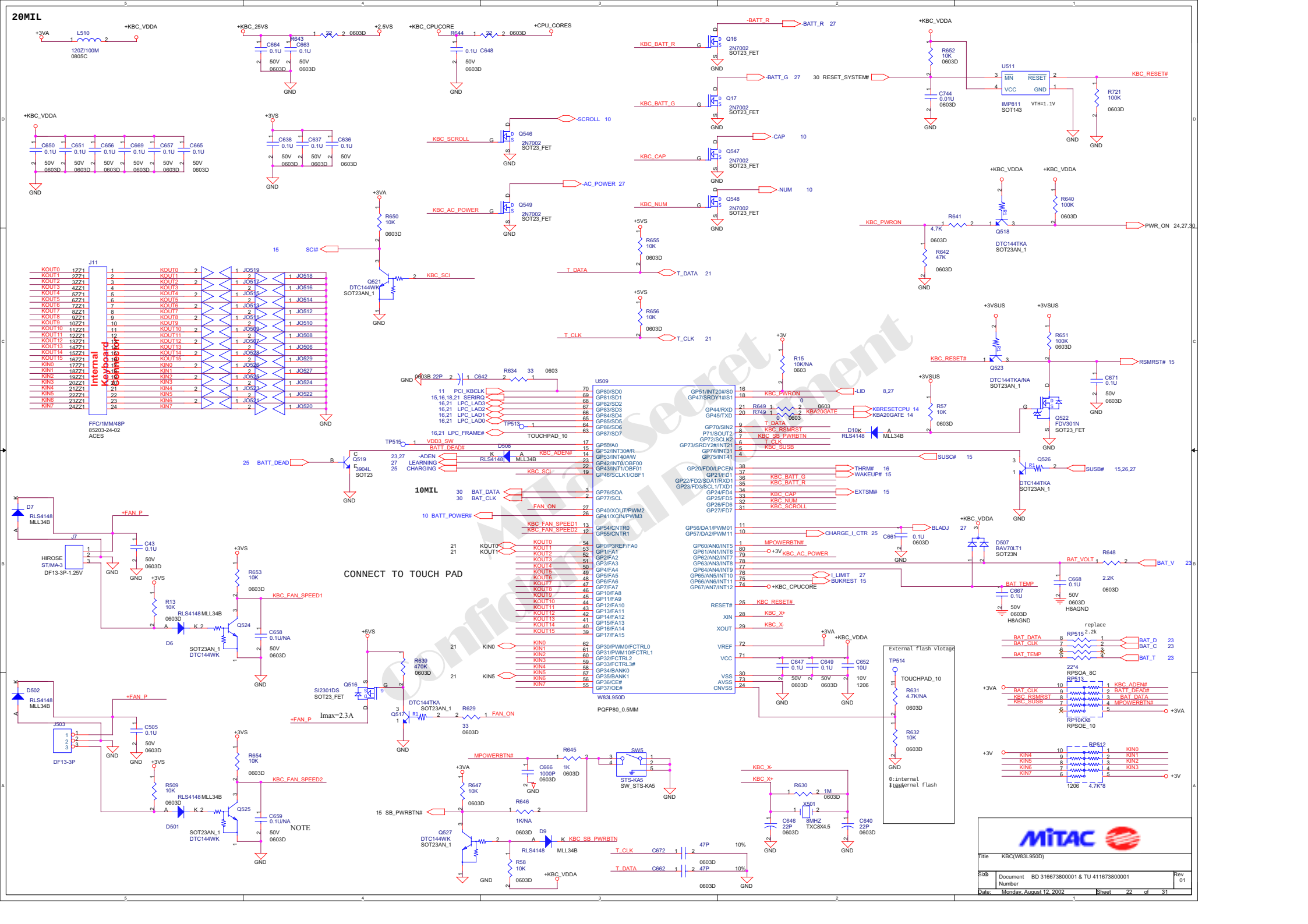

ASIC VT6103 PHY/IEEE802.3 SSOP 48PIN VIA
RJ45
RJ11
Layout Note:
二組各自平行走線等長
二組中間須絕緣, EX: GND SHIELDING
S/W/W/S=12/6/6/12 mils
as short as possible
CLOSE TO TRANSFORMER
CLOSE TO MDC
MDC HARDWARE STRAP
HIGH
LOW
PIN 16
AUDIO CODEC ON MOTHER BD
AUDIO CODEC ON DAUGHTER BOARD
Modem Doughter Board
MDC SCREW HOLE
MiTAC
LAN PHY (ICS1893) & MDC
BD 316673800001 & TU 411673800001
Monday, August 12, 2002
Sheet 19 of 31
Confidential Document

AUDIO CODE & AMPLIFIER

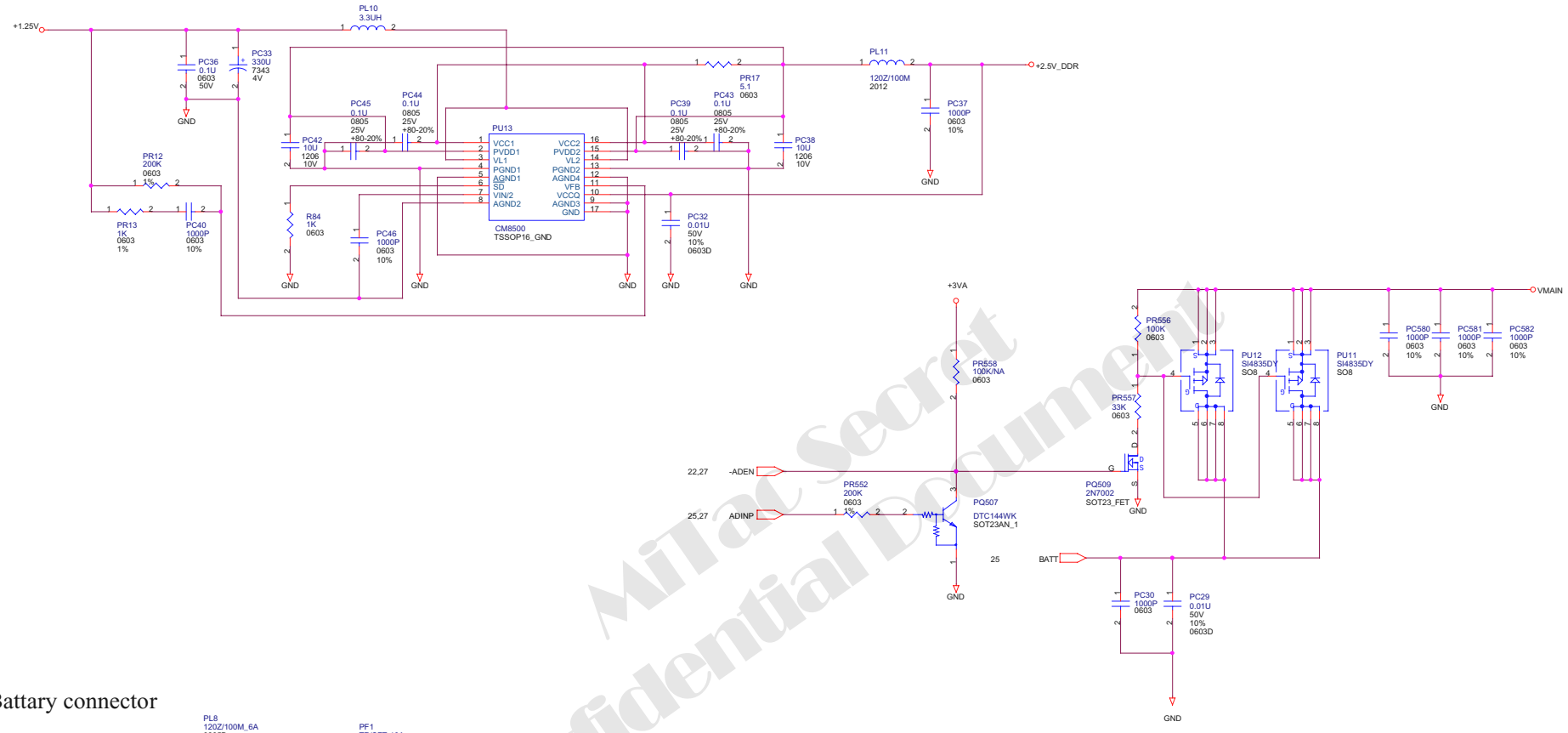


MiTac Secret Confidential Document

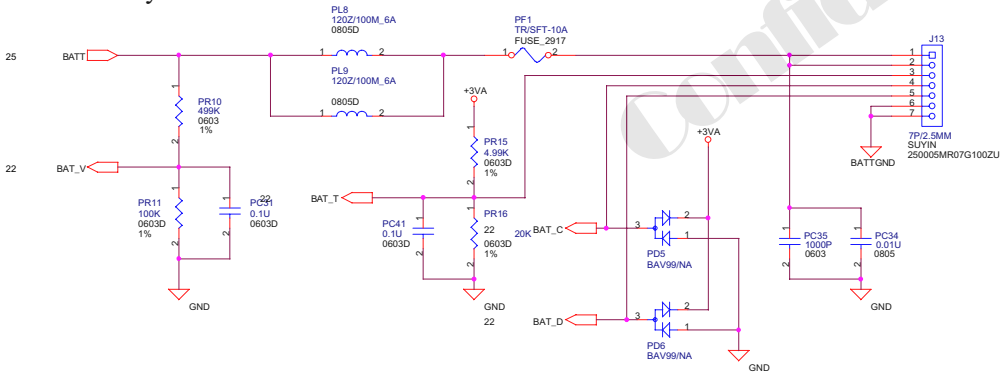

TOUCH_PAD
8575 T/P BRD
VT1211
Flash ROM
Close to EEPROM
MiTAC
SUPER I/O, T/P & BUTTON
Monday, August 12, 2002
MiTac Secret Confidential Document


20MIL
10MIL
CONNECT TO TOUCH PAD
Internal Keyboard Connector
J11
FFC/1MM/48P
85203-24-02
ACES
U509
W83L950D
PQFP80_0.5MM
Imax=2.3A
NOTE
External flash vlotage
0:internal flash
1:external flash
MiTAC
Title KBC(W83L950D)
Size B
Document Number BD 316673800001 & TU 411673800001
Rev 01
Date: Monday, August 12, 2002
Sheet 22 of 31
Mitac Secret confidential Document

1.25V CM8500 & BATTERY CONNECTOR



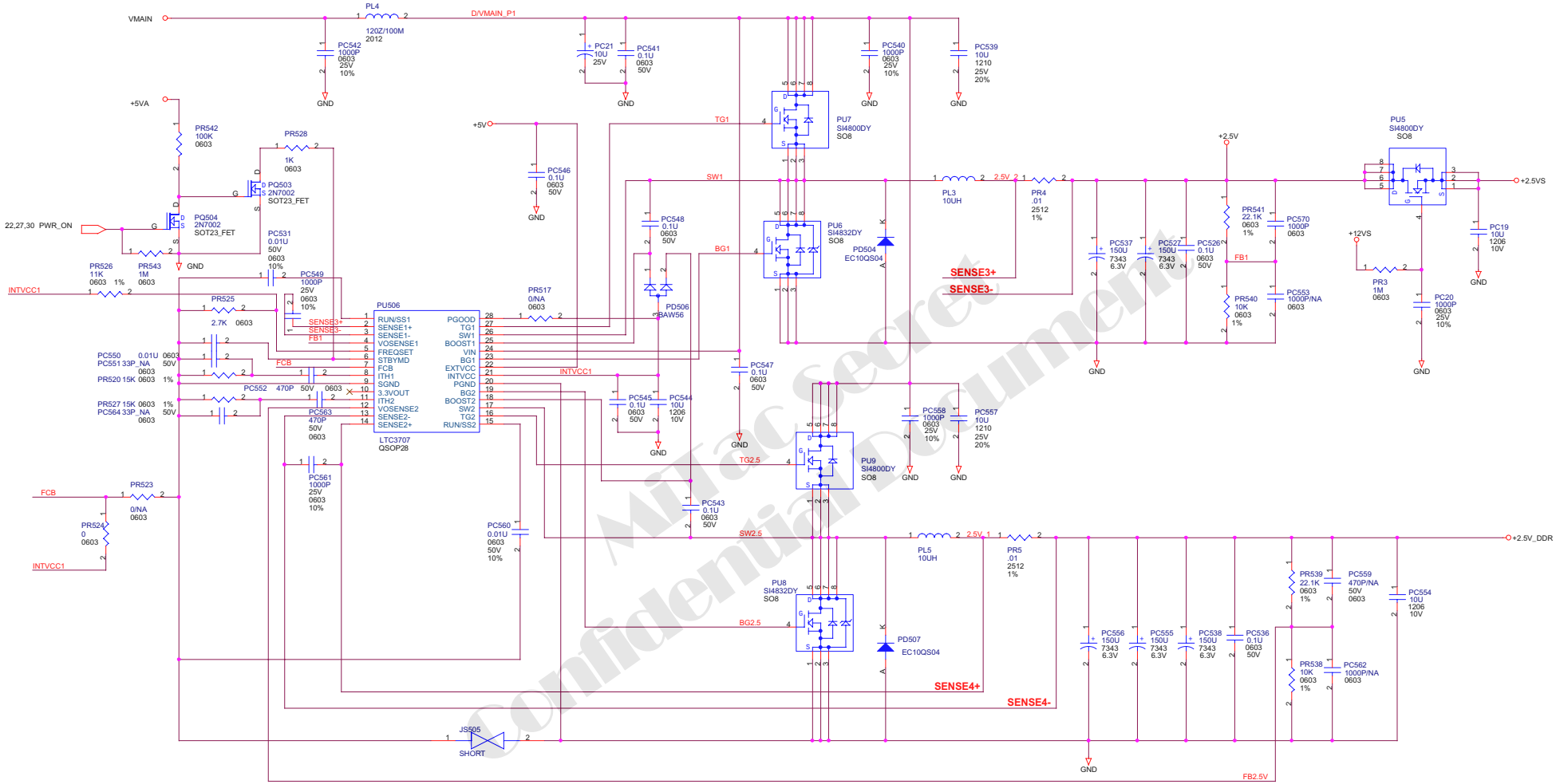
Battary connector



MiTac Secret Confidential Document

MiTAC

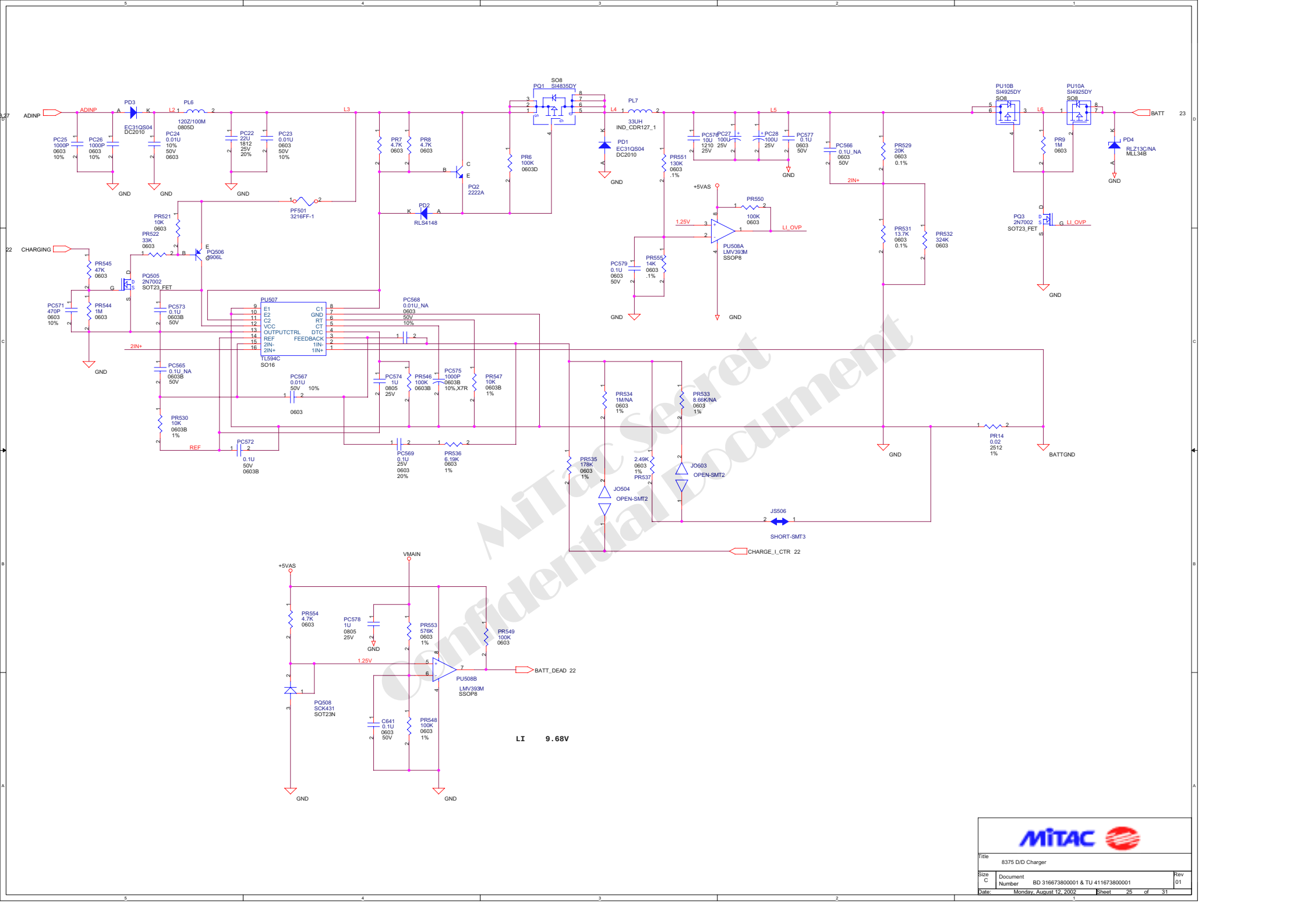
Title	8375 D/D(1.25V CM8500) & BAT CON		
Size C	Document Number	BD 316673800001 & TU 411673800001	Rev 01
Date: Monday, August 12, 2002	Sheet 23 of 31		



MiTac Secret
Confidential Document

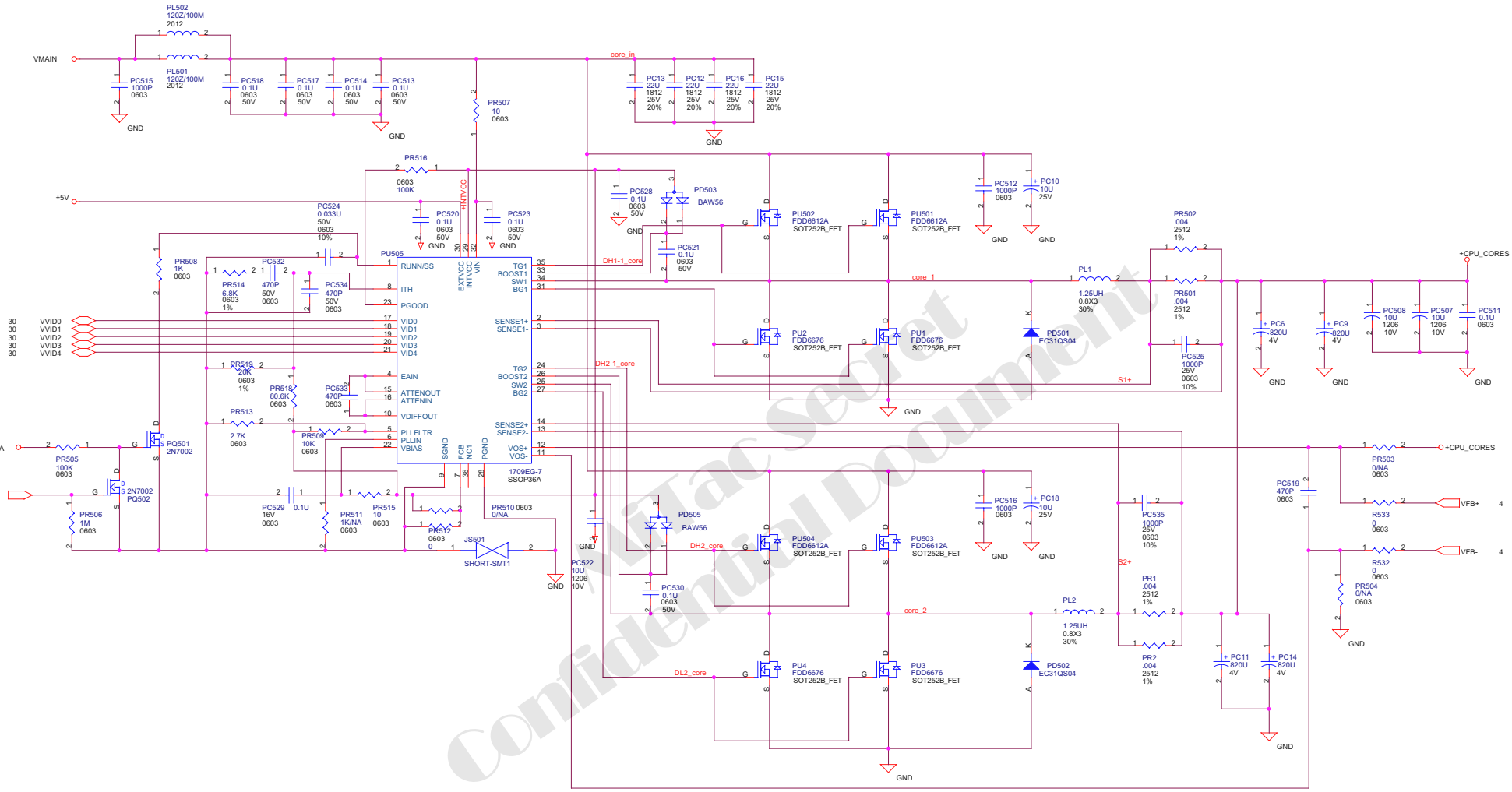
MiTAC

Title	8375 D/D (2.5V LTC3707)	
Size C	Document Number BD 316673800001 & TU 411673800001	Rev 01
Date: Monday, August 12, 2002	Sheet 24 of 31	



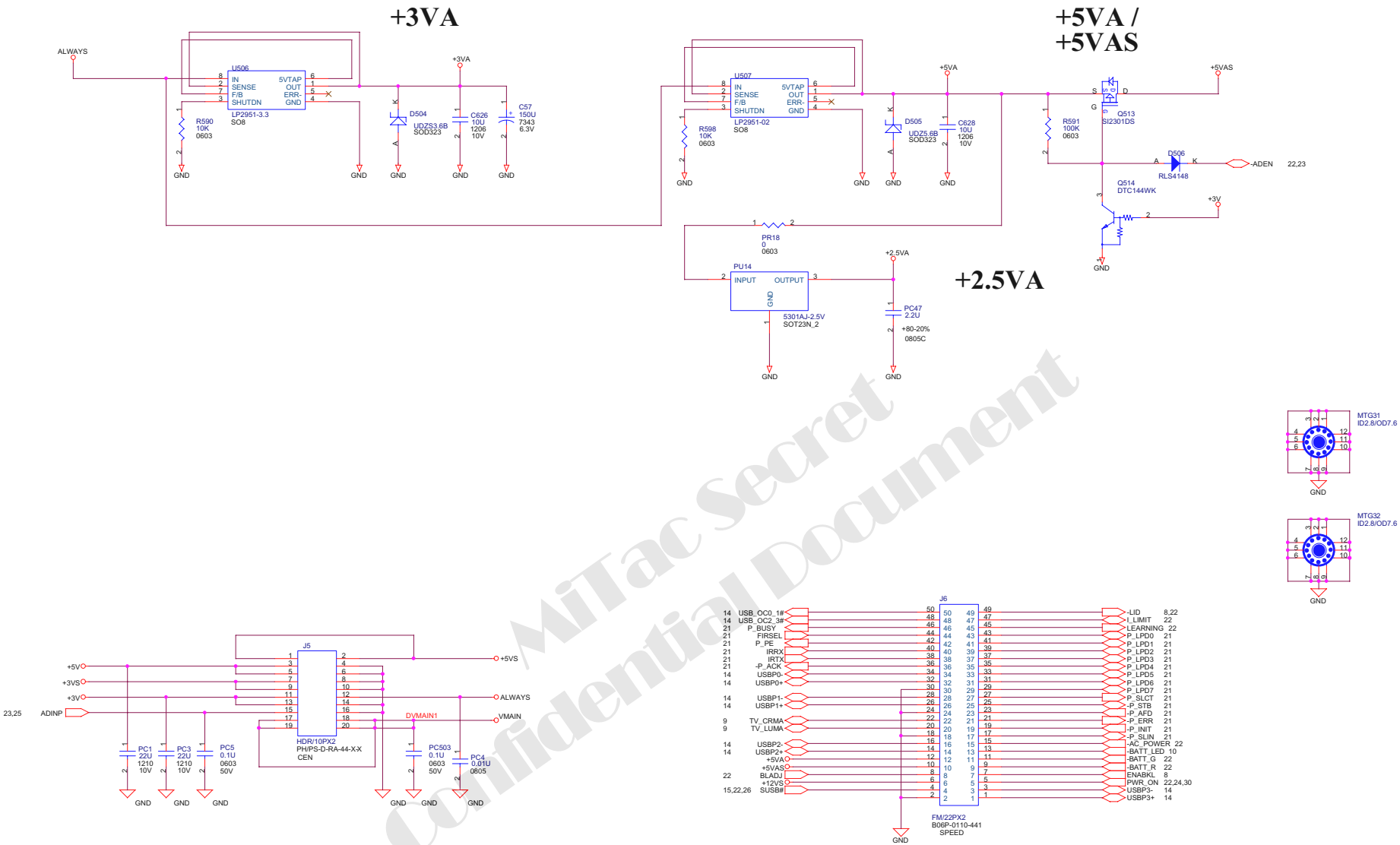
MiTac Secret Confidential Document

Title	8375 D/D Charger	
Size C	Document Number BD 316673800001 & TU 411673800001	Rev 01
Date: Monday, August 12, 2002	Sheet 25 of 31	



MiTac Secret Confidential Document

Title	8375 CPU_CORE		
Size C	Document Number	BD 316673800001 & TU 411673800001	Rev 01
Date:	Monday, August 12, 2002	Sheet 26 of 31	

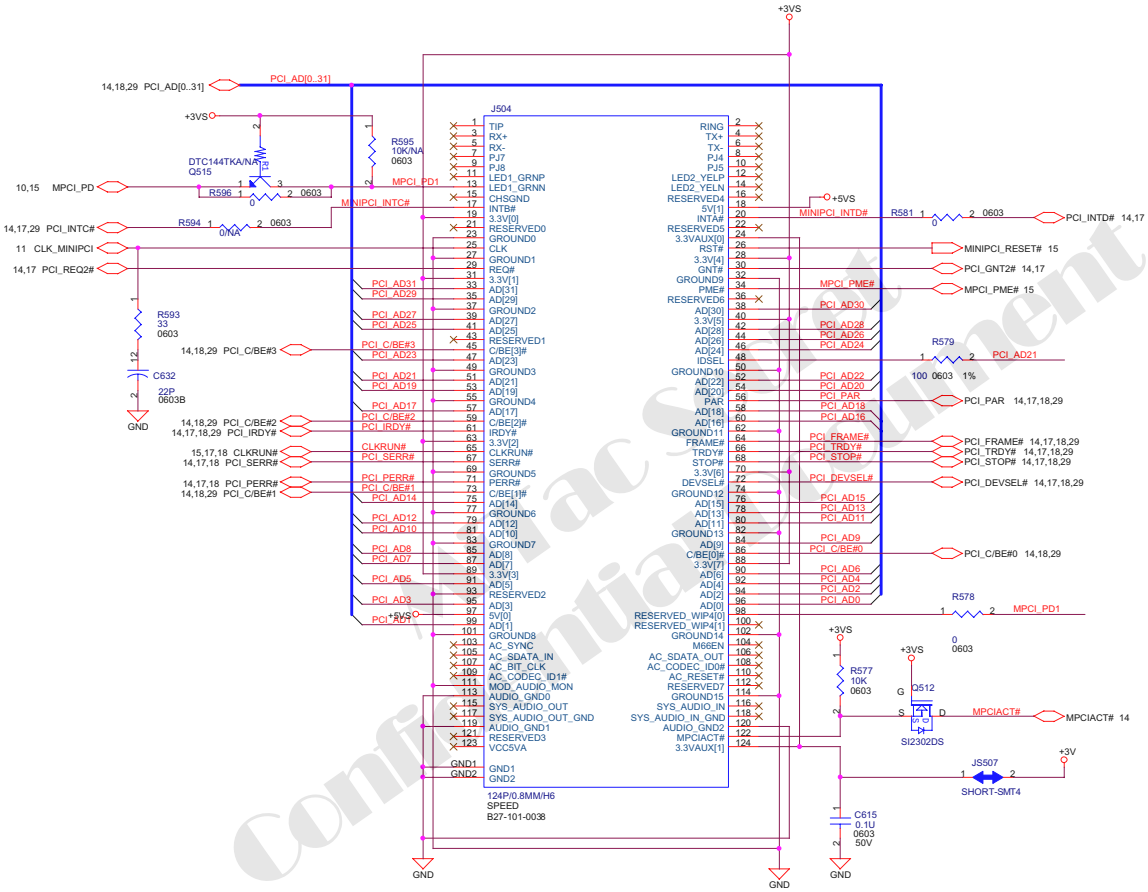


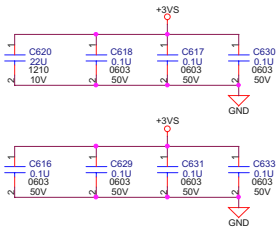
MiTac Secret Confidential Document

Title	8375 D/D CONNECTOR & MISC	
Size C	Document Number BD 316673800001 & TU 411673800001	Rev 01
Date: Monday, August 12, 2002	Sheet 27 of 31	

MINI-PCI

AD21
PCI_INTD#
REQ2#/GNT2#





MiTAC Secret Confidential Document

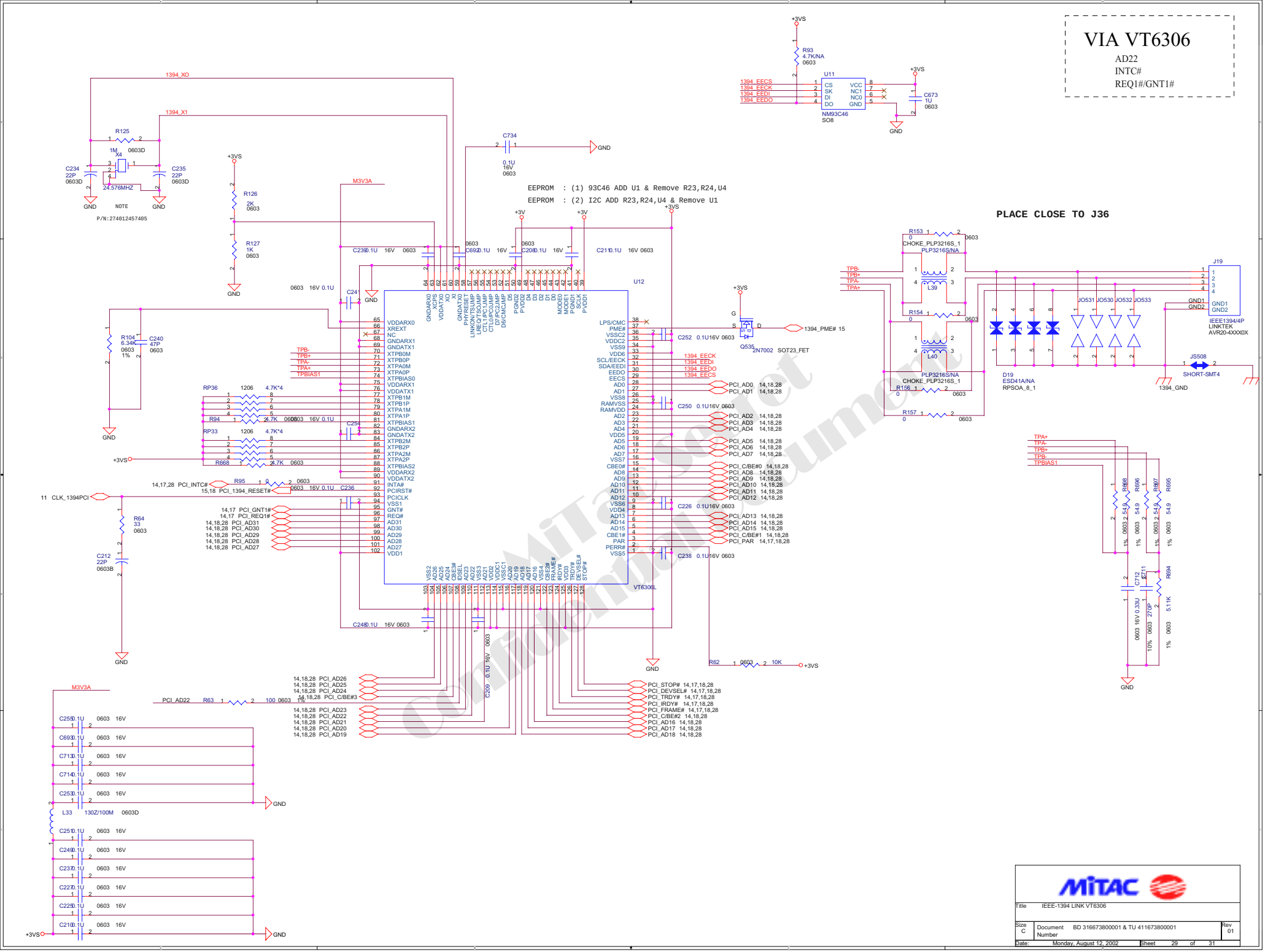
Title	8375 MINIPCI		
Size C	Document Number	BD 316673800001 & TU 411673800001	Rev 01
Date: Monday, August 12, 2002	Sheet 28 of 31		

VIA VT6306

AD22
INTC#
REQ1#/GNT1#

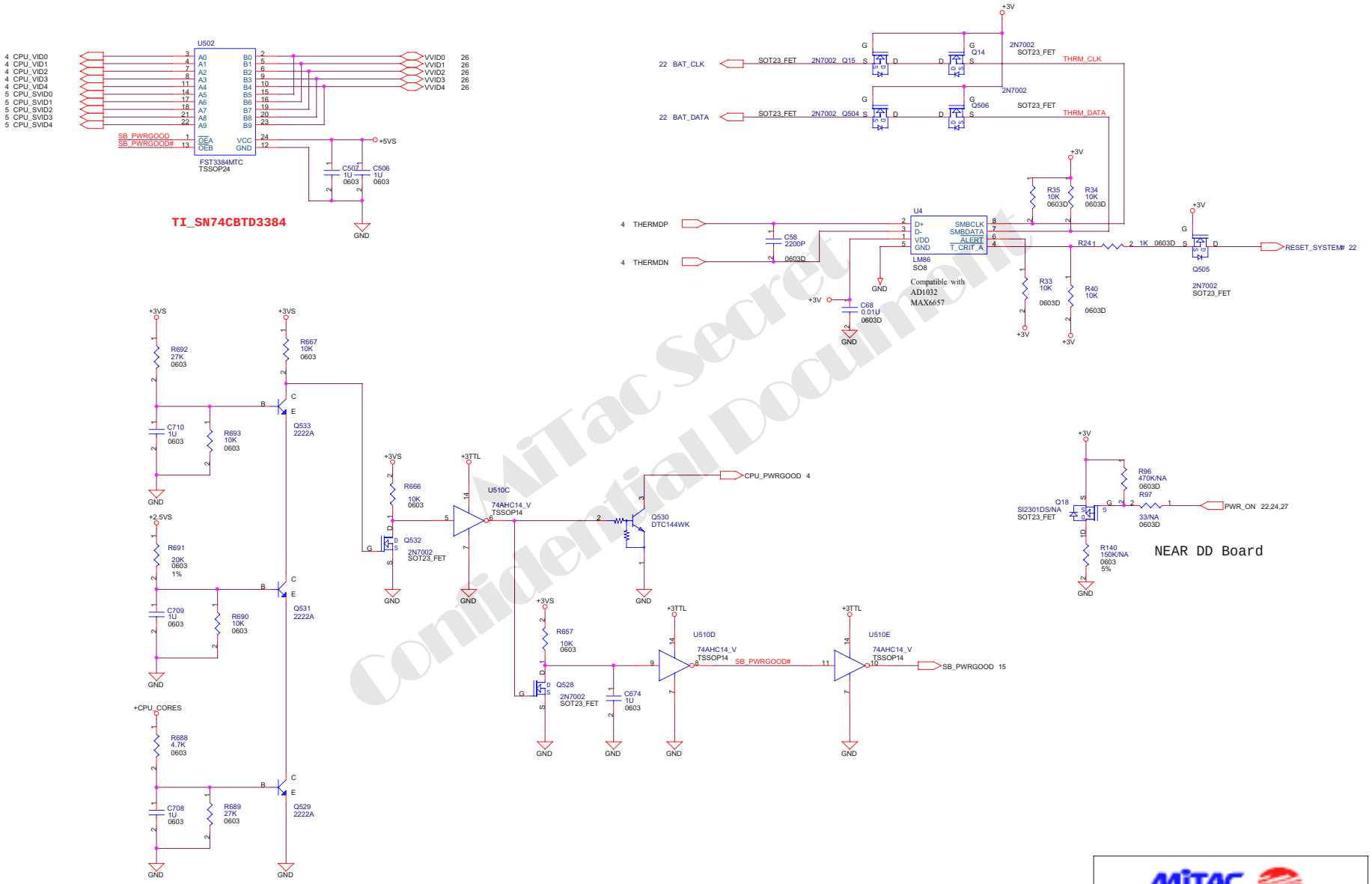
EEPROM : (1) 93C46 ADD U1 & Remove R23,R24,U4
EEPROM : (2) I2C ADD R23,R24,U4 & Remove U1

PLACE CLOSE TO J36



MiTac Secret Confidential Document

MiTAC			
Title	IEEE-1394 LINK VT6306		
Size C	Document Number	BD 316673800001 & TU 411673800001	Rev 01
Date: Monday, August 12, 2002	Sheet 29	of 31	



MiTac Secret Confidential Document

MiTAC

Title	VID OVERRIDE & PWRGD CIRCUIT	
Size C	Document Number BD 316673800001 & TU 411673800001	Rev 01
Date: Monday, August 12, 2002	Sheet 30 of 31	

8375 MB R0B-DVT

R0A	First generation (Base on Scorpio Rev 0B)
5/13	MITAC EMI ENGINEER ADD EMI SOLUTION
5/14	PR61,PR64,PR78,PR79 -> 0.004 Ohm p26
5/15	U22,C406,R287,C416 ->DELETE P20
	5V_AMP Rename to AVDDAD.....P20
	Add CPURST# level shift circuit Q541.....P15
	Modify R6,R7,R8,R9 -> 100 Ohm p4
	Add R671 , R672 10K Ohm p4
	Change ALC201 (U23) library ;Delete C428,C433,C434,C437,C441 ....P20
5/16	GND_CRT15 Rename GNDRGB P10
	ADD R677 R678 +3VSUS for +3VA and +3V Switch Circuit p15 P16 P22
	ADD R673 R674 R675 R676 C743 C744 C745 C746 for CLK_DDR2/2# CLK_DDR5/5# P11 P12
	J3 J4 Pin197 Rename +3VS to +2.5V_DDR , Pin78 pull to GND P12
	Modify U12C Pin D26 pull to +2.5VS ...P16
	R61 R174 2.1K Ohm -> 2k Ohm p8 p16
	Remove L19 L21 .....P9
	Add L79 L80 L81 L82 L83 L84 C747 C748 C749 C750 C751 C752 C753 ...P11
	Add L85 L86 R679 R681 R682 .... P19
	Add C754 C755 ...P14
5/17	Remove +3VCLK power & Cap page11
5/18	Modified Signal PDD6 then PDD7 connect to R214.... P17
	Modified RP60 RP61 RP63 RP64 R205 R206 R207 R208 R209 R210 R212 R215 R216 R217 R218 R219 value ->33 ohm ...p17
	Del NET +3V_U18 +5V_U19 ..... P18
	Rename KB/T_CLK KB/T_DATA to T_CLK T_DATA p22
	Rename MINI-PCI AD[0..31] to PCI_AD[0..31] P28
	Modified J26 Library p22
	Add TestPad TP43 for U1A Pin AA1 ....P4

	R0B-EVT
5/21	RP37 pin 5 , 6 NET SWAP P16
	DEL NET PCOMPP P16
	Add C763 C769 C771 .....P6

	R0B-DVT
6/11	Del R543
	Q529 Q531 Q533 chang parts
	R721 NA
	Modified signals DDR_CLK0/# DDR_CLK3/#
	Modified signals CRT_GREEN CRT_BLUE
	U7 pin F10 F15 connect to +2.5VS
	DEL R535
6/17	DEL PC2 PC17 PC501 PC502
	PC505 PC509 PC510 NA
6/18	ADD EC503 EC504 EC505
7/05	Add Capacitor for EMI solution
	PR10 324K -> 499K
7/15	
	ADD X502 R755 C553 C770
	SPD1 SPDCLK1 pull 2K to +3VS
	Q507 Q508 change parts from MOS to BJT
	C263 20P ->15P R686 51K -> 20K

	R01
8/12	U511Change to IMP811 from MAX809
	Modified RTC circuit: ADD U514 C782 C783 D514
	Modified thermal sensor power plane:+3VS->+3V
	ADD discharge circuit for +3V

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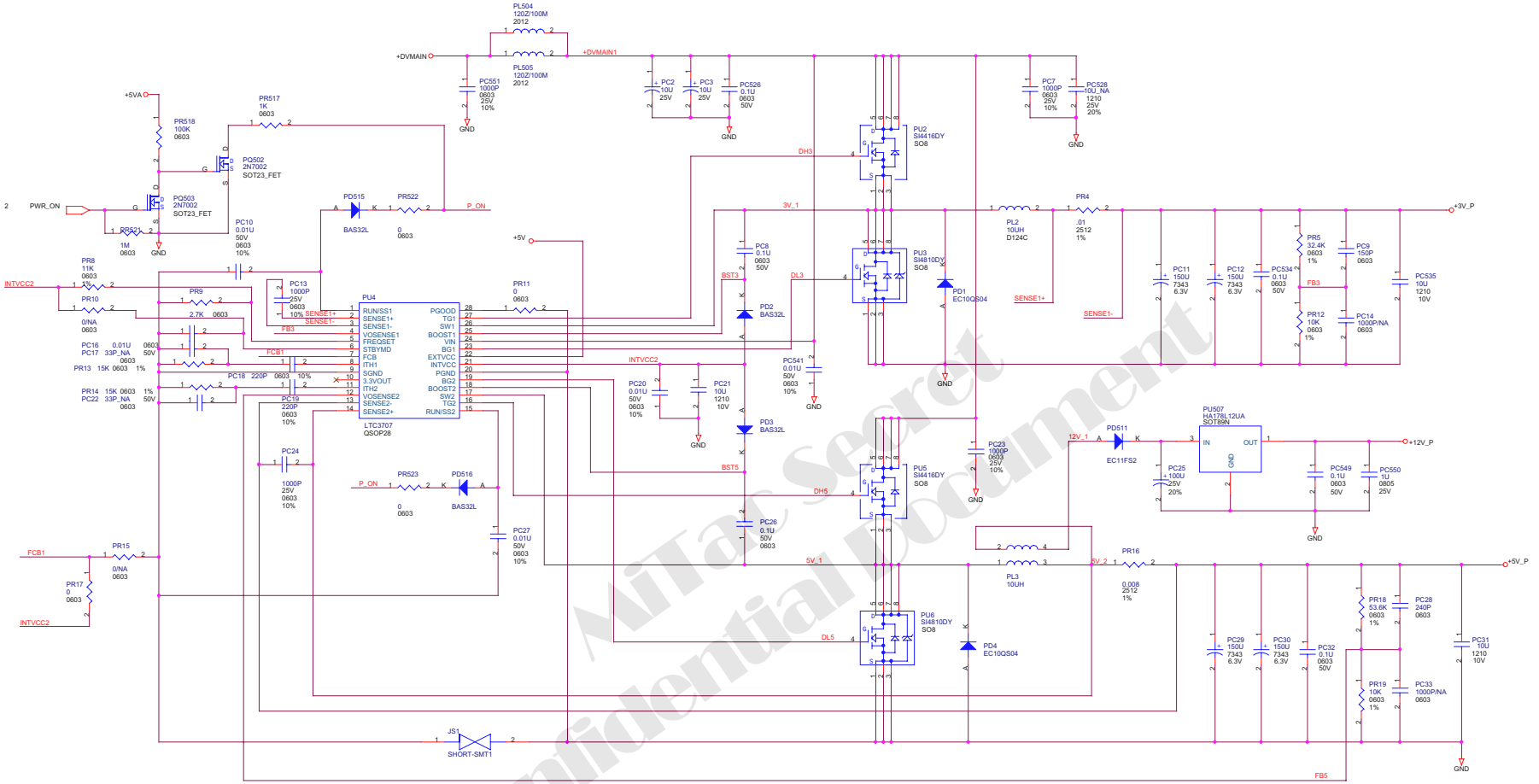
Title	M/B Revision	
Size C	Document Number BD 316673800001 & TU 411673800001	Rev 01
Date: Monday, August 12, 2002	Sheet 31 of 31	

8375 DD BOARD R01

SYSTEM POWER (+3V +5V +12V)



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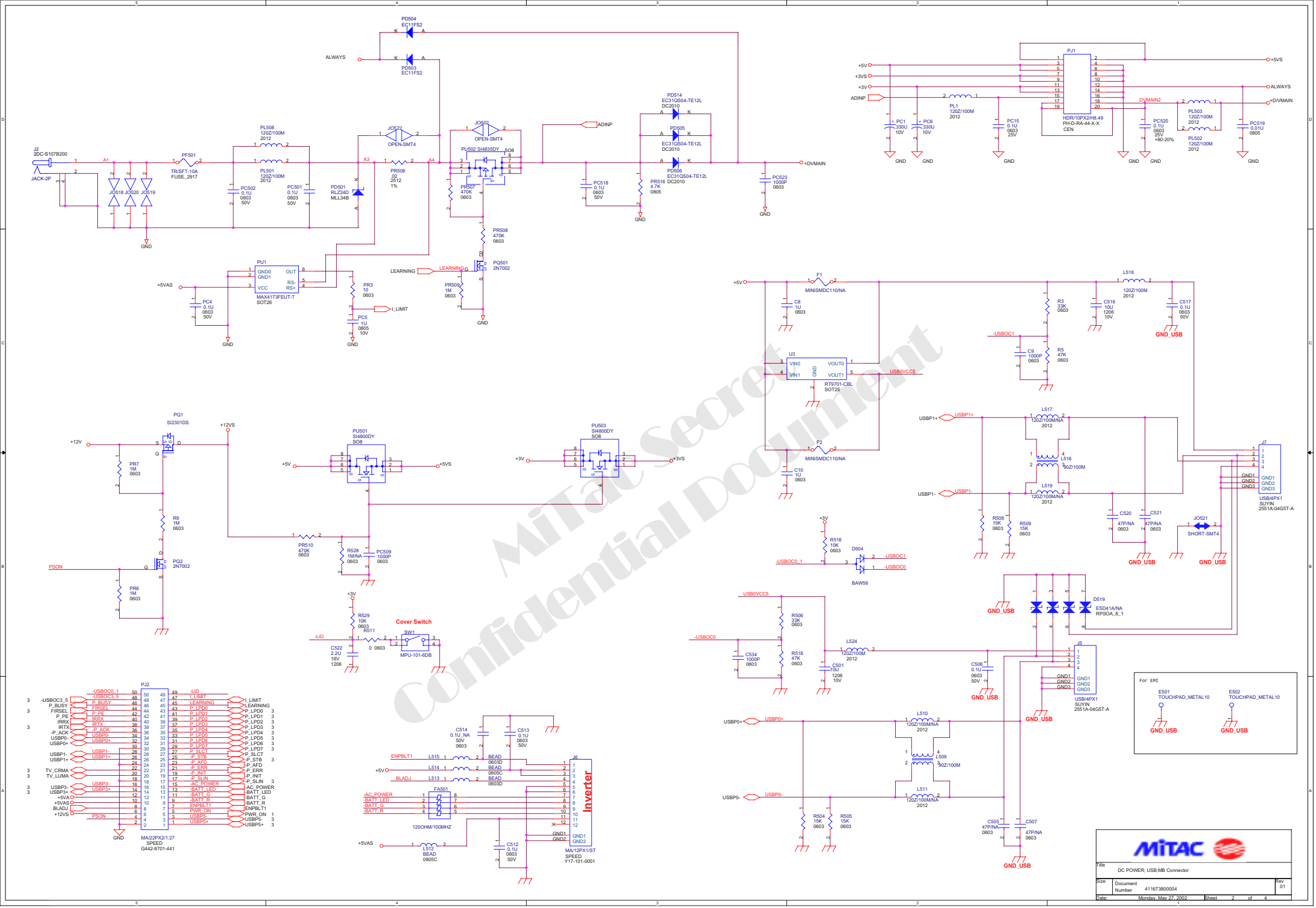
Title	SYSTEM POWER
Size	Document Number 411673800004
Rev	01
Date	Monday, May 27, 2002
Sheet	1 of 4



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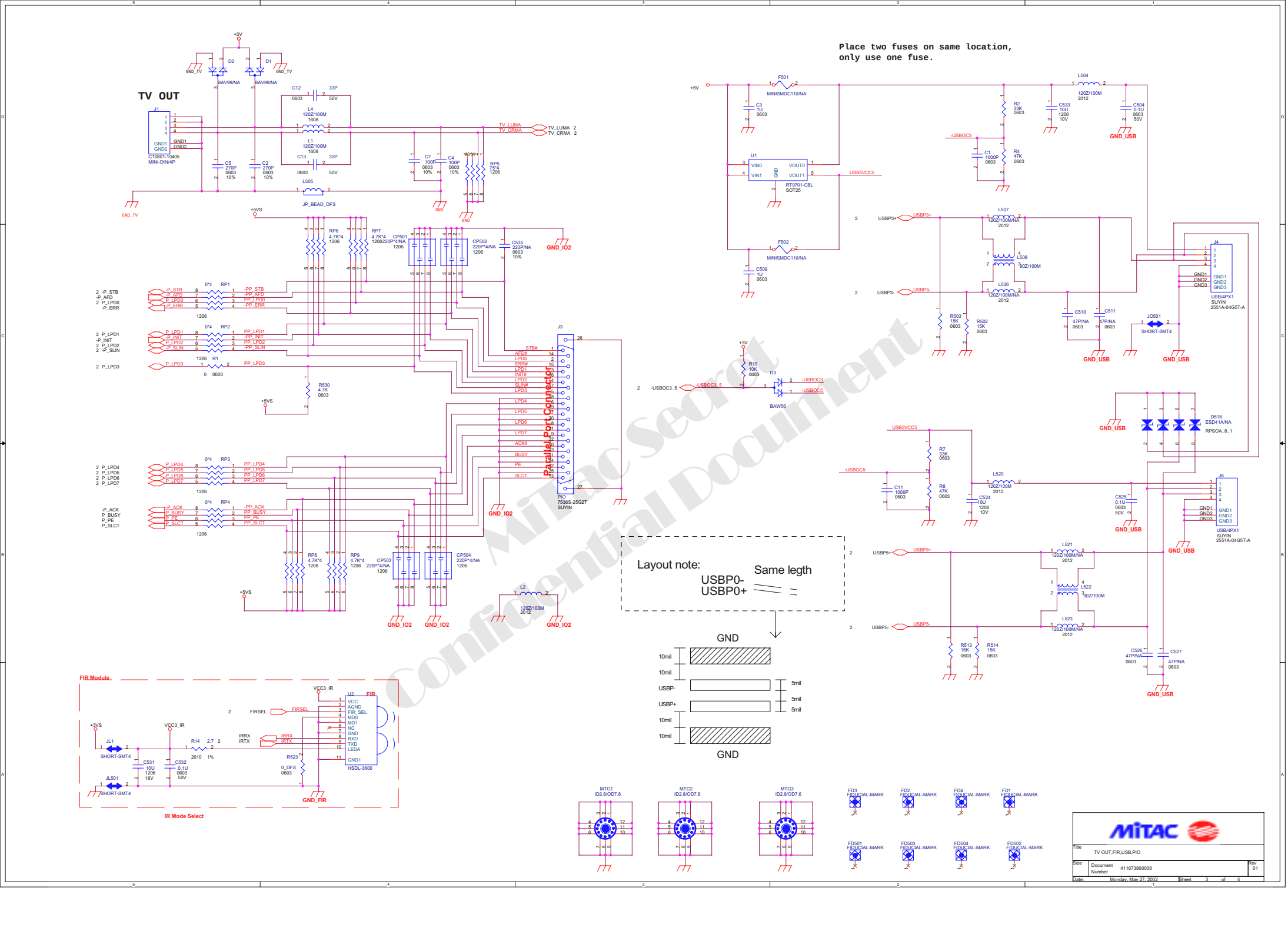
TV OUT
Place two fuses on same location,
only use one fuse.
Parallel Port Connector
Layout note:
USBP0-
USBP0+
Same legth
GND
10mil
USBP-
USBP+
5mil
FIR Module
IR Mode Select
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TV OUT,FIR,USB,PIO
411673800006
Monday, May 27, 2002

8375 D/D R01

R0B	**First generation**
6/17	Add R529 10K
	R0C
8/1	ADD Array capacitor(CP501 CP502 CP503 CP504) x 4 capacitor(C535) x 1 PC10 .02UF -> .033UF DEL U501 U502 Change signal -LID power plane from +3VS to +3V Change common choke value(L508 L509 L518 L522) from 120ohm/100M to 90ohm/100M and footprint Increasing ground area of parallel port
	R01
8/27	PC10 .033UF -> .01UF ADD array resister(RP6 RP7 RP8 RP9) x 4 resister(R530) x 1

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Title: 8375 D/D Revision

Size | Document Number: 411673800004 | Rev: 01

Date: Monday, May 27, 2002 | Sheet 4 of 4

Reference Material

- **AMD Athlon™ XP Processor Model 8** ..... ***AMD. INC***
- **VIA VT8372 North Bridge** ..... ***VIA. INC***
- **VIA VT8235 South Bridge** ..... ***VIA. INC***
- **Engineer Hardware Specification** ..... ***Technology.Corp/MiTAC***

SERVICE MANUAL FOR 8375

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