SERVICE MANUAL FOR

8350

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MiTAC

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1. Hardware Engineering Specification

1.1 Introduction

1.1.1 General Description

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The 8350 motherboard implements 35W(25W) Mobile AMD Athlon™ 64 processor with 512KB L2 cache/ Mobile AMD Sempron™ processor with 128KB L2 cache with uPGA Package. The processor provides a high-performance HyperTransport™ link to I/O, as well as a single 64-bit high performance DDR SDRAM memory controller.

8350 platform implements ATI RS480M / ULI M1573M core logic. The RS480M is a sixth generation Integrated Graphics Processor (IGP) that integrates 2D/3D graphics and a system controller in a single chip. It is designed to support the Mobile Athlon™ 64 / Mobile Sempron™ systems in both the performance and value sectors. It is also the first IGP in the world to fully support DirectX 9.0 in hardware for the Mobile Athlon™ 64 / Mobile Sempron™ platform.

The RS480M integrates an ATI RADEON 9600-based 2D/3D graphics engine, dual display, a TV encoder, an LVDS interface and north bridge functionality in a single BGA package. This high level of integration and scalability enables manufacturers to offer enthusiast level capabilities and performance while minimizing board space and system cost.

The M1573M integrates a High Definition (HD) Audio/AC'97 Host Controller, 2-channel dedicated Ultra-66/100/133 IDE Master controller, USB 2.0/1.1 Host controllers, IO APIC controller, as well as 1/10/100 Mb/s Fast Ethernet MAC layer and PCI Express interface. Additional features include Host Signal Processing (HSP) software modem

solution, ACPI support, green function, and Real Time Clock.

Featuring PCI Express, the newest high-performance and low-cost I/O interconnect architecture, the M1573M is the highest integration south bridge solution between PCI-Express Link bus, PCI bus.

User expendable peripheral interface built on 8350 system are 3 USB ports. Based on TI PCI4511 CardBus / IEEE1394 combo controller, 8350 system provides a PCMCIA / CardBus, and a 4-pin IEEE1394a interface. User interface includes internal keyboard, touch pad. Realtek ALC655 AC'97 Codec based multimedia interface includes Microphone-in and SPDIF / headphone-out audio jacks. There are two stereo internal speakers and one woofer on board as well. The communication interface are Billinton MDC56S-I MDC modem and VIA VT6301L Ethernet PHY to support standard RJ-11 phone jack and RJ-45 Ethernet jack.

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1.2 System Hardware Part(1)

8350 External Specifications	
CPU	Mobile AMD Turion (35W& 25W),Athlon 64 (35W) & Sempron (25W)
Chip Set	ATI RS480M (NB) +**ULi1573M(SB)**
L2 Cache	Turion(1MB), Athlon 64(512KB),Sempron(256KB and 128)
System BIOS	512KB Flash EPROM - include System BIOS, VGA BIOS
MEMORY	200-pin SO-DIMM DDR Memory Slot x2
	Support DDR333/400
	0MB Memory onboard ; Expandable to 2.0GB
Video Controller	Integrated in ATI RS480M
	Reserve for local frame buffer 32MB or 64MB
Optical drive	2.5" Combo / DVD-Dual (12.7mm)
HDD	PATA 2.5" 40GB / 60GB / 80 /100 GB HDD(9.5mm) 4200rpm or 5400rpm
DISPLAY	15.4" Wide WXGA TFT
	-Resolution: 1280x800
	- 1 CCFT Typical 185cd/m2
KEYBOARD	19mm key pitch / 3mm stroke
POINTING DEVICE	Intelligence Glide pad without scroll button, 2 touch pad buttons
INDICATOR	5 LEDs for HDD/ODD Access , Num lock, Cap lock,AC/Battery Power/Charger
PC CARD SLOT	TypeII x 1
	-PCMCIA Standard Rev.2.1 , CardBus support , w/o ZV port

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1.2 System Hardware Part(2)

8350 External Specifications	
AUDIO SYSTEM	Built-in Sound system, AC97
	- Built-in 2W Sub- Woofer
	- Built-in stereo speaker 1W x2 , Built-in microphone
	- Sound Volume control by Hot-Key (Fn + F3 : Volume down, Fn + F4 : Volume up)
I/O PORT	USB(2.0) x 3
	Mic-in(mono) x 1
	Audio out for SPDIF
	TV-out (PAL/NTSC) x 1 (7pins)
	RJ-45 LAN Jack x 1, RJ-11Modem Jack x 1
	Mini-PCI connetor (for WirelessLAN Card)
	VGA port x 1, DC-in x 1
COMMUNICATION	56Kbps(V.90) Fax Modem(MDC) and 10/100Base-TX LAN
	Wireless LAN (IEEE802.11b+g)
Battery	-Li-ion Battery 2200mAh(6-cell) - Battery Life: 130min
	-Power off charge to 90% full take 150 min, support power-on charge
POWER SUPPLY	65W Universal AC Adapter(100-240V)
SAFETY LOCK	Security Lock hole (Kensington)
DIMENSION	W353.8 x D250 x H29.58~33mm
WEIGHT	(P)2.8kg

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1.2.1 CPU

- **AMD64 Technology**
  - AMD64 technology instruction set extensions
  - 64-bit integer registers, 48-bit virtual addresses, 40-bit physical addresses
  - Eight new 64-bit integer registers (16 total)
  - Eight new 128-bit SSE/SSE2/SSE3 registers (16 total)
- **Compatible with Existing 32-Bit Code Base**
  - Including support for SSE, SSE2, SSE3, MMX™, 3DNow!™ technology and legacy x86 Instructions
  - Runs existing operating systems and drivers
  - Local APIC on-chip
- **HyperTransport Technology to I/O Devices**
  - One 16-bit link supporting speeds up to 800 MHz (1600 MT/s) or 3.2 Gigabytes/s in each direction
- **Integrated Memory Controller**
  - Low-latency, high-bandwidth

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- 72-bit DDR SDRAM at 100, 133, 166, and 200 MHz
- Supports up to two unbuffered SO-DIMMs

❖ **Packaging**

- 754 pin lidless micro-PGA processor package

1.2.2 Core Logic

1.2.2.1 ATI RS480M North Bridge

❖ **CPU Interface**

- Supports the mobile AMD Athlon™ 64 and Sempron™ processors
- Supports 200, 400, 800, and 1000MHz HyperTransport (HT) interface speeds
- Supports dynamic link width and frequency change
- Supports LDTSTP interface, CPU throttling, and stutter mode

❖ **Memory Interface**

- Support for 2Mx32 (with 64-bit interface only), 4Mx32, 8Mx32, and 16Mx16 memory devices

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- Supports GDDR SDRAM self refresh mechanism

❖ **A-Link Express Interface**

- 1 x 2 (expandable to x4) A-Link Express interface (PCI Express 1.0a compliant) for connection to the Uli M1573M

❖ **2D/3D Acceleration Features**

- Highly-optimized 128-bit engine, capable of processing multiple pixels per clock
- 2D Supports a maximum resolution of 2048x1536 @ 32bpp
- 3D Supports a maximum resolution of 2536x2536 @ 32bpp
- Full DirectX 9.0 support (Vertex Shader version 2.0 and Pixel Shader version 2.0)

❖ **Multiple Display interface**

- An integrated TV encoder with an on-chip DAC
- Integrated dual 24-bit LVDS interface, 595 Mbps/channel with 85 MHz pixel clock rate
- Primary display path supports VGA and accelerated modes, video overlay, hardware cursor, hardware icon and palette gamma correction. It supports full radiometric expansion ability for source modes up to 1280x1024
- Dual independent displays: LCD/CRT, LCD/TV

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- With the proper BIOS implementation, supports different TV standards including NTSC,
- NTSC-J, PAL-M, PAL-CN, PAL-B, PAL-G, PAL-D, PAL-H, PAL-I, PAL-K, and PAL-N

1.2.2.2 ULI M1573M South Bridge

- ❖ Supports A-Link PCI Express Interface technology
- ❖ Concurrent PCI BUS controller
- ❖ Integrates the HD Audio Controller with AC97 Interface
- ❖ Integrates the Ethernet MAC Controller W/ standard MII interface
- ❖ Integrates Universal Serial Bus 2.0/1.1 Host Controllers
- ❖ Integrates the Ultra DMA133/100 EIDE Master/Slave controllers
- ❖ Integrates the PCI to LPC bridge
- ❖ Integrates I/O Advanced Programmable Interrupt Controller
- ❖ Integrates legacy system I/O and legacy power management functionalities
- ❖ PC2001 compatible mobile power management

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1.2.3 Memory

- Support unbuffer DDR 333/400MHz SO-DIMM expandable to 1024MB (2 DDR-SODIMM slots)

Slot1	Slot2	Total
128MB	0	128MB
128MB	128MB	256MB
128MB	256MB	384MB
128MB	512MB	640MB
256MB	0	256MB
256MB	256MB	512MB
256MB	512MB	768MB
512MB	0	512MB
512MB	512MB	1024MB

Table 1: Memory Expansion Capacity

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1.2.4 I/O Ports

- CRT Port
  - Standard VGA compatible port

- DDC1 and DDC2B compliant

Pin	Signal	Description
1	CRT_RED	Red analog video output
2	CRT_GREEN	Green analog video output
3	CRT_BLUE	Blue analog video output
4	Monitor Sense	NC
5	GND	Monitor Sense
6	GND	Ground
7	GND	Ground
8	GND	Ground
9	VCC	+5VDC
10	GND	Ground
11	Monitor Sense	NC
12	CRT_DDDA	Data from DDC monitor
13	CRT_HSYNC	Horizontal Sync control
14	CRT_VSYNC	Vertical Sync control
15	CRT_DDCK	Clock to DDC monitor

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Table 2: CRT Connector

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❖ 7Pins S-VIDEO port for TV-Out

- Support up 1024*768 resolution
- Support PAL and NTSC system

Pin	Signal name	Direction
1	GND	-
2		-
3	GND	O
4	TV_COMP	O
5		
6	TV_LUMA	O
5	TV_CRMA	O

Table 3: S-Video Port

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System	Input(Active) Resolution	Active TV lines	Over/Under scan
NTSC	320x200	480 ~ 400	+
NTSC	640x480	480 ~ 400	+
NTSC	720x480	480 ~ 400	+
NTSC	720x400	480 ~ 400	+
NTSC	800x600	480 ~ 420	+
NTSC	1024x768	480	Over
System	Input(Active) Resolution	Active TV lines	Over/Under scan
PAL	320x200	540 ~ 500	+
PAL	640x480	540 ~ 500	+
PAL	720x400	540 ~ 500	+
PAL	720x576	576 ~ 510	+
PAL	800x600	600 ~ 510	+
PAL	1024x768	520	Under

Table 4: TV Out Support Modes

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❖ RJ-11

- Connection to Modem Daughter Board Connector or Mini-PCI Modem Card
- Support 56Kbps/V.92

Pin	Signal Name	Direction	Description
1	NC	-	No Connect
2	TIP	I/O	Phone Line Positive
3	RING-	I/O	Phone Line Negative
4	NC	-	No Connect

Table 5: Modem Port

❖ RJ-45

- The Fast Ethernet MAC Controller features an IEEE802.3 and IEEE802.3x compliant MAC with external LAN physical layer chip (VT6103) supporting full duplex 10 Base-T,100 Base-T Ethernet

- Support Wake-up On-LAN function in System enter to S3

Pin	Signal Name	Direction	Description
1	PJTX+	Out	Transmit Data Ring
2	PJTX-	Out	Transmit Data Tip
3	PJRX+	IN	Receive Data Ring
4	RJ45_PJ4	-	Internal termination resistor
5	RJ45_PJ4	-	Internal termination resistor
6	PJRX-	IN	Receive Data Tip.
7	RJ45_PJ7	-	Internal termination resistor
8	RJ45_PJ7	-	Internal termination resistor

Table 6: LAN Port

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❖ USB Ports

- Three industry standard USB 2.0 ports (Backward compatible to USB 1.1)

- Support maximum transfer rate up to 480Mbits/s

Pin	Signal Name	Direction	Description
1	VCC	Power	USB Device Power (+5VDC)
2	DATA-	I/O	Balanced Data Negative
3	DATA+	I/O	Balanced Data Positive
4	GND	Power	Ground

Table 7: USB Port

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1.2.5 PC Card Slot

- One Type II/I slot supporting the 1997 PC Card standard and including full R2 (16-bit) and 32-bit Cardbus data transfer
- Ti PCI4510 (PCMCIA Controller) & Ti TPS2211A (Power Switch)
- Mixed-and-match 5V/3.3V 16 bits PC CARDs and 3.3V Cardbus Card

1.2.6 Graphical Subsystem

- Integrated graphics with 2D/3D/Video Controllers
- Support up to 128 MB frame buffer size

1.2.7 Display

- 15”XGA TFT Display; Resolution: 1024x768
- Dual View of LCD+CRT / LCD+TV independent display
- External Video refresh rate of up to 100Hz supported
  - Vertical refresh frequencies to meet VESA requirements
  - Simultaneous video in specified video modes – switchable with hot key

1.2.8 IDE Interface

- Support Dual Independent IDE Channels, One is Hard-Disk. The other one is Optical Device
- Supports PIO mode 0,1,2,3,4,5 and Ultra DMA 33/66/100/133

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1.2.9 Read Only Memory(BIOS Flash)

- Fully compatible with industry standard software including Windows XP home & professional edition
- Fully supports APM V1.2 and latest ACPI specification
- 512Kx8 (4Mbit) Flash BIOS
- Insyde BIOS core

1.2.10 Power Management Features

- Local standby mode (Individual devices such as HDD, graphics controller, LCD etc..)
- CPU Idle mode (Including ACPI modes C1,C2 and C3)
- Suspend mode (Including S1 and S3 ACPI modes)
- Fully APM V1.2 compliant
- Fully ACPI V1.1 compliant
- Hibernate for Windows XP

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- Thermal management
- Fully US EPA Energy Start compliant

1.2.11 Keyboard Controller

- Winbond W83L950D

1.2.12 LEDS Indicator

- CDROM /HDD & NUM & CAP & SCROLL & Wireless & 2 LEDs for Power/Battery status Indicator

1.2.13 Touch-Pad Module

- Synaptics TM61PUZG385

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1.2.14 Modem(MDC)

Pin	Signal name	Pin	Signal name
1	TP	2	NC
3	GND	4	MODEM_SPK
5	NC	6	NC
7	NC	8	GND
9	NC	10	+5V
11	NC	12	NC
13	NC	14	NC
15	GND	16	Pull Up to +3V
17	+3V	18	+5V
19	GND	20	GND
21	+3V	22	AC97_SYNC
23	AC97_SDOUT	24	AC97_SDIN1
25	AC97_RST#	26	AC97_SDIN1
27	GND	28	GND
29	GND	30	AC97_BITCLK

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Table 8: Modem Daughter Board Connector

1.3 Electrical Characteristic

1.3.1 M1573M GPI/O Pin Define

Pin Name	Pin #	Mux Function	GPIO Function	Power Plane	Signal Name	Operation
GPIO0	Y4		GPI	MAIN	MB_ID0	PULL_DOWN
GPIO1	AE3		GPO	MAIN	MB_ID1	PULL_DOWN
GPIO2	AD2		GPI	MAIN	-MPCIACT	PULL_UP(RESERVE)
GPIO3	AA5		GPO	MAIN	LPM_CPU	PULL_UP(RESERVE)
GPI4	C6	PCIREQ#4	GPI	MAIN	-PCIREQ4	PULL_UP
GPI5	B4	PCIREQ#5	GPI	MAIN	-PCIREQ5	PULL_UP
GPI6	B6	PCIREQ#6	GPI	MAIN	-PCIREQ6	PULL_UP
GPI7	D2	PCIIRQ#[E]	GPI	MAIN	-PCIIRQ[E]	PULL_UP
GPI8	E2	PCIIRQ#[F]	GPI	MAIN	-PCIIRQ[F]	PULL_UP
GPI9	E5	PCIIRQ#[G]	GPI	MAIN	-PCIIRQ[G]	PULL_UP
GPI10	E6	PCIIRQ#[H]	GPI	MAIN	-PCIIRQ[H]	PULL_UP
GPI11	W4	VOL_UP	GPI	MAIN	VOL_UP	
GPI12	W5	VOL_DOWN	GPI	MAIN	VOL_DOWN	
GPI13	Y5	VOL_MUTE	GPI	MAIN	VOL_MUTE	
GPI14	AB5	LDRQ#[1]	GPI	MAIN		
GPI15	AA4	A20GATE	GPI	MAIN	A20GATE	
GPI16	AF2	KBCRC#	GPI	MAIN	-RCIN	
GPI17	AC20	VRGATE	GPI	MAIN	ALLOW_STOP	PULL_UP
GPI18	Y2	ACB_BITCLK	GPI	MAIN		
GPI19	AD6	SATA_GPI0	GPI	MAIN		
GPI20	AE4	SATA_GPI1	GPI	MAIN		

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Pin Name	Pin #	Mux Function	GPIO Function	Power Plane	Signal Name	Operation
GPI21	AF4	SATA_GPI2	GPI	MAIN		
GPI22	AE6	SATA_GPI3	GPI	MAIN		
GPO4	C5	PCIGNT#4	GPO	MAIN		PULL_UP
GPO5	B3	PCIGNT#5	GPO	MAIN		PULL_UP
GPO6	B5	PCIGNT#6	GPO	MAIN		PULL_UP
GPO7	AC5	CPUSTP#	GPO	MAIN		
GPO8	AC4	PCISTP#	GPO	MAIN		
GPO9	D3	CLKRUN#	GPO/OD	MAIN		
GPO10	AB20	DSPVRHI	GPO	MAIN		
GPO11	AB19	VRHI#	GPO	MAIN		
GPO12	AF22	A20M#	GPO	MAIN		
GPO13	AC22	CPUHI#	GPO	MAIN		
GPO14	AE22	CPUPWG	GPO	MAIN		
GPO15	AD22	DSLEEP#	GPO	MAIN		
GPO16	AE24	IGNNE#	GPO	MAIN		
GPO17	AC21	INIT#	GPO	MAIN	-MINIPCI_PD	PULL_UP
GPO18	AD24	INTR	GPO	MAIN		
GPO19	AF26	NMI	GPO	MAIN		
GPO20	AD23	SLEEP#	GPO	MAIN		
GPO21	AE23	SMI#	GPO	MAIN		
GPO22	AD21	STPCLK#	GPO	MAIN		
GPO23	Y6	ACB_SYNC	GPO	MAIN		
GPO24	Y3	ACB_SDOUT	GPO	MAIN		
GPO25	AE5	SATA_GPO0	GPO	MAIN		
GPO26	AD5	SATA_GPO1	GPO	MAIN		
GPO27	AF1	SATA_GPO2	GPO	MAIN		
GPO28	AC6	SATA_GPO3	GPO	MAIN		
GPO29	AE26	HTTPWROK	GPO/OD	MAIN		PULL_UP

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Pin Name	Pin #	Mux Function	GPIO Function	Power Plane	Signal Name	Operation
GPO30	AE25	HTTRESET#	GPO/OD	MAIN		PULL_UP
GPO31	AD25	HTTSTOP#	GPO/OD	MAIN		PULL_UP
GPO32	AE21	CPURST#	GPO	MAIN		
RSMGPIO0	K23		GPI	Resume	SPK_OFF	PULL_UP
RSMGPIO1	K24		GPI	Resume	-KBC_US/JP	PULL_UP
RSMGPIO2	J22		GPI	Resume	-EXTSMI	PULL_UP
RSMGPIO3	K22		GPI	Resume	-SCI	PULL_UP(RESERVE)
RSMGPI4	G23	USBOVR#0	GPI	Resume	-USBOVR0	
RSMGPI5	G22	USBOVR#1	GPI	Resume	-USBOVR1	
RSMGPI6	F25	USBOVR#2	GPI	Resume	-USBOVR2	
RSMGPI7	F24	USBOVR#3	GPI	Resume	-USBOVR3	
RSMGPI8	E26	USBOVR#4	GPI	Resume	-USBOVR4	
RSMGPI9	E25	USBOVR#5	GPI	Resume	-USBOVR5	
RSMGPI10	D12	SMB_ALERT#	GPI	Resume	-SMB_ALERT	
RSMGPI11	C11	RI	GPI	Resume	-WAKE_UP	
RSMGPI12	H23	ACPWR	GPI	Resume		
RSMGPI13	H25	LOWBAT#	GPI	Resume	-CARD_RI	PULL_UP(RESERVE)
RSMGPI14	J24	LID	GPI	Resume	-LID_SW	PULL_UP
RSMGPI15	E9	ACB_SDATAIN	GPI	Resume		
RSMGPIL0	B8	SLPBTN#	GPI	Resume		
RSMGPO4	E12	OFFCLKS1#	GPO	Resume		
RSMGPO5	C8	OFFCLKS3#	GPO	Resume	-SUSB	
RSMGPO6	B9	OFFCLKS4_S5#	GPO	Resume	-SUSC	
RSMGPO7	H24	SUSLED	GPO	Resume		
RSMGPO8	J26	CLK32KO	GPO	Resume		
RSMGPO9	J23	SUSPEND#	GPO	Resume	-SUS_STAT	
RSMGPO10	F9	ACB_RST#	GPO	Resume		

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1.3.2 Keyboard Controller Pin Define

Pin	Port	Signal Name	Type	Connect To	Description
39~54	GP17~GP0	KO[0..15]	O	Internal Keyboard	Keyboard Matrix
55~62	GP37~GP30	KI[7..0]	O	Internal Keyboard	Keyboard Matrix
65~68	GP85~GP82	LAD[0..3]	I/O	M1573M	LPC BUS
70	GP80	PCI_KBC_CLK	I	CLKGEN	LPC CLK
69	GP81	SERIRQ	O	M1573M	Serial IRQ
64	GP86	-KBCLRST	I	M1573M	LPC Reset
63	GP87	-LPC_FRAME	I/O	M1573M	LPC FRAME
17	GP50	MAINPWR	O	W83L950D	We use this signal to control "VS" power on/off. HI : ON, LOW : OFF
15	GP52	-SUSB	I	M1573M	STR Indicator signal
14	GP53	-ADEN	I	DC TO DC	ADAPTOR IN
18	GP42	-NUM_LOCK	O	LED	Keyboard NUMBERI Lock indicator
22	GP43	CHG_ON	O	Charger Cricuitry	Control charger ON/OFF
19	GP46	SCI	O	M1573M	Connect to South Bridge (M1573M) to system configuration interrupt (ACPI mode)
3	GP76	KBC_DATA	I/O	BAT & LM86	SMBUS DATA for LM86 thermal sensor & BATT THERMAL
2	GP77	KBC_CLK	I/O	BAT & LM86	SMBUS CLK for LM86 thermal sensor BATT THERMAL
27	GP40	-FAN_O	O	CPU FAN	Control CPU FAN ON & Turn ON/OFF Duty
26	GP41	NB_CORE_EN	O	NB PWM	Enable M480m core power
13	GP54	FAN_SPD	I	CPU FAN	Return FAN (CPU FAN) Speed.
12	GP55	PG_CPU_CORE	I	CPU PWM	Indicated CPU Vcore is good.
16	GP51	PG_NB_CORE	I	NB PWM	Indicate NB Vcore POWER is ok .
23	GP47	PWR_ON	O	switch	Control System Power ON/OFF
21	GP44	-RCIN	O	M1573M	Keyboard Reset for CPURST# gerneration
20	GP45	A20GATE	O	M1573M	GATE A20 OUTPUT
9	GP70	T_DATA	I/O	Touch PAD	Connect to touch Pad DATA
8	GP71	-LEARNING	O		

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Pin	Port	Signal Name	Type	Connect To	Description
7	GP72	-SB_PWRBTN	O	M1573M	Power Button Signal to M1573M
6	GP73	T_CLK	I/O	Touch PAD	Connect to Touch Pad clock
5	GP74	SB_PWRGD	O	M1573M	System Power Good
4	GP75	-SUSC	I	M1573M	System inter S4~S5,Positive Logic.
38	GP20	-AC_LED	O	LED	The indicator when power supply from ac- adapter.
37	GP21	-WAKE_UP	O	M1573M	Connect to South Bridge (M1573M) to wake up system
36	GP22	-BATT_G	O	LED	The indicator when battery in charging
35	GP23	-BATT_R	O	LED	The indicator when battery in charging
34	GP24	-EXTSMI	O	M1573M	Connect to South Bridge (M1573M) to system management interrupt (Non-ACPI mode)
33	GP25	-CAP_LOCK	O	LED	Keyboard CAP lock indicator
32	GP25	NB_PWRGD	I	NB	Indicate NB POWER is ok.
31	GP27	-BAT_LED	O	LED	The indicator when power supply from battery.
11	GP56	BLADJ	O	Inverter	Back / Light Adjust Control
10	GP57	IR_PWRON	O	IR	control IR Power ON/OFF
1	GP60	KBC_PWRBTN#	I	POWER SW	Power Switch Signal to KBC
80	GP61		I	1.8VS	Indicate 1.8VS ok
79	GP63		I	3V	Indicate 3V ok
78	GP63	BAT_TEMP	I	Battery	Report Battery Thermal
77	GP64	BAT_VOLT	I	Battery	Report Battery Voltage
76	GP65	I_LIMIT	I	CHARGE	FOR BATTERY CHARGE
75	GP66	-IR_POWERBTN	I	IR	Use IR function control system power on.
74	GP67	BATT_DEAD	I	Power Circuitry	Indicated the battery capacity is not enough to power on system
25	RESET#	KBCRST#			
28	XIN		I		
29	XOUT	EXTSMI#	O	M1573M	Connect to South Bridge (M1573M) to system management interrupt (Non-ACPI mode)
72	VREF	+3VA			
71	VCC	+3VA			

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1.3.3 Power Consumption of Suspend Mode

- Suspend to RAM < 80mA
- Suspend to Disk / Soft-Off /Mechanical Off < 5mA

1.3.4 Audio Performance

- 8350 meet all the following items

Test Items	Mobile System
Full Scale Output Voltage	≧0.7Vrms (3.3V audio)
Sample Frequency Accuracy	≦0.1%
Frequency Response (44.1ks/sec)	20Hz ~ 15kHz
Frequency Response (48ks/sec)	20Hz ~ 15kHz
Dynamic Range (SNR)	≧70dBFSA
THD+N	≦-55dBFS
Cross-talk	≧50dB

Table 9: Digital Playback (PC-D-A) for Line Output

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Test Items	Mobile System
Frequency Response	100Hz ~ 12kHz
Dynamic Range (SNR)	≧60dBFSA
THD+N	≦-50dBFS

Table 10: Analog Pass-Through (A-A) for Microphone Input to Line Output

Test Items	Mobile System
Full Scale Input Voltage	≧100mVrms
Sample Frequency Accuracy	≦0.1%
Frequency Response(22.05ks/sec)	100Hz ~ 8.8kHz
Dynamic Range (SNR)	≧60dBFSA
THD+N	≦-50dBFS

Table 11: Digital Recording (A-D-PC) for Microphone Input

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1.4 Reference Documents

Documents	Revision
Mobile AMD Athon64 Processor Data Sheet	2.05
Mobile AMD Athon64 Processor Motherboard Design Guide	2.21
Ati 480M North Bridge	0.4
Ati 480M Platform Design Guide	0.3
Uli M1573M V-Link Client highly integrated South Bridge	0.7
Cardbus Controller Datasheet(Ti PCI4510)	2002.07
Clock generator ICS951412	2004.10.21
VT6103L Tahoe Fast Ethernet 10/100 Base-TX, 1-Port PHY / Transceiver Data Sheet	1.42
VT6103L Tahoe Fast Ethernet 10/100 Base-TX, 1-Port PHY / Transceiver Design Guide	1.4
Winbond notebook keyboard/embedded controller W83L950D Data Sheet	1.4
PC2001 System Design Guide	0.7
PCI Local Bus Specification	2.2

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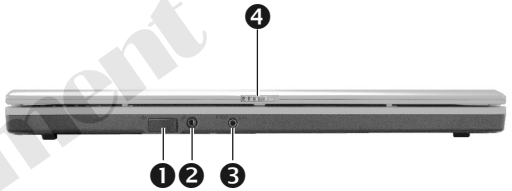
2. System View and Disassembly

2.1 System View

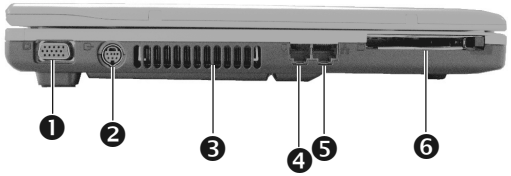
2.1.1 Front View

❶ USB Ports *1
❷ Line Out Connector
❸ Line In Connector
❹ Top Cover Latch



2.1.2 Left-side View

❶ VGA Port
❷ S-Video Port
❸ Ventilation Openings
❹ RJ-11 Connector
❺ RJ-45 Connector
❻ PCMCIA Card Socket



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2.1.3 Right-side View

❶ CD-ROM/DVD-ROM Drive

❷ Kensington Lock

2.1.4 Rear View

❶ Kensington Lock

❷ Power Connector

❸ USB Port*2

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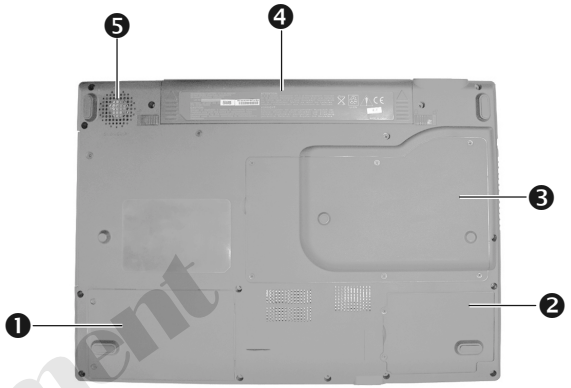
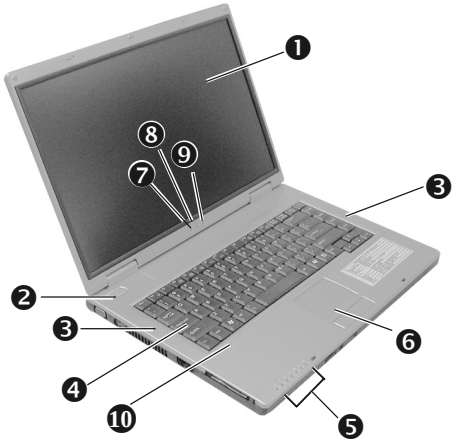
2.1.5 Bottom View



❶ Hard Disk Drive
❷ Wireless Card
❸ CPU & DDR SDRAM Card
❹ Battery Park
❺ Stereo Speaker Set

2.1.6 Top-open View



❶ LCD Screen
❷ Power Button
❸ Stereo Speaker Set
❹ Keyboard
❺ Device LED Indicators
❻ Touch Pad
❼ Battery Power Indicator
❽ Battery Charge Indicator
❾ AC Power Indicator
❿ Internal MIC In

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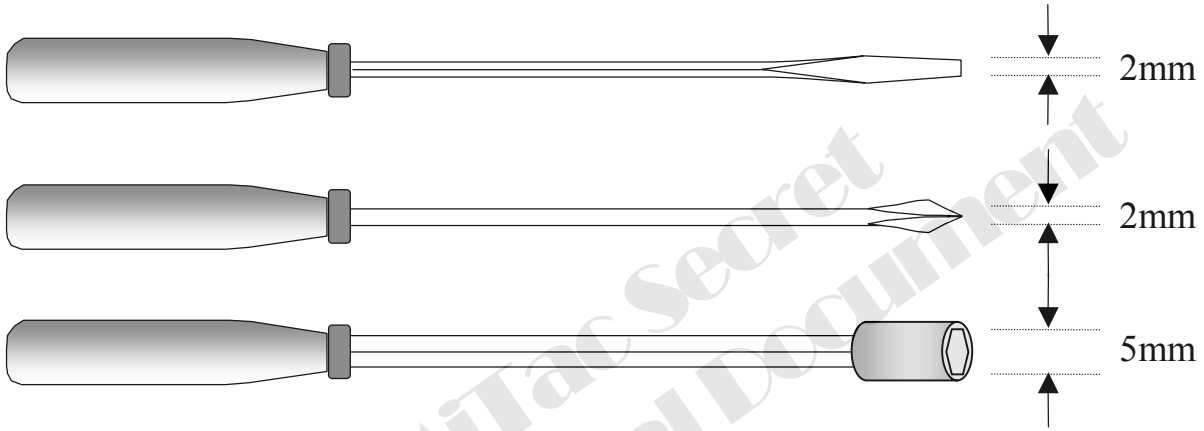
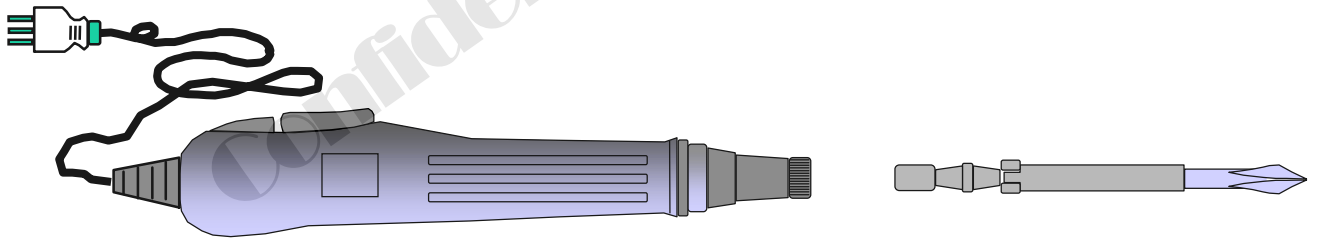
2.2 Tools Introduction

1. Screw driver with bit size for notebook assembly & disassembly.



2. Auto screw driver for notebook assembly & disassembly.



Bit Size

#0

Screw Size	Tooling	Tor.	Bit Size
1. M2.0	Auto Screwdriver	2.0-2.5 kg/cm2	#0

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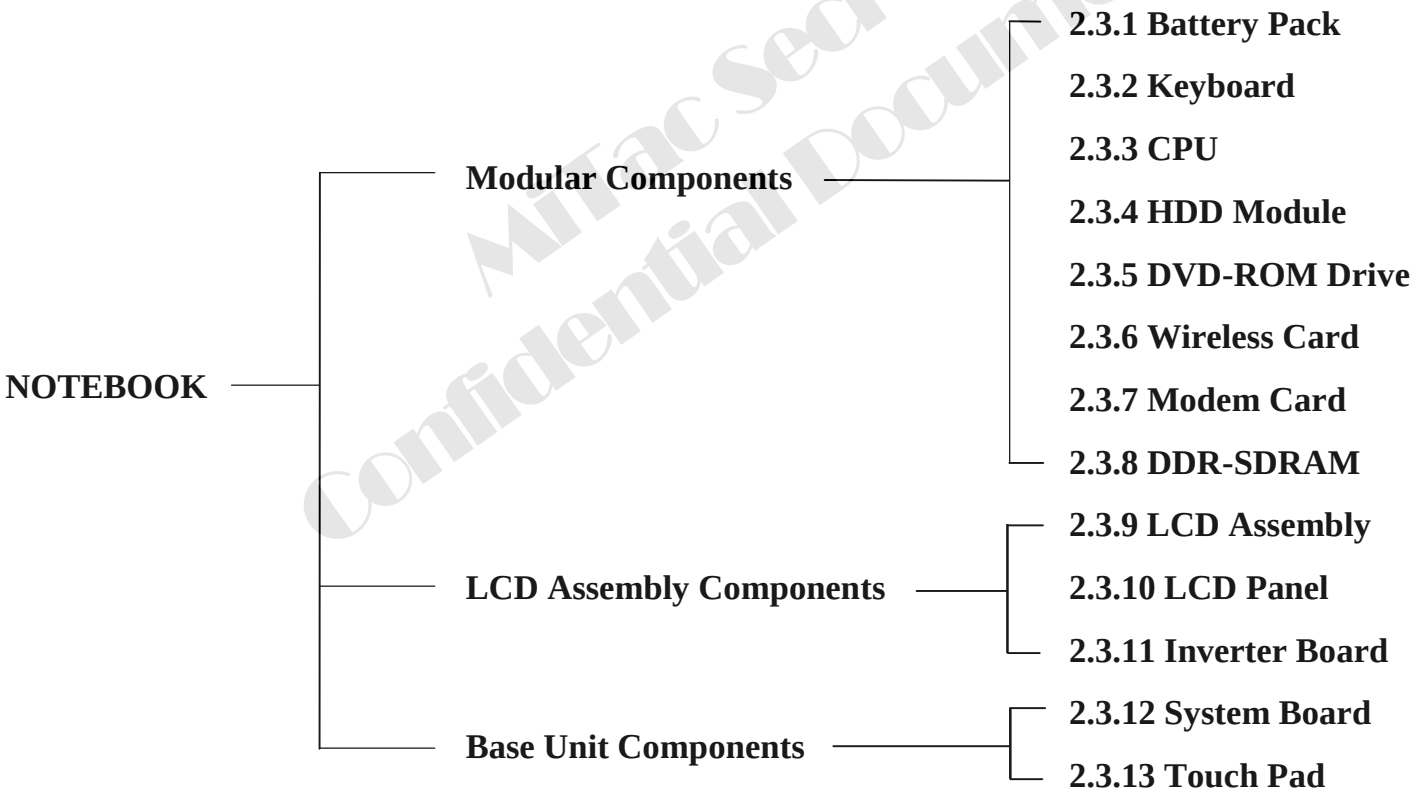
2.3 System Disassembly

The section discusses at length each major component for disassembly/reassembly and show corresponding illustrations.Use the chart below to determine the disassembly sequence for removing components from the notebook.

NOTE: *Before you start to install/replace these modules, disconnect all peripheral devices and make sure the notebook is not turned on or connected to AC power.*



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2.3.1 Battery Pack

Disassembly

1. Carefully put the notebook upside down.
2. Slide the two release lever outwards to the "unlock" ( ) position (❶), while take the battery pack out of the compartment (❷). (Figure 2-1)

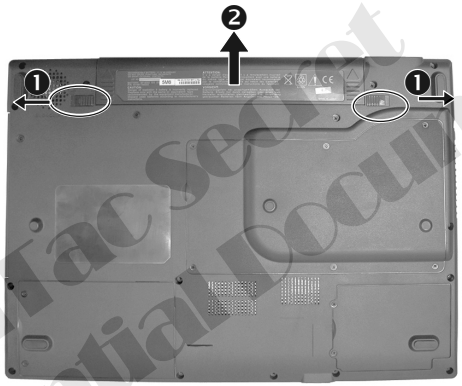

Figure 2-1 Remove the battery pack

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Reassembly

1. Replace the battery pack into the compartment. The battery pack should be correctly connected when you hear a clicking sound.
2. Slide the release lever to the "lock" ( ) position.

2.3.2 Keyboard

Disassembly

1. Remove the battery pack. (Refer to section 2.3.1 Disassembly)
2. Open the top cover.
3. Loosen the five latches locking the keyboard. (Figure 2-2)
4. Slightly lift up the keyboard and disconnect the cable from the mother board, then separate the keyboard. (Figure 2-3)

Figure 2-2 Loosen the five latches

Figure 2-3 Disconnect the cable

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Reassembly

1. Reconnect the keyboard cable and fit the keyboard back into place with five latches.
2. Replace the battery pack. (Refer to section 2.3.1 reassembly)

2.3.3 CPU

Disassembly

1. Remove the battery pack. (Refer to section 2.3.1 Disassembly)
2. Remove six screws fastening the heatsink cover. (Figure 2-4)
3. Remove four spring screws that secure the heatsink upon the CPU and disconnect the fan's power cord from system board. (Figure 2-5)

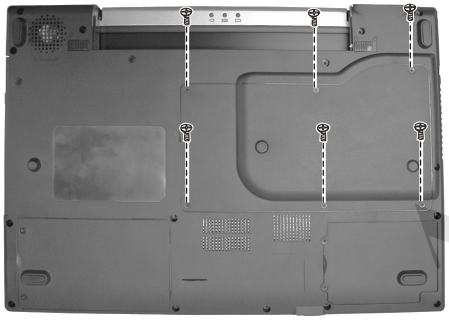

Figure 2-4 Remove six screws

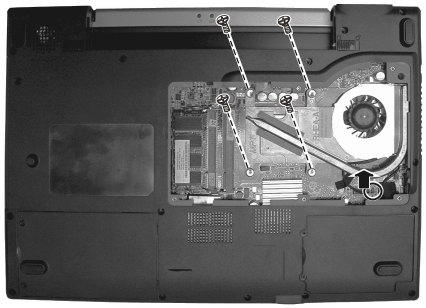

Figure 2-5 Free the heatsink

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4. To remove the existing CPU, lift the socket arm up to the vertical position. (Figure 2-6)

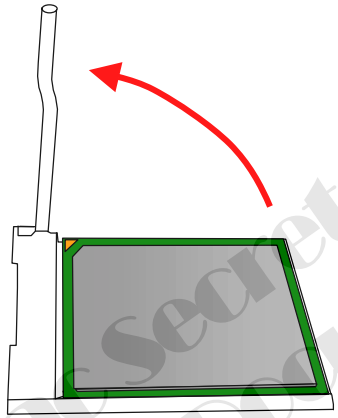

Figure 2-6 Remove the CPU

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Reassembly

1. Carefully, align the arrowhead corner of the CPU with the beveled corner of the socket, then insert CPU pins into the holes. Place the lever back to the horizontal position and push the lever to the left.
2. Connect the fan's power cord to the system board, fit the heatsink upon the CPU and secure with four spring screws.
3. Replace the CPU cover and secure with six screws.
4. Replace the battery pack. (Refer to section 2.3.1 reassembly)

2.3.4 HDD Module

Disassembly

1. Carefully put the notebook upside down. Remove the battery pack. (Refer to section 2.3.1 Disassembly)
2. Remove two screws fastening the HDD compartment cover. (Figure 2-7)
3. Remove the one screw and slide the HDD module out of the compartment. (Figure 2-8)

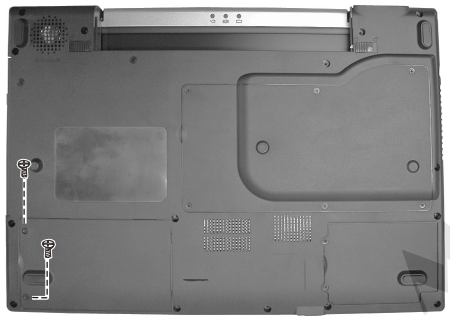

Figure 2-7 Remove the HDD compartment cover

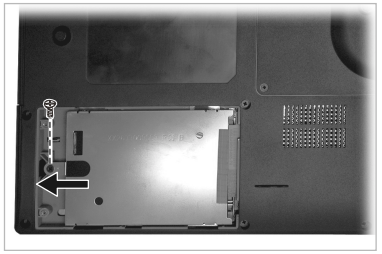

Figure 2-8 Remove HDD module

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4. Remove four screws to separate the hard disk drive from the bracket, remove four screws. (Figure 2-9)

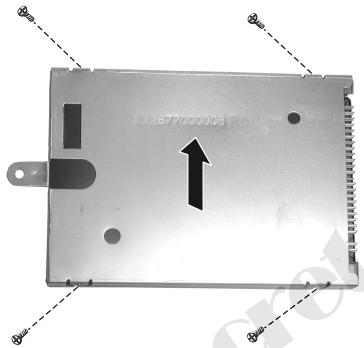

Figure 2-9 Remove hard disk drive

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Reassembly

1. Attach the bracket to hard disk drive and secure with four screws.
2. Slide the HDD module into the compartment and secure with one screw.
3. Place the HDD compartment cover and secure with two screws.
4. Replace the battery pack. (Refer to section 2.3.1 reassembly)

2.3.5 CD/DVD-ROM Drive

Disassembly

1. Carefully put the notebook upside down. Remove the battery pack. (Refer to section 2.3.1 Disassembly)
2. Remove one screw fastening the CD/DVD-ROM drive. (Figure 2-10)
3. Push firmly to release the tray (❶). Then gently pull out the CD/DVD-ROM drive by holding the tray that pops out (❷). (Figure 2-10)

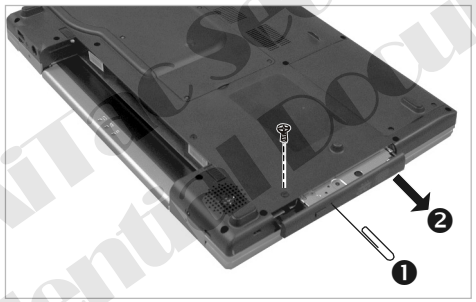

Figure 2-10 Remove the CD/DVD-ROM drive

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Reassembly

1. Push the CD/DVD-ROM drive into the compartment and secure with one screw.
2. Replace the battery pack. (Refer to section 2.3.1 reassembly)

2.3.6 Wireless Card

Disassembly

1. Carefully put the notebook upside down. Remove the battery pack. (Refer to sections 2.3.1 Disassembly)
2. Remove the two screws fastening the Mini PCI compartment cover. (Figure 2-11)
3. Disconnect the wireless card's antennae first (❶). Then pull the retaining clips outwards (❷) and remove the wireless card (❸). (Figure 2-12)

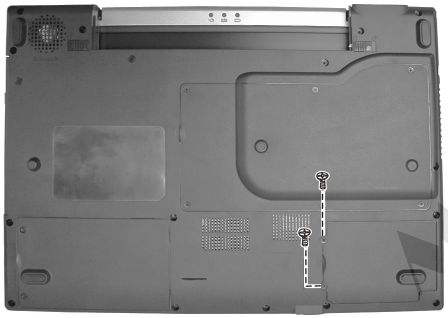

Figure 2-11 Remove two screws

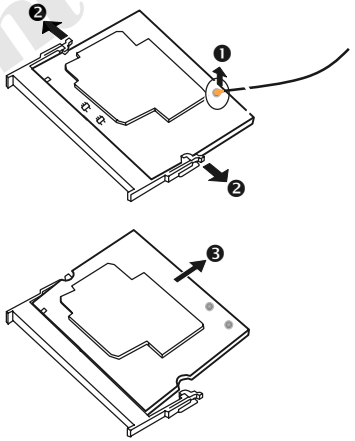

Figure 2-12 Remove the Wireless card

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Reassembly

1. To install the wireless card, match the wireless card 's notched part with the socket's projected part and firmly insert it into the socket. Then push down until the retaining clips lock the wireless card into position. Then sure that the antennae fully populated.
2. Tighten the screws to secure the wireless card compartment cover to the housing.
3. Replace the battery pack. (Refer to section 2.3.1 reassembly)

2.3.7 Modem Card

Disassembly

1. Carefully put the notebook upside down. Remove the battery pack. (Refer to section 2.3.1 Disassembly)
2. Remove two screws fastening modem card's compartment cover. (Refer to steps 1-2 of section 2.3.6 Disassembly)
3. Remove two screws fastening the modem card. (Figure 2-13)
4. Lift up the modem card and disconnect the cord. (Figure 2-14)

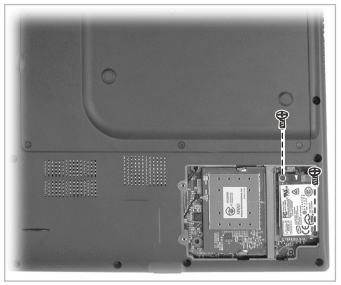

Figure 2-13 Remove two screws

Figure 2-14 Disconnect the cord

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Reassembly

1. Reconnect the cord and fit the modem card.
2. Fasten the modem card by two screws.
3. Replace the modem card's compartment cover by two screws. (Refer to step 2 of section 2.3.6 reassembly).
4. Replace the battery pack. (Refer to section 2.3.1 reassembly)

2.3.8 DDR-SDRAM

Disassembly

1. Carefully put the notebook upside down. And remove the battery pack. (See section 2.3.1 disassembly)
2. Remove six screws fastening the DDR compartment cover to access the SO-DIMM socket. (Figure 2-15)
3. Pull the retaining clips outwards (❶) and remove the SO-DIMM (❷). (Figure 2-16)

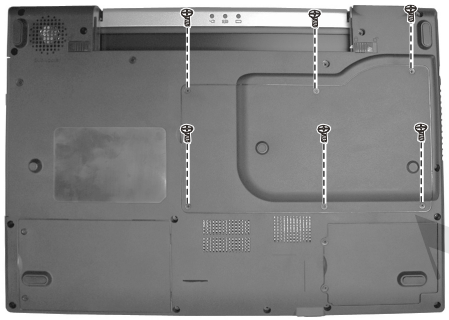

Figure 2-15 Remove the cover

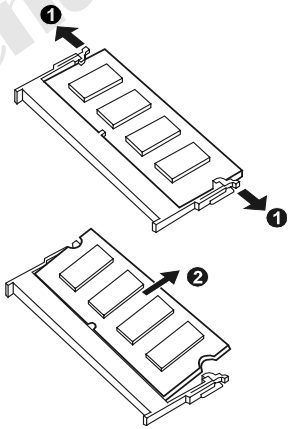

Figure 2-16 Remove the SO-DIMM

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Reassembly

1. To install the DDR, match the DDR's notched part with the socket's projected part and firmly insert the SO-DIMM into the socket at 20-degree angle. Then push down until the retaining clips lock the DDR into position.
2. Replace six screws to fasten the DDR compartment cover.
3. Replace the battery pack. (See section 2.3.1 reassembly)

2.3.9 LCD ASSY

Disassembly

1. Remove the battery pack, keyboard,CPU, hard disk drive, CD/DVD-drive, wireless card, modem card and DDR. (See sections 2.3.1, 2.3.2, 2.3.3, 2.3.4, 2.3.5, 2.3.6, 2.3.7 and 2.3.8 Disassembly)
2. Remove the nineteen screws on the bottom of notebook. (Figure 2-17)
3. Remove the four screws that secure the hinge cover. (Figure 2-18)

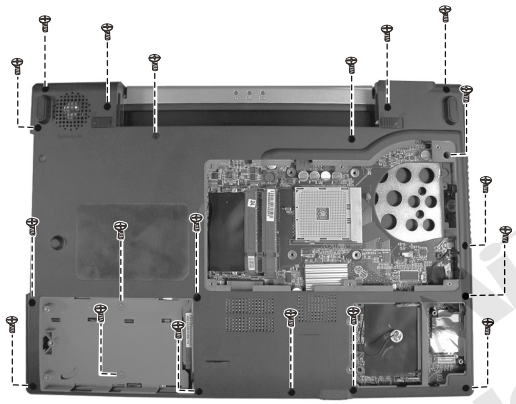

Figure 2-17 Remove nineteen screws

Figure 2-18 Remove four screws

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4. Remove the two screws and disconnect the touch pad's cable, then free the top cover.(Figure 2-19)
5. Remove the two hinge covers. (Figure 2-20)

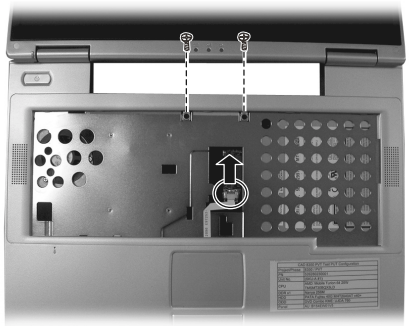

Figure 2-19 Free the Top cover

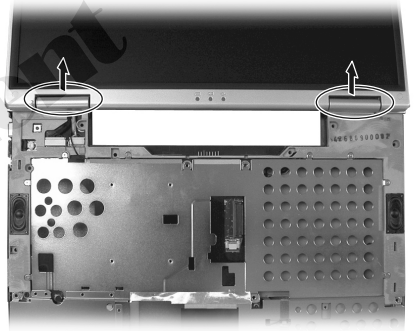

Figure 2-20 Remove the hinge covers

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6. Disconnect the two cables and remove the four screws. (Figure 2-21)
7. Remove the eight screws. (Figure 2-22)

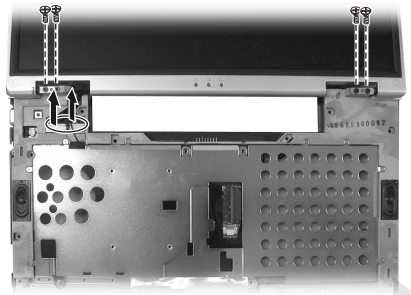

Figure 2-21 Remove the four screws and Disconnect the two cables

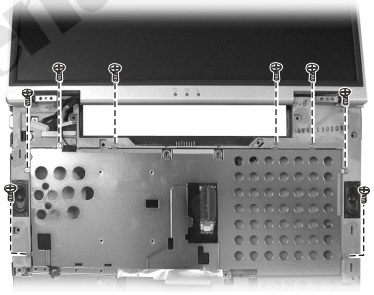

Figure 2-22 Remove the eight screws

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8. Carefully pull the antenna wires out. Now you can lift up the LCD ASSY from base unit. (Figure 2-23)

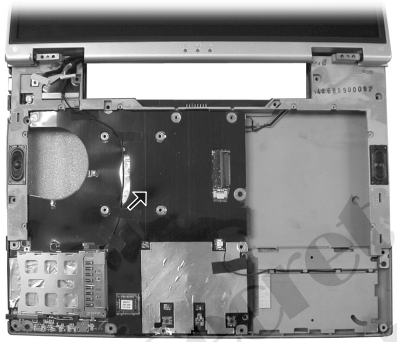

Figure 2-23 Free the LCD ASSY

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Reassembly

1. Attach the LCD assembly to the base unit and secure with four screws.
2. Rip the antenna wires back into Min-PCI compartment.
3. Reconnect the two cables to the system board. Screw the hinge covers by two screws.
4. Replace the shield and secure with eight screws.
5. Replace the top cover and secure with two screws. And reconnect the touch pad's cable.
6. Upside down the notebook. secure the housing by nineteen screws and secure two screws in the rear.
7. Replace the DDR, modem cad, Wireless card, CD/DVD-ROM, hard disk drive, CPU, keyboard and battery pack. (Refer to sections 2.3.8, 2.3.7, 2.3.6, 2.3.5, 2.3.4, 2.3.3, 2.3.2 and 2.3.1 reassembly)

2.3.10 LCD Panel

Disassembly

1. Remove the battery, keyboard, hard disk drive, CD/DVD-ROM drive and LCD assembly. (Refer to section 2.3.1, 2.3.2, 2.3.4, 2.3.5 and 2.3.9 Disassembly)
2. Remove the two rubber pads and two screws on the corners of the panel. (Figure 2-24)
3. Insert a flat screwdriver to the lower part of the LCD cover and gently pry the frame out. Repeat the process until the cover is completely separated from the housing.
4. Remove the twelve screws and disconnect the cable. (Figure 2-25)

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Figure 2-24 Remove LCD cover

Figure 2-25 Remove twelve screws and disconnect the cable

5. Remove the six screws that secure the LCD bracket. (Figure 2-26)
6. Disconnect the cable to free the LCD panel. (Figure 2-27)

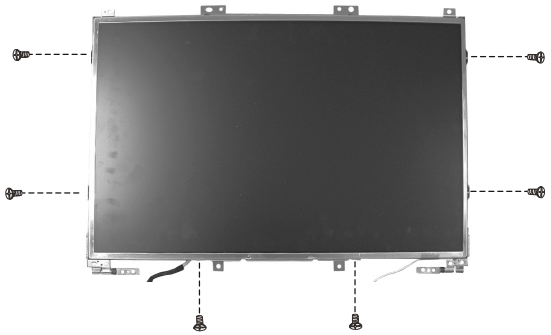

Figure 2-26 Remove the six screws

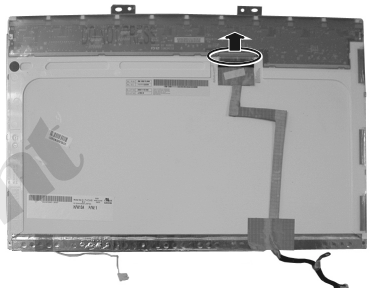

Figure 2-27 Free the LCD panel

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Reassembly

1. Replace the cable to the LCD.
2. Attach the LCD panel's bracket back to LCD panel and secure with six screws.
3. Replace the LCD panel into LCD housing. And reconnect two cables to inverter board and secure with two screws.
4. Fasten the LCD panel by ten screws.
5. Fit the LCD cover and secure with two screws and rubber pads.
6. Replace the LCD assembly, CD/DVD-ROM drive, hard disk drive, keyboard, battery pack. (See sections 2.3.9, 2.3.5, 2.3.4, 2.3.2, and 2.3.1 reassembly)

2.3.11 Inverter Board

Disassembly

1. Remove the battery, keyboard, hard disk drive, CD/DVD-ROM drive and LCD assembly. (Refer to section 2.3.1, 2.3.2, 2.3.4, 2.3.5 and 2.3.9 Disassembly)
2. Remove the LCD cover and LCD panel. (Refer to the steps 1-4 of section 2.3.10 Disassembly)
3. Remove the one screw fastening the inverter board and disconnect the cable, Then free the inverter board. (Figure 2-28)

Figure 2-28 Free the inverter board

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Reassembly

1. Reconnect the cable. Fit the inverter board back into place and secure with one screw.
2. Replace the LCD Panel and LCD cover. (Refer to section 2.3.10 reassembly)
3. Replace the LCD assembly. (Refer to section 2.3.9 reassembly)
4. Replace the CD/DVD-ROM drive, hard disk drive, keyboard and battery pack. (Refer to sections 2.3.5, 2.3.4, 2.3.2 and 2.3.1 reassembly)

2.3.12 System Board

Disassembly

1. Remove the battery, keyboard, hard disk drive, CD/DVD-ROM drive, Wireless card and LCD assembly. (Refer to sections 2.3.1, 2.3.2, 2.3.4, 2.3.5, 2.3.6 and 2.3.9 Disassembly)
2. Remove the four screws that secure the system board and disconnect the two speaker's cables. Then lift it up from the housing. (Figure 2-29)
3. Disconnect the one speaker's cables from the system board and remove the two screws, Then separate the bracket and free the system board. (Figure 2-30)

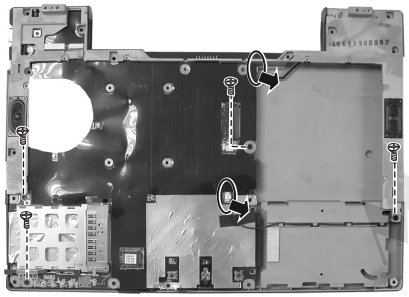

Figure 2-29 Remove four screws and disconnect the two cables

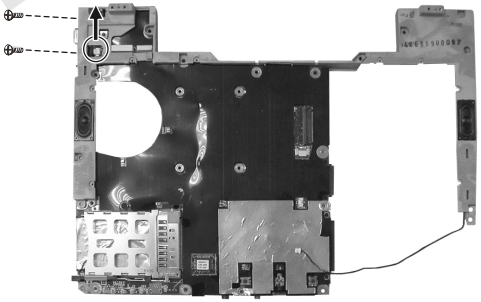

Figure 2-30 Free the system board

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Reassembly

1. Fit the bracket and secure with two screws .
2. Turn over the system board. Reconnect the speaker's cords.
3. Replace the system board back into the housing and secure with four screws, then reconnect the cable.
4. Replace the LCD assembly, CD/DVD-ROM, HDD, keyboard and battery pack. (Refer to previous section reassembly)

2.3.13 Touch Pad

Disassembly

1. Remove the battery pack, keyboard, hard disk drive and CD/DVD-drive. (See sections 2.3.1, 2.3.2 , 2.3.4 and 2.3.5 Disassembly)
2. Remove the top cover. (See steps 1-5 in section 2.3.9 Disassembly)
3. Remove the two screws and free the touch pad. (Figure 2-31).

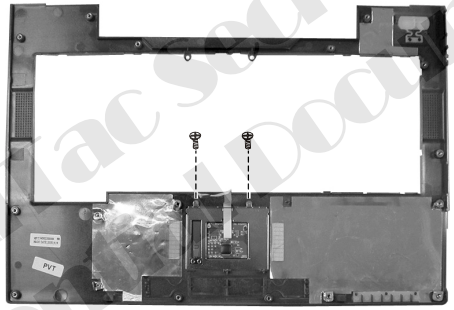

Figure 2-31 Remove the two screws

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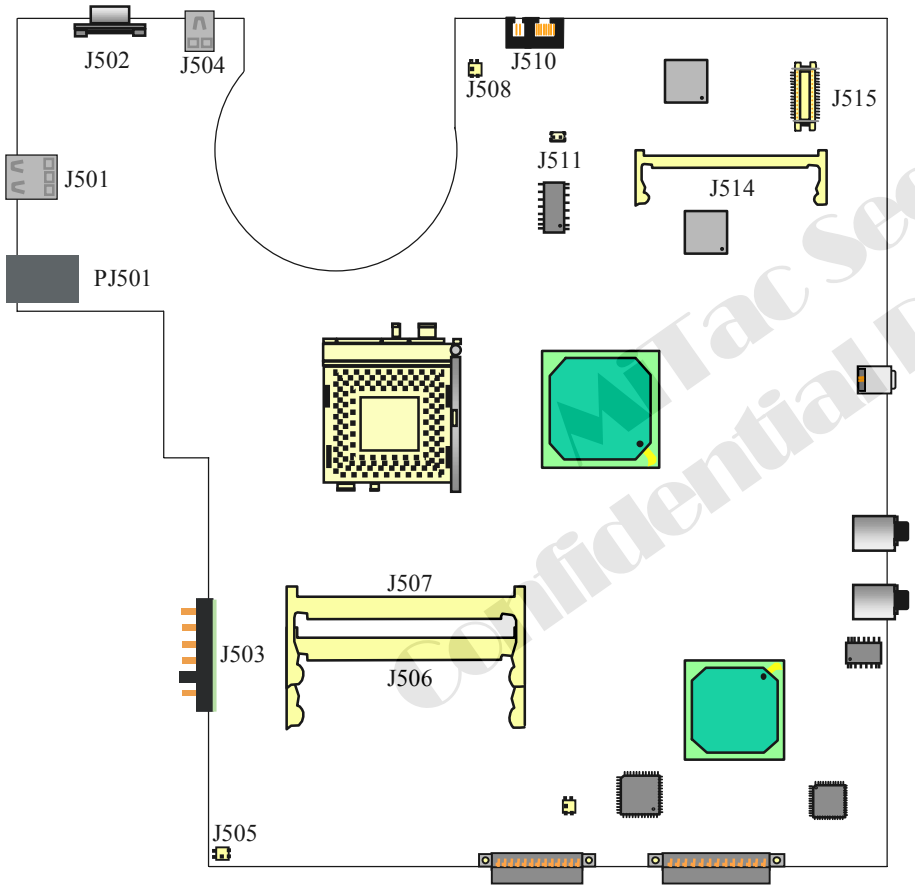
Reassembly

1. Replace the touch pad and secure the two screws.
2. Replace the top cover. (Refer to the section in 2.3.9 reassembly)
3. Replace the battery pack, keyboard, hard disk drive and CD/DVD-drive. (See sections 2.3.1,2.3.2 , 2.3.4 and 2.3.5 Disassembly).

3. Definition & Location of Connectors / Switches

3.1 Mother Board-A(1)



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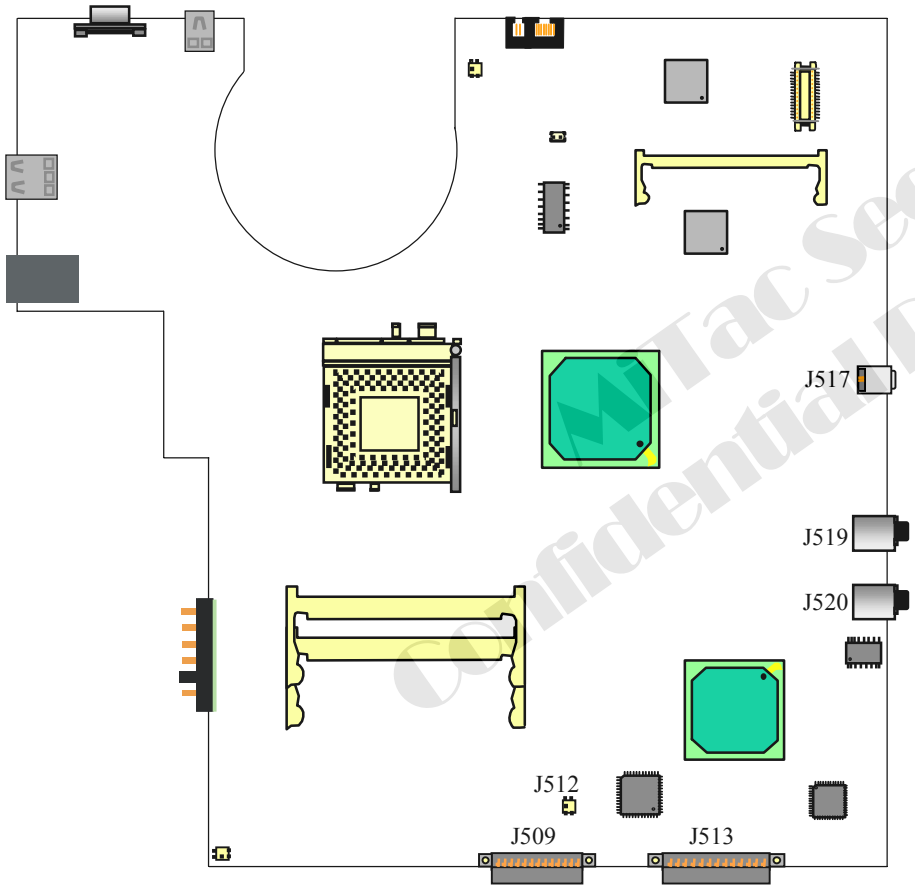
- **PJ501 : Power Jack**
- **J501 : USB Port**
- **J502 : External VGA Connector**
- **J503 : Battery Connector**
- **J504 : TV-Out Connector**
- **J505 : Internal Subwoofer Connector**
- **J506, J507 : Extend DDR SDRAM Connector**
- **J508 : Modem Connector**
- **J510 : RJ45 & RJ11 Connector**
- **J511 : CPU Fan Connector**
- **J514 : MINI-PCI Connector**
- **J515 : MDC Connector**

------ To next page ------

3. Definition & Location of Connectors / Switches

3.1 Mother Board-A(2)



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- **J509 : CDROM-Secondary IDE Connector**
- **J512 : CMOS Battery Connector**
- **J513 : HDD-Primary IDE Connector**
- **J517 : USB Port**
- **J519 : Internal MIC In Connector**
- **J520 : Line Out Connector**

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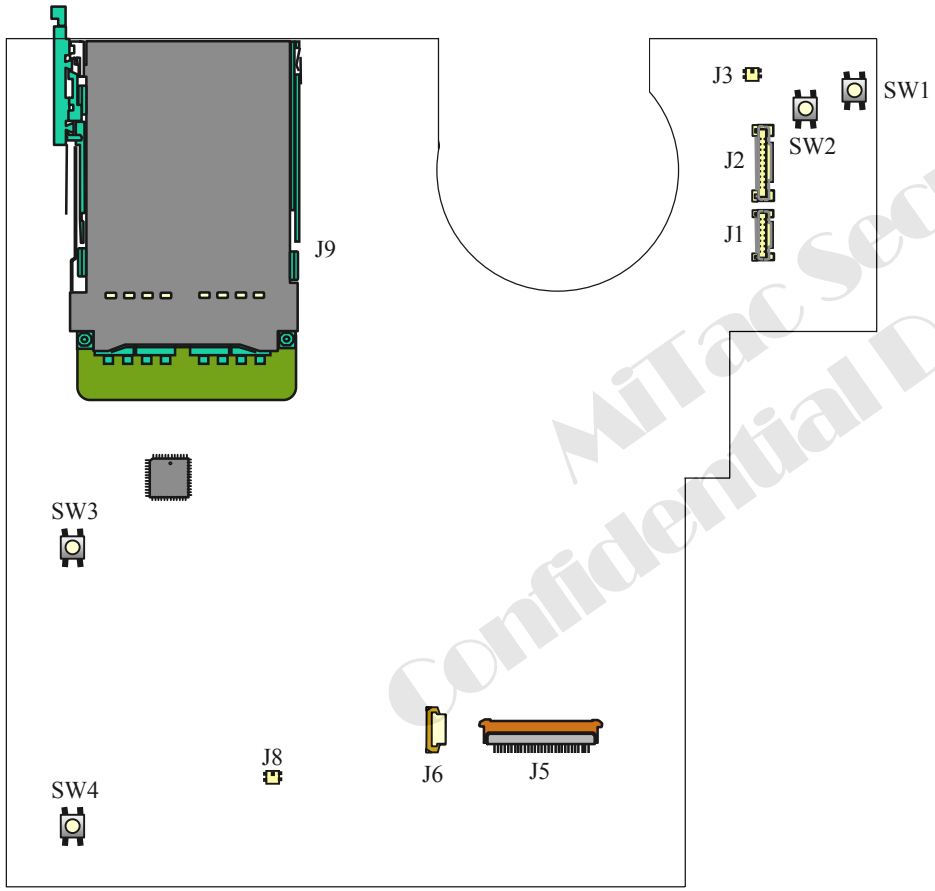
3. Definition & Location of Connectors / Switches

3.1 Mother Board-B



- J1 : Inverter Board Connector
- J2 : LCD Connector
- J3 : Left Speaker Connector
- J5 : Internal Keyboard Connector
- J6 : Touch-Pad Connector
- J8 : Right Speaker Connector
- J9 : PCMCIA Card Socket

- SW1 : LID Switch Button
- SW2 : Power On/Off Button
- SW3 : Touch-Pad Left Button
- SW4 : Touch-Pad Right Button

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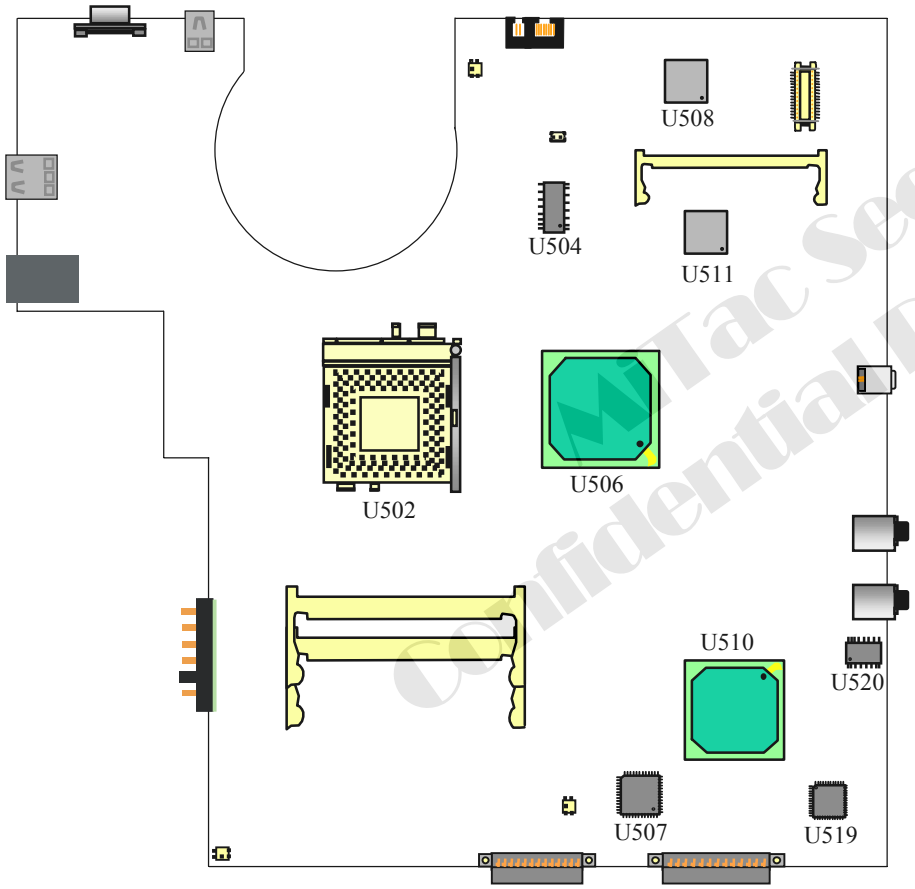
4. Definition & Location of Major Components

4.1 Mother Board-A



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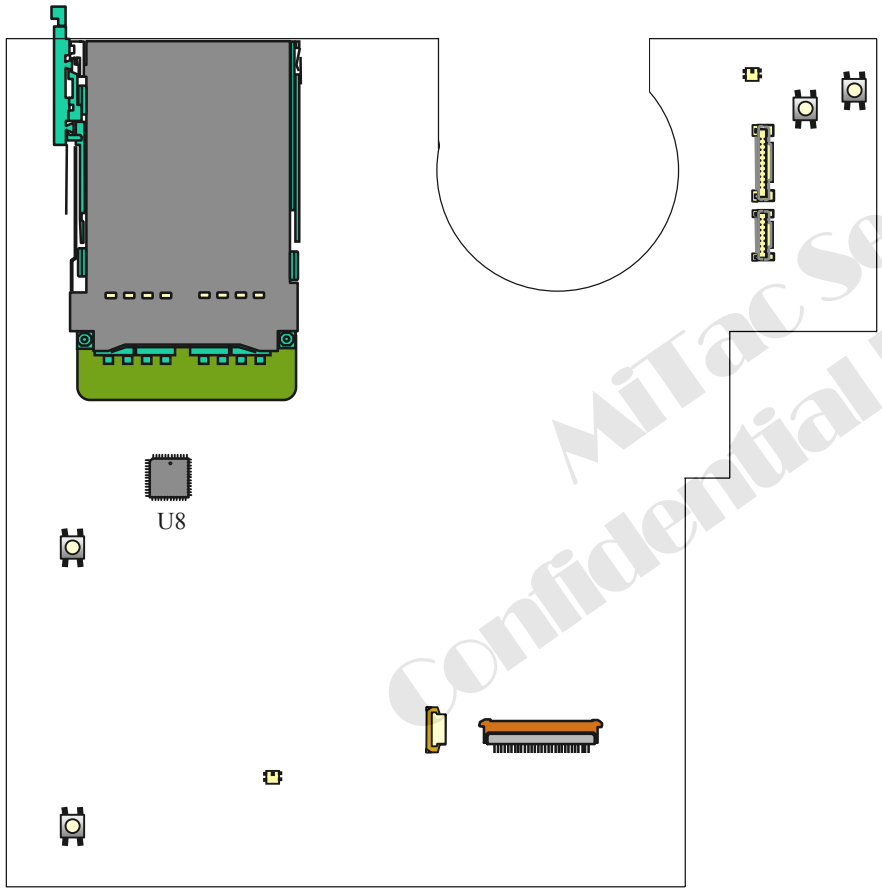
- U502 : CPU (AMD Mobile K8) Socket
- U504 : ICS951412 Clock Generator
- U506 : North Bridge(ATI RS480M)
- U507 : Keyboard BIOS(W83L950D)
- U508 : VT6103L LAN Controller
- U510 : South Bridge(ULI M1573M)
- U511 : CardBus PCI4510
- U519 : Audio Codec ALC655
- U520 : Audio Amplifier TPA0212

4. Definition & Location of Major Components

4.1 Mother Board-B



U8 : System BIOS

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5. Pin Descriptions of Major Components

5.1 AMD Mobile K8 BGA754_SKT Pin(1)

Miscellaneous Pin Descriptions

Signal Name	Type	Description
RESET_L	I-IOS	System Reset
PWROK	I-IOS	Indicates that voltages and clocks have reached specified operation
LDTSTOP_L	I-IOS	HyperTransport™ Technology Stop Control Input. Used for power management and for changing HyperTransport link width and frequency.
VID[4:0]	O-IOS	Voltage ID to the regulator
THERMDA	A	Anode (+) of the thermal diode
THERMDC	A	Cathode (–) of the thermal diode
THERMTRIP_L	O-IO-OD	Thermal Sensor Trip output, asserted at nominal temperature of 125 ℃.
COREFB_H/L	A	Differential feedback for VDD Power Supply
VDDIOFB_H/L	A	Differential feedback for VDDIO Power Supply
CORE_SENSE	A	VDD voltage monitor pin
VDDA	S	Filtered PLL Supply Voltage
VTT_SENSE	A	VTT voltage monitor pin
VDDIO_SENSE	A	VDDIO voltage monitor pin
VDD	S	Core power supply
VDDIO	S	DDR SDRAM I/O ring power supply
VLDT_A VLDT_B	S	HyperTransport™ I/O ring power supply for side A and side B of the package
VTT_A VTT_B	S	VTT regulator voltage for side A and side B of the die
VSS	S	Ground

Debug Pin Descriptions

Signal Name	Type	Description
DBREQ_L	I-IOS	Debug Request
DBRDY	O-IOS	Debug Ready

JTAG Pin Descriptions

Signal Name	Type	Description
TCK	I-IOS	JTAG Clock
TMS	I-IOS	JTAG Mode Select
TRST_L	I-IOS	JTAG Reset
TDI	I-IOS	JTAG Data Input
TDO	O-IOS	JTAG Data Output

Clock Pin Descriptions

Signal Name	Type	Description
CLKIN_H/L	I-IOD	200-MHz PLL Reference Clock
FBCLKOUT_H/L	O-IOD	Core Clock PLL 200-MHz Feedback Clock

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5.1 AMD Mobile K8 BGA754_SKT Pin(2)

DDR SDRAM Memory Interface Pins

Signal Name	Type	Description
MEMCLK_H/L[7]	O-IOD	Differential DDR SDRAM clock to the top of DIMM 0 for unbuffered DIMMs.1
MEMCLK_H/L[6]	O-IOD	Differential DDR SDRAM clock to the top of DIMM 1 for unbuffered DIMMs.1
MEMCLK_H/L[5]	O-IOD	Differential DDR SDRAM clock to the bottom of DIMM 0 for unbuffered DIMMs.1
MEMCLK_H/L[4]	O-IOD	Differential DDR SDRAM clock to the bottom of DIMM 1 for unbuffered DIMMs.1
MEMCLK_H/L[3]	O-IOD	Differential DDR SDRAM clock to DIMM 3 for registered DIMMs.1
MEMCLK_H/L[2]	O-IOD	Differential DDRS DRAM clock to DIMM 2 for registered DIMMs.1
MEMCLK_H/L[1]	O-IOD	Differential DDR SDRAM clock to the middle of DIMM 1 for unbuffered DIMMs, or DIMM 1 for registered DIMMs.1
MEMCLK_H/L[0]	O-IOD	Differential DDR SDRAM clock to the middle of DIMM 0 for unbuffered DIMMs, or DIMM 0 for registered DIMMs.1
MEMCKEA MEMCKEB	O-IOS	Clock Enables to DIMMs. Used to gate clocks for power management functionality.1
MEMDQS[17:0]	B-IOS	DRAM Data Strobes synchronous with MEMDATA and MEMCHECK during DRAM read and writes.1
MEMDATA[63:0]	B-IOS	DRAM Interface Data Bus
MEMCHECK[7:0]	B-IOS	DRAM Interface ECC Check Bits
MEMCS_L[7:0]	O-IOS	DRAM Chip Selects 1
MEMRASA_L MEMRASB_L	O-IOS	DRAM Row Address Select. MEMRASA_L and MEMRASB_L are functionally identical. Two copies are provided to accommodate the loading of unbuffered DIMMs.1
MEMCASA_L MEMCASB_L	O-IOS	DRAM Column Address Select. MEMCASA_L and MEMCASB_L are functionally identical. Two copies are provided to accommodate the loading of unbuffered DIMMs.1
MEMWEA_L MEMWEB_L	O-IOS	DRAM Write Enable. MEMWEA_L and MEMWEB_L are functionally identical. Two copies are provided to accommodate the loading of unbuffered DIMMs.1
MEMADDA[13:0] MEMADDB[13:0]	O-IOS	DRAM Column/Row Address. Two copies are provided to accommodate the loading of unbuffered DIMMs. During precharges, activates, reads, and writes, the two copies are inverted from each other (except A[10] which is used for auto-precharge) to minimize switching noise. The signals are inverted only when the bus is used to carry address information.1

DDR SDRAM Memory Interface Pins (Continued)

Signal Name	Type	Description
MEMBANKA[1:0] MEMBANKB[1:0]	O-IOS	DRAM Bank Address. Two copies are provided to accommodate the loading of unbuffered DIMMs. During precharges, activates, reads, and writes the two copies are inverted from each other to minimize switching noise. The signals are inverted only when the bus is used to carry address information.1
MEMRESET_L	O-IOS	DRAM Reset pin for Suspend-to-RAM power management mode. This pin is required for registered DIMMs only.
MEMVREF	VREF	DRAM Interface Voltage Reference 1
MEMZP	A	Compensation Resistor tied to VSS 1
MEMZN	A	Compensation Resistor tied to 2.5 V 1

Notes:

1. For connection details and proper resistor values, see the AMD Athlon™ 64 Processor Motherboard Design Guide*, order# 24665.*

HyperTransport™ Technology Pin Descriptions

Signal Name	Type	Description
L0_CLKIN_H/L[1:0]	I-HT	Link 0 Clock Input
L0_CTLIN_H/L[1:0]	I-HT	Link 0 Control Input 2
L0_CADIN_H/L[15:0]	I-HT	Link 0 Command/Address/Data Input
L0_CLKOUT_H/L[1:0]	O-HT	Link 0 Clock Outputs
L0_CTLOUT_H/L[1:0]	O-HT	Link 0 Control Output
L0_CADOUT_H/L[15:0]	O-HT	Link 0 Command/Address/Data Outputs
L0_REF1	A	Compensation Resistor to VLDT 1
L0_REF0	A	Compensation Resistor to VSS 1

Notes:

*1. These pins are used in an alternating fashion to compensate R TT by internal comparison to 3/4 VLDT and 1/4 VLDTand compensate R ON by comparison to each other around 1/2 VLDT. For proper resistor value, see the*AMD Athlon™ 64 Processor Motherboard Design Guide*, order# 24665.*

2. The unused L0_CTLIN_H/L[1] pins must be properly terminated such that the true pin is pulled High and thecomplement is pulled Low. Refer to the AMD Athlon™ 64 Processor Motherboard Design Guide*, order# 24665, for details.*

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5.2 ATI RS480M North Bridge(1)

CPU Interface

Pin Name	Type	Power Domain	Ground Domain	Functional Description
HT_RXCAD[15:0]P, HT_RXCAD[15:0]N	I	VDDHT	VSS	Receiver Command, Address, and Data Differential Pairs
HT_RXCLK[1:0]P, HT_RXCLK[1:0]N	I	VDDHT	VSS	Receiver Clock Signal Differential Pair. Forwarded clock signal. Each byte of RXCAD uses a different clock signal. Data is transferred on each clock edge.
HT_RXCTLP, HT_RXCTLN	I	VDDHT	VSS	Receiver Control Differential Pair. For distinguishing control packets from data packets.
HT_TXCAD[15:0]P, HT_TXCAD[15:0]N	O	VDDHT	VSS	Transmitter Command, Address, and Data Differential Pairs
HT_TXCLK[1:0]P, HT_TXCLK[1:0]N	O	VDDHT	VSS	Transmitter Clock Signal Differential Pair. Each byte of TXCAD uses a different clock signal. Data is transferred on each clock edge.
HT_TXCTLP, HT_TXCTLN	O	VDDHT	VSS	Transmitter Control Differential Pair. Forwarded clock signal. For distinguishing control packets from data packets.
HT_RXCALN	Other	VDDHT	VSS	Receiver Calibration Resistor to VDD_HT power rail.
HT_RXCALP	Other	VDDHT	VSS	Receiver Calibration Resistor to Ground
HT_TXCALP	Other	VDDHT	VSS	Transmitter Calibration Resistor to HTTX_CALN
HT_TXCALN	Other	VDDHT	VSS	Transmitter Calibration Resistor to HTTX_CALP
HTREFCLK	I	HTPVDD	HTPVSS	HyperTransport 66 MHz reference clock from external clock source
HTTSTCLK	I	HTPVDD	HTPVSS	HyperTransport Bus Test Clock. Drives test clock in test mode. Connect to ground in functional mode.

GDDR Side-Port Memory Interface

Pin Name	Type	Power Domain	Ground Domain	Integrated Termination	Functional Description
MEM_A[14:0]	O	VDD_MEM	VSS	None	Memory Address Bus. Provides the multiplexed row and column addresses to the memories.
MEM_RAS#	O	VDD_MEM	VSS	None	Row Address Strobe
MEM_CAS#	O	VDD_MEM	VSS	None	Column Address Strobe
MEM_WE#	O	VDD_MEM	VSS	None	Write Enable Strobe
MEM_CKE	O	VDD_MEM	VSS	None	Clock Enable
MEM_CKP	O	VDD_MEM	VSS	None	Memory Differential Positive Clock
MEM_CKN	O	VDD_MEM	VSS	None	Memory Differential Negative Clock
MEM_CS#	O	VDD_MEM	VSS	None	Chip Select
MEM_DQ[63:0]	I/O	VDD_MEM	VSS	None	Memory Data Bus. Supports SSTL2 and SSTL3.
MEM_DM[7:0]	I/O	VDD_MEM	VSS	None	Data masks for each byte during memory write cycles
MEM_DQS[7:0]P	I/O	VDD_MEM	VSS	None	GDDR Data Strobes. These are bi-directional data strobes for latching read/write data.
MEM_DQS[7:0]N	I/O	VDD_MEM	VSS	None	Do not connect.
MEM_VMODE	I	–	VSS	None	Selects Memory I/O type. This pin must be tied to the appropriate level depending on the memories connected to the interface. For VDD_MEM=2.5V, connect MEM_VMODE 0V. For VDD_MEM=1.8V, connect MEM_VMODE to 1.8V. **NOTES:** (1) All DRAM connected must be of the SAME interface type; (2) In Sleep mode, when the memory power is on and when MEM_VMODE selects VDD_MEM=1.8V, MEM_VMODE pad MUST ALSO have 1.8V applied to it.

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5.2 ATI RS480M North Bridge(2)

4 x 1 Lane PCI Express Interface for General Purpose External Devices

Pin Name	Type	Power Domain	Ground Domain	Integrated Termination	Functional Description
GPP_TX0P/SB_TX2P, GPP_TX0N/SB_TX2N	O	VDDA_18	VSSA	50Ω between complements	Transmit Data Differential Pair for general purpose external devices or A-Link Express interface expansion. Connect to an external connector on the motherboard for New Card support or to the IXP for A-Link Expression expansion.
GPP_TX1P/SB_TX3P, GPP_TX1N/SB_TX3N	O	VDDA_18	VSSA	50Ω between complements	Transmit Data Differential Pair for general purpose external devices or A-Link Express interface expansion. Connect to an external connector on the motherboard for New Card support or to the IXP for A-Link Expression expansion.
GPP_TX2P, GPP_TX2N	O	VDDA_18	VSSA	50Ω between complements	Transmit Data Differential Pair. Connect to an external connector on the motherboard for New Card support.
GPP_TX3P, GPP_TX3N	O	VDDA_18	VSSA	50Ω between complements	Transmit Data Differential Pair. Connect to an external connector on the motherboard for New Card support.
GPP_RX0P/SB_RX2P, GPP_RX0N/SB_RX2N	I	VDDA_18	VSSA	50Ω between complements	Receive Data Differential Pair for general purpose external devices or A-Link Express interface expansion. Connect to an external connector on the motherboard for New Card support or to the IXP for A-Link Expression expansion.
GPP_RX1P/SB_RX3P, GPP_RX1N/SB_RX3N	I	VDDA_18	VSSA	50Ω between complements	Receive Data Differential Pair for general purpose external devices or A-Link Express interface expansion. Connect to an external connector on the motherboard for New Card support or to the IXP for A-Link Expression expansion.
GPP_RX2P, GPP_RX2N	I	VDDA_18	VSSA	50Ω between complements	Receive Data Differential Pair. Connect to an external connector on the motherboard for New Card support.
GPP_RX3P, GPP_RX3N	I	VDDA_18	VSSA	50Ω between complements	Receive Data Differential Pair. Connect to an external connector on the motherboard for New Card support.

Clock Interface

Pin Name	Type	Power Domain	Ground Domain	Integrated Termination	Functional Description
HTREFCLK	I	HTPVDD	HTPVSS	–	HyperTransport 66 MHz reference clock from external clock source
	I	HTPVDD	HTPVSS	–	HyperTransport Bus Test Clock. Drives test clock in test mode Connect to ground in functional mode.
TVCLKIN	I	VDDR3	VSS	–	Input pin for reference clock for TV-out support (3.3 volt signaling)
OSCOUT		VDDR3	VSS	Disabled	Buffered output of 14MHz reference clock to the IXP (3.3 volt signaling)
OSCIN	I	VDDR3	VSS	Disabled	14MHz Reference clock input from the External Clock chip (3.3 volt signaling)

CRT and TV Interface

Pin Name	Type	Power Domain	Ground Domain	Integrated Termination	Functional Description
RED	A-O	AVDD	AVSSN	–	Red for CRT monitor output
GREEN	A-O	AVDD	AVSSN	–	Green for CRT monitor output
BLUE	A-O	AVDD	AVSSN	–	Blue for CRT monitor output
Y	A-O	AVDD	AVSSN	–	SVID luminance output for TV out
C	A-O	AVDD	AVSSN	–	SVID chrominance output for TV out
COMP	A-O	AVDD	AVSSN	–	Composite video TV output
DACHSYNC	A-O	VDDR3	VSS	50kΩ programmable: PU/PD/none	Display Horizontal Sync
DACVSYNC	A-O	VDDR3	VSS	50kΩ programmable: PU/PD/none	Display Vertical Sync
RSET	Other	N/A	AVSSQ	–	DAC internal reference to set full scale DAC current through 1% resistor to AVSS
DACSCL	I/O	VDDR3	VSS	50kΩ programmable: PU/PD/none	I2C clock for VGA interface (to video monitor)
DACSDA	I/O	VDDR3	VSS	50kΩ programmable: PU/PD/none	I2C data for VGA interface (to video monitor)

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5.2 ATI RS480M North Bridge(3)

LVDS Interface

Pin Name	Type	Power Domain	Ground Domain	Integrated Termination	Functional Description
TXOUT_U0N	O	LVDDR18A	LVSSR	None	LVDS upper data channel 0 (-) Transmitting at a bit rate of 7x pixel clock, up to 85MHz pixel clock. Only used in dual-channel LVDS mode
TXOUT_U0P	O	LVDDR18A	LVSSR	None	LVDS upper data channel 0 (+) Transmitting at a bit rate of 7x pixel clock, up to 85MHz pixel clock. Only used in dual-channel LVDS mode.
TXOUT_U1N	O	LVDDR18A	LVSSR	None	LVDS upper data channel 1 (-) Transmitting at a bit rate of 7x pixel clock, up to 85MHz pixel clock. Only used in dual-channel LVDS mode.
TXOUT_U1P	O	LVDDR18A	LVSSR	None	LVDS upper data channel 1 (+) Transmitting at a bit rate of 7x pixel clock, up to 85MHz pixel clock. Only used in dual-channel LVDS mode.
TXOUT_U2N	O	LVDDR18A	LVSSR	None	LVDS upper data channel 2 (-) Transmitting at a bit rate of 7x pixel clock, up to 85MHz pixel clock. Only used in dual-channel LVDS mode.
TXOUT_U2P	O	LVDDR18A	LVSSR	None	LVDS upper data channel 2 (+) Transmitting at a bit rate of 7x pixel clock, up to 85MHz pixel clock. Only used in dual-channel LVDS mode.
TXOUT_U3N	O	LVDDR18A	LVSSR	None	LVDS upper data channel 3 (-) Transmitting at a bit rate of 7x pixel clock, up to 85MHz pixel clock. Only used in dual-channel LVDS mode.
TXOUT_U3P	O	LVDDR18A	LVSSR	None	LVDS upper data channel 3 (+) Transmitting at a bit rate of 7x pixel clock, up to 85MHz pixel clock. Only used in dual-channel LVDS mode.
TXCLK_UN	O	LVDDR18A	LVSSR	None	LVDS upper clock channel (-) Transmitting at pixel clock rate, up to 85MHz pixel clock. Only used in dual-channel LVDS mode.
TXCLK_UP	O	LVDDR18A	LVSSR	None	LVDS upper clock channel (+) Transmitting at pixel clock rate, up to 85MHz pixel clock. Only used in dual-channel LVDS mode.

LVDS Interface (Continued)

Pin Name	Type	Power Domain	Ground Domain	Integrated Termination	Functional Description
TXOUT_L0N	O	LVDDR18A	LVSSR	None	LVDS lower data channel 0 (-) Transmitting at a bit rate of 7x pixel clock, up to 85MHz pixel clock. This channel is used as the transmitting channel in single channel LVDS mode.
TXOUT_L0P	O	LVDDR18A	LVSSR	None	LVDS lower data channel 0 (+) Transmitting at a bit rate of 7x pixel clock, up to 85MHz pixel clock. This channel is used as the transmitting channel in single channel LVDS mode.
TXOUT_L1N	O	LVDDR18A	LVSSR	None	LVDS lower data channel 1 (-) Transmitting at a bit rate of 7x pixel clock, up to 85MHz pixel clock. This channel is used as the transmitting channel in single channel LVDS mode.
TXOUT_L1P	O	LVDDR18A	LVSSR	None	LVDS lower data channel 1 (+) Transmitting at a bit rate of 7x pixel clock, up to 85MHz pixel clock. This channel is used as the transmitting channel in single channel LVDS mode.
TXOUT_L2N	O	LVDDR18A	LVSSR	None	LVDS lower data channel 2 (-) Transmitting at a bit rate of 7x pixel clock, up to 85MHz pixel clock. This channel is used as the transmitting channel in single channel LVDS mode.
TXOUT_L2P	O	LVDDR18A	LVSSR	None	LVDS lower data channel 2 (+) Transmitting at a bit rate of 7x pixel clock, up to 85MHz pixel clock. This channel is used as the transmitting channel in single channel LVDS mode.
TXOUT_L3N	O	LVDDR18A	LVSSR	None	LVDS lower data channel 3 (-) Transmitting at a bit rate of 7x pixel clock, up to 85MHz pixel clock. This channel is used as the transmitting channel in single channel LVDS mode.
TXOUT_L3P	O	LVDDR18A	LVSSR	None	LVDS lower data channel 3 (+) Transmitting at a bit rate of 7x pixel clock, up to 85MHz pixel clock. This channel is used as the transmitting channel in single channel LVDS mode.

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5.2 ATI RS480M North Bridge(4)

LVDS Interface (Continued)

Pin Name	Type	Power Domain	Ground Domain	Integrated Termination	Functional Description
TXCLK_LN	O	LVDDR18A	LVSSR	None	LVDS lower clock channel (-) Transmitting at pixel clock rate, up to 85MHz pixel clock. This channel is used as the transmitting channel in single channel LVDS mode.
LPVSS	Gnd	–	–	–	LVDS PLL macro ground pin.
LVDDR18D	Pwr	–	–	–	1.8V LVDS Digital Power, used for the digital portions of the LVDS transmitter.
LVSSR	Gnd	–	–	–	LVDS IO ground pin.
LVDS_BLON	I/O	VDDR3	VSS	50kΩ programmable: PU/PD/none	Digital panel backlight brightness control. Active high. It controls backlight on/off or acts as PWM output to adjust brightness. If LVDS_GEN_CNTL.LVDS_BL_MOD_EN = 0, the pin controls backlight on/off. Otherwise, it is the PWM output to adjust the brightness. LVDS_GEN_CNTL.LVDS_BL_MOD_LEVEL can be used to control the backlight level (256 steps) by means of pulse width modulation. The duty cycle of the backlight signal can be set through the LVDS_GEN_CNTL.LVDS_BL_MOD_LEVEL bits. For example, setting these bits to a value of 32 will set the on-time to 32/256*(1/f) and the off-time to (256-32)/256*(1/f), where f is the XTALIN frequency and is typically 14MHz. Note that the PWM frequency can range from 5Hz to 50KHz and is set by LVDS_PWM_CNTL.PWM_CLK_CONF. For more information, refer to the Register Reference Manual. In CPIS mode, LVDS_BLON is VARY_BL as defined in CPIS. PWM mode should be enabled. LVDS_BLEN should be connected to ENA_BL, which turns the backlight AC inverter on/off.

LVDS Interface (Continued)

Pin Name	Type	Power Domain	Ground Domain	Integrated Termination	Functional Description
TXCLK_LP	O	LVDDR18A	LVSSR	None	LVDS lower clock channel (+) Transmitting at pixel clock rate, up to 85MHz pixel clock. This channel is used as the transmitting channel in single channel LVDS mode.
LPVDD	Pwr	–	–	–	Power for LVDS PLL macro (1.8V).
LVDDR18A	A-Pwr	–	–	–	1.8V LVDS Analog Power, used for the output stage of the transmitter. This power supply needs to be adequately filtered to prevent noise injection.
LVDS_DIGON	I/O	VDDR3	VSS	50kΩ programmable: PU/PD/none	Control Panel Digital Power On/Off. Active high.
LVDS_BLEN	I/O	VDDR3	VSS	50kΩ programmable: PU/PD/none	Enables Backlight for CPIS compliant LVDS panels. Active high.Controlled by the hardware power up/down sequencer. For more details, refer to *Figure 4-3, "LCD Panel Power Up/Down Timing," on page 4-* 3.

1 x 16 Lane PCI Express Interface for External Graphics

Pin Name	Type	Power Domain	Ground Domain	Integrated Termination	Functional Description
GFX_TX[15:0]P, GFX_TX[15:0]N	O	VDDA_18	VSSA	50Ω between complements	Transmit Data Differential Pairs. Connect to external connector for an external graphics card on the motherboard (if implemented).
GFX_RX[15:0]P, GFX_RX[15:0]N	I	VDDA_18	VSSA	50Ω between complements	Receive Data Differential Pairs. Connect to external connector for an external graphics card on the motherboard (if implemented).
GFX_CLKP, GFX_CLKN	I/O	VDDA_18	VSSA	50Ω between complements	Clock Differential Pairs. Connect to external clock generator when an external graphics card is implemented.

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5.2 ATI RS480M North Bridge(5)

Power Management Pins

Pin Name	Type	Power Domain	Ground Domain	Functional Description
SYSRESET#	I	VDDR3	VSS	Global Hardware Reset. This signal comes from the south bridge.
SUS_STAT#	I	VDD_18	VSS	Disable internal clock tree during S1-S3 states. Keep frame buffer side port memory, when installed, in self refresh mode when system is in S3 mode. (NOTE: Signaling level is 1.8V)
POWERGOOD	I	VDDR3	VSS	Input from the motherboard signifying that the power to the RS480M is up and ready. Signal High means all power planes are valid. It is not observed internally until it has been high for more than 6 consecutive REFCLK cycles. The rising edge of this signal is deglitched. Needs an external pull-up to a minimum of 2.5V.
LDTSTOP#	I	VDDR3	VSS	HyperTransport Stop. Input from the IXP to enable and disable the HyperTransport link during system state transitions. For systems requiring power management. Single-ended.
ALLOW_LDTSTOP	O	VDDR3	VSS	Output going to the IXP to allow LDTSTOP assertions: 1 = LDTSTOP# can be asserted 0 = LDTSTOP# has to be de-asserted

GDDR Side-Port Memory Interface (Continued)

Pin Name	Type	Power Domain	Ground Domain	Integrated Termination	Functional Description
MEM_COMPP, MEM_COMPN	Other	VDD_MEM	VSS	None	Memory interface compensation pins for N and P channel devices. Connect through resistors to VDD_MEM and ground respectively (refer to the reference schematics for the proper resistor values).
MEM_VREF	Other	–	VSS	None	Reference voltage(1.25V typ. for SSTL-2 / 0.5 * VDD, 1.5V typ. for SSTL-3 / 0.45 * VDD). **Note:** If the differential signaling interface is not used, this pin must be connected to the memory IO's VDD_MEM (1.8 or 2.5V).
MEM_CAP[2:1]	Other	VDD_MEM	VSS	None	These pads provide off-chip filtering of the VDD_MEM power. This is required for 2.5V support of GDDR.

DVO Interface

Pin Name	DVO Function	Type	Functional Description
MEM_DQ52	DVO_D0	O	DVO Data for panel
MEM_DQ49	DVO_D1	O	DVO Data for panel
MEM_DQ50	DVO_D2	O	DVO Data for panel
MEM_DQ51	DVO_D3	O	DVO Data for panel
MEM_DQ39	DVO_D4	O	DVO Data for panel
MEM_DQ48	DVO_D5	O	DVO Data for panel
MEM_DQ38	DVO_D6	O	DVO Data for panel
MEM_DQ37	DVO_D7	O	DVO Data for panel
MEM_DQ36	DVO_D8	O	DVO Data for panel
MEM_DQ35	DVO_D9	O	DVO Data for panel
MEM_DQ34	DVO_D10	O	DVO Data for panel
MEM_DQ33	DVO_D11	O	DVO Data for panel
MEM_DQ53	DVO_DE	O	DVO Display Enable signal for panel
MEM_DQ54	DVO_HSYNC	O	DVO Horizontal Sync signal for panel
MEM_DQ55	DVO_VSYNC	O	DVO Vertical Sync signal for panel
MEM_DQS4P	DVO_CLK *	O	DVO clock
MEM_DQS4N	DVO_CLK# *	O	DVO clock
TMDS_HPD	DVO_HPD **	I	"Hot Plug" panel detection input pin that monitors if the voltage is greater than 2.0V on the hot-plugging line
I2C_CLK	DVO_DVI_CLK	I/O	DDC clock for the DVO interface
DDC_DATA	DVO_DVI_DATA	I/O	DDC data for the DVO interface

* The clock signal and its inverses are required for implementation of the DVO interface.
** Optional for the implementation of the DVO interface.

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5.2 ATI RS480M North Bridge(6)

Miscellaneous Pins

Pin Name	Type	Power Domain	Ground Domain	Integrated Termination	Functional Description
BMREQ#	Out	VDDR3	VSS	–	This pin is connected to the south bridge. This signal indicates that there is a DMA request from a PCI Express Bus device.
I2C_CLK	I/O	VDDR3	VSS	–	I2C interface clock signal. Can also be used simultaneously as DDC interface clock for the LVDS interface or the external DVO interface. It can also be used as GPIO.
I2C_DATA	I/O	VDDR3	VSS	–	I2C interface data signal. Can also be used as GPIO.
DDC_DATA	I/O	VDDR3	VSS	50kΩ programmable: PU/PD/none	Pin for additional DDC Data Channel for the LVDS interface or the external DVO interface. It makes use of I2C_CLK to create an I2C interface. Can also be used as GPIO.
STRP_DATA	I/O	VDDR3	VSS	–	I2C interface data signal for external EEPROM based strap loading. See the RS480M Strap Document for details on the operation. Can also be used as GPIO or NB Voltage throttling on mobile platforms.
TESTMODE	I	VDDR3	VSS	–	When High, puts the RS480M in Tester mode and disables the RS480M from operating normally.
THERMALDIODE_P, THERMALDIODE_N	A-O	–	–	–	Diode connections to external SM Bus microcontroller for monitoring IC thermal characteristics.
TMDS_HPD	I	VDDR3	VSS	PU	TMDS Hot Plug Detect. “Hot Plug” panel detection input pin that monitors if the voltage is greater than 2.0V on the hot-plugging line.
DFT_GPIO[5:0]	I/O	VDDR3	VSS	PU	GPIO for DFT use. **Note:** Because DFT_GPIO[5, 1:0] are used as strap pins (see *Table 3-15, “Strap Definitions for the RS480M”*), they cannot be used for general GPIO functions.

Strap Definitions for the RS480M

Strap Function	Strap Pin	Description
LOAD_MEM_STRAPS#	DFT_GPIO5*	Selects loading of straps from MEM_DQ pins for debug bus 0 : Capture MEM_DQ pins for debug bus straps. **1 : Use Default Values (Default)** Note : More information about straps on the MEM_DQ pins is available in the Debug Bus specification.
HT_FREQ_OVERRIDE	DFT_GPIO[4:3]	Overrides HT Link frequency at power up 00 : Reserved – for testing only. 01 : Reserved – for testing only. 10 : Reserved – for testing only. **11 : 200 MHz (Default)**
HT_WIDTH_OVERRIDE	DFT_GPIO2	Override HT Link width at power up 0 : Reserved – for testing only. **1 : 8 Bit Link (Default)**
LOAD_ROM_STRAPS#	DFT_GPIO1*	Selects loading of strap values from EEPROM 0: I2C master can load strap values from EEPROM if connected, or use default values if not connected **1: Use Default Values (Default)**
SIDE_PORT_EN#	DFT_GPIO0*	Indicates if memory side port is available or not 0: Memory side port available **1: Memory side port NOT available (Default)**

Note: Strap pins marked by “*” cannot be used for general GPIO functions.

PCI Express Interface for Miscellaneous PCI Express Signals

Pin Name	Type	Power Domain	Ground Domain	Functional Description
PCE_ISET	Other	VDDA_18	VSSA	Current Calibration for for Rx Channel
PCE_TXISET	Other	VDDA_18	VSSA	Current Calibration for for Tx Channel
PCE_NCAL	Other	VDDA_18	VSSA	N channel Driver Compensation Calibration for Rx and Tx Channels
PCE_PCAL	Other	VDDA_18	VSSA	P channel Driver Compensation Calibration for Rx and Tx Channels

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5.2 ATI RS480M North Bridge(7)

Power Pins

Pin Name	Voltage	Pin Count	Ball Reference	Comments
AVDD	2.5V or 3.3V	2	B27, C27	Dedicated power for the DAC. Effort should be made at the board level to provide as clean a power as possible to this pin to avoid noise injection, which can affect display quality. Adequate decoupling should be provided between this pin and AVSS.
AVDDQ	1.8V	1	E24	DAC Bandgap Reference Voltage
AVDDDI	1.8V	1	C24	Dedicated digital power for the DAC
VDD_CORE	1.2V	47	A22, B21, B22, C21, C22, D21, D22, E21, E22, F21, F22, G21, G22, H21, H22, M13, M15, M17, M19, N12, N14, N16, N18, P13, P15, P17, P19, R12, R14, R16, R18, T13, T15, T17, T19, U12, U14, U16, U18, V13, V15, V17, V19, W12, W14, W16, W18	Core power
VDD_18	1.8V	3	AC15, AC17, H15	I/O Transform Power for memory, CPU, and GPIO sections.
VDDA_12	1.2 V	14	AA7, AA8, B1, F9, G7, G8, G9, H9, J7, J8, N7, N8, U7, U8	PCI Express interface main I/O power
VDDA_18	1.8V	13	AC7, AC8, AE6, AF5, AF6, AG4, AK2, L7, L8, R7, R8, W7, W8	PCI Express interface power for output Tx stage
VDD_MEM	1.8 / 2.5V	18	AC10, AC12, AC14, AC18, AC20, AC22, AD10, AD12, AD14, AD15, AD18, AD20, AD22, AE30, AK11, AK23, AK28, AK4	Isolated IO power for memory interface

Power Pins (Continued)

Pin Name	Voltage	Pin Count	Ball Reference	Comments
VDD_MEMCK	1.8 / 2.5V	1	AH15	IO Power for memory clocks
VDD_HT	1.2V	31	A23, A29, AA23, AA27, AB23, AB24, AB27, AC30, B23, C23, D23, E23, F23, G23, G27, H23, H27, J23, J27, K23, K24, K27, N27, P24, P27, U23, U27, V23,V24,V27,W23	IO power for HyperTransport interface
VDDR3	3.3V	2	H12, H13	IO power for the following I/O pads: OSC, POWERGOOD, SYSRESET#
LPVDD	1.8V	1	E18	Power for LVDS PLL macro.
LVDDR18D	1.8V	1	E19	1.8V LVDS Digital Power
LVDDR18A	1.8V	2	G20, H20	1.8V LVDS Analog Power
PLLVDD	1.8V	1	A14	Power for PLL
HTPVDD	1.8V	1	M23	Power for HyperTransport interface PLL
MPVDD	1.8V	1	AJ15	Power for memory interface PLL
Total Power Pin Count		140		

1 x 2 Lane A-Link Express Interface for IXP

Pin Name	Type	Power Domain	Ground Domain	Integrated Termination	Functional Description
SB_TX[1:0]P, SB_TX[1:0]N	O	VDDA_18	VSSA	50Ω between complements	Transmit Data Differential Pairs. Connect to the corresponding Receive Data Differential pairs on the IXP.
SB_RX[1:0]P, SB_RX[1:0]N	I	VDDA_18	VSSA	50Ω between complements	Receive Data Differential Pairs. Connect to the corresponding Transmit Data Differential pairs on the IXP.
SB_CLKP, SB_CLKN	I/O	VDDA_18	VSSA	50Ω between complements	Clock Differential Pair. Connect to an external clock generator on the motherboard.

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5.2 ATI RS480M North Bridge(8)

Ground Pins

Pin Name	Pin Count	Ball Reference	Comments
AVSSN	2	D25, D26	Dedicated analog ground for the DAC.
AVSSQ	1	D24	Dedicated ground for the Band Gap Reference. Effort should be made at the board level to provide as clean a ground as possible to this pin to avoid noise injection, which can affect display quality. Adequate decoupling should be provided between this pin and AVDD.
LVSSR	8	E20, F18, F19, F20, G18, G19, H18, H19	LVDS Interface ground pin. For Desktop: bond it to VSS (core ground) on the substrate
VSS	131	AA28, AB25, AB28, AC11, AC13, AC16, AC19, AC21, AC23, AC27, AC9, AD11, AD13, AD16, AD17, AD19, AD21, AD23, AD24, AD25, AD27, AD28, AD29, AD7, AD8, AD9, AE26, AE27, AF30, AG12, AG15, AG18, AG21, AG24, AG27, AG5, AG6, AG9, AJ30, AK10, AK22, AK29, AK5, B30, C28, D10, D11, D12, D15, D9, E15, E16, E26, E9, F15, F16, F24, F25, F26, F27, F28, G10, G11, G12, G13, G14, G15, G16, G17, G28, G30, H10, H11, H14, H16, H17, H24, H28, J28, K25, K28, L27, M12, M14, M16, M18, M24, M27, N13, N15, N17, N19, N28, P12, P14, P16, P18, P25, P28, R13, R15, R17, R19, R23, R27, T12, T14, T16, T18, T23, T24, T27, U13, U15, U17, U19, U28, V12, V14, V16, V18, V25, V28, W13, W15, W17, W19, W27, Y23, Y24, Y27	Common Ground

Ground Pins (Continued)

Pin Name	Pin Count	Ball Reference	Comments
AVSSDI	1	B24	Dedicated digital ground for the DAC (1.8V)
LPVSS	1	F17	LVDS PLL macro ground pin. For Desktop: bond it to VSS (core ground) on the substrate
VSSA	68	A2 AA3, AA5, AA6, AB3, AB7, AB8, AD3, AD5, AD6, AE3, AE5, AF3, AG3, AJ1, B4, C2, C3, C4, C5, C6, C7, C8, C9, D3, D6, E5, E6, F3, F5, F6, F7, F8, G3, H7, H8, J3, J5, J6, K3, K7, K8, L5, L6, M3, M5, M6, M7, M8, N3, P7, P8, R3, R5, R6, T3, T7, T8, U5, U6, V3, V5, V6, V7, V8, W3, Y7, Y8	PCI Express Interface Ground
PLLVSS	1	B14	Ground pin for PLL
HTPVSS	1	L23	Ground pin for HyperTransport interface PLL
MPVSS	1	AJ14	Ground pin for memory interface PLL
Total Ground Pin Count	215		

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5.3 ULI M1573M South Bridge(1)

PCI Interface

Pin Name	I/O Type	Description
PCICLK	I	**PCI Clock for Internal PCI Interface.** This is a PCI clock input that is controlled by clock generator.
PCI_OUTCLK[9:0]	O	**PCI Clock Output.** This is PCI output clocks for PCI device.
PCICLK_FBKO	O	**PCI Clock Feedback Out Signal.** This is a PCI clock feedback input path.
PCICLK_FBKI	I	**PCI Clock Feedback In Signal.** This is a PCI clock feedback input path.
PCIREQ#[3:0] PCIREQ#[6:4]/ RUNGPI[6:4]	I	**PCI Requests.** PCI master requests for the PCI bus ownership. M1573 supports up to 7 masters on the PCI bus. PCIREQ#[0] is programmable to have the highest priority of the PCI arbitration for supporting PCI-based 1394 controller. PCIREQ#[6:4] can be configured as RUNGPI.
PCIGNT#[3:0] PCIGNT#[6:4]/ RUNGPO[6:4]	O	**PCI Grants.** PCI master be granted for the PCI bus ownership. M1573 supports up to 7 masters on the PCI bus. PCIGNT#[6:4] can be configured as RUNGPO.
PIRQ#[D:A] PIRQ#[H:E]/ RUNGPI[10:7]	I	**PCI Interrupt Requests.** In legacy 8259 mode, PIRQ#[H:A] signals can be routed to legacy IRQs through the routing table defined in the PCI-legacy device configuration registers 4Bh – 48h. In APIC mode, PIRQ#[A] is connected to entry-16, PIRQ#[B] to entry-17, PIRQ#[C] to entry-18, PIRQ#[D] to entry-19, PIRQ#[E] is connected to entry-20, PIRQ#[F] to entry-21, PIRQ#[G] to entry-22, and PIRQ#[H] to entry-23. PIRQ#[H:E] can be configured as RUNGPI.
CLKRUN#/ RUNGPO[9]	I/O O	**PCI Clock Run control.** This signal is used to support PCI Clock Run CLKRUN# protocol. It can also be configured as RUNGPO.
AD[31:0]	I/O	**PCI Address and Data Multiplexed Bus.** During the first clock of a PCI transaction, AD[31:0] contain a physical address. During subsequent clocks, AD[31:0] contain data.
CBE#[3:0]	I/O	**PCI Bus Command and Byte Enable.** During address phase, CBE#[3:0] define the Bus Command. During the data phase, CBE#[3:0] define the Byte Enables.

PCI Interface (Continued)

Pin Name	I/O Type	Description
FRAME#	I/O	**PCI Cycle Frame.** Cycle Frame is driven by current initiator to indicate the beginning and duration of a PCI access.
IRDY#	I/O	**PCI Initiator Ready.** Initiator Ready indicates the initiator's ability to complete the current data phase of the transaction.
TRDY#	I/O	**Target Ready.** Target Ready indicates the target's ability to complete the current data phase of the transaction.
DEVSEL#	I/O	**PCI Device Select.** This signal indicates that the target device has decoded the address as its own cycle.
STOP#	I/O	**Cycle Stop Request.** Cycle Stop indicates the target is requesting the master to stop the current transaction.
SERR#	I	**PCI System Error.** This signal may be pulsed active by any agent that detects a system error condition. When SERR# is sampled low, the M1573 will assert NMI to generate non-maskable interrupt to CPU.
PAR	I/O	**PCI Parity Signal.** PAR is an Even Parity and is calculated on AD[31:0] and CBE#[3:0].
PCIRST#	O	**PCI Bus Reset.** This is an output signal to reset the entire PCI Bus.
PME#	I/O	**PCI Power Management Event.** This signal is used by a PCI device to request a change of its power consumption state. Typically, an active PME# issued by a device is to wake up a power saving state of device or system to the fully operational state.

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5.3 ULI M1573M South Bridge(2)

LAN Interface

Pin Name	I/O Type	Description
MII Interface		
MII_COL	I	**Collision Detect.** Asserted high to indicate detection of collision conditions in 10Mbps and 100Mbps Half Duplex modes. In Full Duplex mode, this signal is always logic 0. There is no heartbeat function in Full-Duplex mode.
MII_CRS	I	**Carrier Sense.** This pin is asserted high to indicate the presence of carrier due to receive or transmit activities in 10BASE-T or 100BASE-TX Half Duplex modes. In Repeater, when Full Duplex or Loopback mode is a logic 1, it indicates the presence of carrier due only to receive activity.
MII_RXER	I	**Receiver Error.** Receiver error asserts when a data decoding error is detected by the external PHY device.
MII_RXC	I	**Receive Clock.** Provides the recovered receive clock for different modes of operation: - 25MHz nibble clock in 100Mbps mode - 2.5MHz nibble clock in 10Mbps nibble mode
MII_RXD[3:0]	I	**Receive Data.** Nibble wide receive data (synchronous to RX_CLK – 25MHz for 100BASETX mode, 2.5MHz for 10BASE-T nibble mode).
MII_RXDV	I	**Receive Data Valid.** Data valid is asserted by the external PHY device when receive data is present on the RXD lines and is de-asserted at the end of packet.
MII_TXC	I	**Transmit Clock.** Transmit clock input from the PHY. - 25MHz nibble transmit clock derived from transmit Phase Locked Loop(TX PLL) in 100BASE-TX mode - 2.5MHz transmit clock in 10BASE-T nibble mode
MII_TXD[3:0]	O	**Transmit Data.** Transmit data output pins for nibble data from the MII in 100Mbps or 10Mbps nibble mode (25 MHz for 100Mbps mode, 2.5MHz for 10Mbps nibble mode).
MII_TXEN	O	**Transmit Enable.** Active high output indicates the presence of valid nibble data on TXD[3:0] for both 100Mbps or 10Mbps nibble mode.

LAN Interface (Continued)

Pin Name	I/O Type	Description
MII Interface		
MII_MDC	O	**Management Data Clock.** Synchronous clock to the MDIO management data input/output serial interface which is asynchronous to transmit and receive clocks. The maximum clock rate is 2.5MHz.
MII_MDIO	I/O	**Management Data I/O.** Bi-directional management instruction/data signal that may be sourced by the station management entity or the PHY. This pin requires a 4.7Kohm pull-up resistor.
EEPROM Interface		
EEDO	O	**Serial EEPROM data output** It is connected to DI(data input) pin of the serial EEPROM and used to transfer the data from the south bridge to the EEPROM. The Serial ROM is used to auto-load Ethernet GUID.
EEDI	I	**Serial EEPROM data input** It is connected to DO(data output) pin of the serial EEPROM and used to transfer the data from the EEPROM to south bridge. The Serial ROM is used to auto-load Ethernet GUID.
EECS	O	**EEPROM Chip Select.** This pin will enable the EEPROM during loading of the Configuration Data.
EECK	O	**EEPROM Serial Clock.** This pin provides the clock for the EEPROM data transfer.

SMBus Interface

Pin Name	I/O Type	Description
SMB_ALERT#/ RSMGPI[10]	I	SMBus Alert SMBus devices can signal alert to SMBus host by asserting this signal to generate SMI or to wake up the system. This pin can be configured as RSMGPI.
SMB_CLK	I/OD	SMBus Clock SMBus clock signal driven by cycle initiator.
SMB_DATA	I/OD	SMBus Data SMBus data signal carries serial data information based on SMCLK.

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5.3 ULI M1573M South Bridge(3)

IDE Interface

Pin Name	I/O Type	Description
Parallel ATA Interface		
PIDEA[2:0]	O	**Primary Channel IDE ATA Address Bus.** These are the Address pins connected to Primary Channel.
PIDECS1#	O	**Primary Channel 0 IDE Chip Select 1.** This is the Chip Select 1 command output pin to enable the Primary IDE device to watch the Read/Write Command.
PIDECS3#	O	**Primary Channel 1 IDE Chip Select 3.** This is the Chip Select 3 command output pin to enable the Primary IDE device to watch the Read/Write Command.
PIDED[15:0]	I/O	**Primary IDE ATA Data Bus.** These are the Data pins connected to Primary Channel.
PIDEDAK#	O	**Primary IDE DACK# for IDE Master.** This is the output pin to grant the Primary Channel IDE DMA request to begin the IDE Master Transfer in DMA or Ultra-33/66/100/133 mode.
PIDEDRQ	I	**Primary IDE DMA Request for IDE Master.** This is the input pin from the Primary Channel IDE DMA request to do the IDE Master Transfer. It will be active high in DMA or Ultra-33/66/100/133 mode and always be inactive low in PIO mode.
PIDEIOR#	O	**Primary IDE IOR# Command.** This is the IOR# command output pin to notify the Primary IDE device to assert the Read Data in PIO and DMA mode. In Ultra-33/66/100/133 mode, this pin has different functions. In read cycle, this pin is used by IDE Controller to notify IDE device as DMA Ready (DDMARDY#). In write cycles, IDE Controller will drive this signal as Data Strobe (DSTROBE) to use by IDE device to strobe the output data.
PIDEIOW#	O	**Primary IDE IOW# Command.** This is the IOW# command output pin to notify the Primary IDE device that the available Write Data is already asserted by IDE Controller in PIO and DMA mode. In Ultra-33/66/100/133 mode, this pin is driven by IDE Controller to force IDE device to terminate current transaction. After receiving this input, IDE device will de-assert DRQ to STOP current transaction.
PIDEIRQ	I	**Primary IDE IRQ Input1.** This is a steer-able Interrupt input, the M1573 will provide a Routing Mechanism to route this Interrupt to any 8259 input for built-in IDE Controller.

IDE Interface (Continued)

Pin Name	I/O Type	Description
Parallel ATA Interface		
PIDERDY	I	**Primary IDE Ready.** This is the input pin from the Primary IDE Channel to indicate the IDE device is ready to terminate the IDE command in PIO mode. The IDE device can de-assert this input (logic 0) to expand the IDE command if the device is not ready. In Ultra-33/66/100/133 mode, this pin has different functions. In read cycles, IDE device will drive this signal as Data Strobe (DSTROBE) to use by IDE controller to strobe the input data. In write cycle, this pin is used by IDE device to notify IDE Controller as DMA Ready (DDMARDY#).
SIDEA[2:0]	O	**Secondary IDE ATA Address Bus.** These are the Address pins connected to Secondary Channel.
SIDECS1#	O	**Secondary Channel 0 IDE Chip Select 1.** This is the Chip Select 1 command output pin to enable the Secondary IDE device to watch the Read/Write Command.
SIDECS3#	O	**Secondary Channel 1 IDE Chip Select 3.** This is the Chip Select 3 command output pin to enable the Secondary IDE device to watch the Read/Write Command.
SIDED[15:0]	I/O	**Secondary IDE ATA Data Bus.** These are the Data pins connected to Secondary Channel.
SIDEDAK#	O	**Secondary IDE DACK# for IDE Master.** This is the output pin to grant the Secondary Channel IDE DMA request to begin the IDE Master Transfer in DMA or Ultra-33/66/100/133 mode.
SIDEDRQ	I	**Secondary IDE DMA Request for IDE Master.** This is the input pin from the Secondary Channel IDE DMA request to do the IDE Master Transfer. It will be active high in DMA or Ultra-33/66/100/133 mode and always be inactive low in PIO mode.
SIDEIOR#	O	**Secondary IDE IOR# Command.** This is the IOR# command output pin to notify the Secondary IDE device to assert the Read Data in PIO and DMA mode. In Ultra-33/66/100/133 mode, this pin has different functions. In read cycle, this pin is used by IDE Controller to notify IDE device as DMA Ready (DDMARDY#). In write cycle, IDE Controller will drive this signal as Data Strobe (DSTROBE) to use by IDE device to strobe the output data.

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5.3 ULI M1573M South Bridge(4)

IDE Interface (Continued)

Pin Name	I/O Type	Description
Parallel ATA Interface		
SIDEIOW#	O	**Secondary IDE IOW# Command.** This is the IOW# command output pin to notify the Secondary IDE device that the available Write Data is already asserted by IDE Controller in PIO and DMA mode. In Ultra-33/66/100/133 mode, this pin is driven by IDE Controller to force IDE device to terminate current transaction. After receiving this input, IDE device will de-assert DRQ to STOP current transaction.
SIDEIRQ	I	**Secondary IDE IRQ Input2.** This is a steer-able Interrupt input, the M1573 will provide a Routing Mechanism to route this Interrupt to any 8259 input for built-in IDE Controller.
SIDERDY	I	**Secondary IDE Ready.** This is the input pin from the Secondary IDE Channel to indicate the IDE device is ready to terminate the IDE command in PIO mode. The IDE device can de-assert this input (logic 0) to expand the IDE command if the device is not ready. In Ultra-33/66/100/133 mode, this pin has different functions. In read cycles, IDE device will drive this signal as Data Strobe (DSTROBE) to use by IDE Controller to strobe the input data. In write cycles, this pin is used by IDE device to notify IDE Controller as DMA Ready (DDMARDY#).
Serial ATA Interface		
SATA0_TX0P, SATA0_TX0N	O	Serial-ATA0 port0 Transmission signal pair
SATA0_RX0P, SATA0_RX0N	I	Serial-ATA0 port0 Receiving signal pair
SATA0_TX1P, SATA0_TX1N	O	Serial-ATA0 port1 Transmission signal pair
SATA0_RX1P, SATA0_RX1N	I	Serial-ATA0 port1 Receiving signal pair
SATA0_REXT	I	SATA0 External Resistor reference for impendence adjustment.
SATA1_TX0P, SATA1_TX0N	O	Serial-ATA1 port0 Transmission signal pair
SATA1_RX0P, SATA1_RX0N	I	Serial-ATA1 port0 Receiving signal pair
SATA1_TX1P, SATA1_TX1N	O	Serial-ATA1 port1 Transmission signal pair

IDE Interface (Continued)

Pin Name	I/O Type	Description
Serial ATA Interface		
SATA1_RX1P, SATA1_RX1N	I	Serial-ATA1 port1 Receiving signal pair
SATA1_REXT	I	SATA1 External Resistor reference for impendence adjustment.
SATA_GPI[3:0]/ RUNGPI[22:19]	I	Serial-ATA General Purpose IO. It can be configured as RUNGPI.
SATA_GPO[3:0]/ RUNGPO[28:25]	O	Serial-ATA1 General Purpose IO. It can be configured as RUNGPO.
SATA_LED	OD	Serial-ATA LED

Host PCI Express Interface

Pin Name	I/O Type	Description
PE_RefClkP, PE_RefClkN	I	**Differential reference clock signals.** Clock frequency ranges from 100 MHz.
Lane Transmit Interface		
SB_TAP, SB_TAN	O	Differential transmit outputs for lane A
SB_TBP, SB_TBN	O	Differential transmit outputs for lane B
SB_TCP, SB_TCN	O	Differential transmit outputs for lane C
SB_TDP, SB_TDN	O	Differential transmit outputs for lane D
Lane Receive Interface		
SB_RAP, SB_RAN	I	Differential receive inputs for lane A
SB_RBP, SB_RBN	I	Differential receive inputs for lane B
SB_RCP, SB_RCN	I	Differential receive inputs for lane C
SB_RDP, SB_RDN	I	Differential receive inputs for lane D
Reference Resistors		
REF	I	Used to connect a (2.4K? +/- 1%) external resistor to VSS to provide a reference current for the driver and equalization circuits

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5.3 ULI M1573M South Bridge(5)

Audio Interface

Pin Name	I/O Type	Description
AC-Link Signals		
ACZ_RST#	O	**AC97 Reset Signal.** This is the AC'97 Codec(s) master hardware reset signal output. **HD Audio Reset Signal.** This is the HD Audio Codec(s) master hardware reset signal output.
ACZ_SYNC	O	**AC'97 SYNC Signal.** This signal is used for AC'97 48 KHz fixed rate sample sync. **HD Audio SYNC Signal.** This signal is used for HD Audio 48 KHz fixed rate sample sync.
ACZ_SDOUT	O	**AC'97 Serial Data Output Signal.** This signal is used for serial, time division multiplexing, AC'97 output stream to the Codec(s). **HD Audio Serial Data Output Signal.** This signal is used for serial, time division multiplexing, HD Audio output stream to the Codec(s).
ACZ_BITCLK	I/O	**AC97 Bit Clock Input Signal.** This signal is used for AC97 12.288 MHz serial data clock. **HD Audio Bit Clock Output Signal.** This signal is used for HD Audio 12.288 MHz serial data clock.
ACZ_SDATAIN[2:0]	I/O	**AC97 Serial Data Input[2:0].** These signals are used for serial, TDM (Time Division Multiplexing), AC'97 input stream from the Codecs. **HD Audio Serial Data Input[2:0].** These signals are used for serial, TDM (Time Division Multiplexing), HD Audio input stream from the Codecs.
ACB_RST#/ RSMGPO[10]	O	**AC97 LinkB Reset Signal.** This is the AC'97 Codec(s) master hardware reset signal output. This pin can be configured as RSMGPO.
ACB_SYNC / RUNGPO[23]	O	**AC'97 LinkB SYNC Signal.** This signal is used for AC'97 48 KHz fixed rate sample sync. This pin can be configured as RUNGPO.
ACB_SDOUT / RUNGPO[24]	O	**AC'97 Serial Data Output Signal.** This signal is used for serial, time division multiplexing, AC'97 output stream to the Codec(s). This pin can be configured as RUNGPO.
ACB_BITCLK / RUNGPI[18]	I	**AC97 LinkB Bit Clock Input Signal.** This signal is used for AC97 12.288 MHz serial data clock. This pin can be configured as RUNGPI.

Audio Interface (Continued)

Pin Name	I/O Type	Description
AC-Link Signals		
ACB_SDATAIN / RSMGPI[15]	I	**AC97 LinkB Serial Data Input.** These signals are used for serial, TDM (Time Division Multiplexing), AC'97 input stream from the CODEC. This pin can be configured as RSMGPI.
Audio Miscellaneous Interface		
VOL_UP#/ RUNGPI[11]	I	**Volume Up Control Signal for Audio.** This pin is used to tune up audio volume and connects to AC97 GPIO[1] input. This pin can be configured as RUNGPI.
VOL_DOWN#/ RUNGPI[12]	I	**Volume Down Control Signal for Audio.** This pin is used to down audio volume connects to AC97 GPIO[0] input. This pin can be configured as RUNGPI.
VOL_MUTE#/ RUNGPI[13]	I	**Volume Mute Control Signal for Audio.** This pin is used to mute audio and connects to AC97 GPIO[2] input. This pin can be configured as RUNGPI.

LPC Interface

Pin Name	I/O Type	Description
LFRAME#	O	**Low Pin Count FRAME# Signal.** This signal is the frame signal of Low Pin Count interface.
LAD[3:0]	I/O	**LAD[3:0].** These pins are address/data signals for Low-Pin-Count interface.
LDRQ[0]# LDRQ[1]#/ RUNGPI[14]	I	**Low Pin Count DMA Request Signal[1:0].** These pins are DMA request signals used by LPC devices. LDRQ[1]# can be configured as RUNGPI.

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5.3 ULI M1573M South Bridge(6)

PMU Interface

Pin Name	I/O Type	Description
ACPWR (Mobile Only) / RSMGPI[12]	I	**AC Power Plug-in Indication.** This active high input indicates the AC adapter is plugged in the mobile mode. This pin can be configured as RSMGPI.
AGPSTOP# (Mobile Only)	O	**Stop AGP Device Clock.** This signal is used by M1573 to indicate that the AGP clock will be stopped.
CLK32KO/ RSMGPO[8]	O	**32 KHz Clock Output for DRAM Refresh.** In S1 and S3 states, this output will send 32KHz clock to Memory controller to support suspend-mode DRAM refresh. In S4 and S5 states, this output will be driven low. This pin can be configured as RSMGPO.
CPUSTP#/ RUNGPO[7]	O	**CPU Clock Stop.** This output signal controls clock generator to stop the CPU Clock. This signal can be configured as RUNGPO.
LID (Mobile Only) / RSMGPI[14]	I	**LID Cover Switch.** The input indicates LID status of a mobile system and can issue SMI, SCI. This pin can be configured as RSMGPI.
LOWBAT# (Mobile Only) / RSMGPI[13]	I	**Battery Low Indication.** The input indicates the battery status for a mobile system. This pin can be configured as RSMGPI.
OFFCLKS1# / RSMGPO[16]	O	**Clock Generator OFF.** This output signal is used to power down the clock generator. This signal can be configured as RSMGPO.
OFFPWRS3# / RSMGPO[17]	O	**Power Off Control in S3.** This output is used to shut off all the non-required power when system gets into S3-S5 states. This signal can be configured as RSMGPO.
OFFPWRS4_S5# / RSMGPO[18]	O	**Power Off Control in S4/S5.** This output is used to shut off all the non-required power when system gets into S4-S5 states. This signal can be configured as RSMGPO.
PCISTP# / RUNGPO[8]	O	**PCI Clock Stop.** This output is used to control clock generator stopping the PCI Bus Clock. This signal can be configured as RUNGPO.
PWG	I	**Power-Good Input.** This signal indicates that system power is available and stable. M1573 uses this signal to generate reset sequence for the system.

PMU Interface (Continued)

Pin Name	I/O Type	Description
PWRBTN#	I	**Power Button Input.** This input is used to support the ACPI Power Button function. Both 4-second Override to Soft Off state and Resume from Suspend mode functions are supported.
RI	I	**Ring In.** This input connects to Modem Ring-in input to support ACPI Ring-in function. There exists a Ring counter to count the amount of Ring-In pulses for generating events.
RSMRST#	I	**Resume Circuit Reset Input.** The M1573 will activate internal reset signal to initialize the resume-region circuits.
SLPBTN# / RSMGPIL[0]	I	**Sleep Button Input.** This input is used to support the ACPI Sleep Button function. This signal can be configured as RSMGPIL.
SUSLED / RSMGPO[7]	O	**Suspend LED Output**. This output pin controls LED on/off and is served as suspend status indicator. This signal can be configured as RSMGPO.
THRM#	I	**Thermal Event Input.** THRM# is a triggered input and indicates that the external thermal detect circuits request for entering power management mode.
THRMTRIP#	I	**Thermal Trip.** This input is a hardware failsafe mechanism of CPU to avoid damages in thermal run-away situation. It's a 2.5V open-drain output from CPU.
PCIEX_WAKEUP#	I	**PCI Express Wakeup.** This signal is used by the PCI Express devices to wake up system from power suspend states.
DSPVRHI / RUNGPO[10]	O	**Deeper Sleep – Voltage Regulator High/Low Selection.** This signal is used to select the voltage regulator high/low voltage for the CPU normal/deeper sleep state, and can be optionally configured as RUNGPO.
SUSPEND# / RSMGPO[9]	O	**Suspend Status for North Bridge.** This output is used to request the north bridge to switch from normal DRAM refresh to suspend DRAM refresh mode. This signal can be configured as RSMGPO.

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5.3 ULI M1573M South Bridge(7)

PMU Interface (Continued)

Pin Name	I/O Type	Description
VRMPWG / VRGATE / ALLOW_HTTSTOP	I	**VRM Power Good (for P4 Desktop) / VRM Power Good Gate(for P4 Mobile)/NB Allow HTTSTOP#(for K8).** In P4 platform, this signal is used indicate that the CPU voltage is stable. In K8 platform, this signal output from the NB to notifies the SB whether it is allowed to assert or deassert HTTSTOP#. This controls the timing of the CPU entering and exiting C3.
AGPBUSY# (Mobile Only) / HTTREQ#(K8 Mode Only)	I	**AGP Device Busy.** This signal is used by M1573 to indicate that the AGP device is busy. **HyperTransport Request.** HTT device can use this input signal to request re-enabling HTT links for normal operation. It can also be used as AGP Busy in HyperTransport system implementation, i.e., the AGPBUSY# from AGP device can be connected to this pin.
VRHI# / RUNGPO[11]	O	**CPU High/Low Voltage Selection.** This signal is used to select the voltage high/low level for the CPU and can be optionally configured as RUNGPO.

Test Signals

Pin Name	I/O Type	Description
DFTSE/ NANDTEST	I	**DFT Scan Enable.** This signal is used as the DFT Scan Enable for ATPG pattern input when DFT_MODE is tied to high. It should be pull-low for normal operation. **NAND Tree TEST pin.** This signal is used as the NANDTREE TEST mode enable if it is tied to high when DFT_MODE is tied to low. It should be pull-low for normal operation.
DFTTM	I	**DFT Test Mode.** This signal is used as the DFT Test Mode Enable for ATPG pattern input. It should be pull-low for normal operation.

Clocks

Pin Name	I/O Type	Description
Real Time Clock Interface		
X32KI	I	**32 KHz Oscillator Input 1. This is a crystal input 1 from a 32.768 KHz Quartz Crystal. The input oscillator pad will generate the 32 KHz clock into the internal Suspend circuit and output the clock from the CLK32KO to DRAM Suspend Refresh Circuit. If a crystal is not used, this pin should be pulled to ground.**
X32KII	I	**32 KHz Oscillator Input 2.** This is a crystal input 2 from a 32.768 KHz Quartz Crystal. The input oscillator pad will generate the 32 KHz clock for the internal Suspend circuit and output the clock from the CLK32KO to DRAM Suspend Refresh Circuit. If a crystal is not used, an external 32 KHz clock input should be connected to this pin.
RTCRST#	I	**RTC Reset.** The input pin is used to reset internal battery-powered RTC SRAM.
X32K_OSC_MODE	I	**32K oscillator PAD large or small current mode switch.** It's Reserved for internal test only and should be tied low.
Other Clocks		
CLK14M	I	**14.318 MHz Clock Input.** This input clock will be used for Power Management timer, 8254 timer.
X25M1	I	Optional external 25MHz crystal input for SATA reference clock
X25M2	I	Optional external 25MHz crystal input for SATA reference clock
CLK24_48M	I	24/48 MHz Clock Output.

Miscellaneous Signals

Pin Name	I/O Type	Description
SPKR	O	**Speaker Output.** This output pin should be connected to the on-board speaker.
SERIRQ	I/O	**Serial Interrupt Request.** This pin is used to support the serial interrupt request protocol of common architecture.

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5.3 ULI M1573M South Bridge(8)

CPU Interface

Pin Name	I/O Type	Description
P4 Mode Interface		
A20M# / RUNGPO[12]	O	**CPU A20 Mask.** This is the CPU Address line A20 mask signal. It can be configured as RUNGPO.
CPUHI# (Mobile Only) / RUNGPO[13]	O	**CPU High/Low Performance Selection.** This signal is used to select the CPU high/low performance and can be optionally configured as RUNGPO.
CPUPWG/ RUNGPO[14]	O	**CPU Power Good.** This signal is connected to the PWRGOOD input of CPU and can be optionally configured as RUNGPO.
CPURST#/ RUNGPO[32]	OD	**CPU Cold Reset.** When system is powered on, this reset signal will be asserted and become de-asserted until 4 ms after HTTPWROK becomes high. This pin can be configured as RUNGPO.
DSLEEP#/ RUNGPO[15]	O	**CPU Deep Sleep.** This signal is used to force CPU entering deep sleep state. This signal can be configured as RUNGPO.
FERR#	I	**Floating Point Error.** FERR# input from coprocessor to generate IRQ13.
IGNNE#/ RUNGPO[16]	O	**Ignore Error.** This pin is used as the "ignore numeric coprocessor error" signal and connects to CPU. It can be configured as RUNGPO.
INIT#/ RUNGPO[17]	O	**CPU Initialization.** This signal will be asserted for 16 PCI clocks when M1573 resets the CPU. It can be configured as RUNGPO.
INTR/ RUNGPO[18]	O	**Interrupt Request to CPU.** This is the interrupt signal generated by the internal 8259 and should connect to CPU INTR as a maskable interrupt. It can be configured as RUNGPO.
NMI/ RUNGPO[19]	O	**Non-Maskable Interrupt to CPU.** This is generated by the PCI Parity error or SERR# assertion, and the other internal error event. This output should connect to CPU NMI as a non-maskable interrupt. It can be configured as RUNGPO.
SLEEP#/ RUNGPO[20]	O	**CPU Sleep.** This signal is used to force CPU entering sleep state. This signal can be configured as RUNGPO.
SMI#/ RUNGPO[21]	O	**System Management Interrupt.** This signal should be connected to CPU SMI# input. It can be configured as RUNGPO.

CPU Interface (Continued)

Pin Name	I/O Type	Description
P4 Mode Interface		
STPCLK#/ RUNGPO[22]	O	**Stop CPU Internal Clock Request.** This signal is used to make CPU enter power saving mode and stop the CPU internal clock. The signal should be connected to CPU STPCLK# input. It can be configured as RUNGPO.
A20GATE/ RUNGPI[15]	I	**A20 Gate.** This pin is the external Keyboard A20 gate signal and can be configured as RUNGPI.
KBCRC#/ RUNGPI[16]	I	**Keyboard RC.** This pin is the external Keyboard RC signal and can be configured as RUNGPI.
HTT Interface		
HTTSTOP#/ RUNGPO[31]	OD	**HyperTransport Stop** This output signal is used to enable and disable HyperTransport links during C3/C4 state or system power saving state transitions. This output should be externally pulled high as 2.5V with 10K resistor. This pin can be configured as RUNGPO.
HTTRESET#/ RUNGPO[30]	OD	**HyperTransport Reset** This output signal is used to reset the HyperTransport chain. This output should be externally pulled high as 2.5V with 10K resistor. This pin can be configured as RUNGPO.
HTTPWROK/ RUNGPO[29]	OD	**HyperTransport Power OK.** This output signal is used by a HyperTransport device to indicate that the power and clocks are stable. This output should be externally pulled high as 2.5V with 10K resistor. This pin can be configured as RUNGPO.

General Purpose I/O

Pin Name	I/O Type	Description
RUNGPIO[3:0]/ RUNGPI[3:0]/RUNGPO[3:0]	IO	**General-Purpose Input/Output.** These pins can be configured as RUNGPI[3:0](default) or RUNGPO[3:0].
RSMGPIO[3:0]/ RSMGPO[3:0]/RSMGPI[3:0]	IO	**Resume Region General-Purpose Input/Output**. These pins can be configured as RSMGPI[3:0] or RSMGPO[3:0](default).

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5.3 ULI M1573M South Bridge(9)

USB Interface

Pin Name	I/O Type	Description
USBCLK	I	**48 MHz USB Clock Input.** This clock will send to USB state machine to generate USB signals.
USBOVR#[7:6], USBOVR#[5:0]/ RSMGPI[9:4]	I	**Over Current Detect for USB Host Controller[7:0].** These pins are used to monitor the USB Power Over Current status. USBOVR#[5:0] can be configured as RSMGPI.
USB_DN0, USB_DP0	I/O	**Universal Serial Bus Port 0.** These are the serial data pair for USB Port 0.
USB_DN1, USB_DP	I/O	**Universal Serial Bus Port 1.** These are the serial data pair for USB Port 1.
USB_DN2, USB_DP2	I/O	**Universal Serial Bus Port 2.** These are the serial data pair for USB Port 2.
USB_DN3, USB_DP3	I/O	**Universal Serial Bus Port 3.** These are the serial data pair for USB Port 3.
USB_DN4, USB_DP4	I/O	**Universal Serial Bus Port 4.** These are the serial data pair for USB Port 4.
USB_DN5, USB_DP5	I/O	**Universal Serial Bus Port 5.** These are the serial data pair for USB Port 5.
USB_DN6, USB_DP6	I/O	**Universal Serial Bus Port 6.** These are the serial data pair for USB Port 6.
USB_DN7, USB_DP7	I/O	**Universal Serial Bus Port 7.** These are the serial data pair for USB Port 7.
USB_RX_TERM	I	USB PHY Receiving Termination
USB_TX_CS	I	USB PHY Transmission Current Source

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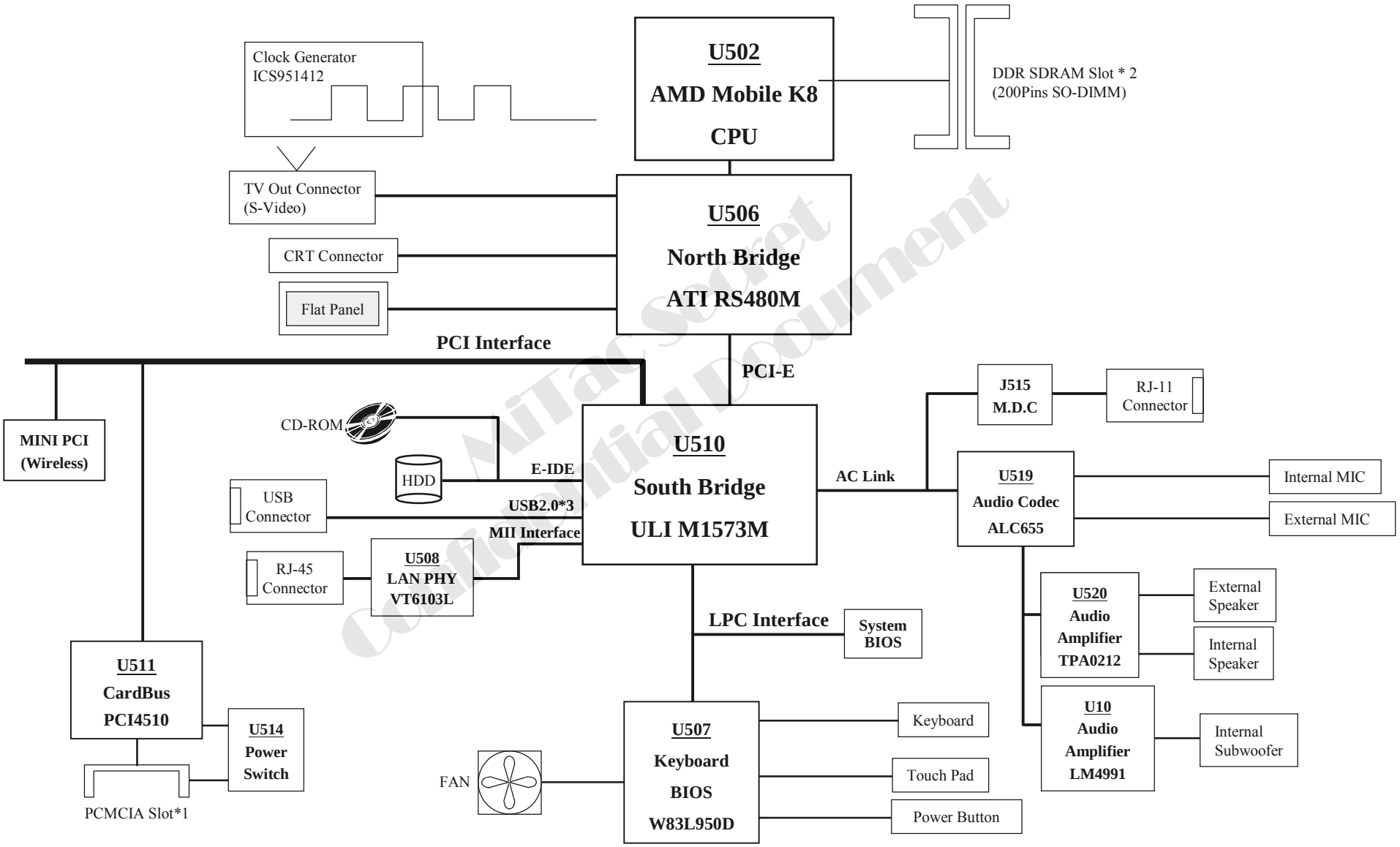
6. System Block Diagram



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7. Maintenance Diagnostics

7.1 Introduction

Each time the computer is turned on, the system bios runs a series of internal checks on the hardware. This power-on self test (post) allows the computer to detect problems as early as the power-on stage. Error messages of post can alert you to the problems of your computer.

If an error is detected during these tests, you will see an error message displayed on the screen. If the error occurs before the display is initialized,then the screen cannot display the error message. Error codes or system beeps are used to identify a post error that occurs when the screen is not available.

The value for the diagnostic port (378H) is written at the beginning of the test. Therefore, if the test failed, the user can determine where the problem occurred by reading the last value written to port 378H by the Mini PCI debug board.

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7.2 Error Codes(1)

Following is a list of error codes in sequent display on the MINI PCI debug card.

Code	POST Routine Description
10h	Some type of lone reset
11h	Turn off FAST A20 for POST
12h	Signal power on reset
13h	Initialize the chipset
14h	Search for ISA Bus VGA adapter
15h	Reset counter / Timer 1
16h	User register config through CMOS
17h	Size memory
18h	Dispatch to RAM test
19h	Check sum the ROM
1Ah	Reset PIC's
1Bh	Initialize video adapter(s)
1Ch	Initialize video (6845Regs)
1Dh	Initialize color adapter
1Eh	Initialize monochrome adapter
1Fh	Test 8237A page registers

Code	POST Routine Description
20h	Test keyboard
21h	Test keyboard controller
22h	Check if CMOS RAM valid
23h	Test battery fail & CMOS X-SUM
24h	Test the DMA controller
25h	Initialize 8237A controller
26h	Initialize int vectors
27h	RAM quick sizing
28h	Protected mode entered safely
29h	RAM test completed
2Ah	Protected mode exit successful
2Bh	Setup shadow
2Ch	Going to initialize video
2Dh	Search for monochrome adapter
2Eh	Search for color adapter
2Fh	Sign on messages displayed

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7.2 Error Codes(2)

Following is a list of error codes in sequent display on the MINI PCI debug card.

Code	POST Routine Description
30h	Special init of keyboard ctlr
31h	Test if keyboard Present
32h	Test keyboard Interrupt
33h	Test keyboard command byte
34h	Test, blank and count all RAM
35h	Protected mode entered safely(2)
36h	RAM test complete
37h	Protected mode exit successful
38h	Update output port
39h	Setup cache controller
3Ah	Test if 18.2Hz periodic working
3Bh	Test for RTC ticking
3Ch	Initialize the hardware vectors
3Dh	Search and init the mouse
3Eh	Update NUMLOCK status
3Fh	Special init of COMM and LPT ports

Code	POST Routine Description
40h	Configure the COMM and LPT ports
41h	Initialize the floppies
42h	Initialize the hard disk
43h	Initialize option ROMs
44h	OEM's init of power management
45h	Update NUMLOCK status
46h	Test for coprocessor installed
47h	OEM functions before boot
48h	Dispatch to operate system boot
49h	Jump into bootstrap code
50h	ACPI init
51h	PM init & Geyserville CPU init
52h	USB HC init

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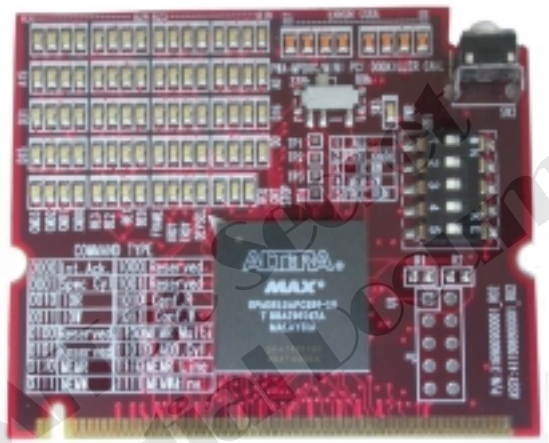
7.3 Debug Tool

7.3.1 Diagnostic Tool for Mini PCI Slot :



P/N:411906900001
Description: PWA-MPDOG;MINI PCI DOGKELLER CARD
Note: Order it from MIC/TSSC

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8. Trouble Shooting

- 8.1 No Power (*1)
- 8.2 No Display (*2)
- 8.3 VGA Controller Test Error LCD No Display
- 8.4 External Monitor No Display
- 8.5 Memory Test Error
- 8.6 Keyboard (K/B)/Touch-Pad (T/P) Test Error
- 8.7 Hard Disk Drive Test Error
- 8.8 CD-ROM Drive Test Error
- 8.9 USB Test Error
- 8.10 Audio Test Error
- 8.11 LAN Test Error
- 8.12 PC Card & Card Reader Socket Test Error
- 8.13 Mini-PCI Socket Test Error

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8350 N/B Maintenance

*1: No Power Definition

Base on ACPI Spec. We define the no power as while we press the power button, the system can't leave S5 status or none the PG signal send out from power supply.

Judge condition:

- Check whether there are any voltage feedback control to turn off the power.
- Check whether no CPU power will cause system can't leave S5 status.

If there are not any diagram match these condition, we should stop analyzing the schematic in power supply sending out the PG signal. If yes, we should add the effected analysis into no power chapter.

*2: No Display Definition

Base on the digital IC three basic working conditions: working power, reset, Clock. We define the no display as while system leave S5 status but can't get into S0 status.

Judge condition:

- Check which power will cause no display.
- Check which reset signal will cause no display.
- Check which Clock signal will cause no display

Base on these three conditions to analyze the schematic and edit the no display chapter.

Keyword:

- S5: *Soft Off*
- S0: *Working*

For detail please refer the ACPI specification

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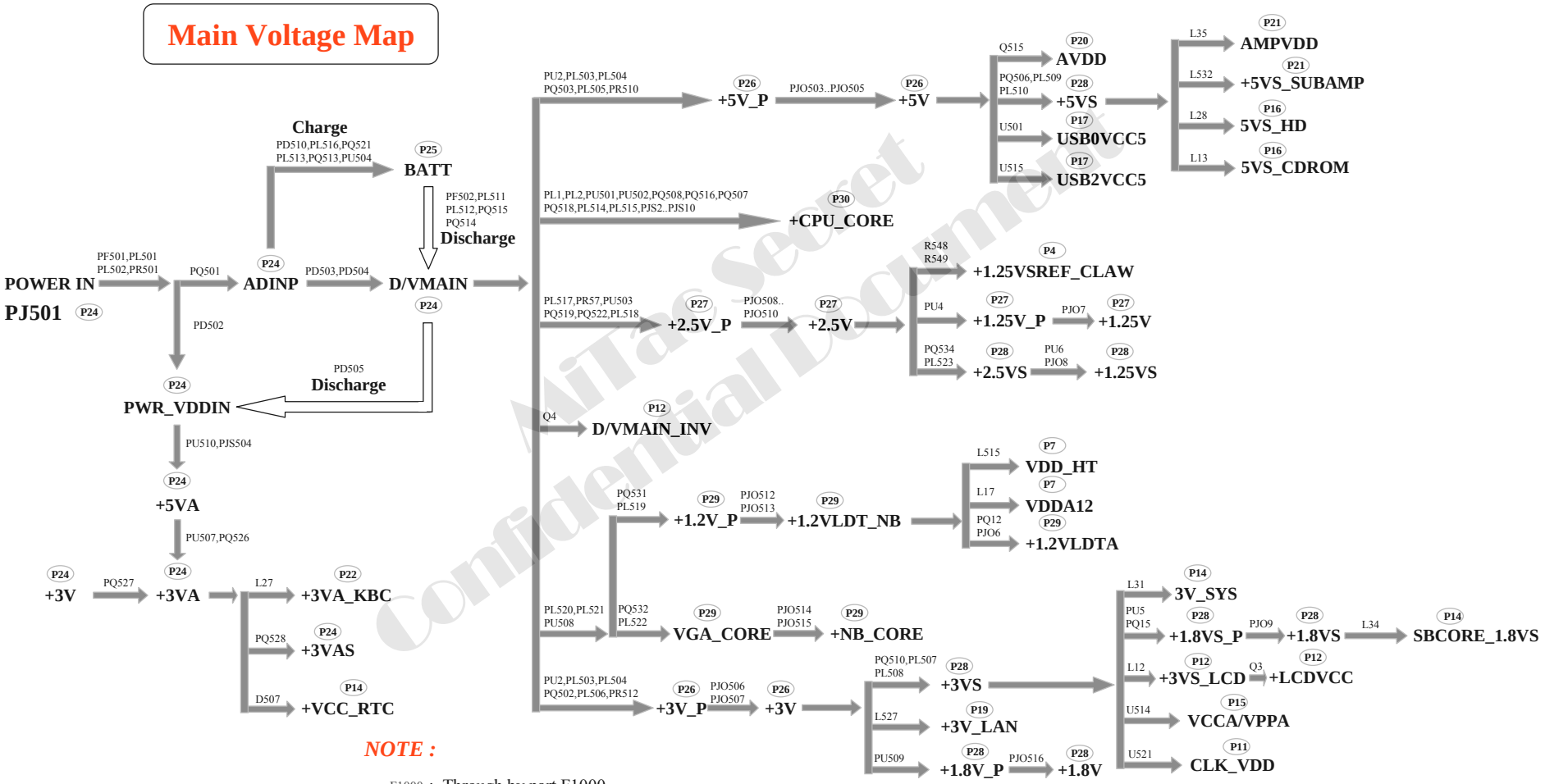
8350 N/B Maintenance

8.1 No Power(1)

When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.

Main Voltage Map



NOTE :

F1000 : Through by part F1000.

P38 : Page 38 on M/B Board circuit diagram.

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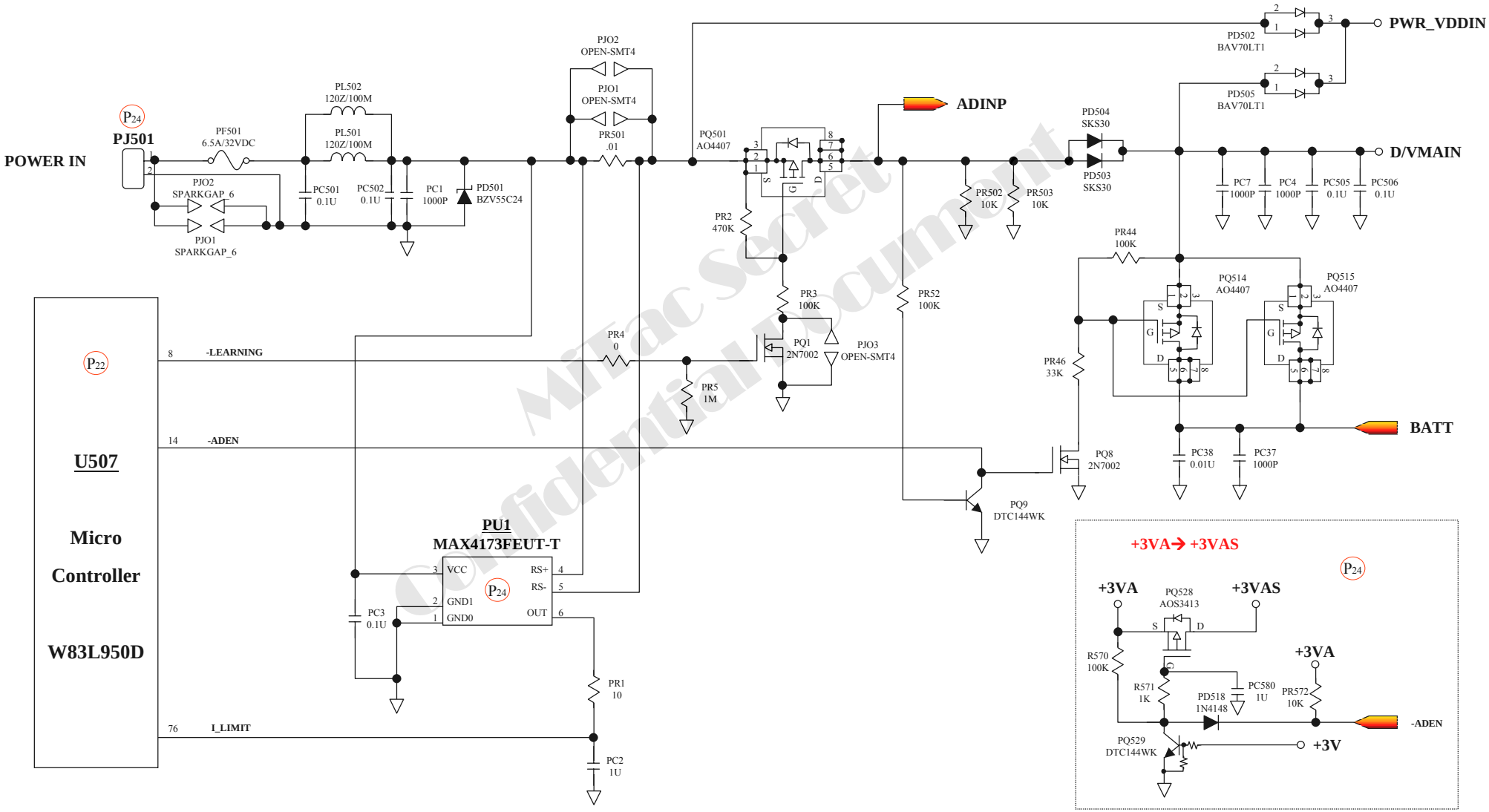
8350 N/B Maintenance

8.1 No Power(2)

When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.



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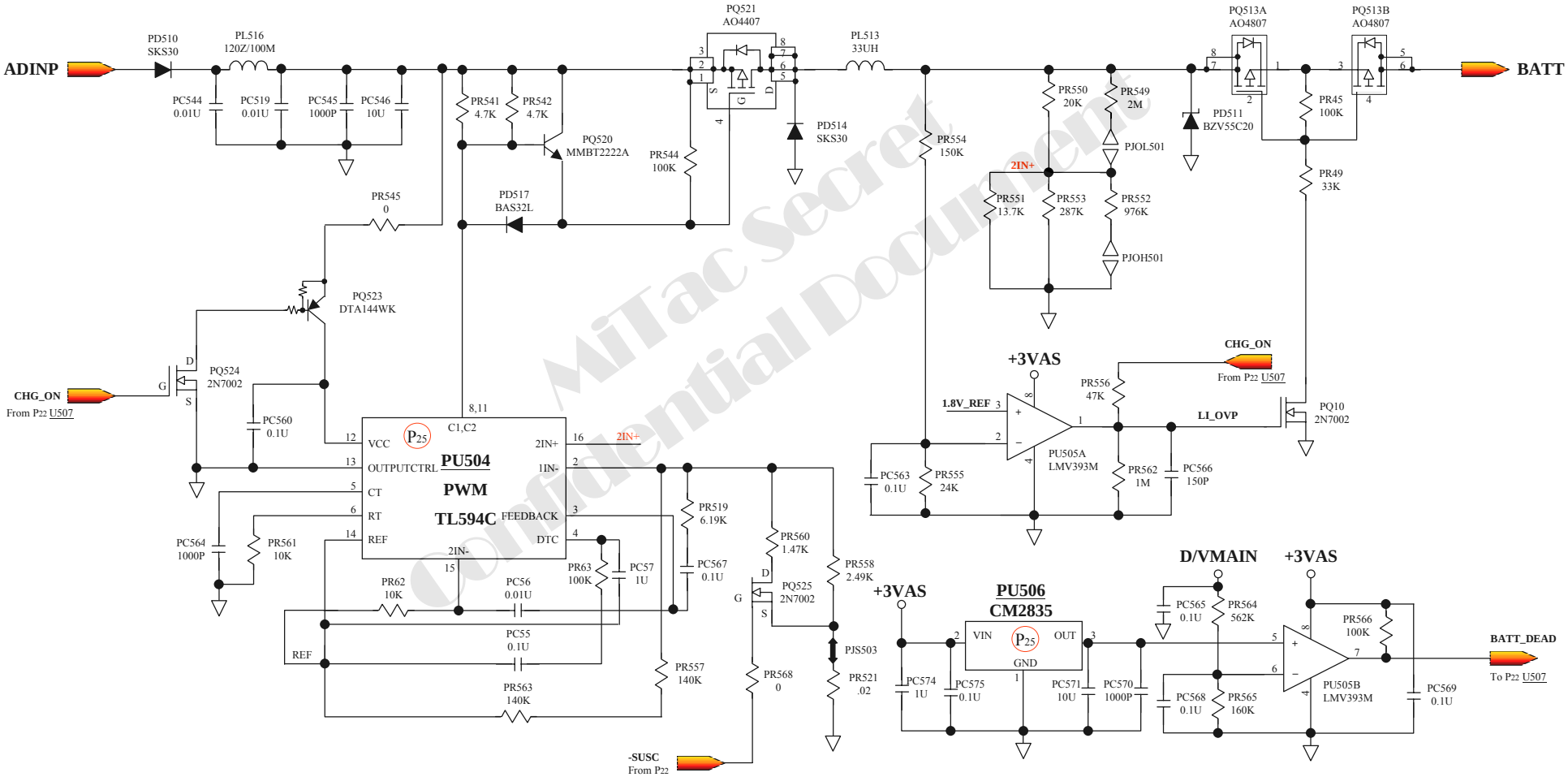
8.1 No Power(3)

When the battery is installed but the battery status indicate LED display abnormal.



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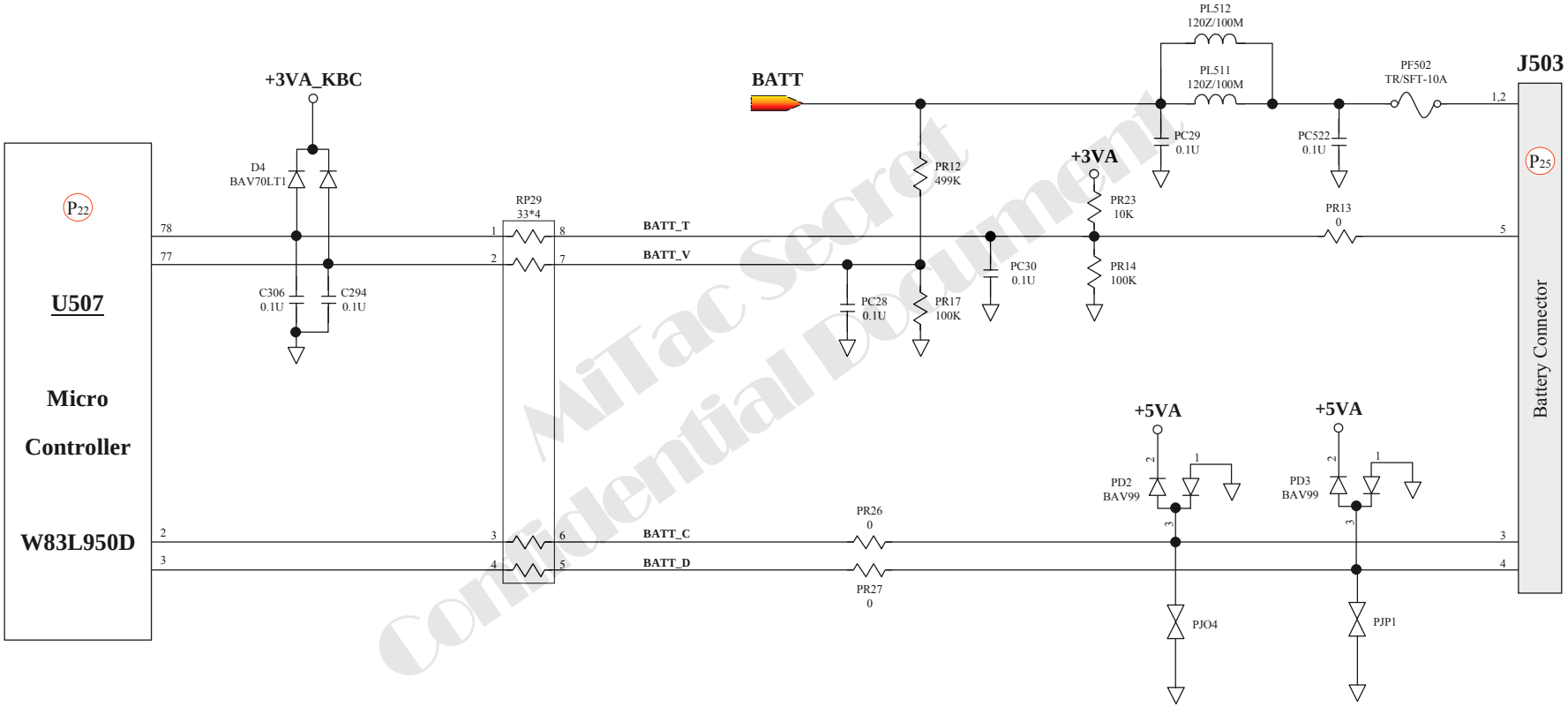
8.1 No Power(4)

When the battery is installed but the battery status indicate LED display abnormal.



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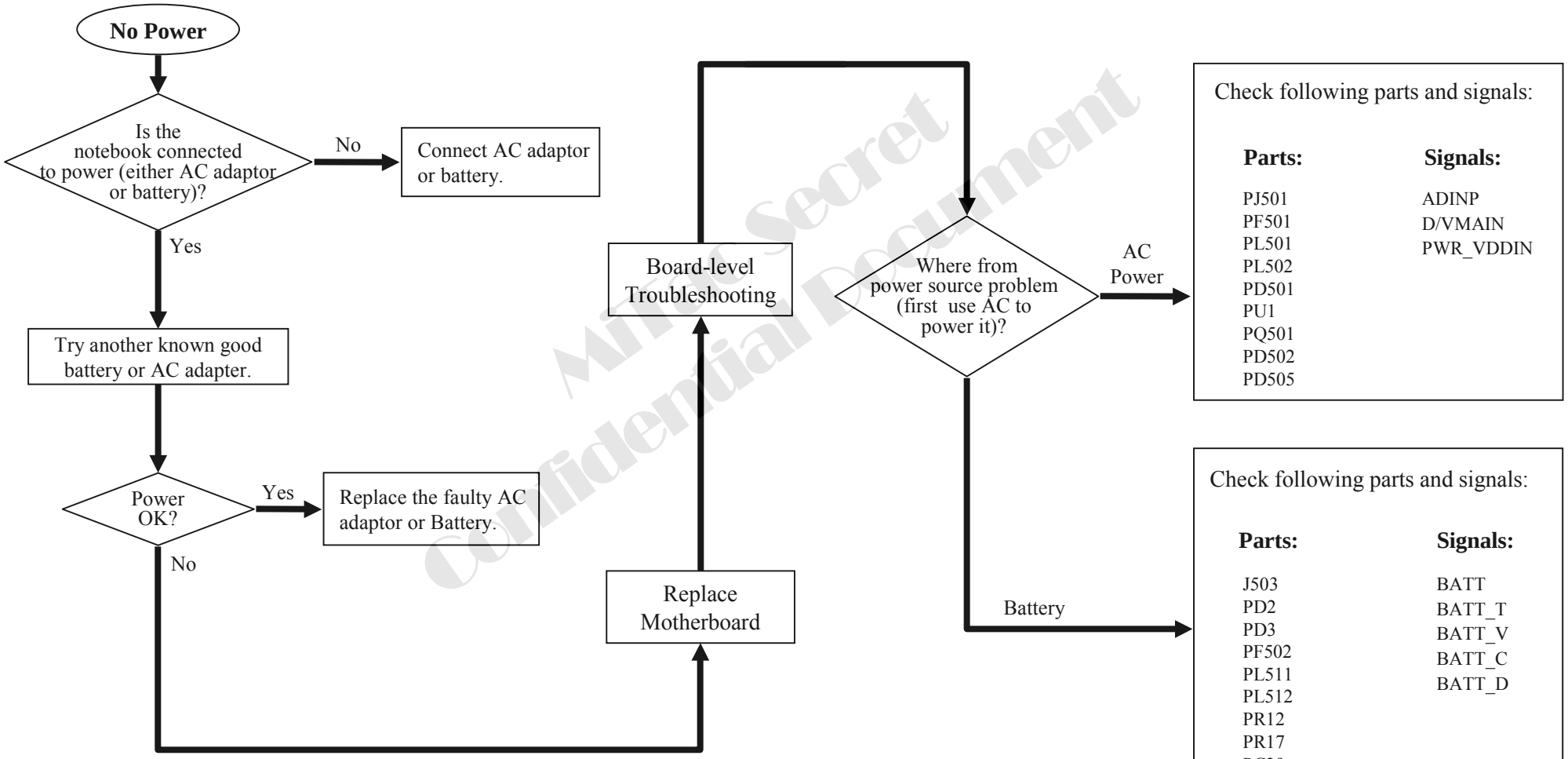
8.1 No Power(5)

When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.



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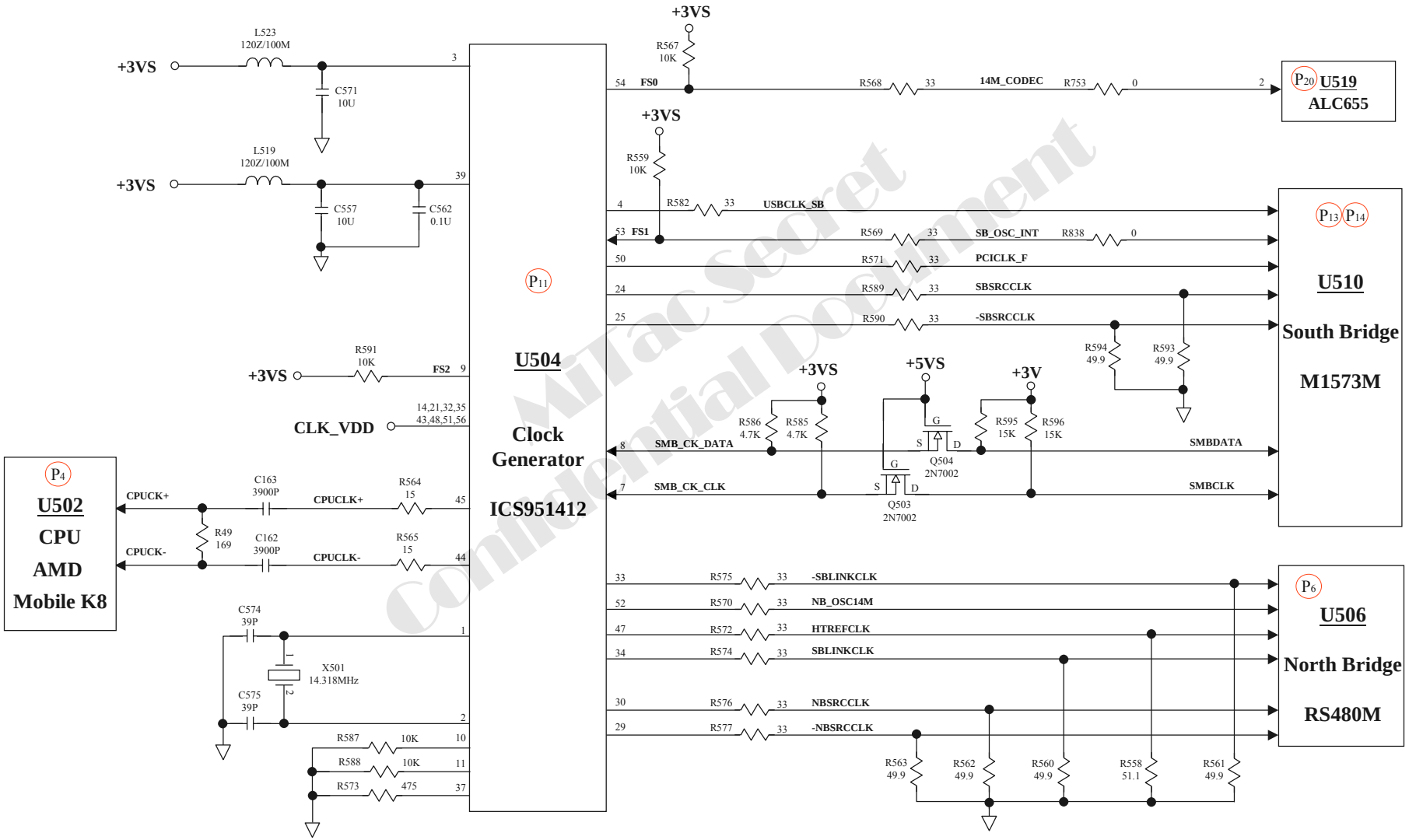
8350 N/B Maintenance

8.2 No Display(1)

****** System Clock Check ******



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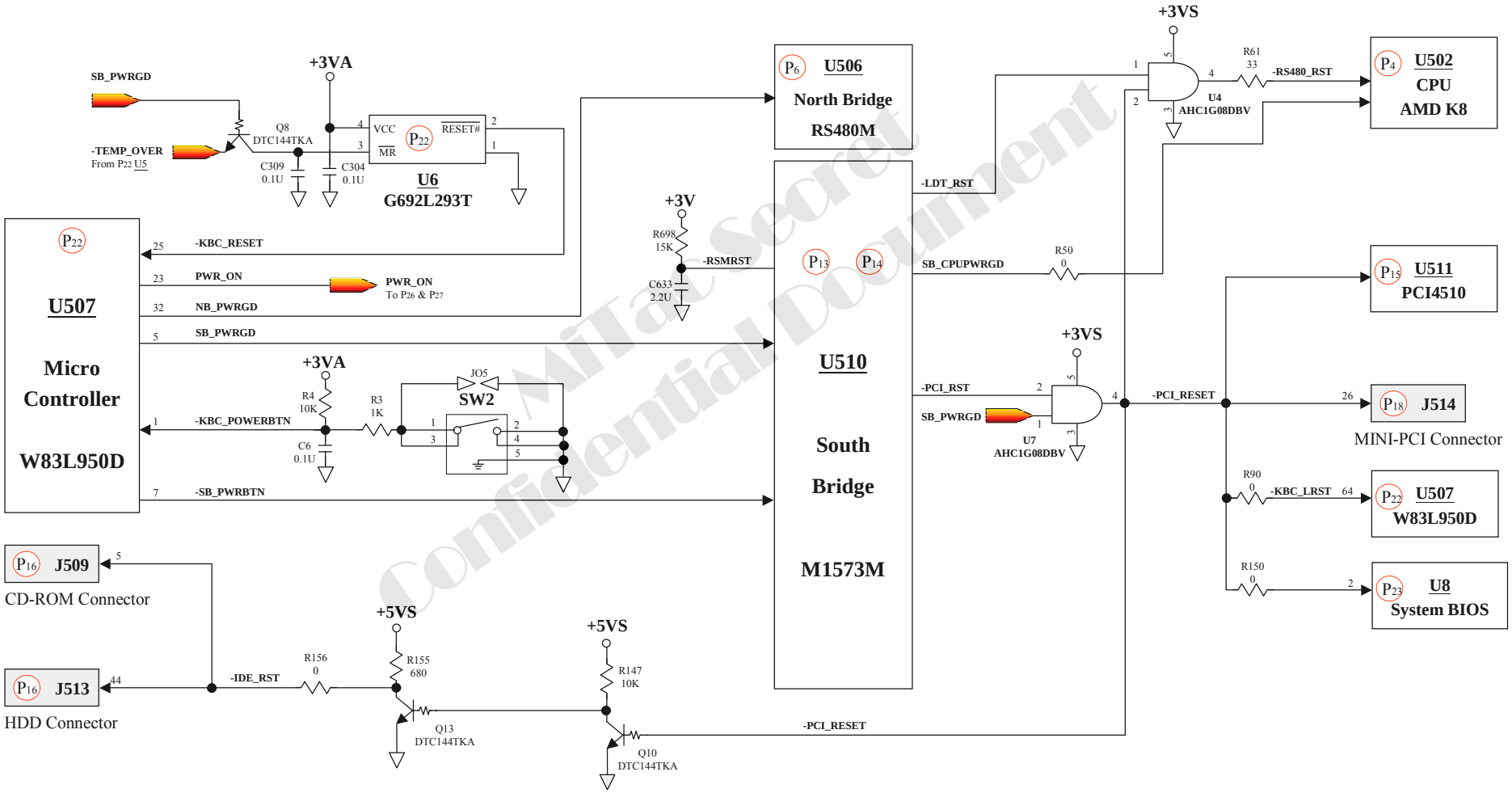
8350 N/B Maintenance

8.2 No Display(2)

****** Power Good & Reset Circuit Check ******



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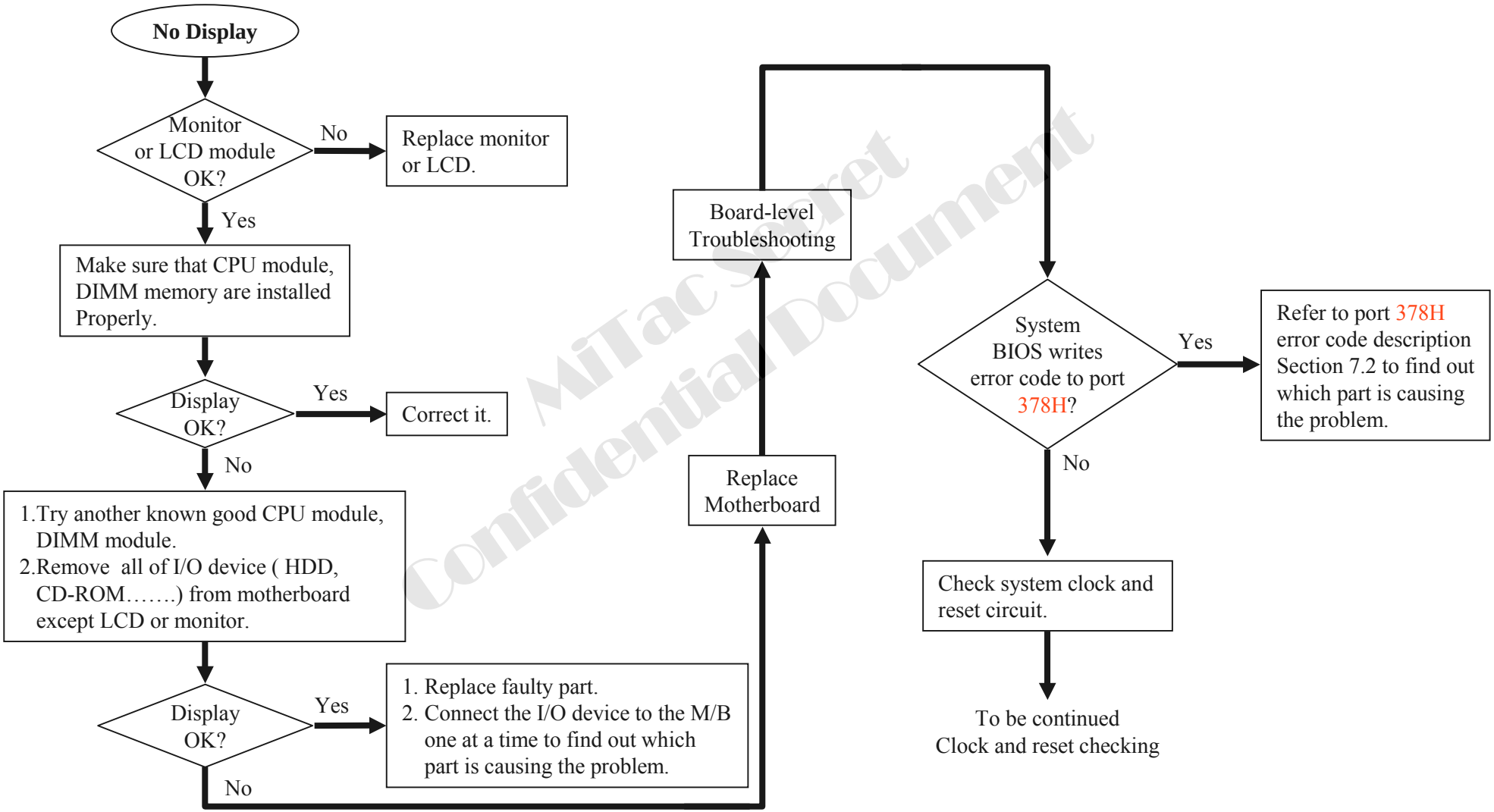
8.2 No Display(3)

There is no display on both LCD and VGA monitor after power on although the LCD and monitor is known-good.



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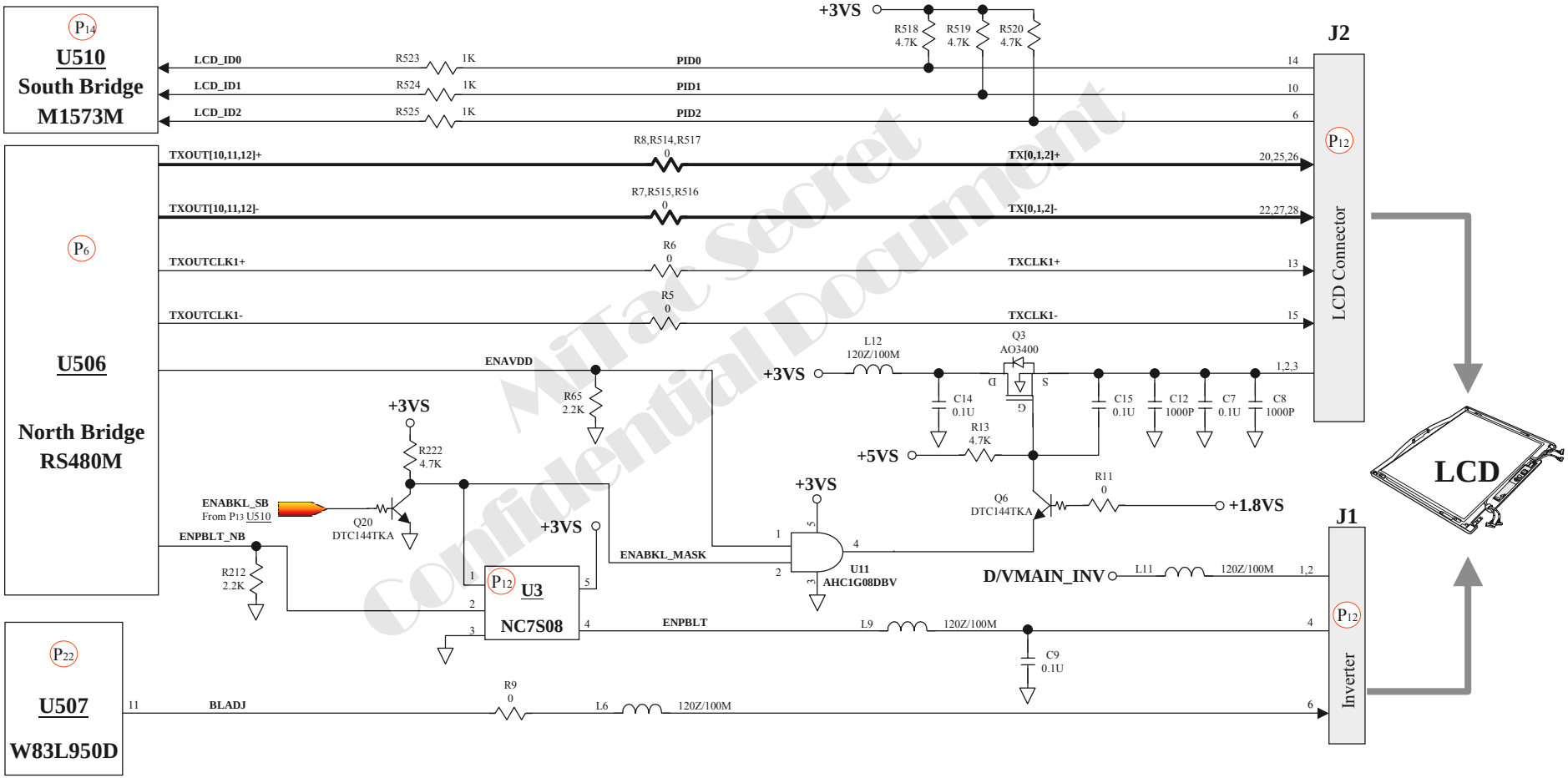
8.3 VGA Controller Test Error LCD No Display(1)

There is no display or picture abnormal on LCD although power-on-self-test is passed.



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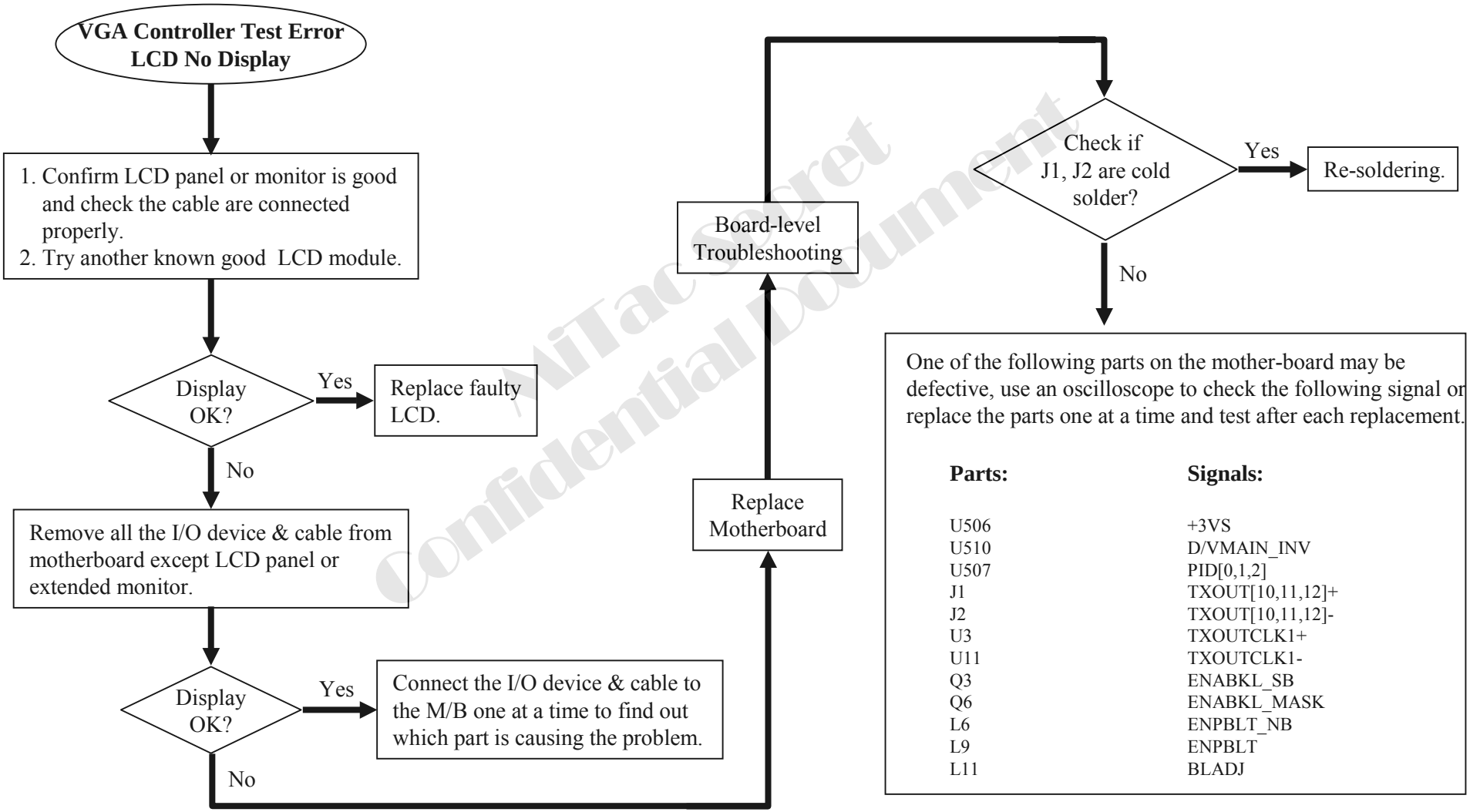
8.3 VGA Controller Test Error LCD No Display(2)

There is no display or picture abnormal on LCD although power-on-self-test is passed.



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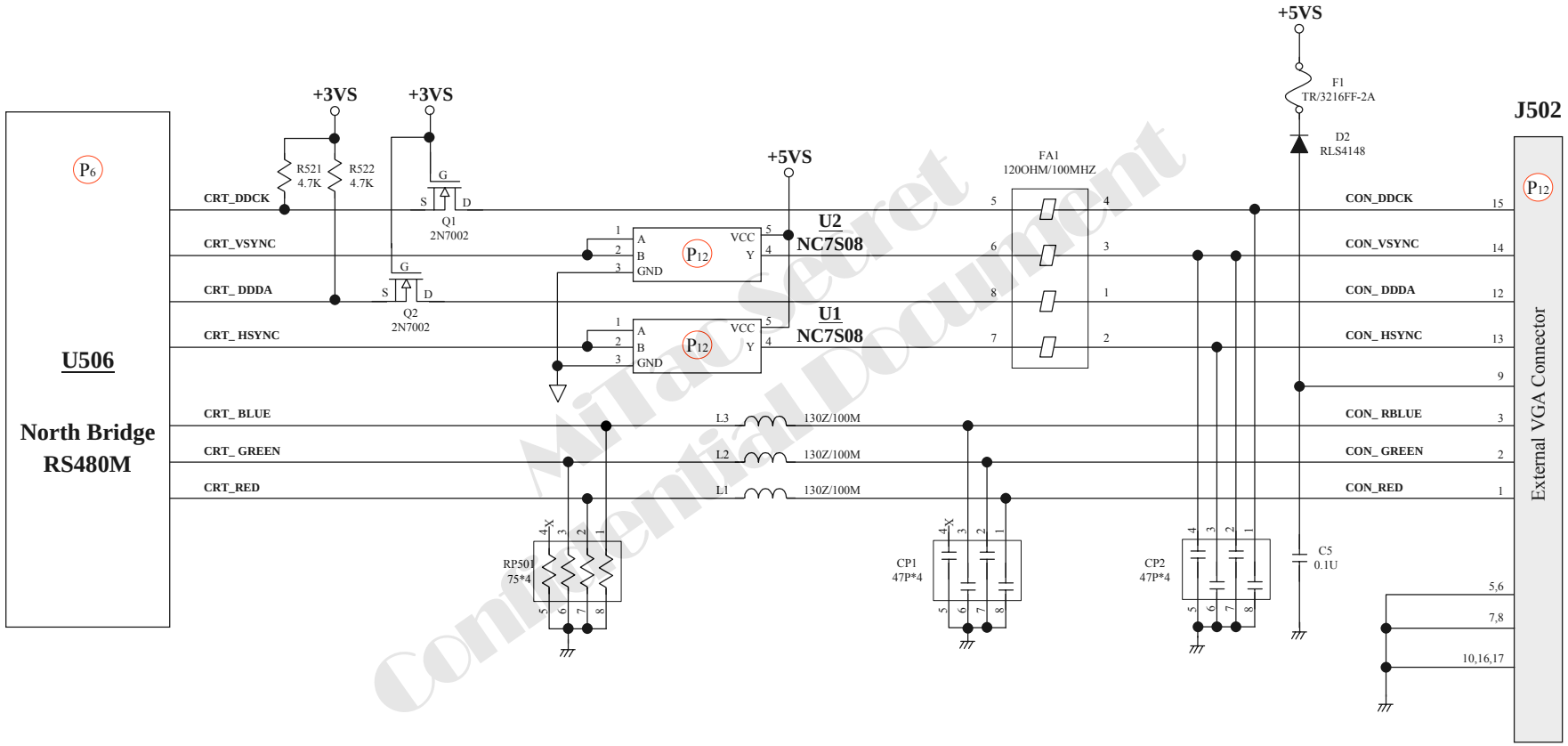
8.4 External Monitor No Display(1)

There is no display or picture abnormal on CRT monitor, but it is OK for LCD.



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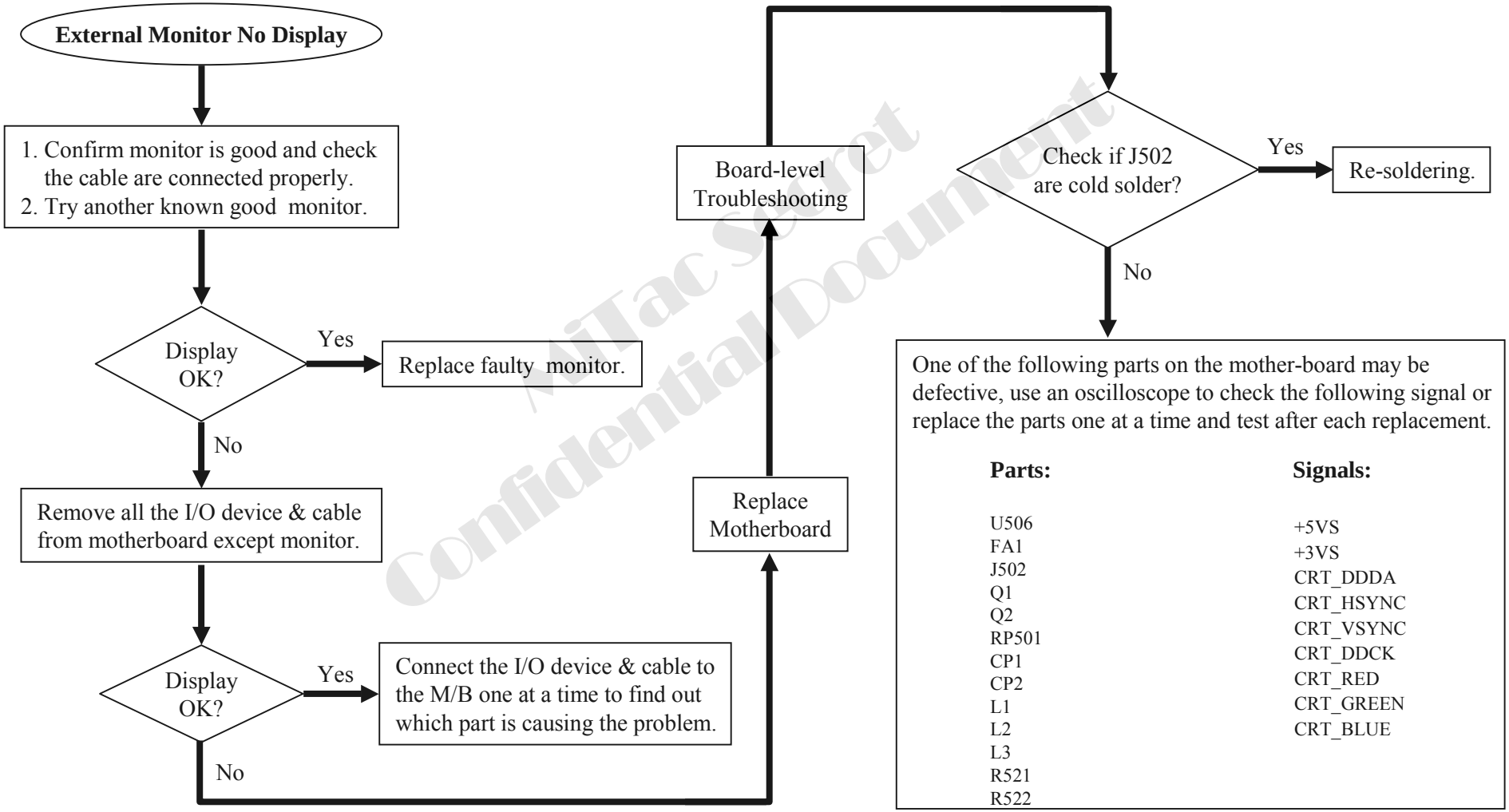
8.4 External Monitor No Display(2)

There is no display or picture abnormal on CRT monitor, but it is OK for LCD.



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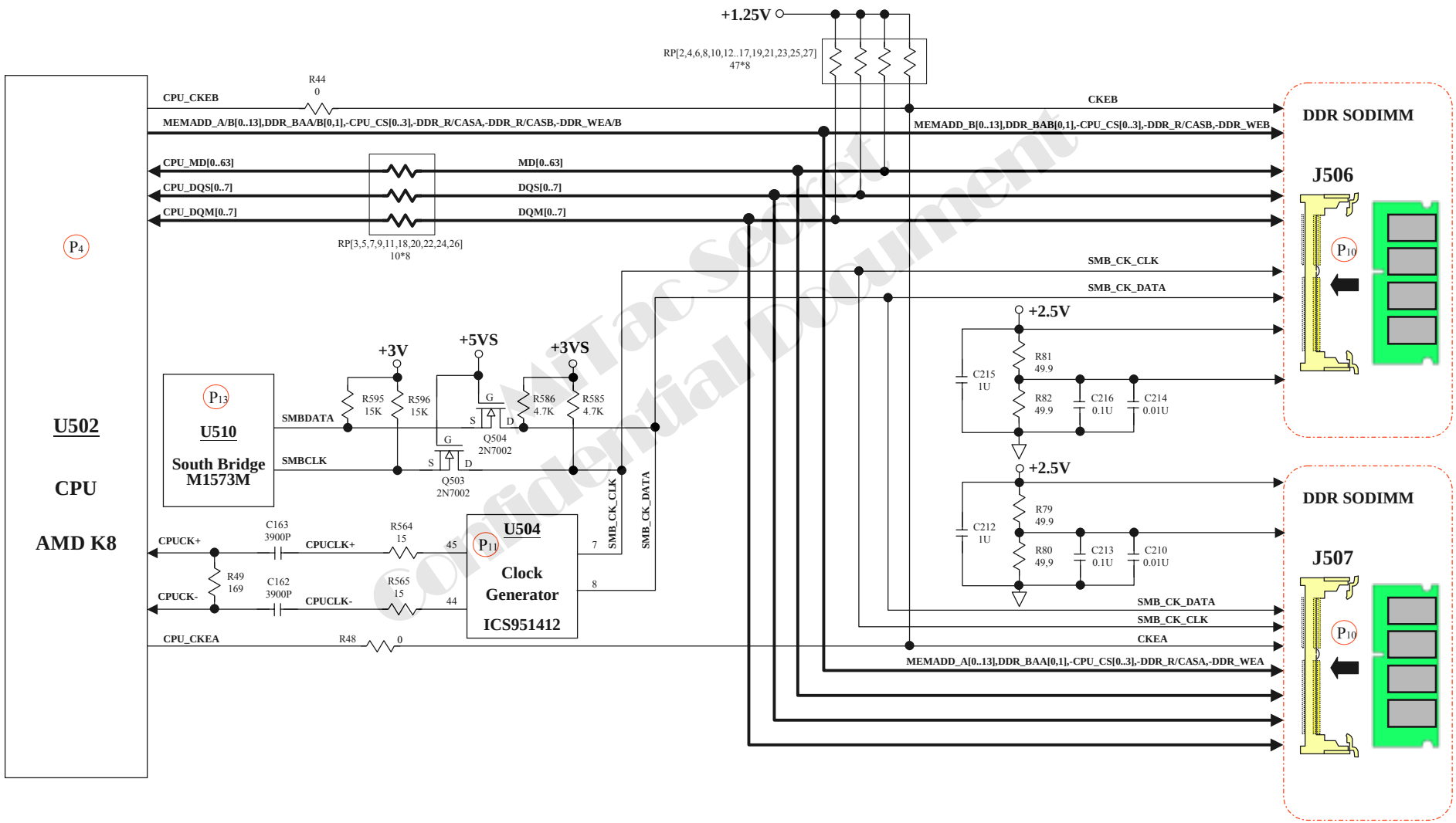
8.5 Memory Test Error(1)

Extend DDR SODIMM is Test Error or system hangs up.



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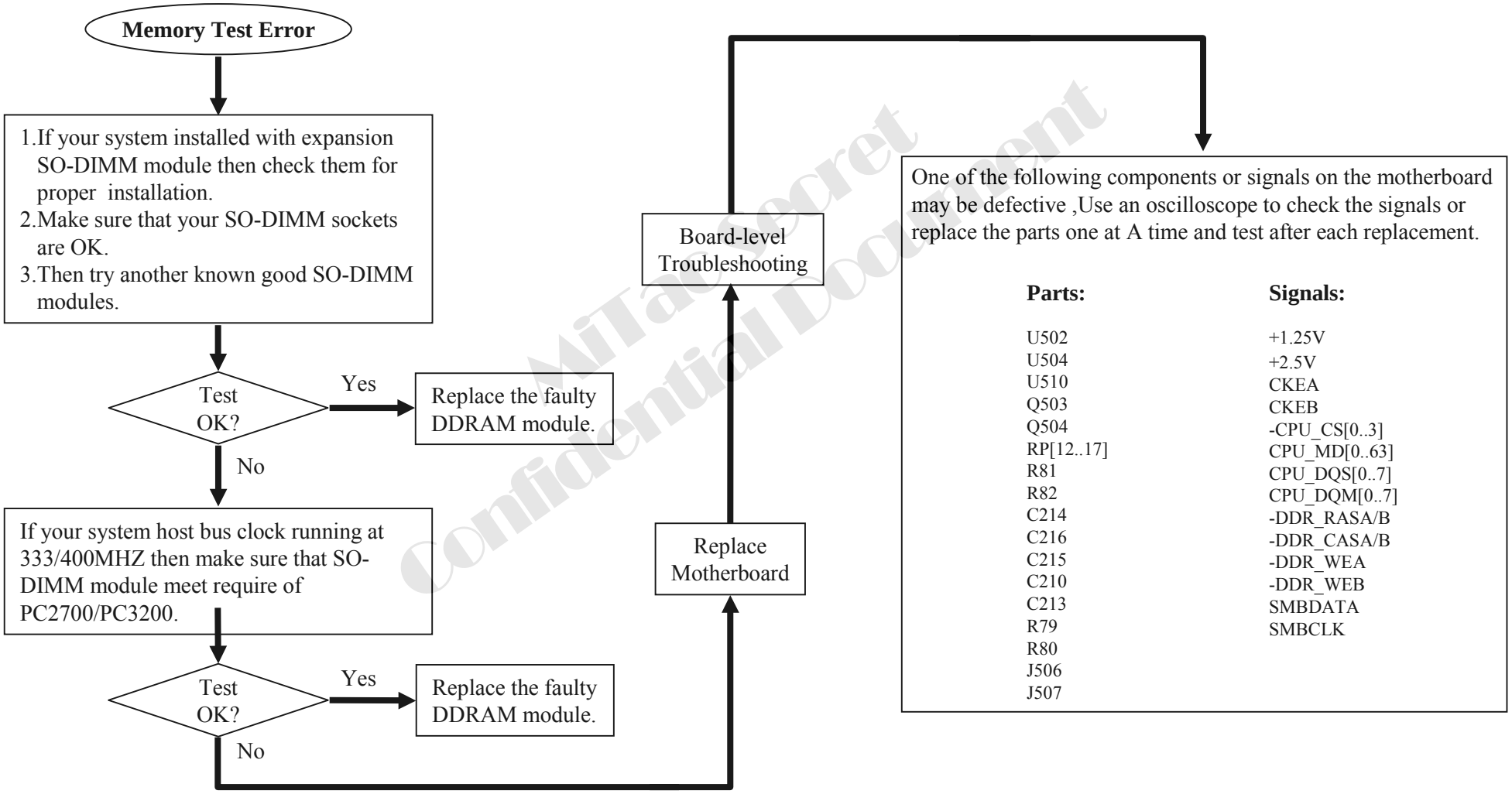
8.5 Memory Test Error(2)

Extend DDRAM is Test Error or system hangs up.



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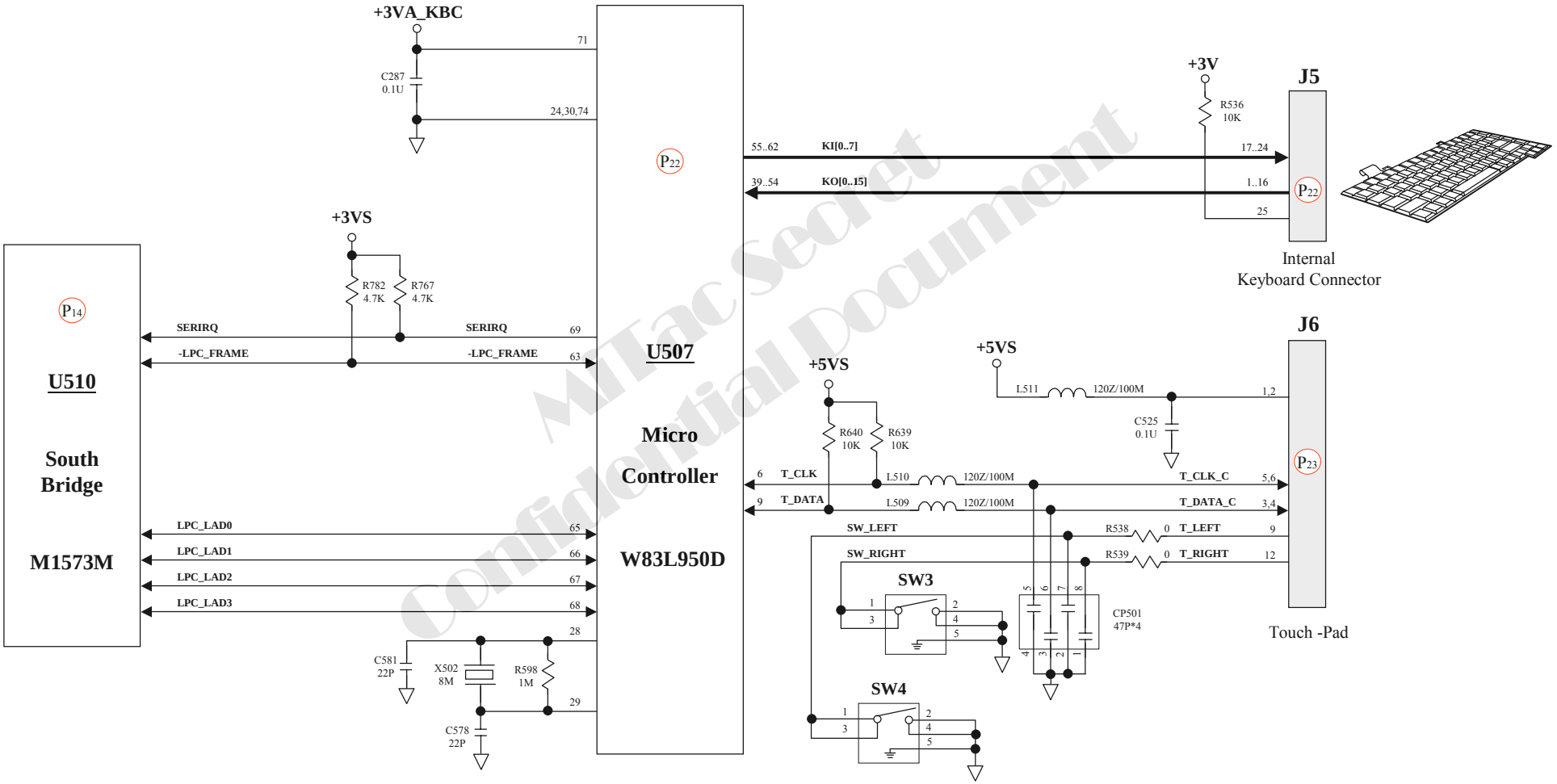
8.6 Keyboard (K/B)/Touch-Pad(T/P) Test Error(1)

Error message of keyboard or touch-pad Test Error is shown or any key does not work.



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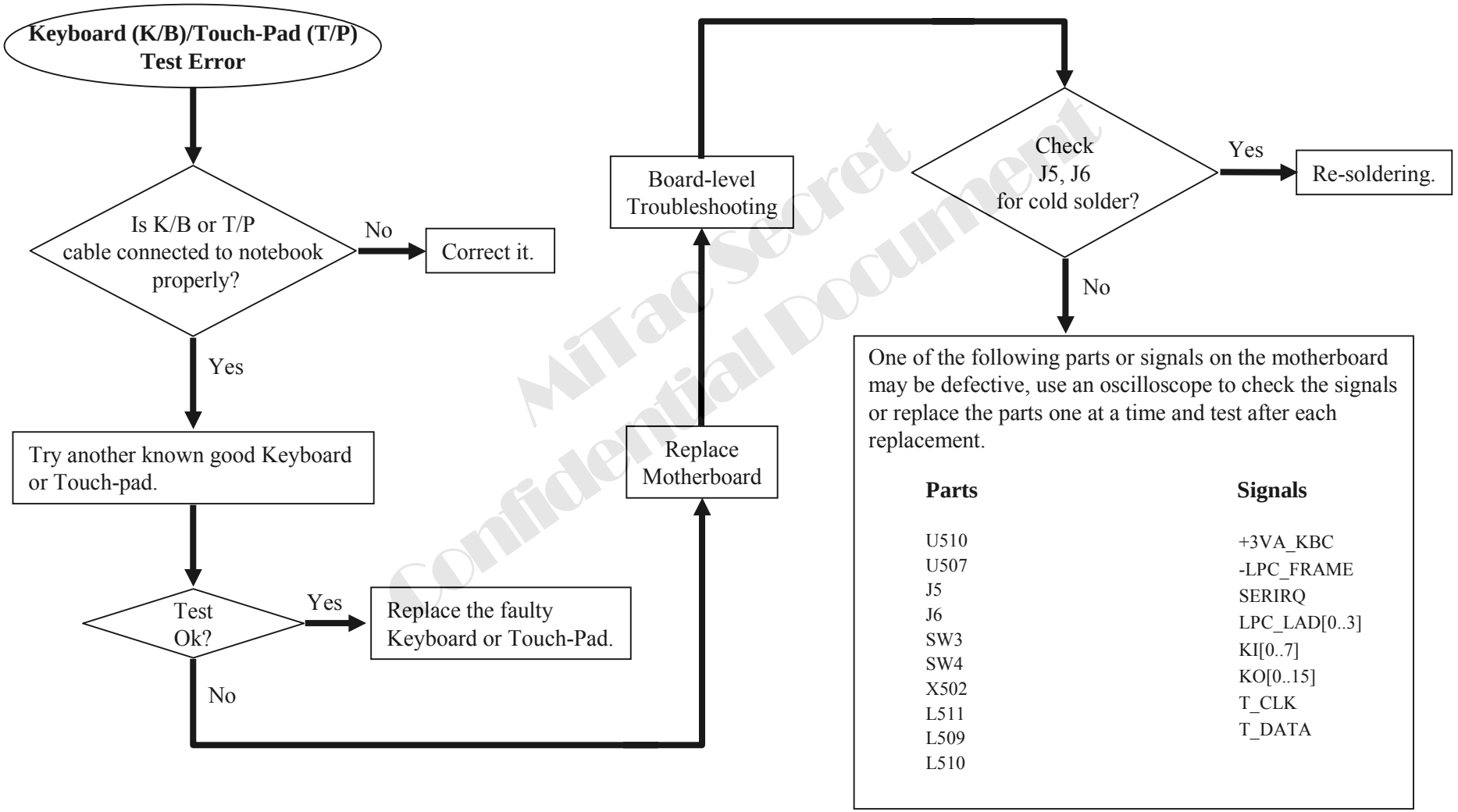
8.6 Keyboard (K/B)/Touch-Pad(T/P) Test Error(2)

Error message of keyboard or touch-pad Test Error is shown or any key does not work.



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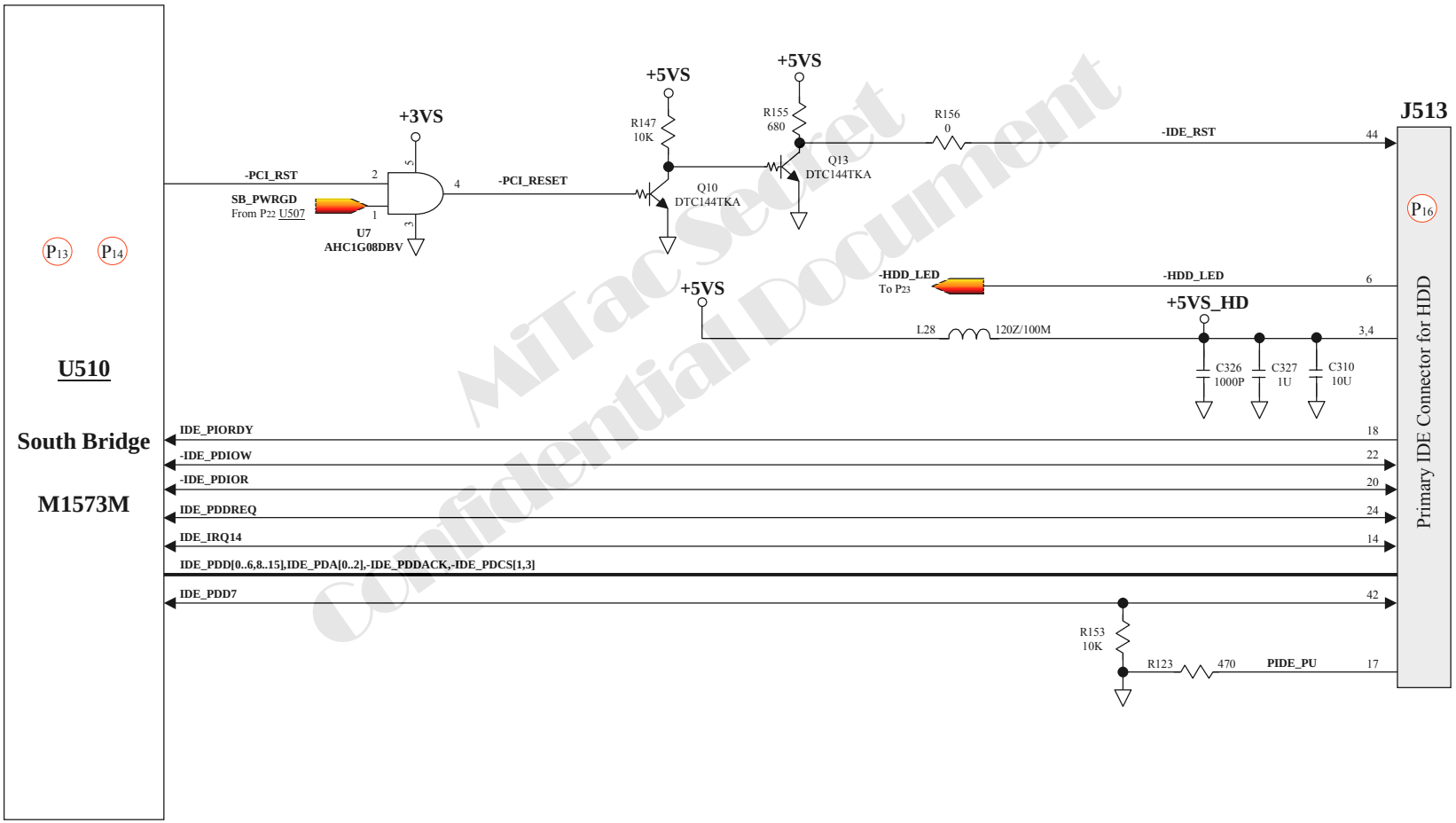
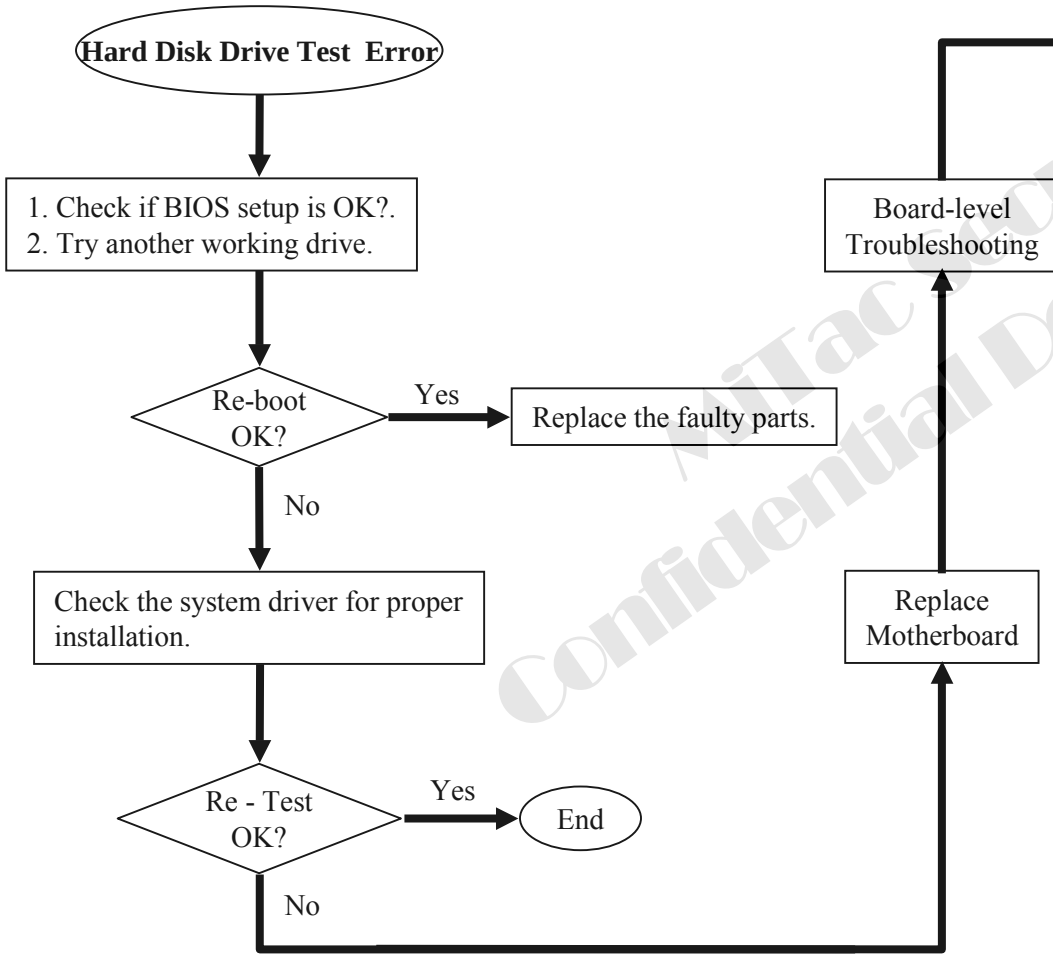
8.7 Hard Disk Drive Test Error(1)

Either an error message is shown, or the drive motor spins non-stop, while reading data from or writing data to hard disk.



8.7 Hard Disk Drive Test Error(2)

Either an error message is shown, or the drive motor spins non-stop, while reading data from or writing data to hard disk.



One of the following parts or signals on the motherboard may be defective, use an oscilloscope to check the signals or replace the parts one at a time and test after each replacement.

Parts:	Signals:
U510	5VS_HD
U7	-HDD_LED
Q10	IDE_PDD[0..15]
Q13	-PCI_RESET
L28	-PCI_RST
R123	-IDE_RST
R153	IDE_PDA[0..2]
C310	-IDE_PDDACK
C326	IDE_PIORDY
C327	-IDE_PDIOR
J513	-IDE_PDIOW
	IDE_PDDREQ
	-IDE_PDCS[1,3]
	IDE_IRQ14

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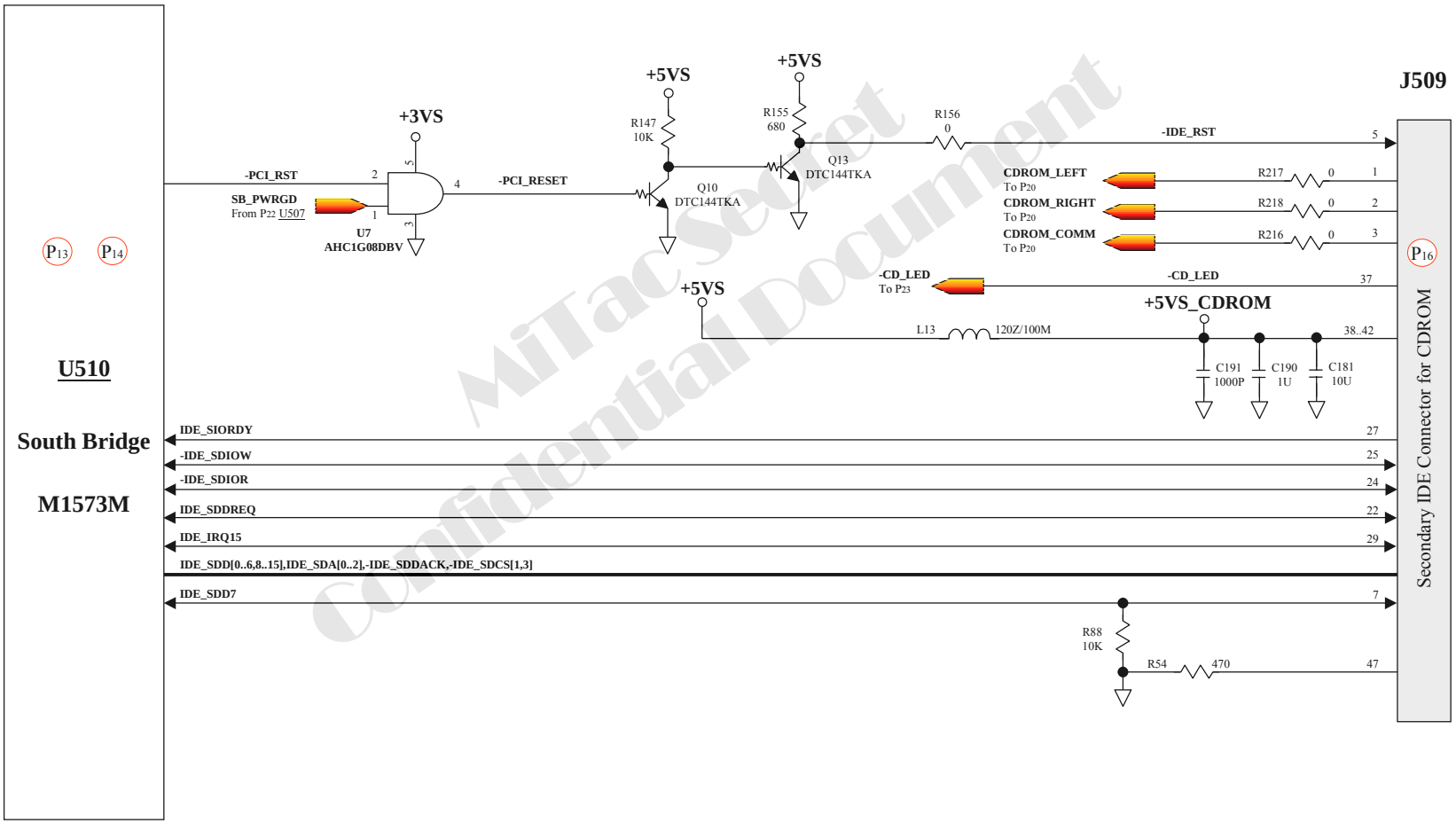
8.8 CD-ROM Drive Test Error(1)

An error message is shown when reading data from CD-ROM drive.



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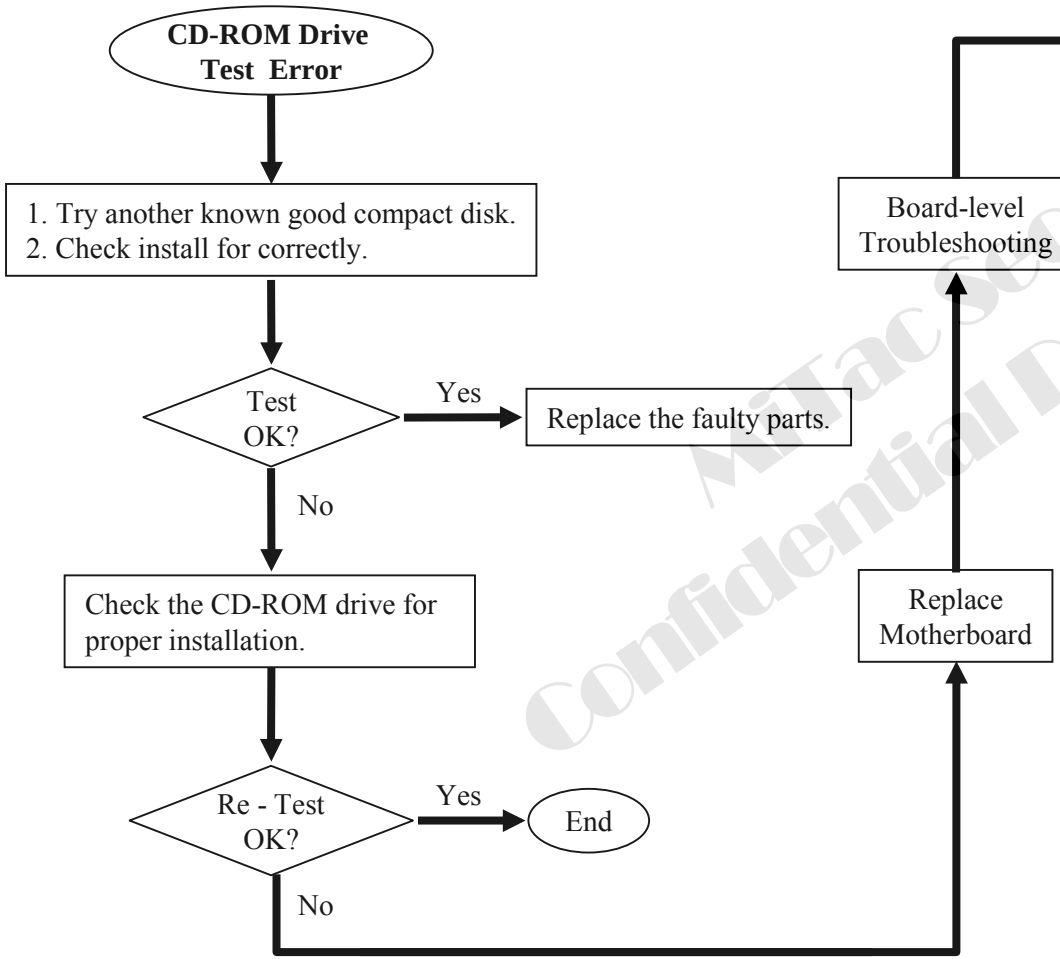
8.8 CD-ROM Drive Test Error(2)

An error message is shown when reading data from CD-ROM drive.



One of the following parts or signals on the motherboard may be defective, use an oscilloscope to check the signals or replace the parts one at a time and test after each replacement.

Parts:	Signals:
U510	+5VS
U7	+5VS_CDROM
Q10	-CD_LED
Q13	IDE_SDD[0..15]
J509	-IDE_RST
R216	IDE_SDA[0..2]
R217	IDE_IRQ15
R218	-IDE_SDDACK
R88	IDE_SIORDY
R54	-IDE_SDIOW
L13	IDE_SDDREQ
C181	-IDE_SDIOR
C190	-IDE_SDCS[1,3]
C191	CDROM_COMM
	CDROM_LEFT
	CDROM_RIGHT

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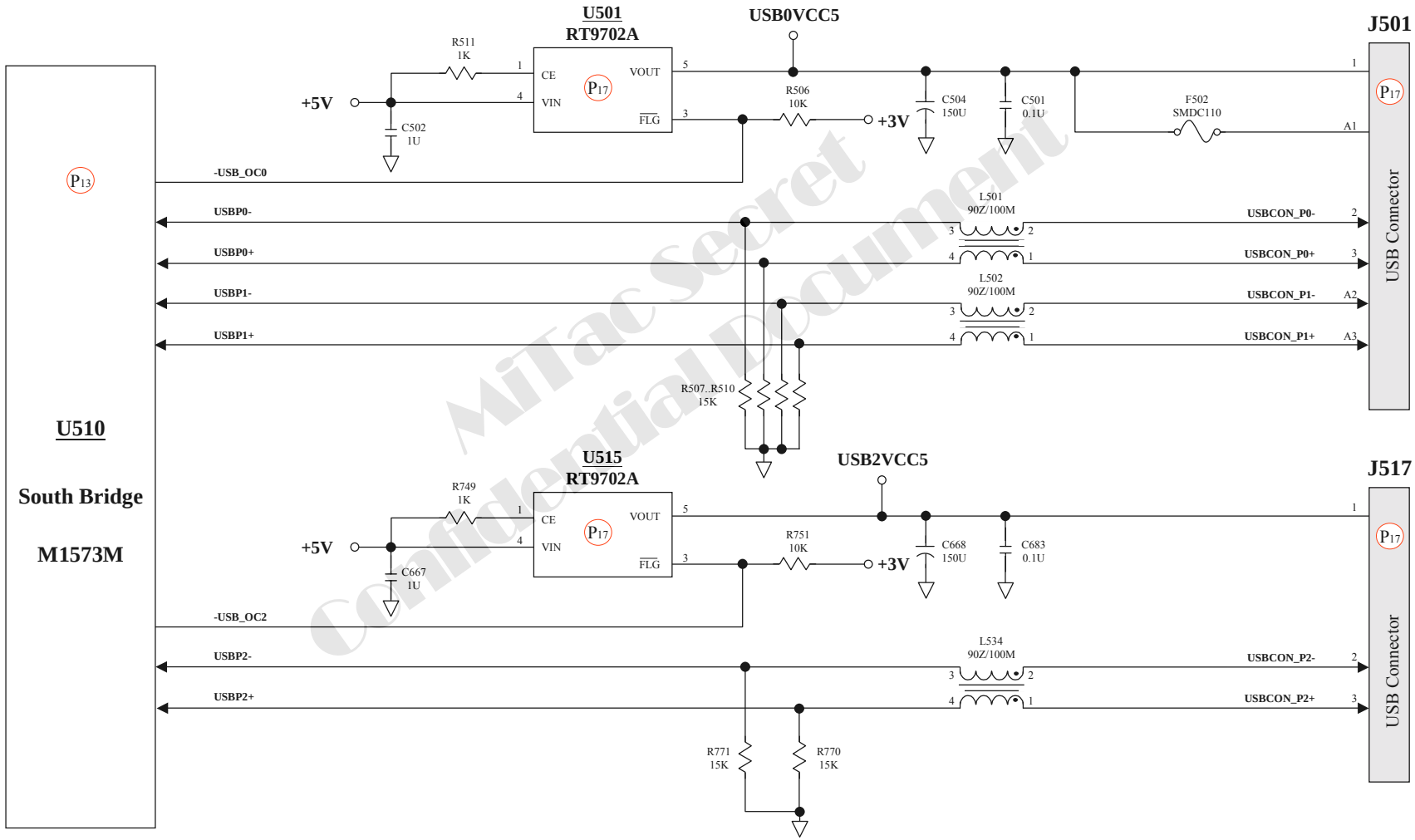
8.9 USB Test Error(1)

An error occurs when a USB I/O device is installed.



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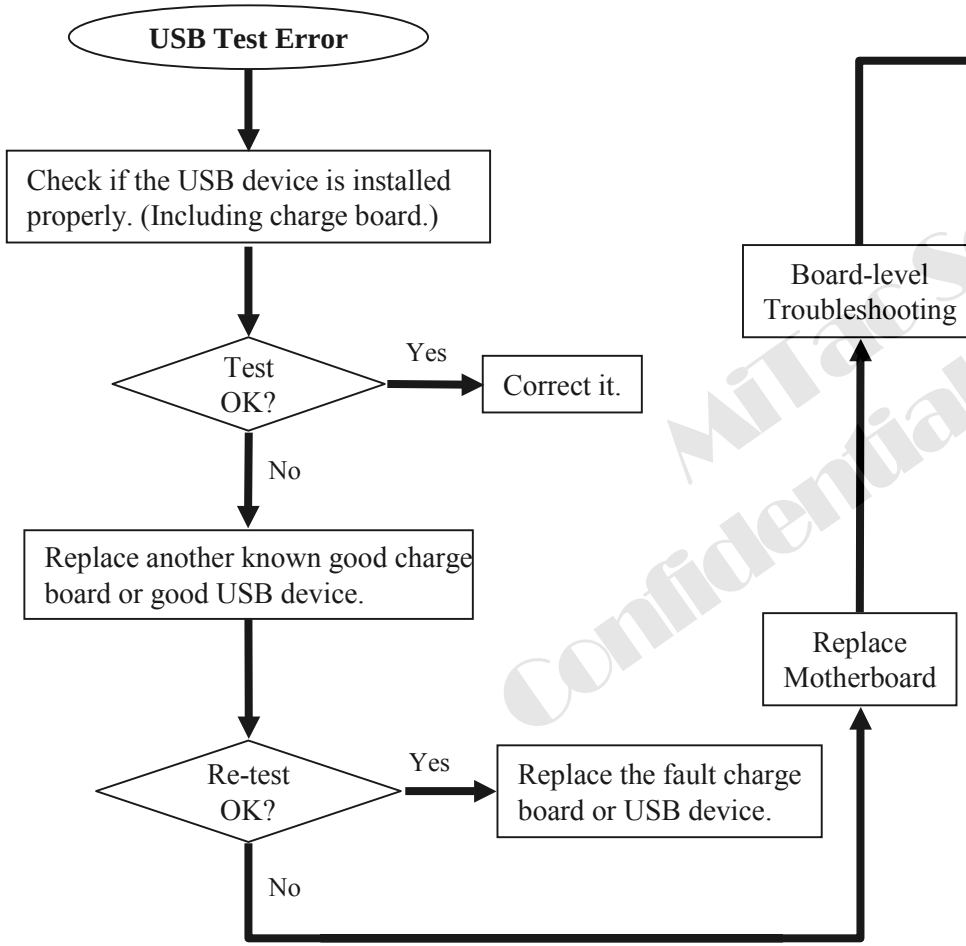
8.9 USB Test Error(2)

An error occurs when a USB I/O device is installed.



Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:	**Signals:**
U510	+5V
J501	+3V
J517	-USB_OC0
F502	-USB_OC2
U501	USBP[0..2]+
U515	USBP[0..2]-
C504	USBCON_P[0..2]+
C668	USBCON_P[0..2]-
L501	
L502	
L534	
R507..R510	
R770	
R771	

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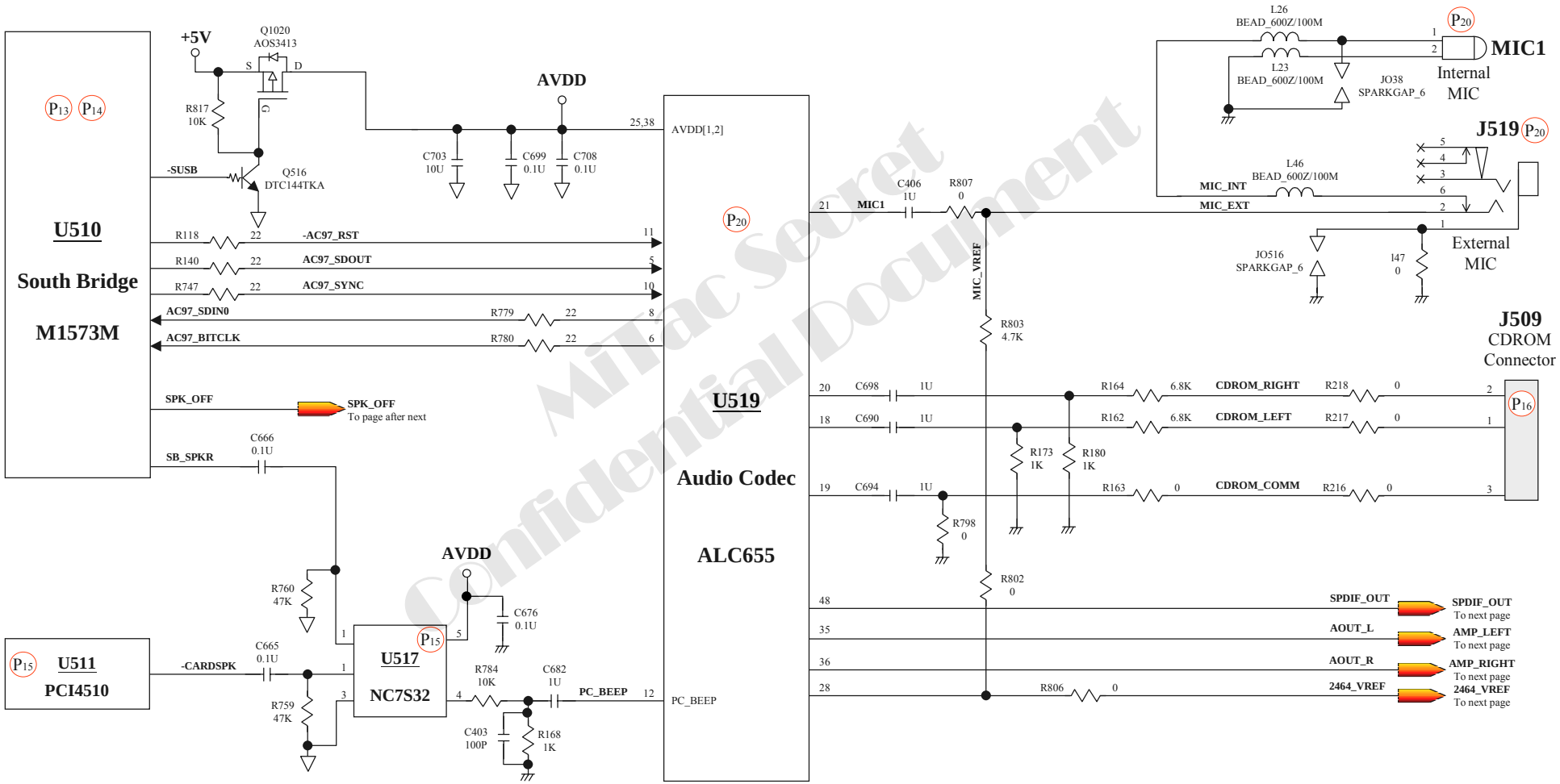
8.10 Audio Test Error(1) – Audio IN

No sound from speaker after audio driver is installed.



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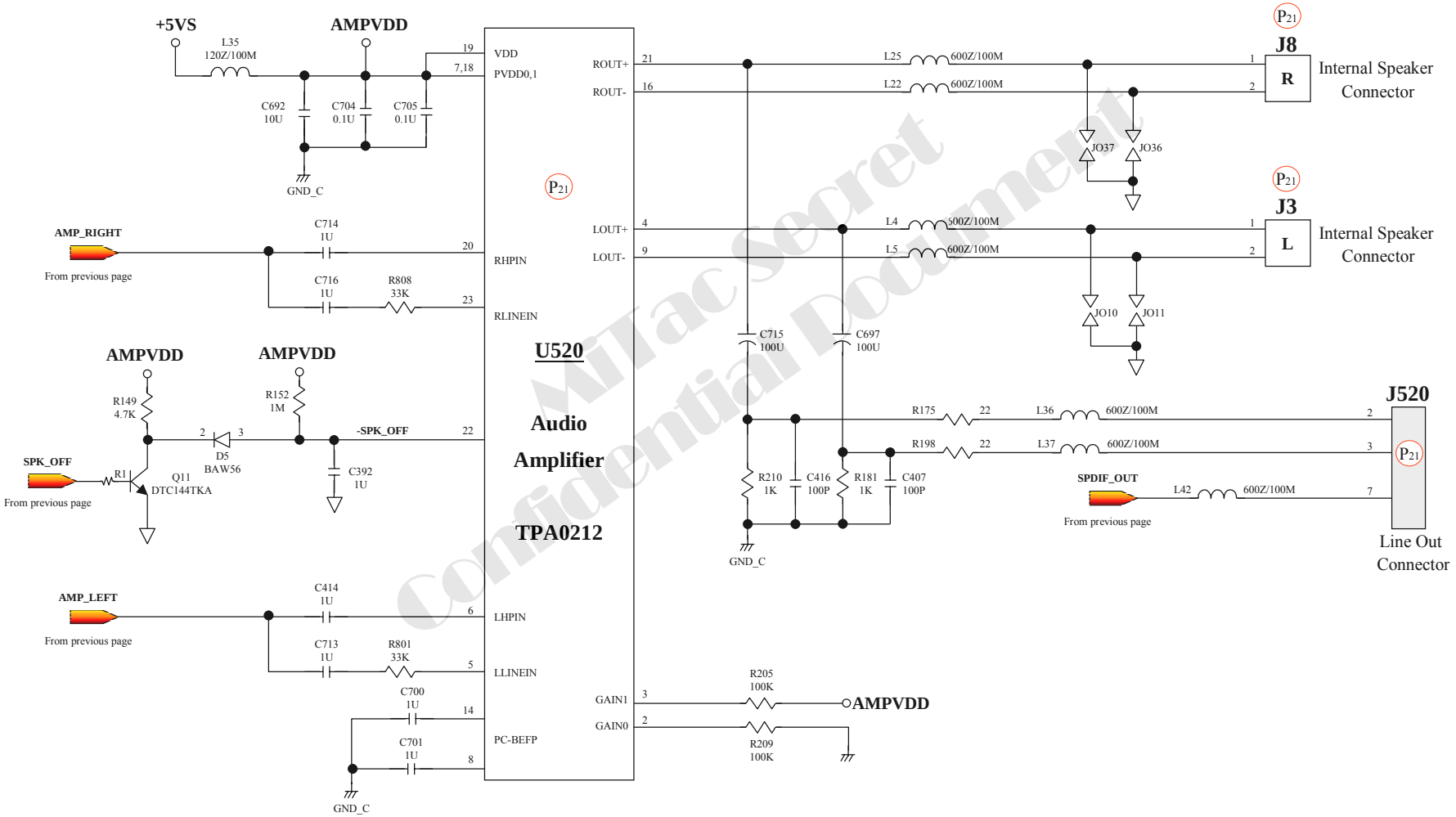
8.10 Audio Test Error(2) – Audio OUT-1

No sound from speaker after audio driver is installed.



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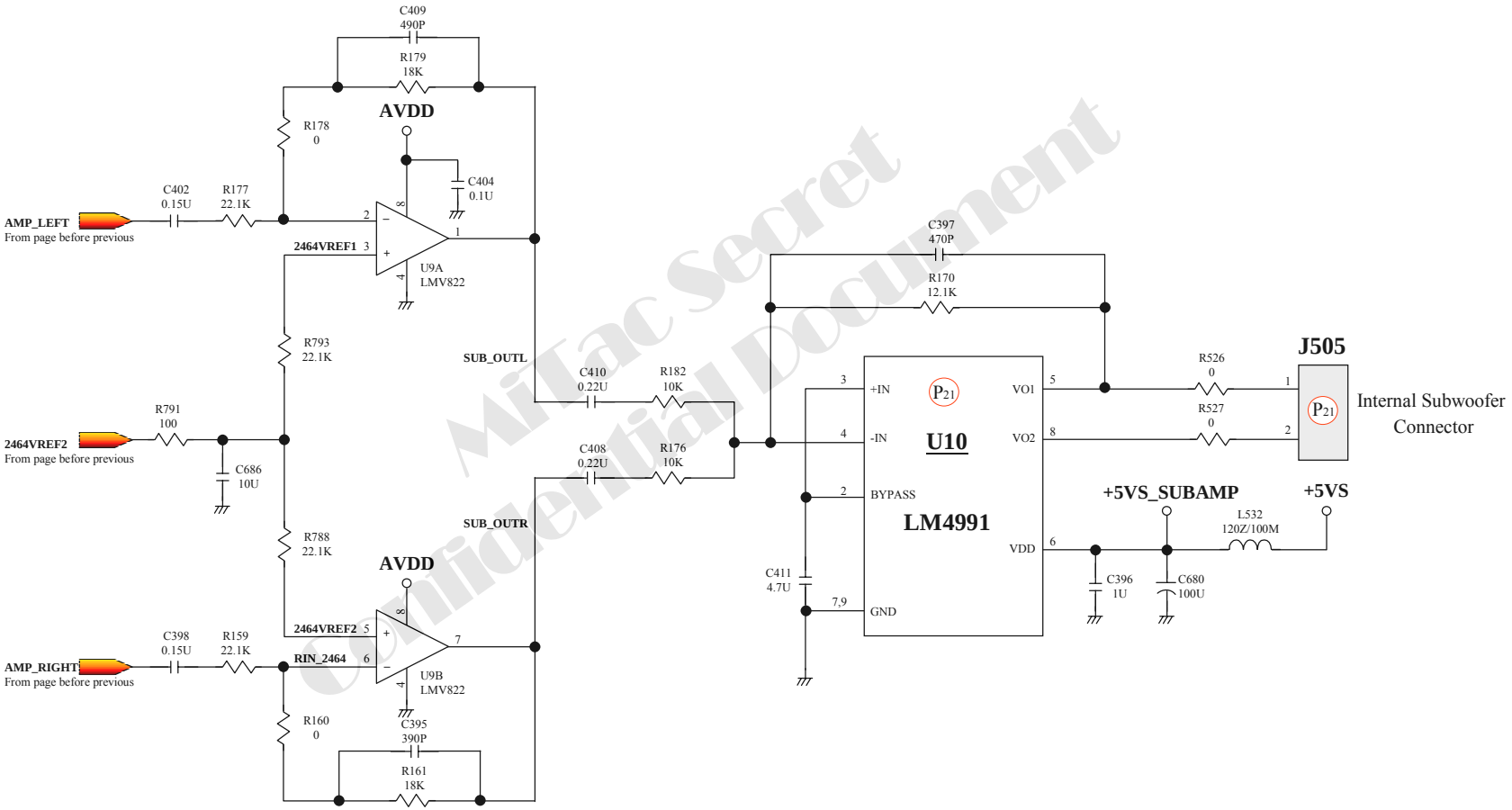
8.10 Audio Test Error(3) – Audio OUT-2

No sound from speaker after audio driver is installed.



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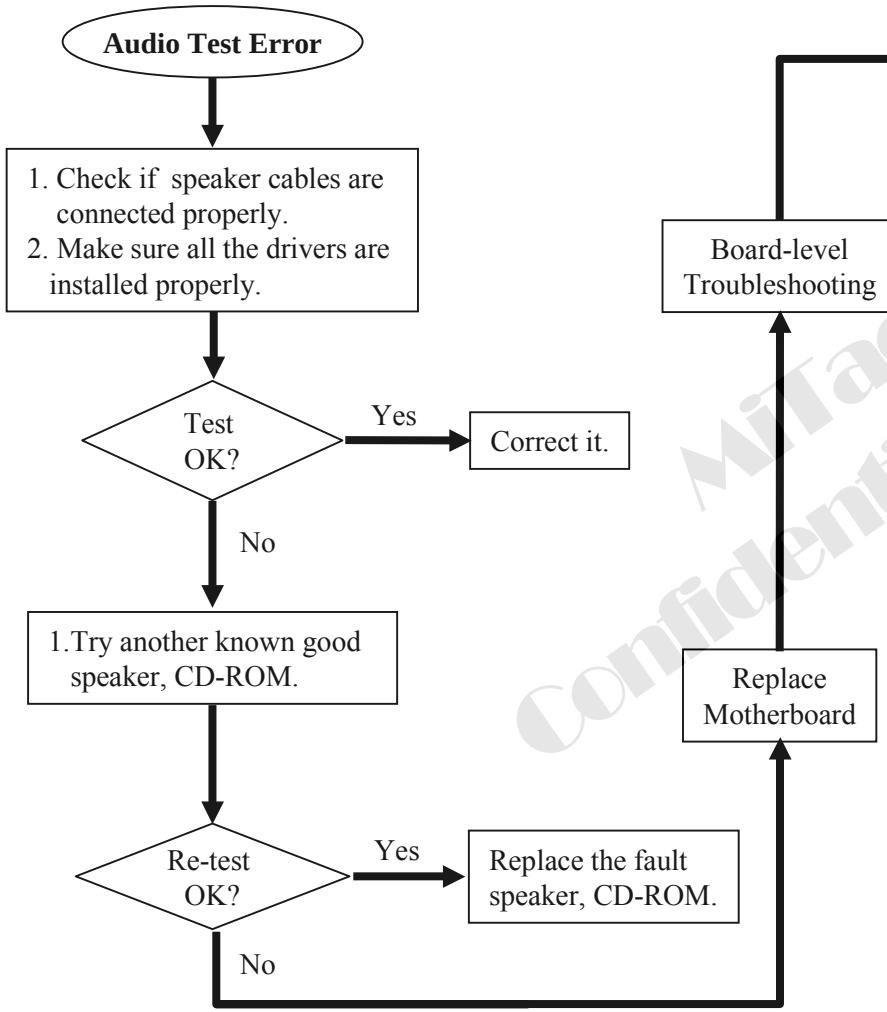
8.10 Audio Test Error(4)

No sound from speaker after audio driver is installed.



Check the following parts for cold solder or one of the following parts on the motherboard may be defective,use an oscilloscope to check the following signal or replace parts one at a time and test after each replacement.

1.If no sound cause of line out, check the following parts & signals:

Parts:	Signals:
U510	ROUT+/-
U511	TOUT+/-
U519	SPK_OFF
U520	AMP_LEFT
J8	AMP_RIGHT
J3	SPDIF_OUT
J20	
L26	
L27	
L35	
LQ11	
D5	

2. If no sound cause of MIC, check the following parts & signals:

Parts:	Signals:
U510	MIC_EXT
U511	MIC_INT
U519	MIC_VREF
J519	
MIC1	
C406	
R807	
L46	
L23	
L26	

3. If no sound cause of CD-ROM, check the following parts & signals:

Parts:	Signals:
U510	CDROM_LEFT
U511	CDROM_RIGHT
U519	CDROM_COMM
J520	
R162	
R163	
R164	
R173	
R180	
R798	

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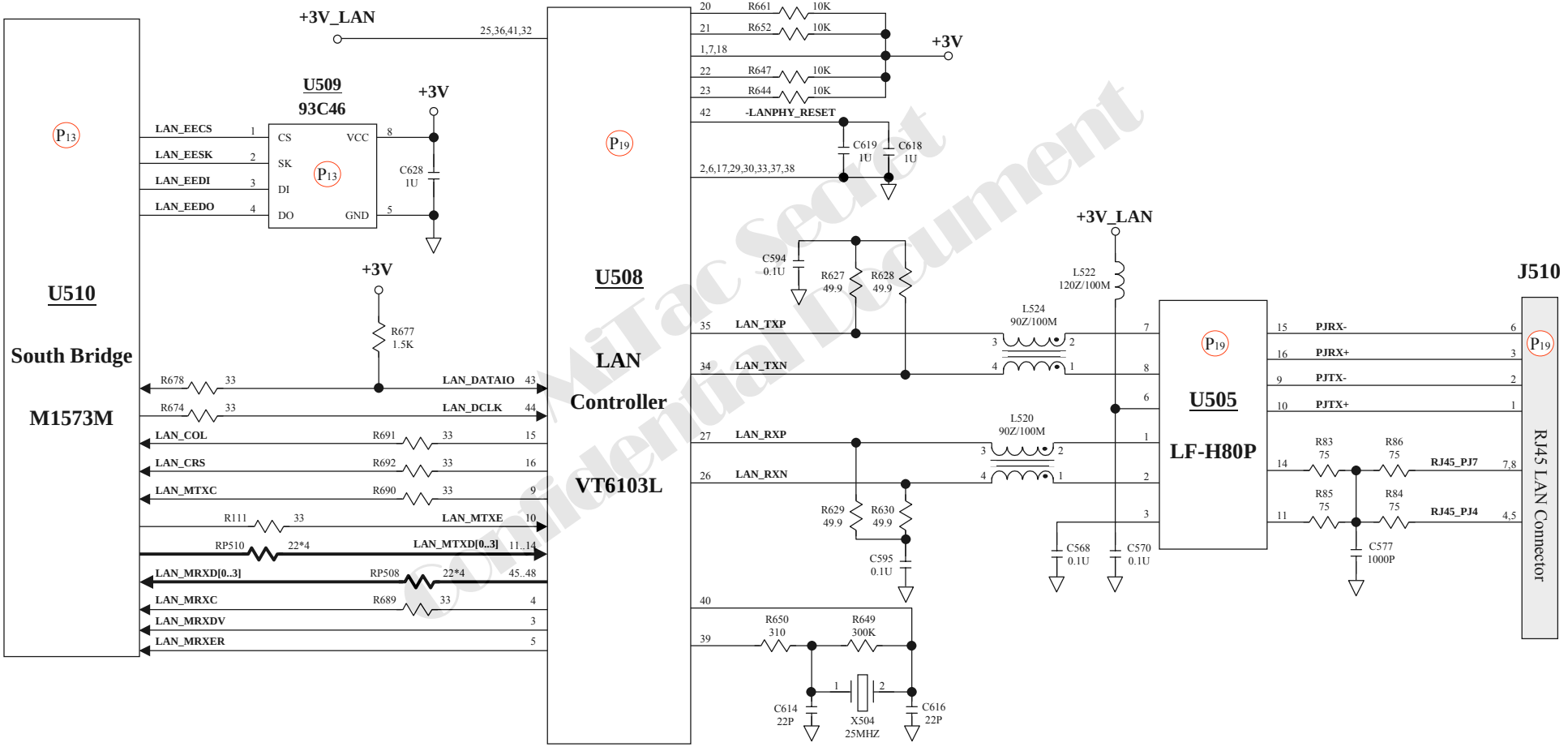
8.11 LAN Test Error(1)

An error occurs when a LAN device is installed.



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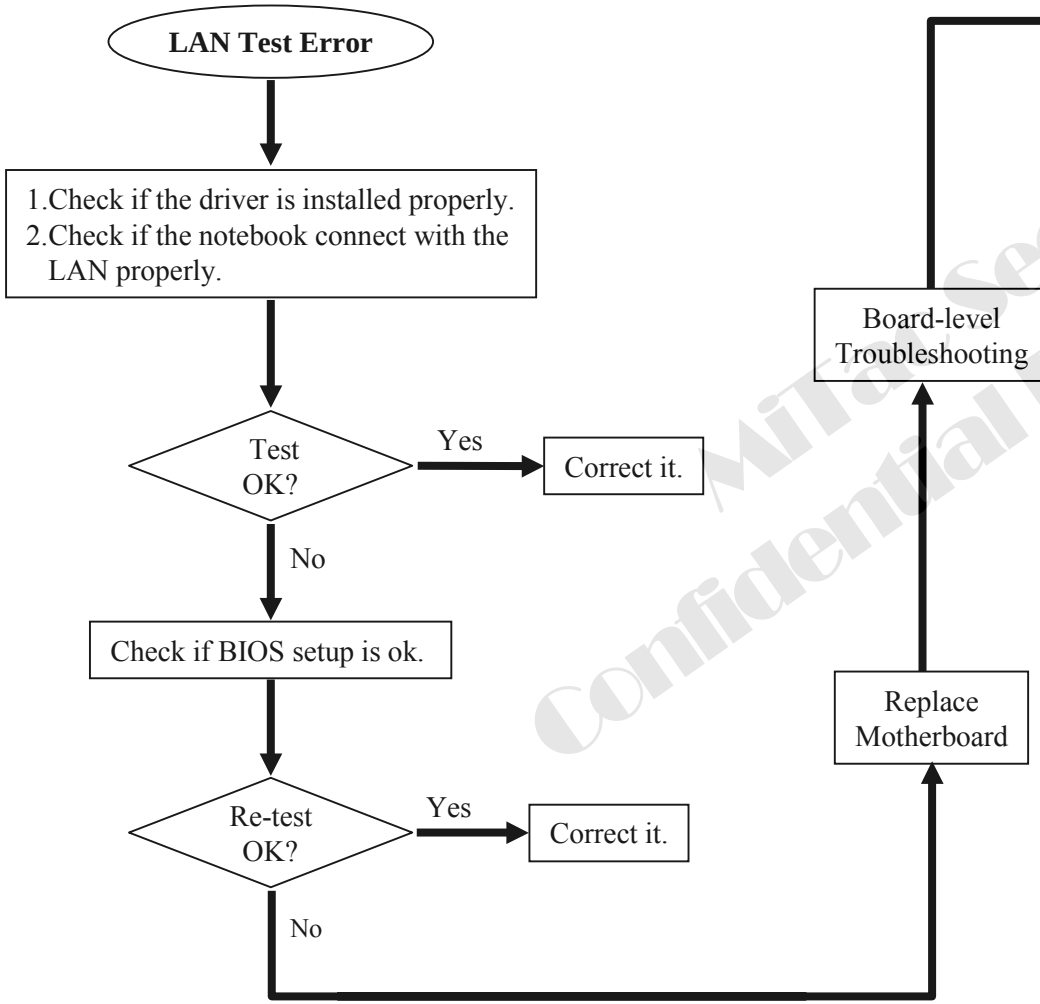
8.11 LAN Test Error(2)

An error occurs when a LAN device is installed.



Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:

U510
U505
U508
U509
J510
L520
L524
L522
X504
C614
C616
R649
R650

Signals:

+3V
+3V_LAN
LAN_DATAIO
LAN_DCLK
LAN_COL
LAN_CRS
LAN_MTXC
LAN_MTXE
LAN_MTXD[0..3]
LAN_MRXD[0..3]
LAN_MRXDV
LAN_MRXER
LAN_MRXC
-LANPHY_RESET
LAN_TXP
LAN_TXN
LAN_RXP
LAN_RXN
LAN_EECS
LAN_EESK
LAN_EEDI
LAN_EEDO
PJRX+,PJRX-
PJTX+,PJRX-

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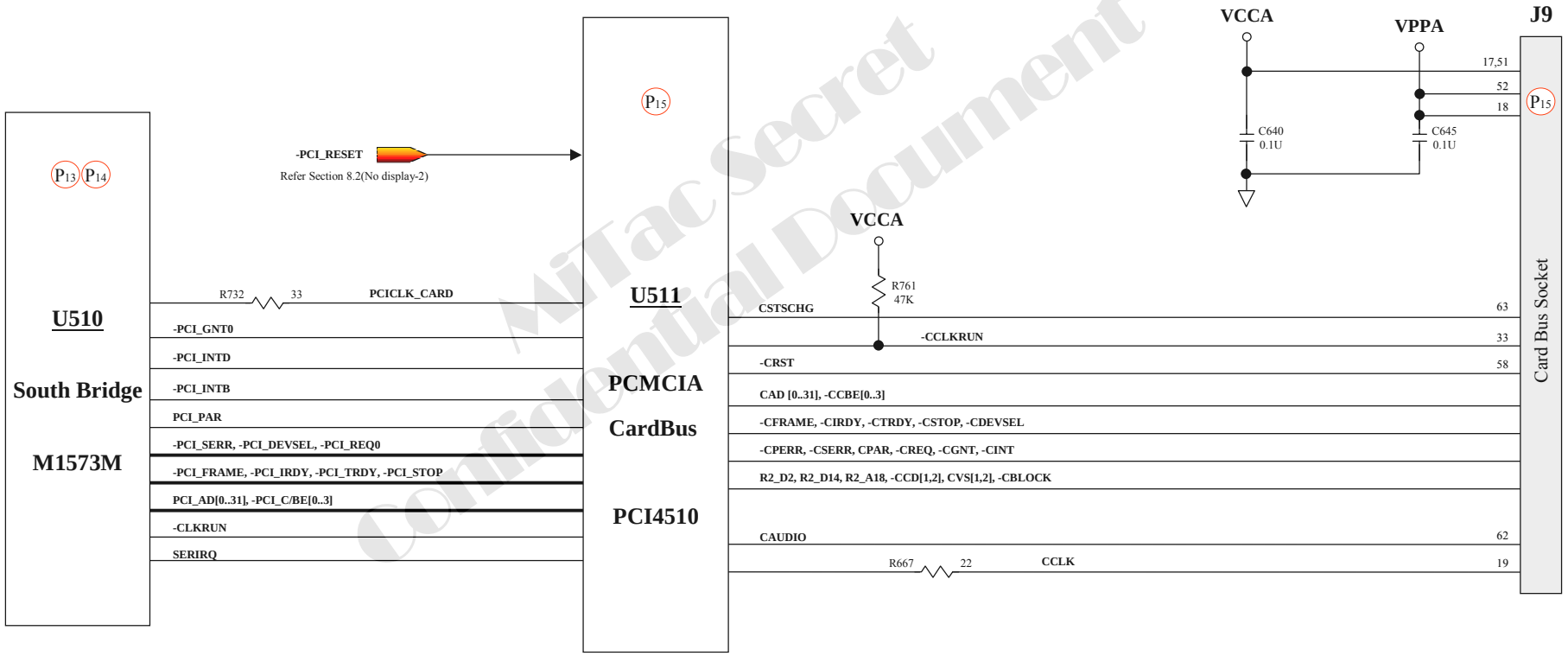
8.12 PC Card & Card Reader Socket Test Error(1)

An error occurs when a PC Card device is installed.



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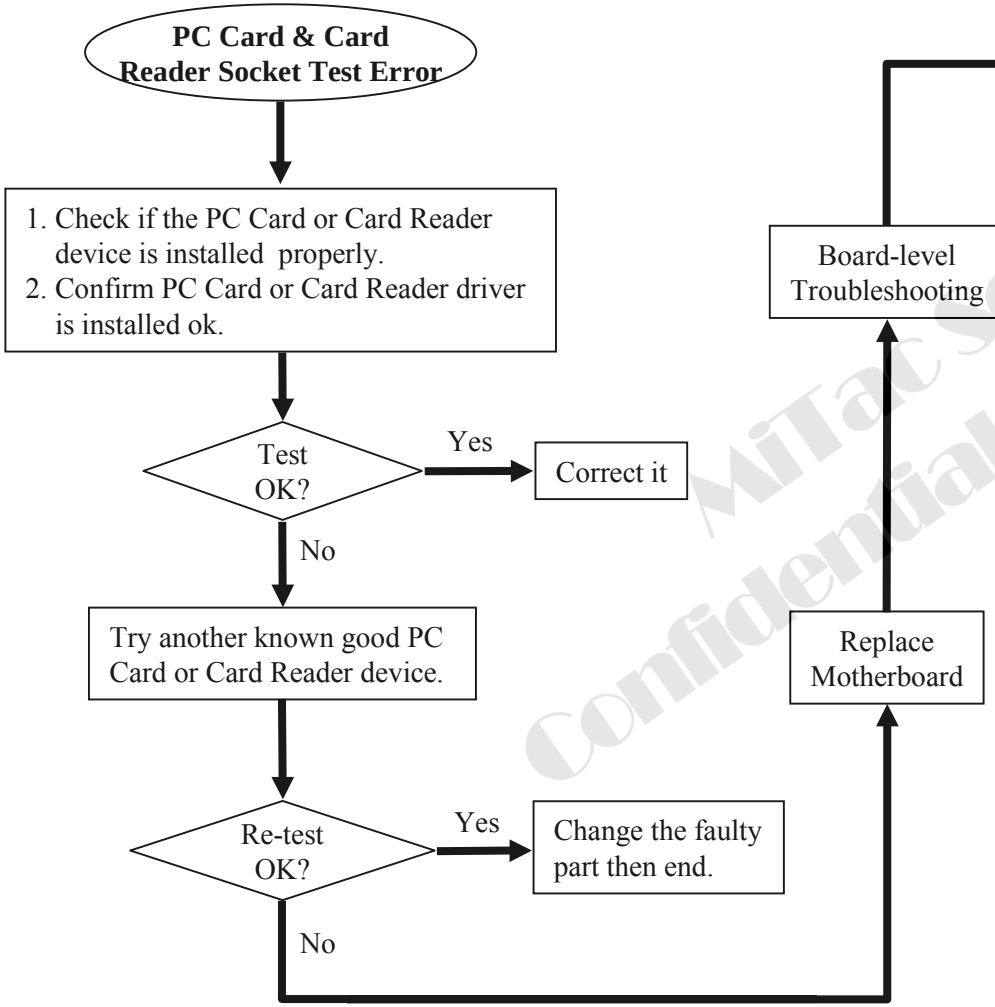
8.12 PC Card & Card Reader Socket Test Error(2)

An error occurs when a PC Card or SD Card device is installed.



Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:	**Signals**	
U510	-PCI_INTB	-PCI_IRDY
U511	-PCI_INTD	-PCI_TRDY
J9	-PCI_REQ0	-PCI_STOP
R761	-PCI_GNT0	PCI_AD[0..31]
C640	-PCI_SERR	-PCI_C/BE[0..3]
C645	-PCI_PERR	SERIRQ
R667	-PCI_DEVSEL	-CLKRUN
C1229	PCI_PAR	VCCA
	-PCI_FRAME	VCCP

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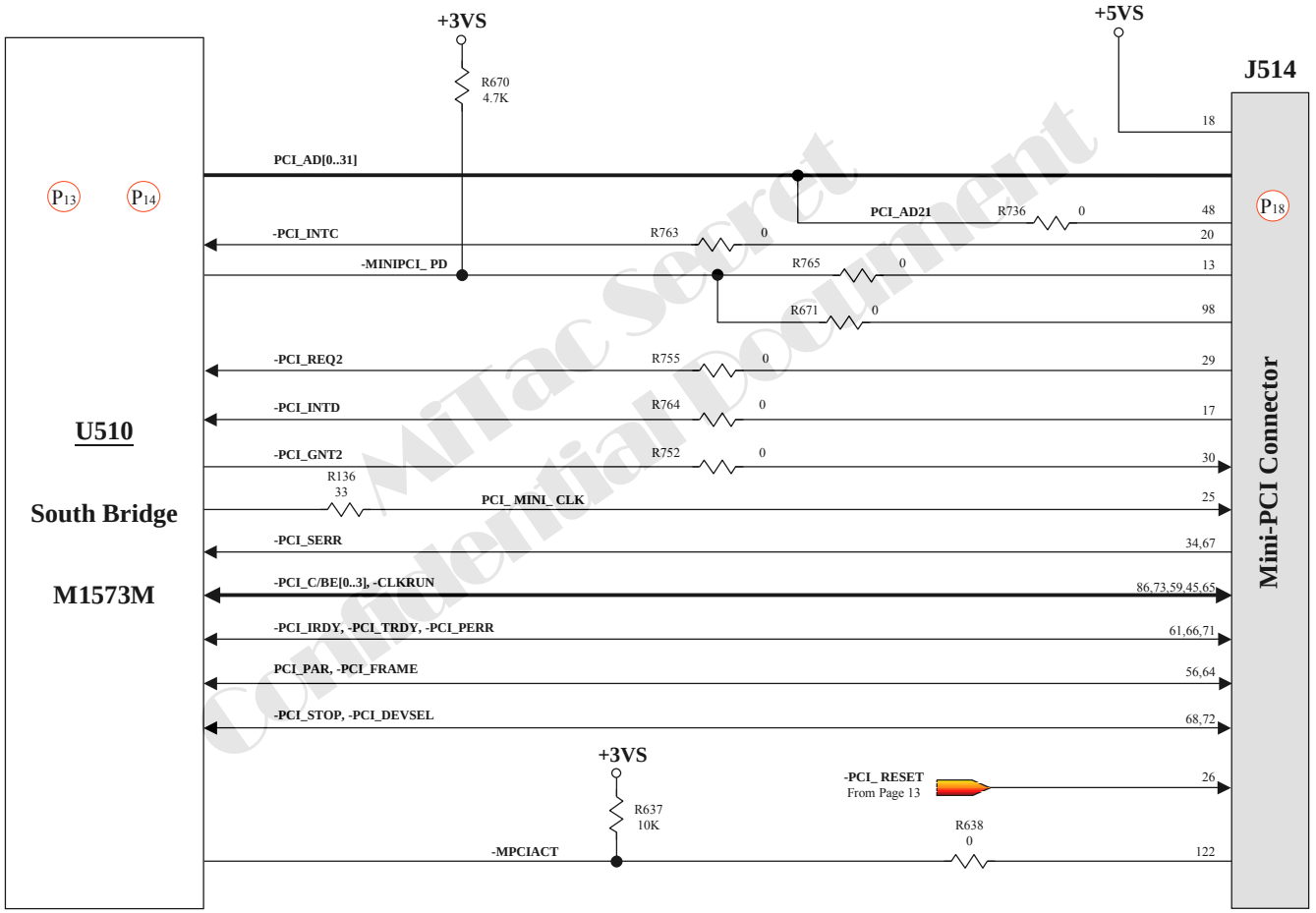
8.13 Mini-PCI Socket Test Error(1)

An error occurs when a PC Card device is installed.



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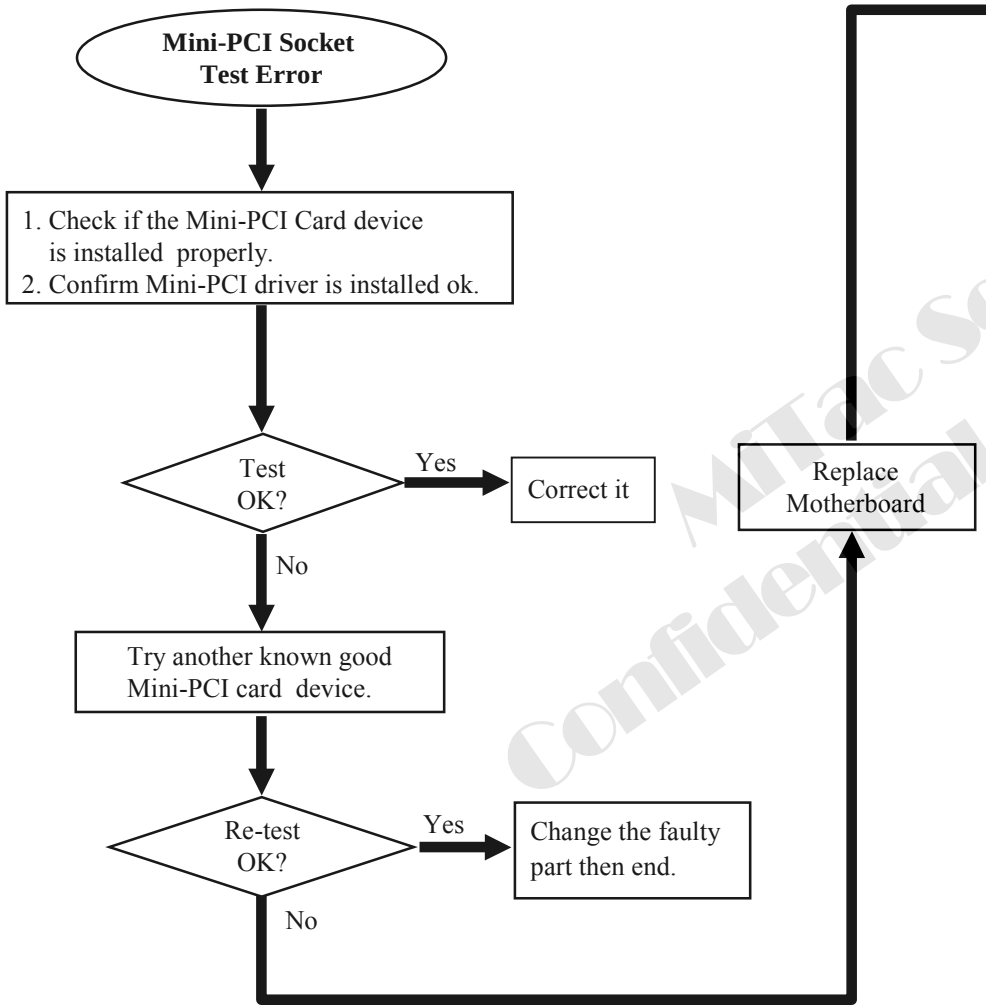
8.13 Mini-PCI Socket Test Error(2)

An error occurs when a PC Card device is installed.



Board-level Troubleshooting

Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:	Signals	
U510	+3VS	-PCI_SERR
J514	PCI_AD[0..31]	-PCI_PERR
R752	-PCI_C/BE[0..3]	-PCI_INTD
R763	-MINIPCI_PD	PCI_PAR
R736	-PCI_GNT2	-PCI_FRAME
R637	PCI_MINI_CLK	-PCI_TRDY
R764	-PCI_REQ2	-PCI_STOP
R638	-PCI_IRDY	-PCI_DEVSEL
R670	-CLKRUN	
R136		

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9. Spare Parts List(1)

Part Number	Description	Location(S)
221673120003	CARTON;N-B,8060	
221673140001	BOX;AK,8060	
221673150001	PARTITION;AK BOX,8060	
221673150002	CARD BOARD;FRAME,PALLET,8060	
221673150003	CARD BOARD;TOP/BTM,PALLET,8060	
221673150004	PARTITION;PALLET,8060	
222503220001	PE BUBBLE BAG;BATTERY,GRAMPUS	
222600020049	PE BAG;50*70MM,W/SEAL,COMMON	
222600020310	PE BAG;70X100MM,W/SEAL,COMMON	
222670820003	PE BAG;L560*W345,7521N	
222671330003	PE BAG;LCD BRACKET,STINGRAY	
222671330003	PE BAG;LCD BRACKET,STINGRAY	
222671620001	PE BUBBLE BAG;CD-ROM HOUSING,8175	
224670830002	PALLET;1250*1080*130,7521N	
225600000054	TAPE;INSULATING,POLYESTER FILM,17.5MM,13	
225600000061	TAPE;ADHENSIVE,DOUBLE-FACE,W20,UL,PRC	
225681320001	TAPE;3M,1350F,W6,YELLOW,PWR	
225681320001	TAPE;3M,1350F,W6,YELLOW,PWR	
227680900002	PAD;LCD/KB,8050	
227680900003	END CAP;NORMAL,L/R,8050	
242600000157	LABEL;BAR CODE,125*65,COMMON	
242664800013	LABEL;CAUTION,INVERT BD,PITCHING	
242669600005	LABEL;LOT NUMBER,RACE	
242669900009	LABEL;BLANK,60*80MM,7170	
242680900007	LABEL;17.3*5MM,BLANK,PWR	

Part Number	Description	Location(S)
242680900013	LABEL;BATT,11.1V/6.6AH,LI,PANASONIC,8050	
242683700006	LABEL;48*6mm,EMPTY,WHITE,MIO 136 BATT,P	
271044100101	RES;0.010,1.5W, 1%,2512,SMT;PWR	R6
271045507103	RES;0.050,1W, 1%,2512,SMT, only KOA;PWR	R24,R24A,R24C
271071101301	RES;100 ,1/16W,5% ,0603,SMT	R11,R12,R14,R15,R16,R20,R21
271071102302	RES;1K ,1/16W,5% ,0603,SMT	R11
271071103302	RES;10K ,1/16W,5% ,0603,SMT	R2
271071103302	RES;10K ,1/16W,5% ,0603,SMT	R5,R7,R8
271071104101	RES;100K ,1/16W,1% ,0603,SMT	R18,R22,R23,R9
271071104302	RES;100K ,1/16W,5% ,0603,SMT	R7
271071105301	RES;1M ,1/16W,5% ,0603,SMT	R10,R3
271071122102	RES;1.2K ,1/16W,1% ,0603,SMT	R14B
271071124101	RES;120K ,1/16W,1% ,0603,SMT	R6
271071151101	RES;150 ,1/16W,1% ,0603,SMT	R14A
271071154311	RES;154K ,1/16W,1% ,0603,SMT	R1
271071201301	RES;200 ,1/16W,5% ,0603,SMT	R1A,R1B
271071202301	RES;2K ,1/16W,5% ,0603,SMT	R12
271071224301	RES;220K ,1/16W,5% ,0603,SMT	R1
271071301311	RES;301K ,1/16W,1% ,0603,SMT	R13,R3
271071331301	RES;330 ,1/16W,5% ,0603,SMT	C14
271071432111	RES;4.32K,1/16W,1% ,0603,SMT	R10
271071499311	RES;499K ,1/16W,1% ,0603,SMT	R17
271071753301	RES;75K ,1/16W,5% ,0603,SMT	R8
271072474101	RES;470K ,1/10W,1% ,0603,SMT	R4,R5
272005104705	CAP ;1U CR 50V +80-20% 0805 Y5V SMT only TDK	C14A,C14B,C4A,C4B

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9. Spare Parts List(2)

Part Number	Description	Location(S)
272010560301	CAP;56P,2KV,5%,1206,NPO,SMT,only HolyStone	
272010560302	CAP;56P,2KV,5%,1206,NPO,SMT,only JOHANSON	C18
272012105401	CAP;1U ,CR,16V,10%,1206,X7R,SMT	C14A,C14B
272023475502	CAP;4.7U ,CR,25V,20%,1210,X7R,SMT	C1
272071105403	CAP;1U ,10V,10%,0603,X5R,SMT	C10,C4
272071332401	CAP;.33U ,10V,10%,0603,X7R,SMT	C2
272072104402	CAP;.1U ,CR,16V,10%,0603,X7R,SMT	C12,C17,C6
272072824401	CAP;.082U ,16V,10%,0603,X7R,SMT	C16
272073104401	CAP;.1U ,CR,25V,10%,0603,X7R,PRC	C22,C7
272073223401	CAP;.022U,CR,25V,10%,0603,X7R,SMT	C9
272075101401	CAP;100P ,50V,10%,0603,COG,SMT	C20,C21
272075101404	CAP; 0.001U CR 50V 10% 0603 X7R SMT only TDK	C13
272075103401	CAP;.01U ,CR,50V,10%,0603,X7R,SMT	C11,C13,C3,C8
272075103408	CAP ;0.1U CR 50V 10% 0603 X7R SMT only TDK	C10,C11,C12,C15
272075222401	CAP;2200P,50V,10%,0603,X7R,SMT	C5
272075223702	CAP; 0.22U CR 50V +80-20% 0603 Y5V SMT only TD	C1,C2,C20A,C24,C25
272075331401	CAP;330P ,CR,50V,10%,0603,X7R,SMT	C15B
272075471409	CAP; 0.0047U CR 50V 10% 0603 X7R SMT only TDK	C4
272075472701	CAP;4700P,50V ,+ -20%,0603,X7R,SMT	C15A
272990100301	CAP;10P,3000V,+- 5%,NPO,SMT	C19
273001050160	XFMR;CI8.5,25T/2150T,300mH,ONLY TMP,PWR	T1
273001050188	XFMR;CI8.5,25/2150,290mH,ONLY SHOU BANG,PW	
281101015001	IC;MP1015EM-Z,CCFL CTRL,TSSOP20,MPS	U1
283467530001	IC;EEPROM,S24CC02A,2K,SO8,SMT,ONLY SEIKO;P	
283467540001	IC;EEPROM,M24C02-WMN6T,2K,SO8,SMT	IC2

Part Number	Description	Location(S)
286002040001	IC;BQ2040,GAS GAUGE,SO,16P,SMT	IC1
286300812002	IC;S-812C,DECECTOR,SOT-89,PRC	IC3
286301414001	IC;MM1414,PROTECTION,TSOP-20A,PRC	IC4
288100056005	DIODE;UDZ5.6B,ZENER,5.6V,UMD2,SMT	ZD3,ZD4
288110355001	DIODE;1SS355,80V,100mA,SOD-23,SMT	D2
288111544001	DIODE; 1SR-154-400 400V 1.0A SMT	D1
288200144008	TRANS;DTA144EKA,PNP,SMT	Q1
288204409001	TRANS;AO4409,P-MOSFET,SO-8P,MSL,PWR	Q3,Q5
291000000203	CON;HDR,MA,2P*1,3.5MM,R/A,SMT,SM02B,only AC	J2
291000020204	CON;HDR,MA,2P*1,3.5MM,R/A,SMT,SMO2B	
291000021105	CON;HDR,MA,11P*1,ACES,87213-1100,SMT	CN1
295000010140	FUSE;FAST,2A,63VDC,1206,SMT,0433002	F1
310111103029	THERMISTOR;10K,1%,BN35-3H103F,180.5mm,MIT	RT1
316680900006	PCB;PWA-8050/BATT ,PR AND GA BD,PWR	
316681301001	PCB;PWA-INVERTER BD(DA-1A08-N02)/MIC;PWR	R0A
323768710001	DDR SODIMM MODULE;DDR333 256MB PC2700 CL	
324180787123	IC;CPU,AMD-Turion 64,1600MHZ,TMSMT30BQX5L	
331000007025	CONNECTOR;7 PIN,DIP,ALLTOP,C10345-10701	CON1
332110020173	WIRE ;#20AWG,UL1007,L=256mm,BLACK,PWR	CN4
332110026150	WIRE ;#26AWG,UL1007,L=212mm,BLUE,PWR	CN2
332110026151	WIRE ;#26AWG,UL1007,L=146mm,YELLOW,PWR	CN3
332160020008	WIRE;#20,UL1007,113MM,RED,YIYI;PWR	CN1
332810000033	PWR CORD;125V/7A,2P,BLACK,AMERICA	
333025000005	SHRINK TUBE;300V,125,I.D=2.5,T=0.15,L=13,BLAC	
333050000117	SHRINK TUBE;UL,600V,105'C,ID2.5*7MM,8175	

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9. Spare Parts List(3)

Part Number	Description	Location(S)
333050000117	SHRINK TUBE;UL,600V,105'C,ID2.5*7MM,8175	
335152000044	CFM-BAT;FUSE THERMAL 98'C	
335152000085	FUSE; 128 DC-7A/50V 139℃only UCHIHASHI（内橋	F2
335152000097	FUSE;LR4-73X,POLY SWITCH,PWR	
338536010053	TF041-BATTERY;LI,3.6V/2.2AH,CGR18650C,PAN,P	
340680900002	SPEAKER ASSY;L,8050	
340680900003	SPEAKER ASSY;R,8050	
340680900004	COVER ASSY;8050	
340680900006	BRACKET ASSY;SYSTEM,8050	
340680900009	BRACKET ASSY;TP,8050	
340680900011	HOUSEING ASSY;LCD,8050	
340680900012	COVER ASSY;LCD,8050	
340680900015	BEZEL ASSY;COMBO,MKE,730,8050	
340680900026	SHIELDING ASSY;HDD,8050	
340680900028	WIRE ASSY;INVERTER,8050	
340680900034	SPEAKER ASSY;WOOFER,NEW,8050	
340687800006	HEATSINK;ASSY,RHEA-A	
340687800008	HEATSINK;ASSY,ALRO,RHEA-A	
340802300001	COVER ASSY;MINIPCI,8350	
340802300002	COVER ASSY;HDD,8350	
340802300003	HOUSING ASSY;8350	
340802300004	SHIELDING ASSY;COVER,8350	
341680900001	SPC SCREW;#4-1/4,8050	
341687800004	SCREW;SPRING,CPU,RHEA-A	
342503400007	CONTACT PLATE;W5L45T0.13 ,1/3T,7170LI,PRC	

Part Number	Description	Location(S)
342672200010	BRACKET;CD-ROM,8500	
342680900005	HINGE;R,8050	
342680900006	HINGE;L,8050	
342680900010	CONTACT PLATE;W5L102T0.13mm,8050 ID BATT	
342682300001	CONTACT PLATE;W5L104T0.13,PWR	
342686900019	T-SCREW;M26L6_5,8066	
344680900009	COVER;REAR,R,8050	
344680900010	COVER;REAR,L,8050	
344680900011	COVER;HINGE,R,8050	
344680900048	DUMMY CARD;PCMCIA,8050	
344680900049	COVER;HINGE,L,8050	
344680900067	COVER ;BATT,9-CELL,8050	
344680910012	HOUSING;BATTERY,9CELL,8050ID2	
344802300004	COVER;CPU,8350	
345677000018	CONDUCTIVE TAPE;LCD,LYNX	
345680900004	RUBBER;12*12*4.0T,8050MP,PWR	
346503100005	INSULATOR;5,BATTERY ASSY,7521Li	
346503200202	INSULATOR;BATT ASSY,ONE ROUND,BLAC,WEAS	
346503400301	INSULATOR;FOR 3 CELLS,DOUBLE-FA,8170LI,PRC	
346680900005	INSULATOR;INVERTER,LCD,8050	
346680900007	INSULATOR;PCB,ASSY,L105,W12T1.0 ,8050,PWR	
346680900011	MYLAR;COVER,LCD,8050	
346680900017	INSULATOR;L16W8.5T0.05MM,DIALAMY,8050,PV	
346681300001	THERMAL PAD;L17*W10*T=0.5MM,PWR	
346681300001	THERMAL PAD;L17*W10*T=0.5MM,PWR	

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9. Spare Parts List(4)

Part Number	Description	Location(S)
346681800004	INSULATOR;BATT,ASSY,L129W15T0.25MM,8677C	
361400003003	JET-MELT ADHESIVES;3478-Q,5/8in*8in,PRC	
361400003021	SOLDER CREAM;NOCLEAN,P4020870980	SOLDER CREAM
361400003030	ADHESIVE;ABS+PC PACK,G485,CEMIDAIN	
361400003249	ADHESIVE;HEAT,TRANSFER,ES2031L,PWR	
365350000003	SOLDER WIRE;0.8MM,SN43/PB43/BI14,N/C,TELEC(	
370102010201	SPC-SCREW;M2L2,NIW,K-HD,t=0.8,NLK	
370102010303	SPC-SCREW;M2L3,NIW,K-HD(+),NYLOK	
370102010409	SPC-SCREW;M2L4,K-HD(t0.3),NIB/NLK	
370102010409	SPC-SCREW;M2L4,K-HD(t0.3),NIB/NLK	
370102030301	SPC-SCREW;M2L3,K-HD,1,NIB/NLK	
370102610401	SPC-SCREW;M2.6L4,K-HD,t0.8,NIB/NLK	
370102610401	SPC-SCREW;M2.6L4,K-HD,t0.8,NIB/NLK	
370102610603	SPC-SCREW;M2.6L6,K-HD,NIB/NLK	
370102610603	SPC-SCREW;M2.6L6,K-HD,NIB/NLK	
370102611601	SPC-SCREW;M2.6*L16,NIB,K-HD	
370103010405	SPC-SCREW;M3L4,NIW,K-HD,T0.3	
371102010252	SCREW;M2L2.5,K-HEAD(+),NIB/NLK	
371102010252	SCREW;M2L2.5,K-HEAD(+),NIB/NLK	
373101713502	T-SCREW;B.M1.7L3.5,HD04t0.25,0,BCT	
411680900038	PWA;PWA-8050ID1/BATT PANASONICS CELLS,BC	
411681340001	PWA;PWA-INVERTER BD,DA-1A08-N02/Rhea A(QI	
411681340002	PWA;PWA-INVERTER BD,SMT,DA-1A08-N02/Rhea	
411681710002	PWA-PWA-BATT BD;SMT,BL3244G095/8050/P,PW	
411802300004	PWA;PWA-8350,W/O LFB,MOTHER BD	

Part Number	Description	Location(S)
412600000037	TF041-PCB ASSY;WIRELESS LAN CARD ,WLL3090(	
412682500007	PCB ASSY;FAX MODEM 56K,1456VQL4A(INT),ASK	
413000021026	LCD;B154EW01 V.5,TFT,15.4",WXGA,AU	
416280230011	LT PF;15.4",WXGA,AU,W/O LFB,8350	
422674300071	WIRE ASSY;MDC,E-NOTE	
422680900003	WIRE CABLE;SAM LTN154X1,8050	
422688000006	WIRE;ANTENNA,ASSY,L,8050QMA	
422802300001	CABLE FFC;TP,8350	
431802300002	CASE KIT;W/O LFB,8350	
441680900007	BATT ASSY;8050ID1/11.1V,2200mH,SILVER,PANAS	
441802300002	LCD ASSY;15.4",WXGA,AU,8350	
442680900012	BATT ASSY;11.1V,6.6AH,LI,3S3P,PANASONIC,8050	
442681400051	AC ADPT ASSY;19V,3.43A,HIPRO HP-OK065B03 B	
442687600001	Touch Pad;Single-Chip Atp-Ultra Thin Module Model T	
451680900031	HDD ME KIT;8050	
451680900151	ROM ME KIT;8050	
451802300032	LCD ME KIT;15.4",WXGA,AU,8350	
451802300051	HOUSING KIT;8350	
451802300052	HEATSINK ME KIT;8350	
461680900006	PACKING KIT;N-B BOX,8050	
523402379051	HDD DRIVE;40GB,2.5",MHT2040AT,V40+ FW0022,1	
523410484014	DVD COMBO DRIVE; UJ-DA760,8X24X24X24X, PA1	
523468090041	COMBO ASSY;UJDA-760,KME,8050	
523480230001	HDD ASSY;40GB,FUJI,MHT2040AT,8350	
526280230001	LTXXNON;8350ID1/T5AJ/0C04D/1XUSX	

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9. Spare Parts List(5)

Part Number	Description	Location(S)
531068780018	KBD;88,US,K011818P1,RHEA-A	
541668090009	AK;EN,8050,UTILITY ONLY	
541680230001	AK;N-B BOX,8350	
561568090025	MANUAL;QSG,EN,8050	
565168090001	S/W;CD ROM,SYSTEM DRIVER,8050	
600100010009	SOLDER WIRE;63/37,0.8,CM,N/C,PRC	
600100010009	SOLDER WIRE;63/37,0.8,CM,N/C,PRC	
624200010140	LABEL;5*20,BLANK,COMMON	
624200010140	LABEL;5*20,BLANK,COMMON	
		P/N:526280230001

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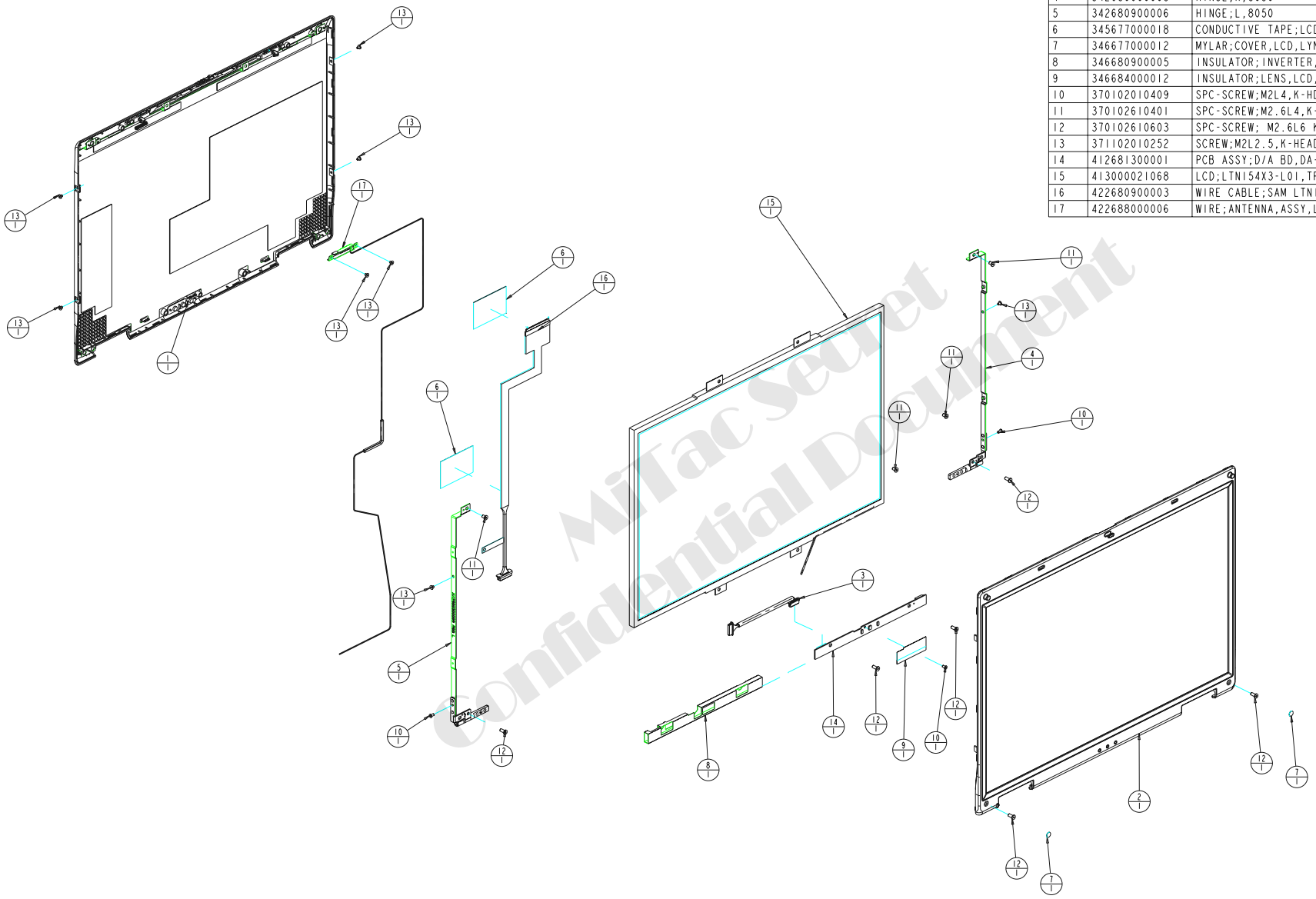

ITEM	PART NO	DESCRIPTION	Q'TY	TYPE	REMARK
1	340680900011	HOUSING ASSY;LCD,8050	1	ASSEMBLY	
2	340680900012	COVER ASSY;LCD,8050	1	ASSEMBLY	
3	340680900028	WIRE ASSY;INVERTER,8050	1	ASSEMBLY	
4	342680900005	HINGE;R,8050	1	ASSEMBLY	
5	342680900006	HINGE;L,8050	1	ASSEMBLY	
6	345677000018	CONDUCTIVE TAPE;LCD,LYNX	2	PART	
7	346677000012	MYLAR;COVER,LCD,LYNX	2	PART	
8	346680900005	INSULATOR;INVERTER,LCD,8050	1	PART	
9	346684000012	INSULATOR;LENS,LCD,8050M	1	PART	
10	370102010409	SPC-SCREW;M2L4,K-HD(±0.3),NIB/NL	3	PART	
11	370102610401	SPC-SCREW;M2.6L4,K-HD,±0.8,NIB/N	4	PART	
12	370102610603	SPC-SCREW; M2.6L6 K-HEAD,NIB/NLK	6	PART	
13	371102010252	SCREW;M2L2.5,K-HEAD(+),NIB/NLK	8	PART	
14	412681300001	PCB ASSY;D/A BD,DA-IA08-A,PWR	1	ASSEMBLY	
15	413000021068	LCD;LTN154X3-L01,TFT,15.4",WXGA,	1	PART	
16	422680900003	WIRE CABLE;SAM LTN154X1,8050	1	ASSEMBLY	
17	422688000006	WIRE;ANTENNA,ASSY,L,8050QMA	1	ASSEMBLY	

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ITEM	CONTENTS OF CHANGE	RVS	CHK	APV	M/D/Y
					/ /
					/ /
					/ /
					/ /

TOL ± RANGE	Plg	Met	Ins	Per	Cab	Pac	Gas	PCB
0-6	0.1	0.1	0.1	0.2	0.5	1	0.5	0.1
6-30	0.1	0.1	.15	.25	1	1	0.5	0.1
30-80	0.1	.15	0.2	0.3	2	1.5	1	0.1
80-180	.15	.15	.25	0.3	2	2	1	.15
180-315	.15	0.2	0.3	0.4	2.5	2	1	.15
315-800	0.2	0.3	0.4	0.5	3	3	2	.15

DATE	26-Apr-05	MATERIAL	SEE NOTES	TREATMENT		REMARK	
UNIT	MM	SCALE	0.50	DRAWING NAME	LCD ME KIT;15.4",WXGA,8350		
DRAWN	DESIGNED	CHECKED	APPROVED	MATERIAL NO.	MF 441 8023 00001 R 00		

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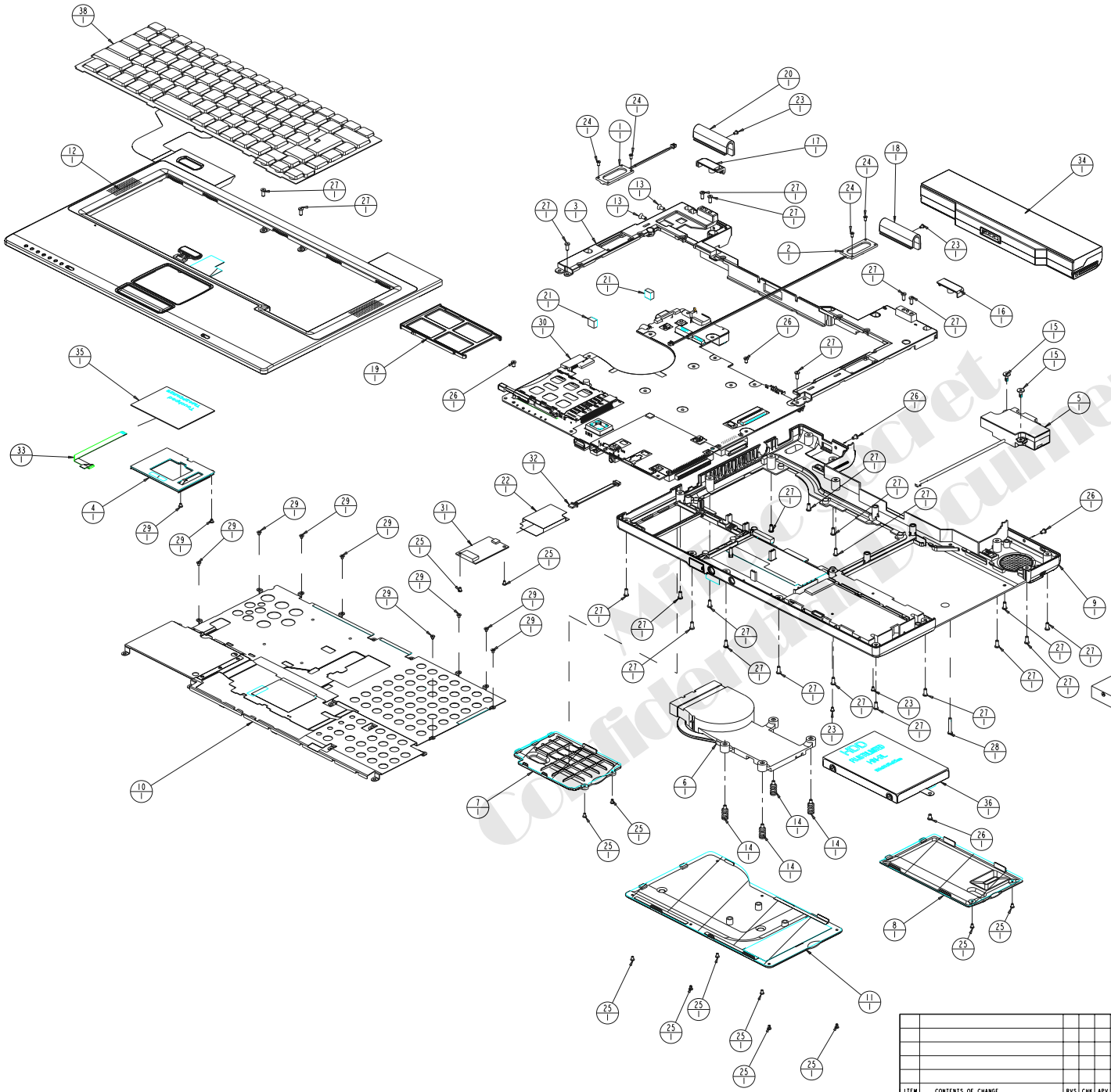
[SHEET NO. 1 of 1]

model name:LCD_ASSY-8350 | file name:LCD_ASSY-8350



ITEM	PART NO	DESCRIPTION	Q'TY	TYPE	REMARK
1	340680900002	SPEAKER ASSY;L,8050	1	ASSEMBLY	
2	340680900003	SPEAKER ASSY;R,8050	1	ASSEMBLY	
3	340680900006	BRACKET ASSY;SYSTEM,8050	1	ASSEMBLY	
4	340680900009	BRACKET ASSY;TP,8050	1	ASSEMBLY	
5	340680900034	SPEAKER ASSY;WOOFER,NEW,8050	1	ASSEMBLY	
6	340687800006	HEATSINK;ASSY,ALRO,RHEA-A	1	ASSEMBLY	
7	340802300001	COVER ASSY;MINIPCI,8350	1	ASSEMBLY	
8	340802300002	COVER ASSY;HDD,8350	1	ASSEMBLY	
9	340802300003	HOUSING ASSY;8350	1	ASSEMBLY	
10	340802300004	SHIELDING ASSY;COVER,8350	1	ASSEMBLY	
11	340802300005	COVER ASSY;CPU,8350	1	ASSEMBLY	
12	340802300006	COVER ASSY;8350	1	ASSEMBLY	
13	341680900001	SPC SCREW;#4-1/4,8050	2	PART	
14	341687800004	SCREW;SPRING,CPU,RHEA-A	4	PART	
15	342686900019	T-SCREW;M26L6.5,8066	2	PART	
16	344680900009	COVER;REAR,R,8050	1	PART	
17	344680900010	COVER;REAR,L,8050	1	PART	
18	344680900011	COVER;HINGE,R,8050	1	PART	
19	344680900048	DUMMY CARD;PCMCIA,8050	1	PART	
20	344680900049	COVER;HINGE,L,8050	1	PART	
21	345684000002	SPONGE;HEATSINK,SIDE,CPU,8050M	2	PART	
22	346670500014	INSULATOR;MDC,TETRA	1	PART	
23	370102010303	SPC-SCREW; M2L3,NIW,K-HD(+),NYLO	4	PART	
24	370102010409	SPC-SCREW;M2L4,K-HD(t0.3),NIB/NL	4	PART	
25	370102030301	SPC-SCREW; M2L3,K-HEAD,1,NIB,NLK	12	PART	
26	370102610401	SPC-SCREW;M2.6L4,K-HD,t0.8,NIB/N	5	PART	
27	370102610603	SPC-SCREW; M2.6L6 K-HEAD,NIB/NLK	25	PART	
28	370102611601	SPC-SCREW; M2.6L16 K-HEAD,NIB	1	PART	
29	371102010252	SCREW;M2L2.5,K-HEAD(+),NIB/NLK	10	PART	
30	411802300004	PWA;PWA-8350,W/O LFB,MOTHER	1	ASSEMBLY	
31	412671800001	PCB ASSY;FAXMODEM,56K,MDC,GP2	1	PART	
32	422684000001	WIRE ASSY;MDC,8050M	1	ASSEMBLY	
33	422802300001	CABLE FFC;TP,8350	1	PART	
34	441681700001	8050/11.1V,4.4AH,LI-ION(SANYO 2	1	ASSEMBLY	
35	442687600001	T/P MODULE;M42PDM1211	1	PART	
36	451687800091	HDD ME KIT;RHEA A	1	ASSEMBLY	
37	523480240003	COMBO MEKIT;KME,UJDA760,8050IL	1	ASSEMBLY	
38	531068780018	KBD;88,US,K011818P1,RHEA-A	1	PART	

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ITEM	CONTENTS OF CHANGE	RVS	CHK	APV	M/D/Y
					/ /
					/ /
					/ /
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					/ /

TOL ± RANGE	Pla	Met	Ins	Per	Cab	Pac	Gas	PCB
0-6	0.1	0.1	0.1	0.2	0.5	1	0.5	0.1
6-30	0.1	0.1	.15	.25	1	1	0.5	0.1
30-80	0.1	.15	0.2	0.3	2	1.5	1	0.1
80-180	.15	.15	.25	0.3	2	2	1	.15
180-315	.15	0.2	0.3	0.4	2.5	2	1	.15
315-800	0.2	0.3	0.4	0.5	3	3	2	.15

DATE	21-Apr-05	MATERIAL	SEE NOTES	TREATMENT		REMARK	
UNIT	MM	SCALE	0.50	DRAWING NAME	HOUSING ME KIT,8350		
DRAWN	DESIGNED	CHECKED	APPROVED	MATERIAL NO.	MF 451 8023 00051 R 00		

MiTAC Technology Corp.

model name:8350-STRU

file name:8350-STRU

Reference Material

❖ AMD Model K8	AMD, INC
❖ ATI RS480M North Bridge	ATI, INC
❖ ULI M1573M South Bridge	ULI, INC
❖ Keyboard controller W83L950D	WIN, INC
❖ 8350 Hardware Engineering Specification	*Technology Corp*/MITAC

SERVICE MANUAL FOR 8350

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