SERVICE MANUAL FOR

8317

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MiTAC

8317 N/B Maintenance

Contents

1. Hardware Engineering Specification 4

1.1 Introduction 4

1.2 System Hardware Part 5

1.3 ULI M1573 GPIO Pin Re-Define 19

1.4 I/O Ports 20

1.5 Super I/O 26

1.6 H8/Keyboard BIOS Controller 27

1.7 Function Key 38

1.8 Power Specification 39

2. System View and Disassembly 47

2.1 System View 47

2.2 Tools Introduction 51

2.3 System Disassembly 52

3. Definition & Location of Connectors / Switches 75

3.1 Mother Board 75

3.2 Audio Jack Board 79

3.3 Modem Board 81

4. Definition & Location of Major Components 82

8317 N/B Maintenance

Contents

4.1 Mother Board 82

5. Pin Description of Major Component 84

5.1 AMD Mobile K8 BGA754_SKT Pin 84

5.2 ATI RS480M North Bridge 86

5.3 ULI M1573 South Bridge 94

6. System Block Diagram 103

7. Maintenance Diagnostics 104

7.1 Introduction 104

7.2 Error Codes 105

7.3 Debug Tool 107

8. Trouble Shooting 108

8.1 No Power 110

8.2 No Display 115

8.3 VGA Controller Test Error LCD No Display 118

8.4 External Monitor No Display 120

8.5 Memory Test Error 122

8.6 Keyboard (K/B)/Touch-Pad(T/P) Test Error 124

8317 N/B Maintenance

Contents

8.7 Hard Disk Drive Test Error 126

8.8 CD-ROM Drive Test Error 128

8.9 USB Port Test Error 130

8.10 Audio Test Error 133

8.11 LAN Test Error 139

8.12 PC Card & Card Reader Socket Test Error 141

8.13 Mini-PCI Socket Test Error 144

9. Spare Parts List 146

10. System Exploded Views 160

11. Reference Material 162

8317 N/B Maintenance

1. Hardware Engineering Specification

1.1 Introduction

This document provides the hardware specification of 8317, 8317 is a high performance notebook based on AMD platform with 17” LCD display. The main system base architecture contains two PCBs, the system Mother Board and the Modem Board.

1.2 System Hardware Part(1)

Item	Description
CPU	- Mobile AMD Athlon 64 62W, “Odessa”, “Newark” - Mobile AMD Sempron 62W, “Dublin”, “Georgetown” - CPU Thermal ceiling: 62W
Core logic	- ATI RS480M + ULi M1573,
L2 Cache	- 256K/512K/1M
System BIOS	- Inside 512KB Flash EPROM - Include System BIOS, VGA BIOS - ACPI2.0; 2.31 compliant - Boot from USB mass storage device
Memory	- 200-pin SO-DIMM DDR Memory Slot x2 - Support DDR333/400 - 0MB Memory onboard; - Expandable to 2.0GB
Video Controller	- Integrate ATI M10c (RS480M) in north bridge - Co-layout local frame buffer 4 chips (64M)
ROM Drive	12.7mm Height - Combo Drive - DVD Dual - DVD Super Multi drive
HDD	One 2.5" 9.5 mm height HDD; - 5400/7200 RPM Serial ATA HDD - 40/60/80 GB Capacity - Support Parallel PATA HDD by option module - Share 8050QD HDD Daughter card without bridge chip - ODD, PATA HDD go individual PATA channel. SATA HDD for SATA channel
Display	17.0”W TFT display; - Resolution WXGA 1440x900 - Resolution WSXGA+ 1680x1050 - Reserve dual channel LVDS display
Keyboard	- Key pitch: 19mm, Key travel: 3.0mm - Windows Logo Key x 2 - W/z Hot Key Functions - Number pad
Touch Pad	- Intelligence Glide pad without scroll button - 2 touch pad buttons
PCMCIA	- Type II x 1 - CardBus Support

1.2 System Hardware Part(2)

Audio System	- High definition audio spec (Azalia), support S/P DIF output - 7.1 channel analog output - 4.1 channel system speaker. Two tweeter speakers (1W Panel), two full range speakers (2W), one subwoofer (3W) - Build in microphone
I/O Port	***I/O:*** USB (support USB 1.1 and USB 2.0) port x 6 RJ-11 port x 1 (4Pin) RJ-45 port x 1 DC input (2.5*5.5*11mm) x 1 IEEE1394 x 1(4 pin) FIR x 1 Type III B MiniPCI x 1 (For wireless LAN) ***Audio (Normal /7.1Analog output):*** Audio-out (SPDIF) x 1 (Front) (Locate at machine front side) Mic-in x 1 (Center, LFB) (Locate at machine front side) Line-in x 1 (Rear) (Locate at machine rear side) Line-out x 1 (Locate at machine rear side) ***Video*** DVI-Digital x 1 TV-Out x 1 (7 Pin S-Video connector NTSC/PAL) VGA monitor port x 1
Communication	- PCI Giga LAN solution - MDC 56K, V.90 Modem - Blue tooth 1.2 module (MDC Combo solution) - 802.11g wireless LAN (MiniPCI optional) with built-in 2 Antenna - Consumer IR for remote controller
AC adapter	- Universal AC adapter 3 Pin 2.5*5.5*11 90W 19V DC output, Input: 100-240V, 50/60Hz AC
Dimensions	- 393mm x 275mm x 38mm(Max)
Power Supply	- 6/9-cell Li-ion (2200mAH/3.7V) Battery pack
Accessories	- AC Adapter, - Power Cord - RJ-11 cable, (Option)
Architecture	- Support PC2001 specifications; - WHQL-certified for Windows XP Professional/Home edition SP2
Weight	- 3.5KG(TBD)
Options	- 128MB/256MB/512MB DDR SDRAM, 6-cell Li-ION Battery Pack, AC Adapter w/o Power Cord,
Certification	EMI: FCC, CE, CB
	Safety: TUV, UL

1.2.1 CPU AMD Athlon 64 Processor

- AMD64 instructions
- MMX™ and 3DNow!™ technology instructions
- SSE, SSE2 and SSE3 instructions
- L1 data cache (L1 D-Cache) contains 64 Kbytes of storage organized as two-way set associative
- L2 cache contains both instruction and data stream information
- The machine check architecture is defined with ECC single-bit detection/correction and double-bit detection
- The processor includes a 16-bit Hyper Transport™ technology interface designed to be capable of operating up to 1600 mega-transfers per second (MT/s) with a resulting bandwidth of up to 6.4 Gbytes/s (3.2 Gbytes/s in each direction)
- The processor's memory controller provides a programmable interface to a variety of standard DDR SDRAM DIMM configurations
- Both lidded and lidless processors provide the following power management features designed to be compliant with the Advanced Configuration and Power Interface (ACPI) Specification and Hyper Transport™ technology
- When the HLT instruction is executed, the processor stops program execution and issues a Halt special cycle

- AMD64 instructions
- When the processor recognizes the STPCLK assertion message, it will enter the Stop Grant state on the next instruction boundary and issue a Stop Grant special cycle
- After RESET_L is deasserted, BIOS must program the appropriate clock divisor in the memory controller configuration registers
- The processor provides an on-die thermal diode with anode and cathode brought out to processor pins
- Both lidded and lidless processors provide a hardware enforced thermal protection mechanism

1.2.2 ATI RS480M

1.2.2.1 CPU Interface

- Supports the mobile and desktop AMD Athlon 64 and Athlon 64 FX processors
- Supports 200,400,800,and 1000MHZ Hyper Transport (HT) interface speeds
- Supports dynamic link width and frequency change
- Supports LDTSTP interface, CPU throttling, and stutter mode

1.2.2.2 Memory Interface

- Optional dedicated frame buffer (side-port) configuration for a 32-bit or 64bit interface and up to 128MB of memory
- Supports for GDDR memories
- Supports for 2M*32(with 64-bit interface only), 4M*32,8M*32,and 16M*16 memory devices
- Asynchronous Hyper Transport and memory controller interface speeds
- Supports GDDR SDRAM self refresh mechanism
- Supports dynamic CKE for power conservation (for GDDR SDRAM only)

1.2.2.3 PCI Express Interface

- Compliant with the PCI Express 1.0a Specifications
- 1*16 graphics interface, which can be divided into two smaller links for use by other devices
- Up to four *1 PCI Express general-purpose links

1.2.2.4 A-Link Express Interface

- 1*2(expandable to *4) A-link Express interface (PCI Express 1.0a compliant) for connection to the ATI IXP

1.2.2.5 2D Acceleration Features

- Highly optimized 128-bit engine, capable of processing multiple pixels per clock
- Hardware acceleration of Bitblt, Line Draw, Polygon/Rectangle Fill, Bit Masking, Monochrome Expansion, Panning/Scolling, Scissoring, and full ROP support(including ROP3)
- Optimized handling of fonts and text using ATI proprietary techniques
- Game acceleration including support for Microsoft's DirectDraw: Double Buffering, Virtual Sprites, Transparent Blit, and Masked Blit
- Supports a maximum resolution of 2048*153632bpp
- Acceleration in 8/15/16/32bpp modes
- Significant increase in the High-End Graphics WinBench score due to capability for C18 color expansion
- Setup of 2D polygons and lines

- Support for new GDI extensions in Windows 2000 and Windows XP: Alpha BLT, Transparent BLT and Gradient Fill
- Hardware cursor (up to 64*64*32bpp), with alpha channel for direct support of Windows 2000 and Windows XP alpha cursor

1.2.2.6 3D Acceleration Features

- Multi-texturing via one texture-blending unit per pixel pipes, allowing up to thirty-two texel reads per pixel in a single pass
- 3D Texture support for bump mapping: emboss, dot product and environment bump maps
- Improved precision in anisotropic filtering and bilinear filtering
- Complete 3D primitive support: points, lines, triangles, lists, strips and quadrilaterals and BLTs with Z compare
- Improve texture composting
- Supports 2536*253632bpp
- Hidden surface removal using 16,24,or 32-bit Z-buffering (maximum Z-buffer depth is 24 bits when stencil buffer enabled) and Early Z hardware

- 8-bit stencil buffer
- Bilinear and trilinear texture lighting
- Dithering support in 16 bpp for near 24-bpp quality in less memory
- Extensive 3D mode support
- Anti-aliasing using multi-sampling algorithm with support for 2,4,and 6 samples
- Optimized for full performance in true color triple buffered 32bpp acceleration modes
- New generation rendering engine provides top 3D performance
- Support for OpenGL format for Indirect Vertices in Vertex Walker
- Full DirectX 9.0 support (Vertex Shader version 2.0 and Pixel shader version 2.0)
- Support for Microsoft's next generation GDI+ user interface

1.2.2.7 Motion Video Acceleration Features

- Video scaling and fully programmable YC

1.2.3 ULI M1573

1.2.3.1 PCI Bridge

- Supports up to 7 external PCI masters
- Parity check on PCI bus AD and CBE# signals
- Fully supports PCI Configuration Space Enable (CSE) protocol
- Fully compliant with PCI Rev. 2.3
- Supports delayed transactions
- Dynamic memory prefetch algorithm and programmable post write flush algorithm
- Supports concurrent PCI bus burst transfers with zero wait-state
- PCI Power Management Interface spec. 1.1 Compliant

1.2.3.2 USB Controller

- Compliant with USB2.0 specification
- Compliant with OHCI 1.0a specification
- Compliant with EHCI 1.0 specification

1.2.3.3 HD Audio Controller

- Azalia spec 0.7 compliant
- 1 SDO sharing by all CODEC
- 3 SDI for 3 CODEC
- 6 output streams
- 5 input streams
- Corb support with sizes of 2, 16 & 256
- RIRB support with sizes of 2, 16 & 256

- Immediate command/response interface
- FIFO sharing technology
- Max output sample rate: 8 channel, 32-bit, 192kHz
- Max input sample rate: 8 channel, 32-bit, 96kHz

1.2.3.4 System Management Bus(SMB)

M1573 internal System Management Bus (SMBus) host controller is designed based on System Management Bus Specifications Rev 2.0. It can communicate with the system clock generator and DRAM SPD via SMBus protocol.

1.2.3.5 Serialized IRQ

M1573 supports Serialized IRQ protocol and thus allows a device using the signal SERIRQ to request for interrupt service. M1573 Serialized IRQ provides 21 frames including IRQ0, IRQ1, SMI#, IRQ3~IRQ15, IOCHCK#, INTA#, INTB#, INTC# and INTD#. Moreover, its operating mode (quiet or continuous) and Start Frame Pulse Width (4/6/8 CICLK periods) are also programmable.

1.2.3.6 Advanced Power Management Controller(M7101)

The Power Management Unit fully supports ACPI specifications and legacy power management functions including: SMM, Stop clock control unit, APM, External SMI-switch control and Programmable counters for time-out event generation.

M1573 can provide G0 (ON, Standby), G1 (S1: Power On Suspend, S3: Suspend To RAM and S4: Suspend To Disk), G2 (Soft-Off) and G3 (Mechanical-Off) global system states to minimize the overall system power consumption. M1573 also provides an extra Standby state for monitoring over 16 peripheral devices' activity.

M1573 supports programmable Stop Clock with Throttle/ Stop Grant/ Stop Clock control for fitting the ACPI C0-C3 clock states. M1573 provides several hot plugging events detection and multiple external wake-up events for satisfying the notebook requirements. M1573 supports the battery, thermal detected logic and system/chip/devices power plane management logic. M1573 provides full support for Advanced Configuration and Power Interface (ACPI), On Now technology and OS Directed Power management (OSPM). M1573 also supports the legacy power management control, such as SMM and SMI features.

1.2.3.7 IDE Controller

- Both two channel support ATA/ATAPI 7
- Both two channel support up to PIO4, MDMA2 and UDMA5/6

- Both two channel support Native and Compatibility Mode
- Can Combine with SATA port0 and port1 in Compatibility Mode
  - SATA port0/1 as channel1, PATA channel 2 as channel2
  - PATA channel1 as channel 1, SATA port0/1 as channel2

1.2.3.8 SATA Controller

- Implement 4 SATA port support SATA Gen 1 1.5G
- Both 4 SATA ports support AHCI 0.98a
- Master Only Emulation to support legacy driver in Native Mode
- Master/Slave Emulation for legacy driver in Combine Mode
- Support SATA II features
- Support Native Command Queue (First party DMA)

1.2.4 Memory

- No onboard memory
- Two 200-pin DDR SDRAM Memory Module
- Support DDR333/400

1.3 ULI M1573 GPIO Pin Re-Define

Pin Num	Name	Type	Power Plane	Current Define	Notice
Y4	RUNGPIO [0]	I/O	MAIN POWER WELL	LCD_ID0	
AF2	RUNGPIO [1]	I/O	MAIN POWER WELL	LCD_ID1	
AB5	RUNGPIO [2]	I/O	MAIN POWER WELL	LCD_ID2	
AB6	RUNGPIO [3]	I/O	MAIN POWER WELL	MUTE#	When MUTE key is pushed, Southbridge will pull low this pin.
E28	RSMGPIO [0]	I/O	MAIN POWER WELL	NA	
E29	RSMGPIO [1]	I/O	MAIN POWER WELL	SW_2.5V/2.6V	Power system auto switch DDR work voltage according to DDR type
C29	RSMGPIO [2]	I/O	MAIN POWER WELL	EXT_SMI#	
D29	RSMGPIO [3]	I/O	MAIN POWER WELL	SCI#	

1.4 I/O Ports

1.4.1 CRT Port

- Standard VGA compatible port

1.4.2 RJ-11

- Connection to Mini-PCI Modem card
- Support 56Kbps / V.92

1.4.3 RJ-45

- The Fast Ethernet LAN Connector features an IEEE802.3 and IEEE802.3x compliant supporting full duplex 10 Base-T, 100 Base-T and 1000 Base-T Ethernet
- LAN PHY: RTL8110SBL

1.4.4 USB2.0 Port

The USB2.0 Host Controller includes one high-speed mode host controller and three USB1.1 host controllers. The high-speed host controller implements an EHCI interface that provides 480Mb/s bandwidth for six USB 2.0 ports. The three USB1.1 host controllers implement an OHCI interface and each USB1.1 host controller provides 12Mb/s bandwidth for two USB 1.1 ports. Each of six USB ports can be automatically routed to support a High-speed USB 2.0 device or Full- or Low-speed USB 1.1 device. Besides, each port can be optionally configured as the wake-up source. Legacy USB devices as well as over current detection are also implemented.

- Two industry standard USB 2.0 Ports (Backward compatible to USB 1.1)
- Support maximum transfer rate up to 480 Mbits /S

1.4.5 LCD Port

- 595 Mbps/channel with 85MHz pixel clock rate
- Integrated dual 24-bit LVDS interface
- Programmable internal spread spectrum controller for the LVDS signals
- Provides fixed resolution displays from scale VGA Low Resolution Mode up for LCD Display to 640 x480 or up to 1600 x1200

- Support DVI, DFP, and VESA P&D digital interface

1.4.6 IEEE 1394

The integrated 1394a host controller complies with 1394 Open Host Controller Interface Specification 1.1, IEEE 1394-1995 and IEEE 1394a-2000. The bus transfer rate of 100, 200, 400 Mbits/s is supported and both Asynchronous and Isochronous data transfers are supported as well. With external 1394 physical layer chip(IC FW802C), it can support up to two 1394 ports to connect with 1394 devices.

1.4.7 CardBus

The Texas Instruments PCI7411 controller is an integrated single-socket UltraMedia PC Card controller, IEEE 1394 open HCI host controller and PHY, and flash media controller. This high-performance integrated solution provides the latest in PC Card, IEEE 1394, SD, MMC, Memory Stick/PRO, SmartMedia and XD technology.

The PCI7411 controller is a four-function PCI controller compliant with *PCI Local Bus Specification*, Revision 2.3. Function 0 provides an independent PC Card socket controller compliant with the *PC Card Standard* (Release 8.1). The PCI7411 controller provides features that make it the best choice for bridging between the PCI bus and PC Cards, and supports Smart Card, Flash Media, 16-bit, CardBus or USB custom card interface PC Cards, powered at 5 V or 3.3 V, as required.

8317 N/B Maintenance

All card signals are internally buffered to allow hot insertion and removal without external buffering. The PCI7411 controller is registering compatible with the Intel 82365SL-DF ExCA controller. The PCI7411 internal data path logic allows the host to access 8-, 16- and 32-bit cards using full 32-bit PCI cycles for maximum performance. Independent buffering and pipeline architecture provide an unsurpassed performance level with sustained bursting. The PCI7411 controller can be programmed to accept posted writes to improve bus utilization.

Function 2 of the PCI7411 controller is compatible with IEEE STD 1394a-2000 and the latest *1394 Open Host Controller Interface Specification*. The chip provides the IEEE1394 link and 2-port PHY function and is compatible with data rates of 100, 200 and 400 Mbits per second. Deep FIFOs are provided to buffer 1394 data and accommodate large host bus latencies. The PCI7411 controller provides physical write posting and a highly tuned physical data path for SBP-2 performance.

Function 3 of the PCI7411 controller is a PCI-based Flash Media controller that supports Memory Stick, Memory Stick-Pro, SmartMedia, XD, SD and MMC cards. This function controls communication with these Flash Media cards through a passive PC Card adapter or through a dedicated Flash Media socket. In addition, this function includes DMA capabilities for improved Flash Media performance.

Function 4 of the PCI7411 controller is a PCI-based SD host controller that supports MMC, SD and SDIO cards. This function controls communication with these Flash Media cards through a passive PC Card adapter or through a dedicated Flash Media socket. In addition, this function is compliant with the *SD Host Controller Standard Specification* and includes both DMA capabilities and support for SD suspend/resume.

1.4.7.1 PCI Bus Power Management

Controller is compliant with the latest PCI Bus Power Management Specification and provides several low-power modes, which enable the host power system to further reduce power consumption.

1.4.7.2 Power Switch Interface

Controller also has a three-pin serial interface compatible with the Texas Instruments TPS2228(Default), TPS2226, TPS2224 and TPS2223A power switches. All four-power switches provide power to the CardBus socket(s) on the PCI7x21/PCI7x11 controller. The power to each dedicated socket is controlled through separate power control pins. Each of these power control pins can be connected to an external 3.3-V power switch.

1.4.8 Audio Port

- Microphone In, Line Out, Line In
- Built in 4 high quality internal speakers (3W), two are on the panel, two are on the top
- SPDIF out

8317 N/B Maintenance

- Support 7.1 channel Azalia
- Microphone shares with central and low frequency channel
- Line Out shares with front right and front left channel
- Line In shares with surround right and left channel
- SPDIF shares with side surround right and left channel
- Built in microphone

1.5 Super I/O

- LPC Bus
- W83L517D Controller
- Infrared (IR) port

The Infrared (IR) function provides a point-to-point (or multi-point to multi-point) wireless communication which can operate under various transmission protocols including IRDA 1.0 SIR, IrDA 1.1 MIR (1.152 Mbps), IrDA 1.1 FIR (4 Mbps), SHARP ASK-IR and remote control (NEC, RC-5, advanced RC-5 and RECS-80 protocol.

1.6 H8/Keyboard BIOS Controller

CPU

- Sixty-five basic instructions
- Sixteen 16-bit general registers also usable as sixteen 8-bit registers or eight 32-bit registers
- Eight addressing modes
- 16-Mbyte address space
- High-speed operation
- Two CPU operating modes
- Power-down state

MCU Operating Modes

- MCU Operating Mode Selection
- SYSCR selects a system pin function, monitors a reset source, selects the interrupt control mode and the detection edge for NMI, pin location selection, enables or disables register access to the on-chip peripheral modules and enables or disables on-chip RAM address space
- STCR enables or disables register access

8317 N/B Maintenance

Exception Handling

- Exception handling may be caused by a reset, interrupt, direct transition, or trap instruction
- A reset has the highest exception priority
- The interrupt controller controls interrupts
- Trap instruction exception handling starts when a TRAPA instruction is executed

Interrupt Controller

- Two interrupt control modes
- Priorities settable with ICR
- Independent vector addresses
- Thirty-one external interrupts
- DTC control

Bus Controller(BSC)

- Basic bus interface
- Burst ROM interface

8317 N/B Maintenance

- Idle cycle insertion
- Bus arbitration function

Data Transfer Controller(DTC)

- Transfer is possible over any number of channels
- Three transfer modes
- One activation source can trigger a number of data transfers (chain transfer)
- Direct specification of 16-Mbyte address space is possible
- Activation by software is possible
- Transfer can be set in byte or word units
- A CPU interrupt can be requested for the interrupt that activated the DTC
- Module stop mode can be set

I/O Ports

- This LSI has ten I/O ports (ports 1 to 6, 8, 9, A, and B), and one input-only port (port 7)

8317 N/B Maintenance

8-Bit PWM Timer(PWM)

- Operable at a maximum carrier frequency of 625 kHz using pulse division (at 10 MHz operation)
- Duty cycles from 0 to 100% with 1/256 resolution (100% duty realized by port output)
- Direct or inverted PWM output, and PWM output enable/disable control

14-Bit PWM Timer(PWMX)

- Division of pulse into multiple base cycles to reduce ripple
- Two resolution settings
- Two base cycle settings
- Four operating speeds
- Four operation clocks (by combination of two resolution settings and two base cycle settings)

16-Bit Free-Running Timer(FRT)

- Selection of four clock sources
- Two independent comparators
- Four independent input capture channels

8317 N/B Maintenance

- Counter clearing
- Seven independent interrupts
- Special functions provided by automatic addition function

8-Bit Timer (TMR)

- Selection of clock sources
- Selection of three ways to clear the counters
- Timer output controlled by two compare-match signals
- Cascading of TMR_0 and TMR_1
- Multiple interrupt sources for each channel

Timer Connection

- Five input pins and four output pins, all of which can be designated for phase inversion. Positive logic is assumed for all signals used within the timer connection facility
- An edge-detection circuit is connected to the input pins, simplifying signal input detection
- TMR_X can be used for PWM input signal decoding
- TMR_X can be used for clamp waveform generation

8317 N/B Maintenance

- An external clock signal divided by TMR_1 can be used as the FRT capture input signal
- An internal synchronization signal can be generated using the FRT and TMR_Y
- A signal generated/modified using an input signal and timer connection can be selected and output

Watchdog Timer (WDT)

- Selectable from eight (WDT_0) or 16 (WDT_1) counter input clocks
- Switchable between watchdog timer mode and interval timer mode
- Watchdog Timer Mode
- Internal Timer Mode

Serial Communication Interface (SCI and IRDA)

- Choice of asynchronous or clocked synchronous serial communication mode
- Full-duplex communication capability
- The on-chip baud rate generator allows any bit rate to be selected
- Choice of LSB-first or MSB-first transfer (except in the case of asynchronous mode 7-bit data)
- Four interrupt sources

8317 N/B Maintenance

I^2C Bus Interface (IIC) (Optional)

- Selection of addressing format or non-addressing format
- Conforms to Philips I2C bus interface (I2C bus format)
- Two ways of setting slave address (I2C bus format)
- Start and stop conditions generated automatically in master mode (I2C bus format)
- Selection of the acknowledge output level in reception (I^2C bus format)
- Automatic loading of an acknowledge bit in transmission (I2C bus format)
- Wait function in master mode (I2C bus format)
- Wait function (I^2C bus format)
- Interrupt sources
- Selection of 16 internal clocks (in master mode)
- Direct bus drive (SCL/SDA pin)
- Automatic switching from formatless mode to I2C bus format (IIC_0 only)

8317 N/B Maintenance

Keyboard Buffer Controller

- Conforms to PS/2 interface specifications
- Direct bus drive (via the KCLK and KD pins)
- Interrupt sources: on completion of data reception and on detection of clock edge
- Error detection: parity error and stop bit monitoring

Host Interface X-Bus Interface (XBS)

- Control of the fast GATE A20 function
- Shutdown of the XBS module by the HIFSD pin
- Five host interrupt requests

Host Interface LPC Interface (LPC)

- Supports LPC interface I/O read cycles and I/O write cycles
- Has three register sets comprising data and status registers
- Supports SERIRQ
- Eleven interrupt sources

8317 N/B Maintenance

D/A Converter

- 8-bit resolution
- Two output channels
- Conversion time: Max. 10 µs (when load capacitance is 20 pF)
- Output voltage: 0 V to Avref
- D/A output retaining function in software standby mode

A/D Converter

- 10-bit resolution
- Input channels: eight analog input channels and 16 digital input channels
- Analog conversion voltage range can be specified using the reference power supply voltage pin (AVref) as an analog reference voltage
- Conversion time: 13.4 µs per channel (at 10-MHz operation)
- Two kinds of operating modes
- Four data registers
- Sample and hold function

8317 N/B Maintenance

- Three kinds of conversion start
- Interrupt request

Power-Down Modes

- Medium-speed mode
- Subactive mode
- Sleep mode
- Subsleep mode
- Watch mode
- Software standby mode
- Hardware standby mode

1.6.1 H8S/2140B GPIO Pins Re-Defined from HOOK

Hitachi H8S/2140B to ULI M1573 pin function definitions for Inside code.

Index	Pin Num	Hook Definition	8317 Re-definition	Notice
1	81	AMP_PROT	CAP_LOCK	Use this pin to driver LED when CPA key in keyboard is pushed.
2	57	NA	NUM_LOCK	Use this pin to driver LED when NUM key in keyboard is pushed.
3	50	H8_TV_DECT#	PLAY	When Instant Play is pushed, this pin will be pulled low to indicate that H8 would execute some code to play the CD.
4	54	TP726	VGA_THERMAL	When this pin is pulled high H8 would know that VGA working temperature is higher than 60 degree.
5	58	RESERVE_LED2#	LOCK#	When this Pin is pulled low, H8 would know that locks instant play function.

1.7 Function Key

1.7.1 Switch

Mute: When this switch is pushed, H8 will send message to Southbridge and make it send signal through GPIO to do Mute function

Backward: For Instant play function, when this switch is pushed, H8 would execute scanning code to do backward function

Forward: For Instant play function, when this switch is pushed, H8 would execute scanning code to do forward function

Stop: For Instant play function, when this switch is pushed, H8 would execute scanning code to do stop function

These four switches is scanned by H8

Play: When this switch is pushed, it will send signal to H8 and make it execute scanning code to do play function

WLAN On_Off: When this switch is pushed, it will send signal to mini-PCI and make it do on/off action

Bluetooth On_Off: Disable Bluetooth functions

Lock SW: When this switch is pushed, it will send signal to H8 and make it to lock all instant play functions

1.8 Power Specification

- +1.2VLDTA: Main Power Source that turns off in S3
- +NB_CORE: Main Power Source that turn off in S3
- +3V: Main Power Source that exist only the system is power on
- +3VS: Main Power Source that turns off in S3
- +5V: Main Power Source that exist only the system is power on
- +5VS: Main Power Source that turns off in S3
- VDD3: Auxiliary power that exist regardless the system is power down or power up
- VDD5: Auxiliary power that exist regardless the system is power down or power up
- +1.8VS: Main Power Source that turn off in S3
- +2.5V: Main Power Source that provides 1.25V for the termination of the signal of DDR
- +1.25V: Main Power Source that provides 1.25V for the termination of the signal of DDR
- +1.25VS: Main Power Source that turns off in S3
- +VCC_CORE: Main Power Source it can match AMD MOBILE K8

- D/VMAIN: Power supply from AC adapter or battery for main power

1.8.1 Battery Management Definitions

1.8.1.1 Li-ION Battery Packs 1

- Battery Type: Li-ION
- Battery Cells: 9 Cells
- Battery Specs: 11.1V/6000mAh with 3.7V/2000mAh / Cell
- Battery Output Power - Total: 66.6 watts
- Smart Battery
- Battery Protections: Over Charge Protects, Over Discharge Protects, Over Temperature Protects and Over Current Protects

1.8.1.2 Battery Gauge

- Gas Gauge IC packed into Battery Packages
- Supports SM Bus V.1.0 Specs
- Supports SM Bus Master Mode for Battery Low Broadcast

1.8.2 Battery Warning

1.8.2.1 Low Battery Warning

When the Current Capacity of the Battery Pack is Less Than or Equal to 10% Capacity, the indicator will turn to flashing in blue.

1.8.2.2 Smart Battery Charger

A Normal Battery Charger IC is used to Charges the Battery. The Embedded Controller H8 controls charge IC. The H8 will Emulate Smart Battery Interface needed to Talking with Smart Battery Packs.

1.8.2.3 Battery Gas Gauge Views Utilities

Windows98 SE, Windows ME, Windows 2000, Windows XP and Power.exe in DOS. Battery Gas Gauge can be quick Pop-Up on Screen in any time.

1.8.3 Power Supplies

1.8.3.1 General Description

- The DC/DC (on board) can support:
  - +VCC_CORE, +NB_CORE,+1.25V, +1.2VLDTA
  - +2.5V, +5V, +3V, +5VS, +3VS, +1.8VS for the M/B.

1.8.4 Electronically Specifications

DC OUTPUT					
Voltage	Tolerance	Ripple & noise	Line / load regulation	Transient response	A. Max current (Total)
+5V	±5 %	250mVp-p	±2.5 %	500mVp-p	5A
+3V	±5 %	165mVp-p	±2.5 %	330mVp-p	4A
+2.5V	±5 %	125mVp-p	--- / ±2.5 %	250mVp-p	4.5A
+1.25V	±5 %	62.5mVp-p	--- / ±2.5 %	125mVp-p	3A
+NB_CORE	±5 %	60mVp-p	--- / ±2.5 %	120mVp-p	5A
+1.2VLDTA	±5 %	60mVp-p	--- / ±2.5 %	120mVp-p	4A
+1.4V@1.8G (+VCC_CORE)	When frequency of cup is 1.8GHZ,Vo=1.4V,Imax=42.7A. When system enter into S3, Frequency of cpu is 800MHZ,Vo=0.95v, Imax=11.4a				

Note: The following output ripple/noise requirements shall be meet throughout the load range and under input voltage from 8Vdc to 21Vdc. Measurements shall be made with an oscilloscope with 20MHZ bandwidth output shall be bypassed at connector with a 0.1uF ceramic capacitor and a 10 uF electrolytic capacitor to simulate loading.

1.8.4.1 Input

Input voltage range: 8V~12.8Vdc (Battery) or 18.6V~21.4Vdc (Adaptor)

Adapter: 19V @ 5A, 90W constant voltage mode

Battery: Li-Ion Battery Pack 9 Cells (3S3P) DC 11.1V

1.8.4.2 Inrush Current

Condition	All operation condition turn on/off 1 second at all of input power source. 40 degree C air ambient.
Limit	No damage shall occur or components over stress, input fuse shall not blow.

1.8.4.3 Efficiency

A. +5V&3.3V: (1) 88% min (@+5V/5A,+3.3V/4A & Vin : 19V-from adaptor)

(2) 90% min (@+5V/5A,+3.3V/4A & Vin : 8V-from battery)

B. +2.5V: 88% min (@+2.5V/4.5A & Vin = DNMAIN)

C. +1.05V: 88% min (@+1.2V/5A & Vin = DNMAIN)

D. VCORE (+1.4V typ.): 76% min (@+1.4V/42.7A & Vin : DVMAIN)

1.8.4.4 Protection Requirements

A-1. Over voltage protection activated when (VCORE) output voltage over 7.5% (max) of normal value

A-2. Over voltage protection activated when (+2.5V_DDR_P,) output voltage over 1.0V (max) of normal value

B-1. Vcore: 60A

B-2. +5V: 8~12A

B-3. +3.3V: 8~12A

C. Short Protection activated when +VCC_CORE, +3.3V_P,+5V_P,+2.5V _P,+1.25V_P, +1.2V_P output short circuit the dc/dc converter output voltage shutdown or holding

Note: The OVP&OCP&SCP protection shall cause the system no fire or no smoke**.**

1.8.4.5 Transient Response

The transient response is measured by switching the output load from 0 to 50 and 50 to 100 percent of its full value at a frequency of 100Hz and 50% duty cycle, step load change is 1.0A/μsec. The recovery time is less than 1ms and the regulation shall be less than the unit of output spec**.**

1.8.4.6 Power Up Overshoot and Undershoot

Power up overshoot and undershoot must be within tolerance of each output voltage spec.

1.8.4.7 System Overall Leakage Current

When system only connects DC-battery , it's leakage current though from battery 12.6V under 1mA at system power off .

1.8.4.8 Environment

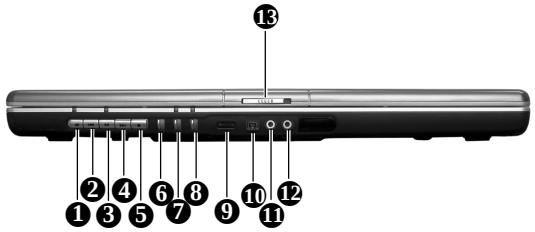
ITEM	CONDITION	LIMITS	
TEMPERATURE	OPERATION	0℃	40℃
	STORAGE	-20℃	70℃
HUMIDITY	OPERATION	20%	80%
	STORAGE	10%	90%

2. System View and Disassembly

2.1 System View

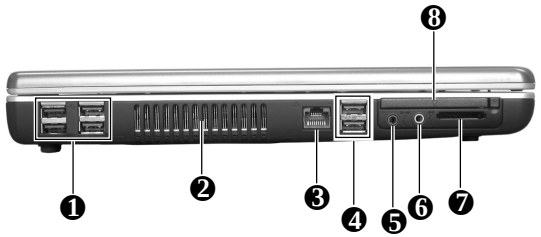
2.1.1 Front View

❶ Mute Button
❷ Forward Button
❸ Play Button
❹ Backward Button
❺ Stop Button
❻ Holder On/Off
❼ WLAN On/Off
❽ Blue Tooth On/Off
❾ Volume Control
❿ IEEE1394 Port
⓫ Line Out Connector
⓬ Line In Connector
⓭ Top Cover Latch



2.1.2 Left-side View

❶ USB Ports *4
❷ Ventilation Openings
❸ RJ-45 Connector
❹ USB Ports *2
❺ SPDIF Out Connector
❻ Line In Connector
❼ SD/MMC/MS Carder Socket
❽ PCMCIA Card Socket



2.1.3 Right-side View

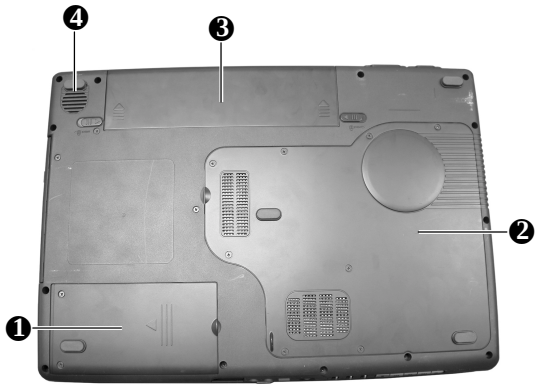
❶ RJ-11 Connector
❷ CD/DVD-ROM Drive

2.1.4 Rear View

❶ Lock
❷ AC Power Connector
❸ DVI Port
❹ VGA Port
❺ S-Video

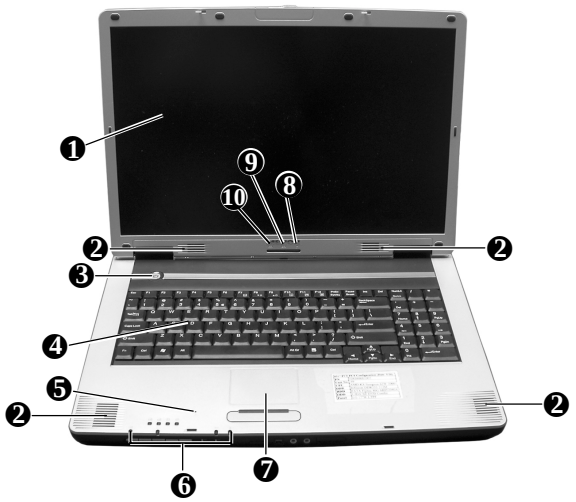
2.1.5 Bottom View

❶ Hard Disk Drive
❷ CPU
❸ Battery Pack
❹ Stereo Speaker Set



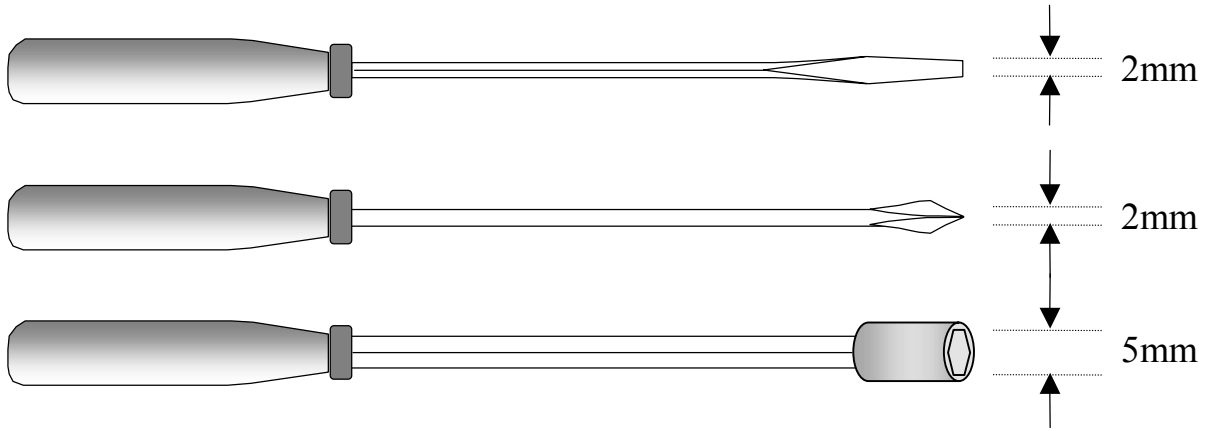
2.1.6 Top-open View

❶ LCD Screen
❷ Stereo Speaker Set
❸ Power Button
❹ Keyboard
❺ Internal MIC In
❻ Device LED Indicators
❼ Touch Pad
❽ AC Power Indicator
❾ Battery Charge Indicator
❿ Battery Power Indicator

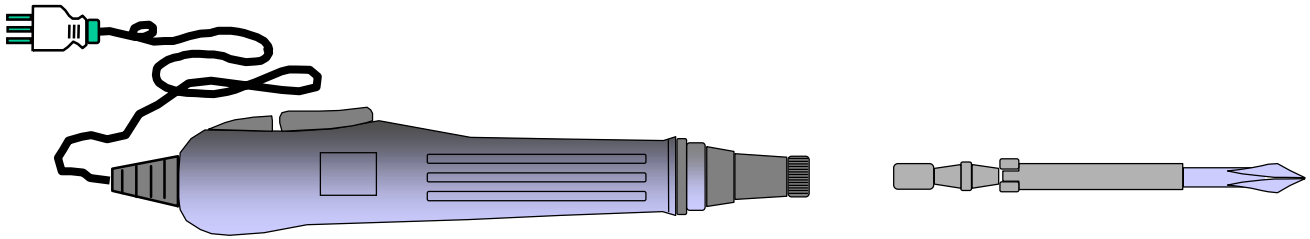


2.2 Tools Introduction

1. Minus screw driver with bit size 2mm for notebook assembly & disassembly.



2. Auto screw driver for notebook assembly & disassembly.



Bit Size

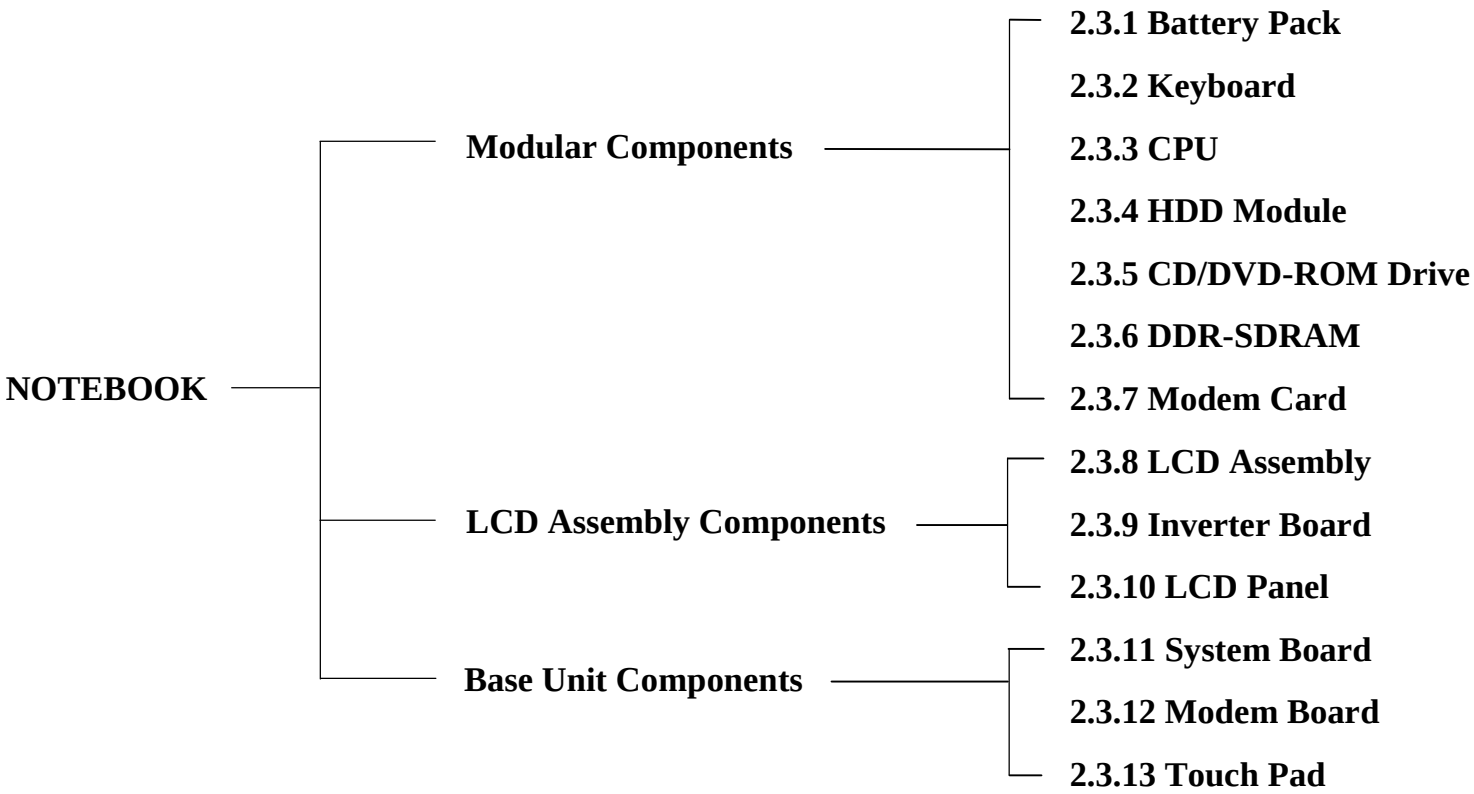
#0

Screw Size	Tooling	Tor.	Bit Size
1. M2.0	Auto-Screw driver	2.0-2.5 kg/cm2	#0

2.3 System Disassembly

The section discusses at length each major component for disassembly/reassembly and show corresponding illustrations.Use the chart below to determine the disassembly sequence for removing components from the notebook.

NOTE: *Before you start to install/replace these modules, disconnect all peripheral devices and make sure the notebook is not turned on or connected to AC power.*



2.3.1 Battery Pack

Disassembly

1. Carefully put the notebook upside down.
2. Slide the two release levers outwards to the "unlock" position (❶), while take the battery pack out of the compartment (❷). (Figure 2-1)

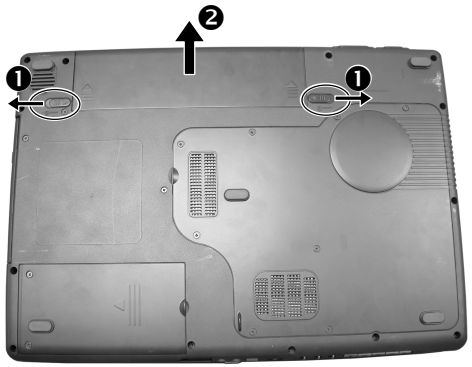


Figure 2-1 Remove the battery pack

Reassembly

1. Replace the battery pack into the compartment. The battery pack should be correctly connected when you hear a clicking sound.
2. Slide the release lever to the "lock" (🔒) position.

2.3.2 Keyboard

Disassembly

1. Remove the battery pack. (Refer to section 2.3.1 Disassembly)
2. Open the top cover.
3. Loosen the four latches locking the keyboard. (Figure 2-2)

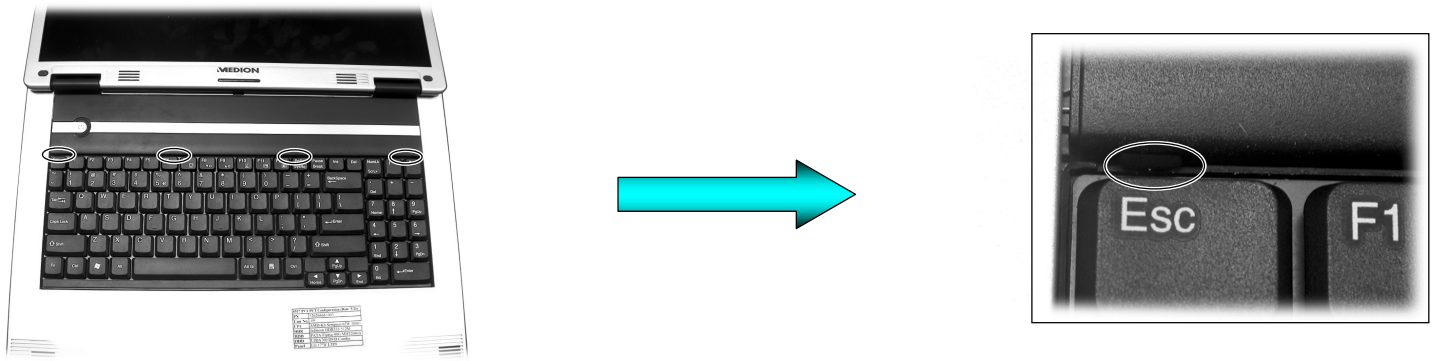


Figure 2-2 Loose the four latches

4. Slightly put the keyboard upside down and disconnect the cable from the system board, then separate the keyboard. (Figure 2-3)

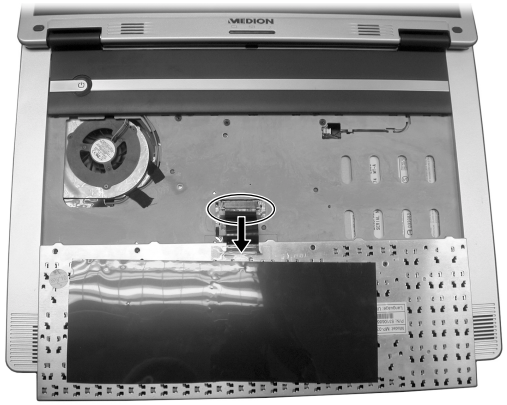


Figure 2-3 Free the keyboard

Reassembly

1. Reconnect the keyboard cable and fit the keyboard back into place.
2. Replace the keyboard fasten the four latches.
3. Replace the battery pack. (Refer to section 2.3.1 Reassembly)

2.3.3 CPU

Disassembly

1. Remove the battery pack. (Refer to section 2.3.1 Disassembly)
2. Remove the eight screws fastening the CPU cover. (Figure 2-4)
3. Remove the four spring screws that secure the heatsink upon the CPU and disconnect the fan's power cord from the system board. (Figure 2-5)

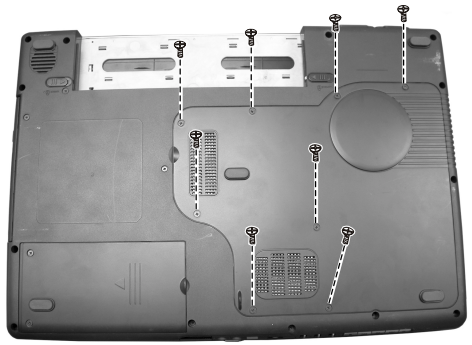


Figure 2-4 Remove the eight screws

Figure 2-5 Free the heatsink

4. To remove the existing CPU, lift the socket arm up to the vertical position. (Figure 2-6)

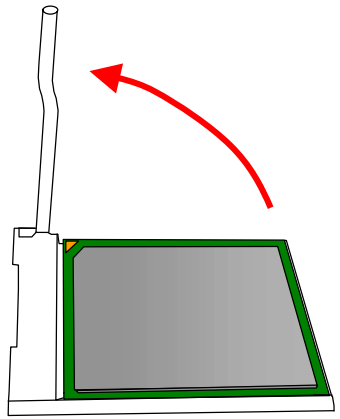


Figure 2-6 Free the CPU

Reassembly

1. Carefully, align the arrowhead corner of the CPU with the beveled corner of the socket, then insert CPU pins into the holes. Place the lever back to the horizontal position and push the lever to the left.
2. Reconnect the fan's power cord to the system board, fit the heatsink onto the top of the CPU and secure with four screws.
3. Replace the CPU cover and secure with eight screws.
4. Replace the battery pack. (See section 2.3.1 reassembly)

2.3.4 HDD Module

Disassembly

1. Carefully put the notebook upside down. Remove the battery pack. (Refer to section 2.3.1 Disassembly)
2. Remove the two screws fastening the HDD compartment cover. (Figure 2-7)
3. Remove the one screw and slide the HDD module out of the compartment. (Figure 2-8)

Figure 2-7 Remove the HDD compartment cover

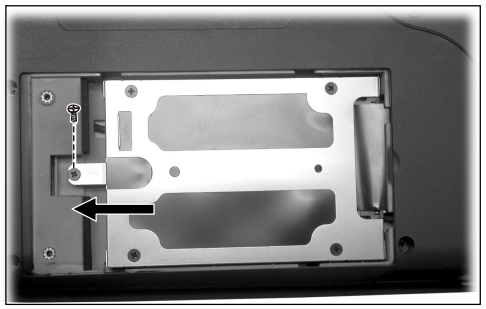


Figure 2-8 Remove HDD module

4. Remove the six screws to separate the hard disk drive from the bracket, remove the hard disk drive. (Figure 2-9)

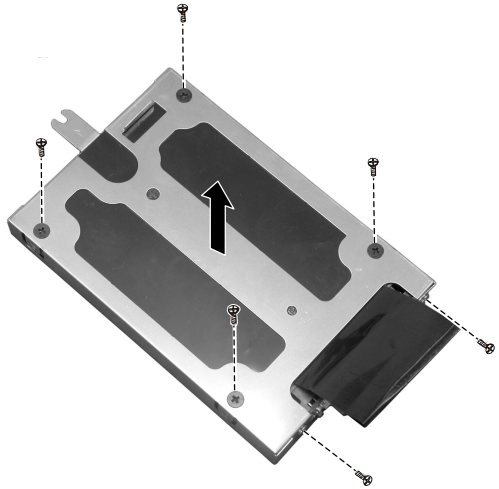


Figure 2-9 Remove hard disk drive

Reassembly

1. Attach the bracket to hard disk drive and secure with six screws.
2. Slide the HDD module into the compartment and secure with one screw.
3. Place the HDD compartment cover and secure with two screws.
4. Replace the battery pack. (Refer to section 2.3.1 Reassembly)

2.3.5 CD/DVD-ROM Drive

Disassembly

1. Carefully put the notebook upside down. Remove the battery pack. (See section 2.3.1 Disassembly)
2. Remove the two screws fastening the CD/DVD-ROM drive. (Figure 2-10)
3. Insert a small rod, such as a straightened paper clip, into CD/DVD-ROM drive's manual eject hole (❶) and push firmly to release the tray. Then gently pull out the CD/DVD-ROM drive by holding the tray that pops out (❷).

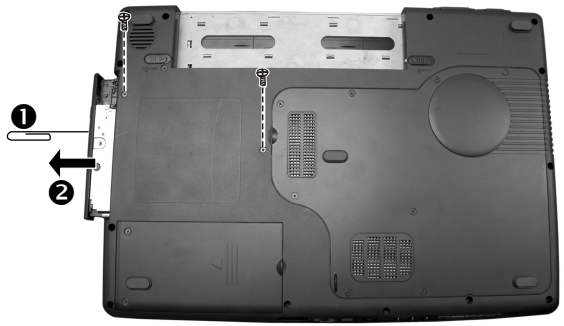


Figure 2-10 Remove the CD/DVD-ROM drive

Reassembly

1. Push the CD/DVD-ROM drive into the compartment and secure with two screws.
2. Replace the battery pack. (See section 2.3.1 Reassembly)

2.3.6 DDR-SDRAM

Disassembly

1. Carefully put the notebook upside down. Remove the battery pack. (See section 2.3.1 Disassembly)
2. Remove the eight screws fastening the CPU cover. (Refer to the step 2 of section 2.3.3 Disassembly)

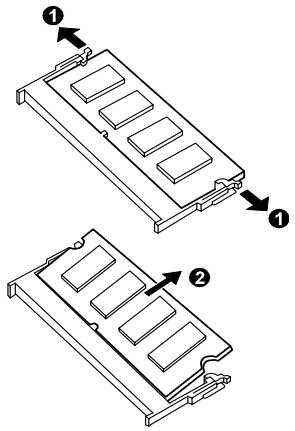


Figure 2-11 Remove the SO-DIMM

3. Pull the retaining clips outwards (❶) and remove the SO-DIMM (❷). (Figure 2-11)

Reassembly

1. To install the DDR, match the DDR's notched part with the socket's projected part and firmly insert the SO-DIMM into the socket at 20-degree angle. Then push down until the retaining clips lock the DDR into position.
2. Replace the CPU cover and secure with eight screws. (Refer to the step 3 of section 2.3.3 Reassembly)
3. Replace the battery pack. (See section 2.3.1 Reassembly)

2.3.7 Modem Card

Disassembly

1. Carefully put the notebook upside down. Remove the battery pack. (Refer to section 2.3.1 Disassembly)
2. Remove eight screws fastening CPU cover. (Refer to step 2 of section 2.3.3 Disassembly)
3. Remove two screws fastening the modem card. (Figure 2-12)
4. Lift up the modem card and disconnect the cord. (Figure 2-13)

Figure 2-12 Remove two screws

Figure 2-13 Disconnect the cord

Reassembly

1. Reconnect the cord and fit the modem card.
2. Fasten the modem card by two screws.
3. Replace the CPU cover by eight screws. (Refer to step 3 of section 2.3.3 Reassembly).
4. Replace the battery pack. (Refer to section 2.3.1 Reassembly)

2.3.8 LCD ASSY

Disassembly

1. Remove the battery pack and keyboard. (See sections 2.3.1 and 2.3.2 Disassembly)
2. Remove the CPU cover. (Refer to the step 2 of section 2.3.3 Disassembly)
3. Separate the antennae from the system board. (Figure 2-14)
4. Remove the KB cover from the top cover. And separate the antennae from the case kit. (Figure 2-15)

Figure 2-14 Separate the antennae

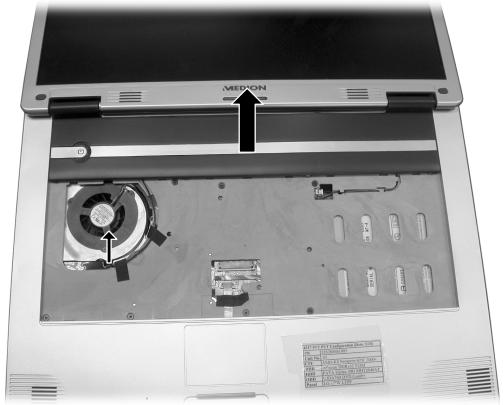


Figure 2-15 Remove the KB cover

5. Disconnect the three cables from the system board and separate the antennae. (Figure 2-16)
6. Remove the four screws and free the LCD assembly. (Figure 2-17)

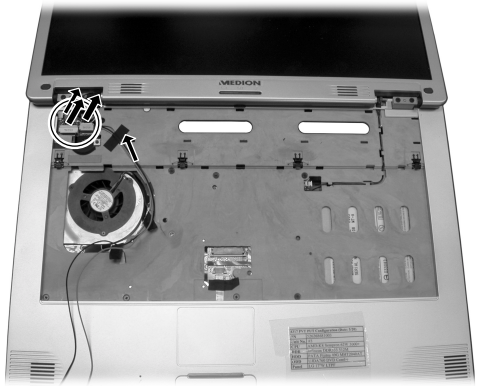


Figure 2-16 Disconnect the three cables and separate the antennae

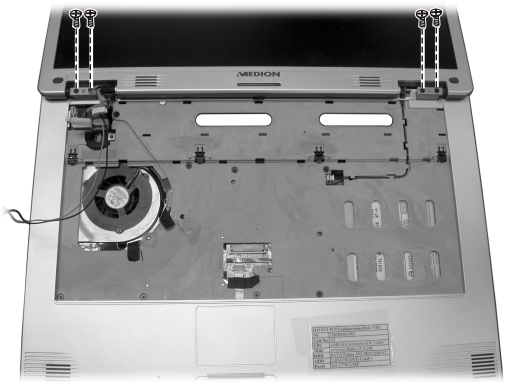


Figure 2-17 Free the LCD assembly

Reassembly

1. Attach the LCD assembly to the base unit and secure with four screws.
2. Replace the antennae back into Mini PCI compartment.
3. Reconnect the three cables to the system board.
4. Replace the KB cover.
5. Replace the CPU cover. (Refer to the step 3 of section 2.3.3 Reassembly)
6. Replace the keyboard and battery pack. (Refer to section 2.3.2 and 2.3.1 Reassembly)

2.3.9 Inverter Board

Disassembly

1. Remove the battery, keyboard and LCD assembly. (Refer to section 2.3.1, 2.3.2 and 2.3.8 Disassembly)
2. Remove the six rubber pads and six screws on the corners of the panel. (Figure 2-18)
3. Insert a flat screwdriver to the lower part of the LCD cover and gently pry the frame out. Repeat the process until the cover is completely separated from the housing.
4. Remove the two screws and disconnect the cable. (Figure 2-19)

Figure 2-18 Remove LCD cover

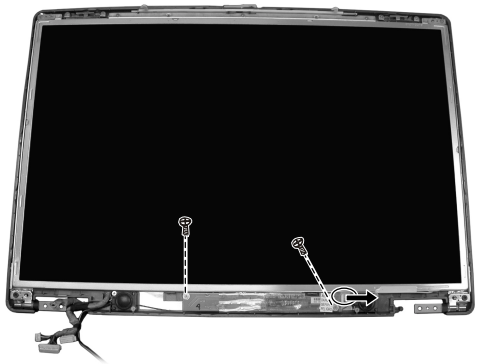


Figure 2-19 Remove the two screws and disconnect the cable

5. Disconnect the cable from the inverter board and free the inverter board. (Figure 2-20)

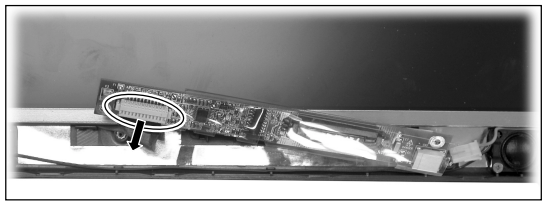


Figure 2-20 Free the inverter board

Reassembly

1. Reconnect the cable into the inverter board, then replace the inverter board into the LCD housing and secure with two screws.
2. Reconnect the cable into the inverter board.
3. Replace the LCD cover and secure with six screws and six rubber pads.
4. Replace the LCD assembly, keyboard and battery pack. (Refer to section 2.3.8, 2.3.2, 2.3.1 Reassembly)

2.3.10 LCD Panel

Disassembly

1. Remove the battery, keyboard, LCD assembly and inverter board. (Refer to section 2.3.1, 2.3.2, 2.3.8 and 2.3.9 Disassembly)
2. Remove the four screws. (Figure 2-21)
3. Remove the four screws that secure the LCD brackets. (Figure 2-22)

Figure 2-21 Remove the four screws

Figure 2-22 Remove the four screws

4. Disconnect the cable to free the LCD panel. (Figure 2-23)

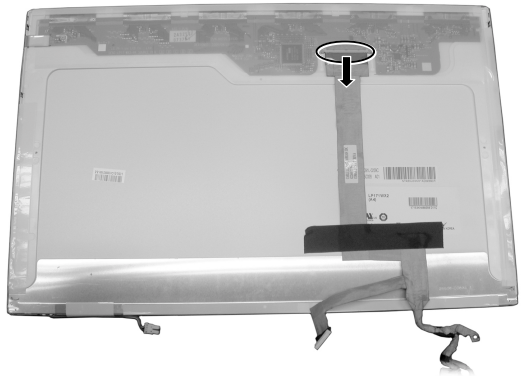


Figure 2-23 Free the LCD panel

Reassembly

1. Replace the cable to the LCD panel.
2. Attach the LCD panel's brackets back to LCD panel and secure with four screws.
3. Replace the LCD panel into LCD housing and secure with four screws.
4. Replace the inverter board, LCD assembly, keyboard and battery pack. (Refer to section 2.3.9, 2.3.8, 2.3.2 and 2.3.1 Reassembly)

2.3.11 System Board

Disassembly

1. Remove the battery, keyboard, CPU, hard disk drive, CD/DVD-ROM drive, DDR, modem card and LCD assembly. (Refer to sections 2.3.1, 2.3.2, 2.3.3, 2.3.4, 2.3.5, 2.3.6, 2.3.7 and 2.3.8 Disassembly)
2. Disconnect the touch pad's cable and the cover switch's cable from the system board, then remove the eight screws fastening the top cover. (Figure 2-24)
3. Disconnect the woofer speaker's cable from the system board, then remove the sixteen screws fastening the housing and free the housing. (Figure 2-25)

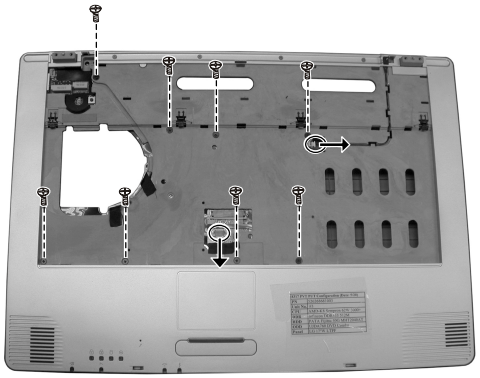


Figure 2-24 Disconnect the two cables and remove the eight screws

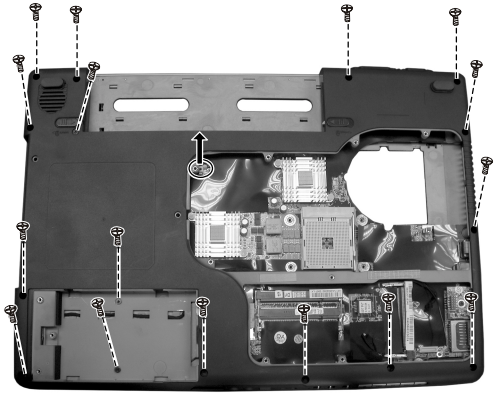


Figure 2-25 Free the housing

4. Disconnect the two speakers' cables from the system board. (Figure 2-26)
5. Remove the two screws and four hex nuts, then lift the system board from the top cover and free the system board. (Figure 2-27)

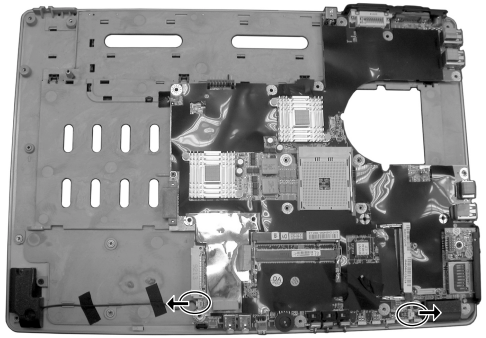


Figure 2-26 Disconnect the cables

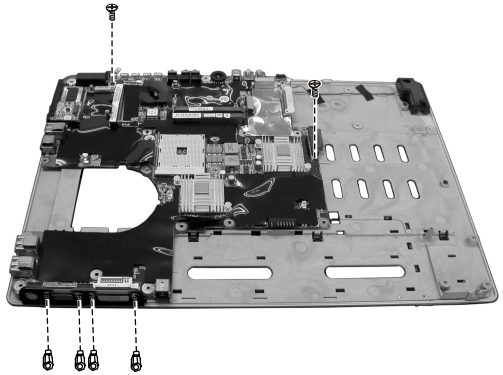


Figure 2-27 Free the system board

Reassembly

1. Fit the system board into the top cover and secure with two screws and four hex nuts.
2. Reconnect the two speakers' cables into the system board.
3. Replace the housing into the top cover and secure with sixteen screws, then reconnect the woofer speaker's cable.
4. Reconnect the touch pad's cable and the cover switch's cable, then secure with eight screws.
5. Replace the LCD assembly, modem card, DDR, CD/DVD-ROM drive, hard disk drive, CPU, keyboard and battery pack. (Refer to the section 2.3.8, 2.3.7, 2.3.6, 2.3.5, 2.3.4, 2.3.3, 2.3.2 and 2.3.1 Reassembly)

2.3.12 Modem Board

Disassembly

1. Remove the battery pack, keyboard, CPU, hard disk drive, CD/DVD-ROM drive, DDR, modem card and LCD assembly. (See sections 2.3.1, 2.3.2, 2.3.3, 2.3.4, 2.3.5, 2.3.6, 2.3.7 and 2.3.8 Disassembly)
2. Remove the housing. (Refer to the steps 1-3 of section 2.3.11 Disassembly)
3. Remove the one screw and lift the modem board, then free it. (Figure 2-28)

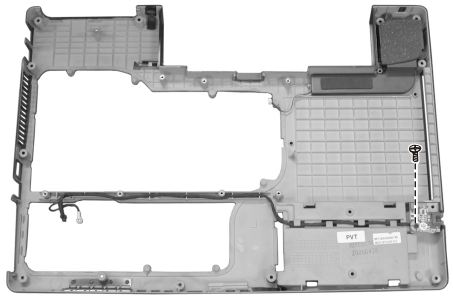


Figure 2-28 Free the modem board

Reassembly

1. Replace the modem board into the housing and secure with one screw.
2. Replace the housing. (Refer to the step 3-4 of section 2.3.11 Disassembly)
3. Replace the LCD assembly, modem card, DDR, CD/DVD-ROM drive, hard disk drive, CPU, keyboard and battery pack. (See sections 2.3.8, 2.3.7, 2.3.6, 2.3.5, 2.3.4, 2.3.3, 2.3.2 and 2.3.1 Reassembly)

2.3.13 Touch Pad

Disassembly

1. Remove the battery pack, keyboard, CPU, hard disk drive, CD/DVD-ROM drive, DDR, modem card, LCD assembly and system board. (See sections 2.3.1, 2.3.2, 2.3.3, 2.3.4, 2.3.5, 2.3.6, 2.3.7, 2.3.8 and 2.3.11 Disassembly)
2. Remove the four screws from the top cover. (Figure 2-29)
3. Disconnect the cable from the touch pad, then remove the two screws and free the shielding. (Figure 2-30)
4. Touch pad can't be taken apart from the top cover. It is necessary to replace the top cover, if defect.

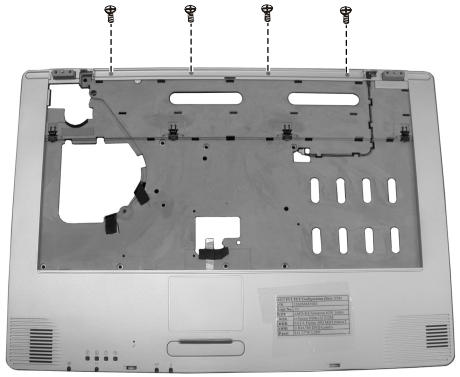


Figure 2-29 Remove four screws

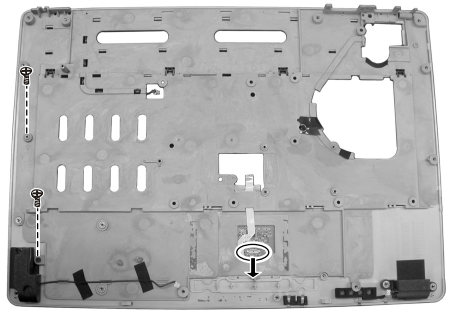


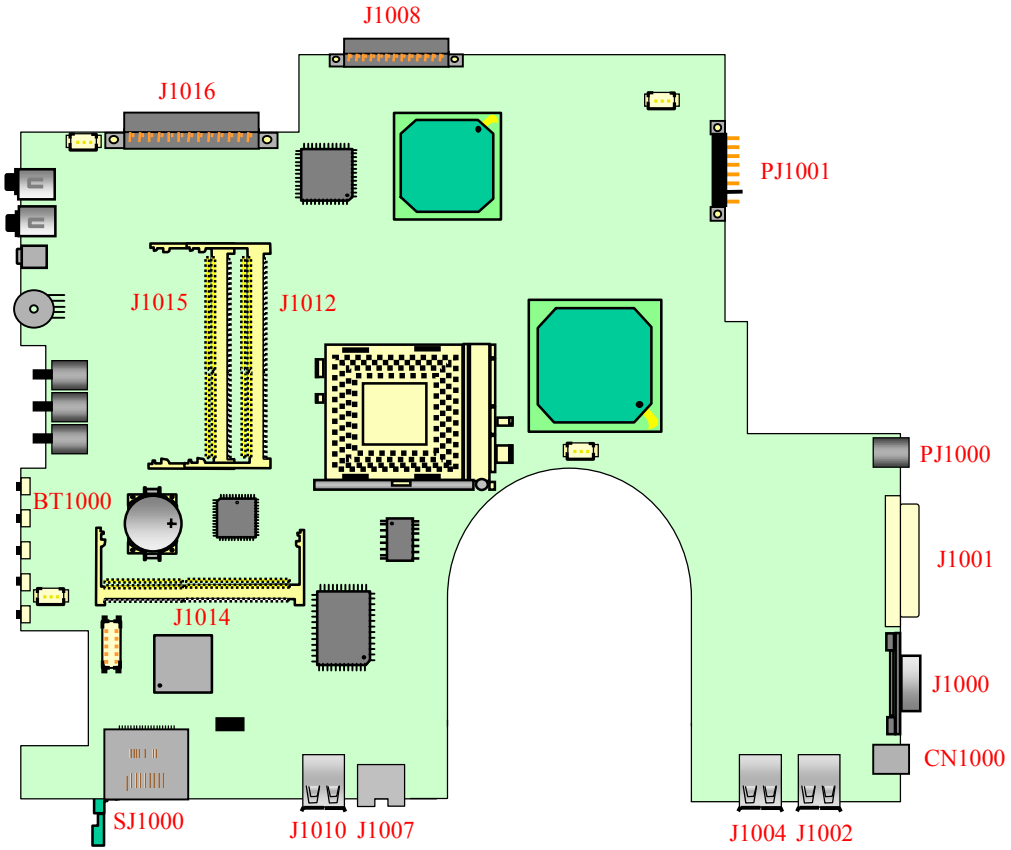
Figure 2-30 Free the shielding

Reassembly

1. Reconnect the cable into the touch pad.
2. Fit the shielding and secure with six screws.
3. Replace the system board, LCD assembly, modem card, DDR, CD/DVD-ROM drive, hard disk drive, CPU, keyboard and battery pack. (See the previous sections reassembly)

3. Definition & Location of Connectors / Switches

3.1 Mother Board-A(1)



- **PJ1000 : Power Jack**
- **PJ1001 : Battery Connector**
- **J1000 : External VGA Connector**
- **J1001 : DVI Port**
- **J1002, J1004, J1010 : USB Port**
- **J1007 : RJ45 Connector**
- **J1008 : Secondary IDE Connector**
- **J1012, J1015 : Extend DDR SDRAM Connector**
- **J1014 : MINI-PCI Connector**
- **J1016 : Serial-ATA and Para-ATA Connector**
- **SJ1000 : Card Reader Socket**
- **BT1000 : CMOS Battery**
- **CN1000 : TV-Out Connector**

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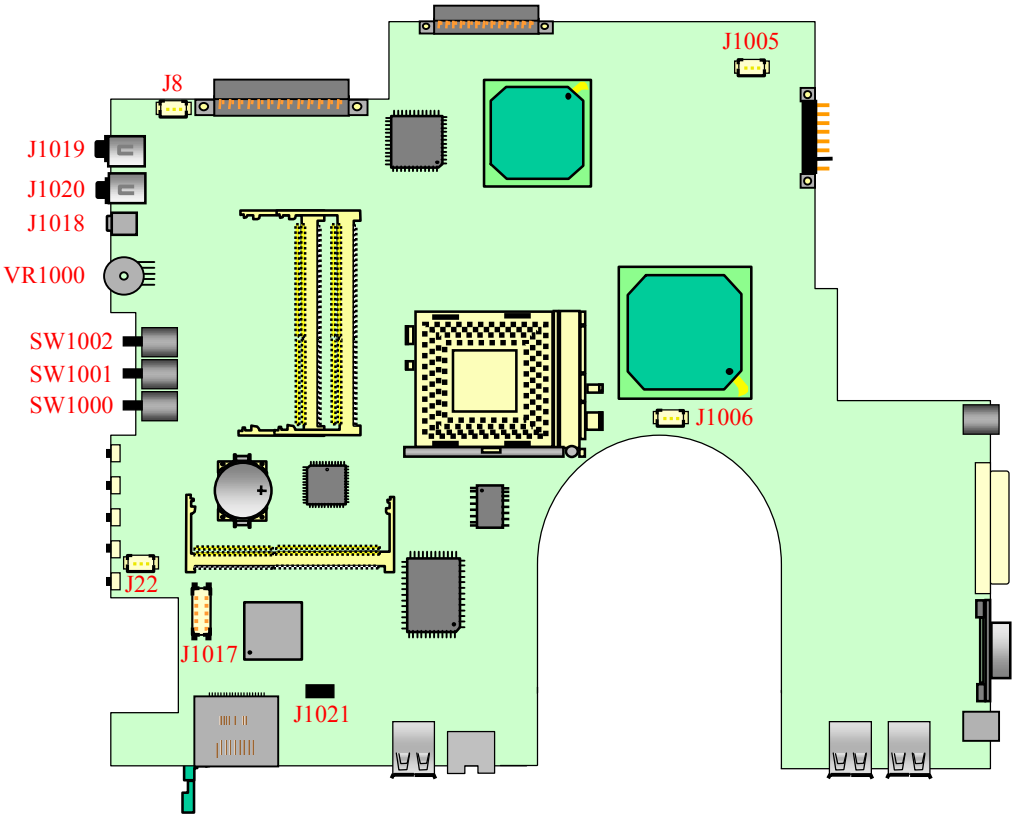
3. Definition & Location of Connectors / Switches

3.1 Mother Board-A(2)



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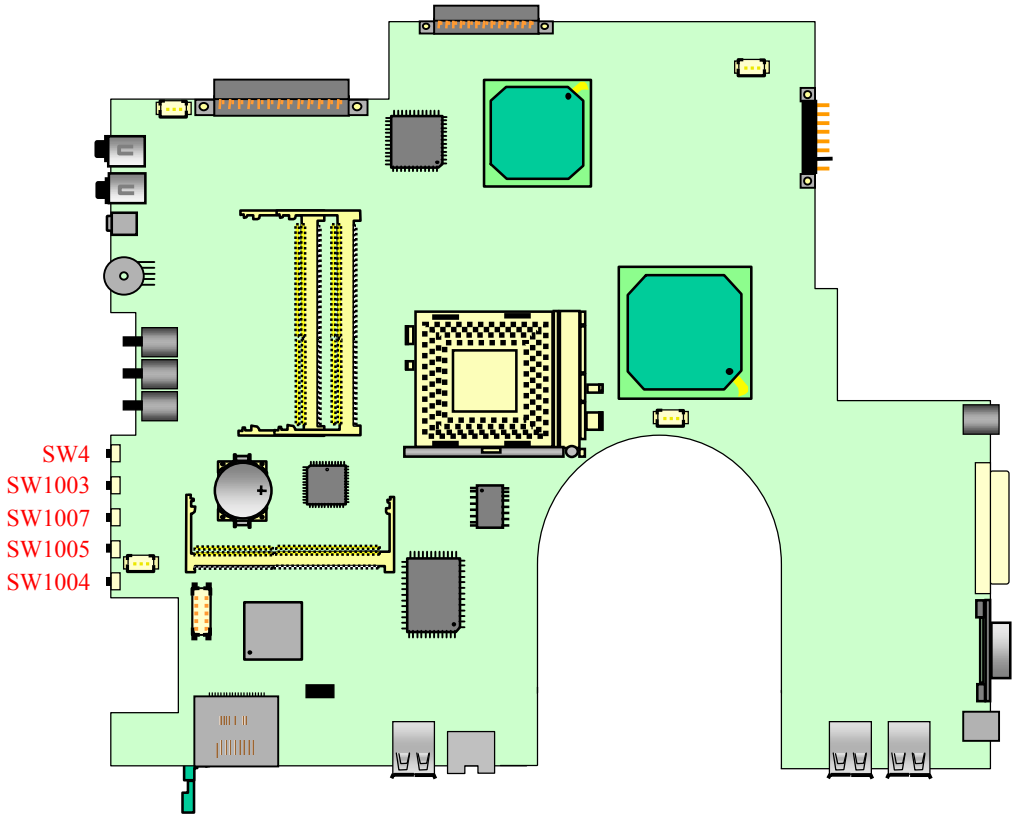
- J8 : Full Range Right Speak Connector
- J22 : Full Range Left Speak Connector
- J1005 : Internal Subwoofer Connector
- J1006 : CPU Fan Connector
- J1017 : MDC Jump Wire Connector
- J1018 : IEEE 1394 Connector
- J1019 : Internal MIC In Connector
- J1020 : Line Out Connector
- J1021 : Daughter Board Connector
- VR1000 : Volume Controller
- SW1002 : Bluetooth On/Off Button(Function SW)
- SW1001 : WLAN On/Off Button(Function SW)
- SW1000 : Lock Button(Function SW)

3. Definition & Location of Connectors / Switches

3.1 Mother Board-A(3)



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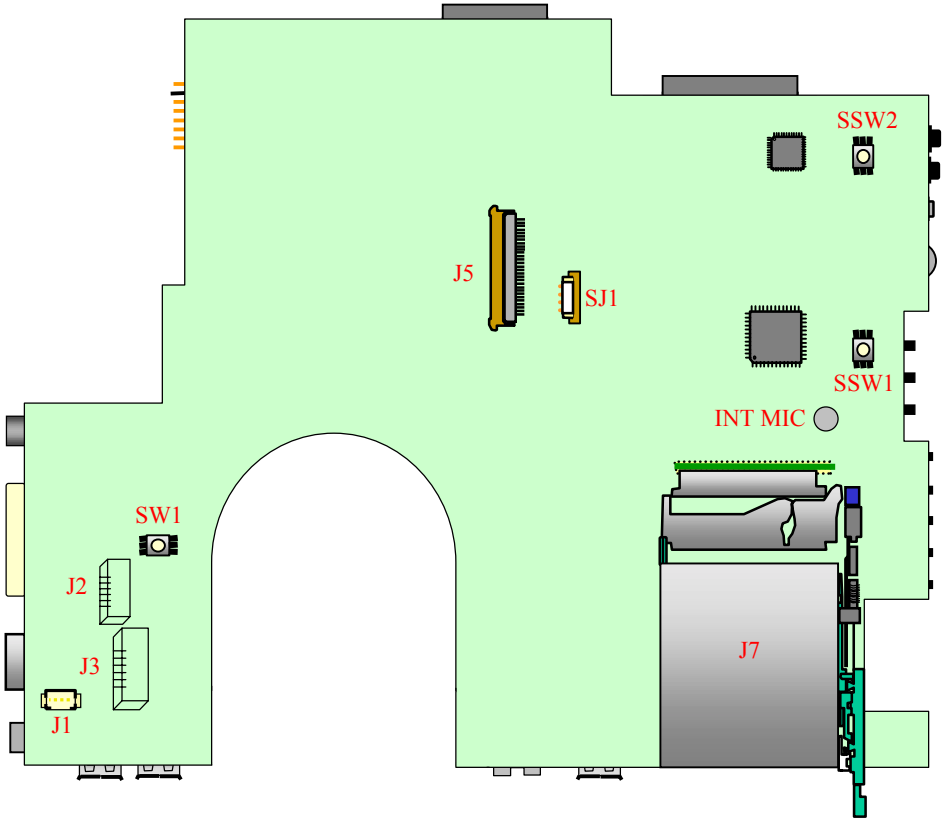
- SW4 : Stop Button(Instant Play SW)
- SW1003 : Forward Button(Instant Play SW)
- SW1004 : Mute Button(Instant Play SW)
- SW1005 : Backward Button(Instant Play SW)
- SW1007 : Play Button(Instant Play SW)

3. Definition & Location of Connectors / Switches

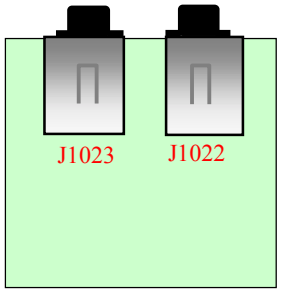
3.1 Mother Board-B



- J1 : Internal Tweeter Speaker Connector
- J2 : Inverter Board Connector
- J3 : LCD Connector
- J5 : Internal Keyboard Connector
- J7 : PCMCIA Card Socket
- SJ1 : Touch-Pad Connector
- SW1 : Power On/Off Button
- SSW1 : Touch-Pad Left Button
- SSW2 : Touch-Pad Right Button

3. Definition & Location of Connectors / Switches

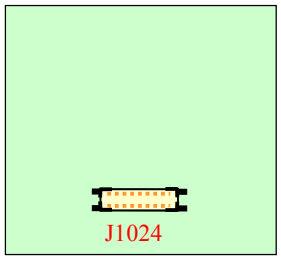
3.2 Audio Jack Board-A



- **J1022 : SPDIF Connector**
- **J1023 : Line In Connector**

3. Definition & Location of Connectors / Switches

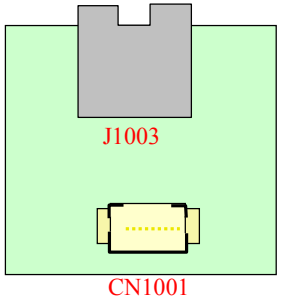
3.2 Audio Jack Board-B



- **J1024 : Daughter Board Connector**

3. Definition & Location of Connectors / Switches

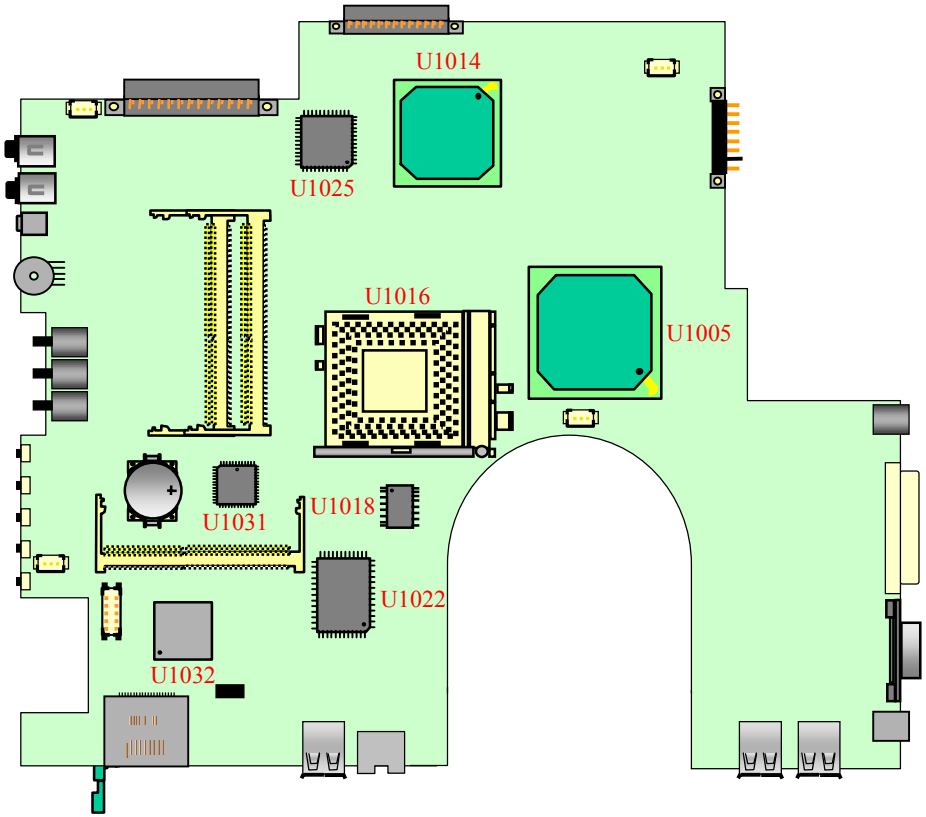
3.3 Modem Board-A



- **J1003 : RJ11 Connector**
- **CN1001 : MDC Board Connector**

4. Definition & Location of Major Components

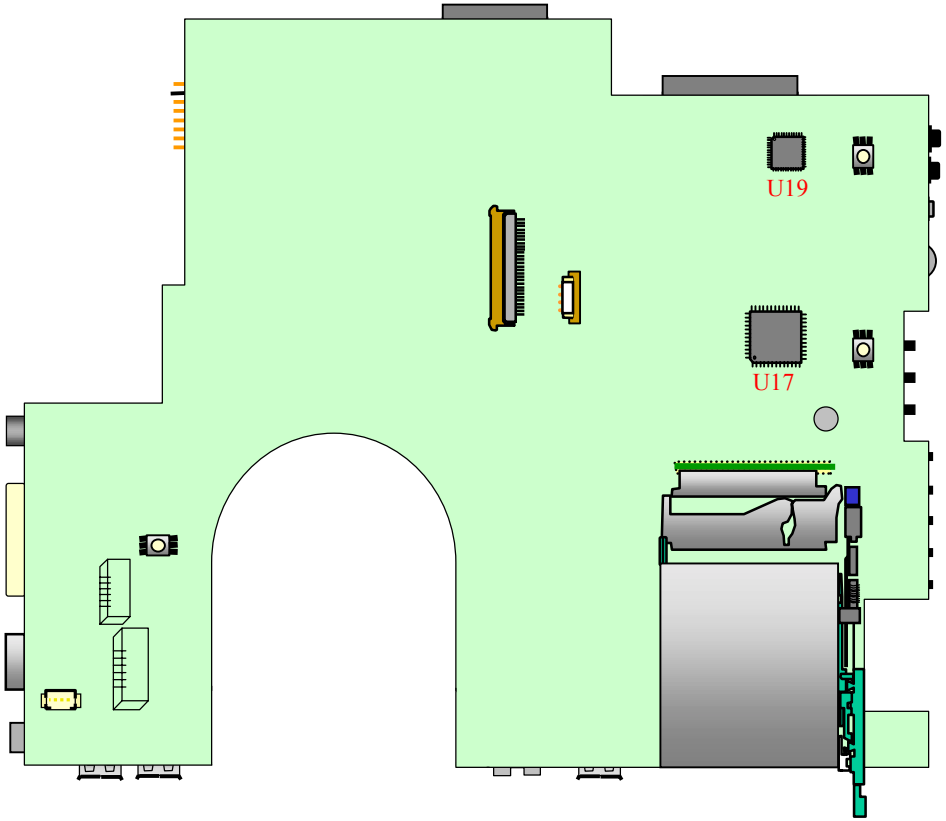
4.1 Mother Board-A



- U1005 : North Bridge(ATI RS480M)
- U1014 : South Bridge(ULI M1573)
- U1016 : CPU (AMD Mobile K8) Socket
- U1018 : ICS951412 Clock Generator
- U1022 : RTL8110SBL LAN Controller
- U1025 : Keyboard BIOS(H8S/2140)
- U1031 : System BIOS
- U1032 : CardBus PCI7411

4. Definition & Location of Major Components

4.1 Mother Board-B



- U17 : Super IO W83L517D
- U19 : Audio Codec ALC880

5. Pin Descriptions of Major Components

5.1 AMD Mobile K8 BGA754_SKT Pin(1)

Miscellaneous Pin Descriptions

Signal Name	Type	Description
RESET_L	I-IOS	System Reset
PWROK	I-IOS	Indicates that voltages and clocks have reached specified operation
LDTSTOP_L	I-IOS	HyperTransport™ Technology Stop Control Input. Used for power management and for changing HyperTransport link width and frequency.
VID[4:0]	O-IOS	Voltage ID to the regulator
THERMDA	A	Anode (+) of the thermal diode
THERMDC	A	Cathode (–) of the thermal diode
THERMTRIP_L	O-IO-OD	Thermal Sensor Trip output, asserted at nominal temperature of 125 ℃.
COREFB_H/L	A	Differential feedback for VDD Power Supply
VDDIOFB_H/L	A	Differential feedback for VDDIO Power Supply
CORE_SENSE	A	VDD voltage monitor pin
VDDA	S	Filtered PLL Supply Voltage
VTT_SENSE	A	VTT voltage monitor pin
VDDIO_SENSE	A	VDDIO voltage monitor pin
VDD	S	Core power supply
VDDIO	S	DDR SDRAM I/O ring power supply
VLDT_A VLDT_B	S	HyperTransport™ I/O ring power supply for side A and side B of the package
VTT_A VTT_B	S	VTT regulator voltage for side A and side B of the die
VSS	S	Ground

Debug Pin Descriptions

Signal Name	Type	Description
DBREQ_L	I-IOS	Debug Request
DBRDY	O-IOS	Debug Ready

JTAG Pin Descriptions

Signal Name	Type	Description
TCK	I-IOS	JTAG Clock
TMS	I-IOS	JTAG Mode Select
TRST_L	I-IOS	JTAG Reset
TDI	I-IOS	JTAG Data Input
TDO	O-IOS	JTAG Data Output

Clock Pin Descriptions

Signal Name	Type	Description
CLKIN_H/L	I-IOD	200-MHz PLL Reference Clock
FBCLKOUT_H/L	O-IOD	Core Clock PLL 200-MHz Feedback Clock

5.1 AMD Mobile K8 BGA754_SKT Pin(2)

DDR SDRAM Memory Interface Pins

Signal Name	Type	Description
MEMCLK_H/L[7]	O-IOD	Differential DDR SDRAM clock to the top of DIMM 0 for unbuffered DIMMs.1
MEMCLK_H/L[6]	O-IOD	Differential DDR SDRAM clock to the top of DIMM 1 for unbuffered DIMMs.1
MEMCLK_H/L[5]	O-IOD	Differential DDR SDRAM clock to the bottom of DIMM 0 for unbuffered DIMMs.1
MEMCLK_H/L[4]	O-IOD	Differential DDR SDRAM clock to the bottom of DIMM 1 for unbuffered DIMMs.1
MEMCLK_H/L[3]	O-IOD	Differential DDR SDRAM clock to DIMM 3 for registered DIMMs.1
MEMCLK_H/L[2]	O-IOD	Differential DDRS DRAM clock to DIMM 2 for registered DIMMs.1
MEMCLK_H/L[1]	O-IOD	Differential DDR SDRAM clock to the middle of DIMM 1 for unbuffered DIMMs, or DIMM 1 for registered DIMMs.1
MEMCLK_H/L[0]	O-IOD	Differential DDR SDRAM clock to the middle of DIMM 0 for unbuffered DIMMs, or DIMM 0 for registered DIMMs.1
MEMCKEA MEMCKEB	O-IOS	Clock Enables to DIMMs. Used to gate clocks for power management functionality.1
MEMDQS[17:0]	B-IOS	DRAM Data Strobes synchronous with MEMDATA and MEMCHECK during DRAM read and writes.1
MEMDATA[63:0]	B-IOS	DRAM Interface Data Bus
MEMCHECK[7:0]	B-IOS	DRAM Interface ECC Check Bits
MEMCS_L[7:0]	O-IOS	DRAM Chip Selects 1
MEMRASA_L MEMRASB_L	O-IOS	DRAM Row Address Select. MEMRASA_L and MEMRASB_L are functionally identical. Two copies are provided to accommodate the loading of unbuffered DIMMs.1
MEMCASA_L MEMCASB_L	O-IOS	DRAM Column Address Select. MEMCASA_L and MEMCASB_L are functionally identical. Two copies are provided to accommodate the loading of unbuffered DIMMs.1
MEMWEA_L MEMWEB_L	O-IOS	DRAM Write Enable. MEMWEA_L and MEMWEB_L are functionally identical. Two copies are provided to accommodate the loading of unbuffered DIMMs.1
MEMADDA[13:0] MEMADDB[13:0]	O-IOS	DRAM Column/Row Address. Two copies are provided to accommodate the loading of unbuffered DIMMs. During precharges, activates, reads, and writes, the two copies are inverted from each other (except A[10] which is used for auto-precharge) to minimize switching noise. The signals are inverted only when the bus is used to carry address information.1

DDR SDRAM Memory Interface Pins (Continued)

Signal Name	Type	Description
MEMBANKA[1:0] MEMBANKB[1:0]	O-IOS	DRAM Bank Address. Two copies are provided to accommodate the loading of unbuffered DIMMs. During precharges, activates, reads, and writes the two copies are inverted from each other to minimize switching noise. The signals are inverted only when the bus is used to carry address information.1
MEMRESET_L	O-IOS	DRAM Reset pin for Suspend-to-RAM power management mode. This pin is required for registered DIMMs only.
MEMVREF	VREF	DRAM Interface Voltage Reference 1
MEMZP	A	Compensation Resistor tied to VSS 1
MEMZN	A	Compensation Resistor tied to 2.5 V 1

Notes:

1. For connection details and proper resistor values, see the AMD Athlon™ 64 Processor Motherboard Design Guide*, order# 24665.*

HyperTransport™ Technology Pin Descriptions

Signal Name	Type	Description
L0_CLKIN_H/L[1:0]	I-HT	Link 0 Clock Input
L0_CTLIN_H/L[1:0]	I-HT	Link 0 Control Input 2
L0_CADIN_H/L[15:0]	I-HT	Link 0 Command/Address/Data Input
L0_CLKOUT_H/L[1:0]	O-HT	Link 0 Clock Outputs
L0_CTLOUT_H/L[1:0]	O-HT	Link 0 Control Output
L0_CADOUT_H/L[15:0]	O-HT	Link 0 Command/Address/Data Outputs
L0_REF1	A	Compensation Resistor to VLDT 1
L0_REF0	A	Compensation Resistor to VSS 1

Notes:

*1. These pins are used in an alternating fashion to compensate R TT by internal comparison to 3/4 VLDT and 1/4 VLDTand compensate R ON by comparison to each other around 1/2 VLDT. For proper resistor value, see the*AMD Athlon™ 64 Processor Motherboard Design Guide*, order# 24665.*

2. The unused L0_CTLIN_H/L[1] pins must be properly terminated such that the true pin is pulled High and thecomplement is pulled Low. Refer to the AMD Athlon™ 64 Processor Motherboard Design Guide*, order# 24665, for details.*

5.2 ATI RS480M North Bridge(1)

CPU Interface

Pin Name	Type	Power Domain	Ground Domain	Functional Description
HT_RXCAD[15:0]P, HT_RXCAD[15:0]N	I	VDDHT	VSS	Receiver Command, Address, and Data Differential Pairs
HT_RXCLK[1:0]P, HT_RXCLK[1:0]N	I	VDDHT	VSS	Receiver Clock Signal Differential Pair. Forwarded clock signal. Each byte of RXCAD uses a different clock signal. Data is transferred on each clock edge.
HT_RXCTLP, HT_RXCTLN	I	VDDHT	VSS	Receiver Control Differential Pair. For distinguishing control packets from data packets.
HT_TXCAD[15:0]P, HT_TXCAD[15:0]N	O	VDDHT	VSS	Transmitter Command, Address, and Data Differential Pairs
HT_TXCLK[1:0]P, HT_TXCLK[1:0]N	O	VDDHT	VSS	Transmitter Clock Signal Differential Pair. Each byte of TXCAD uses a different clock signal. Data is transferred on each clock edge.
HT_TXCTLP, HT_TXCTLN	O	VDDHT	VSS	Transmitter Control Differential Pair. Forwarded clock signal. For distinguishing control packets from data packets.
HT_RXCALN	Other	VDDHT	VSS	Receiver Calibration Resistor to VDD_HT power rail.
HT_RXCALP	Other	VDDHT	VSS	Receiver Calibration Resistor to Ground
HT_TXCALP	Other	VDDHT	VSS	Transmitter Calibration Resistor to HTTX_CALN
HT_TXCALN	Other	VDDHT	VSS	Transmitter Calibration Resistor to HTTX_CALP
HTREFCLK	I	HTPVDD	HTPVSS	HyperTransport 66 MHz reference clock from external clock source
HTTSTCLK	I	HTPVDD	HTPVSS	HyperTransport Bus Test Clock. Drives test clock in test mode. Connect to ground in functional mode.

GDDR Side-Port Memory Interface

Pin Name	Type	Power Domain	Ground Domain	Integrated Termination	Functional Description
MEM_A[14:0]	O	VDD_MEM	VSS	None	Memory Address Bus. Provides the multiplexed row and column addresses to the memories.
MEM_RAS#	O	VDD_MEM	VSS	None	Row Address Strobe
MEM_CAS#	O	VDD_MEM	VSS	None	Column Address Strobe
MEM_WE#	O	VDD_MEM	VSS	None	Write Enable Strobe
MEM_CKE	O	VDD_MEM	VSS	None	Clock Enable
MEM_CKP	O	VDD_MEM	VSS	None	Memory Differential Positive Clock
MEM_CKN	O	VDD_MEM	VSS	None	Memory Differential Negative Clock
MEM_CS#	O	VDD_MEM	VSS	None	Chip Select
MEM_DQ[63:0]	I/O	VDD_MEM	VSS	None	Memory Data Bus. Supports SSTL2 and SSTL3.
MEM_DM[7:0]	I/O	VDD_MEM	VSS	None	Data masks for each byte during memory write cycles
MEM_DQS[7:0]P	I/O	VDD_MEM	VSS	None	GDDR Data Strobes. These are bi-directional data strobes for latching read/write data.
MEM_DQS[7:0]N	I/O	VDD_MEM	VSS	None	Do not connect.
MEM_VMODE	I	–	VSS	None	Selects Memory I/O type. This pin must be tied to the appropriate level depending on the memories connected to the interface. For VDD_MEM=2.5V, connect MEM_VMODE 0V. For VDD_MEM=1.8V, connect MEM_VMODE to 1.8V. **NOTES:** (1) All DRAM connected must be of the SAME interface type; (2) In Sleep mode, when the memory power is on and when MEM_VMODE selects VDD_MEM=1.8V, MEM_VMODE pad MUST ALSO have 1.8V applied to it.

5.2 ATI RS480M North Bridge(2)

4 x 1 Lane PCI Express Interface for General Purpose External Devices

Pin Name	Type	Power Domain	Ground Domain	Integrated Termination	Functional Description
GPP_TX0P/SB_TX2P, GPP_TX0N/SB_TX2N	O	VDDA_18	VSSA	50Ω between complements	Transmit Data Differential Pair for general purpose external devices or A-Link Express interface expansion. Connect to an external connector on the motherboard for New Card support or to the IXP for A-Link Expression expansion.
GPP_TX1P/SB_TX3P, GPP_TX1N/SB_TX3N	O	VDDA_18	VSSA	50Ω between complements	Transmit Data Differential Pair for general purpose external devices or A-Link Express interface expansion. Connect to an external connector on the motherboard for New Card support or to the IXP for A-Link Expression expansion.
GPP_TX2P, GPP_TX2N	O	VDDA_18	VSSA	50Ω between complements	Transmit Data Differential Pair. Connect to an external connector on the motherboard for New Card support.
GPP_TX3P, GPP_TX3N	O	VDDA_18	VSSA	50Ω between complements	Transmit Data Differential Pair. Connect to an external connector on the motherboard for New Card support.
GPP_RX0P/SB_RX2P, GPP_RX0N/SB_RX2N	I	VDDA_18	VSSA	50Ω between complements	Receive Data Differential Pair for general purpose external devices or A-Link Express interface expansion. Connect to an external connector on the motherboard for New Card support or to the IXP for A-Link Expression expansion.
GPP_RX1P/SB_RX3P, GPP_RX1N/SB_RX3N	I	VDDA_18	VSSA	50Ω between complements	Receive Data Differential Pair for general purpose external devices or A-Link Express interface expansion. Connect to an external connector on the motherboard for New Card support or to the IXP for A-Link Expression expansion.
GPP_RX2P, GPP_RX2N	I	VDDA_18	VSSA	50Ω between complements	Receive Data Differential Pair. Connect to an external connector on the motherboard for New Card support.
GPP_RX3P, GPP_RX3N	I	VDDA_18	VSSA	50Ω between complements	Receive Data Differential Pair. Connect to an external connector on the motherboard for New Card support.

Clock Interface

Pin Name	Type	Power Domain	Ground Domain	Integrated Termination	Functional Description
HTREFCLK	I	HTPVDD	HTPVSS	–	HyperTransport 66 MHz reference clock from external clock source
	I	HTPVDD	HTPVSS	–	HyperTransport Bus Test Clock. Drives test clock in test mode Connect to ground in functional mode.
TVCLKIN	I	VDDR3	VSS	–	Input pin for reference clock for TV-out support (3.3 volt signaling)
OSCOUT		VDDR3	VSS	Disabled	Buffered output of 14MHz reference clock to the IXP (3.3 volt signaling)
OSCIN	I	VDDR3	VSS	Disabled	14MHz Reference clock input from the External Clock chip (3.3 volt signaling)

CRT and TV Interface

Pin Name	Type	Power Domain	Ground Domain	Integrated Termination	Functional Description
RED	A-O	AVDD	AVSSN	–	Red for CRT monitor output
GREEN	A-O	AVDD	AVSSN	–	Green for CRT monitor output
BLUE	A-O	AVDD	AVSSN	–	Blue for CRT monitor output
Y	A-O	AVDD	AVSSN	–	SVID luminance output for TV out
C	A-O	AVDD	AVSSN	–	SVID chrominance output for TV out
COMP	A-O	AVDD	AVSSN	–	Composite video TV output
DACHSYNC	A-O	VDDR3	VSS	50kΩ programmable: PU/PD/none	Display Horizontal Sync
DACVSYNC	A-O	VDDR3	VSS	50kΩ programmable: PU/PD/none	Display Vertical Sync
RSET	Other	N/A	AVSSQ	–	DAC internal reference to set full scale DAC current through 1% resistor to AVSS
DACSCL	I/O	VDDR3	VSS	50kΩ programmable: PU/PD/none	I2C clock for VGA interface (to video monitor)
DACSDA	I/O	VDDR3	VSS	50kΩ programmable: PU/PD/none	I2C data for VGA interface (to video monitor)

5.2 ATI RS480M North Bridge(3)

LVDS Interface

Pin Name	Type	Power Domain	Ground Domain	Integrated Termination	Functional Description
TXOUT_U0N	O	LVDDR18A	LVSSR	None	LVDS upper data channel 0 (-) Transmitting at a bit rate of 7x pixel clock, up to 85MHz pixel clock. Only used in dual-channel LVDS mode
TXOUT_U0P	O	LVDDR18A	LVSSR	None	LVDS upper data channel 0 (+) Transmitting at a bit rate of 7x pixel clock, up to 85MHz pixel clock. Only used in dual-channel LVDS mode.
TXOUT_U1N	O	LVDDR18A	LVSSR	None	LVDS upper data channel 1 (-) Transmitting at a bit rate of 7x pixel clock, up to 85MHz pixel clock. Only used in dual-channel LVDS mode.
TXOUT_U1P	O	LVDDR18A	LVSSR	None	LVDS upper data channel 1 (+) Transmitting at a bit rate of 7x pixel clock, up to 85MHz pixel clock. Only used in dual-channel LVDS mode.
TXOUT_U2N	O	LVDDR18A	LVSSR	None	LVDS upper data channel 2 (-) Transmitting at a bit rate of 7x pixel clock, up to 85MHz pixel clock. Only used in dual-channel LVDS mode.
TXOUT_U2P	O	LVDDR18A	LVSSR	None	LVDS upper data channel 2 (+) Transmitting at a bit rate of 7x pixel clock, up to 85MHz pixel clock. Only used in dual-channel LVDS mode.
TXOUT_U3N	O	LVDDR18A	LVSSR	None	LVDS upper data channel 3 (-) Transmitting at a bit rate of 7x pixel clock, up to 85MHz pixel clock. Only used in dual-channel LVDS mode.
TXOUT_U3P	O	LVDDR18A	LVSSR	None	LVDS upper data channel 3 (+) Transmitting at a bit rate of 7x pixel clock, up to 85MHz pixel clock. Only used in dual-channel LVDS mode.
TXCLK_UN	O	LVDDR18A	LVSSR	None	LVDS upper clock channel (-) Transmitting at pixel clock rate, up to 85MHz pixel clock. Only used in dual-channel LVDS mode.
TXCLK_UP	O	LVDDR18A	LVSSR	None	LVDS upper clock channel (+) Transmitting at pixel clock rate, up to 85MHz pixel clock. Only used in dual-channel LVDS mode.

LVDS Interface (Continued)

Pin Name	Type	Power Domain	Ground Domain	Integrated Termination	Functional Description
TXOUT_L0N	O	LVDDR18A	LVSSR	None	LVDS lower data channel 0 (-) Transmitting at a bit rate of 7x pixel clock, up to 85MHz pixel clock. This channel is used as the transmitting channel in single channel LVDS mode.
TXOUT_L0P	O	LVDDR18A	LVSSR	None	LVDS lower data channel 0 (+) Transmitting at a bit rate of 7x pixel clock, up to 85MHz pixel clock. This channel is used as the transmitting channel in single channel LVDS mode.
TXOUT_L1N	O	LVDDR18A	LVSSR	None	LVDS lower data channel 1 (-) Transmitting at a bit rate of 7x pixel clock, up to 85MHz pixel clock. This channel is used as the transmitting channel in single channel LVDS mode.
TXOUT_L1P	O	LVDDR18A	LVSSR	None	LVDS lower data channel 1 (+) Transmitting at a bit rate of 7x pixel clock, up to 85MHz pixel clock. This channel is used as the transmitting channel in single channel LVDS mode.
TXOUT_L2N	O	LVDDR18A	LVSSR	None	LVDS lower data channel 2 (-) Transmitting at a bit rate of 7x pixel clock, up to 85MHz pixel clock. This channel is used as the transmitting channel in single channel LVDS mode.
TXOUT_L2P	O	LVDDR18A	LVSSR	None	LVDS lower data channel 2 (+) Transmitting at a bit rate of 7x pixel clock, up to 85MHz pixel clock. This channel is used as the transmitting channel in single channel LVDS mode.
TXOUT_L3N	O	LVDDR18A	LVSSR	None	LVDS lower data channel 3 (-) Transmitting at a bit rate of 7x pixel clock, up to 85MHz pixel clock. This channel is used as the transmitting channel in single channel LVDS mode.
TXOUT_L3P	O	LVDDR18A	LVSSR	None	LVDS lower data channel 3 (+) Transmitting at a bit rate of 7x pixel clock, up to 85MHz pixel clock. This channel is used as the transmitting channel in single channel LVDS mode.

5.2 ATI RS480M North Bridge(4)

LVDS Interface (Continued)

Pin Name	Type	Power Domain	Ground Domain	Integrated Termination	Functional Description
TXCLK_LN	O	LVDDR18A	LVSSR	None	LVDS lower clock channel (-) Transmitting at pixel clock rate, up to 85MHz pixel clock. This channel is used as the transmitting channel in single channel LVDS mode.
LPVSS	Gnd	–	–	–	LVDS PLL macro ground pin.
LVDDR18D	Pwr	–	–	–	1.8V LVDS Digital Power, used for the digital portions of the LVDS transmitter.
LVSSR	Gnd	–	–	–	LVDS IO ground pin.
LVDS_BLON	I/O	VDDR3	VSS	50kΩ programmable: PU/PD/none	Digital panel backlight brightness control. Active high. It controls backlight on/off or acts as PWM output to adjust brightness. If LVDS_GEN_CNTL.LVDS_BL_MOD_EN = 0, the pin controls backlight on/off. Otherwise, it is the PWM output to adjust the brightness. LVDS_GEN_CNTL.LVDS_BL_MOD_LEVEL can be used to control the backlight level (256 steps) by means of pulse width modulation. The duty cycle of the backlight signal can be set through the LVDS_GEN_CNTL.LVDS_BL_MOD_LEVEL bits. For example, setting these bits to a value of 32 will set the on-time to 32/256*(1/f) and the off-time to (256-32)/256*(1/f), where f is the XTALIN frequency and is typically 14MHz. Note that the PWM frequency can range from 5Hz to 50KHz and is set by LVDS_PWM_CNTL.PWM_CLK_CONF. For more information, refer to the Register Reference Manual. In CPIS mode, LVDS_BLON is VARY_BL as defined in CPIS. PWM mode should be enabled. LVDS_BLEN should be connected to ENA_BL, which turns the backlight AC inverter on/off.

LVDS Interface (Continued)

Pin Name	Type	Power Domain	Ground Domain	Integrated Termination	Functional Description
TXCLK_LP	O	LVDDR18A	LVSSR	None	LVDS lower clock channel (+) Transmitting at pixel clock rate, up to 85MHz pixel clock. This channel is used as the transmitting channel in single channel LVDS mode.
LPVDD	Pwr	–	–	–	Power for LVDS PLL macro (1.8V).
LVDDR18A	A-Pwr	–	–	–	1.8V LVDS Analog Power, used for the output stage of the transmitter. This power supply needs to be adequately filtered to prevent noise injection.
LVDS_DIGON	I/O	VDDR3	VSS	50kΩ programmable: PU/PD/none	Control Panel Digital Power On/Off. Active high.
LVDS_BLEN	I/O	VDDR3	VSS	50kΩ programmable: PU/PD/none	Enables Backlight for CPIS compliant LVDS panels. Active high.Controlled by the hardware power up/down sequencer. For more details, refer to *Figure 4-3, "LCD Panel Power Up/Down Timing," on page 4-* 3.

1 x 16 Lane PCI Express Interface for External Graphics

Pin Name	Type	Power Domain	Ground Domain	Integrated Termination	Functional Description
GFX_TX[15:0]P, GFX_TX[15:0]N	O	VDDA_18	VSSA	50Ω between complements	Transmit Data Differential Pairs. Connect to external connector for an external graphics card on the motherboard (if implemented).
GFX_RX[15:0]P, GFX_RX[15:0]N	I	VDDA_18	VSSA	50Ω between complements	Receive Data Differential Pairs. Connect to external connector for an external graphics card on the motherboard (if implemented).
GFX_CLKP, GFX_CLKN	I/O	VDDA_18	VSSA	50Ω between complements	Clock Differential Pairs. Connect to external clock generator when an external graphics card is implemented.

5.2 ATI RS480M North Bridge(5)

Power Management Pins

Pin Name	Type	Power Domain	Ground Domain	Functional Description
SYSRESET#	I	VDDR3	VSS	Global Hardware Reset. This signal comes from the south bridge.
SUS_STAT#	I	VDD_18	VSS	Disable internal clock tree during S1-S3 states. Keep frame buffer side port memory, when installed, in self refresh mode when system is in S3 mode. (NOTE: Signaling level is 1.8V)
POWERGOOD	I	VDDR3	VSS	Input from the motherboard signifying that the power to the RS480M is up and ready. Signal High means all power planes are valid. It is not observed internally until it has been high for more than 6 consecutive REFCLK cycles. The rising edge of this signal is deglitched. Needs an external pull-up to a minimum of 2.5V.
LDTSTOP#	I	VDDR3	VSS	HyperTransport Stop. Input from the IXP to enable and disable the HyperTransport link during system state transitions. For systems requiring power management. Single-ended.
ALLOW_LDTSTOP	O	VDDR3	VSS	Output going to the IXP to allow LDTSTOP assertions: 1 = LDTSTOP# can be asserted 0 = LDTSTOP# has to be de-asserted

GDDR Side-Port Memory Interface (Continued)

Pin Name	Type	Power Domain	Ground Domain	Integrated Termination	Functional Description
MEM_COMPP, MEM_COMPN	Other	VDD_MEM	VSS	None	Memory interface compensation pins for N and P channel devices. Connect through resistors to VDD_MEM and ground respectively (refer to the reference schematics for the proper resistor values).
MEM_VREF	Other	–	VSS	None	Reference voltage(1.25V typ. for SSTL-2 / 0.5 * VDD, 1.5V typ. for SSTL-3 / 0.45 * VDD). **Note:** If the differential signaling interface is not used, this pin must be connected to the memory IO's VDD_MEM (1.8 or 2.5V).
MEM_CAP[2:1]	Other	VDD_MEM	VSS	None	These pads provide off-chip filtering of the VDD_MEM power. This is required for 2.5V support of GDDR.

DVO Interface

Pin Name	DVO Function	Type	Functional Description
MEM_DQ52	DVO_D0	O	DVO Data for panel
MEM_DQ49	DVO_D1	O	DVO Data for panel
MEM_DQ50	DVO_D2	O	DVO Data for panel
MEM_DQ51	DVO_D3	O	DVO Data for panel
MEM_DQ39	DVO_D4	O	DVO Data for panel
MEM_DQ48	DVO_D5	O	DVO Data for panel
MEM_DQ38	DVO_D6	O	DVO Data for panel
MEM_DQ37	DVO_D7	O	DVO Data for panel
MEM_DQ36	DVO_D8	O	DVO Data for panel
MEM_DQ35	DVO_D9	O	DVO Data for panel
MEM_DQ34	DVO_D10	O	DVO Data for panel
MEM_DQ33	DVO_D11	O	DVO Data for panel
MEM_DQ53	DVO_DE	O	DVO Display Enable signal for panel
MEM_DQ54	DVO_HSYNC	O	DVO Horizontal Sync signal for panel
MEM_DQ55	DVO_VSYNC	O	DVO Vertical Sync signal for panel
MEM_DQS4P	DVO_CLK *	O	DVO clock
MEM_DQS4N	DVO_CLK# *	O	DVO clock
TMDS_HPD	DVO_HPD **	I	"Hot Plug" panel detection input pin that monitors if the voltage is greater than 2.0V on the hot-plugging line
I2C_CLK	DVO_DVI_CLK	I/O	DDC clock for the DVO interface
DDC_DATA	DVO_DVI_DATA	I/O	DDC data for the DVO interface

* The clock signal and its inverses are required for implementation of the DVO interface.
** Optional for the implementation of the DVO interface.

5.2 ATI RS480M North Bridge(6)

Miscellaneous Pins

Pin Name	Type	Power Domain	Ground Domain	Integrated Termination	Functional Description
BMREQ#	Out	VDDR3	VSS	–	This pin is connected to the south bridge. This signal indicates that there is a DMA request from a PCI Express Bus device.
I2C_CLK	I/O	VDDR3	VSS	–	I2C interface clock signal. Can also be used simultaneously as DDC interface clock for the LVDS interface or the external DVO interface. It can also be used as GPIO.
I2C_DATA	I/O	VDDR3	VSS	–	I2C interface data signal. Can also be used as GPIO.
DDC_DATA	I/O	VDDR3	VSS	50kΩ programmable: PU/PD/none	Pin for additional DDC Data Channel for the LVDS interface or the external DVO interface. It makes use of I2C_CLK to create an I2C interface. Can also be used as GPIO.
STRP_DATA	I/O	VDDR3	VSS	–	I2C interface data signal for external EEPROM based strap loading. See the RS480M Strap Document for details on the operation. Can also be used as GPIO or NB Voltage throttling on mobile platforms.
TESTMODE	I	VDDR3	VSS	–	When High, puts the RS480M in Tester mode and disables the RS480M from operating normally.
THERMALDIODE_P, THERMALDIODE_N	A-O	–	–	–	Diode connections to external SM Bus microcontroller for monitoring IC thermal characteristics.
TMDS_HPD	I	VDDR3	VSS	PU	TMDS Hot Plug Detect. “Hot Plug” panel detection input pin that monitors if the voltage is greater than 2.0V on the hot-plugging line.
DFT_GPIO[5:0]	I/O	VDDR3	VSS	PU	GPIO for DFT use. **Note:** Because DFT_GPIO[5, 1:0] are used as strap pins (see *Table 3-15, “Strap Definitions for the RS480M”*), they cannot be used for general GPIO functions.

Strap Definitions for the RS480M

Strap Function	Strap Pin	Description
LOAD_MEM_STRAPS#	DFT_GPIO5*	Selects loading of straps from MEM_DQ pins for debug bus 0 : Capture MEM_DQ pins for debug bus straps. **1 : Use Default Values (Default)** Note : More information about straps on the MEM_DQ pins is available in the Debug Bus specification.
HT_FREQ_OVERRIDE	DFT_GPIO[4:3]	Overrides HT Link frequency at power up 00 : Reserved – for testing only. 01 : Reserved – for testing only. 10 : Reserved – for testing only. **11 : 200 MHz (Default)**
HT_WIDTH_OVERRIDE	DFT_GPIO2	Override HT Link width at power up 0 : Reserved – for testing only. **1 : 8 Bit Link (Default)**
LOAD_ROM_STRAPS#	DFT_GPIO1*	Selects loading of strap values from EEPROM 0: I2C master can load strap values from EEPROM if connected, or use default values if not connected **1: Use Default Values (Default)**
SIDE_PORT_EN#	DFT_GPIO0*	Indicates if memory side port is available or not 0: Memory side port available **1: Memory side port NOT available (Default)**

Note: Strap pins marked by “*” cannot be used for general GPIO functions.

PCI Express Interface for Miscellaneous PCI Express Signals

Pin Name	Type	Power Domain	Ground Domain	Functional Description
PCE_ISET	Other	VDDA_18	VSSA	Current Calibration for for Rx Channel
PCE_TXISET	Other	VDDA_18	VSSA	Current Calibration for for Tx Channel
PCE_NCAL	Other	VDDA_18	VSSA	N channel Driver Compensation Calibration for Rx and Tx Channels
PCE_PCAL	Other	VDDA_18	VSSA	P channel Driver Compensation Calibration for Rx and Tx Channels

5.2 ATI RS480M North Bridge(7)

Power Pins

Pin Name	Voltage	Pin Count	Ball Reference	Comments
AVDD	2.5V or 3.3V	2	B27, C27	Dedicated power for the DAC. Effort should be made at the board level to provide as clean a power as possible to this pin to avoid noise injection, which can affect display quality. Adequate decoupling should be provided between this pin and AVSS.
AVDDQ	1.8V	1	E24	DAC Bandgap Reference Voltage
AVDDDI	1.8V	1	C24	Dedicated digital power for the DAC
VDD_CORE	1.2V	47	A22, B21, B22, C21, C22, D21, D22, E21, E22, F21, F22, G21, G22, H21, H22, M13, M15, M17, M19, N12, N14, N16, N18, P13, P15, P17, P19, R12, R14, R16, R18, T13, T15, T17, T19, U12, U14, U16, U18, V13, V15, V17, V19, W12, W14, W16, W18	Core power
VDD_18	1.8V	3	AC15, AC17, H15	I/O Transform Power for memory, CPU, and GPIO sections.
VDDA_12	1.2 V	14	AA7, AA8, B1, F9, G7, G8, G9, H9, J7, J8, N7, N8, U7, U8	PCI Express interface main I/O power
VDDA_18	1.8V	13	AC7, AC8, AE6, AF5, AF6, AG4, AK2, L7, L8, R7, R8, W7, W8	PCI Express interface power for output Tx stage
VDD_MEM	1.8 / 2.5V	18	AC10, AC12, AC14, AC18, AC20, AC22, AD10, AD12, AD14, AD15, AD18, AD20, AD22, AE30, AK11, AK23, AK28, AK4	Isolated IO power for memory interface

Power Pins (Continued)

Pin Name	Voltage	Pin Count	Ball Reference	Comments
VDD_MEMCK	1.8 / 2.5V	1	AH15	IO Power for memory clocks
VDD_HT	1.2V	31	A23, A29, AA23, AA27, AB23, AB24, AB27, AC30, B23, C23, D23, E23, F23, G23, G27, H23, H27, J23, J27, K23, K24, K27, N27, P24, P27, U23, U27, V23,V24,V27,W23	IO power for HyperTransport interface
VDDR3	3.3V	2	H12, H13	IO power for the following I/O pads: OSC, POWERGOOD, SYSRESET#
LPVDD	1.8V	1	E18	Power for LVDS PLL macro.
LVDDR18D	1.8V	1	E19	1.8V LVDS Digital Power
LVDDR18A	1.8V	2	G20, H20	1.8V LVDS Analog Power
PLLVDD	1.8V	1	A14	Power for PLL
HTPVDD	1.8V	1	M23	Power for HyperTransport interface PLL
MPVDD	1.8V	1	AJ15	Power for memory interface PLL
Total Power Pin Count		140		

1 x 2 Lane A-Link Express Interface for IXP

Pin Name	Type	Power Domain	Ground Domain	Integrated Termination	Functional Description
SB_TX[1:0]P, SB_TX[1:0]N	O	VDDA_18	VSSA	50Ω between complements	Transmit Data Differential Pairs. Connect to the corresponding Receive Data Differential pairs on the IXP.
SB_RX[1:0]P, SB_RX[1:0]N	I	VDDA_18	VSSA	50Ω between complements	Receive Data Differential Pairs. Connect to the corresponding Transmit Data Differential pairs on the IXP.
SB_CLKP, SB_CLKN	I/O	VDDA_18	VSSA	50Ω between complements	Clock Differential Pair. Connect to an external clock generator on the motherboard.

5.2 ATI RS480M North Bridge(8)

Ground Pins

Pin Name	Pin Count	Ball Reference	Comments
AVSSN	2	D25, D26	Dedicated analog ground for the DAC.
AVSSQ	1	D24	Dedicated ground for the Band Gap Reference. Effort should be made at the board level to provide as clean a ground as possible to this pin to avoid noise injection, which can affect display quality. Adequate decoupling should be provided between this pin and AVDD.
LVSSR	8	E20, F18, F19, F20, G18, G19, H18, H19	LVDS Interface ground pin. For Desktop: bond it to VSS (core ground) on the substrate
VSS	131	AA28, AB25, AB28, AC11, AC13, AC16, AC19, AC21, AC23, AC27, AC9, AD11, AD13, AD16, AD17, AD19, AD21, AD23, AD24, AD25, AD27, AD28, AD29, AD7, AD8, AD9, AE26, AE27, AF30, AG12, AG15, AG18, AG21, AG24, AG27, AG5, AG6, AG9, AJ30, AK10, AK22, AK29, AK5, B30, C28, D10, D11, D12, D15, D9, E15, E16, E26, E9, F15, F16, F24, F25, F26, F27, F28, G10, G11, G12, G13, G14, G15, G16, G17, G28, G30, H10, H11, H14, H16, H17, H24, H28, J28, K25, K28, L27, M12, M14, M16, M18, M24, M27, N13, N15, N17, N19, N28, P12, P14, P16, P18, P25, P28, R13, R15, R17, R19, R23, R27, T12, T14, T16, T18, T23, T24, T27, U13, U15, U17, U19, U28, V12, V14, V16, V18, V25, V28, W13, W15, W17, W19, W27, Y23, Y24, Y27	Common Ground

Ground Pins (Continued)

Pin Name	Pin Count	Ball Reference	Comments
AVSSDI	1	B24	Dedicated digital ground for the DAC (1.8V)
LPVSS	1	F17	LVDS PLL macro ground pin. For Desktop: bond it to VSS (core ground) on the substrate
VSSA	68	A2 AA3, AA5, AA6, AB3, AB7, AB8, AD3, AD5, AD6, AE3, AE5, AF3, AG3, AJ1, B4, C2, C3, C4, C5, C6, C7, C8, C9, D3, D6, E5, E6, F3, F5, F6, F7, F8, G3, H7, H8, J3, J5, J6, K3, K7, K8, L5, L6, M3, M5, M6, M7, M8, N3, P7, P8, R3, R5, R6, T3, T7, T8, U5, U6, V3, V5, V6, V7, V8, W3, Y7, Y8	PCI Express Interface Ground
PLLVSS	1	B14	Ground pin for PLL
HTPVSS	1	L23	Ground pin for HyperTransport interface PLL
MPVSS	1	AJ14	Ground pin for memory interface PLL
Total Ground Pin Count	215		

5.3 ULI M1573 South Bridge(1)

PCI Interface

Pin Name	I/O Type	Description
PCICLK	I	**PCI Clock for Internal PCI Interface.** This is a PCI clock input that is controlled by clock generator.
PCI_OUTCLK[9:0]	O	**PCI Clock Output.** This is PCI output clocks for PCI device.
PCICLK_FBKO	O	**PCI Clock Feedback Out Signal.** This is a PCI clock feedback input path.
PCICLK_FBKI	I	**PCI Clock Feedback In Signal.** This is a PCI clock feedback input path.
PCIREQ#[3:0] PCIREQ#[6:4]/ RUNGPI[6:4]	I	**PCI Requests.** PCI master requests for the PCI bus ownership. M1573 supports up to 7 masters on the PCI bus. PCIREQ#[0] is programmable to have the highest priority of the PCI arbitration for supporting PCI-based 1394 controller. PCIREQ#[6:4] can be configured as RUNGPI.
PCIGNT#[3:0] PCIGNT#[6:4]/ RUNGPO[6:4]	O	**PCI Grants.** PCI master be granted for the PCI bus ownership. M1573 supports up to 7 masters on the PCI bus. PCIGNT#[6:4] can be configured as RUNGPO.
PIRQ#[D:A] PIRQ#[H:E]/ RUNGPI[10:7]	I	**PCI Interrupt Requests.** In legacy 8259 mode, PIRQ#[H:A] signals can be routed to legacy IRQs through the routing table defined in the PCI-legacy device configuration registers 4Bh – 48h. In APIC mode, PIRQ#[A] is connected to entry-16, PIRQ#[B] to entry-17, PIRQ#[C] to entry-18, PIRQ#[D] to entry-19, PIRQ#[E] is connected to entry-20, PIRQ#[F] to entry-21, PIRQ#[G] to entry-22, and PIRQ#[H] to entry-23. PIRQ#[H:E] can be configured as RUNGPI.
CLKRUN#/ RUNGPO[9]	I/O O	**PCI Clock Run control.** This signal is used to support PCI Clock Run CLKRUN# protocol. It can also be configured as RUNGPO.
AD[31:0]	I/O	**PCI Address and Data Multiplexed Bus.** During the first clock of a PCI transaction, AD[31:0] contain a physical address. During subsequent clocks, AD[31:0] contain data.
CBE#[3:0]	I/O	**PCI Bus Command and Byte Enable.** During address phase, CBE#[3:0] define the Bus Command. During the data phase, CBE#[3:0] define the Byte Enables.

PCI Interface (Continued)

Pin Name	I/O Type	Description
FRAME#	I/O	**PCI Cycle Frame.** Cycle Frame is driven by current initiator to indicate the beginning and duration of a PCI access.
IRDY#	I/O	**PCI Initiator Ready.** Initiator Ready indicates the initiator's ability to complete the current data phase of the transaction.
TRDY#	I/O	**Target Ready.** Target Ready indicates the target's ability to complete the current data phase of the transaction.
DEVSEL#	I/O	**PCI Device Select.** This signal indicates that the target device has decoded the address as its own cycle.
STOP#	I/O	**Cycle Stop Request.** Cycle Stop indicates the target is requesting the master to stop the current transaction.
SERR#	I	**PCI System Error.** This signal may be pulsed active by any agent that detects a system error condition. When SERR# is sampled low, the M1573 will assert NMI to generate non-maskable interrupt to CPU.
PAR	I/O	**PCI Parity Signal.** PAR is an Even Parity and is calculated on AD[31:0] and CBE#[3:0].
PCIRST#	O	**PCI Bus Reset.** This is an output signal to reset the entire PCI Bus.
PME#	I/O	**PCI Power Management Event.** This signal is used by a PCI device to request a change of its power consumption state. Typically, an active PME# issued by a device is to wake up a power saving state of device or system to the fully operational state.

5.3 ULI M1573 South Bridge(2)

LAN Interface

Pin Name	I/O Type	Description
MII Interface		
MII_COL	I	**Collision Detect.** Asserted high to indicate detection of collision conditions in 10Mbps and 100Mbps Half Duplex modes. In Full Duplex mode, this signal is always logic 0. There is no heartbeat function in Full-Duplex mode.
MII_CRS	I	**Carrier Sense.** This pin is asserted high to indicate the presence of carrier due to receive or transmit activities in 10BASE-T or 100BASE-TX Half Duplex modes. In Repeater, when Full Duplex or Loopback mode is a logic 1, it indicates the presence of carrier due only to receive activity.
MII_RXER	I	**Receiver Error.** Receiver error asserts when a data decoding error is detected by the external PHY device.
MII_RXC	I	**Receive Clock.** Provides the recovered receive clock for different modes of operation: - 25MHz nibble clock in 100Mbps mode - 2.5MHz nibble clock in 10Mbps nibble mode
MII_RXD[3:0]	I	**Receive Data.** Nibble wide receive data (synchronous to RX_CLK – 25MHz for 100BASETX mode, 2.5MHz for 10BASE-T nibble mode).
MII_RXDV	I	**Receive Data Valid.** Data valid is asserted by the external PHY device when receive data is present on the RXD lines and is de-asserted at the end of packet.
MII_TXC	I	**Transmit Clock.** Transmit clock input from the PHY. - 25MHz nibble transmit clock derived from transmit Phase Locked Loop(TX PLL) in 100BASE-TX mode - 2.5MHz transmit clock in 10BASE-T nibble mode
MII_TXD[3:0]	O	**Transmit Data.** Transmit data output pins for nibble data from the MII in 100Mbps or 10Mbps nibble mode (25 MHz for 100Mbps mode, 2.5MHz for 10Mbps nibble mode).
MII_TXEN	O	**Transmit Enable.** Active high output indicates the presence of valid nibble data on TXD[3:0] for both 100Mbps or 10Mbps nibble mode.

LAN Interface (Continued)

Pin Name	I/O Type	Description
MII Interface		
MII_MDC	O	**Management Data Clock.** Synchronous clock to the MDIO management data input/output serial interface which is asynchronous to transmit and receive clocks. The maximum clock rate is 2.5MHz.
MII_MDIO	I/O	**Management Data I/O.** Bi-directional management instruction/data signal that may be sourced by the station management entity or the PHY. This pin requires a 4.7Kohm pull-up resistor.
EEPROM Interface		
EEDO	O	**Serial EEPROM data output** It is connected to DI(data input) pin of the serial EEPROM and used to transfer the data from the south bridge to the EEPROM. The Serial ROM is used to auto-load Ethernet GUID.
EEDI	I	**Serial EEPROM data input** It is connected to DO(data output) pin of the serial EEPROM and used to transfer the data from the EEPROM to south bridge. The Serial ROM is used to auto-load Ethernet GUID.
EECS	O	**EEPROM Chip Select.** This pin will enable the EEPROM during loading of the Configuration Data.
EECK	O	**EEPROM Serial Clock.** This pin provides the clock for the EEPROM data transfer.

SMBus Interface

Pin Name	I/O Type	Description
SMB_ALERT#/ RSMGPI[10]	I	SMBus Alert SMBus devices can signal alert to SMBus host by asserting this signal to generate SMI or to wake up the system. This pin can be configured as RSMGPI.
SMB_CLK	I/OD	SMBus Clock SMBus clock signal driven by cycle initiator.
SMB_DATA	I/OD	SMBus Data SMBus data signal carries serial data information based on SMCLK.

5.3 ULI M1573 South Bridge(3)

IDE Interface

Pin Name	I/O Type	Description
Parallel ATA Interface		
PIDEA[2:0]	O	**Primary Channel IDE ATA Address Bus.** These are the Address pins connected to Primary Channel.
PIDECS1#	O	**Primary Channel 0 IDE Chip Select 1.** This is the Chip Select 1 command output pin to enable the Primary IDE device to watch the Read/Write Command.
PIDECS3#	O	**Primary Channel 1 IDE Chip Select 3.** This is the Chip Select 3 command output pin to enable the Primary IDE device to watch the Read/Write Command.
PIDED[15:0]	I/O	**Primary IDE ATA Data Bus.** These are the Data pins connected to Primary Channel.
PIDEDAK#	O	**Primary IDE DACK# for IDE Master.** This is the output pin to grant the Primary Channel IDE DMA request to begin the IDE Master Transfer in DMA or Ultra-33/66/100/133 mode.
PIDEDRQ	I	**Primary IDE DMA Request for IDE Master.** This is the input pin from the Primary Channel IDE DMA request to do the IDE Master Transfer. It will be active high in DMA or Ultra-33/66/100/133 mode and always be inactive low in PIO mode.
PIDEIOR#	O	**Primary IDE IOR# Command.** This is the IOR# command output pin to notify the Primary IDE device to assert the Read Data in PIO and DMA mode. In Ultra-33/66/100/133 mode, this pin has different functions. In read cycle, this pin is used by IDE Controller to notify IDE device as DMA Ready (DDMARDY#). In write cycles, IDE Controller will drive this signal as Data Strobe (DSTROBE) to use by IDE device to strobe the output data.
PIDEIOW#	O	**Primary IDE IOW# Command.** This is the IOW# command output pin to notify the Primary IDE device that the available Write Data is already asserted by IDE Controller in PIO and DMA mode. In Ultra-33/66/100/133 mode, this pin is driven by IDE Controller to force IDE device to terminate current transaction. After receiving this input, IDE device will de-assert DRQ to STOP current transaction.
PIDEIRQ	I	**Primary IDE IRQ Input1.** This is a steer-able Interrupt input, the M1573 will provide a Routing Mechanism to route this Interrupt to any 8259 input for built-in IDE Controller.

IDE Interface (Continued)

Pin Name	I/O Type	Description
Parallel ATA Interface		
PIDERDY	I	**Primary IDE Ready.** This is the input pin from the Primary IDE Channel to indicate the IDE device is ready to terminate the IDE command in PIO mode. The IDE device can de-assert this input (logic 0) to expand the IDE command if the device is not ready. In Ultra-33/66/100/133 mode, this pin has different functions. In read cycles, IDE device will drive this signal as Data Strobe (DSTROBE) to use by IDE controller to strobe the input data. In write cycle, this pin is used by IDE device to notify IDE Controller as DMA Ready (DDMARDY#).
SIDEA[2:0]	O	**Secondary IDE ATA Address Bus.** These are the Address pins connected to Secondary Channel.
SIDECS1#	O	**Secondary Channel 0 IDE Chip Select 1.** This is the Chip Select 1 command output pin to enable the Secondary IDE device to watch the Read/Write Command.
SIDECS3#	O	**Secondary Channel 1 IDE Chip Select 3.** This is the Chip Select 3 command output pin to enable the Secondary IDE device to watch the Read/Write Command.
SIDED[15:0]	I/O	**Secondary IDE ATA Data Bus.** These are the Data pins connected to Secondary Channel.
SIDEDAK#	O	**Secondary IDE DACK# for IDE Master.** This is the output pin to grant the Secondary Channel IDE DMA request to begin the IDE Master Transfer in DMA or Ultra-33/66/100/133 mode.
SIDEDRQ	I	**Secondary IDE DMA Request for IDE Master.** This is the input pin from the Secondary Channel IDE DMA request to do the IDE Master Transfer. It will be active high in DMA or Ultra-33/66/100/133 mode and always be inactive low in PIO mode.
SIDEIOR#	O	**Secondary IDE IOR# Command.** This is the IOR# command output pin to notify the Secondary IDE device to assert the Read Data in PIO and DMA mode. In Ultra-33/66/100/133 mode, this pin has different functions. In read cycle, this pin is used by IDE Controller to notify IDE device as DMA Ready (DDMARDY#). In write cycle, IDE Controller will drive this signal as Data Strobe (DSTROBE) to use by IDE device to strobe the output data.

5.3 ULI M1573 South Bridge(4)

IDE Interface (Continued)

Pin Name	I/O Type	Description
Parallel ATA Interface		
SIDEIOW#	O	**Secondary IDE IOW# Command.** This is the IOW# command output pin to notify the Secondary IDE device that the available Write Data is already asserted by IDE Controller in PIO and DMA mode. In Ultra-33/66/100/133 mode, this pin is driven by IDE Controller to force IDE device to terminate current transaction. After receiving this input, IDE device will de-assert DRQ to STOP current transaction.
SIDEIRQ	I	**Secondary IDE IRQ Input2.** This is a steer-able Interrupt input, the M1573 will provide a Routing Mechanism to route this Interrupt to any 8259 input for built-in IDE Controller.
SIDERDY	I	**Secondary IDE Ready.** This is the input pin from the Secondary IDE Channel to indicate the IDE device is ready to terminate the IDE command in PIO mode. The IDE device can de-assert this input (logic 0) to expand the IDE command if the device is not ready. In Ultra-33/66/100/133 mode, this pin has different functions. In read cycles, IDE device will drive this signal as Data Strobe (DSTROBE) to use by IDE Controller to strobe the input data. In write cycles, this pin is used by IDE device to notify IDE Controller as DMA Ready (DDMARDY#).
Serial ATA Interface		
SATA0_TX0P, SATA0_TX0N	O	Serial-ATA0 port0 Transmission signal pair
SATA0_RX0P, SATA0_RX0N	I	Serial-ATA0 port0 Receiving signal pair
SATA0_TX1P, SATA0_TX1N	O	Serial-ATA0 port1 Transmission signal pair
SATA0_RX1P, SATA0_RX1N	I	Serial-ATA0 port1 Receiving signal pair
SATA0_REXT	I	SATA0 External Resistor reference for impendence adjustment.
SATA1_TX0P, SATA1_TX0N	O	Serial-ATA1 port0 Transmission signal pair
SATA1_RX0P, SATA1_RX0N	I	Serial-ATA1 port0 Receiving signal pair
SATA1_TX1P, SATA1_TX1N	O	Serial-ATA1 port1 Transmission signal pair

IDE Interface (Continued)

Pin Name	I/O Type	Description
Serial ATA Interface		
SATA1_RX1P, SATA1_RX1N	I	Serial-ATA1 port1 Receiving signal pair
SATA1_REXT	I	SATA1 External Resistor reference for impendence adjustment.
SATA_GPI[3:0]/ RUNGPI[22:19]	I	Serial-ATA General Purpose IO. It can be configured as RUNGPI.
SATA_GPO[3:0]/ RUNGPO[28:25]	O	Serial-ATA1 General Purpose IO. It can be configured as RUNGPO.
SATA_LED	OD	Serial-ATA LED

Host PCI Express Interface

Pin Name	I/O Type	Description
PE_RefClkP, PE_RefClkN	I	**Differential reference clock signals.** Clock frequency ranges from 100 MHz.
Lane Transmit Interface		
SB_TAP, SB_TAN	O	Differential transmit outputs for lane A
SB_TBP, SB_TBN	O	Differential transmit outputs for lane B
SB_TCP, SB_TCN	O	Differential transmit outputs for lane C
SB_TDP, SB_TDN	O	Differential transmit outputs for lane D
Lane Receive Interface		
SB_RAP, SB_RAN	I	Differential receive inputs for lane A
SB_RBP, SB_RBN	I	Differential receive inputs for lane B
SB_RCP, SB_RCN	I	Differential receive inputs for lane C
SB_RDP, SB_RDN	I	Differential receive inputs for lane D
Reference Resistors		
REF	I	Used to connect a (2.4K? +/- 1%) external resistor to VSS to provide a reference current for the driver and equalization circuits

5.3 ULI M1573 South Bridge(5)

Audio Interface

Pin Name	I/O Type	Description
AC-Link Signals		
ACZ_RST#	O	**AC97 Reset Signal.** This is the AC'97 Codec(s) master hardware reset signal output. **HD Audio Reset Signal.** This is the HD Audio Codec(s) master hardware reset signal output.
ACZ_SYNC	O	**AC'97 SYNC Signal.** This signal is used for AC'97 48 KHz fixed rate sample sync. **HD Audio SYNC Signal.** This signal is used for HD Audio 48 KHz fixed rate sample sync.
ACZ_SDOUT	O	**AC'97 Serial Data Output Signal.** This signal is used for serial, time division multiplexing, AC'97 output stream to the Codec(s). **HD Audio Serial Data Output Signal.** This signal is used for serial, time division multiplexing, HD Audio output stream to the Codec(s).
ACZ_BITCLK	I/O	**AC97 Bit Clock Input Signal.** This signal is used for AC97 12.288 MHz serial data clock. **HD Audio Bit Clock Output Signal.** This signal is used for HD Audio 12.288 MHz serial data clock.
ACZ_SDATAIN[2:0]	I/O	**AC97 Serial Data Input[2:0].** These signals are used for serial, TDM (Time Division Multiplexing), AC'97 input stream from the Codecs. **HD Audio Serial Data Input[2:0].** These signals are used for serial, TDM (Time Division Multiplexing), HD Audio input stream from the Codecs.
ACB_RST#/ RSMGPO[10]	O	**AC97 LinkB Reset Signal.** This is the AC'97 Codec(s) master hardware reset signal output. This pin can be configured as RSMGPO.
ACB_SYNC / RUNGPO[23]	O	**AC'97 LinkB SYNC Signal.** This signal is used for AC'97 48 KHz fixed rate sample sync. This pin can be configured as RUNGPO.
ACB_SDOUT / RUNGPO[24]	O	**AC'97 Serial Data Output Signal.** This signal is used for serial, time division multiplexing, AC'97 output stream to the Codec(s). This pin can be configured as RUNGPO.
ACB_BITCLK / RUNGPI[18]	I	**AC97 LinkB Bit Clock Input Signal.** This signal is used for AC97 12.288 MHz serial data clock. This pin can be configured as RUNGPI.

Audio Interface (Continued)

Pin Name	I/O Type	Description
AC-Link Signals		
ACB_SDATAIN / RSMGPI[15]	I	**AC97 LinkB Serial Data Input.** These signals are used for serial, TDM (Time Division Multiplexing), AC'97 input stream from the CODEC. This pin can be configured as RSMGPI.
Audio Miscellaneous Interface		
VOL_UP#/ RUNGPI[11]	I	**Volume Up Control Signal for Audio.** This pin is used to tune up audio volume and connects to AC97 GPIO[1] input. This pin can be configured as RUNGPI.
VOL_DOWN#/ RUNGPI[12]	I	**Volume Down Control Signal for Audio.** This pin is used to down audio volume connects to AC97 GPIO[0] input. This pin can be configured as RUNGPI.
VOL_MUTE#/ RUNGPI[13]	I	**Volume Mute Control Signal for Audio.** This pin is used to mute audio and connects to AC97 GPIO[2] input. This pin can be configured as RUNGPI.

LPC Interface

Pin Name	I/O Type	Description
LFRAME#	O	**Low Pin Count FRAME# Signal.** This signal is the frame signal of Low Pin Count interface.
LAD[3:0]	I/O	**LAD[3:0].** These pins are address/data signals for Low-Pin-Count interface.
LDRQ[0]# LDRQ[1]#/ RUNGPI[14]	I	**Low Pin Count DMA Request Signal[1:0].** These pins are DMA request signals used by LPC devices. LDRQ[1]# can be configured as RUNGPI.

5.3 ULI M1573 South Bridge(6)

PMU Interface

Pin Name	I/O Type	Description
ACPWR (Mobile Only) / RSMGPI[12]	I	**AC Power Plug-in Indication.** This active high input indicates the AC adapter is plugged in the mobile mode. This pin can be configured as RSMGPI.
AGPSTOP# (Mobile Only)	O	**Stop AGP Device Clock.** This signal is used by M1573 to indicate that the AGP clock will be stopped.
CLK32KO/ RSMGPO[8]	O	**32 KHz Clock Output for DRAM Refresh.** In S1 and S3 states, this output will send 32KHz clock to Memory controller to support suspend-mode DRAM refresh. In S4 and S5 states, this output will be driven low. This pin can be configured as RSMGPO.
CPUSTP#/ RUNGPO[7]	O	**CPU Clock Stop.** This output signal controls clock generator to stop the CPU Clock. This signal can be configured as RUNGPO.
LID (Mobile Only) / RSMGPI[14]	I	**LID Cover Switch.** The input indicates LID status of a mobile system and can issue SMI, SCI. This pin can be configured as RSMGPI.
LOWBAT# (Mobile Only) / RSMGPI[13]	I	**Battery Low Indication.** The input indicates the battery status for a mobile system. This pin can be configured as RSMGPI.
OFFCLKS1# / RSMGPO[16]	O	**Clock Generator OFF.** This output signal is used to power down the clock generator. This signal can be configured as RSMGPO.
OFFPWRS3# / RSMGPO[17]	O	**Power Off Control in S3.** This output is used to shut off all the non-required power when system gets into S3-S5 states. This signal can be configured as RSMGPO.
OFFPWRS4_S5# / RSMGPO[18]	O	**Power Off Control in S4/S5.** This output is used to shut off all the non-required power when system gets into S4-S5 states. This signal can be configured as RSMGPO.
PCISTP# / RUNGPO[8]	O	**PCI Clock Stop.** This output is used to control clock generator stopping the PCI Bus Clock. This signal can be configured as RUNGPO.
PWG	I	**Power-Good Input.** This signal indicates that system power is available and stable. M1573 uses this signal to generate reset sequence for the system.

PMU Interface (Continued)

Pin Name	I/O Type	Description
PWRBTN#	I	**Power Button Input.** This input is used to support the ACPI Power Button function. Both 4-second Override to Soft Off state and Resume from Suspend mode functions are supported.
RI	I	**Ring In.** This input connects to Modem Ring-in input to support ACPI Ring-in function. There exists a Ring counter to count the amount of Ring-In pulses for generating events.
RSMRST#	I	**Resume Circuit Reset Input.** The M1573 will activate internal reset signal to initialize the resume-region circuits.
SLPBTN# / RSMGPIL[0]	I	**Sleep Button Input.** This input is used to support the ACPI Sleep Button function. This signal can be configured as RSMGPIL.
SUSLED / RSMGPO[7]	O	**Suspend LED Output**. This output pin controls LED on/off and is served as suspend status indicator. This signal can be configured as RSMGPO.
THRM#	I	**Thermal Event Input.** THRM# is a triggered input and indicates that the external thermal detect circuits request for entering power management mode.
THRMTRIP#	I	**Thermal Trip.** This input is a hardware failsafe mechanism of CPU to avoid damages in thermal run-away situation. It's a 2.5V open-drain output from CPU.
PCIEX_WAKEUP#	I	**PCI Express Wakeup.** This signal is used by the PCI Express devices to wake up system from power suspend states.
DSPVRHI / RUNGPO[10]	O	**Deeper Sleep – Voltage Regulator High/Low Selection.** This signal is used to select the voltage regulator high/low voltage for the CPU normal/deeper sleep state, and can be optionally configured as RUNGPO.
SUSPEND# / RSMGPO[9]	O	**Suspend Status for North Bridge.** This output is used to request the north bridge to switch from normal DRAM refresh to suspend DRAM refresh mode. This signal can be configured as RSMGPO.

5.3 ULI M1573 South Bridge(7)

PMU Interface (Continued)

Pin Name	I/O Type	Description
VRMPWG / VRGATE / ALLOW_HTTSTOP	I	**VRM Power Good (for P4 Desktop) / VRM Power Good Gate(for P4 Mobile)/NB Allow HTTSTOP#(for K8).** In P4 platform, this signal is used indicate that the CPU voltage is stable. In K8 platform, this signal output from the NB to notifies the SB whether it is allowed to assert or deassert HTTSTOP#. This controls the timing of the CPU entering and exiting C3.
AGPBUSY# (Mobile Only) / HTTREQ#(K8 Mode Only)	I	**AGP Device Busy.** This signal is used by M1573 to indicate that the AGP device is busy. **HyperTransport Request.** HTT device can use this input signal to request re-enabling HTT links for normal operation. It can also be used as AGP Busy in HyperTransport system implementation, i.e., the AGPBUSY# from AGP device can be connected to this pin.
VRHI# / RUNGPO[11]	O	**CPU High/Low Voltage Selection.** This signal is used to select the voltage high/low level for the CPU and can be optionally configured as RUNGPO.

Test Signals

Pin Name	I/O Type	Description
DFTSE/ NANDTEST	I	**DFT Scan Enable.** This signal is used as the DFT Scan Enable for ATPG pattern input when DFT_MODE is tied to high. It should be pull-low for normal operation. **NAND Tree TEST pin.** This signal is used as the NANDTREE TEST mode enable if it is tied to high when DFT_MODE is tied to low. It should be pull-low for normal operation.
DFTTM	I	**DFT Test Mode.** This signal is used as the DFT Test Mode Enable for ATPG pattern input. It should be pull-low for normal operation.

Clocks

Pin Name	I/O Type	Description
Real Time Clock Interface		
X32KI	I	**32 KHz Oscillator Input 1. This is a crystal input 1 from a 32.768 KHz Quartz Crystal. The input oscillator pad will generate the 32 KHz clock into the internal Suspend circuit and output the clock from the CLK32KO to DRAM Suspend Refresh Circuit. If a crystal is not used, this pin should be pulled to ground.**
X32KII	I	**32 KHz Oscillator Input 2.** This is a crystal input 2 from a 32.768 KHz Quartz Crystal. The input oscillator pad will generate the 32 KHz clock for the internal Suspend circuit and output the clock from the CLK32KO to DRAM Suspend Refresh Circuit. If a crystal is not used, an external 32 KHz clock input should be connected to this pin.
RTCRST#	I	**RTC Reset.** The input pin is used to reset internal battery-powered RTC SRAM.
X32K_OSC_MODE	I	**32K oscillator PAD large or small current mode switch.** It's Reserved for internal test only and should be tied low.
Other Clocks		
CLK14M	I	**14.318 MHz Clock Input.** This input clock will be used for Power Management timer, 8254 timer.
X25M1	I	Optional external 25MHz crystal input for SATA reference clock
X25M2	I	Optional external 25MHz crystal input for SATA reference clock
CLK24_48M	I	24/48 MHz Clock Output.

Miscellaneous Signals

Pin Name	I/O Type	Description
SPKR	O	**Speaker Output.** This output pin should be connected to the on-board speaker.
SERIRQ	I/O	**Serial Interrupt Request.** This pin is used to support the serial interrupt request protocol of common architecture.

5.3 ULI M1573 South Bridge(8)

CPU Interface

Pin Name	I/O Type	Description
P4 Mode Interface		
A20M# / RUNGPO[12]	O	**CPU A20 Mask.** This is the CPU Address line A20 mask signal. It can be configured as RUNGPO.
CPUHI# (Mobile Only) / RUNGPO[13]	O	**CPU High/Low Performance Selection.** This signal is used to select the CPU high/low performance and can be optionally configured as RUNGPO.
CPUPWG/ RUNGPO[14]	O	**CPU Power Good.** This signal is connected to the PWRGOOD input of CPU and can be optionally configured as RUNGPO.
CPURST#/ RUNGPO[32]	OD	**CPU Cold Reset.** When system is powered on, this reset signal will be asserted and become de-asserted until 4 ms after HTTPWROK becomes high. This pin can be configured as RUNGPO.
DSLEEP#/ RUNGPO[15]	O	**CPU Deep Sleep.** This signal is used to force CPU entering deep sleep state. This signal can be configured as RUNGPO.
FERR#	I	**Floating Point Error.** FERR# input from coprocessor to generate IRQ13.
IGNNE#/ RUNGPO[16]	O	**Ignore Error.** This pin is used as the "ignore numeric coprocessor error" signal and connects to CPU. It can be configured as RUNGPO.
INIT#/ RUNGPO[17]	O	**CPU Initialization.** This signal will be asserted for 16 PCI clocks when M1573 resets the CPU. It can be configured as RUNGPO.
INTR/ RUNGPO[18]	O	**Interrupt Request to CPU.** This is the interrupt signal generated by the internal 8259 and should connect to CPU INTR as a maskable interrupt. It can be configured as RUNGPO.
NMI/ RUNGPO[19]	O	**Non-Maskable Interrupt to CPU.** This is generated by the PCI Parity error or SERR# assertion, and the other internal error event. This output should connect to CPU NMI as a non-maskable interrupt. It can be configured as RUNGPO.
SLEEP#/ RUNGPO[20]	O	**CPU Sleep.** This signal is used to force CPU entering sleep state. This signal can be configured as RUNGPO.
SMI#/ RUNGPO[21]	O	**System Management Interrupt.** This signal should be connected to CPU SMI# input. It can be configured as RUNGPO.

CPU Interface (Continued)

Pin Name	I/O Type	Description
P4 Mode Interface		
STPCLK#/ RUNGPO[22]	O	**Stop CPU Internal Clock Request.** This signal is used to make CPU enter power saving mode and stop the CPU internal clock. The signal should be connected to CPU STPCLK# input. It can be configured as RUNGPO.
A20GATE/ RUNGPI[15]	I	**A20 Gate.** This pin is the external Keyboard A20 gate signal and can be configured as RUNGPI.
KBCRC#/ RUNGPI[16]	I	**Keyboard RC.** This pin is the external Keyboard RC signal and can be configured as RUNGPI.
HTT Interface		
HTTSTOP#/ RUNGPO[31]	OD	**HyperTransport Stop** This output signal is used to enable and disable HyperTransport links during C3/C4 state or system power saving state transitions. This output should be externally pulled high as 2.5V with 10K resistor. This pin can be configured as RUNGPO.
HTTRESET#/ RUNGPO[30]	OD	**HyperTransport Reset** This output signal is used to reset the HyperTransport chain. This output should be externally pulled high as 2.5V with 10K resistor. This pin can be configured as RUNGPO.
HTTPWROK/ RUNGPO[29]	OD	**HyperTransport Power OK.** This output signal is used by a HyperTransport device to indicate that the power and clocks are stable. This output should be externally pulled high as 2.5V with 10K resistor. This pin can be configured as RUNGPO.

General Purpose I/O

Pin Name	I/O Type	Description
RUNGPIO[3:0]/ RUNGPI[3:0]/RUNGPO[3:0]	IO	**General-Purpose Input/Output.** These pins can be configured as RUNGPI[3:0](default) or RUNGPO[3:0].
RSMGPIO[3:0]/ RSMGPO[3:0]/RSMGPI[3:0]	IO	**Resume Region General-Purpose Input/Output**. These pins can be configured as RSMGPI[3:0] or RSMGPO[3:0](default).

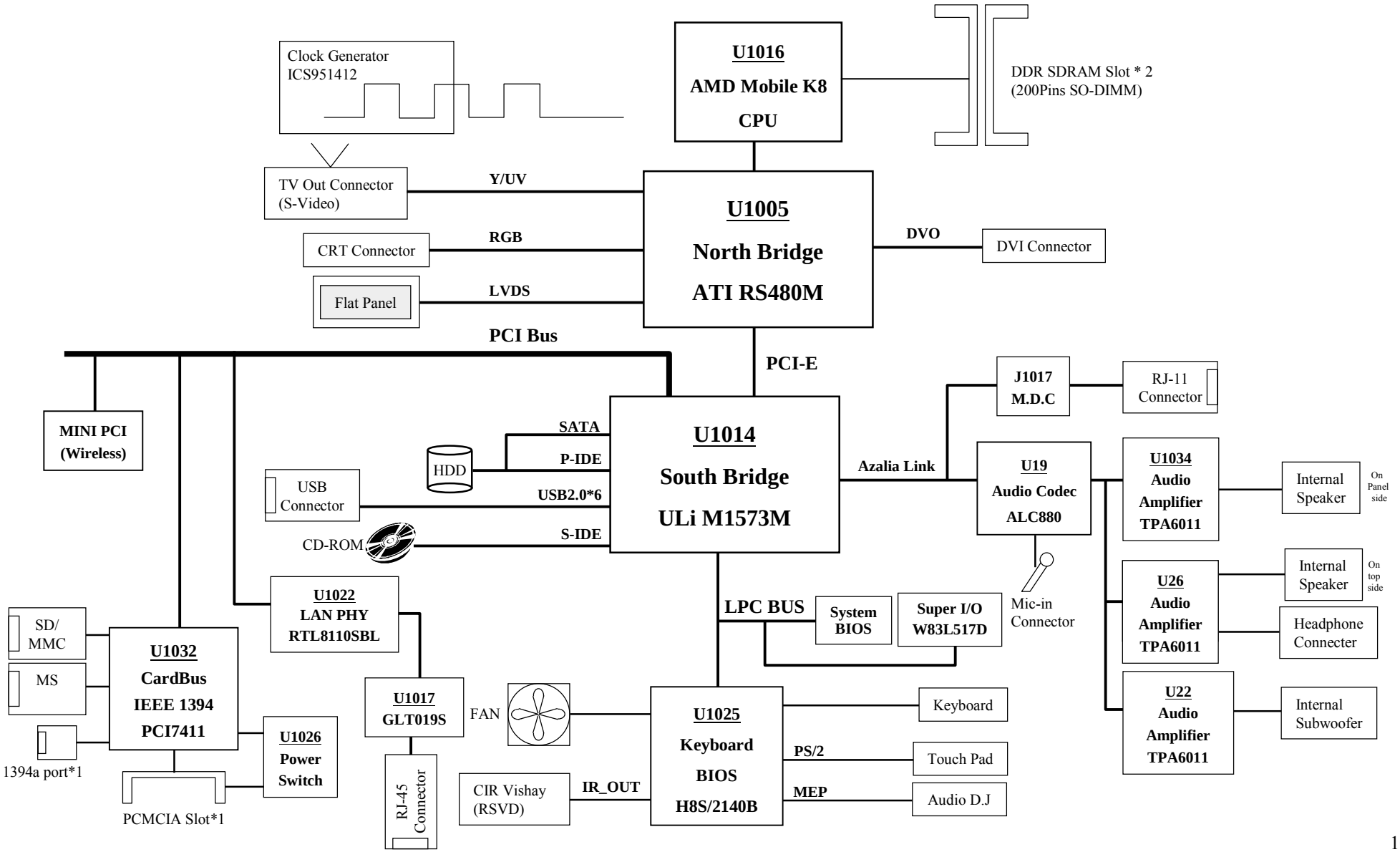
5.3 ULI M1573 South Bridge(9)

USB Interface

Pin Name	I/O Type	Description
USBCLK	I	**48 MHz USB Clock Input.** This clock will send to USB state machine to generate USB signals.
USBOVR#[7:6], USBOVR#[5:0]/ RSMGPI[9:4]	I	**Over Current Detect for USB Host Controller[7:0].** These pins are used to monitor the USB Power Over Current status. USBOVR#[5:0] can be configured as RSMGPI.
USB_DN0, USB_DP0	I/O	**Universal Serial Bus Port 0.** These are the serial data pair for USB Port 0.
USB_DN1, USB_DP	I/O	**Universal Serial Bus Port 1.** These are the serial data pair for USB Port 1.
USB_DN2, USB_DP2	I/O	**Universal Serial Bus Port 2.** These are the serial data pair for USB Port 2.
USB_DN3, USB_DP3	I/O	**Universal Serial Bus Port 3.** These are the serial data pair for USB Port 3.
USB_DN4, USB_DP4	I/O	**Universal Serial Bus Port 4.** These are the serial data pair for USB Port 4.
USB_DN5, USB_DP5	I/O	**Universal Serial Bus Port 5.** These are the serial data pair for USB Port 5.
USB_DN6, USB_DP6	I/O	**Universal Serial Bus Port 6.** These are the serial data pair for USB Port 6.
USB_DN7, USB_DP7	I/O	**Universal Serial Bus Port 7.** These are the serial data pair for USB Port 7.
USB_RX_TERM	I	USB PHY Receiving Termination
USB_TX_CS	I	USB PHY Transmission Current Source

8317 N/B Maintenance

6. System Block Diagram



7. Maintenance Diagnostics

7.1 Introduction

Each time the computer is turned on, the system bios runs a series of internal checks on the hardware. This power-on self test (post) allows the computer to detect problems as early as the power-on stage. Error messages of post can alert you to the problems of your computer.

If an error is detected during these tests, you will see an error message displayed on the screen. If the error occurs before the display is initialized,then the screen cannot display the error message. Error codes or system beeps are used to identify a post error that occurs when the screen is not available.

The value for the diagnostic port (378H) is written at the beginning of the test. Therefore, if the test failed, the user can determine where the problem occurred by reading the last value written to port 378H by the Mini PCI debug board.

7.2 Error Codes(1)

Following is a list of error codes in sequent display on the MINI PCI debug card.

Code	POST Routine Description
10h	Some type of lone reset
11h	Turn off FAST A20 for POST
12h	Signal power on reset
13h	Initialize the chipset
14h	Search for ISA Bus VGA adapter
15h	Reset counter / Timer 1
16h	User register config through CMOS
17h	Size memory
18h	Dispatch to RAM test
19h	Check sum the ROM
1Ah	Reset PIC's
1Bh	Initialize video adapter(s)
1Ch	Initialize video (6845Regs)
1Dh	Initialize color adapter
1Eh	Initialize monochrome adapter
1Fh	Test 8237A page registers

Code	POST Routine Description
20h	Test keyboard
21h	Test keyboard controller
22h	Check if CMOS RAM valid
23h	Test battery fail & CMOS X-SUM
24h	Test the DMA controller
25h	Initialize 8237A controller
26h	Initialize int vectors
27h	RAM quick sizing
28h	Protected mode entered safely
29h	RAM test completed
2Ah	Protected mode exit successful
2Bh	Setup shadow
2Ch	Going to initialize video
2Dh	Search for monochrome adapter
2Eh	Search for color adapter
2Fh	Sign on messages displayed

7.2 Error Codes(2)

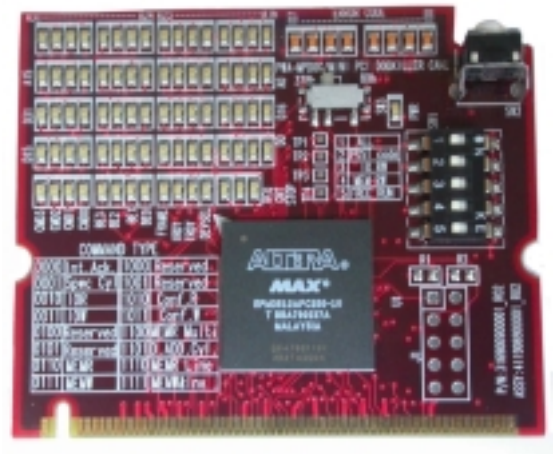
Following is a list of error codes in sequent display on the MINI PCI debug card.

Code	POST Routine Description
30h	Special init of keyboard ctlr
31h	Test if keyboard Present
32h	Test keyboard Interrupt
33h	Test keyboard command byte
34h	Test, blank and count all RAM
35h	Protected mode entered safely(2)
36h	RAM test complete
37h	Protected mode exit successful
38h	Update output port
39h	Setup cache controller
3Ah	Test if 18.2Hz periodic working
3Bh	Test for RTC ticking
3Ch	Initialize the hardware vectors
3Dh	Search and init the mouse
3Eh	Update NUMLOCK status
3Fh	Special init of COMM and LPT ports

Code	POST Routine Description
40h	Configure the COMM and LPT ports
41h	Initialize the floppies
42h	Initialize the hard disk
43h	Initialize option ROMs
44h	OEM's init of power management
45h	Update NUMLOCK status
46h	Test for coprocessor installed
47h	OEM functions before boot
48h	Dispatch to operate system boot
49h	Jump into bootstrap code
50h	ACPI init
51h	PM init & Geyserville CPU init
52h	USB HC init

7.3 Debug Tool

7.3.1 Diagnostic Tool for Mini PCI Slot :



P/N:411906900001
Description: PWA-MPDOG;MINI PCI DOGKELLER CARD
Note: Order it from MIC/TSSC

8. Trouble Shooting

- 8.1 No Power (*1)
- 8.2 No Display (*2)
- 8.3 VGA Controller Test Error LCD No Display
- 8.4 External Monitor No Display
- 8.5 Memory Test Error
- 8.6 Keyboard (K/B)/Touch-Pad (T/P) Test Error
- 8.7 Hard Disk Drive Test Error
- 8.8 CD-ROM Drive Test Error
- 8.9 USB Test Error
- 8.10 Audio Test Error
- 8.11 LAN Test Error
- 8.12 PC Card & Card Reader Socket Test Error
- 8.13 Mini-PCI Socket Test Error

8317 N/B Maintenance

*1: No Power Definition

Base on ACPI Spec. We define the no power as while we press the power button, the system can't leave S5 status or none the PG signal send out from power supply.

Judge condition:

- Check whether there are any voltage feedback control to turn off the power.
- Check whether no CPU power will cause system can't leave S5 status.

If there are not any diagram match these condition, we should stop analyzing the schematic in power supply sending out the PG signal. If yes, we should add the effected analysis into no power chapter.

*2: No Display Definition

Base on the digital IC three basic working conditions: working power, reset, Clock. We define the no display as while system leave S5 status but can't get into S0 status.

Judge condition:

- Check which power will cause no display.
- Check which reset signal will cause no display.
- Check which Clock signal will cause no display

Base on these three conditions to analyze the schematic and edit the no display chapter.

Keyword:

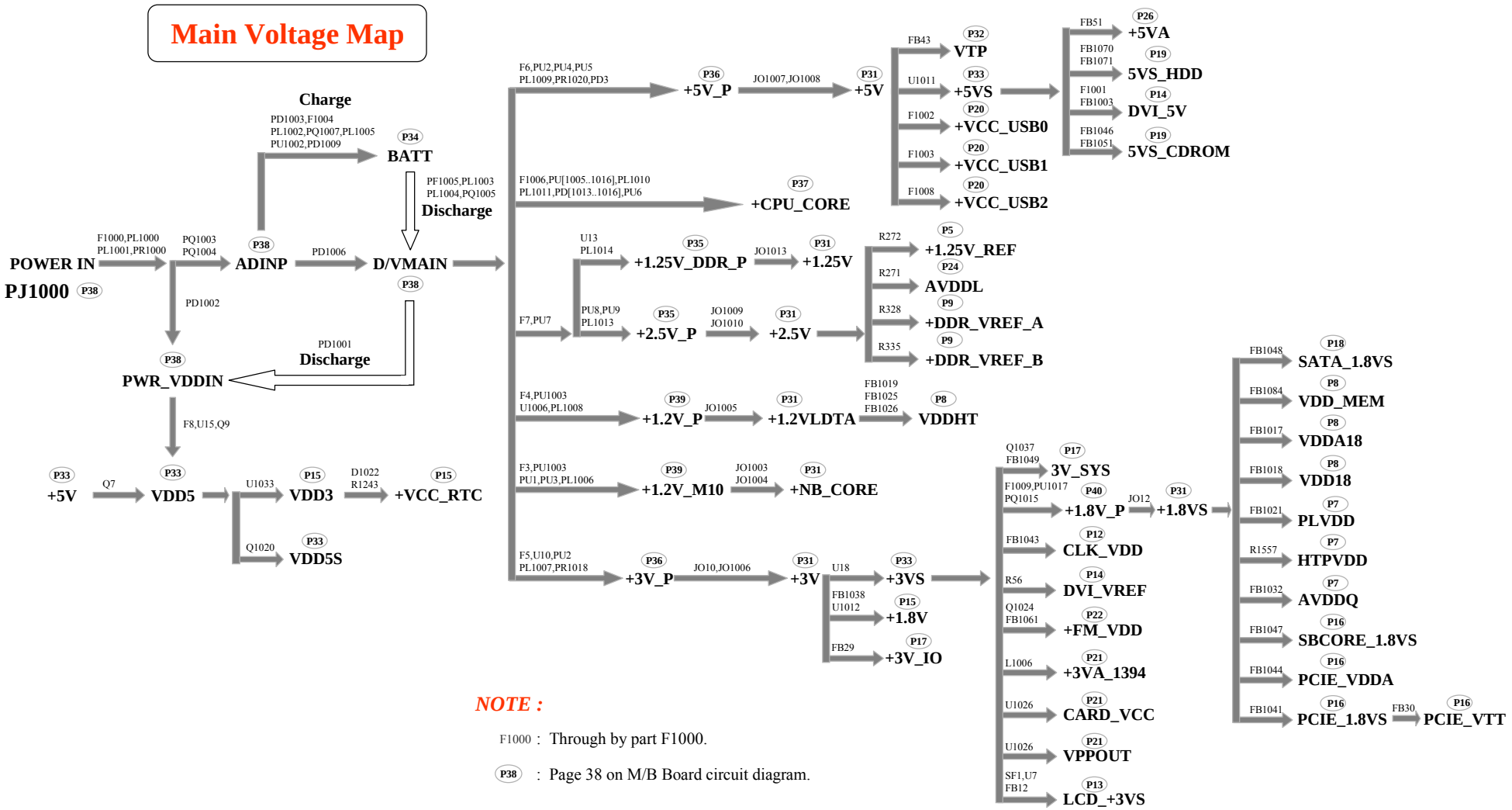
- S5: *Soft Off*
- S0: *Working*

For detail please refer the ACPI specification

8317 N/B Maintenance

8.1 No Power(1)

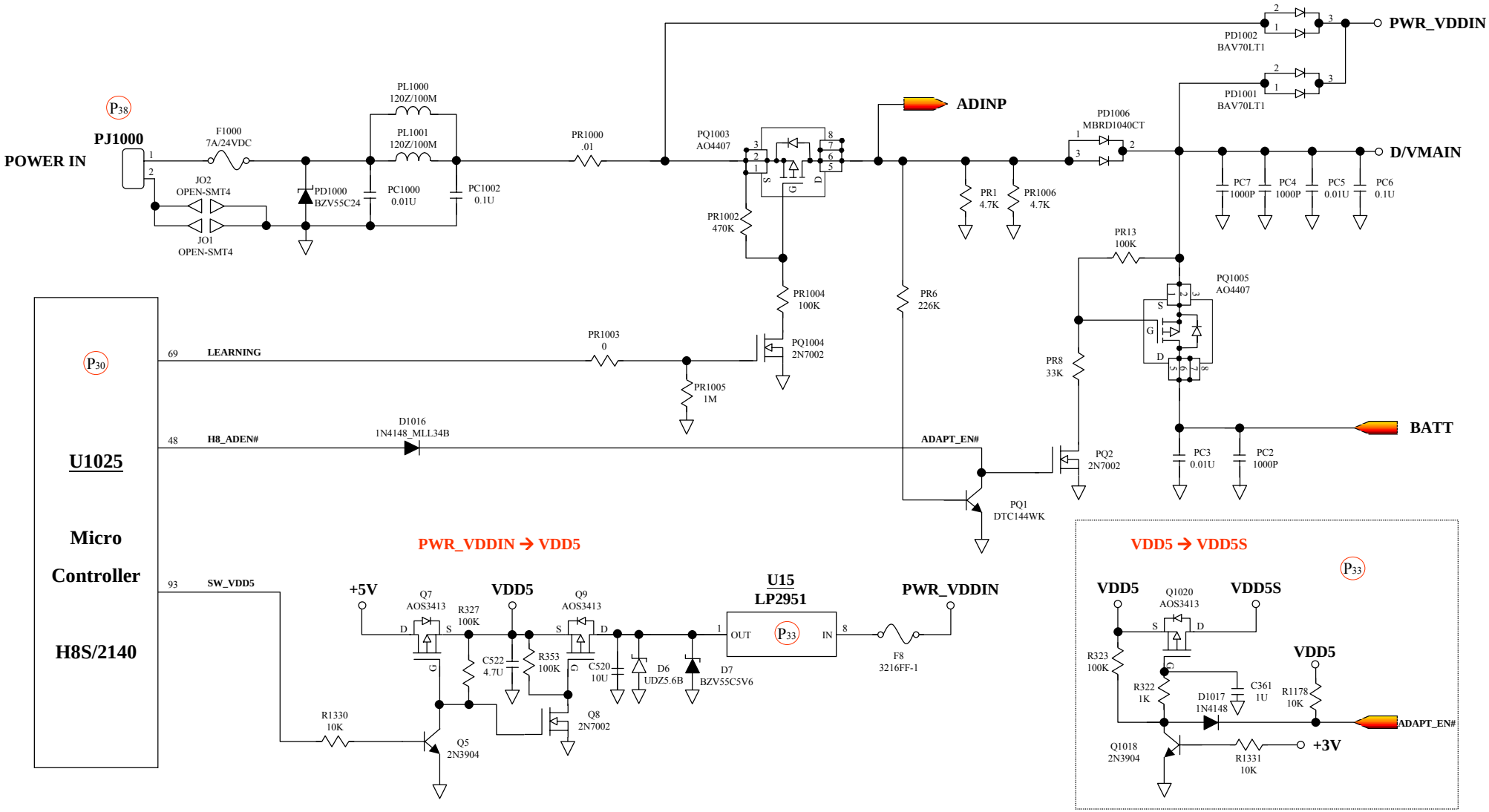
When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.



8317 N/B Maintenance

8.1 No Power(2)

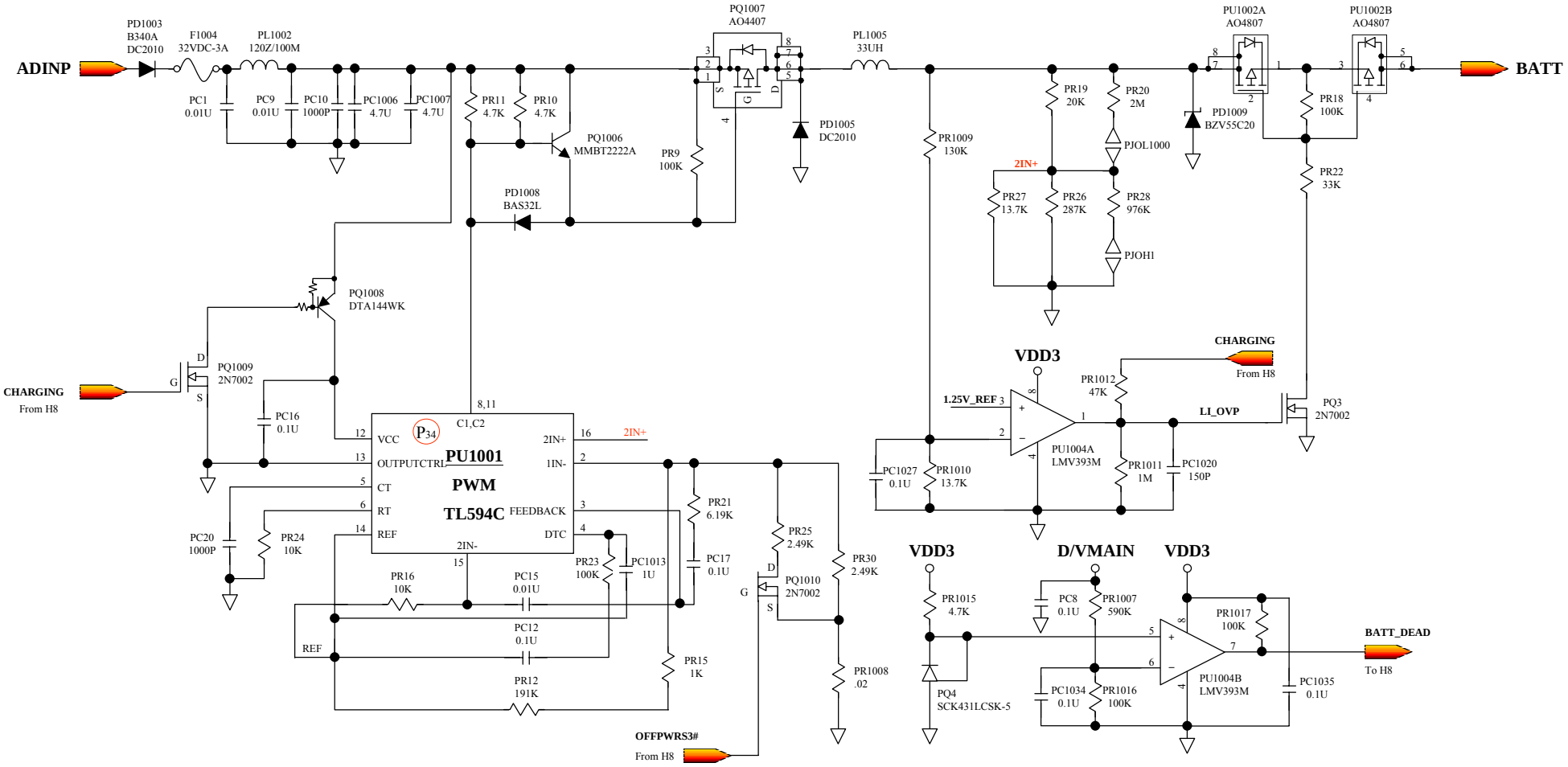
When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.



8317 N/B Maintenance

8.1 No Power(3)

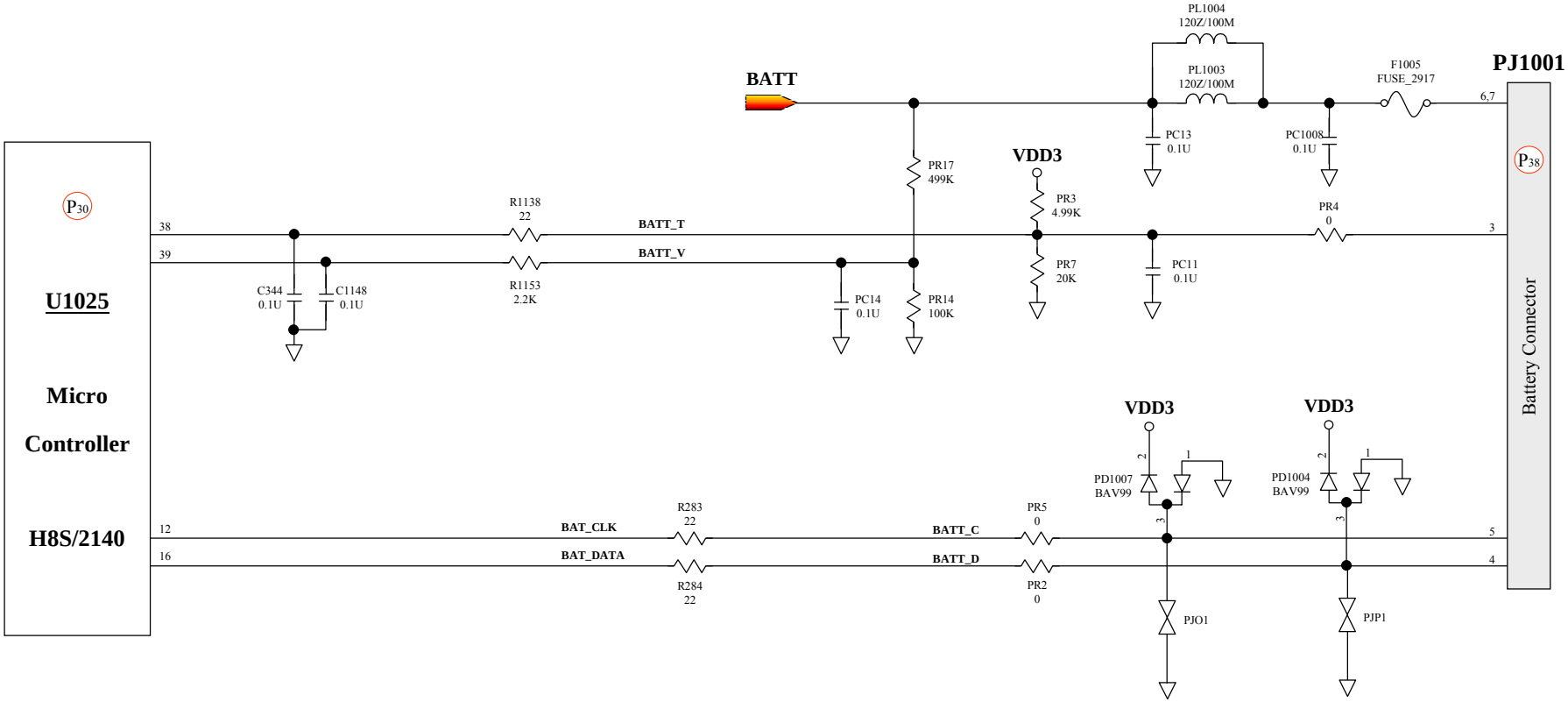
When the battery is installed but the battery status indicate LED display abnormal.



8317 N/B Maintenance

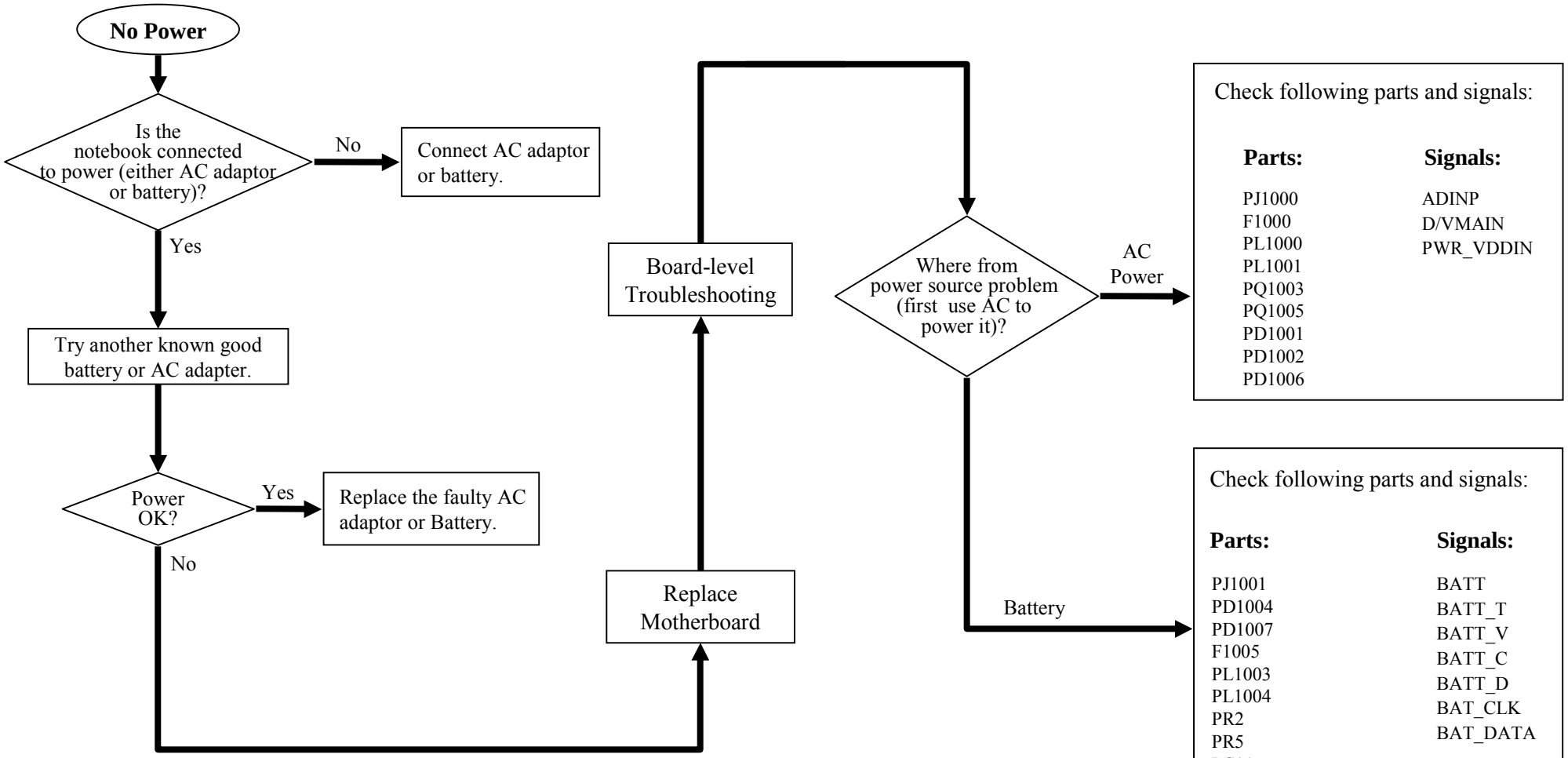
8.1 No Power(4)

When the battery is installed but the battery status indicate LED display abnormal.



8.1 No Power(5)

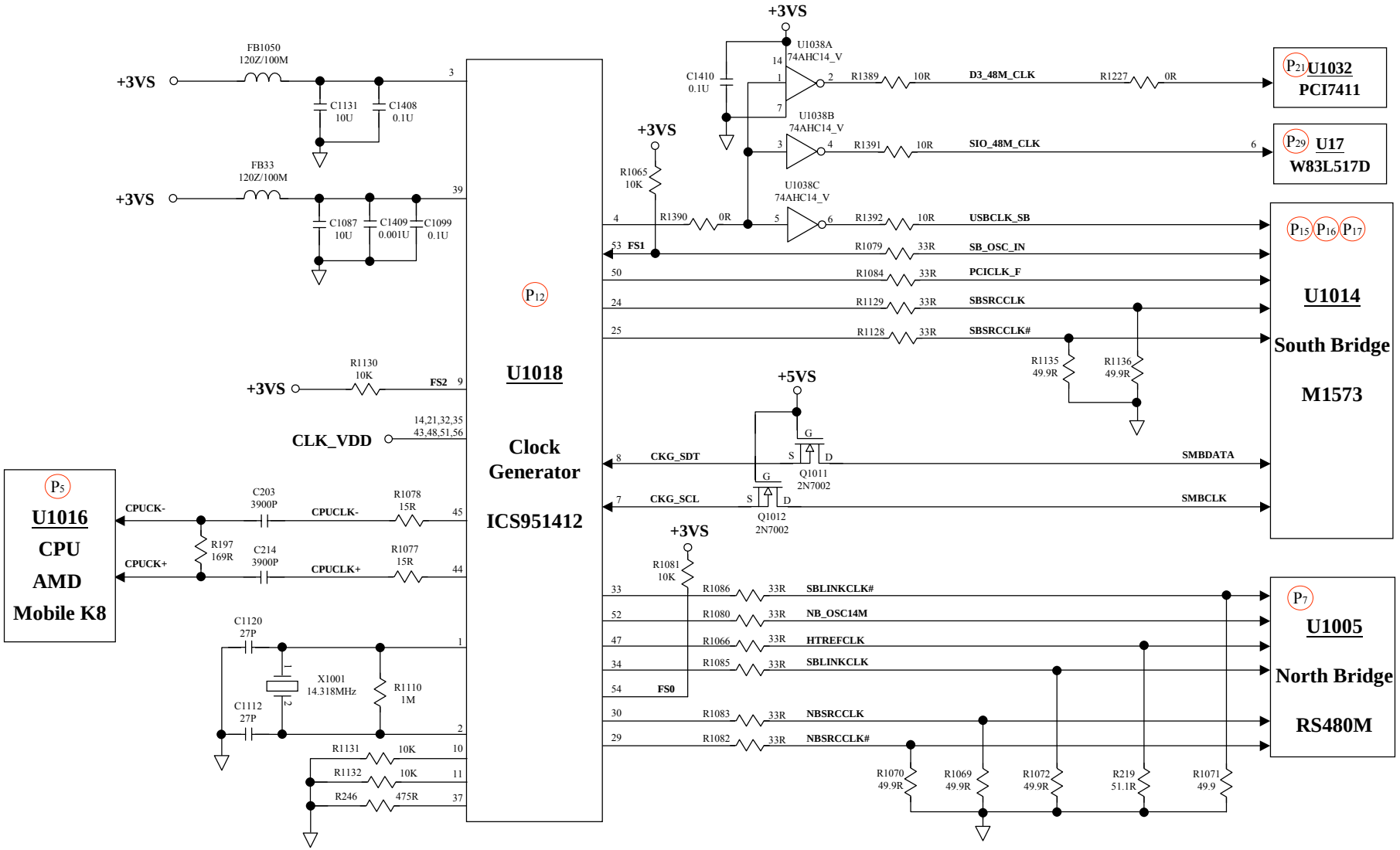
When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.



8317 N/B Maintenance

8.2 No Display(1)

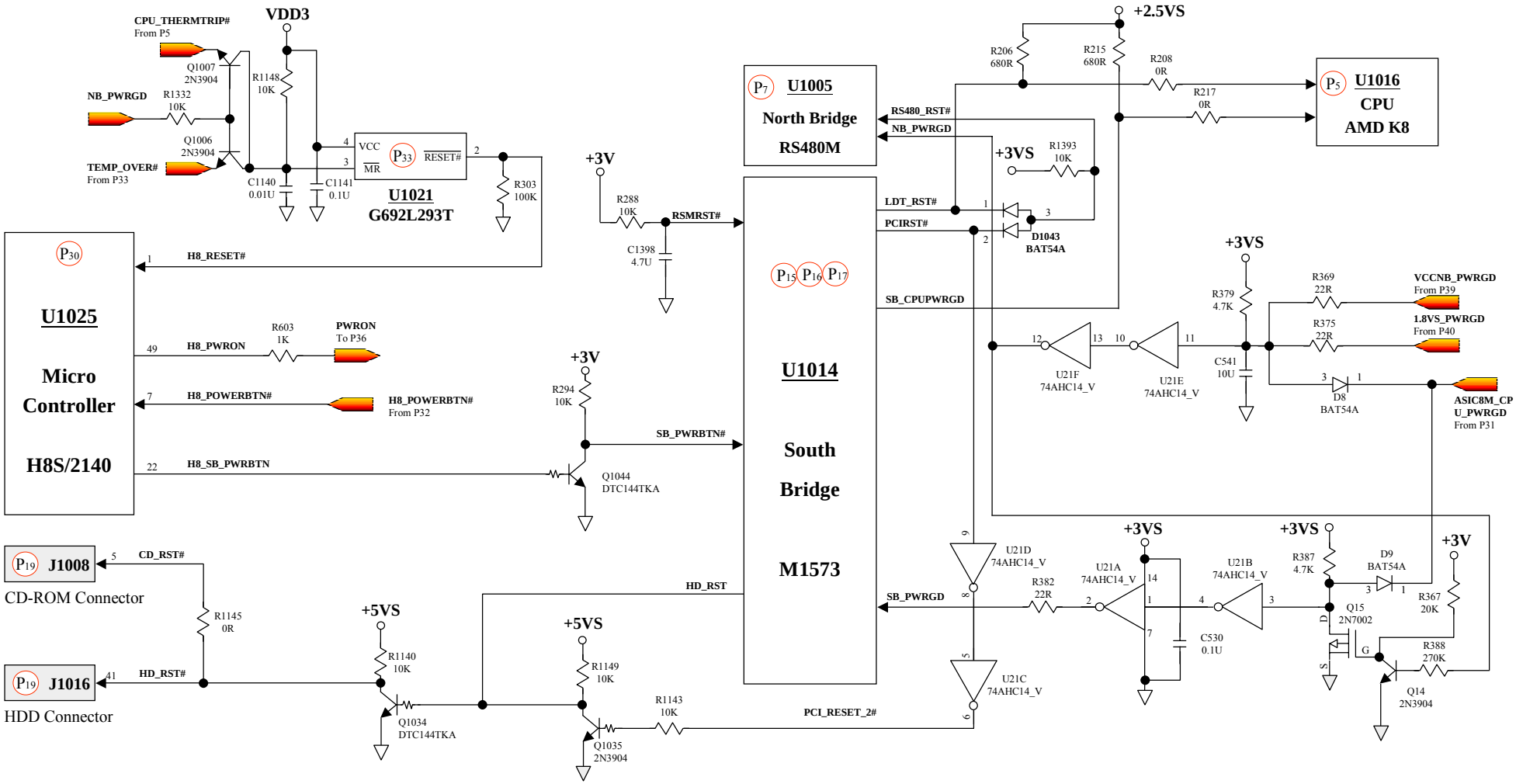
****** System Clock Check ******



8317 N/B Maintenance

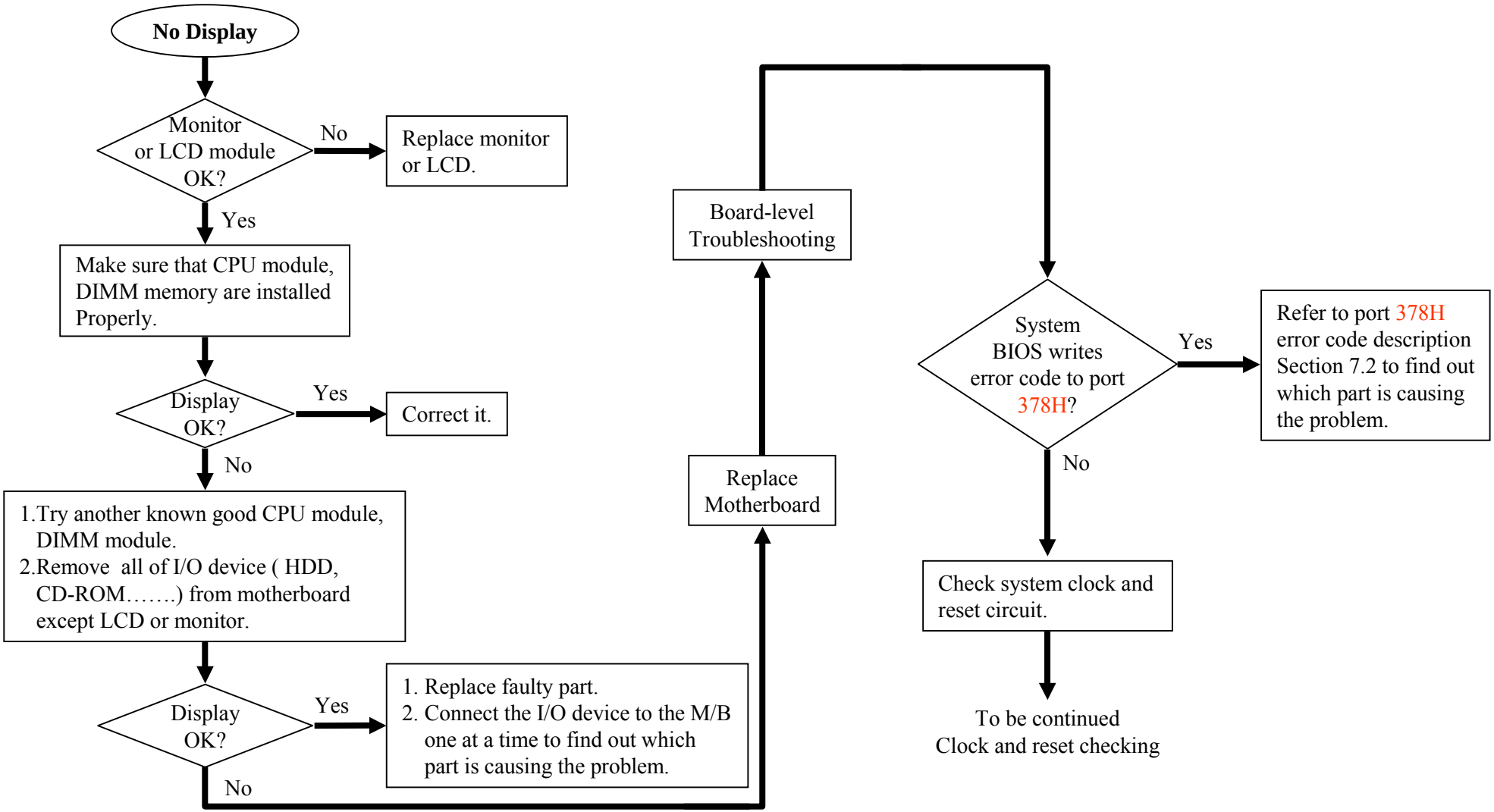
8.2 No Display(2)

****** Power Good & Reset Circuit Check ******



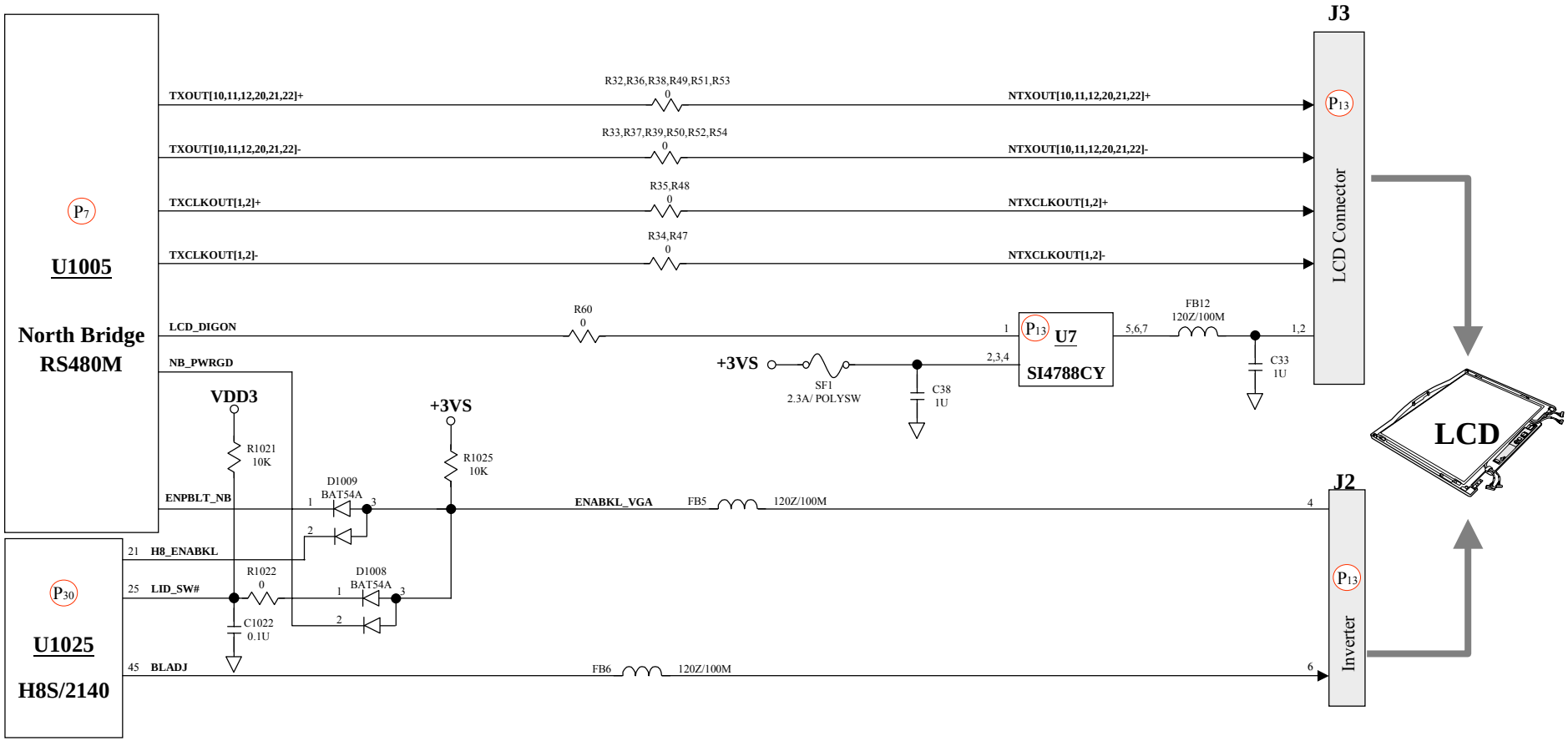
8.2 No Display(3)

There is no display on both LCD and VGA monitor after power on although the LCD and monitor is known-good.



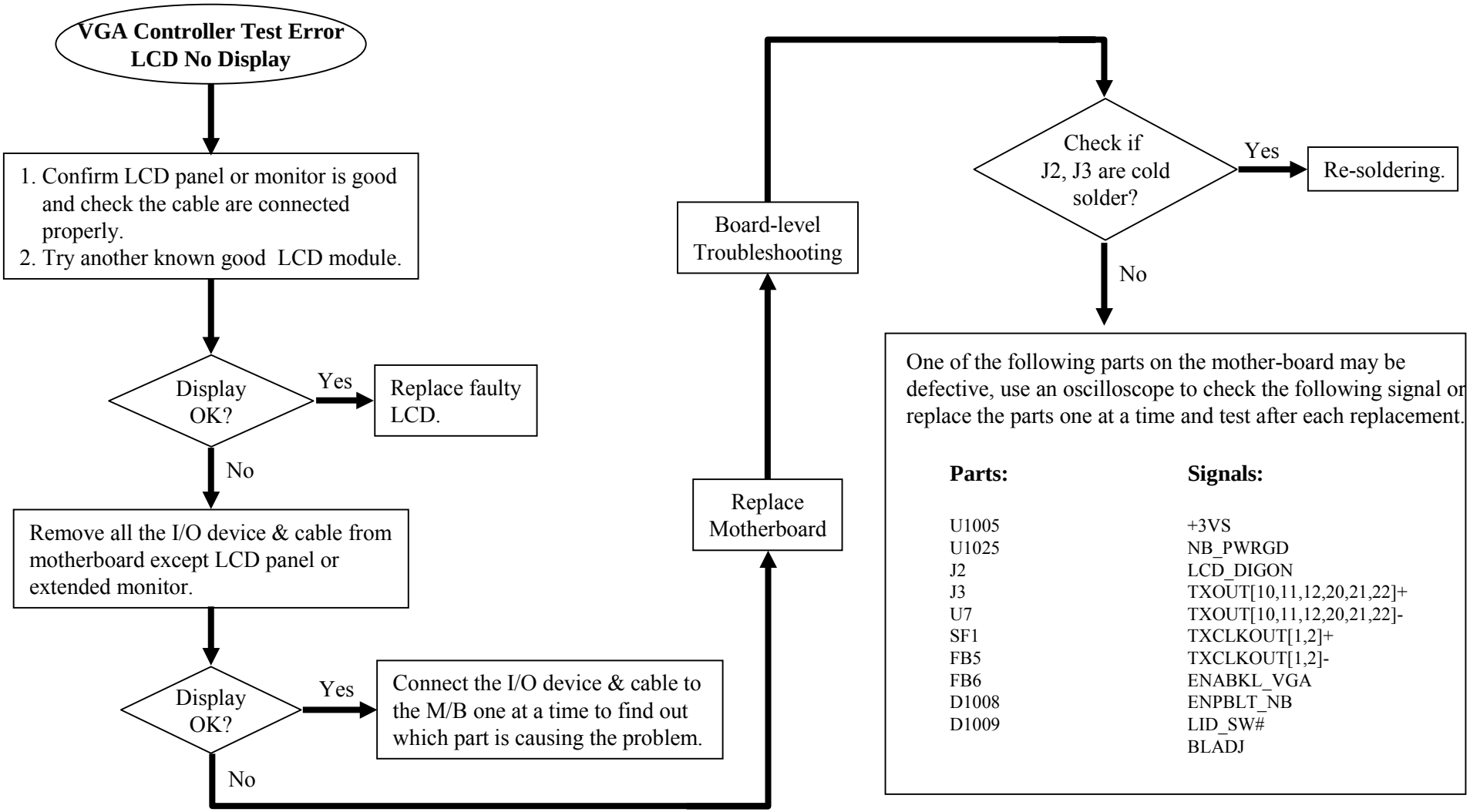
8.3 VGA Controller Test Error LCD No Display(1)

There is no display or picture abnormal on LCD although power-on-self-test is passed.



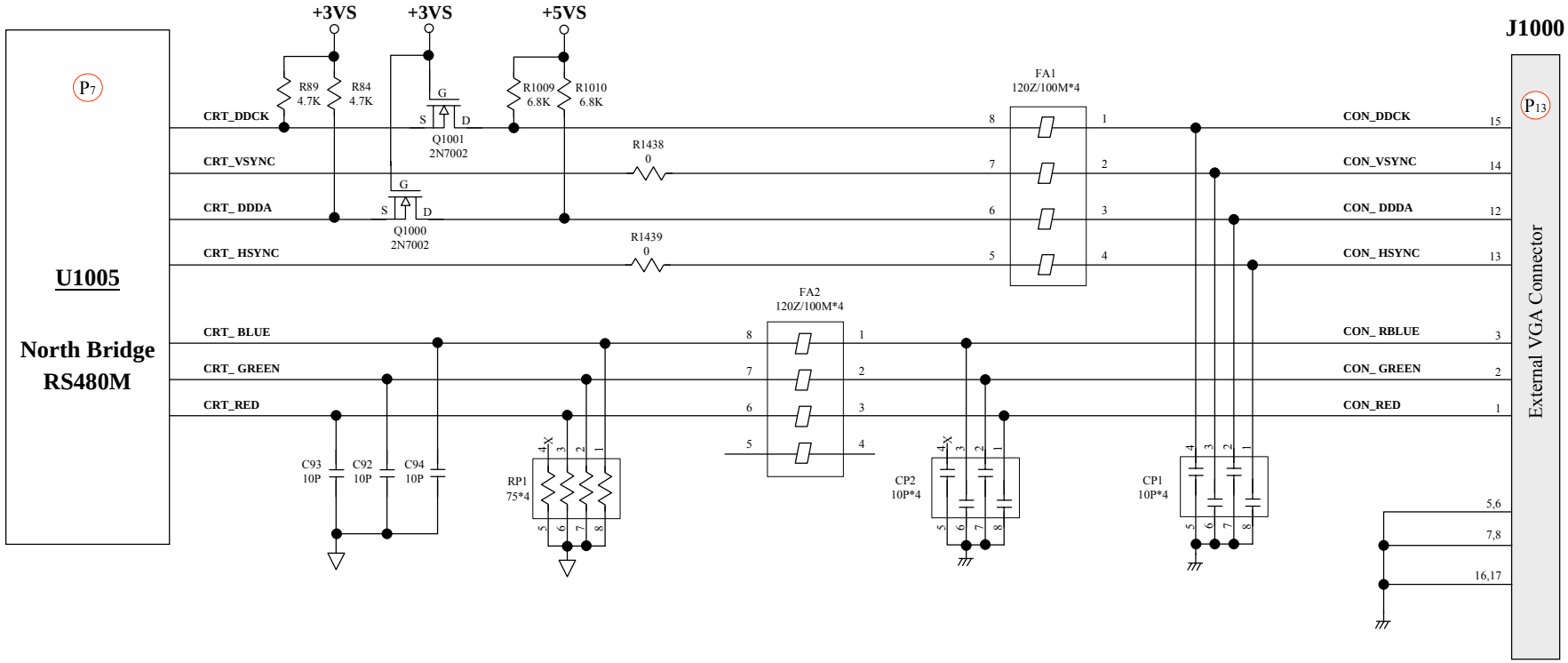
8.3 VGA Controller Test Error LCD No Display(2)

There is no display or picture abnormal on LCD although power-on-self-test is passed.



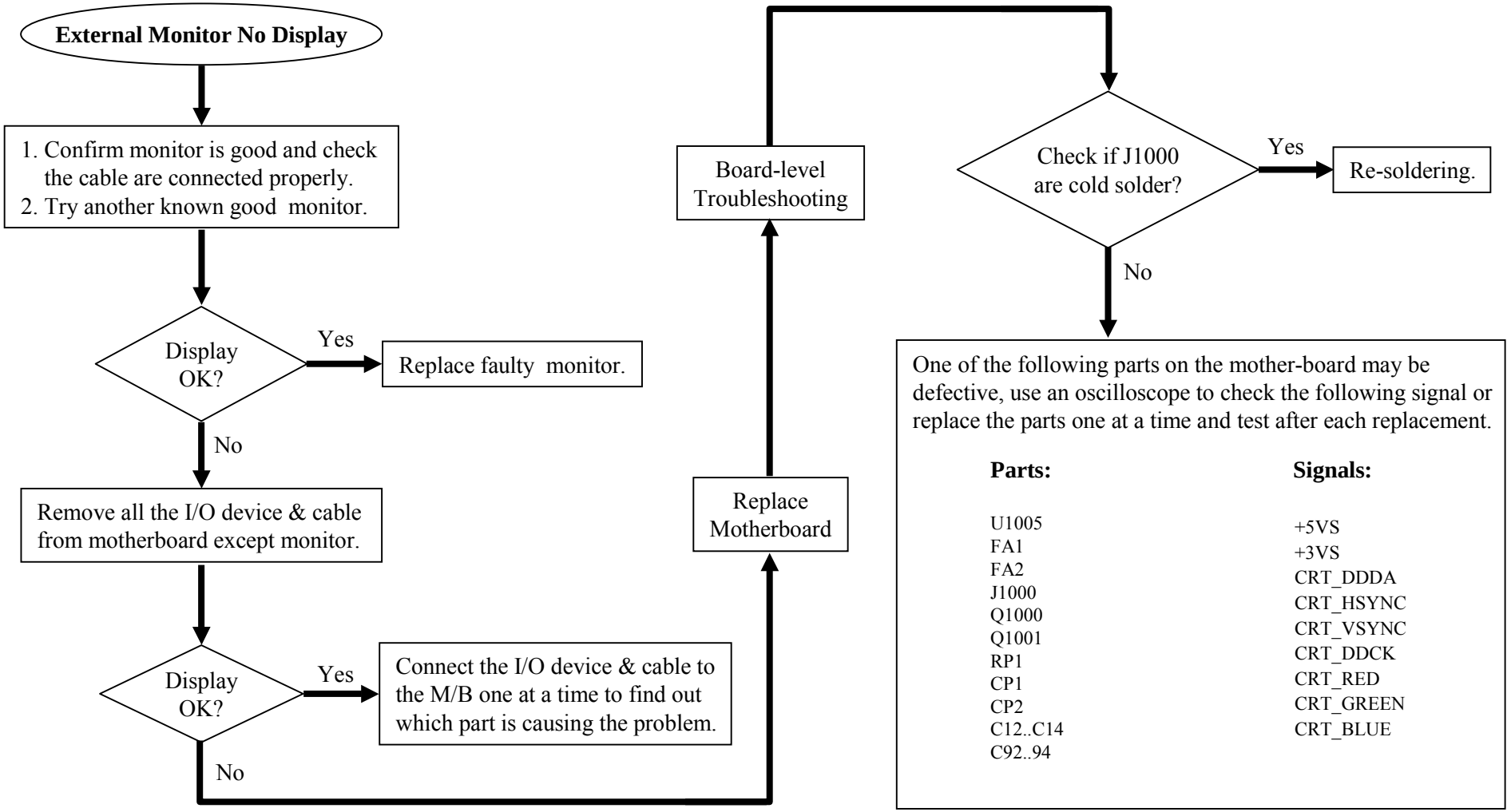
8.4 External Monitor No Display(1)

There is no display or picture abnormal on CRT monitor, but it is OK for LCD.



8.4 External Monitor No Display(2)

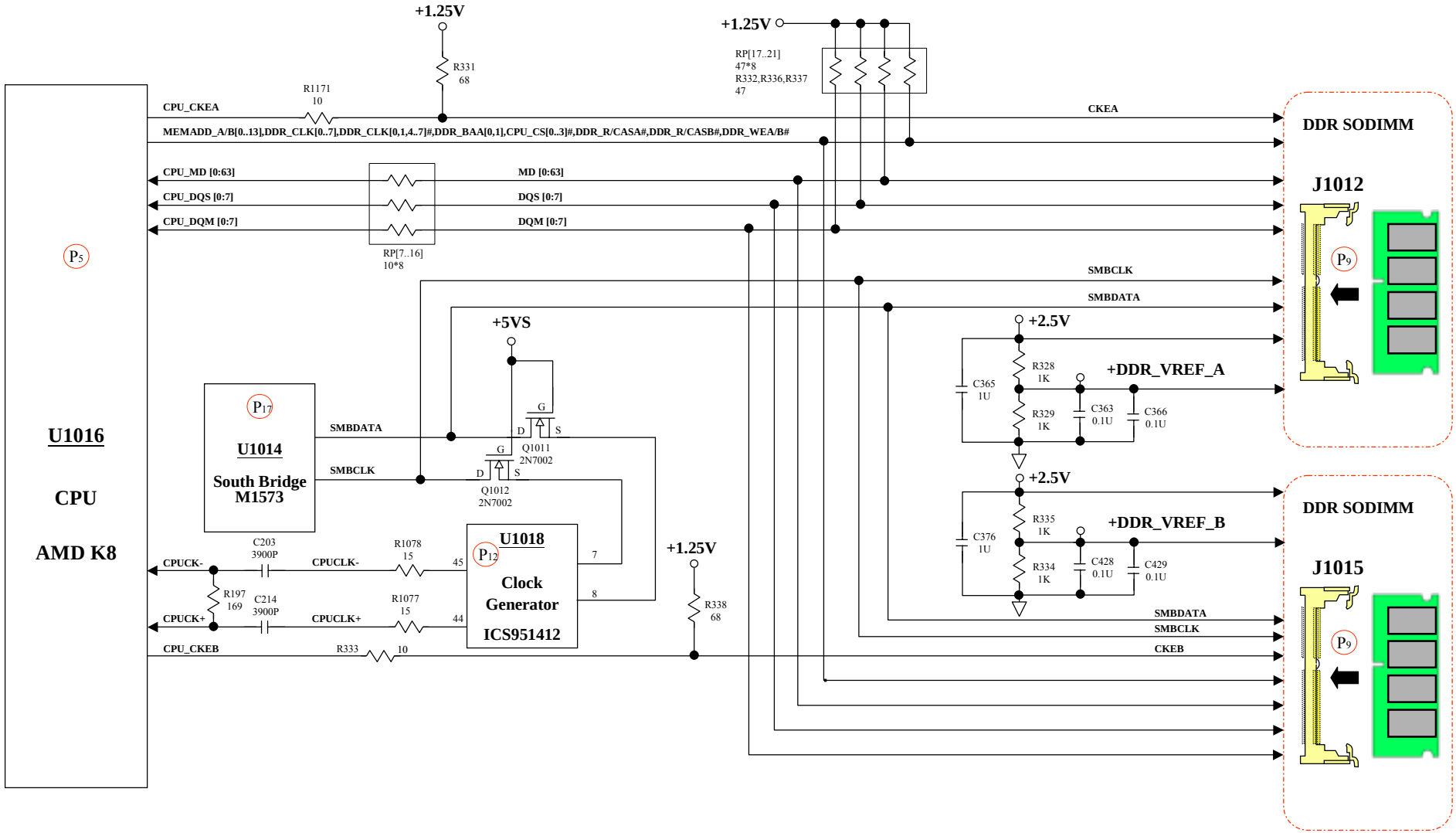
There is no display or picture abnormal on CRT monitor, but it is OK for LCD.



8317 N/B Maintenance

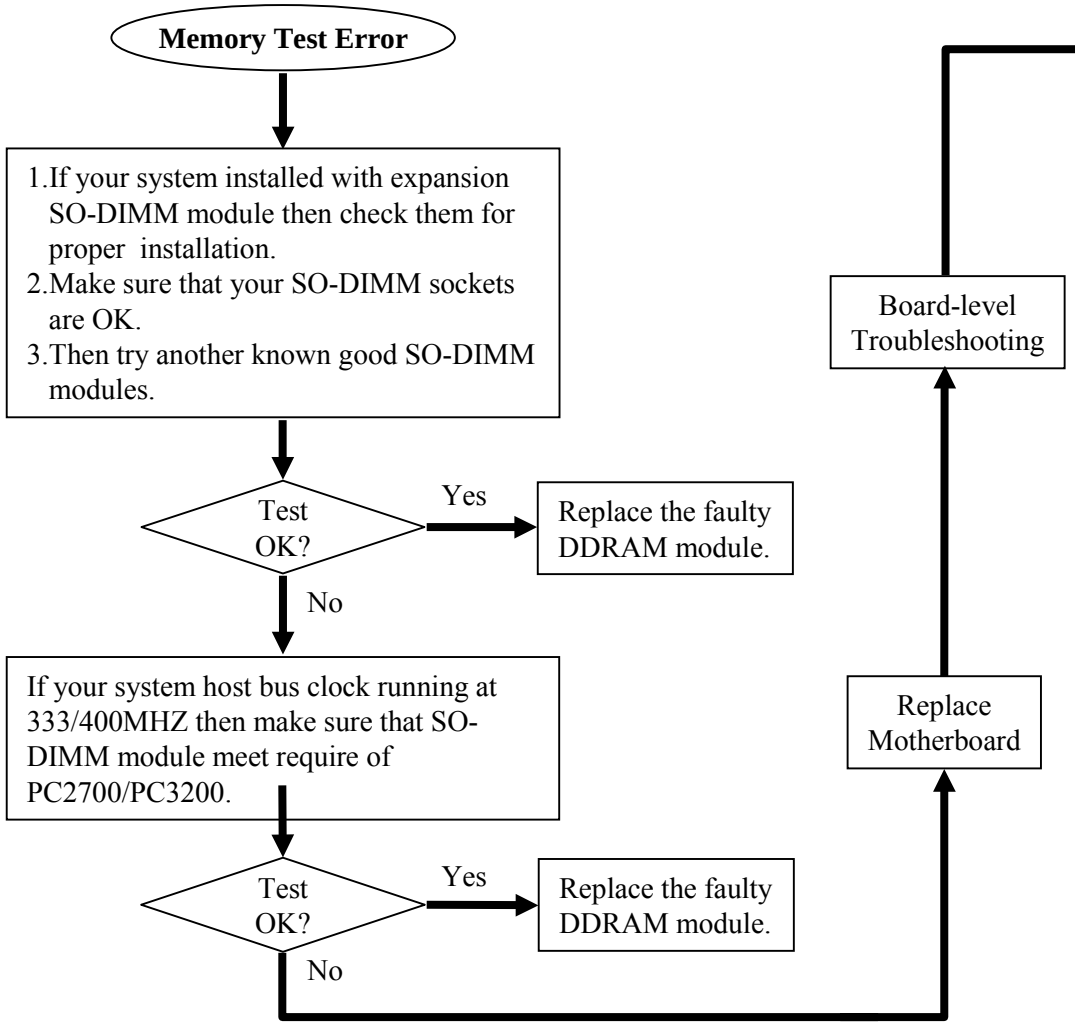
8.5 Memory Test Error(1)

Extend DDR SODIMM is Test Error or system hangs up.



8.5 Memory Test Error(2)

Extend DDRAM is Test Error or system hangs up.



One of the following components or signals on the motherboard may be defective ,Use an oscilloscope to check the signals or replace the parts one at A time and test after each replacement.

Parts:

U1016
U1018
U1014
Q1011
Q1012
RP[7..16]
RP[17..21]
R328
R329
C365
C376
R334
C363
C366
R335
C428
C429
J1012
J1015

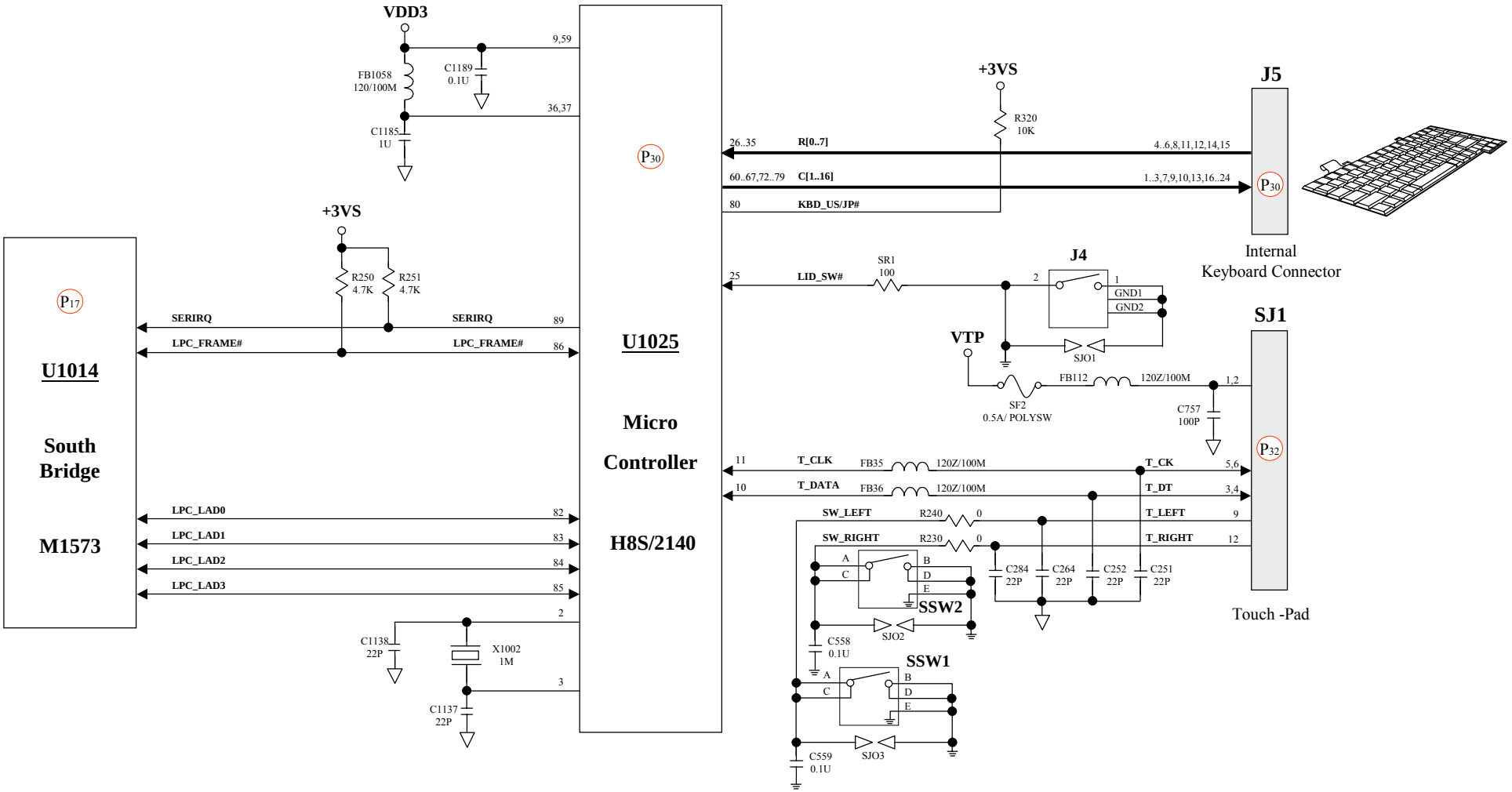
Signals:

+1.25V
+2.5V
+DDR_VREF_A/B
CKEA
CKEB
CPU_CS# [0..3]
CPU_MD [0..63]
CPU_DQS [0..7]
CPU_DQM [0..7]
DDR_RASA/B#
DDR_CASA/B#
DDR_WEA#
DDR_WEB#
DDR_CLK[0,1]#
DDR_CLK[4..7]#
SMBDATA
SMBCLK

8317 N/B Maintenance

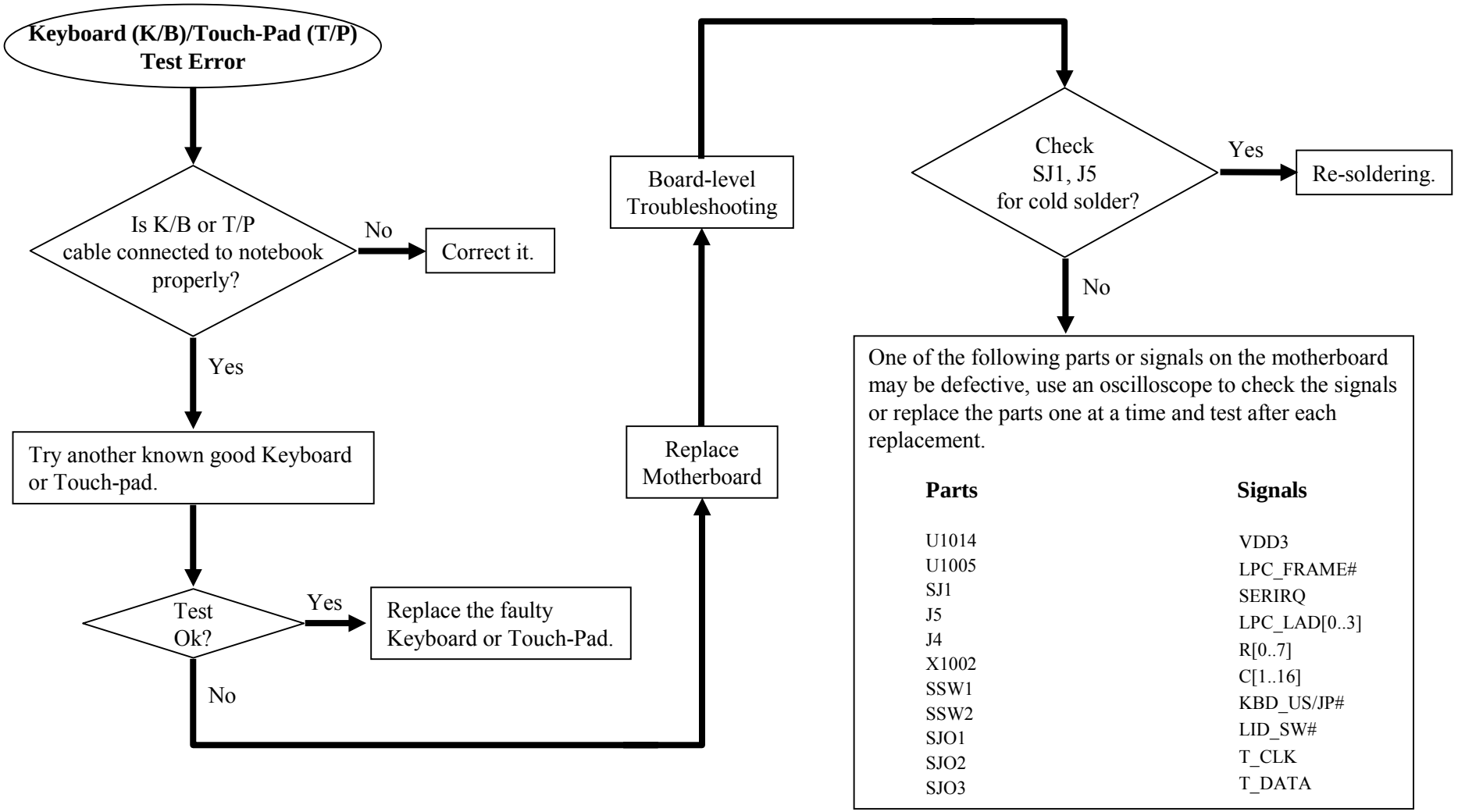
8.6 Keyboard (K/B)/Touch-Pad(T/P) Test Error(1)

Error message of keyboard or touch-pad Test Error is shown or any key does not work.



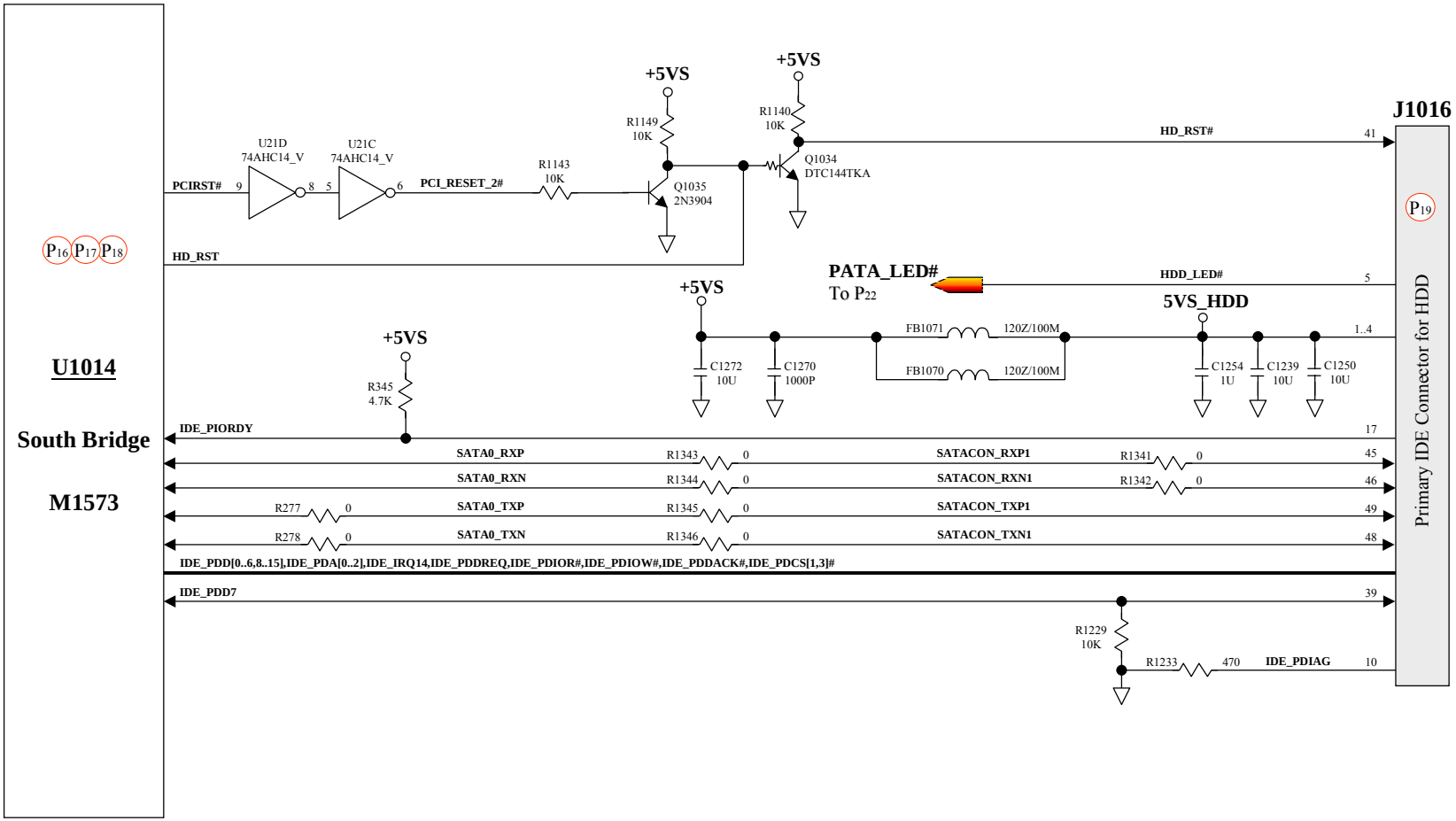
8.6 Keyboard (K/B)/Touch-Pad(T/P) Test Error(2)

Error message of keyboard or touch-pad Test Error is shown or any key does not work.



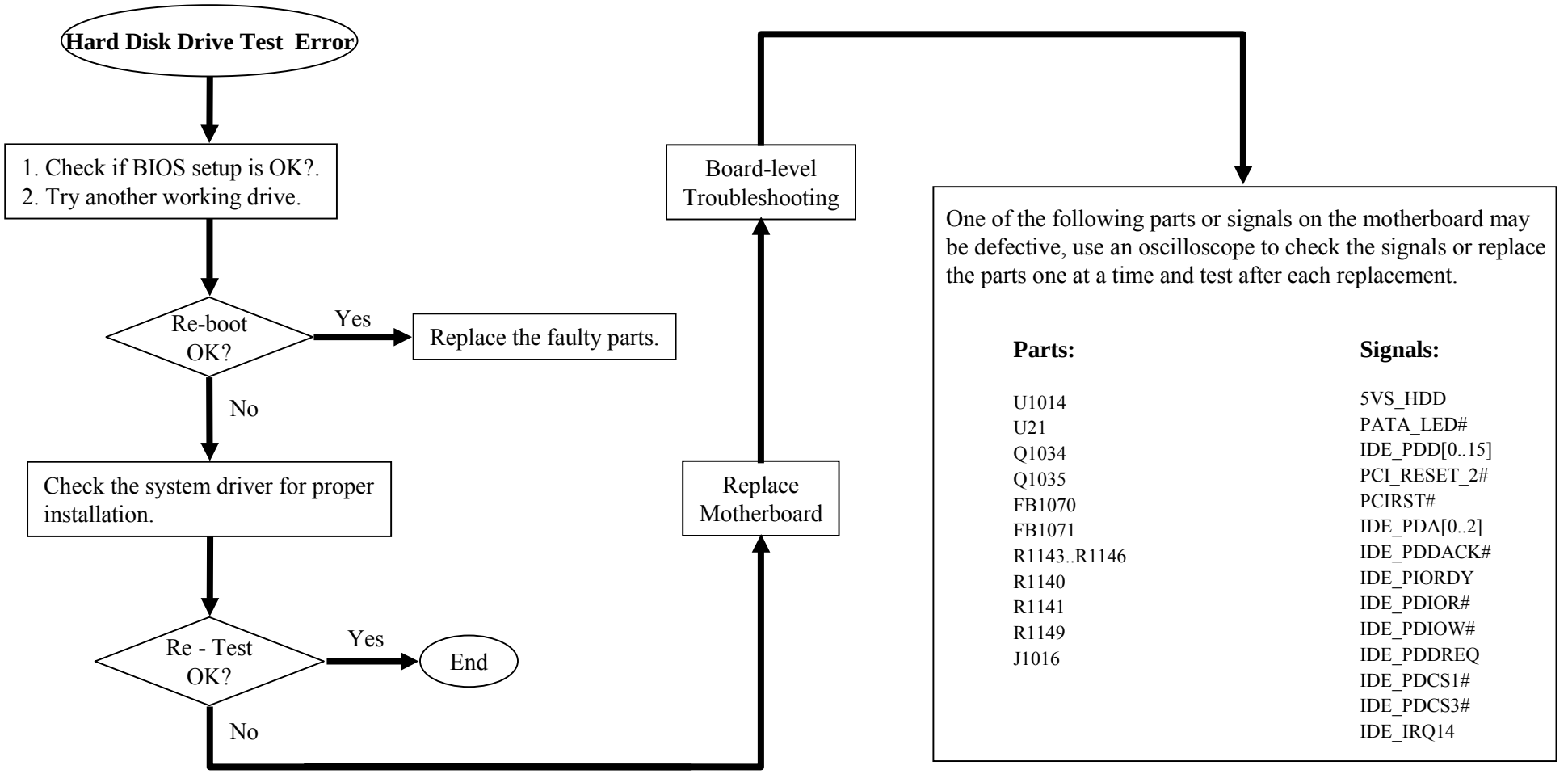
8.7 Hard Disk Drive Test Error(1)

Either an error message is shown, or the drive motor spins non-stop, while reading data from or writing data to hard disk.



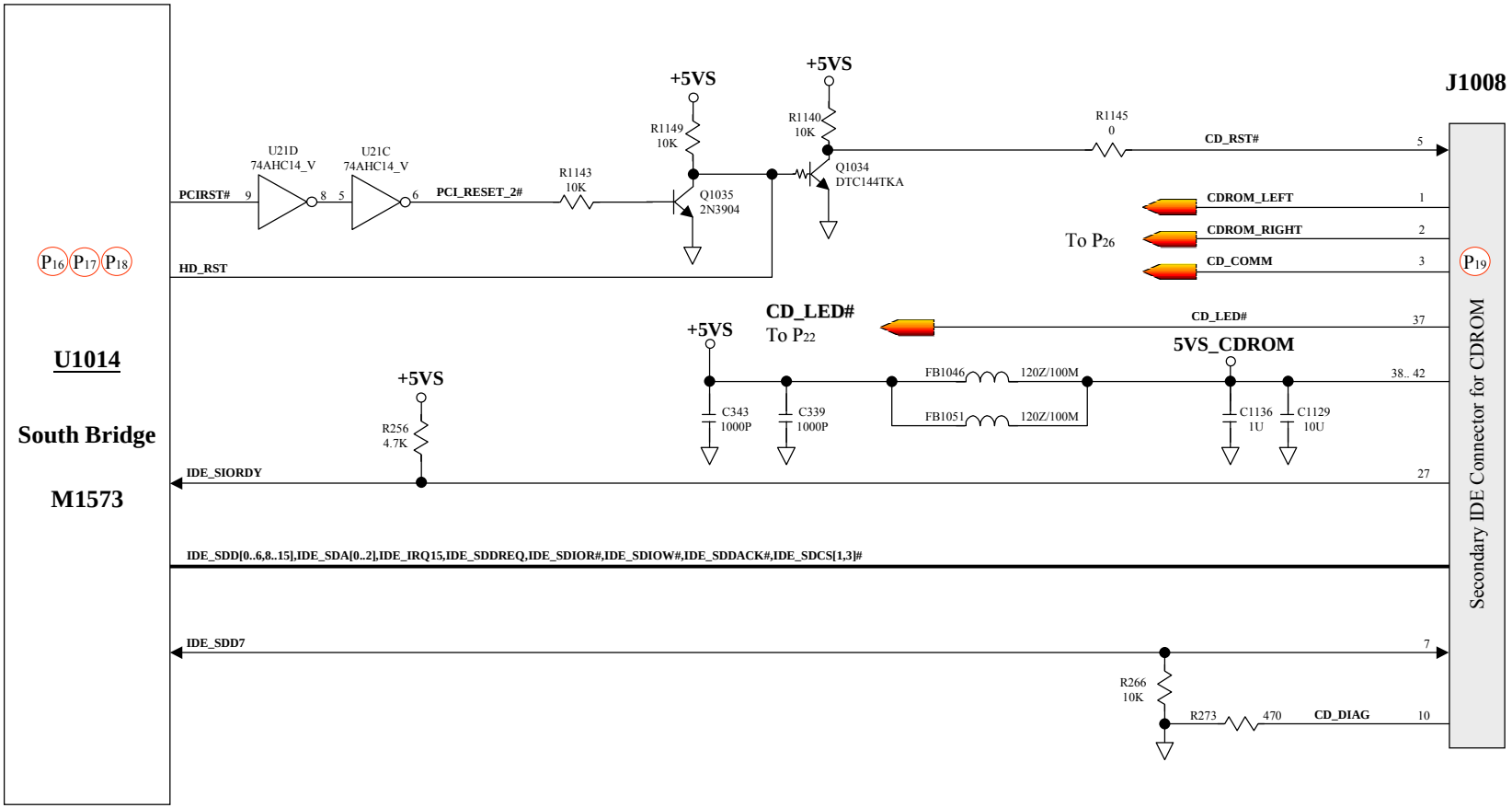
8.7 Hard Disk Drive Test Error(2)

Either an error message is shown, or the drive motor spins non-stop, while reading data from or writing data to hard disk.



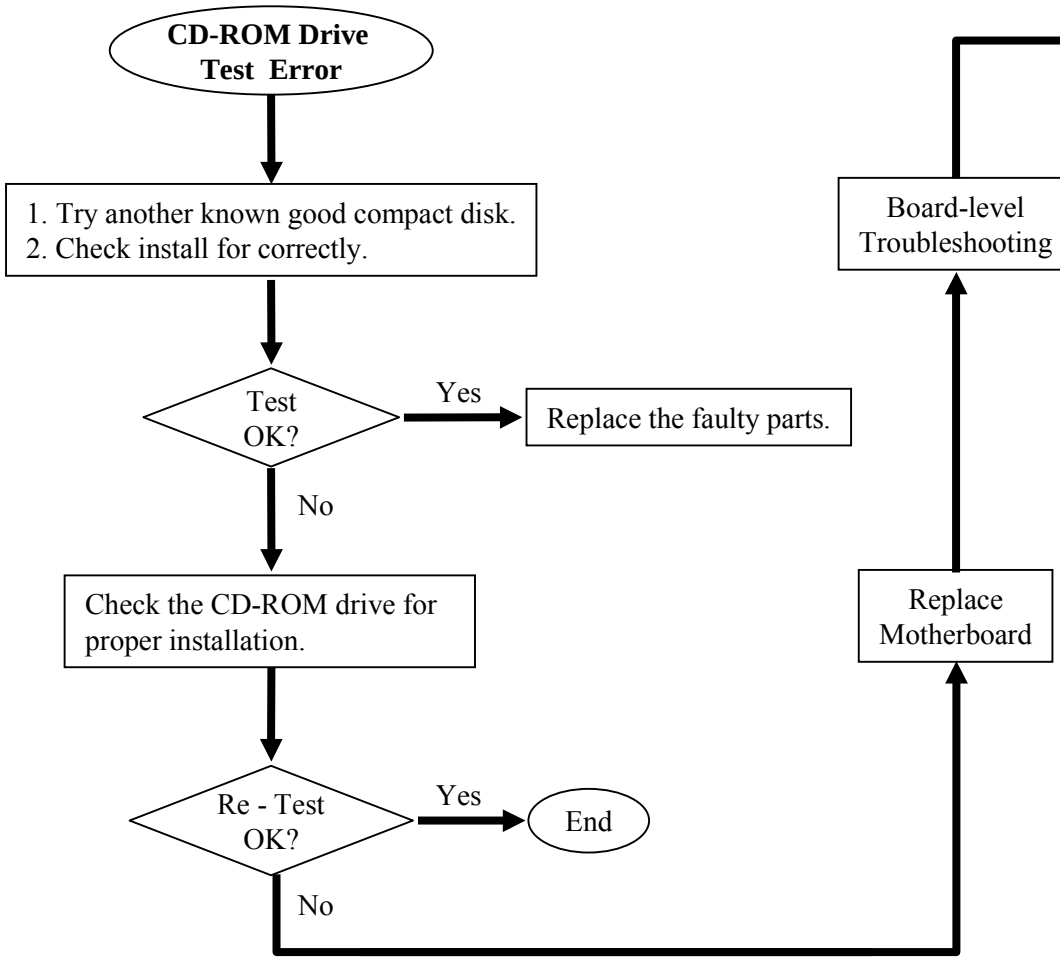
8.8 CD-ROM Drive Test Error(1)

An error message is shown when reading data from CD-ROM drive.



8.8 CD-ROM Drive Test Error(2)

An error message is shown when reading data from CD-ROM drive.

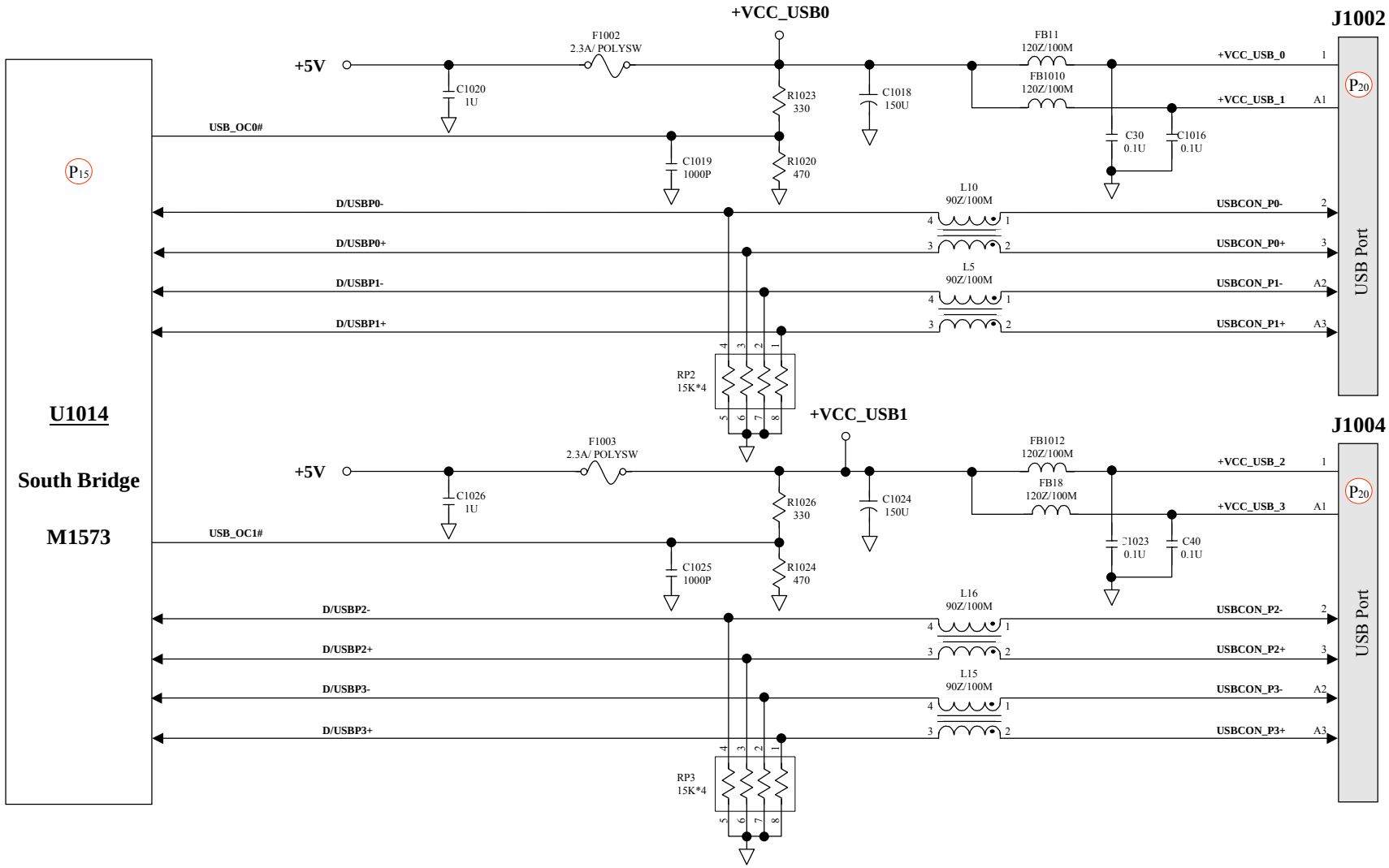


One of the following parts or signals on the motherboard may be defective, use an oscilloscope to check the signals or replace the parts one at a time and test after each replacement.

Parts:	**Signals:**
U1014	+5VS
U21	5VS_CDROM
Q1034	CD_LED#
Q1035	IDE_SDD[0..15]
J1008	CD_RST#
R1140	IDE_SDA[0..2]
R1145	IDE_IRQ15
R1149	IDE_SDDACK#
R256	IDE_SIORDY
R266	IDE_SDIOW#
R273	IDE_SDDREQ
FB1046	IDE_SDIOR#
FB1045	IDE_SDCS1#
	IDE_SDCS3#

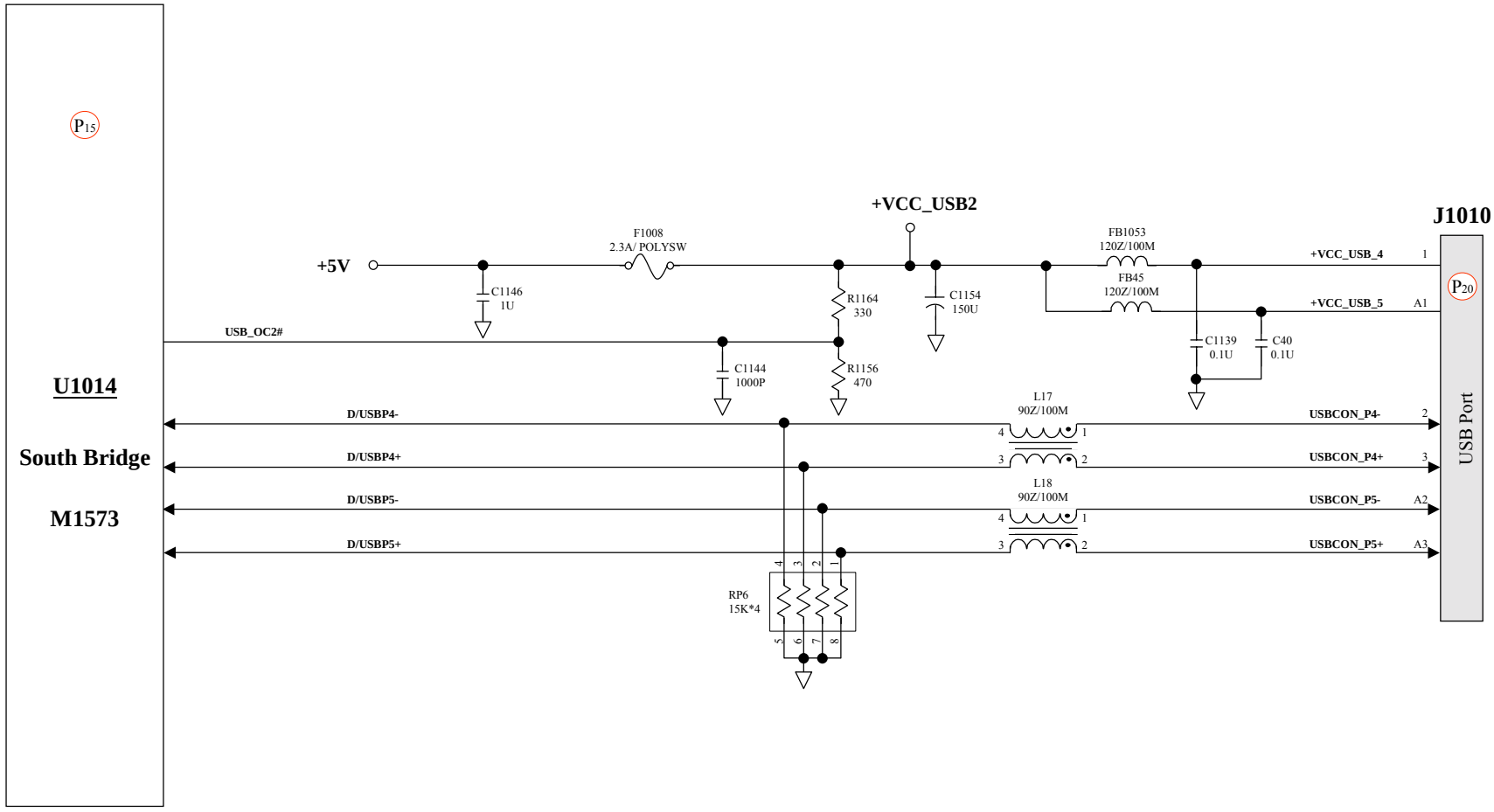
8.9 USB Test Error(1)

An error occurs when a USB I/O device is installed.



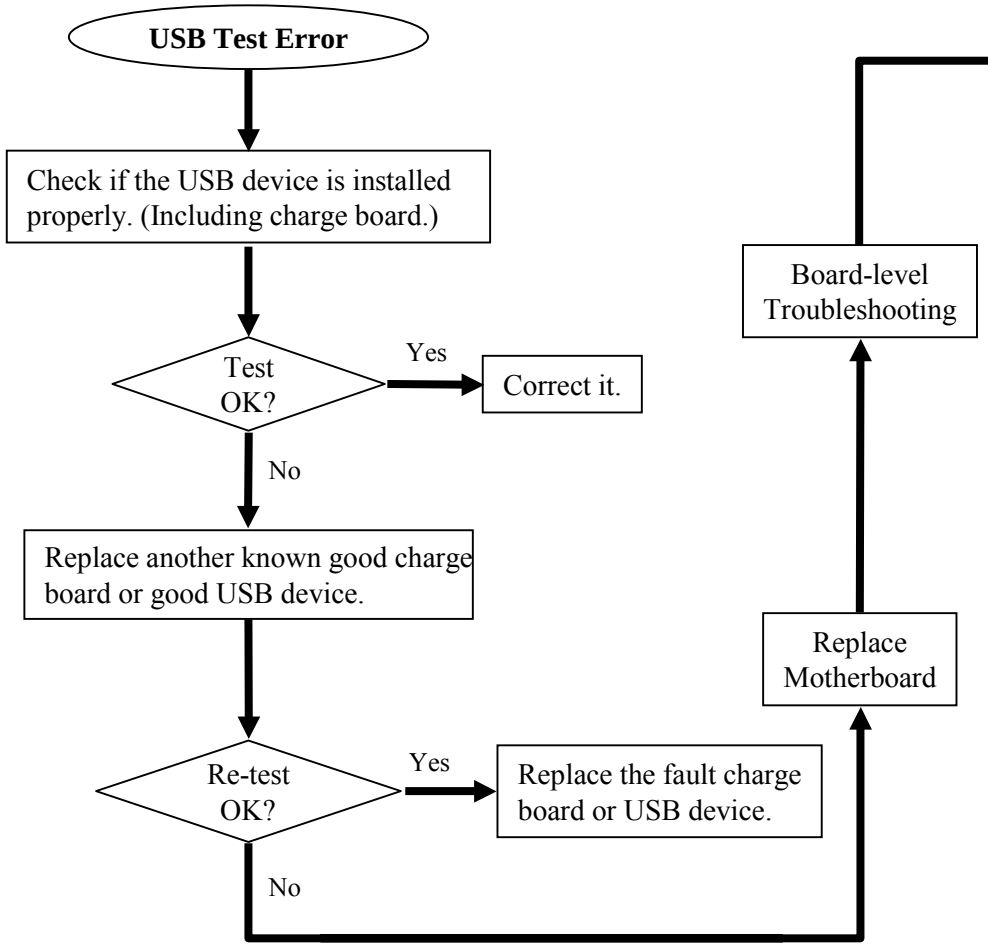
8.9 USB Test Error(2)

An error occurs when a USB I/O device is installed.



8.9 USB Test Error(3)

An error occurs when a USB I/O device is installed.



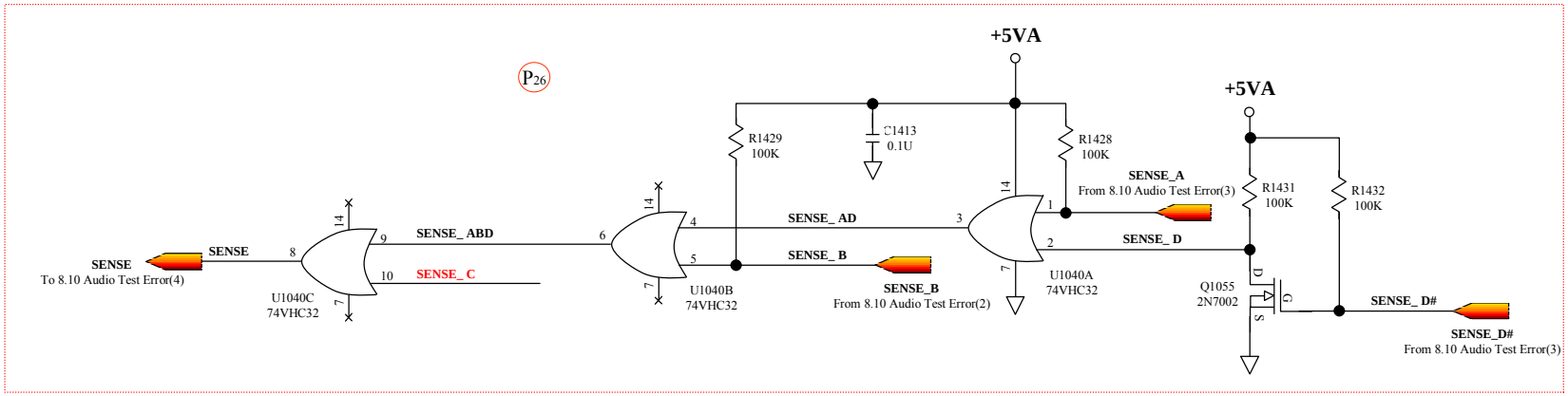
Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

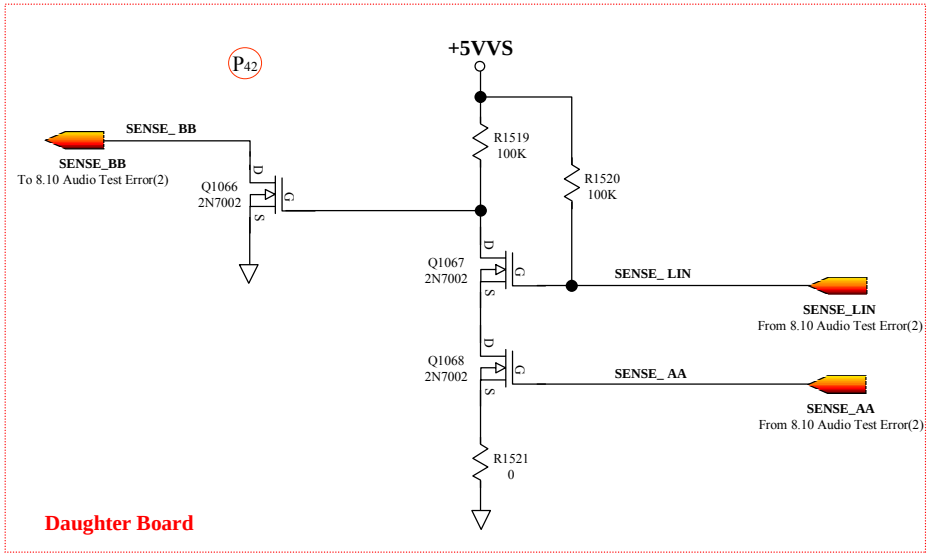
Parts:		**Signals:**
U1014	RP2	+5V
J1002	RP3	USBOC0#
J1004	RP9	D/USBP[0..5]+
J1010	L5	USBCON_P[0..5]+
FB10	L10	D/USBP [0:5] –
FB11	L15	USBCON_P[0..5]-
FB12	L16	USBOC1#
FB18	L17	USBOC2#
FB45	L18	
FB1053	C1018	
F1002	C1024	
F1003	C1154	
F1008		

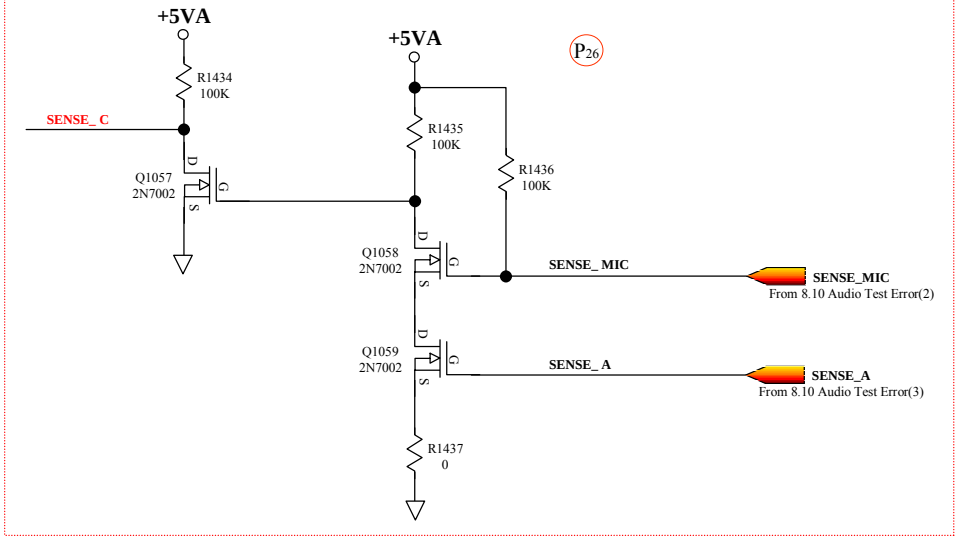
8317 N/B Maintenance

8.10 Audio Test Error(1)

No sound from speaker after audio driver is installed.

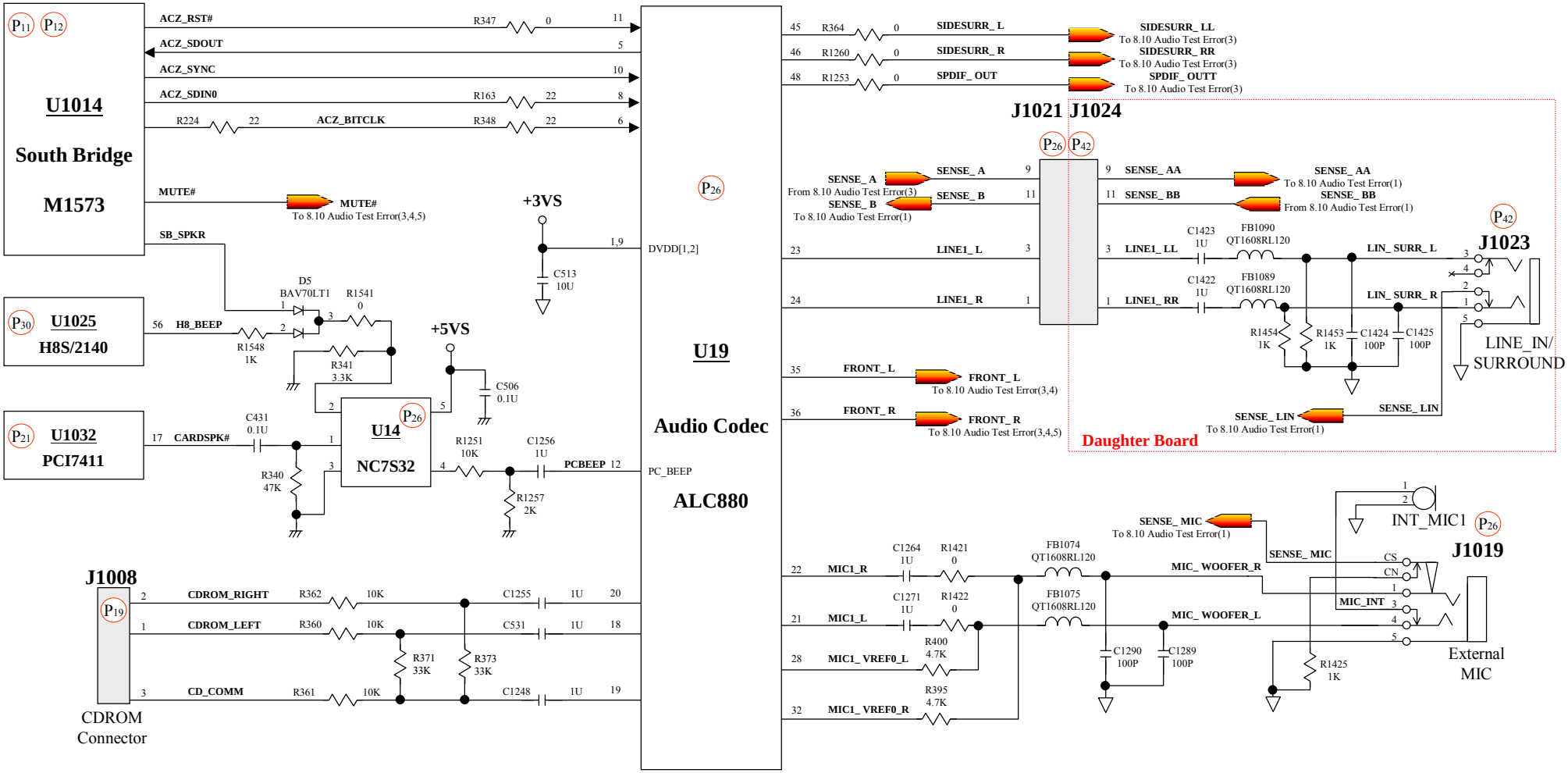






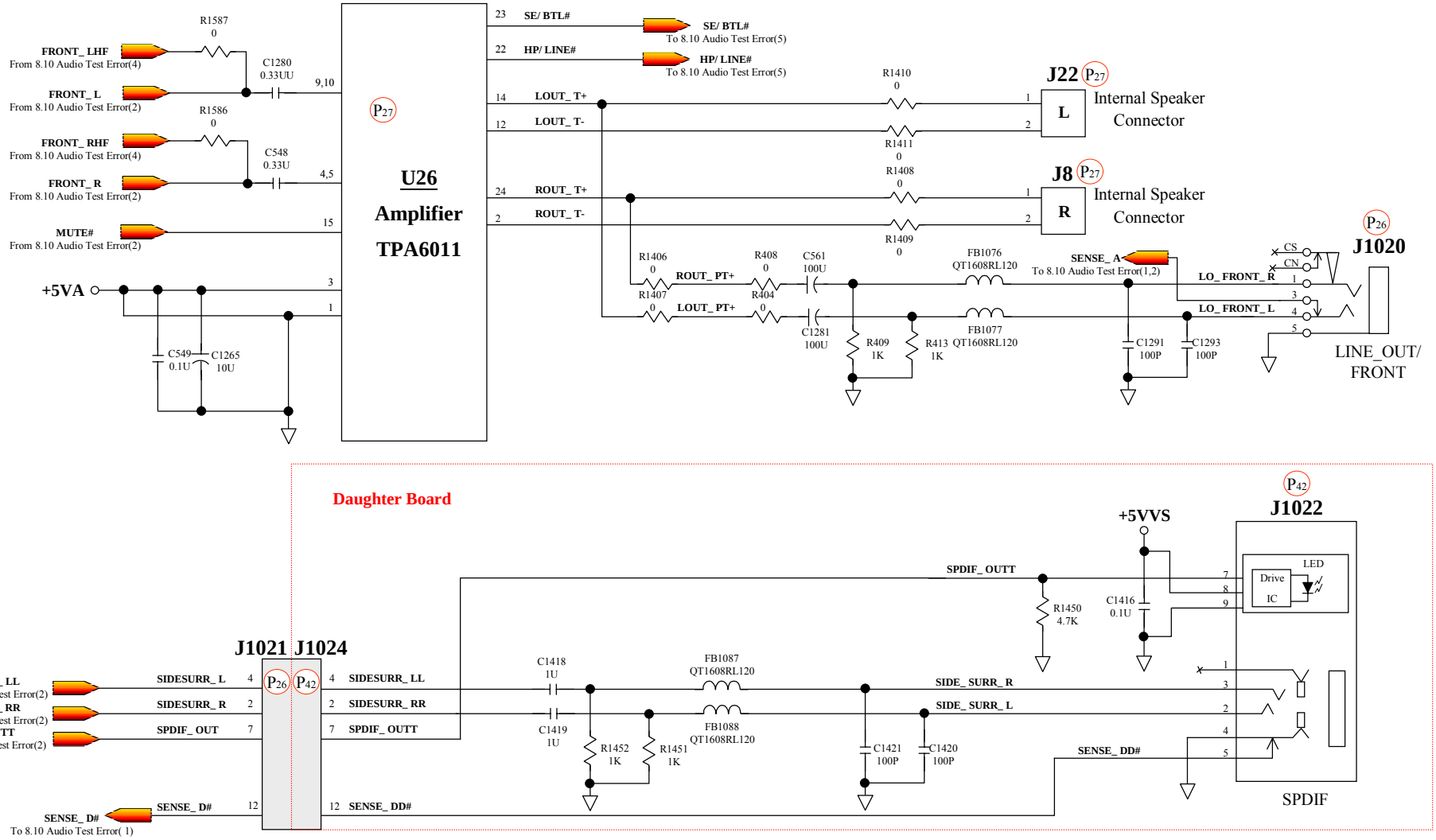
8.10 Audio Test Error(2) – Audio IN

No sound from speaker after audio driver is installed.



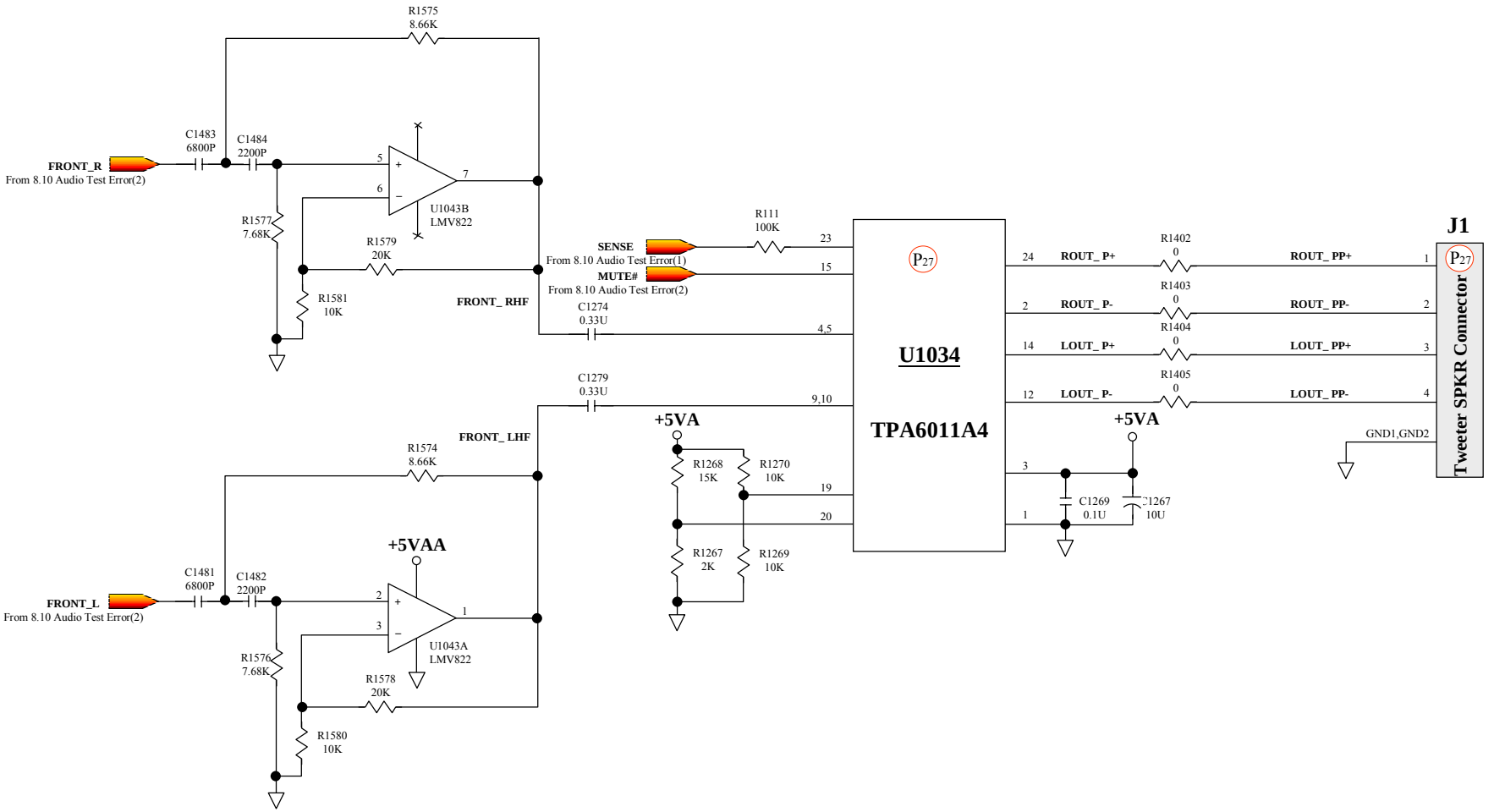
8.10 Audio Test Error(3) – Audio OUT-1

No sound from speaker after audio driver is installed.



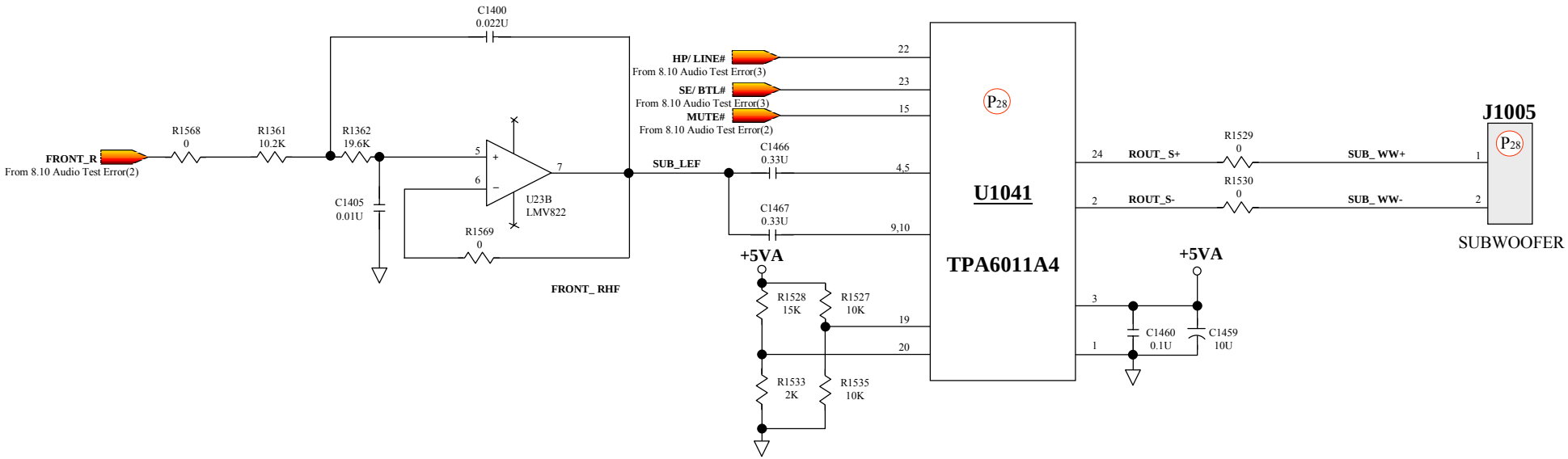
8.10 Audio Test Error(4) – Audio OUT-2

No sound from speaker after audio driver is installed.



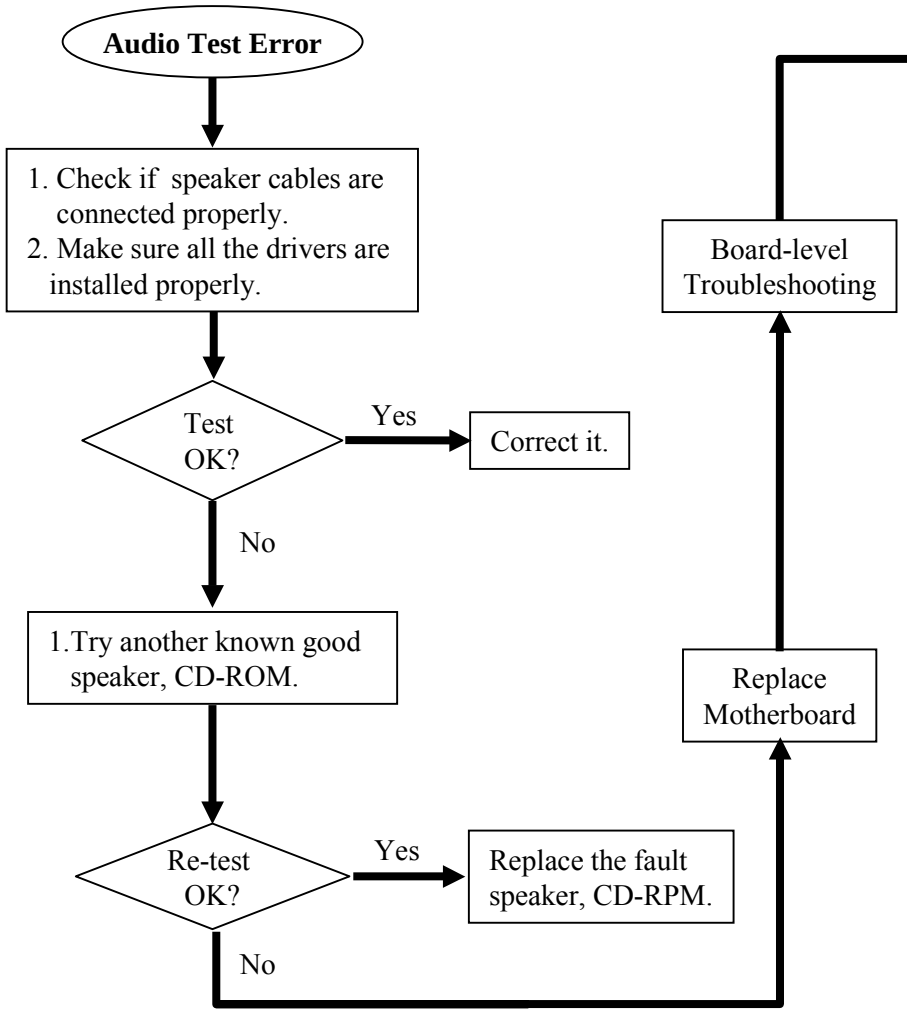
8.10 Audio Test Error(5) – Audio OUT-3

No sound from speaker after audio driver is installed.



8.10 Audio Test Error(6)

No sound from speaker after audio driver is installed.



Check the following parts for cold solder or one of the following parts on the motherboard may be defective,use an oscilloscope to check the following signal or replace parts one at a time and test after each replacement.

1.If no sound cause of line out, check the following parts & signals:

Parts:	Signals:
U1014	ROUT_T+/-
U19	TOUT_T+/-
U26	ROUT_PT+/-
U14	SIDESURR_R
J8	SIDESURR_L
J22	SPDIFOUT
J1020	
J1022	
C561	
C1281	
FB1076	
FB1077	

2. If no sound cause of MIC, check the following parts & signals:

Parts:	Signals:
U1014	MIC1_R
U19	MIC1_L
J1019	MIC_INT
C1264	MIC1_ VREF0_L
C1271	MIC1_ VREF0_R
FB1074	
FB1075	
R1421	
R1422	

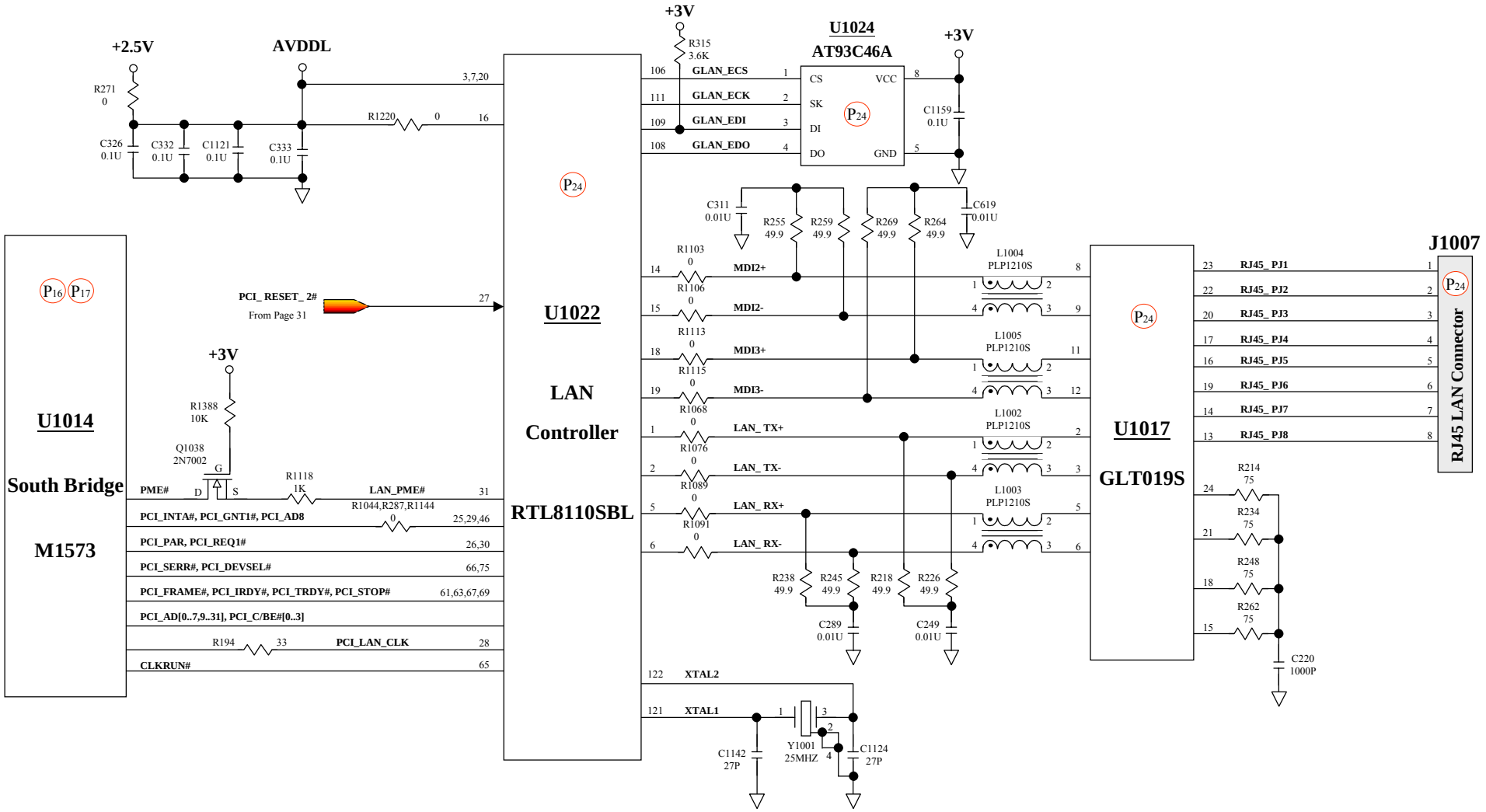
3. If no sound cause of CD-ROM, check the following parts & signals:

Parts:	Signals:
U1014	CDROM_L
U19	CDROM_R
J1008	CDROM_GND
R371	
R373	
R360	
R361	
R362	

8317 N/B Maintenance

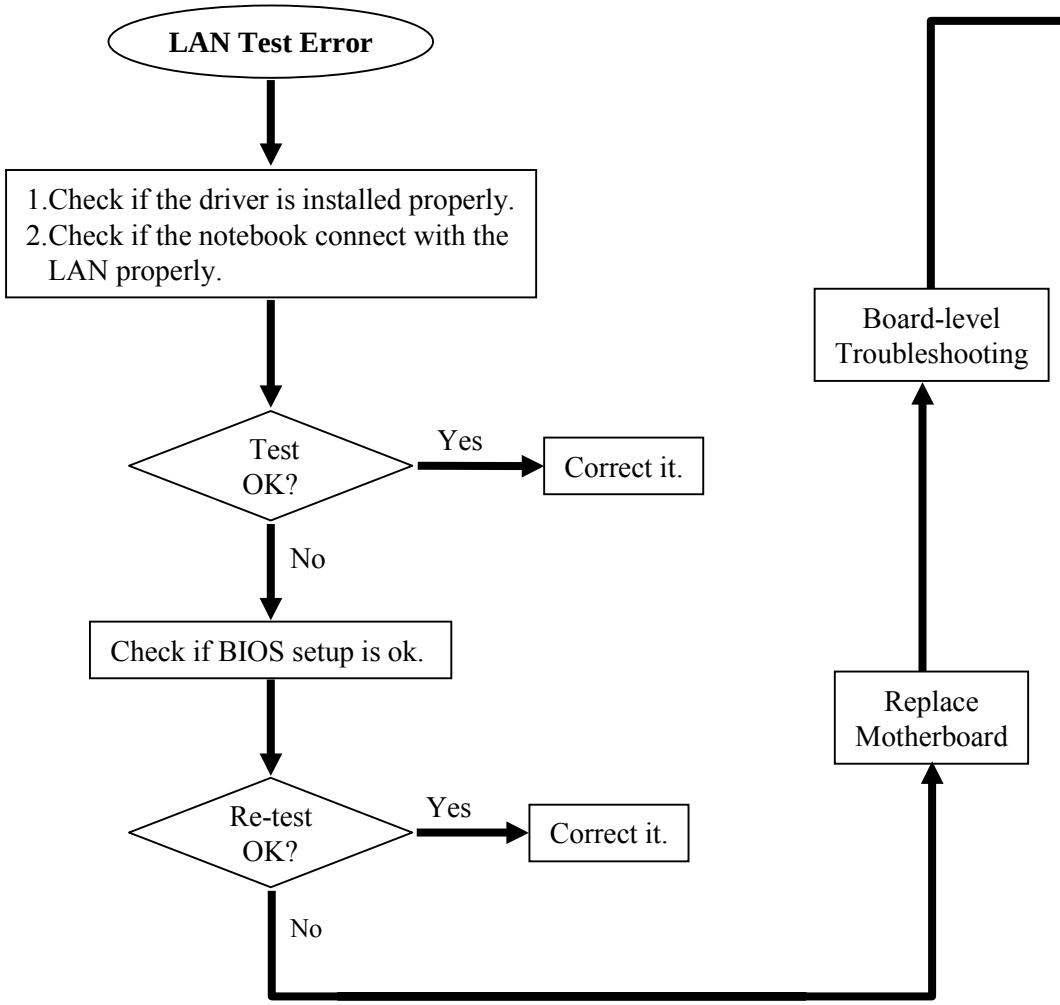
8.11 LAN Test Error(1)

An error occurs when a LAN device is installed.



8.11 LAN Test Error(2)

An error occurs when a LAN device is installed.



Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:

U1014
U1022
U1017
U1024
J1007
L1002
L1003
L1004
L1005
X1001
C249
C289
C311
C319

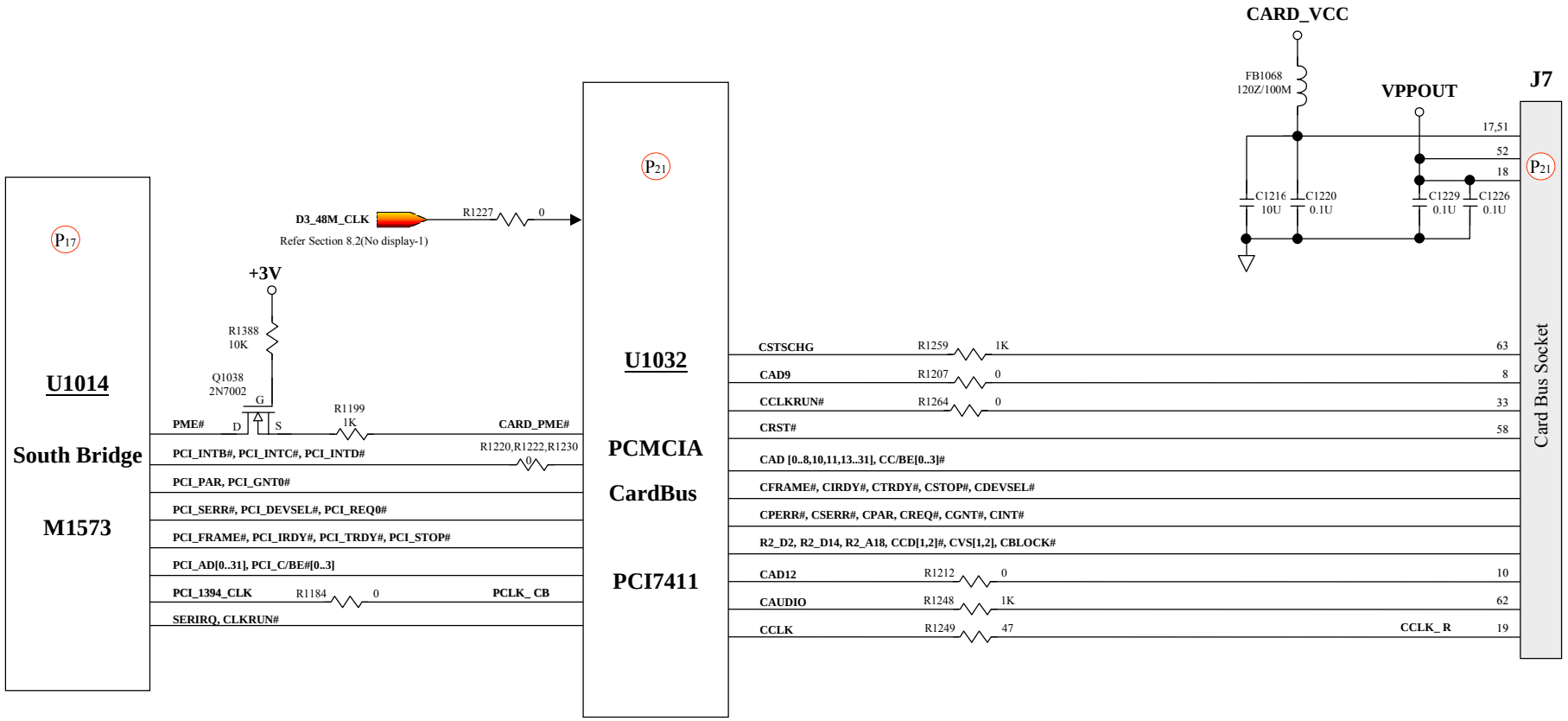
Signals:

PCI_LAN_CLK
PCI_RESET_2#
LAN_PME#
PCI_INTA#
PCI_REQ1#
PCI_GNT1#
PCI_SERR#
PCI_DEVSEL#
PCI_PAR
PCI_FRAME#
PCI_IRDY#
PCI_TRDY#
PCI_STOP#
PCI_AD[0..31]
PCI_C/BE#[0..3]
CLKRUN#

8317 N/B Maintenance

8.12 PC Card & Card Reader Socket Test Error(1)

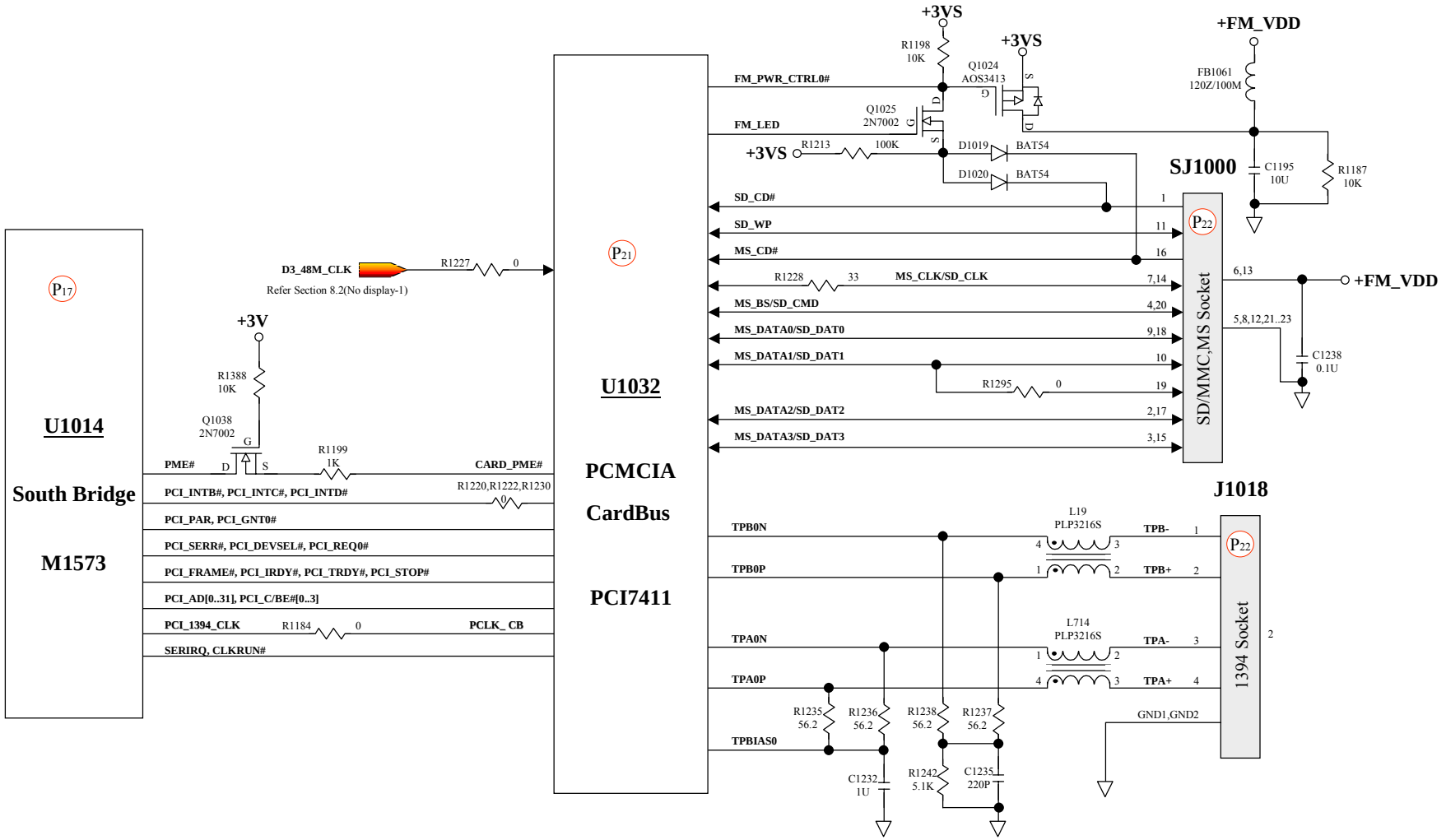
An error occurs when a PC card device is installed.



8317 N/B Maintenance

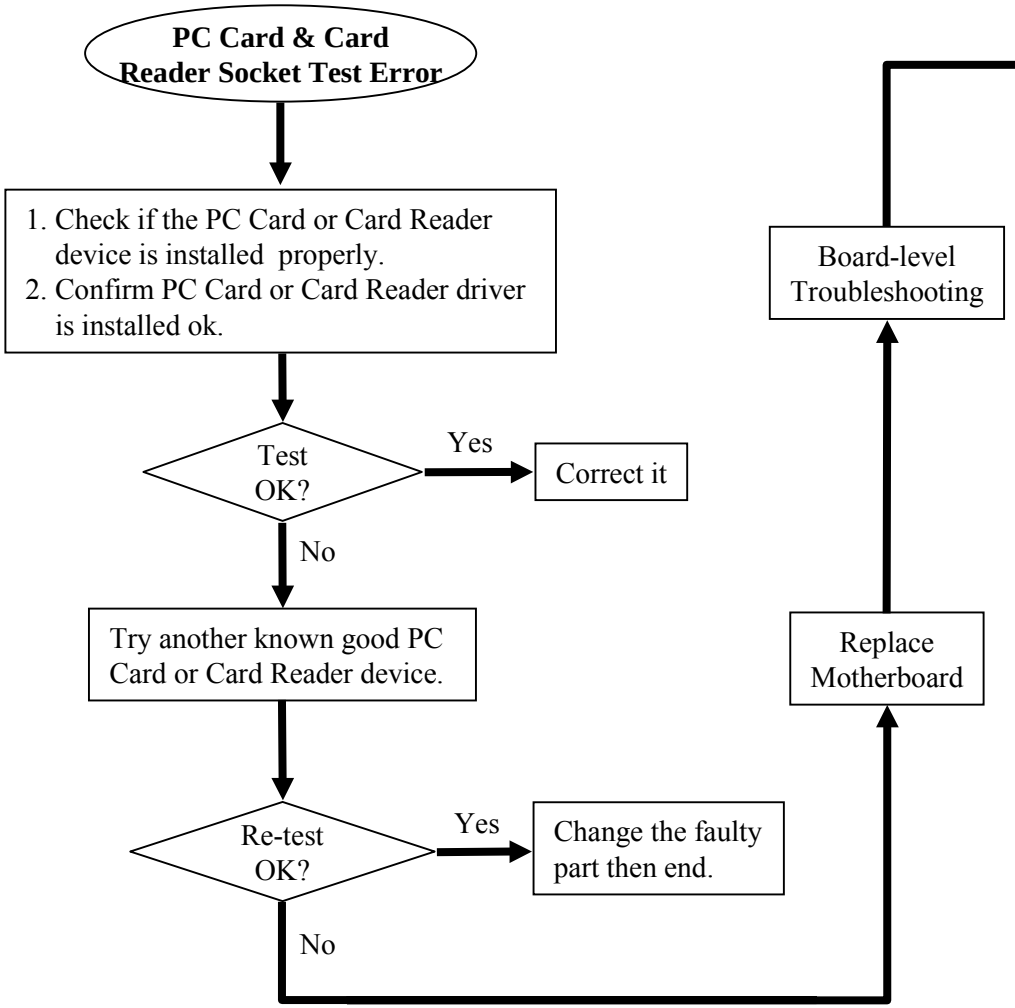
8.12 PC Card & Card Reader Socket Test Error(2)

An error occurs when a Card Reader device is installed.



8.12 PC Card & Card Reader Socket Test Error(3)

An error occurs when a PC card or SD Card device is installed.



Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:

U1014
U1032
J7
J1018
SJ1000
Q1038
R1199
FB1068
C1216
C1220
C1226
C1229
L19
L20
FB1061
Q1024
Q1025
D1019
D1020
C1195
R1187
R1295
C1238

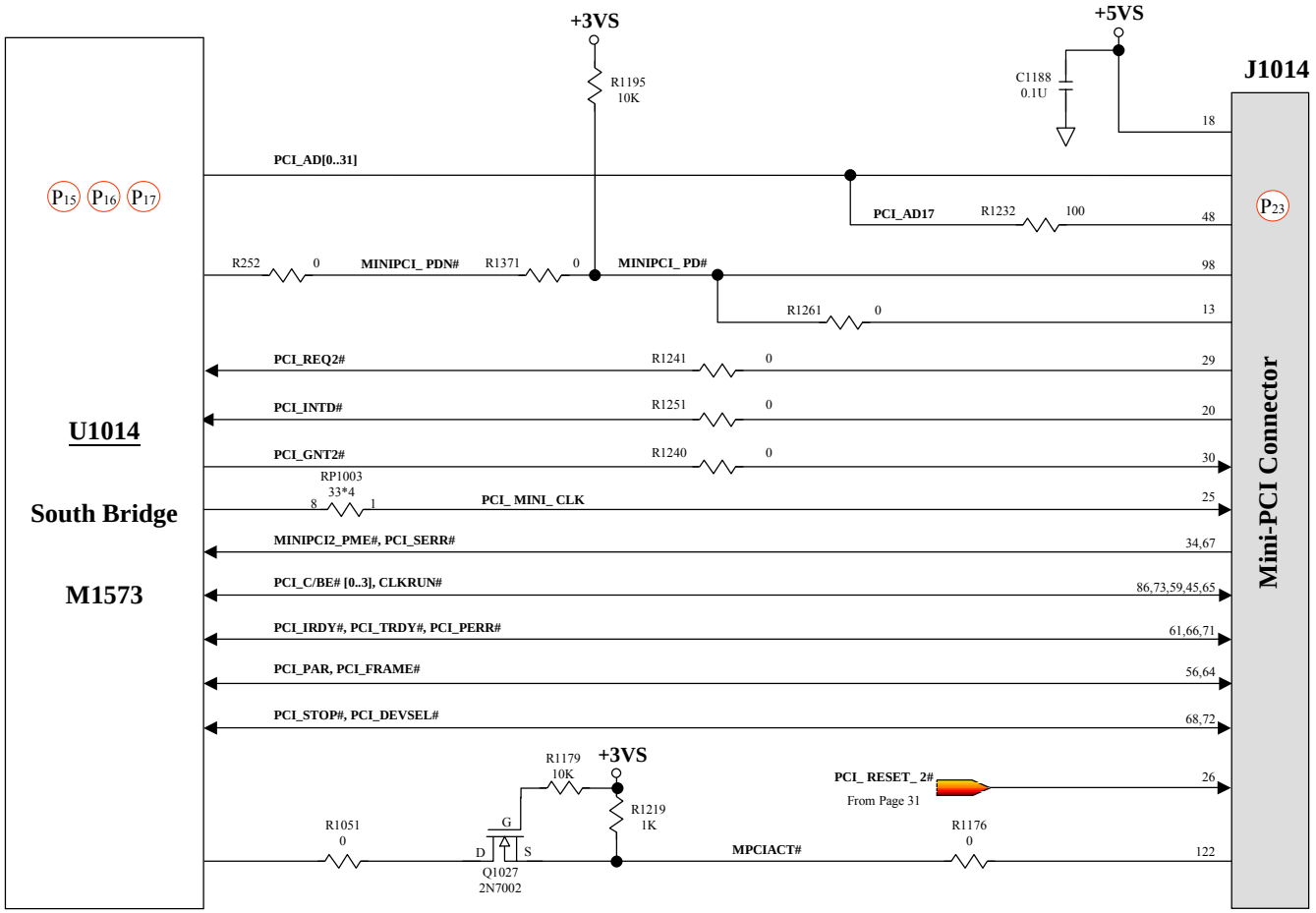
Signals

PCI_1394_CLK
D3_48M_CLK
CARD_PME#
PCI_INTB#
PCI_INTC#
PCI_INTD#
PCI_REQ0#
PCI_GNT0#
PCI_SERR#
PCI_PERR#
PCI_DEVSEL#
PCI_PAR
PCI_FRAME#
PCI_IRDY#
PCI_TRDY#
PCI_STOP#
PCI_AD[0..31]
PCI_C/BE[0..3]#
SERIRQ
CLKRUN#
VPPOUT
CARD_VCC

8317 N/B Maintenance

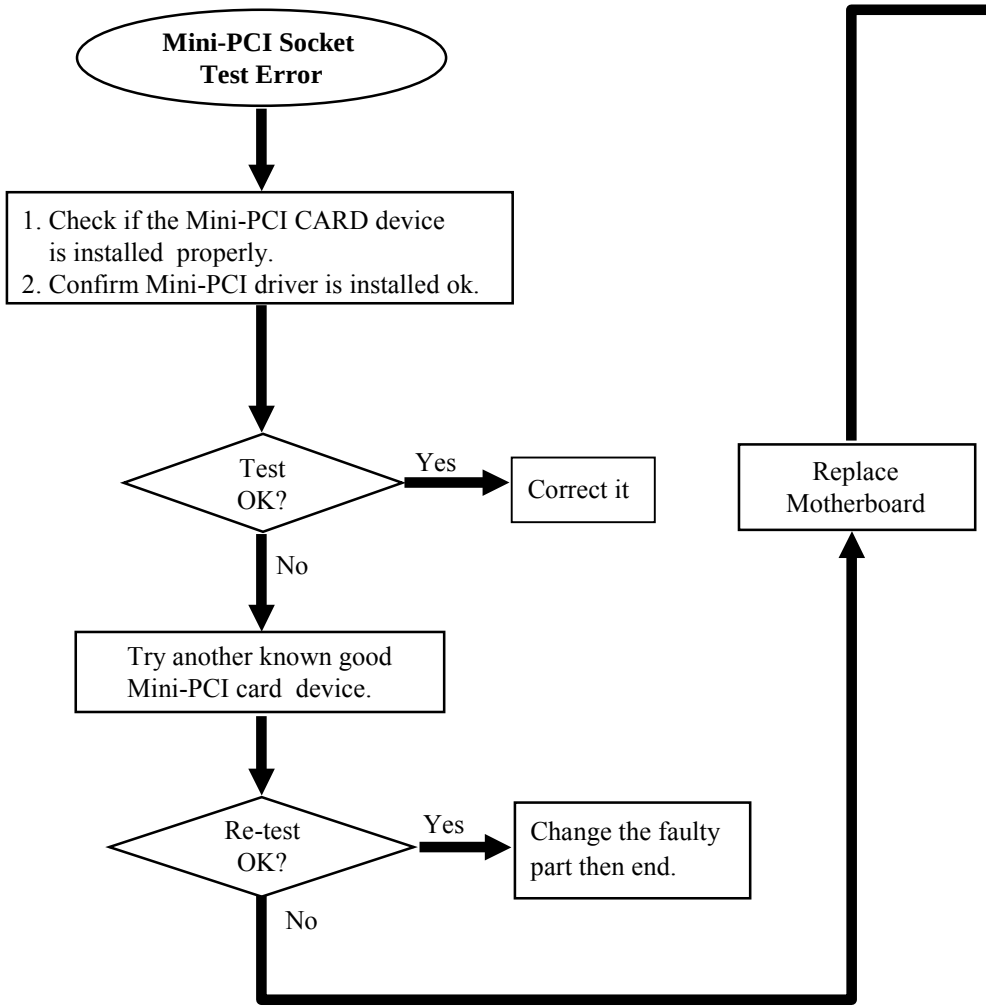
8.13 Mini-PCI Socket Test Error(1)

An error occurs when a PC card device is installed.



8.13 Mini-PCI Socket Test Error(2)

An error occurs when a PC card device is installed.



Board-level Troubleshooting

Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:	**Signals**	
U1014	+3VS	PCI_SERR#
J1014	PCI_AD[0..31]	PCI_PERR#
Q1027	PCI_C/BE#[0..3]	PCI_INTD#
R1219	MINIPCI_PD#	PCI_PAR
R1179	PCI_GNT2#	PCI_FRAME#
R1176	PCI_MINI_CLK	PCI_TRDY#
R1195	PCI_REQ2#	PCI_STOP#
R1371	PCI_IRDY#	PCI_DEVSEL#
R1232	CLKRUN#	
R1240		
R1241		

Reference Material

❖ AMD Model K8	AMD, INC
❖ ATI RS480M North Bridge	ATI, INC
❖ ULI M1573 South Bridge	ULI, INC
❖ HITACHI H8S/2140	HITACH, INC
❖ 8317 Hardware Engineering Specification	*Technology Corp*/MITAC

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