SERVICE MANUAL FOR

8080

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MiTAC

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1. Hardware Engineering Specification

1.1 Introduction

1.1.1 General Description

This document describes the brief introduction for MiTAC 8080 portable notebook computer system.

1.1.2 System Overview

The MiTAC 8080 model is designed for Intel Banias processor with 400MHz FSB with Micro-FCPGA package. It can support Banias 1.3GHz ~ 1.7GHz.

This system is based on PCI architecture and is fully compatible with IBM PC/AT specification, which has standard hardware peripheral interface. The power management complies with Advanced Configuration and Power Interface (ACPI) 2.0. It also provides easy configuration through CMOS setup, which is built in system BIOS software and can be pop-up by pressing F2 key at system start up or warm reset. System also provides icon LEDs to display system status, such as AC Power indicator, Battery Power indicator, Battery status indicator, CD-ROM, HDD, NUM LOCK, CAP LOCK, SCROLL LOCK, RF on/off status and Card Reader indicator. It also equipped with LAN, 56K Fax MODEM, 3 USB port, 3D stereo audio functions, S-Video and audio line out(S/PDIF), external microphone and an optional finger printer in function.

The memory subsystem supports two expansion DDR SDRAM slot with unbuffered PC1600/PC2100 DDR-SDRAM.

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The Montara-GM GMCH Host Memory Controller integrates a high performance host interface for Intel Banias processor, a high performance 2D/3D Graphic Engine, a high performance memory controller, Digital Video port (DVOB & DVOC) interface, and Intel Hub interface Technology connecting with Intel 82801DBM ICH4-M.

The Intel ICH4-M integrates three Universal Serial Bus 2.0 Host Controllers Interface (UHCI), the Audio Controller with AC97 interface, the Ethernet includes a 32-bit PCI controller, the IDE Master/Slave controllers, and Intel Hub interface technology.

The VIA VT6105LOM “Rhine III” Ethernet controller is a cutting edge, feature-rich, and cost-competitive single ASIC chip solution for PC “Lan On Motherboard” applications or Low Cost NIC applications. The 6105LOM eases server processor utilization by optimizing throughput between NIC and PCI bus allowing data transfers of up to at 200Mbps in full duplex mode, without using the system CPU. The VT6105LOM contains advanced power management feature for low power consumption including Wake On LAN (WOL) and is implemented using a low power 0.22 micron design.

The VT6307L is a single chip PCI Host Controller for IEEE 1394-1995 Release 1.0 and IEEE 1394a P2000. It implements the Link and PHY layers for IEEE 1394-1995 High Performance Serial Bus specification release 1.0 and 1394a P2000. It is compliant with 1394 Open HCI 1.0 and 1.1 with DMA engine support for high performance data transfer via a 32-bit bus master PCEI host bus interface. The VT6307L supports 100, 200 and 400 Mbit/sec transmission via an integrated 2-port PHY. The VT6307L services two types of data packets: asynchronous and isochronous(real time). The 1394 link core performs arbitration requesting, packet generation and checking, and bus cycle master operations. It also has root node capability and performs retry operations.

The ENE CB710 CardBus/Media Reader controller functions as a single slot PCI to Cardbus bridge and also PCI interface smart card and MS/SD/SM flash card reader. The CB710 provide one Cardbus slot and all reader interface may operate simultaneously.

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The NS PC87393 LPC Super I/O device is targeted for a wide range of portable applications. PC99 and ACPI compliant, it also incorporates: a Floppy Disk Controller (FDC), two enhanced Serial Ports (UARTs), one with Fast Infrared (FIR, IrDA 1.1 compliant), General-Purpose Input/Output (GPIO) support for a total of 32 ports, Interrupt Serializer for Parallel IRQs and an enhanced WATCHDOG timer.

The NS PC87393 Super I/O controller integrates the standard PC I/O functions: LPC bus interface, X-Bus Extension for read and write operations, floppy disk interface and one EPP/ECP capable parallel port. Like all LPC Super I/O devices, the PC87393 offers a single-chip solution to the most commonly used PC I/O peripherals to provide for the increasing number of multimedia application.

The STAC9750 is a 2 channel, 20-Bit DAC and 20-Bit ADC, full duplex AC'97 2.2 compatible stereo audio CODEC designed for PC multimedia systems, including soft/host audio and riser card base design. The STAC9750 supports with independent variable hardware sampling rates. The STAC9750 CODEC provides two pairs of stereo outputs with independent volume control, a mono output, a headphone output, and multiple stereo and mono inputs, alone with flexible mixing, gain and mute functions to provide a complete integrated audio solution for PCs. The STAC9750 also support an AC'97 2.2 compliant S/PDIF out functions which allows easy connection from the PC to consumer electronic products.

The CH7011A is a display controller device which accepts a digital graphics input signal, and encodes and transmits data to a TV output (analog composite, s-video or RGB). The device accepts data over one 12-bit wide variable voltage data port which supports five different data format including RGB and YcrCb. The TV-Out processor will perform non-interlace to interlace conversion with scaling and flicker filters, and encode the data into any of the NTSC or PAL video standards. The scaling and flicker filter is adaptive and programmable to enable superior text display. Eight graphics resolutions are supported up to 1024 X 768 with full vertical and horizontal underscan capability in all modes. A high accuracy low jitter phase locked loop is integrated to create outstanding video quality.

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Support is provided for Macrovision and RGB bypass mode which enable driving a VGA CRT with the input data.

The H8/F3437 is a high performance microcontroller with a fast H8/300 CPU core and a set of on-chip supporting functions optimized for embedded control. These include ROM, RAM, four types of timers, a serial communication interface, optional I²C bus interface, host interface, A/D converter, D/A converter, I/O ports, and other functions needed in control system configurations, so that compact, high performance systems can be implemented easily.

A full set of software drivers and utilities are available to allow advanced operating systems such as Windows ME, Windows 2000 and Windows XP to take full advantage of the hardware capabilities. Features such as bus mastering IDE, Plug and Play, Advanced Power Management (APM) with application restart, software-controlled power shutdown.

Following chapters will have more detail description for each individual sub-systems and functions.

System parts

- **CPU : Intel Banias processors in Micro-FCPGA package.**
- **Synthesizer : ICS950810.**
- **North Bridge : Montara-GM GMCH.**
- **South Bridge: ICH4-M**
- **TV-OUT : CH7011A**
- **Super I/O controller : NS PC87393**
- **Keyboard System : Hitachi H8/F3437 Universal Controller**
- **FAX/MODEM : Billonton MDC56S-I 56Kbps Fax Modem**

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- **LAN single chip : VT6105LOM**
- **PCMCIA controller : ENE CB710**
- **AC’97 Codec : STAC9750**
- **Thermal sensor : ADM1021A**
- **System Flash Memory (BIOS)**

1.1.2.1 CPU Module

- Intel Banias Processors with 478 pins Micro-FCPGA package.
- The first Intel mobile processor with the Intel NetBurst micro-architecture which features include hyper-pipelined technology, a rapid execution engine, a 400MHz system, an execution trace cache, advanced dynamic execution, advanced transfer cache, enhanced floating point and multi-media unit, and Streaming SIMD Extensions 2 (SSE2).
- The Streaming SIMD Extensions 2 (SSE2) enable break-through levels of performance in multimedia applications including 3-D graphics, video decoding/encoding, and speech recognition.
- Use Source-Synchronous Transfer (SST) of address and data to improve performance by transferring data four times per bus clock.
- Support Enhanced Intel SpeedStep technology, which enables real-time dynamic switching of the voltage and frequency between two performance modes.

1.1.2.2 Synthesizer

- System frequency synthesizer: ICS950810
- Programmable output frequency, divider ratios, output rise/fall time, output skew.
- Programmable spread percentage for EMI control.
- Watchdog timer technology to reset system if system malfunctions.
- Programmable watchdog safe frequency.
- Support I2C Index read/write and block read/write operations.

1.1.2.3 Montara-GM GMCH IGUI 3D Graphic DDR/SDR Chipset

Montara-GM GMCH IGUI Host Memory Controller integrates a high performance host interface for Intel Banias processor, a high performance 2D/3D Graphic Engine, a high performance memory controller, an AGP 4X interface, and Intel® I/O Hub architecture INTEL 82801DBM ICH4-M.

Montara-GM GMCH Host Interface features the AGTL & AGTL+ compliant bus driver technology with integrated on-die termination to support Intel Banias processors. Montara-GM GMCH provides a 12-deep In-Order-Queue to support maximum outstanding transactions up to 12. It integrated a high performance 2D/3D Graphic Engine, Video Accelerator and Advanced Hardware Acceleration MPEGI/MPEGII Video Decoder for the Intel Banias series based PC systems. It also integrates a high performance 2.1GB/s DDR266 Memory controller to sustain the bandwidth demand from the integrated GUI or external AGP master, host processor, as well as the multi I/O masters. In addition to integrated GUI, Montara-GM GMCH also can support external AGP slot with AGP 1X/2X/4X capability and Fast Write Transactions.

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A high bandwidth and mature Intel®' I/O Hub architecture is incorporated to connect Montara-GM GMCH and Intel 82801DBM ICH4-M together. Intel® I/O Hub architecture is developed into three layers, the Multi-threaded I/O Link Layer delivering 1.2GB bandwidth to connect embedded DMA Master devices and external PCI masters to interface to Multi-threaded I/O Link layer, the Multi-threaded I/O Link Encoder/Decoder in Intel 82801DBM ICH4-M to transfer data w/ 533 MB/s bandwidth from/to Multi-threaded I/O Link layer to/from Montara-GM GMCH, and the Multi-threaded I/O Link Encoder/Decoder in Montara-GM GMCH to transfer data w/ 533 MB/s from/to Multi-threaded I/O Link layer to/from Intel 82801DBM ICH4-M.

An Unified Memory Controller supporting DDR266 DRAM is incorporated, delivering a high performance data transfer to/from memory subsystem from/to the Host processor, the integrated graphic engine or external AGP master, or the I/O bus masters. The memory controller also supports the Suspend to RAM function by retaining the CKE# pins asserted in ACPI S3 state in which only AUX source deliver power. The Montara-GM GMCH adopts the Shared Memory Architecture, eliminating the need and thus the cost of the frame buffer memory by organizing the frame buffer in the system memory. The frame buffer size can be allocated from 8MB to 64MB.

Features :

- **Processor/Host Bus Support**
  - Intel® Banias processor
  - 2X Address, 4X data
  - Support host bus Dynamic Bus Inversion (DBI)
  - Supports system bus at 400MT/s (100 MHz)
  - Supports 64-bit host bus addressing
  - 8-deep In-Order-Queue
  - AGTL+ bus driver technology with integrated GTL termination resistors and low voltage operation (1.05V)
  - Supports Enhanced Intel® SpeedStep™ Technology (EIST) and Geyserville III

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- Support for DPWR# signal to Banias processor for PSB power management

- **Memory System**

  - Directly supports one DDR channel, 64-bts wide (72-b with ECC).
  - Supports 200-MHz and 266-MHz DDR devices with max of 2 Double-Sided SO-DIMMs(4 rows populated) with unbuffered PC1600/PC2100 DDR(with ECC).
  - Supports 128-Mb, 256-Mb and 512-Mbit technologies providing maximum capacity of 1-GB with only x 16 devices.
  - All supported devices have 4 banks.
  - Supports up to 16 simultaneous open pages.
  - Supports page sizes of 2KB, 4KB, 8KB, and 16KB. Page size is individually selected for every row.
  - UMA support only.

- **System interrupt**

  - Supports 8259 and Processor System Bus interrupt delivery mechanism
  - Supports interrupts signaled as upstream Memory Writes from PCI and Hub interface
  - MSI sent to the CPU through the system Bus
  - From IOxAPIC in ICH4-M
  - Provides redirection for upstream interrupts to the System Bus
  - Video Stream Decoder
  - Improved HW Motion Compensation for MPEG2
  - All format decoder (18 ATSC formats) supported
  - Dynamic Bob and Weave support for Video Streams
  - Software DVD at 60 fields/second and 30 frames/second full screen
  - Support for 720x480 pixel resolution DVD quality encoding at low CPU utilization

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- Video Overlay
- Single high quality scalable overlay and second Sprite to support second overlay
- Multiple overlay functionality provided via Arithmetic Stretch Blt
- Direct YUV from Overlay to TV-out
- Independent Gamma Correction
- Independent Brightness / Contrast / Saturation
- Independent Tint / Hue support
- Destination Color keying
- Source Chromakeying
- Maximum source resolution of 1920x1080 pixels
- Maximum overlay clock of 133 MHz/200 MHz provides a pixel resolution up to 1600x1200@ 60Hz or 1280x 1024@ 85 Hz

Display

- Analog Display Support
- 350 MHz integrated 24-bit RAMDAC that can drive a standard progressive scan analog monitor up to 1800 x1350@ 85 Hz.
- Accompanying I2C and DDC channels provided through multiplexed interface Hot-plug and display support
- Dual independent pipe with single display support Simultaneous: Same images and native display timings on each display device
- DVO (DVOB) support
- Digital video out port DVOB with 165-MHz dot clock on 12-bit interface
  - -- Variety of DVO devices channel
  - -- Compliant with DVI Specification 1.0, thereby providing support for a flat panel up to 2048x1536 pixel resolution, or digital CRT up to 1920x1080 pixel resolution

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- Dedicated LFP (local flat panel) interface
  - -- Single or dual channel LVDS panel support up to SXGA+ panel resolution with frequency range from 25MHz to 112MHz per channel
  - -- SSC support of 0.5%, 1.0%, and 2.5% center and down spread with external SSC clock
  - -- Supports data format of 18 bpp
  - -- Direct YUV from Overlay to TV-out
  - -- LCD panel power sequencing compliant with SPWG timing specification
  - -- Compliant with ANSI/TIA/EIA –644-1995 spec
  - -- Integrated PWM interface for LCD backlight inverter control
  - -- Bi-linear Panel fitting
- Tri-view support through LFP interface, DVO ports and CRT
- Internal Graphics Features
- Core Frequency
  - -- Display Core frequency of 133MHz
  - -- Render Core frequency of 133MHz
- 2D Graphics Engine
- Optimized 128 bit BLT engine
- Ten programmable and predefined monochrome patterns
- Alpha Stretch Blt (via 3D pipeline)
- Anti-aliased lines
- Hardware-based BLT Clipping & Scissoring
- 32-bit Alpha Blended cursor
- Programmable 64*64 3-color Transparent cursor
- Color Space Conversion
- 3 Operand Raster BLTs

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- 8-bit, 16-bit, and 32-bit color
- ROP support
- DIB translation and Linear/Title addressing
- 3D Graphics Engine
- 3D Setup and Render Engine
- Viewpoint Transform and Perspective Divide
- Triangle Lists, Strips and Fans support
- Indexed Vertex and Flexible Vertex formats
- Pixel accurate Fast Scissoring and Clipping operation
- Back-face Culling support
- DirectX™ and OGL Pixelization rules
- Anti-Aliased Lines support
- Sprite Points support
- Zone Rendering
- Provides the highest sustained fill rate performance in 32-bit color and 24-bit W mode
- High quality performance Texture Engine
- 266 MegaTexel/speak performance
- Per Pixel Perspective corrected Texture Mapping
- Single Pass Texture Composting (Multi-Texture) at rate
- Enhanced Texture Blending functions
- Twelve Level of Detail MIP Map Sizes from 1x1 to 2Kx2K
- Numerous Texture formats including 32-bit RGBA
- Alpha and Luminance Maps
- Texture Chromakeying

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- Bilinear, Trilinear, Anisotropic MIP-Mapped Filtering
- Cubic Environment Reflection Mapping
- Embossed Bump-mapping
- DXTn Texture Decompression
- 3D Graphics Rasterrization enhancements
- One Pixel per Clock
- Flat and Gouraud Shading
- Color Alpha Blending for Transparency
- Vertex and Programmable Pixel Fog and Atmospheric effects
- Color Specular Lighting
- Vertex and Programmable Pixel Fog and Atmospheric effects
- Z Bais support
- Dithering
- Line and Full-Scence Anti-Aliasing
- 16 and 24-bit Z Buffering
- 16 and 24-bit W Buffering
- 8-bit Stencil Buffering
- Double and Triple Render Buffer support
- 16 and 32 –bit color
- Destination Alpha
- Vertex Cache
- Maximum 3D resolution of 1600x1200 x32 bpp at 85 Hz
- Optimal 3D resolution supported
- Fast Clear support

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- **HUB Interface for ICH4**

  - 266 MB/s point to point hub interface to ICH4-M
  - 66-M Hz base clock
  - Supports the following traffic types to the ICH4-M
  - Hub interface-to DRAM
  - CPU-to-Hub interface
  - Messaging
  - MSI interrupt messages
  - Power Management state change
  - SMI, SCI, and SERR error indication
  - Power Management
    - -- SMRAM space remapping to A0000h (128-KB)
    - -- Supports extended SMRAM space above 256- MB ,additional 1 MB TSEG from top of Memory, cacheable (cacheability controlled by CPU)
    - -- APM rev 1.2 compliant power management
    - -- Supports Suspend to System Memory(S3),Suspend to Disk(S4) and Hard Off/Total Reboot(S5)
    - -- ACPI 1.0b,2.0 Support

1.1.2.4 I/O Controller Hub : Intel 82801DBM

The Intel 82801DBM ICH4-M integrates three Universal Serial Bus 2.0 Host Controllers, the Audio Controller with AC 97 Interface, the IDE Master/Slave controllers, and Intel® I/O Hub architecture. The PCI to LPC Bridge, I/O Advanced Programmable Interrupt Controller, legacy system I/O and legacy power management functionalities are integrated as well.

The integrated Universal Serial Bus Host Controllers features Dual Independent UHCI Compliant Host controllers with six USB ports delivering 480 Mb/s bandwidth and rich connectivity. Besides, Legacy USB devices as well as over current detection are also implemented.

The Integrated AC97 v2.3 compliance Audio Controller that features a 7-channels of audio speaker out and HSP v.90 modem support. Additionally, the AC97 interface supports 4 separate SDATAIN pins that is capable of supporting multiple audio codecs with one separate modem codec.

The integrated IDE Master/Slave controllers features Dual Independent IDE channels supporting PIO mode transfers up to 16 Mbytes/sec and Ultra DMA 33/66/100. It provides two separate data paths for the dual IDE channels that sustain the high data transfer rate in the multitasking environment.

Intel 82801DBM ICH4-M supports 6 PCI masters and complies with PCI 2.2 specification. It also incorporates the legacy system I/O like: two 82C37 compatible DMA controllers, Channels 0-3 are hardwired to 8 bit, three 8254 compatible programmable 16-bit counters channels 5-7, hardwired keyboard controller and PS2 mouse interface(not use in MiTAC 8080 model), Real Time clock with 512Bytes CMOS SRAM and two 82C59 compatible Interrupt controllers. Besides, the I/O APIC managing up to 14 interrupts with both Serial and FSB interrupt delivery modes is supported.

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The integrated power management module incorporates the ACPI 1.0b compliance functions, the APM 1.2 compliance functions, and the PCI bus power management interface spec. v1.1. Numerous power-up events and power down events are also supported. 21 general purposed I/O pins are provided to give an easy to use logic for specific application. In addition, the Intel 82801DBM ICH4-M supports Deeper Sleep power state for Intel Mobile processor.

A high bandwidth and mature Intel®' I/O Hub architecture is incorporated to connect Montara and Intel 82801DBM ICH4-M Hub interface together. Intel® I/O Hub architecture is developed

Features :

- PCI Bus Interface
- Supports PCI Revision 2.2 Specification at 33 MHz
- 133 MB/sec maximum throughput
- Supports up to six master devices on PCI
- One PCI REQ/GNT pair can be given higher arbitration priority (intended for external 1394 host controller)
- Support for 44-bit addressing on PCI using DAC protocol Integrated LAN Controller
- WfM 2.0 and IEEE 802.3 compliant
- LAN Connect Interface (LCI)
- 10/100 Mbit/sec Ethernet support_ Integrated IDE Controller
- Supports "Native Mode" register and interrupts
- Independent timing of up to 4 drives, with separate primary and secondary IDE cable connections

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- Ultra ATA/100/66/33, BMIDE and PIO modes
- Tri-state modes to enable swap bay
- USB
- Includes three UHCI host controllers that support six external ports
- New: Includes one EHCI high-speed USB 2.0 Host Controller that supports all six ports
- New: Supports a USB 2.0 high-speed debug port
- Supports wake-up from sleeping states S1–S5
- Supports legacy keyboard/mouse software AC-Link for Audio and Telephony CODECs
- Supports AC ’97 2.3
- New: Third AC_SDATA_IN line for three codec support
- New: Independent bus master logic for seven channels (PCM In/Out, Mic 1 input, Mic 2 input, modem in/out, S/PDIF out)
- Separate independent PCI functions for audio and modem
- Support for up to six channels of PCM audio output (full AC3 decode)
- Supports wake-up events Interrupt Controller
- Support up to eight PCI interrupt pins
- Supports PCI 2.2 message signaled interrupts
- Two cascaded 82C59 with 15 interrupts
- Integrated I/O APIC capability with 24 interrupts

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- Supports serial interrupt protocol
- Supports processor system bus interrupt delivery New: 1.5 V operation with 3.3 V I/O
- 5 V tolerant buffers on IDE, PCI, USB over current and legacy signals Timers Based on 82C54
- System timer, refresh request, speaker tone output Power Management Logic
- ACPI 2.0 compliant
- ACPI-defined power states (C1–C2, S3–S5)
- Supports Desktop S1 state (like C2 state, only STPCLK# active)
- ACPI power management timer
- PCI PME# support
- SMI# generation
- All registers readable/restorable for proper resume from 0 V suspend states External Glue Integration
- Integrated pull-up, pull-down and series termination resistors on IDE, processor interface
- Integrated Pull-down and Series resistors on USB Enhanced Hub Interface Buffers Improve Routing flexibility (Not available with all Memory Controller Hubs)

1.1.2.5 CH7011A

The CH7011 is a Display controller device which accepts a digital graphics input signal, and encodes and transmits data to a TV output (analog composite, s-video or RGB). The device accepts data over one 12-bit wide variable voltage data port which supports five different data formats including RGB and YCrCb.The TV-Out processor will perform non-interlace to interlace conversion with scaling and flicker filters, and encode the data into any of the NTSC or PAL video standards. The scaling and flicker filter is adaptive and programmable to enable superior text display. Eight graphics resolutions are supported up to 1024 by 768 with full vertical and horizontal underscan capability in all modes. A high accuracy low jitter phase locked loop is integrated to create outstanding video quality. Support is provided for Macrovision™ and RGB bypass mode which enables driving a VGA CRT with the input data.

Features :

- TV output supporting up to 1024x768 graphics resolutions
- Macrovision™ 7.X copy protection support
- Programmable digital interface supports RGB and YCrCb
- True scale rendering engine supports underscan in all TV output resolutions
- Enhanced text sharpness and adaptive flicker removal with up to 7 lines of filtering
- Support for all NTSC and PAL formats
- Provides CVBS, S-Video and SCART (RGB) outputs
- TV connection detect
- Programmable power management
- 10-bit video DAC outputs

- Fully programmable through serial port
- Complete Windows and DOS driver support
- Low voltage interface support to graphics device

1.1.2.6 Super I/O_NS PC87393

National Semiconductor's PC8739x family of LPC Super I/O devices is targeted for a wide range of portable applications. PC99 and ACPI compliant, the PC8739x family features an X-Bus Extension for read and write operations over the X-Bus, a full IEEE 1284 Parallel Port with a Parallel Port Multiplexer (PPM) for external Floppy Disk Drive (FDD) support, a Musical Instrument Digital Interface (MIDI) port, and a Game port. Like all National LPC Super I/O devices, the PC8739x offers a single-chip solution to the most commonly used PC I/O peripherals.

The PC8739x family also incorporates: a Floppy Disk Controller (FDC), two enhanced Serial Ports (UARTs), one with Fast Infrared (FIR, IrDA 1.1 compliant), General-Purpose Input/Output (GPIO) support for a total of 32 ports, Interrupt Serializer for Parallel IRQs and an enhanced WATCH DOG timer.

1.1.2.7 Keyboard controller Hitachi H8/3437

The H8/3437 Series is a series of high-performance micro-controllers with a fast H8/300 CPU core and a set of on-chip supporting functions optimized for embedded control. These include ROM, RAM, four types of timers, a serial communication interface, optional I2C bus interface, host interface, A/D converter, D/A converter, I/O ports, and other functions needed in control system configurations, so that compact, high-performance systems can be implemented easily. The series includes the H8/3437 with 60kbyte ROM and 2kbyte RAM, the H8/3436 with 48kbyte ROM and 2kbyte RAM, and the H8/3434 with 32kbyte ROM and 1kbyte RAM.

The H8/3437, H8/3436, and H8/3434 are available in mask-ROM versions. The H8/3437 and H8/3434 are also available in ZTAT™*1 (zero turn-around time) versions, providing a quick and flexible response to conditions from ramp-up through full-scale volume production, even for applications with frequently-changing specifications. In addition, the H8/3434 and H8/3437 have F-ZTAT™*2 (flexible-ZTAT) versions with on-board programmability.

1.1.2.8 Fast Ethernet Controller VT6105LOM

The VIA Rhine III VT6105LOM is a 10/100Mbps Fast Ethernet controller designed to provide system designers an easy to integrate single chip solution, with advanced management and power conservation features. Featuring a 3-in-1 design the VIA VT6105LOM integrates the physical, media, and management layers into a single chip.

Features :

- Single chip full/half duplex 10/100Mbps Fast Ethernet Management Controller
- IEEE 802.3/802.3u 10BASE-T and 100BASE-T Compatible

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- 32bit PCI Bus-Master Interface
- VIA Rhine based CSR definition provides efficiency PCI bus-mastering
- Low power 100base-TX transceiver embedded Support 10Mbps and 100Mbps N-way Auto-negotiation operation Support Auto-MDIX function
- Enhancement MAC functions for 802.3 networking 802.1 Priority Transmit Maximum eight priority queues by drivers programmable 802.1q Multiple VLAN support VLAN long frames support (1518+4bytes) VLAN tag auto inserting and extracting on TX and RX side (VT6105LOM) NIC auto filtering on VLAN ID optional (VT6105LOM)
- IP header Checksum Offload supporting for Ipv4 frames. Support both of TCP and UDP protocol (VT6105LOM)
- Support Physical, Broadcast, and Multicast addresses filtering using both hashing table look-up and perfect-match mechanisms (VT6105LOM)
- 12 sets hardware 16 bit MIB counters (VT6105LOM)
- Fiber Optic network support (VT6105LOM)
- WFM 2.0 (VT6105LOM)
- DMI 2.0 (H/W)
- IO 3.3v with PCI bus 5V tolerant / Core 2.5v power, using low power 0.22um TSMC CMOS process, 128pin PQFP package.

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1.1.2.9 Fax/Modem module

- Made by Billionton Computer corporation
- Integrated PCI v2.2 Interface
- Host-based ITU V.70 DSVD.
- Operation support: Windows 95/NT/ME/2000
- K56flex for internet connection rates approaching 56kbits/s.
- Data Modes capabilities
- On Chip PnP Logic
- ACPI support “On Now”
- Support “Call ID”
- PC 97 Compliant – Unimodem/V Compliant
- Low Power Consumption
- Operation Voltage 3.3V

1.1.2.10 PCMCIA controller_ ENE CB710 + ENE CP2211

CB710

It’s function as a signal-slot PCI-to-Cardbus bridge and also PCI-interface smart card and MS/SD/SM flash card readers.

Features :

- One Cardbus slot and all reader interfaces may operate simultaneously.

  - 280pin LPFQ or 209pin-ball LFBGA package.
  - 3.3V core operation with 5V tolerant I/O pads.
  - Compliant with PCI 2.2, ACPI 1.0, ect.
  - One traffic LED pin for each reader interface.

- Cardbus Controller:

  - working with ENE CP2211 Cardbus power switch.
  - Compliant with PC Card Standard 8.0.
  - Configurable interrupts and miscellaneous control logic.

- Smart Card Reader:

  - Compliant with PC/SC Specification 1.0.
  - Support ISO7816 T=0 and T=1 protocols and 3V/5V cards.

- Secure Digital (SD) Reader:

  - Compliant with SD Memory Card Specification Version 1.0.
  - Max 10MBps data rate with 16-byte data buffer and optional clock source.

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- Support 4-bit data lines, write protect switch, card detection by DAT3 or a dedicated switch.

- Memory Stick (MS) Reader:
  - Compliant with Memory Stick Standard Format Specification Version 1.3
  - Max 2.5MBps data rate with 16-byte data buffer and optional clock source.

- Smart Media (SM) Reader:
  - Compliant with SmartMedia Standard 2000 and SmartMedia Interface Library (SMIL) version 1.0.
  - Support 5V and 3V SmartMedia cards.
  - Support Hardware ECC (1-bit correction and 2-bits detection)

CP2211 (Power Switch)

- Fully integrated V_{CC} and V_{PP} switching
- Low $r_{DS(ON)}$: 90-mΩ 5V and 3.3V V_{CC} Switches
- Compatible with industry standard controllers
- 12V supply not required unless the PC Card uses 12V for flash programming or other applications
- 3.3V low voltage mode
- Short-circuit and thermal protection
- Compatible with 3.3V, 5V, and 12V PC Cards

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1.1.2.11 AC”97 Codec _ STAC9750

- High performance CODEC with high S/N ratio (>90 dB).
- Compliant with AC’97 2.2 specifications
- 20-bit stereo Digital-to-Analog Converter with variable sampling rate.
- 20-bit stereo Analog-to-Digital Converter with variable sampling rate.
- 4 analog line-level stereo inputs with 5-bit volume control: LINE_IN, CD, VIDEO, AUX.
- 2 analog line-level mono inputs: PC_BEEP, PHONE_IN.
- Mono output with 5-bit volume control.
- Stereo output with 5-bit volume control.
- 2 MIC inputs are software selectable.
- Power management capabilities.
- 3D Stereo Enhancement
- Embedded 50mW/20 ohm at LINE output.
- External amplifier power down capability.
- Digital S/PDIF output.
- Built in 14.318M 24.576MHz PLL to save external 24.576MHz crystal
- Supports 2 general-purpose I/O pins.
- Power supply: Digital: 3.3V; Analog: 5V/3.3V
- Standard 48-Pin LQFP Package

1.1.2.12 Thermal Sensor_ ADM1021A

- On-Chip and Remote Temperature Sensing
- No Calibration Necessary
- 1_C Accuracy for On-Chip Sensor
- 3_C Accuracy for Remote Sensor
- Programmable Over/Under Temperature Limits
- Programmable Conversion Rate
- 2-Wire SMBus Serial Interface
- Supports System Management Bus (SMBus) Alert
- 200 _A Max Operating Current
- 1 _A Standby Current
- 3 V to 5.5 V Supply
- Small 16-Lead QSOP Package

1.1.2.13 System Flash Memory (BIOS)

- 4M bit Flash memory
- Flashed by 5V only
- User can upgrade the system BIOS in the future just running flash program.

1.1.2.14 IEEE1394a Controller VT6307L

The VIA Fire IIM VT6307 is a single-chip, low power 2-port IEEE 1394 host controller providing PC systems with high speed, flexible connectivity to a wide range of peripherals and consumer electronics. Supporting the latest high speed IEEE 1394a standards, the VIA VT6307 can detect connected device types and automatically configure data speeds to 100, 200, or 400 Mbps, transmitting both asynchronous and isochronous (real-time) data packets.

Features :

- Single chip PCI Host Controller for IEEE 1394-1995 Release 1.0 and IEEE 1394a P2000 Embedded 1394 Link core
  - Dual Buffer mode enhancements
  - Skip Processing enhancements
  - Block Read Request handling
  - 32 bit CRC generator and checker for receive and transmit data
- Integrated 400Mbps 2-port PHY
  - Supports two 1394a fully compliant cable ports at 100/200/400Mbps
  - Supports IEEE 1394-1995 Standard for High Performance Serial Bus 1.0 and 1394a P2000

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- Full 1394a P2000 support
- Logic performs bus initialization and arbitration functions
- 2KV ESD protection

- 32-Bit Power-Managed PCI Bus-Interface
  - Compliant with PCI specification v2.2
  - Supports CardBus interface
- Supports I2C EEPROM and 4-Wire Serial ROM with GUID PROM Shadow to EEPROM
- OHCI Compliant Programming Interface
- Pin Compatible with VIA VT6306 1394a PCI Host Controller
- 3.3V Power Supply with 5V Tolerant Inputs
- 0.30 micron low power CMOS process
- 128-Pin, LQFP Package
- PCB reference designs & schematics available

1.2 Other Functions

1.2.1 Hot Key Function

Keys combination	Feature	Meaning
Fn + F1	Reserve	
Fn + F2	Reserve	
Fn + F3	Volume Down	
Fn + F4	Volume Up	
Fn + F5	LCD/External CRT Switching	Rotate display mode in LCD only, CRT only and simultaneously display.
Fn + F6	Brightness Down	Decreases the LCD brightness
Fn + F7	Brightness Up	Increases the LCD brightness
Fn + F8	Reserve	
Fn + F9	Reserve	
Fn + F10	Battery beep enable/disable	Battery low beep sound enable/disable
Fn + F11	Panel Off/On	Toggle Panel Off/On
Fn + F12	Suspend to DRAM/HDD	Force the computer into either Suspend to HDD or Suspend to RAM mode.

1.2.2 Power On/Off/Suspend/Resume Button

1.2.2.1 APM Mode

At APM mode, Power button is on/off system power.

1.2.2.2 ACPI Mode

At ACPI mode. Power button behavior was set by windows power management control panel.

You could set “standby” , “power off” or “hibernate”(must enable hibernate function in power management) to power button function. Continue pushing power button over 4 seconds will force system off at ACPI mode.

1.2.3 Cover Switch

System automatically provides power saving by monitoring Cover Switch. It will save battery power and prolong the usage time when user closes the notebook cover.

At ACPI mode there are four functions to be chosen at windows power management control panel.

1. None
2. Standby
3. Off
4. Hibernate (must enable hibernate function in power management)

1.2.4 LED Indicators

System has eight status LED indicators to display system activity, which include three at front side and five above keyboard.

1.2.4.1 Three LED indicators on LCD panel:

From left to right that indicate: AC POWER, BATTERY POWER and BATTERY STATUS.

AC POWER : This LED lights green when the notebook is being powered by AC, and flash (on 1 second, off 1 second) when Suspend to DRAM is active using AC power. The LED is off when the notebook is off or powered by batteries.

BATTERY POWER : This LED lights green when the notebook is being powered by Battery , and flash (on 1 second, off 1 second) when Suspend to DRAM is active using Battery power. The LED is off when the notebook is off or powered by batteries, or when Suspend to Disk.

BATTERY STATUS : During normal operation, this LED stays off as long as the battery is charged. When the battery charge drops to 10% of capacity, the LED lights red, flashes per 1 second and beeps per 2 second. When AC is connected, this indicator glows green if the battery pack is fully charged or orange (amber) if the battery is being charged.

1.2.4.2 Five LED indicators at front side:

From left to right that indicates CD-ROM/HARD DISK DRIVE, NUM LOCK, CAPS LOCK and SCROLL LOCK.

1.2.5 Battery status

1.2.5.1 Battery Warning

System also provides Battery capacity monitoring and gives user a warning so that users have chance to save his data before battery dead. Also, this function protects system from mal-function while battery capacity is low.

Battery Warning: Capacity below 10%, Battery Capacity LED flashes per second, system beeps per 2 seconds.

System will Suspend to HDD after 2 Minutes to protect users data.

1.2.5.2 Battery Low State

After Battery Warning State, and battery capacity is below 4%, system will generate beep for twice per second.

1.2.5.3 Battery Dead State

When the battery voltage level reaches 7.6 volts, system will shut down automatically in order to extend the battery packs' life.

1.2.6 Fan Power On/Off Management

FAN is controlled by H8 embedded controller using ADM1021A to sense CPU temperature and PWM control fan speed. Fan speed is depended on CPU temperature. Higher CPU temperature faster Fan Speed.

1.2.7 CMOS Battery

CR2032 3V 220mAh lithium battery.

When AC in or system main battery inside, CMOS battery will consume no power. AC or main battery not exist, CMOS battery life at less (220mAh/5.8uA) 4 years. Battery was put in battery holder, can be replaced.

1.2.8 I/O Port

- One Power Supply Jack.
- One External CRT Connector For CRT Display
- One S-Video TV Output Connector
- Supports three USB2.0 port for all USB devices.
- One MODEM RJ-11 phone jack for PSTN line
- One RJ-45 for LAN.
- Microphone Input Jack.
- S/PIDF out Jack
- One CardBus Sockets for one type II PC card extension
- Two Card Reader Sockets for SM/MMC/SD/MS
- One IR port (use SHARP GP2W1001YP)
- One IEEE 1394a port for all firewire devices

1.3 Peripheral Components

1.3.1 LCD Panel

- 1st Source QDI 14.1” TFT: QD141X1LH03-MP01
- 2nd Source: Chi-Mei 14.1 TFT : N141X6-L0

1.3.2 Ext. Floppy Disk Drive

- External USB 3.5” 1.44MB /1.2 MB/720KB FDD (Option)
- 1st Source :Mitsumi D353FUE
- 2nd Source :NEC UF0002

1.3.3 HDD

- Fujitsu 20GB: MHR2020AT / 30GB: MHR2030AT/ 40GB : MHR2040AT
- Hitachi 20 GB: DK23DA-20F / 30GB DK23DA-30F/ 40GB DK23DA-40F

1.3.4 Keyboard

- JME 19mm pitch/3.0mm stroke

1.3.5 DVD ROM Drive

- 1st source :TEAC DV-28E-B93
- 2nd source: QSI SDR-083

1.3.6 COMBO Drive

- 1st source : KME UJDA730-MT-A
- 2nd source : QSI SBW-161(16X Combo)
- 3rd source : NEC CB2100A

1.3.7 Track Pad : Synaptics TM41PUM311-2

- Accurate positioning
- Low fatigue pointing action
- Low profile
- No moving part, high reliability
- Low power consumption
- Environmentally sealed
- Compact size

- Software configurable
- Low weight
- Operating temperature: 0 to 60 degree C
- Operating humidity : 5%-95% relative humidity, non condensing
- Storage temperature: -40 to +65 degree C
- ESD: 15KV applied to front surface SEE ESD Testing specification PN 520-000270-01
- Power supply voltage : 5.0Voltage ± 10%
- Power supply current : 4.0mA max operating

1.3.8 Fan

- HY45J05-001

1.4 Power Management

The MiTAC 8080 system has built in several power saving modes to prolong the battery usage for mobile purpose. User can enable and configure different degrees of power management modes via ROM CMOS setup (booting by pressing F2 key). Following are the descriptions of the power management modes supported.

1.4.1 System Management Mode

1.4.1.1 Full On Mode

In this mode, each devices is running with the maximal speed. CPU clock is up to its maximum.

1.4.1.2 Doze Mode

In this mode, CPU will be toggling between on & stop grant mode either. The technology is clock throttling. This can save battery power without loosing much computing capability.

The CPU power consumption and temperature is lower in this mode.

1.4.1.3 Standby Mode

For more power saving, it turns of the peripheral components. In this mode, the following is the status of each device:

CPU: Stop grant
LCD: backlight off
HDD: spin down

1.4.1.4 Suspend to DRAM and HDD

The most chipset of the system is entering power down mode for more power saving. In this mode, the following is the status of each device:

Suspend to DRAM

- CPU: off
- NB: Partial off
- VGA: Suspend
- PCMCIA: Suspend
- Audio: off
- SDRAM: self Refresh

Suspend to HD

- All devices are stopped clock and power-down
- System status is saved in HDD
- All system status will be restored when powered on again

1.4.2 Other Power Management Functions

1.4.2.1 HDD & Video Access

System has the ability to monitor video and hard disk activity. User can enable monitoring video and/or hard disk individually. When there is no video and/or hard disk activity, system will enter next PMU state depending on the application. When the VGA activity monitoring is enabled, the performance of the system will have some impact.

1.5 Appendix 1: Intel 82801DBM ICH4-M GPIO Definitions

Pin Name	MUX Function	GPIO Function	Power Plane
GPIO0	CRT_IN#	GPI	MAIN
GPIO1	X	GPI	MAIN
GPIO2	INT_PIRQE#	GPI	MAIN
GPIO3	INT_PIRQF#	GPI	MAIN
GPIO4	INT_PIRQG#	GPI	MAIN
GPIO5	X	GPI	MAIN
GPIO6	AGP_BUSY#	GPI	MAIN
GPIO7	KB_US/JP#	GPI	MAIN
GPIO8	EXTSMI#	GPI	RESUME
GPIO11	SMBALERT#	GPI	RESUME
GPIO12	SCI#	GPI	RESUME
GPIO13	WAKE_UP#	GPI	RESUME
GPIO16	SIDE_OFF#	GPO	MAIN
GPIO17	PIDE_OFF#	GPO	MAIN
GPIO18	STOP_PCI	GPO	MAIN
GPIO19	SUSA#	GPO	MAIN
GPIO20	STOP_CPU	GPO	MAIN
GPIO21	X	GPO	MAIN
GPIO22	CPUPERF#	OD	MAIN

Pin Name	MUX Function	GPIO Function	Power Plane
GPIO23	X	O	MAIN
GPIO24	PCLKRUN#	GPIO	RESUME
GPIO25	X	GPIO	RESUME
GPIO27	X	GPIO	RESUME
GPIO28	X	GPIO	RESUME
GPIO32	WIRELESS_PD#	GPIO	MAIN
GPIO33	LCDID0	GPIO	MAIN
GPIO34	LCDID1	GPIO	MAIN
GPIO35	LCDID2	GPIO	MAIN
GPIO36	SIDE_IN#	GPIO	MAIN
GPIO37	ICH_SIDE_IN#	GPIO	MAIN
GPIO38	IDERST#	GPIO	MAIN
GPIO39	MINIPCI_ACT#	GPIO	MAIN
GPIO40	DEBIG_EN	GPIO	MAIN
GPIO41	SIDEDET	GPIO	MAIN
GPIO42	SPK_OFF	GPIO	MAIN
GPIO43	SIDERST#	GPIO	MAIN

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1.6 Appendix 2: MiTAC 8080 Product Specification

CPU	- Intel Banias Processor CPU Support 1.4GHz ~ 1.7GHz or above - FSB 400MHz
Chipset	- Montara-GM + ICH4-M
L2 Cache	- 1M
System BIOS	- Flash EPROM (Include System BIOS and VGA BIOS) - ACPI 1.0b; DMI 2.3.1 compliant(P)
Memory	- 0MB on board; Expandable to 1024MB - Expandable with combination of optional 128MB/256MB/512MB(P)memory - Two 200-pin DDR SDRAM Memory Module, PC 2100/1600 specifications
ROM Drive	- 24X CD ROM Drive - 8X DVD ROM Drive - 24X10x24 CD-RW or above - 16X10X8X24 Combo or above - 2X2X1X8X24X10X24 DVD Multi
HDD	- 2.5’’9.5 mm height: 20/30/40/60GB; Support Ultra DMA 66/100 - Reseller Exchangeable
Ext. FDD	- Support External FDD w/z USB I/F; 3.5" Format for 720KB/1.2MB/1.44MB
Display	- 14.1” XGA/SXGA+ TFT display; Resolution: 1024x768/1400x1050
Video Controller	- Integrate in Northbridge - Support Multi Monitor - Ultra AGP
Keyboard	- 19mm pitch/2.7mm stroke - Windows Logo Key x 1; Application Key x 1
Button	- 5x Easy Start Buttons (functions defined by user)I/ instant play for Audio CD When System off - 1xWireless RF ON/OFF
Pointing Device	- Glide pad with 6x buttons - Finger printer for option (P)
PCMCIA	- Type II x 1 - CardBus Support
Card Reader	- 4 in 1 card reader for (MS,SM,SD,MMC)

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Continued to the previous table

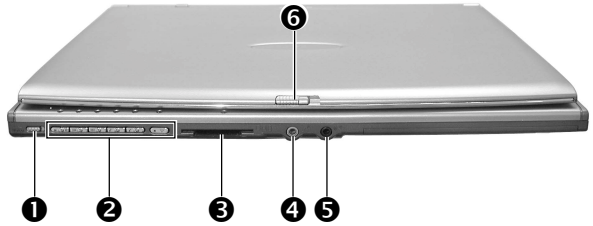
Audio System	- Sound Blaster Pro compatible - Built-in mono microphone - Support AC97 2.1 - 2X Speakers (2 Watt each)
I/O Port	- Standard USB2.0 port x 3 - RJ-11 port x 1 - RJ-45 port x 1 - IR port x1, complies with IrDA 1.1 - DC input x 1 - VGA monitor port x1 - Audio-out x 1 (S/PIDF) - Mic-in x 1 - IEEE1394a Port x 1 - S-Video Out Port (7 pins)x 1 (NTSC/PAL)
Communication	- Built-in 56Kbps V.90 MDC modem - Built-in 10/100 based-T LAN - Built-in antenna for Mini-PCI wireless communication
Power Supply	- 8-cell Li-ion (2200mAh/3.7V) Cylindrical Type - User swappable - Min Battery Life: 5 hrs (P) - Support Power on charge
AC Adapter	Universal AC adapter 60/70 W(P) ; Input: 100-240V, 50/60Hz AC
Dimensions	318x275 mm, thickness 25~30mm
Weight	2kg (P)
Accessories	Power Cord, AC Adapter, RJ-11 Phone Cable, Manual, System Driver CD-Title
Architecture	Support PC2001 Specification, Designed for Windows 2000 & Windows XP
Options	128MB/256MB/512MB DDR SDRAM, 8-cell Li-ION Battery Pack, AC Adapter w/o Power Cord, Notebook Carry Bag

2. System View and Disassembly

2.1 System View

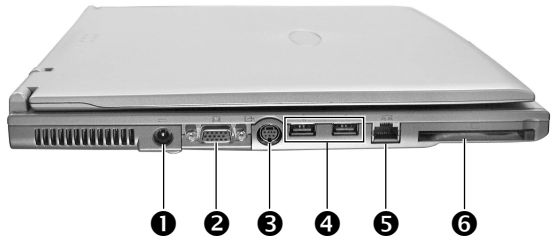
2.1.1 Front View

❶ Hold Switch
❷ Audio Play Button
❸ Card Reader Slot
❹ Audio Output
❺ Microphone Input
❻ Top Cover Latch



2.1.2 Left-side View

❶ Power Jack
❷ VGA Port
❸ S-Video Output Connector
❹ USB Port
❺ RJ-45 Connector
❻ PC Card Slot

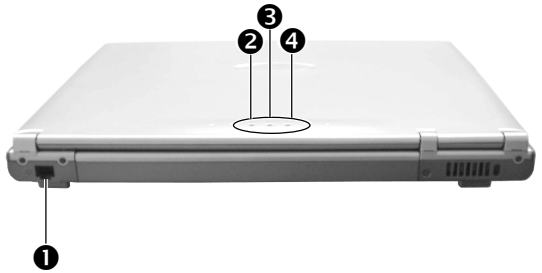


2.1.3 Right-side View

❶ CD-ROM/DVD-ROM Drive
❷ USB Port
❸ 1394 Port
❹ IR Module

2.1.4 Rear View

❶ RJ-11 Connector
❷ Battery Charging LED Indicator
❸ Battery Power LED Indicator
❹ AC Power LED Indicator



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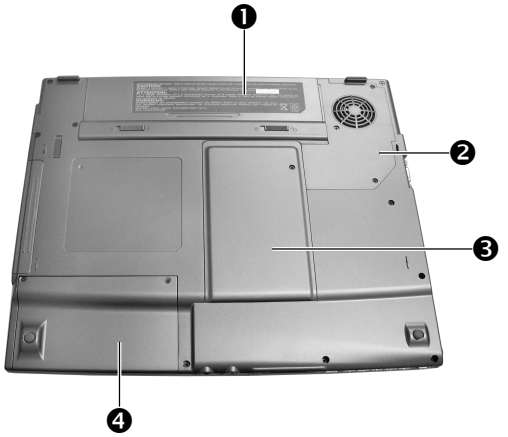
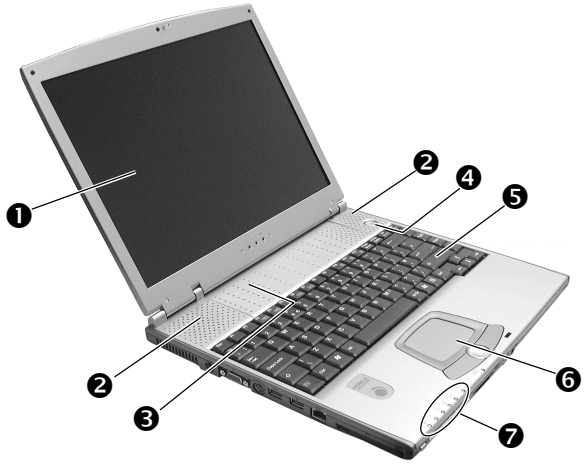
2.1.5 Bottom View



❶ Extend SO-DIMM Cover
❷ CPU Cover
❸ Hard Disk Drive Cover
❹ Battery Pack

2.1.6 Top-open View



❶ LCD Screen
❷ Stereo Speaker
❸ Battery Pack
❹ Power Button
❺ Keyboard
❻ Touch Pad
❼ Device Indicators

2.2 System Disassembly

The section discusses at length each major component for disassembly/reassembly and show corresponding illustrations. Use the chart below to determine the disassembly sequence for removing components from the notebook.

NOTE: *1. Before you start to install/replace these modules, disconnect all peripheral devices and make sure the notebook is not turned on or connected to AC power.*

2. During disassembly, 1) Label each cable as you disconnect it, noting its position and routing;
2) Keep all the screws.

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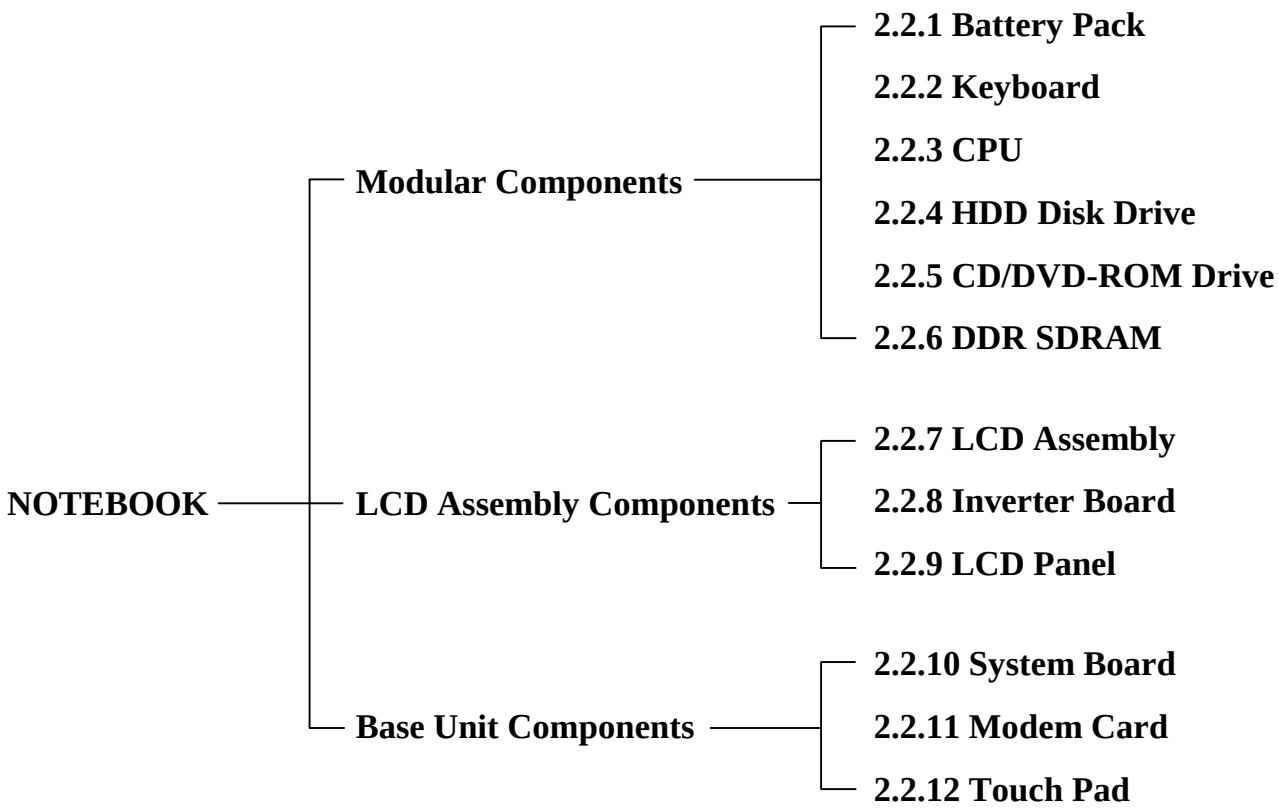

2.2.1 Battery Pack

Disassembly

1. Carefully put the notebook upside down.
2. Pull the battery pack out of the compartment (❷) while sliding and holding the release levers outwards to the "unlock" (🔓) position (❶). (Figure 2-1)

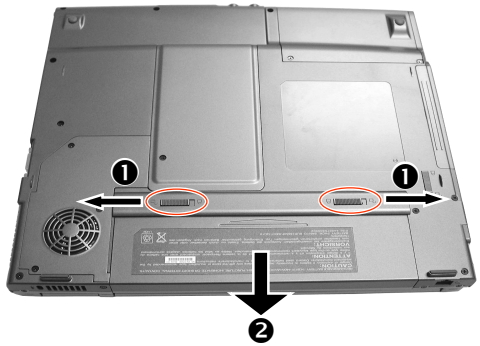

Figure 2-1 Remove the battery pack

Reassembly

1. Replace the battery pack into the compartment. The battery pack should be correctly connected when you hear a clicking sound.
2. Slide the release lever to the "lock" (🔒) position.

2.2.2 Keyboard

Disassembly

1. Remove the battery pack. (See section 2.2.1 Disassembly)
2. Open the top cover. Remove three screws fastening the keyboard. (Figure 2-2)

Figure 2-2 Remove three screws

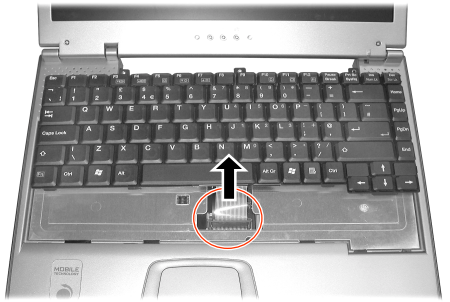

Figure 2-3 Disconnect the cable

4. Disconnect the cable from system board. (Figure 2-3)

Reassembly

1. Reconnect the keyboard cable
2. Replace the keyboard and secure with three screws.
2. Replace the battery pack. (See section 2.2.1 Reassembly)

2.2.3 CPU

Disassembly

1. Carefully put the notebook upside down.
2. Remove the battery pack. (See section 2.2.1 Disassembly)
3. Remove five screws fastening the heatsink and DDR SDRAM's compartment covers. (Figure 2-4)

Figure 2-4 Remove five screws

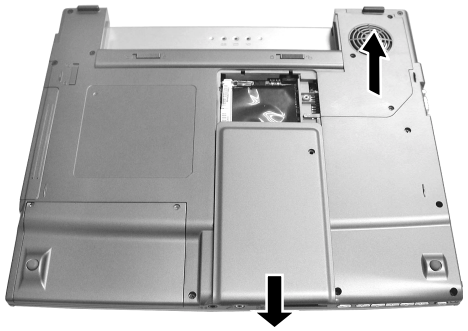

Figure 2-5 Remove the CPU compartment cover

4. First, sliding out the DDR SDRAM compartment cover . And then you can easy to remove the CPU compartment cover. (Figure 2-5)

5. Remove four spring screws fastening the heatsink. (Figure 2-6)

Figure 2-6 Unscrew four screws

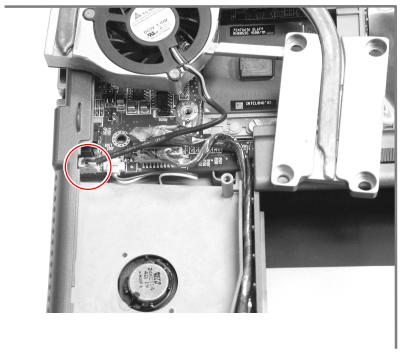

Figure 2-7 Disconnect the fan's cord

6. Disconnect the fan's power cord to detach the heatsink from the CPU compartment. (Figure 2-7)

7. Loosen the screw by a flat screwdriver,upraise the CPU socket to unlock the CPU. (Figure 2-8)

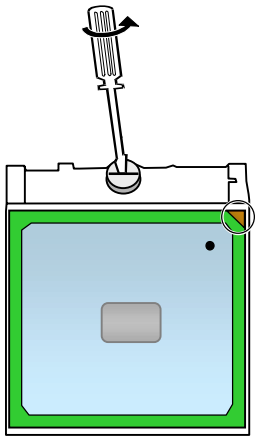

Figure 2-8 Remove the CPU

Reassembly

1. Carefully, align the arrowhead corner of the CPU with the beveled corner of the socket, then insert CPU pins into the holes. Tighten the screw by a flat screwdriver to locking the CPU.
2. Connect the fan's power cord to the system board, fit the heatsink onto the top of the CPU and secure with four spring screws.
3. First, replace the heatsink compartment cover. Then fit the DDR SDRAM compartment cover and secure them with five screws.
4. Replace the battery pack. (See section 2.2.1 Reassembly)

2.2.4 HDD Module

Disassembly

1. Carefully put the notebook upside down.
2. Remove the battery pack. (See section 2.2.1 Disassembly)
3. Remove two screws fastening the HDD compartment cover. Then sliding it outward. (Figure 2-9)

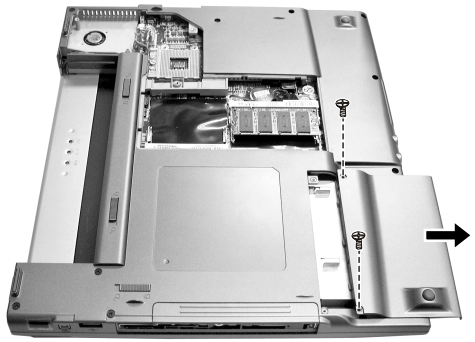

Figure 2-9 Remove HDD module

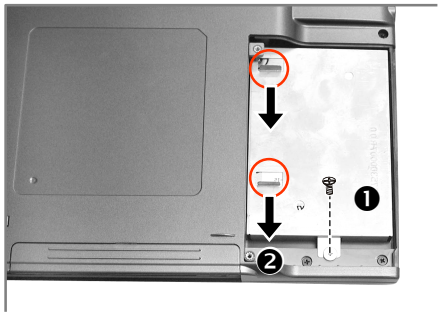

Figure 2-10 Disassemble the hard disk

4. To remove the hard disk drive, first unscrew one screw (❶), then sliding out the hard disk drive (❷). (Figure 2-10)

5. Unscrew four screws to remove the hard disk drive from the holding. (Figure 2-11)

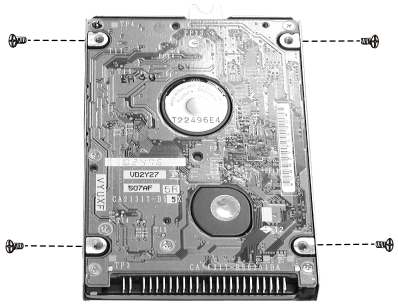

Figure 2-11 Free the hard disk

Reassembly

1. Fit the hard disk drive into the holding and secure with four screws.
2. Replace the hard disk drive into compartment and secure with one screws.
3. Replace the HDD’s cover and secure with two screws.
4. Replace the keyboard. (See section 2.2.2 Reassembly)
5. Then replace battery pack. (See section 2.2.1 Reassembly)

2.2.5 CD/DVD-ROM Drive

Disassembly

1. Carefully put the notebook upside down.
2. Remove the battery pack. (See section 2.2.1 Disassembly)
3. Pull the CD/DVD-ROM out of the compartment (❷) while sliding and holding the release lever outwards to the "unlock" ( ) position (❶). (Figure 2-12)

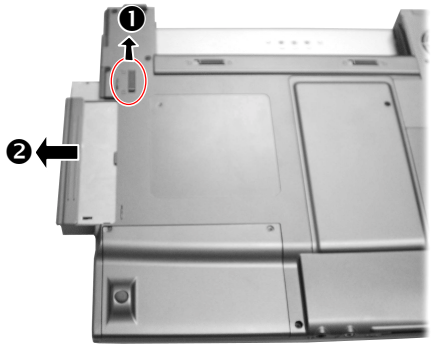

Figure 2-12 Remove CD/DVD-ROM

Reassembly

1. Push the battery pack into the compartment. The battery pack should be correctly connected when you hear a clicking sound.
2. Ensure the release lever being the "lock" ( ) position.
3. Replace the battery pack. (See section 2.2.1 Reassembly)

2.2.6 DDR SDRAM

Disassembly

1. Carefully put the notebook upside down.
2. Remove the battery pack. (See section 2.2.1 Disassembly)
3. Remove one screw to access the DDR-SARAM's socket. (Figure 2-13)
4. Pull the retaining clips outwards (❶) and remove the SO-DIMM (❷). (Figure 2-14)

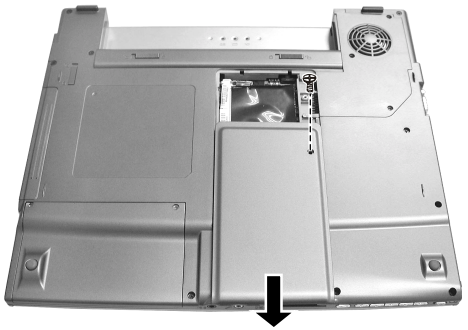

Figure 2-13 Remove the compartment cover

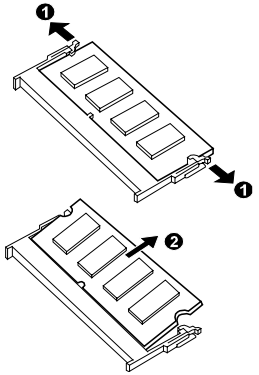

Figure 2-14 Remove the DDR SDRAM

Reassembly

1. To install the DDR-SDRAM, match the its notched part with the socket's projected part and firmly insert the SDRAM into the socket at 20-degree angle. Then push down until the retaining clips lock the SO-DIMM into position.
2. Replace the DDR-SDRAM compartment cover and secure with one screw.
3. Replace the battery pack. (See section 2.2.1 Reassembly)

2.2.7 LCD Assembly

Disassembly

1. Carefully put the notebook upside down.
2. Remove the battery pack. (See section 2.2.1 Disassembly)
3. Remove nine screws. (Figure 2-15)
4. Remove the heatsink. (See the steps 3, 4, 5 of section 2.2.3 Disassembly)
5. Disconnect two wires from system board in heatsink compartment. (Figure 2-16)

Figure 2-15 Unscrew nine screws

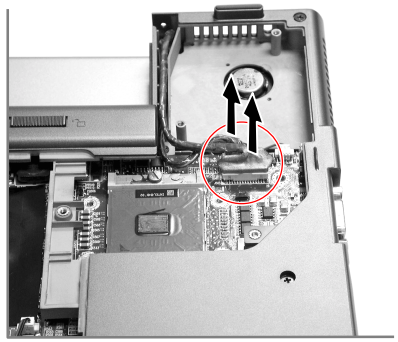

Figure 2-16 Disconnect two wires

6. Carefully turnover the notebook. Close the top cover, remove three hinge covers. Then lift up the LCD ASSY. (Figure 2-17)

Figure 2-17 Remove the hinge covers

Reassembly

1. Replace the LCD Assembly and reconnect two wires.
2. Replace the heatsink, heatsink compartment cover and DDR SDRAM compartment cover. (See the step 2, 3 of section 2.2.3 Reassembly)
3. Fasten the LCD Assembly by four screws.
4. Fit three hinge covers.
5. Replace the battery pack. (See section 2.2.1 Reassembly)

2.2.8 Inverter Board

Disassembly

1. Carefully put the notebook upside down.
2. Remove the battery pack. (See section 2.2.1 Disassembly)
3. Remove the LCD Assembly. (See section 2.2.7 Disassembly)
4. Remove the five rubber pads and five screws. (figure 2-18)
5. Insert a flat screwdriver to the lower part of the top cover and gently pry the frame out. Repeat the process until the cover is completely separated from the housing.
6. Disconnect one wire from inverter board and remove two screws fastening the inverter board. (Figure 2-19)

Figure 2-18 Unscrew five screws

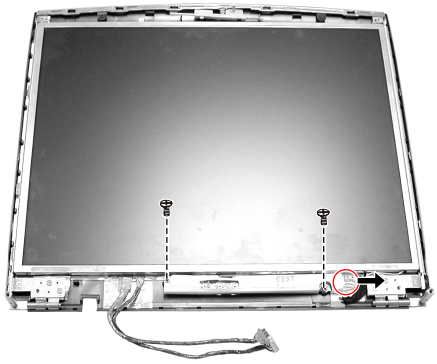

Figure 2-19 Disconnect one cables

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Reassembly

1. Fit the inverter board back into place and secure with two screws, and reconnect the wire to the inverter board. .
2. Fit the LCD top cover back into the housing and secure with five screws and five rubber pads
3. Replace the LCD Assembly. (See section 2.2.7 Reassembly)
4. Replace the battery pack. (See section 2.2.1 Reassembly)

2.2.9 LCD Panel

Disassembly

1. Carefully put the notebook upside down.
2. Remove the battery pack. (See section 2.2.1 Disassembly)
3. Remove the LCD Assembly. (See section 2.2.7 Disassembly)
4. Remove the inverter board. (See section 2.2.8 Disassembly)
5. Remove four screws. And then lift up LCD panel. (Figure 2-20)
6. To free the LCD panel, remove six screws. (Figure 2-21)

Figure 2-20 Unscrew four screws

Figure 2-21 Unscrew six screws

Reassembly

1. Attach the LCD panel holding to panel and secure with six screws.
2. Fit the LCD panel into place and secure with four screws.
3. Replace the inverter board. (See section 2.2.8 Reassembly)
4. Replace the LCD assembly. (See section 2.2.7 Reassembly)
5. Replace the battery pack. (See section 2.2.1 Reassembly)

2.2.10 System Board

Disassembly

1. Carefully put the notebook upside down.
2. Remove the battery pack. (See section 2.2.1 Disassembly)
3. Remove the keyboard, CPU, hard disk drive, CD/DVD-ROM drive, DDR-SDRAM and LCD Assembly. (See the previous sections Disassembly)
4. Remove nine screws on the bottom of notebook. (Figure 2-22)
5. Disconnect the speaker's cord from system board in the heatsink compartment. (Figure 2-23)

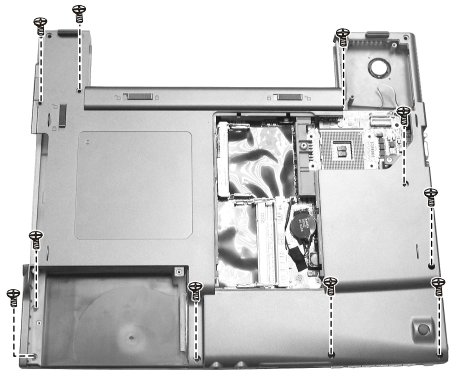

Figure 2-22 Unscrew nine screws

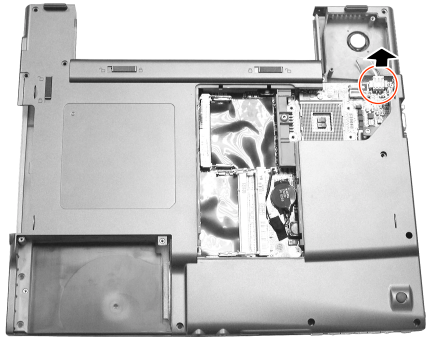

Figure 2-23 Disconnect the cord

6. Carefully, turnover the notebook. Then remove seven screws. (Figure 2-24)

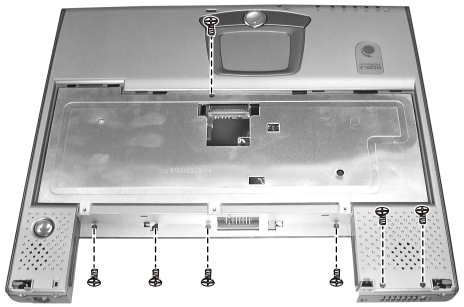

Figure 2-24 Unscrew seven screws

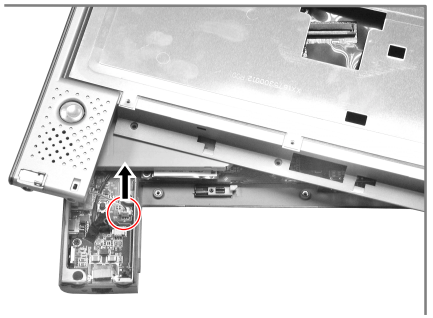

Figure 2-25 Disconnect the cord

7. Lift notebook up carefully. Disconnect the speaker’s cord. (Figure 2-25)

8. Disconnect the touch pad's cable. Then lift up the system top cover. (Figure 2-26)

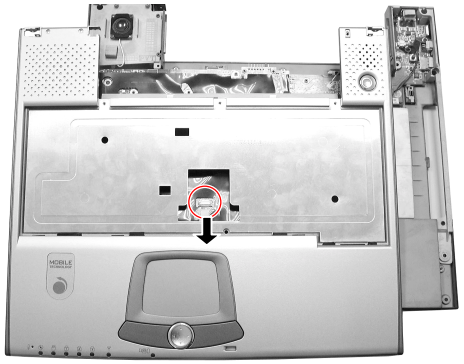

Figure 2-26 Disconnect the cable

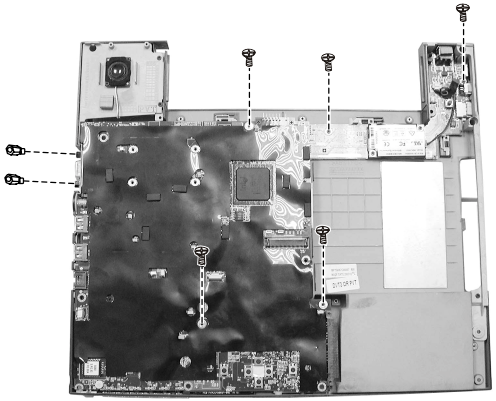

Figure 2-27 Unscrew screws and hex nuts

9. Remove five screws and two hex nuts beside the VGA port. Now you can lift up system board from housing. (Figure 2-27)

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Reassembly

1. Fit the system board back into housing and secure with five screws and two hex nuts.
2. Reconnect the touch pad’s cable to system board.
3. Reconnect the speaker’s cord to system board.
4. Then fit the system top cover and secure with seven screws.
5. Up the notebook upside down. Reconnect the other speaker’s cord.
6. Fasten the housing by nine screws.
7. Reassemble the notebook. (See the previous sections Reassembly)

2.2.11 Modem Card

Disassembly

1. Carefully put the notebook upside down.
2. Remove the battery pack. (See section 2.2.1 Disassembly)
3. Remove the keyboard, CPU, hard disk drive, CD/DVD-ROM drive, DDR-SDRAM and LCD Assembly. (See the previous sections Disassembly)
4. Remove the system top cover. (See the steps 3 to 7 of section 2.2.10 Disassembly)
5. Remove two screws fastening the modem card. disconnect cord from system board. (Figure 2-28)

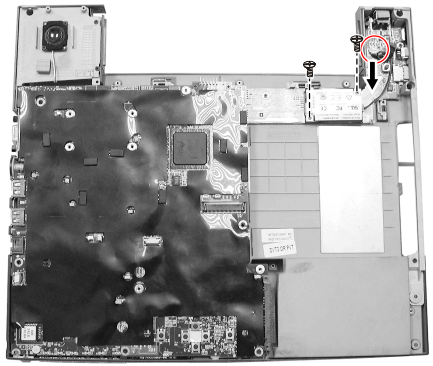

Figure 2-28 Remove the modem card

Reassembly

1. Reconnect the cord. Then fit the modem card and secure with two screws.
2. Reassemble the notebook. (See the previous sections Reassembly)

2.2.12 Touch Pad

Disassembly

1. Carefully put the notebook upside down.
2. Remove the battery pack. (See section 2.2.1 Disassembly)
3. Remove the keyboard, CPU, hard disk drive, CD/DVD-ROM drive, DDR-SDRAM and LCD Assembly. (See the previous sections Disassembly)
4. Remove the system top cover. (See the steps 3 to 7 of section 2.2.10 Disassembly)
5. Remove four screws fastening the touch pad bracket. Then remove it. (Figure 2-29)
6. Remove the click holder and touch pad panel. (Figure 2-30)

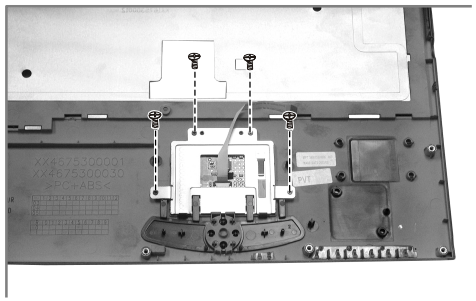

Figure 2-29 Disconnect the cable

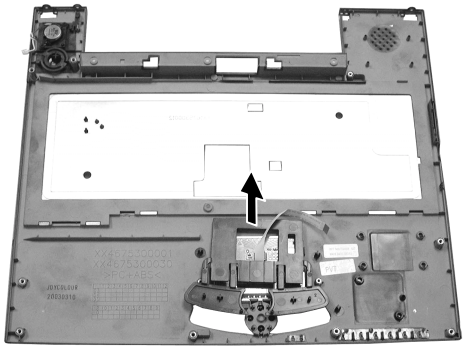

Figure 2-30 Unscrew screws and hex nuts

Reassembly

1. Fit the touch pad panel and click holder
2. Then fit the touch pad bracket and secure with four screws.
3. Reassemble the notebook. (See the previous sections Reassembly)

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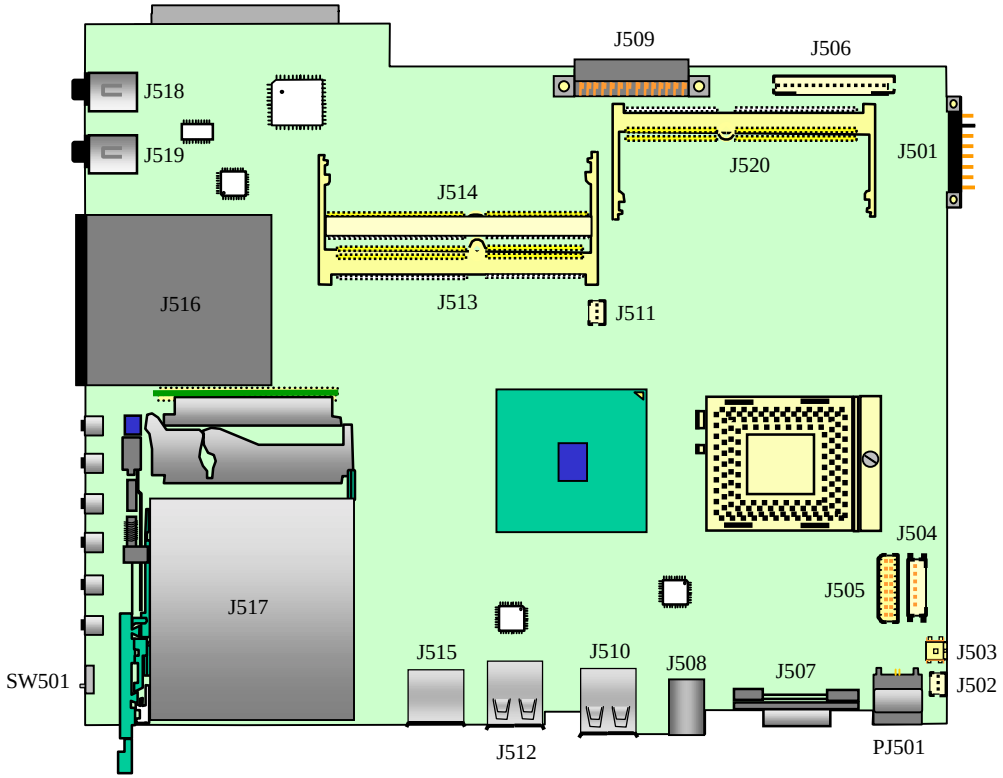
3. Definition & Location of Connectors / Switches

3.1 Main Board (Side A) – 1



- **PJ501 : AC Power Jack**
- **J501 : Battery Connector**
- **J502 : Fan Connector**
- **J503 : Left Internal Speaker Jack**
- **J504 : Inverter Board Connector**
- **J505 : LCD Connector**
- **J506 : DC to DC Board Connector**
- **J507 : External VGA Connector**
- **J508 : S-Video Connector**
- **J509 : Secondary EIDE Connector**
- **J510 : USB Port Connector**

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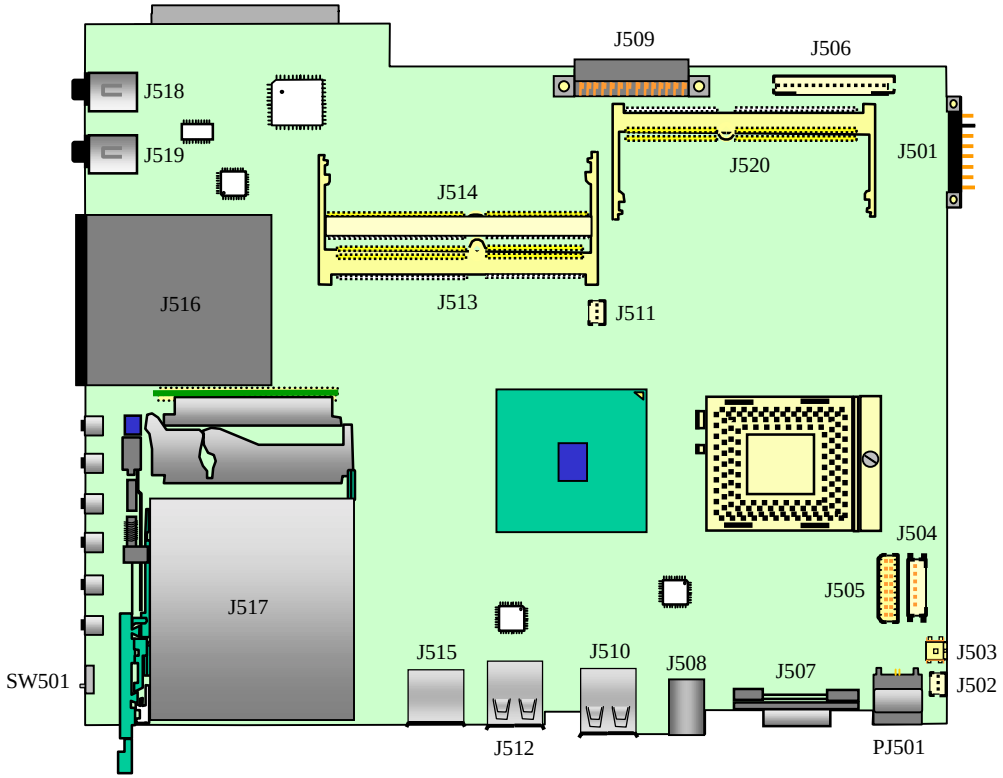
3. Definition & Location of Connectors / Switches

3.1 Main Board (Side A) – 2



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- **J511 : RTC Battery Connector**
- **J512 : USB Port Connector**
- **J513, J514 : DDR SO-DIMM Module Socket**
- **J515 : RJ-45 Connector**
- **J516 : Card Reader Socket**
- **J517 : PCMCIA Card Socket**
- **J518 : Line Out Jack**
- **J519 : External Microphone Jack**
- **J520 : Mini PCI Socket**
- **SW501 : Audio DJ Button**

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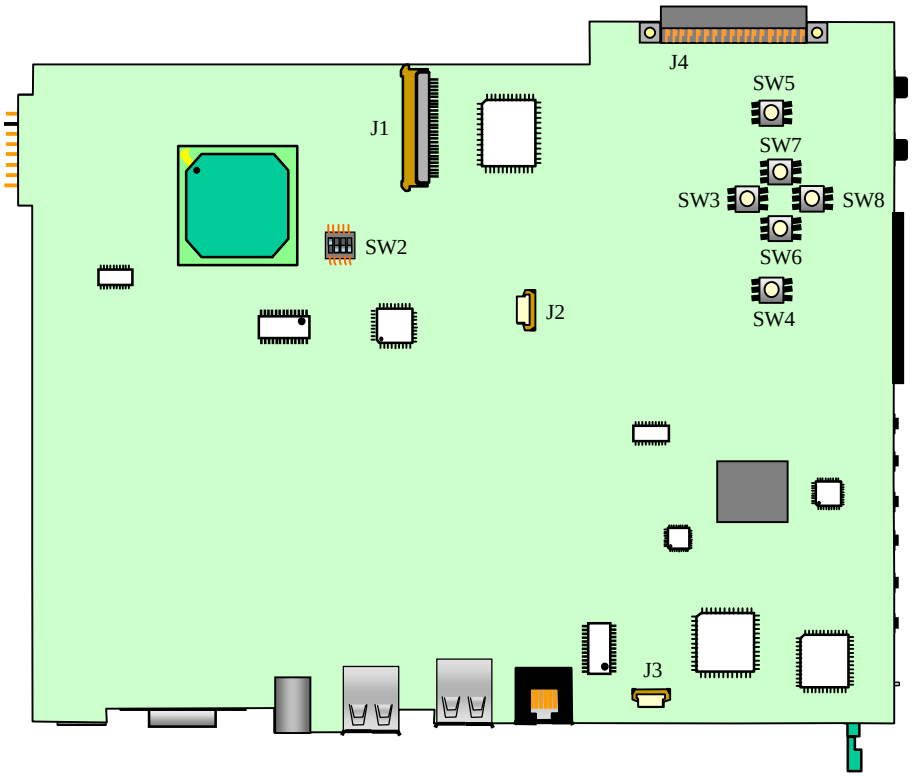
3. Definition & Location of Connectors/ Switches

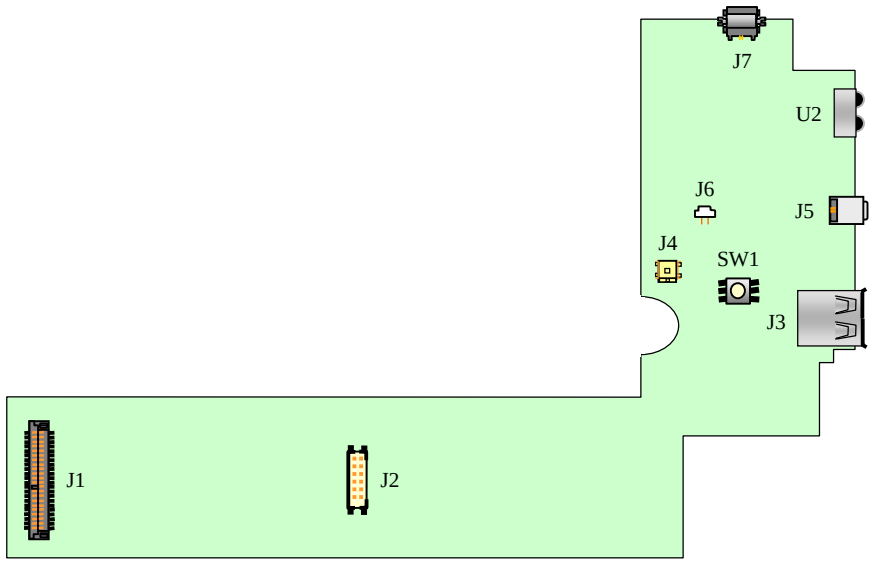
3.1 Main Board (Side B)



- **J1 : Internal Keyboard Connector**
- **J2 : Touch-Pad Connector**
- **J3 : MDC Jump Wire Connector**
- **J4 : Primary EIDE Connector**
- **SW2 : LCD ID Select Switch**
- **SW3, SW8 : SCRL Up / Down Switch**
- **SW6, SW7 : SCRL Left / Right Switch**
- **SW4, SW5 : Left / Right Switch**

3. Definition & Location of Connectors / Switches

3.2 DC to DC Board



- **J1 : DC to DC Board Connector**
- **J2 : Modem Daughter Board (MDC) Connector**
- **J3 : USB Port Connector**
- **J4 : Right Internal Speaker Connector**
- **J5 : IEEE1394 Port Connector**
- **J6 : MDC Jump Wire Connector**
- **J7 : RJ-11 Connector**
- **U2 : FIR Module**
- **SW2 : Power Button**

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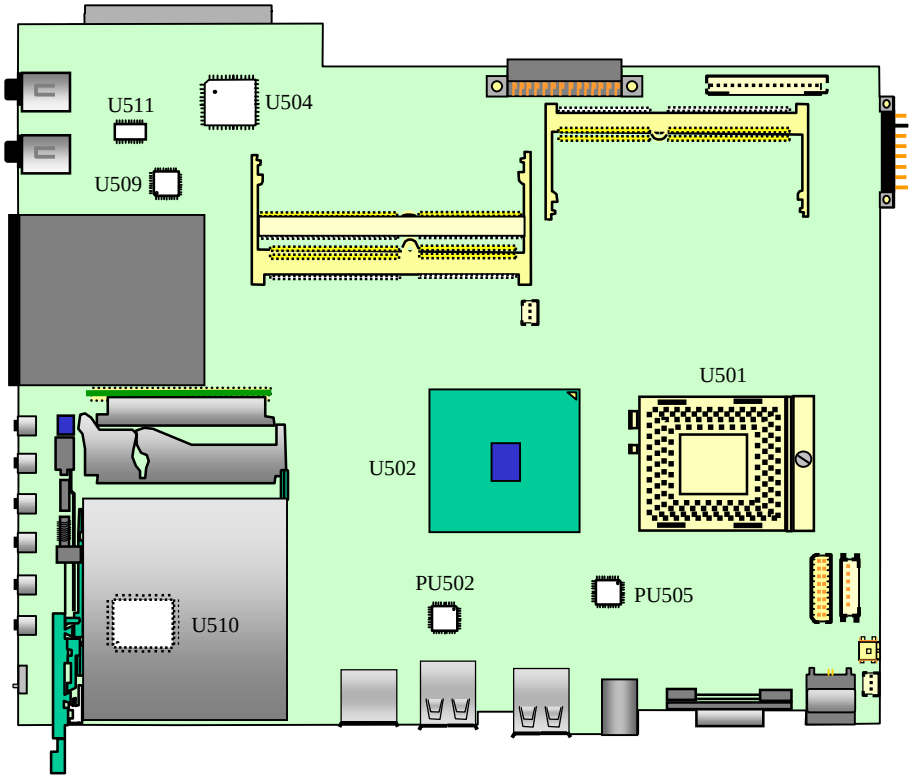
4. Definition & Location of Major Components

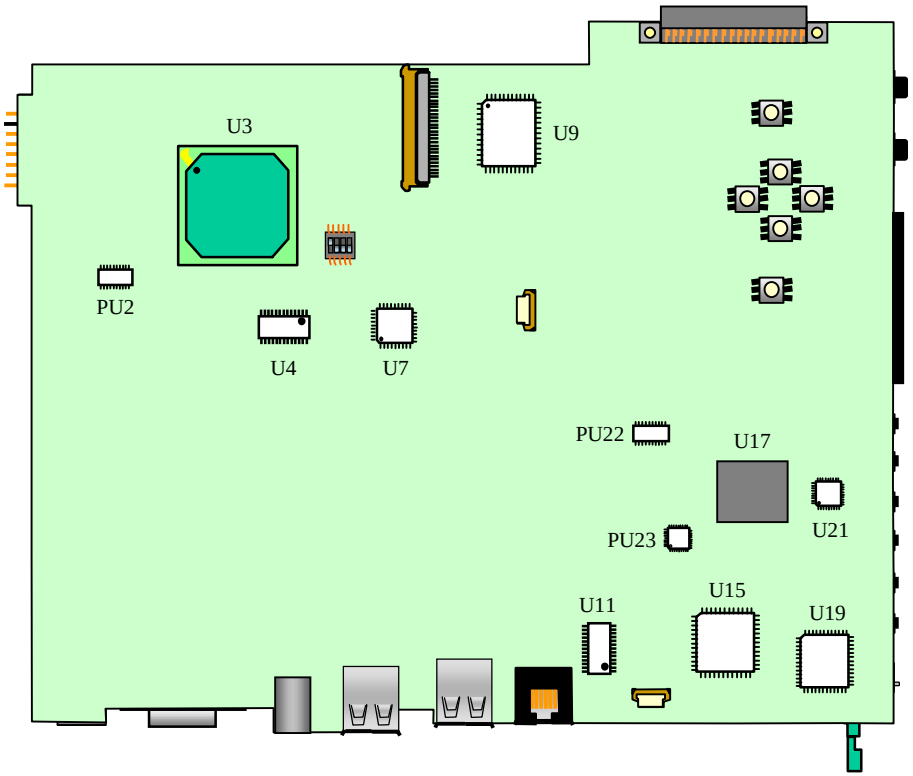
4.1 Main Board (Side A)



- **U501 : Intel Banais Micro-FCPGA Processor**
- **U502 : Intel 82855GM GMCH**
- **U504 : H8/F3437 Micro Controller**
- **U509 : STAC9570 Audio Codec**
- **U510 : PC87393 Super I/O Controller**
- **U511 : APA2020A Audio Amplifier**
- **PU502 : LTC3728L +1.05V / +1.2V Voltage Converter**
- **PU505 : MAX1907 CPU Core Voltage Converter**

4. Definition & Location of Major Components

4.1 Main Board (Side B)



- **U3 : Intel 82801DBM ICH4-M**
- **U4 : PLL207-151 Clock Generator**
- **U7 : CH7011A TV Encode**
- **U9 : VT6307 IEEE1394 Controller**
- **U11 : LF-H80P LAN Buffer**
- **U15 : VT6105-LOM LAN Controller**
- **U17 : CB710 CardBus & Card Reader Controller**
- **U19 : System Flash BIOS**
- **U21 : TPS2211A Power Switch**
- **PU2 : TL594C Battery Charging**
- **PU22 : +1.25V_DDR/+2.5V_DDR Voltage Converter**
- **PU23 : LTC3728L +3V/+5V Voltage Converter**

5. Pin Descriptions of Major Components

5.1 Intel Pentium M Processor

Signal Name	Type	Description
A[31:3]#	I/O	A[31:3]# (Address) define a 2 32 -byte physical memory address space. In sub-phase 1 of the address phase, these pins transmit the address of a transaction. In sub-phase 2, these pins transmit transaction type information. These signals must connect the appropriate pins of both agents on the Intel Pentium M processor system bus. A[31:3]# are source synchronous signals and are latched into the receiving buffers by ADSTB[1:0]#. Address signals are used as straps which are sampled before RESET# is deasserted.
A20M#	I	If A20M# (Address-20 Mask) is asserted, the processor masks physical address bit 20 (A20#) before looking up a line in any internal cache and before driving a read/write transaction on the bus. Asserting A20M# emulates the 8086 processor's address wrap-around at the 1-Mbyte boundary. Assertion of A20M# is only supported in real mode. A20M# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction.
ADS#	I/O	ADS# (Address Strobe) is asserted to indicate the validity of the transaction address on the A[31:3]# and REQ[4:0]# pins. All bus agents observe the ADS# activation to begin parity checking, protocol checking, address decode, internal snoop, or deferred reply ID match operations associated with the new transaction.
ADSTB[1:0]#	I/O	Address strobes are used to latch A[31:3]# and REQ[4:0]# on their rising and falling edges. Strobes are associated with signals as shown below. **Signals** / **Associated Strobe** REQ[4:0]#, A[16:3]# — ADSTB[0]# A[31:17]# — ADSTB[1]#
BCLK[1:0]	I	The differential pair BCLK (Bus Clock) determines the system bus frequency. All processor system bus agents must receive these signals to drive their outputs and latch their inputs.
BNR#	I/O	BNR# (Block Next Request) is used to assert a bus stall by any bus agent that is unable to accept new bus transactions. During a bus stall, the current bus owner cannot issue any new transactions.
BPM[2:0]# **BPM[3]**	O I/O	BPM[3:0]# (Breakpoint Monitor) are breakpoint and performance monitor signals. They are outputs from the processor that indicate the status of breakpoints and programmable counters used for monitoring processor performance. BPM[3:0]# should connect the appropriate pins of all Intel Pentium M processor system bus agents. This includes debug or performance monitoring tools.

Signal Name	Type	Description
BPRI#	I	BPRI# (Bus Priority Request) is used to arbitrate for ownership of the processor system bus. It must connect the appropriate pins of both processor system bus agents. Observing BPRI# active (as asserted by the priority agent) causes the other agent to stop issuing new requests, unless such requests are part of an ongoing locked operation. The priority agent keeps BPRI# asserted until all of its requests are completed, then releases the bus by deasserting BPRI#.
BR0#	I/O	BR0# is used by the processor to request the bus. The arbitration is done between the Intel Pentium M processor (Symmetric Agent) and the MCH-M (High Priority Agent) of the Intel 855PM or Intel 855GM chipset.
COMPP3:0]	Analog	COMP[3:0] must be terminated on the system board using precision (1% tolerance) resistors. Refer to the platform design guides for more implementation details.
D[63:0]#	I/O	D[63:0]# (Data) are the data signals. These signals provide a 64-bit data path between the processor system bus agents, and must connect the appropriate pins on both agents. The data driver asserts DRDY# to indicate a valid data transfer. D[63:0]# are quad-pumped signals and will thus be driven four times in a common clock period. D[63:0]# are latched off the falling edge of both DSTBP[3:0]# and DSTBN[3:0]#. Each group of 16 data signals correspond to a pair of one DSTBP# and one DSTBN#. The following table shows the grouping of data signals to data strobes and DINV#. **Quad-Pumped Signal Groups** **Data Group** / **DSTBN#/DSTBP#** / **DINV#** D[15:0]# — 0 — 0 D[31:16]# — 1 — 1 D[47:32]# — 2 — 2 D[63:48]# — 3 — 3 Furthermore, the DINV# pins determine the polarity of the data signals. Each group of 16 data signals corresponds to one DINV# signal. When the DINV# signal is active, the corresponding data group is inverted and therefore sampled active high.
DBR#	O	DBR# (Data Bus Reset) is used only in processor systems where no debug port is implemented on the system board. DBR# is used by a debug port interposer so that an in-target probe can drive system reset. If a debug port is implemented in the system, DBR# is a no connect. DBR# is not a processor signal.

5.1 Intel Pentium M Processor

Signal Name	Type	Description
DBSY#	I/O	DBSY# (Data Bus Busy) is asserted by the agent responsible for driving data on the processor system bus to indicate that the data bus is in use. The data bus is released after DBSY# is deasserted. This signal must connect the appropriate pins on both processor system bus agents.
DEFER#	I	DEFER# is asserted by an agent to indicate that a transaction cannot be guaranteed in-order completion. Assertion of DEFER# is normally the responsibility of the addressed memory or Input/Output agent. This signal must connect the appropriate pins of both processor system bus agents.
DINV[3:0]#	I/O	DINV[3:0]# (Data Bus Inversion) are source synchronous and indicate the polarity of the D[63:0]# signals. The DINV[3:0]# signals are activated when the data on the data bus is inverted. The bus agent will invert the data bus signals if more than half the bits, within the covered group, would change level in the next cycle. **DINV[3:0]# Assignment To Data Bus** Bus Signal / Data Bus Signals: DINV[3]# — D[63:48]# DINV[2]# — D[47:32]# DINV[1]# — D[31:16]# DINV[0]# — D[15:0]#
DPSLP#	I	DPSLP# when asserted on the platform causes the processor to transition from the Sleep state to the Deep Sleep state. In order to return to the Sleep state, DPSLP# must be deasserted. DPSLP# is driven by the ICH4-M component and also connects to the MCH-M component of the Intel 855PM or Intel 855GM chipset.
DRDY#	I/O	DRDY# (Data Ready) is asserted by the data driver on each data transfer, indicating valid data on the data bus. In a multi-common clock data transfer, DRDY# may be deasserted to insert idle clocks. This signal must connect the appropriate pins of both processor system bus agents.
DSTBN[3:0]#	I/O	Data strobe used to latch in D[63:0]#. Signals / Associated Strobe: D[15:0]#, DINV[0]# — DSTBN[0]# D[31:16]#, DINV[1]# — DSTBN[1]# D[47:32]#, DINV[2]# — DSTBN[2]# D[63:48]#, DINV[3]# — DSTBN[3]#
DSTBP[3:0]#	I/O	Data strobe used to latch in D[63:0]#. Signals / Associated Strobe: D[15:0]#, DINV[0]# — DSTBP[0]# D[31:16]#, DINV[1]# — DSTBP[1]# D[47:32]#, DINV[2]# — DSTBP[2]# D[63:48]#, DINV[3]# — DSTBP[3]#

Signal Name	Type	Description
DPWR#	I	DPWR# is a control signal from the Intel 855PM and Intel 855GM chipsets used to reduce power on the Intel Pentium M data bus input buffers.
FERR#/PBE#	O	FERR# (Floating-point Error)/PBE#(Pending Break Event) is a multiplexed signal and its meaning is qualified by STPCLK#. When STPCLK# is not asserted, FERR#/PBE# indicates a floating point when the processor detects an unmasked floating-point error. FERR# is similar to the ERROR# signal on the Intel 80387 coprocessor, and is included for compatibility with systems using MS-DOS* type floating-point error reporting. When STPCLK# is asserted, an assertion of FERR#/PBE# indicates that the processor has a pending break event waiting for service. The assertion of FERR#/PBE# indicates that the processor should be returned to the Normal state. When FERR#/PBE# is asserted, indicating a break event, it will remain asserted until STPCLK# is deasserted. Assertion of PREQ# when STPCLK# is active will also cause an FERR# break event.
GTLREF	I	GTLREF determines the signal reference level for AGTL+ input pins. GTLREF should be set at 2/3 V_{CCP}. GTLREF is used by the AGTL+ receivers to determine if a signal is a logical 0 or logical 1.
HIT# **HITM#**	I/O I/O	HIT# (Snoop Hit) and HITM# (Hit Modified) convey transaction snoop operation results. Either system bus agent may assert both HIT# and HITM# together to indicate that it requires a snoop stall, which can be continued by reasserting HIT# and HITM# together.
IERR#	O	IERR# (Internal Error) is asserted by a processor as the result of an internal error. Assertion of IERR# is usually accompanied by a SHUTDOWN transaction on the processor system bus. This transaction may optionally be converted to an external error signal (e.g., NMI) by system core logic. The processor will keep IERR# asserted until the assertion of RESET#, BINIT#, or INIT#.
IGNNE#	I	IGNNE# (Ignore Numeric Error) is asserted to force the processor to ignore a numeric error and continue to execute noncontrol floating-point instructions. If IGNNE# is deasserted, the processor generates an exception on a noncontrol floating-point instruction if a previous floating-point instruction caused an error. IGNNE# has no effect when the NE bit in control register 0 (CR0) is set. IGNNE# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction.
REQ[4:0]#	I/O	REQ[4:0]# (Request Command) must connect the appropriate pins of both processor system bus agents. They are asserted by the current bus owner to define the currently active transaction type. These signals are source synchronous to ADSTB[0]#.

5.1 Intel Pentium M Processor

Signal Name	Type	Description
INIT#	I	INIT# (Initialization), when asserted, resets integer registers inside the processor without affecting its internal caches or floating-point registers. The processor then begins execution at the power on Reset vector configured during power on configuration. The processor continues to handle snoop requests during INIT# assertion. INIT# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output Write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction. INIT# must connect the appropriate pins of both processor system bus agents. If INIT# is sampled active on the active to inactive transition of RESET#, then the processor executes its Built-in Self-Test (BIST)
LINT[1:0]	I	LINT[1:0] (Local APIC Interrupt) must connect the appropriate pins of all APIC Bus agents. When the APIC is disabled, the LINT0 signal becomes INTR, a maskable interrupt request signal, and LINT1 becomes NMI, a nonmaskable interrupt. INTR and NMI are backward compatible with the signals of those names on the Pentium processor. Both signals are asynchronous. Both of these signals must be software configured using BIOS programming of the APIC register space and used either as NMI/INTR or LINT[1:0]. Because the APIC is enabled by default after Reset, operation of these pins as LINT[1:0] is the default configuration.
LOCK#	I/O	LOCK# indicates to the system that a transaction must occur atomically. This signal must connect the appropriate pins of both processor system bus agents. For a locked sequence of transactions, LOCK# is asserted from the beginning of the first transaction to the end of the last transaction. When the priority agent asserts BPRI# to arbitrate for ownership of the processor system bus, it will wait until it observes LOCK# deasserted. This enables symmetric agents to retain ownership of the processor system bus throughout the bus locked operation and ensure the atomicity of lock.
PRDY#	O	Probe Ready signal used by debug tools to determine processor debug readiness.
PREQ#	I	Probe Request signal used by debug tools to request debug operation of the processor.
PROCHOT#	O	PROCHOT# (Processor Hot) will go active when the processor temperature monitoring sensor detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit has been activated, if enabled. This signal may require voltage translation on the motherboard.
PSI#	O	Processor Power Status Indicator signal. This signal is asserted when the processor is in a lower state (Deep Sleep and Deeper Sleep).

Signal Name	Type	Description
PWRGOOD	I	PWRGOOD (Power Good) is a processor input. The processor requires this signal as a clean indication that the clocks and power supplies are stable and within their specifications. 'Clean' implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high state. PWRGOOD can be driven inactive at any time, but clocks and power must again be stable before a subsequent rising edge of PWRGOOD. The PWRGOOD signal must be supplied to the processor; it is used to protect internal circuits against voltage sequencing issues. It should be driven high throughout the boundary scan operation.
ITP_CLK[1:0]	I	ITP_CLK[1:0] are copies of BCLK that are used only in processor systems where no debug port is implemented on the system board. ITP_CLK[1:0] are used as BCLK[1:0] references for a debug port implemented on an interposer. If a debug port is implemented in the system, ITP_CLK[1:0] are no connects. These are not processor signals.
RESET#	I	Asserting the RESET# signal resets the processor to a known state and invalidates its internal caches without writing back any of their contents. For a power-on Reset, RESET# must stay active for at least two milliseconds after VCC and BCLK have reached their proper specifications. On observing active RESET#, both system bus agents will deassert their outputs within two clocks. All processor straps must be valid within the specified setup time before RESET# is deasserted.
RS[2:0]#	I	RS[2:0]# (Response Status) are driven by the response agent (the agent responsible for completion of the current transaction), and must connect the appropriate pins of both processor system bus agents.
RSVD	-	These pins are RESERVED and must be left unconnected on the board. However, it is recommended that routing channels to these pins on the board be kept open for possible future use. Please refer to the platform design guides for more details.
SLP#	I	SLP# (Sleep), when asserted in Stop-Grant state, causes the processor to enter the Sleep state. During Sleep state, the processor stops providing internal clock signals to all units, leaving only the Phase-Locked Loop (PLL) still operating. Processors in this state will not recognize snoops or interrupts. The processor will recognize only assertion of the RESET# signal, deassertion of SLP#, and removal of the BCLK input while in Sleep state. If SLP# is deasserted, the processor exits Sleep state and returns to Stop-Grant state, restarting its internal clock signals to the bus and processor core units. If DPSLP# is asserted while in the Sleep state, the processor will exit the Sleep state and transition to the Deep Sleep state.

5.1 Intel Pentium M Processor

Signal Name	Type	Description
SMI#	I	SMI# (System Management Interrupt) is asserted asynchronously by system logic. On accepting a System Management Interrupt, the processor saves the current state and enter System Management Mode (SMM). An SMI Acknowledge transaction is issued, and the processor begins program execution from the SMM handler. If SMI# is asserted during the deassertion of RESET# the processor will tristate its outputs.
STPCLK#	I	STPCLK# (Stop Clock), when asserted, causes the processor to enter a low power Stop-Grant state. The processor issues a Stop-Grant Acknowledge transaction, and stops providing internal clock signals to all processor core units except the system bus and APIC units. The processor continues to snoop bus transactions and service interrupts while in Stop-Grant state. When STPCLK# is deasserted, the processor restarts its internal clock to all units and resumes execution. The assertion of STPCLK# has no effect on the bus clock; STPCLK# is an asynchronous input.
TCK	I	TCK (Test Clock) provides the clock input for the processor Test Bus (also known as the Test Access Port).
TDI	I	TDI (Test Data In) transfers serial test data into the processor. TDI provides the serial input needed for JTAG specification support.
TDO	O	TDO (Test Data Out) transfers serial test data out of the processor. TDO provides the serial output needed for JTAG specification support.
TEST1, TEST2, TEST3	I	TEST1, TEST2, and TEST3 must be left unconnected but should have a stuffing option connection to V SS separately using 1-k, pull-down resisitors.
THERMDA	Other	Thermal Diode Anode.
THERMDC	Other	Thermal Diode Cathode.
THERMTRIP#	O	The processor protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all execution when the junction temperature exceeds approximately 125°C. This is signalled to the system by the THERMTRIP# (Thermal Trip) pin.
TMS	I	TMS (Test Mode Select) is a JTAG specification support signal used by debug tools.
TRDY#	I	TRDY# (Target Ready) is asserted by the target to indicate that it is ready to receive a write or implicit writeback data transfer. TRDY# must connect the appropriate pins of both system bus agents.
TRST#	I	TRST# (Test Reset) resets the Test Access Port (TAP) logic. TRST# must be driven low during power on Reset.

Signal Name	Type	Description
VCC	I	Processor core power supply.
VCCA[3:0]	I	VCCA provides isolated power for the internal processor core PLL's.
VCCP	I	Processor I/O Power Supply.
VCCQ[1:0]	I	Quiet power supply for on die COMP circuitry. These pins should be connected to VCCP on the motherboard. However, these connections should enable addition of decoupling on the VCCQ lines if necessary.
VCCSENSE	O	VCCSENSE is an isolated low impedance connection to processor core power (VCC). It can be used to sense or measure power near the silicon with little noise.
VID[5:0]	O	VID[5:0] (Voltage ID) pins are used to support automatic selection of power supply voltages (Vcc). Unlike some previous generations of processors, these are CMOS signals that are driven by the Intel Pentium M processor. The voltage supply for these pins must be valid before the VR can supply Vcc to the processor. Conversely, the VR output must be disabled until the voltage supply for the VID pins becomes valid. The VID pins are needed to support the processor voltage specification variations.
VSSSENSE	O	VSSSENSE is an isolated low impedance connection to processor core VSS. It can be used to sense or measure ground near the silicon with little noise.

5.2 Intel 82855GM Graphics and Memory Controller Hub (GMCH)

Host Interface Signals

Signal Name	Type	Description
ADS#	I/O AGTL+	**Address Strobe:** The system bus owner asserts ADS# to indicate the first of two cycles of a request phase. The GMCH can assert this signal for snoop cycles and interrupt messages.
BNR#	I/O AGTL+	**Block Next Request:** Used to block the current request bus owner from issuing a new request. This signal is used to dynamically control the CPU bus pipeline depth.
BPRI#	O AGTL+	**Bus Priority Request:** The GMCH is the only Priority Agent on the system bus. It asserts this signal to obtain the ownership of the address bus. This signal has priority over symmetric bus requests and will cause the current symmetric owner to stop issuing new transactions unless the HLOCK# signal was asserted.
BREQ0#	I/O AGTL+	**Bus Request 0#:** The GMCH pulls the processor bus BREQ**0#** signal low during **CPURST#.** The signal is sampled by the processor on the active-to-inactive transition of CPURST#. The minimum setup time for this signal is 4 BCLKs. The minimum hold time is 2 clocks and the maximum hold time is 20 BCLKs. BREQ0# should be tristated after the hold time requirement has been satisfied. During regular operation, the GMCH will use BREQ0# as an early indication for PSB Address and Ctl input buffer and sense amp activation.
CPURST#	O AGTL+	**CPU Reset:** The CPURST# pin is an output from the GMCH. The GMCH asserts CPURST# while RESET# (PCIRST# from ICH4-M) is asserted and for approximately 1 ms after RESET# is deasserted. The CPURS**T#** allows the processor to begin execution in a known state. Note that the ICH4-M must provide CPU strap set-up and hold-times around CPURST#. This requires strict synchronization between GMCH, CPURST# deassertion and ICH4-M driving the straps.
DBSY#	I/O AGTL+	**Data Bus Busy:** Used by the data bus owner to hold the data bus for transfers requiring more than one cycle.
DEFER#	O AGTL+	**Defer:** GMCH will generate a deferred response as defined by the rules of the GMCH's Dynamic Defer policy. The GMCH will also use the DEFER# signal to indicate a CPU retry response.
DPSLP#	I CMOS	**Deep Sleep #:** This signal comes from the ICH4-M device, providing an indication of C3 and C4 state control to the CPU. Deassertion of this signal is used as an early indication for C3 and C4 wake up (to active HPLL). Note that this is a low-voltage CMOS buffer operating on the PSB VTT power plane.
HD[63:0]#	I/O AGTL+	**Host Data:** These signals are connected to the CPU data bus. HD[63:0]# are transferred at 4x rate. Note that the data signals are inverted on the CPU bus.

Signal Name	Type	Description
DINV[3:0]#	I/O AGTL+	**Dynamic Bus Inversion:** Driven along with the HD[63:0]# signals. Indicates if the associated signals are inverted or not. DINV[3:0]# are asserted such that the number of data bits driven electrically low (low voltage) within the corresponding 16-bit group never exceeds 8. **DINV#** — **Data Bits** DNIV[3]# — HD[63:48]# DNIV[2]# — HD[47:32]# DINV[1]# — HD[31:16]# DINV[0]# — HD[15:0]#
HA[31:0]#	I/O AGTL+	**Host Address Bus:** HA[31:3]# connects to the CPU address bus. During processor cycles the HA[31:3]# are inputs. The GMCH drives HA[31:3]# during snoop cycles on behalf of Hub Interface. HA[31:3]# are transferred at 2x rate. Note that the address is inverted on the CPU bus.
HADSB[1:0]#	I/O AGTL+	**Host Address Strobe:** HA[31:3]# connects to the CPU address bus. During CPU cycles, the source synchronous strobes are used to transfer HA[31:3]# and HREQ[4:0]# at the 2x transfer rate. **Strobe** — **Address Bits** HADSTB[0]# HA[16:3]#, HREQ[4:0]# HADSTB[1]# HA[31:17]#
DRDY#	I/O AGTL+	**Data Ready:** Asserted for each cycle that data is transferred.
HDSTBP[3:0]# **HDSTBN[3:0]#**	I/O AGTL+	**Differential Host Data Strobes:** The differential source synchronous strobes are used to transfer HD[63:0]# and DINV[3:0]# at the 4x transfer rate. **Strobe** — **Data Bits** HDSTBP[3]#, HDSTBN[3]# — HD[63:48]#, DINV[3]# HDSTBP[2]#, HDSTBN[2]# — HD[47:32]#, DINV[2]# HDSTBP[1]#, HDSTBN[1]# — HD[31:16]#, DINV[1]# HDSTBP[0]#, HDSTBN[0]# — HD[15:0]#, DINV[0]#
HIT#	I/O AGTL+	**Hit:** Indicates that a caching agent holds an unmodified version of the requested line. Also, driven in conjunction with **HITM#** by the target to extend the snoop window.
HITM#	I/O AGTL+	**Hit Modified:** Indicates that a caching agent holds a modified version of the requested line and that this agent assumes responsibility for providing the line. Also, driven in conjunction with HIT# to extend the snoop window.
HLOCK#	I/O AGTL+	**Host Lock:** All CPU bus cycles sampled with the assertion of HLOCK# and ADS#, until the negation of HLOCK# must be atomic, i.e. no Hub Interface snoopable access to System Memory is allowed when HLOCK# is asserted by the CPU.

5.2 Intel 82855GM Graphics and Memory Controller Hub (GMCH)

Host Interface Signals (Continued)

Signal Name	Type	Description
HREQ[4:0]#	I/O AGTL+	**Host Request Command:** Defines the attributes of the request. HREQ[4:0]# are transferred at 2x rate. Asserted by the requesting agent during both halves of the Request Phase. In the first half the signals define the transaction type to a level of detail that is sufficient to begin a snoop request. In the second half the signals carry additional information to define the complete transaction type.
HTRDY#	O AGTL+	**Host Target Ready:** Indicates that the target of the processor transaction is able to enter the data transfer phase.
RS[2:0]#	O AGTL+	**Response Status:** Indicates type of response according to the following the table: **RS[2:0]** — **Response type** 000 — Idle state 001 — Retry response 010 — Deferred response 011 — Reserved (not driven by MCH-M) 100 — Hard Failure (not driven by MCH-M) 101 — No data response 110 — Implicit Write back 111 — Normal data response

DDR SDRAM Interface Signals

Signal Name	Type	Description
SCS [3:0]#	O SSTL_2	**Chip Select:** These pins select the particular DDR SDRAM components during the active state. **Note:** There is one SCS# per DDR-SDRAM Physical SO-DIMM device row. These signals can be toggled on every rising System Memory Clock edge.
SMA[12:0]	O SSTL_2	**Multiplexed Memory Address:** These signals are used to provide the multiplexed row and column address to DDR SDRAM.
SBA[1:0]	O SSTL_2	**Bank Select (Memory Bank Address):** These signals define which banks are selected within each DDR SDRAM row. The SMA and SBA signals combine to address every possible location within a DDR SDRAM device.
SRAS#	O SSTL_2	**DDR Row Address Strobe: SRAS#** may be heavily loaded and requires tw0 DDR SDRAM clock cycles for setup time to the DDR SDRAMs. Used with SCAS# and SWE# (along with SCS#) to define the System Memory commands.
SCAS#	O SSTL_2	**DDR Column Address Strobe:** SCAS# may be heavily loaded and requires two clock cycles for setup time to the DDR SDRAMs. Used with SRAS# and SWE# (along with SCS#) to define the System Memory commands.
SWE#	O SSTL_2	**Write Enable:** Used with SCAS# and SRAS# (along with SCS#) to define the DDR SDRAM commands. SWE# is asserted during writes to DDR SDRAM. SWE# may be heavily loaded and requires two clock cycles for setup time to the DDR SDRAMs.
SDQ[71:0]	I/O SSTL_2	**Data Lines:** These signals are used to interface to the DDR SDRAM data bus. **NOTE:** ECC error detection is supported: by the SDQ[71:64] signals.
SDQS[8:0]	I/O SSTL_2	**Data Strobes:** Data strobes are used for capturing data. During writes, SDQS is centered on data. During reads, SDQS is edge aligned with data. The following list matches the data strobe with the data bytes. There is an associated data strobe (DQS) for each data signal (DQ) and check bit (CB) group. SDQS[7] -> SDQ[63:56] SDQS[6] -> SDQ[55:48] SDQS[5] -> SDQ[47:40] SDQS[4] -> SDQ[39:32] SDQS[3] -> SDQ[31:24] SDQS[2] -> SDQ[23:16] SDQS[1] -> SDQ[15:8] SDQS[0] -> SDQ[7:0] **NOTE:** ECC error detection is supported by the SDQS[8] signal.
SCKE[3:0]	O SSTL_2	**Clock Enable:** These pins are used to signal a self-refresh or power down command to the DDR SDRAM array when entering system suspend. SCKE is also used to dynamically power down inactive DDR SDRAM rows. There is one SCKE per DDR SDRAM row. These signals can be toggled on every rising SCK edge.
SMAB[5,4,2,1]	O SSTL_2	**Memory Address Copies:** These signals are identical to SMA[5,4,2,1] and are used to reduce loading for selective CPC(clock-per-command). These copies are not inverted.
SDM[8:0]	O SSTL_2	**Data Mask:** When activated during writes, the corresponding data groups in the DDR SDRAM are masked. There is one SDM for every eight data lines. SDM can be sampled on both edges of the data strobes. **NOTE:** ECC error detection is supported by the SDM[8] signal.
RCVENOUT#	O SSTL_2	**Clock Output:** Reserved, NC.
RCVENIN#	I SSTL_2	**Clock Input:** Reserved, NC.

5.2 Intel 82855GM Graphics and Memory Controller Hub (GMCH)

Hub Interface Signals

Signal Name	Type	Description
HI_[10:0]	I/O Hub	**Packet Data:** Data signals used for HI read and write operations.
HI_STB	I/O Hub	**Packet Strobe:** One of two differential strobe signals used to transmit or receive packet data over HI.
HI_STB#	I/O Hub	**Packet Strobe Complement**: One of two differential strobe signals used to transmit or receive packet data over HI.

Clock Signals

Signal Name	Type	Description
Host Processor Clocking		
BC.LK **BCLK#**	I CMOS	**Differential Host Clock In:** These pins receive a buffered host clock from the external clock synthesizer. This clock is used by all of the GMCH logic that are in the Host clock domain (Host, Hub and System Memory). The clock is also the reference clock for the graphics core PLL. This is a low voltage differential input.
System Memory Clocking		
SCK[5:0]	O SSTL_2	**Differential DDR SDRAM Clock:** SCK and SCK# pairs are differential clock outputs. The crossing of the positive edge of SCK and the negative edge of SCK# is used to sample the address and control signals on the DDR SDRAM. There are 3 pairs to each SO-DIMM. **NOTE:** ECC error detection is supported by the SCK[2] and SCK[5] signals.
SCK[5:0]#	O SSTL_2	**Complementary Differential DDR SDRAM Clock:** These are the complimentary differential DDR SDRAM clock signals. **NOTE:** ECC error detection is supported by the SCK[2]# and SCK[5]# signals.
DVO/Hub Input Clocking		
GCLKIN	I CMOS	**Input Clock:** 66-MHz, 3.3-V input clock from external buffer DVO/Hub Interface.
DVO Clocking		
DVOBC.LK **DVOBCLK#**	O DVO	**Differential DVO Clock Output:** These pins provide a differential pair reference clock that can run up to 165-MHz. DVOBCLK corresponds to the primary clock out. DVOBCLK# corresponds to the primary complementary clock out. DVOBCLK and DVOBCLK# should be left as NC (“Not Connected”) if the DVO B port is not implemented.
DVOCC.LK **DVOCCLK#**	O DVO	**Differential DVO Clock Output**: These pins provide a differential pair reference clock that can run up to 165-MHz. DVOCCLK corresponds to the primary clock out. DVOCCLK# corresponds to the primary complementary clock out. DVOCCLK and DVOCCLK# should be left as NC (“Not Connected”) if the DVO C port is not implemented.
DVOBCCLKINT	I DVO	**DVOBC Pixel Clock Input/Interrupt:** This signal may be selected as the reference input to either dot clock PLL (DPLL) or may be configured as an interrupt input. A TV-out device can provide the clock reference. The maximum input frequency for this signal is 85 -MHz. DVOBC Pixel Clock Input: When selected as the dot clock PLL (DPLL) reference input, this clock reference input supports SSC clocking for DVO LVDS devices. DVOBC Interrupt: When configured as an interrupt input, this interrupt can support either DVOB or DVOC. DVOBCCLKINT needs to be pulled down if the signal is NOT used.
DPMS	I DVO	**Display Power Management Signaling:** This signal is used only in mobile systems to act as the DREFCLK in certain power management states(i.e. Display Power Down Mode); DPMS Clock is used to refresh video during S1-M. Clock Chip is powered down in S1-M. DPMS should come from a clock source that runs during
DAC Clocking		
DREFCLK	I LVTTL	**Display Clock Input:** This pin is used to provide a 48-MHz input clock to the Display PLL that is used for 2D/Video and DAC.
LVDS LCK Flat Panel Clocking		
DREFSSCLK	I LVTTL	**Display SSC Clock Input:** This pin provides a 48-MHz or 66-MHz input clock (SSC or non-SSC) to the Display PLL B.

Dedicated LVDS LCD Flat Panel Interface Signals

Signal Name	Type	Voltage	Description
ICLKAP	O LVDS	1.25 V± 225 mV	**Channel A differential clock pair output (true):** 245-800 MHz
ICLKAM	O LVDS	1.25 V± 225 mV	**Channel A differential clock pair output (compliment):** 245-800 MHz.
IYAP[3:0]	O LVDS	1.25 V± 225 mV	**Channel A differential data pair 3:0 output (true):** 245-800 MHz.
IYAM[3:0]	O LVDS	1.25 V± 225 mV	**Channel A differential data pair 3:0 output (compliment):** 245-800 MHz.

5.2 Intel 82855GM Graphics and Memory Controller Hub (GMCH)

Dedicated LVDS LCD Flat Panel Interface Signals (Continued)

Signal Name	Type	Voltage	Description
ICLKBP	O LVDS	1.25 V± 225 mV	**Channel B differential clock pair output (true):** 245-800 MHz.
ICLKBM	O LVDS	1.25 V± 225 mV	**Channel B differential clock pair output (compliment):** 245-800 MHz.
IYBP[3:0]	O LVDS	1.25 V± 225 mV	**Channel B differential data pair 3:0 output (true):** 245-800 MHz.
IYBM[3:0]	O LVDS	1.25 V± 225 mV	**Channel B differential data pair 3:0 output (compliment):** 245-800 MHz.

Digital Video Output B (DVOB) Port Signals

Signal Name	Type	Description
DVOBD[11:0]	O DVO	**DVOB Data:** This data bus is used to drive 12-bit RGB data on each edge of the differential clock signals, DVOBCLK and DVOBCLK#. This provides 24-bits of data per clock period. In dual channel mode, this provides the lower 12-bits of pixel data. DVOBD[11:0] should be left as left as NC (“Not Connected”) if not used.
DVOBHSYNC	O DVO	**Horizontal Sync**: HSYNC signal for the DVOB interface. **DVOBHSYNC** should be left as left as NC (“Not Connected”) if not used.
DVOBVSYNC	O DVO	**Vertical Sync**: VSYNC signal for the DVOB interface. DVOBVSYNC should be left as left as NC (“Not Connected”) if the signal is NOT used when using internal graphics device.
DVOBBLANK#	O DVO	**Flicker Blank or Border Period Indication: DVOBBLANK# is** a programmable output pin driven by the GMCH. When programmed as a blank period indication, this pin indicates active pixels excluding the border. When programmed as a border period indication, this pin indicates active pixel including the border pixels. DVOBBLANK# should be left as left as NC (“Not Connected”) if not used.
DVOBFLDSTL	I DVO	**TV Field and Flat Panel Stall Signa**l. This input can be programmed to be either a TV Field input from the TV encoder or Stall input from the flat panel. DVOB TV Field Signal: When used as a Field input, it synchronizes the overlay field with the TV encoder field when the overlay is displaying an interleaved source. DVOB Flat Panel Stall Signal: When used as the Stall input, it indicates that the pixel pipeline should stall one horizontal line. The signal changes during horizontal blanking. The panel fitting logic, when expanding the image vertically, uses this. DVOBFLDSTL needs to be pulled down if not used.

Digital Video Output C (DVOC) Port Signals

Signal Name	Type	Description
DVOCD[11:0]	O DVO	**DVOC Data**: This data bus is used to drive 12-bit RGB data on each edge of the differential clock signals, DVOCCLK and DVOCCLK#. This provides 24-bits of data per clock period. In dual channel mode, this provides the upper 12-bits of pixel data. DVOCD[11:0] should be left as left as NC (“Not Connected”) if not used.
DVOCHSYNC	O DVO	**Horizontal Sync**: HSYNC signal for the DVOC interface. DVOCHSYNC should be left as left as NC (“Not Connected”) if not used.
DVOCVSYNC	O DVO	**Vertical Sync**: VSYNC signal for the DVOC interface. DVOCVSYNC should be left as left as NC (“Not Connected”) if the signal is NOT used when using internal graphics device.
DVOCBLANK#	O DVO	**Flicker Blank or Border Period Indicatio**n: **DVOCBLANK#** is a programmable output pin driven by the GMCH. When programmed as a blank period indication, this pin indicates active pixels excluding the border. When programmed as a border period indication, this pin indicates active pixel including the border pixels. DVOCBLANK# should be left as left as NC (“Not Connected”) if not used.
DVOCFLDSTL	I DVO	**TV Field and Flat Panel Stall Signa**l. This input can be programmed to be either a TV Field input from the TV encoder or Stall input from the flat panel. DVOC TV Field Signal: When used as a Field input, it synchronizes the overlay field with the TV encoder field when the overlay is displaying an interleaved source. DVOC Flat Panel Stall Signal: When used as the Stall input, it indicates that the pixel pipeline should stall one horizontal line. The signal changes during horizontal blanking. The panel fitting logic, when expanding the image vertically, uses this. DVOCFLDSTL needs to be pulled down if not used.

DVOB and DVOC Port Common Signals

Signal Name	Type	Description
DVOBCINTR#	I DVO	**DVOBC Interrup**t: This pin is used to signal an interrupt, typically used to indicate a hot plug or unplug of a digital display.
ADDID[7:0]	I DVO	**ADDID[7:0**]: These pins are used to communicate to the Video BIOS when an external device is interfaced to the DVO port. **Not**e: Bit[7] needs to be strapped low when an on-board DVO device is present. The other pins should be left as NC.
DVODETECT	I DVO	**DVODETEC**T: This strapping signal indicates to the GMCH whether a DVO device is present or not. When a DVO device is connected, then DVODETECT = 0.

5.2 Intel 82855GM Graphics and Memory Controller Hub (GMCH)

Analog CRT Display Signals

Signal Name	Type	Description
VSYNC	O CMOS	**CRT Vertical Synchronizatio**n: This signal is used as the vertical sync signal.
HSYNC	O CMOS	**CRT Horizontal Synchronizatio**n: This signal is used as the horizontal sync signal.
RED	O Analog	**Red (Analog Video Output**): This signal is a CRT Analog video output from the internal color palette DAC. The DAC is designed for a 37.5-ohm equivalent load on each pin (e.g., 75-ohm resistor on the board, in parallel with the 75-ohm. CRT load).
RED#	O Analog	**Red# (Analog Output):** Tied to ground.
GREEN	O Analog	**Green (Analog Video Output**): This signal is a CRT analog video output from the internal color palette DAC. The DAC is designed for a 37.5-ohm equivalent load on each pin (e.g., 75-ohm resistor on the board, in parallel with the 75-ohm . CRT load).
GREEN#	O Analog	**Green# (Analog Output):** Tied to ground.
BLUE	O Analog	**Blue (Analog Video Output)** : This signal is a CRT Analog video output from the internal color palette DAC. The DAC is designed for a 37.5-ohm equivalent load on each pin (e.g., 75- ohm resistor on the board, in parallel with the 75-ohm. CRT load).
BLUE#	O Analog	**Blue# (Analog Output):** Tied to ground.

GPIO Signals

GPIO I/F Total	Type	Comments
RSTIN#	I CMOS	**Reset:** Primary Reset, Connected to PCIRST# of ICH4-M.
PWROK	I CMOS	**Power O**K: Indicates that power to GMCH is stable.
AGPBUSY#	O CMOS	**AGPBUSY:** Output of the GMCH IGD to the ICH4-M, which indicates that certain graphics activity is taking place. It will indicate to the ACPI software not to enter the C3 state. It will also cause a C3/C4 exit if C3/C4 was being entered, or was already entered when AGPBUSY# went active. Not active when the IGD is in any ACPI state other than D0.
EXTTS_0	I CMOS	**External Thermal Sensor Input:** This signal is an active low input to the GMCH and is used to monitor the thermal condition around the System Memory and is used for triggering a read throttle. The GMCH can be optionally programmed to send a SERR, SCI, or SMI message to the ICH4-M upon the triggering of this signal.

GPIO I/F Total	Type	Comments
LCLKCTLA	O CMOS	**SSC Chip Clock Control:** Can be used to control an external clock chip with SSC control.
LCLKCTLB	O CMOS	**SSC Chip Data Control:** Can be used to control an external clock chip for SSC control.
PANELVDDEN	O CMOS	**LVDS LCD Flat Panel Power Control:** This signal is used enable power to the panel interface.
PANELBKLTEN	O CMOS	**LVDS LCD Flat Panel Backlight Enable:** This signal is used to enable the backlight inverter (BLI).
PANELBKLTCTL	O CMOS	**LVDS LCD Flat Panel Backlight Brightness Control:** This signal is used as the Pulse Width Modulated (PWM) control signal to control the backlight inverter.
DDCACLK	I/O CMOS	**CRT DDC Clock:** This signal is used as the DDC clock signal between the CRT monitor and the GMCH.
DDCADATA	I/O CMOS	**CRT DDC Data:** This signal is used as the DDC data signal between the CRT monitor and the GMCH.
DDCPCLK	I/O CMOS	**Panel DDC Clock:** This signal is used as the DDC clock signal between the LFP and the GMCH.
DDCPADATA	I/O CMOS	**Panel DDC Data:** This signal is used as the DDC data signal between the LFP and the GMCH.
MI2CCLK	I/O DVO	**DVO I2C Clock:** This signal is used as the I2C_CLK for a digital display (i.e. TV-Out Encoder, TMDS transmitter). This signal is tri-stated during a hard reset.
MI2CDATA	I/O DVO	**DVO I2C Data:** This signal is used as the I2C_DATA for a digital display (i.e. TV-Out Encoder, TMDS transmitter). This signal is tri-stated during a hard reset.
MDVICLK	I/O DVO	**DVI DDC Clock:** This signal is used as the DDC clock for a digital display connector (i.e. primary digital monitor). This signal is tri-stated during a hard reset.
MDVIDATA	I/O DVO	**DVI DDC Data:** The signal is used as the DDC data for a digital display connector (i.e. primary digital monitor). This signal is tri-stated during a hard reset.
MDDCDATA	I/O DVO	**DVI DDC Clock:** The signal is used as the DDC data for a digital display connector (i.e. secondary digital monitor). This signal is tri-stated during a hard reset.
MDDCCLK	I/O DVO	**DVI DDC Data:** The signal is used as the DDC clock for a digital display connector (i.e. secondary digital monitor). This signal is tri-stated during a hard reset.

5.2 Intel 82855GM Graphics and Memory Controller Hub (GMCH)

Voltage Reference, PLL Power Signals

Signal Name	Type	Description
Host Processor		
HXRCOMP	Analog	**Host RCOMP:** Used to calibrate the Host AGTL+ I/O buffers.
HYRCOMP	Analog	**Host RCOMP:** Used to calibrate the Host AGTL+ I/O buffers.
HXSWING	Analog	**Host Voltage Swing (RCOMP reference voltage):** These signals provide a reference voltage used by the PSB RCOMP circuit.
HYSWING	Analog	**Host Voltage Swing (RCOMP reference voltage**): These signals provide a reference voltage used by the PSB RCOMP circuit.
HDVREF[2:0]	Ref Analog	**Host Data (input buffer) VREF**: Reference voltage input for the data signals of the Host AGTL+ Interface. Input buffer differential amplifier to determine a high versus low input voltage.
HAVREF	Ref Analog	**Host Address (input buffer) VREF**: Reference voltage input for the address signals of the Host AGTL+ Interface. This signal is connected to the input buffer differential amplifier to determine a high versus low input voltage.
HCCVREF	Ref Analog	**Host Common Clock (Command input buffer) VREF**: Reference voltage input for the common clock signals of the Host AGTL+ Interface. This signal is connected to the input buffer differential amplifier to determine a high versus low input voltage.
VTTLF	Power	**PSB Power Supply:** VTTLF is the low frequency connection from the board. This signal is the primary connection of power for GMCH.
VTTHF	Power	**PSB Power Supply:** VTTHF is the high frequency supply. It is for direct connection from an internal package plane to a capacitor placed immediately adjacent to the GMCH. **NOTE:** Not to be connected to power rail.
System Memory		
SMRCOMP	Analog	**System Memory RCOMP**: This signal is used to calibrate the memory I/O buffers.
SMVREF_0	Ref Analog	**Memory Reference Voltage(Input buffer VREF**):Reference voltage input for Memory Interface. Input buffer differential amplifier to determine a high versus low input voltage.
SMVSWINGH	Ref Analog	**RCOMP reference voltage:** This is connected to the RCOMP buffer differential amplifier and is used to calibrate the I/O buffers.
SMVSWINGL	Ref Analog	**RCOMP reference voltage**: This is connected to the RCOMP buffer differential amplifier and is used to calibrate the I/O buffers.
VCCSM	Power	Power supply for Memory I/O.
VCCQSM	Power	Power supply for System Memory clock buffers.
VCCASM	Power	Power supply for System Memory logic running at the core voltage (isolated supply, not connected to the core).

Signal Name	Type	Description
Hub Interface		
HLRCOMP	Analog	**Hub Interface RCOMP**: This signal is connected to a reference resistor in order to calibrate the buffers.
PSWING	Ref Analog	**Input buffer VREF**: Input buffer differential amplifier to determine a high versus low input voltage.
VCCHL	Power	Power supply for Hub Interface buffers
DVO		
DVORCOMP	Analog	**Compensation for DVO**: This signal is used to calibrate the DVO I/O buffers.
GVREF	Ref Analog	**Input buffer VREF**: Input buffer differential amplifier to determine a high versus low input voltage.
VCCDVO	Power	Power supply for DVO.
GPIO		
VCCGPIO	Power	Power supply for GPIO buffers
DAC		
REFSET	Ref Analog	**Resistor Set:** Set point resistor for the internal color palette DAC.
VCCADAC	Power	Power supply for the DAC
VSSADAC	Power	Ground supply for the DAC
LVDS		
LIBG	Analog	LVDS reference current: signal connected to reference resistor.
VCCDLVDS	Power	Digital power supply.
VCCTXLVDS	Power	Data/Clk Tx power supply.
VCCALVDS	Power	Analog power supply.
VSSALVDS	Power	Ground supply for LVDS.
Clocks		
VCCAHPLL	Power	Power supply for the Host PLL.
VCCAGPLL	Power	Power supply for the Hub/DVO PLL.
VCCADPLLA	Power	Power supply for the display PLL A.
VCCADPLLB	Power	Power supply for the display PLL B.
Core		
VCC	Power	Power supply for the core.
VSS	Power	Ground supply for the chip.

5.3 Intel 82801DBM I/O Controller Hub 4 Mobile (ICH4-M)

Hub Interface Signals

Signal Name	Type	Description
HI[11:0]	I/O	**Hub Interface Signals**
HI_STB/HI_STBS	I/O	**Hub Interface Strobe/ Hub Interface Strobe Second:** One of two differential strobe signals used to transmit and receive data through the hub interface. Hub Interface 1.5 mode this signal is not differential and is the second of the two strobe signals.
HI_STB#/ HI_STBF	I/O	**Hub Interface Strobe Complement / Hub Interface Strobe First:** One of two differential strobe signals used to transmit and receive data through the hub interface. Hub Interface 1.5 mode this signal is not differential and is the first of the two strobe signals.
HICOMP	I/O	**Hub Interface Compensation:** Used for hub interface buffer compensation.
HI_VSWING	I	**Hub Interface Voltage Swing:** Analog input used to control the voltage swing and impedance strength of hub interface pins.

LAN Connect Interface Signals

Signal Name	Type	Description
LAN_CLK	I	**LAN I/F Clock:** Driven by the LAN Connect component. Frequency range is 5 MHz to 50 MHz.
LAN_RXD[2:0]	I	**Received Data:** The LAN Connect component uses these signals to transfer data and control information to the integrated LAN Controller. These signals have integrated weak pull-up resistors.
LAN_TXD[2:0]	O	**Transmit Dat**a: The integrated LAN Controller uses these signals to transfer data and control information to the LAN Connect component.
LAN_RSTSYNC	O	**LAN Reset/Sync:** The LAN Connect component's Reset and Sync signals are multiplexed onto this pin.

EEPROM Interface Signals

Signal Name	Type	Description
EE_SHCLK	O	**EEPROM Shift Cloc**k: Serial shift clock output to the EEPROM.
EE_DIN	I	**EEPROM Data I**n: Transfers data from the EEPROM to the ICH3. This signal has an integrated pull-up resistor.
EE_DOUT	O	**EEPROM Data Ou**t: Transfers data from the ICH3 to the EEPROM.
EE_CS	O	**EEPROM Chip Selec**t: Chip select signal to the EEPROM.

Firmware Hub Interface Signals

Signal Name	Type	Description
FWH[3:0]/ LAD[3:0]	I/O	**Firmware Hub Signals.** Muxed with LPC address signals.
FWH[4]/ LFRAME#	I/O	LFRAME# **Firmware Hub Signals.** Muxed with LPC LFRAME# signal.

PCI Interface Signals

Signal Name	Type	Description
AD[31:0]	I/O	**PCI Address/Data:** AD[31:0] is a multiplexed address and data bus. During the first clock of a transaction, AD[31:0] contain a physical address (32 bits). During subsequent clocks, AD[31:0] contain data. The ICH4 drives all 0s on AD[31:0] during the address phase of all PCI Special Cycles.
C/BE[3:0]#	I/O	**Bus Command and Byte Enables:** The command and byte enable signals are multiplexed on the same PCI pins. During the address phase of a transaction, C/BE[3:0]# define the bus command. During the data phase, C/BE[3:0]# define the Byte Enables. **C/BE[3:0]# Command Type** 0 0 0 0 Interrupt Acknowledge 0 0 0 1 Special Cycle 0 0 1 0 I/O Read 0 0 1 1 I/O Write 0 1 1 0 Memory Read 0 1 1 1 Memory Write 1 0 1 0 Configuration Read 1 0 1 1 Configuration Write 1 1 0 0 Memory Read Multiple 1 1 1 0 Memory Read Line 1 1 1 1 Memory Write and Invalidate All command encodings not shown are reserved. The ICH4 does not decode reserved values, and therefore will not respond if a PCI master generates a cycle using one of the reserved values.
DEVSEL#	I/O	**Device Select:** The ICH4 asserts DEVSEL# to claim a PCI transaction. As an output, the ICH4 asserts DEVSEL# when a PCI master peripheral attempts an access to an internal ICH4 address or an address destined for the hub interface (main memory or AGP). As an input, DEVSEL# indicates the response to an ICH4-initiated transaction on the PCI bus. DEVSEL# is tri-stated from the leading edge of PCIRST#. DEVSEL# remains tri-stated by the ICH4 until driven by a Target device.

5.3 Intel 82801DBM I/O Controller Hub 4 Mobile (ICH4-M)

PCI Interface Signals (Continued)

Signal Name	Type	Description
FRAME#	I/O	**Cycle Frame:** The current Initiator drives FRAME# to indicate the beginning and duration of a PCI transaction. While the Initiator asserts FRAME#, data transfers continue. When the Initiator negates FRAME#, the transaction is in the final data phase. FRAME# is an input to the ICH4 when the ICH4 is the Target, and FRAME# is an output from the ICH4 when the ICH4 is the Initiator. FRAME# remains tri- stated by the ICH4 until driven by an Initiator.
IRDY#	I/O	**Initiator Ready:** IRDY# indicates the ICH4's ability, as an Initiator, to complete the current data phase of the transaction. It is used in conjunction with TRDY#. A data phase is completed on any clock that both IRDY# and TRDY# are sampled asserted. During a write, IRDY# indicates the ICH4 has valid data present on AD[31:0]. During a read, it indicates the ICH4 is prepared to latch data. IRDY# is an input to the ICH4 when the ICH4 is the Target and an output from the ICH4 when the ICH4 is an Initiator. IRDY# remains tri-stated by the ICH4 until driven by an Initiator.
TRDY#	I/O	**Target Ready:** TRDY# indicates the ICH4's ability, as a Target, to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#. A data phase is completed when both TRDY# and IRDY# are sampled asserted. During a read, TRDY# indicates that the ICH4, as a Target, has placed valid data on AD[31:0]. During a write, TRDY# indicates that the ICH4, as a Target, is prepared to latch data. TRDY# is an input to the ICH4 when the ICH4 is the Initiator and an output from the ICH4 when the ICH4 is a Target. TRDY# is tri-stated from the leading edge of PCIRST#. TRDY# remains tri-stated by the ICH4 until driven by a target.
PAR	I/O	**Calculated/Checked Parity:** PAR uses “even” parity calculated on 36 bits, AD[31:0] plus C/BE[3:0]#. “Even” parity means that the ICH4 counts the number of 1s within the 36 bits plus PAR and the sum is always even. The ICH4 always calculates PAR on 36 bits regardless of the valid byte enables. The ICH4 generates PAR for address and data phases and only guarantees PAR to be valid one PCI clock after the corresponding address or data phase. The ICH4 drives and tri-states PAR identically to the AD[31:0] lines except that the ICH4 delays PAR by exactly one PCI clock. PAR is an output during the address phase (delayed one clock) for all ICH4 initiated transactions. PAR is an output during the data phase (delayed one clock) when the ICH4 is the Initiator of a PCI write transaction, and when it is the Target of a read transaction. ICH4 checks parity when it is the Target of a PCI write transaction. If a parity error is detected, the ICH4 will set the appropriate internal status bits, and has the option to generate an NMI# or SMI#.

Signal Name	Type	Description
STOP#	I/O	**Stop:** STOP# indicates that the ICH4, as a Target, is requesting the Initiator to stop the current transaction. STOP# causes the ICH4, as an Initiator, to stop the current transaction. STOP# is an output when the ICH4 is a Target and an input when the ICH4 is an Initiator. STOP# is tri-stated from the leading edge of PCIRST#. STOP# remains tri-stated until driven by the ICH4.
PERR#	I/O	**Parity Error:** An external PCI device drives PERR# when it receives data that has a parity error. The ICH4 drives PERR# when it detects a parity error. The ICH4 can either generate an NMI# or SMI# upon detecting a parity error (either detected internally or reported via the PERR# signal).
REQ[4:0]# **REQ[5]#/** REQ[B]#/ GPIO[1]	I	**PCI Requests:** The ICH4 supports up to 6 masters on the PCI bus. REQ[5]# is muxed with PC/PCI REQ[B]# (must choose one or the other, but not both). If not used for PCI or PC/PCI, REQ[5]#/REQ[B]# can instead be used as GPIO[1]. **NOTE:** REQ[0]# is programmable to have improved arbitration latency for for supporting PCI-based 1394 controllers.
GNT[4:0]# **GNT[5]#/** GNT[B]#/ GPIO[17]	O	**PCI Grants:** The ICH4 supports up to 6 masters on the PCI bus. GNT[5]# is muxed with PC/PCI GNT[B]# (must choose one or the other, but not both). If not needed for PCI or PC/PCI, GNT[5]# can instead be used as a GPIO. Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3 power rail. GNT[B]#/GNT[5]#/GPIO[17] has an internal pull-up.
PCICLK	I	**PCI Clock:** This is a 33 MHz clock. PCICLK provides timing for all transactions on the PCI Bus. **NOTE:** This clock does not stop based on STP_PCI# signal. PCICLK only stops based on SLP_S1# or SLP_S3#.
PCIRST#	O	**PCI Reset:** ICH4 asserts PCIRST# to reset devices that reside on the PCI bus. The ICH4 asserts PCIRST# during power-up and when S/W initiates a hard reset sequence through the RC (CF9h) register. The ICH4 drives PCIRST# inactive a minimum of 1 ms after PWROK is driven active. The ICH4 drives PCIRST# active a minimum of 1 ms when initiated through the RC register.
PLOCK#	I/O	**PCI Lock:** This signal indicates an exclusive bus operation and may require multiple transactions to complete. ICH4 asserts PLOCK# when it performs non- exclusive transactions on the PCI bus. Devices on the PCI bus (other than the ICH4) are not permitted to assert the PLOCK# signal.
SERR#	I/OD	**System Error:** SERR# can be pulsed active by any PCI device that detects a system error condition. Upon sampling SERR# active, the ICH4 has the ability to generate an NMI, SMI#, or interrupt.

5.3 Intel 82801DBM I/O Controller Hub 4 Mobile (ICH4-M)

PCI Interface Signals (Continued)

Signal Name	Type	Description
PME#	I/OD	**PCI Power Management Event:** PCI peripherals drive PME# to wake the system from low-power states S1-M–S5. PME# assertion can also be enabled to generate an SCI from the S0 state. In some cases the ICH4 may drive PME# active due to an internal wake event. The ICH4 will not drive PME# high, but it will be pulled up to VccSus3_3 by an internal pull-up resistor.
CLKRUN#	I/O	**PCI Clock Run:** Used to support PCI Clock Run protocol. Connects to PCI devices that need to request clock re-start, or prevention of clock stopping. **NOTE:** An external pull-up to the core power plane is required.
REQ[A]#/ GPIO[0] **REQ[B]#/** REQ[5]#/ GPIO[1]	I	**PC/PCI DMA Request [A:B]:** This request serializes ISA-like DMA Requests for the purpose of running ISA-compatible DMA cycles over the PCI bus. This is used by devices such as PCI based Super I/O or audio codecs which need to perform legacy 8237 DMA but have no ISA bus. When not used for PC/PCI requests, these signals can be used as General Purpose Inputs. REQ[B]# can instead be used as the 6th PCI bus request.
GNT[A]#/ GPIO[16] **GNT[B]#/** GNT[5]#/ GPIO[17]	O	**PC/PCI DMA Acknowledges [A: B]:** This grant serializes an ISA-like DACK# for the purpose of running DMA/ISA Master cycles over the PCI bus. This is used by devices such as PCI based Super/IO or audio codecs which need to perform legacy 8237 DMA but have no ISA bus. When not used for PC/PCI, these signals can be used as General Purpose Outputs. GNTB# can also be used as the 6th PCI bus master grant output. These signal have internal pull-up resistors.

IDE Interface Signals

Signal Name	Type	Description
PDCS1#, SDCS1#	O	**Primary and Secondary IDE Device Chip Selects for 100 Range:** For ATA command register block. This output signal is connected to the corresponding signal on the primary or secondary IDE connector.
PDCS3#, SDCS3#	O	**Primary and Secondary IDE Device Chip Select for 300 Range:** For ATA control register block. This output signal is connected to the corresponding signal on the primary or secondary IDE connector.
PDA[2:0], SDA[2:0]	O	**Primary and Secondary IDE Device Address:** These output signals are connected to the corresponding signals on the primary or secondary IDE connectors. They are used to indicate which byte in either the ATA command block or control block is being addressed.
PDD[15:0], SDD[15:0]	I/O	**Primary and Secondary IDE Device Data:** These signals directly drive the corresponding signals on the primary or secondary IDE connector. There is a weak internal pull-down resistor on PDD[7] and SDD[7].
PDDREQ, SDDREQ	I	**Primary and Secondary IDE Device DMA Request:** These input signals are directly driven from the DRQ signals on the primary or secondary IDE connector. It is asserted by the IDE device to request a data transfer, and used in conjunction with the PCI bus master IDE function and are not associated with any AT compatible DMA channel. There is a weak internal pull-down resistor on these signals.
PDDACK#, SDDACK#	O	**Primary and Secondary IDE Device DMA Acknowledge:** These signals directly drive the DAK# signals on the primary and secondary IDE connectors. Each is asserted by the ICH4 to indicate to IDE DMA slave devices that a given data transfer cycle (assertion of DIOR# or DIOW#) is a DMA data transfer cycle. This signal is used in conjunction with the PCI bus master IDE function and are not associated with any AT-compatible DMA channel.
PDIOR#/ (PDWSTB/PRDMARDY#) **SDIOR#/** (SDWSTB/SRDMARDY#)	O	**Primary and Secondary Disk I/O Read (PIO and Non-Ultra DMA):** This is the command to the IDE device that it may drive data onto the PDD or SDD lines. Data is latched by the ICH4 on the deassertion edge of PDIOR# or SDIOR#. The IDE device is selected either by the ATA register file chip selects (PDCS1# or SDCS1#, PDCS3# or SDCS3#) and the PDA or SDA lines, or the IDE DMA acknowledge (PDDAK# or SDDAK#). Primary and Secondary Disk Write Strobe (Ultra DMA Writes to Disk): This is the data write strobe for writes to disk. When writing to disk, ICH4 drives valid data on rising and falling edges of PDWSTB or SDWSTB. Primary and Secondary Disk DMA Ready (Ultra DMA Reads from Disk): This is the DMA ready for reads from disk. When reading from disk, ICH4 deasserts PRDMARDY# or SRDMARDY# to pause burst data transfers.
PDIOW#/ (PDSTOP) **SDIOW#/** (SDSTOP)	O	**Primary and Secondary Disk I/O Write (PIO and Non-Ultra DMA):** This is the command to the IDE device that it may latch data from the PDD or SDD lines. Data is latched by the IDE device on the deassertion edge of PDIOW# or SDIOW#. The IDE device is selected either by the ATA register file chip selects (PDCS1# or SDCS1#, PDCS3# or SDCS3#) and the PDA or SDA lines, or the IDE DMA acknowledge (PDDAK# or SDDAK#). Primary and Secondary Disk Stop (Ultra DMA): ICH4 asserts this signal to terminate a burst.

5.3 Intel 82801DBM I/O Controller Hub 4 Mobile (ICH4-M)

IDE Interface Signals (Continued)

Signal Name	Type	Description
PIORDY#/ (PDRSTB/PWDMARDY#) **SIORDY#/** (SDRSTB/SWDMARDY#)	I	**Primary and Secondary I/O Channel Ready (PIO):** This signal will keep the strobe active (PDIOR# or SDIOR# on reads, PDIOW# or SDIOW# on writes) longer than the minimum width. It adds wait states to PIO transfers. Primary and Secondary Disk Read Strobe (Ultra DMA Reads from Disk): When reading from disk, the ICH4 latches data on rising and falling edges of this signal from the disk. Primary and Secondary Disk DMA Ready (Ultra DMA Writes to Disk): When writing to disk, this is de-asserted by the disk to pause burst data transfers.

Interrupt Signals

Signal Name	Type	Description
SERIRQ	I/O	**Serial Interrupt Request:** This pin implements the serial interrupt protocol.
PIRQ[D:A]#	I/OD	**PCI Interrupt Requests:** In Non-APIC Mode the PIRQx# signals can be routed to interrupts 3, 4, 5, 6, 7, 9, 10, 11, 12, 14 or 15 as described in the Interrupt Steering section. Each PIRQx# line has a separate Route Control Register. In APIC mode, these signals are connected to the internal I/O APIC in the following fashion: PIRQ[A]# is connected to IRQ16, PIRQ[B]# to IRQ17, PIRQ[C]# to IRQ18, and PIRQ[D]# to IRQ19. This frees the legacy interrupts.
PIRQ[H:E]#/ GPIO[5:2]	I/OD	**PCI Interrupt Requests:** In Non-APIC Mode the PIRQx# signals can be routed to interrupts 3, 4, 5, 6, 7, 9, 10, 11, 12, 14 or 15 as described in the Interrupt Steering section. Each PIRQx# line has a separate Route Control Register. In APIC mode, these signals are connected to the internal I/O APIC in the following fashion: PIRQ[E]# is connected to IRQ20, PIRQ[F]# to IRQ21, PIRQ[G]# to IRQ22, and PIRQ[H]# to IRQ23. This frees the legacy interrupts. If not needed for interrupts, these signals can be used as GPIO.
IRQ[14:15]	I	**Interrupt Request 14:15:** These interrupt inputs are connected to the IDE drives. IRQ14 is used by the drives connected to the Primary controller and IRQ15 is used by the drives connected to the Secondary controller.
APICCLK	I	**APIC Clock:** This clock operates up to 33.33 MHz.
APICD[1:0]	I/OD	**APIC Data:** These bi-directional open drain signals are used to send and receive data over the APIC bus. As inputs the data is valid on the rising edge of APICCLK. As outputs, new data is driven from the rising edge of the APICCLK.

LPC Interface Signals

Signal Name	Type	Description
LAD[3:0]/ FWH[3:0]	I/O	**LPC Multiplexed Command, Address, Data:** For the LAD[3:0] signals, internal pull-ups are provided.
LFRAME#/ FWH[4]	O	**LPC Frame:** LFRAME# indicates the start of an LPC cycle, or an abort.
LDRQ[1:0]#	I	**LPC Serial DMA/Master Request Inputs:** LDRQ[1:0]# are used to request DMA or bus master access. These signals are typically connected to an external Super I/O device. An internal pull-up resistor is provided on these signals.

USB Interface Signals

Signal Name	Type	Description
USBP0P, USBP0N, USBP1P, USBP1N	I/O	**Universal Serial Bus Port 1:0 Differential:** These differential pairs are used to transmit data/address/command signals for ports 0 and 1. These ports can be routed to USB UHCI Controller #1 or the USB EHCI Controller. **NOTE:** No external resistors are required on these signals. The ICH4 integrates 15 k . pull-downs and provides an output driver impedance of 45 . which requires no external series resistor
USBP2P, USBP2N, USBP3P, USBP3N	I/O	**Universal Serial Bus Port 3:2 Differential:** These differential pairs are used to transmit data/address/command signals for ports 2 and 3. These ports can be routed to USB UHCI Controller #2 or the USB EHCI Controller. **NOTE:** No external resistors are required on these signals. The ICH4 integrates 15 k . pull-downs and provides an output driver impedance of 45 . which requires no external series resistor.
USBP4P, USBP4N, USBP5P, USBP4N	I/O	**Universal Serial Bus Port 5:4 Differential:** These differential pairs are used to transmit data/address/command signals for ports 4 and 5. These ports can be routed to USB UHCI Controller #3 or the USB EHCI Controller **NOTE:** No external resistors are required on these signals. The ICH4 integrates 15 k . pull-downs and provides an output driver impedance of 45 . which requires no external series resistor
OC[5:0]#	I/O	**Overcurrent Indicators:** These signals set corresponding bits in the USB controllers to indicate that an overcurrent condition has occurred.
USBRBIAS	O	**USB Resistor Bias:** Analog connection point for an external resistor to ground. USBRBIAS should be connected to USBRBIAS# as close to the resistor as possible.
USBRBIAS#	I	**USB Resistor Bias Complement:** Analog connection point for an external resistor to ground. USBRBIAS# should be connected to USBRBIAS as close to the resistor as possible.

5.3 Intel 82801DBM I/O Controller Hub 4 Mobile (ICH4-M)

Power Management Interface Signals

Signal Name	Type	Description
THRM#	I	**Thermal Alarm:** This is an active low signal generated by external hardware to start the hardware clock throttling mode. The signal can also generate an SMI# or an SCI.
THRMTRIP#	I	**Thermal Trip:** When low, THRMTRIP# indicates that a thermal trip from the processor occurred; the ICH4 will immediately transition to a S5 state. The ICH4 will not wait for the processor stop grant cycle since the processor has overheated.
SLP_S1#	O	**S1 Sleep Control:** SLP_S1# provides Clock Synthesizer or Power plane control. Optional use is to shut off power to non-critical systems when in the S1- M (Powered On Suspend), S3 (Suspend To RAM), S4 (Suspend to Disk) or S5 (Soft Off) states.
SLP_S3#	O	**S3 Sleep Control:** SLP_S3# is for power plane control. It shuts off power to all non-critical systems when in S3 (Suspend To RAM), S4 (Suspend to Disk), or S5 (Soft Off) states.
SLP_S4#	O	**S4 Sleep Control:** SLP_S4# is for power plane control. It shuts power to all non-critical systems when in the S4 (Suspend to Disk) or S5 (Soft Off) state.
SLP_S5#	O	**S5 Sleep Control:** SLP_S5# is for power plane control. The signal is used to shut power off to all non-critical systems when in the S5 (Soft Off) states.
PWROK	I	**Power OK:** When asserted, PWROK is an indication to the ICH4 that core power and PCICLK have been stable for at least 1 ms. PWROK can be driven asynchronously. When PWROK is negated, the ICH4 asserts PCIRST#. **NOTE:** PWROK must deassert for a minimum of 3 RTC clock periods for the ICH4 to fully reset the power and properly generate the PCIRST# output
PWRBTN#	I	**Power Button:** The Power Button causes SMI# or SCI to indicate a system request to go to a sleep state. If the system is already in a sleep state, this signal causes a wake event. If PWRBTN# is pressed for more than 4 seconds, this causes an unconditional transition (power button override) to the S5 state with only the PWRBTN# available as a wake event. Override occurs even if the system is in the S1-M–S4 states. This signal has an internal pull-up resistor.
RI#	I	**Ring Indicate:** This signal is an input from the modem interface. It can be enabled as a wake event, and this is preserved across power failures.
SYS_RESET#	I	**System Reset:** This pin forces an internal reset after being debounced. The ICH4 will reset immediately if the SMBus is idle; otherwise, it will wait up to 25 ms ± 2 ms for the SMBus to idle before forcing a reset on the system.
RSMRST#	I	**Resume Well Reset:** This signal is used for resetting the resume power plane logic.

Signal Name	Type	Description
LAN_RST#	I	**LAN Reset:** This signal must be asserted at least 10 ms after the resume well power (VccLAN3_3 and VccLAN1_5 is valid. When deasserted, this signal is an indication that the resume well power is stable.
SUS_STAT#/ LPCPD#	O	**Suspend Status:** This signal is asserted by the ICH4 to indicate that the system will be entering a low power state soon. This can be monitored by devices with memory that need to switch from normal refresh to suspend refresh mode. It can also be used by other peripherals as an indication that they should isolate their outputs that may be going to powered-off planes. This signal is called LPCPD# on the LPC I/F.
C3_STAT#	O	**C3_STAT#:** This signal will typically be configured as C3_STAT#. It is used for indicating to an AGP device that a C3 state transition is beginning or ending. If C3_STAT# functionality is not required, this signal may be used as a GPO. **NOTE:** This signal will be asserted in S1-M on the ICH4-M.
SUSCLK	O	**Suspend Clock:** Output of the RTC generator circuit to use by other chips for refresh clock.
AGPBUSY#	I	**AGP Bus Busy:** To support the C3 state. This signal is an indication that the AGP device is busy. When this signal is asserted, the BM_STS bit will be set. If this functionality is not needed, this signal may be configured as a GPI.
STP_PCI#	O	**Stop PCI Clock:** This signal is an output to the external clock generator for it to turn off the PCI clock. Used to support PCI CLKRUN# protocol. If this functionality is not needed, This signal can be configured as a GPO.
STP_CPU#	O	**Stop CPU Clock:** Output to the external clock generator for it to turn off the processor clock. Used to support the C3 state. If this functionality is not needed, this signal can be configured as a GPO.
BATLOW#	I	**Battery Low:** This signal is an input from the battery to indicate that there is insufficient power to boot the system. Assertion will prevent wake from S1-M–S5 state. Can also be enabled to cause an SMI# when asserted.
CPUPERF#	OD	**CPU Performance:** CPUPERF# is used for Intel SpeedStep technology support. The signal selects which power state to put the processor in.
SSMUXSEL	O	**SpeedStep Mux Select:** SSMUXSEL is used for Intel SpeedStep technology support. The signal selects the voltage level for the processor.
VGATE/ VRMPWRGD	I	**VGATE/VRM Power Good:** VGATE/VRMPWRGD is used for Intel SpeedStep technology support. This is an output from the processor's voltage regulator to indicate that the voltage is stable. This signal may go inactive during an Intel SpeedStep transition.

5.3 Intel 82801DBM I/O Controller Hub 4 Mobile (ICH4-M)

Power Management Interface Signals (Continued)

Signal Name	Type	Description
DPRSLPVR	O	**Deeper Sleep - Voltage Regulator:** This signal is used to lower the voltage of VRM during C4 and S1-M states. When the signal is high, the voltage regulator outputs the lower “Deeper Sleep” voltage. When the signal is low (default), the voltage regulator outputs the higher “Normal” voltage. During PCIRST#, the output driver is disabled and an internal pull-down is enabled. This is needed for implementing a strap on the pin. When PCIRST# deasserts, the output driver is enabled. To guarantee no glitches on the DPRSLPVR pin, the pull-down is disabled after the output driver is fully enabled. **NOTE:** DPRSLPVR is sampled at the rising edge of PWROK as a functional strap.

Processor Interface Signals

Signal Name	Type	Description
A20M#	O	**Mask A20:** A20M# will go active based on either setting the appropriate bit in the Port 92h register, or based on the A20GATE input being active. **Speed Strap:** During the reset sequence, ICH4 drives A20M# high if the corresponding bit is set in the FREQ_STRP register.
CPUSLP#	O	**CPU Sleep:** This signal puts the processor into a state that saves substantial power compared to Stop-Grant state. However, during that time, no snoops occur. The ICH4 can optionally assert the CPUSLP# signal when going to the S1-M state.
FERR#	I	**Numeric Coprocessor Error:** This signal is tied to the coprocessor error signal on the processor. FERR# is only used if the ICH4 coprocessor error reporting function is enabled in the General Control Register (Device 31:Function 0, Offset D0, bit 13). If FERR# is asserted, the ICH4 generates an internal IRQ13 to its interrupt controller unit. It is also used to gate the IGNNE# signal to ensure that IGNNE# is not asserted to the processor unless FERR# is active. FERR# requires an external weak pull-up to ensure a high level when the coprocessor error function is disabled. **NOTE:** FERR# can be used in some states for notification by the processor of pending interrupt events. This functionality is independent of the General Control Register bit setting.
INTR	O	**CPU Interrupt:** INTR is asserted by the ICH4 to signal the processor that an interrupt request is pending and needs to be serviced. It is an asynchronous output and normally driven low. **Speed Strap:** During the reset sequence, ICH4 drives INTR high if the corresponding bit is set in the FREQ_STRP register.
IGNNE#	O	**Ignore Numeric Error:** This signal is connected to the ignore error pin on the processor. IGNNE# is only used if the ICH4 coprocessor error reporting function is enabled in the General Control Register (Device 31:Function 0, Offset D0, bit 13). If FERR# is active, indicating a coprocessor error, a write to the Coprocessor Error Register (F0h) causes the IGNNE# to be asserted. IGNNE# remains asserted until FERR# is negated. If FERR# is not asserted when the Coprocessor Error Register is written, the IGNNE# signal is not asserted. **Speed Strap:** During the reset sequence, ICH4 drives IGNNE# high if the corresponding bit is set in the FREQ_STRP register.
INIT#	O	**Initialization:** INIT# is asserted by the ICH4 for 16 PCI clocks to reset the processor. ICH4 can be configured to support CPU BIST. In that case, INIT# will be active when PCIRST# is active.
NMI	O	**Non-Maskable Interrupt:** NMI is used to force a non-Maskable interrupt to the processor. The ICH4 can generate an NMI when either SERR# or IOCHK# is asserted. The processor detects an NMI when it detects a rising edge on NMI. NMI is reset by setting the corresponding NMI source enable/disable bit in the NMI Status and Control Register. **Speed Strap:** During the reset sequence, ICH4 drives NMI high if the corresponding bit is set in the FREQ_STRP register.
SMI#	O	**System Management Interrupt:** SMI# is an active low output synchronous to PCICLK. It is asserted by the ICH4 in response to one of many enabled hardware or software events.
STPCLK#	O	**Stop Clock Request:** STPCLK# is an active low output synchronous to PCICLK. It is asserted by the ICH4 in response to one of many hardware or software events. When the processor samples STPCLK# asserted, it responds by stopping its internal clock.
RCIN#	I	**Keyboard Controller Reset CPU:** The keyboard controller can generate INIT# to the processor. This saves the external OR gate with the ICH4’s other sources of INIT#. When the ICH4 detects the assertion of this signal, INIT# is generated for 16 PCI clocks. **NOTE:** The ICH4 ignores RCIN# assertion during transitions to the S1-M, S3, S4 and S5 states.
A20GATE	I	**A20 Gate:** A20GATE is from the keyboard controller. The signal acts as an alternative method to force the A20M# signal active. It saves the external OR gate needed with various other PCIsets.

5.3 Intel 82801DBM I/O Controller Hub 4 Mobile (ICH4-M)

Processor Interface Signals (Continued)

Signal Name	Type	Description
CPUPWRGD	OD	**CPU Power Good:** This signal should be connected to the processor's PWRGOOD input. To allow for Intel ® SpeedStep™ technology support, this signal is kept high during an Intel SpeedStep technology state transition to prevent loss of processor context. This is an open-drain output signal (external pull-up resistor required) that represents a logical AND of the ICH4's PWROK and VGATE / VRMPWRGD signals.
DPSLP#	O	**Deeper Sleep:** This signal is asserted by the ICH4 to the processor. When the signal is low, the processor enters the Deeper Sleep state by gating off the processor Core clock inside the processor. When the signal is high (default), the processor is not in the Deeper Sleep state. This signal behaves identically to the STP_CPU# signal, but at the processor voltage level.

SMBus Interface Signals

Signal Name	Type	Description
SMBDATA	I/OD	**SMBus Data:** External pull-up is required.
SMBCLK	I/OD	**SMBus Clock:** External pull-up is required.
SMBALERT#/ GPIO[11]	I	**SMBus Alert:** This signal is used to wake the system or generate SMI#. If not used for SMBALERT#, it can be used as a GPI.

System Management Interface Signals

Signal Name	Type	Description
INTRUDER#	I	**Intruder Detect:** Can be set to disable system if box detected open. This signal's status is readable, so it can be used like a GPI if the Intruder Detection is not needed.
SMLINK[1:0]	I/OD	**System Management Link:** SMBus link to optional external system management ASIC or LAN controller. External pull-ups are required. Note that SMLINK[0] corresponds to an SMBus Clock signal, and SMLINK[1] corresponds to an SMBus Data signal.

Real Time Clock Interface Signals

Signal Name	Type	Description
RTCX1	Special	**Crystal Input 1:** This signal is connected to the 32.768 kHz crystal.
RTCX2	Special	**Crystal Input 2:** This signal is connected to the 32.768 kHz crystal.

Other Clock Signals

Signal Name	Type	Description
CLK14	I	**Oscillator Clock:** Used for 8254 timers. It runs at 14.31818 MHz. This clock is permitted to stop during S1-M (or lower) states.
CLK48	I	**48 MHz Clock:** This clock is used to run the USB controller. It runs at 48 MHz. This clock is permitted to stop during S1-M (or lower) states.
CLK66	I	**66 MHz Clock:** This is used to run the hub interface. It runs at 66 MHz. This clock is permitted to stop during S1-M (or lower) states.

Miscellaneous Signals

Signal Name	Type	Description
SPKR	O	**Speaker:** The SPKR signal is the output of counter 2 and is internally "ANDed" with Port 61h bit 1 to provide Speaker Data Enable. This signal drives an external speaker driver device, which in turn drives the system speaker. Upon PCIRST#, its output state is 0. **NOTE:** SPKR is sampled at the rising edge of PWROK as a functional strap.
RTCRST#	I	**RTC Reset:** When asserted, this signal resets register bits in the RTC well and sets the RTC_PWR_STS bit (bit 2 in GEN_PMCON3 register). **NOTES:** 1. Clearing CMOS in an ICH4-based platform can be done by using a jumper on RTCRST# or GPI, or using SAFEMODE strap. Implementations should not attempt to clear CMOS by using a jumper to pull VccRTC low. 2. Unless entering the XOR Chain Test Mode, the RTCRST# input must always be high when all other RTC power planes are on.

5.3 Intel 82801DBM I/O Controller Hub 4 Mobile (ICH4-M)

AC'97 Link Signals

Signal Name	Type	Description
AC_RST#	O	**AC '97 Reset:** This signal is a master hardware reset to external Codec(s).
AC_SYNC	O	**AC '97 Sync:** This signal is a 48 kHz fixed rate sample sync to the Codec(s).
AC_BIT_CLK	I	**AC97 Bit Clock:** This signal is a 12.288 MHz serial data clock generated by the external Codec(s). This signal has an integrated pull-down resistor.
AC_SDOUT	O	**AC97 Serial Data Out:** Serial TDM data output to the Codec(s). **NOTE:** AC_SDOUT is sampled at the rising edge of PWROK as a functional strap.
AC_SDIN[1:0]	I	**AC97 Serial Data In 2:**0: These signals are Serial TDM data inputs from the three Codecs.

NOTE: An integrated pull-down resistor on AC_BIT_CLK is enabled when either: The ACLINK Shutoff bit in the AC'97 Global Control Register is set to 1, or Both Function 5 and Function 6 of Device 31 are disabled. Otherwise, the integrated pull-down resistor is disabled.

General Purpose I/O Signals

Signal Name	Type	Description
GPIO[43:32]	I/O	Can be input or output. Main power well.
GPIO[31:29]	O	Not implemented.
GPIO[28:27]	I/O	Can be input or output. Resume power well. Unmuxed.
GPIO[26]	I/O	Not implemented.
GPIO[25]	I/O	Can be input or output. Resume power well. Unmuxed.
GPIO[24:18]	I/O	Not Implemented in Mobile (Assign to native Functionality).
GPIO[17:16]	O	Fixed as Output only. Main power well. Can be used instead as PC/PCI GNT[A:B]#. GPIO[17] can also alternatively be used for PCI GNT[5]#. Integrated pull-up resistor.
GPIO[15:14]	I	Not implemented.
GPIO[13:12]	I	Fixed as Input only. Resume power well. Unmuxed.
GPIO[11]	I	Fixed as Input only. Resume power well. Can be used instead as SMBALERT#.
GPIO[10:9]	I	Not implemented.
GPIO[8]	I	Fixed as Input only. Resume power well. Unmuxed.
GPIO[7]	I	Fixed as Input only. Main power well. Unmuxed.
GPIO[6]	I	Not Implemented in Mobile (Assign to Native Functionality)
GPIO[5:2]	I	Fixed as Input only. Main power well. Can be used instead as PIRQ[E:H]#.
GPIO[1:0]	I	Fixed as Input only. Main power well. Can be used instead as PC/PCI REQ[A:B]#. GPIO[1] can also alternatively be used for PCI REQ[5]#.

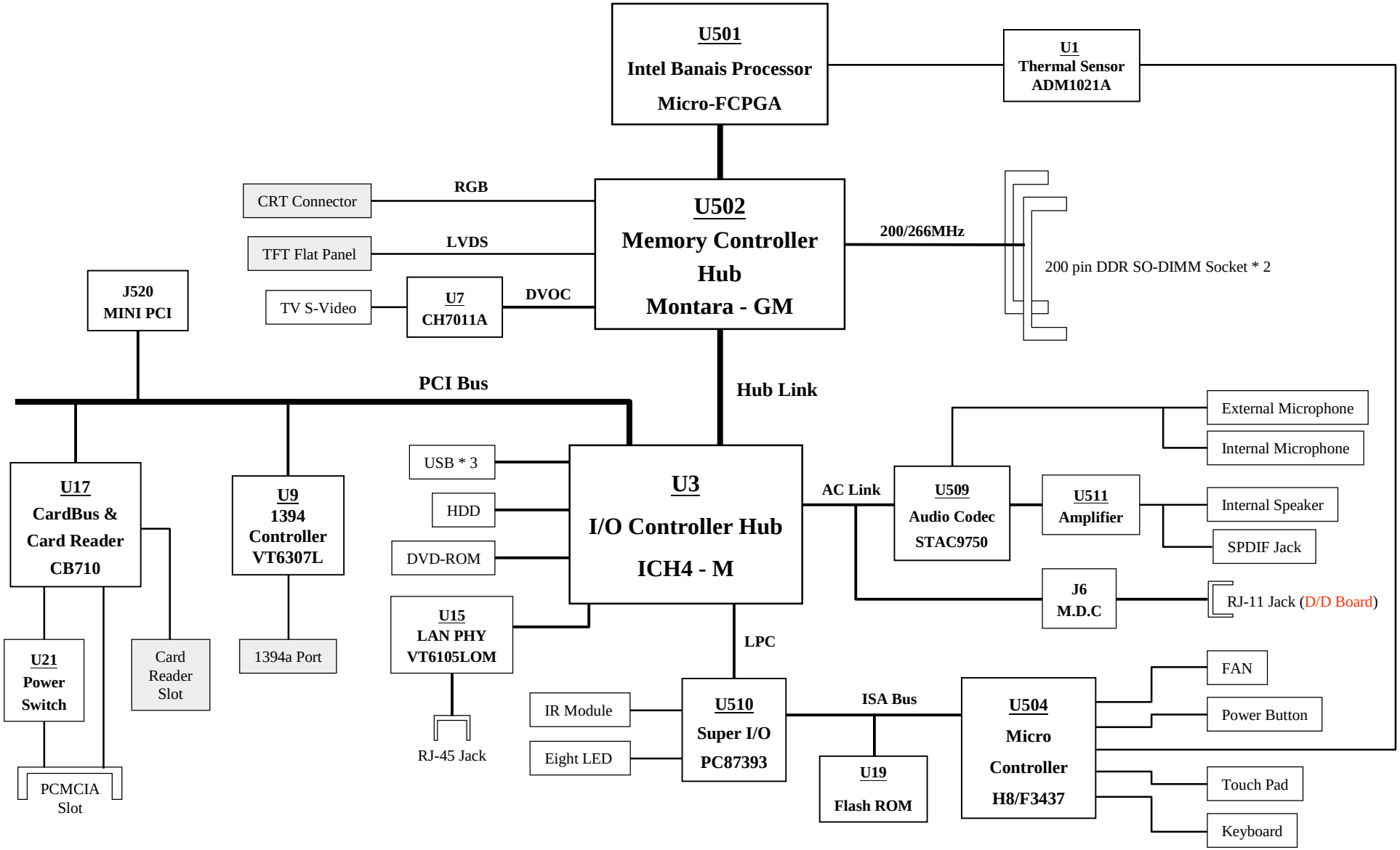
NOTE: Main power well GPIO are 5V tolerant, except for GPIO[43:32]. Resume power well GPIO are not 5V tolerant.

Power and Ground Signals

Signal Name	Description
VCC3_3	3.3 V supply for core well I/O buffers. This power may be shut off in S3, S4, S5 or G3 states.
VCC1_5	1.5 V supply for core well logic. This power may be shut off in S3, S4, S5 or G3 states.
VCCHI	1.5 V supply for Hub Interface 1.5 logic. 1.8 V supply for Hub Interface 1.0 logic. This power may be shut off in S3, S4, S5 or G3 states.
V5REF	Reference for 5 V tolerance on core well inputs. This power may be shut off in S3, S4, S5 or G3 states.
HIREF	Analog Input. Expected voltages are: • 0.9 V for HI 1.0 (Normal Hub Interface) Series Termination • 350 mV for HI 1.5 (Enhanced Hub Interface) Parallel Termination This power is shut off in S3, S4, S5, and G3 states.
VCCSUS3_3	3.3 V supply for resume well I/O buffers. This power is not expected to be shut off unless the main battery is removed or completely drained and AC power is not available.
VCCSUS1_5	1.5 V supply for resume well logic. This power is not expected to be shut off unless the main battery is removed or completely drained and AC power is not available.
V5REF_SUS	Reference for 5 V tolerance on resume well inputs. This power is not expected to be shut off unless the main battery is removed or completely drained and AC power is not available.
VCCLAN3_3	3.3 V supply for LAN Connect interface buffers. This is a separate power plane that may or may not be powered in S3–S5 states depending upon the presence or absence of AC power and network connectivity. This plane must be on in S0 and S1-M.
VCCLAN1_5	1.5 V supply for LAN Controller logic. This is a separate power plane that may or may not be powered in S3–S5 states depending upon the presence or absence of AC power and network connectivity. This plane must be on in S0 and S1-M.
VCCRTC	3.3 V (can drop to 2.0 V min. in G3 state) supply for the RTC well. This power is not expected to be shut off unless the RTC battery is removed or completely drained. **NOTE:** Implementations should not attempt to clear CMOS by using a jumper to pull VccRTC low. Clearing CMOS in an ICH4-based platform can be done by using a jumper on RTCRST# or GPI, or using SAFEMODE strap.
VCCPLL	1.5 V supply for core well logic. This signal is used for the USB PLL. This power may be shut off in S3, S4, S5 or G3 states.
VBIAS	RTC well bias voltage. The DC reference voltage applied to this pin sets a current that is mirrored throughout the oscillator and buffer circuitry.
V_CPU_IO	Powered by the same supply as the processor I/O voltage. This supply is used to drive the processor interface outputs.
VSS	Grounds.

8080 N/B Maintenance

6. System Block Diagram



7. Maintenance Diagnostics

7.1 Introduction

Each time the computer is turned on, the system bios runs a series of internal checks on the hardware. This power-on self test (post) allows the computer to detect problems as early as the power-on stage. Error messages of post can alert you to the problems of your computer.

If an error is detected during these tests, you will see an error message displayed on the screen. If the error occurs before the display is initialized,then the screen cannot display the error message. Error codes or system beeps are used to identify a post error that occurs when the screen is not available.

The value for the diagnostic port (378H) is written at the beginning of the test. Therefore, if the test failed, the user can determine where the problem occurred by reading the last value written to port 378H by the 378H port debug board plug at PIO PORT.

7.2 Error Codes

Following is a list of error codes in sequent display on the PIO debug board.

Code	POST Routine Description
10h	Some type of lone reset
11h	Turn off FAST A20 for POST
12h	Signal power on reset
13h	Initialize the chipset
14h	Search for ISA Bus VGA adapter
15h	Reset counter / Timer 1
16h	User register config through CMOS
17h	Size memory
18h	Dispatch to RAM test
19h	Check sum the ROM
1Ah	Reset PIC's
1Bh	Initialize video adapter(s)
1Ch	Initialize video (6845Regs)
1Dh	Initialize color adapter
1Eh	Initialize monochrome adapter
1Fh	Test 8237A page registers

Code	POST Routine Description
20h	Test keyboard
21h	Test keyboard controller
22h	Check if CMOS RAM valid
23h	Test battery fail & CMOS X-SUM
24h	Test the DMA controller
25h	Initialize 8237A controller
26h	Initialize int vectors
27h	RAM quick sizing
28h	Protected mode entered safely
29h	RAM test completed
2Ah	Protected mode exit successful
2Bh	Setup shadow
2Ch	Going to initialize video
2Dh	Search for monochrome adapter
2Eh	Search for color adapter
2Fh	Sign on messages displayed

7.2 Error Codes

Following is a list of error codes in sequent display on the PIO debug board.

Code	POST Routine Description
30h	Special init of keyboard ctlr
31h	Test if keyboard Present
32h	Test keyboard Interrupt
33h	Test keyboard command byte
34h	Test, blank and count all RAM
35h	Protected mode entered safely(2)
36h	RAM test complete
37h	Protected mode exit successful
38h	Update output port
39h	Setup cache controller
3Ah	Test if 18.2Hz periodic working
3Bh	Test for RTC ticking
3Ch	Initialize the hardware vectors
3Dh	Search and init the mouse
3Eh	Update NUMLOCK status
3Fh	Special init of COMM and LPT ports

Code	POST Routine Description
40h	Configure the COMM and LPT ports
41h	Initialize the floppies
42h	Initialize the hard disk
43h	Initialize option ROMs
44h	OEM’s init of power management
45h	Update NUMLOCK status
46h	Test for coprocessor installed
47h	OEM functions before boot
48h	Dispatch to operate system boot
49h	Jump into bootstrap code
50h	ACPI init
51h	PM init & Geyserville
52h	USB HC init

7.3 Debug Tool

8080 MB would not support Parallel Port, then we could not plug the Debug Card to PIO Port to get the Port 378 error code. For this cause, 8080 MB have reserved eight LEDs that are parallel connection with PIO output lines (Figure 1), when the system BIOS write the error code to Port 378, the LEDs can show the messages.

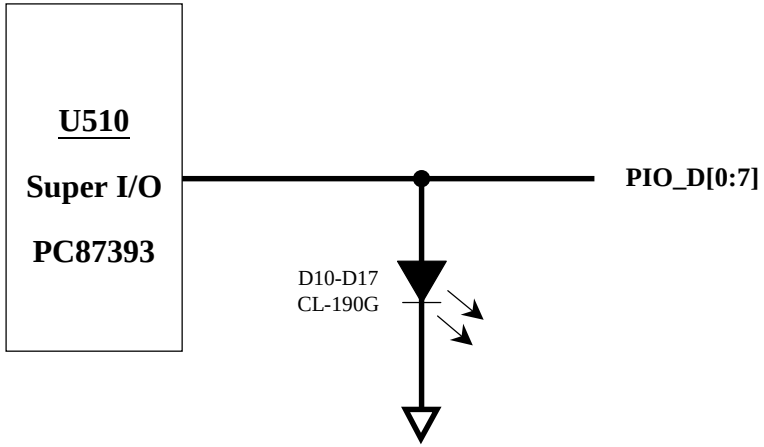


Figure 1

8. Trouble Shooting

- 8.1 No Power
- 8.2 No Display
- 8.3 VGA Controller Failure LCD No Display
- 8.4 External Monitor No Display
- 8.5 Memory Test Error
- 8.6 Keyboard (K/B) Touch-Pad (T/P) Test Error
- 8.7 Hard Driver Test Error
- 8.8 CD-ROM Driver Test Error
- 8.9 USB Port Test Error
- 8.10 Audio Failure
- 8.11 LAN Test Error
- 8.12 PC Card & Card Reader Socket Failure
- 8.13 IEEE1394 Failure

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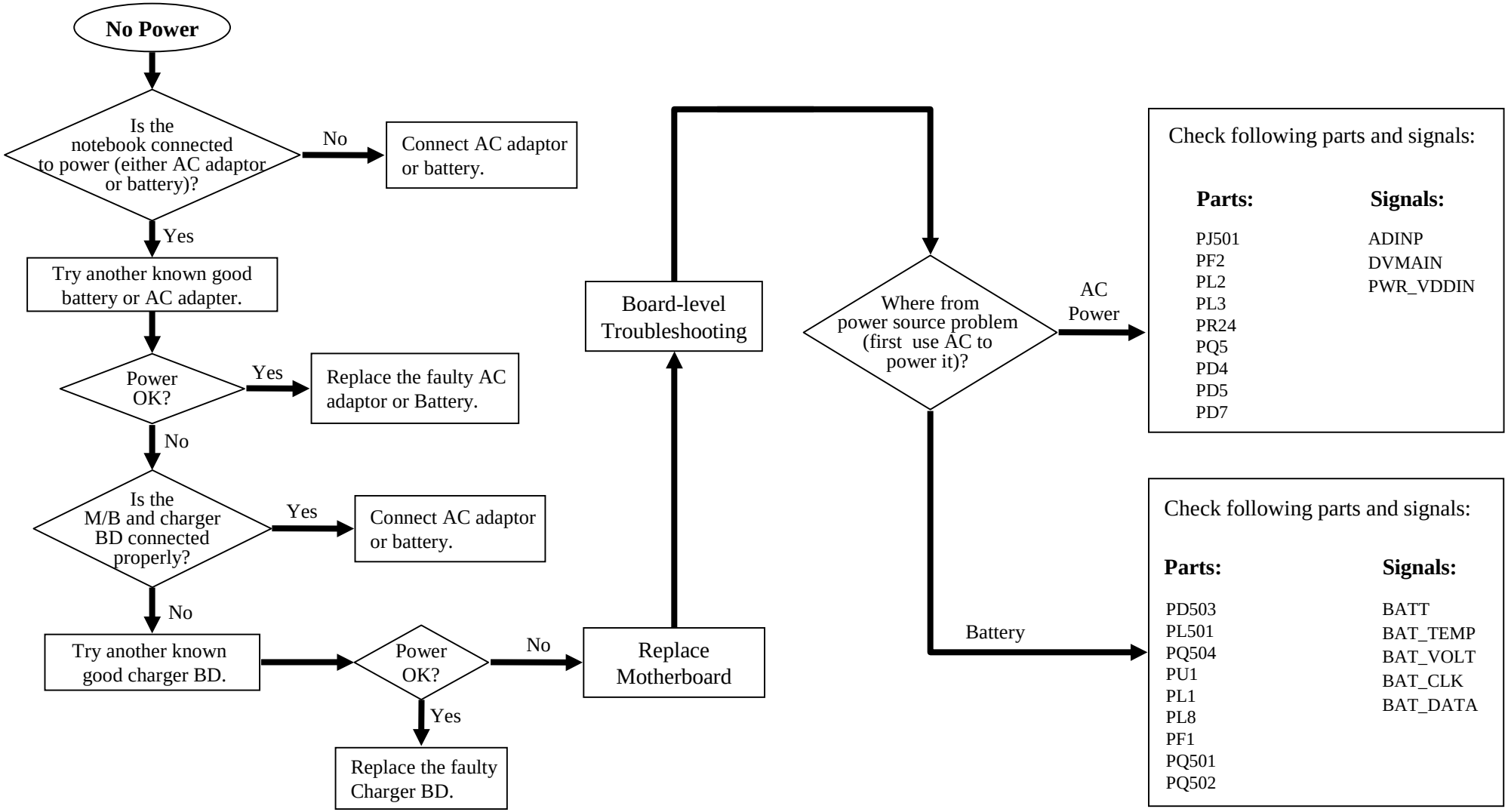
8.1 No Power

When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.

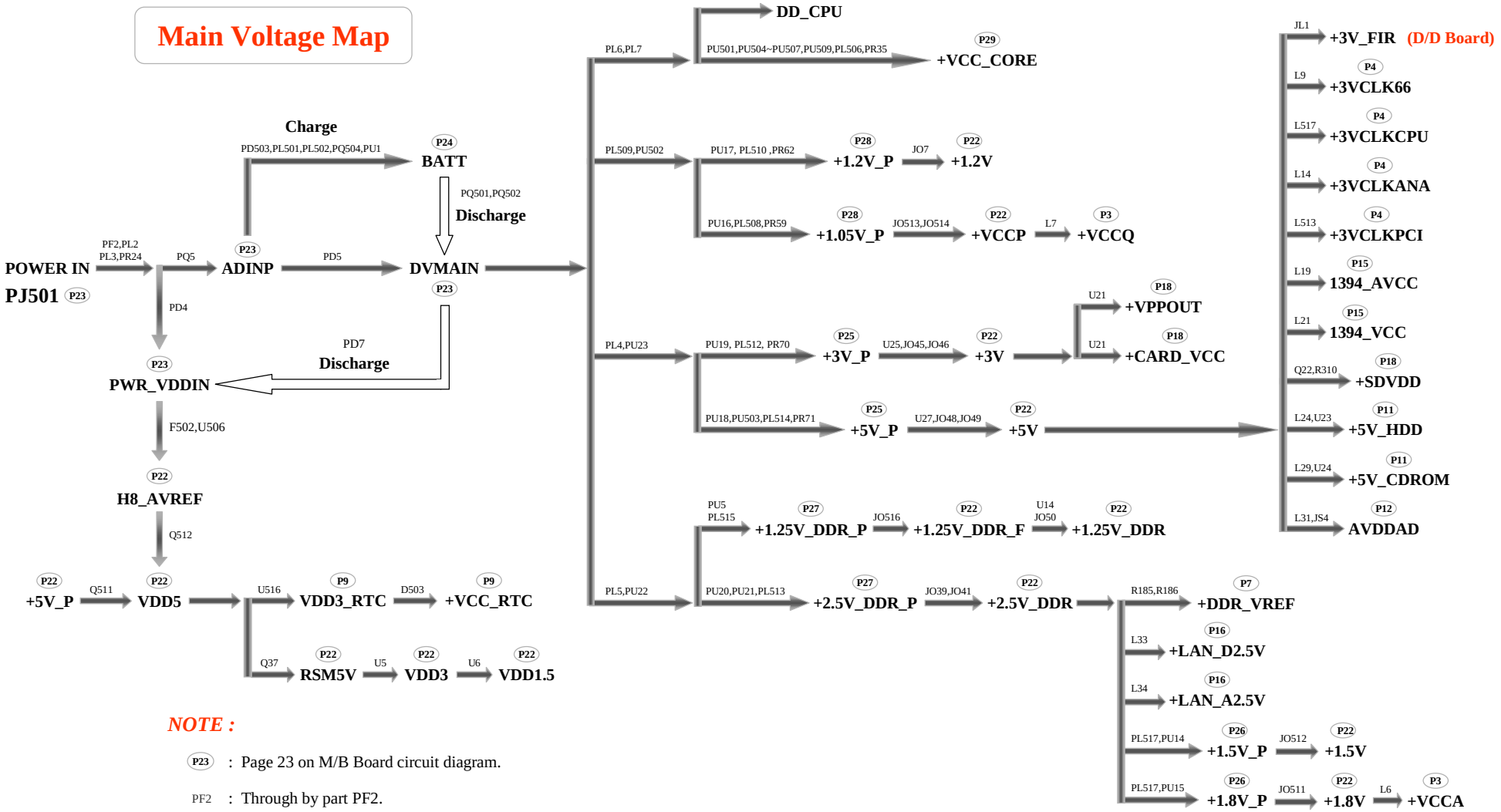


8080 N/B Maintenance

8.1 No Power

When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.

Main Voltage Map



NOTE :

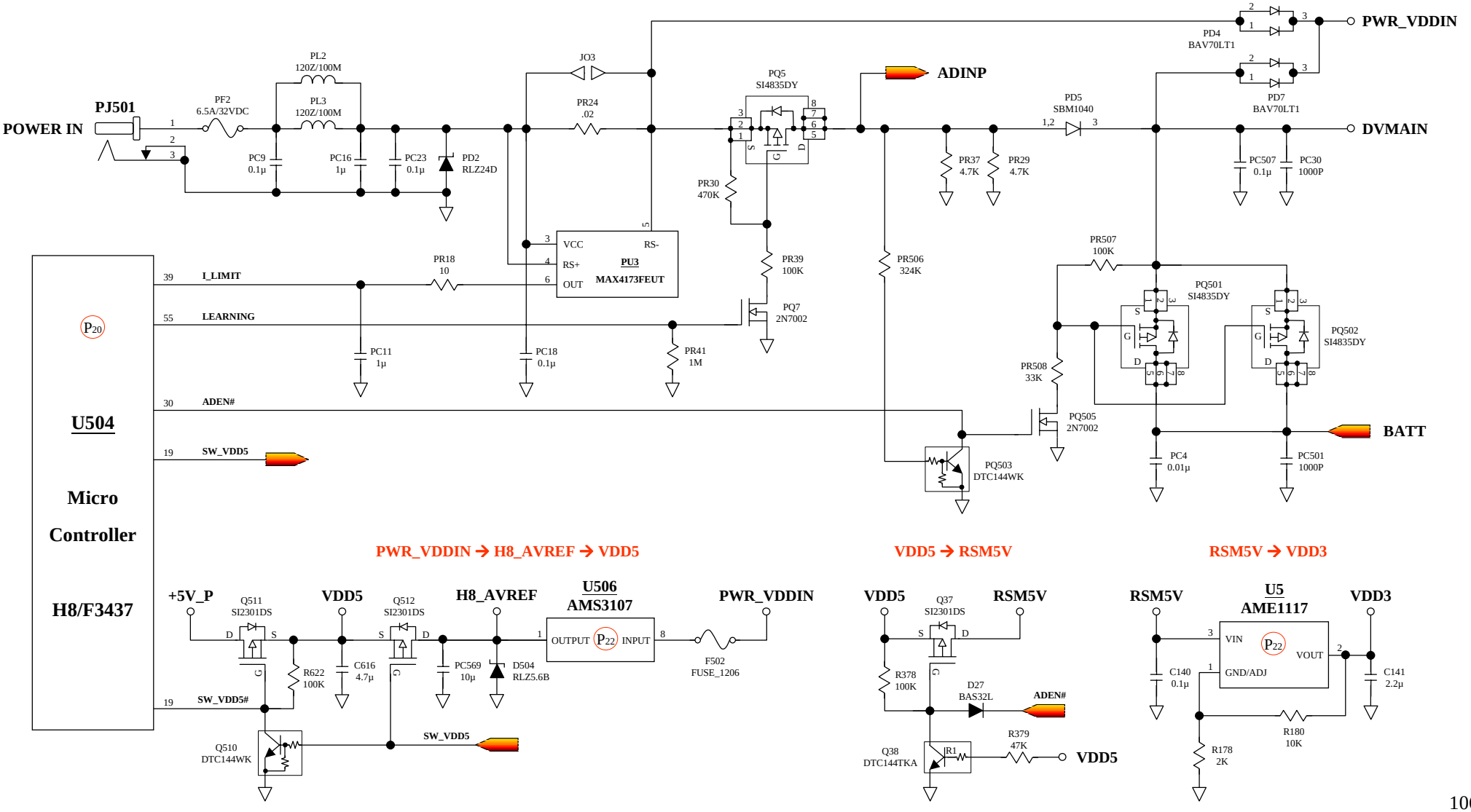
P23 : Page 23 on M/B Board circuit diagram.

PF2 : Through by part PF2.

8080 N/B Maintenance

8.1 No Power

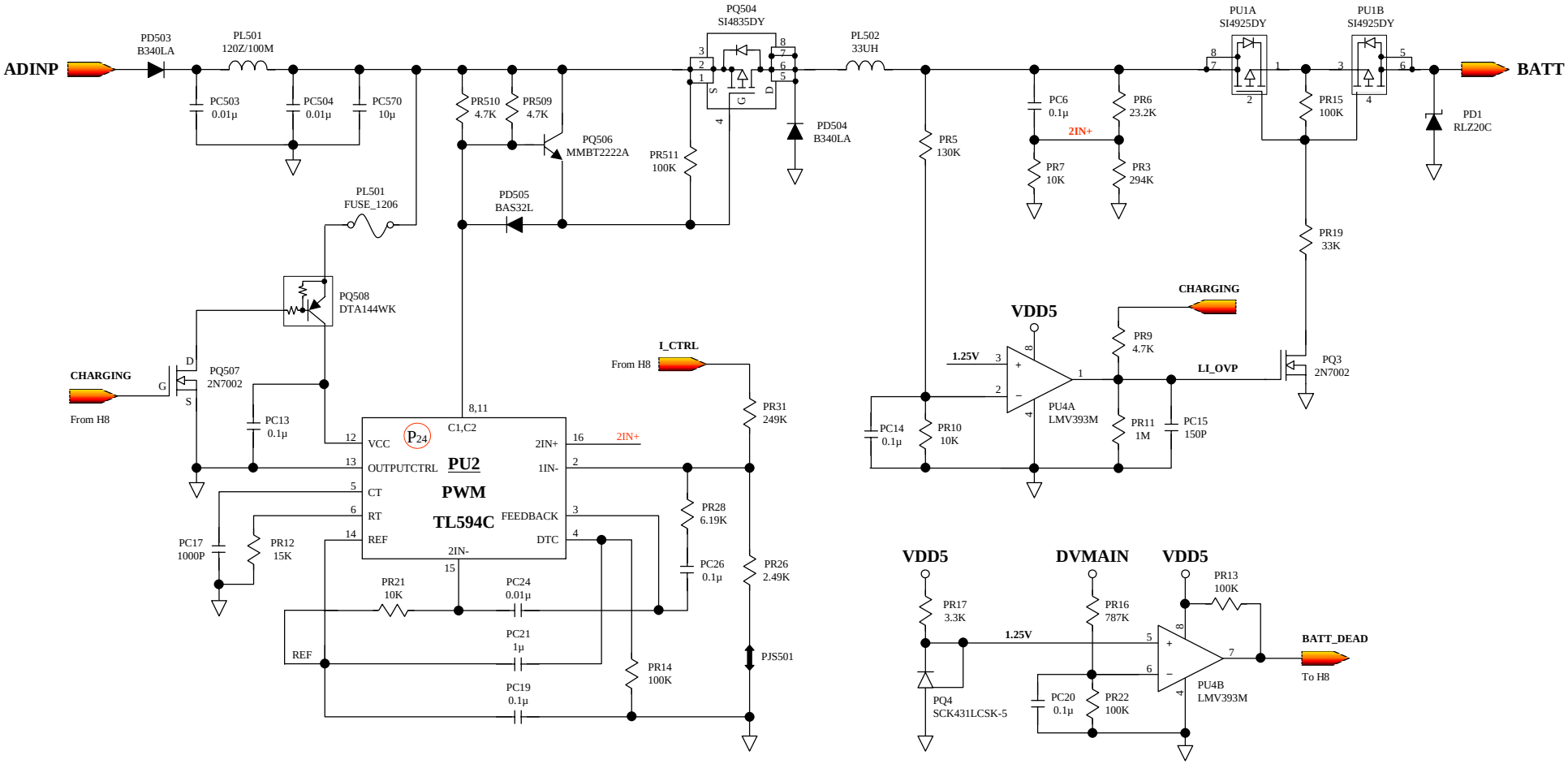
When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.



8080 N/B Maintenance

8.1 No Power

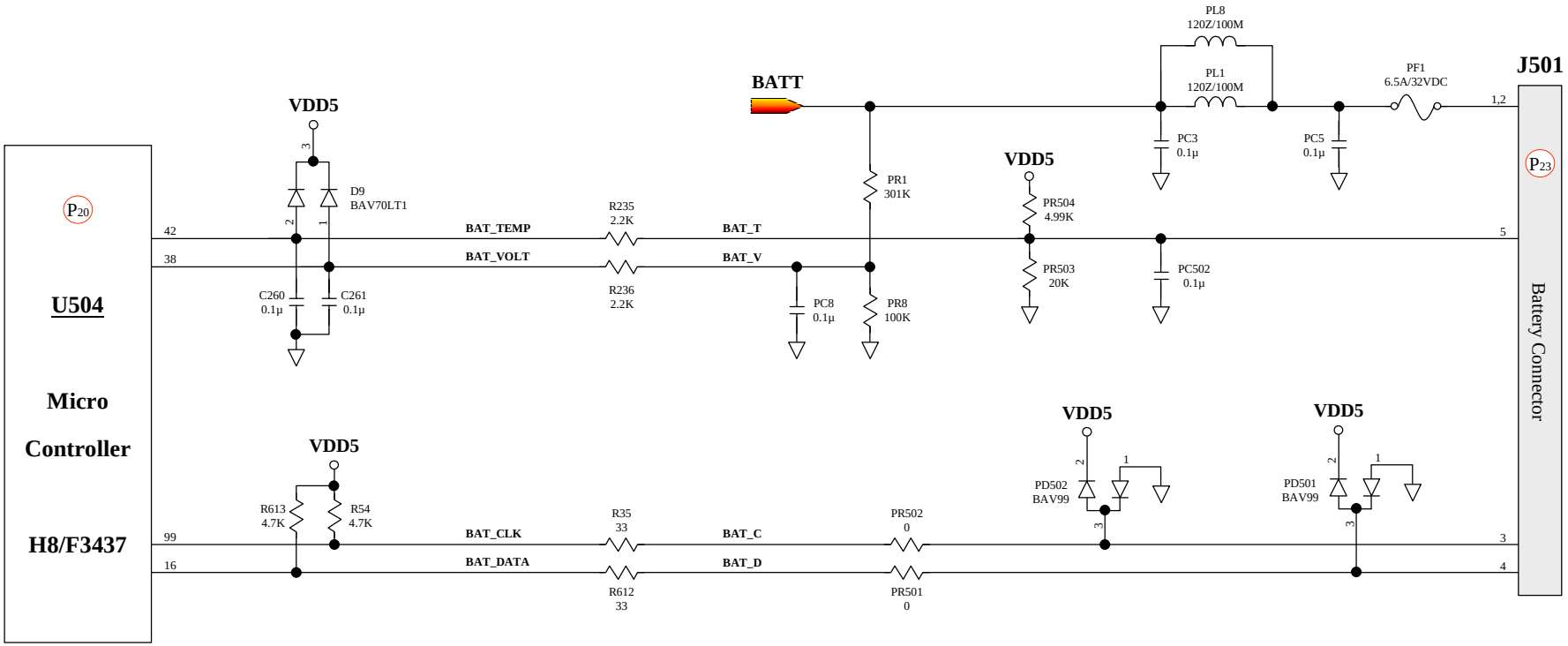
When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.



8080 N/B Maintenance

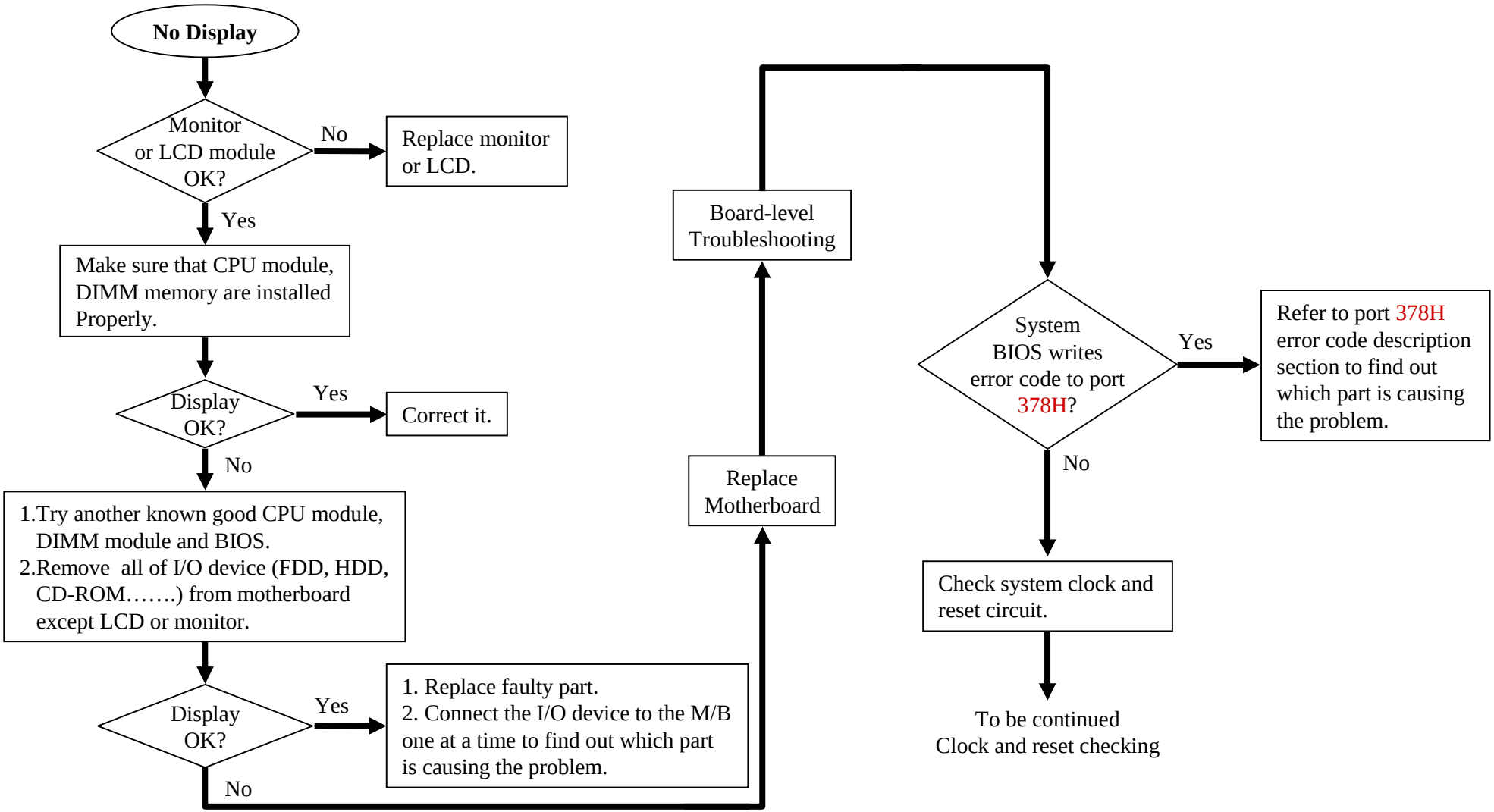
8.1 No Power

When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.



8.2 No Display

There is no display on both LCD and VGA monitor after power on although the LCD and monitor is known-good.



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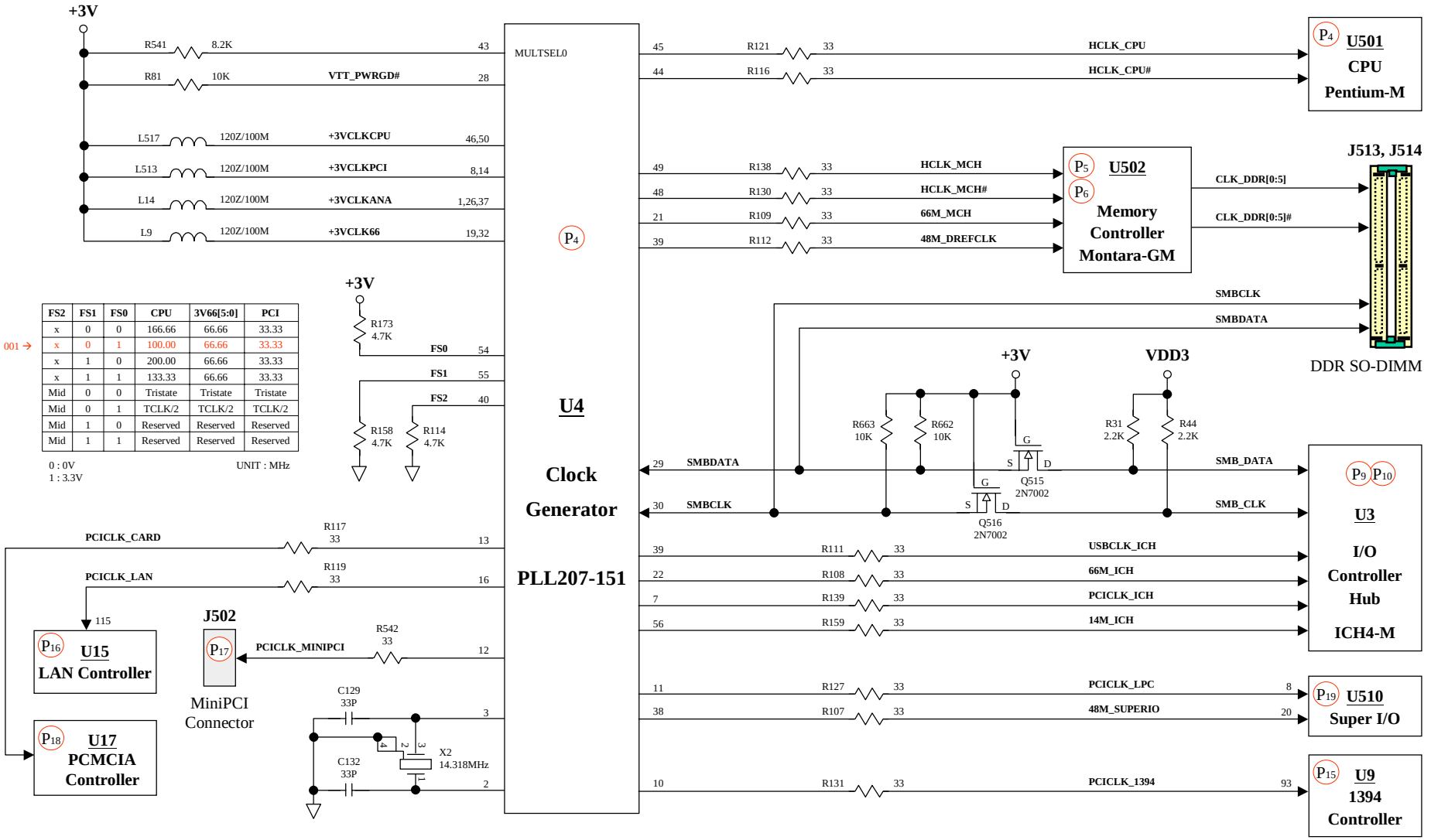
8.2 No Display

****** System Clock Check ******



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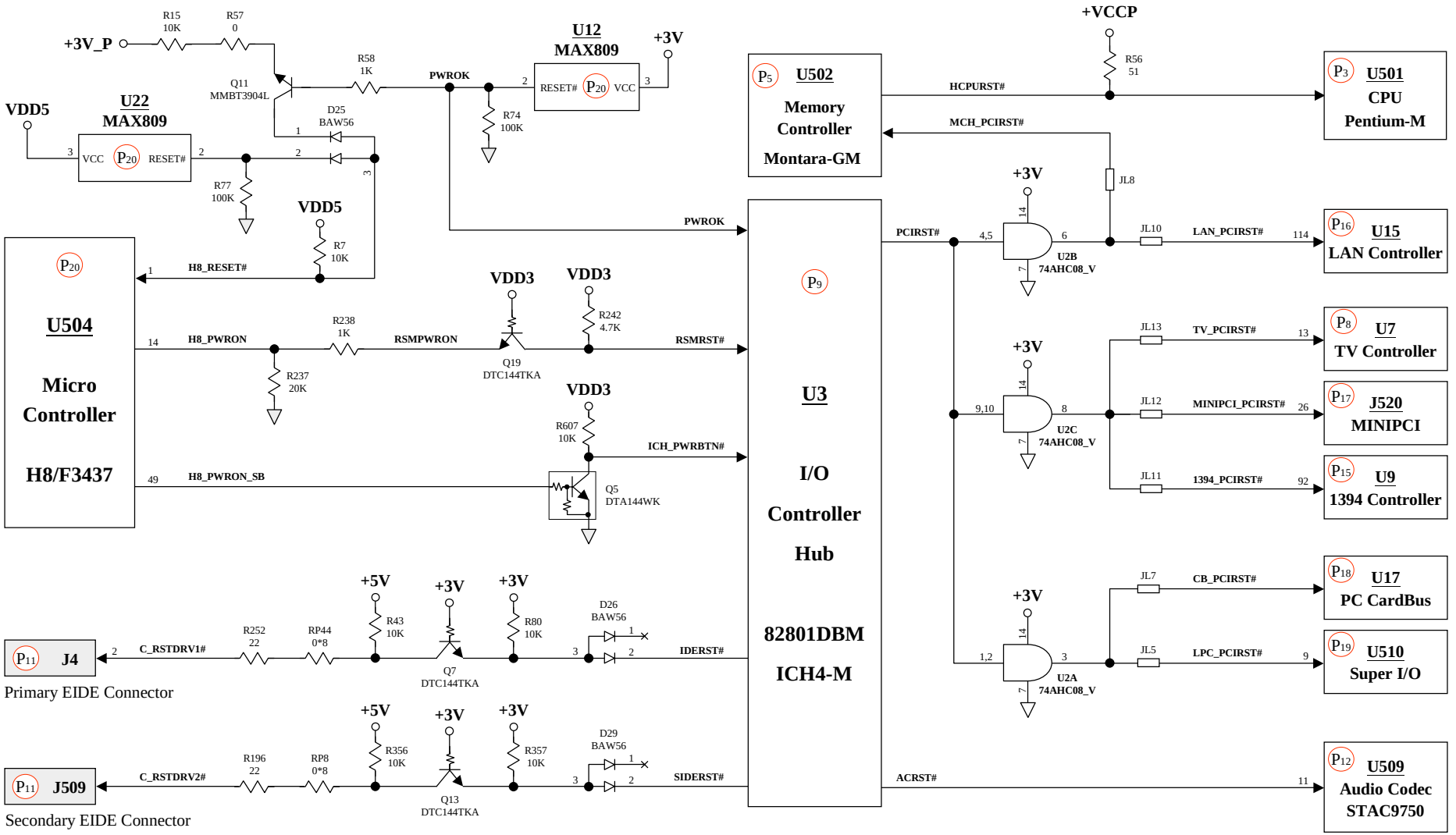
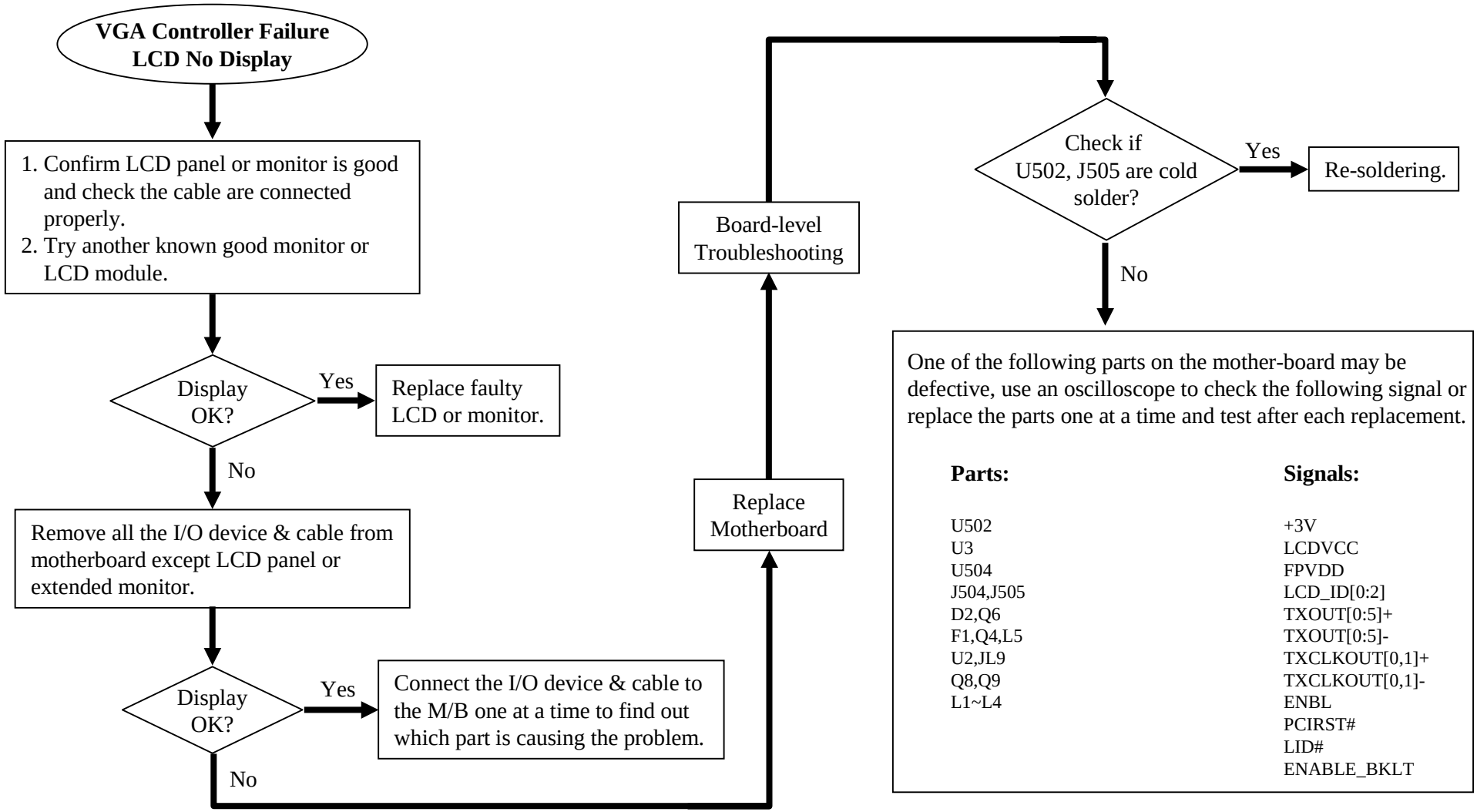
8.2 No Display

****** Power Good & Reset Circuit Check ******



8.3 VGA Controller Failure LCD No Display

There is no display or picture abnormal on LCD although power-on-self-test is passed.



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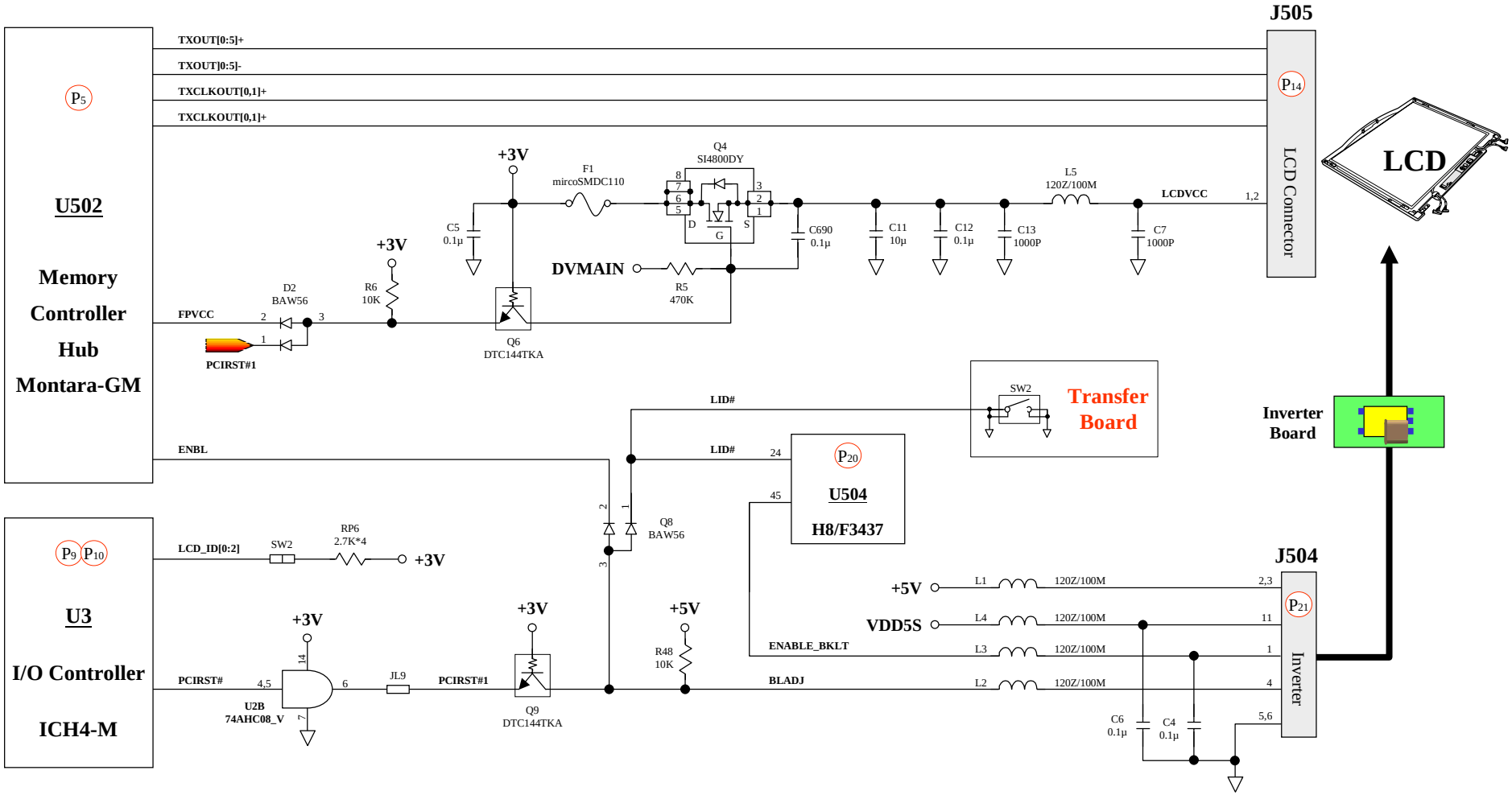
8.3 VGA Controller Failure LCD No Display

There is no display or picture abnormal on LCD although power-on-self-test is passed.



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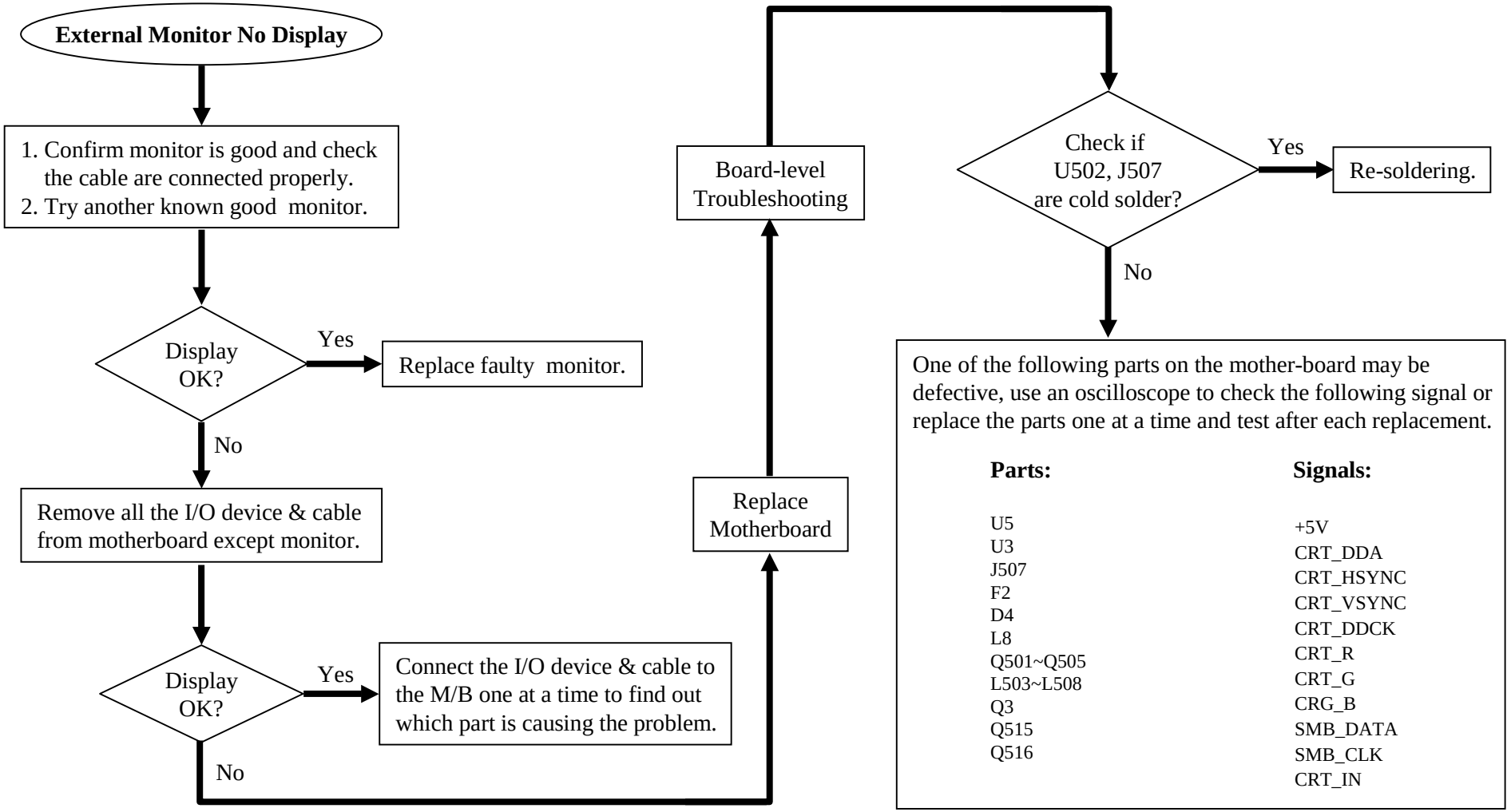
8.4 External Monitor No Display

There is no display or picture abnormal on CRT monitor, but it is OK for LCD.



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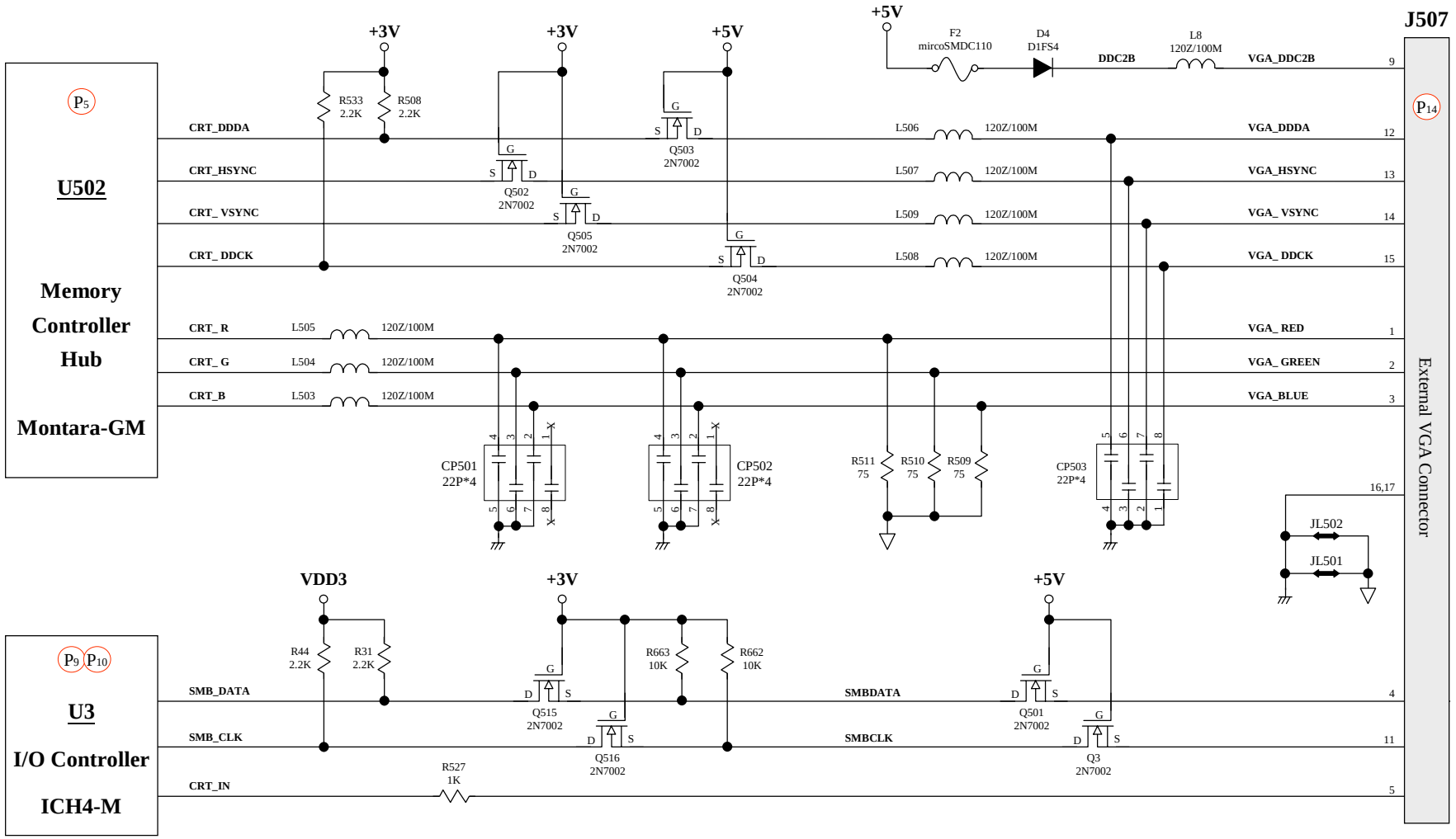
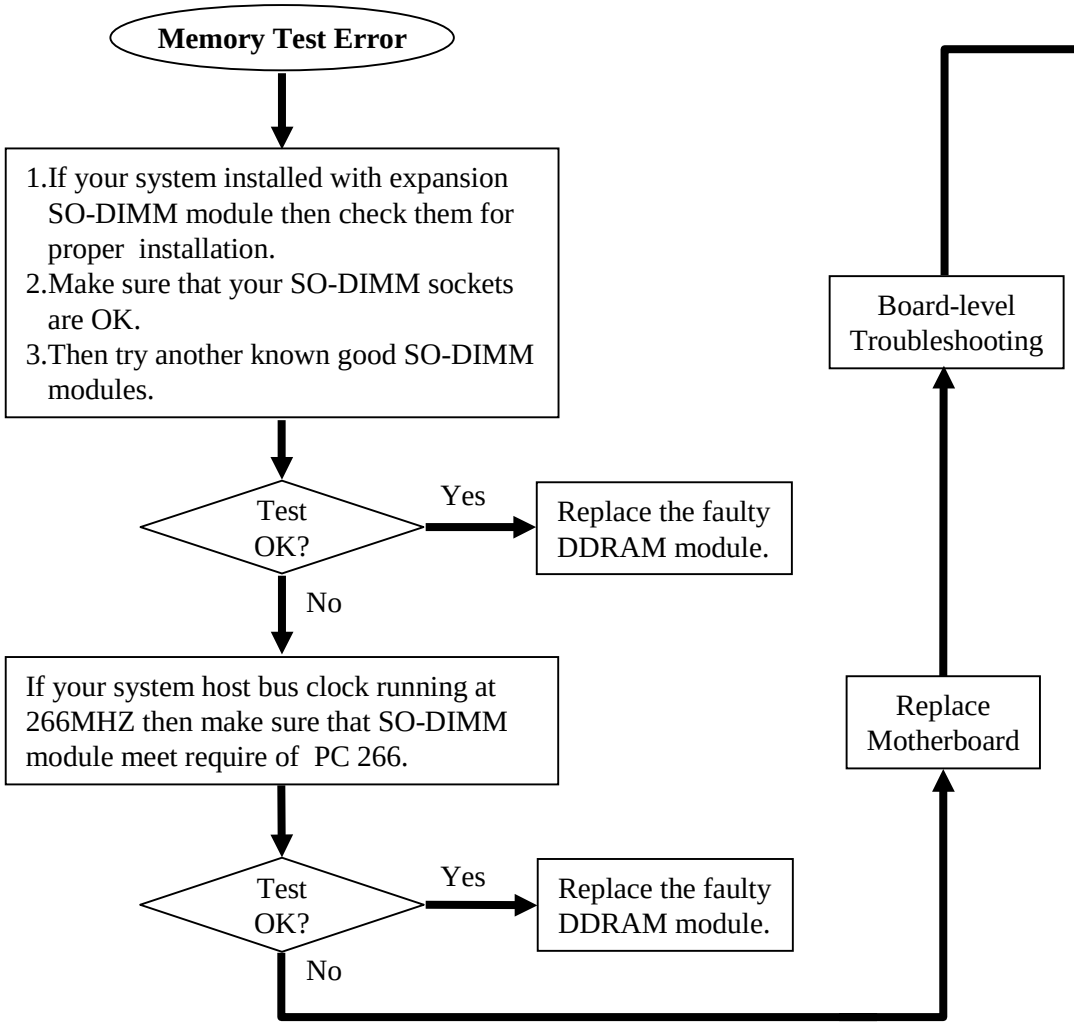
8.4 External Monitor No Display

There is no display or picture abnormal on CRT monitor, but it is OK for LCD.



8.5 Memory Test Error

Extend DDRAM is failure or system hangs up.



One of the following components or signals on the motherboard may be defective ,Use an oscilloscope to check the signals or replace the parts one at A time and test after each replacement.

Parts:

RP11	R216
RP13	R225
RP15	Q515
RP17	Q516
RP20	R138
RP22	R130
RP25	R108
RP28	U502
RP31	U3
RP33	U4
RP34	J513
RP37	J514
PR40	

Signals:

+1.25V_DDR	SMB_DATA
+2.5V_DDR	SMB_CLK
CKE [0:3],	HCLK_MCH
CS# [0:3]	HCLK_MCH#
SMA [1,2,4,5]	66M_MCH
SMAB [1,2,4,5]	CLK_DDR [0:5]
NB_MA [0,3,6:12]	CLK_DDR [0:5]#
NB_MD [0:63]	
NB_DQS [0:7],	
NB_BA [0,1]	
NB_CB [0:7],	
NB_DM [0:8]	
NB_RAS#	
NB_CAS#	
NB_WE#	

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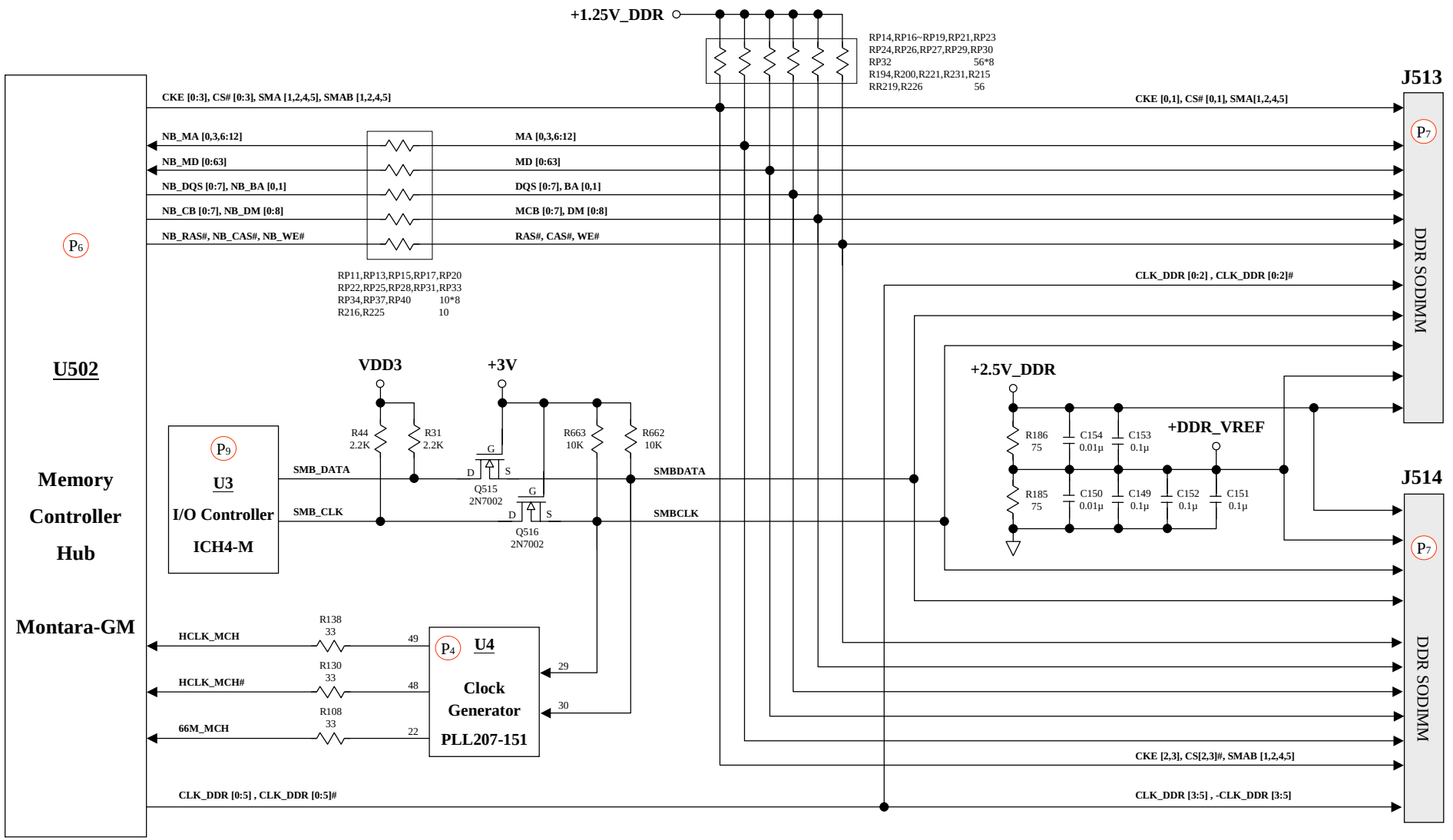
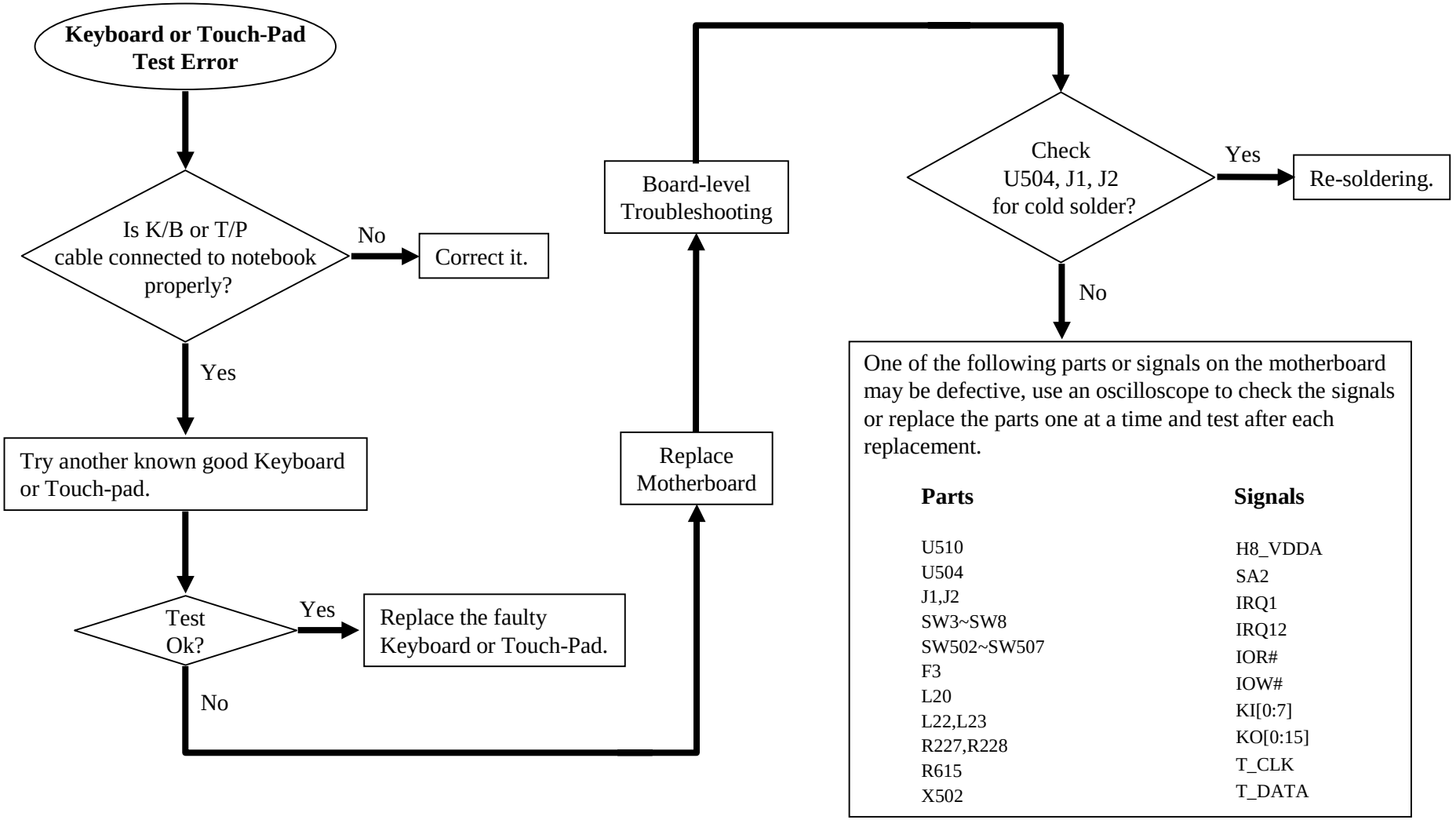
8.5 Memory Test Error

Extend DDRAM is failure or system hangs up.



8.6 Keyboard (K/B) Touch-Pad (T/P) Test Error

Error message of keyboard or touch-pad failure is shown or any key does not work.



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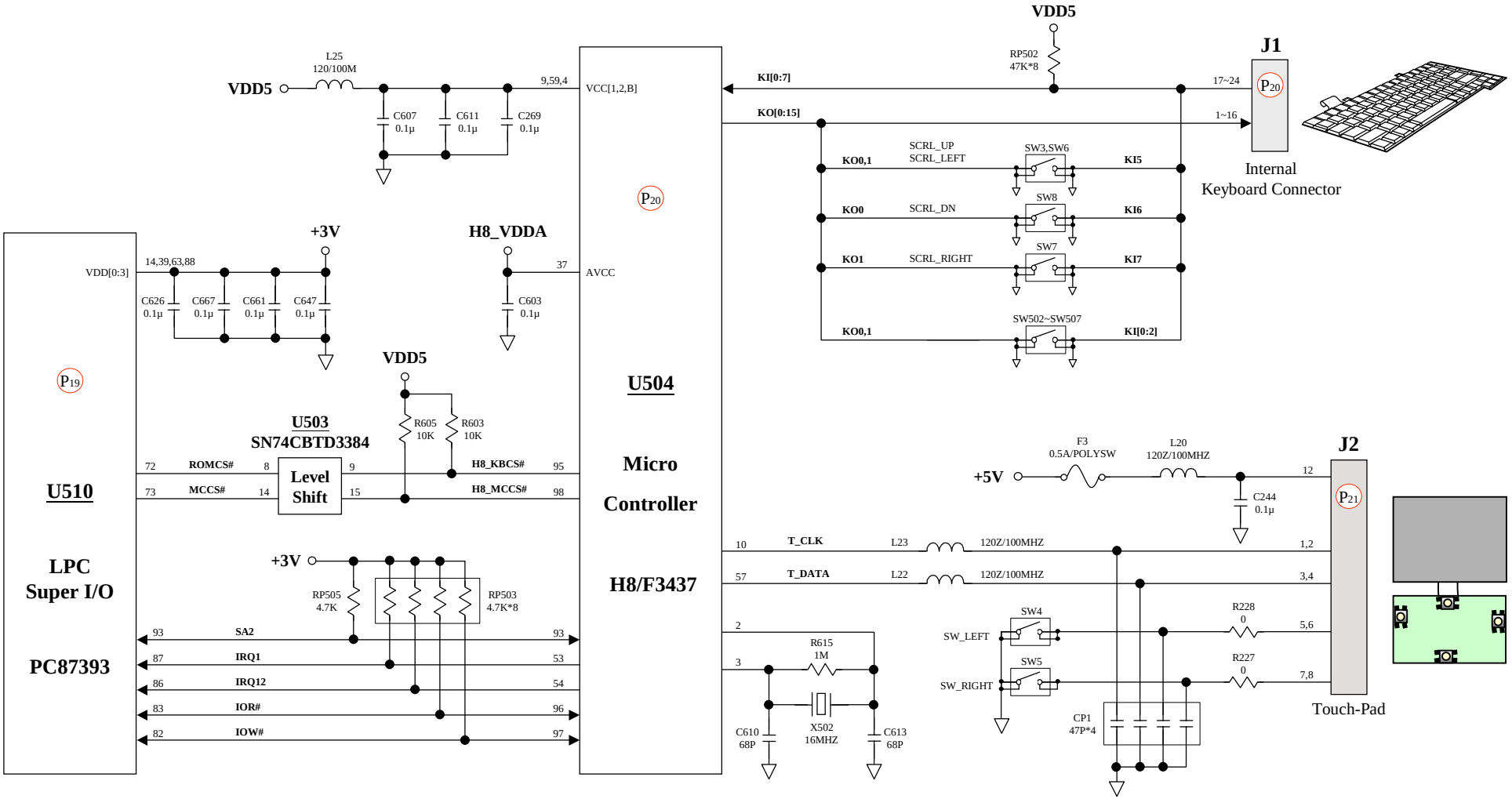
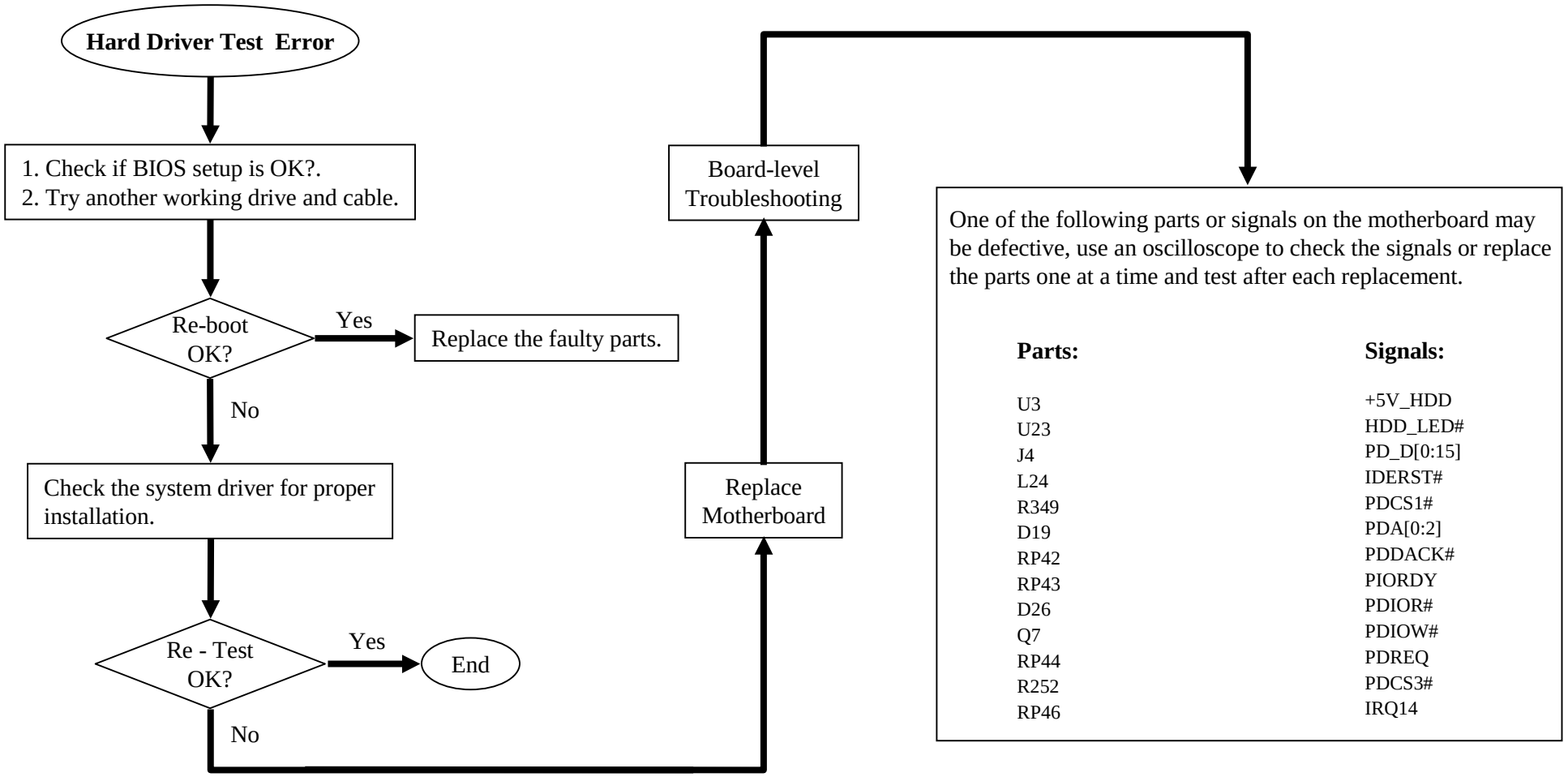
8.6 Keyboard (K/B) Touch-Pad (T/P) Test Error

Error message of keyboard or touch-pad failure is shown or any key does not work.



8.7 Hard Drive Test Error

Either an error message is shown, or the drive motor spins non-stop, while reading data from or writing data to hard disk.



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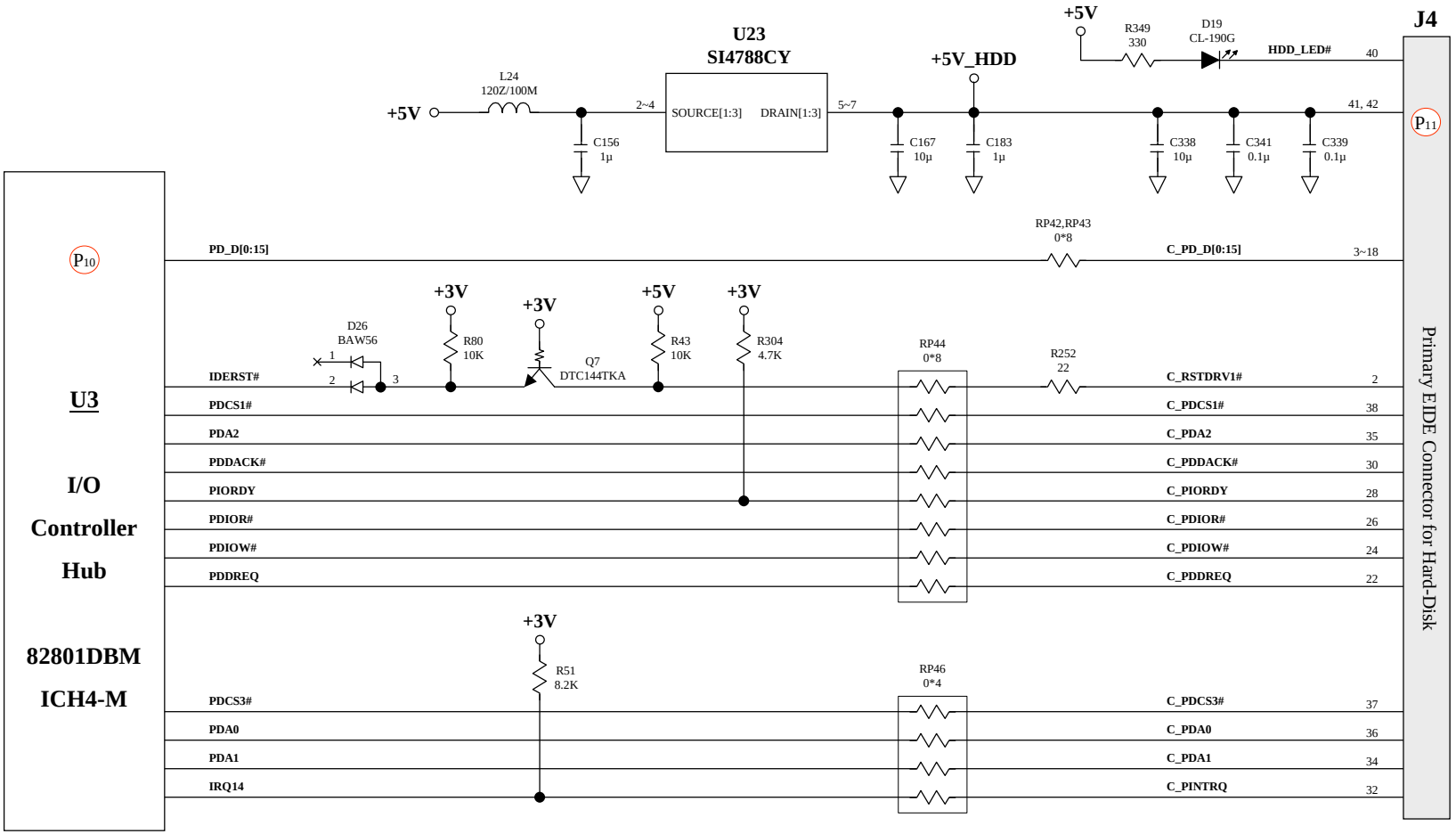
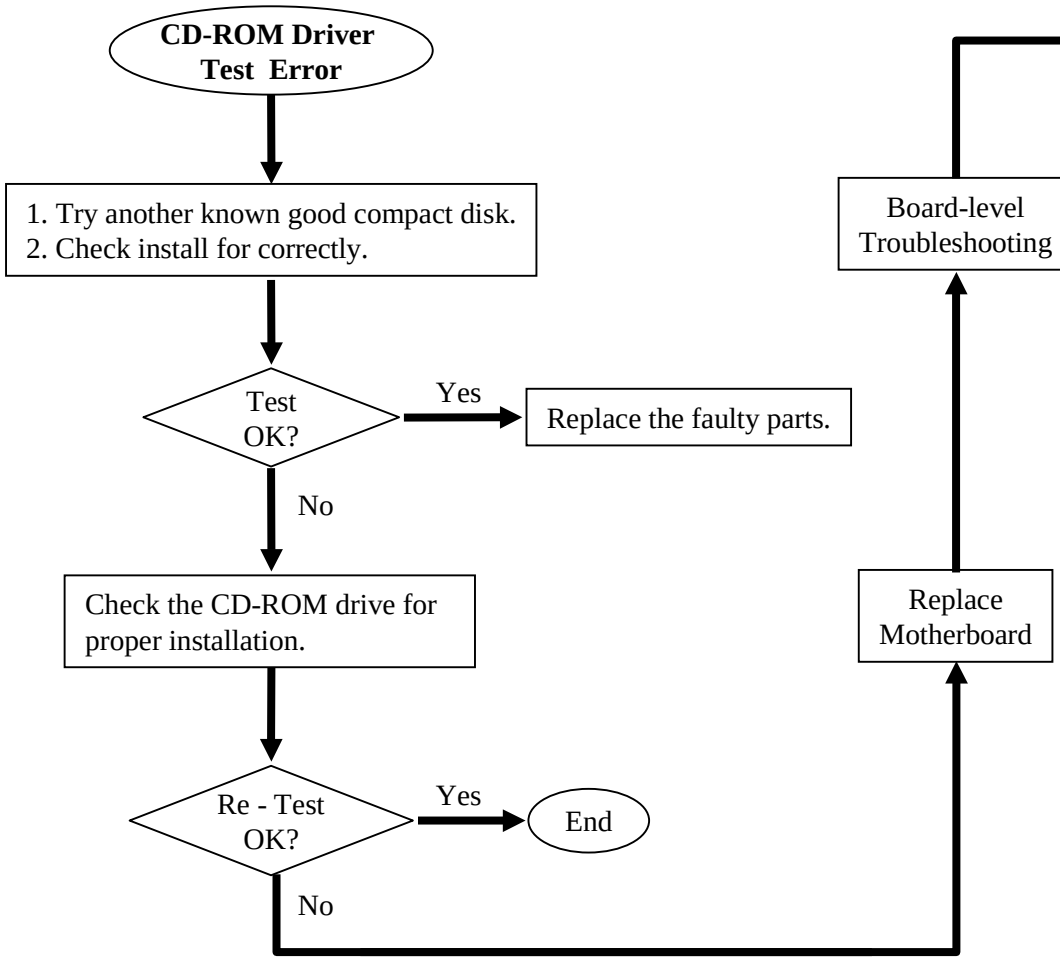
8.7 Hard Drive Test Error

Either an error message is shown, or the drive motor spins non-stop, while reading data from or writing data to hard disk.



8.8 CD-ROM Drive Test Error

An error message is shown when reading data from CD-ROM drive.



One of the following parts or signals on the motherboard may be defective, use an oscilloscope to check the signals or replace the parts one at a time and test after each replacement.

Parts:	**Signals:**
U3	+5V_CDROM
U24	CD_LED#
J509	SIDE_OFF#
D28	SD_D]0:5]
L29	SIDERST#
R352	SDA[0:2]
D18	IRQ15
D29	SDDACK#
Q13	SIORDY
RP8~RP10	SDIOW#
R196	SDDREQ
RP3	SDIOR#
R366	SDCS1#
R375	SDCS3#
	ICH_SIDE_IN#
	SIDEDET

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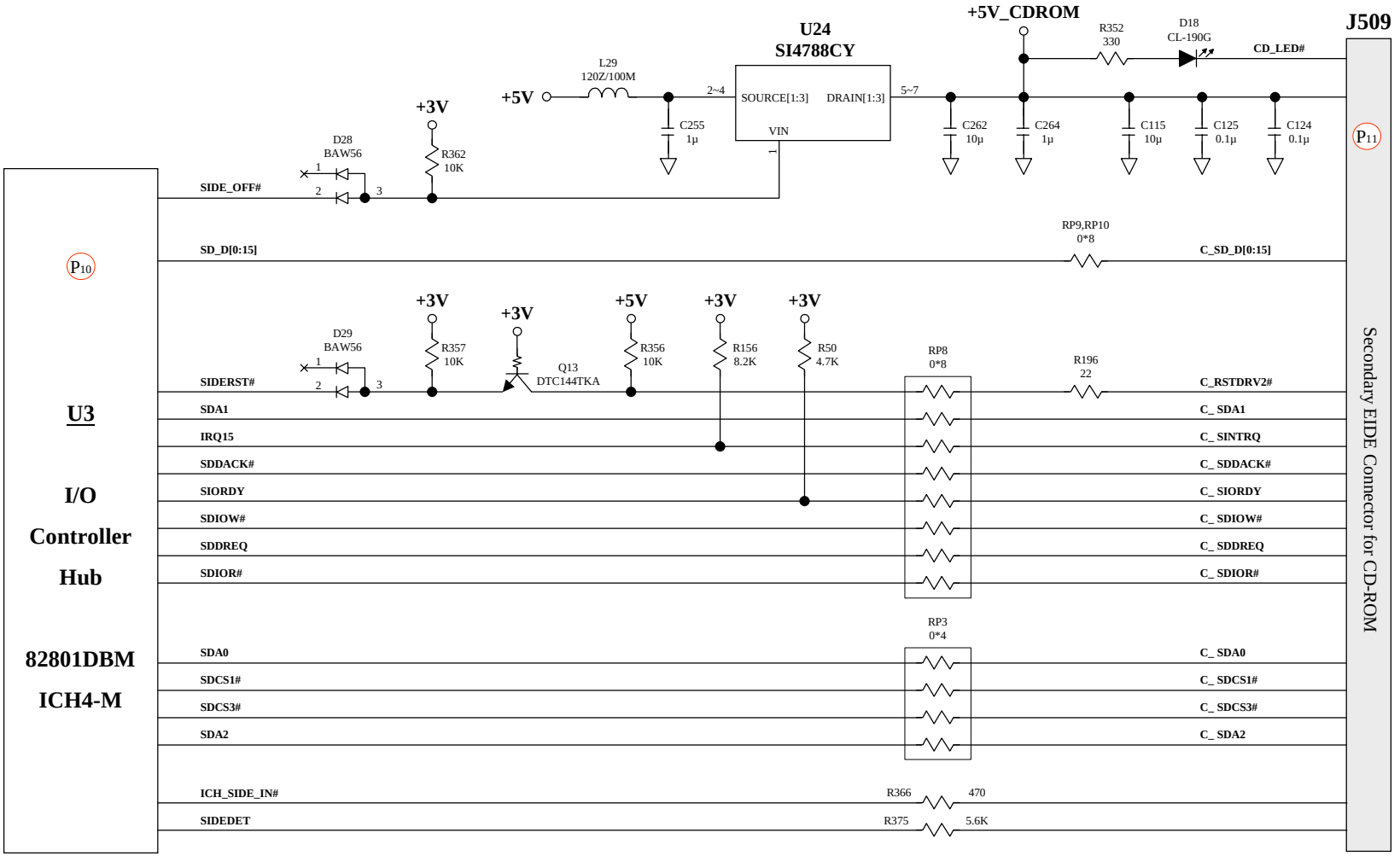
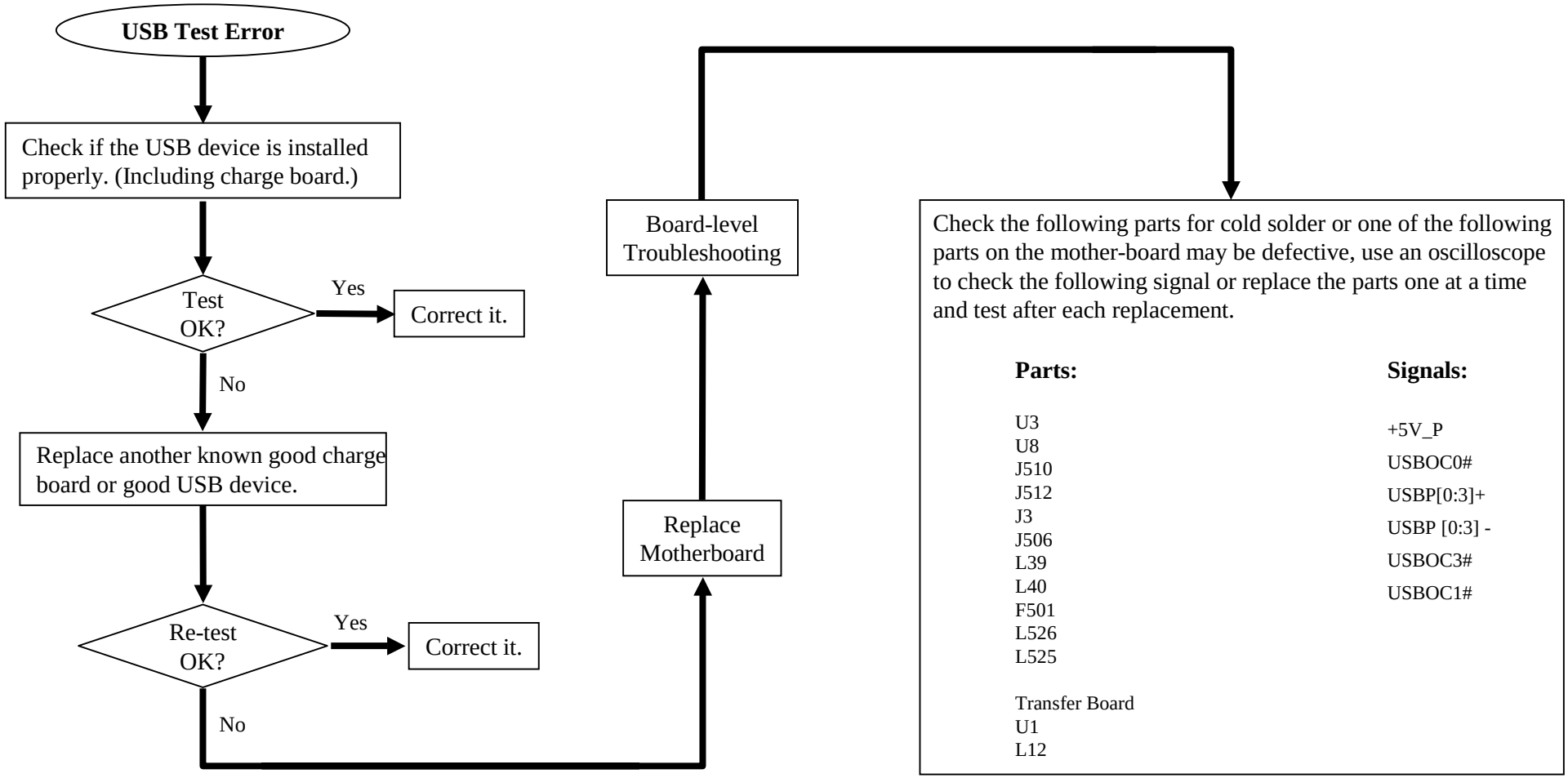
8.8 CD-ROM Drive Test Error

An error message is shown when reading data from CD-ROM drive.



8.9 USB Test Error

An error occurs when a USB I/O device is installed.



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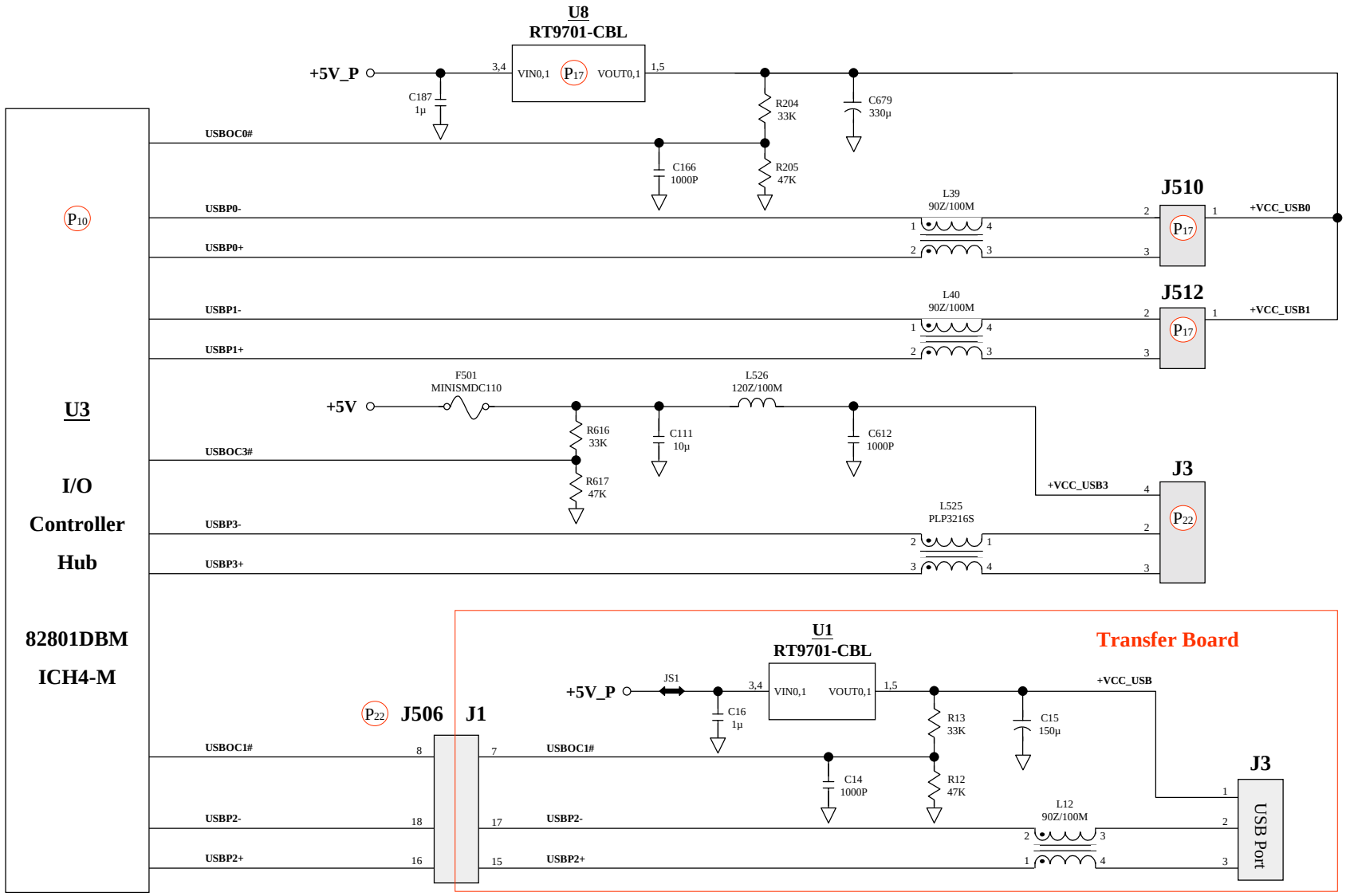
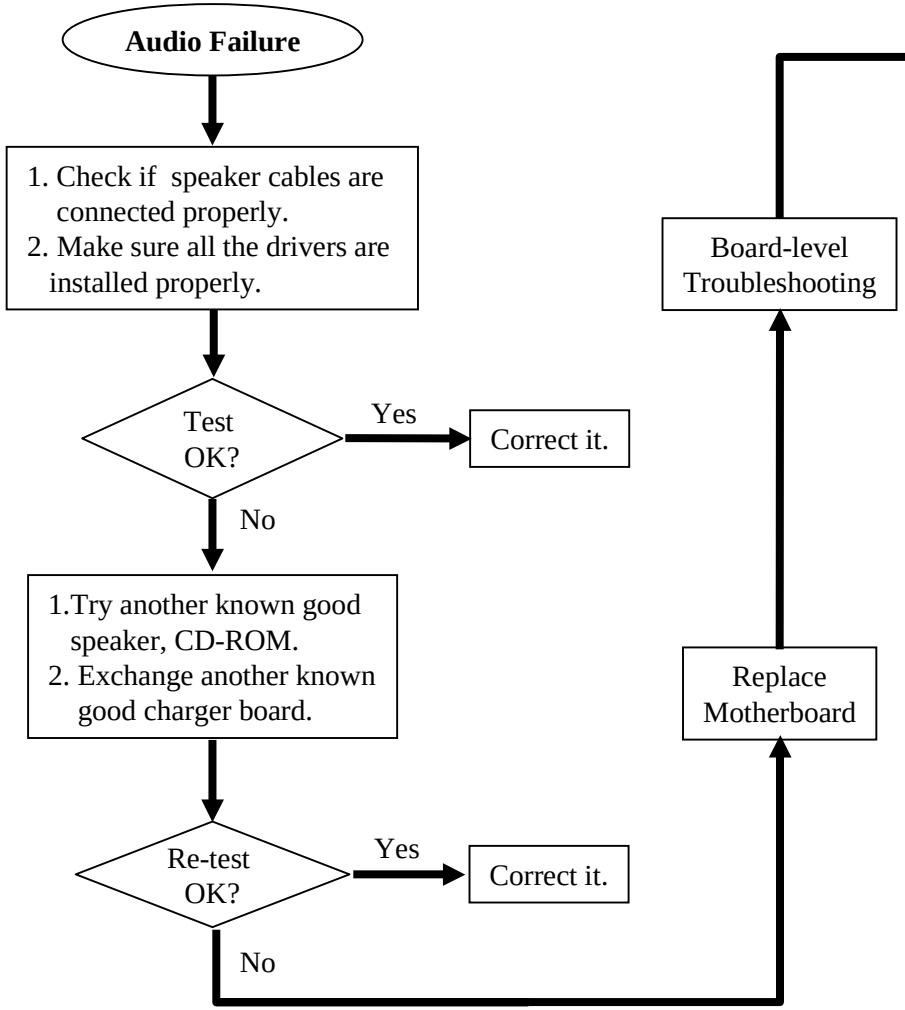
8.9 USB Test Error

An error occurs when a USB I/O device is installed.



8.10 Audio Failure

No sound from speaker after audio driver is installed.



Check the following parts for cold solder or one of the following parts on the motherboard may be defective,use an oscilloscope to check the following signal or replace parts one at a time and test after each replacement.

1.If no sound cause of line out, check the following parts & signals:

Parts:	Signals:
U3	AOUT_R
U509	AOUT_L
U511	DEVICE_DECT#
U18	SPDIFOUT
Q23	DECT_HP#/OPT
Q26	SPK_OFF
Q31	
L533	
L535	
L536	
L37	
L38	

2. If no sound cause of MIC, check the following parts & signals:

Parts:	Signals:
U3	H8_AVREF
U509	MIC
J519	
L537	
L35	

3. If no sound cause of CD-ROM, check the following parts & signals:

Parts:	Signals:
U3	CDROM_LEFT
U509	CDROM_RIGHT
J509	
R309	
R302	

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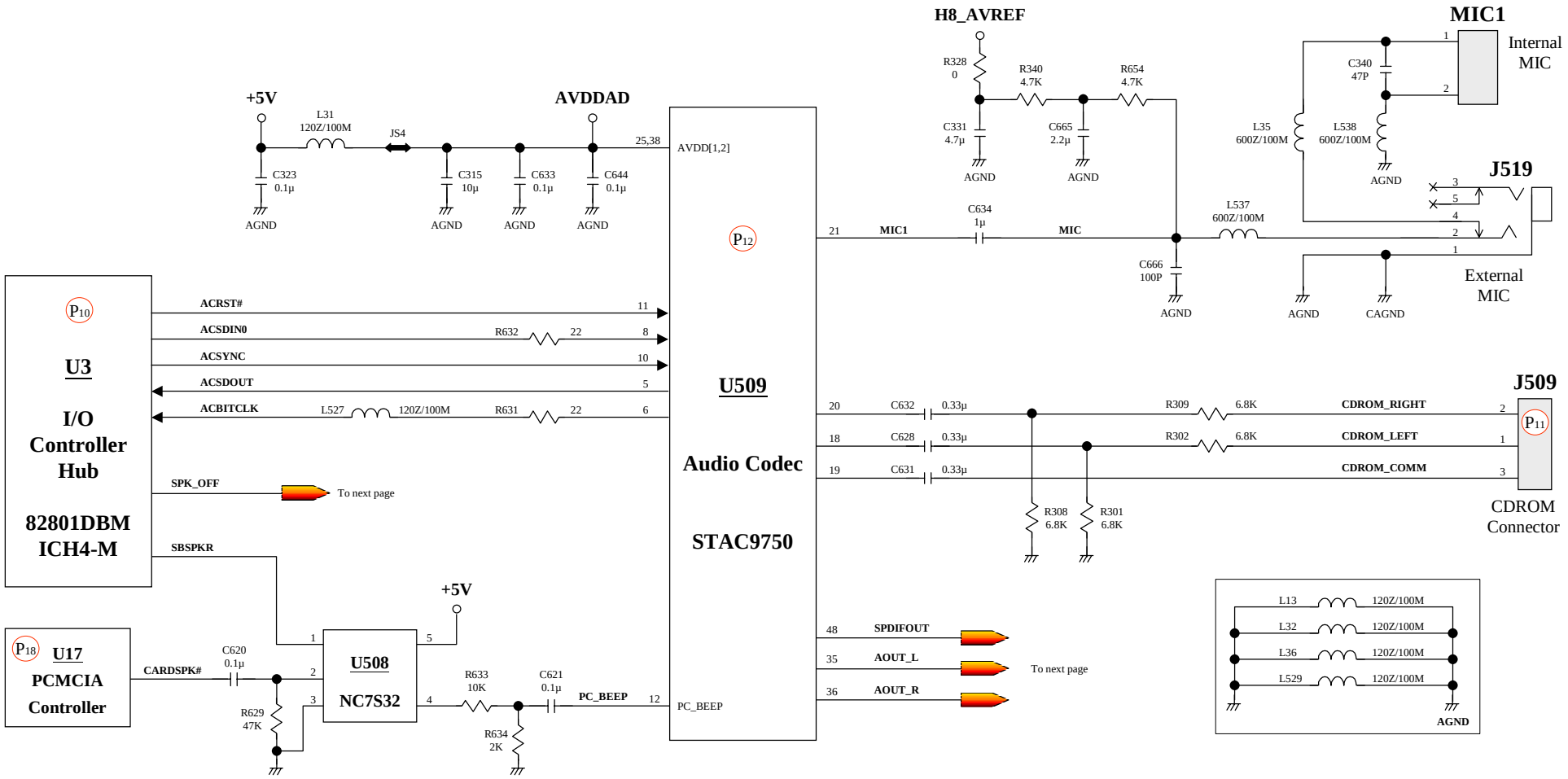
8.10 Audio Failure – Audio IN

No sound from speaker after audio driver is installed.



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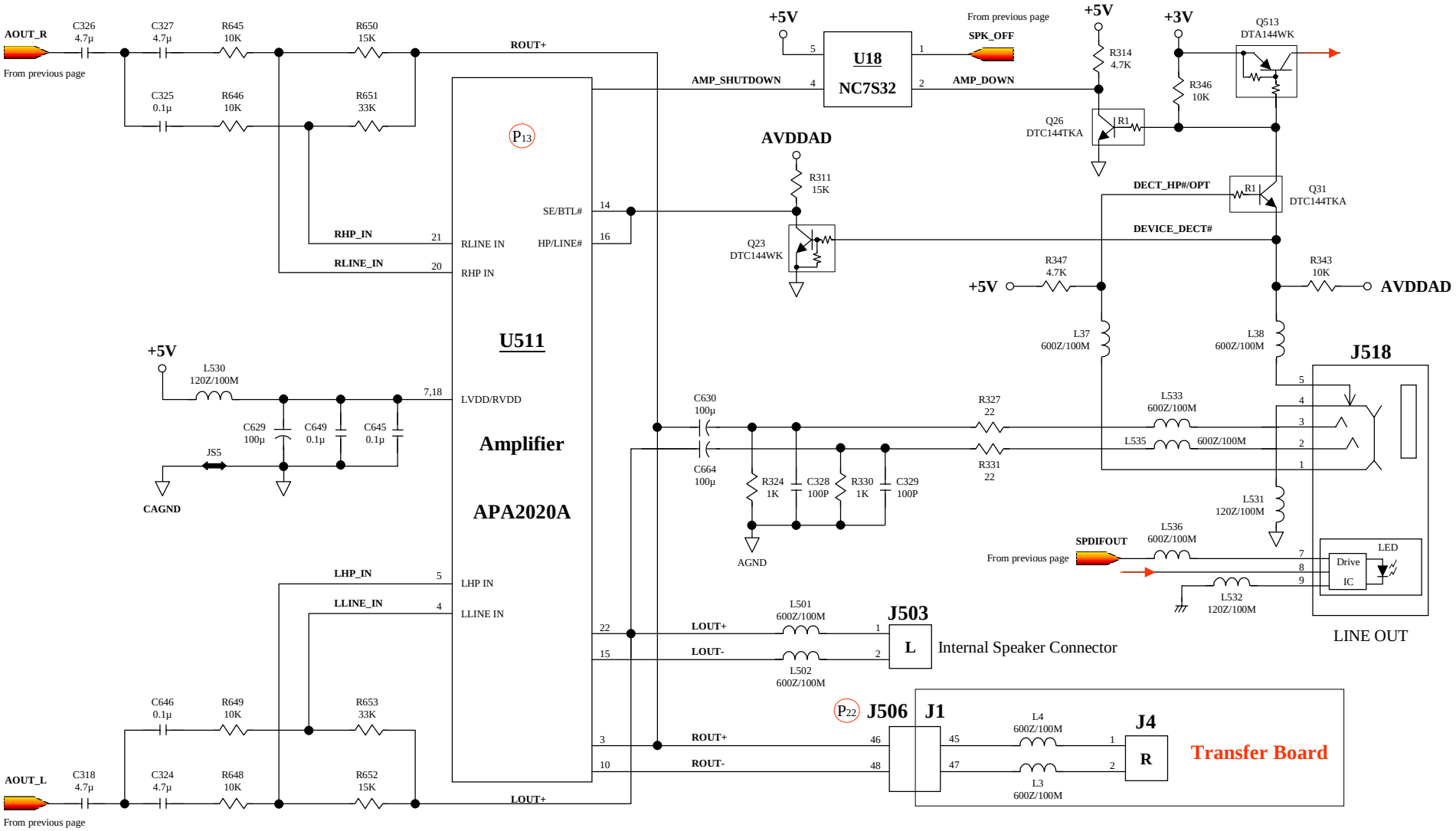
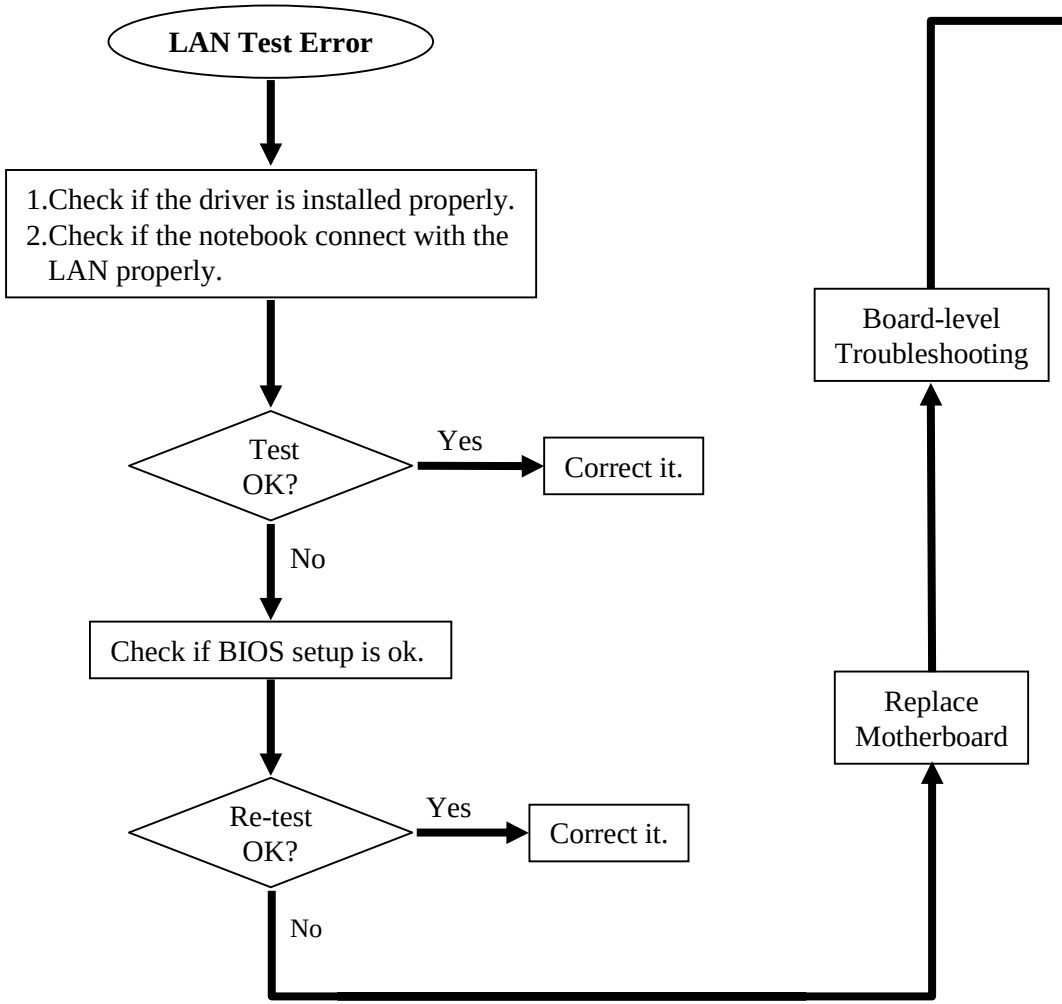
8.10 Audio Failure – Audio OUT

No sound from speaker after audio driver is installed.



8.11 LAN Test Error

An error occurs when a LAN device is installed.



Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:	**Signals:**	
U3	+LAN_A2.5V	PCI_GNT1#
U15	+LAN_D2.5V	PCI_PAR
U17	CARD_RI#	AD[0:31]
U16	PCICLK_LAN	CBE#]0:3]
U11	PCIRST#	RXIN+
J515	IN_PIRQE#	RXIN-
Q24	PCI_REQ1	TXD+
Q20	PCI_FRAME#	TXD-
U2	PCI_DEVSEL#	EECS
L26	PCI_TRDY#	EESK
L27	PCI_IRDY#	EEDI
X4	PCI_PME#	EEDO
	PCI_STOP#	

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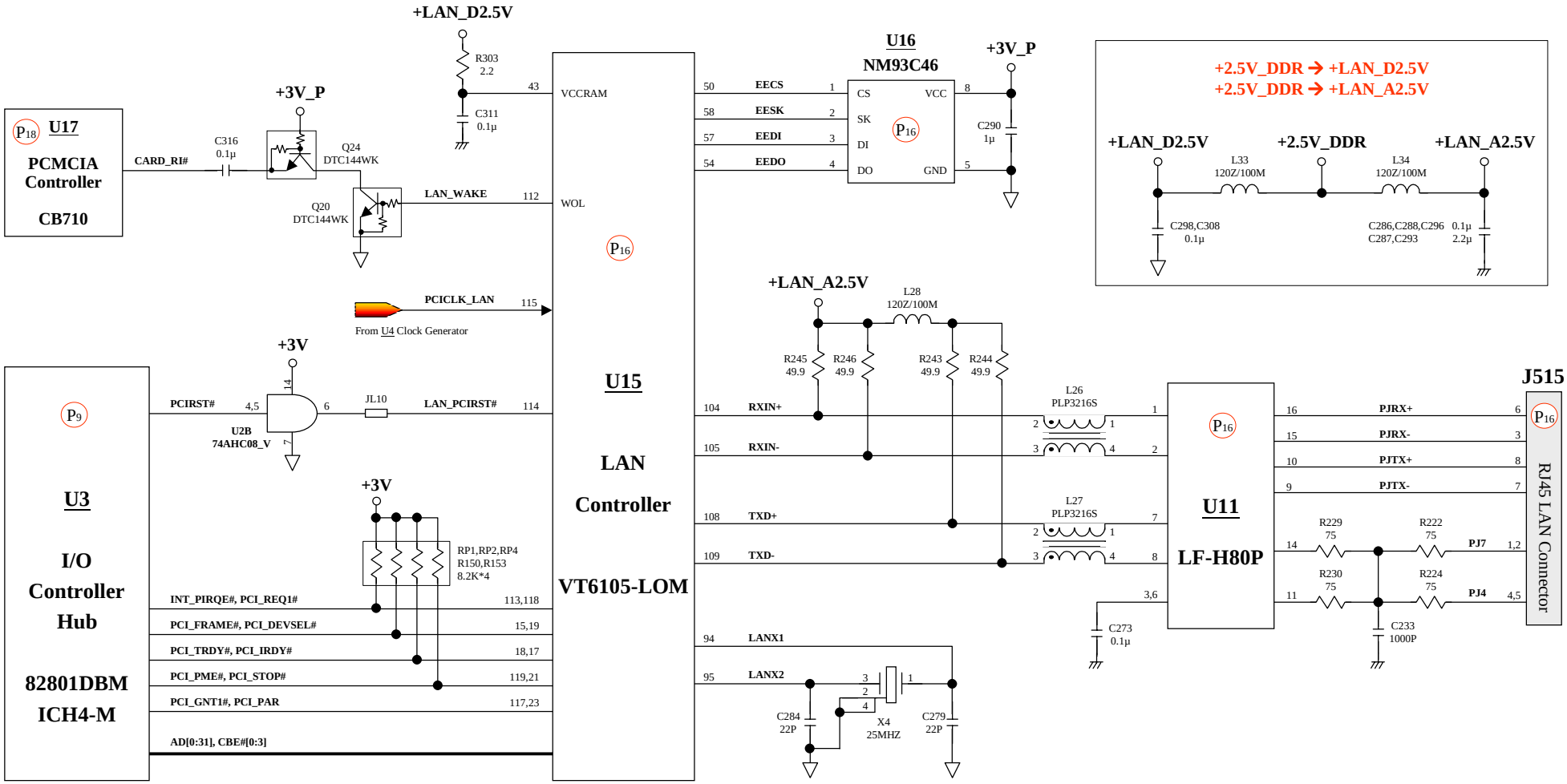
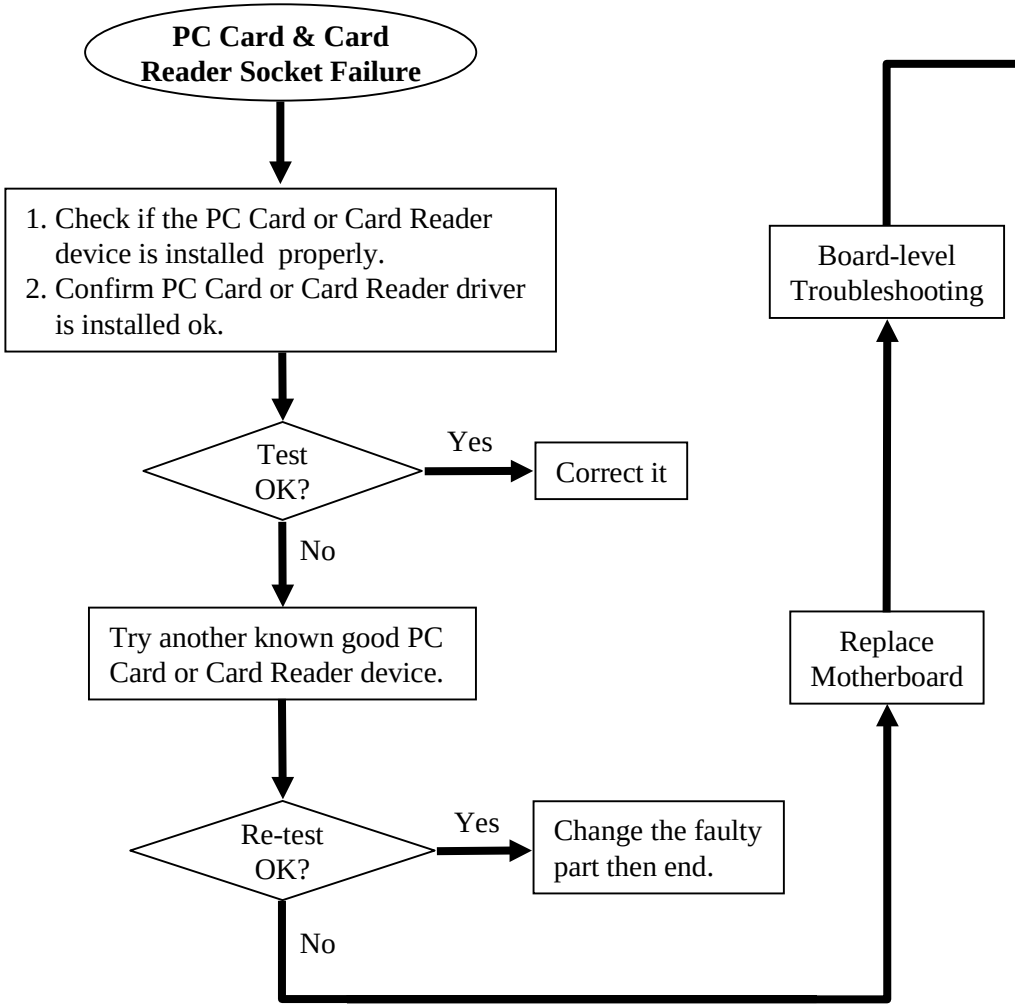
8.11 LAN Test Error

An error occurs when a LAN device is installed.



8.12 PC Card & Card Reader Socket Failure

An error occurs when a PC card or SD Card device is installed.



Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:

U3
U17
U21
J517
J516
U2
Q22
R270
R279

Signals

PCICLK_CARD
PCIRST#
INT_PIRQF#
PCI_REQ2#
PCI_SERR#
PCI_PERR#
PCI_DEVSEL#
PCI_FRAME#
PCI_IRDY#
PCI_TRDY#
PCI_STOP#
PCLKRUN#
PCI_PME#
PCI_GNT2#
PIC_PAR
SERIRQ
SUSB#
AD[0:31]
CBE#[0:3]
VCC5_EN#
VCC3_EN#
VPPD0
VPPD1

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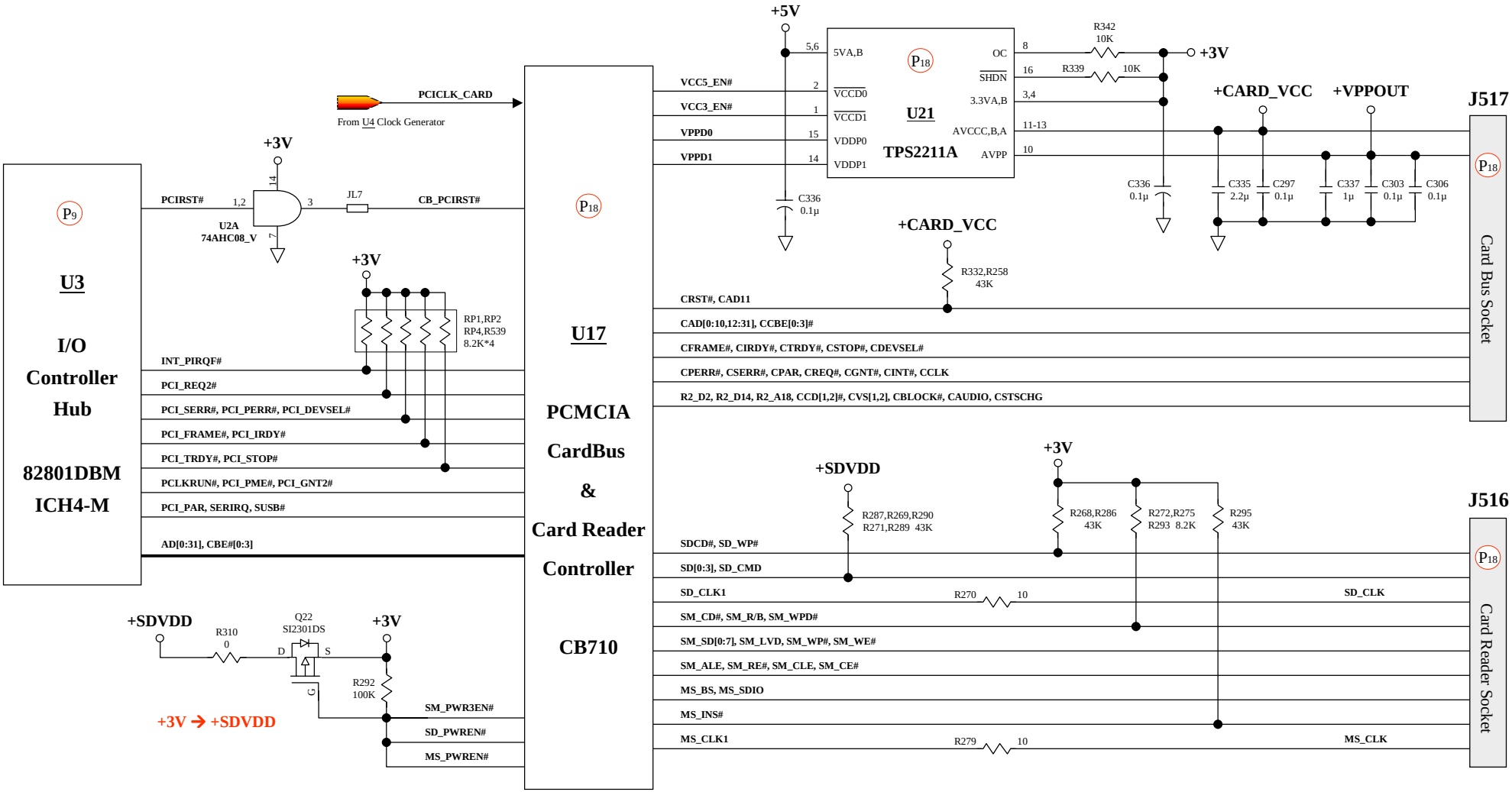
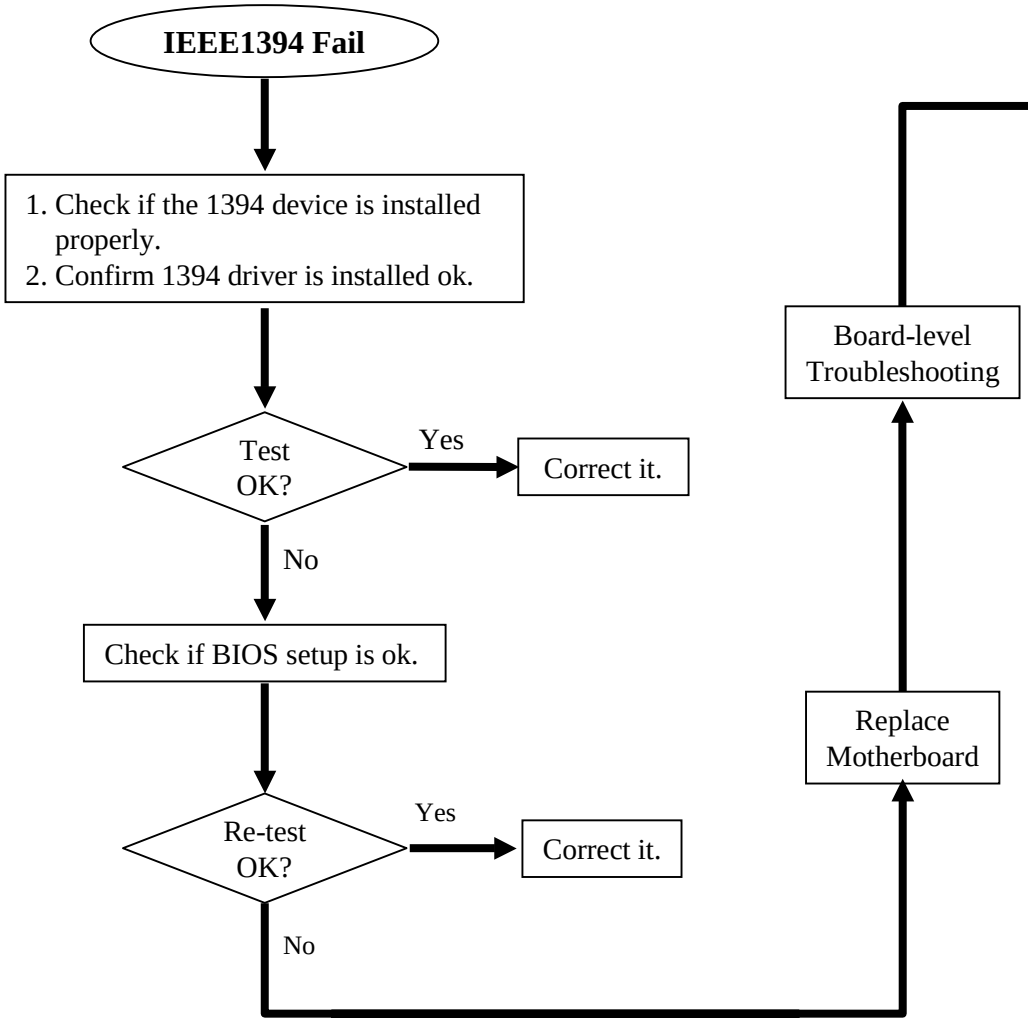
8.12 PC Card & SD Card Socket Failure

An error occurs when a PC card or SD Card device is installed.



8.13 IEEE 1394 Failure

An error occurs when a IEEE 1394 device is installed.



Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:	**Signals**	
U3	AD[0:31]	PCI_SERR#
U9	CBE# [0:3]	PCI_PME#
U10	PCI_REQ0#	PCICLK_1394
J506	PCI_FRAME#	EECS
U2	PCI_IRDY#	EECK
JL11	PCI_TRDY#	EEDI
R220	PCI_DEVSEL#	EEDO
X3	PCI_STOP#	TPA+
	INT_PIRQG#	TPA-
Transfer Board	PCIRST#	TPB+
	PCI_GNT0#	TPB-
J1	PCI_PAR	TPBIAS1
J5	PCI_PERR#	+3V
L5		1394_VCC
L6		1394_AVCC

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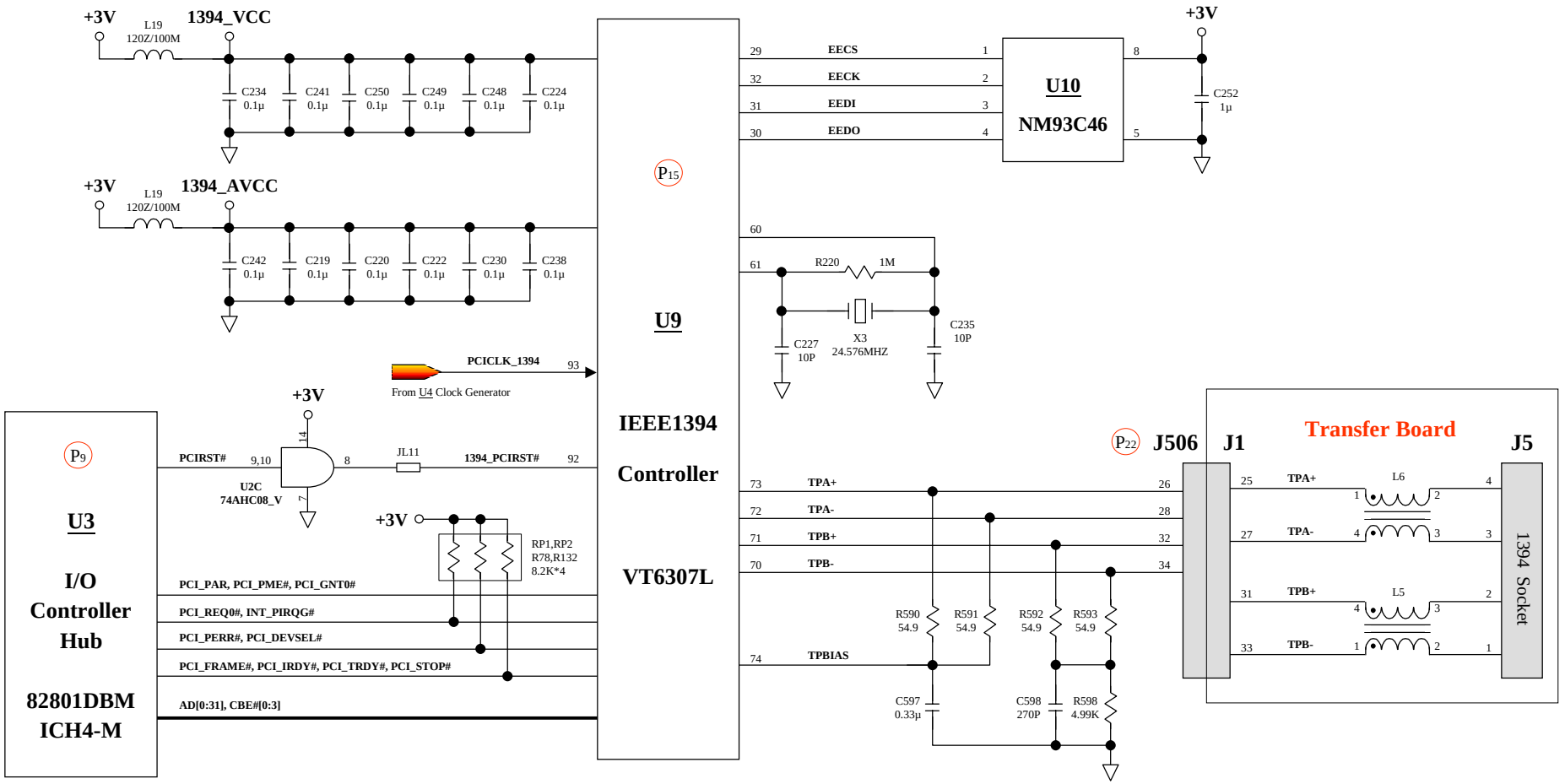
8.13 IEEE 1394 Failure

An error occurs when a IEEE 1394 device is installed.



9. Spare Parts List - 1

Part Number	Description	Location(US)
441999900215	AC ADPT ASSY OPTION;8080	
442672600031	AC ADPT ASSY;19V,3.16A,DELTA,706	
361400003030	ADHESIVE;ABS+PC PACK,G485,CEMIDA	
361400003005	ADHESIVE;HEAT,TRANSFER,HTA-48(W)	
541667530026	AK;EN,8080,UTILITY ONLY	
541667530013	AK;EU,BOX,8080	
441999900212	BATT ASSY OPTION;LI,8-CELL,8080	
441675300037	BATT ASSY,SANYO,8CELLS/4.0AH,808	
442675300002	BATT ASSY;14.8V/4.4AH,LI,4S2P,SA	
338536010052	BATTERY;LI,3.7V/2.2AH,18650,SANY	
242670800113	BFM-WORLD MARK;WINXP,7521N	
221675340001	BOX;AK,8080	
340675300015	BRACKET ASSY;TOUCHPAD,8080	
343675300001	BRACKET;HINGE,R,8080	
343675300004	BRACKET;IO,8080	
341675300004	BRACKET;LCD,QDI,L,8080	
341675300003	BRACKET;LCD,QDI,R,8080	
421015560001	CABLE ASSY;PHONE LINE,6P2C,W/Z C	
421673400005	CABLE ASSY;TV-OUT,8640S	
272075103403	CAP;.01U ,50V,10%,0603,X7R,SMT	
272075103403	CAP;.01U ,50V,10%,0603,X7R,SMT	C16,C3,C4,C5
272075103702	CAP;.01U ,50V,+80-20%,0603,Y5V,S	C121,C150,C154,C160,C175,C179
272075103401	CAP;.01U ,CR,50V ,10%,0603,X7R,S	PC106,PC24,PC4,PC503,PC504,P
272072473401	CAP;.047U,16V ,10%,0603,X7R,SMT	
272072473401	CAP;.047U,16V ,10%,0603,X7R,SMT	C678

Part Number	Description	Location(US)
272072104702	CAP;.1U ,16V,+80-20%,0603,Y5V,S	C149,C151,C152,C153,C185,C218
272073104703	CAP;.1U ,25V,+80-20%,0603,X7R,S	
272073104501	CAP;.1U ,25V,+80-20%,0603,Y5V,S	PC578,PC6
272075104701	CAP;.1U ,50V,+80-20%,0603,Y5V,S	C1,C100,C102,C106,C110,C113,C
272075104701	CAP;.1U ,50V,+80-20%,0603,Y5V,S	C1,C10,C11,C12,C13,C2,C3,C4,C5
272075104703	CAP;.1U ,50V,+80-20%,0603,Y5V,S	C10,C11,C14,C15
272075104703	CAP;.1U ,50V,+80-20%,0603,Y5V,S	C6,C8
272072104402	CAP;.1U ,CR,16V,10%,0603,X7R,SM	PC26
272005104502	CAP;.1U ,CR,50V,20%,0805,Z5U,SM	PC544
272005104402	CAP;.1U ,50V,+/-10%,0805,X7R,SMT	C690,PC529,PC579
272072224402	CAP;.22U ,10V ,10%,0603,X7R,SMT	PC574
272072334701	CAP;.33U ,CR,16V ,+80-20%,0603,Y	
272072334701	CAP;.33U ,CR,16V ,+80-20%,0603,Y	C597,C628,C631,C632
272072474701	CAP;.47U ,16V,+80-20%,0603,Y5V,S	C12
272072474701	CAP;.47U ,16V,+80-20%,0603,Y5V,S	C17,C9
272002474401	CAP;.47U ,CR,16V ,10%,0805,X7R,S	C1,C2
272030102401	CAP;1000P,2KV,10%,1808,X7R,SMT	C233
272030102401	CAP;1000P,2KV,10%,1808,X7R,SMT	C19,C20
272075102701	CAP;1000P,50V ,+/-20%,0603,X7R,S	C13,C166,C612,C642,C653,C7,PC
272075102701	CAP;1000P,50V ,+/-20%,0603,X7R,S	C14
627207510241	CAP;1000P,50V ,10%,0603,X7R,SMT	C7
272075102403	CAP;1000P,CR,50V,10%,0603,X7R,SM	PC102,PC104,PC105,PC17,PC44,
272075101701	CAP;100P ,50V ,+ -10%,0603,NPO,S	C517,C666
272075101401	CAP;100P ,50V ,10%,0603,COG,SMT	C328,C329,C530,C536,C562,PC10
272991107502	CAP;100u,6.3V,20%,18m,SMT,MASTUS	C679

9. Spare Parts List - 2

Part Number	Description	Location(US)
272991107502	CAP;100u,6.3V,20%,18m,SMT,MASTUS	C15
272075100701	CAP;10P ,50V ,+-10%,0603,NPO,SM	C227,C235,C299,C302
272011106701	CAP;10U ,10V,+80-20%,1206,Y5V,S	C11,C111,C115,C127,C134,C144,(
272023106502	CAP;10U,25V,M,1210,T2.5MM,X5R,SM	PC510,PC511,PC512,PC519,PC52
272075152401	CAP;1500P,CR,50V,10%,0603,X7R,SM	PC108,PC550
272073151301	CAP;150P ,CR,25V,5% ,0603,NPO,SM	PC15
272431157507	CAP;150U ,TPC,6.3V,20%,H1.9,7343	PC539,PC540,PC70,PC71,PC76,P
272433156502	CAP;15U ,TQC,25V,20%,H=1.9 ,7343	PC46,PC48,PC508,PC509,PC59,P
272075181301	CAP;180P ,50V ,5% ,0603,NPO,SMT	PC54
272073180401	CAP;18P ,CR,25V ,10%,0603,NPO,S	C36,C40
272001105403	CAP;1U ,10%,10V ,0805,X7R,SMT	PC11,PC575
272071105701	CAP;1U ,CR,10V ,80-20%,0603,Y5	C156,C157,C168,C183,C187,C190
272071105701	CAP;1U ,CR,10V ,80-20%,0603,Y5	C16,C21,C22
272002105403	CAP;1U ,CR,16V,10%,0805,X7R,SM	
272003105701	CAP;1U ,CR,25V ,+80%-20%,0805,	PC16
272002105701	CAP;1U ,CR,16V ,-20+80%,0805,Y5	PC21
272001225401	CAP;2.2U ,CR,10V ,10%,0805,X7R,S	
272002225701	CAP;2.2U ,CR,16V ,+80-20%,0805,Y	C135,C139,C141,C312,C346,C542
272012225702	CAP;2.2U ,CR,16V ,+80-20%,1206,Y	C108,C14,C287,C293,C335
272075200302	CAP;20P ,CR,50V ,5% ,0603,NPO,S	C572,C581
272075222401	CAP;2200P,50V ,10%,0603,X7R,SMT	C10
272075221401	CAP;220P ,CR,50V ,10%,0603,X7R,S	C91
272431227504	CAP;220U ,4V ,20%,7343,POSCAP,SM	PC565,PC67
272431227528	CAP;220U,2.5V,TPE-MC,20%,POSCAP,	PC28,PC29,PC31,PC32,PC515,PC
272075220701	CAP;22P ,50V ,+ -10%,0603,NPO,S	

Part Number	Description	Location(US)
272075220301	CAP;22P ,50V ,5% ,0603,COG,SMT	C279,C284
272011226701	CAP;22U ,CR,10V,1206,Y5V,+80~20%	C131,C155,C540,C545,C559,C590
272075271401	CAP;270P ,50V,+-10%,0603,X7R,SMT	C114,C118,C126,C598
272075209001	CAP;2P ,CR,50V ,+-0.25PF,0603,	
272431337510	CAP;330U,2.5V,20%,POSCAP,H1.8,73	PC33,PC45,PC548,PC567
272075330302	CAP;33P ,50V,5% ,0603,NPO,SMT	C129,C132
272075330401	CAP;33P ,CR,50V ,10%,0603,X7R,S	C529,C543,C548
272002475701	CAP;4.7U ,CR,10V ,+80-20%,0805,S	PC100,PC82,PC99
272001475701	CAP;4.7U ,CR,10V ,+80-20%,0805,Y	C331,C332,C591,C692
272001475701	CAP;4.7U ,CR,10V ,+80-20%,0805,Y	C18
272012475701	CAP;4.7U ,CR,16V ,+80-20%,1206,Y	C318,C324,C326,C327,C616
272012475502	CAP;4.7U ,CR,16V,20%,1206,Y5U,SM	
272013475701	CAP;4.7U ,CR,25V ,+80-20%,1206,Y	C13
272075472701	CAP;4700P,50V ,+ -20%,0603,X7R,S	PC527
272072471301	CAP;470P ,CR,16V ,5% ,0603,NPO,P	
272075470401	CAP;47P ,50V ,10%,0603,COG,SMT	C340,C601,PC577
272431476502	CAP;47U ,6.3V,20%,SP-CAP,7343,S	
272030680402	CAP;68P ,3KV,5%,1808,NPO,SMT,PR	
272075680302	CAP;68P ,50V ,5% ,0603,NPO,SMT	C610,C613
221675350012	CARD BOARD;FRAME,PALLET,W/CARRYI	
221675350011	CARD BOARD;TOP/BTM,PALLET,W/CARR	
221600020252	CARTON;BATTERY,CAIMAN,PWR	
221675320008	CARTON;NON-BRAND,W/CARRYING BAG,	
431675300001	CASE KIT;8080	
335152000044	CFM-BAT;FUSE THERMAL 98'C	

9. Spare Parts List - 3

Part Number	Description	Location(US)
310111103007	CFM-BAT;THERMISTOR,10K,1%DISK,50	
273000111002	CHOKE COIL;120OHM/100MHZ,20%,321	L26,L27,L525
273000111002	CHOKE COIL;120OHM/100MHZ,20%,321	L5,L6
273000150313	CHOKE COIL;90OHM/100MHZ,20%,2012	L39,L40
273000150313	CHOKE COIL;90OHM/100MHZ,20%,2012	L12
361200001018	CLEANNER;YC-336,LIQUID,STENCIL/P	
331000008038	CON;BAT,8P,2.5MM,SUYIN	J501
291000001001	CON;BATTERY,10P,FM,2MM,R/A,SMT	
331000007015	CON;BATTERY,FM,7P,R/A,8175,PRC	
331720015023	CON;D,FM,15P,2.29,R/A,3 ROW,TITA	J507
291000622007	CON;DIMM,R/A,200P,.6,H9.2,REVERS	J513
291000151201	CON;FPC/FFC,12P,0.5MM,R/A,SMT	J2
291000153011	CON;FPC/FFC,15P*2,.8MM,BD/BD,C10	J2
291000152603	CON;FPC/FFC,26P,1MM,R/A,KBD,SMT	J1
331040050017	CON;HDR,FM,25P*2,R/A,C14301-1500	J501
291000015201	CON;HDR,FM,26P*2,.5MM,ST,SMT	J509
291000015202	CON;HDR,FM,26P*2,1.0MM,ST,SMT,HR	J1
291000021101	CON;HDR,MA,11P*1,1.25,R/A,DF13-1	
291000011101	CON;HDR,MA,11P*1,1.25,ST,SMT	J504
291000013011	CON;HDR,MA,15P*2,1.0MM,H4.75,ST,	J505
291000024419	CON;HDR,MA,22P*2,2MM,H2.35,R/A,C	J4
291000015031	CON;HDR,MA,25P*2,0.3,ST,SMT,K071	J506
291000015031	CON;HDR,MA,25P*2,0.3,ST,SMT,K071	J1
291000020206	CON;HDR,MA,2P*1,1.25MM,H2.57,R/A	J503
291000020206	CON;HDR,MA,2P*1,1.25MM,H2.57,R/A	J6

Part Number	Description	Location(US)
291000010209	CON;HDR,MA,2P*1,1.25MM,H4.2,ST,S	J511
291000010209	CON;HDR,MA,2P*1,1.25MM,H4.2,ST,S	J4
291000000203	CON;HDR,MA,2P*1,3.5MM,R/A,SMT,SM	J2
291000010503	CON;HDR,R/A,5P,.5,87152-0507,ACE	J3
331000004009	CON;IEEE1394,MA,4P*1,0.8MM,R/A	J5
291000253702	CON;MEMORY CARD,37P,SD,SM,SSFDC,	J516
331870007007	CON;MINI DIN,7P,R/A,W/GROUND,330	J508
291000616801	CON;PCMCIA CARD,68P,TAI-SOL,WEAS	J517
331810006044	CON;PHONE JACK,6P2C,H11.5,RJ11,T	J7
291000810806	CON;PHONE JACK,8P8C,SMD,RJ45	J515
331840010005	CON;POF MINI JACK,10P,W/SPDIF,2F	J518
331910003034	CON;POWER JACK,3P,D=2.5,SINGATRO	PJ501
331840005013	CON;STEREO JACK,5P,R/A,28MF60-07	J519
331040008015	CON;USB,MA,R/A,4P*1,DIP,C10713,A	J510,J512
331040008015	CON;USB,MA,R/A,4P*1,DIP,C10713,A	J3
291000410301	CON;WFR,MA,3P,1.25,ST,SMT/MB	J502
346673800009	CONDUCTIVE TAPE;CONNECTOR,LCD,83	
342503200003	CONTACT PLATE;W4L18T0.15,7521/GR	
342502900001	CONTACT PLATE;W4L27T0.15,7068	
342503200005	CONTACT PLATE;W4L30T0.15,GRAMPUS	
342503200004	CONTACT PLATE;W4L63T0.15,1/4,T T	
342675300005	CONTACT PLATE;W5L27T0.13,8080,PW	
342675300007	CONTACT PLATE;W5L43.5T0.13,8080,	
342675300006	CONTACT PLATE;W5L45T0.13,8080,PW	
342503400002	CONTACT PLATE;W5L9T0.13,7170LI,P	

9. Spare Parts List - 4

Part Number	Description	Location(US)
340675300006	COVER ASSY;8080	
340675300013	COVER ASSY;DIMM,8080	
340675300010	COVER ASSY;HDD,8080	
340675300008	COVER ASSY;LCD,8080	
344675300019	COVER;BATT,8080	
344675300012	COVER;CABLE,LCD,8080	
344675300027	COVER;HEATSINK,8080	
344675300011	COVER;HINGE,L,8080	
344675300010	COVER;HINGE,R,8080	
272625220401	CP;22P*4 ,8P,50V ,10%,1206,NPO,S	CP501,CP502,CP503
272625470401	CP;47P*4 ,8P,50V ,10%,1206,NPO,S	CP1
331660020005	DIMM SOCKET;DDR SODIMM 200P, CA0	J514
288100140007	DIODE;B140,40V,1A,SMA,DIODES,SMT	PD12,PD508,PD510,PD511
288100340008	DIODE;B340LA,40V,3A,SMA,DIODES,S	PD503,PD504,PD506,PD507
288100032013	DIODE;BAS32L,VRRM75V,MELF,SOD-80	D27,PD10,PD11,PD505
288100054001	DIODE;BAT54,30V,200mA,SOT-23	D501,D502
288100701002	DIODE;BAV70LT1,70V,225MW,SOT-23	D503,D9,PD4,PD7
288100099001	DIODE;BAV99,70V,450MA,SOT-23	
288100099001	DIODE;BAV99,70V,450MA,SOT-23	PD501,PD502
288100056003	DIODE;BAW56,70V,215mA,SOT-23	D2,D25,D26,D28,D29,D3,PD509,
288100084002	DIODE;BZX84C5V6,5.2~6V,350mA,SOT	ZD3,ZD4
288101004024	DIODE;EC10QS04,RECT,40V,1A,CHIP,	D4
288104148001	DIODE;RLS4148,200MA,500MW,MELF,S	D30
288100020001	DIODE;RLZ20C,ZENER,19.23V,5%,SMT	PD1
288100024002	DIODE;RLZ24D,ZENER,23.63V,5%,SMT	PD2

Part Number	Description	Location(US)
288100056001	DIODE;RLZ5.6B,ZENER,5.6V,5%,LL34	D1,D504
288101040006	DIODE;SBM1040,10A,SCHOTTKY,POWER	PD5
288100056005	DIODE;UDZ5.6B,ZENER,5.6V,UMD2,SM	ZD5
288100018003	DIODE;UDZS18B,ZENER,18V,SOD-323,	ZD1,ZD2
344675300034	DUMMY CARD;PCMCIA,8080	
272602107501	EC;100U,16V,M,6.3*5.5,-55+85'C,S	C629,C630,C664
227675300006	END CAP;W/CARRYING BAG,8080	
481675300002	F/W ASSY;KBD CTRL,8080	U504
481675300001	F/W ASSY;SYS/VGA BIOS,8080	U19
273000150002	FERRIET CHIP;120OHM/100MHZ,2012,	L14,L19,L20,L21,L33,L34,L513,L
273000610008	FERRITE ARRAY;120OHM/100MHZ,TKIN	FA1
273000130001	FERRITE CHIP;120OHM/100MHZ,1608,	L15,L17,L2,L22,L23,L25,L28,L3,
273000130001	FERRITE CHIP;120OHM/100MHZ,1608,	L1,L7,L8
273000150013	FERRITE CHIP;120OHM/100MHZ,2012,	L1,L24,L29,L31,L4,L5,L8,PL1,PL
273000150013	FERRITE CHIP;120OHM/100MHZ,2012,	L10,L11
273000150001	FERRITE CHIP;220OHM/100MHZ,2012,	L1
273000130006	FERRITE CHIP;600OHM/100MHZ,.2A,1	L35,L37,L38,L501,L502,L536,L5
273000130006	FERRITE CHIP;600OHM/100MHZ,.2A,1	L3,L4
421467530001	FFC;TOUCHPAD,8080	
342600002059	FINGER;EMI GROUNDING SMD FINGER	TP18,TP19,TP21,TP22,TP23
342600002062	FINGER;EMI GROUNDING SMD FINGER,	TP1,TP12,TP14,TP16,TP2,TP3,T
288001001001	FIR,GP2W1001YP,GDE VIEW,10P,SMT,	U2
245600010007	FLOW CARD;M/B,WHITE	
245600010016	FLOW CARD;SPS,GRAY	
295000010028	FUSE;0.14A/60V,POLY SWITCH,PTC,S	F1

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Part Number	Description	Location(US)
295000010048	FUSE;0.5A/15V,POLY SWITCH,SMD	F3
295000010014	FUSE;1.1A/6V,POLY SWITCH,PTC,SMD	F1,F2,F501
295000010105	FUSE;1A,NORMAL,1206,SMT	F502,PF501
295000010114	FUSE;FAST,1.75A,63VDC,1206,SMT,P	
335152000062	FUSE;LR4-730,POLY SWITCH,PRC	
295000010016	FUSE;NORMAL,6.5A/32VDC,3216,SMT	PF1,PF2
345675300027	GASKET; AUDIO, 8080	
345675300028	GASKET; CARD_READ, M/B, 8080	
345675300029	GASKET; PCMCIA, M_b-1, 8080	
345675300030	GASKET; PCMCIA, M_b-2, 8080	
345675300008	GASKET;1394, TRANS-B,8080	
345675300010	GASKET;BRACKET, I/O,8080	
345675300011	GASKET;I/O,8080	
345675300012	GASKET;LANS,M-B,8080	
345675300007	GASKET;MODEM, TRANS-B,8080	
345675300014	GASKET;USB, TRANS-B,8080	
345675300013	GASKET;USB,M-B,8080	
230000010004	GLUE;9001B,BLACK,PRC	
230000010003	GULE;9001A,BLACK,PRC	
451675300091	HDD ME KIT;8080	
340675300003	HEATSINK ASSY;8080	
340675300012	HEATSINK ASSY;NORTH BRIDGE,8080	
340675300002	HINGE;LCD,L,8080	
340675300001	HINGE;LCD,R,8080	
344673550001	HOLDER;PCMCIA,TAI-SOL,WEASEL2	

Part Number	Description	Location(US)
340675300007	HOUSING ASSY;8080	
340675300009	HOUSING ASSY;LCD,8080	
451675300001	HOUSING KIT;8080	
344675300020	HOUSING;BATT,8080	
344675300032	HOUSING-ROM,8080	
291000616802	IC SOCKET;BANIAS m-FCBGA478P, TY	U501
282574008005	IC;74AHC08,QUAD 2-I/P AND,TSSOP,	U2
282574014004	IC;74AHC14,HEX INVERTER,TSSOP,14	U20
282574373004	IC;74AHC373,OCT D-TRAN,TSSOP,20P	U512
282574132001	IC;74AHCT1G32,SINGLE OR GAT,SOT2	U18,U508
282074338402	IC;74CBTD3384,10 BIT BUS SW,TSOP	U503
284501021003	IC;ADM1021A,TEMPERATURE MTR,SSOP	U1
286308800006	IC;AME8800AEEV,VOL REG.,SOT23-5,	U516
286301117021	IC;AMS1117,VOL REGULATOR,1A,SOT-	U5,U6
286300317010	IC;AMS3107C, VOLTAGE REGULATOR,	U506
286302020001	IC;APA2020ARI,AUDIO AMP,2W,TSSOP	U511
286002040001	IC;BQ2040,GAS GAUGE,SO,16P,SMT	U4
286300710002	IC;CB710,CARDBUS/CARD READER,LFG	U17
284507011001	IC;CH7011A,TV ENCODER,LQFP,64P	U7
286302211002	IC;CP2211,POWER DISTRI SW,SSOP16	U21
283466570001	IC;EEPROM,9346,64*16 BITS,SO8,SM	U10,U16
283400000003	IC;EEPROM,NM24C02N,2K,SO,8P	U3
283480404002	IC;FLASH,512K*8-70,PLCC32,A29040	
284582801044	IC;FW82801DBM,ICH4-M,BGA,421P	U3
286300690003	IC;G690E,RESET CIRCUIT,4.38V,SOT	U22

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Part Number	Description	Location(US)
284583437003	IC;H8/F3437S,KBD CTRL,TQFP,100P,	
286100393004	IC;LMV393,DUAL COMPARTOR,SSOP,8P	PU4
286303728002	IC;LTC3728LX,PWM CTRL,LTC,5X5 QF	PU23,PU502
286301907001	IC;MAX1907A,PWM CONTROLLER,40-QF	PU505
286104173001	IC;MAX4173F,I-SENSE AMP,SOT23,6P	PU3
286300809009	IC;MAX809STR,RESET CIRCUIT,2.93V	U12
286301414001	IC;MM1414,PROTECTION,TSOP-20A,PR	U1
284500000050	IC;MONTARA-GM GMCH,MICRO-FCBGA,7	U502
286300965001	IC;OZ965R,CCFL CTRL,TSSOP16,O2	
284587393002	IC;PC87393F,TQFP,100P	U510
284520715001	IC;PLL207-151,CLOCK GEN,SSOP,56P	U4
286309701001	IC;RT9701,POWER DISTRI SW,SOT23-	U8
286309701001	IC;RT9701,POWER DISTRI SW,SOT23-	U1
286300812002	IC;S-812C,DECECTOR,SOT-89,PRC	U2
286301486001	IC;SC1486,PWM CTRL,SC,TSSOP-28	PU22
286300338001	IC;SC338,FET CTRL,SC,MSOP-10	PU13
286300431014	IC;SC431LCSK-.5,.5%,ADJ REG,SOT2	PQ4
282074164002	IC;SN74LV164APWR,SIPO REGISTER,T	U513
284509750002	IC;STAC9750T,AC97 CODEC,TQFP,48P	U509
286300594001	IC;TL594C,PWM CONTROL,SO,16P	PU2
284506105001	IC;VT6105LOM, PCI LAN CONTROLLER	U15
284506307001	IC;VT6307L,PCI-1394,2PORT,LQFP,1	U9
273000990018	INDUCTOR;10uH,CDRH125,SUMIDA,SMT	PL512,PL514
273000990158	INDUCTOR;3.0UH,SPC-1205P,H6.0,TM	PL508,PL510,PL515
273000990021	INDUCTOR;33uH,CDRH124,SUMIDA,SMT	PL502

Part Number	Description	Location(US)
273000990159	INDUCTOR;4.7UH,SPC-1205P,H6.0,TM	PL513
273000990127	INDUCTOR;IHLP5050CE-01-0.68uH,VI	PL506
346675300019	INSULATOR; CARD_READ, M_B, 8080	
346675300019	INSULATOR; CARD_READ, M_B, 8080	
346675300019	INSULATOR; CARD_READ, M_B, 8080	
346675300013	INSULATOR; HDD, CONN, M/B, 8080	
346675300012	INSULATOR; MB, 8080	
346503100005	INSULATOR;5,BATTERY ASSY,7521Li	
346503400502	INSULATOR;BATT ASSY,L22R9.2,8175	
346503200101	INSULATOR;BATT ASSY,POLY,W30L64,	
346503400503	INSULATOR;BATT ASSY,W7L13,8175	
346675300003	INSULATOR;DDR,M/B,8080	
346503400301	INSULATOR;FOR 3 CELLS,DOUBLE-FA,	
346669900004	INSULATOR;INVERTER,7170	
346675300020	INSULATOR;INVERTER_B,ESD,LCD,808	
346675300002	INSULATOR;MINIPCI,M/B,8080	
346503400203	INSULATOR;ONE ROUND,STINGRAY	
346675300010	INSULATOR;PCB ASSY,8080	
346675300004	INSULATOR;PCMCIA,M/B,8080	
346675300009	INSULATOR;TRANS-BD,8080	
451675300002	LABEL KIT;NON-BRAND,8080	
242600000145	LABEL;10*10,BLANK,COMMON	
242600000380	LABEL;10*8MM,BIOS,HI-TEMP 260	
242662300009	LABEL;25*10MM,3020F	
242662300009	LABEL;25*10MM,3020F	

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Part Number	Description	Location(US)
242600000439	LABEL;25*6,HI-TEMP,COMMON	
242600000439	LABEL;25*6,HI-TEMP,COMMON	
242600000378	LABEL;27*7MM,HI-TEMP 260'C	
242668300028	LABEL;32*7MM,POLYESTER FILM,HOPE	
624200010140	LABEL;5*20,BLANK,COMMON	
624200010140	LABEL;5*20,BLANK,COMMON	
624200010140	LABEL;5*20,BLANK,COMMON	
242600000232	LABEL;6*6MM,GAL,BLANK,COMMON	
242675300001	LABEL;AGENCY-GLOBAL,8080	
242600000157	LABEL;BAR CODE & S/N,13.5*75,COM	
242675300002	LABEL;BATT 14.8V/4.4AH,LI,SANYO,	
242600000433	LABEL;BLANK,11*5MM,COMMON	
242669900009	LABEL;BLANK,60*80MM,7170	
242600000452	LABEL;BLANK,7MM*7MM,PRC	
242600000452	LABEL;BLANK,7MM*7MM,PRC	
242664800013	LABEL;CAUTION,INVERT BD,PITCHING	
242600000001	LABEL;PAL,20*5MM,COMMON	
242600000315	LABEL;RED ARROW HEAD,PRC	
242600000315	LABEL;RED ARROW HEAD,PRC	
242600000446	LABEL;S/N,INVERTER,20MM*3MM,PRC	
441675300001	LCD ASSY;TFT,QDI,14.1",XGA,W/O G	
451675310001	LCD ME KIT;TFT,QDI,XGA,14",8080	
413000020349	LCD;QD141X1LH12,TFT,XGA,14.1",QD	
294011200150	LED;BLUE,H0.55,LTST-C191TBKT,SMT	D18,D19,D20,D21,D22,D23,D24
294011200069	LED;GREEN,19-21VGC/TR8,LED_CL190	

Part Number	Description	Location(US)
294011200016	LED;GREEN,H0.8,0603,CL-190G,SMT	D10,D11,D12,D13,D14,D15,D16,I
294011200070	LED;RED/GREEN,19-22SRVGC/TR8,LED	
526267530024	LTXNX;8080/T4XX/XXX/3XX9/L1C3A/X	
561567530003	MANUAL KIT;EU,8080,N-B	
561567530021	MANUAL;USER'S,EN,8080,N-B	
561567530023	MANUAL;USER'S,EU,8080,N-B	
339115000030	MICROPHONE;-36dB+-3dB,D5.8*H3.4,	MIC1
291000251246	MINIPCI SOCKET;124P,R/A,0.8MM,H=	J520
242675300003	NAMEPLATE;COVER,8080	
416267530901	NB PF OPTION;XGA,14.1",8080	
416267530001	NB PF;QDI,14.1",XGA,W/O GPRS,808	
461675310002	PACKING KIT;14",NON-BRAND,BAG,80	
461675300003	PACKING KIT;8080 BATT,SANYO,8CEL	
227675300005	PAD;LCD/KB,ANIT-STATIC,8080	
224671830001	PALLET;1300*1100*126,GP2	
221675350002	PARTITION;AK BOX,8080	
221600050218	PARTITION;BATTERY,MARLIN,CAIMAN,	
221675350001	PARTITION;IN CARTON,8080	
221675350013	PARTITION;PALLET,W/CARRYING BAG,	
221600050219	PARTITION;TOP/BTM,BATTERY,MARLIN	
221675350009	PARTITION;W/CARRYING BAG,8080	
412672300001	PCB ASSY;FAX MODEM 56K,MDC56S-I,	
316675300002	PCB;PWA-8080/BATT GAUGE BD,SMT	
316675300003	PCB;PWA-8080/BATT PROTECTION BD,	
316675300005	PCB;PWA-8080/CD-ROM TRANS BD	R00

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Part Number	Description	Location(US)
316675300001	PCB;PWA-8080/MOTHER BD	R03
316675300004	PCB;PWA-8080/TRANS BD	R03
316503400101	PCB;PWA-STINGRAY/INVERTER BD	
222600020049	PE BAG;50*70MM,W/SEAL,COMMON	
222600020310	PE BAG;70X100MM,W/SEAL,COMMON	
222670820003	PE BAG;L560*W345,7521N	
222670000001	PE BUBBLE BAG;BATTERY,7521	
222503220001	PE BUBBLE BAG;BATTERY,GRAMPUS	
411675300013	PWA,PWA-8080/BATT BD,SANYO	
411675300014	PWA,PWA-8080/BATT GAUGE BD,SANYO	
411675300015	PWA,PWA-8080/BATT PROTECTION BD,	
411675300012	PWA;PWA-8080,CD-ROM,TRANSLATION	
411675300001	PWA;PWA-8080,MOTHER BD	
411675300003	PWA;PWA-8080,MOTHER BD,SMT	
411675300002	PWA;PWA-8080,MOTHER BD,T/U	
411675300005	PWA;PWA-8080,TRANSLATION BD,SMT	
411675300004	PWA;PWA-8080,TRANSLATION BD,T/U	
411503400201	PWA;PWA-STINGRAY/INVERTER BD	
411503400202	PWA;PWA-STINGRAY/INVERTER BD,SMT	
332810000034	PWR CORD;250V/2.5A,2P,BLK,EU,175	
271046017301	RES;.001,2W,5%,2512,CYNTEC,SMT	PR35
271046087301	RES;.008 ,2W,5% ,2512,SMT	PR71
271045107101	RES;.01 ,1W ,1% ,2512,SMT	PR59,PR62,PR70
271586026101	RES;.02 ,2W,1%,2512,SMT	PR24,PR505
271046257101	RES;.025 ,2W ,1% ,2512,SMT,PRC	R18,R18A

Part Number	Description	Location(US)
271002000301	RES;0 ,1/10W,5% ,0805,SMT	L13,L32,L36,L529,L6,R202,R310
271002000301	RES;0 ,1/10W,5% ,0805,SMT	R15
271071000002	RES;0 ,1/16W,5% ,0603,SMT	L527,PR103,PR104,PR34,PR38,P
271071000002	RES;0 ,1/16W,5% ,0603,SMT	R10,R4
271071127111	RES;1.27K,1/16W,1% ,0603,SMT	R181
271071152101	RES;1.5K ,1/16W,1% ,0603,SMT	
271071152101	RES;1.5K ,1/16W,1% ,0603,SMT	R540
271071196111	RES;1.96K,1/16W,1% ,0603,SMT	PR105
271071100302	RES;10 ,1/16W,5% ,0603,SMT	
271071100302	RES;10 ,1/16W,5% ,0603,SMT	PR18,PR536,PR77,PR90,PR91,R1
271071102211	RES;10.2K,1/16W,1% ,0603,SMT	
271071101101	RES;100 ,1/16W,1% ,0603,SMT	R191,R208,R576,R582,R586
271071101301	RES;100 ,1/16W,5% ,0603,SMT	R248,R529
271071101301	RES;100 ,1/16W,5% ,0603,SMT	R6
271071104101	RES;100K ,1/16W,1% ,0603,SMT	
271071104101	RES;100K ,1/16W,1% ,0603,SMT	PR22,PR540,PR8
271071104101	RES;100K ,1/16W,1% ,0603,SMT	R14,R16,R23
271071104101	RES;100K ,1/16W,1% ,0603,SMT	R2,R7
271071104302	RES;100K ,1/16W,5% ,0603,SMT	PR13,PR14,PR15,PR39,PR507,PR
271071104302	RES;100K ,1/16W,5% ,0603,SMT	R19
271071107311	RES;107K ,1/16W,1% ,0603,SMT	PR83
271071103701	RES;10K ,1/16W,.1%,0603,SMT	PR10,PR7,R182
271071103101	RES;10K ,1/16W,1% ,0603,SMT	
271071103101	RES;10K ,1/16W,1% ,0603,SMT	PR21,PR25,PR55,PR56,PR63,PR7
271071103302	RES;10K ,1/16W,5% ,0603,SMT	PR537,R10,R110,R126,R135,R142

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Part Number	Description	Location(US)
271071103302	RES;10K ,1/16W,5% ,0603,SMT	R20,R21
271071106301	RES;10M ,1/16W,5% ,0603,SMT	R52,R59
271071131101	RES;130 ,1/16W,1% ,0603,SMT	R83
271071134701	RES;130K ,1/16W,0.1% ,0603,SMT	PR5
271071137011	RES;137 ,1/16W,1% ,0603,SMT	R177
271071141102	RES;140 ,1/16W,1% ,0603,SMT	R584
271071151101	RES;150 ,1/16W,1% ,0603,SMT	R548,R571,R594,R597,R82,R91
271071151302	RES;150 ,1/16W,5% ,0603,SMT	R60
271071154101	RES;150K ,1/16W,1% ,0603,SMT	
271071153101	RES;15K ,1/16W,1% ,0603,SMT	
271071153101	RES;15K ,1/16W,1% ,0603,SMT	PR12
271071153301	RES;15K ,1/16W,5% ,0603,SMT	R311,R650,R652
271071184301	RES;180K ,1/16W,5% ,0603,SMT	R341,R515
271071102102	RES;1K ,1/16W,1% ,0603,SMT	
271071102102	RES;1K ,1/16W,1% ,0603,SMT	PR555,R507,R521,R87,R94
271071102302	RES;1K ,1/16W,5% ,0603,SMT	R210,R211,R218,R232,R238,R284
271071102302	RES;1K ,1/16W,5% ,0603,SMT	R6
271071102302	RES;1K ,1/16W,5% ,0603,SMT	R10,R24,R5,R8
271071105101	RES;1M ,1/16W,1% ,0603,SMT	
271071105101	RES;1M ,1/16W,1% ,0603,SMT	PR85
271071105301	RES;1M ,1/16W,5% ,0603,SMT	PR101,PR11,PR41,PR517,PR68,R
271071105301	RES;1M ,1/16W,5% ,0603,SMT	R11,R3,R9
271071228301	RES;2.2 ,1/16W,5% ,0603,SMT	R303
271071222302	RES;2.2K ,1/16W,5% ,0603,SMT	R235,R236,R31,R44,R508,R533,R
271071225301	RES;2.2M,1/16W,5% ,0603,SMT	R1,R4

Part Number	Description	Location(US)
271071249111	RES;2.49K,1/16W,1% ,0603,SMT	PR26
271071272101	RES;2.7K ,1/16W,1% ,0603,SMT	PR538
271071201301	RES;200 ,1/16W,5% ,0603,SMT	PR32,PR36,R49
271071201301	RES;200 ,1/16W,5% ,0603,SMT	R15,R17
271071203101	RES;20K ,1/16W,1% ,0603,SMT	
271071203101	RES;20K ,1/16W,1% ,0603,SMT	PR503,PR526,PR57,PR64,PR73,P
271071203302	RES;20K ,1/16W,5% ,0603,SMT	R237
271071220101	RES;22 ,1/16W,1% ,0603,SMT	R128
271071221302	RES;22 ,1/16W,5% ,0603,SMT	R196,R252,R327,R331,R355,R364
271071221302	RES;22 ,1/16W,5% ,0603,SMT	R11,R7,R9
271071232271	RES;23.2K,1/16W,.1%,0603,SMT	PR6
271071243011	RES;243 ,1/16W,1% ,0603,SMT	R583
271071249311	RES;249K ,1/16W,1% ,0603,SMT	PR31
271071261212	RES;26.1K,1/16W,1%,0603,SMT	PR58
271071274811	RES;27.4 ,1/16W,1% ,0603,SMT	R25,R520,R549,R566,R573,R98
271071283101	RES;28K ,1/16W,1% ,0603,SMT	PR541
271071294311	RES;294K ,1/16W,1% ,0603,SMT	PR3
271071202102	RES;2K ,1/16W,1% ,0603,SMT	R178,R88
271071202301	RES;2K ,1/16W,5% ,0603,SMT	R634
271071205101	RES;2M ,1/16W,1% ,0603,SMT	
271071332302	RES;3.3K ,1/16W,5% ,0603,SMT	PR17
271071301101	RES;300 ,1/16W,1% ,0603,SMT	PR554
271071301301	RES;300 ,1/16W,5% ,0603,SMT	R22
271071301011	RES;301 ,1/16W,1% ,0603,SMT	R547,R572
271071301311	RES;301K ,1/16W,1% ,0603,SMT	PR1,PR534

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Part Number	Description	Location(US)
271071309311	RES;309K ,1/16W,1% ,0603,SMT	R12
271071324012	RES;324K ,1/16W,1% ,0603,SMT	PR506
271071330302	RES;33 ,1/16W,5% ,0603,SMT	R105,R107,R108,R109,R111,R112
271071331101	RES;330 ,1/16W,1% ,0603,SMT	R580
271071331301	RES;330 ,1/16W,5% ,0603,SMT	R176,R348,R349,R350,R351,R352
271071333301	RES;33K ,1/16W,5% ,0603,SMT	PR19,PR508,R204,R616,R651,R65
271071333301	RES;33K ,1/16W,5% ,0603,SMT	R13
271071390302	RES;39 ,1/16W,5% ,0603,SMT	R65
271071478301	RES;4.7 ,1/16W,5% ,0603,SMT	PR4
271013478301	RES;4.7 ,1/4W,5% ,1206,SMT	R16,R18
271071475112	RES;4.75K,1/16W,1% ,0603,SMT	PR60,PR94
271002472301	RES;4.7K ,1/10W,5% ,0805,SMT	PR29,PR37
271071472302	RES;4.7K ,1/16W,5% ,0603,SMT	PR509,PR510,R114,R158,R173,R2
271071472302	RES;4.7K ,1/16W,5% ,0603,SMT	R3
271071499111	RES;4.99K,1/16W,1% ,0603,SMT	PR504,R598
271071402811	RES;40.2 ,1/16W,1% ,0603,SMT	R556
271071431102	RES;432 ,1/16W,1% ,0603,SMT	PR539
271071433301	RES;43K ,1/16W,5% ,0603,SMT	R258,R268,R269,R271,R273,R274
271071471101	RES;470 ,1/16W,1% ,0603,SMT	
271071471302	RES;470 ,1/16W,5% ,0603,SMT	R323,R366,R376,R687
271071471302	RES;470 ,1/16W,5% ,0603,SMT	R13
271071474301	RES;470K ,1/16W,5% ,0603,SMT	PR30,PR74,PR95,R4,R5
271071475011	RES;475 ,1/16W,1% ,0603,SMT	R124
271071473301	RES;47K ,1/16W,5% ,0603,SMT	PR9,R205,R32,R361,R365,R379,R
271071473301	RES;47K ,1/16W,5% ,0603,SMT	R12

Part Number	Description	Location(US)
271071487811	RES;48.7 ,1/16W,1% ,0603,SMT	R89
271071487211	RES;48.7K,1/16W,1% ,0603,SMT	
271071487011	RES;487 ,1/16W,1% ,0603,SMT,MUS	R90
271071499811	RES;49.9 ,1/16W,1% ,0603,SMT	R115,R120,R125,R129,R137,R154
271071499211	RES;49.9K,1/16W,1% ,0603,SMT	PR535
271002515302	RES;5.1M ,1/8W ,5% ,0805,SMT,PRC	
271071562111	RES;5.62K,1/16W,1% ,0603,SMT	PR78
271071562301	RES;5.6K ,1/16W,5% ,0603,SMT	R375
271071562301	RES;5.6K ,1/16W,5% ,0603,SMT	R25
271071510301	RES;51 ,1/16W,5% ,0603,SMT	R28,R37,R512,R517,R518,R56
271071549811	RES;54.9 ,1/16W,1% ,0603,SMT	R24,R26,R27,R590,R591,R592,R5
271071560301	RES;56 ,1/16W,5% ,0603,SMT	R194,R200,R214,R215,R219,R221
271071561101	RES;560 ,1/16W,1% ,0603,SMT	
271071604111	RES;6.04K,1/16W,1% ,0603,SMT	R259
271071619111	RES;6.19K,1/16W,1% ,0603,SMT	PR28
271071634111	RES;6.34K,1/16W,1% ,0603,SMT	PR525,R599
271071682301	RES;6.8K ,1/16W,5% ,0603,SMT	R301,R302,R308,R309
271071604811	RES;60.4 ,1/16W,1% ,0603,SMT	R587,R588
271071604112	RES;604,1/16W,1% ,0603,SMT	R595,R596
271071634211	RES;63.4K,1/16W,1% ,0603,SMT	PR80
271071681301	RES;680 ,1/16W,5% ,0603,SMT	R75
271071684101	RES;680K ,1/16W,1% ,0603,SMT	PR27
271071683101	RES;68K ,1/16W,1% ,0603,SMT	
271071698311	RES;698K ,1/16W,1% ,0603,SMT	R22
271071750101	RES;75 ,1/16W,1% ,0603,SMT	R185,R186,R222,R224,R229,R230

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Part Number	Description	Location(US)
271071751101	RES;750 ,1/16W,1% ,0603,SMT	R180
271071750311	RES;750K,1/16W,1% ,0603,SMT	PR84
271071787311	RES;787K ,1/16W,1% ,0603,SMT	PR16
271071806111	RES;8.06K,1/16W,1% ,0603,SMT	PR100,PR527
271071822301	RES;8.2K ,1/16W,5% ,0603,SMT	R103,R104,R123,R132,R150,R152
271071806211	RES;80.6K,1/16W,1% ,0603,SMT	PR72
271071887211	RES;88.7K,1/16W,1% ,0603,SMT	
271071909011	RES;909 ,1/16W,1% ,0603,SMT	
451675300031	ROM ME KIT;8080	
271611000301	RP;0*4 ,8P ,1/16W,5% ,0612,SMT	RP3,RP46
271571000301	RP;0*8 ,16P ,1/16W,5% ,1606,SM	RP10,RP42,RP43,RP44,RP8,RP9
271571100301	RP;10*8 ,16P ,1/16W,5% ,1606,SM	RP11,RP13,RP15,RP17,RP20,RP2
271611272301	RP;2.7K*4,8P ,1/16W,5% ,0612,SMT	RP6
271621472302	RP;4.7K*8,10P,1/32W,5% ,1206,SMT	RP39,RP45,RP47,RP503,RP505,R
271611473301	RP;47K*4 ,8P ,1/16W,5% ,0612,SMT	RP5
271621473301	RP;47K*8 ,10P,1/16W,5% ,1206,SMT	RP41,RP502
271611560301	RP;56*4 ,8P ,1/16W,5% ,0612,SMT	RP23,RP27,RP29
271571560302	RP;56*8 ,16P,1/16W,5% ,1606,SMT	RP12,RP14,RP16,RP18,RP19,RP2
271611750301	RP;75*4 ,8P ,1/16W,5% ,0612,SMT	RP501
271611822301	RP;8.2K*4,8P ,1/16W,5% ,0612,SMT	RP1,RP2,RP4,RP7
345503400501	RUBBER;3MM,ROUND,8175	
345675300015	RUBBER;M-B, 8080	
345675300006	RUBBER;PAD DOWN,LCD,8080	
345675300004	RUBBER;PAD.UPPER,LCD,8080	
565167530001	S/W;CD ROM,SYSTEM DRIVER,8080	

Part Number	Description	Location(US)
340675300005	SCREW ASSY;CPU,8080	
341675300007	SHIELDING;HDD,8080	
333050000120	SHRINK TUBE;600V,105'C,D0.8*9MM,	
333050000107	SHRINK TUBE;UL,600V,105'C,ID2.5*	
561860000022	SINGLE PAGE;GN,NOTE FOR BATTERY&	
361400003021	SOLDER CREAM;NOCLEAN,P4020870980	
361400003021	SOLDER CREAM;NOCLEAN,P4020870980	
365350000003	SOLDER WIRE;0.8MM,SN43/PB43/BI14	
600100010009	SOLDER WIRE;63/37,0.8,CM,N/C,PRC	
600100010005	SOLDER WIRE;63/37,0.8,NA,N/C,PRC	
370102610401	SPC-SCREW;M2.6L4,K-HD,t0.8,NIB/N	
370102630601	SPC-SCREW;M2.6L6,HDt0.5,NIWNLK	
370102610603	SPC-SCREW;M2.6L6,K-HD,NIB/NLK	
370102610801	SPC-SCREW;M2.6L8,NIB,K-HD,t=1.1,	
370102010205	SPC-SCREW;M2L2(t0.3),N/W/WLK	
370102030301	SPC-SCREW;M2L3,K-HD,1,NIB/NLK	
370102030301	SPC-SCREW;M2L3,K-HD,1,NIB/NLK	
370102010309	SPC-SCREW;M2L3.0,NIW/NLK,HD07	
370102010407	SPC-SCREW;M2L4,K-HD,NIB/NLK	
370102010407	SPC-SCREW;M2L4,K-HD,NIB/NLK	
370102010407	SPC-SCREW;M2L4,K-HD,NIB/NLK	
370102010505	SPC-SCREW;M2L5,K-HD(t0.4),NIB,NL	
370102010505	SPC-SCREW;M2L5,K-HD(t0.4),NIB,NL	
370102010505	SPC-SCREW;M2L5,K-HD(t0.4),NIB,NL	
370102010702	SPC-SCREW;M2L7,K-HD,NLK,NIW	

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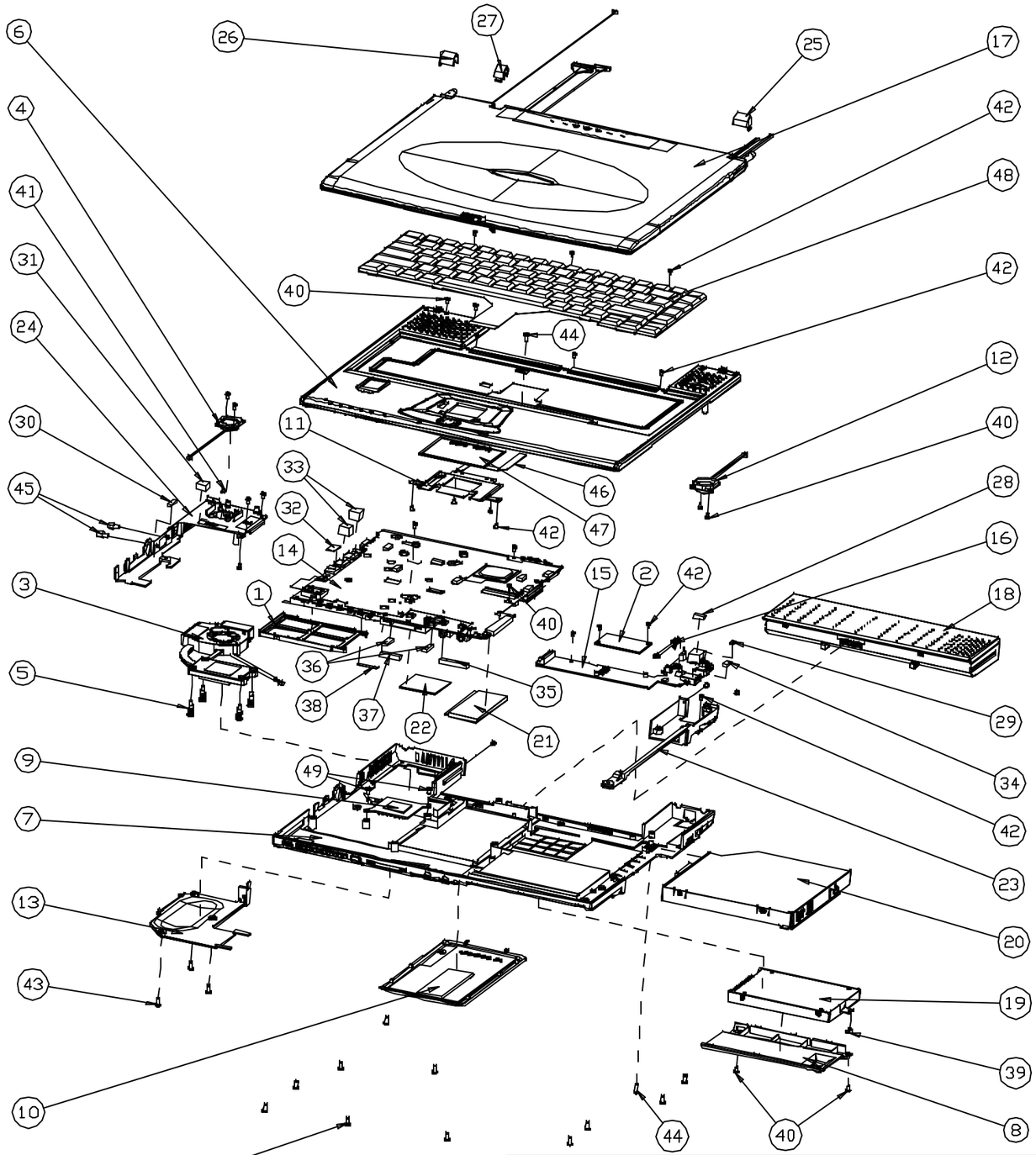
Part Number	Description	Location(US)
370103010405	SPC-SCREW;M3L4,NIW,K-HD,T0.3	
340675300026	SPEAKER ASSY; R, 8080	
340675300004	SPEAKER ASSY;L, 8080	
226600030332	SPONGE;320*290*10,CAIMAN,PWR	
377244010002	STANDOFF;#4-40DP3.5H5L5.5,NIW	
341675300008	STANDOFF;CPU,8080	MTG12,MTG13,MTG14,MTG15
341675300009	STANDOFF;MDC,8080	MTG3,MTG4
297120101005	SW;DIP,SPST,8P,50VDC,.1A,SMT,DHS	SW2
297040100013	SW;MINIATURE SLIDE,300MA,4V,7P,S	SW501
297040105012	SW;PUSH BUTTOM,4P,SP,12V/50MA,H2	SW3,SW4,SW5,SW6,SW7,SW8
297040200004	SW;PUSH BUTTON,4P,12V/50MA,PT-03	SW502,SW503,SW504,SW505,SW
297120100009	SW;SPST,4P,24VDC,50MA,STS-KD5,HC	SW1
297030102001	SW;TOGGLE,SPST,5V/0.2mA,H10.7MM,	SW2
225600000061	TAPE;ADHENSIVE,DOUBLE-FACE,W20,U	
225600000310	TAPE;ADHENSIVE,DOUBLE-FACE,W8,UL	
622200000008	TAPE;CARTON,2.5"W,30M/RL,PRC	
225600000054	TAPE;INSULATING,POLYESTER FILM,1	
335612000004	THERMAL CUTOFFS;378,8A/50VDC,139	
442167530001	TOUCH PAD MODULE;TM41PUR2311-2,S	
288227002006	TRANS;2N7002LT1,N-CHANNEL FET,ES	PQ11,PQ12,PQ14,PQ15,PQ16,PQ
288227002001	TRANS;2N7002LT1,N-CHANNEL FET,SO	Q15,Q16,Q515,Q516,Q517
288204900001	TRANS;AO4900,DUAL N-MOSFET WITH	PU16,PU17,PU19,PU5
628820014401	TRANS;DTA144EKA,PNP,100MA,50V,SO	Q3,Q5
288200144002	TRANS;DTA144WK,PNP,SMT	PQ508,Q513
288200144003	TRANS;DTC144TKA,N-MOSFET,SOT-23	Q10,Q13,Q17,Q18,Q19,Q21,Q25,(

Part Number	Description	Location(US)
288200144001	TRANS;DTC144WK,NPN,SOT-23,SMT	PQ503,Q20,Q23,Q24,Q34,Q5,Q51
288206694002	TRANS;FDS6694,N-MOSFET,SO8,SMT	PU507,PU509
288207822001	TRANS;IRF7822,N-MOSFET,.005OHM,S	PU20,PU501,PU504,PU56
288202222001	TRANS;MMBT2222AL,NPN,TO236AB	PQ506
288203906002	TRANS;MMBT3906L,40V,200mA,SOT23,	
288202301001	TRANS;SI2301DS,P-MOSFET,SOT-23	Q1,Q22,Q37,Q511,Q512
288204532001	TRANS;SI4532DY,N&P-MOSFET,SO8,PR	
288204788001	TRANS;SI4788CY,P-MOS,5A1.8~5.5V,	U14,U23,U24,U25,U27
288204800001	TRANS;SI4800DY,N-MOS,.0185OHM,SO	PU14,PU15,PU18,PU21,Q4
288204832001	TRANS;SI4832DY,N-MOSFET,.028OHM,	PU503
288204835001	TRANS;SI4835DY,PMOS,6A/30V,.035,	PQ5,PQ501,PQ502,PQ504
288204925001	TRANS;SI4925DY,P-MOSFET,SO-8	PU1
288208103001	TRANS;TPC8103,11A/30V,P-MOSFET,S	Q1,Q1A,Q2,Q2A
270140000003	VARISTOR;280V,5.6X3.8MM,TVB280-0	S1
421675300010	WIRE ASSY;ANTENNA,8080	
421675300009	WIRE ASSY;INVERT,8080	
421675300014	WIRE ASSY;LI,3V,RTC BATTERY,CR20	
421675300011	WIRE ASSY;MDC,8080	
421675300005	WIRE ASSY;QDI,14,8080	
332110020111	WIRE;#20,UL1007,120MM,RED,YIYI;P	
332110020162	WIRE;#20,UL1007,45MM,RED,YIYI,PW	
332110020093	WIRE;#20,UL1007,55MM,BLK,YIYI;PW	
332110028161	WIRE;#28,UL1061,132MM,YELLOW,YIY	
332110028164	WIRE;#28,UL1061,26MM,BLACK,YIYI,	
332110028162	WIRE;#28,UL1061,28MM,WHITE,YIYI,	

9. Spare Parts List - 13

Part Number	Description	Location(US)
332110028163	WIRE;#28,UL1061,80MM,BLUE,YIYI,P	
273001050039	XSFORMER;10/100 BASE,LF-H80P,SMT	U11
273001050062	XSFORMER;CI8.5,SIT16260,16/2600T	
274011431408	XTAL;14.318M,50PPM,32PF,7*5,4P,S	X2
274011431424	XTAL;14.318MHZ,20PPM,20PF,7*5,SM	X501
274011600408	XTAL;16MHZ,16PF,50PPM,8*4.5,2P	X502
274012457406	XTAL;24.576MHZ,16PF,50PPM,8*4.5,	X3
274012500401	XTAL;25MHZ,30PPM,18PF,4P,SMT	X4
274013276103	XTAL;32.768KHZ,20PPM,12.5PF,CM20	X1
		P/N:526267530024



ITEM	PART NO	DESCRIPTION	Q'TY	TYPE	REMARK
1	344675300034	DUMMY CARD; PCMCIA. 8080	1	PART	*
2	412674500004	PCB ASSY; FAX, MODEM, 56K, MDC56S-I,GP3	1	PART	*
3	340675300003	HEATSINK ASSY;8080	1	ASSEMBLY	
4	340675300004	SPEAKER ASSY; L, 8080	1	ASSEMBLY	
5	340675300005	SCREW ASSY;CPU,8080	4	ASSEMBLY	
6	340675300006	COVER;ASSY,8080	1	ASSEMBLY	
7	340675300007	HOUSING ASSY; 8080	1	ASSEMBLY	
8	340675300010	COVER ASSY; HDD. 8080	1	ASSEMBLY	
9	340675300012	HEATSINK ASSY;NORTH BRIDGE,8080	1	ASSEMBLY	
10	340675300013	COVER; ASSY, DIMM, 8080	1	ASSEMBLY	
11	340675300015	BRACKET;ASSY,TOUCHPAD,8080	1	ASSEMBLY	
12	340675300026	SPEAKER ASSY; R, 8080	1	ASSEMBLY	
13	344675300027	COVER; HEATSINK, 8080	1	ASSEMBLY	
14	411675300001	PWA; PWA-8080, MOTHER BD	1	ASSEMBLY	
15	411675300004	PWA;PWA-8080,TRANSLATION BD,T/U	1	ASSEMBLY	
16	421675300011	WIRE ASSY;MDC,8080	1	ASSEMBLY	
17	441675300001	LCD ASSY;TFT,QDI,14.1",XGA,X/O GPRS,8080	1	ASSEMBLY	
18	442675300001	BATT ASSY; 14.8V, 4.4AH, LI, NSL, 8080	1	ASSEMBLY	
19	523467530001	HDD ASSY;60GB,MHS6020AT,FUJITSU,8060	1	ASSEMBLY	
20	523467530015	COMBO ASSY; KME, UJDA740,8080	1	ASSEMBLY	
21	323799990090	DDR SDRAM OPTION,512MB,8080	1	PART	
22	324180786389	IC.CPU.BANIAS.1.6GHZ.MICRO-FCPGA.479P.INTE	1	PART	
23	343675300001	BRACKET; HINGE, R, 8080	1	PART	
24	343675300004	BRACKET;IO,8080	1	PART	
25	344675300010	COVER;HINGE,R,8080	1	PART	
26	344675300011	COVER;HINGE,L,8080	1	PART	
27	344675300012	COVER;CABLE,LCD,8080	1	PART	
28	345675300007	GASKET; MODEM, TRANS-B, 8080	1	PART	
29	345675300008	GASKET; 1394, TRANS-B, 8080	1	PART	
30	345675300010	GASKET; BRACKET, I/O 8080	1	PART	
31	345675300011	GASKET; I/O, 8080	1	PART	
32	345675300012	GASKET; LANS, M-B, 8080	1	PART	
33	345675300013	GASKET; USB, M-B, 8080	2	PART	
34	345675300014	GASKET; USB, TRANS-B, 8080	1	PART	
35	345675300027	GASKET; AUDIO. 8080	1	PART	
36	345675300028	GASKET; CARD_READ, M/B, 8080	2	PART	
37	345675300029	GASKET; PCMCIA, M_b-1, 8080	1	PART	
38	345675300030	GASKET; PCMCIA, M_b-2, 8080	1	PART	
39	37012012D309	SPC-SCREW; M2L3, NIV/NLK, HD07	1	PART	
40	37012012D407	SPC-SCREW; M2L4,K-HD,NIB/NLK	17	PART	
41	37012012D505	SPC-SCREW;M2L5,K-HDX10.4),NIB,NLK	2	PART	
42	37012012030D1	SPC-SCREW;M2L3.K-HD.1,NIB/NLK	14	PART	
43	370102610603	SPC-SCREW; M2.6L6, K-HD, NIB/NLK	15	PART	
44	370102610801	SPC SCREW; M2.6L8, NIB, K-HD, NLK	1	PART	
45	377244010002	STANDOFF;#4-40DP3.5H5L5.5,NIV	2	PART	
46	421467530D01	FFC; TOUCHPAD, 8080	1	PART	
47	442167530D01	TOUCH PAD MODULE,TM41PU311-2,SYNAPTICS	2	PART	
48	531017240085	KBD;87, KV-26FA-US5C01,ZIPPY,8080	1	PART	
49	37012D2610401	SPC-SCREW;M2.6L4.K-HD,t0.8,NIB/NLK	2	PART	

ITEM	CONTENTS OF CHANGE	RVS	CHK	APV	M/D/Y
					/ /
					/ /
					/ /
					/ /
					/ /

TOL± RANGE	Pla	Met	Ins	Por	Cab	Poc	Gas	PCB
0~6	0.1	0.1	0.1	0.2	0.5	1	0.5	0.1
6~30	0.1	0.1	.15	.25	1	1	0.5	0.1
30~80	0.1	.15	0.2	0.3	2	1.5	1	0.1
80~180	.15	.15	.25	0.3	2	2	1	.15
180~315	.15	0.2	0.3	0.4	2.5	2	1	.15
315~800	0.2	0.3	0.4	0.5	3	3	2	.15

DATE	26-Mar-03	MATERIAL	SEE NOTES	TREATMENT		REMARK	
UNIT	MM	SCALE	0.300	DRAWING NAME	LTXNX;8080/4GDJ/60J/1US1/L1D3A/XL		
DRAWN	DESIGNED	CHECKED	APPROVED	MATERIAL NO.	AD	526267530003	R00

MiTAC Technology Corp.

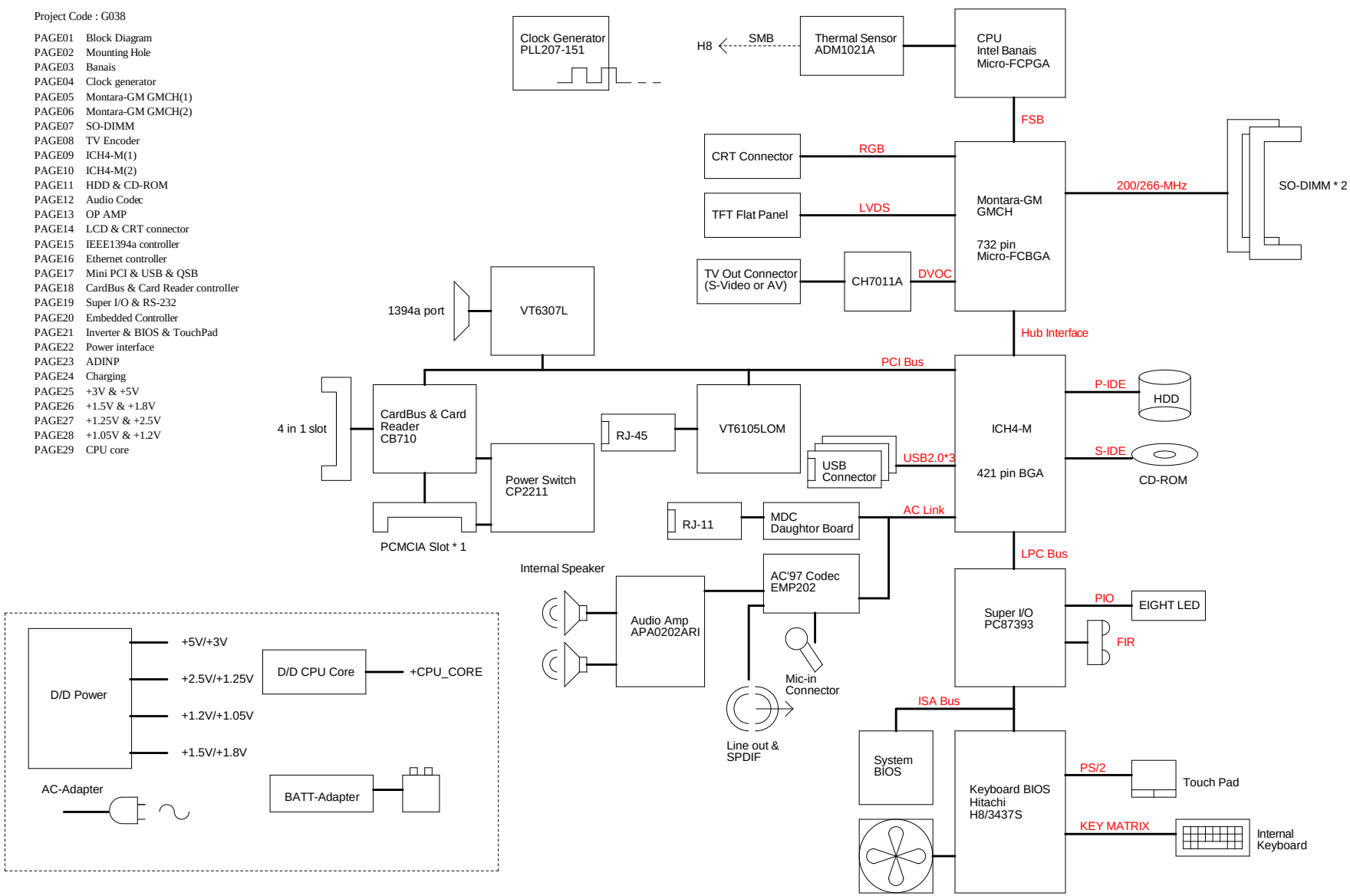
model nameMAIN_ASSY_8080

file nameMAIN_ASSY_8080

8080_R03

Project Code : G038

PAGE01 Block Diagram
PAGE02 Mounting Hole
PAGE03 Banais
PAGE04 Clock generator
PAGE05 Montara-GM GMCH(1)
PAGE06 Montara-GM GMCH(2)
PAGE07 SO-DIMM
PAGE08 TV Encoder
PAGE09 ICH4-M(1)
PAGE10 ICH4-M(2)
PAGE11 HDD & CD-ROM
PAGE12 Audio Codec
PAGE13 OP AMP
PAGE14 LCD & CRT connector
PAGE15 IEEE1394a controller
PAGE16 Ethernet controller
PAGE17 Mini PCI & USB & QSB
PAGE18 CardBus & Card Reader controller
PAGE19 Super I/O & RS-232
PAGE20 Embedded Controller
PAGE21 Inverter & BIOS & TouchPad
PAGE22 Power interface
PAGE23 ADINP
PAGE24 Charging
PAGE25 +3V & +5V
PAGE26 +1.5V & +1.8V
PAGE27 +1.25V & +2.5V
PAGE28 +1.05V & +1.2V
PAGE29 CPU core



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Title: 8080

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VT6307L
IDSEL: AD21
PCI REQ0#
PCI GNT0#
PCI INTG#

VT6105L
IDSEL: AD18
PCI REQ1#
PCI GNT1#
PCI INTE#

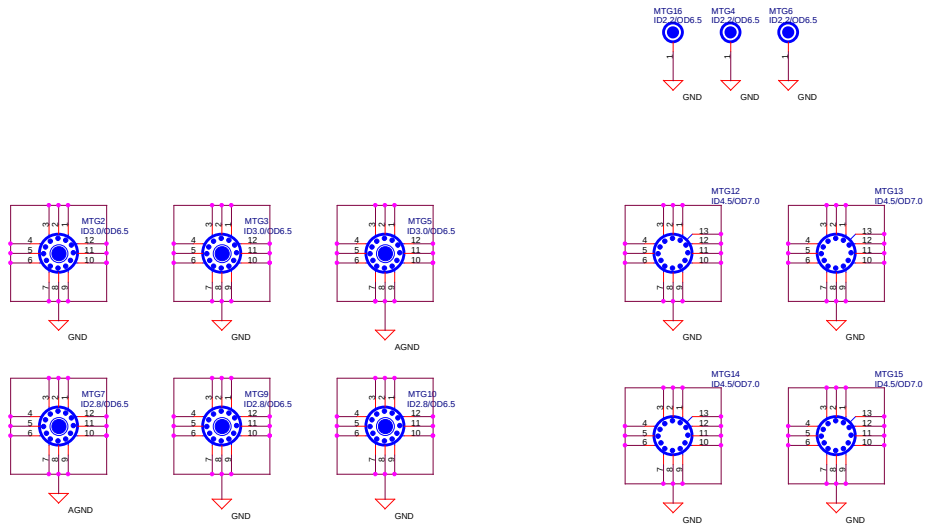
Mini PCI
IDSEL: AD17
PCI REQ3#
PCI GNT3#
PCI INTD# INTF#

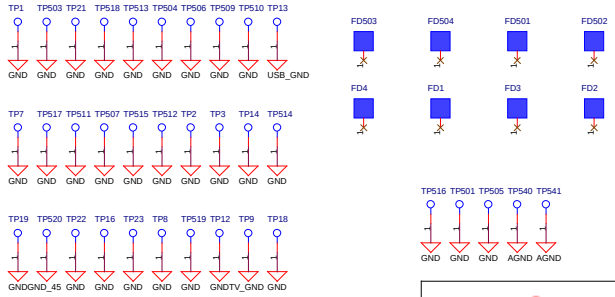
CB710
IDSEL: AD20
PCI REQ2#
PCI GNT2#
PCI INTB# INTF#

8080 Stack Up

Comp	0.5 oz Cu	
4 mil		
GND	0.5 oz Cu	
6 mil		
In1	0.5 oz Cu	
7 mil		
In2	0.5 oz Cu	
6 mil		
PWR	0.5 oz Cu	
7 mil		
In3	0.5 oz Cu	
6 mil		
GND	0.5 oz Cu	
4 mil		
Solder	0.5 oz Cu	

REV	Change detail	DATE	ECR No.
R00	Initail release (base on Banias + Odem + ICH4-M)	2002/10/28	
R01	1.Correcting the error pin definition in EVT(include DIMM, HDD, KBD & TV connector) 2.Add +3V_P for VT6105LOM to support wake on LAN. 3.Add +5V_HDD to reduce the power consumption when into Audio DJ mode. 4.Add +5V_CDROM to support IDE device hot swappable. 5.Add R535 to support Intel Wireless module power down function using quick key. 6.Remove Q21 & R291 to solve the card reader function fail. 7.Reserve the spreading spectrum circuit for EMI. 8.Change the DIMM connector from standard type to reverse type to solve the interfere problem.	2002/12/16	
R02	1.Add +5V_P to solve some USB2.0 device be downgrade to USB1.1 when resume from S3. 2. Reserve RS232 for S/W debugging if necessary.	2003/01/28	





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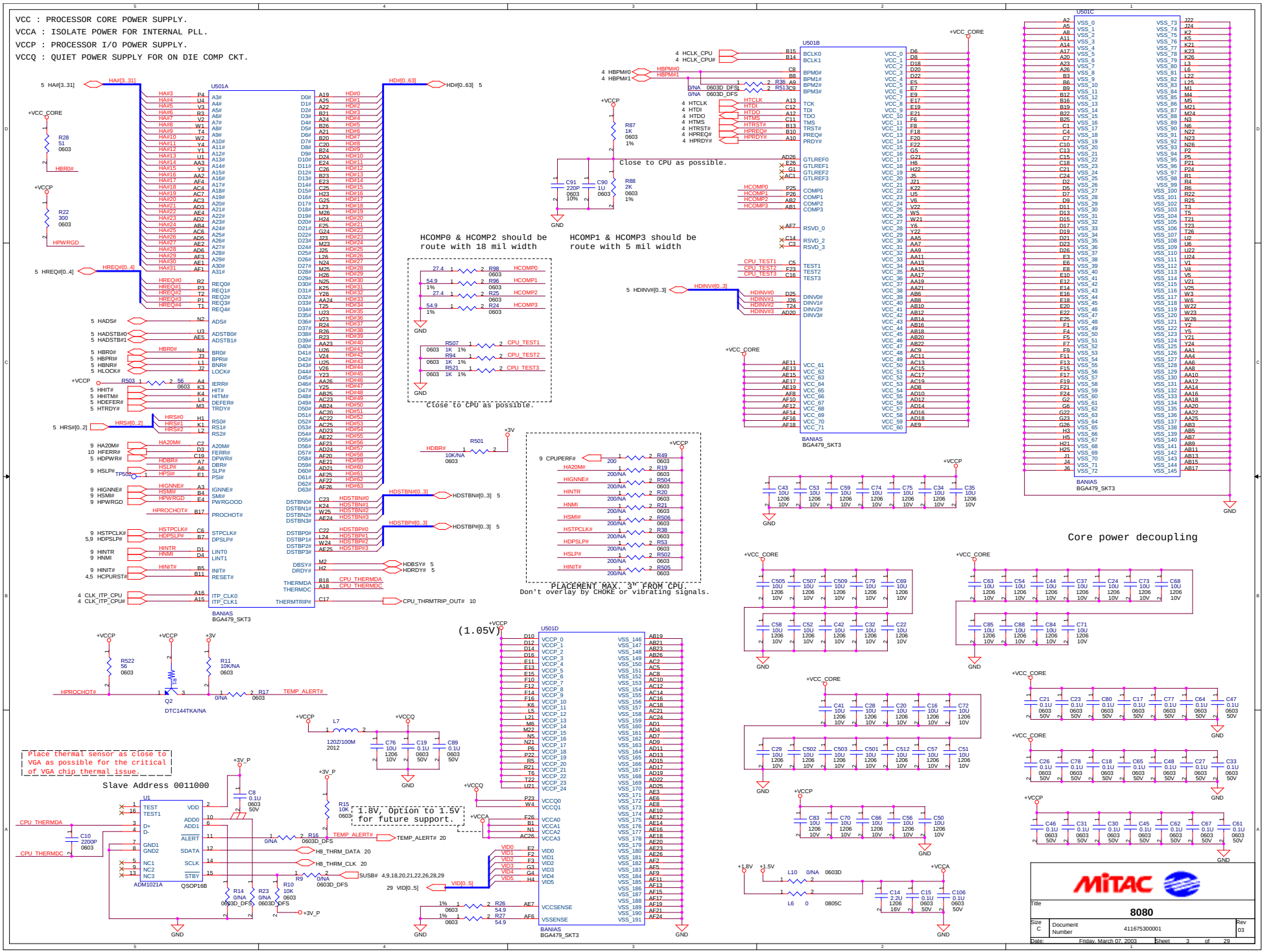

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VID 5 4 3 2 1 0	VCC-Core
0 0 0 0 0 0	1.708
0 0 0 0 0 1	1.692
0 0 0 0 1 0	1.676
0 0 0 0 1 1	1.660
0 0 0 1 0 0	1.644
0 0 0 1 0 1	1.628
0 0 0 1 1 0	1.612
0 0 0 1 1 1	1.596
0 0 1 0 0 0	1.580
0 0 1 0 0 1	1.564
0 0 1 0 1 0	1.548
0 0 1 0 1 1	1.532
0 0 1 1 0 0	1.516
0 0 1 1 0 1	1.500
0 0 1 1 1 0	1.484
0 0 1 1 1 1	1.468
0 1 0 0 0 0	1.452
0 1 0 0 0 1	1.436
0 1 0 0 1 0	1.420
0 1 0 0 1 1	1.404
0 1 0 1 0 0	1.388
0 1 0 1 0 1	1.372
0 1 0 1 1 0	1.356
0 1 0 1 1 1	1.340
0 1 1 0 0 0	1.324
0 1 1 0 0 1	1.308
0 1 1 0 1 0	1.292
0 1 1 0 1 1	1.276
0 1 1 1 0 0	1.260
0 1 1 1 0 1	1.244
0 1 1 1 1 0	1.228
0 1 1 1 1 1	1.212

VID 5 4 3 2 1 0	VCC-Core
1 0 0 0 0 0	1.196
1 0 0 0 0 1	1.180
1 0 0 0 1 0	1.164
1 0 0 0 1 1	1.148
1 0 0 1 0 0	1.132
1 0 0 1 0 1	1.116
1 0 0 1 1 0	1.100
1 0 0 1 1 1	1.084
1 0 1 0 0 0	1.068
1 0 1 0 0 1	1.052
1 0 1 0 1 0	1.036
1 0 1 0 1 1	1.020
1 0 1 1 0 0	1.004
1 0 1 1 0 1	0.988
1 0 1 1 1 0	0.972
1 0 1 1 1 1	0.956
1 1 0 0 0 0	0.940
1 1 0 0 0 1	0.924
1 1 0 0 1 0	0.908
1 1 0 0 1 1	0.892
1 1 0 1 0 0	0.876
1 1 0 1 0 1	0.860
1 1 0 1 1 0	0.844
1 1 0 1 1 1	0.828
1 1 1 0 0 0	0.812
1 1 1 0 0 1	0.796
1 1 1 0 1 0	0.780
1 1 1 0 1 1	0.764
1 1 1 1 0 0	0.748
1 1 1 1 0 1	0.732
1 1 1 1 1 0	0.716
1 1 1 1 1 1	0.700

Place close to CPU socket within 2".

FS2	FS1	FS0	CPU	3V66[5:0]	PCI*
X	0	0	166.66	66.66	33.33
X	0	1	100.00	66.66	33.33
X	1	0	200.00	66.66	33.33
X	1	1	133.33	66.66	33.33
Mid	0	0	Tristate	Tristate	Tristate
Mid	0	1	TCLK/2	TCLK/2	TCLK/2
Mid	1	0	Reserved	Reserved	Reserved
Mid	1	1	Reserved	Reserved	Reserved

001

0:0V
1:3.3V

UNIT: MHz

Layout note: Place crystal within 500 mils of CLK Gen.

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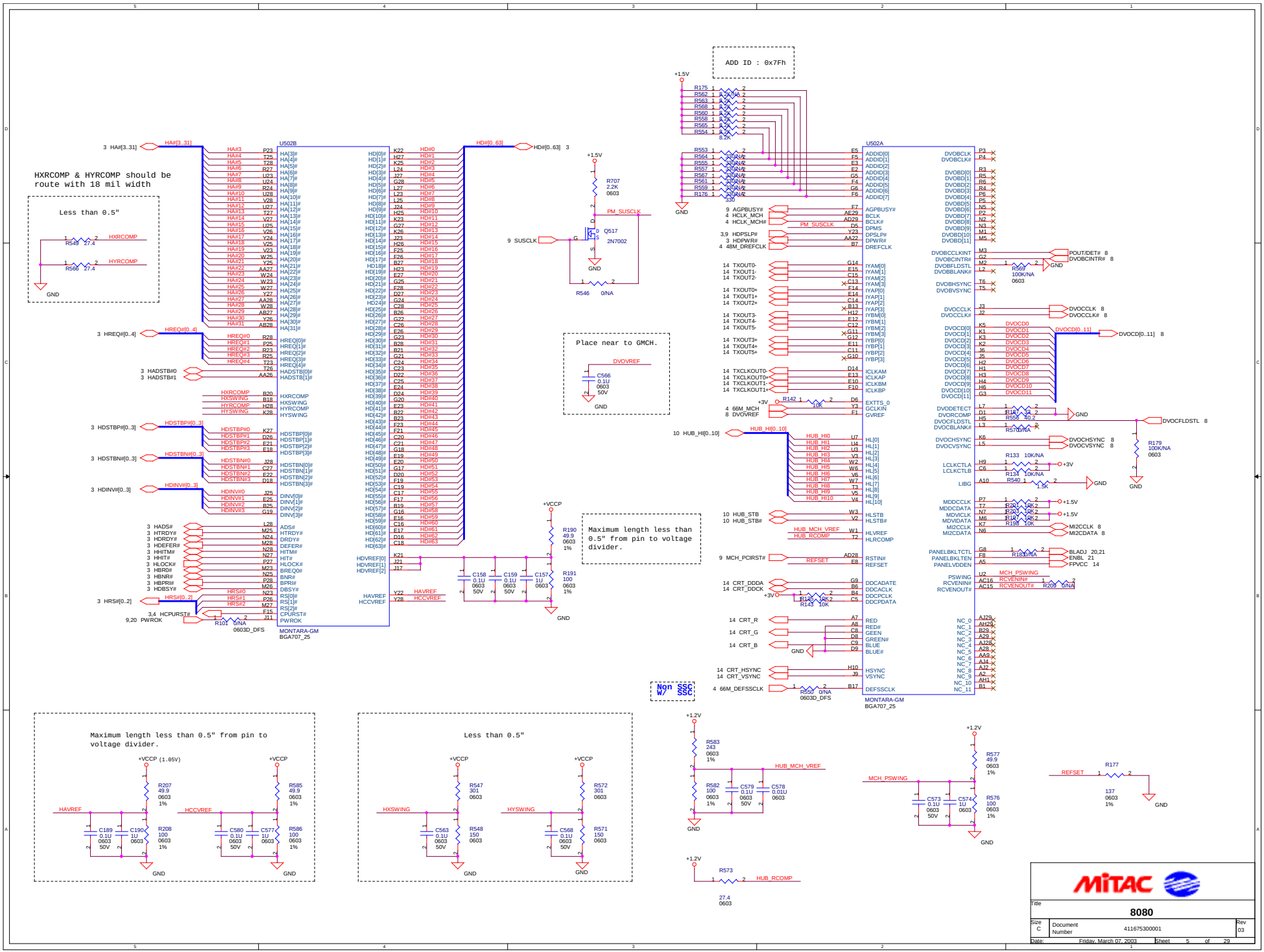

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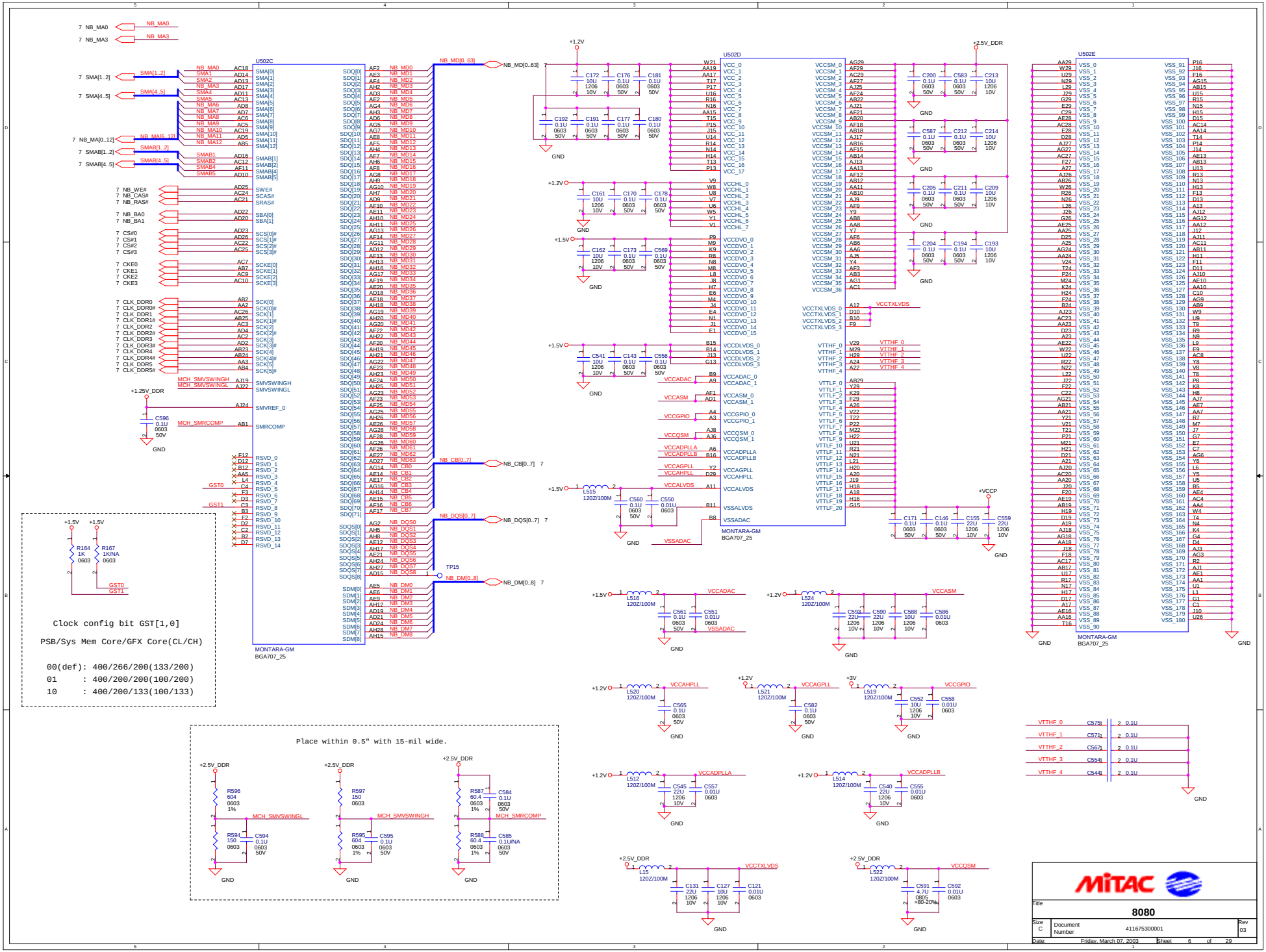

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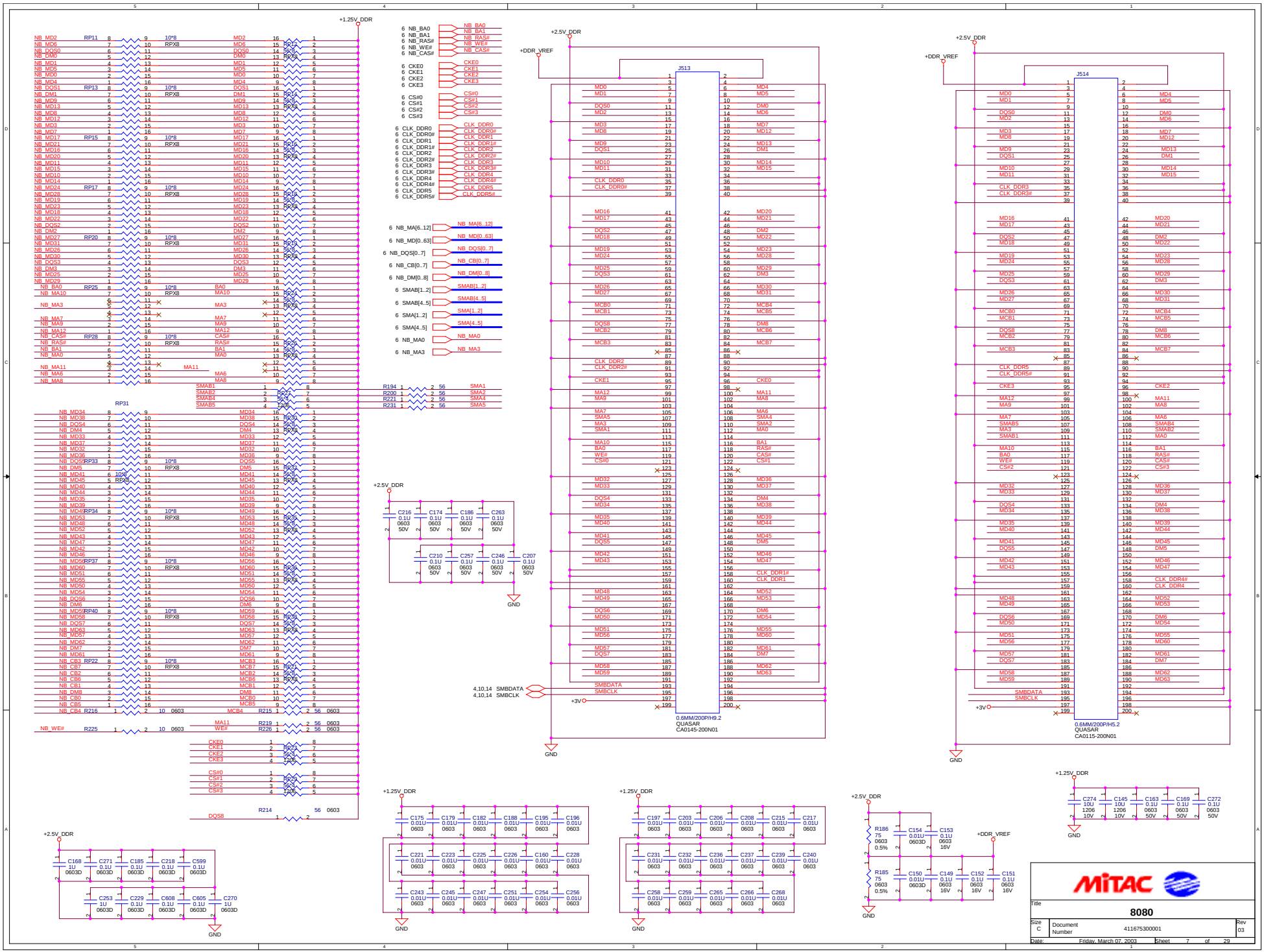

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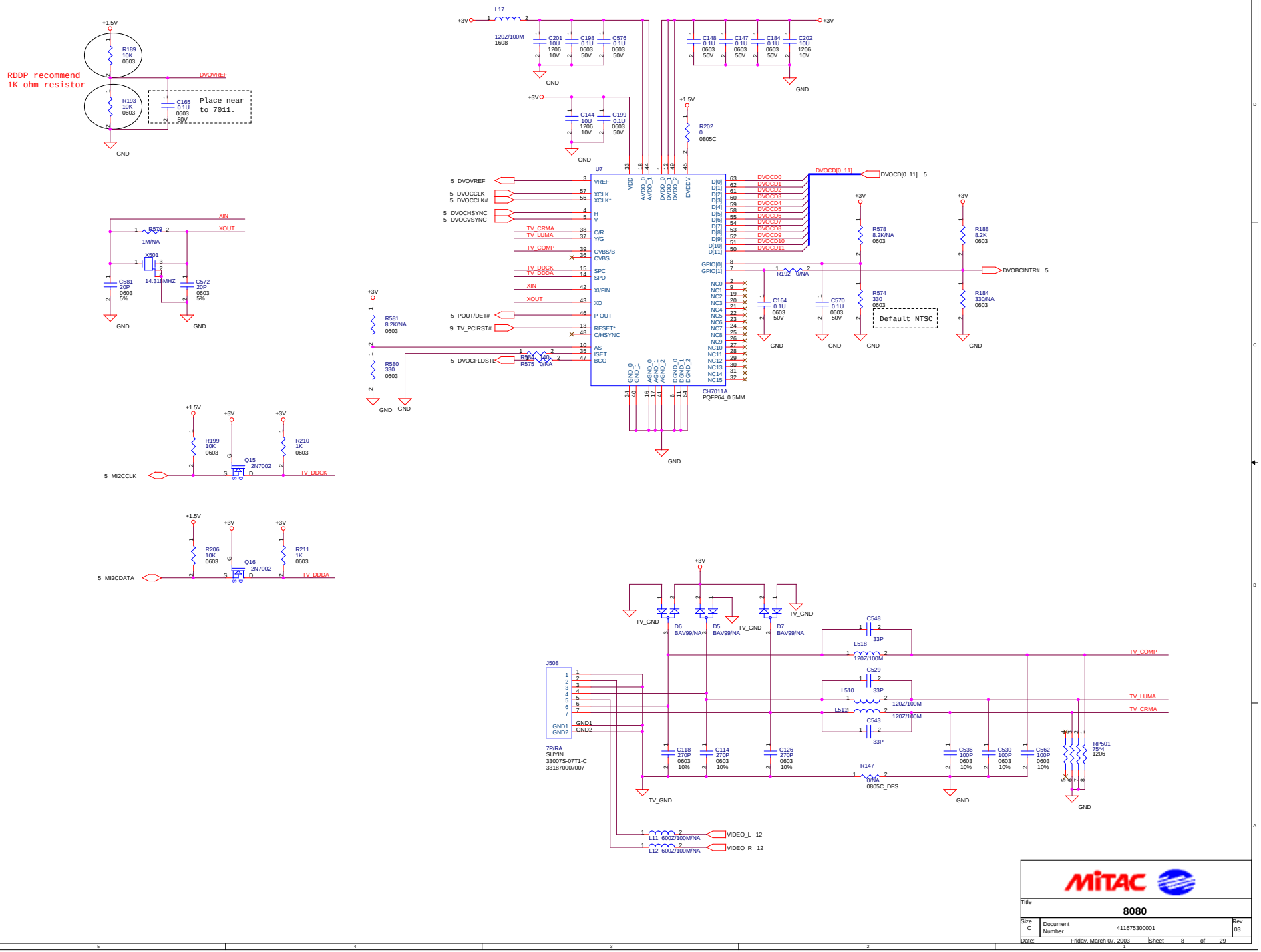

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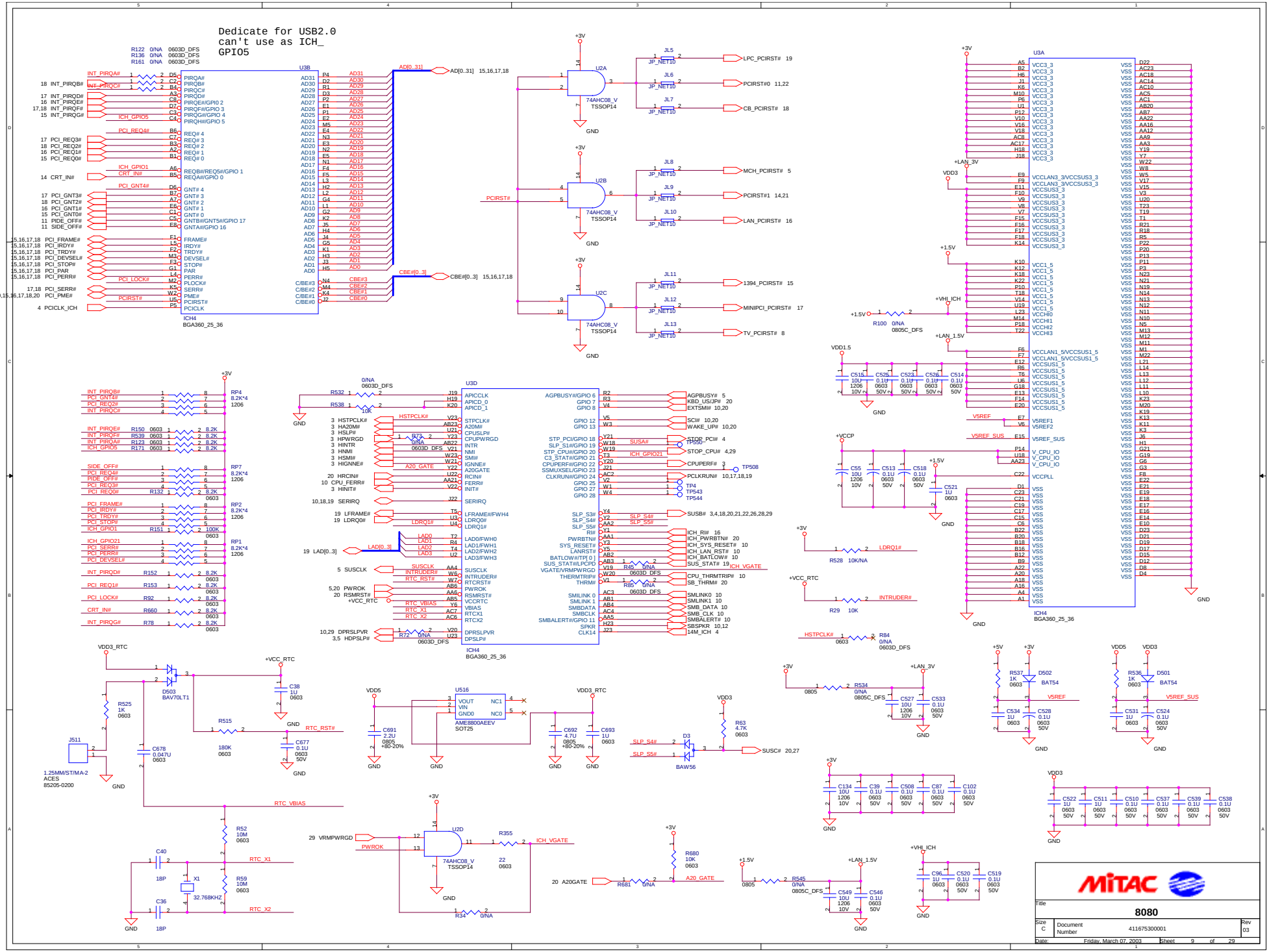

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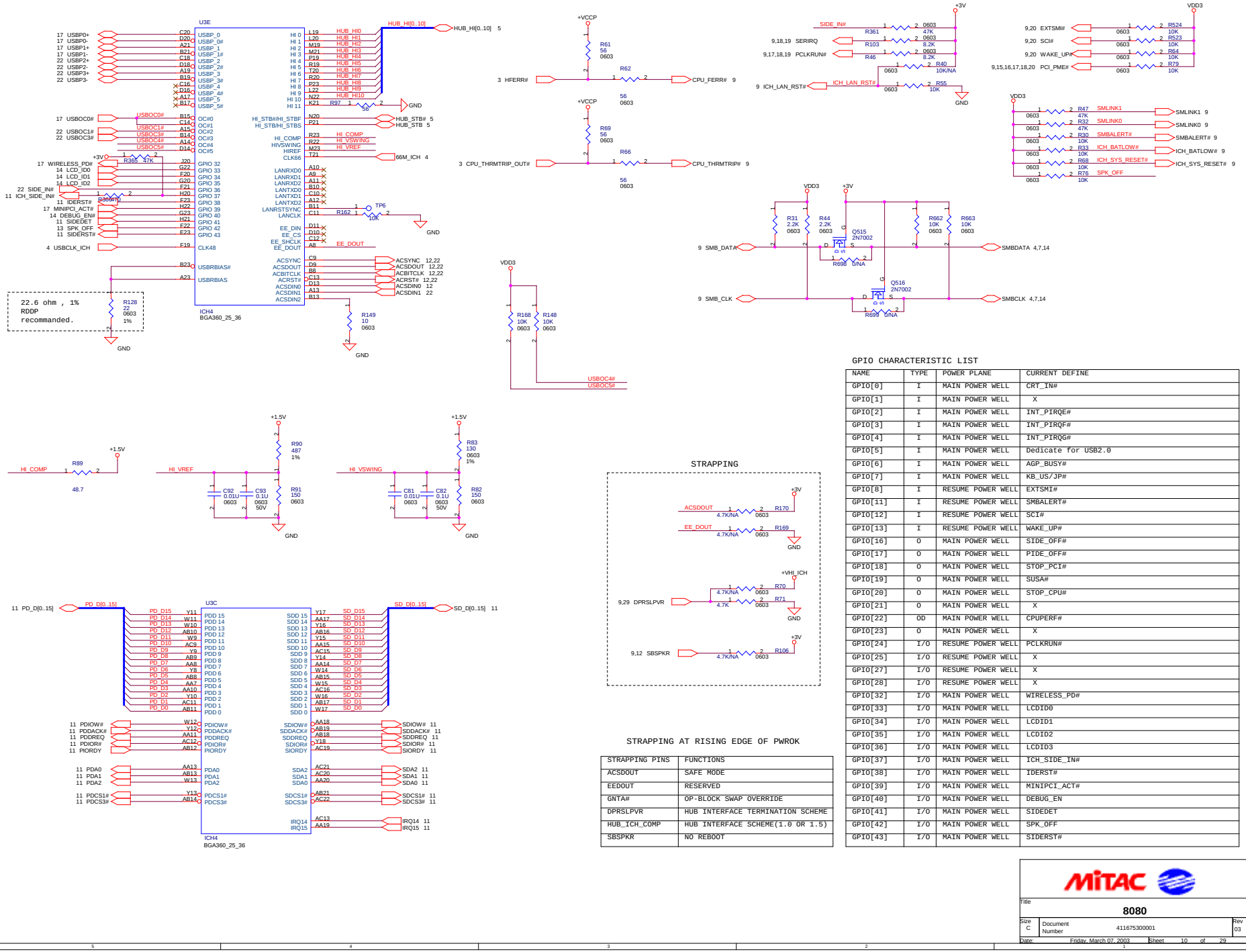

STRAPPING AT RISING EDGE OF PWROK

STRAPPING PINS	FUNCTIONS
ACSDOUT	SAFE MODE
EEDOUT	RESERVED
GNTA#	OP-BLOCK SWAP OVERRIDE
DPRSLPVR	HUB INTERFACE TERMINATION SCHEME
HUB_ICH_COMP	HUB INTERFACE SCHEME(1.0 OR 1.5)
SBSPKR	NO REBOOT

GPIO CHARACTERISTIC LIST

NAME	TYPE	POWER PLANE	CURRENT DEFINE
GPIO[0]	I	MAIN POWER WELL	CRT_IN#
GPIO[1]	I	MAIN POWER WELL	X
GPIO[2]	I	MAIN POWER WELL	INT_PIRQE#
GPIO[3]	I	MAIN POWER WELL	INT_PIRQF#
GPIO[4]	I	MAIN POWER WELL	INT_PIRQG#
GPIO[5]	I	MAIN POWER WELL	Dedicate for USB2.0
GPIO[6]	I	MAIN POWER WELL	AGP_BUSY#
GPIO[7]	I	MAIN POWER WELL	KB_US/JP#
GPIO[8]	I	RESUME POWER WELL	EXTSMI#
GPIO[11]	I	RESUME POWER WELL	SMBALERT#
GPIO[12]	I	RESUME POWER WELL	SCI#
GPIO[13]	I	RESUME POWER WELL	WAKE_UP#
GPIO[16]	O	MAIN POWER WELL	SIDE_OFF#
GPIO[17]	O	MAIN POWER WELL	PIDE_OFF#
GPIO[18]	O	MAIN POWER WELL	STOP_PCI#
GPIO[19]	O	MAIN POWER WELL	SUSA#
GPIO[20]	O	MAIN POWER WELL	STOP_CPU#
GPIO[21]	O	MAIN POWER WELL	X
GPIO[22]	OD	MAIN POWER WELL	CPUPERF#
GPIO[23]	O	MAIN POWER WELL	X
GPIO[24]	I/O	RESUME POWER WELL	PCLKRUN#
GPIO[25]	I/O	RESUME POWER WELL	X
GPIO[27]	I/O	RESUME POWER WELL	X
GPIO[28]	I/O	RESUME POWER WELL	X
GPIO[32]	I/O	MAIN POWER WELL	WIRELESS_PD#
GPIO[33]	I/O	MAIN POWER WELL	LCDID0
GPIO[34]	I/O	MAIN POWER WELL	LCDID1
GPIO[35]	I/O	MAIN POWER WELL	LCDID2
GPIO[36]	I/O	MAIN POWER WELL	LCDID3
GPIO[37]	I/O	MAIN POWER WELL	ICH_SIDE_IN#
GPIO[38]	I/O	MAIN POWER WELL	IDERST#
GPIO[39]	I/O	MAIN POWER WELL	MINIPCI_ACT#
GPIO[40]	I/O	MAIN POWER WELL	DEBUG_EN
GPIO[41]	I/O	MAIN POWER WELL	SIDEDET
GPIO[42]	I/O	MAIN POWER WELL	SPK_OFF
GPIO[43]	I/O	MAIN POWER WELL	SIDERST#

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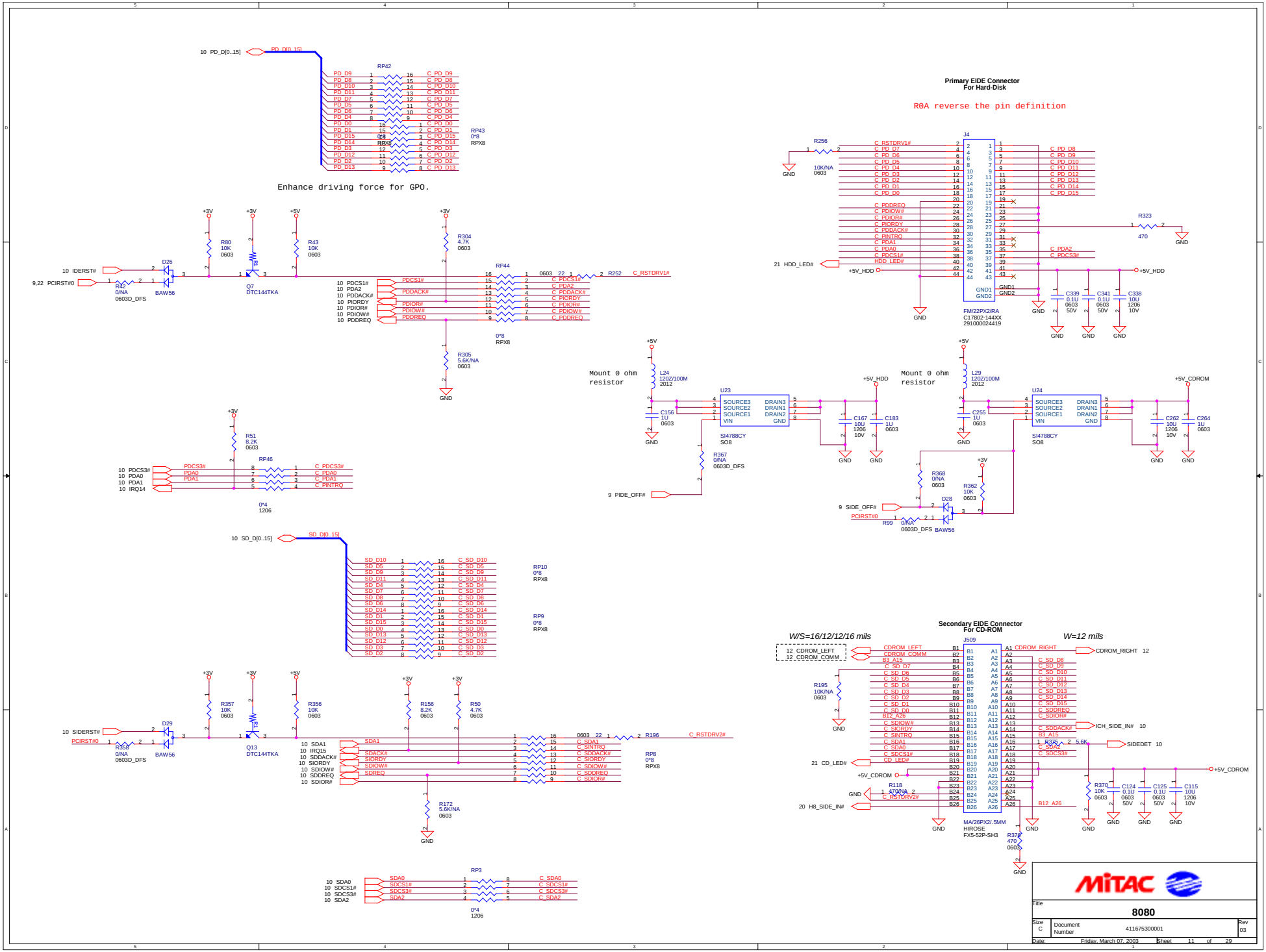

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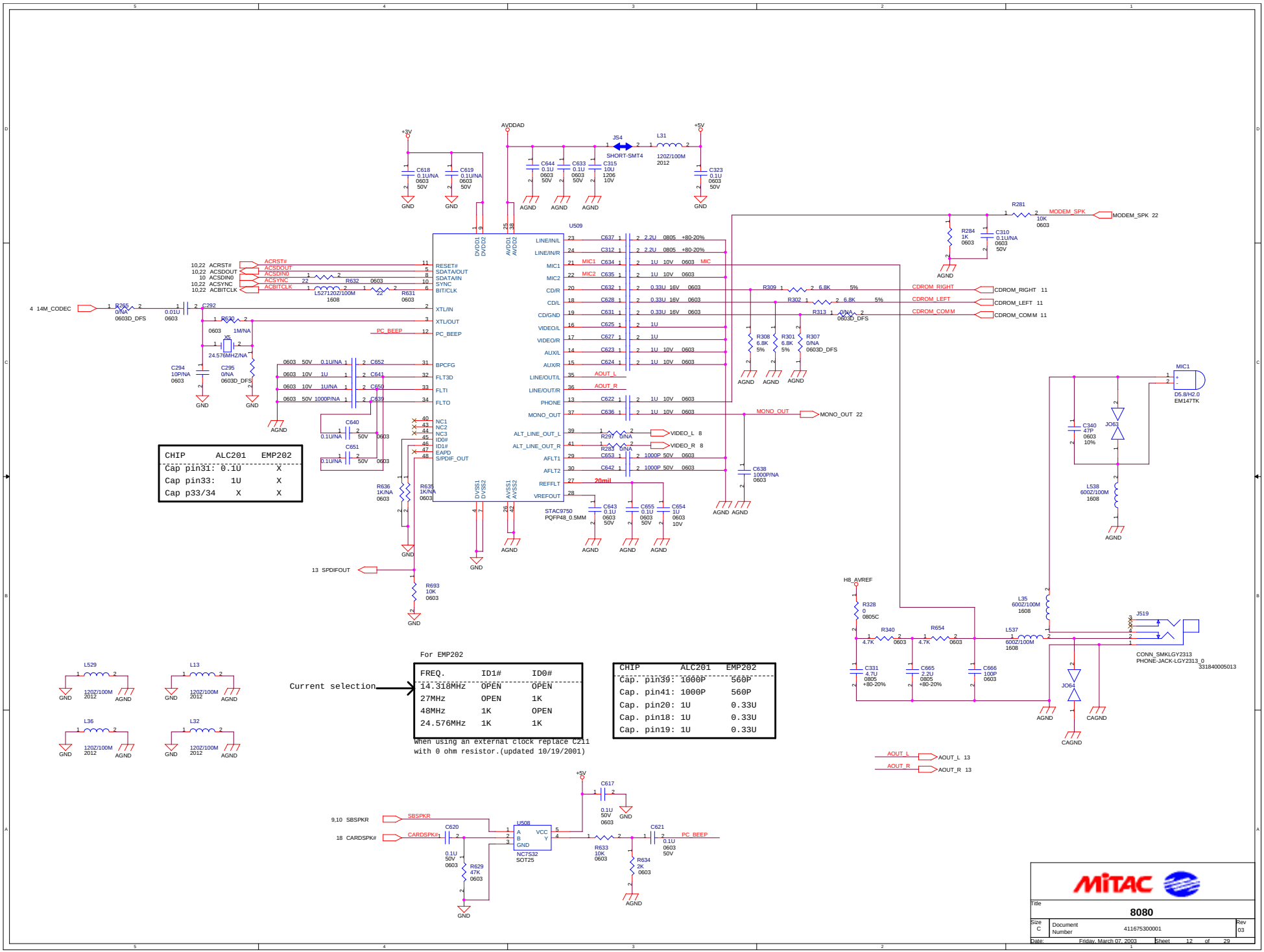

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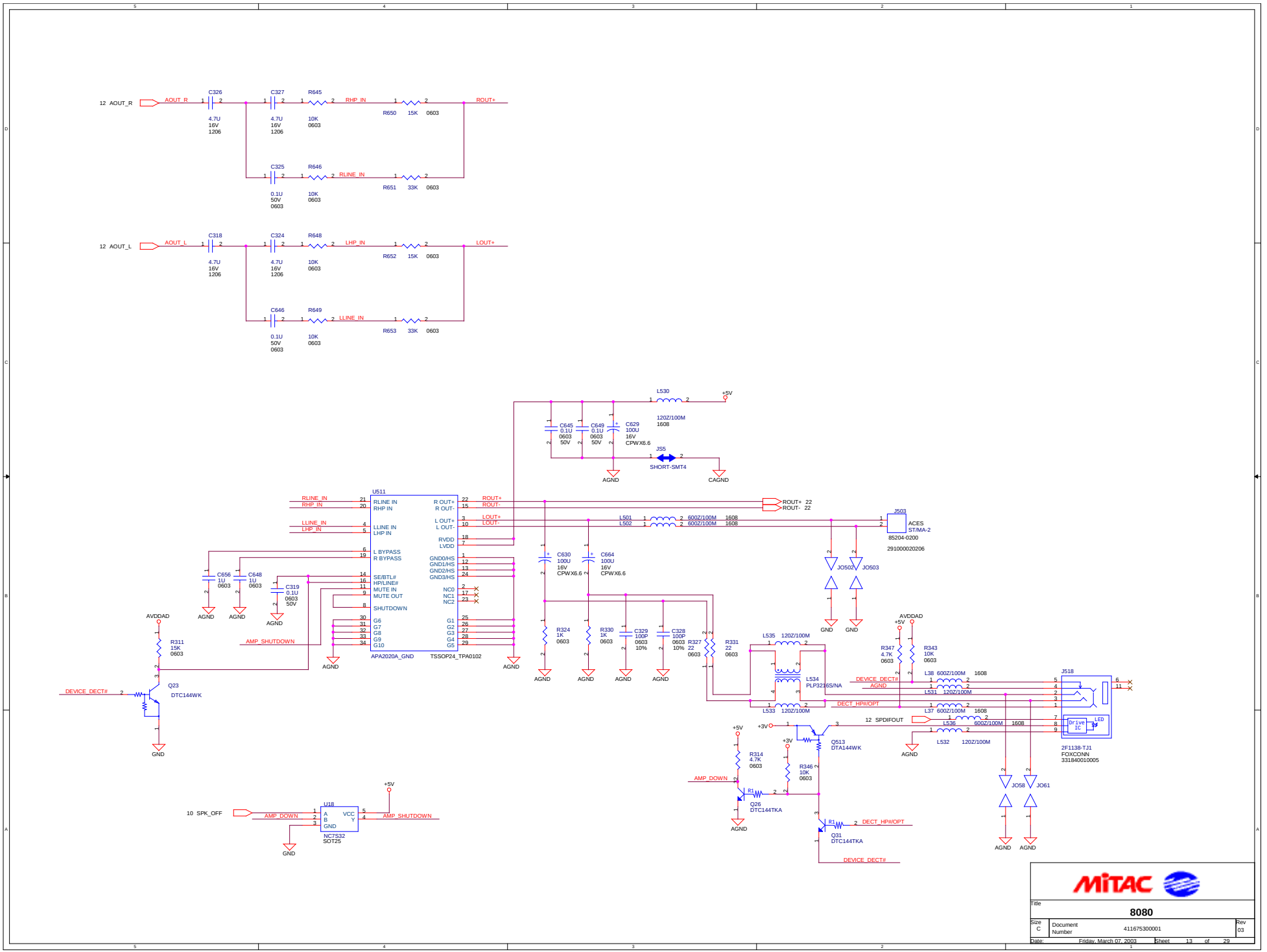

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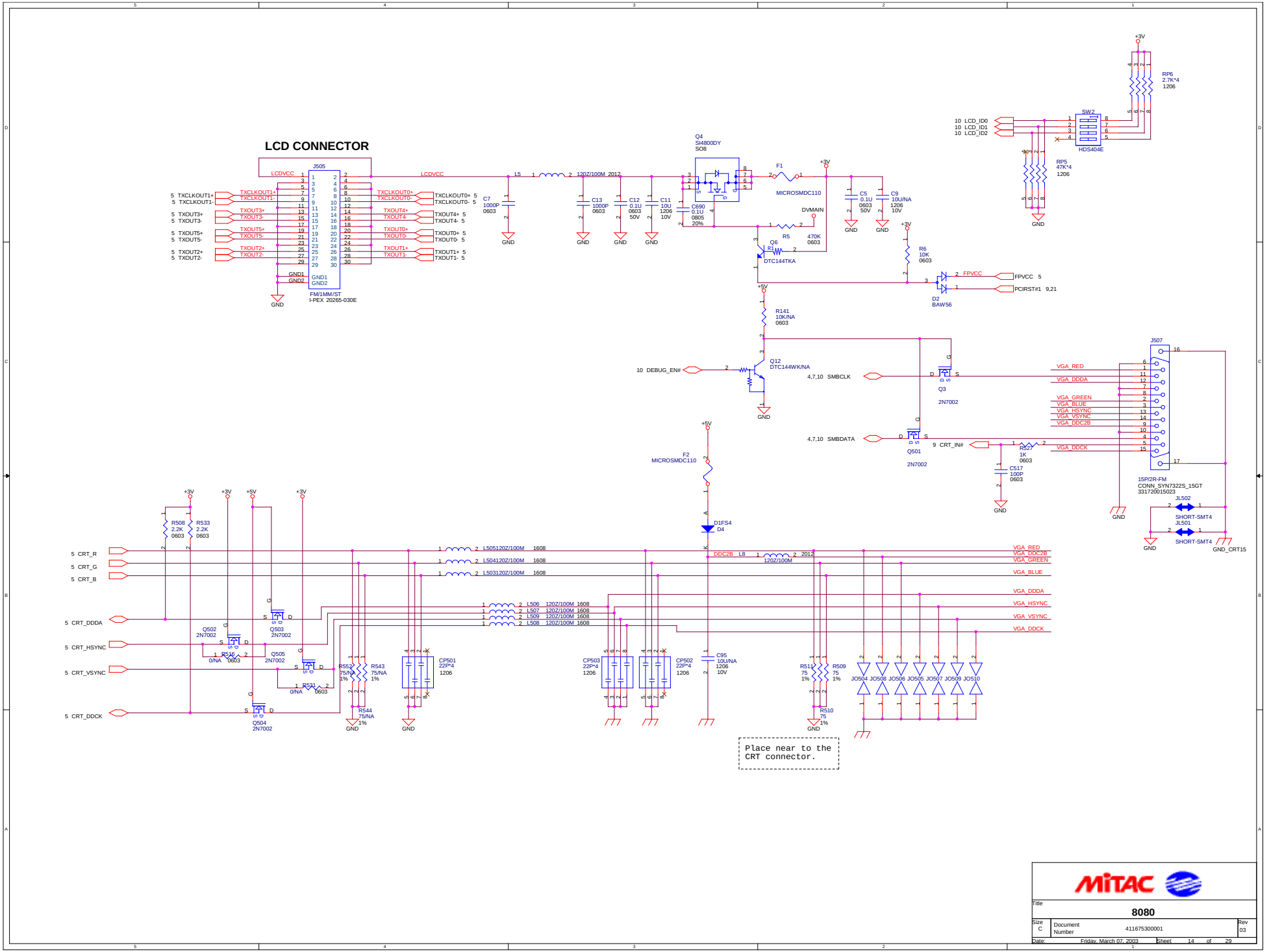

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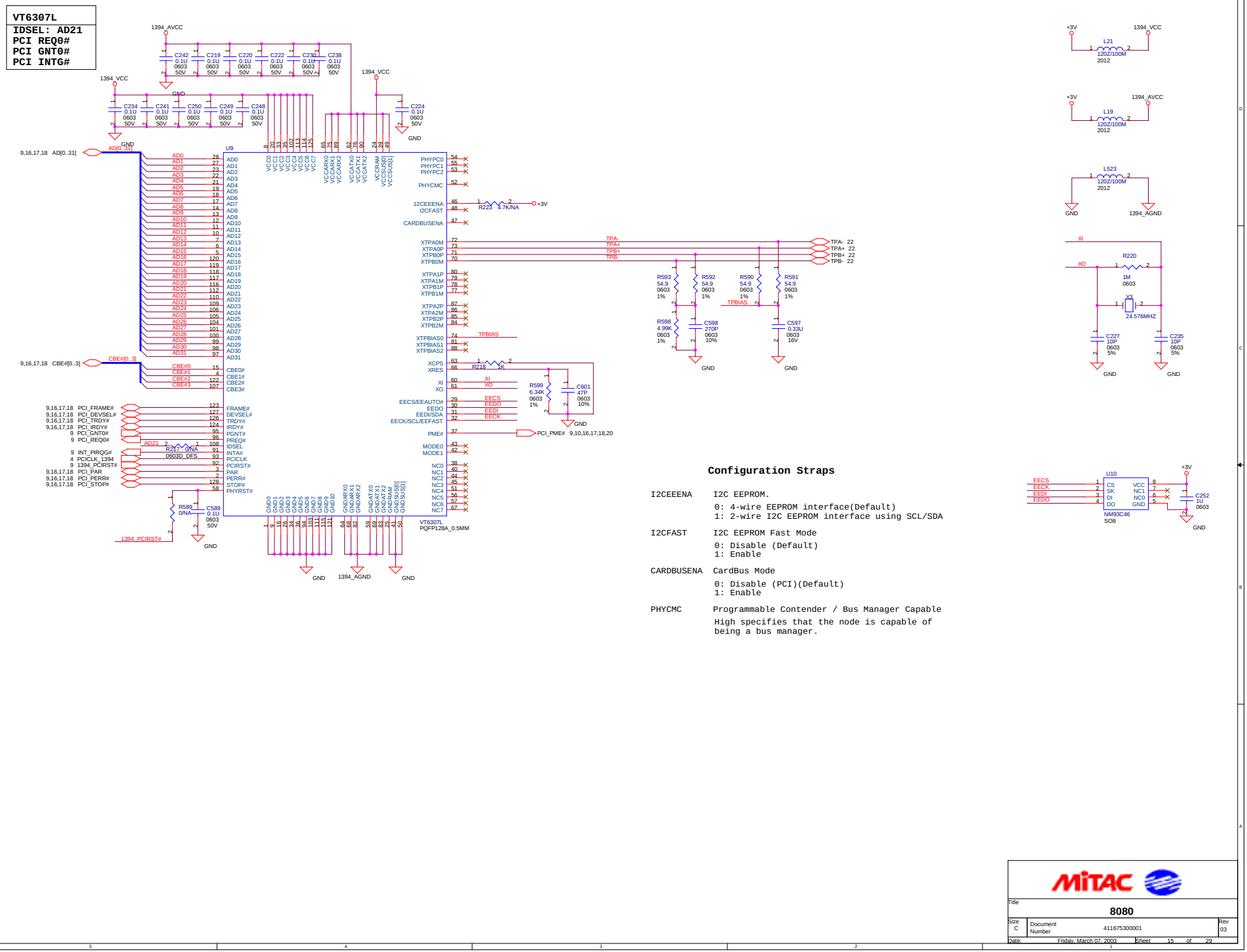

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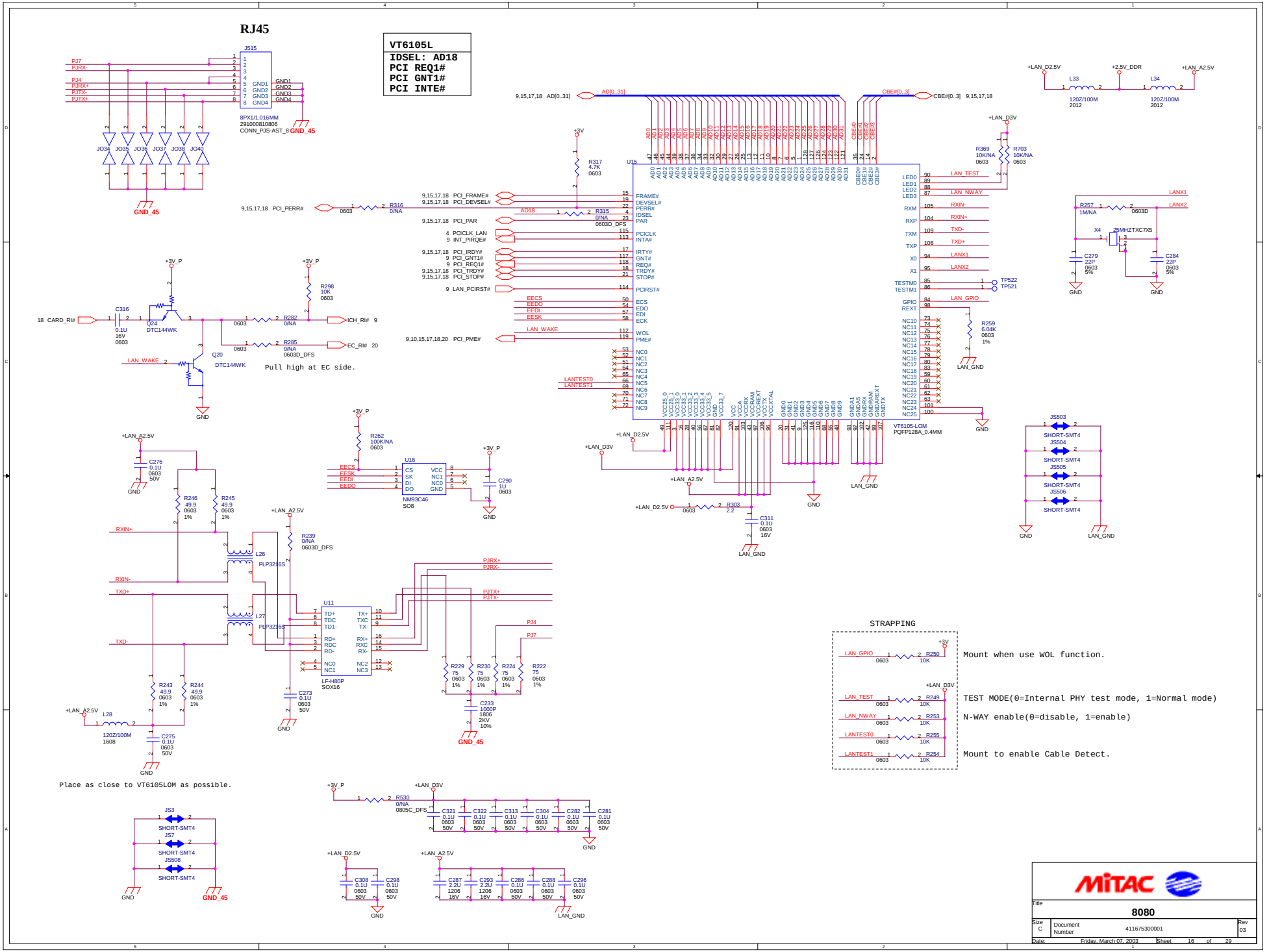

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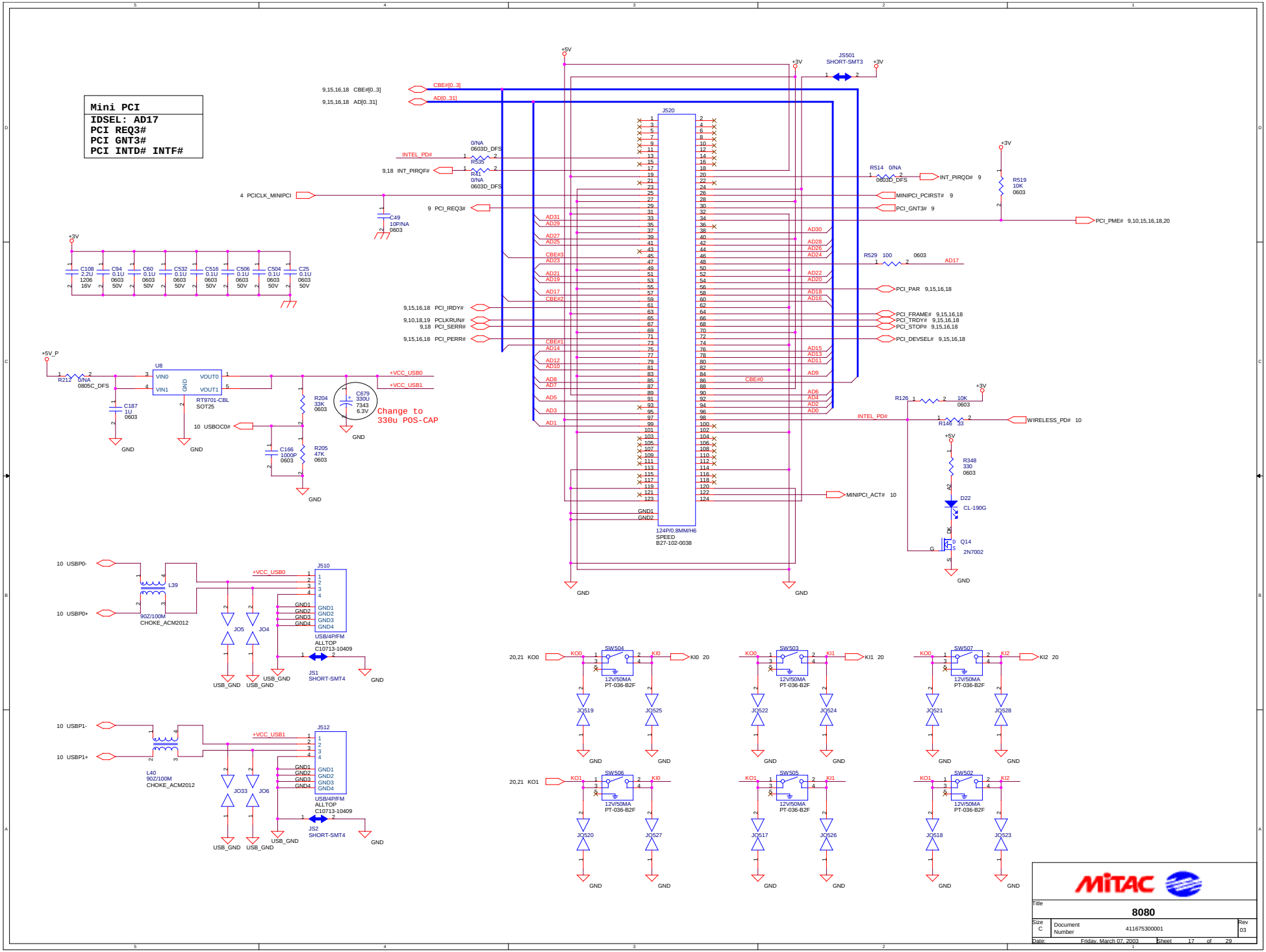

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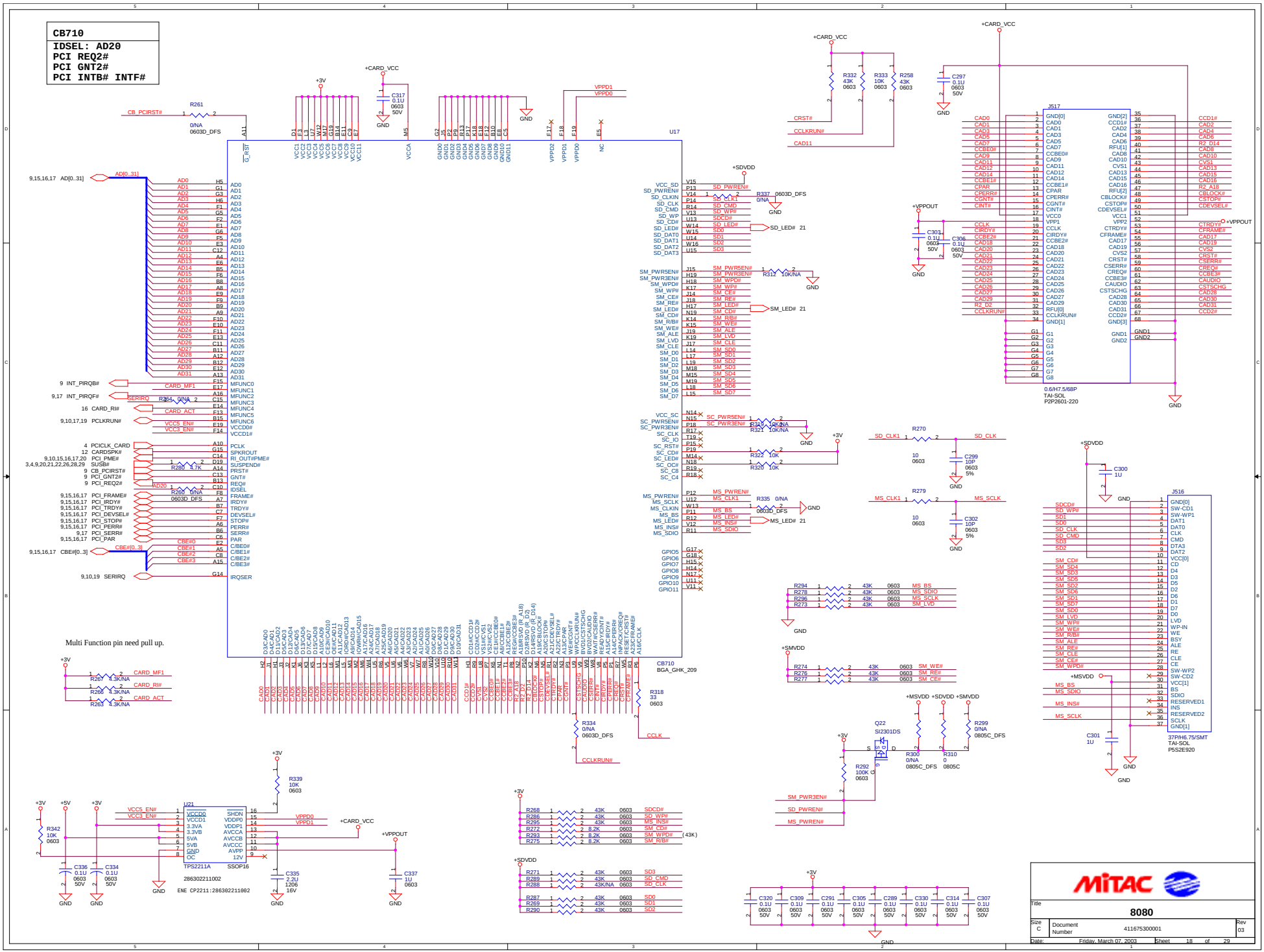

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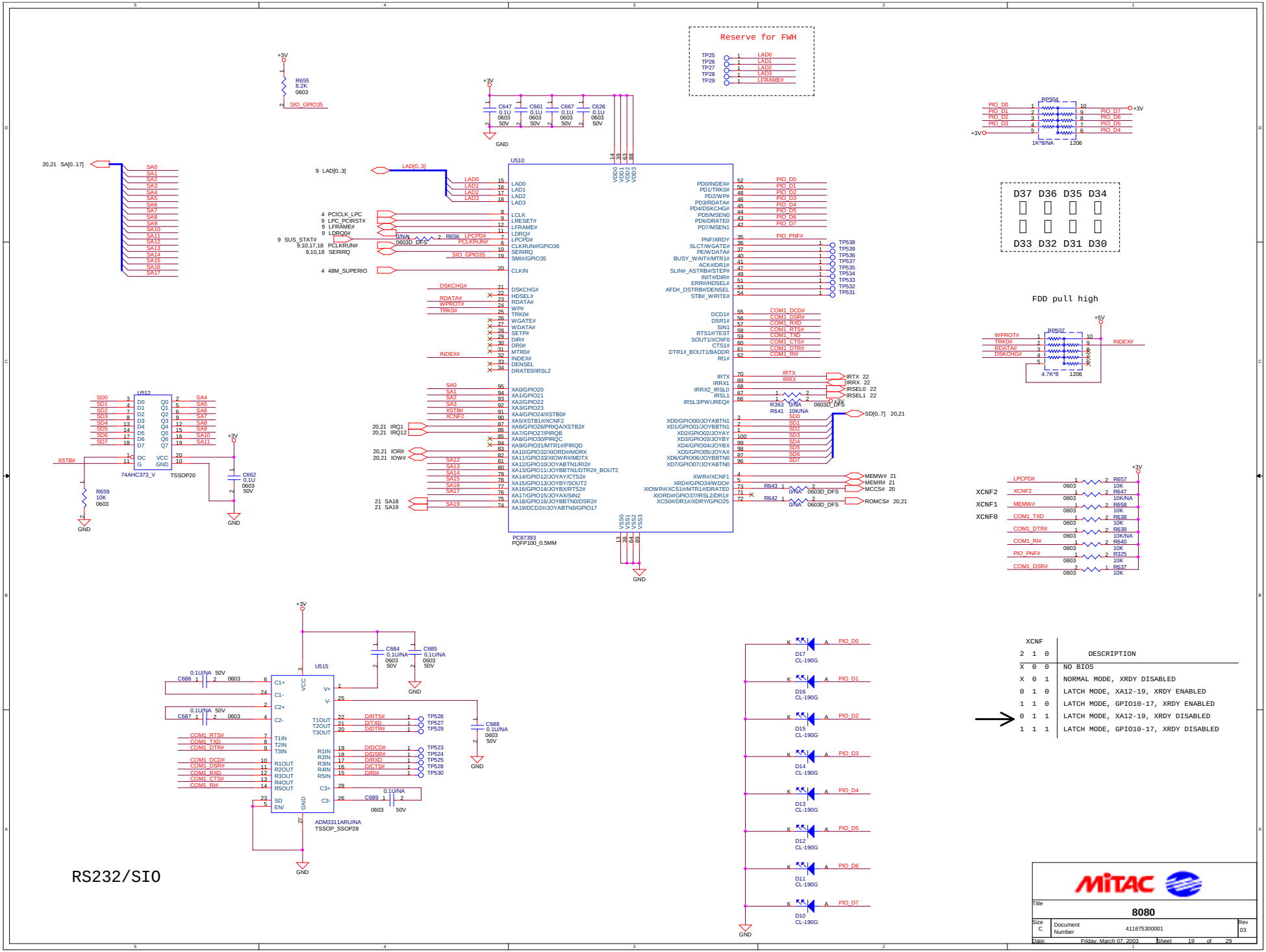

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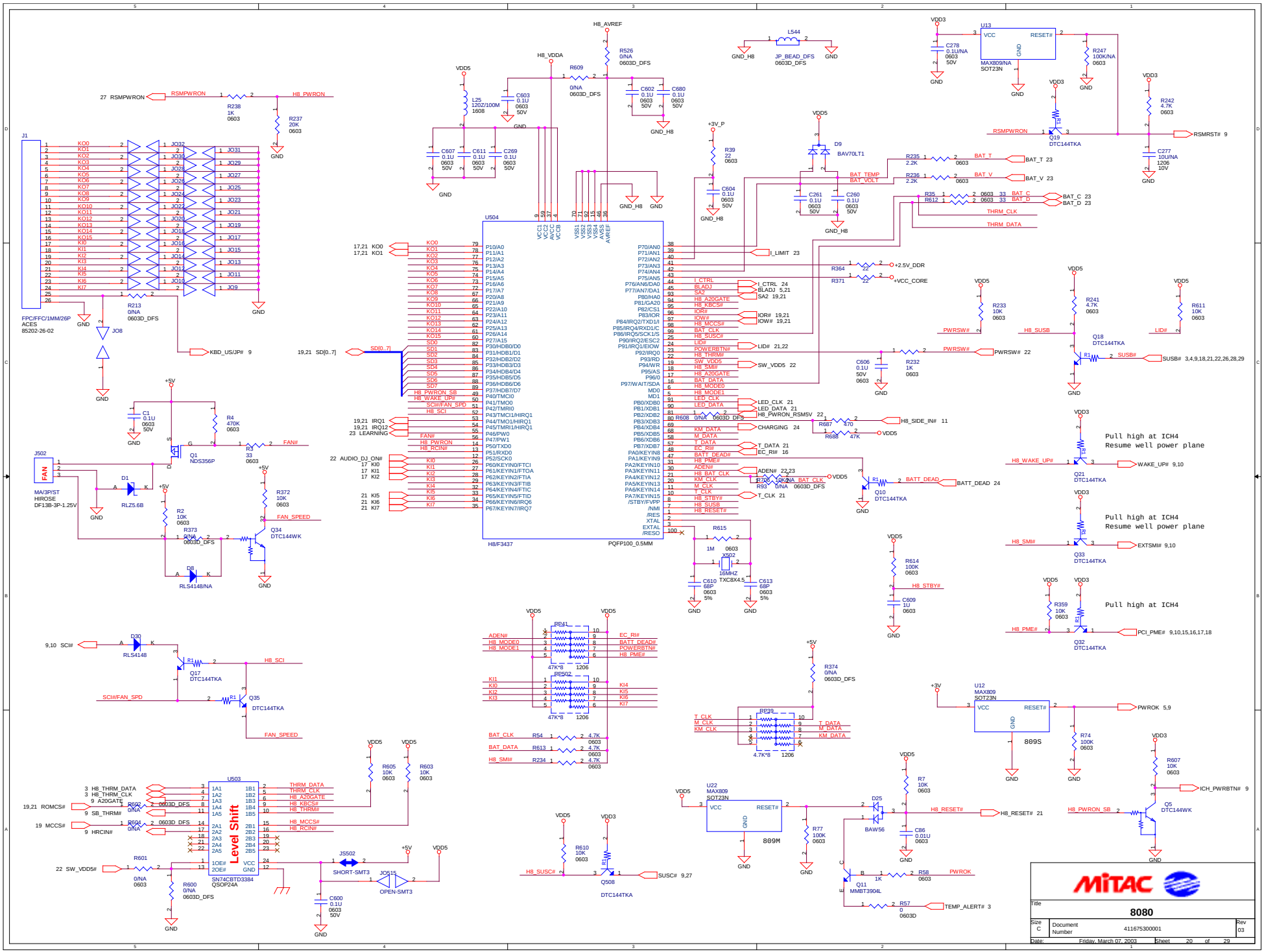

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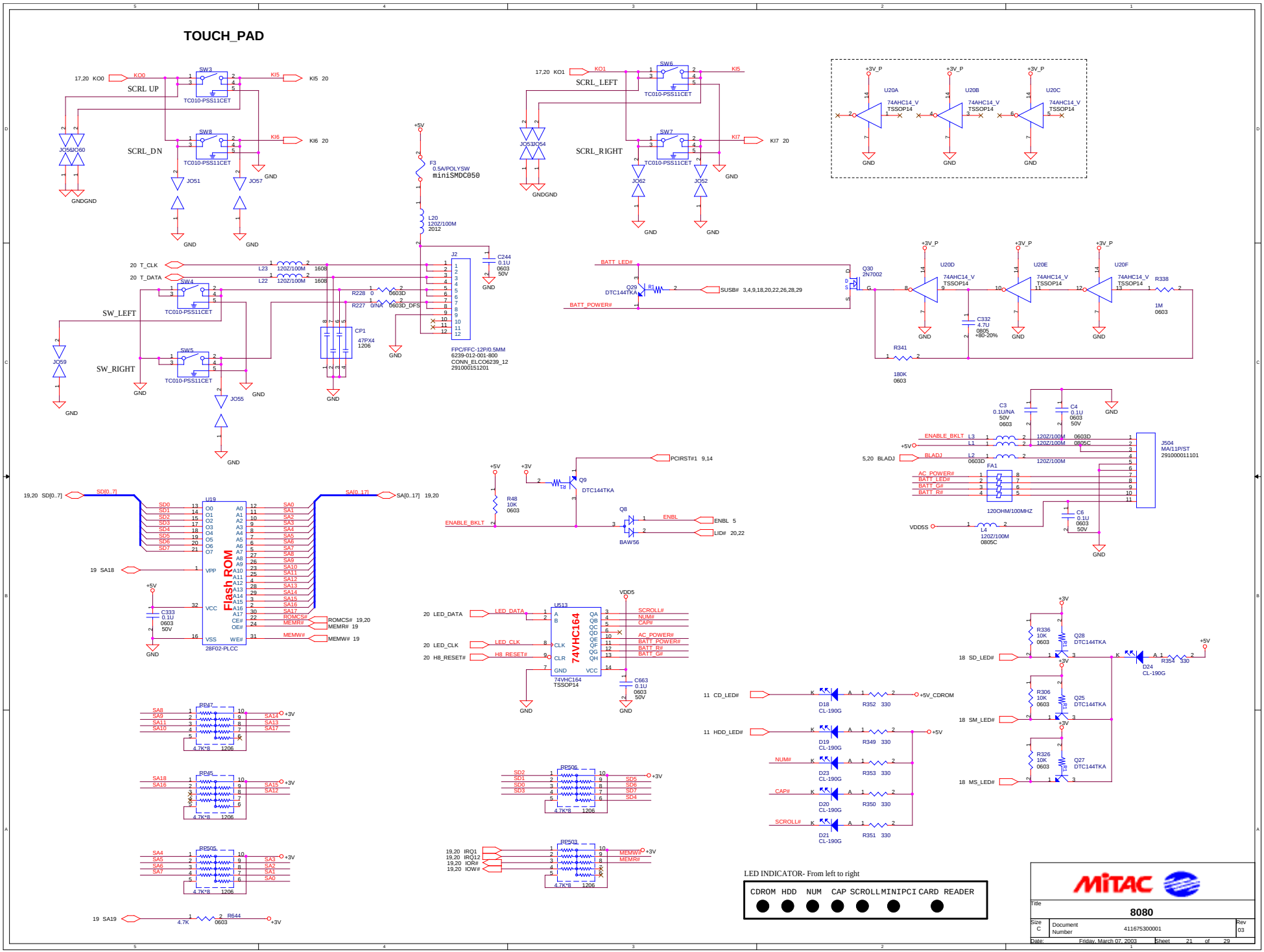

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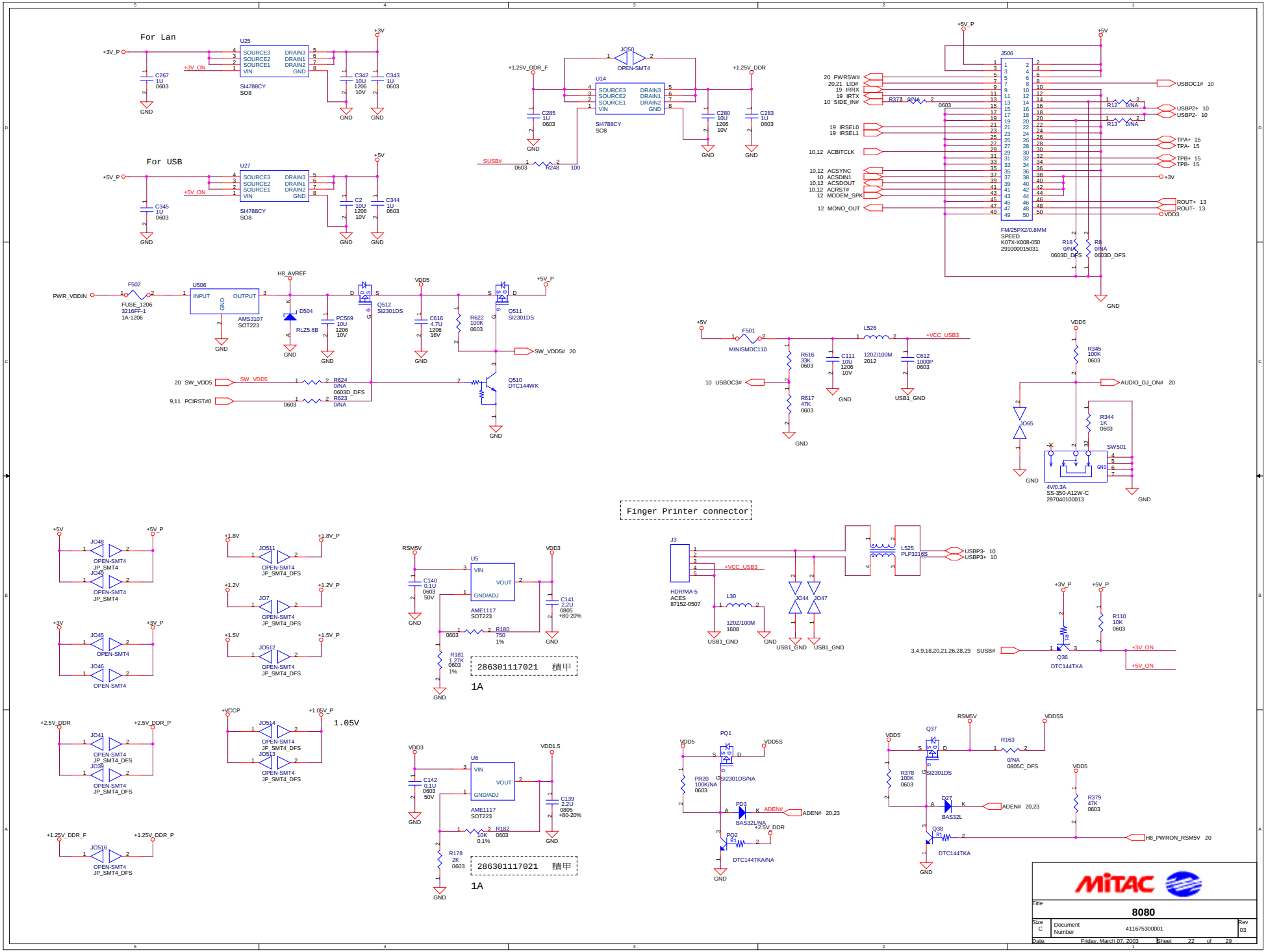

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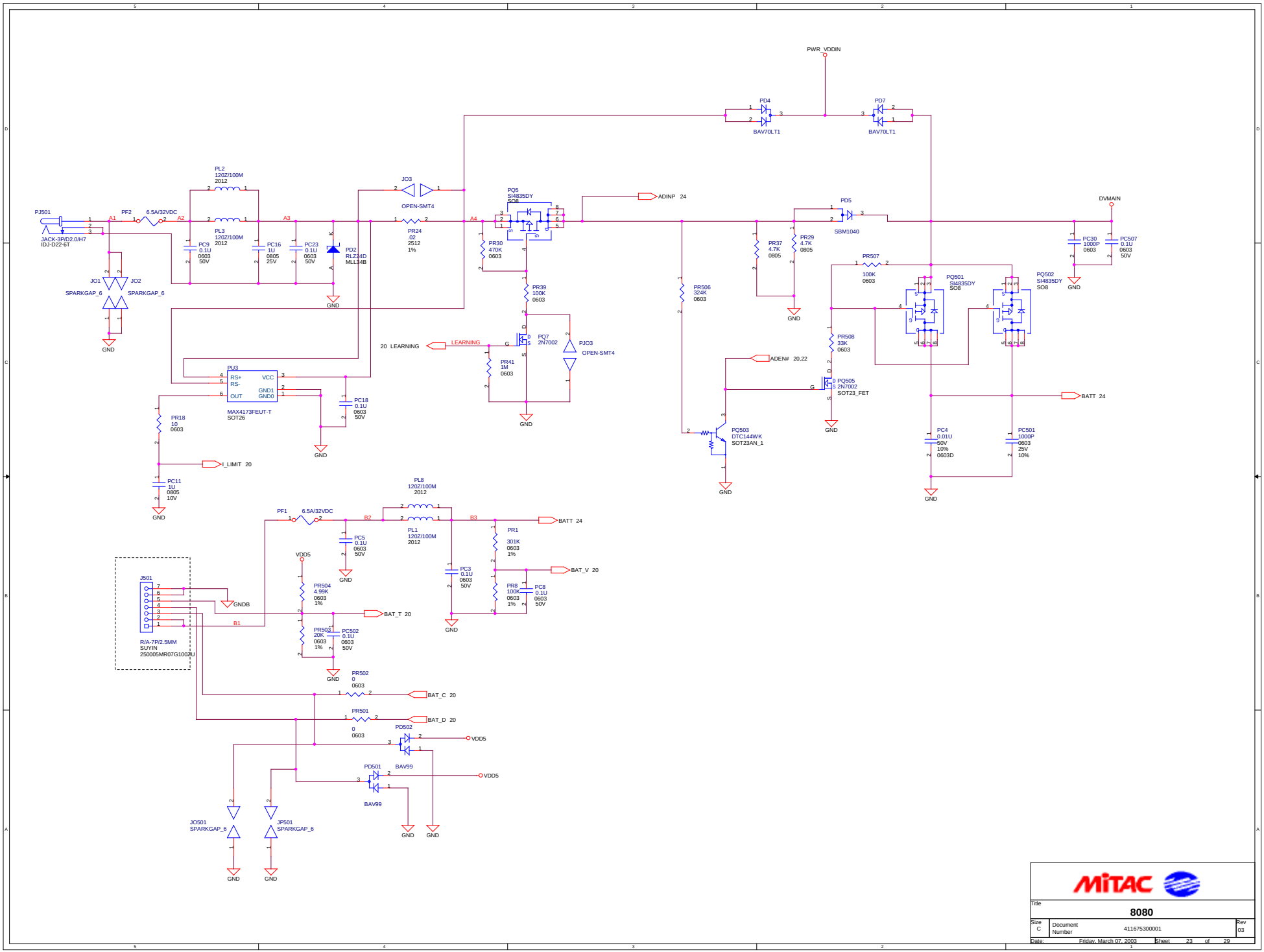

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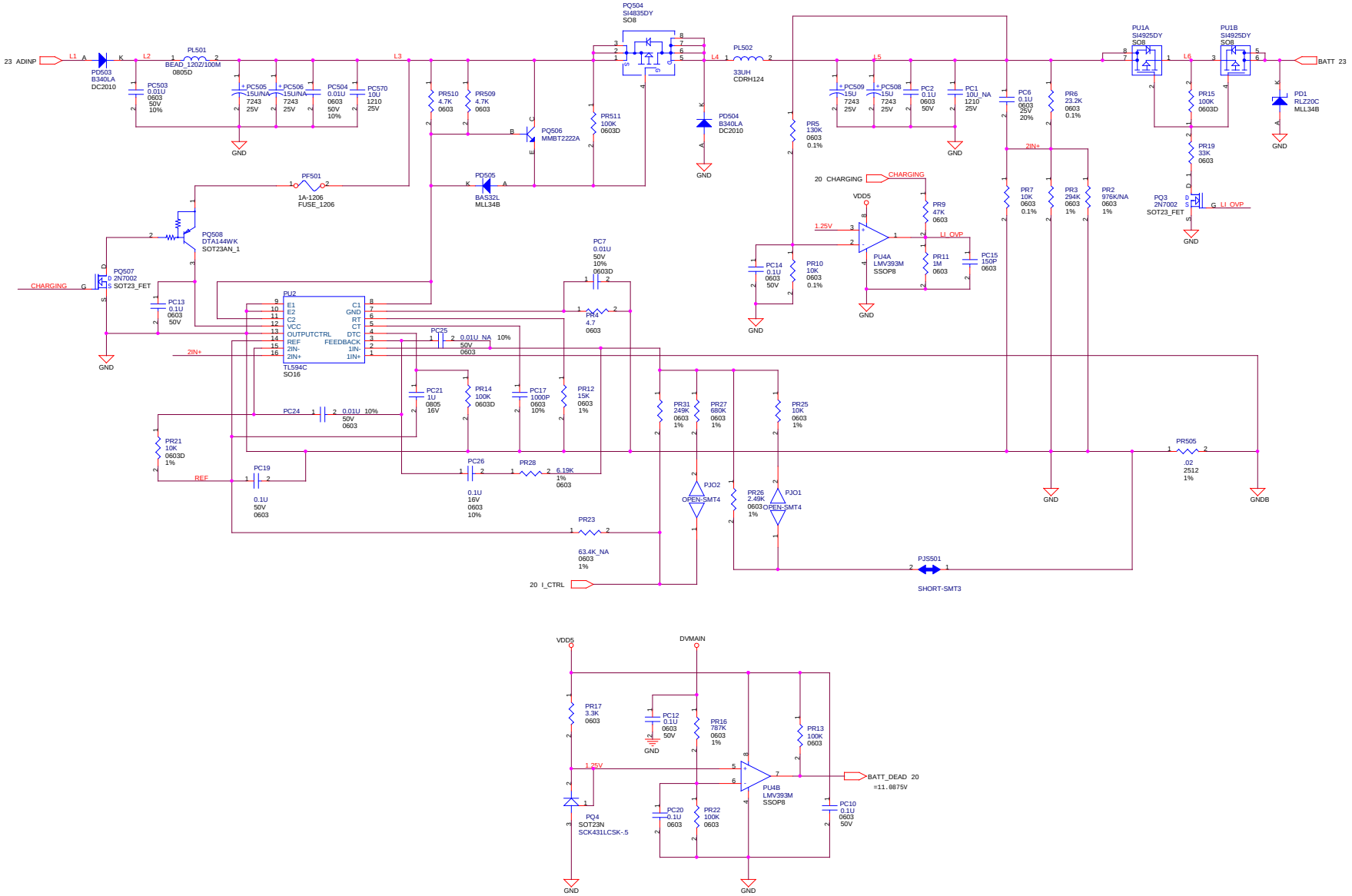

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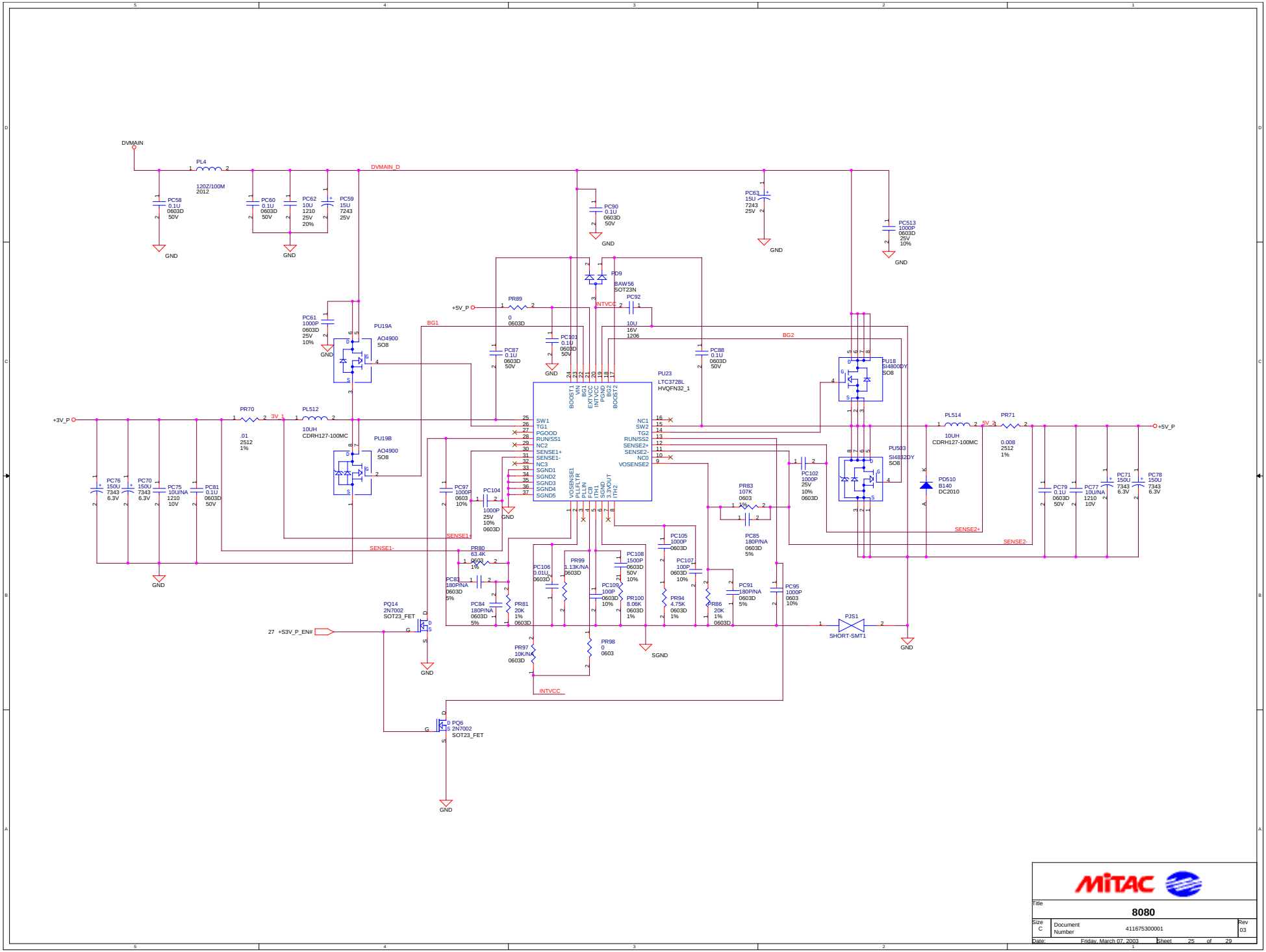

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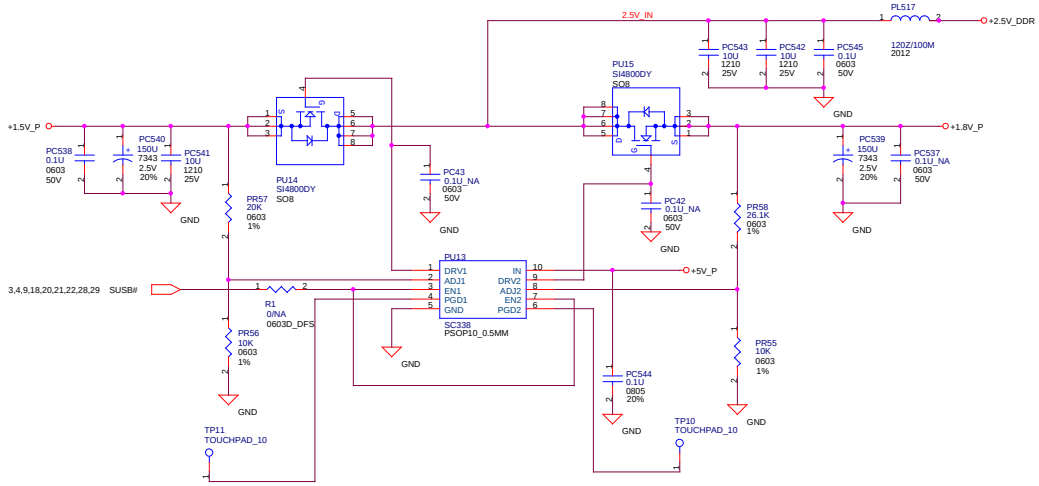

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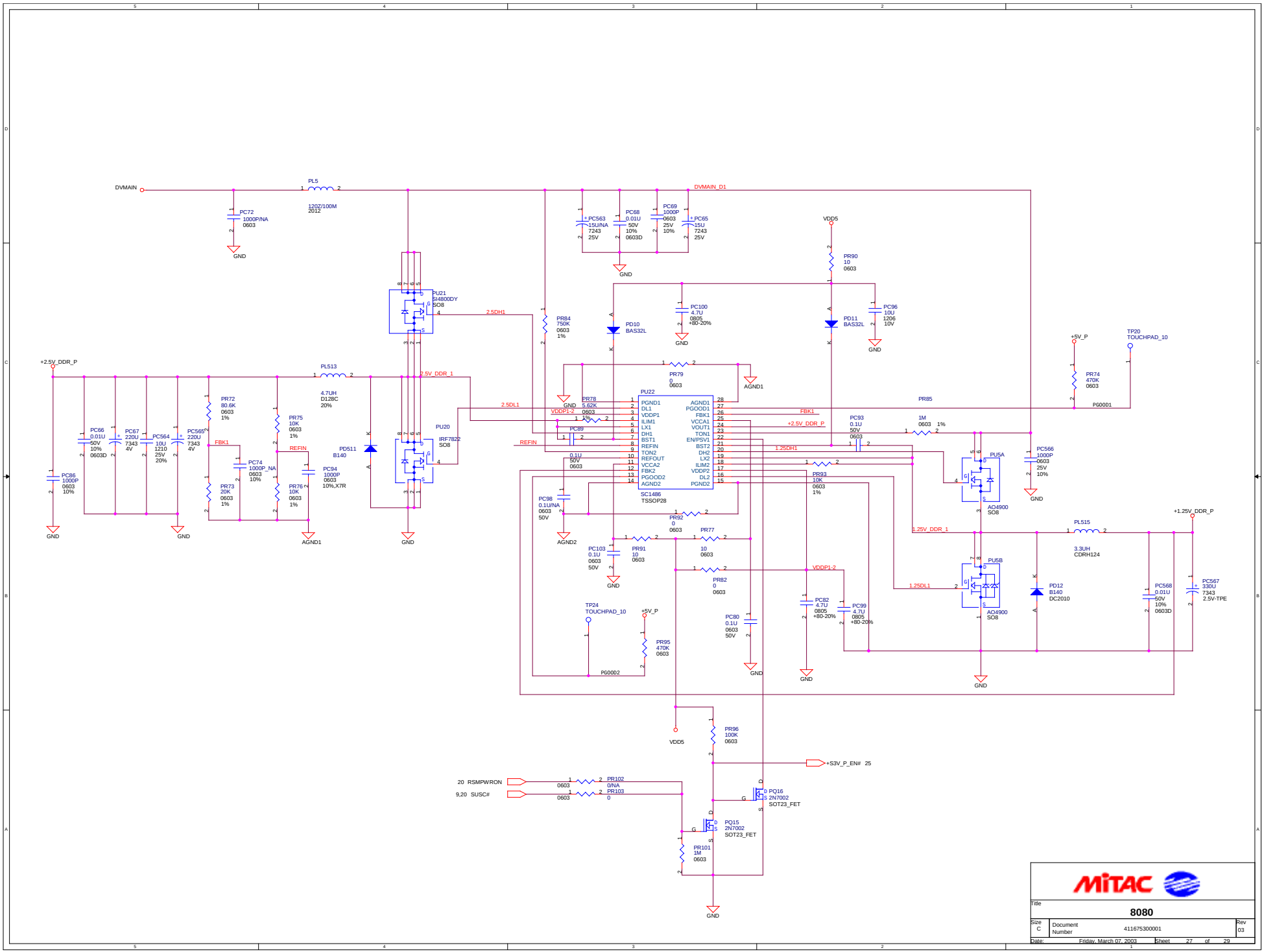

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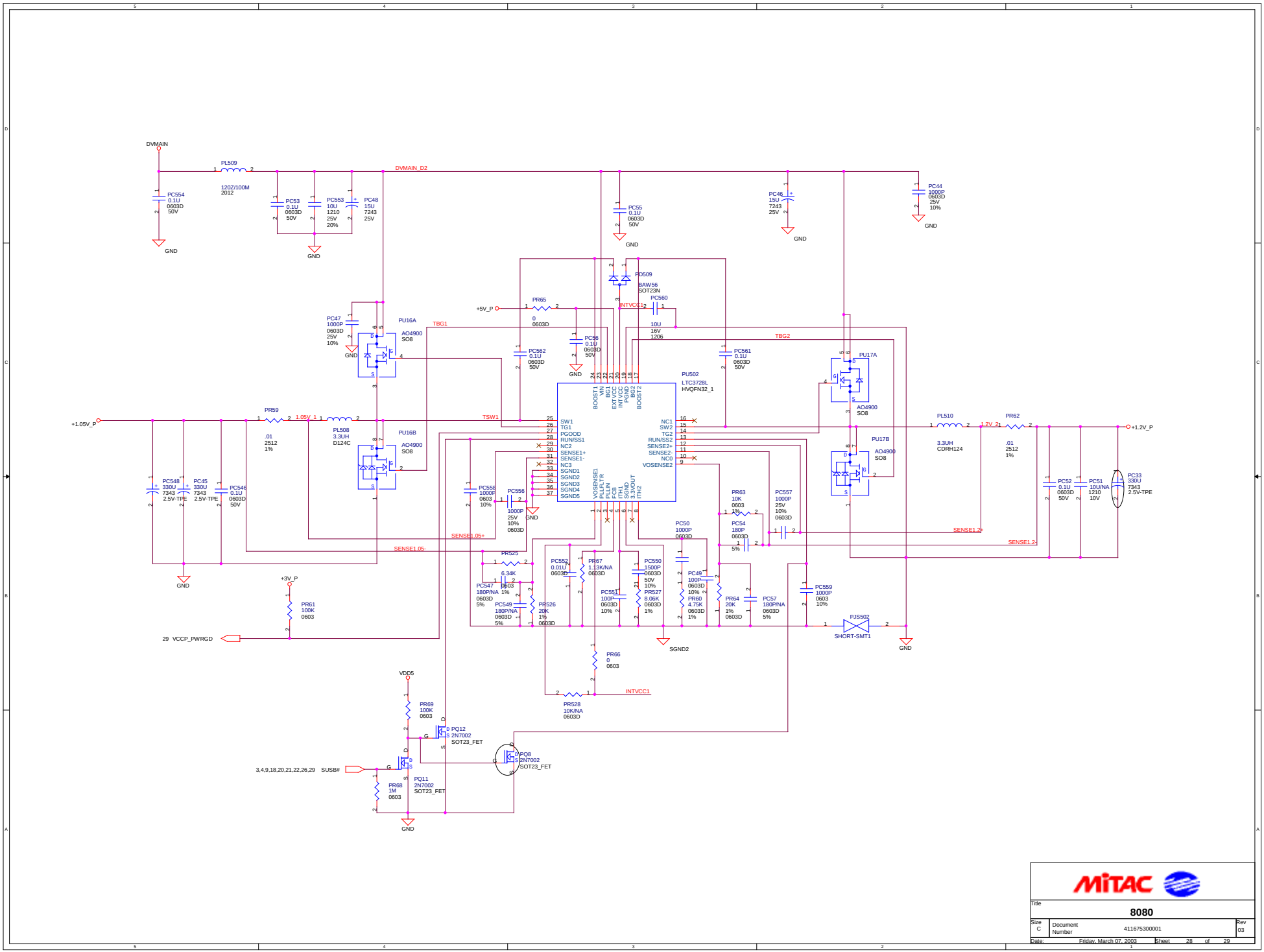

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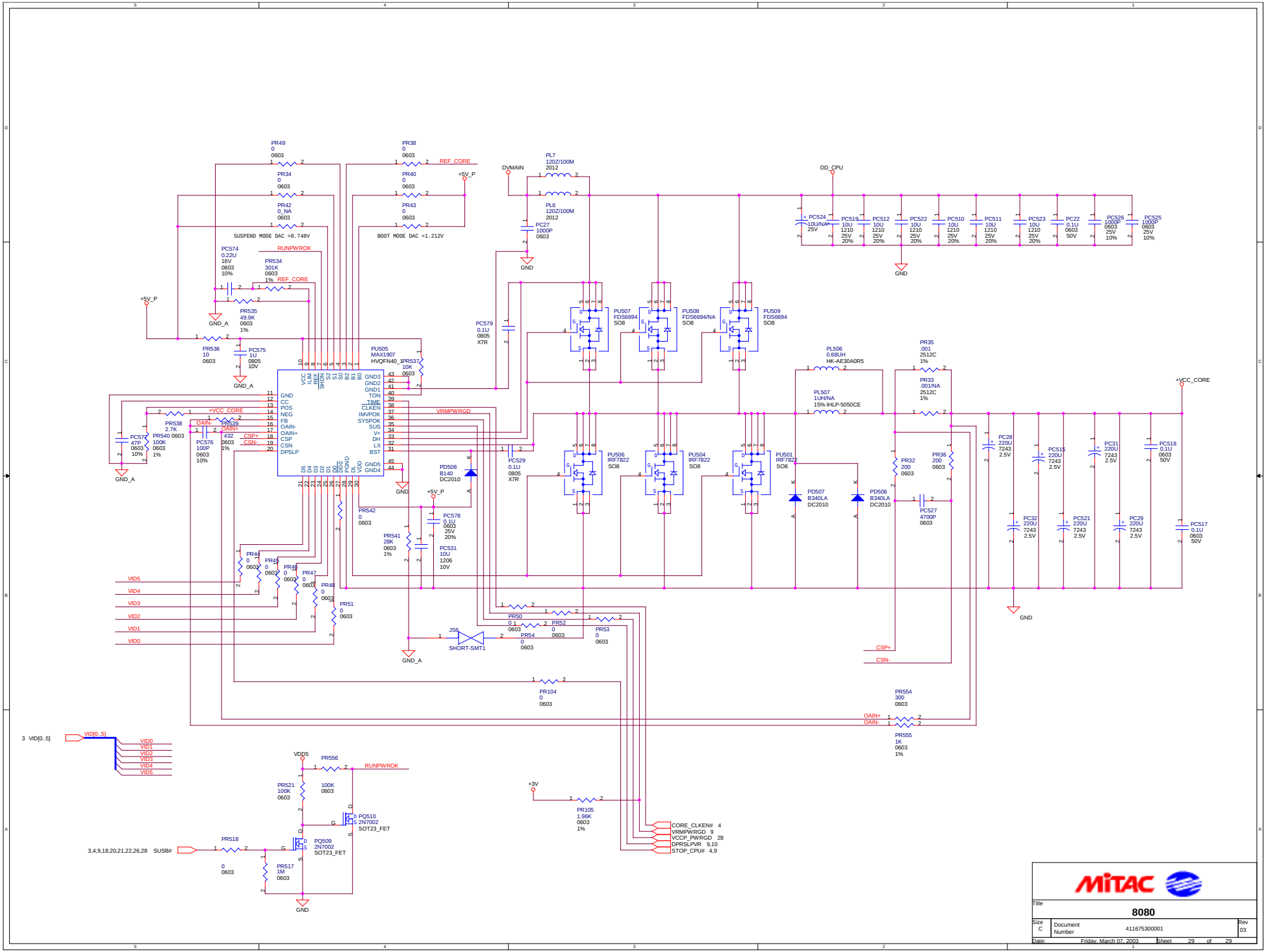

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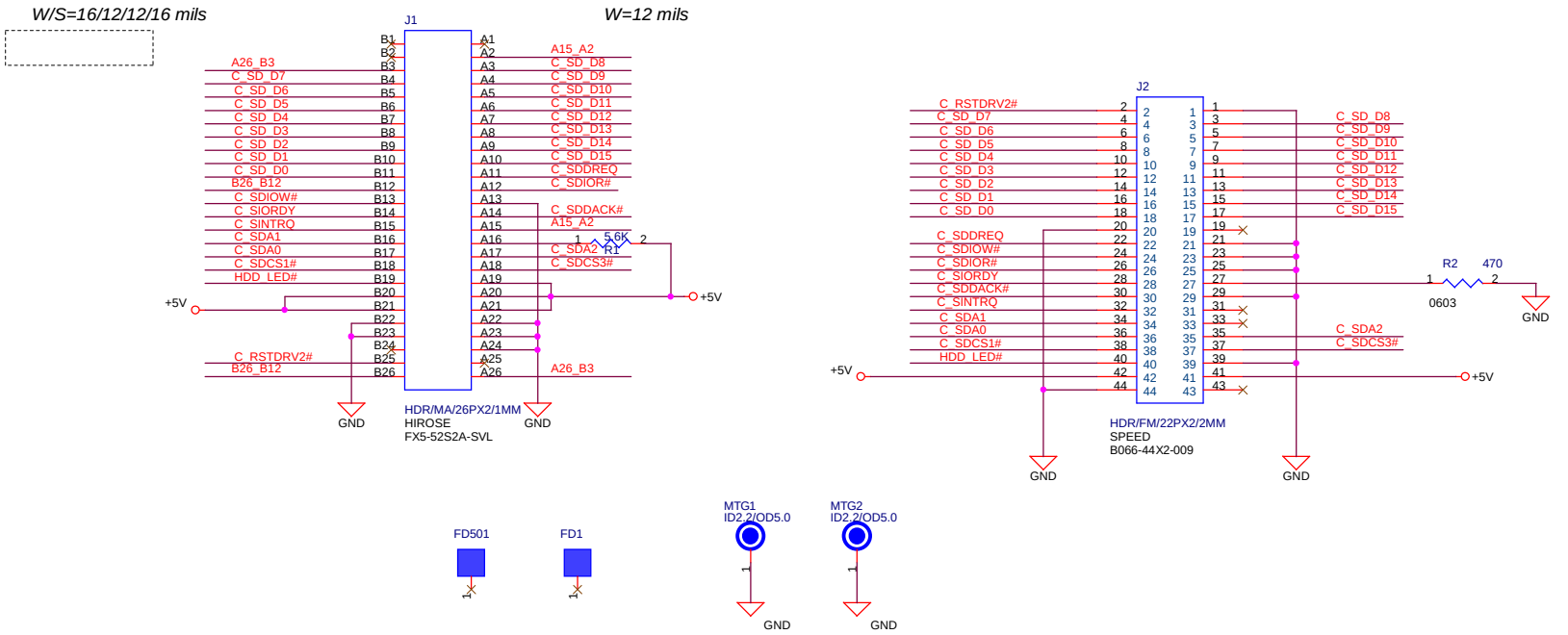

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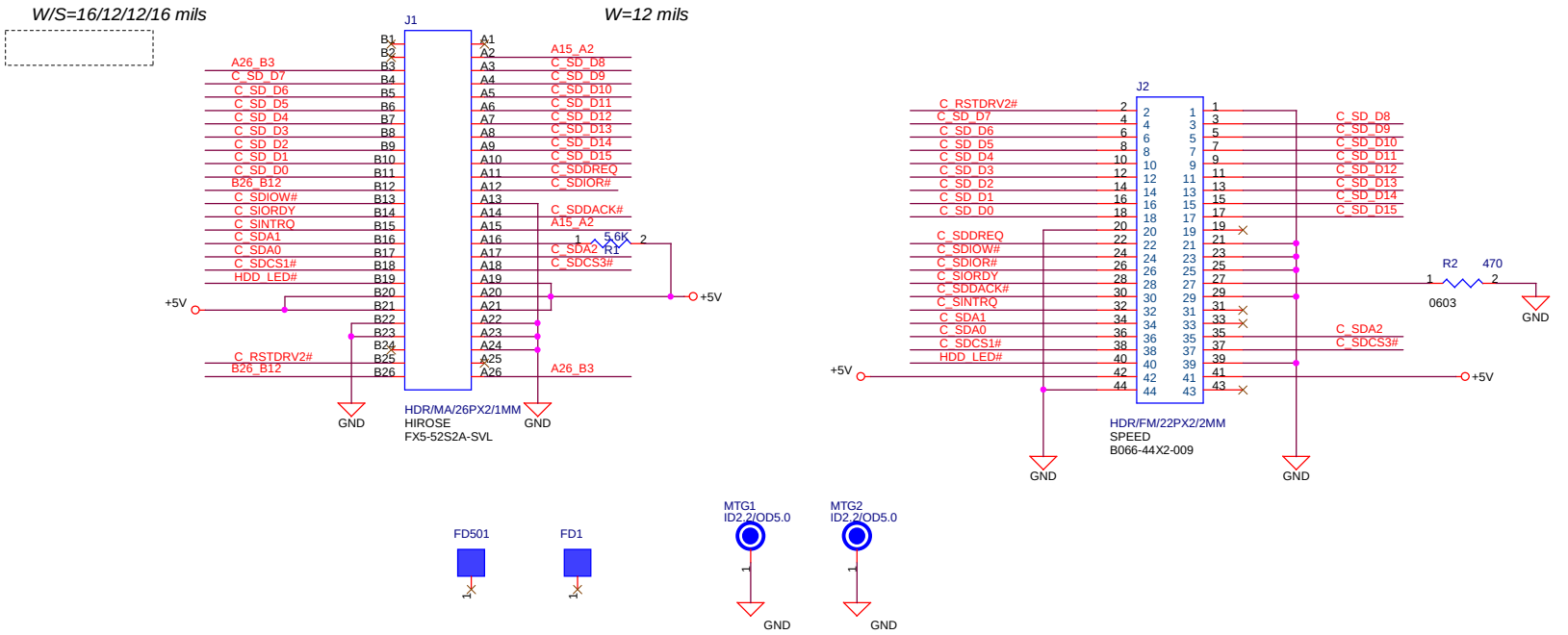

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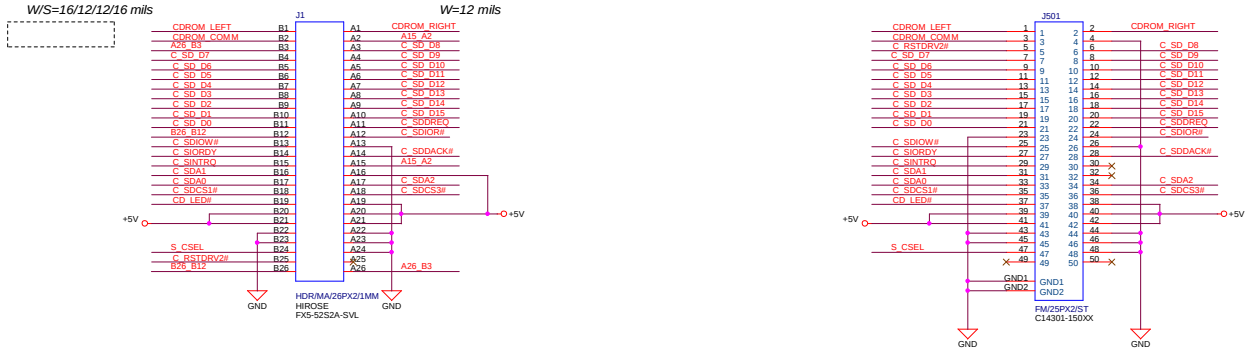

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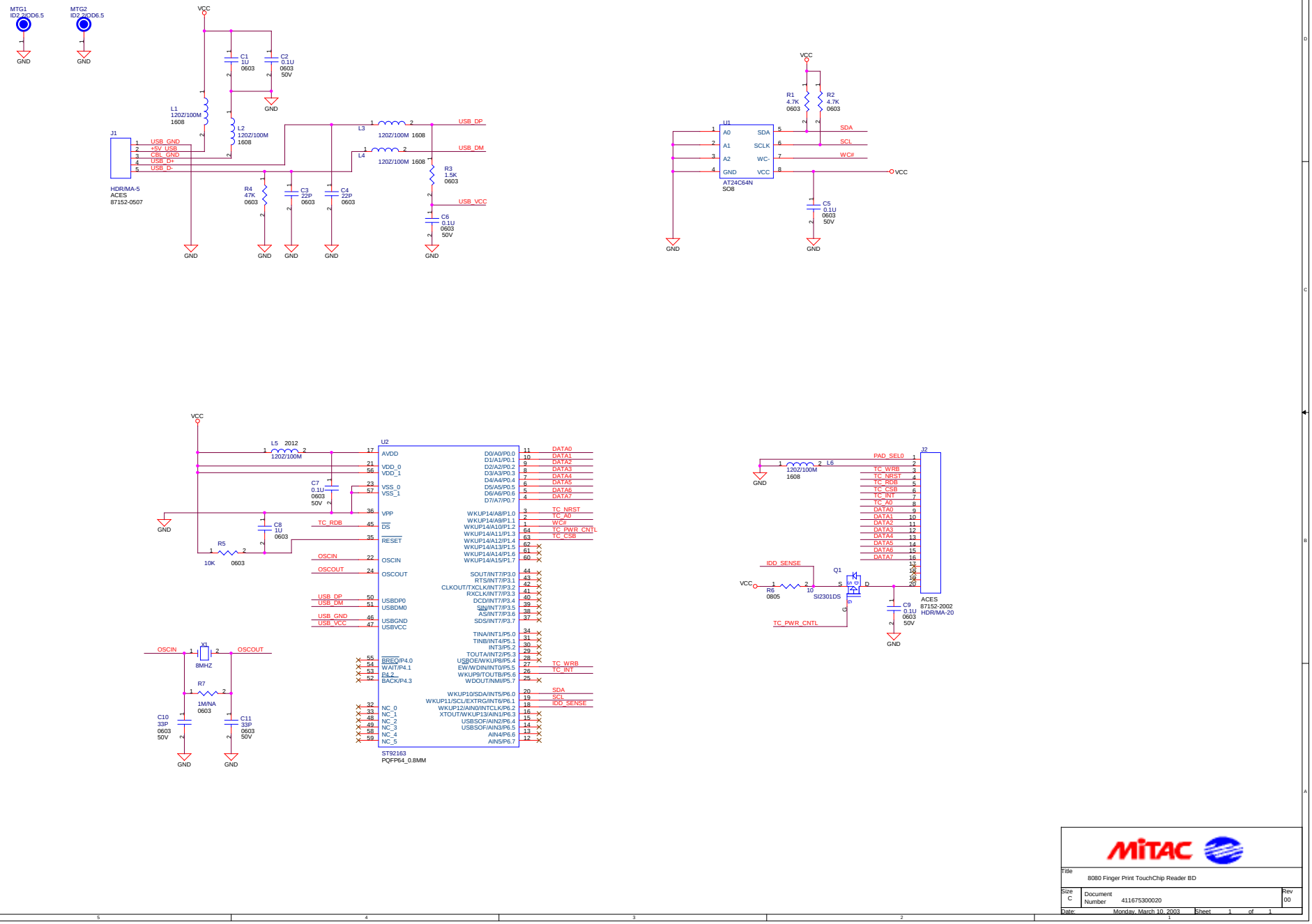

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❖ Intel 82801DBM I/O Controller Hub Mobile (ICH4-M)	Intel, INC
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