SERVICE MANUAL & TROUBLESHOOTING GUIDE FOR

7521

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MiTAC

7521 N/B MAINTENANCE

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1.1 HARDWARE ENGINEERING SPECIFICATION

1.1.1 General Description

This document describes the engineering specification for 7521 portable notebook computer system.

1.1.2 System Overview

The 7521 model motherboard will accept Intel Pentium III and Celeron processor with FC-PGA packaged. Which will supports the different levels of Pentium III CPU with FC-PGA package. Those are Pentium III 600/650/700/750/800 MHz, and Celeron 600/633/667/700/733 MHz .

This system is based on PCI architecture and is fully compatible with IBM PC/AT specification, which have standard hardware peripheral interface and support Intel Pentium III with FC-PGA package. The power management complies with Advanced Configuration and Power Interface (ACPI) 1.0. It also provides easy configuration through CMOS setup, which is built in system BIOS software and can be pop-up by pressing F2 at system start up or warm reset. System also provides icon LEDs to display system status, such as AC Power indicator, FDD, HDD, NUM LOCK, CAP LOCK, SCROLL LOCK, SUSPEND MODE and battery present, capacity & charging status. It also equipped with LAN, FIR, USB port, 3D stereo audio functions.

The memory subsystem supports 64MB on board SDRAM, one 144pin DIMM socket for upgrading up to 192 MB of DRAM using SDRAM DIMM module.

The SiS 630 integrates the north bridge chip, super south bridge and the real 128-bit 3D graphics accelerator all into one single chip. It provides 10/100M Fast Ethernet, 3D Positional Audio, Advance H/W DVD playback and 2D/3D graphics engine.

The TI 1225 cardbus controller supports PCMCIA and CARDBUS. The National Semiconductor PC97338 Super I/O controller integrates the standard PC I/O functions: floppy interface, two FIFO serial ports, one EPP/ECP capable parallel port, and support for an IrDA 1.1, 1.0 and sharp ASK compatible infrared interface. To provide for the increasing number of multimedia applications, an CODEC CS4299 is integrated onto the motherboard which support 16-bit stereo, Sound Blaster Pro, Windows Sound System compatibility, and full-duplex capabilities to meet the demands of interactive multimedia applications

A full set of software drivers and utilities are available to allow advanced operating systems such as Windows 95 or Windows 98 to take full advantage of the hardware capabilities. Features such as bus mastering IDE, Windows 95-ready Plug and Play, Advanced Power Management (APM) with application restart, software-controlled power shutdown..

1.2 Hardware System

1.2.1 System parts

- Central Processing Unite : using Intel Pentium Ⅲ or Celeron microprocessors in FC-PGA packaged.
- Synthesizer : ICS9248-102.
- SiS 630 : CPU/ PCI and CPU/AGP bridge with memory controller/LAN/IDE/USB/PMU controller.
- Super I/O Controller : NS PC 97338VJG.
- PCMCIA Interface Controller : TI 1225.
- Keyboard System : Hitachi H8 (3434F) universal keyboard controller.
- 3D Audio System : CRYSTAL CS 4299 CODEC.
- FIR port : HP HSDL-3600#007 FIR module.
- FAX/ MODEM : ASKEY 56Kbps Fax MODEM, software Modem (Option) .

1.2.2 CPU MODULE

- Intel Pentium Ⅲ/ Celeron Processors with 370 pins PGA package.
- Pentium Ⅲ 600/650/700/750/800 MHz, FC-PGA package at FSB 100MHz.
- Celeron 600/ 633/ 667/ 700/ 733 MHz, FC-PGA package.

1.2.3 Synthesizer

- System frequency synthesizer : ICS9248-102
  - Maximized EMI suppression using Integrate Circuit System's spread spectrum technology.
  - Three copies of CPU output, output to output skew between them within 175ps and seven copies of PCI output, output to output skew between them 500ps, fourteen copies of SDRAM output, output to output skew between them within 250ps.
  - One 48MHz outout for USB and selectable 24/48 MHz output (pin25).
  - Two buffer copies of 14.318MHz input reference signal.
  - Supports up to 166MHz CPU or SDRAM operation.
  - Supports two SDRAM DIMMS.
  - Ideal for high performance Desktop/ Notebook designed using SIS630 chip set.
  - I^2C serial configuration interface.

1.2.4 SiS630 Slot 1/Socket 370 2D/3D Ultra-AGP™ Single Chipset

The single chipset SiS630, provide a high performance/ low cost Desktop soloution for the Intel Slot 1 and socket 370 series CPUs based system by integrated a high performance North Bridge, advanced hardware 2D/3D GUI engine and Super-South bridge. In addition. SiS630 provides system-on-chip solution that complies with Easy PC Initiative which supports instantly Available OnNow PC technology, USB, Legacy Removal and Slotless Design and FlexATX form factor.

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By integrating the UltraAGP™ technology and advanced 128-bit graphic display interface, SiS630 delivers AGP 4x-like performance and up to 2 GB/s memory bandwidth. Furthermore, SiS630 provides powerful hardware decoding DVD accelerator to improve the DVD playback performance. In addition to providing the standard interface for CRT monitors, SiS630 also

provides the Digital Flat Panel Port (DFP) for a standard interface between a personal computer and a digital flat panel monitor. To extend functionality and flexibility, SiS also provides the ?Video Bridge?(SiS301) to support the NTSC/PAL Video Output, Digital LCD Monitor and Secondary CRT Monitor, which reduces the external Panel Link transmitter and TV-Out encoder

for cost effected solution. SiS630 also adopts Share System Memory Architecture which can flexibly utilize the frame buffer size up to 64MB.

The “Super-South Bridge” in SiS630 integrates peripheral controllers / accelerators / interfaces. SiS630 provides a total communication solution including 10/100Mb Fast Ethernet for Office requirement and 1Mb HomePNA for Home Networking. SiS630 offers AC’97 compliant interface that comprises digital audio engine with 3D-hardware accelerator, on-chip

sample rate converter, and professional wavetable along with separate modem DMA controller. SiS630 also provides interface to Low Pin Count (LPC) operating at 33 MHz clock which is the same as PCI clock on the host, and dual USB host controller with five USB ports that deliver better connectivity and 2 x 12Mb bandwidth.

The built-in fast PCI IDE controller supports the ATA PIO/DMA, and the Ultra DMA33/66 function that supports the data transfer rate up to 66 MB/s. It provides the separate data path for two IDE channels that can eminently improve the performance under the multi-tasking environment.

Features

Host Interface Controller

- Supports Intel Pentium III/Celeron CPU at 100/66MHz Front Side Bus Frequency
- Synchronous Host/DRAM Clock Scheme
- Asynchronous Host/Dram Clock Scheme

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Integrated DRAM Controller

- 3-DIMM/6-Bank of 3.3V SDRAM
- Supports NEC Virtual Channel Memory (VC-SDRAM) Technology
- Supports Memory Bus up to 133MHz
- System Memory Size up to 1.5GB
- Up to 512 MB per Row
- Supports 16Mb, 64Mb, 128Mb, 256Mb, 512Mb, SDRAM Technology
- Suspend-to-RAM (STR)
- Relocatable System Management Memory Region
- Programmable Buffer Strength for CS#, DQM[7:0], WE#, RAS#, CAS#, CKE, MA[14:0] and MD[63:0]
- Shadow RAM Size from 640KB to 1MB in 16KB incrementss
- Two Programmable PCI Hole Areas

Integrated A.G.P. Compliant Target /66Mhz Host-to-PCI Bridge

- AGP v2.0 Compliant
- Supports Graphic Window Size from 4MBytes to 256MBytes
- Supports Pipelined Process in CPU-to Integrated 3D A.G.P. VGA Access
- Supports 8 Way, 16 Entries Page Table Cache for GART to Enhance Integrated A.G.P. VGA Controller Read/Write Performance
- Supports PCI-to-PCI Bridge Function for Memory Write from 33MHz PCI Bus to Integrated A.G.P. VGA

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Meet PC99 Requirements PCI 2.2 Specification Compliant High Performance PCI Arbiter

- Supports up o 4 PCI Masters
- Rotating Priority Arbitration Scheme
- Advanced Arbitration Scheme Minimizing Arbitration Overhead
- Guaranteed Minimum Access Time for CPU and PCI Masters

Integrated Host-to-PCI Bridge

- Zero Wait State Burst Cycles
- CPU-to-PCI Pipeline Access
- 256B to 4KB PCI Burst Length for PCI Masters
- PCI Master Initiated Graphical Texture Write Cycles Re-mapping
- Reassembles PCI Burst Data Size into Optimized Block Size

Fast PCI IDE Master/Slave Controller

- Supports PCI Bus Mastering
- Native Mode and Compatibility Mode
- PIO Mode 0,1,2,3,4
- Multiword DMA Mode 0,1,2
- Ultra DMA 33/66
- Two Independent IDE Channels Each with 16 DW FIFO

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Virtual PCI-to-PCI Bridge

Integrated Ultra AGP VGA for Hardware 2D/3D Video/Graphics Accelerators

- Supports Tightly Coupled 64 Bits 100mhz Host Interface to VGA to Speed Up GUI Performance and Video Playback Frame Rate
- AGP v. 2.0 Compliant
- Zero-Wait-State 128x4 Post-Write Buffer with Write Combine Capability
- Zero-Wait-State 128x4 2-Way Read Ahead Cache Capability
- Re-locatable Memory-Mapped and I/O Address Decoding
- Flexible Design Shared Frame Buffer architecture for Display Memory
- Shared System Memory Area up to 64MB
- Built-in 8K Bytes Texture Cache
- 32-Bit VLIW Floating-Point Primitive Setup Engine
- Peak Polygon Rate : 4M Polygon/Sec@1 Pixel/Polygon With 16bpp, Bilinear Textured, Z Buffered and Alpha Blended
- Supports Flat and Ground Shading
- Supports High Quality Dithering
- Supports Z-Test, Stencil Test, Alpha Test and Scissors Clipping Test
- Supports Z Pre-Test for Reducing texture Read Dram Bandwidth
- Supports 256 Rops
- Supports Individual Z-Buffer and Render Buffer at the same time
- Supports 16/24/32 BPP Z Buffer Integrater/Floating Formats

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- Supports 16/32 BPP Render Buffer Foramt
- Supports 1/2/4/8 Stencil Format
- Supports Per-Pixel Texture/Fog Perspective Correction
- Supports MIPMAP with Point-Sampled, Linear, Bi-Linear and Tri-Linear Texture Filtering
- Supports Single Pass Two MIPMAP Texture, One Texture on Clock
- Supports up to 2048x2048 Texture Size
- Supports 2?s Power of Width and height structure rectangular texture
- Supports 1/2/4/8 BPP Palletize Texture with 32 Bit ARGB Format
- Supports Fogging and Alpha Blending
- Supports Hardware Back Face Culling
- Supports YUV-to-RGB Color Space Conversion
- Supports CD/DVD to TV Playback Mode
- Supports DVD Sub-Picture Playback Overlay
- Built-in Programmble 24-bits True-Color RAMDAC up to 270 MHz Pixel Clock RAMDAC Snoop Function
- Supports VESA Standard Super High Resolution Graphic Modes

- 640x480 16/256/32K/64K/16M colors 120 Hz NI
- 800x600 16/256/32K/64K/16M colors 120 Hz NI
- 1024x768 256/32K/64K/16M colors 120Hz NI
- 1280x1024 256/32K/64K/16M colors 120Hz NI
- 1600x1200 256/32K/64K/16M colors 100Hz NI
- 1920x1200 256/32K/64K/16M colors 80Hz NI

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- Cooperate with iS Video Bridge ?to support
  - NTSC/PAL Video Output
  - Digital LCD Monitor
  - Secondary CRT Monitor

Low Pin Count Interface

- Forwards PCI I/O and Memory Cycles into LPC bus
- Translates 8/16 bit DMA cycles into PCI bus cycles

Advanced PCI H/W Audio & Modem

- Advanced Wavetable Synthesizer
- DirectSound™ 3D
- Advanced Streaming Architecture
- High Quality Audio and AC”97/98 Support
- Full Legacy Compatibility
- Telephony & Modem
- Software support
- Meets ACPI 1.0 Requirement
- Meets APM 1.2 Requirement
- ACPI Sleep States Include S1, S2, S3, S4, S5
- CPU Power States Include C0, C1, C2, C3
- Power Button with Override

- RTC Day-of-Month, Month-of-Year Alarm
- LED Blinking in S0, S1, S2, S3
- PCI Bus Power Management Interface Spec. 1.0

Integrated DMA Controller

- Two 8237A Compatible DMA Controller
- 8/16 bit DMA data transfer
- Distributed DMA Support

Integrated Interrupt Controller

- Two 8237A Compatible DMA Controller
- Two 8259A Compatible Interrupt Controllers
- Level or Edge Triggered programmable
- Serial IRQ
- Interrupt Source Re-routable to Any IRQ channel

Three 8254 Compatible Programmable 16-bits counters

- System timer interrupt
- Generate refresh request
- Speaker output

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Integrated Keyboard Controller

- Supports PS/2 mouse interface
- Password security and password power-up
- System sleep and power-up by Hot-Key
- KBC and PS2 mouse can be individually disabled

Integrated Real Time Clock (RTC) with 256B CMOS SRAM

- Supports ACPI Day-Month and Month-of-Year- Alarm
- 256 Bytes of CMOS SRAM
- Provides RTC H/W Year 2000 Solution

Universal Serial Bus Host Controller

- Open HCI Host Controller with Root Hub
- Two USB Host Controller
- Five USB Ports
- Supports Legacy Devices
- Over Current Detection

I²C Bus/SMBus Series Interface

- Plug and Play Compatible
- High-Performance 32-Bit PCI Bus Master Architecture with Integrated Direct Memory
- Access (DMA) Controller for Low CPU and Bus utilization
- Supports PCI Device ID, Vendor ID / Subsystem ID , Subsystem Vendor ID
- Programming through the EEPROM interface
- Implements Optional PCI 3.3v Auxiliary Power Source 3.3Vaux Pin and Optional PCI
- IEEE 802.3 and 802.3u Standard Compatible
- IEEE 802.3u Auto Negotiation and Parallel Detection for Automatic Speed Selection
- Full Duplex and Half Duplex Mode for both 10 and 100 Mbps
- Fully Compliant Ansi X3.263 Tp-Pmd Physical Sub-Layer which includes adaptive
- Single 25mhz Clock for 10 and 100 Mbps Operation
- Power Down of 10 base-T/100base-Tx sections when not in use
- Supports 10base-Tx, 100base-Tx

1.2.5 Super IO: NS PC 97338VJG

- High speed PC16550A compatible UART with receive/transmit 16 Bytes FIFO programmable serial baud rate generator
- Multi-mode parallel port support including standard port, EPP/ECP (IEEE1284 compliant, 2 interrupt pins)
- Plug and Play module
- FDC, 100% IBM compatible, S/W & register compatible to 82077 with 16Bytes data FIFO Support 3-Mode FDD
- FIR/MIR/SIR/SHARP ASK for Infrared application.
- COM2

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- IrDA 1.0 / IrDA 1.1 / SHARP ASK
  - Baud rate: max. 4Mb
  - Link distance: 0.01 to 1 m
  - Half angle: ±15…〉.Bιτ Error Rate (BER) : 10^{-9}
  - Peak wavelength: 0.85 - 0.90 mm.
- TQFP 100 pins
- Standby mode: control by software

Default configuration :

	IO address	IRQx	DRQx
COM1	3F8-3FF	4	-
FIR/MIR/SIR/ SHARP ASK (COM2)	278-27F	3	-
PIO	378-37F	7	-
FDD	3F0-3FF	6	2

1.2.6 PC CARD interface controller: TI1225

- ACPI 1.0 Compliance
- PCI Power Management interface specification 1.0 Compliance
- Supports distributed DMA (DDMA) and PC/PCI DMA
- Advanced submicron, low-power CMOS technology.
- Supports two I/O windows and two memory windows available to each cardbus socket.
- Supports five PCI memory windows and two I/O windows available to each PC CARD16 socket.
- Supports Burst Transfers To Maximize Data Throughput On Both PCI Buses
- Provides Serial Interface To TI TPS2202/TPS2206 Dual Slot PC CARD Power Interface Switch
- Supports up to 5 general purpose I/O
- Multi-Function PCI Device With Separate Configuration Space For Each Socket
- Pipelined architecture allows greater than 130Mbps second throughput from cardbus to PCI and from PCI to cardbus.
- Support PCI Bus Lock (/LOCK)
- 3.3-V core logic with universal PCI interface
- PCI Local Bus Specification Revision 2.1 compliant
- Fully compatible with the Intel 430TX(Mobile Triton II) chipset
- 1995 PC Card Standard compliant
- Supports two 16-bit PC card or Cardbus card; sockets powered at 3.3V or 5V with hot insertion and removal
- Provides a serial EEPROM interface for loading the subsystem ID and subsystem vendor ID.
- ExCA compatible Registers mapped in memory or I/O space.
- Supports ring indicate output, SUSPEND# , and programmable output select for CLKRUN#.

- Provides socket activity LED signals.
- Provides zoom video support signals.
- Provides zoom video port function in socket B.
- 208-Pin LQFP package

1.2.7 DUAL-SLOT PC CARD POWER INTERFACE SWITCH: TPS2206

- Fully Integrated Vcc and Vpp Switching for Dual-Slot PC Card Interface
- P 2 C3-Lead Serial Interface Compatible With CardBus Controllers
- 3.3 V Low-Voltage Mode
- Meets PC Card Standards
- RESET for System Initialization of PC Cards
- 12-V Supply Can Be Disabled Except During 12-V Flash Programming
- Short Circuit and Thermal Protection
- 30-Pin SSOP (DB) and 32-Pin TSSOP (DAP)
- Compatible With 3.3-V, 5-V and 12-V PC Cards
- Lower DS(on) (140-m .5-V Vcc Switch; 110-m .3.3-V Vcc Switch)
- Break-Before-Make Switching

1.2.8 Keyboard system: H8(3434F) universal keyboard controller

- CPU
  - Two-way general register configuration
  - Eight 16-bit registers or Sixteen 8-bit registers
  - High-speed operation
  - Maximum clock rate: 16Mhz at 5V
- Memory
  - Include 32KB ROM and 1KB RAM
- 16-bit free-running timer
  - One 16-bit free-running counter
  - Two output-compare lines
  - Four input capture lines
- 8-bit timer (2 channels)
  - Each channel has one 8-bit up-counter , two time constant registers
- PWM timer (2 channels)
  - Resolution: 1/250
  - Duty cycle can be set from 0 to 100%
- I²C bus interface (one channel)
  - Include single master mode and slave mode
- Host interface (HIF)
  - 8-bit host interface port
  - Three host interrupt requests (HIRQ1,11,12)
  - Regular and fast A20 gate output

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- Keyboard controller
  - Controls a matrix-scan keyboard by providing a keyboard scan function with wake-up
  - Interrupts and sense ports
- A/D converter
  - 10-bit resolution
  - 8 channels : single or scan mode (selectable)
- D/A converter
  - 8-bit resolution
  - 2 channels
- Interrupts
  - nine external interrupt lines : NMI# , IRQ0 to 7#
  - 26 on-chip interrupt sources
- Power-down modes
  - Sleep mode
  - Software standby mode
  - Hardware standby mode
- A single chip microcomputer
- On-chip flash memory
- Maximum 64-kbyte address space
- Support three PS/2 port for external keyboard ,mouse and internal track pad.
- Support SMI,SCI trigger input:
- Cover switch

- Battery charging control
- Smart Battery monitoring
- Control D/D system on/off
- Fan control and LED indicator serial interface
- 100pin TQFP

1.2.9 Memory System

1.2.9.1 Main Memory

- HYUNDAI : GM72V281641AT-7K SDRAM
- NEC : UPD45128163G5-A80-9JF SDRAM
  - one chip memory size: 4Banksx1Mx16bit SDRAM.
  - Standard 54 pin TSOP-II package.
  - Power supply: 3 ±0.3V
- Supports One JEDEC 144-pin S.O. DIMM sockets on Mother Board for expansion
- Supports 3.3V SDRAM
- 2 banks on one socket.
- SDRAM accesses time from clock: 6ns
- Memory bus bandwidth: 64 bits

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■7521 Supports 64 MB SDRAM on board and one 144pin DIMM socket for upgrading up to 320MB of DRAM .

Here are some main memory system essential characteristics:

- One chip 4Banksx1Mx16bit on board	64 MB
- 144-pin S.O. DIMM socket	1
- Memory Voltage	3.3V ± 10%
- Banks on DIMM	Total:2
- Mixed type DRAM	Only supports SDRAM

1.2.10 Interface

- Power Supply Jack.
- One Standard Parallel Port With ECP/EPP Functions
- Supports Two USB port for all USB device.
- Supports Macrovision's TV-OUT connector.(layout only)
- Tunable volume by variable resistor .
- Two Serial Ports, One For COM1/COM2, The Other For FIR/MIR/SIR/SHARP ASK
- One External CRT Connector For CRT Display
- One PS/2 Interface For External KB, Mouse Or Other Devices
- Two Cardbus Sockets
- Cable For Connection Between M/B And Panel.
- Cable For Connection Between M/B And Backlight BD.
- Headphone Out Jack, Microphone Input Jack And Line In Jack.
- One MODEM RJ-11 phone jack for PSTN line and RJ-45 for LAN.

- Battery translation board connection between M/B and battery.
- Quick start buttons translation board (QSB) connection between M/B and five Buttons.
- Internet quick start button translation board (IQSB) connection between M/B and touch pad, five LEDs, two Buttons.
- FDD-HDD translation board connection between M/B and floppy, hard disk.
- One CD-ROM connector on M/B.

1.2.11 Audio System: AC'97 CODEC CS4299

- AC'97 CODEC CS4299 provides a complete high quality audio solution, Feature Include:
  - MPU-401 interface
  - FM synthesizer
  - Game Port
  - MIDI port.
  - MODEM
  - CD-ROM
  - User-Defined GPIO
  - Volume Control: Rotary VR
- Stereo BTL 2x1 W Amplifiers(TPA0202) With 8 Ohm Load.
- CD-ROM IDE Interface
- 18-bit Stereo ADC & 20-bit Stereo DAC For Record And Play Back
- Programmable Sample Rates From 20Hz To 20kHz For Record And Playback
- Microphone in * 1 (3.5 mm phone-jack)
- Headphone out * 1: stereo (3.5 mm phone-jack and SCMS support)

- Line in * 1(3.5 mm phone-jack)
- Built-in Speaker * 2 (1w, 8 ohm)
- Built-in Microphone * 1
- Note: For Those Input Source Not Using Should Be Set Mute In Order To Reduce Noise. Like Line In

1.2.12 IR MODULE: HSDL-3600#007

- Fully Compliant to IrDA 1.1 Specifications
  - 115.2 kb/s to 4 Mb/s operation
  - excellent nose-to-nose operation
- Compatible with ASK, HP-SIR, and TV Remote
- IEC825-Class 1 Eye Safe
- Wide Operating Voltage Range
  - 2.7 V to 5.25 V
- Small Module Size
  - 4.0 x 12.2 x 5.1 mm (HxWxD)
- Complete Shutdown
  - TXD, RXD, PIN diode
- Low Shutdown Current
  - 10 nA typical
- Adjustable Optical Power Management
  - Adjustable LED drive-current to maintain link integrity

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- Single Rx Data Output
  - FIR Select pin switch to FIR
- Integrated EMI Shield
  - Excellent noise immunity
- Edge Detection Input
  - Prevents the LED from long turn-on time
- Interface to various Super I/O and Controller Devices
- Designed to Accommodate Light Loss with Cosmetic Window
- Minimum External Components Required

1.2.13 Special Feature Function

1.2.13.1 Hot Key Function

Keys Combination	Feature	Meaning
Fn + F5	LCD/external CRT switching	Rotate display mode in LCD only, CRT only and simultaneously display.
Fn + F6	Brightness down	Decreases the LCD brightness / No function in DSTN model
Fn + F7	Brightness up	Increases the LCD brightness / No function in DSTN model
Fn + F10	Enable/Disable Battery Warning Beep	Toggle Battery Warning on/off
Fn + F11	Panel Off/On	Toggle Panel Off/On
Fn + F12	Suspend to DRAM/HDD	Force the computer into either Suspend to HDD or Suspend to DRAM mode depending on BIOS Setup.

1.2.13.2 Quick Start Button function

Keys	Feature	Meaning
IQSB	Mail Received Button (or function “Recognizable Signal”)	Determined by Software component.
ESB1	Entertainment Quick Key	Determined by Software component.
ESB2	Instant Internet	Determined by Software component.
ESB3	My Presario	Determined by Software component.
ESB4	Search	Determined by Software component.
ESB5	Email	Determined by Software component.

1.2.13.3 Flash ROM (BIOS)

7521 system utilizes the state-of-the-art Flash EEPROM technology. User can upgrade the system BIOS in the future just running the program from MiTAC.

1.2.13.4 LED Indicators

System has ten status LED indicators to display system activity which include above keyboard and below touch pad:

1. Four LED indicators below touch pad:
   From left to right that indicates MAIL RECEIVED, AC POWER, BATTERY POWER and BATTERY STATUS:
   - Mail Received status: This LED lights to indicate that User received E-mail status. User can define color of LED (yellow or green) to indicate relation of transmitter.
   - AC POWER: This LED lights green when the notebook is being powered by AC, and flash (on 1 second, off 1 second) when Suspend to DRAM is active using AC power. The LED is off when the notebook is off or powered by batteries, or when Suspend to Disk.
   - BATTERY POWER: This LED lights green when the notebook is being powered by batteries, and flashes (on 1 second, off 1 second) when Suspend to DRAM is active using battery power. The LED is off when the notebook is off or powered by AC, or when Suspend to Disk.
   - BATTERY STATUS : During normal operation, this LED stays off as long as the battery is charged. When the battery charge drops to 10% of capacity, the LED lights red, flashes per 1 second and beeps per 2 second. When AC is connected, this indicator glows green if the battery pack is fully charged, or orange (amber) if the battery is being charged.
2. Six LED indicators above keyboard:
   From left to right that indicates CD-ROM/MO, HARD DISK DRIVE, FLOPPY DISK DRIVE, NUM LOCK, CAPS LOCK and SCROLL LOCK.

1.2.13.5 COM port assignment

- COM1: MODEM / RS-232 / Disable
- COM2: IR / RS-232 / Disable

1.3 SMM and System BIOS

1.3.1 System Management Mode

7521 system has built in several power saving modes to prolong the battery usage for mobile purpose. User can enable and configure different degrees of power management modes via ROM CMOS setup (booting by pressing F2 key). Following are the descriptions of the SMM and power management modes supported.

1.3.1.1 Full On Mode

In this mode, each device is running with the maximal speed. CPU clock is up to its maximum.

1.3.1.2 Doze Mode

In this mode, CPU will be toggling between on & stop grant mode either. The technology is clock throttling. This can save battery power without loosing much computing capability. The CPU power consumption and temperature is lowered in this mode.

1.3.1.3 Standby Mode

For more power saving, it turns of f the peripheral component. In this mode, the following is the status of each device.

- CPU: Stop grant
- LCD: backlight off
- HDD: spin down
- FDD: standby

1.3.1.4 Suspend Mode

The most chipset of the system is entering power down mode for more power saving. In this mode , the following is the status of each device.

1.3.1.4.1 Suspend to DRAM:

- CPU: off
- SiS630: Partial off
- VGA: off
- PCMCIA: off
- Super IO: off
- Audio: off
- SDRAM: Self Refresh.

1.3.1.4.2 Suspend to HDD:

- All devices are stopped clock and power-down,
- System status is saved in HDD.
- All system status will be restored when powered on again.

1.3.1.5 Other power management functions

1.3.1.5.1 HDD & Video access

System has the ability to monitor video and hard disk activity. User can enable monitoring function for video and/or hard disk individually. When there is no video and/or hard disk activity, system will enter next PMU state depending on the application. **When the VGA activity monitoring is enabled, the performance of the system will have some impact.**

1.3.1.5.2 Battery Warning

System also provides Battery capacity monitoring and gives user a warning so that users have chance to save his data before battery dead. Also, this function protects system from mal-function while battery capacity is low.

-Battery Warning: Capacity below 10%, Battery Capacity LED flashes per second, system beeps per 2 seconds. (System beeps only if BIOS setup enable Battery Warning Beeping.) System will Suspend to HDD after 2 Minute if BIOS setup enable this function or system will runs until battery dead without any protection.

1.3.1.5.3 Cover Switch

System automatically provides power saving on monitoring Cover Switch. It will save battery power and prolong the usage time when user closes the notebook cover unintentionally but the system still in power on mode. There are two functions to be chosen.

1. Switch to CRT
2. Panel Off
3. Suspend to DRAM or Suspend to Disk by CMOS setup

1.3.1.5.4 Battery Warning State

RedSea system provides battery management function and gives warning while battery is in Its low power state. When the battery capacity is below 10% (Battery Warning State), system will generate beep for every 2 seconds. When hearing the beeping, it is recommended that user should plug in AC adapter to get power from external source, or stop working and save his data file to prevent disaster results.

1.3.1.5.5 Battery Low State

After Battery Warning State, and battery capacity is below 4%, system will generate beep for twice second.

1.3.1.5.6 Battery Dead State

When the battery voltage level reaches 9 volts, system will shut down automatically in order to extend the battery packs' life.

1.3.2 System BIOS

1.3.3 Fan power on/off management

FAN is controlled by H8 embedded controller which using LM45 to sense CPU temperature and PWM to control fan speed.

1.4 Power Supply System

- Please refer to the document for 7521 adapter, DC-to-DC and backlight BD.

1.5 Peripheral Components

1.5.1 LCD PANEL

- Hyundai 14X13
  - 1024X768 XGA TFT Panel
  - Display size (diagonal): 14.1 inch
  - 262,144 colors display
  - 1 channel LVDS Interface (Flat Link, Ti)
  - Display Mode: Normal White

- Back-light unit : CCFL, 1 tube
- DC for Panel : 3.3V+-0.3V
- Pixel pitch : 0.279(H)X0.279(V)
- Power supply current : 320 mA (Typ)
- Lamp start Voltage : 1500Vrms (25℃)

1.5.2 HDD

- FUJITSU MHK2120AT : 12 GB Capacity

— 12.0GB Capacity
— Number of head : 3
— Number of cylinders : 14,784
— Bytes per sector : 512
— Recording method : 16/17 MTR
— Track density : 24,300 TPI
— Bit Density : 383 Kbpi
— Rotational Speed : 4,200 rpm +-1%
— Average Latency : 7.14 ms
— Interface : ATA-5 (Max. Cable length : 0.46 m)
— Data transfer rate :
— To/From Media : 12.5 to 22.3 MB/s
— To/From Host : 66.6 MB/s Max (Ultra-DMA mode 4)
— Data Buffer Size : 512 KB
— Spin up current : $0.9A_{rms}$
— Max. Power Consumption : 4.5W (During spin up)
— Physical Dimensions (H X W X D) : 9.5 mm X 100.0 mm X 70.0 mm
— 15GB, 20GB, 24GB HDD To Be Defined.

1.5.3 Keyboard

- External keyboard: Supports IBM 106 key compatible keyboard
  - Key pitch : 19 mm
  - Windows95 applied
- Internal keyboard: Compatible Japanese keyboard layout (90 keys)

1.5.4 Floppy Disk Drive

- Mitsumi D353G
- Using High density (2HD) 3.5 inch disk
- Data transfer rate: 500k bits/sec
- Disk rotational speed: 300 rpm for 2mode, 360rpm for 3mode
- Track density: 135 tpi
- Track to Track time: 3msec

1.5.5 Touch Pad

- Logic Tech : 904255-0002
- Vcc : 5V +- 0.5
- Icc(max) : 15 mA
- Interface : PS/2
- X/Y position resolution : 480+-50 CPI
- Dimension : 66mm x 50mm x 5.0mm
- effective area : 55mm x 39 mm
- Operating Temp. : 0 - 50 degree C
- Storage Humidity : 5 - 90 %,
- Storage Temp. : -20 - + 60 degree C
- ESD : 15KV applied to front surface

1.5.6 24X CD-ROM Drive

- System has optional MATSUSHITA UJDA150 24X speed CD-ROM drive, LGS CRN8241B 24X speed CD-ROM drive, or TEAC CD-224E-A92 24X speed CD-ROM drive.
- Hardware interface is compliant with ATAPI IDE specification.
- IDE second channel (170h). The default drive is D. User should install the CD-ROM device driver in order to operate this device. This CD-ROM drive also support audio interface. Co-operate with audio circuit, CD-ROM drive can work as a CD player.
- Ejection: Manual eject using the eject button/Automatically eject using the tray

- XM-1802B:
  - average data transfer rate of 3,600 KB/s
  - average random seek time of 100ms
  - Random access time of 110ms.
  - Small size (only 12.7(H) x 128(W) x 129(D)mm)
  - Extremely low weight of 230g
  - Low average power consumption of 2.4W (maximum only 3.2W).

1.5.7 DVD-ROM drive

MATSUSHITA: UJDA520L-SH 4X speed

- Fast 170 ms Random Access Time (DVD)
- Max. 4X (DVD)/Max. 24X (CD)
- Max. 5,408 Kbytes/s (DVD)/Max. 3,600 Kbytes/s (CD) Sustained Transfer Rate.
- PIO mode-4 ATAPI Drive (16.7 Mbyte/s)
- DMA: Multi word DMA transfer mode-2 (Transfer Rate 16.7 Mbyte/s)
  : Ultra DMA mode-2 (Transfer Rate 33.3 Mbyte/s)

1.5.8 CD-R/RW drive

- MATSUSHITA: UJDA310
  - WRITE 4X-Speed
  - READ max 20X-Speed (CD-RW max 14X-Speed)
  - PIOMODE: 16.6MB/s ; Mode 4
  - DMAMODE: 4.2MB/s ; Mode 0
  - Write: 150KB/s (Normal speed), 300KB/s(2X speed), 600KB/s(4X speed)
  - Buffer memory: 2MB
  - Access speed 150ms (Typ.)

1.5.9 LED Indicators

- Lower ICON LEDs on M/B
  - Mail Received status (**left** 1)
  - AC POWER(Left 2)
  - BATTERY POWER(**right** 2)
  - BATTERY STATUS(**right** 1)
- Upper ICON LEDs on M/B
  - CD-ROM/MO(**left** 1)
  - HARD DISK DRIVE(**left** 2)
  - FLOPPY DISK DRIVE(**left** 3)
  - NUM LOCK(**right** 3)
  - CAPS LOCK(**right** 2)
  - SCROLL LOCK(**right** 1)

1.5.10 IR port

- HP HSDL-3600#007 FIR Module
  - Meet IrDA Physical Layer Specification
  - 1 cm to 1 Meter Operating Distance
  - 30 degree Viewing Angle
  - Support Two Channels - 2.4 Kb/s to 115.2Kb/s and 1.15Mb/s to 4.0 Mb/s

1.5.11 CMOS Battery

- CR2032 3V 220mAh lithium battery
- When AC in or system main battery in , CMOS battery will no power consumption.
- AC or main battery not exist, CMOS battery life at less (220mAh/5.8uA) 4 years.
- In normal condition, battery life is at less over 4 years. Battery was put in battery holder, can be replaced

1.5.12 Serial Interface

- Using AD ADM3311ARU chip
- ESD rating:±3KV
- Lead TEMP.(Soldering 10sec):+300 ℃
- Number of RS-232 drivers : 3
- Number of RS-232 receivers : 5
- 28 pin SSOP package
- Support shutdown mode(pin 23).
- -40 ℃ - +85 ℃ Operating voltage range : 3V ±0.3V
- MAX. data rate:460 kbps
- Shutdown supply current : 15(TYP)uA- 50(MAX)Ua

1.5.13 PCMCIA socket

- Operating temperature range : -55 ℃- +85 ℃
- Insertion force : 39.2N (MAX)
- 10000 times insertion and withdrawal at the cycle rate 400- 600cycles/hour and no
- evidence of breakage and cracks on the component.
- In +85 ℃ 250h life test conditions should be no evidence of breakage and
- Cracks on the component.
- In -55 ℃ 96h life test conditions should be no evidence of breakage and
- Cracks on the component.

1.5.14 FAN

- Dimension : Made by Sunonwealth Electric Machine Industry Co. Ltd.
- Model number : KD0502PEB2-8 DC brushless fan
- Operating speed: 8000 rpm.
- Input voltage : 5V
- Operating temperature : -10 - +70 degree C.
- Weight : 7g
- Direction of rotation : C.C.W.
- Noise level : 27 dB(A)
- Rated power : 0.6 W
- Static pressure : 0.09 inch-H2O
- Air delivery : 2.3 CFM

1.6 Appendix 1: GPIO definitions

GPI DEFINITIONS

Signal Name	Function	Description	During PCIRST#	After PCIRST#	S1	S3	S4/S5	Remark
GPIO[0]	OC0#	USB OVER CURRENT	High	High	High	Off	Off	
GPIO[2]	RST_CDROM	Reset CD-ROM drive	High	High	High	Off	Off	
GPIO[3]	EEDO	FOR LAN	In	In	Defined	Off	Off	
GPIO[4]	KBD_US/JP#		In	In	Defined	Off	Off	
GPIO[5]	GPIO5		In	In	Defined	Off	Off	
GPIO[6]	EXTSMI#		In	In	Defined	Off	Off	
GPIO[7]	SPDIF	SPDIF enable	In	In	Defined	Off	Off	
GPIO[8]	GPIO8		In	In	Defined	Off	Off	
GPIO[9]	GND		In	In	Defined	Off	Off	
GPIO[10]	FDD_MODE		In	In	Defined	Off	Off	
GPIO[11]	SPK_OFF		In	In	Defined	Off	Off	
GPIO[12]	RS232_OFF#		In	In	Defined	Off	Off	
GPIO[13]	CARD_IN#		In	In	Defined	Off	Off	
GPIO[14]	CRT_IN#		In	In	Defined	Off	Off	
GPIO[15]	CARD_ACT		In	In	Defined	Off	Off	

1.6 Appendix 2: GPIO definitions

GPI DEFINITIONS

Note 1. LCD ID

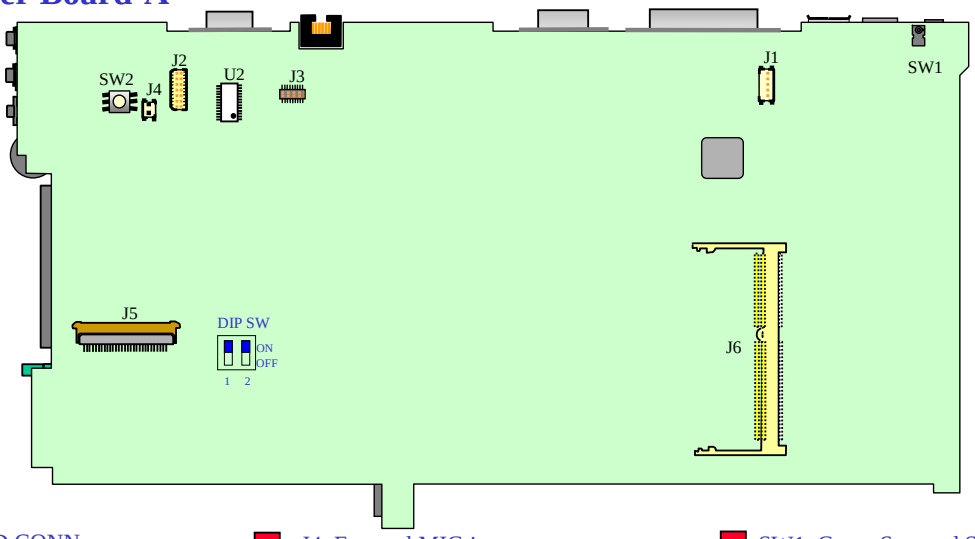
LCD_ID2	LCD_ID1	LCD_ID0	Vendor	PANEL	Description
1	1	1	HUYNDAI	14X13	

Note 3. CPU & SDRAM Frequency setting table:

SW_FS3	SW_FS2	SW_FS1	SW_FS0	CPU	SDRAM
0	0	0	0	66	100
0	0	0	1	100	100
0	0	1	1	133	100
0	1	0	0	66	133
0	1	0	1	100	133
0	1	1	1	133	133
1	0	0	0	66	66

2. DEFINITION & LOCATION OF CONNECTORS/SWITCHES

2.1 Mother Board-A



- J1:Inverter BD CONN.
- J2: LCD panel connector.
- J3: Quick key transfer BD connector.
- J4: External MIC-in connector.
- J5: Internal keyboard connector.
- J6: 144 pins expansion SDRAM socket.
- SW1: Cover Suspend SW.
- SW2: Power button.
- DIP SW : CPU FSB SELECT

FSB	DIP SW /BIT1	DIP SW /BIT2
66MHZ	OFF	OFF
100MHZ	OFF	ON
150MHZ	ON	OFF
133MHZ	ON	ON

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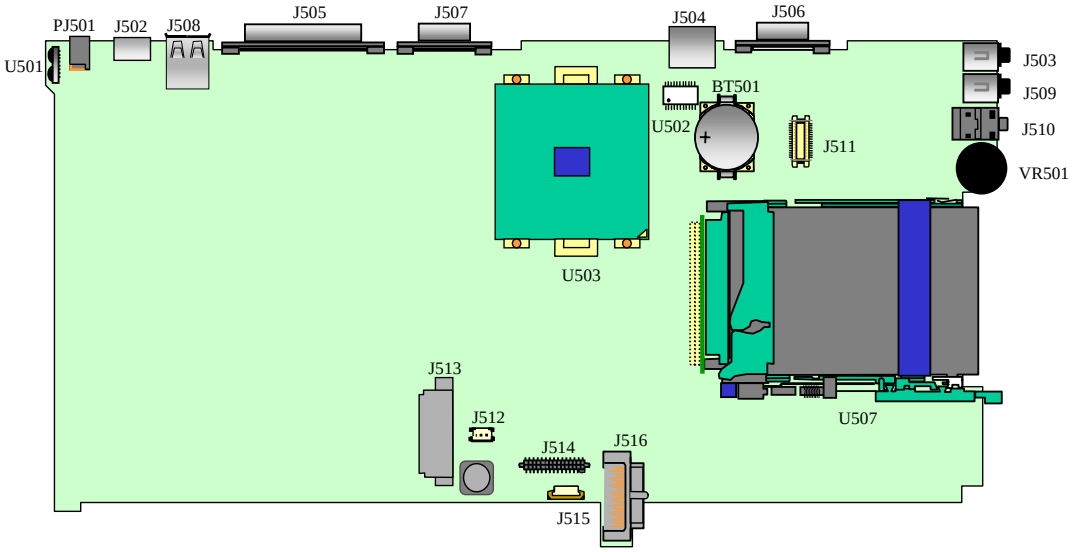
2. DEFINITION & LOCATION OF CONNECTORS/SWITCHES

2.2 Mother Board-B

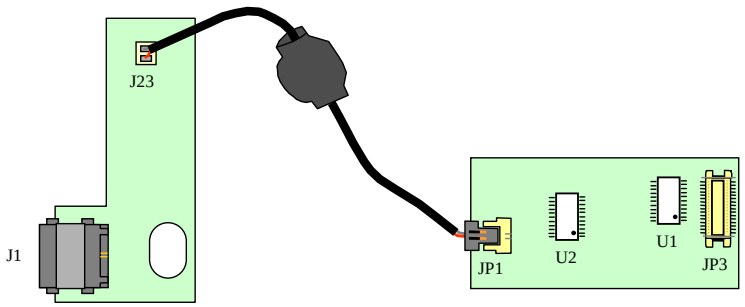


- PJ501: Power jack (AC adapter).
- J502 :PS2 Mouse/keyboard
- J503:Line in Jack.
- J504: LAN connect
- J505:Parallel Port
- J507: VGA Connector.
- J508: USB connector.
- U507: PC card socket.
- U503:CPU & CPU Socket.
- J511: MODEM transfer board connector
- J512: FAN Connector.
- J516 :HDD/FDD Connector.
- J513: CD-ROM drive connector.
- J514:Charger & Touch-Pad connector
- J515:Touch-Pad button connector.
- BT501: CMOS Battery connector.
- VR501: Volume control VR.

2. DEFINITION & LOCATION OF CONNECTORS/SWITCHES

2.3 Daughter Board

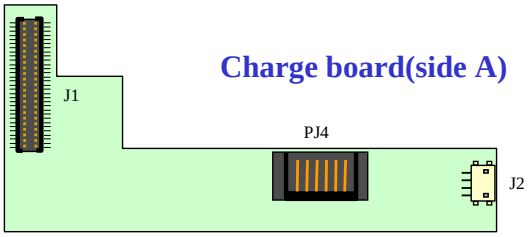
MDC/LAN transfer board

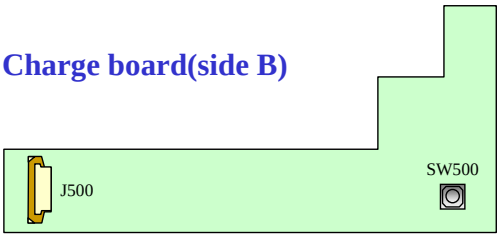


- J1: RJ-11 phone jack for internal modem.
- J23: MDC jump wire connector.
- JP1: MDC jump wire connector.
- JP3: Connector 2 for connected MDC/LAN transfer board to M/B.

2. DEFINITION & LOCATION OF CONNECTORS/SWITCHES

2.4 Charger Board





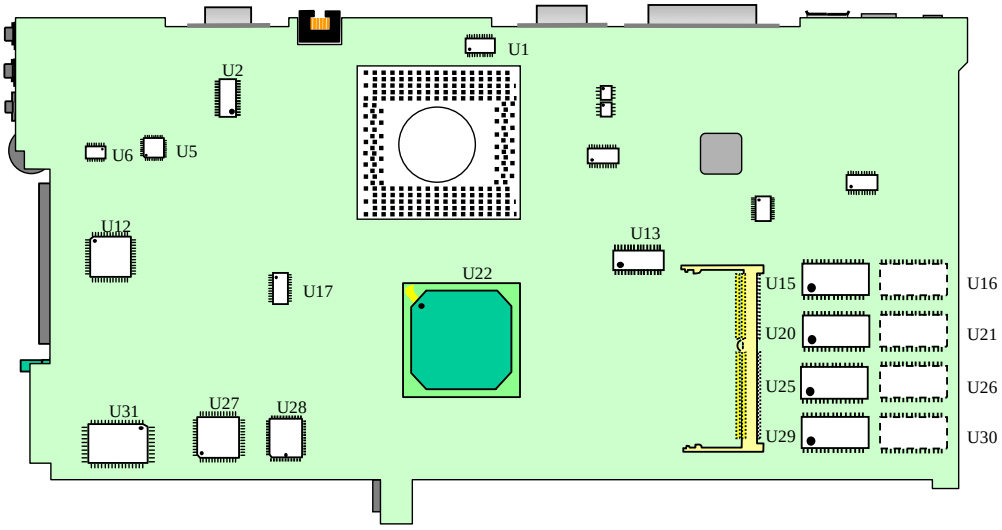
- J1:Charger & Touch-Pad connector to M/B.
- PJ4:Battery pack connector.
- J2: Internal speaker connector.

- J500: Touch-Pad button connector.
- SW500: CMOS Reset

7521 N/B MAINTENANCE

3. DEFINITION & LOCATION OF MAJOR COMPONENTS

3.1 Main Board (Side A)



- U1: ADM3311ARU RS232/SIO.
- U2: DS90C363MTD VGA LVD controller.
- U5: CS4299 AC'97 CODE.
- U6: TPA0202 AUDIO AMP.
- U12: H8(3434F) universal.
- U13: ICS9248-102 Frequency Synthesizer.
- U17: TPS2206 PCcard Power switch matrix.
- U22: SiS630 single chipset.
- U27: Super IO PC97338VJG.
- U28: System BIOS.
- U31:W83626 LPC to ISA.
- U15,U20,U25,U29 : On board SDAM.

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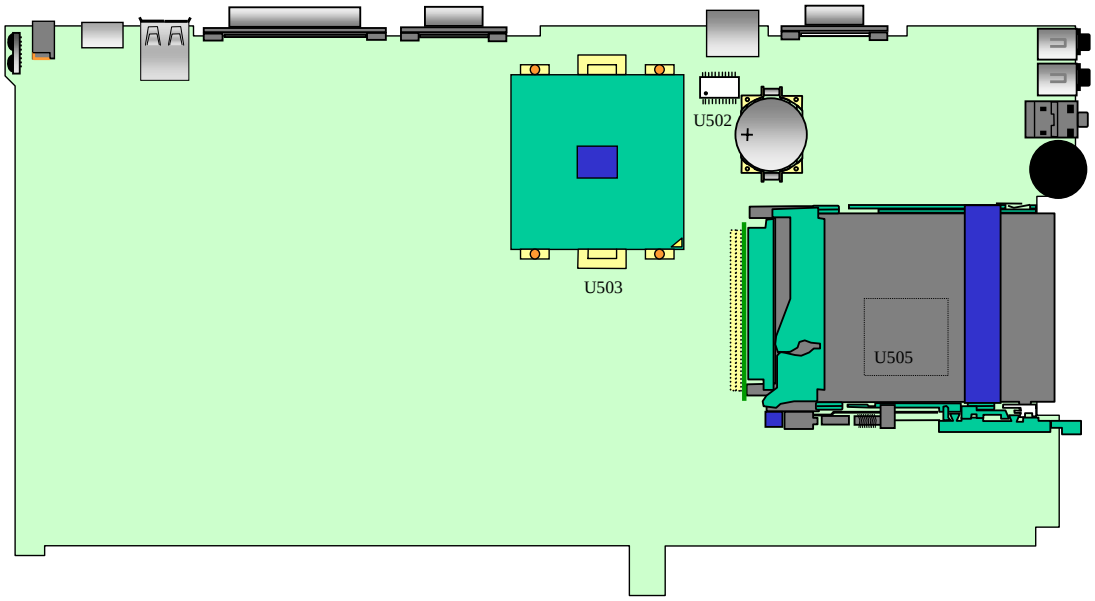
3. DEFINITION & LOCATION OF MAJOR COMPONENTS

3.2 Main Board (SIDE B)

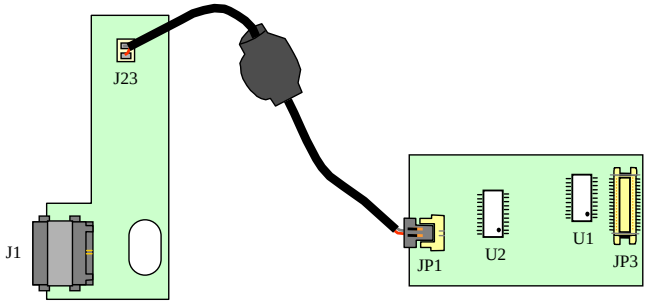


- U502: PH163112 LAN Controller.
- U503: Socket 370 CPU.
- U505: PCI1225PDV PC CARD interface controller.

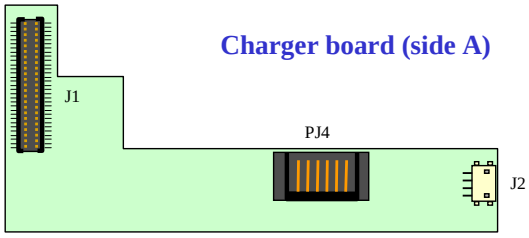
3. DEFINITION & LOCATION OF MAJOR COMPONENTS

3.3 Definition Of Daughter Board

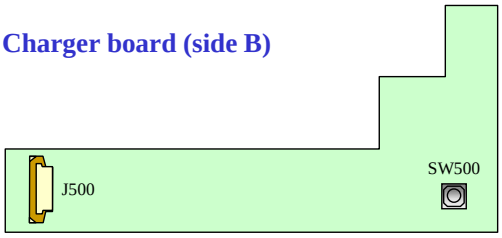
MDC/LAN transfer board



Charger board (side A)



Charger board (side B)



4. PIN DESCRIPTIONS OF MAJOR COMPONENTS

4.1 Pentium III/Celeron FC-PGA2 CPU

Alphabetical Signal Reference

Signal Name	I/O	Signal Description
A[35:3]#	I/O GTL+	The A[35:3]# (Address) signals define a 2^{36}-byte physical memory address space. When ADS# is active, these signals transmit the address of a transaction; when ADS# is inactive, these signals transmit transaction information. These signals must be connected to the appropriate pins/balls of both agents on the system bus. The A[35:24]# signals are protected with the AP1# parity signal, and the A[23:3]# signals are protected with the AP0# parity signal. On the active-to-inactive transition of RESET#, each processor bus agent samples A[35:3]# signals to determine its power-on configuration. See Section 4 of this document and the *PentiumII Processor Developer's Manual* for details.
A20M#	I 1.5V Tolerant	If the A20M# (Address-20 Mask) input signal is asserted, the processor masks physical address bit 20 (A20#) before looking up a line in any internal cache and before driving a read/write transaction on the bus. Asserting A20M# emulates the 8086 processor's address wrap-around at the 1-Mbyte boundary. Assertion of A20M# is only supported in Real mode.
ADS#	I/O GTL+	The ADS# (Address Strobe) signal is asserted to indicate the validity of a transaction address on the A[35:3]# signals. Both bus agents observe the ADS# activation to begin parity checking, protocol checking, address decode, internal snoop or deferred reply ID match operations associated with the new transaction. This signal must be connected to the appropriate pins/balls on both agents on the system bus.
AERR#	I/O GTL+	The AERR# (Address Parity Error) signal is observed and driven by both system bus agents, and if used, must be connected to the appropriate pins/balls of both agents on the system bus. AERR# observation is optionally enabled during power-on configuration; if enabled, a valid assertion of AERR# aborts the current transaction. If AERR# observation is disabled during power-on configuration, a central agent may handle an assertion of AERR# as appropriate to the error handling architecture of the system.
AP[1:0]#	I/O GTL+	The AP[1:0]# (Address Parity) signals are driven by the request initiator along with ADS#, A[35:3]#, REQ[4:0]# and RP#. AP1# covers A[35:24]#. AP0# covers A[23:3]#. A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. This allows parity to be high when all the covered signals are high. AP[1:0]# should be connected to the appropriate pins/balls on both agents on the system bus.
BCLK	I 2.5V Tolerant	The BCLK (Bus Clock) signal determines the system bus frequency. Both system bus agents must receive this signal to drive their outputs and latch their inputs on the BCLK rising edge. All external timing parameters are specified with respect to the BCLK signal.

Signal Name	I/O	Signal Description
BERR#	I/O GTL+	The BERR# (Bus Error) signal is asserted to indicate an unrecoverable error without a bus protocol violation. It may be driven by either system bus agent and must be connected to the appropriate pins/balls of both agents, if used. However, the mobile Pentium III processors do not observe assertions of the BERR# signal. BERR# assertion conditions are defined by the system configuration. Configuration options enable the BERR# driver as follows: • Enabled or disabled • Asserted optionally for internal errors along with IERR# • Asserted optionally by the request initiator of a bus transaction after it observes an error • Asserted by any bus agent when it observes an error in a bus transaction
BINIT#	I/O-GTL+	The BINIT# (Bus Initialization) signal may be observed and driven by both system bus agents and must be connected to the appropriate pins/balls of both agents, if used. If the BINIT# driver is enabled during the power-on configuration, BINIT# is asserted to signal any bus condition that prevents reliable future information. If BINIT# is enabled during power-on configuration, and BINIT# is sampled asserted, all bus state machines are reset and any data which was in transit is lost. All agents reset their rotating ID for bus arbitration to the state after reset, and internal count information is lost. The L1 and L2 caches are not affected. If BINIT# is disabled during power-on configuration, a central agent may handle an assertion of BINIT# as appropriate to the Machine Check Architecture (MCA) of the system.
BNR#	I/O-GTL+	The BNR# (Block Next Request) signal is used to assert a bus stall by any bus agent that is unable to accept new bus transactions. During a bus stall, the current bus owner cannot issue any new transactions. Since multiple agents may need to request a bus stall simultaneously, BNR# is a wired-OR signal that must be connected to the appropriate pins/balls of both agents on the system bus. In order to avoid wire-OR glitches associated with simultaneous edge transitions driven by multiple drivers, BNR# is activated on specific clock edges and sampled on specific clock edges.
BP[3:2]#	I/O GTL+	The BP[3:2]# (Breakpoint) signals are the System Support group Breakpoint signals. They are outputs from the processor that indicate the status of breakpoints.
BPM[1:0]#	I/O GTL+	The BPM[1:0]# (Breakpoint Monitor) signals are breakpoint and performance monitor signals. They are outputs from the processor that indicate the status of breakpoints and programmable counters used for monitoring processor performance.

4. PIN DESCRIPTIONS OF MAJOR COMPONENTS

4.1 Pentium III/Celeron FC-PGA2 CPU

Alphabetical Signal Reference

Signal Name	I/O	Signal Description
BPRI#	I GTL+	The BPRI# (Bus Priority Request) signal is used to arbitrate for ownership of the system bus. It must be connected to the appropriate pins/balls on both agents on the system bus. Observing BPRI# active (as asserted by the priority agent) causes the processor to stop issuing new requests, unless such requests are part of an ongoing locked operation. The priority agent keeps BPRI# asserted until all of its requests are completed and then releases the bus by deasserting BPRI#.
BREQ0#	I/O GTL+	The BREQ0# (Bus Request) signal is a processor Arbitration Bus signal. The processor indicates that it wants ownership of the system bus by asserting the BREQ0# signal. During power-up configuration, the central agent must assert the BREQ0# bus signal. The processor samples BREQ0# on the active-to-inactive transition of RESET#.
BSEL[1:0]	I 1.5V Tolerant	The BSEL[1:0] (Select Processor System Bus Speed) signal is used to configure the processor for the system bus frequency. Table 38 shows the encoding scheme for BSEL[1:0]. The only supported system bus frequency for the mobile Pentium III processor is 100 MHz. If another frequency is used or if the BSEL[1:0] signals are not driven with "1" then the processor is not guaranteed to function properly. **BSEL[1:0] Encoding** **BSEL[1:0] — System Bus Frequency** 00 — 66 MHz 01 — 100 MHz 10 — Reserved 11 — 133 MHz
CLKREF	Analog	The CLKREF (System Bus Clock Reference) signal provides a reference voltage to define the trip point for the BCLK signal. This signal should be connected to a resistor divider to generate 1.25V from the 2.5-V supply.
CMOSREF	Analog	The CMOSREF (CMOS Reference Voltage) signal provides a DC level reference voltage for the CMOS input buffers. A voltage divider should be used to divide a stable voltage plane (e.g., 2.5V or 3.3V). This signal must be provided with a DC voltage that meets the VCMOSREF specification from Table 13.
D[63:0]#	I/O GTL+	The D[63:0]# (Data) signals are the data signals. These signals provide a 64-bit data path between both system bus agents, and must be connected to the appropriate pins/balls on both agents. The data driver asserts DRDY# to indicate a valid data transfer.
DBSY#	I/O-GTL+	The DBSY# (Data Bus Busy) signal is asserted by the agent responsible for driving data on the system bus to indicate that the data bus is in use. The data bus is released after DBSY# is deasserted. This signal must be connected to the appropriate pins/balls on both agents on the system bus.
DEFER#	I GTL+	The DEFER# (Defer) signal is asserted by an agent to indicate that the transaction cannot be guaranteed in-order completion. Assertion of DEFER# is normally the responsibility of the addressed memory agent or I/O agent. This signal must be connected to the appropriate pins/balls on both agents on the system bus.
DEP[7:0]#	I/O GTL+	The DEP[7:0]# (Data Bus ECC Protection) signals provide optional ECC protection for the data bus. They are driven by the agent responsible for driving D[63:0]#, and must be connected to the appropriate pins/balls on both agents on the system bus if they are used. During power-on configuration, DEP[7:0]# signals can be enabled for ECC checking or disabled for no checking.
DRDY#	I/O GTL+	The DRDY# (Data Ready) signal is asserted by the data driver on each data transfer, indicating valid data on the data bus. In a multi-cycle data transfer, DRDY# can be deasserted to insert idle clocks. This signal must be connected to the appropriate pins/balls on both agents on the system bus.
EDGCTRLP	Analog	The EDGCTRLP (Edge Rate Control) signal is used to configure the edge rate of the GTL+ output buffers. Connect the signal to VSS with a 110-Ω, 1% resistor.
FERR#	O 1.5V Tolerant Open-drain)	The FERR# (Floating-point Error) signal is asserted when the processor detects an unmasked floating-point error. FERR# is similar to the ERROR# signal on the Intel 387 coprocessor, and it is included for compatibility with systems using DOS-type floating-point error reporting.
FLUSH#	I 1.5V Tolerant	When the FLUSH# (Flush) input signal is asserted, the processor writes back all internal cache lines in the Modified state and invalidates all internal cache lines. At the completion of a flush operation, the processor issues a Flush Acknowledge transaction. The processor stops caching any new data while the FLUSH# signal remains asserted. On the active-to-inactive transition of RESET#, each processor bus agent samples FLUSH# to determine its power-on configuration.

4. PIN DESCRIPTIONS OF MAJOR COMPONENTS

4.1 Pentium III/Celeron FC-PGA2 CPU

Alphabetical Signal Reference

Signal Name	I/O	Signal Description
GHI#	I 1.5V Tolerant	The GHI# signal controls which operating mode bus ratio is selected in a mobile Pentium III processor featuring Intel SpeedStep technology. On the processor featuring Intel SpeedStep technology, this signal is latched when BCLK restarts in Deep Sleep state and determines which of two bus ratios is selected for operation. This signal is ignored when the processor is not in the Deep Sleep state. This signal is a "Don't Care" on processors that do not feature Intel SpeedStep technology. This signal has an on-die pull-up to VccT and should be driven with an Open-drain driver with no external pull-up.
HIT#, HITM#	I/O GTL+	The HIT# (Snoop Hit) and HITM# (Hit Modified) signals convey transaction snoop operation results, and must be connected to the appropriate pins/balls on both agents on the system bus. Either bus agent can assert both HIT# and HITM# together to indicate that it requires a snoop stall, which can be continued by reasserting HIT# and HITM# together.
IERR#	O 1.5V Tolerant Open-drain	The IERR# (Internal Error) signal is asserted by the processor as the result of an internal error.Assertion of IERR# is usually accompanied by a SHUTDOWN transaction on the system bus. This transaction may optionally be converted to an external error signal (e.g., NMI) by system logic. The processor will keep IERR# asserted until it is handled in software or with the assertion of RESET#, BINIT, or INIT#.
IGNNE#	I 1.5V Tolerant	The IGNNE# (Ignore Numeric Error) signal is asserted to force the processor to ignore a numeric error and continue to execute non-control floating-point instructions. If IGNNE# is deasserted, the processor freezes on a non-control floating-point instruction if a previous instruction caused an error. IGNNE# has no affect when the NE bit in control register 0 (CR0) is set.
INIT#	I 1.5V Tolerant	The INIT# (Initialization) signal is asserted to reset integer registers inside the processor without affecting the internal (L1 or L2) caches or the floating-point registers. The processor begins execution at the power-on reset vector configured during power-on configuration. The processor continues to handle snoop requests during INIT# assertion. INIT# is an asynchronous input. If INIT# is sampled active on RESET#'s active-to-inactive transition, then the processor executes its built-in self test (BIST).

Signal Name	I/O	Signal Description
INTR	I 1.5V Tolerant	The INTR (Interrupt) signal indicates that an external interrupt has been generated. INTR becomes the LINT0 signal when the APIC is enabled. The interrupt is maskable using the IF bit in the EFLAGS register. If the IF bit is set, the processor vectors to the interrupt handler after completing the current instruction execution. Upon recognizing the interrupt request, the processor issues a single Interrupt Acknowledge (INTA) bus transaction. INTR must remain active until the INTA bus transaction to guarantee its recognition.
LINT[1:0]	I 1.5V Tolerant	The LINT[1:0] (Local APIC Interrupt) signals must be connected to the appropriate pins/balls of all APIC bus agents, including the processor and the system logic or I/O APIC component. When APIC is disabled, the LINT0 signal becomes INTR, a maskable interrupt request signal, and LINT1 becomes NMI, a non-maskable interrupt. INTR and NMI are backward compatible with the same signals for the Pentium processor. Both signals are asynchronous inputs. Both of these signals must be software configured by programming the APIC register space to be used either as NMI/INTR or LINT[1:0] in the BIOS. If the APIC is enabled at reset, then LINT[1:0] is the default configuration.
LOCK#	I/O GTL+	The LOCK# (Lock) signal indicates to the system that a sequence of transactions must occur atomically. This signal must be connected to the appropriate pins/balls on both agents on the system bus. For a locked sequence of transactions, LOCK# is asserted from the beginning of the first transaction through the end of the last transaction. When the priority agent asserts BPRI# to arbitrate for bus ownership, it waits until it observes LOCK# deasserted. This enables the processor to retain bus ownership throughout the bus locked operation and guarantee the atomicity of lock.
NMI	I 1.5V Tolerant	The NMI (Non-Maskable Interrupt) indicates that an external interrupt has been generated. NMI becomes the LINT1 signal when the APIC is disabled. Asserting NMI causes an interrupt with an internally supplied vector value of 2. An external interrupt-acknowledge transaction is not generated. If NMI is asserted during the execution of an NMI service routine, it remains pending and is recognized after the IRET is executed by the NMI service routine. At most, one assertion of NMI is held pending. NMI is rising edge sensitive.

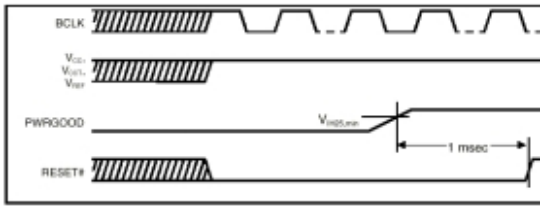
4. PIN DESCRIPTIONS OF MAJOR COMPONENTS

4.1 Pentium III/Celeron FC-PGA2 CPU

Alphabetical Signal Reference

Signal Name	I/O	Signal Description
PICCLK	I 2.5V Tolerant	The PICCLK (APIC Clock) signal is an input clock to the processor and system logic or I/O APIC that is required for operation of the processor, system logic, and I/O APIC components on the APIC bus.
PICD[1:0]	I/O 1.5V Tolerant Open-drain	The PICD[1:0] (APIC Data) signals are used for bi-directional serial message passing on the APIC bus. They must be connected to the appropriate pins/balls of all APIC bus agents, including the processor and the system logic or I/O APIC components. If the PICD0 signal is sampled low on the active-to-inactive transition of the RESET# signal, then the APIC is hardware disabled.
PLL1, PLL2	Analog	The PLL1 and PLL2 signals provide isolated analog decoupling is required for the internal PLL. See Section 3.2.2 for a description of the analog decoupling circuit.
PRDY#	O GTL+	The PRDY# (Probe Ready) signal is a processor output used by debug tools to determine processor debug readiness.
PREQ#	I 1.5V Tolerant	The PREQ# (Probe Request) signal is used by debug tools to request debug operation of the processor.
PWRGOOD	I 2.5V Tolerant	PWRGOOD (Power Good) is a 2.5-V tolerant input. The processor requires this signal to be a clean indication that clocks and the power supplies (Vcc, VccT, etc.) are stable and within their specifications. Clean implies that the signal will remain low, (capable of sinking leakage current) and without glitches, from the time that the power supplies are turned on, until they come within specification. The signal will then transition monotonically to a high (2.5V) state. Figure 26 illustrates the relationship of PWRGOOD to other system signals. PWRGOOD can be driven inactive at any time, but clocks and power must again be stable before the rising edge of PWRGOOD. It must also meet the minimum pulse width specified in Table 17 (Section 3.7) and be followed by a 1 ms RESET# pulse.

PWRGOOD Relationship at Power On



Signal Name	I/O	Signal Description
REQ[4:0]#	I/O GTL+	The REQ[4:0]# (Request Command) signals must be connected to the appropriate pins/balls on both agents on the system bus. They are asserted by the current bus owner when it drives A[35:3]# to define the currently active transaction type.
RESET#	I GTL+	Asserting the RESET# signal resets the processor to a known state and invalidates the L1 and L2 caches without writing back Modified (M state) lines. For a power-on type reset, RESET# must stay active for at least 1 msec after Vcc and BCLK have reached their proper DC and AC specifications and after PWRGOOD has been asserted. When observing active RESET#, all bus agents will deassert their outputs within two clocks. RESET# is the only GTL+ signal that does not have on-die GTL+ termination. A 56.2Ω1% terminating resistor connected to VccT is required. A number of bus signals are sampled at the active-to-inactive transition of RESET# for the power-on configuration. The configuration options are described in Section 4 and in the *Pentium II Processor Developer's Manual*. Unless its outputs are tri-stated during power-on configuration, after an active-to-inactive transition of RESET#, the processor optionally executes its built-in self-test (BIST) and begins program execution at reset-vector 000FFFF0H or FFFFFFF0H. RESET# must be connected to the appropriate pins/balls on both agents on the system bus.
RP#	I/O GTL+	The RP# (Request Parity) signal is driven by the request initiator and provides parity protection on ADS# and REQ[4:0]#. RP# should be connected to the appropriate pins/balls on both agents on the system bus. A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. This definition allows parity to be high when all covered signals are high.
RS[2:0]#	I GTL+	The RS[2:0]# (Response Status) signals are driven by the response agent (the agent responsible for completion of the current transaction) and must be connected to the appropriate pins/balls on both agents on the system bus.

4. PIN DESCRIPTIONS OF MAJOR COMPONENTS

4.1 Pentium III/Celeron FC-PGA2 CPU

PWRGOOD Relationship at Power On

Signal Name	I/O	Signal Description
RSP#	I GTL+	The RSP# (Response Parity) signal is driven by the response agent (the agent responsible for completion of the current transaction) during assertion of RS[2:0]#. RSP# provides parity protection for RS[2:0]#. RSP# should be connected to the appropriate pins/balls on both agents on the system bus. A correct parity signal is high if an even number of covered signals are low, and it is low if an odd number of covered signals are low. During Idle state of RS[2:0]# (RS[2:0]#=000), RSP# is also high since it is not driven by any agent guaranteeing correct parity.
RSVD	TBD	The RSVD (Reserved) signal is currently unimplemented but is reserved for future use. Leave this signal unconnected. Intel recommends that a routing channel for this signal be allocated.
RTTIMPEDP	Analog	The RTTIMPEDP (RTT Impedance/PMOS) signal is used to configure the on-die GTL+ termination. Connect the RTTIMPEDP signal to VSS with a 56.2-Ω, 1% resistor.
SLP#	I 1.5V Tolerant	The SLP# (Sleep) signal, when asserted in the Stop Grant state, causes the processor to enter the Sleep state. During the Sleep state, the processor stops providing internal clock signals to all units, leaving only the Phase-Locked Loop (PLL) still running. The processor will not recognize snoop and interrupts in the Sleep state. The processor will only recognize changes in the SLP#, STPCLK# and RESET# signals while in the Sleep state. If SLP# is deasserted, the processor exits Sleep state and returns to the Stop Grant state in which it restarts its internal clock to the bus and APIC processor units.
SMI#	I 1.5V Tolerant	The SMI# (System Management Interrupt) is asserted asynchronously by system logic. On accepting a System Management Interrupt, the processor saves the current state and enters System Management Mode (SMM). An SMI Acknowledge transaction is issued, and the processor begins program execution from the SMM handler.
STPCLK#	I 1.5V Tolerant	The STPCLK# (Stop Clock) signal, when asserted, causes the processor to enter a low-power Stop Grant state. The processor issues a Stop Grant Acknowledge special transaction and stops providing internal clock signals to all units except the bus and APIC units. The processor continues to snoop bus transactions and service interrupts while in the Stop Grant state. When STPCLK# is deasserted, the processor restarts its internal clock to all units and resumes execution. The assertion of STPCLK# has no affect on the bus clock.
TCK	I 1.5V Tolerant	The TCK (Test Clock) signal provides the clock input for the test bus (also known as the test access port).

Signal Name	I/O	Signal Description
TDI	I 1.5V Tolerant	The TDI (Test Data In) signal transfers serial test data to the processor. TDI provides the serial input needed for JTAG support.
TDO	O 1.5V Tolerant Open-drain	The TDO (Test Data Out) signal transfers serial test data from the processor. TDO provides the serial output needed for JTAG support.
TESTHI	I 1.5V Tolerant	The TESTHI (Test input High) is used during processor test and needs to be pulled high during normal operation.
TESTLO[2:1]	I 1.5V Tolerant	The TESTLO[2:1] (Test input Low) signals are used during processor test and needs to be pulled to ground during normal operation.
TESTP	Analog	The TESTP (Test Point) signals are connected to Vcc and Vss at opposite ends of the die. These signals can be used to monitor the Vcc level on the die. Route the TESTP signals to test points or leave them unconnected. Do not short the TESTP signals together.
THERMDA, THERMDC	Analog	The THERMDA (Thermal Diode Anode) and THERMDC (Thermal Diode Cathode) signals connect to the anode and cathode of the on-die thermal diode.
TMS	I 1.5V Tolerant	The TMS (Test Mode Select) signal is a JTAG support signal used by debug tools.
TRDY#	I GTL+	The TRDY# (Target Ready) signal is asserted by the target to indicate that the target is ready to receive write or implicit write-back data transfer. TRDY# must be connected to the appropriate pins/balls on both agents on the system bus.
TRST#	I 1.5V Tolerant	The TRST# (Test Reset) signal resets the Test Access Port (TAP) logic. The mobile Pentium III processors do not self-reset during power on; therefore, it is necessary to drive this signal low during power-on reset.

4. PIN DESCRIPTIONS OF MAJOR COMPONENTS

4.1 Pentium III/Celeron FC-PGA2 CPU

PWRGOOD Relationship at Power On

Signal Name	I/O	Signal Description
VID[4:0]	O - Open-drain	The VID[4:0] (Voltage ID) pins/balls can be used to support automatic selection of power supply voltages. These pins/balls are not signals, they are either an open circuit or a short to VSS on the processor substrate. The combination of opens and shorts encodes the voltage required by the processor. External to pull-ups are required to sense the encoded VID. For processors that have Intel SpeedStep technology enabled, VID[4:0] encode the voltage required in the battery-optimized mode. VID[4:0] are needed to cleanly support voltage specification changes on mobile Pentium III processors. The voltage encoded by VID[4:0] is defined in Table 39. A "1" in this table refers to an open pin/ball and a "0" refers to a short to VSS. The power supply must provide the requested voltage or disable itself. Please note that in order to implement VID on the BGA2 package, some VID[4:0] balls may be depopulated. For the BGA2 package, a "1" in Table 39 implies that the corresponding VID ball is depopulated, while a "0" implies that the corresponding VID ball is not depopulated. But on the Micro-PGA2 package, VID[4:0] pins are not depopulated.

4. Pin Descriptions Of Major Components

4.2 SiS630 Slot 1/Socket 370 2D/3D Ultra-AGP™ Single Chipset

Host Bus Interface

Name	Tolerance	Power Plane	Type Attr	Description
CPUCLK	3.3V/5V	MAIN	I	**Host Clock :**
ADS#	1.5V	MAIN	I/O GTL+	**Address Strobe :** Address Strobe is driven by CPU to indicate the start of a CPU bus cycle.
HREQ[4:0]#	1.5V	MAIN	I/O GTL+	**Request Command:** HREQ[4:0]# are used to define each transaction type during the clock when ADS# is asserted and the clock after ADS# is asserted.
BREQ0#	1.5V	MAIN	O GTL+	**Symmetric Agent Bus Request:** BREQ0# is driven by the symmetric agent to request for the bus.
BNR#	1.5V	MAIN	I/O GTL+	**Block Next Request:** This signal can be driven asserted by any bus agent to block further requests being pipelined.
HLOCK#	1.5V	MAIN	I GTL+	**Host Lock :** CPU asserts HLOCK# to indicate the current bus cycle is locked.
HIT#	1.5V	MAIN	I/O GTL+	**Keeping a Non-Modified Cache Line:**
HITM#	1.5V	MAIN	I/O GTL+	**Hits a Modified Cache Line:** Hit Modified indicates the snoop cycle hits a modified line in the L1 cache of CPU.
DEFER#	1.5V	MAIN	O GTL+	**Defer Transaction Completion:** SiS630 will use this signal to indicate a retry response to host bus.
RS[2:0]#	1.5V	MAIN	O GTL+	**Response Status:** RS[2:0]# are driven by the response agent to indicate the transaction response type. The following shows the response type. **RS[2:0] Response** 000 Idle State 100 Reserved 001 Retry 101 No data 010 Reserved 110 Implicit Write-back 011 Reserved 111 Normal Data
HTRDY#	1.5V	MAIN	I/O GTL+	**Target Ready:** During write cycles, response agent will drive TRDY# to indicate the agent is ready to accept data.
DRDY#	1.5V	MAIN	I/O GTL+	**Data Ready:** DRDY# is driven by the bus owner whenever the data is valid on the bus.
DBSY#	1.5V	MAIN	I/O GTL+	**Data Bus Busy:** Whenever the data is not valid on the bus with DRDY# is deserted, DBSY# is asserted to hold the bus.

Name	Tolerance	Power Plane	Type Attr	Description
BPRI#	1.5V	MAIN	O GTL+	**Priority Agent Bus Request:** BPRI# is driven by the priority agent that wants to request the bus. BPRI# has higher priority than BREQ0# to access a bus.
CPURST#	1.5V	MAIN	O GTL+	**Host Bus Reset:** CPURST# is used to keep all the bus agents in the same initial state before valid cycles issued.
HA[31:3]#	1.5V	MAIN	I/O GTL+	**Host Address Bus :**
HD[63:0]#	1.5V	MAIN	I/O GTL+	**Host Data Bus :**
FERR#	1.5V~5V	MAIN	I	**Floating Point Error :** CPU will assert this signal upon a floating point error occurring.
IGNE#	1.5V~5V	MAIN	OD	**Ignore Numeric Error :** IGNE# is asserted to inform CPU to ignore a numeric error. **Speed Trap for PII :** This pin will be forced to voltage level according to the input value of MD41 or APC0h.4 during system reset period.
NMI	1.5V~5V	MAIN	OD	**Non-Maskable Interrupt :** A rising edge on NMI will trigger a non-maskable interrupt to CPU. Speed Trap for PII : This pin will be forced to voltage level according to the input value of MD44 or APC0h.7 during system reset period.
INTR	1.5V~5V	MAIN	OD	**Interrupt Request :** High-level voltage of this signal indicates the CPU that there is outstanding interrupt(s) needed to be serviced. **Speed Trap for PII :** This pin will be forced to voltage level according to the input value of MD43 or APC0h.6 during system reset period.
CPUSLP#	1.5V~5V	MAIN	OD	**CPU Sleep :** SiS630 can optionally assert CPUSLP# to force the CPU into deep sleep mode when going to S2 state.
STPCLK#	1.5V~5V	MAIN	OD	**Stop Clock :** STPCLK# will be asserted to inhibit or throttle CPU activities upon a pre-defined power management event occurs.
SMI#	1.5V~5V	MAIN	OD	**System Management Interrupt :** SMI# will be asserted when a pre-defined power management event occurs.

4. Pin Descriptions Of Major Components

4.2 SiS630 Slot 1/Socket 370 2D/3D Ultra-AGP™ Single Chipset

Host Bus Interface

Name	Tolerance	Power Plane	Type Attr	Description
INIT#	1.5V~5V	MAIN	OD	**Initialization :** INIT is used to re-start the CPU without flushing its internal caches and registers. In Pentium II platform it is active high. This signal requires an external pull-up resistor tied to 3.3V.
A20M#	1.5V~5V	MAIN	OD	**Address 20 Mask :** When A20M# is asserted, the CPU A20 signal will be forced to "0". **Speed Trap for PII :** This pin will be forced to voltage level according to the input value of MD42 or APC0h.5 during system reset period.

DRAM Controller

Name	Tolerance	Power Plane	Type Attr	Description
SDCLK	3.3V/5V	MAIN	I	SDRAM Clock Input
MD[63:0]	3.3V	MAIN	I/O	System Memory Data Bus
MA[14:0]	3.3V	MAIN	O	System Memory Address Bus
CSA[5:0]#	3.3V	MAIN	O	SDRAM Chip Select
CSB[5:0]#	3.3V	MAIN	O	SDRAM Chip Select Signals (Duplicated Copy)
DQM[7:0]#	3.3V	MAIN	O	SDRAM Input/Output Data Mask
WE#	3.3V	MAIN	O	SDRAM Write Enable
SRAS#	3.3V	MAIN	O	SDRAM Row Address Strobe
SCAS#	3.3V	MAIN	O	SDRAM Column Address Strobe
CKE	3.3V	AUX	O	SDRAM Clock Enable During Suspend-to-DRAM mode (ACPI S2 or S3 state), SDRAM can be put into self-refresh mode by asserting CKE.

PCI Interface

Name	Tolerance	Power Plane	Type Attr	Description
PCICLK	3.3V/5V	MAIN	I	**PCI Clock :** The PCICLK input provides the fundamental timing and the internal operating frequency for the SiS Chip. It runs at the same frequency and skew of the PCI local bus.
C/BE[3:0]#	3.3V/5V	MAIN	I/O	**PCI Bus Command and Byte Enables:** PCI Bus Command and Byte Enables define the PCI command during the address phase of a PCI cycle, and the PCI byte enables during the data phases. C/BE[3:0]# are outputs when the SiS Chip is a PCI bus master and inputs when it is a PCI slave.
AD[31:0]	3.3V/5V	MAIN	I/O	**PCI Address /Data Bus:** In address phase: 1.When the SiS Chip is a PCI bus master, AD[31:0] are output signals. 2.When the SiS Chip is a PCI target, AD[31:0] are input signals. In data phase: 1.When the SiS Chip is a target of a memory read/write cycle, AD[31:0] are floating. 2.When the SiS Chip is a target of a configuration or an I/O cycle, AD[31:0] are output signals in a read cycle, and input signals in a write cycle.
PAR	3.3V/5V	MAIN	I/O	**Parity :** SiS630 drives out Even Parity covering AD[31:0] and C/BE[3:0]#. It does not check the input parity signal.
FRAME#	3.3V/5V	MAIN	I/O	**Frame#:** FRAME# is an output when the SiS Chip is a PCI bus master. The SiS Chip drives FRAME# to indicate the beginning and duration of an access. When the SiS Chip is a PCI slave device, FRAME# is an input signal.
IRDY#	3.3V/5V	MAIN	I/O	**Initiator Ready :** IRDY# is an output when the SiS Chip is a PCI bus master. The assertion of IRDY# indicates the current PCI bus master's ability to complete the current data phase of the transaction. For a read cycle, IRDY# indicates that the PCI bus master is prepared to accept the read data on the following rising edge of the PCI clock. For a write cycle, IRDY# indicates that the bus master has driven valid data on the PCI bus. When the SiS Chip is a PCI slave, IRDY# is an input pin.
TRDY#	3.3V/5V	MAIN	I/O	**Target Ready :** TRDY# is an output when the SiS Chip is a PCI slave. The assertion of TRDY# indicates the target agent's ability to complete the current data phase of the transaction. For a read cycle, TRDY# indicates that the target has driven valid data onto the PCI bus. For a write cycle, TRDY# indicates that the target is prepared to accept data from the PCI bus. When the SiS Chip is a PCI master, it is an input pin.

4. Pin Descriptions Of Major Components

4.2 SiS630 Slot 1/Socket 370 2D/3D Ultra-AGP™ Single Chipset

PCI Interface

Name	Tolerance	Power Plane	Type Attr	Description
STOP#	3.3V/5V	MAIN	I/O	**Stop# :** STOP# indicates that the bus master must start terminating its current PCI bus cycle at the next clock edge and release control of the PCI bus. STOP# is used for disconnection, retry, and target-abortion sequences on the PCI bus.
DEVSEL#	3.3V/5V	MAIN	I/O	**Device Select :** As a PCI target, SiS Chip asserts DEVSEL# by doing positive or subtractive decoding. SiS Chip positively asserts DEVSEL# when the DRAM address is being accessed by a PCI master, PCI configuration registers or embedded controllers' registers are being addressed, or the BIOS memory space is being accessed. The low 16K I/O space and low 16M memory space are responded subtractively. The DEVESEL# is an input pin when SiS Chip is acting as a PCI master. It is asserted by the addressed agent to claim the current transaction.
PLOCK#	3.3V/5V	MAIN	I/O	**PCI Lock :** When PLOCK# is sampled asserted at the beginning of a PCI cycle, SiS630 considers itself being locked and remains in the locked state until PLOCK# is sampled and negated at the following PCI cycle.
PREQ[2:0]#	3.3V/5V	MAIN	I	**PCI Bus Request :** PCI Bus Master Request Signals
PGNT[2:0]#	3.3V	MAIN	O	**PCI Bus Grant :** PCI Bus Master Grant Signals
INT[A:D]#	3.3V/5V	MAIN	I	**PCI interrupt A,B,C,D :** The PCI interrupts will be connected to the inputs of the internal Interrupt controller through the rerouting logic associated with each PCI interrupt.
PCIRST#	3.3V	AUX	O	**PCI Bus Reset :** PCIRST# will be asserted during the period when PWROK is low, and will be kept on asserting until about 24ms after PWROK goes high.
SERR#	3.3V/5V	MAIN	I	**System Error :** When sampled active low, a non-maskable interrupt (NMI) can be generated to CPU if enabled.

PCI IDE Interface

Name	Tolerance	Power Plane	Type Attr	Description
IDA[15:0]	3.3V/5V	MAIN	I/O	Primary Channel Data Bus
IDB[15:0]	3.3V/5V	MAIN	I/O	Secondary Channel Data Bus
IDECSA[1:0]#	3.3V	MAIN	O	Primary Channel CS[1:0]
IDECSB[1:0]#	3.3V	MAIN	O	Secondary Channel CS[1:0]
IIOR[A:B]#	3.3V	MAIN	O	Primary/Secondary Channel IOR# Signals
IIOW[A:B]#	3.3V	MAIN	O	Primary/Secondary Channel IOW# Signals
ICHRDY[A:B]	3.3V/5V	MAIN	I	Primary/Secondary Channel ICHRDY# Signals
IDREQ[A:B]	3.3V/5V	MAIN	I	Primary/Secondary Channel DMA Request Signals
IDACK[A:B]#	3.3V	MAIN	O	Primary/Secondary Channel DMACK# Signals
IIRQ[A:B]	3.3V/5V	MAIN	I	Primary/Secondary Channel Interrupt Signals
IDSAA[2:0]	3.3V	MAIN	O	Primary Channel Address [2:0]
IDSAB[2:0]	3.3V	MAIN	O	Secondary Channel Address [2:0]
CBLID[A:B]	3.3V/5V	MAIN	I	Primary/Secondary Ultra-66 Cable ID

VGA Interface

Name	Tolerance	Power Plane	Type Attr	Description
HSYNC	3.3V	MAIN	O	Horizontal Sync
VSYNC	3.3V	MAIN	O	Vertical Sync
SSYNC	3.3V	MAIN	O	Stereo Sync
DDCCLK	3.3V/5V	MAIN	I/O	Display Data Channel Clock Line
DDCDATA	3.3V/5V	MAIN	I/O	Display Data Channel Data Line
COMP		MAIN	AI	**Compensation Pin:** Connect this pin to AVDD via a 0.1uF capacitor
RSET		MAIN	AI	**Reference Resistor:** An external resistor is connected between the RSET pin and AGND to control the magnitude of the full-scale current.
VREF		MAIN	AI	**Voltage Reference:** Connect 0.1uF Capacitor to Ground.
VCS#	3.3V	MAIN	I/O	VGA Frame Buffer Cache Chip Select
ROUT		MAIN	AO	Red Signal Output
GOUT		MAIN	AO	Green Signal Output
BOUT		MAIN	AO	Blue Signal Output
VBA1 **VBCLK** **PLPWDN#**	3.3V	MAIN	O I/O O	**Display Memory Bank Select:** When 128bits DRAM interface enable, it represents the Memory Bank Select **Digital Video Clock Input:** When Video Bridge connected, it represents the Digital Video Clock Input **Panel Power Down** When external LCD transmitter connected, it represents power down.

4. Pin Descriptions Of Major Components

4.2 SiS630 Slot 1/Socket 370 2D/3D Ultra-AGP™ Single Chipset

VGA Interface

Name	Tolerance	Power Plane	Type Attr	Description
VMA11 **VGCLK**	3.3V	MAIN	O O	**Display Memory Address bit 11 :** When 128bits DRAM interface enable, it represents the Memory Address bit 11 **Digital Video Clock Output:** When Video Bridge connected, it represents the Digital Video Clock Output
VMA10 **VBHCLK**	3.3V	MAIN	O O	**Display Memory Address bit 10:** When 128bits DRAM interface enable, it represents the Memory Address bit 10 **Control Clock Output:** When Video Bridge connected, it represents the Control Clock Output
VMD[63:60]	3.3V	MAIN	I/O	Display Memory Data Bus bits [63:60]
VMD[59:52] **VBRGB[7:0]**	3.3V	MAIN	I/O O	Display Memory Data Bus bits [59:52] Digital Video Data bits [7:0]
VMD[51:49] **VBRGB[18:16]**	3.3V	MAIN	I/O O	Display Memory Data Bus bits [51:49] Digital Video Data bits [18:16]
VMD[48:44] **VBRGB[19:23]**	3.3V	MAIN	I/O O	Display Memory Data Bus bits [48:44] Digital Video Data bits [19:23]
VMD[43:42] **VBRGB[10:11]**	3.3V	MAIN	I/O O	Display Memory Data Bus bits [43:42] Digital Video Data bits [10:11]
VMD[41:40] **VBRGB[9:8]]**	3.3V	MAIN	I/O O	Display Memory Data Bus bits [41:40] Digital Video Data bits [9:8]
VMD[39:38] **VBRGB[13:12]**	3.3V	MAIN	I/O O	Display Memory Data Bus bits [39:38] Digital Video Data bits [13:12]
VMD[37:36] **VBRGB[14:15]**	3.3V	MAIN	I/O O	Display Memory Data Bus bits [37:36] Digital Video Data bits [14:15]
VMD35 **VBBLANKN**	3.3V	MAIN	I/O O	Display Memory Data Bus bit 35 Digital Video Display Enable
VMD[34:33] **TVCTL[0:1]**	3.3V	MAIN	I/O O	Display Memory Data Bus bits [34:33] Video Bridge Data Control bits [0:1]
VMD32 **VBCAD**	3.3V	MAIN	I/O I/O	Display Memory Data Bus bit 32 Video Bridge Programming Control
VMD31 **VBHSYNC**	3.3V	MAIN	I/O I/O	Display Memory Data Bus bit 31 Digital Video Horizontal Sync
VMD30 **VBVSYNC**	3.3V	MAIN	I/O I/O	Display Memory Data Bus bit 30 Digital Video Vertical Sync
VMD29 **DDC2CLK**	3.3V	MAIN	I/O I/O	Display Memory Data Bus bit 29 Second Display data channel clock line
VMD28 **DDC2DATA**	3.3V	MAIN	I/O I/O	Display Memory Data Bus bit 28 Second Display data channel data line
VMD[27:0]	3.3V	MAIN	I/O	Display Memory Data Bus bits [27:0]

Name	Tolerance	Power Plane	Type Attr	Description
VDQM[7:0]	3.3V	MAIN	O	Display Memory SDRAM Input /Output Mask
OSCI	3.3V/5V	MAIN	I	External 14.318MHz Clock Input
ENTEST	3.3V/5V	MAIN	I	Test Mode Enable

Power management Interface

Name	Tolerance	Power Plane	Type Attr	Description
ACPILED	<=5V	AUX	OD	**ACPILED :** ACPILED can be used to control the blinking of an LED at the frequency of 1 Hz to indicate the system is at power saving mode.
EXTSMI#	3.3V/5V	MAIN	I	**External SMI#:** EXTSMI# can be used to generate wakeup event, sleep event, or SCI/SMI#/GPEIRQ event to the ACPI-compatible power management unit.
PME#	3.3V/5V	AUX	I/O	**PME# :** When the system is in power-down mode, an active low event on PME# will cause the PSON# to go low and hence turn on the power supply. When the system is in suspend mode, an active PME# event will cause the system wakeup and generate an SCI/SMI#/GPEIRQ.
PSON#	<=5V	AUX	OD	**ATX Power ON/OFF control:** PSON# is used to control the on/off state of the ATX power supply. When the ATX power supply is in the OFF state, an activated power-on event will force the power supply to ON state.
PWRBTN#	3.3V/5V	AUX	I	**Power Button:** This signal is from the power button switch and will be monitored by the ACPI- mpatible power management unit to switch the system between working and sleeping states.
RING	3.3V/5V	AUX	I	**Ring Indication :** An active RING pulse and lasting for more than 4ms will cause a wakeup event for system to wake from S1~S5.

4. Pin Descriptions Of Major Components

4.2 SiS630 Slot 1/Socket 370 2D/3D Ultra-AGP™ Single Chipset

Power management Interface

Name	Tolerance	Power Plane	Type Attr	Description
THERM#	3.3V/5V	MAIN	I	**Thermal Detect :** THERM# is connected to the internal ACPI-compatible power management unit as an indication of outstanding thermal event. An active THERM# event can be used to generate SCI/SMI#/GPEIRQ. If THERM# is activated for more than 2 second, a thermal override event will occur and the system will enter CPU thermal throttling mode automatically.
GPIO[6:4]	3.3V/5V	AUX	I/O/OD	General Purpose Input/Output [6:4]: Refer to GPIO description.

SMBus Interface

Name	Tolerance	Power Plane	Type Attr	Description
SMBDAT **I2CDAT**	3.3V/5V	MAIN	I/OD I/OD	**SMBus Data :** SMBus data input/output pin. **I2C Data :** I2C data input/output pin.
SMCLK **I2CCLK**	3.3V/5V	MAIN	I/OD I/OD	**SMBus Clock :** SMBus clock input/output pin. **I2C Clock :** I2C clock input/output pin.
SMBALT# **I2CALT#** **GPIO15**	3.3V/5V	AUX	I/OD I/OD I/O/OD	**SMBus Alert :** This pin is used for SMBus device to wake up the system from sleep state or to generate SCI/SMI#/GPEIRQ. **I2C Alert :** This pin is used for I2C device to wake up the system from sleep state or to generate SCI/SMI#/GPEIRQ. **General Purpose Input/Output 15 :** Refer to GPIO description.

Keyboard controller Interface

Name	Tolerance	Power Plane	Type Attr	Description
KBDAT **GPIO10**	3.3V/5V	AUX	I/OD I/O/OD	**Keyboard Dada :** When the internal keyboard controller is enabled, this pin is used as the keyboard data signal. **General Purpose Input/Output 10 :** Refer to GPIO description.
KBCLK **GPIO11**	3.3V/5V	AUX	I/OD I/O/OD	**Keyboard Clock :** When the internal keyboard controller is enabled, this pin is used as the keyboard clock signal. General Purpose Input/Output 11 : Refer to GPIO description.

Name	Tolerance	Power Plane	Type Attr	Description
PMDAT **GPIO12**	3.3V/5V	AUX	I/OD I/O/OD	**PS2 Mouse Data:** When the internal keyboard and PS2 mouse controllers are enabled, this pin is used as PS2 mouse data signal. **General Purpose Input/Output 12 :** Refer to GPIO description.
PMCLK **GPIO13**	3.3V/5V	AUX	I/OD I/O/OD	**PS2 Mouse Clock:** When the internal keyboard and PS2 mouse controllers are enabled, this pin is used as the PS2 mouse clock signal. **General Purpose Input/Output 13 :** Refer to GPIO description.
KLOCK# **GPIO14**	3.3V/5V	AUX	I I/O/OD	**Keyboard Lock:** When KLOCK# is tied low, the internal keyboard controller will not respond to any key-strikes. **General Purpose Input/Output 14 :** Refer to GPIO description.

LPC Interface

Name	Tolerance	Power Plane	Type Attr	Description
LAD[3:0]	3.3V/5V	MAIN	I/O	**LPC Address/Data Bus :** LPC controller drives these four pins to transmit LPC command, address, and data to LPC device.
LDRQ#	3.3V/5V	MAIN	I	**LPC DMA Request 0:** This pin is used by LPC device to request DMA cycle.
LFRAME#	3.3V	MAIN	O	**LPC Frame :** This pin is used to notify LPC device that a start or a abort LPC cycle will occur.
SIRQ	3.3V/5V	MAIN	I/OD	**Serial IRQ :** This signal is used as the serial IRQ line signal.

4. Pin Descriptions Of Major Components

4.2 SiS630 Slot 1/Socket 370 2D/3D Ultra-AGP™ Single Chipset

RTC Interface

Name	Tolerance	Power Plane	Type Attr	Description
AUXOK	1.8V	RTC	I	**Auxiliary Power OK :** This signal is supplied from the power source of resume well. It is also used to reset the logic in resume power well. If there is no auxiliary power source on the system, this pin should be tied together with PWROK.
BATOK	1.8V	RTC	I	**Battery Power OK:** When the internal RTC is enabled, this signal is used to indicate that the power of RTC well is stable. It is also used to reset the logic in RTC well. If the internal RTC is disabled, this pin should be tied low.
OSC32KHI	1.8V	RTC	I	**RTC 32.768 KHz Input** : When internal RTC is enabled, this pin provides the 32.768 KHz clock signal from external crystal or oscillator.
OSC32KHO	<1.8V	RTC	O	**RTC 32.768 KHz Output :** When internal RTC is enabled, this pin should be connected with the other end of the 32.768 KHz crystal or left unconnected if an oscillator is used.
PWROK	1.8V	RTC	I	**Main Power OK** : A high-level input to this signal indicates the power being supplied to the system is in stable operating state. During the period of PWROK being low, CPURST and PCIRST# will all be asserted until after PWROK goes high for 24 ms.

AC'97 interface

Name	Tolerance	Power Plane	Type Attr	Description
AC_BITCLK	3.3V/5V	MAIN	I	**AC'97Bit Clock :** This signal is a 12.288MHz serial data clock, which is generated by primary Codec.
AC_RESET#	3.3V	AUX	O	**AC'97 Reset :** Hardware reset signal for external Codecs.
AC_SDIN[1:0]	3.3V/5V	AUX	I	**AC'97 Serial Data input :** Serial data input from primary Codec and secondary Codec.
AC_SDOUT	3.3V	MAIN	O	**AC'97 Serial Data output :** Serial data output to Codecs.
AC_SYNC	3.3V	MAIN	O	**AC'97 Syncronization :** This is a 48KHz signal, which is used to syncronize the Codecs.
SPDIF **GPIO7**	3.3V/5V	MAIN	O I/O/OD	**S/PDIF Transmitter Output** **General Purpose Input/Output 7 :** Refer to GPIO description.

Fast Ethernet and Homenetworking interface

Name	Tolerance	Power Plane	Type Attr	Description
EECS	3.3V	AUX	O	**Serial EEPROM Chip Select :** This enables the EEPROM during loading of the Ethernet configuration data.
EEDI	3.3V	AUX	O	**Serial EEPROM Data Input :** During serial EEPROM access cycle, the SiS630 will use this pin to serially write OP codes, addresses and data into the serial EEPROM.
EEDO **GPIO3**	3.3V/5V	AUX	I I/O/OD	**Serial EEPROM Data Output :** During serial EEPROM access cycle, the SiS630 will read the contents of the EEPROM serially through this pin. Requires external pull-up resistor. **General Purpose Input/Output 3 :** Refer to GPIO description.
EESK	3.3V	AUX	O	**Serial EEPROM Clock :** This pin provides the clock for the serial EEPROM.
OSC25MHI	3.3V	AUX	I	**PHY 25MHz Clock Input :** This pin is supplied the 25MHz clock signal input from the external crystal or an oscillator.
PLEDO# **OC3#** **GPIO8**	3.3V	AUX	OD O I/O/OD	**Programmable LED Output :** (A)Select 10/100Mbps LAN Mode: This pin is used as an LINK/ACTIVITY indication output. (B)Select Home Networking Mode: This pin is also an LINK/ACTIVITY indication output. **OC3# :** When this pin is configured as OC3#, it can detects USB Port 3 over current condition. **General Purpose Input/Output 8 :** Refer to GPIO description.
REXT		AUX	I	**Transmit Current Set :** An external resistor connected between this pin and GND will set the output current level for the twisted pair outputs.
TPIP		AUX	I	Twisted Pair Receive Positive Input
TPIN		AUX	I	Twisted Pair Receive Negative Input
TPOP		AUX	O	Twisted Pair Transmit Positive Output
TPON		AUX	O	Twisted Pair Transmit Negative Output
HRTXRXP		AUX	I/O	Twisted Pair Transmit / Receive Positive Data
HRTXRXN		AUX	I/O	Twisted Pair Transmit / Receive Negative Data

4. Pin Descriptions Of Major Components

4.2 SiS630 Slot 1/Socket 370 2D/3D Ultra-AGP™ Single Chipset

USB interface

Name	Tolerance	Power Plane	Type Attr	Description
CLK48M	3.3V/5V	MAIN	I	**USB 48 MHz clock input :** This signal provides the fundamental clock for the USB Controller.
OC0# **PCIREQ3#** **GPIO0**	3.3V/5V	MAIN	I I I/O/OD	**USB Port 0 Over Current Detection :** OC0# is used to detect the over current condition of USB Port 0. **External PCI Master Request 3:** PCIREQ3# is used for PCI Device on PCI Slot 3 to assert its request to hold PCI Bus. **General Purpose Input/Output 0 :** Refer to GPIO description.
OC1# **PCIGNT3#** **GPIO1**	3.3V/5V	MAIN	I O I/O/OD	**USB Port 1 Over Current Detection :** OC1# is used to detect the over current condition of USB Port 1. **External PCI Master Grant 3 :** PCIGNT3# is used to indicate PCI Device on PCI Slot 3 the PCI Bus has been granted. **General Purpose Input/Output 1 :** Refer to GPIO description.
OC3# **LDRQ1#** **GPIO2**	3.3V/5V	MAIN	I I I/O/OD	**USB Port 3 Over Current Detection:** OC3# is used to detect the over current condition of USB Port 3. **LPC DMA Request 1 :** LDRQ1# is the second LPC DMA request signal used by LPC Device to request DMA cycles. **General Purpose Input/Output 2 :** Refer to GPIO description.
USBP[4:0]P	3.3V	AUX	I/O	USB Port [4:0] Positive Input/Output
USBP[4:0]N	3.3V	AUX	I/O	USB Port [4:0] Negative Input/Output

Legacy I/o and Miscellaneous Signals

Name	Tolerance	Power Plane	Type Attr	Description
SPK	3.3V	MAIN	O	**Speaker output :** The SPK is connected to the system speaker.

Power and Ground Signals

Name	Tolerance	Power Plane	Type Attr	Description
VSS		GROUND		0V
IVDD		MAIN		1.8V
IVDD (AUX)		AUX		1.8V
OVDD (AUX)		AUX		3.3V
USBVDD		AUX		3.3V
RTCVDD		RTC		1.8V
DCLKAVDD		MAIN		3.3V
ECLKAVDD		MAIN		3.3V
TXAVDD		AUX		3.3V
RXAVDD		AUX		3.3V
DACAVDD		MAIN		3.3V
IDEAVDD		MAIN		1.8V
SDAVDD		MAIN		3.3V
CPUAVDD		MAIN		3.3V
VTTB		MAIN		1.5V
VSSQ		GROUND		0V
VTTA		MAIN		1.5V
VCC3		MAIN		3.3V

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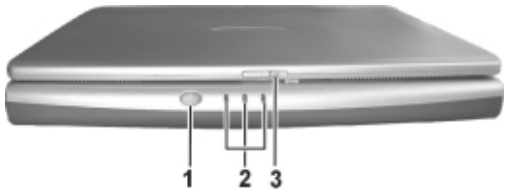
5 System View and Disassembly

5.1 System View

5.1.1 Front View

❶ Mail-Received Button/Indicator
❷ Power Indicators
❸ Top Cover Latch



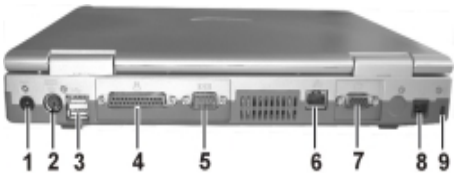
5.1.2 Left-Side View

❶ Audio Input Connector
❷ Microphone Connector
❸ Audio Output Connector
❹ Volume Control
❺ PC Card Slots
❻ Floppy Disk Drive

5.1.3 Right-Side View

❶ Battery Pack
❷ CD-ROM/DVD-ROM Drive
❸ IR Port

5.1.4 Rear View



❶ Power Connector
❷ PS/2 Port
❸ USB Ports
❹ Parallel Port
❺ Serial Port
❻ RJ-45 Connector
❼ VGA Port
❽ RJ-11 Connector
❾ Kensington Lock

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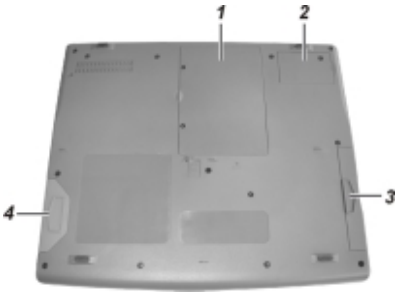
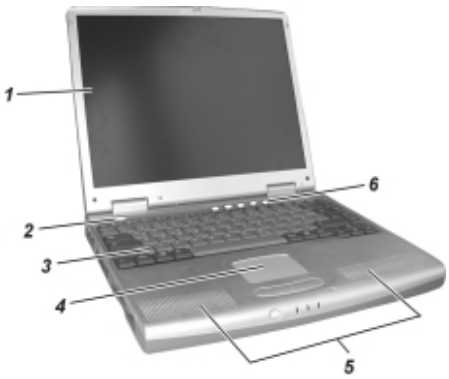
5.1.5 Bottom View



❶ CPU Cover
❷ Modem Card Cover
❸ FDD/HDD Module
❹ Battery Pack

5.1.6 Top-Open View

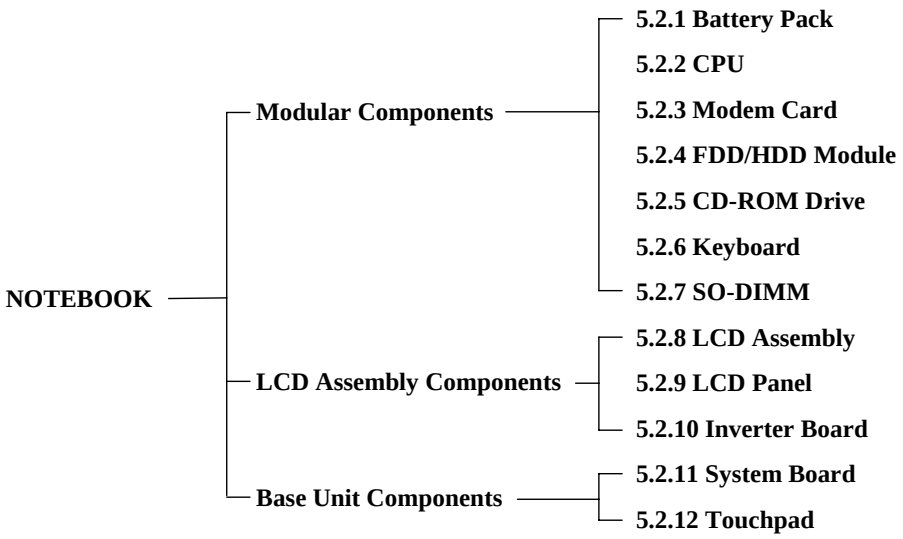


❶ LCD Screen
❷ Power Button
❸ Keyboard
❹ Touchpad
❺ Stereo Speaker Set
❻ Easy Start Buttons

5.2 System Disassembly

The section discusses at length each major component for disassembly/reassembly and show corresponding illustrations. Use the chart below to determine the disassembly sequence for removing components from the notebook.

NOTE: *Before you start to install/replace these modules, disconnect all peripheral devices and make sure the notebook is not turned on or connected to AC power.*



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5.2.1 Battery Pack

Disassembly

1. Carefully put the notebook upside down.
2. Turn the locking button to the "unlock" (🔓) position (❶), then slide and hold the latch in the unlock position and pull the battery pack out of the compartment (❷).(figure 5-1)

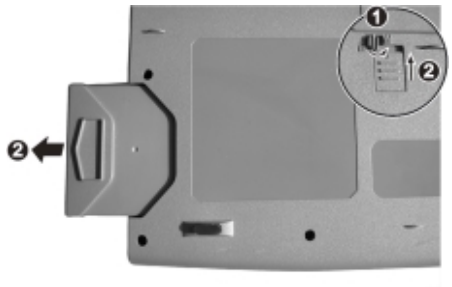


Figure 5-1

Reassembly

1. Push the battery pack into the compartment. The battery pack should be correctly connected when you hear a clicking sound.
2. Turn the locking button to the "lock" (🔒) position.

5.2.2 CPU

Disassembly

1. Carefully put the notebook upside down.
2. Remove two screws locking the CPU compartment cover, and then lift the cover up. (figure 5-2)

Figure 5-2

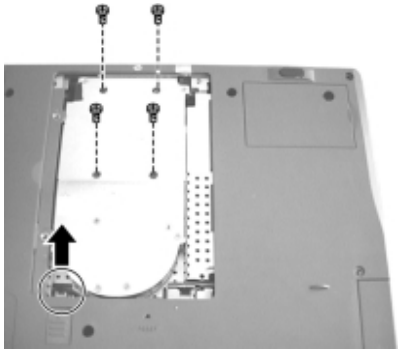


Figure 5-3

3. Remove four screws fastening the heatsink and disconnect the fan's power cord to free the heatsink from the CPU module. (figure 5-3)

4. Insert a minus screwdriver 101 (JIS standard) into the “OPEN” hole of the socket, and push the screwdriver toward the CPU to free the CPU. Now you can take out the CPU from the socket. (figure 5-4)

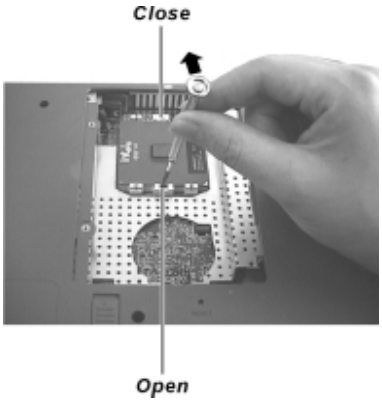


Figure 5-4

Reassembly

1. Align the arrowhead corner of the CPU with the beveled corner of the socket, and insert the CPU pins into the holes. Insert the flat screwdriver into the “CLOSE” hole of the socket, and push the screwdriver toward the CPU to secure the CPU in place.
2. Connect the fan’s power cord to the system board, fit the heatsink onto the top of the CPU and secure with four screws.
3. Replace the CPU compartment cover and secure with two screws.

5.2.3 Modem Card

Disassembly

1. Carefully put the notebook upside down.
2. Remove one screw locking the modem card compartment cover, and then lift the cover up. (figure 5-5)

Figure 5-5

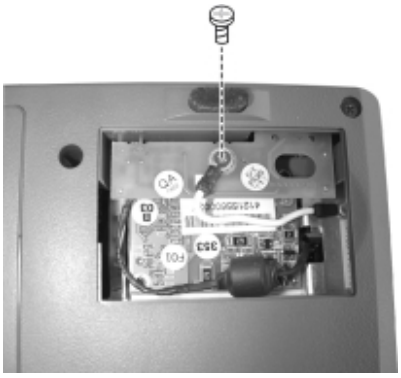


Figure 5-6

3. Remove one screw fastening the connector board and the grounding cable. (figure 5-6)

4. Slightly lift up the connector board, and then remove one screw fastening the modem card. Now you can take out the modem card from the compartment. (figure 5-7)

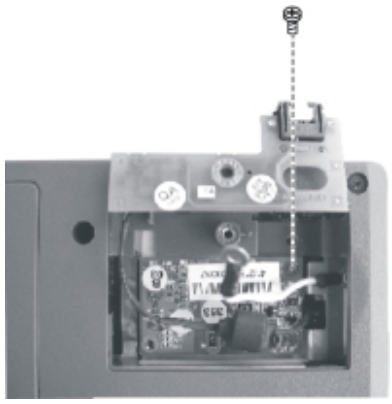


Figure 5-7

Reassembly

1. Reconnect the modem card into the system board and secure with two screws.
2. Hold the connector board an angle so that the phone line connector is pointed towards the opening on the notebook. Insert the connector into the opening and secure with a screw which fastening both the connector board and the grounding cable.
3. Replace the compartment cover and secure with one screw.

5.2.4 FDD/HDD Module

Disassembly

1. Carefully put the notebook upside down.
2. Remove one screw and slide the FDD/HDD module out of the compartment. (figure 5-8)

Figure 5-8

3. To take the hard disk drive apart, remove two screws of the hard disk. Then lift the hard disk up and unplug the connector to remove it. (figure 5-9)

Figure 5-9

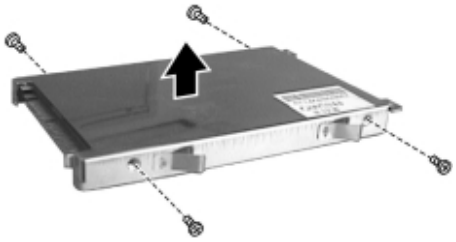


Figure 5-10

4. Remove four screws to separate the hard disk drive from the metal shield. (figure 5-10)

Reassembly

1. To install the hard disk drive, place it in the bracket and secure with four screws.
2. Connect the hard disk to the connector on the FDD/HDD module and secure with two screws.
3. Slide the FDD/HDD module into the compartment and secure with one screw.

5.2.5 CD-ROM Drive

Disassembly

1. Carefully put the notebook upside down.
2. Remove the battery pack. (See section 5.2.1 Disassembly.)
3. Remove the modem card. (See section 5.2.3 Disassembly.)
4. Remove the FDD/HDD module. (See step 2 in section 5.2.4 Disassembly.)
5. Remove one screw locking the CD-ROM (❶), and then the other twelve screws locking the base unit frame. (figure 5-11) Now you can lift the base unit frame up.

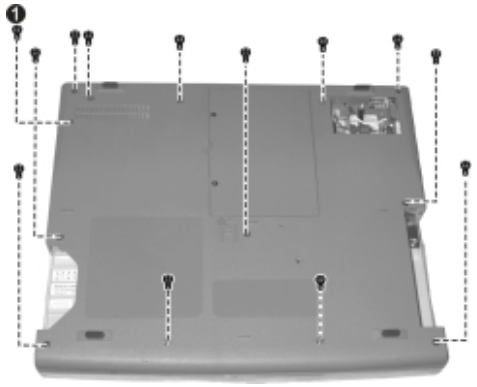


Figure 5-11

6. Hold the CD-ROM drive and slide it outward carefully. (figure 5-12).

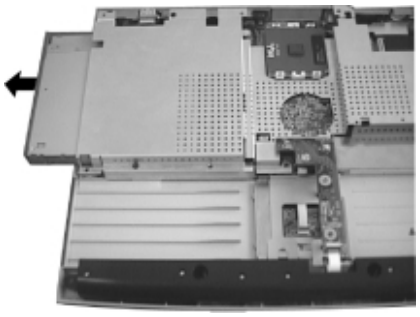


Figure 5-12

Reassembly

1. Push the CD-ROM drive into the compartment.
2. Replace the base unit frame and secure with thirteen screws (includes one locking the CD-ROM drive).
3. Replace the FDD/HDD module. (See section 5.2.4 Reassembly.)
4. Replace the modem card. (See section 5.2.3 Reassembly.)
5. Replace the modem card. (See section 5.2.3 Reassembly.)
6. Replace the battery pack. (See section 5.2.1 Reassembly.)

5.2.6 Keyboard

Disassembly

1. Open the top cover.
2. Press the locking latch downward to unlatch the Easy Start panel (❶) , push it leftward and lift it up from the left side (❷). (figure 5-13)

Figure 5-13

Figure 5-14

3. Slightly lift up the keyboard and disconnect the cable from the system board to detach the keyboard.

Reassembly

1. Reconnect the keyboard cable and fit the keyboard back into place.
2. Replace the Easy Start panel.

5.2.7 SO-DIMM

Disassembly

1. Remove the keyboard to access the SO-DIMM sockets. (See section 5.2.6 Disassembly.)
2. Pull the retaining clips outwards (❶) and remove the SO-DIMM (❷). (figure 5-15)

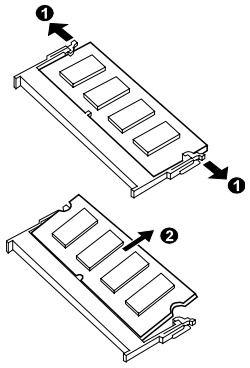


Figure 5-15

Reassembly

1. To install the SO-DIMM, match the SO-DIMM's notched part with the socket's projected part and firmly insert the SO-DIMM into the socket at 20-degree angle. Then push down until the retaining clips lock the SO-DIMM into position.
2. Replace the keyboard and the Easy Start panel. (See section 5.2.6 Reassembly.)

5.2.8 LCD Assembly

Disassembly

1. Open the top cover and remove the Easy Start panel. (See steps 1 to 2 in section 5.2.6 Disassembly.)
2. Remove the two hinge covers by inserting a flat screwdriver to the rear of the cover and pry the cover out. (figure 5-16)

Figure 5-16

Figure 5-17

3. Open the top cover. Unplug the three cable connectors coming from the LCD assembly, and remove four screws of the hinges. Now you can separate the LCD assembly from the base unit. (figure 5-17)

Reassembly

1. Attach the LCD assembly to the base unit and secure with four screws on the hinges.
2. Reconnect the LCD cable connectors to the system board.
3. Replace the two hinge covers.
4. Replace the Easy Start panel.

5.2.9 LCD Panel

Disassembly

1. Remove the LCD assembly. (See section 5.2.8 Disassembly.)
2. Remove the two rubber pads and two screws on the lower part of the panel. (figure 5-18)

Figure 5-18

Figure 5-19

3. Insert a flat screwdriver to the lower part of the frame and gently pry the frame out. Repeat the process until the frame is completely separated from the housing.
4. Remove the four screws on the two sides of the LCD panel, and unplug the cable from the inverter board. (figure 5-19)

Reassembly

1. Fit the LCD panel back into place and secure with four screws, and reconnect the cable to the inverter board.
2. Fit the LCD frame back into the housing and replace the two screws and two rubber pads.
3. Replace the LCD assembly. (See section 5.2.8 Reassembly.)

5.2.10 Inverter Board

Disassembly

1. Remove the LCD assembly and detach the LCD frame (see instructions in previous two sections).
2. To remove the inverter board at the bottom side of the LCD assembly, unplug the cable and remove the two screws. (figure 5-20)

Figure 5-20

Reassembly

1. Fit the inverter board back into place and secure with two screws.
2. Reconnect the cables.
3. Replace the LCD frame. (See section 5.2.9 Reassembly.)
4. Replace the LCD assembly. (See section 5.2.8 Reassembly.)

5.2.11 System Board

Disassembly

1. Remove the Keyboard. (See section 5.2.6 Disassembly.)
2. Remove the LCD assembly. (See section 5.2.8 Disassembly.)
3. Remove seven screws, and then take out the Easy Start board. (figure 5-21)

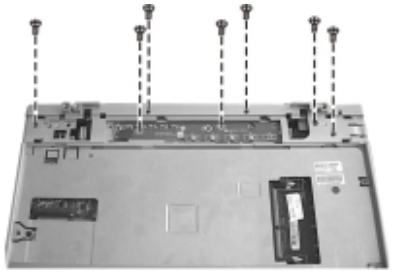


Figure 5-21

Figure 5-22

4. Remove four screws on the rear side of the notebook. (figure 5-22)
5. Remove the battery pack, heatsink, modem card, FDD/HDD module, and CD-ROM drive. (See section 5.2.1 to 5.2.5 Disassembly.)

6. Remove six screws and two hexnut screws fastening the metal shield, and then lift the shield up from the system board carefully. (figure 5-23)

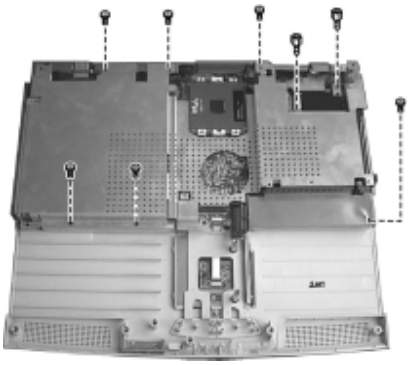


Figure 5-23

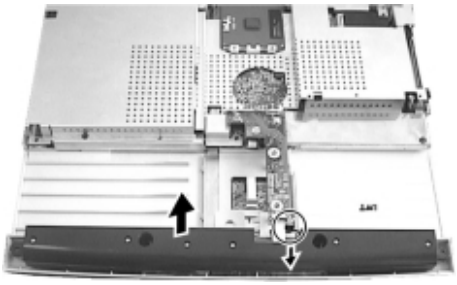


Figure 5-24

7. Lift up the speaker assembly and disconnect the cable. (figure 5-24)

8. Remove four screws to take the recharge board apart. (figure 5-25)

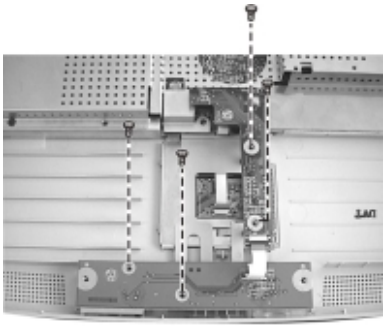


Figure 5-25

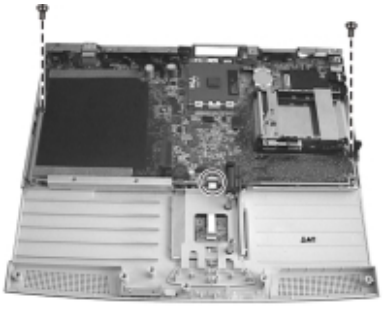


Figure 5-26

9. Remove two screws fastening the system board and disconnect the cable of the touchpad. Now you can lift the system board up from the base unit. (figure 5-26)

Reassembly

1. Fit the system board into place and secure with two screws.
2. Reconnect the touchpad's cable.
3. Replace the metal shield and secure with six screws and two hexnut screws.
4. Replace the recharge board and secure with four screws.
5. Replace the speaker assembly and reconnect the cable.

6. Replace the base unit frame and secure with twelve screws.
7. Replace the battery pack, heatsink, modem card, FDD/HDD module, and CD-ROM drive.
8. Secure the four screws on the rear side of the notebook.
9. Put the notebook back to the upright position. Replace the Easy Start board into the housing, then secure with seven screws.
10. Replace the LCD assembly.
11. Replace the keyboard and Easy Start panel.

5.2.12 Touchpad

Disassembly

1. Remove the system board. (See section 5.2.11 Disassembly.)
2. Remove the four screws to lift up the touchpad holder and touchpad panel. (figure 5-27)

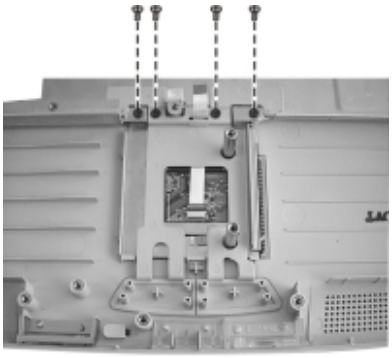


Figure 5-27

Reassembly

1. Replace the touchpad holder and touchpad panel, and secure with four screws.
2. Replace the system board and assemble the notebook. (See section 5.2.11 Reassembly.)

7521 N/B MAINTENANCE

6. Maintenance Diagnostics

6.1 Introduction

Each time the computer is turned on, the system bios runs a series of internal checks on the hardware. This power-on self test (post) allows the computer to detect problems as early as the power-on stage. Error messages of post can alert you to the problems of your computer.

If an error is detected during these tests, you will see an error message displayed on the screen. If the error occurs before the display is initialized,then the screen cannot display the error message. Error codes or system beeps are used to identify a post error that occurs when the screen is not available.

The value for the diagnostic port (378H) is written at the beginning of the test. Therefore, if the test failed, the user can determine where the problem occurred by reading the last value written to port 378H by the 378H port debug board plug at PIO PORT.

6. Maintenance Diagnostics

6.2 Error Codes : Following is a list of error codes in sequent display on the PIO debug board.

SYSTEM SOFT BIOS:

CODE	DESCRIPTION
01h	Start of boot loader sequence.
02h	Initialize chipset.
03h	Memory Sizing.
04h	Perform conventional RAM(1st 640K) test with crossed-
	pattern R/W
05h	Move boot loader to the RAM.
06h	Start point of execution of boot loader in RAM.
07h	Shadow system BIOS.
08h	Initialize clock synthesizer
09h	Initialize audio controller.
0Ah	Detect internal ISA MODEM
0Bh	Proceed with normal boot
0Ch	Proceed with crisis boot
0Fh	DRAM sizing
10h	Initial L1,L2 cache, make stack and diagnose CMOS.
11h	Turn off fast A20 for post. Reset GDT's, 8259s quickly.
12h	Signal power on reset at COMS.
13h	Initialize the chipset, (SDRAM).
14h	Search for ISA bus VGA adapter
15h	Reset counter/timer 1, exite the RAM.
16h	User register config through CMOS
18h	Dispatch to 1st 64K RAM test
19h	Checksum the ROM
1Ah	Reset PIC's(8259s)
1Bh	Initialize video adapter(s)
1Ch	Initialize video (6845 regs)

CODE	DESCRIPTION
1Dh	Initialize color adapter
1Eh	Initialize monochrome adapter
1Fh	Test 8237A page registers
20h	Perform keyboard self test
21h	Test & initialize keyboard controller
22h	Check if CMOS RAM valid
23h	Test battery fail & CMOS X-SUM
24h	Test the DMA controllers
25h	Initialize 8237A controller
26h	Initialize interrupt vectors table.
27h	RAM quick sizing
28h	Protected mode entered safely
29h	RAM test completed
2Ah	Protected mode exit successful
2Bh	Setup shadow
2Ch	Prepare to initialize video
2Dh	Search for monochrome adapter
2Eh	Search for color adapter, VGA initialize.
2Fh	Signon messages displayed
30h	Special init of keyboard ctlr
31h	Test if keyboard present
32h	Test keyboard interrupt
33h	Test keyboard command Byte
34h	Test, blank and count all RAM
35h	Protected mode entered safely (2).
36h	RAM test complete

6. Maintenance Diagnostics

6.2 Error Codes : Following is a list of error codes in sequent display on the PIO debug board.

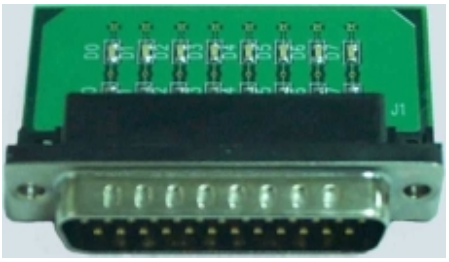
SYSTEM SOFT BIOS:

CODE	DESCRIPTION
37h	Protected mode exit successful
38h	Update keyboard output port to disable gate of A20
39h	Setup cache controller
3Ah	Test if 18.2Hz periodic working
3Bh	Initialize BIOS data area at 40:0.
3Ch	Initialize the hardware interrupt vector tabl
3Dh	Search and init the Mouse
3Eh	Update num lock status
3Fh	OEM initialization of COMM and LPT ports
40h	Configure the COMM and LPT ports
41h	Initialize the floppies
42h	Initialize the hard disk
43h	OEM's init of PM with USB
44h	Initialize additional ROMs
45h	Update NUMLOCK status
46h	Test for coprocessor installed
47h	OEM's init of power management, (check SMI)
48h	OEM functions before boot (PCMCIA, CardBus)
49h	Dispatch to operation system boot
4Ah	Jump into bootstrap code

6. Maintenance Diagnostics

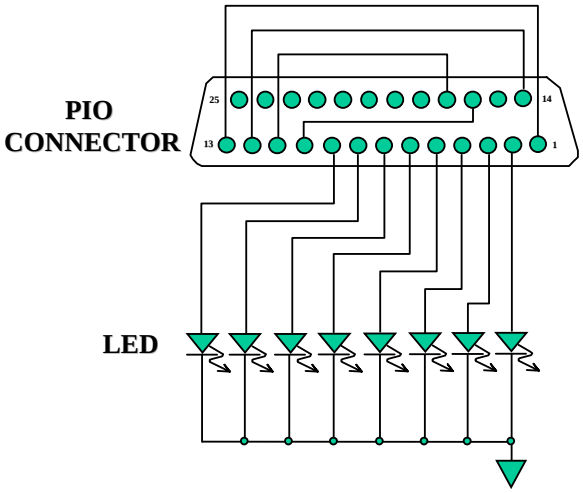
6.3.1 Diagnostic Tools :

- LED * 8 OR
- PIO CONNECTOR * 1



P/N:411904800001
DESCRIPTION :PWA;PWA-378PORT DEBUG BD
Note:Order it from MIC/TSSC

6.3.2 CIRCUIT:



PIN1 : STROBE ⟷ PIN 13 : SLCT

PIN10: ACK# ⟷ PIN 16 : INT#

PIN11: BUSY ⟷ PIN 17 : SELIN#

PIN12: PTERR ⟷ PIN 14 : AUTOFD#

PIN{9:2}: PD{7:0}

7. TROUBLE SHOOTING

7.1 NO POWER

7.2 NO DISPLAY

7.3 VGA CONTROLLER FAILURE LCD NO DISPLAY

7.4 EXTERNAL MONITOR NO DISPLAY

7.5 MEMORY TEST ERROR

7.6 KEYBOARD TEST ERROR OR TRACK PAD TEST ERROR

7.7 CD-ROM DRIVE TEST ERROR

7.8 HARD DRIVE TEST ERROR

7.9 USB PORT TEST ERROR

7.10 AUDIO FAILURE

7.11 SIO PORT TEST ERROR

7.12 PIO PORT TEST ERROR

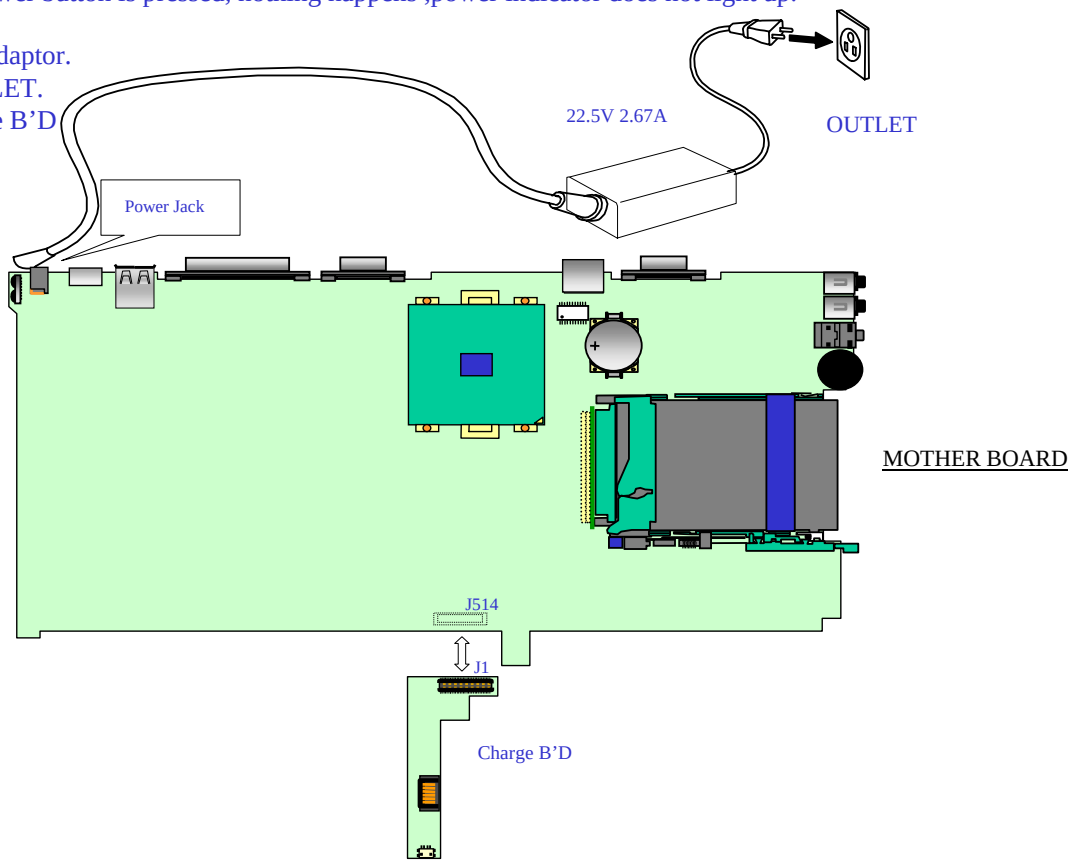
7.13 PC-CARD SOKET FAIL

7521 N/B MAINTENANCE

7.1 NO POWER:

When the power button is pressed, nothing happens ,power indicator does not light up.

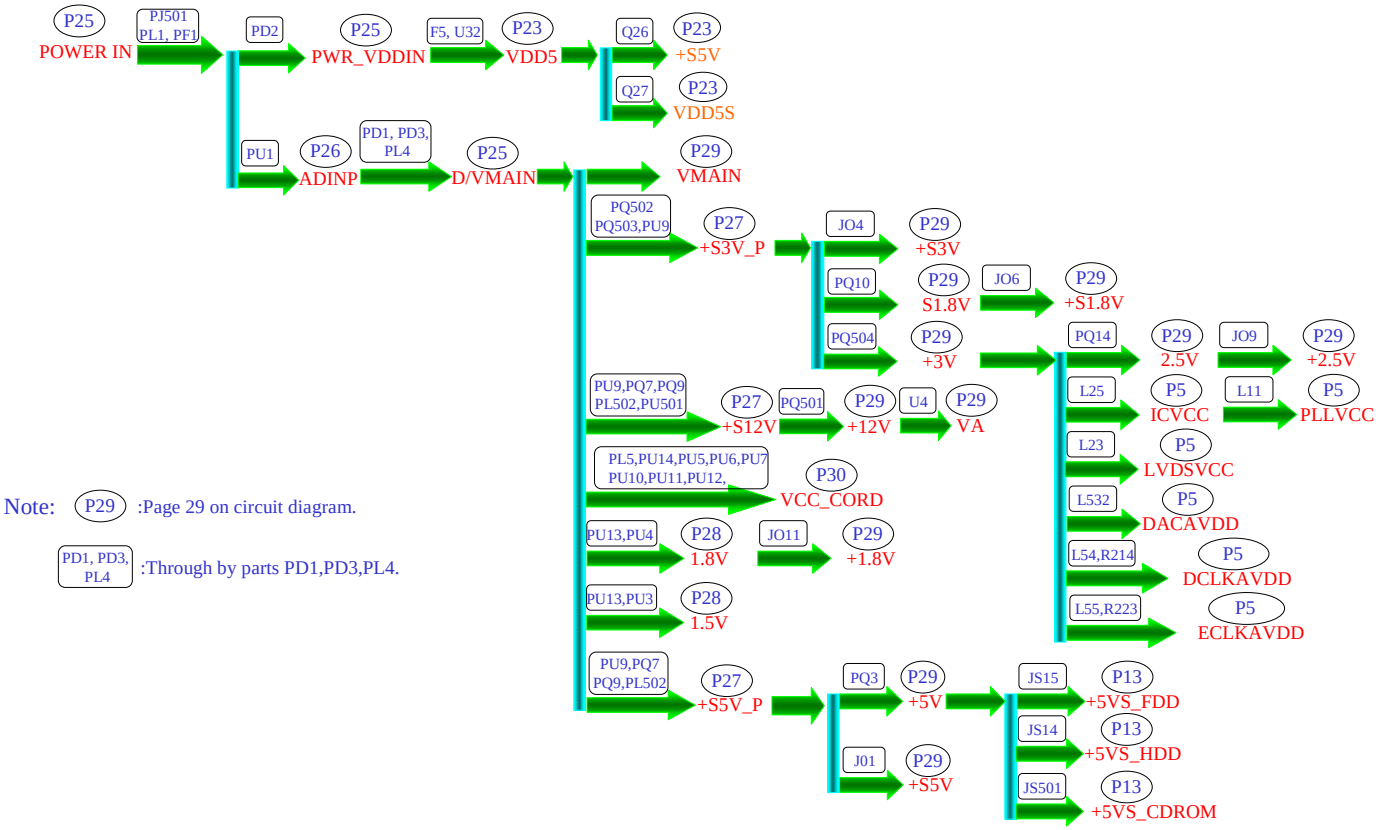
1. Check AC Adaptor.
2. Check OUTLET.
3.Check Charge B'D



7521 N/B MAINTENANCE

7.1 NO POWER:

When the power button is pressed, nothing happens ,power indicator does not light up.



Note: P29 :Page 29 on circuit diagram.

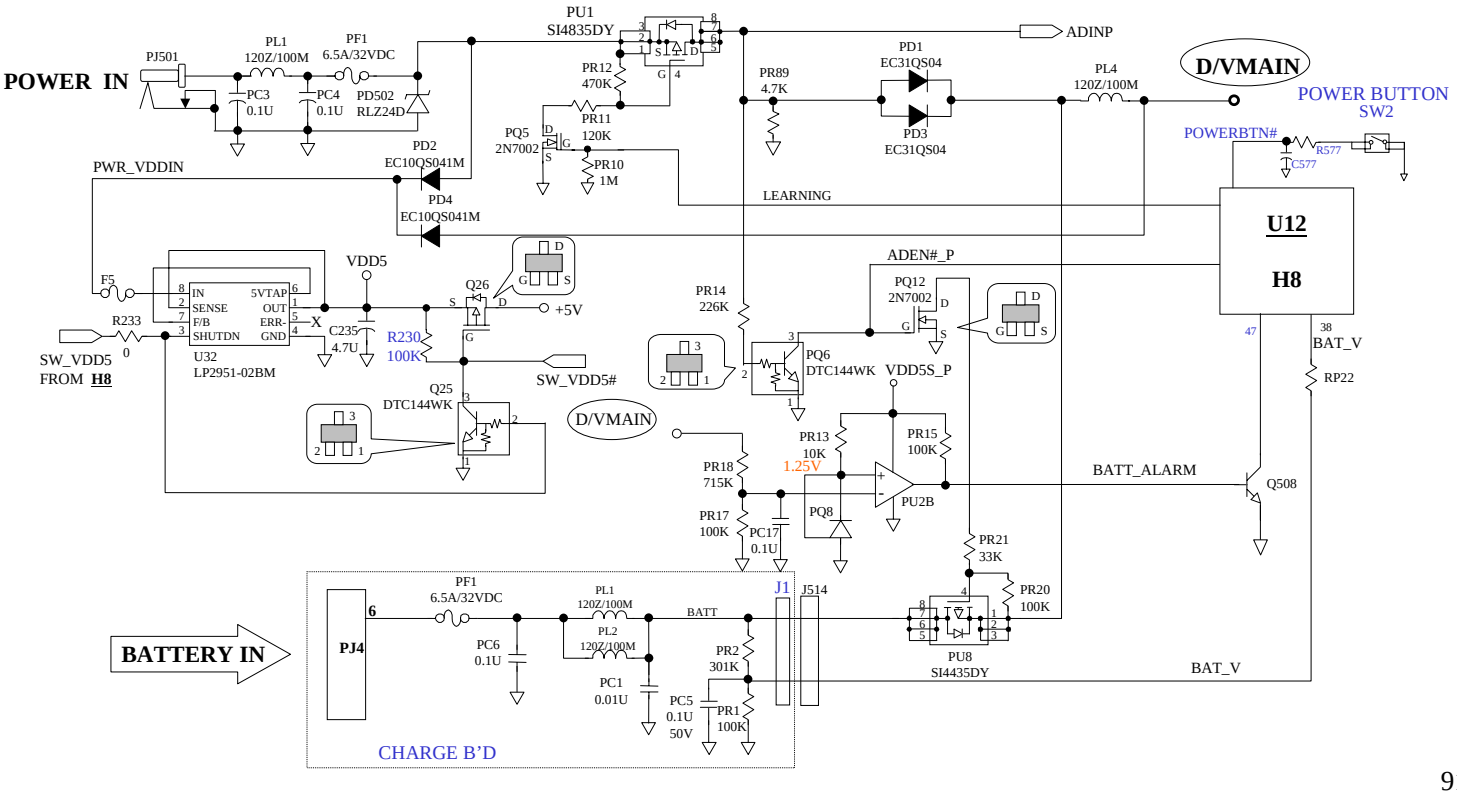
PD1, PD3, PL4 :Through by parts PD1,PD3,PL4.

7521 N/B MAINTENANCE

7.1 NO POWER:

Symptom:

When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.

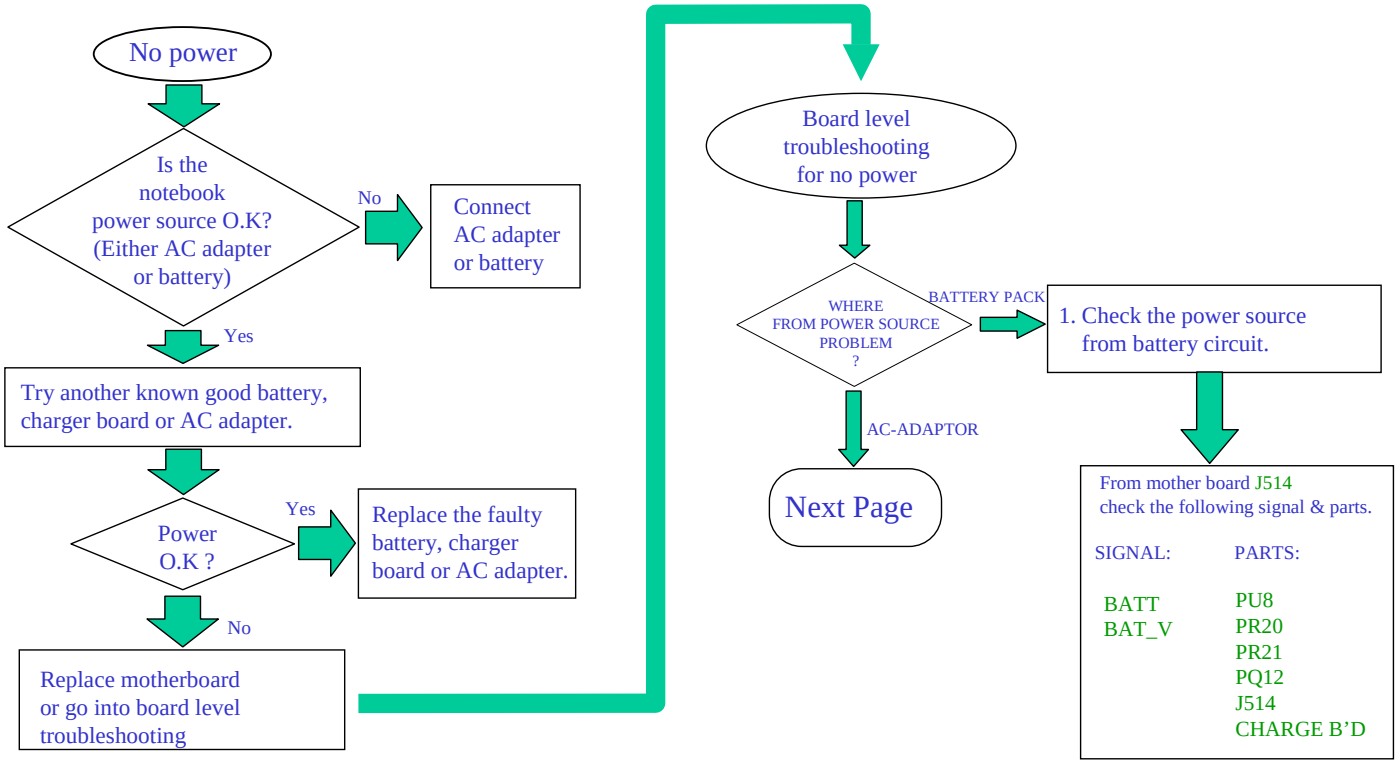


7521 N/B MAINTENANCE

7.1 NO POWER:

Symptom:

When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.

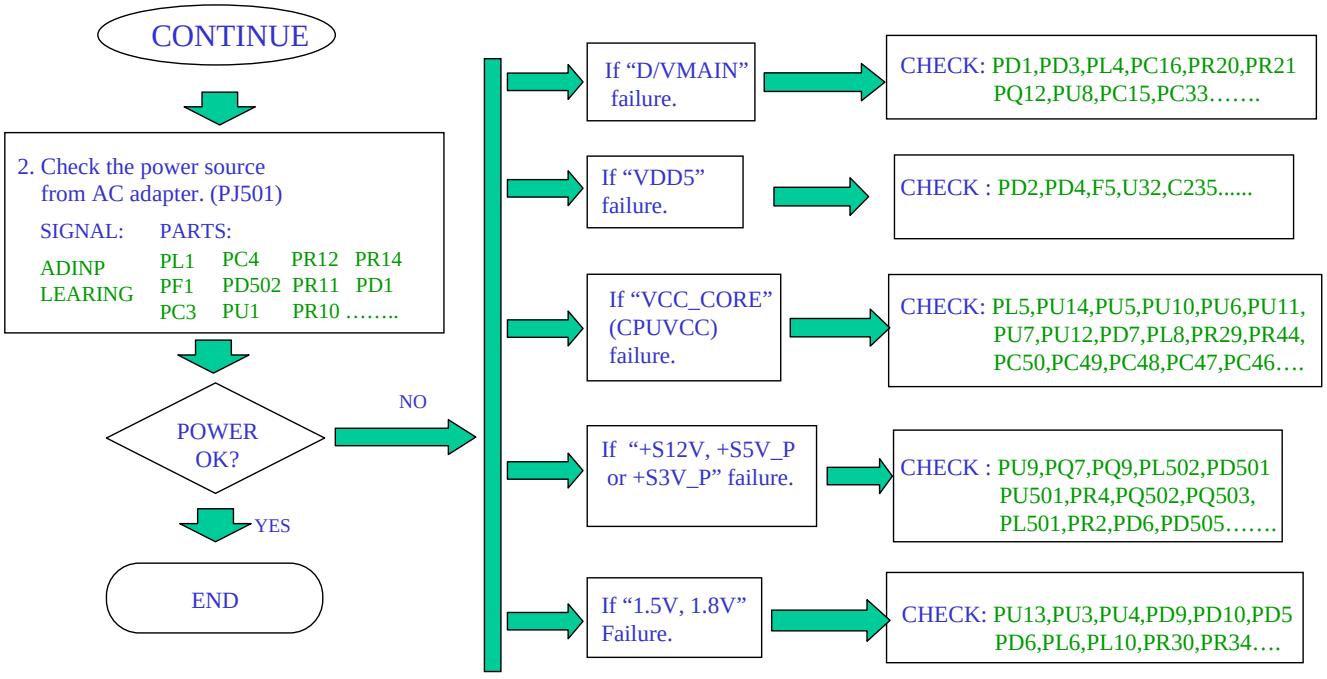


7521 N/B MAINTENANCE

7.1 NO POWER:

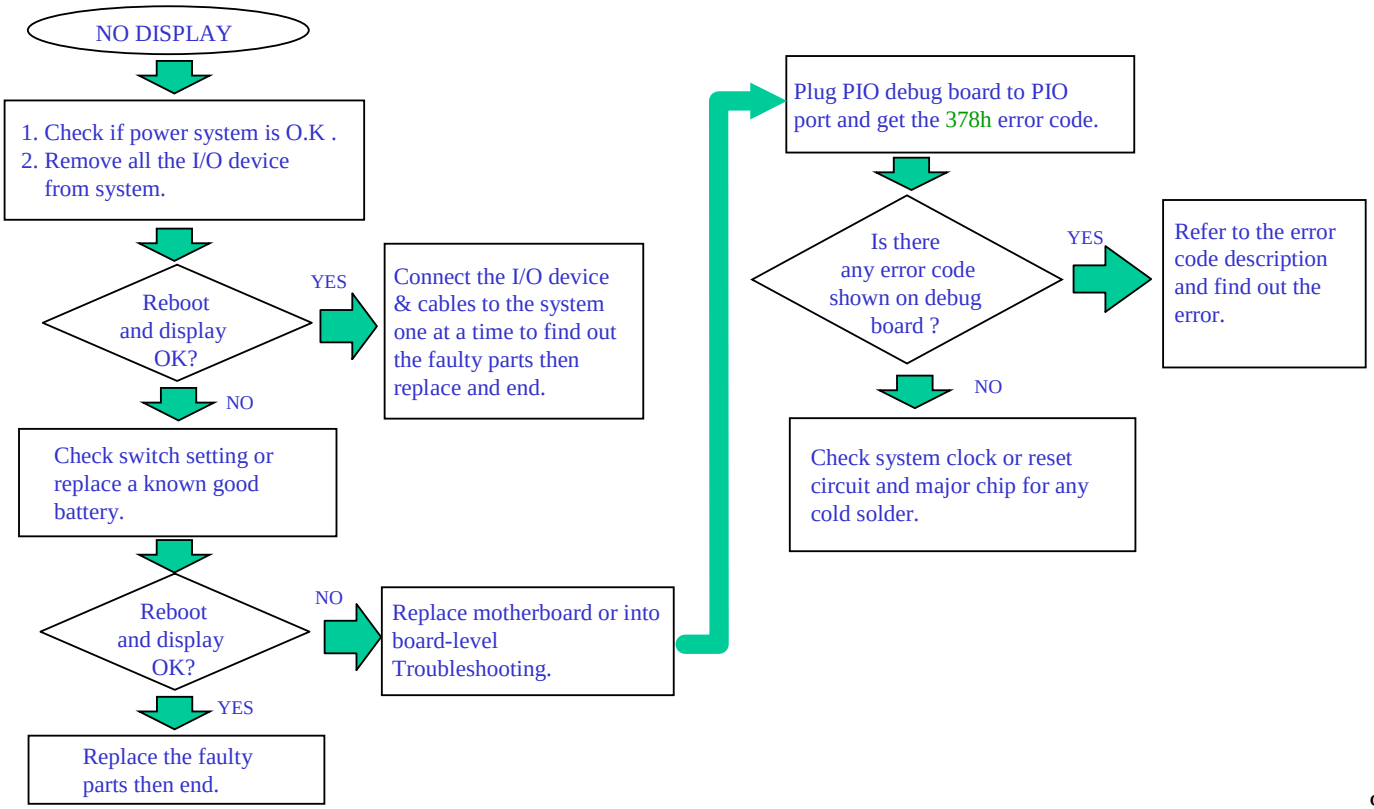
Symptom:

When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.



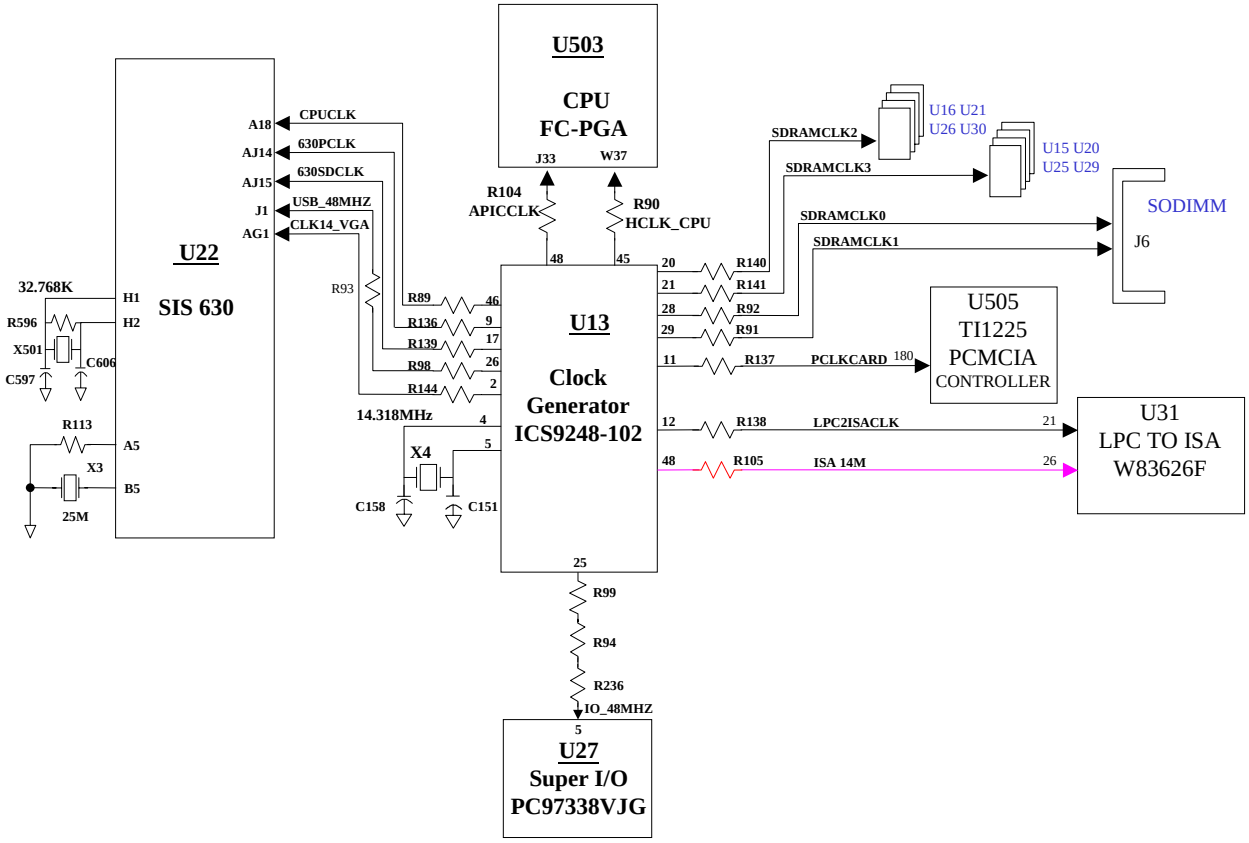
7.2 NO DISPLAY

There is no display on both LCD and monitor



7.2 NO DISPLAY

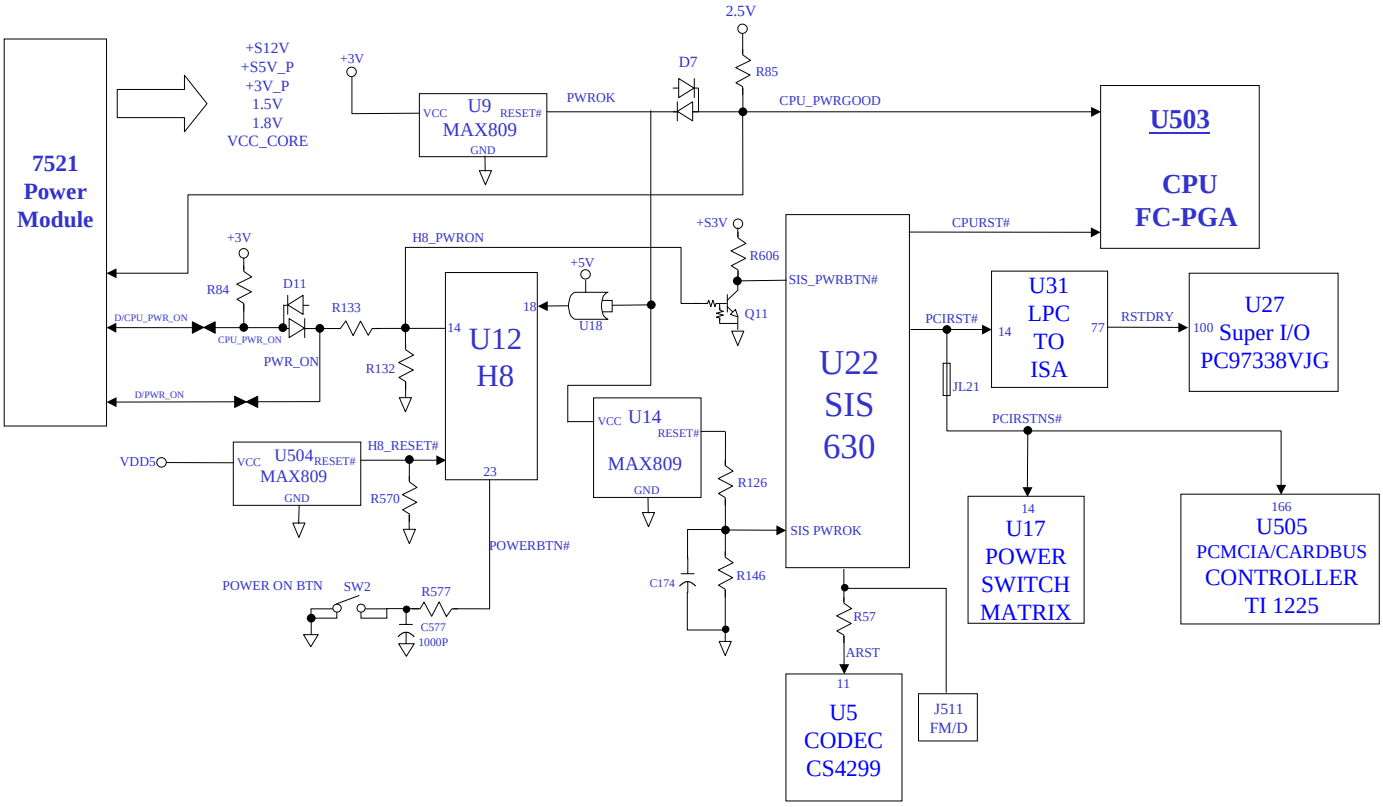
******System Clock Check ******



7521 N/B MAINTENANCE

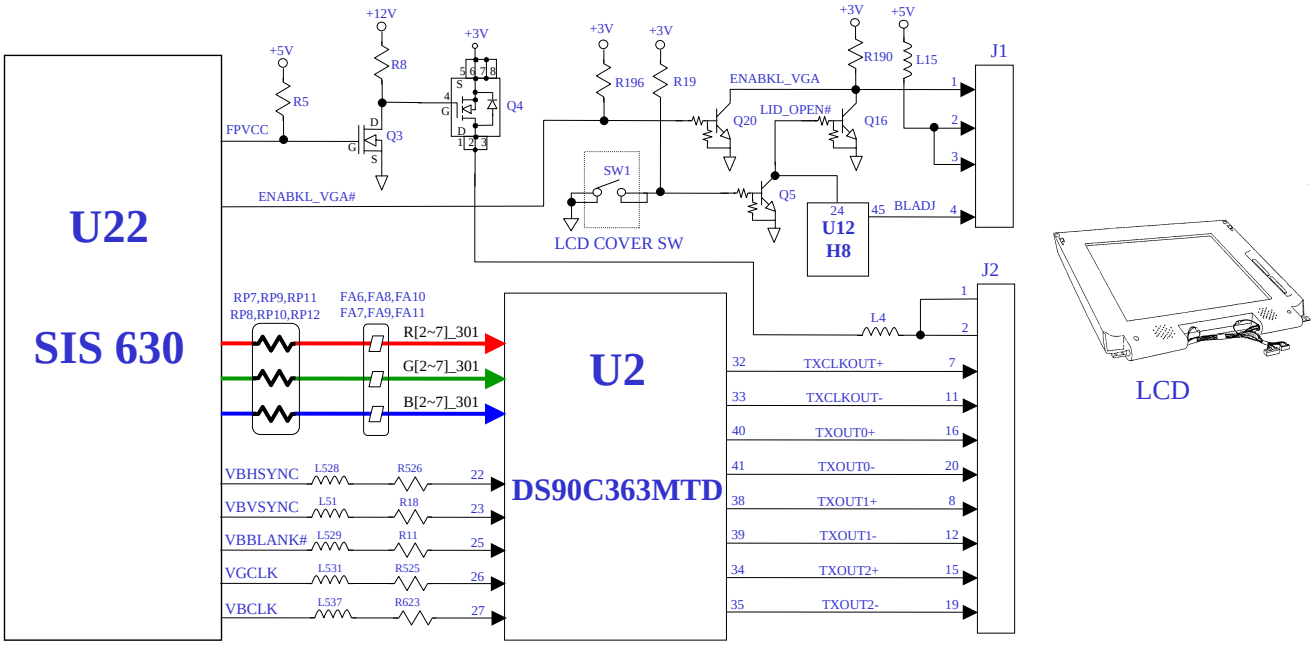
7.2 NO DISPLAY

********Power Good & Reset System ********



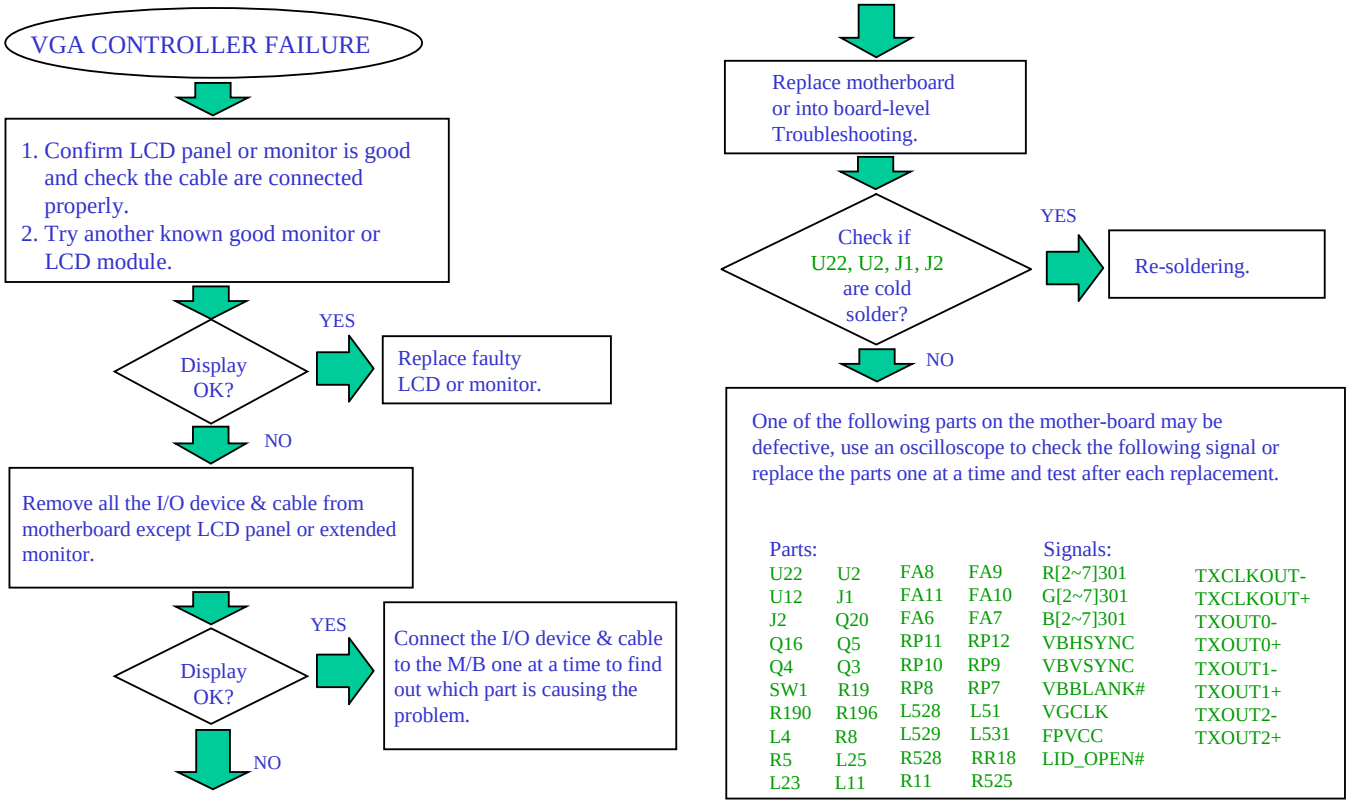
7.3. VGA CONTROLLER FAILURE LCD NO DISPLAY

There is no display or picture abnormal on LCD.



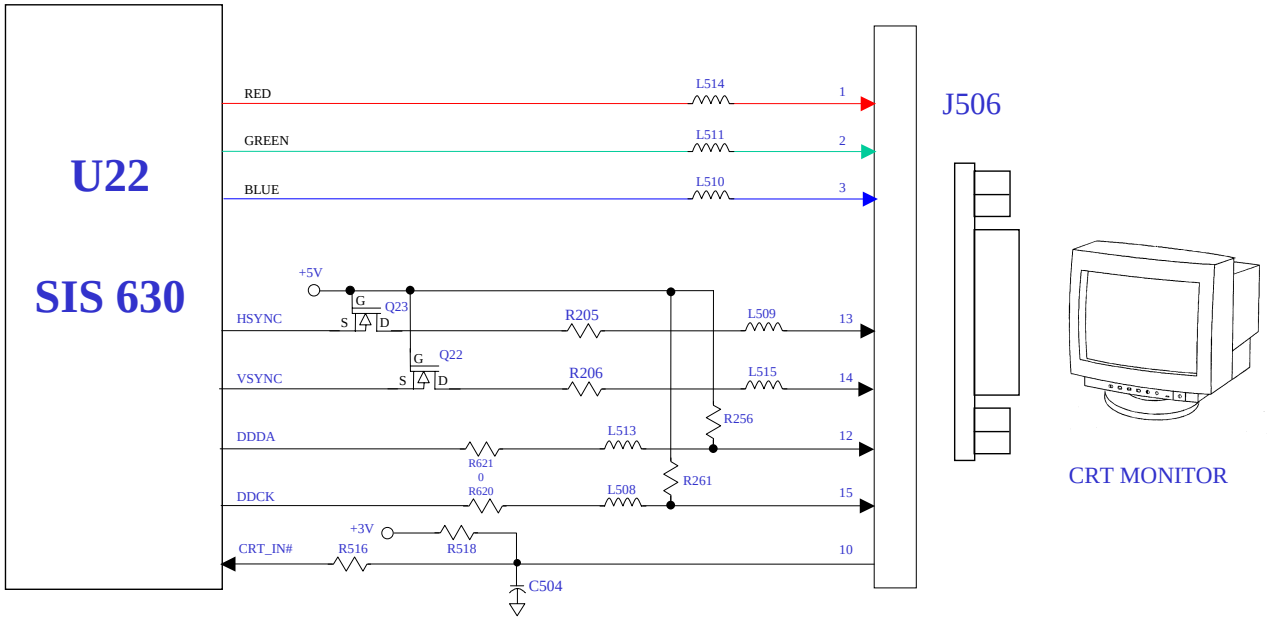
7.3. VGA CONTROLLER FAILURE LCD NO DISPLAY

There is no display or picture abnormal on LCD.



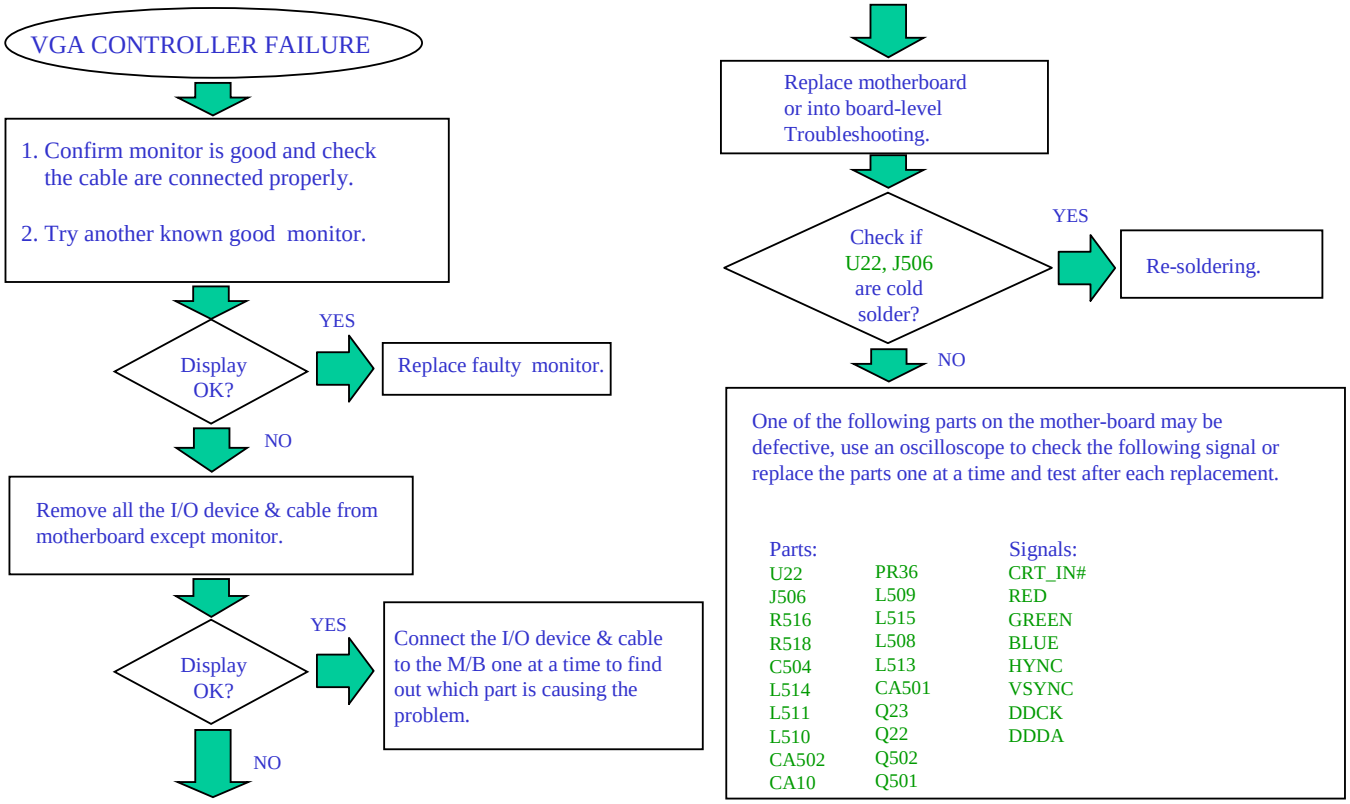
7.4 EXTERNAL MONITOR NO DISPLAY

There is no display or picture abnormal on CRT monitor.



7.4 EXTERNAL MONITOR NO DISPLAY

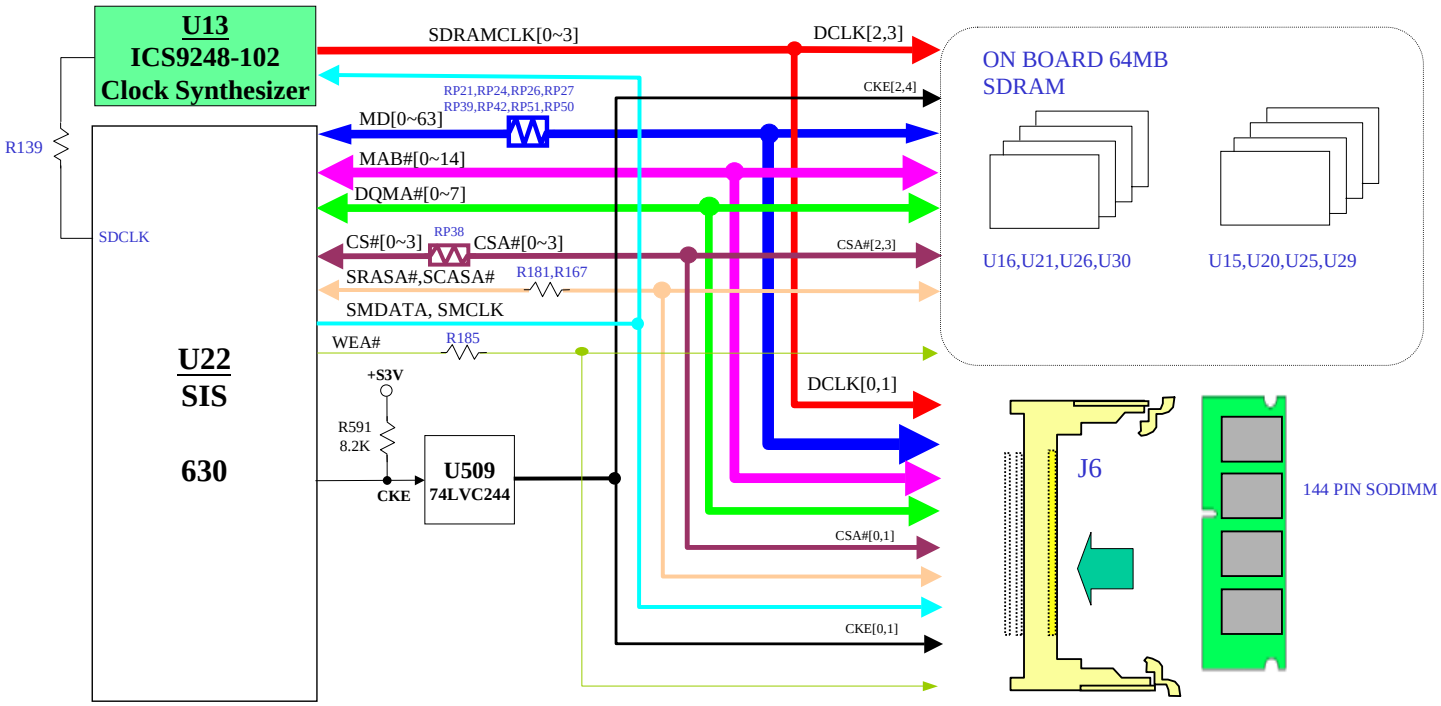
There is no display or picture abnormal on CRT monitor.



7521 N/B MAINTENANCE

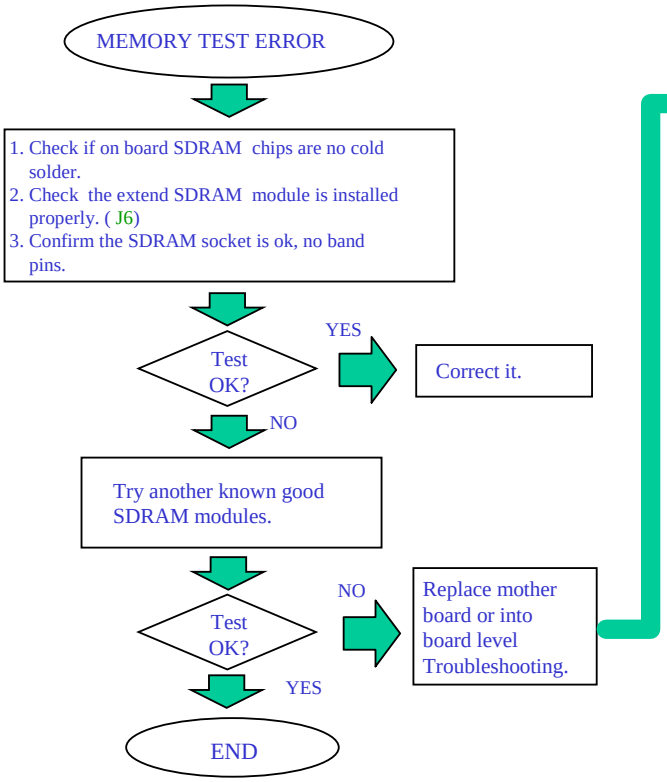
7.5 MEMORY TEST ERROR

Either on board or extend SDRAM is failure or system hangs up.



7.5 MEMORY TEST ERROR

Either on board or extend SDRAM is failure or system hangs up.



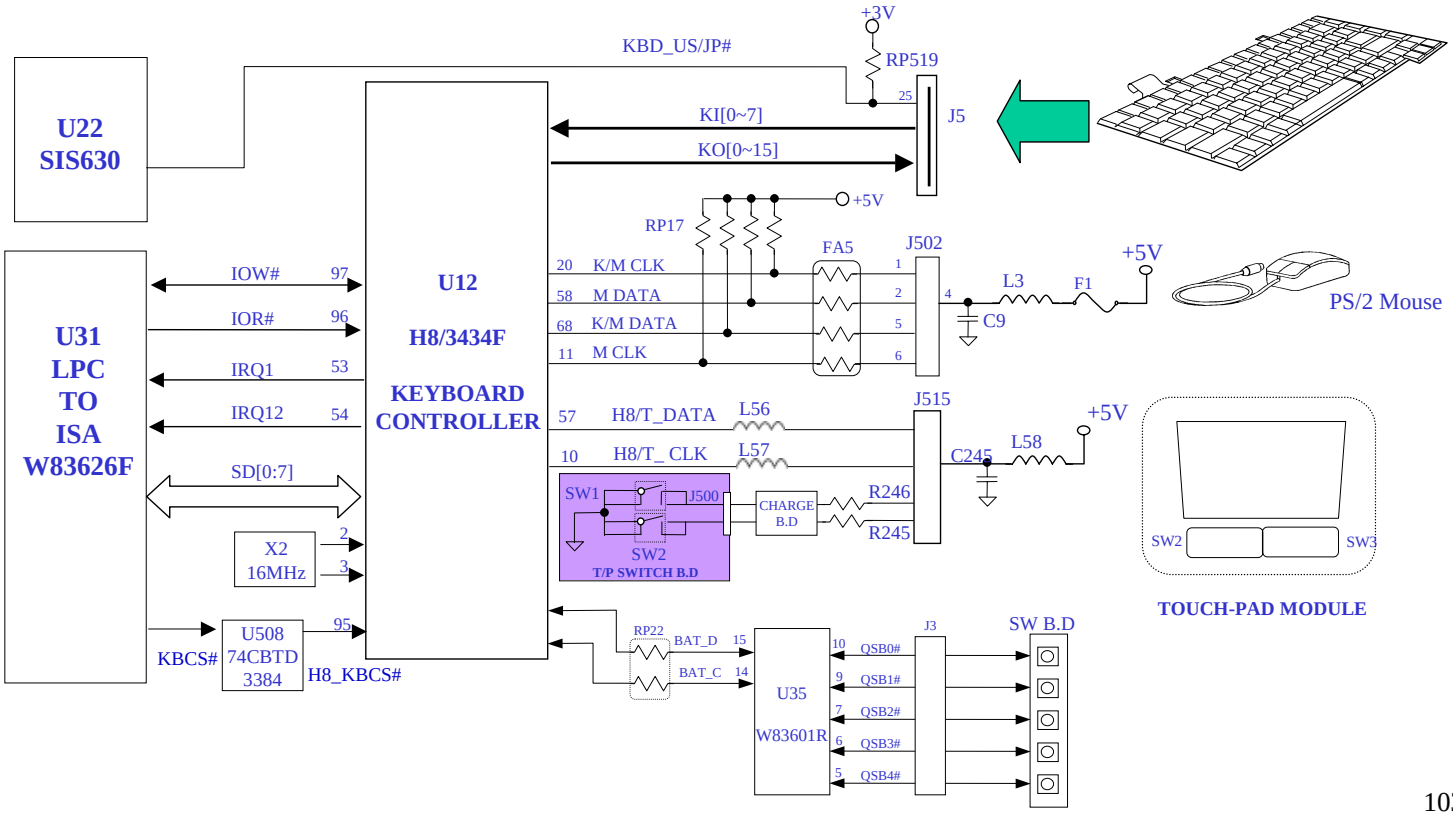
Board-level Troubleshooting for Memory test error.

Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:	Signals:	
U22, U13	MDR[0~63]	CSA#[0:3]
U15, U16	MD[0~63]	CKE[0:3]
U20, U21	MAB#[0~9]	SDRAMCLK[0:3]
U25, U26	MAB[10,13]	SMBDATA
U29, U30	MAB#[11,12]	SMBCLK
RP21, RP24	SCASA#,	
RP26, RP27	SRASA#	
RP39, RP42	WEA#	
RP51, RP50	DQMA#[0:7]	
RP38, J6, U509		

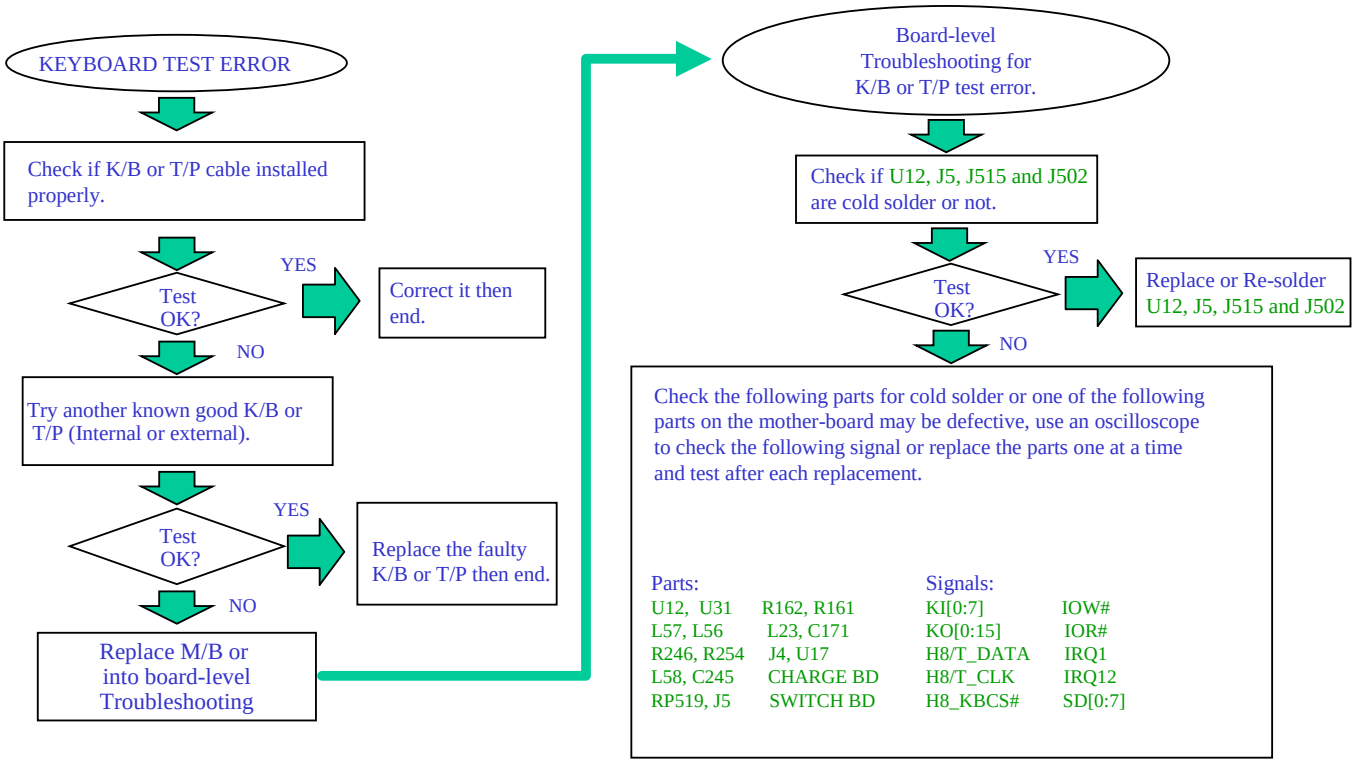
7.6 KEYBOARD(K/B) TOUCH-PAD(T/P) TEST ERROR

Error message of keyboard failure is shown or any key doesn't work.



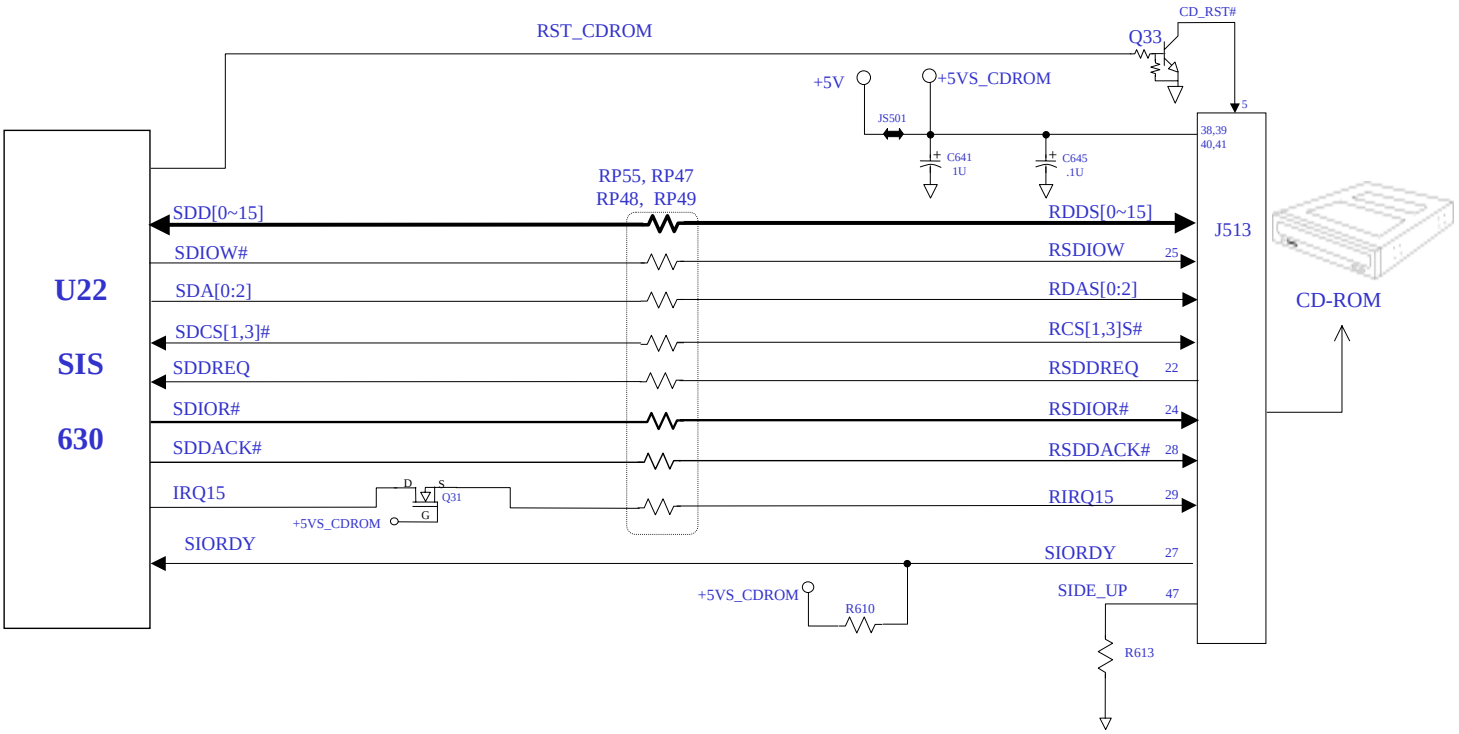
7.6 KEYBOARD(K/B) TOUCH-PAD(T/P) TEST ERROR

Error message of keyboard or touch pad failure is shown or any key doesn't work.



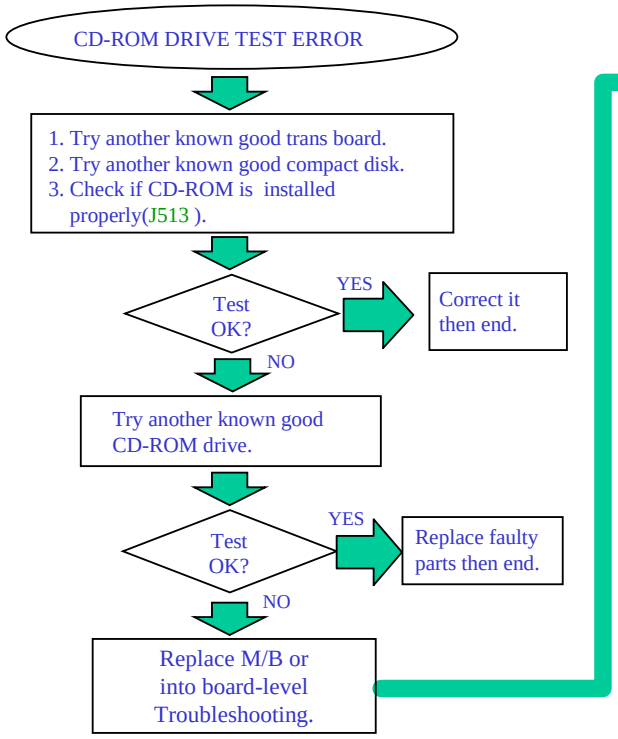
7.7 CD-ROM DRIVE TEST ERROR

An error message is shown when reading data from CD-ROM drive.



7.7 CD-ROM DRIVE TEST ERROR

An error message is shown when reading data from CD-ROM drive.



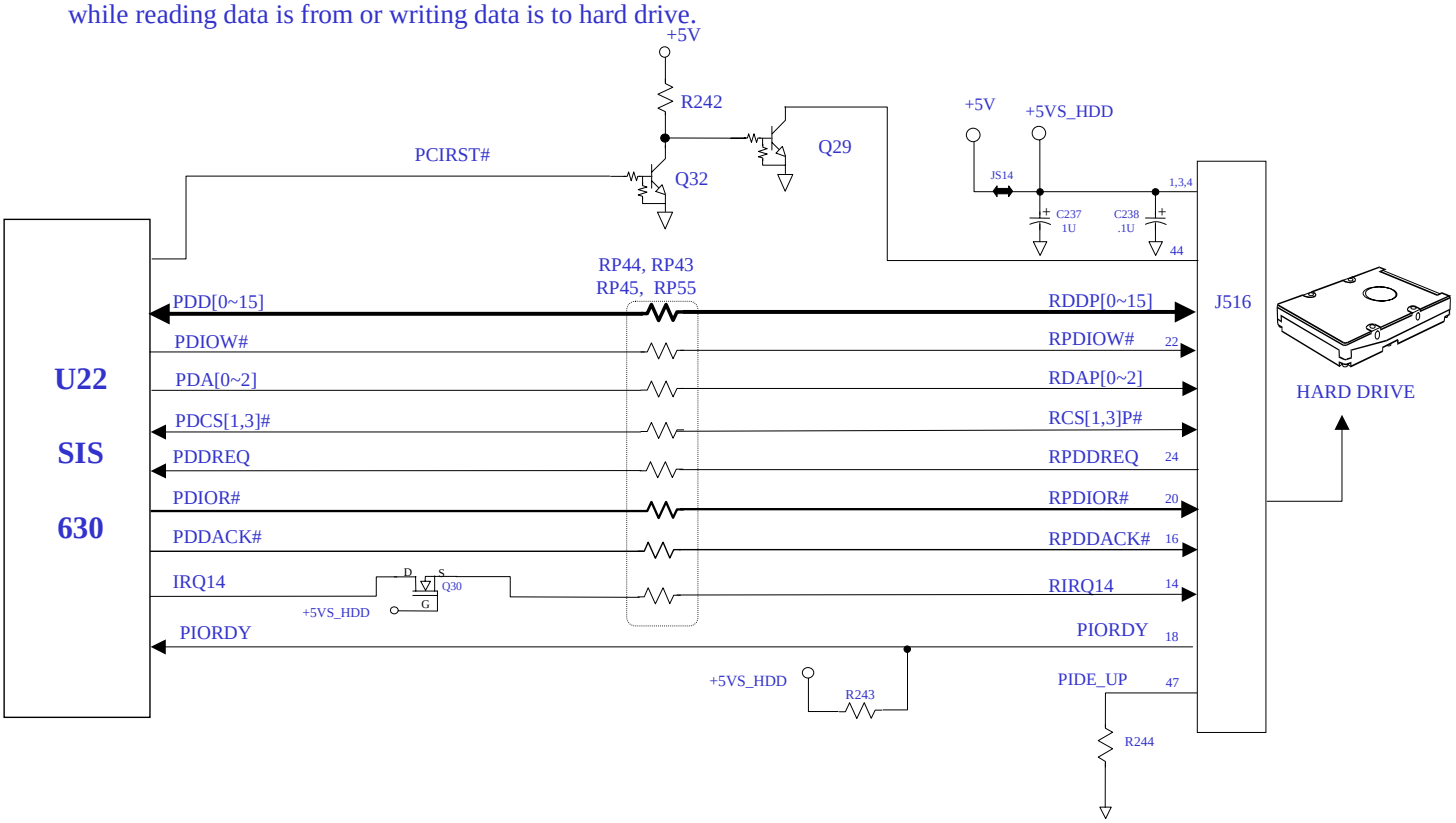
Board-level Troubleshooting for CD-ROM drive test error.

Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:	Signals:	
U22, Q33	SDD[0~15]	RDDS[0~15]
RP55, RP47	SDDACK#	RSDDACK#
RP48, RP49	SDIOR#	RSDIOR#
R611, R227	SDIOW#	RSDIOW#
R610, R613	SDDREQ	RCS[1,3]S#
C641, C645	SDCS[1,3]#	RDAS[0~2]
J513, Q31	SDA[0:2]	CD_RST#
	SIDEACTS#	RST_CDROM
	SIDE_ PU	

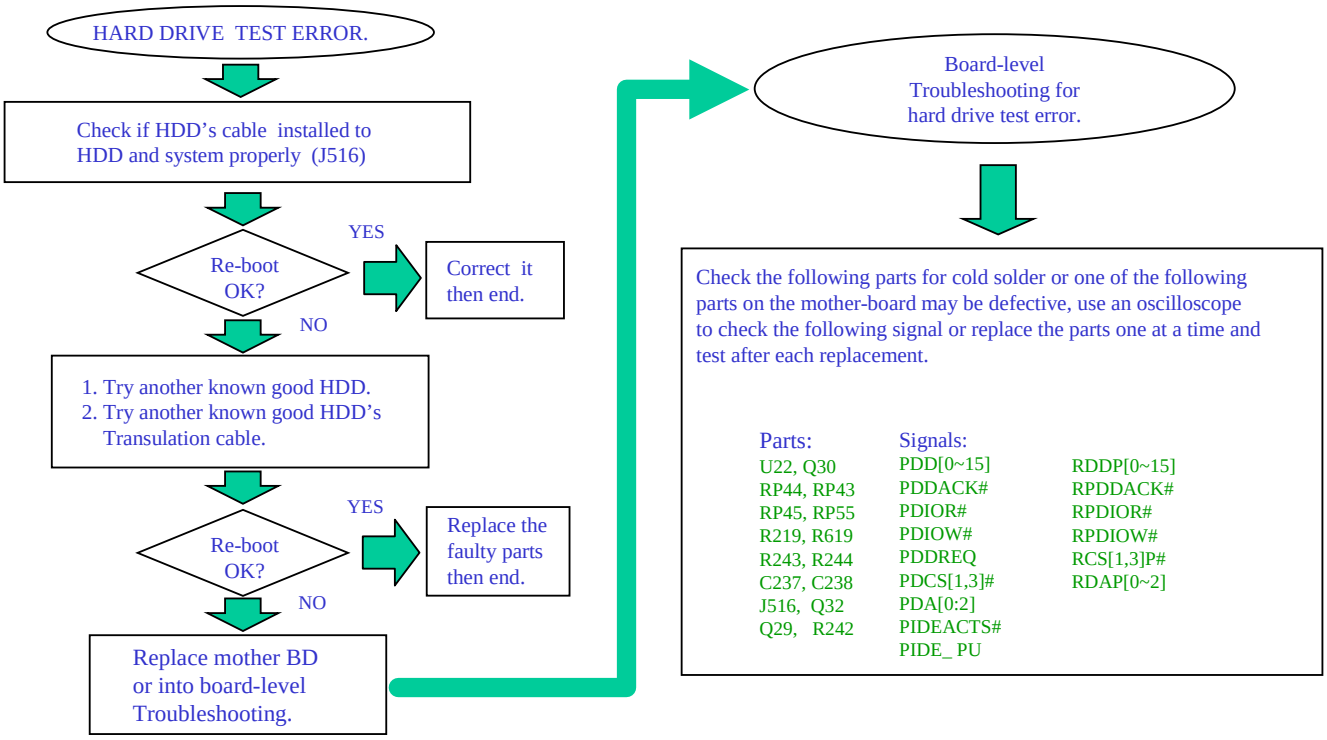
7.8 HARD DRIVE TEST ERROR

Either an error message is shown , or the driver motor continues spinning , while reading data is from or writing data is to hard drive.



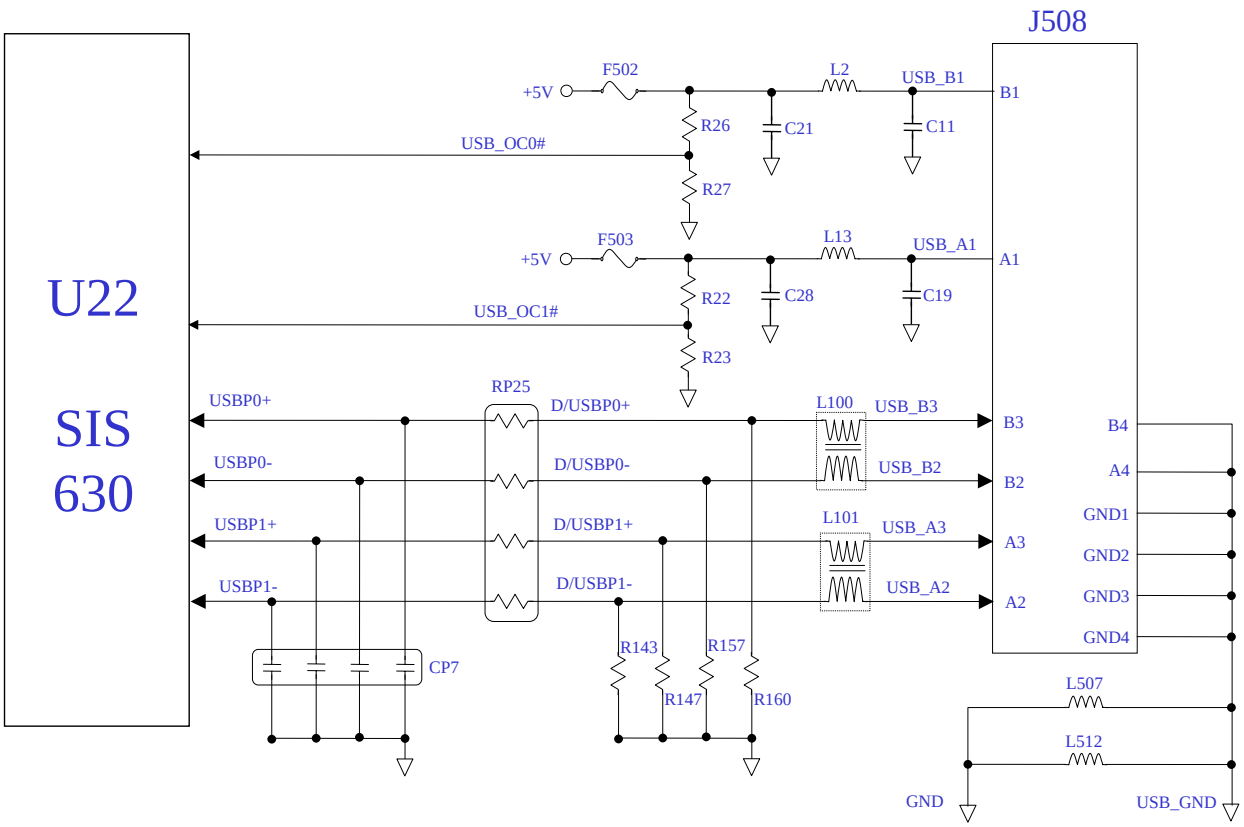
7.8 HARD DRIVE TEST ERROR

Either an error message is shown , or the driver motor continues spinning , while reading data is from or writing data is to hard drive.



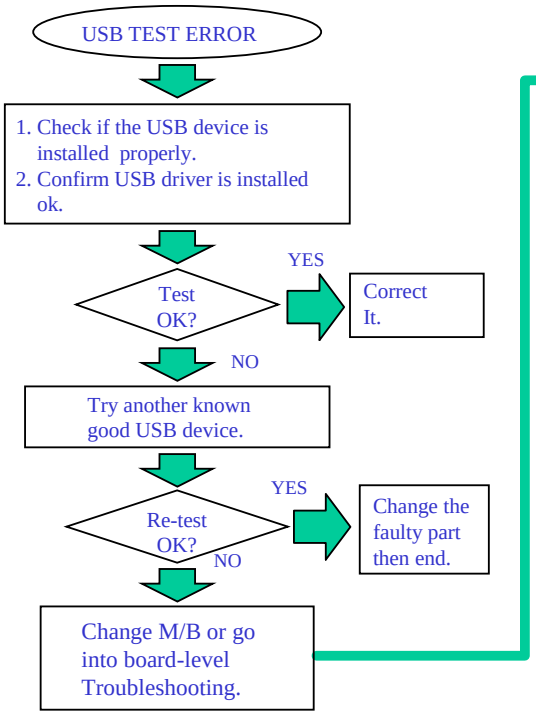
7.9 USB PORT TEST ERROR

An error occurs when a USB I/O device is installed.



7.9 USB PORT TEST ERROR

An error occurs when a USB I/O device is installed.



Board-level Troubleshooting for USB test error

Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

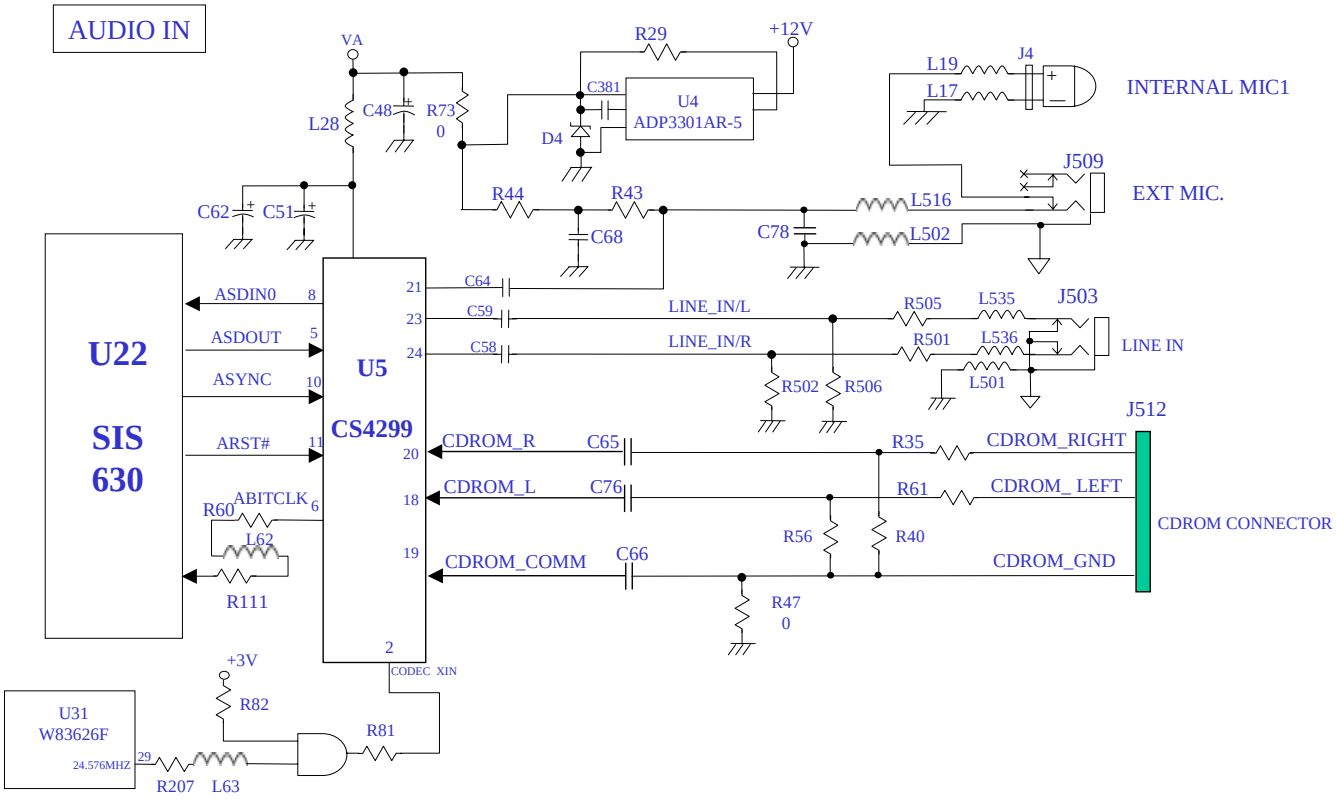
Parts:
U22, RP25, CP7
F502, R26, R27
C21, L2, C11
L100, R157
R160, F503, R22
R23, C28, L13
C19, L101
R143, R147
L507, L512

Signals:

USBP1-	USB_B1
USBP1+	USB_B2
USBP0-	USB_B3
USBP0+	USB_B4
D/USBP1-	USB_A1
D/USBP1+	USB_A2
D/USBP0-	USB_A3
D/USBP0+	USB_A4
USB_OC0#	
USB_OC1#	

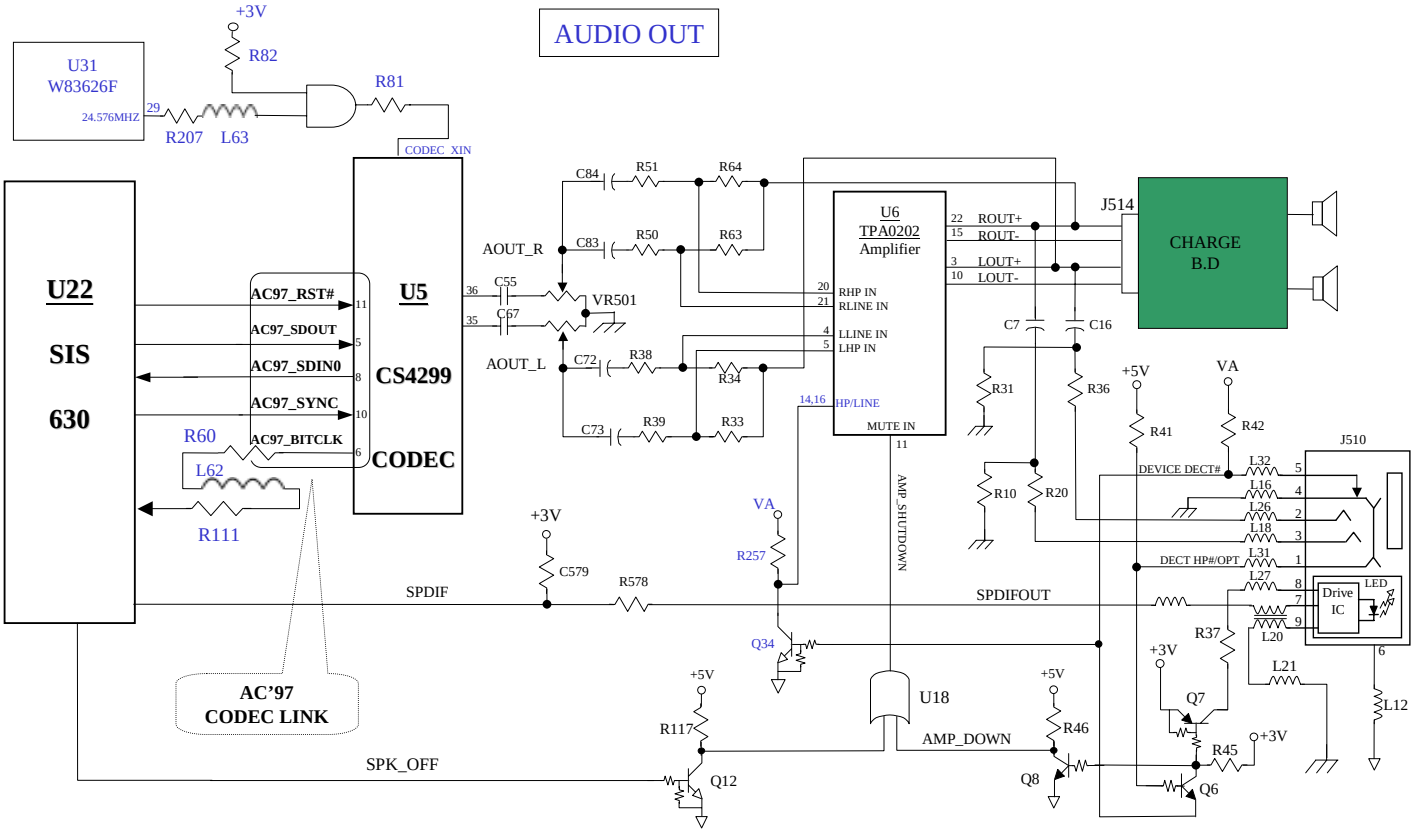
7.10 AUDIO FAILURE

No sound from speaker after audio driver is installed.



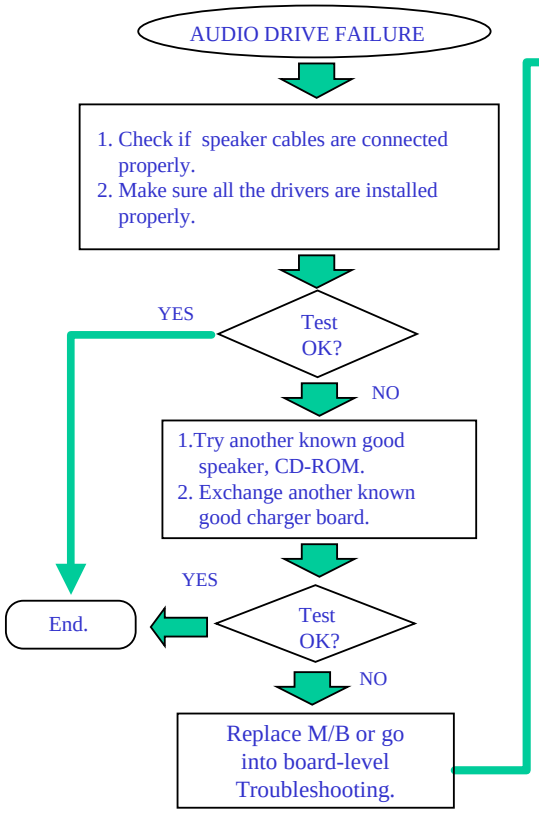
7.10 AUDIO FAILURE

No sound from speaker after audio driver is installed.



7.10 AUDIO FAILURE

No sound from speaker after audio driver is installed.



Board-level Troubleshooting for audio test error.

Check the following parts for cold solder or one of the following parts on the motherboard may be defective,use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

1. If no sound cause of line out, check the following parts & signals:

Parts:	Signals:
U5, C55	AOUT_R
U6, C67	AOUT_L
VR501	ROUT+
C84, C83	ROUT-
C72, C73	LOUT+
R51, R50	LOUT-
R38, R39	SPK_OFF
Charge BD	

2. If no sound cause of MIC, check the following parts & signals:

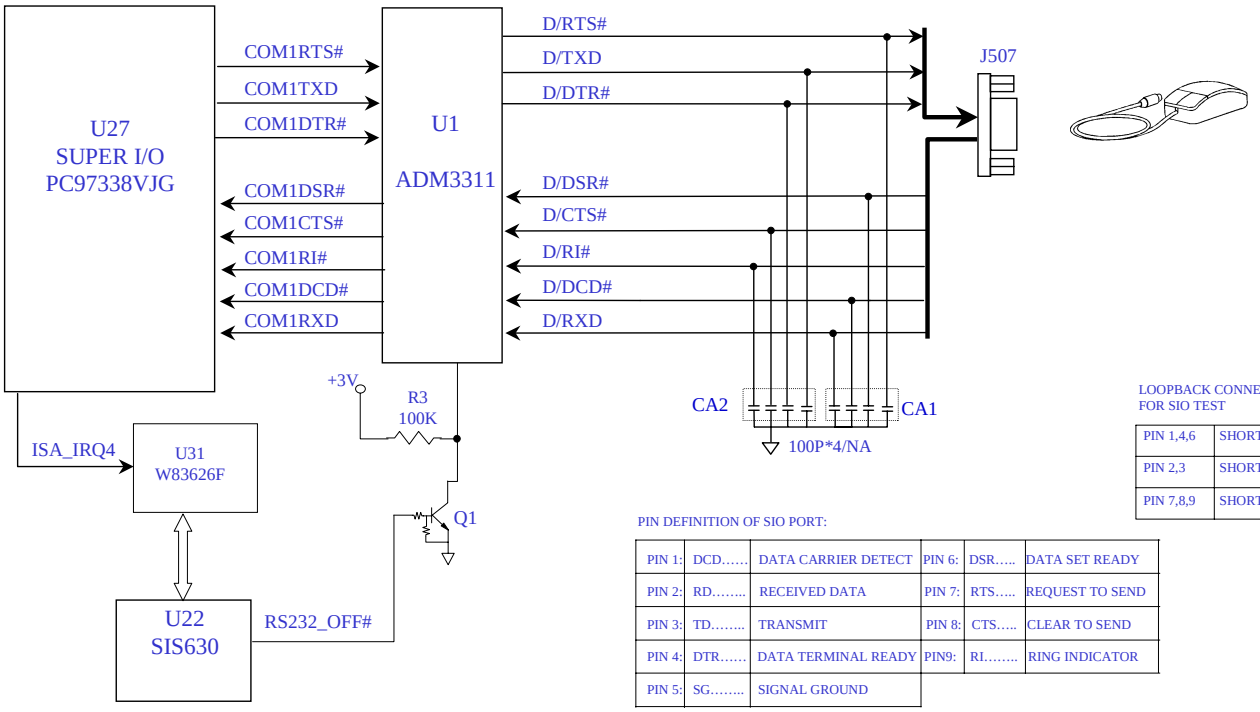
Parts:	Signals:
U5, C64	MIC1
L516, L502	
C78, J509	
J4, L19, L17	
R43, R44	
C68, R66	
D4, U4	

3. If no sound cause of CD-ROM, check the following parts & signals:

Parts:	Signals:
U5, C65	CDROM_LEFT
C76, C66	CDROM_RIGHT
J513	CDROM_GND

7.11 SIO PORT TEST ERROR

An error occurs when a mouse or other I/O device is installed.



LOOPBACK CONNECTOR FOR SIO TEST

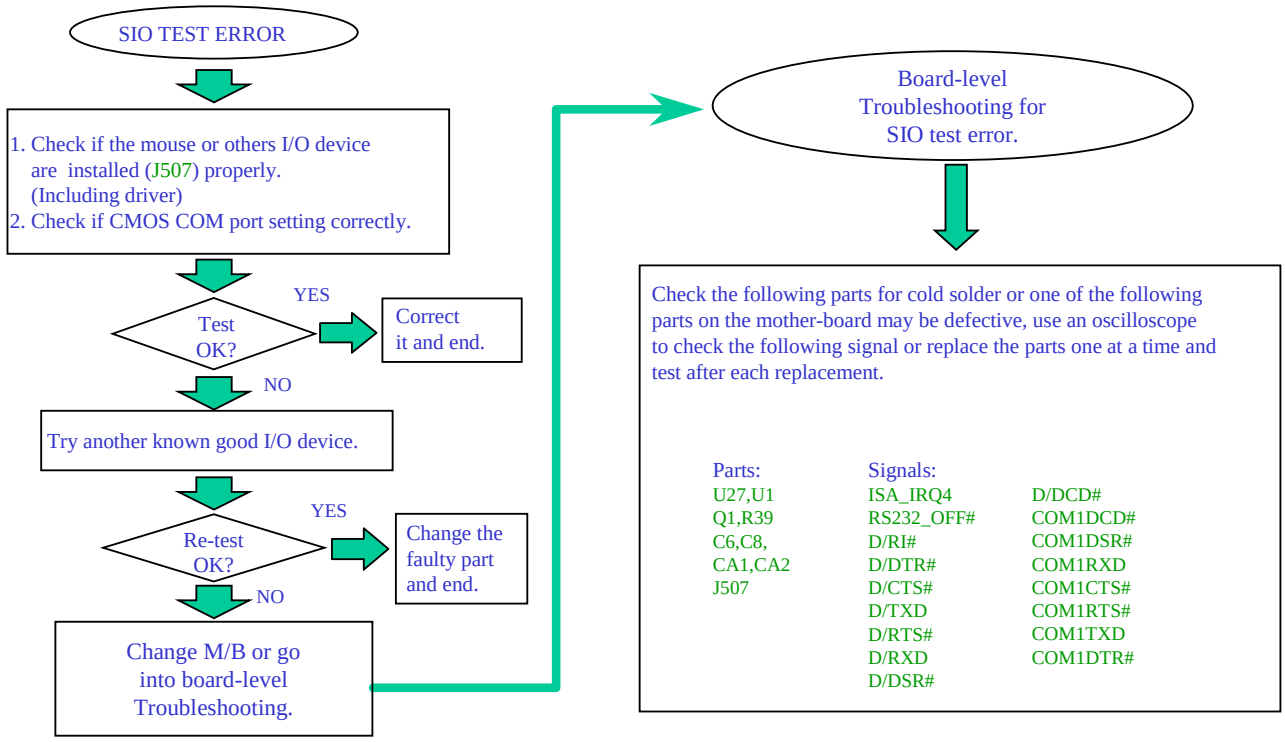
PIN 1,4,6	SHORT
PIN 2,3	SHORT
PIN 7,8,9	SHORT

PIN DEFINITION OF SIO PORT:

PIN 1:	DCD……	DATA CARRIER DETECT	PIN 6:	DSR…..	DATA SET READY
PIN 2:	RD……..	RECEIVED DATA	PIN 7:	RTS…..	REQUEST TO SEND
PIN 3:	TD……..	TRANSMIT	PIN 8:	CTS…..	CLEAR TO SEND
PIN 4:	DTR……	DATA TERMINAL READY	PIN9:	RI……..	RING INDICATOR
PIN 5:	SG……..	SIGNAL GROUND			

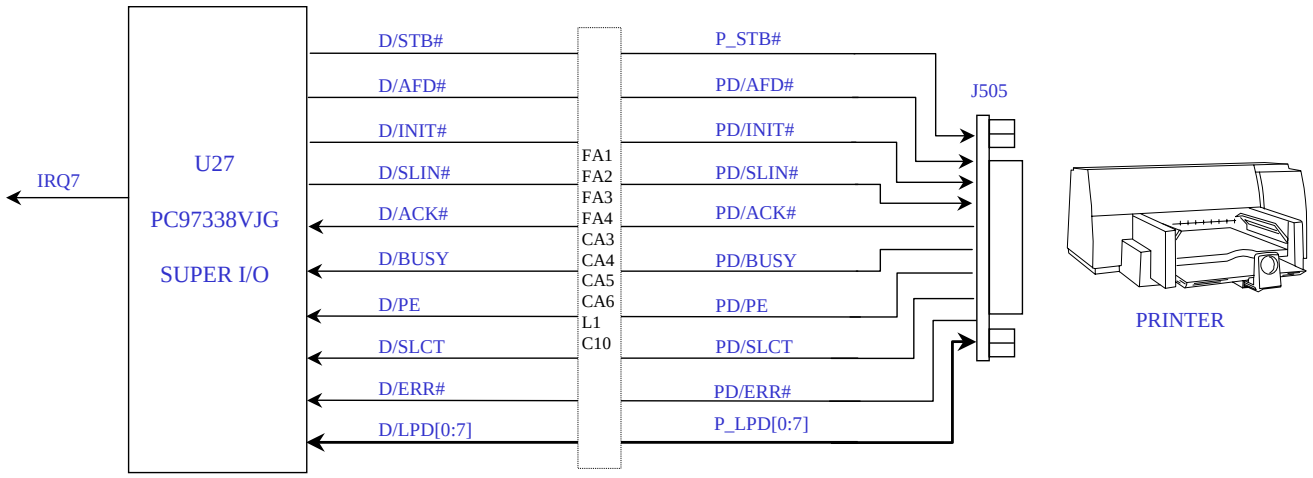
7.11 SIO PORT TEST ERROR

An error occurs when a mouse or other I/O device is installed.



7.12 PIO PORT TEST ERROR

When a print command is issued, printer prints nothing or garbage.



PIN DEFINITION OF PIO PORT

PIN 1	STB	STROBE SIGNAL	PIN 14	AFD	AUTO LINE FEED
PIN 2-9	D0 - D7	PARALLEL PORT DATA BUS D0 TO D7	PIN 15	ERR	ERROR AT PRINTER
PIN 10	ACK	ACKNOWLEDGE HANDSHANK	PIN 16	INIT	INITIATE OUTPUT
PIN 11	BUSY	BUSY SIGNAL	PIN 17	SLIN	PRINTER SELECT
PIN 12	PE	PAPER END	PIN 18-25:		SIGNAL GROUND
PIN 13	SLCT	PRINTER SELECTED			

LOOPBACK CONNECTOR FOR PIO TEST:

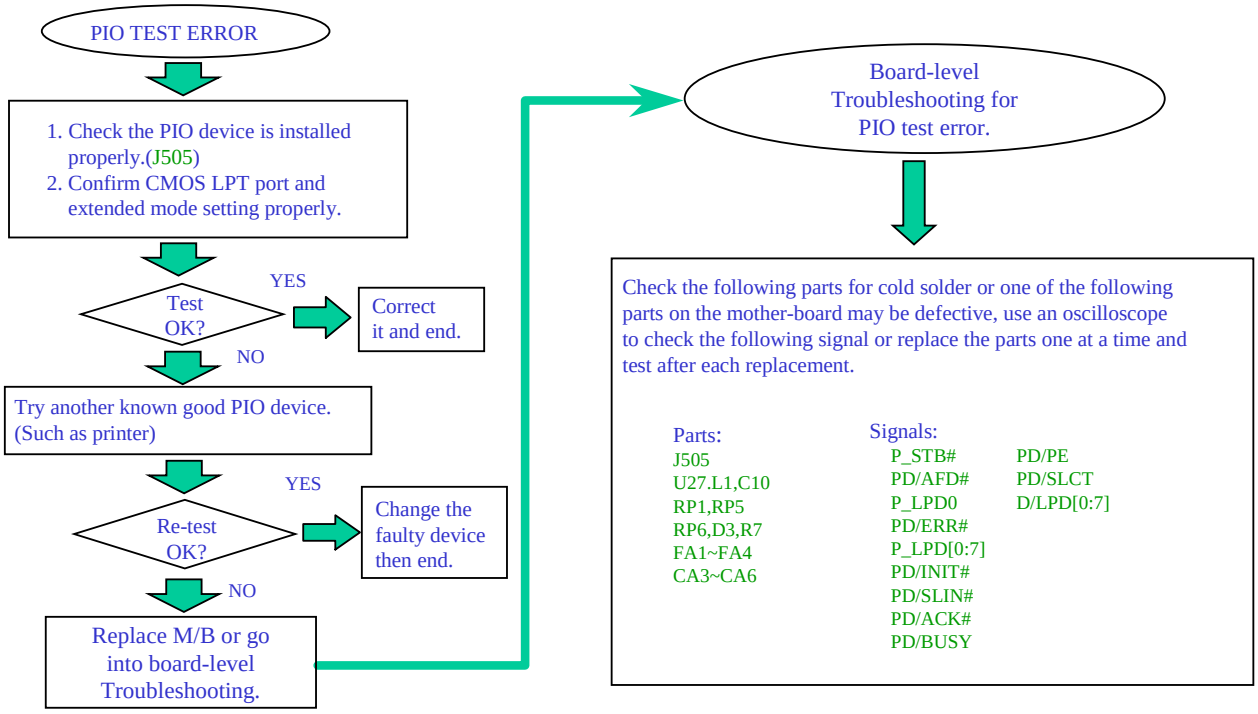
PIN 1, 13	SHORT	PIN 10,16	SHORT
PIN 2, 15	SHORT	PIN 11,17	SHORT
PIN 12, 14	SHORT		

LOOPBACK CONNECTOR FOR EPP TEST:

PIN 1, 2, 4, 6, 8	SHORT
PIN 3, 5, 7, 9, 16	SHORT
PIN 18, 19, 20, 21, 22, 23, 24, 25	SHORT

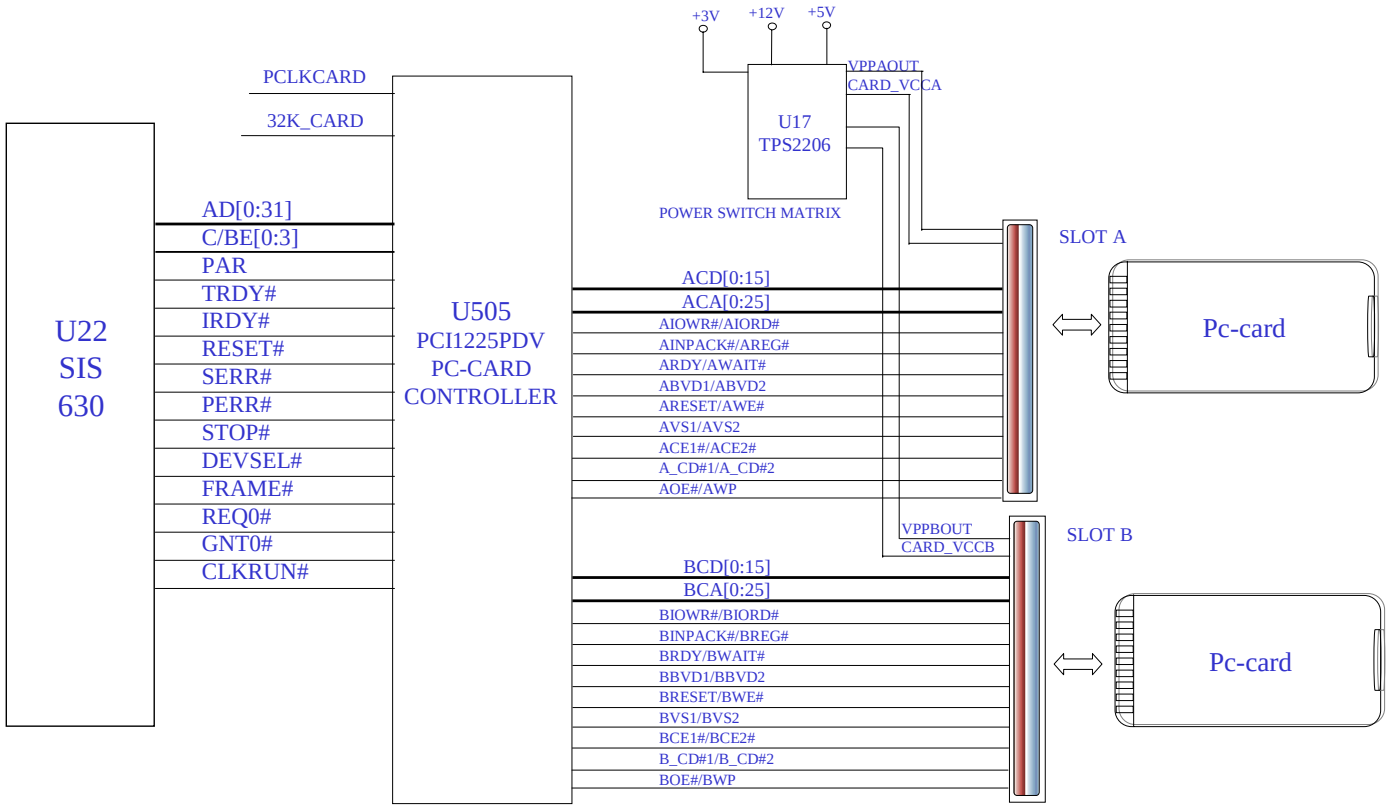
7.12 PIO PORT TEST ERROR

When a print command is issued, printer prints nothing or garbage.



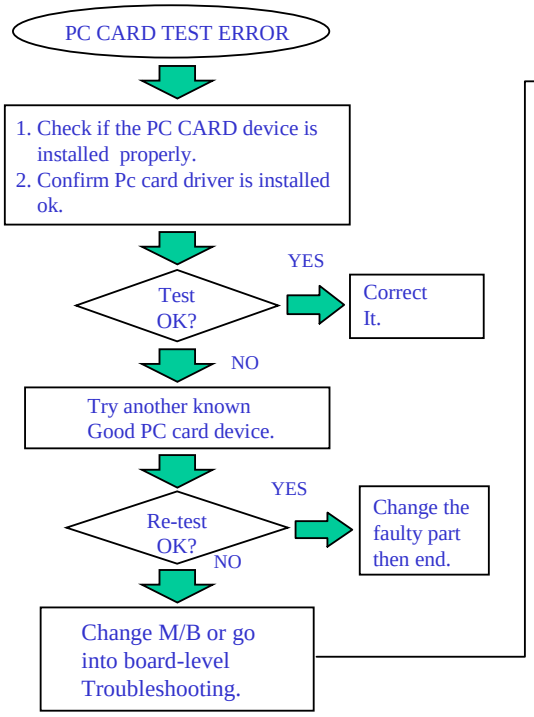
7.13 PC-CARD SOCKET FAIL

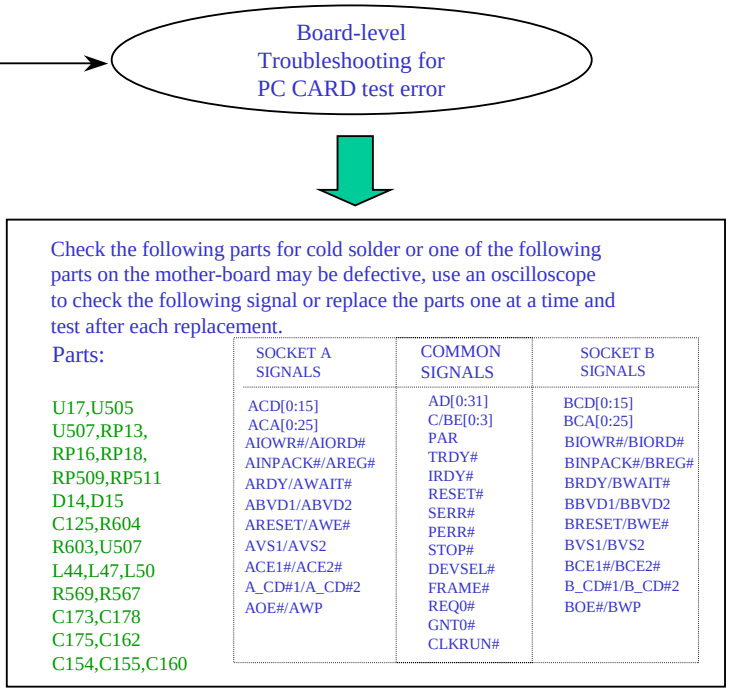
An error occurs when a PC card device is installed.

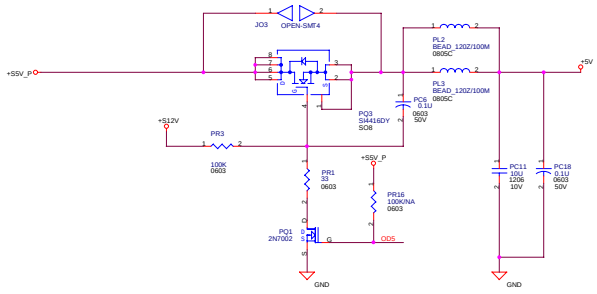


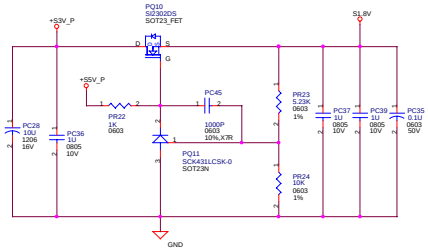
7.13 PC-CARD SOCKET FAIL

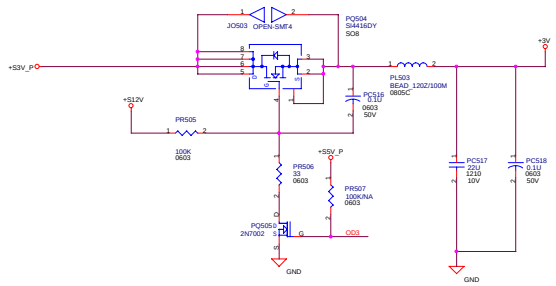
An error occurs when a PC card device is installed.

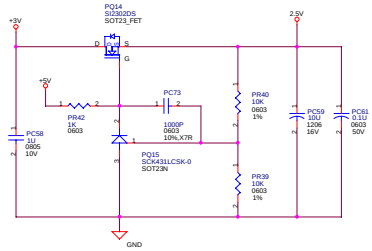


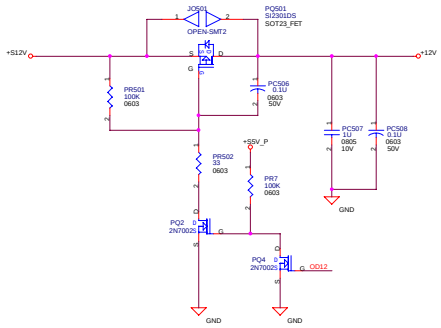


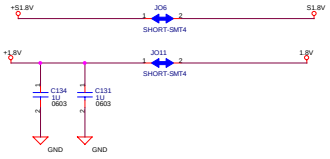


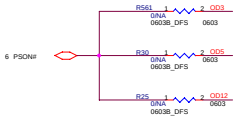












MiTAC

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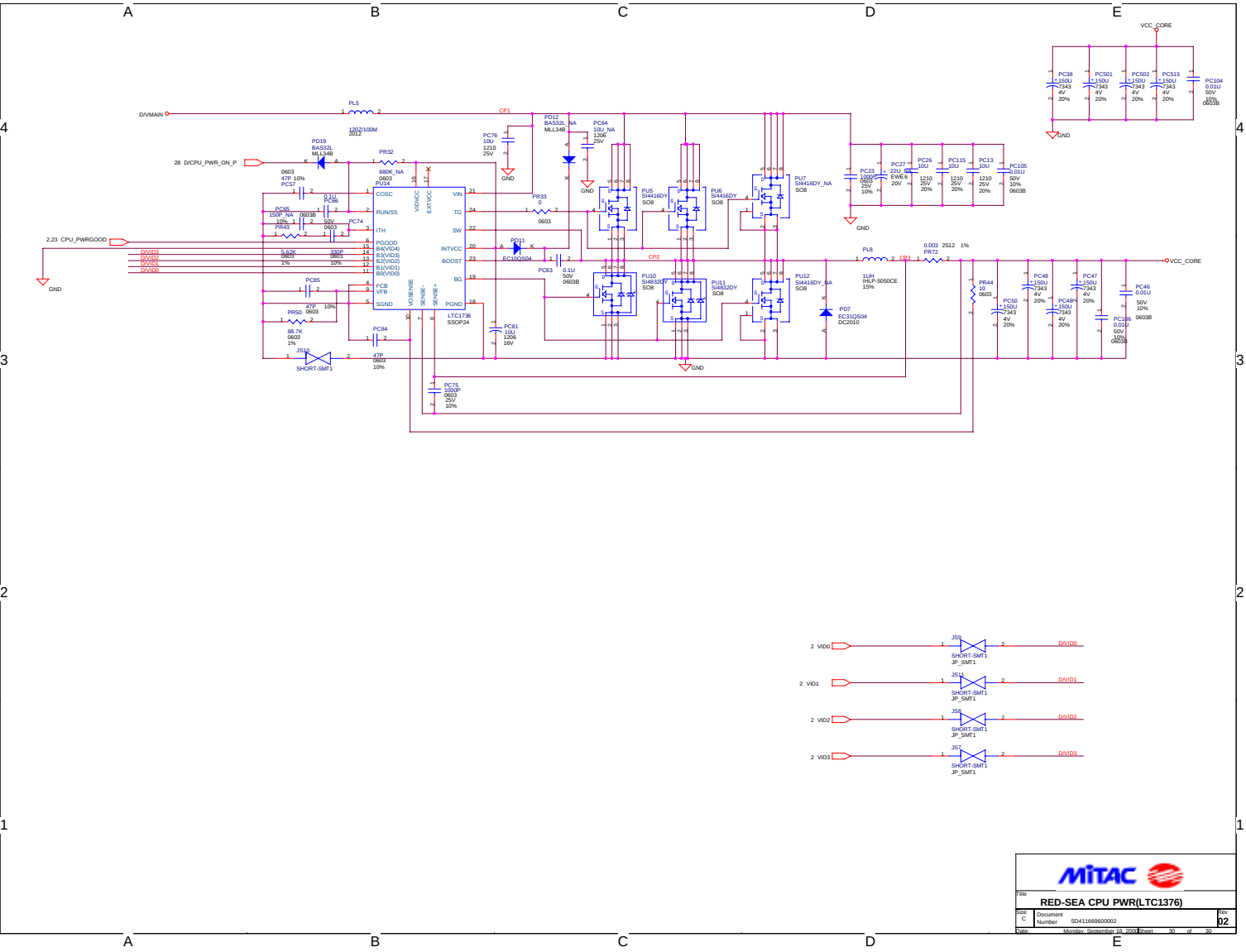

MiTAC

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