SERVICE MANUAL FOR

7321

BY: Jacey Liu

TESTING TECHNOLOGY DEPARTMENT / TSSC

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MiTAC

7321 N/B Maintenance

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1.Hardware Engineering Specification

1.1 Introduction

The 7321 model motherboard would support the AMD K7 processor with CPGA packaged,socket A,which will supports the different levels of AMD K7 CPU with CPGA package,Including Athlon 650/700/750/800/900/1000 MHz,and Duron 600/650/700/750/800/900 MHz.

This system is based on PCI architecture which have standard hardware peripheral interface. The power management complies with Advanced Configuration and Power Interface (ACPI) 1.0. It also provides easy configuration through CMOS setup, which is built in system BIOS software and can be pop-up by pressing F2 at system start up or warm reset. System also provides icon LEDs to display system status, such as Power indicator, LAN, HDD/CDROM, NUM LOCK,CAP LOCK, SCROLL LOCK, SUSPEND MODE and Battery charging status. It also equipped with Zoom Video capture port, FIR, 2 USB ports.

The memory subsystem supports 64MB SDRAM on board and one 144 pin SO-DIMM socket for upgrading up to maximum 320MB of DRAM using PC-100 or PC-133 SDRAM SO-DIMM module.

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The TwisterK integrates VIA's VT8362 KN133 system controller,S3's Savage4 2D/3D graphics accelerator and S3's flat panel interfaces into a single 552 BGA package. The TwisterK SMA system controller provides superior performance between the CPU,DRAM and PCI bus with, pipelined,burst and concurrent operation.

Savage4 graphic accelerator integrated in TwisterK brings mainstream graphics performance with leading-edge 2D,3D and DVD video acceleration .Also with a new super-pipelined 128-bit engine for utilizing a single cycle architecture that provides high performance along with superior image quality.Several new features enhance the 3D architecture,including single-pass multitexturing, full scene anti-aliasing,anisotropic filtering,and an 8-bit stencil buffer.It also offers the industry's only simultaneous usage of single-pass multitexturing and single-cycle trilinear filtering – enabling stunning image quality without performance loss.

The 352-pin VT8231 BGA PCI-LPC bridge supports four levels(doublewords) of line buffers,type F DMA transfers and delay transaction to allow efficient PCI bus utilization and (PCI-2.2 compliant) The VT8231 also includes an integrated Super I/O,integrated DS12885 style real time clock with extended 256 byte CMOS RAM,integrated master mode enhanced IDE controller with full scatter/gather capability and extension to UltraDMA-33/66/100 for 33/66/100 MB/sec transfer rate,integrated four

capability and extension to UltraDMA-33/66/100 for 33/66/100 MB/sec transfer rate,integrated four USB interface with root hub and two function ports with built-in physical layer transceivers,Distributed DMA support, integrated AC-97 link for basic audio and HSP based modem functions,integrated hardware monitoring and On Now / ACPI compliant advanced configuration and power management interface.The VT8231 also has an integrated MAC and 10Mbit PHY for LAN connection.It can bypass the internal PHY with external home PNA with a 1Mbit PHY or a 10/100Mbit PHY through the MII interface.

A full set of software drivers and utilities are available to allow advanced operating systems such as Windows 98/millennium to take full advantage of the hardware capabilities such as bus mastering IDE, Windows 95-ready Plug & Play, Advanced Power Management (APM) and Advance configuration and power interface (ACPI)

1.2 System Hardware Parts

- Central Processing Unit

  AMD K7 microprocessors in CPGA package

- System frequency synthesizer

  ICS9248-193

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- Core Logic
  VIA KN133+VT8231:CPU/PCI and CPU/AGP bridge with memory/AGP/LAN/IDE/USB/PMU and Super I/O controller
- LAN—PHY
  ICS1893
- PC Card Interface Controller
  EnE CB-1420
- Dual–Slot PC Card Power Interface Switch
  EnE CP-2216
- AC’97 AUDIO SYSTEM
  CRYSTAL CS 4299
- 1394
  NEC uPD72872
- IR MODULE
  HP HSDL-3600#007
- Keyboard System
  HITACH H8(3434) Universal Keyboard Controller

- System Flash Memory(BIOS)
- Memory System(PC-133 compliance)

1.2.1 CPU_AMD K7(Athlon / Duron) Processor

- The industry's first nine-issue,superpiplined,superscalar x86 processor micro architecture designed for high clock frequencies
- Multiple x86 instruction decoders
- Fully pipelined floating-point execution unit which executes all x87(floating point),MMX and 3Dnow! instructions
- Three out-of-order,superscalar,pipelined address calculation units
- Three out-of-order,superscalar,pipelined integer units
- 72-entry instruction control unit
- Advanced dynamic branch prediction
- Enhanced 3Dnow! technology with new instructions to enable improved integer math calculations for speech or video encoding and improved data movement for internet plug-ins and other streaming applications
- 200-MHz AMD Athlon System Bus (scalable beyond 400 MHz) enabling leading-edge system bandwidth for data movement-intensive applications
- High-performance cache architecture featuring an integrated 128Kbytes L1(both Athlon and Duron) cache and a 256Kbytes (64Kbytes for Duron) L2 cache

1.2.2 System frequency synthesizer_ICS9248-193

- 1 – Differential pair open drain CPU clocks
- 1 – CPU clock @ 3.3V
- 7 – SDRAM @ 3.3V
- 8 – PCI @ 3.3V
- 1 – 48MHz @ 3.3V fixed
- 1 – 24/48MHz @ 3.3V
- 3 – REF @ 3.3V, 14.318MHz
- Up to 166MHz frequency support
- Support power management via hardware select CPU stop, PCI stop, and SDRAM stop
- Support power management via I^2C programming
- Spread spectrum for EMI control (±0.25% to ±0.06% center, or 0 to –0.5% or –1.0% down spread)
- Uses external 14.318MHz crystal
- CPU – CPU Skew: <175ps
- CPU – SDRAM Skew: ±125ps
- CPU – PCI Skew: ±100ps
- PCI – PCI Skew: <500ps

1.2.3 Core Logic_VT8362 + VT8231

1.2.3.1 VT8362

- **Defines Integrated Solutions for Value PC Mobile Designs**

  --High performance SMA North Bridge : Integrated VIA Apollo KT133 and S3® Savage4™ in a single chip

  --64-bit Advanced Memory controller supporting PC100/PC133 SDRAM and VRM

  --Combines with VIA VT82C686A/B PCI-ISA South Bridge for state-of-the-art power management2

- **High Performance CPU Interface**

  --Socket-A and Slot A support for AMD® Athlon™ processors (pinout optimized for Socket-A)

  --200 or 266 MHz CPU Front Side Bus (FSB)

  --Built-in Phase Lock Loop circuitry for optimal skew control within and between clocking regions

  --Five outstanding transactions(four In-Order Queue(IOQ)plus one output latch)

  --Dynamic deferred transaction support

- **Advanced High-Performance DRAM Controller**

  --DRAM interface runs synchronous(66/266,100/200,133/266)mode or pseudo- synchronous (66/200,100/266,133/200)mode with FSB

  --Concurrent CPU,internal AGP,and PCI access

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--Supports SDRAM and VCM SDRAM memory types

--Supports 3 DIMMs or 6 banks for up to 1.5 GB of DRAM(256Mb DRAM technology)

--64-bit data width

--Supports maximum 8-bank interleave(8 pages open simultaneously);banks are allocated based on LRU

- **Integrated Savage4 2D/3D/Video Accelerator**

--Optimized Shared Memory Architecture(SMA)

--8/16/32 MB frame buffer using system memory

--Floating point triangle setup engine

--Single cycle 128-bit 3D architecture

--8M triangles/second setup engine

--140M pixels/second trilinear fill rate

--Full internal AGP 4x performance

--S3 DX7 texture compression(S3TC™)

--Next generation,128-bit 2D graphics engine

--High quality DVD video playback

--Flat panel monitor support

--2D/3D resolutions up to 1920x1440

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- **3D Rendering Features**

  --Single-pass multiple textures

  --Anisotropic filtering

  --8-bit stencil buffer

  --32-bit true color rendering

  --Specular lighting and diffuse shading

  --Alpha blending modes

  --Massive 2Kx2K textures

  --MPEG-2 video textures

  --Vertex and table fog

  --16 or 24-bit Z-buffering

  --Sprite anti-aliasing,reflection mapping,texture morphing,shadows,proceduraltextures and atmospheric effects

- **2D Hardware Acceleration Features**

  --ROP3 Ternary Raster Operation BitBLTs

  --8,16,and 32 bpp mode acceleration

- **Motion Video Architecture**

  --High quality up/down scaler

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--Planar to packed format conversion

--Motion compensation for full speed DVD playback

--Hardware subpicture blending and highlights

--Multiple video windows for video conferencing

--Contrast,hue,saturation,brightness and gamma controls

--Digital port for NTSC/PAL TV encoders

- **Extensive LCD Support**

--36-bit DSTN/TFT flat panel interface with 256 gray shade support

--Integrated 2-channel 110 MHz LVDS interface

--Support for all resolutions up to 1600x1200

--ZV-Port Interface

--Panel power sequencing

--Hardware Suspend/Standby control

- **Flat Panel Monitor Support**

--12-bit TFT flat panel interface to TMDS encoders

--Digital Visual Interface(DVI)1.0 compliant

- **Concurrent PCI Bus Controller**

--PCI 2.2 compliant,32-bit 3.3V PCI interface with 5V tolerant inputs

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--Supports up to 5 PCI masters

--PCI to system memory data streaming support

--Delay transaction from PCI master accessing DRAM

--Symmetric arbitration between Host/PCI bus for optimized system performance

- **Advanced System Power Management Support**

--Dynamic power down of SDRAM(CKE)

--Independent clock stop controls for CPU/SDRAM,AGP,and PCI bus

--PCI and AGP bus clock run and clock generator control

--VTT suspend power plane preserves memory data

--Suspend-to-DRAM and self-refresh power down

--Low-leakage I/O pads

--ACPI 1.0B and PCI Bus Power Management 1.1 compliant

- **Full Software Support**

--Drivers for major operating systems and APIs:[Windows® 9x,Windows NT 4.0,Windows 2000,Direct3D™,DirectDraw™ and DirectShow™,OpenGL™ ICD for Windows 9x,NT and 2000]

--North Bridge/Chipset and Video BIOS support

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- **Additional Features**

  --250 MHz RAMDAC with Gamma Correction

  --12-bit interface to external TV encoder

  --I^2C Serial Bus and DDC Monitor Communications

  --2.5V Core and Mixed 3.3V/5V Tolerant and GTL+I/O

  --35x35mm PBGA package with 552 balls

1.2.3.2 VT8231

- **Inter-operable with VIA and other Host-to-PCI Bridges**

  --Combine with VT82C598 for a complete Super-7(66/75/83/100MHz)AGP 2x system(Apollo MVP3)

  --Combine with VT8501 for a complete Super-7 system with integrated 2D/3D graphics(Apollo MVP3)

  --Combine with VT82C694X for a complete 66/100/133 MHz Socket370 / Slot1 AGP 4x system (Apollo Pro133A)

  --Combine with VT8601 for a complete 66/100/133 MHz Socket370/Slot1 system with integrated 2D/3Dgraphics(Apollo ProMedia)

  --Inter-operable with Intel or other Host-to-PCI bridges for a complete PC99 compliant PCI/AGP/LPC system

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- **Integrated Peripheral Controllers**
  - --Integrated Fast Ethernet Controller with 1/10/100 Mbit capability
  - --Integrated USB Controller with two root hub and four function ports
  - --Dual channel UltraDMA-33/66/100 master mode EIDE controller
  - --AC-link interface for AC-97 audio codec and modem codec
  - --HSP modem support
  - --Integrated SoundBlasterPro/DirectSound compatible digital audio controller
  - --LPC interface for Low Pin Count interface to Super-I/O or ROM
- **Integrated Legacy Functions**
  - --Integrated Keyboard Controller with PS2 mouse support
  - --Integrated DS12885-style Real Time Clock with extended 256 byte CMOS RAM and Day/ Month Alarm for ACPI
  - --Integrated Bus Controller including DMA,timer,and interrupt controller
  - --Serial IRQ for docking and non-docking applications
  - --Flash EPROM,32Mbit(4Mbyte)EPROM and combined BIOS support
  - --Fast reset and Gate A20 operation
- **Integrated Peripheral Controllers**
  - --Integrated Fast Ethernet Controller with 1/10/100 Mbit capability

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--LPC interface for Low Pin Count interface to Super-I/O or ROM

- **Fast Ethernet Controller**

--High performance PCI master interface with scatter/gather and bursting capability

--Standard MII interface to Ethernet or HomePNA PHYceiver

--1/10/100 MHz full and half duplex operation

--Transmit data buffer byte alignment for low CPU utilization

--Separate 2K byte FIFOs for receive and transmit of full Ethernet packets

--Flexible dynamically loadable EEPROM algorithm

--Physical,Broadcast,and Multicast address filtering using hashing function

--Flexible wakeup events: link status change,magic packet,unicast physical address match, predefined pattern match

--Software controllable power down

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- **UltraDMA-33/66/100 Master Mode PCI EIDE Controller**

  --Dual channel master mode PCI supporting four Enhanced IDE devices

  --Transfer rate up to 100MB/sec to cover up to PIO mode 4,multi-word DMA mode

  --Thirty-two levels(doublewords)of prefetch and write buffers per channel

  --Dual DMA engine for concurrent dual channel operation

  --Bus master programming interface for SFF-8038i rev.1.0 and Windows-95/98/2000 compliant

  --Support ATAPI compliant devices including DVD devices

  --Support PCI native and ATA compatibility modes

  --Complete software driver support

- **Integrated Super IO Controller**

  --Supports serial port,IR port,parallel port,and floppy disk controller functions

  --Serial Port

  Programmable character lengths(5,6,7,8)

  Even,odd,stick or no parity bit generation and detection

  Programmable baud rate generator

  High speed baud rate(230Kbps,460Kbps)support

  Independent transmit/receiver FIFOs

  Modem Control

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Plug and Play with 96 base IO address and 12 IRQ options

--Fast IR(FIR)port

IrDA 1.0 SIR and IrDA 1.1 FIR compliant

IR function through the second serial port

Infrared-IrDA(HPSIR)and ASK(Amplitude Shift Keyed)IR

--Multi-mode parallel port

Standard mode,ECP and EPP support

Dynamic and static switch between parallel port pinout and FDC pinout

Plug and play with 192 base IO address,12 IRQ and 4 DMA options

--Floppy Disk Controller

16 bytes of FIFO

Data rates up to 1 Mbps

Prependicular recording driver support

Two FDDs with drive swap support

Plug and play with 48 base IO address,12 IRQ and 4 DMA options

- **Low Pin Count(LPC)Bus Interface**

--Provides connection to external LPC I/O controllers and LPC BIOS ROMs

--Enables removal of legacy ISA bus and related pins

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--Low pin count interface:two control pins and four address/data pins

- **SoundBlaster Pro Hardware and Direct Sound Ready AC97 Digital Audio Controller**

  --Dual full-duplex Direct Sound channels between system memory and AC97 link

  --PCI master interface with scatter/gather and bursting capability

  --32 byte FIFO of each direct sound channel

  --Host based sample rate converter and mixer

  --Standard v1.0 or v2.0 AC97 Codec interface for single or cascaded AC97 Codec's from multiple vendors

  --Loopback capability for re-directing mixed audio streams into USB and 1394 speakers

  --Hardware SoundBlaser Pro for Windows DOS box and real-mode DOS legacy compatibility

  --Plug and play with 4 IRQ,4 DMA,and 4 I/O space options for SoundBlaster Pro and MIDI hardware

  --Hardware assisted FM synthesis for legacy compatibility

  --Direct two game ports and one MIDI port interface

  --Complete software driver support for Windows-95/98/2000 and Windows-NT

- **MC97 HSP Modem Controller**

  --PCI bus master interface with scatter/gather and burst capability

--Standard AC97 codec interface for MC or AMC codec

--Wake on ring in APM or ACPI mode through AC97 link

--Supported by most HSP modem vendors

- **Universal Serial Bus Controller**

--USB v1.1 and Intel Universal HCI v1.1 compatible

--Eighteen level (doublewords)data FIFO with full scatter and gather capability

--Root hub and four function ports

--Integrated physical layer transceivers with optional over-current detection status on USB inputs

--Legacy keyboard and PS/2 mouse support

- **System Management Bus Interface**

--One master/slave SMBus and one slave-only SMBus

--Host interface for processor communications

--Slave interface for external SMBus masters

1.2.4 PC Card Interface Controller_TI PCI1420

- **A 208-Pin Low-Profile QFP(PDV)or MicroStar Ball Grid Array(GHK)package**
- **3.3-V core logic with universal PCI interfaces compatible with 3.3-V and 5-V PCI signaling environments**

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- Mix-and-match 5-V/3.3-V 16 bit PC Cards and 3.3-V CardBus Cards
- Two PC Card or CardBus slots with hot insertion and removal
- Uses serial interface to TI™ TPS2206/2216 dual-slot PC Card power switch
- Burst transfers to maximize data throughput with CardBus Card
- Parallel PCI interrupts,parallel ISA IRQ and parallel PCI interrupts,serial ISA IRQ with parallel PCI interrupts,and serial ISA IRQ and PCI interrupts
- Serial EEPROM interface for loading subsystem ID and subsystem vendor ID
- Pipelined architecture allows greater than 130Mbps throughput from CardBus-to-PCI and from PCI-to-CardBus
- Up to five general-purpose I/Os
- Programmable output select for #CLKRUN
- Multifunction PCI device with separate configuration space for each socket
- Five PCI memory windows and two I/O windows available for each R2 socket
- Two I/O windows and two memory windows available to each CardBus socket
- Exchangeable Card Architecture(ExCA) compatible registers are mapped in memory and I/O space
- Intel 82365SL-DF and 82365SL register compatible
- Distributed DMA(DDMA) and PC/PCI DMA

- **16-bit DMA on both PC Card sockets**
- **Ring indicate,#SUSPEND,PCI #CLKRUN,and CardBus#CCLKRUN**
- **Socket activity LED pins**
- **PCI Bus Lock(#LOCK)**
- **Advanced Submicron,Low-Power CMOS Technology**
- **Internal Ring Oscillator**

1.2.5 LAN—PHY_LSI80227

- **Supports category 5 cables with attenuation in excess of 24 dB at 100 MHz across a temperature range from -5℃ to +85℃**
- **DSP-based baseline wander correction to virtually eliminate killer packets across temperature range of from -5℃ to +85℃**
- **Low-power, 0.35-micron CMOS (typically 400 mW)**
- **Single 3.3-V power supply**
- **Single-chip, fully integrated PHY provides PCS, PMA, PMD, and AUTONEG sublayers of IEEE standard**
- **10Base-T and 100Base-TX IEEE 802.3 compliant**

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- **Fully integrated, DSP-based PMD includes:**
- **10Base-T and 100Base-TX IEEE 802.3 compliant**
- **Fully integrated, DSP-based PMD includes:**
  --Adaptive equalization and baseline wander correction
  --Transmit wave shaping and stream cipher scrambler
  --MLT-3 encoder and NRZ/NRZI encoder
- **Highly configurable design supports:**
  --Node, repeater, and switch applications
  --Managed and unmanaged applications
  --10M or 100M half- and full-duplex modes
  --Parallel detection
  --Auto-negotiation, with Next Page capabilities
- **MAC/Repeater Interface can be configured as**
  --10M or 100M Media Independent Interface
  --100M Symbol Interface (bypasses the PCS)
  --10M 7-wire Serial Interface
- **Small Footprint 64-pin Thin Quad Flat Pack(TQFP)**

1.2.6 Dual-Slot PC Card Power-Interface Switch_TPS2216

- **Fully integrated Vcc and Vpp switching for dual-slot PC Card™ interface**
- **P^2C™ 3-Lead Serial Interface compatible with CardBus™ controllers**
- **3.3 V low-voltage mode**
- **Meets PC Card standards**
- **RESET for system initialization of PC Cards**
- **12-V supply can be disabled except during 12-V flash programming**
- **Short circuit and thermal protection**
- **30-Pin SSOP(DB) and 32-Pin TSSOP(DAP)**
- **Compatible with 3.3-V,5-V and 12-V PC Cards**
- **Low $r_{DS(ON)}$(140-mΩ 5-V Vcc switch;110-mΩ 3.3-V Vcc switch)**
- **Break-Before-Make switching**

1.2.7 AC'97 AUDIO SYSTEM: CRYSTAL CS4299

The AC'97 CODEC provides a complete high quality audio solution, feature include :

- **20-bit Stereo Digital-to-Analog Converter and 18-bit Stereo Analog to Digital Converter with Sample Rate Conversion**

- **Four Analog Line-level Stereo Inputs for Connection from LINE IN, CD, VIDEO, and AUX**
- **Two Analog Line-level Mono Inputs for Modem Sub-system and Internal PC Beeper**
- **Mono Microphone Input Switch able from Two External Sources**
- **High Quality Pseudo Differential CD Input**
- **Dual Stereo Line-level Outputs**
- **CrystalClear 3D Stereo Enhancement**

1.2.8 IR MODULE : HP HSDL-3600

- **Fully Compliant to IrDA 1.1 Specifications**

  --9.6 kb/s to 4 Mb/s operation

  --Excellent nose-to-nose operation
- **Typical Link Distance > 1.5 m**
- **Compatible with ASK, HP-SIR, and TV Remote**
- **IEC825-Class 1 Eye Safe**
- **Wide Operating Voltage Range**

  -- 2.7 V to 5.25 V
- **Small Module Size**

  -- 4.0 x 12.2 x 5.1 mm (HxWxD)

- **Complete Shutdown**

  --TXD, RXD, PIN diode

- **Low Shutdown Current**

  --10 nA typical

- **Adjustable Optical Power Management**

- **Single Rx Data Output**

  -- FIR Select pin switch to FIR

- **Integrated EMI Shield**

  -- Excellent noise immunity

- **Edge Detection Input**

  -- Prevents the LED from long turn-on time

  Interface to Various Super I/O and Controller Devices Designed to accommodate Light Loss with Cosmetic Window Only 2 External components are Required

1.2.9 Keyboard System : HITACH H8(3434F) Universal Keyboard Controller

- **CPU:**

  -- Two-way general register configuration

  -- Eight 16-bit registers or Sixteen 8-bit registers

  -- High-speed operation

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-- Maximum clock rate : 16Mhz at 5V

- **Memory**

  -- include 32KB ROM and 1KB RAM

- **16-bit free-running timer**

  -- One 16-bit free-running counter

  -- Two output-compare line

  -- Four input capture lines

- **8-bit timer (2 channels)**

  -- Each channel has one 8-bit up-counter , two time constant registers

- **PWM timer (2 channels)**

  -- resolution :1/250

  -- Duty cycle can be set from 0 to 100% at 5V

- **I^2C bus interface (one channel)**

  -- include single master mode and slave mode

- **Host interface (HIF)**

  -- 8-bit host interface port

  -- Three host interrupt requests (HIRQ1,11,12)

  -- Regular and fast A20 gate output

- **Keyboard controller**

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-- Interrupts and sense ports

-- Controls a matrix-scan keyboard by providing a keyboard scan function with wake-up

- **A/D converter**

  -- 10-bit resolution

- **D/A converter**

  -- 8-bit resolution

  -- 2 channels

- **Interrupts**

  -- nine external interrupt lines : NMI# , IRQ0 to 7#

  -- 26 on-chip interrupt sources

- **Power-down modes**

  -- Software standby mode

  -- Sleep mode

- **Hardware standby mode**

- **A single chip microcomputer**

- **On-chip flash memory**

- **Maximum 64-kbyte address space**

- **Support three PS/2 port for external keyboard, mouse and internal track pad.**

- **Support SMI,SCI trigger input:**
- **Cover switch**
- **Battery charging control**
- **Smart Battery monitoring**
- **Fan control and LED indicator serial interface**
- **Control D/D system on/off**
- **100pin TQFP**

1.2.10 System Flash Memory (BIOS)

- **2M bit Flash memory**
- **Flashed by 5V only**
- **User can upgrade the system BIOS in the future just running flash program**

1.2.11 Memory System

1.2.11.1 On Board Main Memory

- **Up to PC-133 SDRAM on board**
- **4Mx16bit SDRAM x8 pcs. Total 64Mbyte**
- **Standard 54 pin TSOPII package.**

- **Power supply: 3.3V±0.3V**
- **Memory bus bandwidth: 64 bits**

1.2.11.2 JEDEC 144-pin SO DIMM sockets

- **Supports one JEDEC 144-pin SO DIMM socket on Mother Board for expansion**
- **Supports 3.3V SDRAM**
- **Banks on one socket**
- **Up to PC-133 DIMM Module**

1.3 Other Functions

1.3.1 Hot Key Function

Keys Combination	Feature	Meaning
Fn + F5	LCD/external CRT switching	Rotate display mode in LCD only, CRT only and simultaneously
Fn + F6	Brightness down	Decreases the LCD brightness/No function in DSTN model
Fn + F7	Brightness up	Increases the LCD brightness/No function in DSTN model
Fn + F10	Enable/Disable BatteryWarning Beep	Toggle Battery Warning on/off
Fn + F11	Panel Off/On	Toggle Panel Off/On
Fn + F12	Suspend to DRAM/HDD	Force the computer into either Suspend to HDD or Suspend to DRAM mode depending on BIOS Setup

1.3.2 Quick Key Function

Keys	Feature	Meaning
QSB1	Entertainment Quick Key	Determined by SW component
QSB2	Instant Internet	Determined by SW component
QSB3	My Presario	Determined by SW component
QSB4	Search	Determined by SW component
QSB5	Email	Determined by SW component

1.3.3 Flash ROM (BIOS)

7321system utilizes the state-of-the-art Flash EEPROM technology.User can upgrade the system BIOS in the future just running the program from MiTAC.

1.3.4 LED Indicators

System has nine status LED indicators to display system activity which include above keyboard and below touch pad:

- **Three LED indicators below touch pad:**

--AC POWER:

This LED lights green when the notebook is being powered by AC, and flash (on 1 second, off one

second) when Suspend to DRAM is active using AC power. The LED is off when the notebook is off or powered by batteries, or when Suspend to Disk.

--BATTERY POWER:

This LED lights green when the notebook is being powered by batteries, and flashes (on one second, off one second) when suspend to DRAM is active using battery power. The LED is off when the notebook is off or powered by AC, or when Suspend to Disk.

--BATTERY STATUS:

During normal operation, this LED stays off as long as the battery is charged. When the battery charge drops to 10 % of capacity, the LED lights red, flashes per 1 second and beeps per 2 seconds. When AC is connected, this indicator glows green if the battery pack is fully charged, or orange (amber) if the battery is being charged.

- **Six LED indicators above keyboard:**

  From left to right that indicates CD-ROM/MO, HARD DISK DRIVE, FLOPPY DISK DRIVE, NUM LOCK, CAPS LOCK and SCROLL LOCK.

1.3.5 COM port assignment

- **COM1: MODEM/RS-232/Disable**

- **COM2: IR/RS-232/Disable**

1.3.6 Reset switch

There is a reset switch at bottom side of notebook. It will reset embedded controller H8 and turn off system totally. This switch was used when H8 hangs up at that time you cannot turn system off.

1.3.7 CMOS Battery

- CR2032 3V 220mAh lithium battery
- When AC in or system main battery inside, CMOS battery will consume no power.
- AC or main battery not exist, CMOS battery life depends on VT8231 RTC power consumption.
- Battery was put in battery holder, can be replaced.

1.3.8 I/O Port

- **Bidirectional Parallel port (EPP/ECP)**
- **VGA monitor port**
- **PS/2 port (active at the same time)**
- **FIR port**
- **2 USB ports**

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- **Serial port**
- **DC input**
- **Microphone port**
- **S-Video Out Port (NTSC/PAL) (Optional)**
- **Line-in port**
- **Line-out port (metal I/F; w/o S/PDIF)**
- **RJ-45 port (Optional)**
- **RJ-11 port (Optional)**

1.4 Peripheral Components

7321 Peripheral Components

	BRAND	MODEL NAME
LCD PANEL	Hyundai	14.1”TFT XGA, HT14X13-101
Floppy Disk Drive	Mitsumi	D353G
HDD	Hiyachi(2.5” 9.5mmH)	20GB— DK23BA-20
CD-ROM Drive	TEAC	CD-224E-A92/B92
CDR-RW	KME	UJDA320/330
DVD-ROM drive	Pioneer	8XDVD-ROM-DVD-K11TA
Pointing Device	Synaptics	TM41PUM220
PCMCIA	TI	PCI1225PDV
Fax Modem	Askey	V1456VQL-P1

Appendix 1: VT8231 GPIO definitions

Group	Pin #	Pin Name	Multi Func.	GPIO	Group	Pin Define in 7321
Strapping						
		SA16	0/1 - Disable/enable LPC ROM			0 - Disable LPC ROM
		SUSA#	0/1 - CPURST/INIT polarity			1 - Socket 462
		MCCS#	0/1 - Enable/disable CPU FREQ strapping			1 - Disable FREQ strap
		SA17	0/1 - Enable/disable auto reboot			1 - Disabe auto reboot
GPI			mux with	Register setting	default	
	F4	**GPI0**	GPI0	N/A		GPI0
	V3	**GPI1**	GPI1	N/A		GPI1
	W1	**GPI2**	EXTSMI#	N/A		EXTSMI#
	U3	**GPI3**	RING#	N/A		WAKEUP#
	V2	**GPI4**	LID	N/A		GPI4
	T3	**GPI5**	BATLOW#	N/A		GPI5
	U1	**GPI6**	PME#	N/A		PME# & SCI# (from H8)
	T2	**GPI7**	SMBALT#	N/A		GPI7
	F3	**GPI8**	INTRUDER#	N/A		GPI8

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	Y3	**GPI9**		~f0_rx58<6>		GPI9
			APICCLK	f0_rx58<6>		
	Y11	**GPI10**		f4_rxe5<3>		PANEL_ID0
			HREQ1#	~f4_rxe5<3>		
	V11	**GPI11**		f4_rxe5<3>		PANEL_ID1
			HREQ2#	~f4_rxe5<3>		
	U10	**GPI12**		f4_rxe5<2>		PANEL_ID2
			LREQ1#	~f4_rxe5<2>		
	W10	**GPI13**		f4_rxe5<2>		PANEL_ID3
			LREQ2#	~f4_rxe5<2>		
	V4	**GPI14**		~f0_rx58<7> & ~f0_rx58<6>		MB_ID0
			WSC#	f0_rx58<7>		
			APICREQ#	f0_rx58<6>		
	Y8	**GPI15**		~f0_rx58<5> & ~f4_rxe5<7>		MB_ID1
			LDRQ#	f0_rx58<5>		
			ACSIN3	~f0_rx58<5> & f4_rxe5<7>		
	V1	**GPI16**	CPUMISS	N/A		CARD_IN#
	P3	**GPI17**		f4_rx40<7>		THRM#
			AOLGPI	f4_rx40<7>		
			THRM	~f4_rx40<7>		
	K3	**GPI18**		~f4_rxe5<0>		GPI18
			GPO18	f4_rxe5<0>		
			FAN2	f4_rxe5<0>		
			SLPBTN#	f4_rx40<6>		
	G5	**GPI19**		~f4_rxe4<5> & ~f4_rxe5<1>		GPI19

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			GPO19	f4_rxe5<1> & f4_rxe4<5>			
			ACSDIN2	~f4_rxe4<5>			
	W13	**GPI20**		~f4_rxe4<6> & pmio_rx4e<4>	OD	GPI20	
			GPO20	~f4_rxe4<6>			
			LA20	f4_rxe4<6>			
			USBOC2#	~f4_rxe4<6> & pmio_rx4e<4>			
	Y13	**GPI21**		~f4_rxe4<6> & pmio_rx4e<5>	OD	SPK_OFF	
			GPO21	~f4_rxe4<6>			
			LA21	f4_rxe4<6>			
			USBOC3#	~f4_rxe4<6> & pmio_rx4e<5>			
	U7	**GPI22**		~f4_rxe4<7> & pmio_rx4e<6>	OD	IOR#	
			GPO22	~f4_rxe4<7>			
			IOR	f4_rxe4<7>			
	T7	**GPI23**		~f4_rxe4<7> & pmio_rx4e<7>	OD	IOW#	
			GPO23	~f4_rxe4<7>			
			IOW	f4_rxe4<7>			
	Y2	**GPI24**		~f4_rxe6<0>	GPI	AGP_BUSY#	
			GPO24	f4_rxe6<0>			
			GPIOA	~/f4_rxe6<0>			
	J5	**GPI25**		~f4_rxe6<1>	GPI	VGA_SUS ?	
			GPO25	f4_rxe6<1>			
			GPIOC	~/f4_rxe6<1>			
			~~ATEST~~	?			
	R2	**GPI26**		f4_rx55<2> & ~f4_rx55<3>	GPI	CARD_ACT#	
			GPO26	f4_rx55<2> & f4_rx55<3>			

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			SMBDT2	~f4_rx55<2>		
	R1	**GPI27**		f4_rx55<2> & ~f4_rx55<3>	GPI	GPO27
			GPO27	f4_rx55<2> & f4_rx55<3>		
			SMBCK2	~f4_rx55<2>		
	G3	**GPI28**		audio ena & game disa		KB_US/JP#
			JAB1	audio ena & game ena		
	F1	**GPI29**		audio ena & game disa		GPI29
			JBB1	audio ena & game ena		
	Y1	**GPI30**		~f4_rxe6<6>	GPI	GPO30
			GPO30	f4_rxe6<6>		
			GPIOD	~/f4_rxe6<6>		
			~~DTEST~~	?		
	W3	**GPI31**		~f4_rxe6<7>	GPI	GPO31
			GPO31	f4_rxe6<7>		
			GPIOE	~/f4_rxe6<7>		
GPO			mux with	Register setting	default	
	R4	**GPO0**		f4_rx54[1-0]=00 & PMIO_rx4c[0]	GPO0	SLOWCLK
			SLOWCLK	f4_rx54[1-0]=01,10,11		
	P1	**GPO1**		f4_rx54<2>	SUSA#	SUSA#
			SUSA#	~f4_rx54<2>		
	P2	**GPO2**		f4_rx54<3>	SUSB#	SUSB#
			SUSB#	~f4_rx54<3>		

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	N5	**GPO3**		f4_rx54<4>	SUSSTAT#	SUSSTAT#
			SUSSTAT#	~f4_rx54<4>		
	W2	**GPO4**		f4_rx55<1>	SUSCLK	SUSCLK
			SUSCLK	~f4_rx55<1>		
	P4	**GPO5**		f4_rxe4<0>	CPUSTP#	CPUSTP#
			CPUSTP#	~f4_rxe4<0>		
	T4	**GPO6**		f4_rxe4<1>	PCISTP#	PCISTP#
			PCISTP#	~f4_rxe4<1>		
	U6	**GPO7**		f4_rxe4<4>	SLP#	SLP#
			SLP#	~f4_rxe4<4>		
	W11	**GPO8**		f4_rxe5<3>	HGNT1#	RSTDRV# (reserved)
			HGNT1#	~f4_rxe5<3>		
	T10	**GPO9**		f4_rxe5<3>	HGNT2#	RS232_OFF#
			HGNT2#	~f4_rxe5<3>		
	Y10	**GPO10**		f4_rxe5<2>	LGNT1#	CARD_SUS#
			LGNT1#	~f4_rxe5<2>		
	V10	**GPO11**		f4_rxe5<2>	LGNT2#	IR_MD0 (for distance)
			LGNT2#	~f4_rxe5<2>		
	H5	**GPO12**		f4_rxe5<4> & ~f0_rx53<7>	JAB2	GP012
			JAB2	f4_rxe5<4>		
	H4	**GPO13**		f4_rxe5<4> & ~f0_rx53<7>	JBB2	GPO13
			JBB2	audio ena & game ena		
	R8	**GPO14**		f4_rxe5<5>	IRTX	IRTX

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			IRTX	~f4_rxe5<5>		
	U8	**GPO15**		f4_rxe5<5>	IRRX	IRRX
			IRRX	~f4_rxe5<5>		
	Y6	**GPO16**		f4_rxe4<2>	PCS0#	PCS0#
			PCS0#	~f4_rxe4<2>		
	W6	**GPO17**		f4_rxe4<3>	MCCS#	MCCS#
			MCCS#	~f4_rxe4<3>		
	K3	**GPO18**	GPI18/FAN2/SLPBT	see above	FAN2	GP018
	G5	**GPO19**	GPI19/ACSDIN2/PCS1#	see above	SDIN2	GPI19
	W13	**GPO20**	GPI20/LA20/USBOC	see above	GPI	GPI20
	Y13	**GPO21**	GPI21/LA21/USBOC	see above	GPI	SPK_OFF
	U7	**GPO22**	GPI22/IOR#	see above	GPI	IOR#
	T7	**GPO23**	GPI23/IOW#	see above	GPI	IOW#
	Y2	**GPO24**	GPI24/GPIOA	see above	GPI	AGP_BUSY#
	J5	**GPO25**	GPI25/GPIOC/ATEST	see above	GPI	RSET_TV
	R2	**GPO26**	GPI26/SMBDT2	see above	SMBDT2	CARD_ACT#
	R1	**GPO27**	GPI27/SMBCK2	see above	SMBCK2	GPO27
	W4	**GPO28**		~f0_rx58<7> & ~f0_rx58<6>	PICD0	GPO28
			APICD0	~f0_rx58<7> & f0_rx58<6>		
			APICCS#	f0_rx58<7> & ~f0_rx58<6>		
	Y4	**GPO29**		~f0_rx58<7> & ~f0_rx58<6>	PICD1	GPO29
			APICD1	~f0_rx58<7> & f0_rx58<6>		
			APICACK#	f0_rx58<7> & ~f0_rx58<6>		

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	Y1	**GPO30**	GPI30/GPIOD/DTEST	see above	GPI	GPO30
	W3	**GPO31**	GPI31/GPIOE	see above	GPI	GPO31
GPIO						
	Y2	**GPIOA**		see above		
	T8	**GPIOB**	IRRX2	FIR I/O Rx33 & 34		IRMODE (for IR type)
	J5	**GPIOC**		see above		
	Y1	**GPIOD**		see above		
	W3	**GPIOE**		see above		

1.5 Software Overview

1.5.1 BIOS features

Including System BIOS , VGA BIOS , POST , PM , PnP , ACPI

Support Shadow RAM BIOS feature

Support Boot Block feature

Support ACPI 1.0b

Support DMI 2.3

Support Quite Boot

Support AMD PowerNow! Technology

Support ACPI Power Management S0, S1, S3, S4 , S5

Operating Systems Support

OS	ACPI	Support	WHQL
Microsoft Windows98 SE	YES	YES	YES
Microsoft Windows ME	YES	YES	YES
Microsoft Windows 2000	YES	YES	YES

1.5.2 USB Legacy Support

USB Legacy Support

Device	DOS Mode	Resume from S1	Resume from S3	Resume from S4
USB Fl	NO	NO	NO	NO

1.6 BIOS Function Description

1.6.1 CMOS Setup

1.6.1.1 Main Menu

The Main pull-down menu contains the basic configuration setting of the system like “ Date and Time “ ,“Boot Sequence”,”Internal Numlock” refer to the BIOS SCU for the detail setting

1.6.1.2 Advance Menu

The Advance pull-down menu contains the I/O configuration setting of the system like “COM Ports“, ”LPT Port “, “Shared Video Memory “ . Please refer to the BIOS SCU for the detail setting

1.6.1.3 Security Menu

The Security pull-down menu contains the security setting which safeguard your system against unauthorized use like “ Set Password “ , “Hard Disk Boot Sector“ . Please refer to the BIOS SCU for the detail setting .

1.6.1.4 Exit Menu

The Exit pull-down menu displays ways of exiting SCU , after finished with your settings , you must save and exit SCU so that the settings can take effect . Please refer to the BIOS SCU for the detail Setting .

1.6.2 Power Management

1.6.2.1 Component Level Power Management Status :

Global power state	G0 Working	G1	Sleep	G2 Soft off
Sleep state	S0	S3	S4	S5
CPU	C0	POWER OFF	POWER OFF	POWER OFF
VIA TwisterK VGA	D0	D3	POWER OFF	POWER OFF
VIA VT8231 Audio	D0	D3	POWER OFF	POWER OFF
VIA VT8231 Modem	D0	D3	POWER OFF	POWER OFF
VIA VT8231 LAN	D0	D3	POWER OFF	POWER OFF
VIA VT8231 USB	D0	D3	POWER OFF	POWER OFF
Hard Drive	D0	D3	POWER OFF	POWER OFF
CD-ROM	D0	D3	POWER OFF	POWER OFF
TI1420 Card Bus	D0	D3	POWER OFF	POWER OFF
Audio AMP	POWER ON	POWER DOWN	POWER OFF	POWER OFF
ICS9248-189 Clock Gen	POWER ON	POWER ON	POWER OFF	POWER OFF
H8 KBC	POWER ON	POWER DOWN	POWER OFF	POWER OFF

1.6.2.2 The Behavior about Component Level Power Management

Component Activity	The capability of Wake upsystem from S3 state	Component activity is monitored,preventing timeout to enter sleep state
VIA TwisterK VGA	Can not wake system	Monitored by driver
VIA VT8231 Audio	Can not wake system	Monitored by driver
Modem Device	Wakeup by incoming call ifapplication is enabled	Monitored by driver
LAN Device	Can not wake system	Monitored by driver
Flop	Can not wake system	Monitored by OS
Hard Drive	Can not wake system	Monitored by OS
CD/DVD playback	Can not wake system	Monitored by driver
USB Device	Can not wake system	Monitored by driver
Touch Pad	Can not wake system	Monitored by OS
H8 KBC	Can wake system	Monitored by KBC/EC

1.6.3 OEM special functions

1.6.3.1 Cover Switch

At ACPI mode there are there functions to be chosen at windows power management of control panel.

1. None
2. Standby
3. Hibernation
4. Power Off

1.6.3.2 Power Button

At ACPI mode. Power button behavior was set by windows power management of control panel.

1. Standby
2. Hibernation
3. Power Off

Continue pushing power button over 4 seconds will force system off at ACPI mode.

1.6.4 Security functions

1.6.4.1 Power-On Password

The Power-On password item allows you to set the password for your system . The password is required for starting up the system

1.6.4.2 BootSctor Protect

The Bootsector protect prevent computer viruses by protecting the hard disk boot sector from any change .

1.6.5 Identification

1.6.5.1 SSID / SSVID

SSID : 7321 h

SSVID : 1071h

1.6.5.2 System LOGO Master ID

Master

ID :XXXXXX

1.7 Driver / Utility Description

1.7.1 Device Driver Support

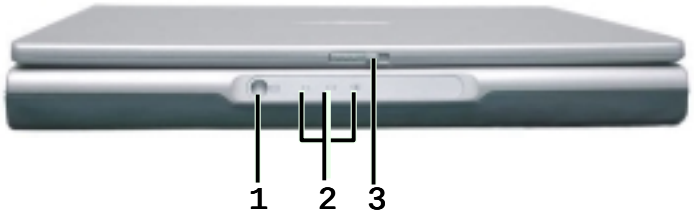
	Win98SE	Win2000	WinMe	Certification
VGA	YES	YES	YES	YES
Audio	YES	YES	YES	YES
PCMCIA	YES	YES	YES	YES
Modem	YES	YES	YES	YES
LAN	YES	YES	YES	YES
Touchpad	YES	YES	YES	YES

2 System View and Disassembly

2.1 System View

2.1.1 Front View

❶ Mail-Received Button/Indicator
❷ Power Indicators
❸ Top Cover Latch

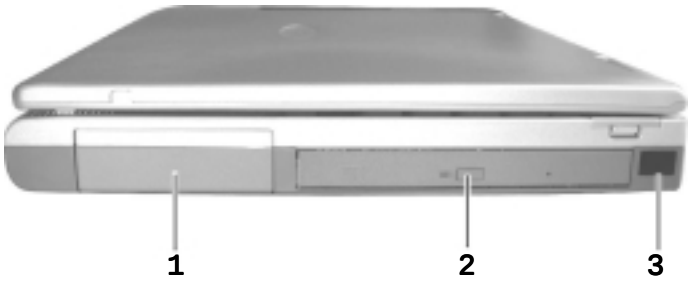


2.1.2 Left-Side View

❶ Audio Input Connector
❷ Microphone Connector
❸ Audio Output Connector
❹ Volume Control
❺ PC Card Slots
❻ Floppy Disk Drive

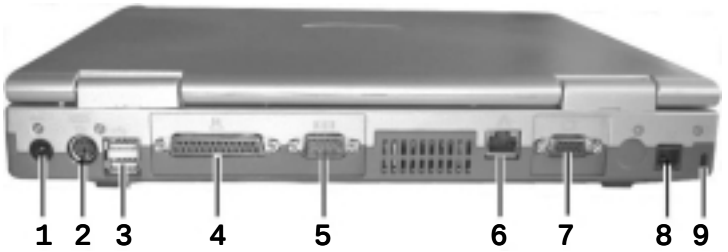
2.1.3 Right-Side View

❶ Battery Pack
❷ CD-ROM/DVD-ROM Drive
❸ IR Port



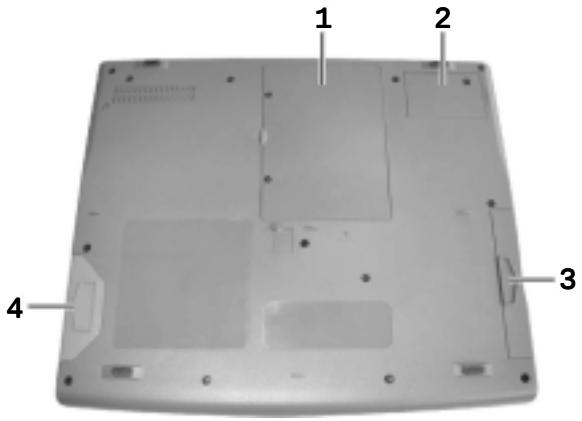
2.1.4 Rear View

❶ Power Connector
❷ PS/2 Port
❸ USB Ports
❹ Parallel Port
❺ Serial Port
❻ RJ-45 Connector
❼ VGA Port
❽ RJ-11 Connector
❾ Kensington Lock



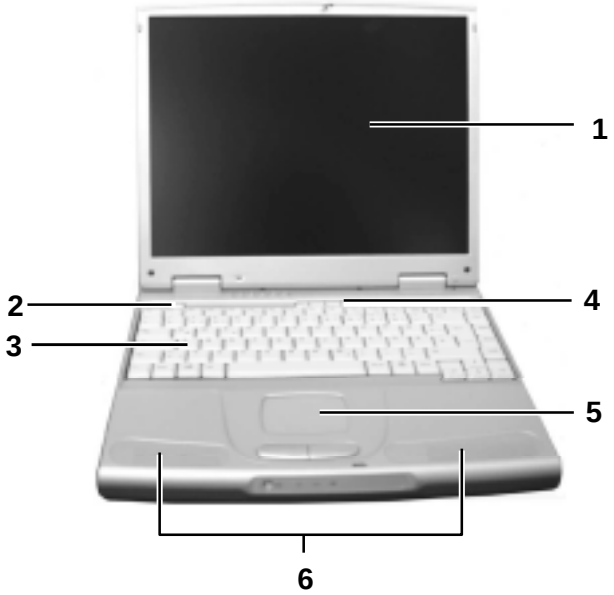
2.1.5 Bottom View

❶ CPU Cover
❷ Modem Card Cover
❸ FDD/HDD Module
❹ Battery Pack



2.1.6 Top-Open View

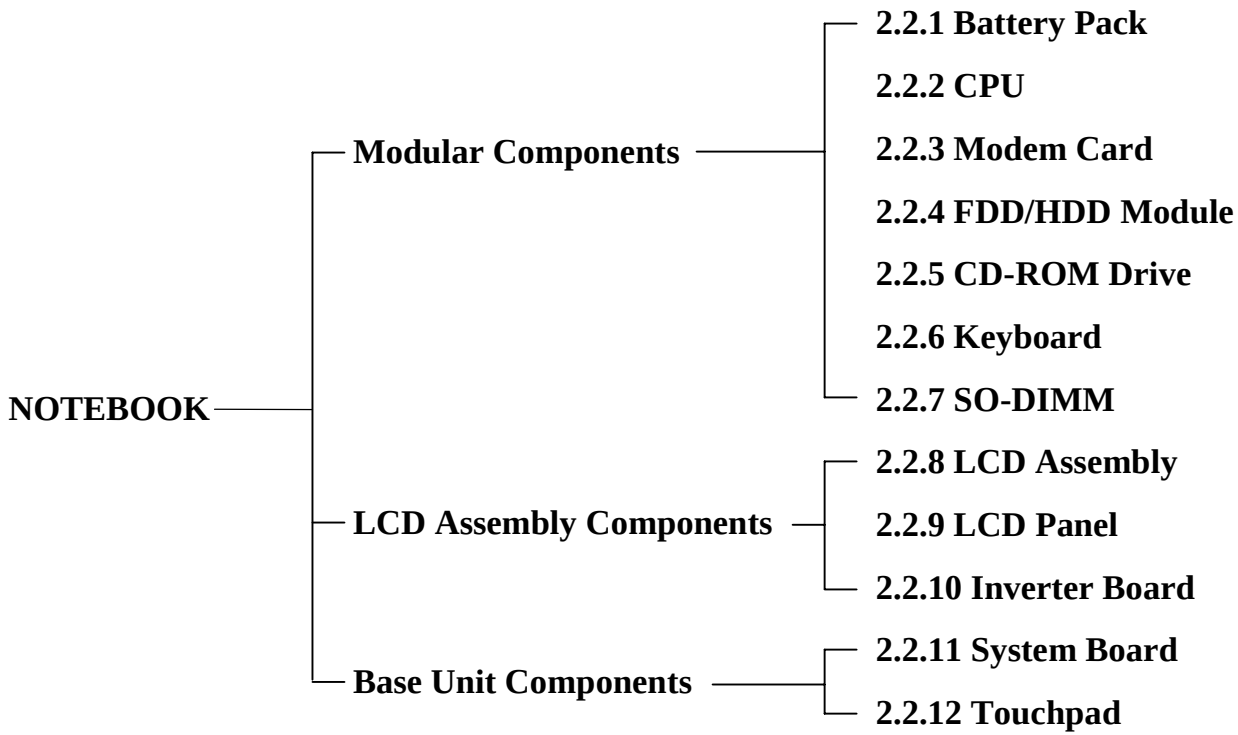
❶ LCD Screen
❷ Power Button
❸ Keyboard
❹ Easy Start Buttons
❺ Touchpad
❻ Stereo Speaker Set



2.2 System Disassembly

The section discusses at length each major component for disassembly/reassembly and show corresponding illustrations. Use the chart below to determine the disassembly sequence for removing components from the notebook.

NOTE: *Before you start to install/replace these modules, disconnect all peripheral devices and make sure the notebook is not turned on or connected to AC power.*



2.2.1 Battery Pack

Disassembly

1. Carefully put the notebook upside down.
2. Turn the locking button to the "unlock" (🔓) position (❶), then slide and hold the latch in the unlock position and pull the battery pack out of the compartment (❷).(figure 2-3)

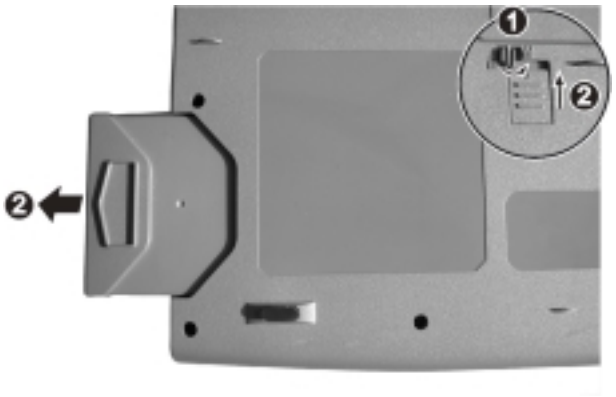


Figure 2-3

Reassembly

1. Push the battery pack into the compartment. The battery pack should be correctly connected when you hear a clicking sound.
2. Turn the locking button to the "lock" (🔒) position.

2.2.2 CPU

Disassembly

1. Carefully put the notebook upside down.
2. Remove two screws locking the CPU compartment cover, and then lift the cover up. (figure 2-4)

Figure 2-4

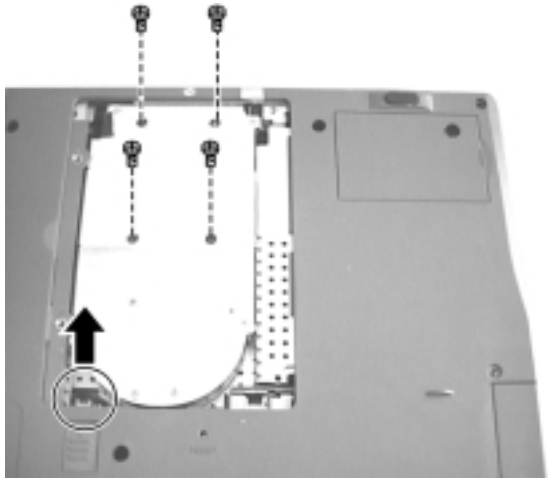


Figure 2-5

3. Remove four screws fastening the heatsink and disconnect the fan’s power cord to free the heatsink from the CPU module. (figure 2-5)

4. Insert a minus screwdriver 101 (JIS standard) into the “OPEN” hole of the socket, and push the screwdriver toward the CPU to free the CPU. Now you can take out the CPU from the socket. (figure 2-6)

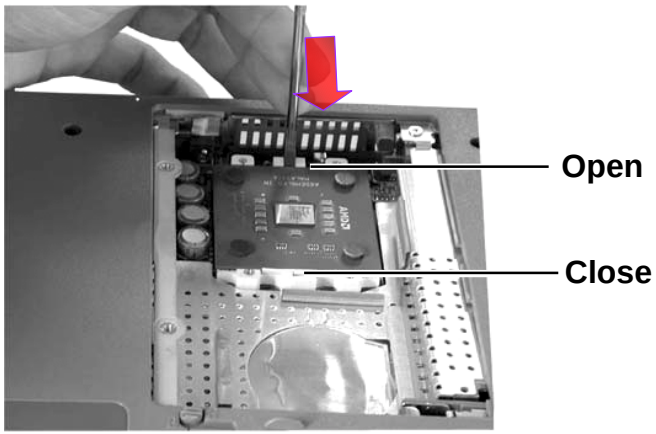


Figure 2-6

Reassembly

1. Align the arrowhead corner of the CPU with the beveled corner of the socket, and insert the CPU pins into the holes. Insert the flat screwdriver into the “CLOSE” hole of the socket, and push the screwdriver toward the CPU to secure the CPU in place.
2. Connect the fan’s power cord to the system board, fit the heatsink onto the top of the CPU and secure with four screws.
3. Replace the CPU compartment cover and secure with two screws.

2.2.3 Modem Card

Disassembly

1. Carefully put the notebook upside down.
2. Remove one screw locking the modem card compartment cover, and then lift the cover up. (figure 2-7)

Figure 2-7

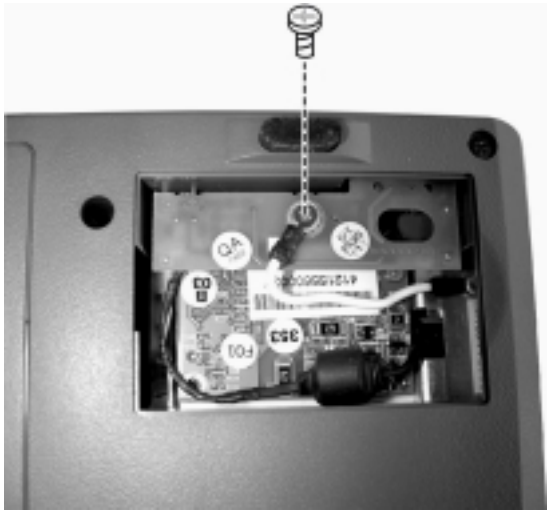


Figure 2-8

3. Remove one screw fastening the connector board and the grounding cable. (figure 2-8)

4. Slightly lift up the connector board, and then remove two screw fastening the modem card. Now you can take out the modem card from the compartment. (figure 2-9)
5. And then disconnect the cable from connector board . (figure 2-10)

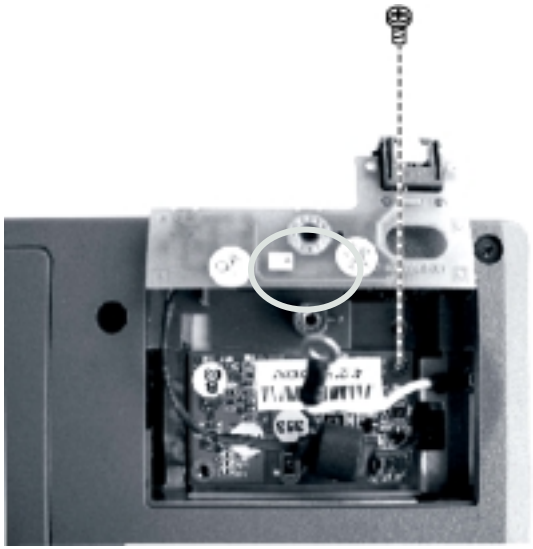


Figure 2-9

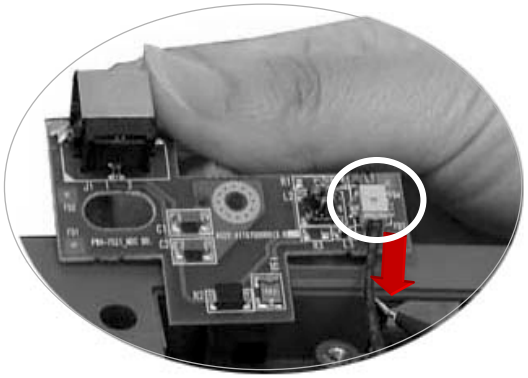


Figure 2-10

Reassembly

1. Reconnect the modem card into the system board and secure with two screws.
2. Hold the connector board an angle so that the phone line connector is pointed towards the opening on the notebook. Insert the connector into the opening and secure with a screw which fastening both the connector board and the grounding cable.
3. Replace the compartment cover and secure with one screw.

2.2.4 FDD/HDD Module

Disassembly

1. Carefully put the notebook upside down.
2. Remove one screw and slide the FDD/HDD module out of the compartment. (figure 2-11)

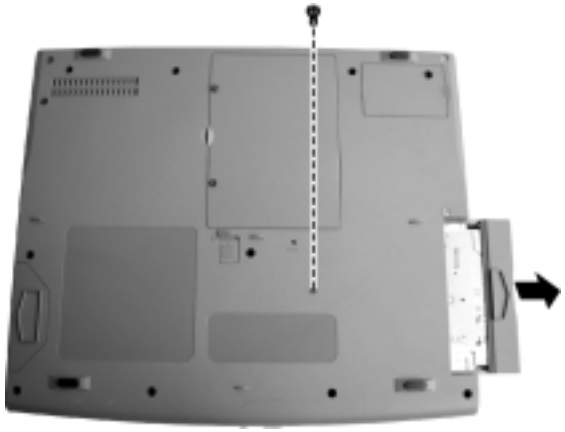


Figure 2-11

3. To take the hard disk drive apart, remove two screws of the hard disk. Then lift the hard disk up and unplug the connector to remove it. (figure 2-12)

Figure 5-12

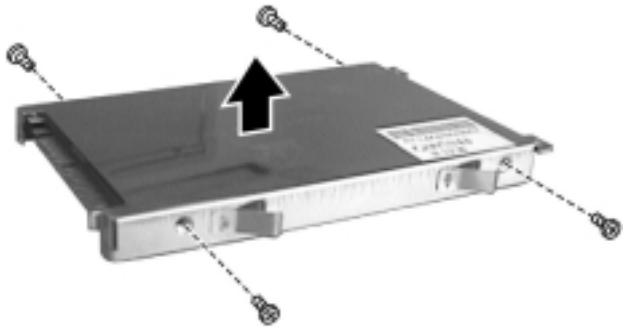


Figure 5-13

4. Remove four screws to separate the hard disk drive from the metal shield. (figure 2-13)

5. Remove five screws to separate the FDD module from plastic shield .(figure 2-14)
6. And then , disconnect the cable after peel off the adhesive tape.On this way,you can separate F DD module . (Figure 2-15)

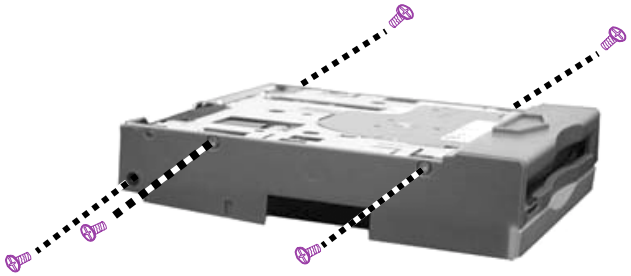


Figure 2-14

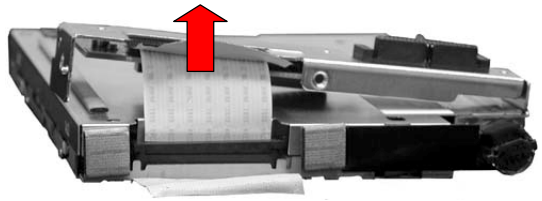


Figure 2-15

Reassembly

1. Reconnect the cable and conglutinate the adhesive tape.
2. Place FDD disk in the plastic shield and secure with two screws .
3. To install the hard disk drive, place it in the bracket and secure with four screws.
4. Connect the hard disk to the connector on the FDD/HDD module and secure with two screws.
5. Slide the FDD/HDD module into the compartment and secure with one screw.

2.2.5 CD-ROM Drive

Disassembly

1. Carefully put the notebook upside down.
2. Remove the battery pack. (See section 2.2.1 Disassembly.)
3. Remove the modem card. (See section 2.2.3 Disassembly.)
4. Remove the FDD/HDD module. (See step 2 in section 2.2.4 Disassembly.)
5. Remove one screw locking the CD-ROM (❶), and then the other twelve screws locking the base unit frame. (figure 2-16) Now you can lift the base unit frame up.

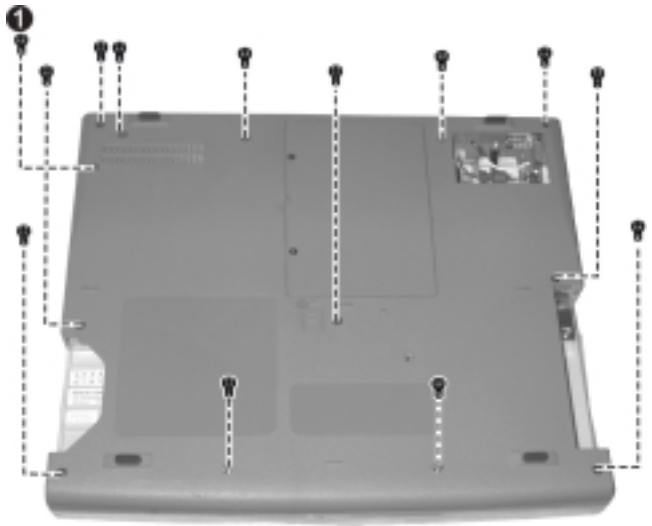


Figure 2-16

6. Hold the CD-ROM drive and slide it outward carefully. (figure 2-17).

Figure 2-17

Reassembly

1. Push the CD-ROM drive into the compartment.
2. Replace the base unit frame and secure with thirteen screws (includes one locking the CD-ROM drive).
3. Replace the FDD/HDD module. (See section 2.2.4 Reassembly.)
4. Replace the modem card. (See section 2.2.3 Reassembly.)
5. Replace the battery pack. (See section 2.2.1 Reassembly.)

2.2.6 Keyboard

Disassembly

1. Open the top cover.
2. Press the locking latch downward to unlatch the Easy Start panel (❶) , push it leftward and lift it up from the left side (❷). (figure 2-18)

Figure 2-18

Figure 2-19

3. Slightly lift up the keyboard and disconnect the cable from the system board to detach the keyboard. (figure 2-19)

Reassembly

1. Reconnect the keyboard cable and fit the keyboard back into place.
2. Replace the Easy Start panel.

2.2.7 SO-DIMM

Disassembly

1. Remove the keyboard to access the SO-DIMM sockets. (See section 2.2.6 Disassembly.)
2. Pull the retaining clips outwards (❶) and remove the SO-DIMM (❷). (figure 2-20)

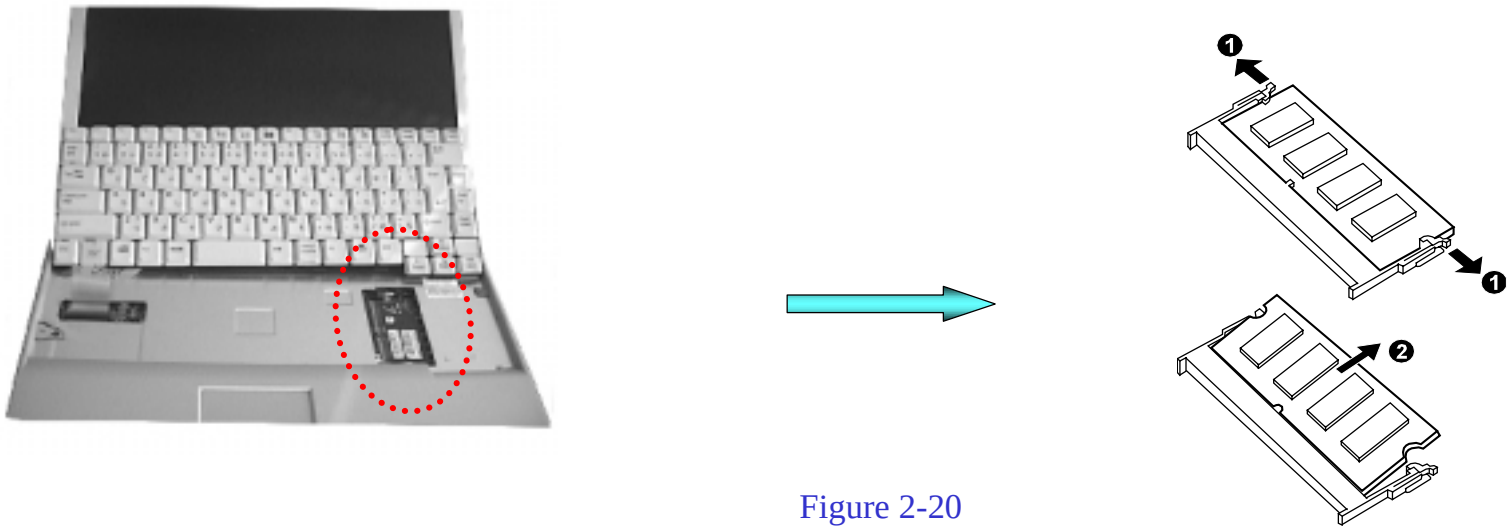


Figure 2-20

Reassembly

1. To install the SO-DIMM, match the SO-DIMM's notched part with the socket's projected part and firmly insert the SO-DIMM into the socket at 20-degree angle. Then push down until the retaining clips lock the SO-DIMM into position.
2. Replace the keyboard and the Easy Start panel. (See section 2.2.6 Reassembly.)

2.2.8 LCD Assembly

Disassembly

1. Open the top cover and remove the Easy Start panel. (See steps 1 to 2 in section 2.2.6 Disassembly.)
2. Remove the two hinge covers by inserting a flat screwdriver to the rear of the cover and pry the cover out. (figure 2-21)

Figure 2-21

Figure 2-22

3. Open the top cover. Unplug the three cable connectors coming from the LCD assembly, and remove four screws of the hinges. Now you can separate the LCD assembly from the base unit. (figure 2-22)

Reassembly

1. Attach the LCD assembly to the base unit and secure with four screws on the hinges.
2. Reconnect the LCD cable connectors to the system board.
3. Replace the two hinge covers.
4. Replace the Easy Start panel.

2.2.9 LCD Panel

Disassembly

1. Remove the LCD assembly. (See section 2.2.8 Disassembly.)
2. Remove the two rubber pads and two screws on the lower part of the panel. (figure 2-23)

Figure 2-23

Figure 2-24

3. Insert a flat screwdriver to the lower part of the frame and gently pry the frame out.Repeat the process until the frame is completely separated from the housing.
4. Remove the four screws on the two sides of the LCD panel, and unplug the cable fro the inverter board. (figure 2-24)

Reassembly

1. Fit the LCD panel back into place and secure with four screws, and reconnect the cable to the inverter board.
2. Fit the LCD frame back into the housing and replace the two screws and two rubber pads.
3. Replace the LCD assembly. (See section 2.2.8 Reassembly.)

2.2.10 Inverter Board

Disassembly

1. Remove the LCD assembly and detach the LCD frame (see instructions in previous two sections).
2. To remove the inverter board at the bottom side of the LCD assembly, unplug the cable and remove the two screws. (figure 2-25)

Figure 2-25

Reassembly

1. Fit the inverter board back into place and secure with two screws.
2. Reconnect the cables.
3. Replace the LCD frame. (See section 2.2.9 Reassembly.)
4. Replace the LCD assembly. (See section 2.2.8 Reassembly.)

2.2.11 System Board Disassembly

1. Remove the Keyboard. (See section 2.2.6 Disassembly.)
2. Remove the LCD assembly. (See section 2.2.8 Disassembly.)
3. Remove seven screws, and then take out the Easy Start board. (figure 2-26)

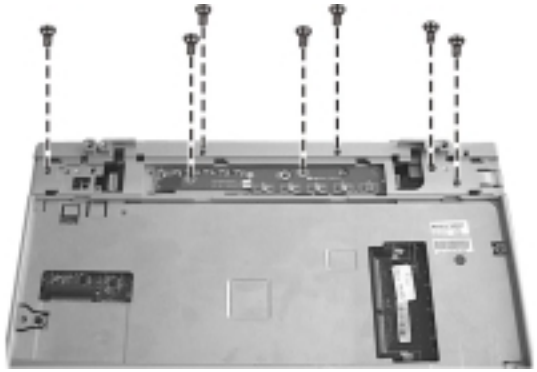


Figure 2-26

Figure 2-27

4. Remove four screws on the rear side of the notebook. (figure 2-27)
5. Remove the battery pack, heatsink, modem card, FDD/HDD module, and CD-ROM drive. (See section 2.2.1 to 2.2.5 Disassembly.)

6. Lift up the speaker assembly and disconnect the cable. (figure 2-28)

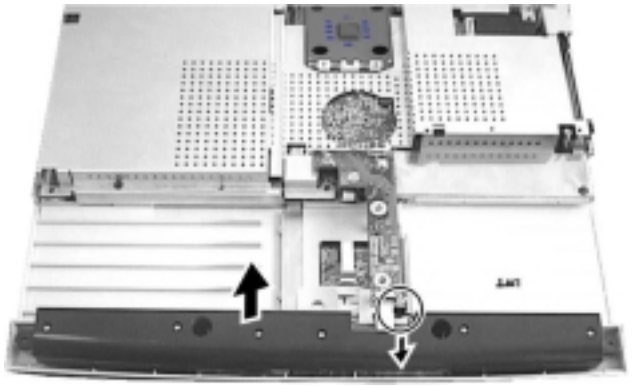


Figure 2-28

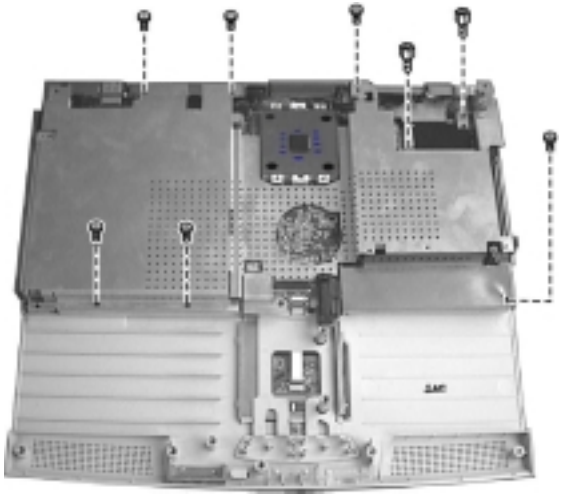


Figure 2-29

7. Remove six screws and two hexnut screws fastening the metal shield, and then lift the shield up from the system board carefully. (figure 2-29)

8. Remove four screws to take the recharge board apart. (figure 2-30)

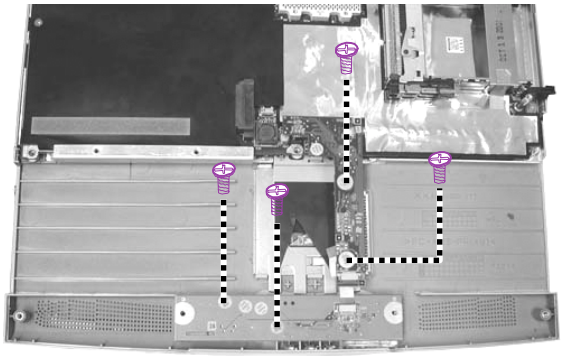


Figure 2-30

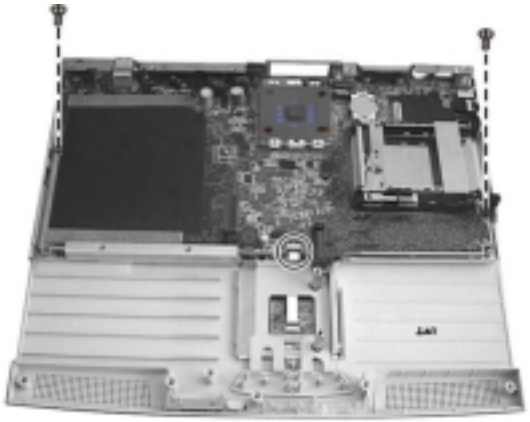


Figure 2-31

9. Remove two screws fastening the system board and disconnect the cable of the touchpad. Now you can lift the system board up from the base unit. (figure 2-31)

Reassembly

1. Fit the system board into place and secure with two screws.
2. Reconnect the touchpad’s cable.
3. Replace the metal shield and secure with six screws and two hexnut screws.
4. Replace the recharge board and secure with four screws.
5. Replace the speaker assembly and reconnect the cable.

6. Replace the base unit frame and secure with twelve screws.
7. Replace the battery pack, heatsink, modem card, FDD/HDD module, and CD-ROM drive.
8. Secure the four screws on the rear side of the notebook.
9. Put the notebook back to the upright position. Replace the Easy Start board into the housing, then secure with seven screws.
10. Replace the LCD assembly.
11. Replace the keyboard and Easy Start panel.

2.2.12 Touchpad

Disassembly

1. Remove the system board. (See section 2.2.11 Disassembly.)
2. Remove the four screws to lift up the touchpad holder and touchpad panel. (figure 2-33)

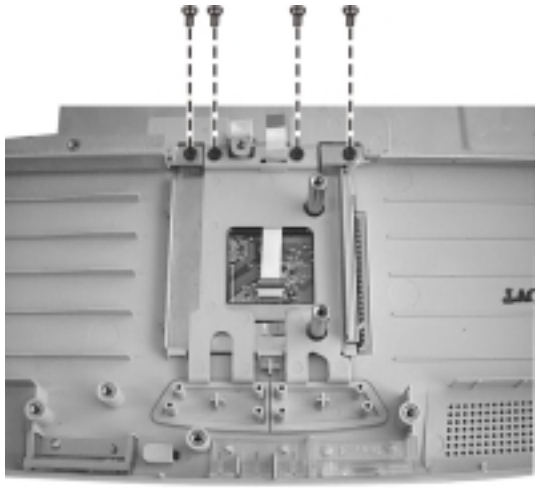


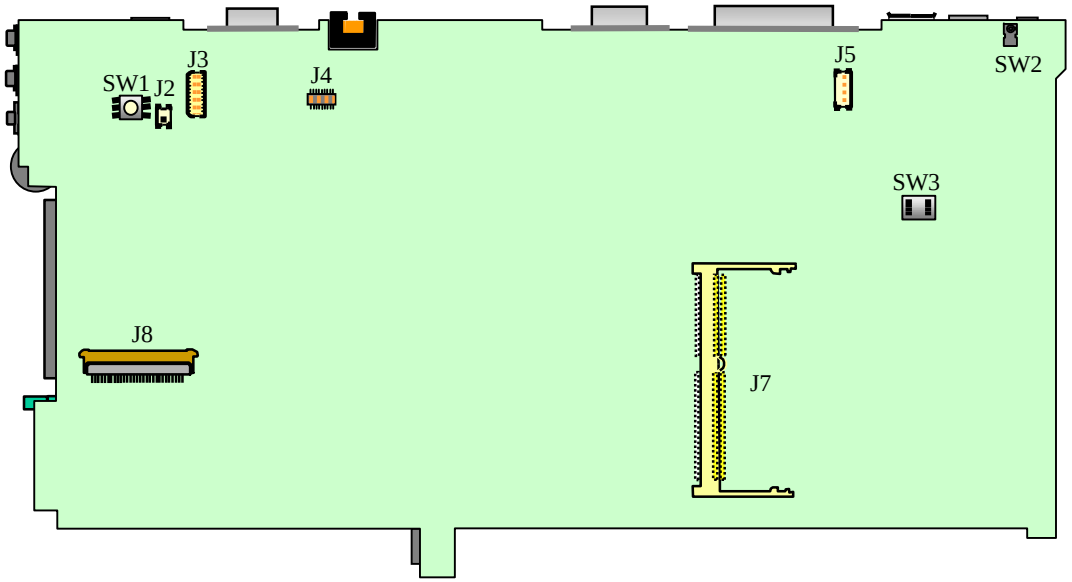
Figure 2-32

Reassembly

1. Replace the touchpad holder and touchpad panel, and secure with four screws.
2. Replace the system board and assemble the notebook. (See section 2.2.11 Reassembly.)

3. Definition & Location Of Connectors/switches

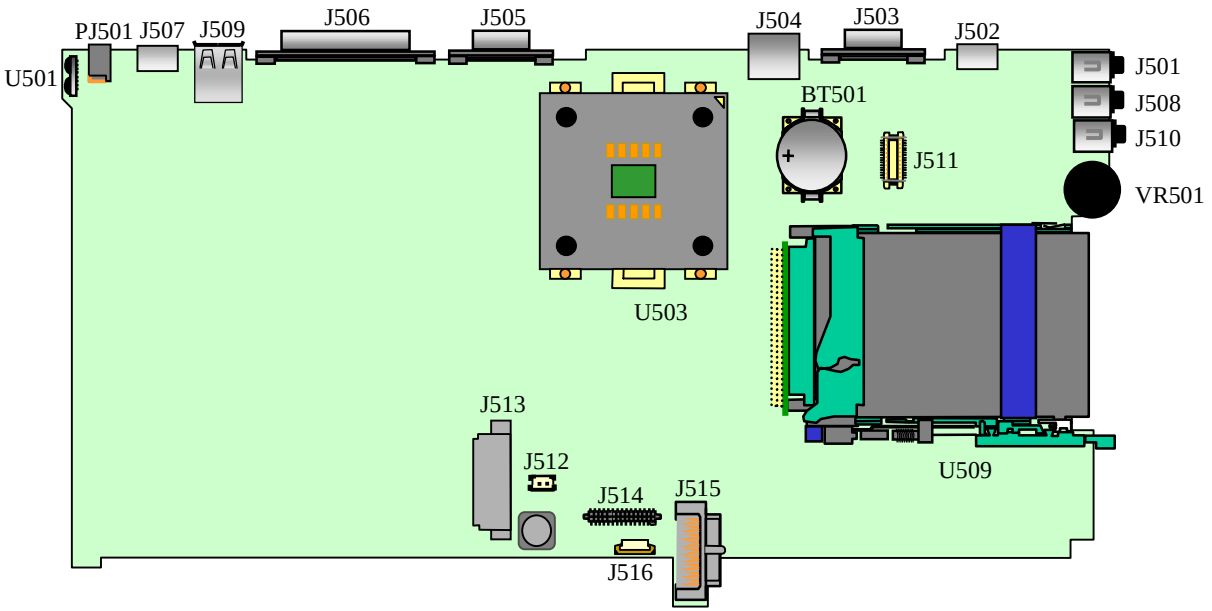
3.1 Mother Board-a



- J2: External MIC-in connector
- J3: LCD panel connector.
- J4: Quick key transfer BD connector.
- J5: Inverter BD connector
- J7: 144 pins expansion SDRAM socket.
- J8: Internal keyboard connector.
- SW1: Power button.
- SW2: Cover Suspend SW.
- SW3: Frequency Jump setting

3. Definition & Location Of Connectors/switches

3.2 Mother Board-b

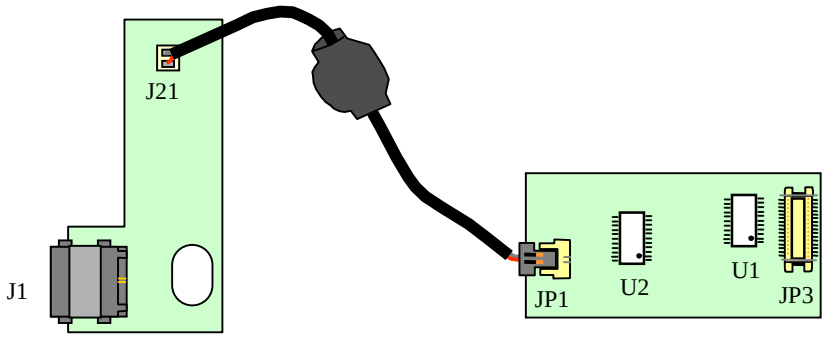


- PJ501: Power jack (AC adapter).
- J501: Line In
- J502: TV Out Port
- J503: SIO Port.
- J504: LAN connector
- J505: VGA Connector.
- J506: Parallel Port
- J507: PS/2 Mouse/keyboard
- J508: MIC In
- J509: USB connector.
- J510: Line Out
- J511: MODEM transfer board connector
- J512: FAN Connector.
- J513: CD-ROM drive connector.
- J514: Charger & Touch-Pad connector
- J515: HDD/FDD Connector.
- J516: Touch-Pad button connector
- BT501: CMOS Battery connector.
- VR501:Volume control VR.
- U503: CPU & CPU Socket.
- U509: PC Card socket

3. Definition & Location Of Connectors/switches

3.3 Daughter Board

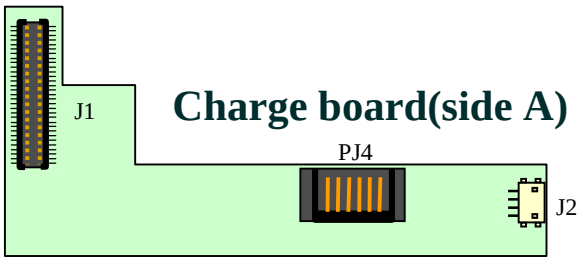
MDC/LAN transfer board

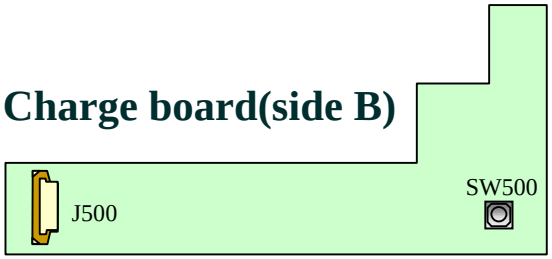


- J1: RJ-11 phone jack for internal modem.
- J21: MDC jump wire connector.
- JP1: MDC jump wire connector.
- JP3: Connector for MDC/LAN transfer board to M/B.

3. Definition & Location Of Connectors/switches

3.4 Charge Board

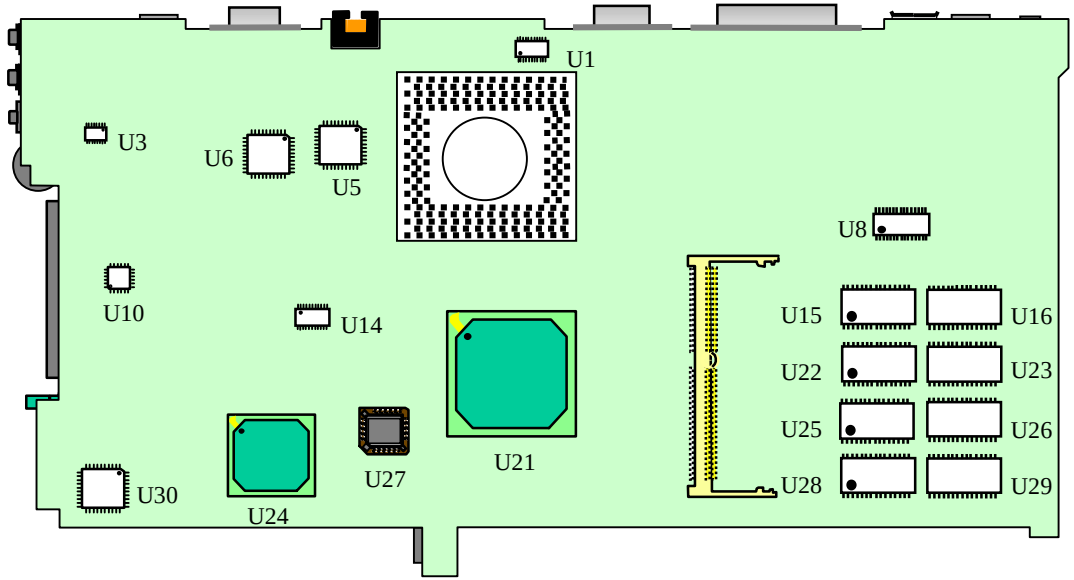




- J1: Charger & Touch-Pad connector to M/B.
- J2: Internal speaker connector.
- PJ4: Battery pack connector.
- J500: Touch-Pad button connector.
- SW500: CMOS Reset

4. Definition & Location Of Major Components

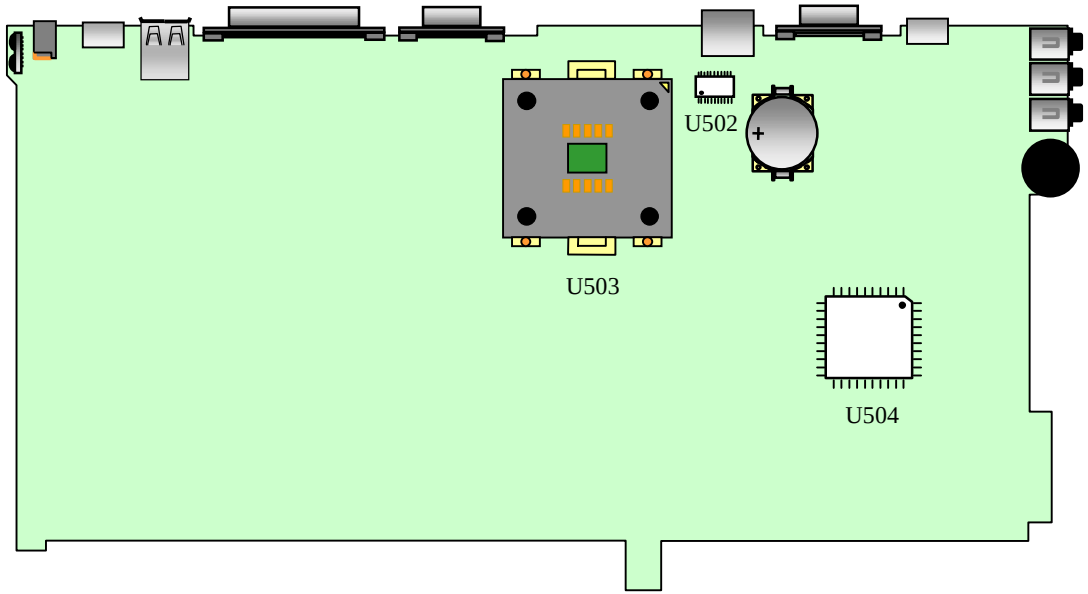
4.1 Main Board (Side a)



- U1: ADM3311ARU RS232/SIO.
- U3: TPA0202 AUDIO AMP
- U5: LANPHY LSIL80227
- U6: CH7005C(TV Encode).
- U8: ICS9248-102(Clock generator
- U10: CS4299 AC’97 CODE
- U14: Power switch matrix(PC CARD)
- U21: North Bridge VT8362
- U24: South Bridge VT8231
- U27: System BIOS.
- U30: H8(3434F,KB BIOS)
- U15,U22,U25,U28 U16,U23,U26,U29: On board SDAM.

4. Definition & Location Of Major Components

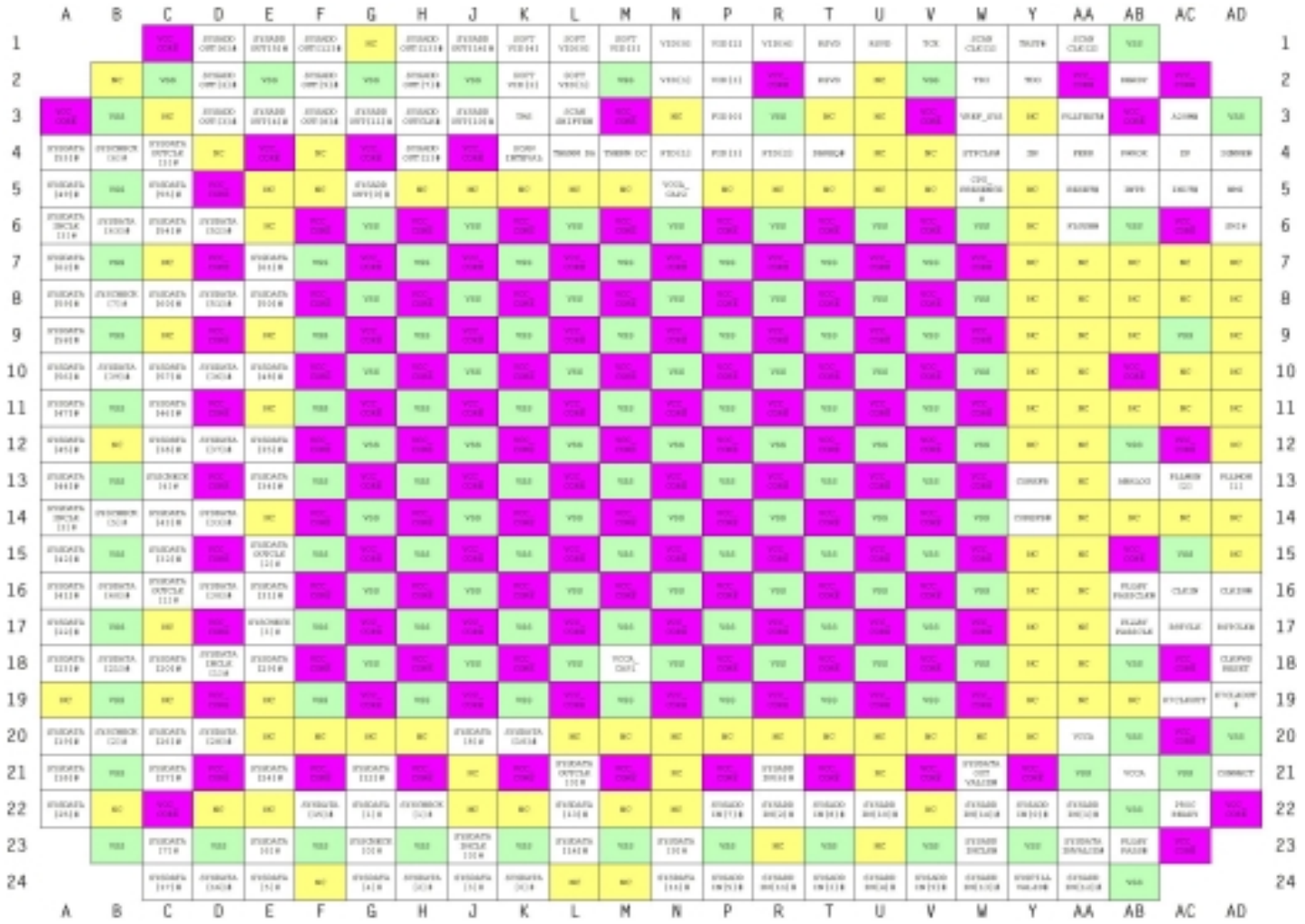
4.2 Main Board (Side b)



- U502: PH163112 LAN Controller.
- U503: Socket A CPU.
- U504: PCI1225PDV PC CARD interface controller.

5. Pin Descriptions of Major Components

5.1 Mobile AMD K7 Processor



Mobile AMD Athlon™ H- series OBGA Processor Model 6 Ball Diagram-Bottomside View

5. Pin Descriptions of Major Components

5.1 Mobile AMD K7 Processor

Detailed Ball Descriptions

Name	Description
A20M# Ball	A20M# is an input from the system used to simulate address wrap-around in the 20-bit 8086.
AMD Athlon™ Processor System Bus Balls	See the *AMD Athlon™ and AMD Duron™ Processor System Bus Specification*, order# 21902 for information about the system bus balls —PROCRDY, PWROK, RESET#, SADDIN[14:2]#, SADDINCLK#, SADDOUT[14:2]#, SADDOUTCLK#, SCHECK[7:0]#, SDATA[63:0]#, SDATAINCLK[3:0]#, SDATAINVALID#, SDATAOUTCLK[3:0]#, SDATAOUTVALID#, SFILLVALID#.
Analog Ball	Treat this ball as a NC.
CLKFWDRST Ball	CLKFWDRST resets clock-forward circuitry for both the system and processor.
CLKIN and RSTCLK (SYSCLK) Balls	Connect CLKIN (AC16) with RSTCLK (AC17) and name it SYSCLK. Connect CLKIN# (AD16) with RSTCLK# (AD17) and name it SYSCLK#. Length match the clocks from the clock generator to the Northbridge and processor. See “SYSCLK and SYSCLK#”, for more information.
CONNECT Ball	CONNECT is an input from the system used for power management and clock-forward initialization at reset.
COREFB and COREFB# Balls	COREFB and COREFB# are outputs to the system that provide processor core voltage feedback to the system.
CPU_PRESENCE# Ball	CPU_PRESENCE# is connected to VSS on the processor package. If pulled-up on the motherboard, CPU_PRESENCE# may be used to detect the presence or absence of a processor.
DBRDY and DBREQ# Balls	DBRDY (AB2) and DBREQ# (T4) are routed to the debug connector. DBREQ# is tied to VCC_CORE with a pullup resistor.
FERR Ball	FERR is an output to the system that is asserted for any unmasked numerical exception independent of the NE bit in CR0. FERR is an open-drain active High signal that must be inverted and level shifted to an active Low signal. For more information about FERR and FERR#, see the “Required Circuits” chapter of the *AMD Athlon™ Processor Motherboard Design Guide*, order# 24363.
FID[3:0] Balls	The FID[3:0] balls drive a value of: FID[3:0] = 0 1 0 0 that corresponds to a 5x SYSCLK multiplier after PWROK is asserted to the processor. This information is used by the Northbridge to create the SIP stream that the Northbridge sends to the processor after RESET# is deasserted. For more information, see “SYSCLK Multipliers”.
FLUSH# Ball	FLUSH# must be tied to VCC_CORE with a pullup resistor. If a debug connector is implemented, FLUSH# is routed to the debug connector.
IGNNE# Ball	IGNNE# is an input from the system that tells the processor to ignore numeric errors.

Name	Description
INIT# Ball	INIT# is an input from the system that resets the integer registers without affecting the floating-point registers or the internal caches. Execution starts at 0FFFF FFF0h.
INTR Ball	INTR is an input from the system that causes the processor to start an interrupt acknowledge transaction that fetches the 8-bit interrupt vector and starts execution at that location.
JTAG Balls	TCK (V1), TMS (K3), TDI (W2), TRST# (Y1), and TDO (Y2) are the JTAG interface. Connect these balls directly to the motherboard debug connector. Pullup TDI, TCK, TMS, and TRST# to VCC_CORE with pullup resistors.
K7CLKOUT and K7CLKOUT# Balls	K7CLKOUT (AC19) and K7CLKOUT# (AD19) are each run for 2 to 3 inches and then terminated with a resistor pair, 100 ohms to VCC_CORE and 100 ohms to VSS. The effective termination resistance and voltage are 50 ohms and VCC_CORE/2.
NC Balls	The motherboard should provide a surface mount pad for all 564 package balls. The pads for NC balls should not be electrically connected to anything.
NMI Ball	NMI is an input from the system that causes a non-maskable interrupt.
PLL Bypass and Test Balls	PLLTEST# (AA3), PLLBYPASS# (AB23), PLLMON1 (AD13), PLLMON2 (AC13), PLLBYPASSCLK (AB17), and PLLBYPASSCLK# (AB16) are the PLL bypass and test interface. This interface is tied disabled on the motherboard. All six ball signals are routed to the debug connector. All four processor inputs (PLLTEST#, PLLBYPASS#, PLLMON1, and PLLMON2) are tied to VCC_CORE with pullup resistors.
PWROK Ball	The PWROK input to the processor must not be asserted until all voltage planes in the system are within specification and all system clocks are running within specification. For more infor mation, s ee “Signal and Power -Up Requirements”.
RSVD Balls	Reserved balls must have pulldown resistors to ground on the motherboards.
SADDIN[1:0]# and SADDOUT[1:0]# Balls	The mobile AMD Athlon H-series OBGA processor model 6 does not support SADDIN[1:0]# or SADDOUT[1:0]#. SADDIN[1]# is tied to VCC_CORE with pullup resistors, if this bit is not supported by the Northbridge (future models of the AMD Athlon processors may support SADDIN[1] #) . SADDOUT[1:0]# are tied to VCC_CORE with pullup resistors if these balls are supported by the Northbridge. For more information, see the *AMD Athlon™ and AMD Duron™ Processor System Bus Specification*, order# 21902.

5. Pin Descriptions of Major Components

5.1 Mobile AMD K7 Processor

Name	Description
Scan Balls	SCANSHIFTEN (L3), SCANCLK1 (W1), SCANINTEVAL (K4), and SCANCLK2 (AA1) are the scan interface. This interface is AMD internal and is tied disabled with pulldown resistors to ground on the motherboard.
SCHECK[7:0]# Ball	For systems that do not support ECC, SCHECK[7:0]# should be treated as NC balls.
SMI# Ball	SMI# is an input that causes the processor to enter the system management mode.
SOFTVID[4:0] and VID[4:0] Balls	The VID[4:0] (Voltage ID) and SOFTVID[4:0] (Software driven Voltage ID) outputs are used by the DC to DC power converter to select the processor core voltage. The VID[4:0] balls are strapped to ground or left unconnected on the package and must be pulled up on the motherboard. The SOFTVID[4:0] balls are open drain and 2.5–V tolerant. The SOFTVID[4:0] balls of the processor must not be pulled to voltages higher than 2.5 V. The motherboard is required to implement a VID multiplexer to select a deterministic voltage for the processor at power–up before the PWROK input is asserted. Before PWROK is asserted, the VID multiplexer drives the VID value from VID[4:0] balls to the DC to DC converter for VCC_CORE. After PWROK is asserted, the VID multiplexer drives the VID value from the SOFTVID[4:0] balls to the DC to DC converter for VCC_CORE of the processor. Refer to the *AMD Athlon™ Processor Motherboard Design Guide*, order# 24363 for the recommended VID multiplexer circuit. The SOFTVID[4:0] balls are driven by the processor to select the maximum VCC_CORE of the processor as reported by the Maximum VID field of the FidVidStatus MSR within 20 ns of PWROK assertion. Bef ore PWROK i s asser t ed, the SOFTVID[4:0] outputs are not driven to a deterministic value. The SOFTVID[4:0] outputs must be used to select VCC_CORE after PWROK is asserted. Any time the RESET# input is asserted, the SOFTVID[4:0] balls will be driven to select the maximum voltage. Note: the Start–up VID and Maximum VID fields of the FidVidStatus MSR report the same value that corresponds to the nominal voltage that the processor requires to operate at maximum frequency. AMD PowerNow!™ technology can use the FID_Change protocol described in Section 4.1 on page 9 to transition the SOFTVID[4:0] outputs and therefore VCC_CORE as part of processor performance state transitions. The VID codes used by the mobile AMD Athlon H-series OBGA processor model 6 are defined in Table 23, “SOFTVID[4:0] and VID[4:0] Code to Voltage Definition,” on page 81. ***Note:*** *VID codes for Mobile AMD Athlon processors are different from the VID codes for desktop AMD Athlon processors.*

Name	Description
SOFTVID[4:0] and VID[4:0] Code to Voltage Definition	

VID[4:0] (V)	VCC_CORE	VID[4:0]	VCC_CORE (V)
00000	2.000	10000	1.275
00001	1.950	10001	1.250
00010	1.900	10010	1.225
00011	1.850	10011	1.200
00100	1.800	10100	1.175
00101	1.750	10101	1.150
00110	1.700	10110	1.125
00111	1.650	10111	1.100
01000	1.600	11000	1.075
01001	1.550	11001	1.050
01010	1.500	11010	1.025
01011	1.450	11011	1.000
01100	1.400	11100	0.975
01101	1.350	11101	0.950
01110	1.300	11110	0.925
01111	Shutdown	11111	Shutdown

STPCLK# Ball	STPCLK# is an input that causes the processor to enter a lower power mode and issue a Stop Grant special cycle.
SYSCLK and SYSCLK#	SYSCLK and SYSCLK# are differential input clock signals provided to the PLL of the processor from a system-clock generator. See “CLKIN and RSTCLK (SYSCLK) Balls” , for more information.
THERMDA and THERMDC Balls	Thermal Diode anode (THERMDA) and cathode (THERMDC) balls are used to monitor the actual temperature of the processor die, providing more accurate temperature control to the system. See Table 17, “Thermal Diode Characteristics”, for more details.
VCCA	VCCA is the processor PLL supply. For information about the VCCA balls, see Table 7, “VCCA AC and DC Characteristics,” and the *AMD Athlon™ Processor Motherboard Design Guide*, order# 24363.
VCCA_CAP1 and VCCA_CAP2 Balls	The motherboard must connect VCCA_CAP1 and VCCA_CAP2 balls to VSS with a capacitor. Refer to *AMD Athlon™ Processor Motherboard Design Guide*, order# 24363 for population details.
VREF_SYS Ball	VREF_SYS (W3) drives the threshold voltage for the system bus input receivers. The value of VREF_SYS is system specific. In addition, to minimize VCC_CORE noise rejection from VREF_SYS, i ncl ude decoupl i ng capaci tors. For more information, see the *AMD Athlon™ Processor Motherboard Design Guide*, order# 24363.
ZN and ZP Balls	ZN (Y4) and ZP (AC4) are the push-pull compensation circuit balls. In Push-Pull mode (selected by the SIP parameter SysPushPull asserted), ZN is tied to VCC_CORE with a resistor that has a resistance matching the impedance Z 0 of the transmission line. ZP is tied to VSS with a resistor that has a resistance matching the impedance Z 0 of the transmission line.

5. Pin Descriptions of Major Components

5.2 VIA VT8362 North Bridge with S3 Savage4 AGPX4

DRAM Interface

Signal Name	PIN #	I/O	Signal Description
MD[63:0]	(see pinout tables)	IO	**Memory Data.** These signals are connected to the DRAM data bus. Output drive strength may be set by Device 0 Rx6D[4].
MA14/ strap, **MA13**/ strap, **MA12**/ strap, **MA11**/ strap, **MA10**/ strap, **MA9**/ strap, **MA8**/ strap, **MA7**/ strap, **MA6**/ strap, **MA5**/ strap, **MA4**/ strap, **MA3**/ strap, **MA2**/ strap, **MA1**/ strap, **MA0**/ strap	W22 W23 W24 W25 W26 V24 V25 U21 V22 U22 V23 T22 V26 U23 U24	O/ I	**Memory Address.** DRAM address lines Strap / Register / Description / Settings MA14 / Rx68[0] / CPU Clock Frequency / 0=100, 1=133 MA13-12 / RxB4[7-6] / Drive Strength for Rise / 11=Auto, ~11=Strap MA11 / RxB6[7] / S2K Edge/Central DQ / 0=Central, 1=Edge MA10-9 / RxB4[3-2] / Drive Strength for Fall / 0=Auto, ~0=Strap MA8-4 / RxB6[5-1] / S2K Strobe Delay / 0=Auto, ~0=Strap MA3-0 / RxB3[6-3] / CPU Clock Divide / 0=11, 1=11.5, 2=12, 3=12.5, 4=5, 5=5.5, 6=6, 7=6.5, 8=7, 9=7.5, 10=8, 11=8.5, 12=9, 13=9.5, 14=10, 15=10.5 SRASA# / RxB2[5] / S2K Slew Rate Control / 0=Enable, 1=Disable SCASA# / RxB3[1] / Fast Command / 0=Disable, 1=Enable SWEA# / RxB6[6] / CPU Edge/Center DQ / 0=Edge, 1=Center Strap option default values are all 0 (internally pulled down) MA output drive strength may be set by Device 0 Rx6C[7] and 6D[2]. Cmd output drive strength may be set by Device 0 Rx6C[6] and 6D[3].
CS[5:0]#	Y23, Y22, AA25, AA26, Y26, Y25	O	**Chip Select.** Chip select of each bank. Output drive strength may be set by Device 0 Rx6D[0].
DQM[7:0]	R24, T26, AA24, AB26, R26, R23, AA22, AA23	O	**Data Mask.** Data mask of each byte lane. Output drive strength may be set by Device 0 Rx6D[1].
SRASA#/ strap	U25	O	**Row Address Command Indicator.** (strap at Device 0 RxB2[5])
SCASA# / strap	P25	O	**Column Address Command Indicator.** (strap at Device 0 RxB3[1])
SWEA# / strap	AB24	O	**Write Enable Command Indicator.** (strap at Device 0 RxB6[6])
CKE0 / SWEC#, **CKE1** / SCASC#, **CKE2** / SWEB#, **CKE3** / SCASB#, **CKE4** / SRASC#, **CKE5** / SRASB#	U26 T25 P26 R25 AC26 AB25	O	**Clock Enables.** Clock enables for each DRAM bank for powering down the SDRAM or clock control for reducing power usage and for reducing heat / temperature in high-speed memory systems. See Device 0 Rx78[0] and RxE0[4].

PCI Bus Interface

Signal Name	PIN #	I/O	Signal Description
AD[31:0]	(see pinout tables)	IO	**Address/Data Bus.** The standard PCI address and data lines. The address is driven with FRAME# assertion and data is driven or received in following cycles.
CBE[3:0]#	AC10, AB12, AF14, AE15	IO	**Command/Byte Enable.** Commands are driven with FRAME# assertion. Byte enables corresponding to supplied or requested data are driven on following clocks.
FRAME#	AC12	IO	**Frame.** Assertion indicates the address phase of a PCI transfer. Negation indicates that one more data transfer is desired by the cycle initiator.
IRDY#	AF12	IO	**Initiator Ready.** Asserted when the initiator is ready for data transfer.
TRDY#	AE12	IO	**Target Ready.** Asserted when the target is ready for data transfer.
STOP#	AB13	IO	**Stop.** Asserted by the target to request the master to stop the current transaction.
DEVSEL#	AD12	IO	**Device Select.** This signal is driven by the VT8362 when a PCI initiator is attempting to access main memory. It is an input when the VT8362 is acting as a PCI initiator.
PAR	AE13	IO	**Parity.** A single parity bit is provided over AD[31:0] and C/BE[3:0].
SERR#	AF13	IO	**System Error.** The VT8362 will pulse this signal when it detects a system error condition.
LOCK#	AC13	IO	**Lock.** Used to establish, maintain, and release resource lock.
PREQ#	AE18	I	**South Bridge Request.** This signal comes from the South Bridge. PREQ# is the South Bridge request for the PCI bus.
PGNT#	AF18	O	**South Bridge Grant.** This signal driven by the VT8362 to grant PCI access to the South Bridge.
REQ[4:0]#	AB8, AC6, AC7, AE6, AE7	I	**PCI Master Request.** PCI master requests for PCI.
GNT[4:0]#	AB7, AD6, AD7, AF6, AF7	O	**PCI Master Grant.** Permission is given to the master to use PCI.
PCLK	AB18	I	**PCI Clock.** From external clock generator.
PCKRUN#	AC17	IO	**PCI Clock Run.** May be used to stop PCI clock.
INTA#	AB6	O	**PCI Interrupt Out.** An asynchronous active low output used to signal an event that requires handling on behalf of the internal integrated graphics controller. If MA2 is strapped high at reset (clearing CR36[0]) no interrupt will be requested during PCI configuration. The default drive strength is 24 mA (other drive strengths may be selected via CR80[1-0]).

5. Pin Descriptions of Major Components

5.2 VIA VT8362 North Bridge with S3 Savage4 AGPX4

PCI Bus Interface			
Signal Name	**PIN #**	**I/O**	**Signal Description**
WSC#	AC18	O	**Write Snoop Complete.** Sideband PCI signal (used on the planar only in multiprocessor configurations) asserted to indicate that all snoop activity on the CPU bus initiated by the last PCI-to-DRAM write is complete and that it is safe to send an APIC interrupt message. Basically this signal is always active except when PCI master write data is not flushed.

LCD Panel Interface			
Signal Name	**PIN #**	**I/O**	**Signal Description**
FPD[35:0]	(see pin table)	O	**Panel Data.** Internally pulled down during reset. 8mA is the default. 16mA is selected via SR3D[6]=1.
FPDET	AA7	I	**Panel Detect.** If SR30[1]=0, SR30[2] will read 1 if a Flat Panel is appropriately connected. Must be tied to GND if not used.
FPVS	G3	O	**Panel VSYNC.** Internally pulled down.
FPHS	G5	O	**Panel HSYNC.** Internally pulled down.
FPDE	H3	O	**Panel Data Enable.** Internally pulled down.
FPCLK	G4	O	**Panel Clock.** Internally pulled down during reset. 8mA is the default. 16mA may also be selected.
FPGPIO	G1	I/O	**General Purpose Input/Output.**
ENVDD	F1	O	**Enable VDD.** This signal is driven high to external logic to initiate a flat panel power up sequence.
ENVEE	H5	O	**Enable VEE.** This signal is driven high to a programmable time after ENVDD is driven high during a flat panel power up sequence.

CRT Interface			
Signal Name	**PIN #**	**I/O**	**Signal Description**
RSET	C1	A	**Reference Resistor.** Tie to GNDRGB through an external 140?esistor to control the RAMDAC full-scale current value.
AR	C2	A	**Analog Red.** Analog red output to the CRT monitor.
AB	B2	A	**Analog Blue.** Analog blue output to the CRT monitor.
AG	B1	A	**Analog Green.** Analog green output to the CRT monitor.
HSYNC	F5	O	**Horizontal Sync.** Output to CRT.
VSYNC	F4	O	**Vertical Sync.** Output to CRT.

Flat Panel Monitor (DVI) Interface			
Signal Name	**PIN #**	**I/O**	**Signal Description**
FPD[11:0]	(see pin table)	O	**Panel Data.** Internally pulled down during reset. 8mA is the default. 16mA is selected via SR3D[6]=1. This function is selected on these pins when SR31[4] = 1.
FPDET	AA7	I	**Panel Detect.** If SR30[1]=0, SR30[2] will read 1 if a Flat Panel is appropriately connected. Must be tied to GND if not used.
FPVS	G3	O	**Panel VSYNC.** Internally pulled down.
FPHS	G5	O	**Panel HSYNC.** Internally pulled down.
FPDE	H3	O	**Panel Data Enable.** Internally pulled down.
FPCLK	G4	O	**Panel Clock.** Internally pulled down during reset. 8mA is the default. 16mA may also be selected.

TV Encoder Interface			
Signal Name	**PIN #**	**I/O**	**Signal Description**
TVD[11:0]	(see pin table)	O	**TV Data.** Internally pulled down during reset
TVCLK / FPD32	N5	I	**TV Clock.** Input clock from encoder. Internally pulled down.
TVCLKR / FPD16	K5	O	**TV Return Clock.** Output clock to TV encoder. Internally pulled down.
TVVS / FPD31	R4	O	**TV VSYNC.** Internally pulled down during reset
TVHS / FPD34	R5	O	**TV HSYNC.** Internally pulled down during reset
TVBL# / FPD17	L1	O	**TV Blanking.** Internally pulled down during reset

LVDS Interface			
Signal Name	**PIN #**	**I/O**	**Signal Description**
Y[2:0]P **Y[2:0]M**	AC2, AD3, AD1 AC1, AD2, AD4	A A	**LVDS Data Positive Output.** **LVDS Data Negative Output.**
YCP **YCM**	AB4 AA5	A A	**LVDS Clock Positive Output.** **LVDS Clock Negative Output.**
Z[2:0]P **Z[2:0]M**	AA4, AB2, AB3 A3, AB1, AC3	A A	**2 nd LVDS Data Positive Output.** **2 nd LVDS Data Negative Output.**
ZCP **ZCM**	AA1 AA2	A A	**2 nd LVDS Clock Positive Output.** **2 nd LVDS Clock Negative Output.**

5. Pin Descriptions of Major Components

5.2 VIA VT8362 North Bridge with S3 Savage4 AGPX4

Miscellaneous Functions			
Signal Name	**PIN #**	**I/O**	**Signal Description**
XIN	E1	I	**Reference Frequency Input.** An external 14.318 MHz crystal is connected between XOUT and this pin. Alternatively, an external oscillator can be connected.
XOUT	E2	O	**Crystal Output.** This pin drives the crystal via an internal oscillator. If an external oscillator is connected to XIN, this pin can be left unconnected.
SPCLK[2:1]	M2, AE5	IO	**Serial Port Clocks.** These are the clocks for serial data transfer. SPCLK1 is typically used for I²C communications. As an output, it is programmed via CRA0[0]. As an input, its status is read via CRA0[2]. In either case the serial port must be enabled by CRA0[4] = 1. SPCLK2 is typically used for DDC monitor communications. As an output, it is programmed via CRB1[0]. As an input, its status is read via CRB1[2]. The port is enabled via CRB1[4] = 1.
SPDAT[2:1]	M3, AD5	IO	**Serial Port Data.** These are the data signals used for serial data transfer. SPDAT1 is typically used for I²C communications. As an output, it is programmed via CRA0[1]. As an input, its status is read via CRA0[3]. In either case the serial port must be enabled by CRA0[4] = 1. SPDAT2 is typically used for DDC monitor communications. As an output, it is programmed via CRB1[1]. As an input, its status is read via CRB1[3]. The port is enabled via CRB1[4] = 1.
STRW / GPOUT	AE2	O	**General Purpose Output.** This pin reflects the state of SRD[0].
GOP0	AF2	O	**General Output Port.** When SR1A[4] is cleared, this pin reflects the state of CR5C[0].
STPAGP#	AE3	I	**Stop AGP.** Power management for internal AGP.
AGPBUSY#	AD4	I/O	**AGP Busy.** Power management for internal AGP.
STANDBY	AE4	I	**Standby.** Used to put the integrated graphics controller in the standby state.
SUSPEND	AC5	I	**Suspend.** Used to put the integrated graphics controller in the suspend state.
SUSST#	AB19	I	**Suspend Status.** For implementation of the Suspend-to-DRAM feature. Connect to an external pullup to disable.

ZV-Port Interface			
Signal Name	**PIN #**	**I/O**	**Signal Description**
ZVD[15:0]	(see pin table)	I	**ZV-Port Data Bus Video Input.**
ZVHS	V3	I	**ZV-Port Horizontal Sync.**
ZVVS	V1	I	**ZV-Port Vertical Sync.**
ZVCLK	W3	I	**ZV-Port Clock.**

Clock / Reset Control			
Signal Name	**PIN #**	**I/O**	**Signal Description**
HCLK	G22	I	**Host Clock.** This pin receives the host CPU clock (66 / 100 / 133 MHz). This clock is used by all TwisterK logic that is in the host CPU domain.
PCLK	AB18	I	**PCI Clock.** This pin receives a buffered host clock divided-by-3 to create 33 MHz. This clock is used by all of the TwisterK logic that is in the PCI clock domain. This clock input must be 33 MHz maximum to comply with PCI specification requirements and must be synchronous with the host CPU clock, HCLK, with an HCLK:PCLK frequency ratio of 3:1. The host CPU clock must lead the PCI clock by 2.0 ± 1.0 nsec.
MCLK	R22	O	**DRAM Clock.** Output from internal clock generator to the external clock buffer.
MCLKF	P23	I	**DRAM Clock Feedback.** Input from the external clock buffer.
RESET#	AD18	I	**Reset.** Input from South Bridge chip. When asserted, this signal resets TwisterK and sets all register bits to the default value. The rising edge of this signal is used to sample all power-up strap options
PWROK	AC19	I	**Power OK.** Connect to South Bridge and Power Good circuitry.

5. Pin Descriptions of Major Components

5.3 VIA VT8231 BGA PCI-LPC/ISA South Bridge

PCI Bus Interface			
Signal Name	**PIN #**	**I/O**	**Signal Description**
AD[31:0]	(see pin list)	IO	**Address/Data Bus.** The standard PCI address and data lines. The address is driven with FRAME# assertion and data is driven or received in following cycles. IDSEL is internally connected to AD28.
C/BE[3:0]#	C5, D6, A8, F10	IO	**Command/Byte Enable.** The command is driven with FRAME# assertion. Byte enables corresponding to supplied or requested data are driven on following clocks.
FRAME#	F6	IO	**Frame.** Assertion indicates the address phase of a PCI transfer. Negation indicates that one more data transfer is desired by the cycle initiator.
IRDY#	C7	IO	**Initiator Ready.** Asserted when the initiator is ready for data transfer.
TRDY#	B7	IO	**Target Ready.** Asserted when the target is ready for data transfer.
STOP#	D7	IO	**Stop.** Asserted by the target to request the master to stop the current transaction.
DEVSEL#	A7	IO	**Device Select.** The VT8231 asserts this signal to claim PCI transactions through positive or subtractive decoding. As an input, DEVSEL# indicates the response to a VT8231-initiated transaction and is also sampled when decoding whether to subtractively decode the cycle.
PAR	C8	IO	**Parity.** A single parity bit is provided over AD[31:0] and C/BE[3:0]#.
SERR#	E7	I	**System Error.** SERR# can be pulsed active by any PCI device that detects a system error condition. Upon sampling SERR# active, the VT8231 can be programmed to generate an NMI to the CPU.
PINTA-D#	B2, B1, C3, C2	I	**PCI Interrupt Request**. These pins are typically connected to the PCI bus INTA#-INTD# pins as follows: PINTA# PINTB# PINTC# PINTD# PCI Slot 1 INTA# INTB# INTC# INTD# PCI Slot 2 INTB# INTC# INTD# INTA# PCI Slot 3 INTC# INTD# INTA# INTB# PCI Slot 4 INTD# INTA# INTB# INTC# PCI Slot 5 INTA# INTB# INTC# INTD#
PCICLK	M17	I	**PCI Clock.** PCLK provides timing for all transactions on the PCI Bus.

Signal Name	PIN #	I/O	Signal Description
PCKRUN#	R5	IO	**PCI Bus Clock Run.** This signal indicates whether the PCI clock is or will be stopped (high) or running (low). The VT8231 drives this signal low when the PCI clock is running (default on reset) and releases it when it stops the PCI clock. External devices may assert this signal low to request that the PCI clock be restarted or prevent it from stopping. Connect this pin to ground using a 100 Ω resistor if the function is not used. Refer to the "PCI Mobile Design Guide" and the VIA "Apollo MVP4 Design Guide" for more details.
PCIRST#	E4	O	**PCI Reset.**
PCISTP# / GPO6	T4	O	**PCI Stop.**
CPUSTP# / GPO5	P4	O	**CPU Stop.**
PREQH#	C1	O	**PCI Request.** This signal goes to the North Bridge REQ4# input to request the PCI bus for high priority access. The internal LAN requests the PCI bus using this signal, so if the LAN subsystem is used, this signal must be connected (one of the H/LREQ/GNT 1 and 2 pairs provided by the VT8231 may be used to implement the fifth PCI slot if desired). If the LAN subsystem is not used, PREQH# / PGNTH# may optionally remain unconnected.
PGNTH#	D3	I	**PCI Grant.** This signal is driven by the North Bridge GNT4# signal to grant high priority PCI access to the VT8231.
PREQL#	D2	O	**PCI Request.** This signal goes to the North Bridge PREQ# input to request the PCI bus for normal priority access.
PGNTL#	D1	I	**PCI Grant.** This signal is driven by the North Bridge PGNT# output to grant normal priority PCI access to the VT8231.
HREQ1#/ GPI10	Y11	I / IO	**High Priority Request 1.** Device 0 Function 4 RxE5[3] = 0.
HGNT1#/ GPO8	W11	O / IO	**High Priority Grant 1.** Device 0 Function 4 RxE5[3] = 0.
HREQ2#/ GPI11	V11	I / IO	**High Priority Request 2.** Device 0 Function 4 RxE5[3] = 0.
HGNT2#/ GPO9	T10	O / IO	**High Priority Grant 2.** Device 0 Function 4 RxE5[3] = 0.
LREQ1#/ GPI12	U10	I / IO	**Low Priority Request 1.** Device 0 Function 4 RxE5[2] = 0.
LGNT1#/ GPO10	Y10	O / IO	**Low Priority Grant 1.** Device 0 Function 4 RxE5[2] = 0.

5. Pin Descriptions of Major Components

5.3 VIA VT8231 BGA PCI-LPC/ISA South Bridge

PCI Bus Interface			
Signal Name	**PIN #**	**I/O**	**Signal Description**
LREQ2#/ GPI13	W10	I / IO	**Low Priority Request 2.** Device 0 Function 4 RxE5[2] = 0.
LGNT2#/ GPO11	V10	O / IO	**Low Priority Grant 2.** Device 0 Function 4 RxE5[2] = 0.

CPU Interface			
Signal Name	**PIN #**	**I/O**	**Signal Description**
CPURST	U4	OD	**CPU Reset.** The VT8231 asserts CPURST to reset the CPU during power-up.
INTR	R6	OD	**CPU Interrupt.** INTR is driven by the VT8231 to signal the CPU that an interrupt request is pending and needs service.
NMI	T5	OD	**Non-Maskable Interrupt.** NMI is used to force a non-maskable interrupt to the CPU. The VT8231 generates an NMI when either SERR# or IOCHK# is asserted.
INIT	V5	OD	**Initialization.** The VT8231 asserts INIT if it detects a shut-down special cycle on the PCI bus or if a soft reset is initiated by the register
STPCLK#	V6	OD	**Stop Clock.** STPCLK# is asserted by the VT8231 to the CPU to throttle the processor clock.
SMI#	Y5	OD	**System Management Interrupt.** SMI# is asserted by the VT8231 to the CPU in response to different Power-Management events.
FERR#	U5	I	**Numerical Coprocessor Error.** This signal is tied to the coprocessor error signal on the CPU. Internally generates interrupt 13 if active.
IGNNE#	T6	OD	**Ignore Numeric Error.** This pin is connected to the “ignore error” pin on the CPU.
SLP#/ GPO7	U6	OD	**Sleep** (F4 RxE4[4] = 1). Used to put the CPU to sleep. Used with slot-1 CPUs only. Not currently used with socket-7 CPUs.
A20M#	W5	OD	**A20 Mask.** Connect to A20 mask input of the CPU to control address bit-20 generation. Logical combination of the A20GATE input (from internal or external keyboard controller) and Port 92 bit-1 (Fast_A20). See Device 0 Function 0 Rx59[1].
DTD+	L2	Analog I	**CPU DTD (Thermal Diode) Channel Plus.** Connect to cathode of first external temperature sensing diode.
DTD-	L3	Analog I	**CPU DTD (Thermal Diode) Channel Minus.** Connect to anode of first external temperature sensing diode.

Note: Connect each of the above signals to 4.7KΩ pullup resistors to VCC3

Strap Options			
Signal Name	**PIN #**	**I/O**	**Signal Description**
Strap/ SUSA#/ GPO1	P1	I / O	**CPURST / INIT Polarity** H: Slot-1 / Socket-370 / Slot-A / Socket-462 L: Socket-7
Strap/ MCCS#/ GPO17	W6	I / O	**CPU Frequency Strapping** H: Disable L: Enable
Strap/ SA16	Y14	I / IO	**BIOS ROM Interface** H: LPC L: Conventional
Strap/ SA17	T13	I / IO	**Auto Reboot** H: Disable (recommended) L: Enable

Note: External strap option values may be set by connecting the indicated external pin to a 4.7K ohm pullup (for 1 or H) or driving it low during reset with a 7407 TTL open collector buffer (for 0 or L) as shown in the suggested circuit below:

Advanced Programmable Interrupt Controller (APIC) Interface			
Signal Name	**PIN #**	**I/O**	**Signal Description**
WSC#/ GPI14	V4	I / I	**Internal APIC Write Snoop Complete.** F0 Rx58[6] = 1. Asserted by the north bridge to indicate that all snoop activity on the CPU bus initiated by the last PCI-to-DRAM write is complete and that it is safe to perform an APIC interrupt.
APICD0/ GPO28	W4	O / O	**Internal APIC Data 0.** F0 Rx58[6] = 1.
APICD1/ GPO29	Y4	O / O	**Internal APIC Data 1.** F0 Rx58[6] = 1.
APICCLK/ GPI9	Y3	I / I	**APIC Clock.** F0 Rx58[6] = 1.

Low Pin Count (LPC) Interface			
Signal Name	**PIN #**	**I/O**	**Signal Description**
LFRAME#	W8	O	**LPC Frame.**
LDRQ#/ GPI15	Y8	I / I	**LPC Data Request.** F0 Rx58[5] = 1.
LAD[3-0]	V7, W7, Y7, V8	IO	**LPC Address / Data.**

Note: For LPC control, see Device 0 Function 0 Rx58[5] and Rx59[4-3]
Note: Connect the LPC interface LPCRST# (LPC Reset) signal to PCIRST#

5. Pin Descriptions of Major Components

5.3 VIA VT8231 BGA PCI-LPC/ISA South Bridge

LAN Controller - Media Independent Interface (MII)			
Signal Name	**PIN #**	**I/O**	**Signal Description**
MCOL	G17	I	**MII Collision Detect.** From the external PHY.
MCRS	G16	I	**MII Carrier Sense.** Asserted by the external PHY when the media is active.
MDCK	C20	O	**MII Management Data Clock.** Sent to the external PHY as a timing reference for MDIO
MDIO	D18	IO	**MII Management Data I/O.** Read from the MDI bit or written to the MDO bit.
MRXCLK	C19	I	**MII Receive Clock.** 2.5 or 25 MHz clock recovered by the PHY.
MRXD[3], **MRXD[2],** **MRXD[1],** **MRXD[0]**	D19 D20 E18 E19	I I I I	**MII Receive Data.** Parallel receive data lines driven by the external PHY synchronous with MRXCLK.
MRXDV	E20	I	**MII Receive Data Valid.**
MRXERR	F18	I	**MII Receive Error.** Asserted by the PHY when it detects a data decoding error.
MTXCLK	F17	I	**MII Transmit Clock.** Always active 2.5 or 25 MHz clock supplied by the PHY.
MTXD[3], **MTXD[2],** **MTXD[1],** **MTXD[0]**	G20 G19 G18 F20	O O O O	**MII Transmit Data.** Parallel transmit data lines synchronized to MTXCLK.
MTXENA	F19	O	**MII Transmit Enable.** Indicates transmit active from the MII port to the PHY.

The internal LAN controller uses the high priority PCI bus request / grant pair (PREQH# / PGNTH#) to request PCI bus access from the chipset north bridge.

Serial EEPROM Interface			
Signal Name	**PIN #**	**I/O**	**Signal Description**
EECS#	C18	O	**Serial EEPROM Chip Select.**
EECK	E16	O	**Serial EEPROM Clock.**
EEDO	D17	O	**Serial EEPROM Data Output.**
EEDI	E17	I	**Serial EEPROM Data Input.**

Universal Serial Bus Interface			
Signal Name	**PIN #**	**I/O**	**Signal Description**
USBP0+	B18	IO	**USB Port 0 Data +**
USBP0-	A18	IO	**USB Port 0 Data -**
USBP1+	B19	IO	**USB Port 1 Data +**
USBP1-	A19	IO	**USB Port 1 Data -**
USBP2+	B20	IO	**USB Port 2 Data +**
USBP2-	A20	IO	**USB Port 2 Data -**
USBP3+	C17	IO	**USB Port 3 Data +**
USBP3-	B17	IO	**USB Port 3 Data -**
USBCLK	C15	I	**USB Clock.** 48MHz clock input for the USB interface
USBOC0#	A17	I	**USB Port 0 Over Current Detect.** Port 0 is disabled if this input is low.
USBOC1#	D16	I	**USB Port 1 Over Current Detect.** Port 1 is disabled if this input is low
USBOC2#/ LA20 / GPI20/ GPO20	W13	I / IO / I / O	**USB Port 2 Over Current Detect.** Port 2 is disabled if this input is low. Device 0 Function 4 RxE4[6] = 0 and Power Management I/O Rx4E[4] = 1.
USBOC3#/ LA21 / GPI20/ GPO21	Y13	I / IO / I / O	**USB Port 3 Over Current Detect.** Port 3 is disabled if this input is low. Device 0 Function 4 RxE4[6] = 0 and Power Management I/O Rx4E[5] = 1.

System Management Bus (SMB) Interface (I²C Bus)			
Signal Name	**PIN #**	**I/O**	**Signal Description**
SMBCK1	R3	IO	**SMB / I²C Channel 1 Clock.**
SMBCK2/ GPIO27	R1	IO / IO	**SMB / I²C Channel 2 Clock†.**
SMBDT1	T1	IO	**SMB / I ²C Channel 1 Data.**
SMBDT2/ GPIO26	R2	IO / IO	**SMB / I²C Channel 2 Data†.**
SMBALRT#/ GPI7	T2	I / I	**SMB Alert.** (System Management Bus I/O space Rx08[3] = 1) When the chip is enabled to allow it, assertion generates an IRQ or SMI interrupt or a power management resume event. The same pin is used as General Purpose Input 6 whose value is reflected in Rx48[6] of function 4 I/O space

* Note: SMBus #2 is a slave-only device used to supply status for external Alert-On-LAN (AOL)

5. Pin Descriptions of Major Components

5.3 VIA VT8231 BGA PCI-LPC/ISA South Bridge

UltraDMA-33 / 66 Enhanced IDE Interface			
Signal Name	**PIN #**	**I/O**	**Signal Description**
PDRDY/ PDDMARDY/ PDSTROBE	N19	I	EIDE Mode: **Primary I/O Channel Ready.** Device ready indicator UltraDMA Mode: **Primary Device DMA Ready**. Output flow control. The device may assert DDMARDY to pause output transfers **Primary Device Strobe**. Input data strobe (both edges). The device may stop DSTROBE to pause input data transfers
SDRDY/ SDDMARDY/ SDSTROBE	Y20	I	EIDE Mode: **Secondary I/O Channel Ready.** Device ready indicator UltraDMA Mode: **Secondary Device DMA Ready**. Output flow control. The device may assert DDMARDY to pause output transfers **Secondary Device Strobe**. Input data strobe (both edges). The device may stop DSTROBE to pause input data transfers
PDIOR#/ PHDMARDY/ PHSTROBE	N18	O	EIDE Mode: **Primary Device I/O Read.** Device read strobe UltraDMA Mode: **Primary Host DMA Ready**. Primary channel input flow control**.** The host may assert HDMARDY to pause input transfers **Primary Host Strobe**. Output data strobe (both edges). The host may stop HSTROBE to pause output data transfers
SDIOR#/ SHDMARDY/ SHSTROBE	W19	O	EIDE Mode: **Secondary Device I/O Read.** Device read strobe UltraDMA Mode: **Secondary Host DMA Ready**. Input flow control. The host may assert HDMARDY to pause input transfers **Host Strobe B**. Output strobe (both edges). The host may stop HSTROBE to pause output data transfers
PDIOW#/ PSTOP	P20	O	EIDE Mode: **Primary Device I/O Write.** Device write strobe UltraDMA Mode: **Primary Stop**. Stop transfer: Asserted by the host prior to initiation of an UltraDMA burst; negated by the host before data is transferred in an UltraDMA burst. Assertion of STOP by the host during or after data transfer in UltraDMA mode signals the termination of the burst.
SDIOW#/ SSTOP	Y19	O	EIDE Mode: **Secondary Device I/O Write.** Device write strobe UltraDMA Mode: **Secondary Stop**. Stop transfer: Asserted by the host prior to initiation of an UltraDMA burst; negated by the host before data is transferred in an UltraDMA burst. Assertion of STOP by the host during or after data transfer in UltraDMA mode signals the termination of the burst.

Signal Name	**PIN #**	**I/O**	**Signal Description**
PDDRQ	P19	I	**Primary Device DMA Request.** Primary channel DMA request
SDDRQ	U17	I	**Secondary Device DMA Request.** Secondary channel DMA request
PDDACK#	N20	O	**Primary Device DMA Acknowledge.** Primary channel DMA acknowledge
SDDACK#	W20	O	**Secondary Device DMA Acknowledge.** Secondary channel DMA acknowledge
IRQ14	T14	I	**Primary Channel Interrupt Request.**
IRQ15	U14	I	**Secondary Channel Interrupt Request.**
PDCS1#	L18	O	**Primary Master Chip Select.** This signal corresponds to CS1FX# on the primary IDE connector.
PDCS3#	L19	O	**Primary Slave Chip Select.** This signal corresponds to CS3FX# on the primary IDE connector.
SDCS1#	U18	O	**Secondary Master Chip Select.** This signal corresponds to CS17X# on the secondary IDE connector.
SDCS3#	U19	O	**Secondary Slave Chip Select.** This signal corresponds to CS37X# on the secondary IDE connector.
PDA[2-0]	M20, M18, M19	O	**Primary Disk Address.** PDA[2:0] are used to indicate which byte in either the ATA command block or control block is being accessed.
SDA[2-0]	V20, V18, V19	O	**Secondary Disk Address.** SDA[2:0] are used to indicate which byte in either the ATA command block or control block is being accessed.
PDD[15-0]	T17, R17, T18, T20, P17, N16, R19, P18, R18, R20, N17, P16, T19, U20, R16, T16	IO	**Primary Disk Data**
SDD[15-0] / SA[15-0]	W18, V17, Y17, W16, V15, Y15, W14, T15, U15, U16, V14, W15, Y16, V16, W17, Y18	IO	**Secondary Disk Data** (SPKR strap 4.7K ohms low) **or ISA Address** (SPKR strap 4.7K ohms high)

MIDI Interface			
Signal Name	**PIN #**	**I/O**	**Signal Description**
MSI	G4	I	**MIDI Serial In**
MSO	J4	O	**MIDI Serial Out**

5. Pin Descriptions of Major Components

5.3 VIA VT8231 BGA PCI-LPC/ISA South Bridge

AC97 Audio / Modem Interface			
Signal Name	**PIN #**	**I/O**	**Signal Description**
ACRST	G2	O	**AC97 Reset**
ACSYNC	G1	O	**AC97 Sync**
ACSDOUT	H3	O	**AC97 Serial Data Out**
ACSDIN0	H1	I	**AC97 Serial Data In 0**
ACSDIN1	H2	I	**AC97 Serial Data In 1**
ACBITCLK	J3	I	**AC97 Bit Clock**

Parallel Port Interface			
Signal Name	**PIN #**	**I/O**	**Signal Description**
PINIT#/ DIR#	B12	IO / O	**Initialize.** Initialize printer. Output in standard mode, I/O in ECP/EPP mode.
STROBE#/ nc	A11	IO / -	**Strobe.** Output used to strobe data into the printer. I/O in ECP/EPP mode.
AUTOFD#/ DRVEN0	E11	IO / O	**Auto Feed.** Output used to cause the printer to automatically feed one line after each line is printed. I/O pin in ECP/EPP mode.
SLCTIN#/ STEP#	D12	IO / O	**Select In.** Output used to select the printer. I/O pin in ECP/EPP mode.
SLCT/ WGATE#	E13	I / O	**Select.** Status output from the printer. High indicates that it is powered on.
ACK#/ DS1#	B14	I / O	**Acknowledge.** Status output from the printer. Low indicates that it has received the data and is ready to accept new data
ERROR#/ HDSEL#	F11	I / O	**Error.** Status output from the printer. Low indicates an error condition in the printer.
BUSY/ MTR1#	A14	I / O	**Busy.** Status output from the printer. High indicates not ready to accept data.
PE/ WDATA#	D13	I / O	**Paper End.** Status output from the printer. High indicates that it is out of paper.
PD7/ nc, **PD6**/ nc, **PD5**/ nc, **PD4**/ DSKCHG#, **PD3**/ RDATA#, **PD2**/ WRTPRT#, **PD1**/ TRK00#, **PD0**/ INDEX#	C14 A13 B13 C13 E12 A12 C12 D11	IO / - IO / - IO / - IO / I IO / I IO / I IO / I IO / I	**Parallel Port Data.**

As shown by the alternate functions above, in mobile applications the parallel port pins can optionally be selected to function as a floppy disk interface for attachment of an external floppy drive using the parallel port connector (see Super I/O Configuration Index F6[5]).

Game Port Interface			
Signal Name	**PIN #**	**I/O**	**Signal Description**
JAX	J1	I	**Joystick A X-axis**
JAY	K4	I	**Joystick A Y-axis**
JBX	K5	I	**Joystick B X-axis**
JBY	J2	I	**Joystick B Y-axis**
JAB1/ GPI28	G3	I	**Joystick A Button 1.** Device 0 Function 0 Rx53[7] = 0.
JAB2/ GPO12	H5	I	**Joystick A Button 2.** Device 0 Function 4 RxE5[4] = 0.
JBB1/ GPI29	F1	I	**Joystick B Button 1.** Device 0 Function 0 Rx53[7] = 0.
JBB2/ GPO13	H4	I	**Joystick B Button 2.** Device 0 Function 4 RxE5[4] = 0.

See Function 0 Rx77[6]

Floppy Disk Interface			
Signal Name	**PIN #**	**I/O**	**Signal Description**
DRVDEN0	L17	O	**Drive Density Select 0.**
DRVDEN1	K17	O	**Drive Density Select 1.**
MTR0#	K18	O	**Motor Control 0.** Select motor on drive 0.
MTR1#	J16	O	**Motor Control 1.** Select motor on drive 1
DS0#	J17	O	**Drive Select 0.** Select drive 0.
DS1#	K19	O	**Drive Select 1.** Select drive 1
DIR#	K20	O	**Direction.** Direction of head movement (0 = inward motion, 1 = outward motion)
STEP#	J18	O	**Step.** Low pulse for each track-to-track movement of the head.
INDEX#	L20	I	**Index.** Sense to detect that the head is positioned over the beginning of a track
HDSEL#	H19	O	**Head Select.** Selects the side for R/W operations (0 = side 1, 1 = side 0)
TRK00#	H16	I	**Track 0.** Sense to detect that the head is positioned over track 0.
RDATA#	H20	I	**Read Data.** Raw serial bit stream from the drive for read operatrions.
WDATA#	J19	O	**Write Data.** Encoded data to the drive for write operations.
WGATE#	J20	O	**Write Gate.** Signal to the drive to enable current flow in the write head.
DSKCHG#	H18	I	**Disk Change.** Sense that the drive door is open or the diskette has been changed since the last drive selection.
WRTPRT#	H17	I	**Write Protect.** Sense for detection that the diskette is write protected (causes write commands to be ignored)

See also Parallel Port pin descriptions for optional Floppy Disk interface functionality

5. Pin Descriptions of Major Components

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Serial Port and Infrared Interface			
Signal Name	**PIN #**	**I/O**	**Signal Description**
TXD	B15	O	**Transmit Data.** Serial port transmit data out.
RXD	E14	I	**Receive Data.** Serial port receive data in.
IRTX/ GPO14	R8	O / O	**Infrared Transmit.** IR transmit data out (Function 4 RxE5[5] = 0) selectable from serial port 1, 2, or 3.
IRRX/ GPO15	U8	I / O	**Infrared Receive.** IR receive data in (Function 4 RxE5[5] = 0) selectable to serial port 1, 2, or 3.
IRRX2/ GPIOB	T8	I	**Infrared Receive.** IR receive data in (see FIR I/O Rx33 and 34)
RTS#	A15	O	**Request To Send.** Indicator that the serial output port is ready to transmit data. Typically used as hardware handshake with CTS# for low level flow control. Designed for direct input to external RS-232C driver.
CTS#	B16	I	**Clear To Send.** Indicator to the serial port that an external communications device is ready to receive data. Typically used as hardware handshake with RTS# for low level flow control. Designed for input from external RS-232C receiver.
DTR#	A16	O	**Data Terminal Ready.** Indicator that serial port is powered, initialized, and ready. Typically used as hardware handshake with DSR# for overall readiness to communicate. Designed for direct input to external RS-232C driver.
DSR#	D14	I	**Data Set Ready.** Indicator to serial port that an external serial communications device is powered, initialized, and ready. Typically used as hardware handshake with DTR# for overall readiness to communicate. Designed for direct input from external RS-232C receiver.
DCD#	D15	I	**Data Carrier Detect.** Indicator to serial port that an external modem is detecting a carrier signal (i.e., a communications channel is currently open). In direct connect environments, this input will typically be driven by DTR# as part of the DTR/DSR handshake. Designed for direct input from external RS-232C receiver.
RI#	C16	I	**Ring Indicator.** Indicator to serial port that an external modem is detecting a ring condition. Used by software to initiate operations to answer and open the communications channel. Designed for direct input from external RS-232C receiver (whose input is typically not connected in direct connect environments).

Conventional BIOS ROM / ISA Bus Interface			
Signal Name	**PIN #**	**I/O**	**Signal Description**
LA21/ USBOC3# / GPI21/ GPO21 **LA20**/ USBOC2# / GPI20/ GPO20	Y13 W13	O O	**System Address Bus** (Device 0 Function 4 RxE4[6] = 1). Allows access to physical memory devices (e.g., BIOS ROMs) up to 4 Mbytes.
SA[19:18], **SA17**/ strap, **SA16**/ strap, **SA[15:0]** / SDD[15:0]	V13, U13, T13, Y14, W18, V17, Y17, 16, V15, Y15, W14, 15, U15, U16, V14, 15, Y16, V16, W17, Y18	IO	**System Address Bus**. These address lines are used to interface to BIOS ROMs but may also be used to implement a subset of the ISA bus if required. SA[19-16] are connected to ISA bus SA[19-16] directly. SA[19-17] are also connected to LA[19-17] of the ISA bus. SA17 strap – 0/1 = Enable / Disable Auto Reboot SA16 strap – 0/1 = Disable / Enable LPC ROM
SD[7-0]	T11, R11, U11, U12, Y12, W12, V12, R12	IO	**System Data.** SD[7:0] provide the data path for BIOS ROMs and other 8-bit devices residing on the ISA bus.
IOR#/ GPI22/ GPO22	U7	IO	**I/O Read** (F4 RxE4[7] = 1). IOR# is the command to an ISA I/O slave device that the slave may drive data on to the ISA data bus.
IOW#/ GPI23/ GPO23	T7	IO	**I/O Write** (F4 RxE4[7] = 1). IOW# is the command to an ISA I/O slave device that the slave may latch data from the ISA data bus.
MEMR#	W9	IO	**Memory Read.** MEMR# is the command to a memory slave that it may drive data onto the ISA data bus.
MEMW#	Y9	IO	**Memory Write.** MEMW# is the command to a memory slave that it may latch data from the ISA data bus.
IRQ1/ MSCK	N2	I	**Interrupt 1 (optional external Keyboard Controller).**
IRQ12/ MSDT	N4	I	**Interrupt 12 (optional external PS2 Mouse Controller).**
IRQ14	T14	I	**Interrupt 14 (IDE Primary Channel).**
IRQ15	U14	I	**Interrupt 15 (IDE Secondary Channel).**
SPKR	U9	O	**Speaker Drive.** Output of internal timer/counter 2.

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Serial IRQ			
Signal Name	**PIN #**	**I/O**	**Signal Description**
SERIRQ	V9	I	**Serial IRQ.**

Internal Keyboard Controller			
Signal Name	**PIN #**	**I/O**	**Signal Description**
MSCK / IRQ1	N2	IO / I	**MultiFunction Pin** (Internal mouse controller enabled by Rx5A[1]) Rx5A[1]=1 **Mouse Clock.** From internal mouse controller. Rx5A[1]=0 **Interrupt Request 1**. Interrupt 1 (external KBC).
MSDT / IRQ12	N4	IO / I	**MultiFunction Pin** (Internal mouse controller enabled by Rx5A[1]) Rx5A[1]=1 **Mouse Data.** From internal mouse controller. Rx5A[1]=0 **Interrupt Request 12**. Interrupt 12 (ext PS2 mouse ctlr).
KBCK / A20GATE	M4	IO / I	**MultiFunction Pin** (Internal keyboard controller enabled by Rx5A[0]) Rx5A[0]=1 **Keyboard Clock.** From internal keyboard controller Rx5A[0]=0 **Gate A20.** Input from external keyboard controller.
KBDT / KBRC	N1	IO / I	**MultiFunction Pin** (Internal keyboard controller enabled by Rx5A[0]) Rx5A[0]=1 **Keyboard Data.** From internal keyboard controller. Rx5A[0]=0 **Keyboard Reset.** From external keyboard controller (KBC) for CPURST# generation
KBCS# / ROMCS#	T9	O / O	**Keyboard Chip Select** (Rx5A[0]=0). To external keyboard controller chip.

Chip Selects			
Signal Name	**PIN #**	**I/O**	**Signal Description**
ROMCS#/ KBCS#	T9	O / O	**ROM Chip Select** (Rx5A[0]=1). Chip Select to the BIOS ROM. See also Device 0 Rx40[5-4] and Rx41.
MCCS#/ GPO17/ strap	W6	O / IO	**Microcontroller Chip Select** (Device 0 Function 4 RxE4[3] = 0). Asserted during read or write accesses to I/O ports 62h or 66h. Strap: 0/1 = Enable / Disable CPU Frequency Strapping
PCS0#/ GPO16	Y6	O / IO / IO	**Programmable Chip Select 0.** (Device 0 Function 4 RxE4[2] = 0). Asserted during I/O cycles to programmable read or write ISA I/O port ranges.
PCS1#/ GPI19/ GPO19	G5	O / I / O	**Programmable Chip Select 1.** See Device 0 Func 4 RxE4[5] and E5[1]

General Purpose Inputs			
Signal Name	**PIN #**	**I/O**	**Signal Description**
GPI0	F4	I / I	**General Purpose Input 0.**
GPI1	V3	I / I	**General Purpose Input 1.**
GPI2 / EXTSMI#	W1	I / IO	**General Purpose Input 2.**
GPI3 / RING#	U3	I / I	**General Purpose Input 3.**
GPI4 / LID	V2	I / I	**General Purpose Input 4.**
GPI5 / BATLOW#	T3	I / I	**General Purpose Input 5.**
GPI6 / PME#	U1	I / I	**General Purpose Input 6.**
GPI7 / SMBALRT#	T2	I / I	**General Purpose Input 7.**
GPI8 / INTRUDER#	F3	I / I	**General Purpose Input 8.**
GPI9 / APICCLK	Y3	I / I	**General Purpose Input 9.** Rx58[6]=0
GPI10 / HREQ1#	Y11	I / I	**General Purpose Input 10.** F4 RxE5[3]=1
GPI11 / HREQ2#	V11	I / I	**General Purpose Input 11.** F4 RxE5[3]=1
GPI12 / LREQ1#	U10	I / I	**General Purpose Input 12.** F4 RxE5[2]=1
GPI13 / LREQ2#	W10	I / I	**General Purpose Input 13.** F4 RxE5[2]=1
GPI14 / WSC#	V4	I / I	**General Purpose Input 14.** Rx58[6]=0
GPI15 / LDRQ#	Y8	I / I / I	**General Purpose Input 15.** Rx58[5]=0 & F4 RxE5[7]=0
GPI16 / CPUMISS	V1	I / I	**General Purpose Input 16.**
GPI17 / AOLGPI / THRM	P3	I / I / I	**General Purpose Input 17.** F4 Rx40[7]=1
GPI18 / GPO18 / FAN2 / SLPBTN#	K3	I / O / I / I	**General Purpose Input 18.** F4 RxE5[0]=0
GPI19 / GPO19 / PCS1#	G5	I / O / I / O	**General Purpose Input 19.** F4 RxE5[1]=0 & E4[5]=1
GPI20 / GPO20 / LA20 / USBOC2#	W13	I / O / IO / I	**General Purpose Input 20.** F4 RxE4[6]=0, PMIO 4E[4]=1
GPI21 / GPO21 / LA21 / USBOC3#	Y13	I / O / IO / I	**General Purpose Input 21.** F4 RxE4[6]=0, PMIO 4E[5]=1
GPI22 / GPO22 / IOR#	U7	I / O / IO	**General Purpose Input 22.** F4 RxE4[7]=0, PMIO 4E[6]=1
GPI23 / GPO23 / IOW#	T7	I / O / IO	**General Purpose Input 23.** F4 RxE4[7]=0, PMIO 4E[7]=1
GPI24 / GPO24 / GPIOA	Y2	I / O / IO	**General Purpose Input 24.** F4 RxE6[0]=0

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Signal Name	PIN #	I/O	Signal Description
GPI25 / **GPO25** / GPIOC / ATEST / CHSINOUT	J5	I/ O/ IO/ O/ IO	**General Purpose Input 25.** F4 RxE6[1]=0 & E5[6]=0 (F4 RxE5[6]=1 to enable CHSINOUT function on this pin)
GPI26 / **GPO26** / SMBDT2	R2	I/ O/ IO	**General Purpose Input 26.** F4 Rx55[2]=1&55[3]=0
GPI27 / **GPO27** / SMBCK2	R1	I/ O / IO	**General Purpose Input 27.** F4 Rx55[2]=1&55[3]=0
GPI28 / JAB1	G3	I / I	**General Purpose Input 28.** Rx53[7]=0
GPI29 / JBB1	F1	I / I	**General Purpose Input 29.** Rx53[7]=0
GPI30 / **GPO30** / GPIOD / DTEST	Y1	I / O / IO / O	**General Purpose Input 30.** F4 RxE6[6]=0
GPI31 / **GPO31** / GPIOE	W3	I / O / IO	**General Purpose Input 31.** F4 RxE6[7]=0

Note: See also Power Management I/O Registers Rx48-4B, 50, and 52 and APIC registers 48-4B for GPI pin control

General Purpose Outputs			
Signal Name	**PIN #**	**I/O**	**Signal Description**
GPO0 / SLOWCLK	R4	O / O	**General Purpose Output 0.** (Func 4 Rx54[1-0] = 00). Output value determined by PMU I/O Rx4C[0]
GPO1 / SUSA# / strap	P1	O / O / I	**General Purpose Output 1.** F4 Rx54[2]=1
GPO2 / SUSB#	P2	O / O	**General Purpose Output 2.** F4 Rx54[3]=1
GPO3 / SUSST1#	N5	O / O	**General Purpose Output 3.** F4 Rx54[4]=1
GPO4 / SUSCLK	P4	O / O	**General Purpose Output 4.** F4 Rx55[1]=1
GPO5 / CPUSTP#	W2	O / O	**General Purpose Output 5.** F4 RxE4[0]=1
GPO6 / PCISTP#	T4	O / O	**General Purpose Output 6.** F4 RxE4[1]=1
GPO7 / SLP#	U6	O / O	**General Purpose Output 7.** F4 RxE4[4]=1
GPO8 / HGNT1#	W11	O / O	**General Purpose Output 8.** F4 RxE5[3]=1
GPO9 / HGNT2#	T10	O / O	**General Purpose Output 9.** F4 RxE5[3]=1
GPO10 / LGNT1#	Y10	O / O	**General Purpose Output 10.** F4 RxE5[2]=1
GPO11 / LGNT2#	V10	O / O	**General Purpose Output 11.** F4 RxE5[2]=1
GPO12 / JAB2	H5	O/I	**General Purpose Output 12.** Rx53[7]=0 & F4 RxE5[4]=1
GPO13 / JBB2	H4	O/I	**General Purpose Output 13.** Rx53[7]=0 & F4 RxE5[4]=1
GPO14 / IRTX	R8	O / O	**General Purpose Output 14.** F4 RxE5[5]=1

Signal Name	PIN #	I/O	Signal Description
GPO15 / IRRX	U8	O / I	**General Purpose Output 15.** F4 RxE5[5]=1
GPO16 / PCS0#	Y6	O / O	**General Purpose Output 16.** F4 RxE4[2]=1
GPO17 / MCCS#	W6	O / O	**General Purpose Output 17.** F4 RxE4[3]=1
GPO18 / **GPI18** / FAN2 / SLPBTN#	K3	O / I / I / I	**General Purpose Output 18.** F4 RxE5[0]=1
GPO19 / **GPI19** / PCS1#	G5	O / I / O / I	**General Purpose Output 19.** F4 RxE4[5]=1 & RxE5[1]=1
GPO20 / **GPI20** / LA20 / USBOC2#	W13	O / IO / I	**General Purpose Output 20.** F4 RxE4[6]=0
GPO21 / **GPI21** / LA21 / USBOC3#	Y13	O / IO / I	**General Purpose Output 21.** F4 RxE4[6]=0
GPO22 / **GPI22** / IOR#	U7	O / I / IO	**General Purpose Output 22.** F4 RxE4[7]=0
GPO23 / **GPI23** / IOW#	T7	O / I / IO	**General Purpose Output 23.** F4 RxE4[7]=0
GPO24 / **GPI24** / GPIOA	Y2	O / I / IO	**General Purpose Output 24.** F4 RxE6[0]=1
GPO25 / **GPI25** / GPIOC / ATEST / CHSINOUT	J5	O/ I/ IO/ O/ IO	**General Purpose Output 25.** F4 RxE6[1]=1
GPO26 / **GPI26** / SMBDT2	R2	O / I / IO	**General Purpose Output 26.** F4 Rx55[3-2]=11
GPO27 / **GPI27** / SMBCK2	R1	O / I / IO	**General Purpose Output 27.** F4 Rx55[3-2]=11
GPO28 / APICD0	W4	O / O	**General Purpose Output 28.** Rx58[7-6]=00
GPO29 / APICD1	Y4	O / O	**General Purpose Output 29.** Rx58[7-6]=00
GPO30 / **GPI30** / GPIOD / DTEST	Y1	O / I / IO / O	**General Purpose Output 30.** F4 RxE6[6]=1
GPO31 / **GPI31** / GPIOE	W3	O / I / IO	**General Purpose Output 31.** F4 RxE6[7]=1

Note: See also Power Management I/O Registers Rx4C-4F to set GPO pin output values and also APIC registers 4C-4F

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General Purpose I/Os			
Signal Name	**PIN #**	**I/O**	**Signal Description**
GPIOA / GPI24 / GPO24	Y2	IO / I / O	**General Purpose I/O A / 24.** (F4 RxE6[0] defines as GPI or GPO)
GPIOB / IRRX2	T8	IO / I	**General Purpose I/O B.** (See FIR I/O Rx33 and 34)
GPIOC / GPI25 / GPO25 / ATEST / CHSINOUT	J5	IO / I / O / O	**General Purpose I/O C / 25.** (F4 RxE6[1] defines as GPI or GPO)
GPIOD / GPI30 / GPO30 / DTEST	Y1	IO / I / O / O	**General Purpose I/O D / 30.** (F4 RxE6[6] defines as GPI or GPO)
GPIOE / GPI31 / GPO31	W3	IO	**General Purpose I/O E / 31.** (F4 RxE6[7] defines as GPI or GPO)

Hardware Monitoring			
Signal Name	**PIN #**	**I/O**	**Signal Description**
UIC1	M1	Analog I	**Universal Input Channel.** For temperature / voltage monitoring.
UIC2	M3	Analog I	**Universal Input Channel.** For temperature / voltage monitoring.
UIC3	M2	Analog I	**Universal Input Channel.** For temperature / voltage monitoring.
UIC4	L4	Analog I	**Universal Input Channel.** For temperature / voltage monitoring.
UIC5	L1	Analog I	**Universal Input Channel.** For temperature / voltage monitoring.
DTD+	L2	Analog I	**CPU DTD (Thermal Diode) Channel Plus.**
DTD-	L3	Analog I	**CPU DTD (Thermal Diode) Channel Minus.**
VREF	K1	O	**Voltage Reference for Thermal Sensing** (2.2V 3%)
FAN1	K2	I	**Fan Speed Monitor 1.** (3.3V only)
FAN2 / SLPBTN# / GPI18 / GPO18	K3	I / I / I / O	**Fan Speed Monitor 2.** (3.3V only) (F4 RxE5[0] = 0)
DTEST / GPIOD (30)	Y1	O	**Hardware Monitor Digital Test Out**
ATEST / GPIOC (25) / CHSINOUT	J2	O	**Hardware Monitor Analog Test Out**

Power Management and External State Monitoring			
Signal Name	**PIN #**	**I/O**	**Signal Description**
PME# / GPI6	U1	I / I	**Power Management Event.** (Rx74[1]=0) (1K PU to VCCS if not used)
EXTSMI# / GPI2	W1	IOD / I	**External System Management Interrupt.** When enabled to allow it, a falling edge on this input causes an SMI# to be generated to the CPU to enter SMI mode. (10K PU to VCCS if not used) (3.3V only)
SMBALRT# / GPI7	T2	I / I	**SMB Alert** (System Management Bus I/O space Rx08[3] = 1). When the chip is enabled to allow it, assertion generates an IRQ or SMI or power management event. (10K PU to VCCS if not used)
THRM / AOLGPI / GPI17	P3	I / I / I	**Monitor Input - Thermal Alarm.** (F4 Rx40[7]=0) (1K PU to VCCS if not used)
LID / GPI4	V2	I / I	**Monitor Input - Notebook Computer Display Lid Open / Closed.** Used by the Power Management subsystem to monitor the opening and closing of the display lid of notebook computers. Can be used to detect either low-to-high and/or high-to-low transitions to generate an SMI#. The VT8231 performs a 200 usec debounce of this input if Function 4 Rx40[5] is set to 1. (10K PU to VCCS if not used)
RING# / GPI3	U3	I / I	**Monitor Input – Modem Ring.** May be connected to external modem circuitry to allow the system to be re-activated by a received phone call. (10K PU to VCCS if not used)
BATLOW# / GPI5	T3	I / I	**Monitor Input - Battery Low.** (10K PU to VCCS if not used)
CPUMISS / GPI16	V1	I / I	**Monitor Input - CPU Missing.** Indicates whether the CPU is plugged in correctly.
AOLGPI / GPI17 / THRM	P3	I / I / I	**Monitor Input - Awake On LAN External Event.** F4 Rx40[7]=1
INTRUDER# / GPI8	F3	I / I	**Monitor Input – Chassis Intrusion.**
RSMRST#	F2	I	**Resume Reset.** Resets the internal logic connected to the VCCS power plane and also resets portions of the internal RTC logic.
SUSA# / GPO1 / strap	P1	O / O / I	**Suspend Plane A Control** (Function 4 Rx54[2]=0). Asserted during power management POS, STR, and STD suspend states. Used to control the primary power plane. (10K PU to VCCS if not used)

5. Pin Descriptions of Major Components

5.3 VIA VT8231 BGA PCI-LPC/ISA South Bridge

Power Management and External State Monitoring			
Signal Name	**PIN #**	**I/O**	**Signal Description**
SUSB#/ GPO2	P2	O / O	**Suspend Plane B Control** (Function 4 Rx54[3]=0). Asserted during power management STR and STD suspend states. Used to control the secondary power plane. (10K PU to VCCS if not used)
SUSC#/ GPO	N3	O / O	**Suspend Plane C Control.** Asserted during power management STD suspend state. Used to control the tertiary power plane. Also connected to ATX power-on circuitry.
SUSST1#/ GPO3	N5	O / O	**Suspend Status 1** (Function 4 Rx54[4] = 0). Typically connected to the North Bridge to provide information on host clock status. Asserted when the system may stop the host clock, such as Stop Clock or during POS, STR, or STD suspend states. Connect 10K PU to VCCS.
SUSCLK GPO4	W2	O / O	**Suspend Clock** (Function 4 Rx55[1]=0). 32.768 KHz output clock for use by the North Bridge (e.g., Apollo MVP3 or MVP4) for DRAM refresh purposes. Stopped during Suspend-to-Disk and Soft-Off modes. Connect 10K PU to VCCS.

Resets, Clocks, and Clock Control			
Signal Name	**PIN #**	**I/O**	**Signal Description**
PWRGD	E2	I	**Power Good.** Connected to the PWRGOOD signal on the Power Supply.
PWRBTN#	U2	I	**Power Button.** Used by the Power Management subsystem to monitor an external system on/off button or switch. The VT8231 performs a 200us debounce of this input if Function 4 Rx40[5] is set to 1. (3.3V only)
SLPBTN#/ FAN2/ GPIO18	K3	I / I / IO	**Sleep Button** (Function 4 Rx40[6] = 1). Used by the power management subsystem to monitor an external system sleep button or switch. Connect to VCC if not used.
PCIRST#	E4	O	**PCI Reset.** Active low reset signal for the PCI bus. The VT8231 will assert this pin during power-up or from the control register.
RTCX1	E3	I	**RTC Crystal Input**: 32.768 KHz crystal or oscillator input. This input is used for the internal RTC and for power-well power management logic.
RTCX2	F5	O	**RTC Crystal Output**: 32.768 KHz crystal output
OSC	T12	I	**Oscillator.** 14.31818 MHz clock signal used by the internal Timer.
SLOWCLK/ GPO0	R4	O	**Slow Clock.** Frequency selectable if PMU function 4 Rx54[1-0] is nonzero (set to 01, 10, or 11).
CPUSTP#/ GPO5	P4	O / O	**CPU Clock Stop** (Function 4 RxE4[0] = 0). Signals the system clock generator to disable the CPU clock outputs. Not connected if not used. See also PMU I/O Rx2C[3].
PCISTP#/ GPO6	T4	O / O	**PCI Clock Stop** (Function 4 RxE4[1] = 0). Signals the system clock generator to disable the PCI clock outputs. Not connected if not used.

5. Pin Descriptions of Major Components

5.4 PC Card Interface controller

Multifunction and Miscellaneous Pins

TERMINAL NAME	TERMINAL NO. PDV	TERMINAL NO. GHK	I/O	DESCRIPTION
MFUNC0	154	F15	I/O	Multifunction terminal 0. MFUNC0 can be configured as parallel PCI interrupt INTA, GPI0, GPO0, socket activity LED output, ZV switching outputs, CardBus audio PWM, GPE, or a parallel IRQ.
MFUNC1	155	E17	I/O	Multifunction terminal 1. MFUNC1 can be configured as parallel PCI interrupt INTB, GPI1, GPO1, socket activity LED output, ZV switching outputs, CardBus audio PWM, GPE, or a parallel IRQ. Serial data (SDA). When LATCH is detected low after a PCI reset, the MFUNC1 terminal provides the SDA signaling for the serial bus interface. The two-pin serial interface loads the subsystem identification and other register defaults from an EEPROM after a PCI reset.
MFUNC2	157	A16	I/O	Multifunction terminal 2. MFUNC2 can be configured as PC/PCI DMA request, GPI2, GPO2, socket activity LED output, ZV switching outputs, CardBus audio PWM, GPE, RI_OUT, or a parallel IRQ.
MFUNC3	158	C15	I/O	Multifunction terminal 3. MFUNC3 can be configured as a parallel IRQ or the serialized interrupt signal IRQSER.
MFUNC4	159	E14	I/O	Multifunction terminal 4. MFUNC4 can be configured as PCI LOCK, GPI3, GPO3, socket activity LED output, ZV switching outputs, CardBus audio PWM, GPE, RI_OUT, or a parallel IRQ. See Section 4.30, Multifunction Routing Register, for configuration details. Serial clock (SCL). When LATCH is detected low after a PCI reset, the MFUNC4 terminal provides the SCL signaling for the serial bus interface. The two-pin serial interface loads the subsystem identification and other register defaults from an EEPROM after a PCI reset.
MFUNC5	160	F13	I/O	Multifunction terminal 5. MFUNC5 can be configured as PC/PCI DMA grant, GPI4, GPO4, socket activity LED output, ZV switching outputs, CardBus audio PWM, GPE, or a parallel IRQ.
MFUNC6	161	B15	I/O	Multifunction terminal 6. MFUNC6 can be configured as a PCI CLKRUN or a parallel IRQ.
RI_OUT/PME	163	C14	O	Ring indicate out and power management event output. Terminal provides an output for ring-indicate or PME signals.
SPKROUT	149	G15	O	Speaker output. SPKROUT is the output to the host system that can carry SPKR or CAUDIO through the PCI1420 from the PC Card interface. SPKROUT is driven as the exclusive-OR combination of card SPKR//CAUDIO inputs.
SUSPEND	156	D19	I	Suspend. SUSPEND protects the internal registers from clearing when the GRST or PRST signal is asserted.

16-Bit PC Card Address and Data (Slots A and B)

TERMINAL NAME	TERMINAL NO. SLOT A† PDV	TERMINAL NO. SLOT A† GHK	TERMINAL NO. SLOT B‡ PDV	TERMINAL NO. SLOT B‡ GHK	I/O	DESCRIPTION
A25	121	M18	55	R6	O	PC Card address. 16-bit PC Card address lines. A25 is the most significant bit.
A24	118	N19	53	W4		
A23	116	N17	51	R3		
A22	114	P19	49	R2		
A21	111	P17	47	R1		
A20	109	R18	45	N5		
A19	107	P15	42	N6		
A18	105	T19	40	N2		
A17	103	U15	37	M6		
A16	112	P18	48	P6		
A15	115	M14	50	P5		
A14	108	N14	43	P1		
A13	106	R17	41	N3		
A12	117	N18	52	T1		
A11	100	P14	34	M1		
A10	95	W14	29	L1		
A9	102	R14	36	M3		
A8	104	W16	39	N1		
A7	119	M15	54	U5		
A6	123	L19	57	V5		
A5	125	L17	59	U6		
A4	126	L15	60	V6		
A3	128	K19	62	W6		
A2	131	K15	65	V7		
A1	132	K14	66	W7		
A0	133	J19	67	R8		

5. Pin Descriptions of Major Components

5.4 PC Card Interface controller

NAME	TERMINAL NO. SLOT A† PDV	SLOT A† GHK	SLOT B‡ PDV	SLOT B‡ GHK	I/O	DESCRIPTION
D15	93	U13	27	K5	I/O	PC Card data. 16-bit PC Card data lines. D15 is the most significant bit.
D14	91	W13	25	K2		
D13	89	P12	23	J6		
D12	87	V12	20	J2		
D11	84	P11	18	H1		
D10	147	F19	81	W11		
D9	145	G17	79	R10		
D8	142	H15	77	V10		
D7	92	V13	26	K3		
D6	90	R12	24	K1		
D5	88	U12	21	J3		
D4	85	R11	19	J1		
D3	83	U11	17	H2		
D2	146	G14	80	P10		
D1	144	G18	78	U10		
D0	141	H14	76	W10		

† Terminal name for slot A is preceded with A_. For example, the full name for terminals 121 and M18 are A_A25.

‡ Terminal name for slot B is preceded with B_. For example, the full name for terminals 55 and R6 are B_A25.

16-Bit PC Card Interface Control (Slots A and B)

NAME	TERMINAL NO. SLOT A† PDV	SLOT A† GHK	SLOT B‡ PDV	SLOT B‡ GHK	I/O	DESCRIPTION
BVD1 (STSCHG/RI)	138	H19	72	V9	I	Battery voltage detect 1. BVD1 is generated by 16-bit memory PC Cards that include batteries. BVD1 is used with BVD2 as an indication of the condition of the batteries on a memory PC Card. Both BVD1 and BVD2 are high when the battery is good. When BVD2 is low and BVD1 is high, the battery is weak and should be replaced. When BVD1 is low, the battery is no longer serviceable and the data in the memory PC Card is lost. See Section 5.6, ExCA Card Status-Change-Interrupt Configuration Register, for enable bits. Status change. STSCHG is used to alert the system to a change in the READY, write protect, or battery voltage dead condition of a 16-bit I/O PC Card. Ring indicate. RI is used by 16-bit modem cards to indicate a ring detection.
BVD2(SPKR)	137	J15	71	W9	I	Battery voltage detect 2. BVD2 is generated by 16-bit memory PC Cards that include batteries. BVD2 is used with BVD1 as an indication of the condition of the batteries on a memory PC Card. Both BVD1 and BVD2 are high when the battery is good. When BVD2 is low and BVD1 is high, the battery is weak and should be replaced. When BVD1 is low, the battery is no longer serviceable and the data in the memory PC Card is lost. See Section 5.6, ExCA Card Status-Change-Interrupt Configuration Register, for enable bits. Speaker. SPKR is an optional binary audio signal available only when the card and socket have been configured for the 16-bit I/O interface. The audio signals from cards A and B are combined by the PCI1420 and are output on SPKROUT. DMA request. BVD2 can be used as the DMA request signal during DMA operations to a 16-bit PC Card that supports DMA. The PC Card asserts BVD2 to indicate a request for a DMA operation.
CD1 CD2	82 140	V11 H17	16 74	H3 R9	I	Card detect 1 and Card detect 2. CD1 and CD2 are internally connected to ground on the PC Card. When a PC Card is inserted into a socket, CD1 and CD2 are pulled low.
CE1 CE2	94 97	P13 R13	28 30	K6 L2	O	Card enable 1 and card enable 2. CE1 and CE2 enable even- and odd-numbered address bytes. CE1 enables even-numbered address bytes, and CE2 enables odd-numbered address bytes.
INPACK	127	L14	61	R7	I	Input acknowledge. INPACK is asserted by the PC Card when it can respond to an I/O read cycle at the current address. DMA request. INPACK can be used as the DMA request signal during DMA operations from a 16-bit PC Card that supports DMA. If it is used as a strobe, then the PC Card asserts this signal to indicate a request for a DMA operation.

5. Pin Descriptions of Major Components

5.4 PC Card Interface controller

16-Bit PC Card Interface Control (Slots A and B)

TERMINAL NAME	TERMINAL NO. SLOT A† PDV	TERMINAL NO. SLOT A† GHK	TERMINAL NO. SLOT B‡ PDV	TERMINAL NO. SLOT B‡ GHK	I/O	DESCRIPTION
IORD	99	W15	33	L5	O	I/O read. IORD is asserted by the PCI1420 to enable 16-bit I/O PC Card data output during host I/O read cycles. DMA write. IORD is used as the DMA write strobe during DMA operations from a 16-bit PC Card that supports DMA. The PCI1420 asserts IORD during DMA transfers from the PC Card to host memory.
IOWR	101	V15	35	M2	O	I/O write. IOWR is driven low by the PCI1420 to strobe write data into 16-bit I/O PC Cards during host I/O write cycles. DMA read. IOWR is used as the DMA write strobe during DMA operations from a 16-bit PC Card that supports DMA. The PCI1420 asserts IOWR during transfers from host memory to the PC Card.

† Terminal name for slot A is preceded with A_. For example, the full name for terminals 127 and L14 are A_INPACK.

‡ Terminal name for slot B is preceded with B_. For example, the full name for terminals 61 and R7 are B_INPACK.

TERMINAL NAME	TERMINAL NO. SLOT A† PDV	TERMINAL NO. SLOT A† GHK	TERMINAL NO. SLOT B‡ PDV	TERMINAL NO. SLOT B‡ GHK	I/O	DESCRIPTION
OE	98	U14	32	L6	O	Output enable. OE is driven low by the PCI1420 to enable 16-bit memory PC Card data output during host memory read cycles. DMA terminal count. OE is used as terminal count (TC) during DMA operations to a 16-bit PC Card that supports DMA. The PCI1420 asserts OE to indicate TC for a DMA write operation.

TERMINAL NAME	TERMINAL NO. SLOT A† PDV	TERMINAL NO. SLOT A† GHK	TERMINAL NO. SLOT B‡ PDV	TERMINAL NO. SLOT B‡ GHK	I/O	DESCRIPTION
READY (IREQ)	135	J17	69	V8	I	Ready. The ready function is provided by READY when the 16-bit PC Card and the host socket are configured for the memory-only interface. READY is driven low by the 16-bit memory PC Cards to indicate that the memory card circuits are busy processing a previous write command. READY is driven high when the 16-bit memory PC Card is ready to accept a new data transfer command. Interrupt request. IREQ is asserted by a 16-bit I/O PC Card to indicate to the host that a device on the 16-bit I /O PC Card requires service by the host software. IREQ is high (deasserted) when no interrupt is requested.
REG	130	K17	63	P8	O	Attribute memory select. REG remains high for all common memory accesses. When REG is asserted, access is limited to attribute memory (OE or WE active) and to the I/O space (IORD or IOWR active). Attribute memory is a separately accessed section of card memory and is generally used to record card capacity and other configuration and attribute information. DMA acknowledge. REG is used as a DMA acknowledge (DACK) during DMA operations to a 16-bit PC Card that supports DMA. The PCI1420 asserts REG to indicate a DMA operation. REG is used in conjunction with the DMA read (IOWR) or DMA write (IORD) strobes to transfer data.
RESET	124	L18	58	W5	O	PC Card reset. RESET forces a hard reset to a 16-bit PC Card.
WAIT	136	J14	70	W8	I	Bus cycle wait. WAIT is driven by a 16-bit PC Card to extend the completion of the memory or I/O cycle in progress.

5. Pin Descriptions of Major Components

5.4 PC Card Interface controller

16-Bit PC Card Interface Control (Slots A and B)

TERMINAL					I/O	DESCRIPTION
NAME	NO.					
	SLOT A†		SLOT B‡			
	PDV	GHK	PDV	GHK		
WE	110	R19	46	P3	O	Write enable. WE is used to strobe memory write data into 16-bit memory PC Cards. WE is also used for memory PC Cards that employ programmable memory technologies. DMA terminal count. WE is used as TC during DMA operations to a 16-bit PC Card that supports DMA. The PCI1420 asserts WE to indicate TC for a DMA read operation.
WP(IOIS16)	139	H18	73	U9	I	Write protect. WP applies to 16-bit memory PC Cards. WP reflects the status of the write-protect switch on 16-bit memory PC Cards. For 16-bit I/O cards, WP is used for the 16-bit port (IOIS16) function. I/O is 16 bits. IOIS16 applies to 16-bit I/O PC Cards. IOIS16 is asserted by the 16-bit PC Card when the address on the bus corresponds to an address to which the 16-bit PC Card responds, and the I/O port that is addressed is capable of 16-bit accesses. DMA request. WP can be used as the DMA request signal during DMA operations to a 16-bit PC Card that supports DMA. If used, then the PC Card asserts WP to indicate a request for a DMA operation.
VS1 VS2	134 122	J18 M19	68 56	U8 P7	I/O	Voltage sense 1 and voltage sense 2. VS1 and VS2, when used in conjunction with each other, determine the operating voltage of the PC Card.

† Terminal name for slot A is preceded with A_. For example, the full name for terminals 110 and R19 are A_WE.

‡ Terminal name for slot B is preceded with B_. For example, the full name for terminals 46 and P3 are B_WE.

CardBus PC Card Interface System (Slots A and B)

TERMINAL					I/O	DESCRIPTION
NAME	NO.					
	SLOT A†		SLOT B‡			
	PDV	GHK	PDV	GHK		
CCLK	112	P18	48	P6	O	CardBus clock. CCLK provides synchronous timing for all transactions on the CardBus interface. All signals except CRST, CCLKRUN, CINT, CSTSCHG, CAUDIO, CCD2, CCD1, CVS2, and CVS1 are sampled on the rising edge of CCLK, and all timing parameters are defined with the rising edge of this signal. CCLK operates at the PCI bus clock frequency, but it can be stopped in the low state or slowed down for power savings.
CCLKRUN	139	H18	73	U9	O	CardBus clock run. CCLKRUN is used by a CardBus PC Card to request an increase in the CCLK frequency, and by the PCI1420 to indicate that the CCLK frequency is going to be decreased.
CRST	124	L18	58	W5	I/O	CardBus reset. CRST brings CardBus PC Card-specific registers, sequencers, and signals to a known state. When CRST is asserted, all CardBus PC Card signals are placed in a high-impedance state, and the PCI1420 drives these signals to a valid logic level. Assertion can be asynchronous to CCLK, but deassertion must be synchronous to CCLK.

† Terminal name for slot A is preceded with A_. For example, the full name for terminals 112 and P18 are A_CCLK.

‡ Terminal name for slot B is preceded with B_. For example, the full name for terminals 48 and P6 are B_CCLK.

5. Pin Descriptions of Major Components

5.4 PC Card Interface controller

CardBus PC Card Address and Data (Slots A and B)

NAME	TERMINAL NO. SLOT A† PDV	SLOT A† GHK	SLOT B‡ PDV	SLOT B‡ GHK	I/O	DESCRIPTION
CAD31	147	F19	81	W11	I/O	CardBus address and data. These signals make up the multiplexed CardBus address and data bus on the CardBus interface. During the address phase of a CardBus cycle, CAD31–CAD0 contain a 32-bit address. During the data phase of a CardBus cycle, CAD31–CAD0 contain data. CAD31 is the most significant bit.
CAD30	145	G17	79	R10		
CAD29	144	G18	78	U10		
CAD28	142	H15	77	V10		
CAD27	141	H14	76	W10		
CAD26	133	J19	67	R8		
CAD25	132	K14	66	W7		
CAD24	131	K15	65	V7		
CAD23	128	K19	62	W6		
CAD22	126	L15	60	V6		
CAD21	125	L17	59	U6		
CAD20	123	L19	57	V5		
CAD19	121	M18	55	R6		
CAD18	119	M15	54	U5		
CAD17	118	N19	53	W4		
CAD16	103	U15	37	M6		
CAD15	101	V15	35	M2		
CAD14	102	R14	36	M3		
CAD13	99	W15	33	L5		
CAD12	100	P14	34	M1		
CAD11	98	U14	32	L6		
CAD10	97	R13	30	L2		
CAD9	95	W14	29	L1		
CAD8	93	U13	27	K5		
CAD7	92	V13	26	K3		
CAD6	89	P12	23	J6		
CAD5	90	R12	24	K1		
CAD4	87	V12	20	J2		
CAD3	88	U12	21	J3		
CAD2	84	P11	18	H1		
CAD1	85	R11	19	J1		
CAD0	83	U11	17	H2		

NAME	TERMINAL NO. SLOT A† PDV	SLOT A† GHK	SLOT B‡ PDV	SLOT B‡ GHK	I/O	DESCRIPTION
CC/BE3	130	K17	63	P8	I/O	CardBus bus commands and byte enables. CC/BE3–CC/BE0 are multiplexed on the same CardBus terminals. During the address phase of a CardBus cycle, CC/BE3–CC/BE0 define the bus command. During the data phase, this 4-bit bus is used as byte enables. The byte enables determine which byte paths of the full 32-bit data bus carry meaningful data. CC/BE0 applies to byte 0 (CAD7–CAD0), CC/BE1 applies to byte 1 (CAD15–CAD8), CC/BE2 applies to byte 2 (CAD23–CAD8), and CC/BE3 applies to byte 3 (CAD31–CAD24).
CC/BE2	117	N18	52	T1		
CC/BE1	104	W16	39	N1		
CC/BE0	94	P13	28	K6		
CPAR	106	R17	41	N3	I/O	CardBus parity. In all CardBus read and write cycles, the PCI1420 calculates even parity across the CAD and CC/BE buses. As an initiator during CardBus cycles, the PCI1420 outputs CPAR with a one-CCLK delay. As a target during CardBus cycles, the calculated parity is compared to the initiator's parity indicator; a compare error results in a parity error assertion.

† Terminal name for slot A is preceded with A_. For example, the full name for terminals 106 and R17 are A_CPAR.

‡ Terminal name for slot B is preceded with B_. For example, the full name for terminals 41 and N3 are B_CPAR.

5. Pin Descriptions of Major Components

5.4 PC Card Interface controller

CardBus PC Card Interface Control (Slots A and B)

NAME	TERMINAL NO. SLOT A† PDV	SLOT A† GHK	SLOT B‡ PDV	SLOT B‡ GHK	I/O	DESCRIPTION
CAUDIO	137	J15	71	W9	I	CardBus audio. CAUDIO is a digital input signal from a PC Card to the system speaker. The PCI1420 supports the binary audio mode and outputs a binary signal from the card to SPKROUT.
CBLOCK	107	P15	42	N6	I/O	CardBus lock. CBLOCK is used to gain exclusive access to a target.
CCD1	82	V11	16	H3	I	CardBus detect 1 and CardBus detect 2. CCD1 and CCD2 are used in conjunction with CVS1 and CVS2 to identify card insertion and interrogate cards to determine the CCD2 140 H17 74 R9 I with CVS1 and CVS2 to identify card insertion and interrogate cards to determine the operating voltage and card type.
CDEVSEL	111	P17	47	R1	I/O	CardBus device select. The PCI1420 asserts CDEVSEL to claim a CardBus cycle as the target device. As a CardBus initiator on the bus, the PCI1420 monitors CDEVSEL until a target responds. If no target responds before timeout occurs, then the PCI1420 terminates the cycle with an initiator abort.
CFRAME	116	N17	51	R3	I/O	CardBus cycle frame. CFRAME is driven by the initiator of a CardBus bus cycle. CFRAME is asserted to indicate that a bus transaction is beginning, and data transfers continue while this signal is asserted. When CFRAME is deasserted, the CardBus bus transaction is in the final data phase.
CGNT	110	R19	46	P3	I	CardBus bus grant. CGNT is driven by the PCI1420 to grant a CardBus PC Card access to the CardBus bus after the current data transaction has been completed.
CINT	135	J17	69	V8	I	CardBus interrupt. CINT is asserted low by a CardBus PC Card to request interrupt servicing from the host.

NAME	NO. SLOT A† PDV	SLOT A† GHK	SLOT B‡ PDV	SLOT B‡ GHK	I/O	DESCRIPTION
CIRDY	115	M14	50	P5	I/O	CardBus initiator ready. CIRDY indicates the CardBus initiator's ability to complete the current data phase of the transaction. A data phase is completed on a rising edge of CCLK when both CIRDY and CTRDY are asserted. Until CIRDY and CTRDY are both sampled asserted, wait states are inserted.
CPERR	108	N14	43	P1	I/O	CardBus parity error. CPERR reports parity errors during CardBus transactions, except during special cycles. It is driven low by a target two clocks following that data when a parity error is detected.
CREQ	127	L14	61	R7	I	CardBus request. CREQ indicates to the arbiter that the CardBus PC Card desires use of the CardBus bus as an initiator.
CSERR	136	J14	70	W8	I	CardBus system error. CSERR reports address parity errors and other system errors that could lead to catastrophic results. CSERR is driven by the card synchronous to CCLK, but deasserted by a weak pullup, and may take several CCLK periods. The PCI1420 can report CSERR to the system by assertion of SERR on the PCI interface.
CSTOP	109	R18	45	N5	I/O	CardBus stop. CSTOP is driven by a CardBus target to request the initiator to stop the current CardBus transaction. CSTOP is used for target disconnects, and is commonly asserted by target devices that do not support burst data transfers.
CSTSCHG	138	H19	72	V9	I	CardBus status change. CSTSCHG alerts the system to a change in the card's status, and is used as a wake-up mechanism.
CTRDY	114	P19	49	R2	I/O	CardBus target ready. CTRDY indicates the CardBus target's ability to complete the current data phase of the transaction. A data phase is completed on a rising edge of CCLK, when both CIRDY and CTRDY are asserted; until this time, wait states are inserted.

5. Pin Descriptions of Major Components

5.4 PC Card Interface controller

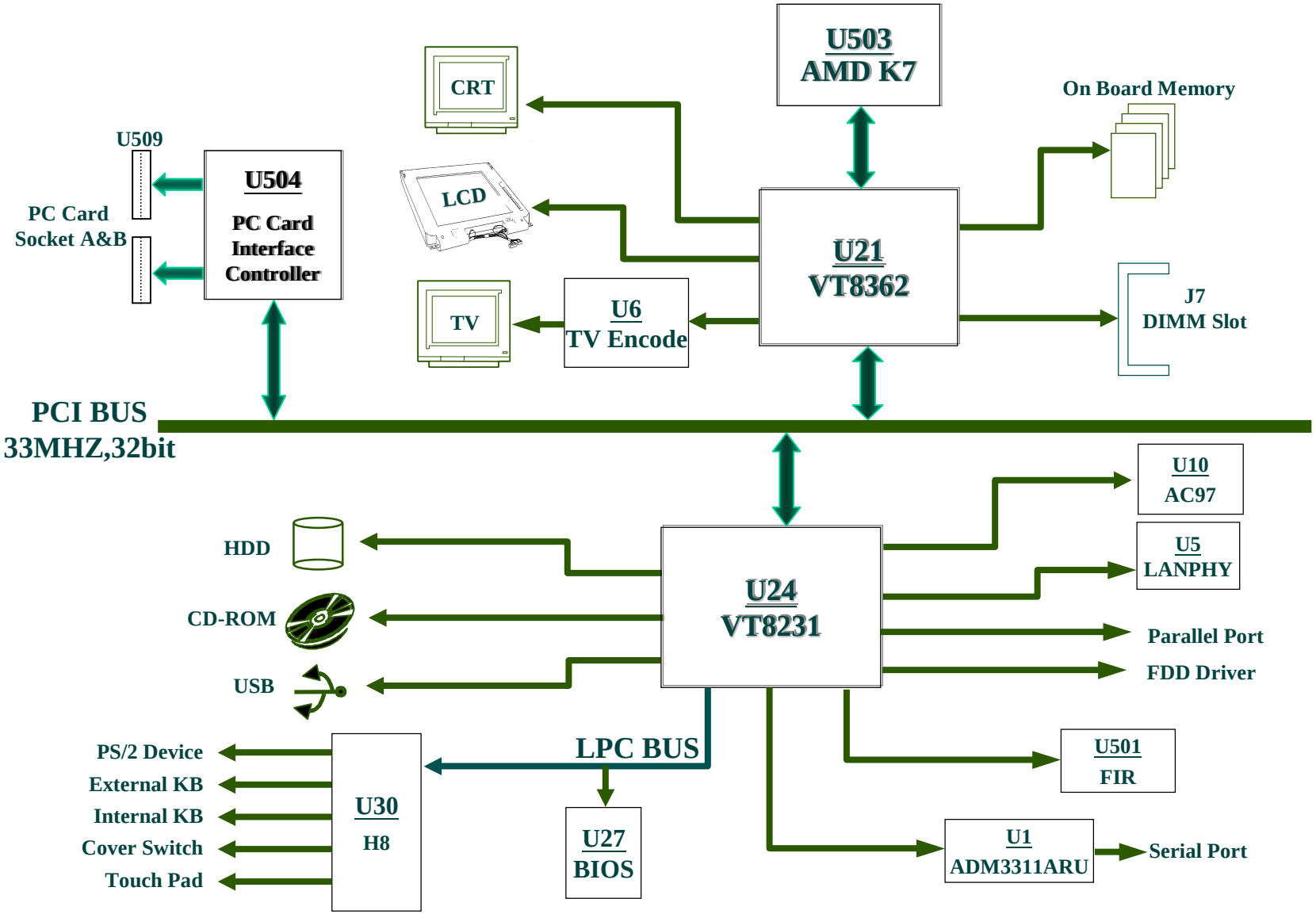
CardBus PC Card Interface Control (Slots A and B)

TERMINAL NO.					I/O	DESCRIPTION
NAME	SLOT A†		SLOT B‡			
	PDV	GHK	PDV	GHK		
CVS1 CVS2	134 122	J18 M19	68 56	U8 P7	I/O	CardBus voltage sense 1 and CardBus voltage sense 2. CVS1 and CVS2 are used in conjunction with CCD1 and CCD2 to identify card insertion and interrogate cards CVS2 122 M19 56 P7 I/O in conjunction with CCD1 and CCD2 to identify card insertion and interrogate cards to determine the operating voltage and card type.

† Terminal name for slot A is preceded with A_. For example, the full name for terminals 137 and J15 are A_CAUDIO.

‡ Terminal name for slot B is preceded with B_. For example, the full name for terminals 71 and W9 are B_CAUDIO.

6. System Block Diagram



7. Maintenance Diagnostics

7.1 Introduction

Each time the computer is turned on, the system BIOS runs a series of internal checks on the hardware. This power-on self test (POST) allows the computer to detect problems as early as the power-on stage. Error messages of post can alert you to the problems of your computer.

If an error is detected during these tests, you will see an error message displayed on the screen. If the error occurs before the display is initialized,then the screen cannot display the error message. Error codes or system beeps are used to identify a post error that occurs when the screen is not available.

The value for the diagnostic port (378H) is written at the beginning of the test. Therefore, if the test failed, the user can determine where the problem occurred by reading the last value written to port 378H by the 378H port debug board plug at PIO PORT.

7. Maintenance Diagnostics

7.2 Error Codes : Following is a list of error codes in sequent display on the PIO debug board.System Soft BIOS:

Code	Description
00	System Initialization
01	Disable A20 through A20
02	Initialize Chipset
03	Test RAM
04	Move BL into the RAM
05	Execution in RAM
06	User Flash Check
07	Shadow system BIOS
08	Check System BIOS ROM
09	Proceed with Normal Boot
0A	Proceed with Crisis Boot
0B	Initialize Clock Sythesizer
0F	Fatal Error
10	Some Type of Long Reset
11	Turn Off Fasta20 for Post
12	Signal Power On Reset
13	Initialize the Chipset
14	Search For ISA Bus VGA Adapter
15	Reset Counter/Timer 1
16	User Register Config Through CMOS
17	Size Memory
18	Dispatch to RAM Test
19	Checksum the ROM
1A	Reset PIC's

Code	Description
1B	Initialize Video Adapter
1C	Initialize Video(6845 Regs)
1D	Initialize Color Adapter
1E	Initialize Monochrome Adapter
1F	Test 8237A Page Registers
20	Test Keyboard
21	Test Keyboard Controller
22	Check If CMOS Ram Valid
23	Test Battery Fail & CMOS X-SUM
24	Test DMA Controller
25	Initialize 8237A Controller
26	Initialize Int Vectors
27	RAM Quick Sizing
28	Protected mode entered safely
29	RAM Test Completed
2A	Protected mode exit successful
2B	Setup Shadow
2C	Going to Initialize Video
2D	Search For Monochrome Adapter
2E	Search For Color Adapter
2F	Signal Messages Displayed
30	Special Into of Keyboard Controller
31	Test If Keyboard Present
32	Test Keyboard Interrupt

7. Maintenance Diagnostics

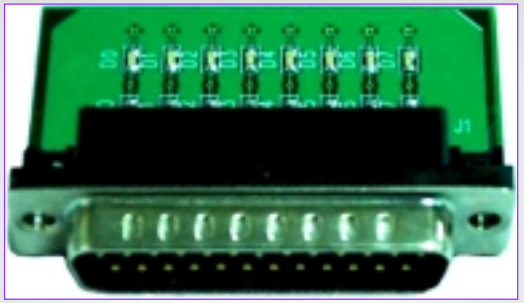
7.2 Error Codes : Following is a list of error codes in sequent display on the PIO debug board.System Soft BIOS:

Code	Description
33	Test Keyboard Command Byte
34	TEST, Blank and Count All RAM
35	Protected mode entered safely
36	RAM Test Complete
37	Protected mode exit successful
38	Update Output Port
39	Setup Cache Controller
3A	Test If 18.2Hz Periodic Working
3B	Test for RTC ticking
3C	Initialize the Hardware Vectors
3D	Search and Init the Mouse
3E	Update NumLock Status
3F	Special init of COMM and LPT ports
40	Configure the COMM and LPT ports
41	Initialize the floppies
42	Initialize the Hard Disk
43	Initialize option ROMs
44	OEM’s init of power management
45	Update NumLock Status
46	Test For Coprocessor Installed
47	OEM Function Before Boot
48	Dispatch To Op.Sys.Boot
49	Jump Into Bootstrap Code
99	Resume SMRAM not Found

7.3 Debug Card

7.3.1 Diagnostic Tools :

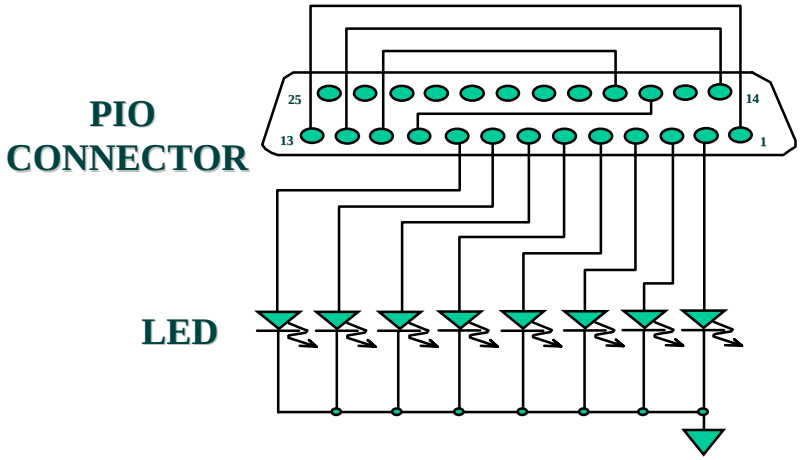
The 378 Port Debug Card, a kind of tool, is designed mainly for Notebook . It can be used to test the process of BIOS POST system. It composed of eight . LED and one PIO CONNECTOR as the below figure shows



P/N:411904800001
DESCRIPTION :PWA;PWA-378PORT DEBUG BD
Note:Order it from MIC/TSSC

7.3 Debug Card

7.3.2 CIRCUIT:

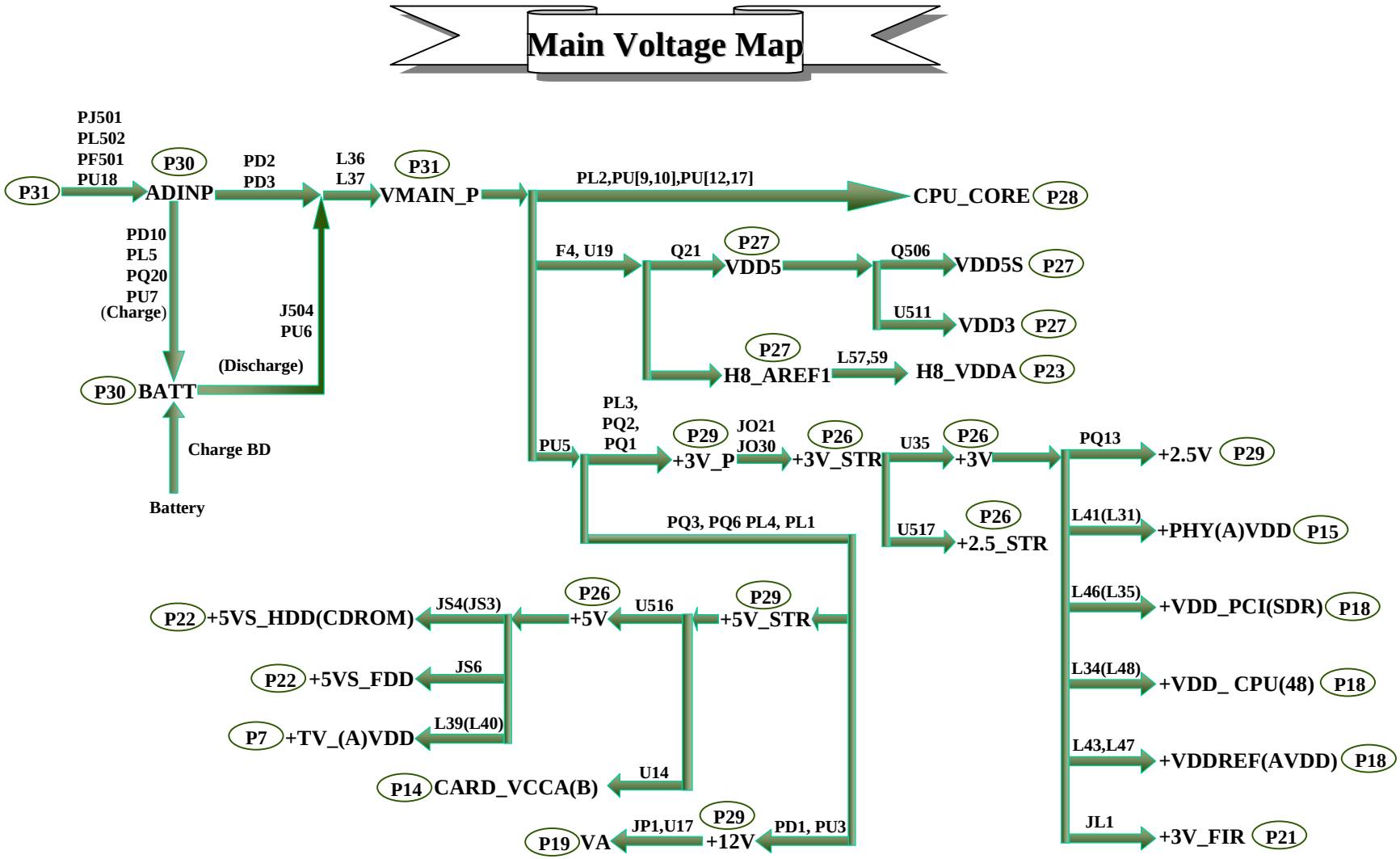


PIN DEFINITION OF PIO PORT					
PIN 1	STB	STROBE SIGNAL	PIN 14	AFD	AUTO LINE FEED
PIN 2-9	D0 - D7	PARALLEL PORT DATA BUS D0 TO D7	PIN15	ERR	ERROR AT PRINTER
PIN10	ACK	ACKNOWLEDGE HANDSHANK	PIN16	INIT	INITIATE OUTPUT
PIN11	BUSY	BUSY SIGNAL	PIN17	SLIN	PRINTER SELECT
PIN12	PE	PAPER END	PIN18-25	SIGNAL GROUND	
PIN13	SLCT	PRINTER SELECTED			

8.Trouble Shooting

8.1 No Power:

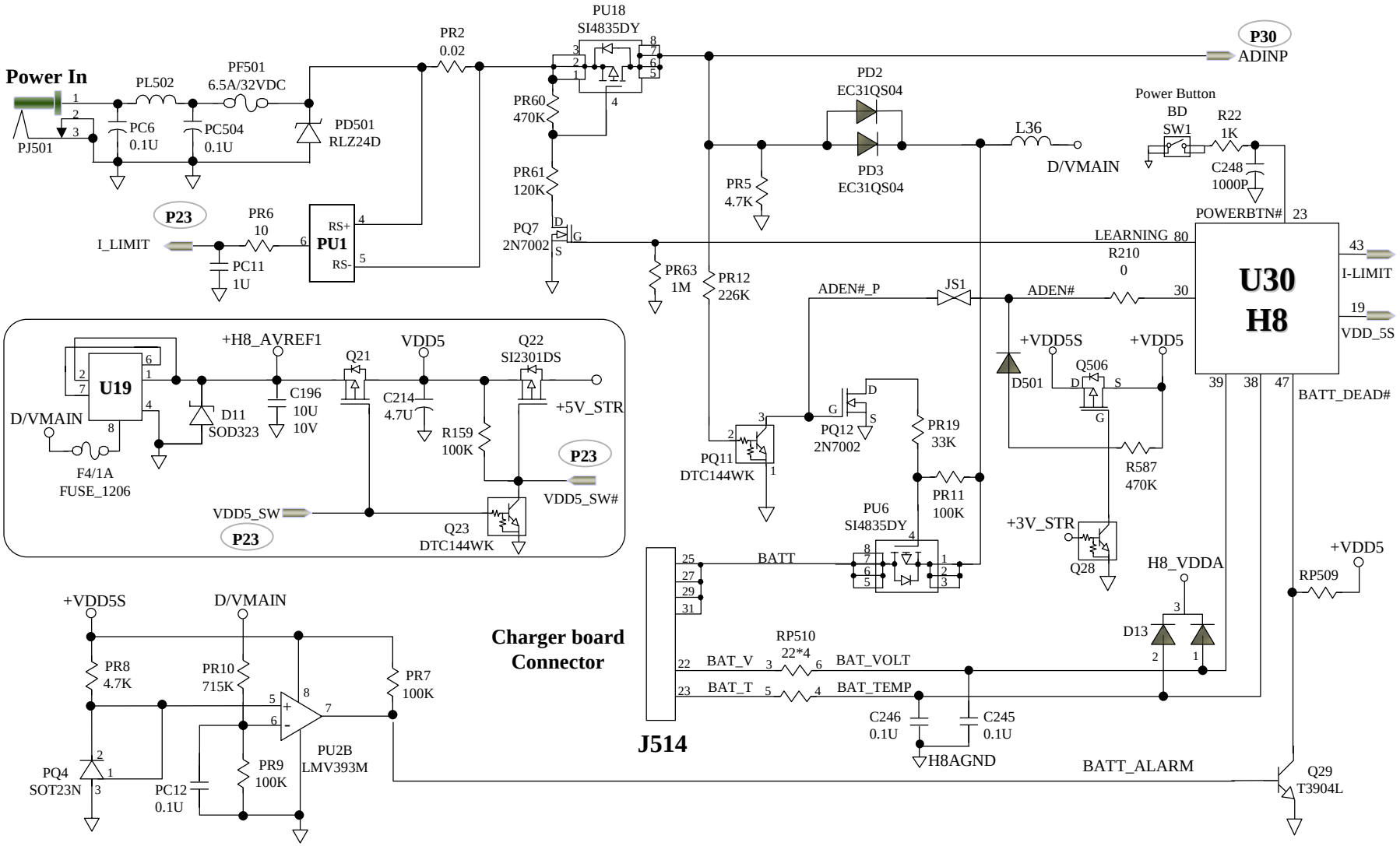
When the power button is pressed, nothing happens ,power indicator does not light up.



7321 N/B Maintenance

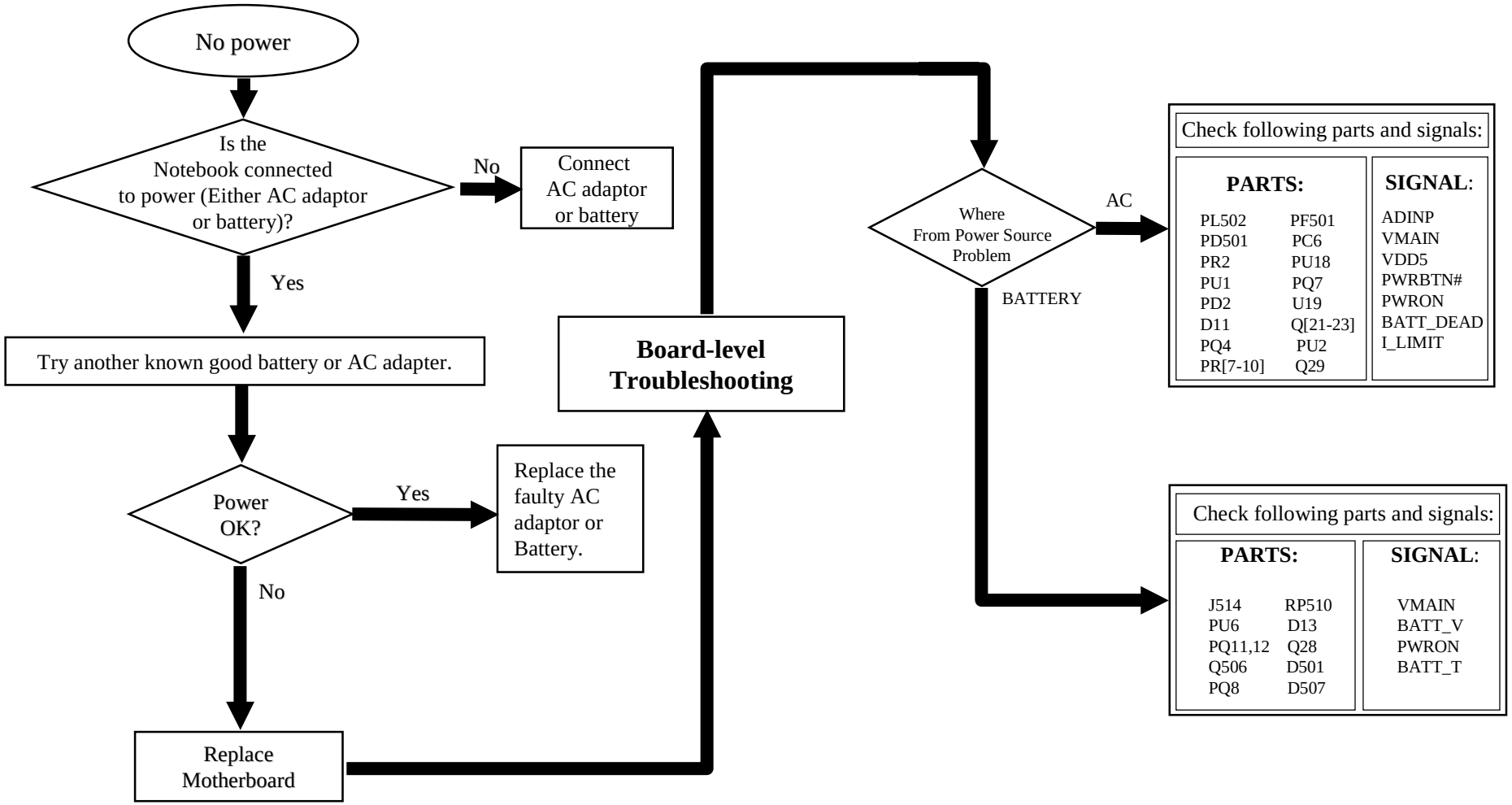
8.1 No Power:

When the power button is pressed, nothing happens ,power indicator does not light up.



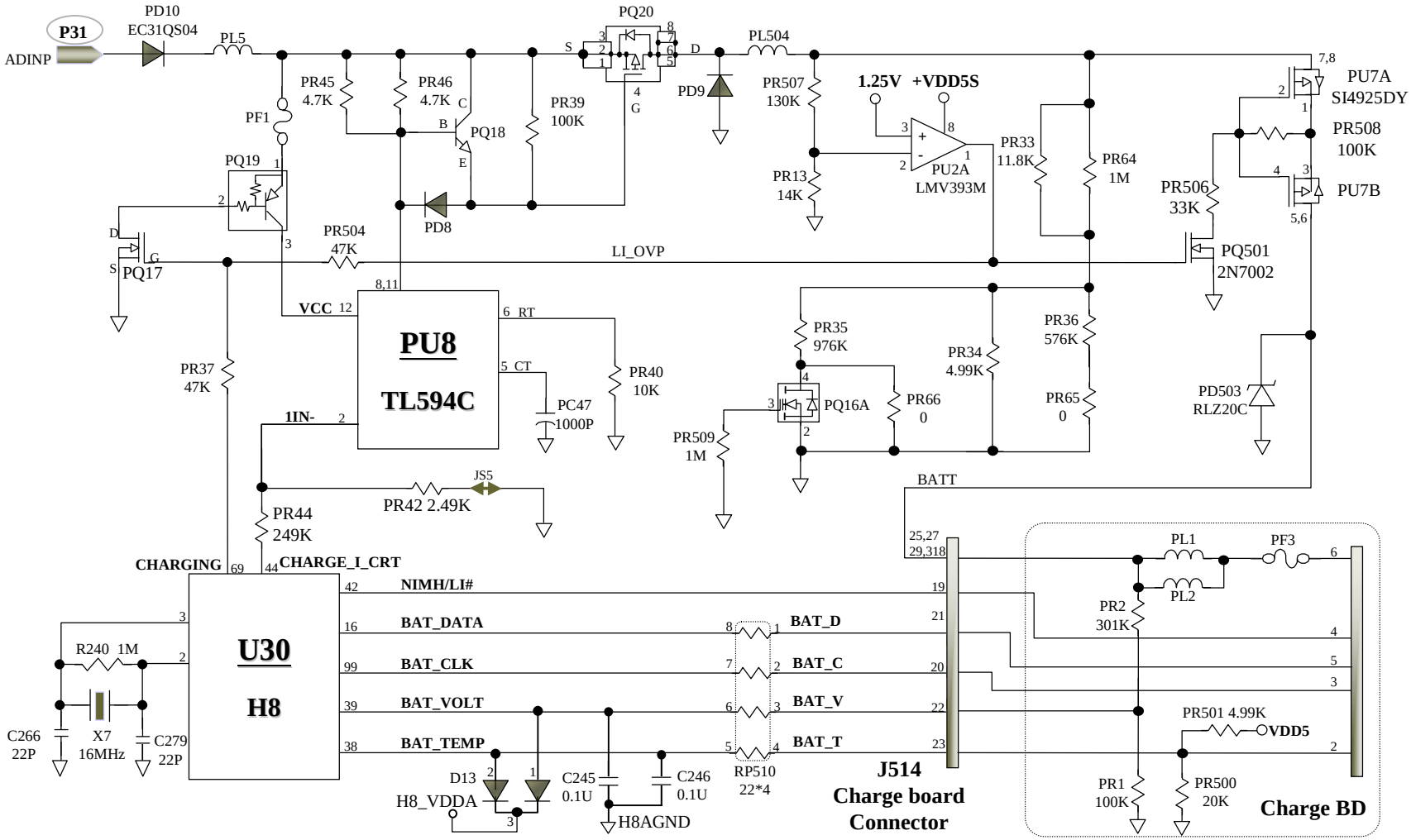
8.1 No Power

When the power button is pressed, nothing happens ,power indicator does not light up.



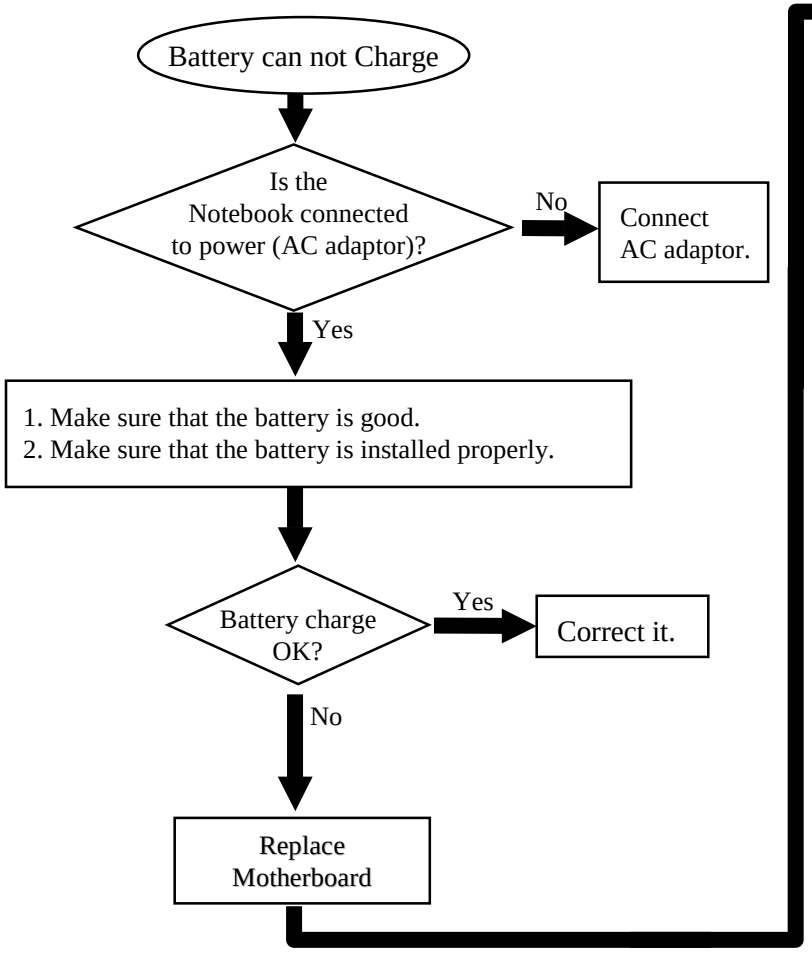
8.2 Battery Can not Be Charged

Symptom:
When the battery is installed but the battery status indicate LED display abnormal.



8.2 Battery Can not Be Charged

Symptom:
When the battery is installed but the battery status indicate LED display abnormal.



Board-level Troubleshooting

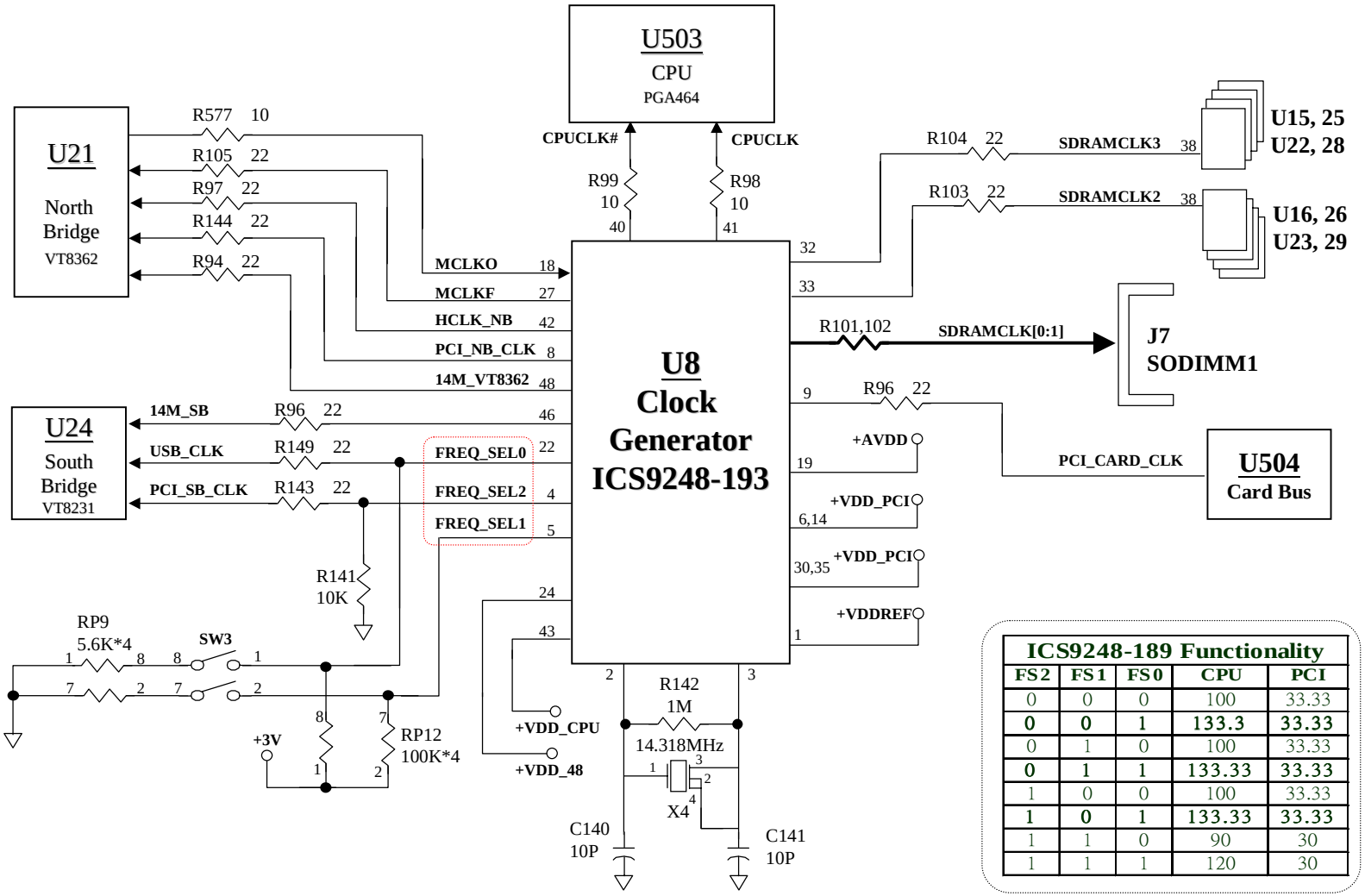
Check the following parts for cold solder or one of the following parts on the **mother-board** may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

PARTS		
PD10	PL5	PF1
PR45	PR46	PQ[17:20]
PD[8:9]	PR39	PL504
PR[506:509]	PU2	PU7
PQ501	PQ16	PD503
PU8	PR[33:37]	PC47
U30	X7	D13
PL[1:2]	PF3	RP510
C266	PR42	Charge BD

SIGNAL	
BAT_VOLT	BAT_V
BAT_TEMP	BAT_C
BAT_CLK	BAT_C
BAT_DATA	BAT_D
SHUTDOWN	NIMH/LI
CHARGE	BATT
LI_OVP	ADINP
VMAIN	VDD5
H8_VDDA	

8.3 No Display

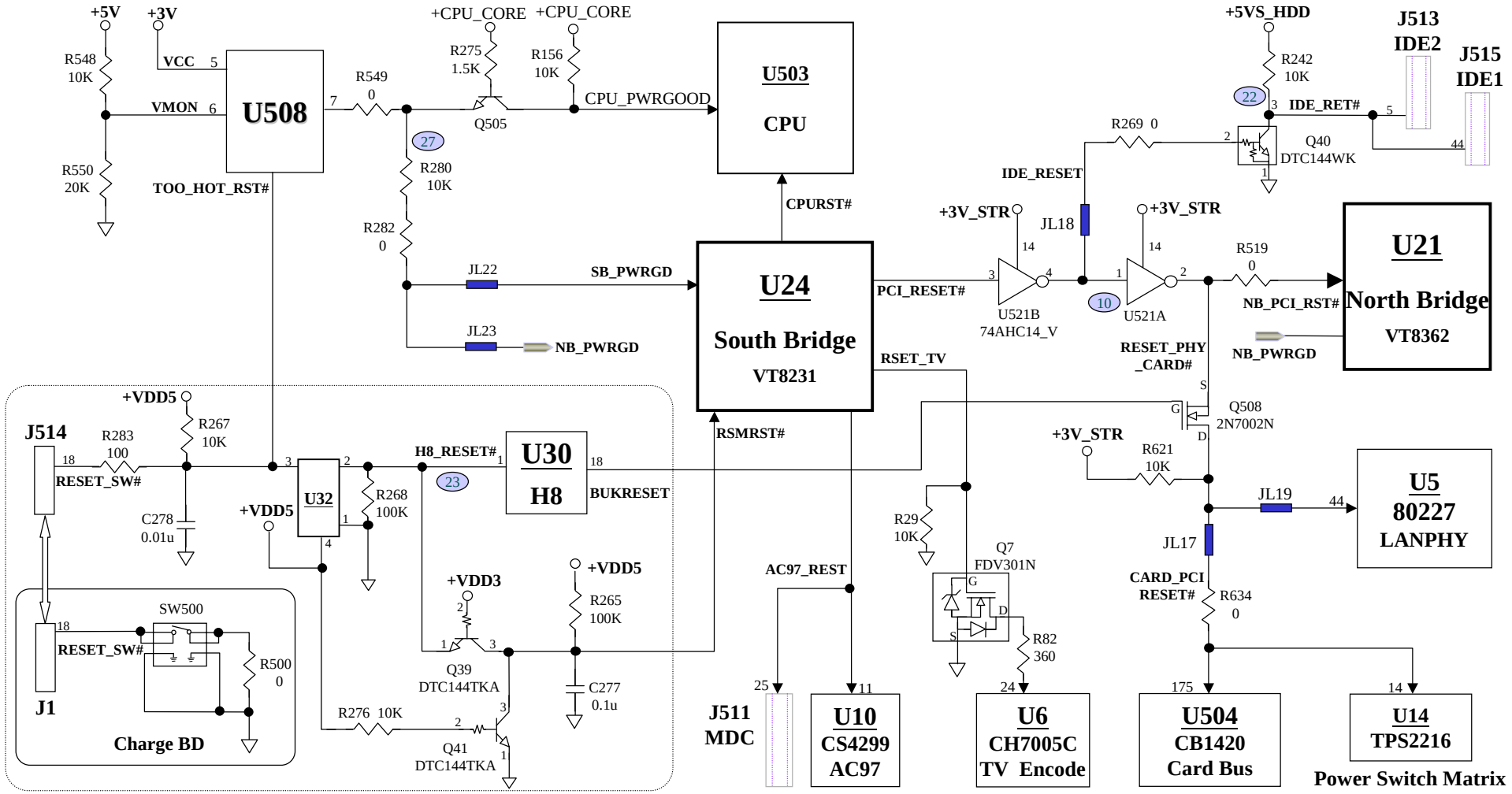
System Clock Checking



ICS9248-189 Functionality				
FS2	FS1	FS0	CPU	PCI
0	0	0	100	33.33
0	0	1	133.3	33.33
0	1	0	100	33.33
0	1	1	133.33	33.33
1	0	0	100	33.33
1	0	1	133.33	33.33
1	1	0	90	30
1	1	1	120	30

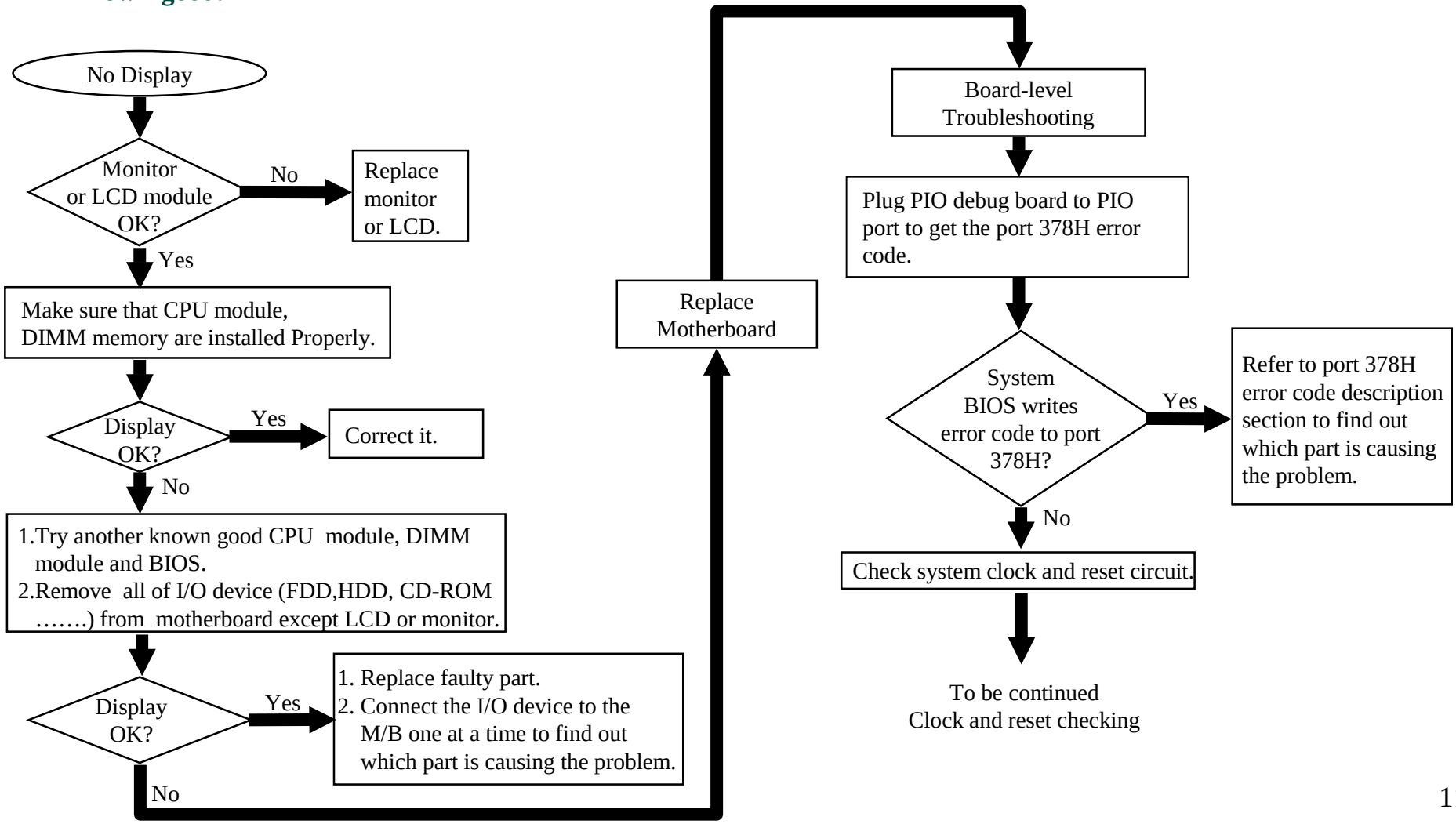
8.3 No Display

Reset Circuit Checking



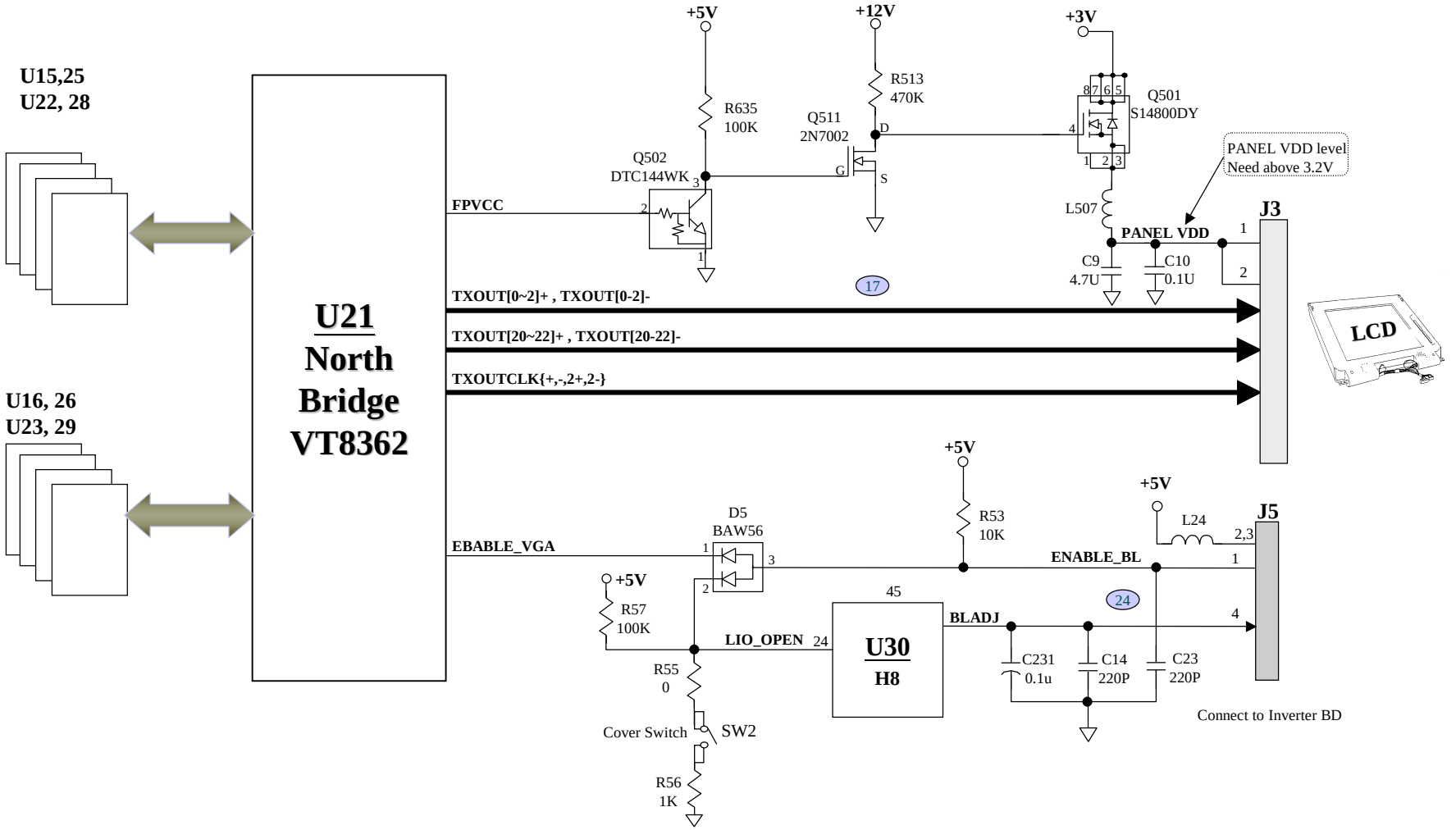
8.3 No Display (System Failure)

Symptom:
There is no display on both LCD and VGA monitor after power on although the LCD and monitor is known-good.



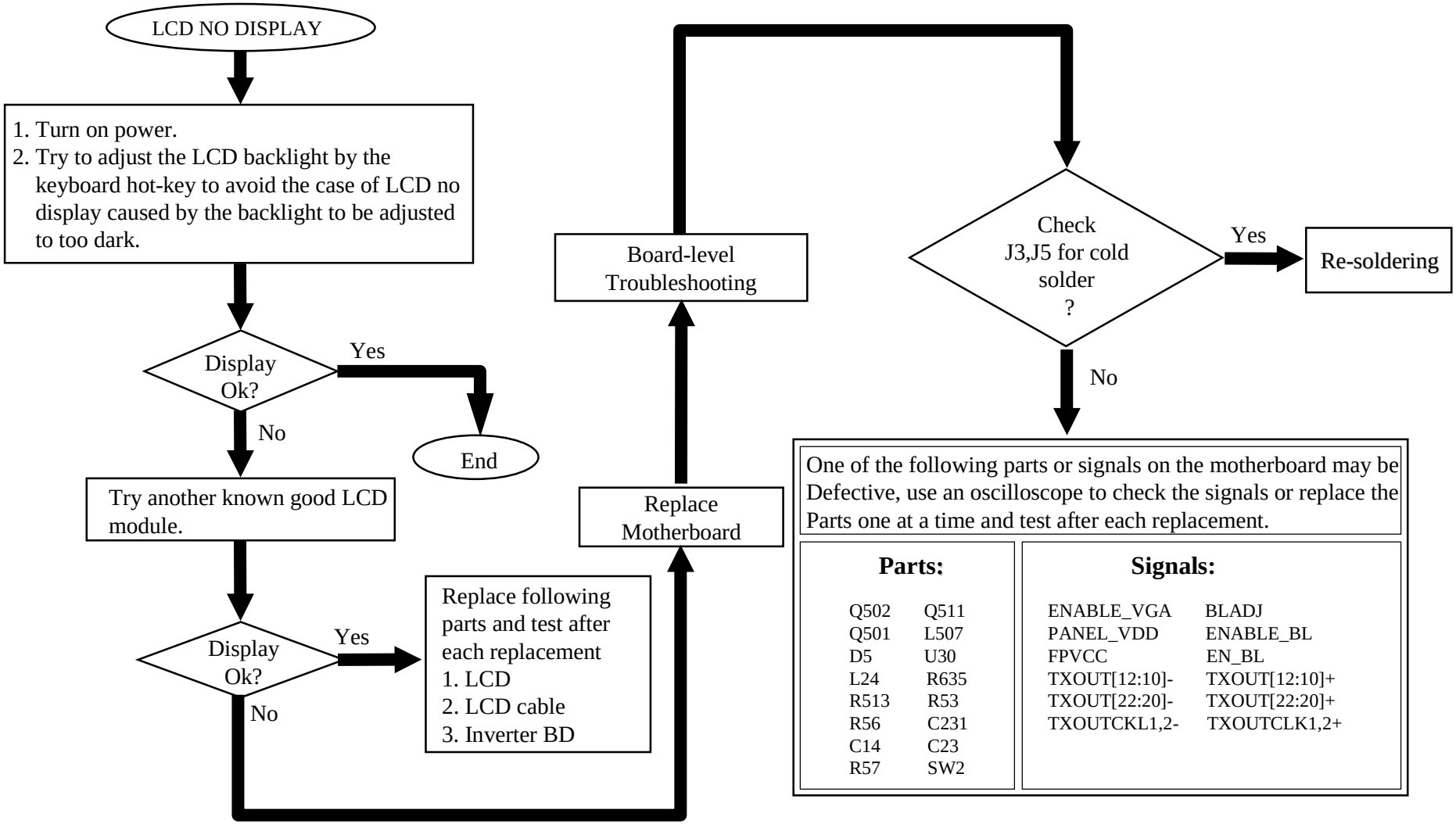
8.4 LCD No Display Or Picture Abnormal

Symptom:
The LCD shows nothing or abnormal picture, but it is ok for external monitor.



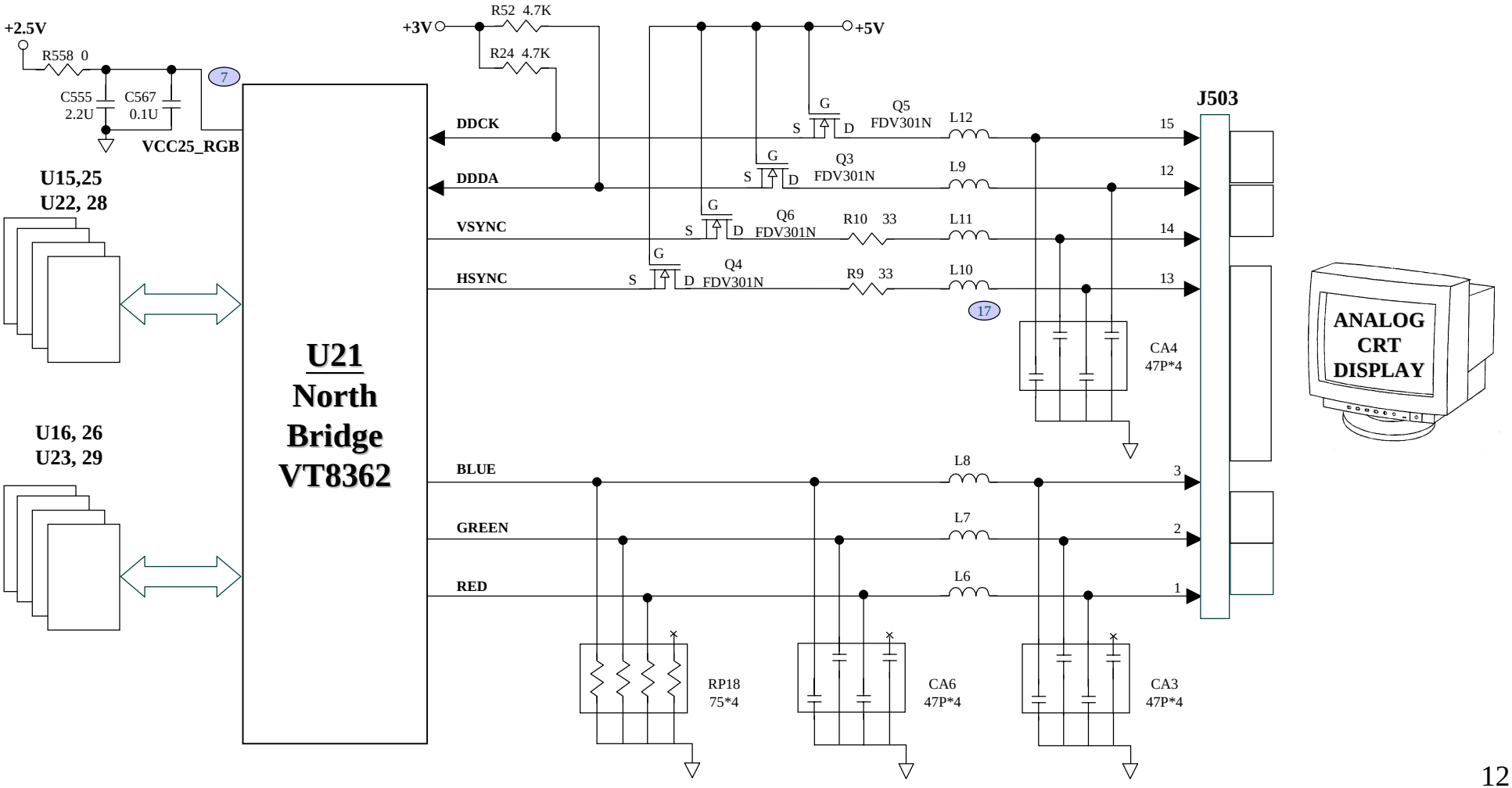
8.4 LCD No Display Or Picture Abnormal

Symptom:
The LCD shows nothing or abnormal picture, but it is ok for external monitor.



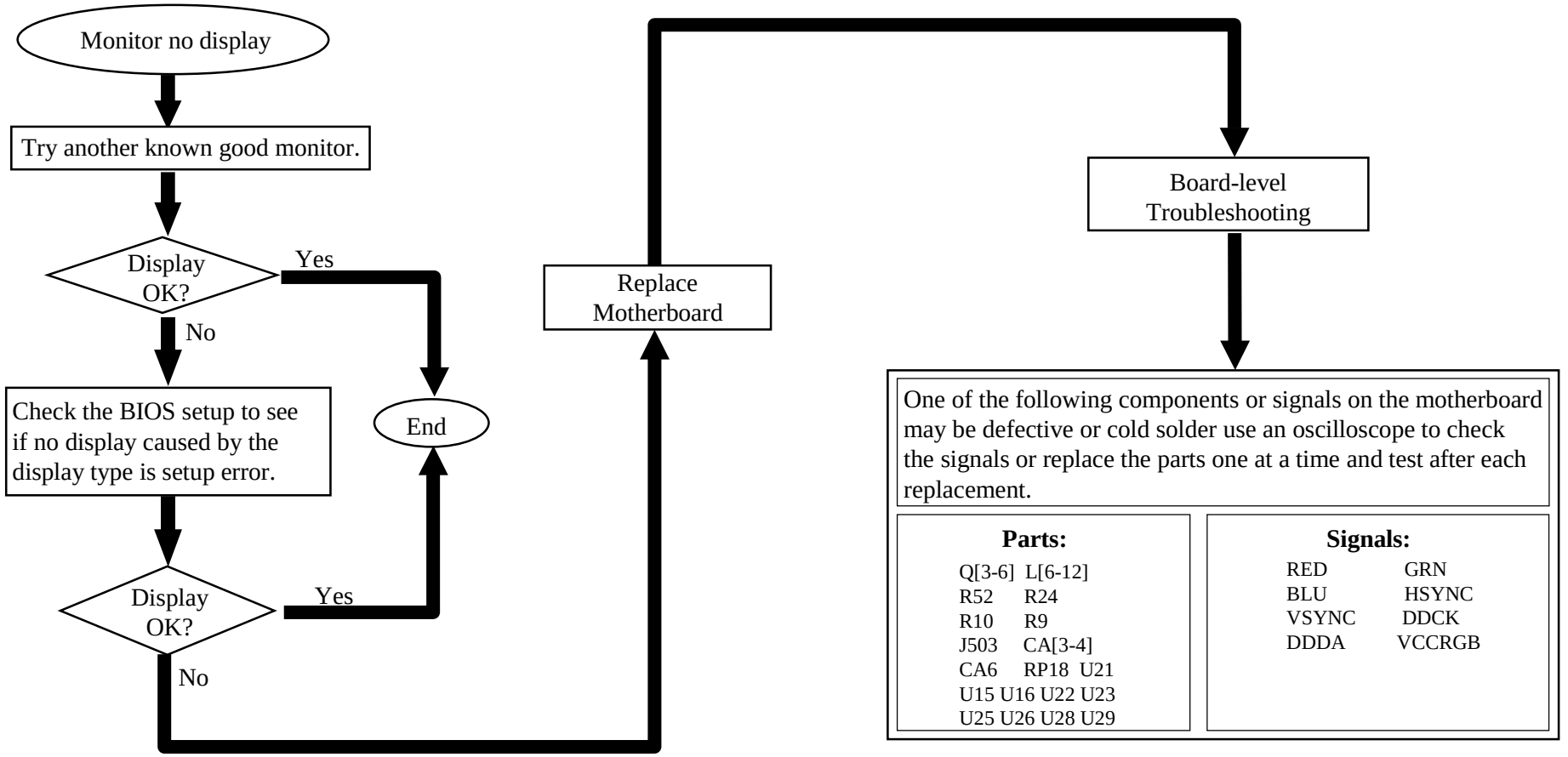
8.5 External Monitor No Display or Color Abnormal

Symptom:
The CRT monitor shows nothing or abnormal color, but it is ok for LCD



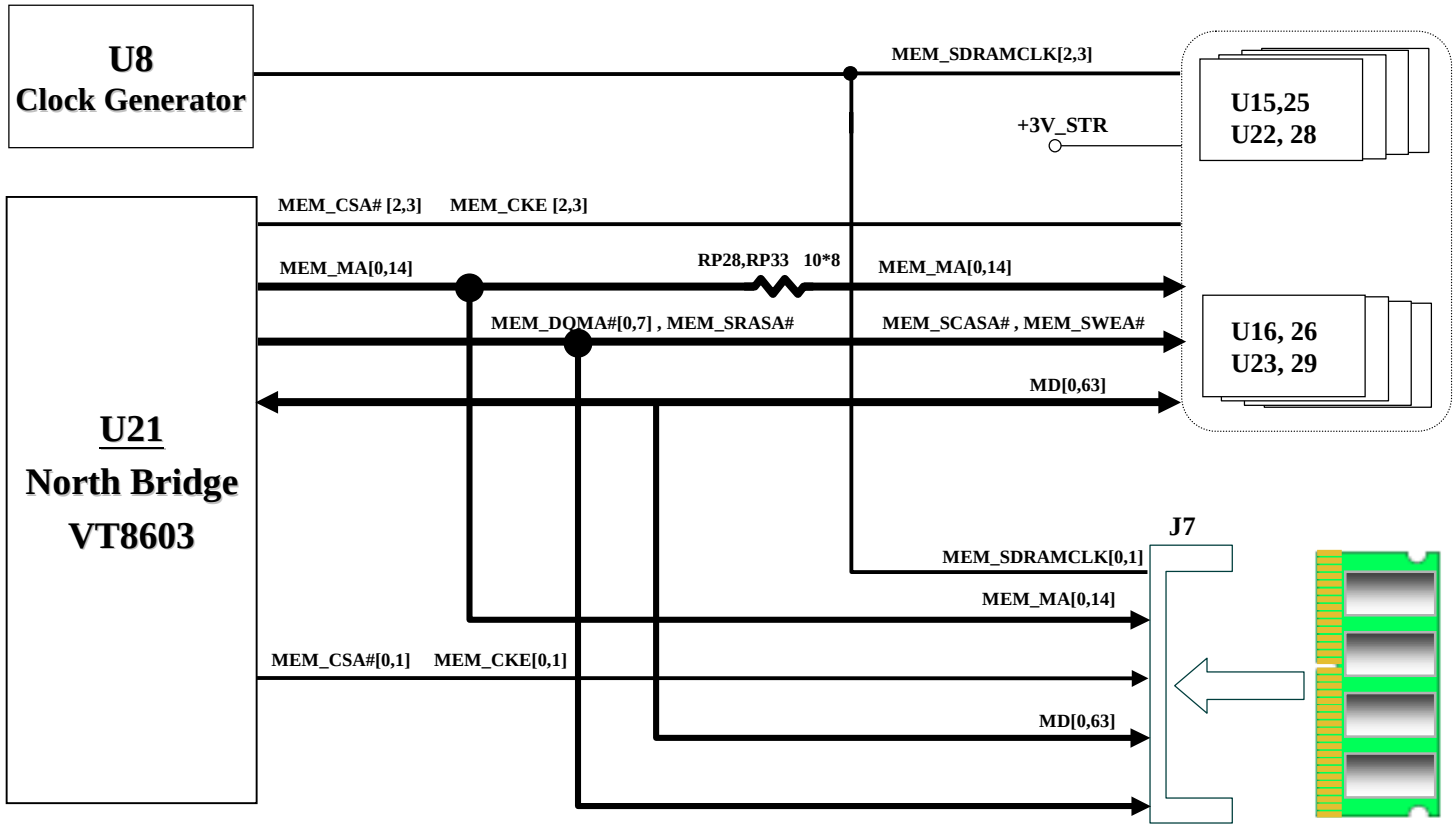
8.5 External Monitor No Display or Color Abnormal

Symptom:
The CRT monitor shows nothing or abnormal color, but it is ok for LCD



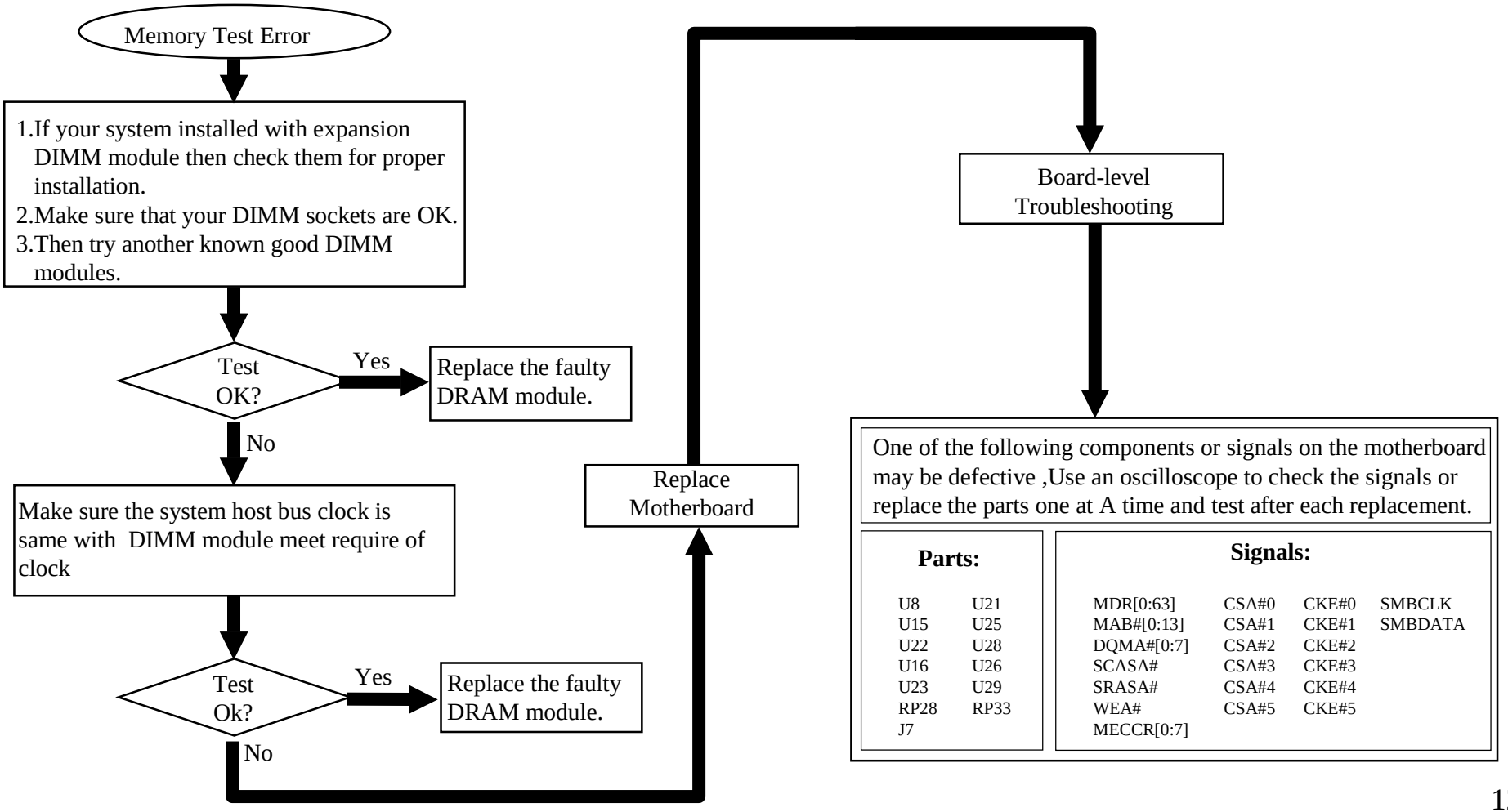
8.6 Memory Test Error

Symptom:
PIO debug board shows the port 378H error code is stopped at 27H,28H or 29H, or error message of memory failure is shown.



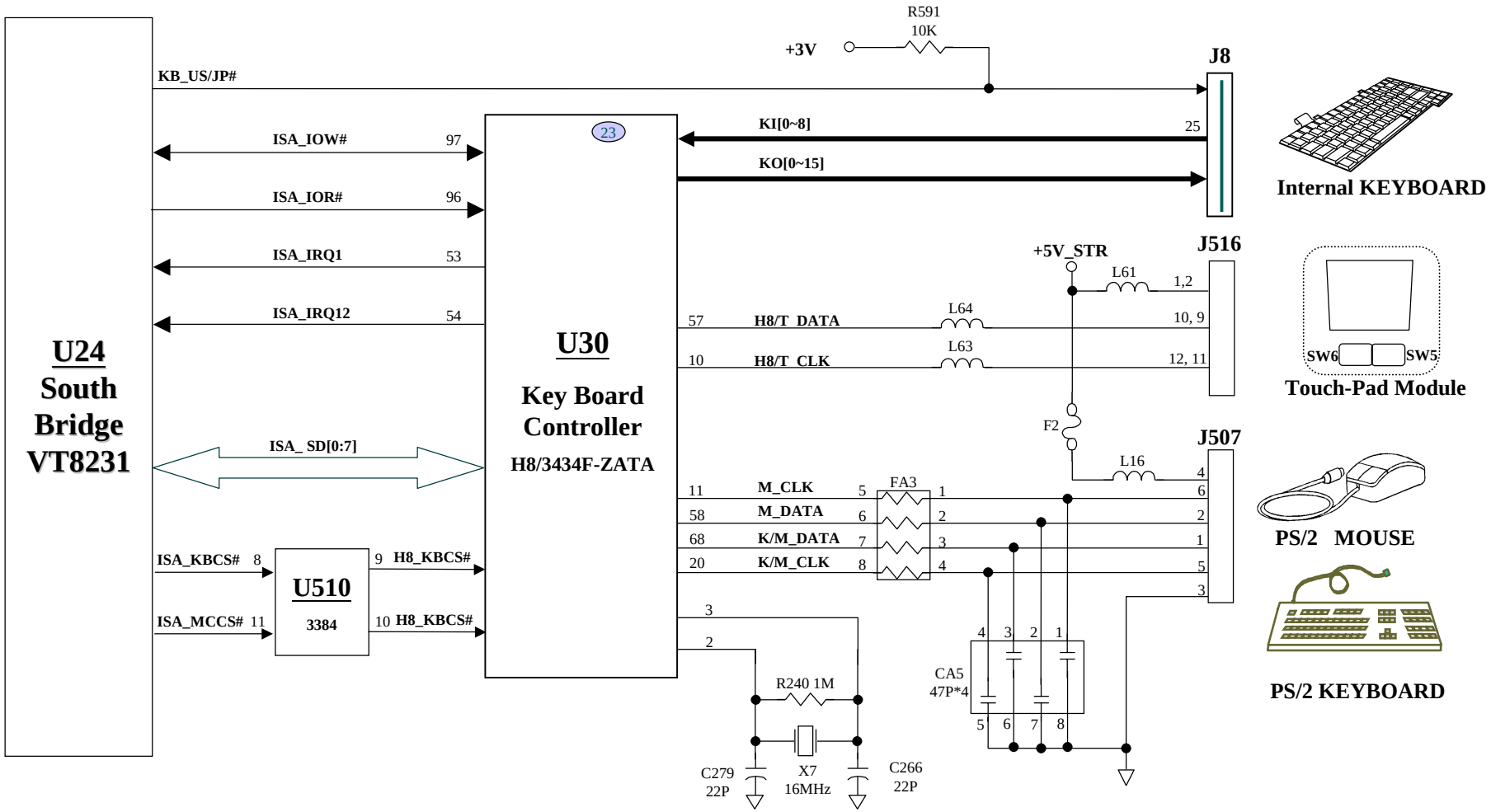
8.6 Memory Test Error

Symptom:
PIO debug board shows the port 378H error code is stopped at 27H,28H or 29H, or error message of memory failure is shown.



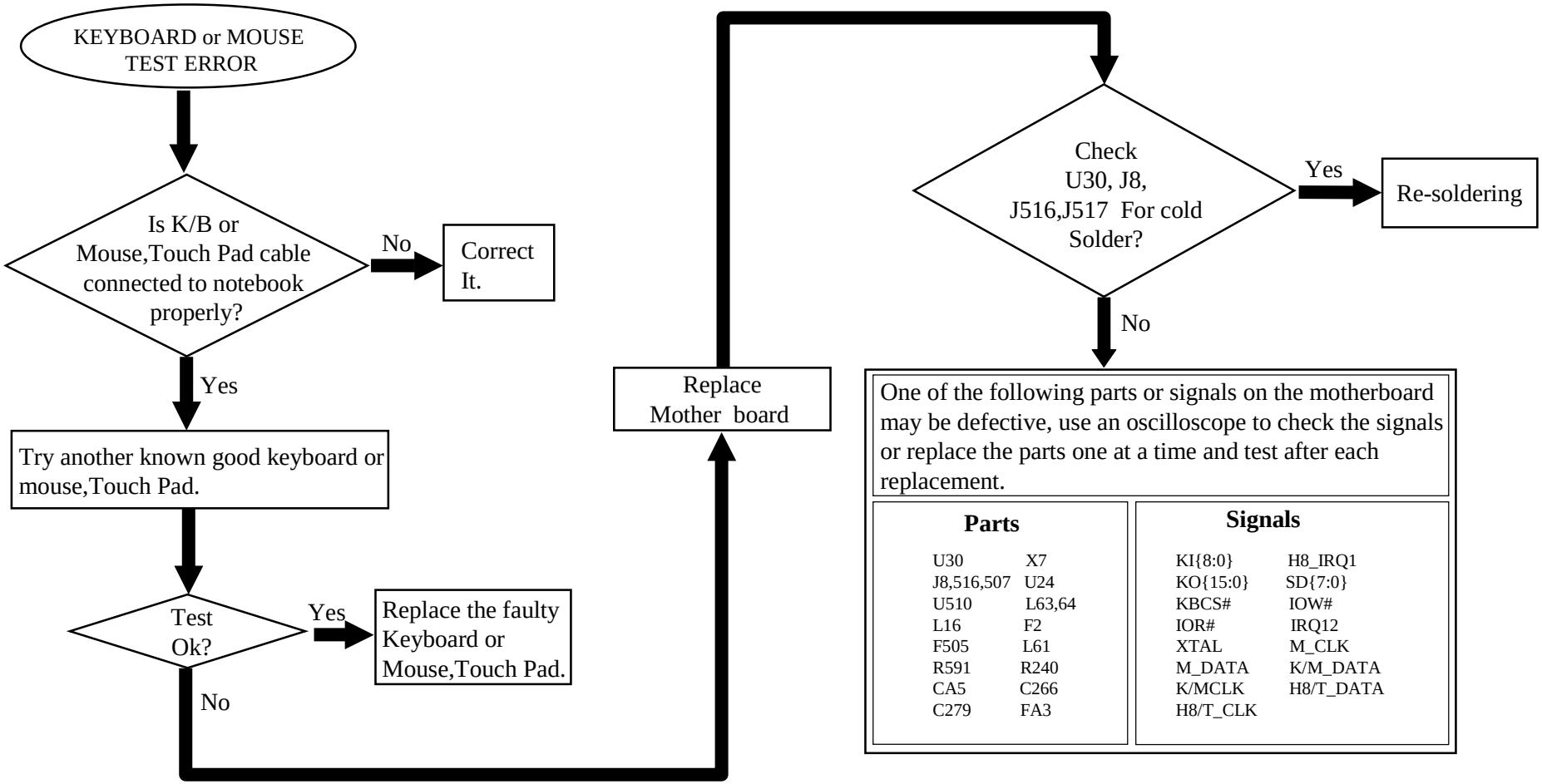
8.7 Keyboard and Touch-Pad Test Error

Symptom:
Error message of keyboard or touch-pad failure is shown or any key does not work.



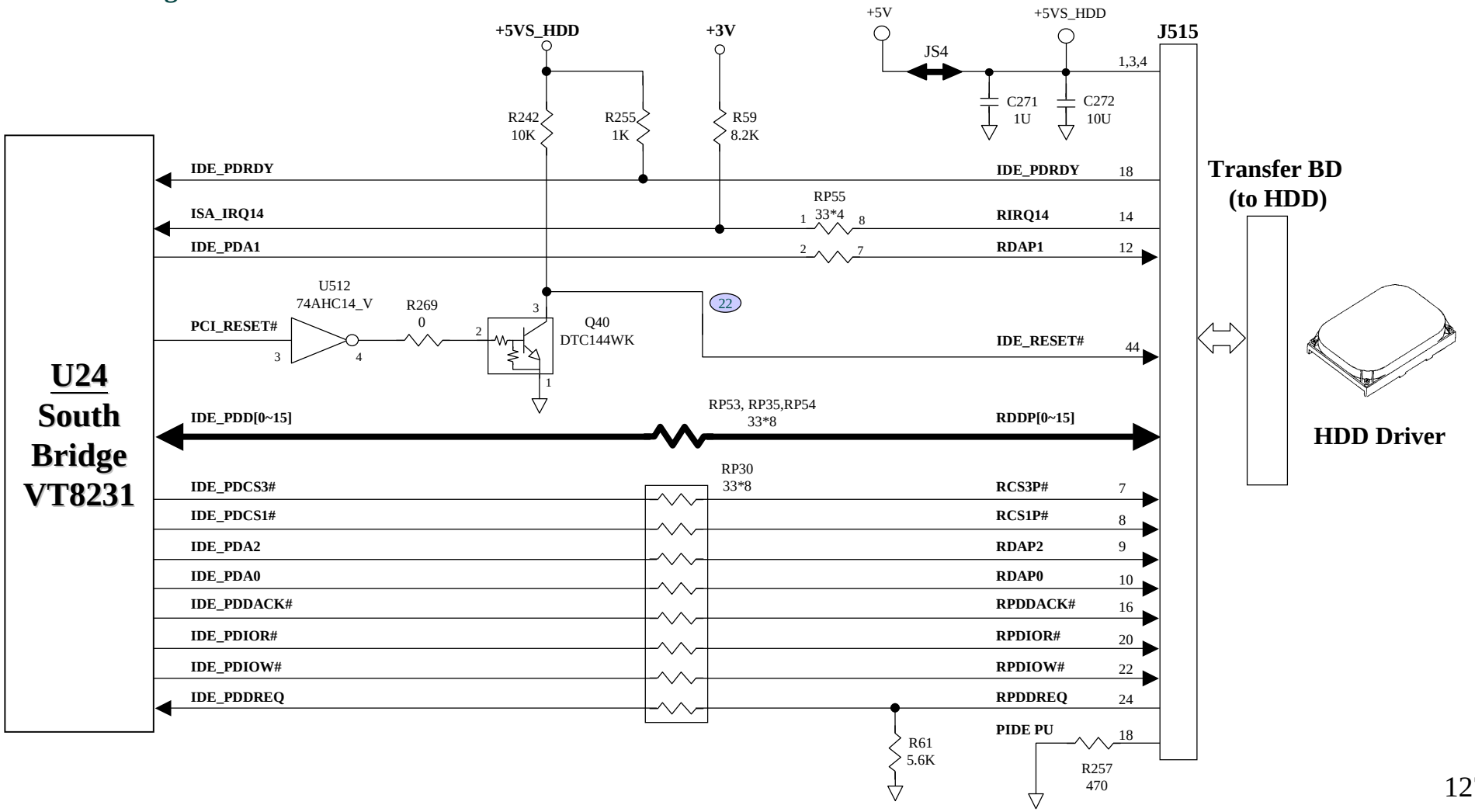
8.7 Keyboard and Touch-Pad Test Error

Symptom:
Error message of keyboard or touch-pad failure is shown or any key does not work.



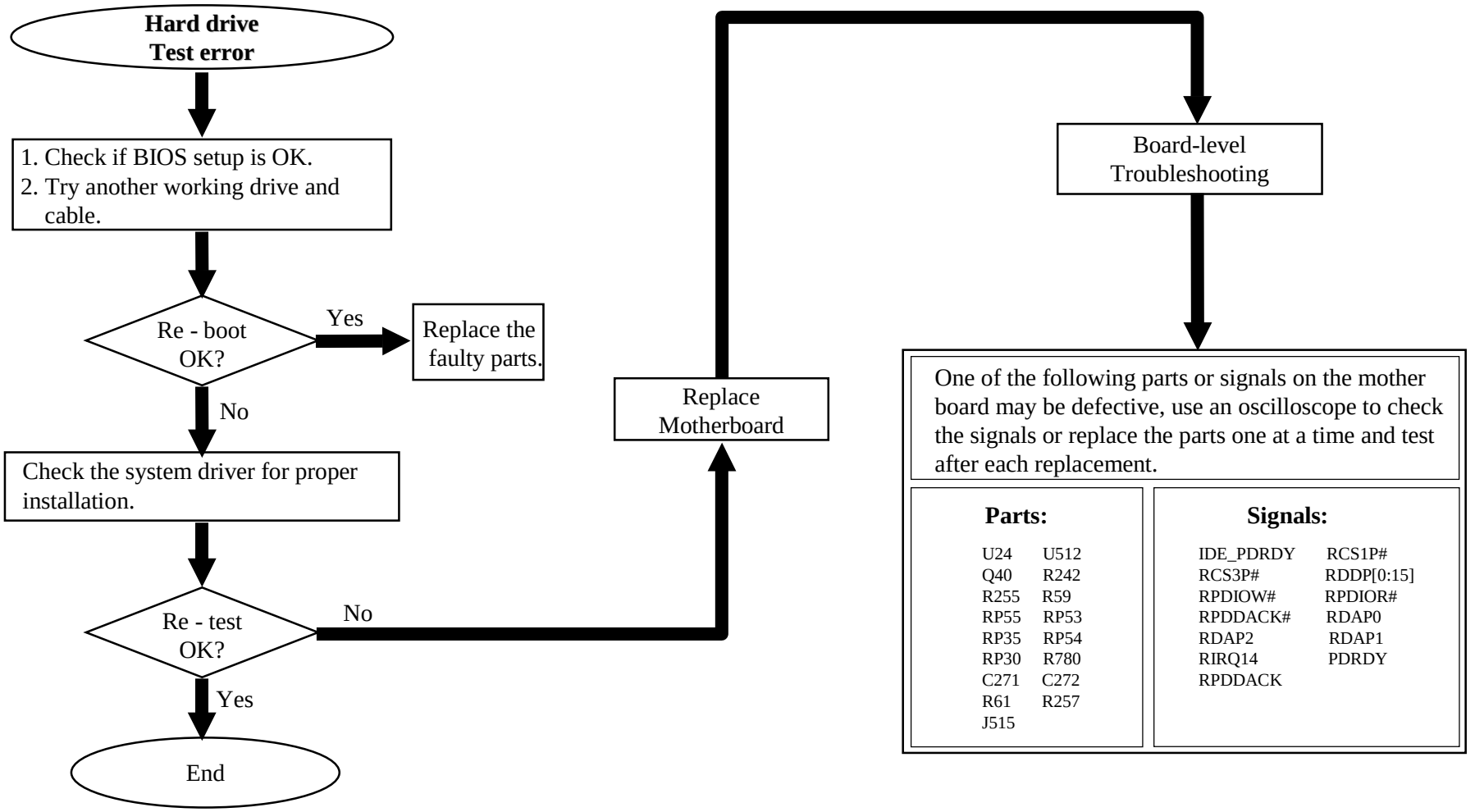
8.8 Hard Drive Test Error

Symptom:
Either an error message is shown, or the drive motor spins non-stop, while reading data from or writing data to hard-disk.



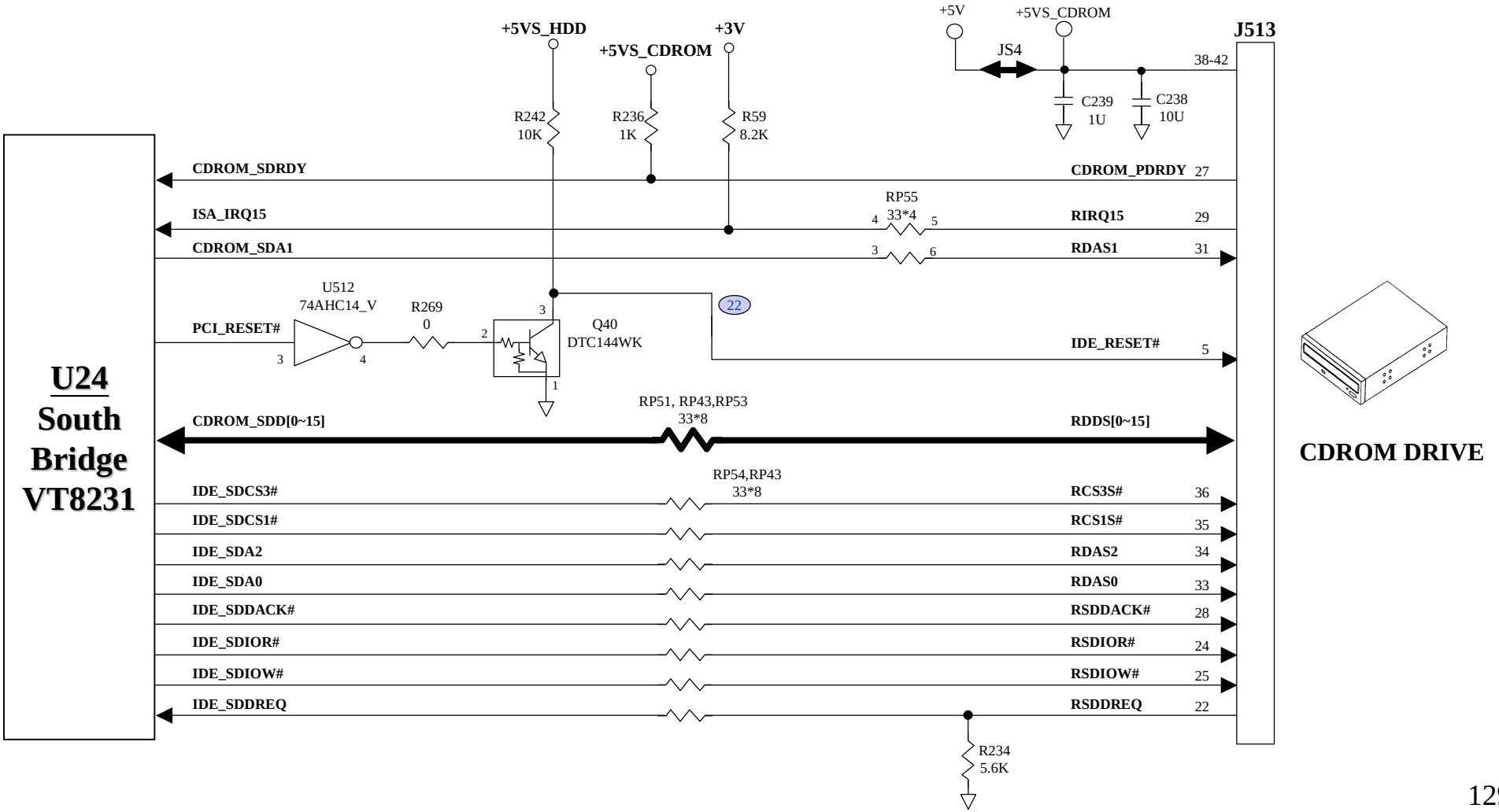
8.8 Hard Drive Test Error

Symptom:
Either an error message is shown, or the drive motor spins non-stop, while reading data from or writing data to hard-disk.



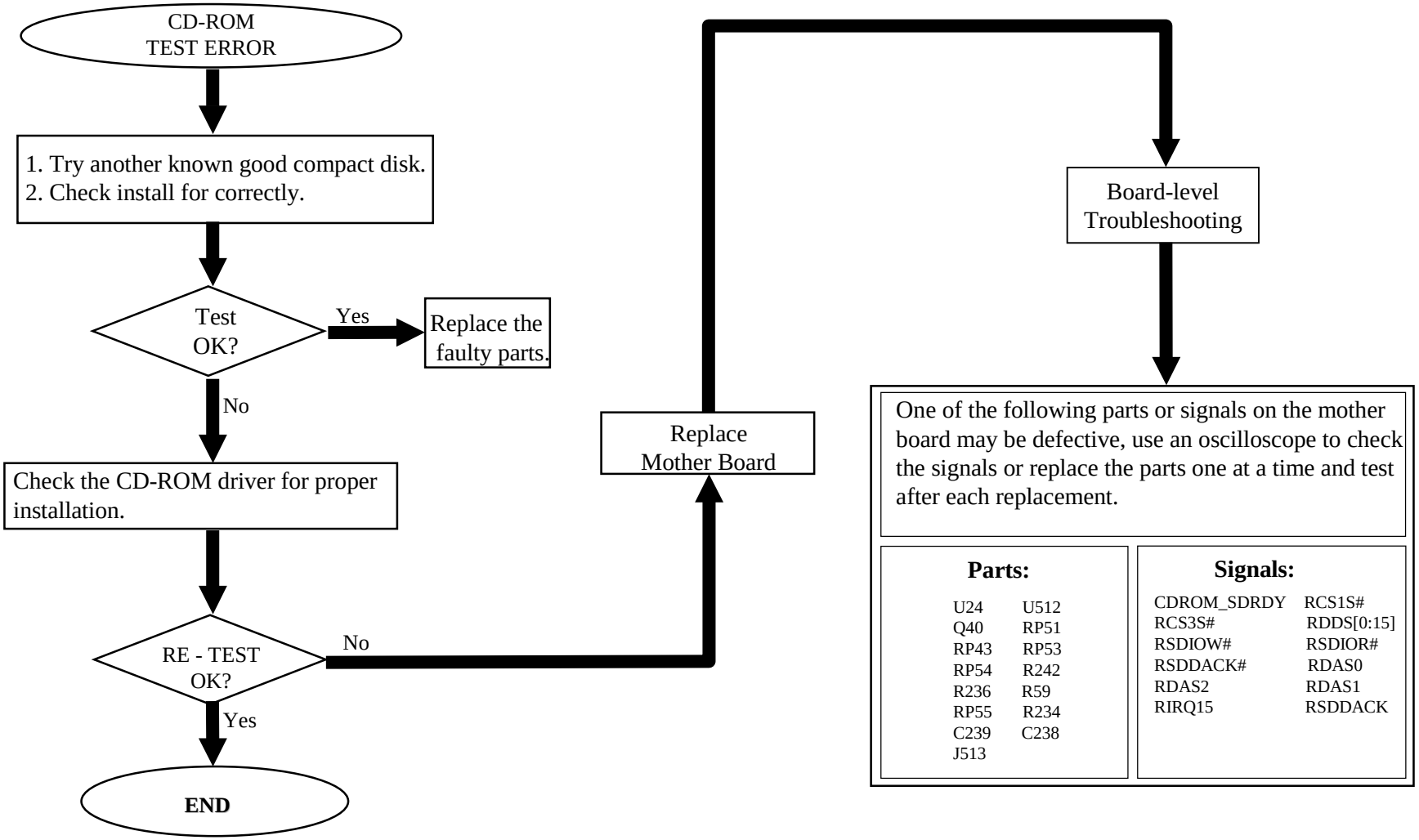
8.9 CD-ROM Test Error

Symptom:
An error message is shown when reading data from CD-ROM drive.



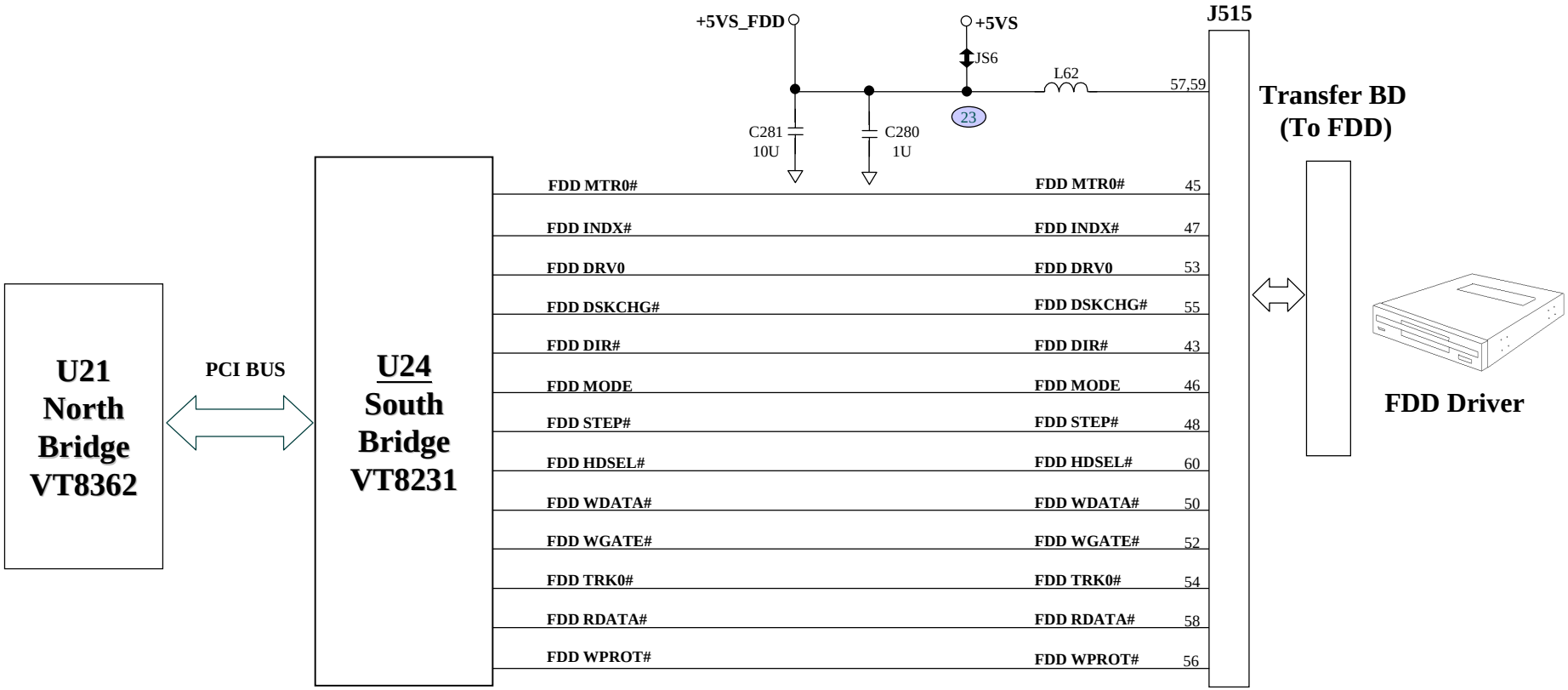
8.9 CD-ROM Test Error

Symptom:
An error message is shown when reading data from CD-ROM drive.



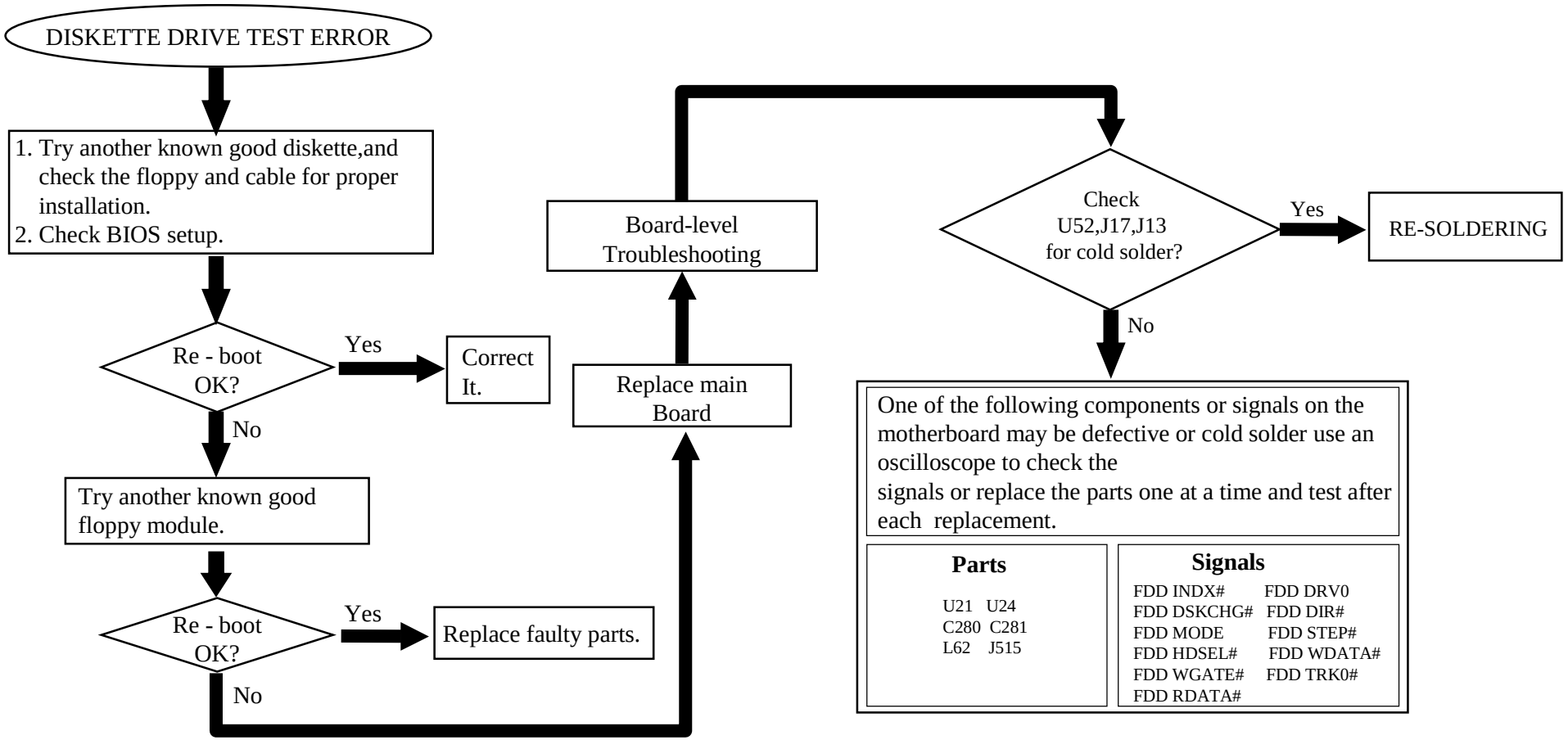
8.10 Diskette Drive Test Error

Symptom:
An Error Message Is Shown When Reading/ Writing Data from/to Diskette Drive.



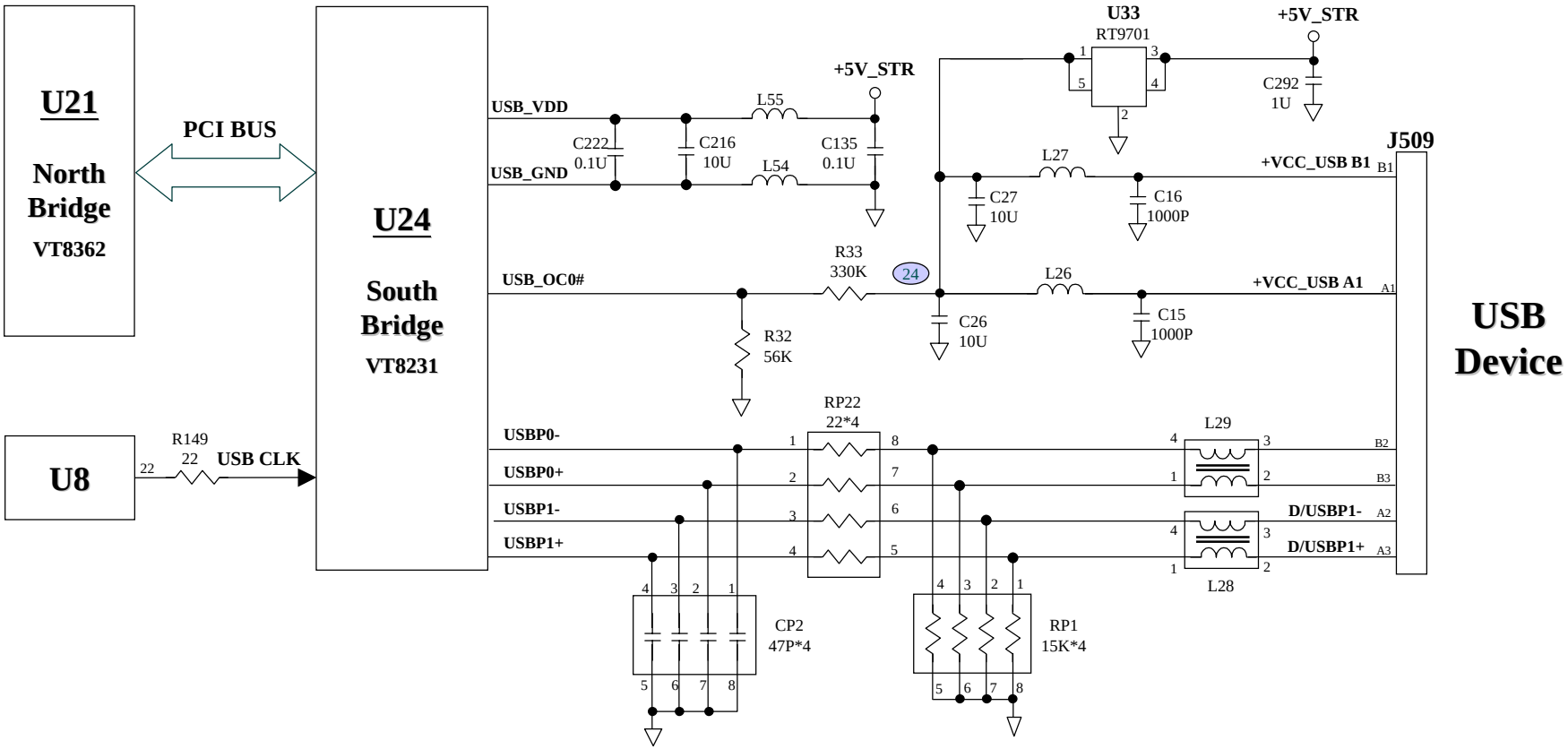
8.10 Diskette Drive Test Error

Symptom:
An Error Message Is Shown When Reading/ Writing Data from/to Diskette Drive.



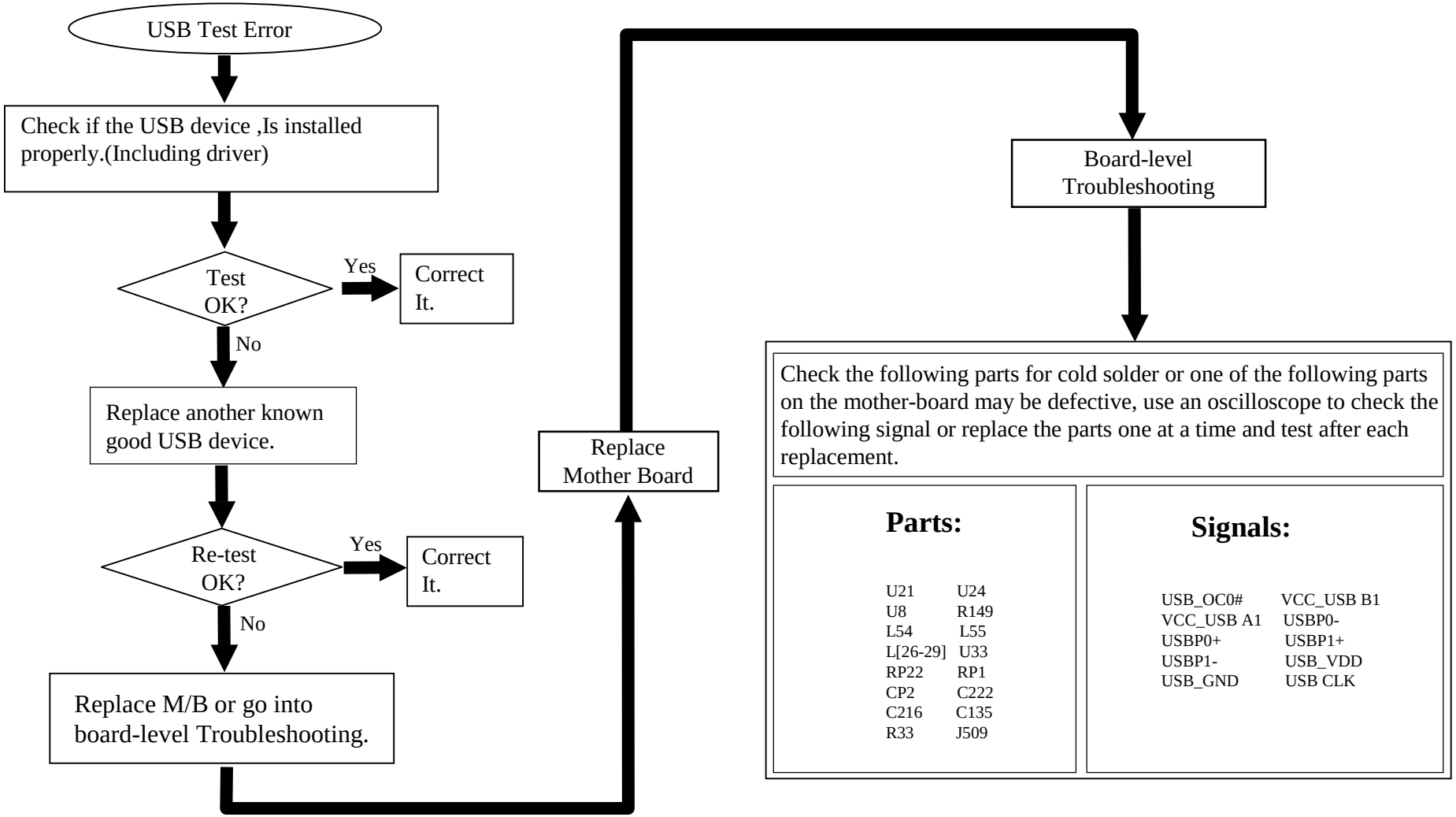
8.11 USB Port Test Error

Symptom:
An error occurs when a USB I/O device is installed.



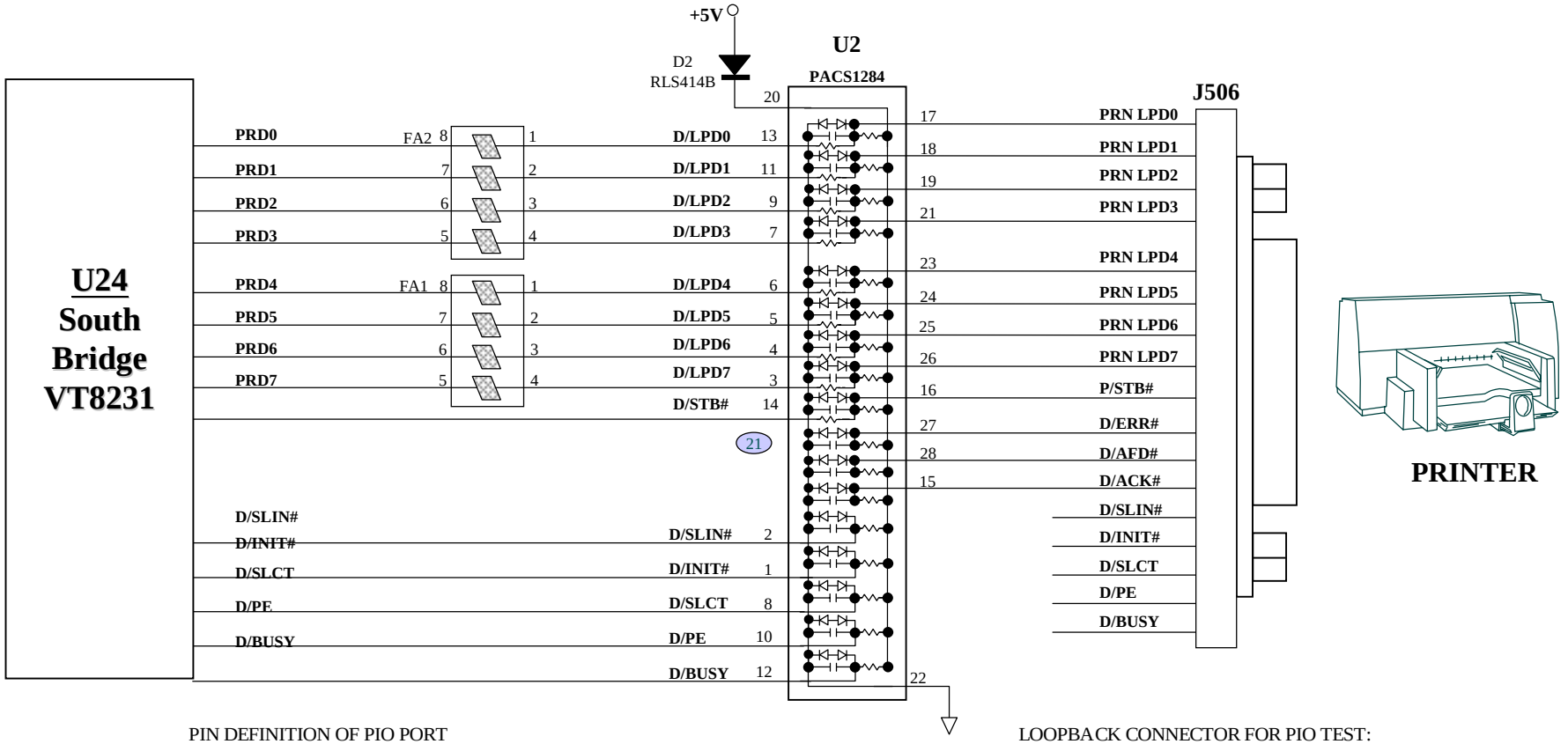
8.11 USB Port Test Error

Symptom:
An error occurs when a USB I/O device is installed.



8.12 PIO Port Test Error

Symptom:
When a print command is issued, printer prints nothing or garbage.



PIN DEFINITION OF PIO PORT

PIN 1	STB	STROBE SIGNAL	PIN 14	AFD	AUTO LINE FEED
PIN 2-9	D0 - D7	PARALLEL PORT DATA BUS D0 TO D7	PIN 15	ERR	ERROR AT PRINTER
PIN 10	ACK	ACKNOWLEDGE HANDSHANK	PIN 16	INIT	INITIATE OUTPUT
PIN 11	BUSY	BUSY SIGNAL	PIN 17	SLIN	PRINTER SELECT
PIN 12	PE	PAPER END	PIN 18-25:		SIGNAL GROUND
PIN 13	SLCT	PRINTER SELECTED			

LOOPBACK CONNECTOR FOR PIO TEST:

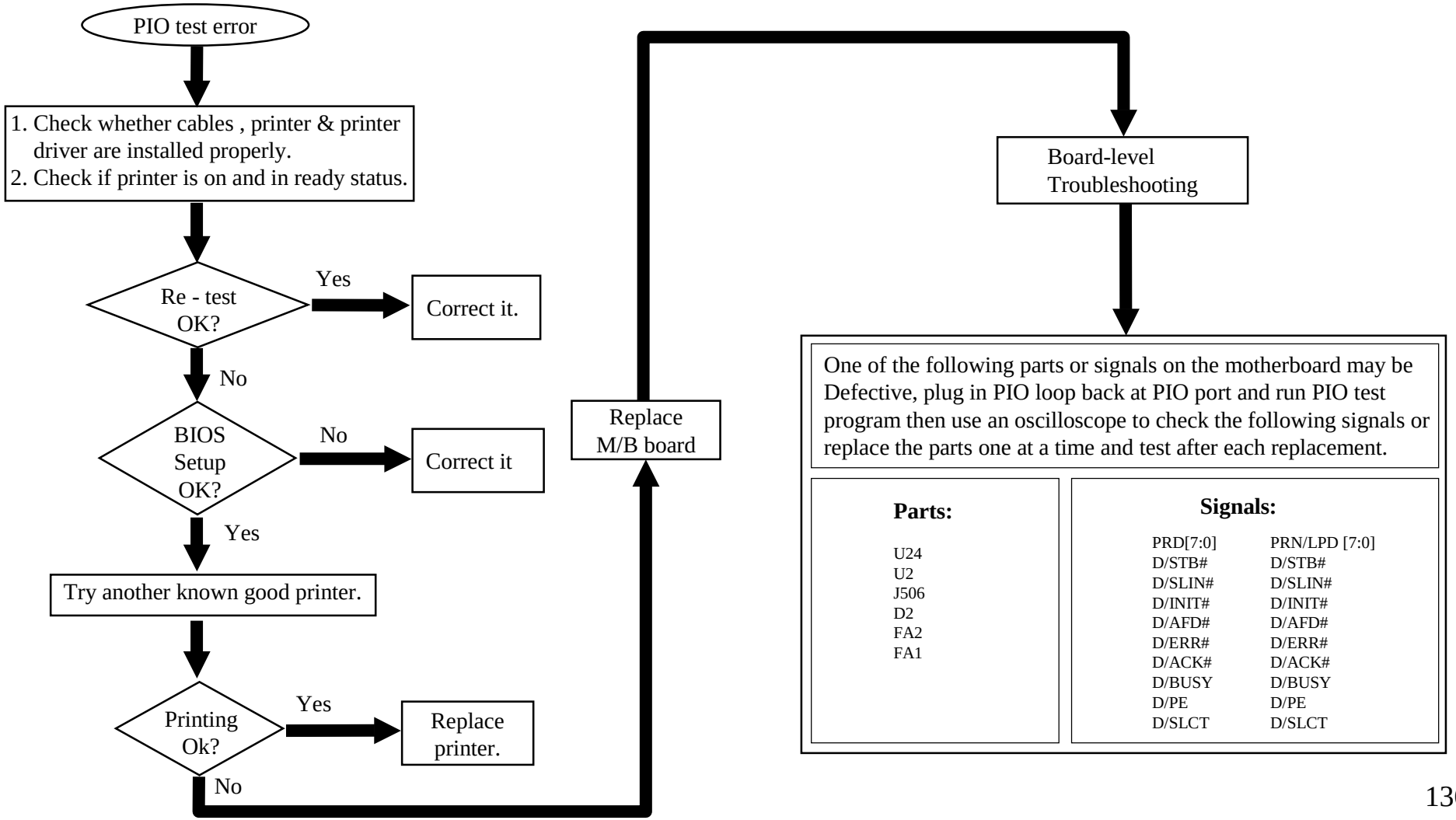
PIN 1, 13	SHORT	PIN 10,16	SHORT
PIN 2, 15	SHORT	PIN 11,17	SHORT
PIN 12, 14	SHORT		

LOOPBACK CONNECTOR FOR EPP TEST:

PIN 1, 2, 4, 6, 8	SHORT
PIN 3, 5, 7, 9, 16	SHORT
PIN 18, 19, 20, 21, 22, 23, 24, 25	SHORT

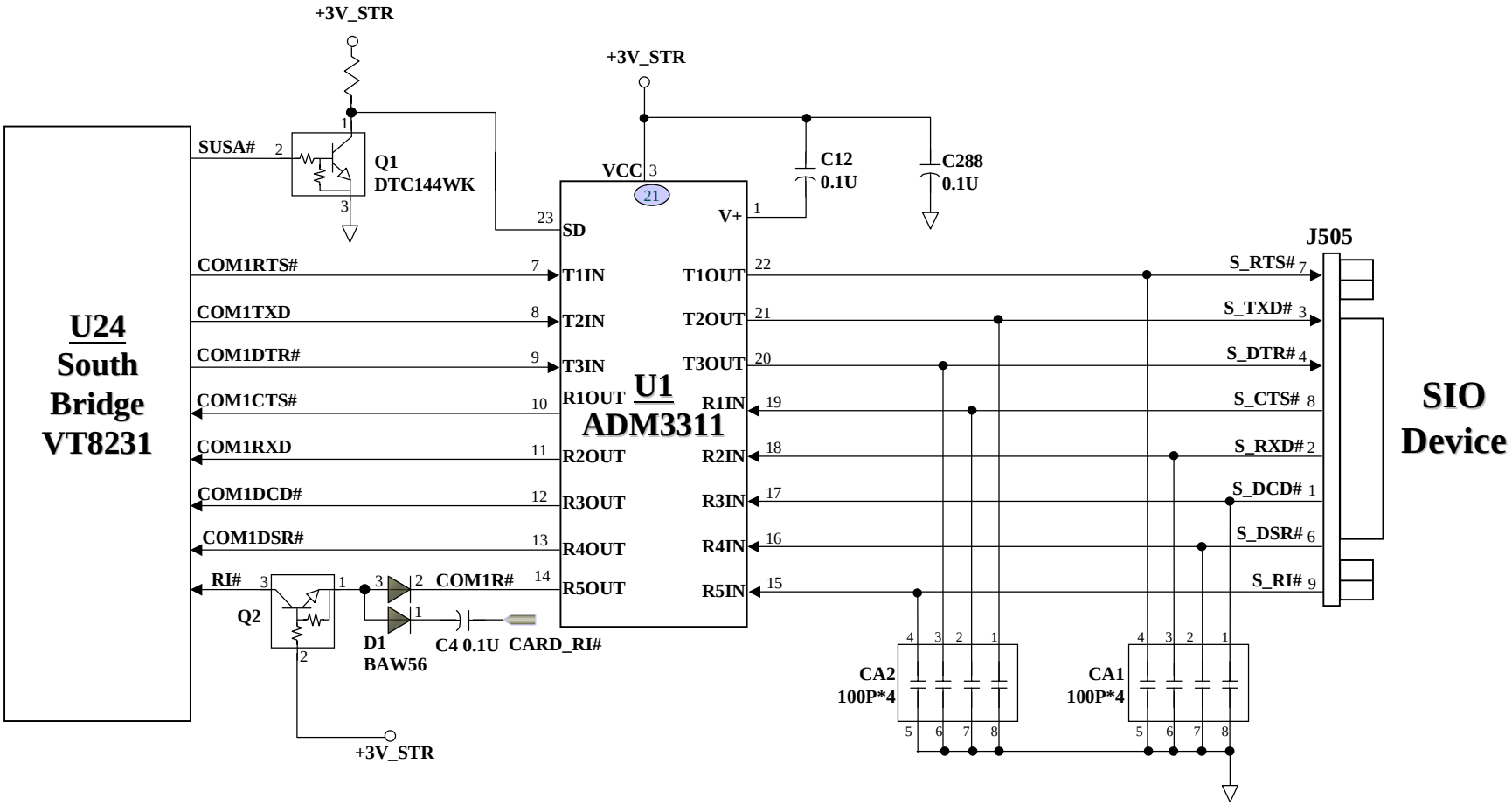
8.12 PIO Port Test Error

Symptom:
When a print command is issued, printer prints nothing or garbage.



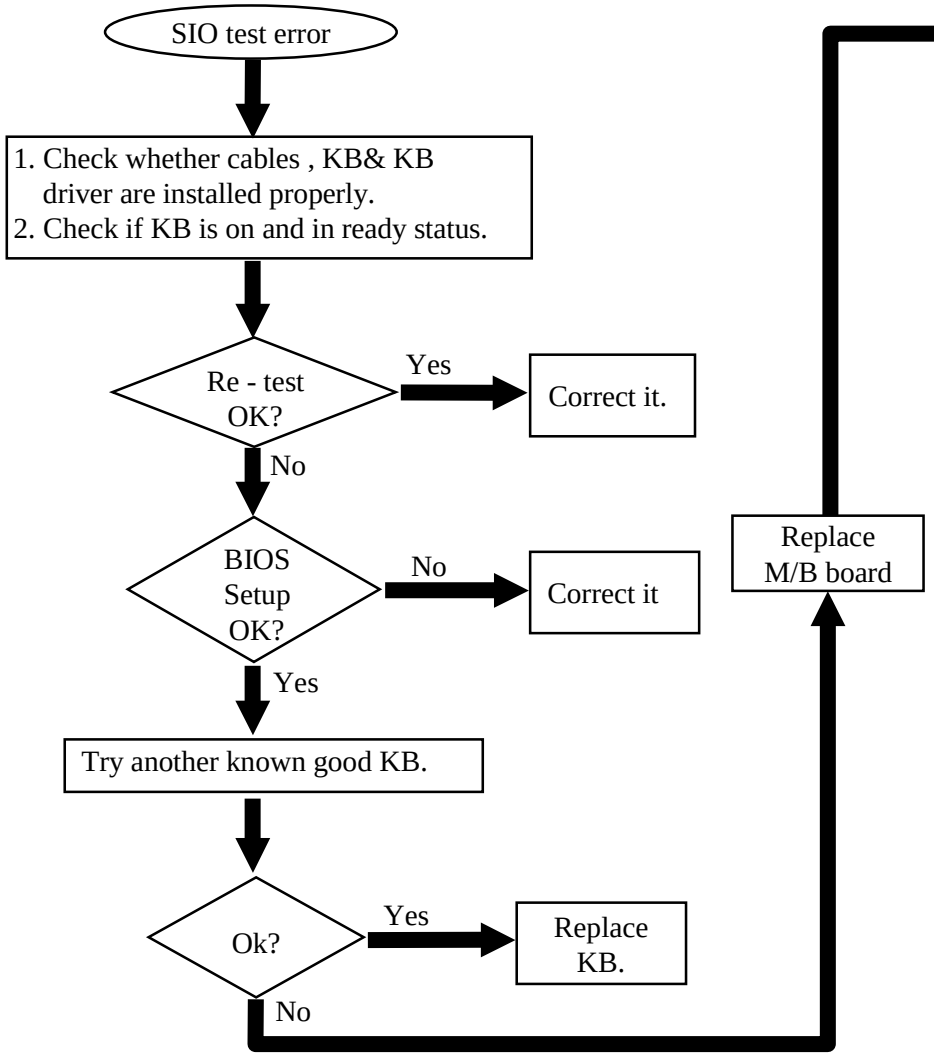
8.13 SIO Port Test Error

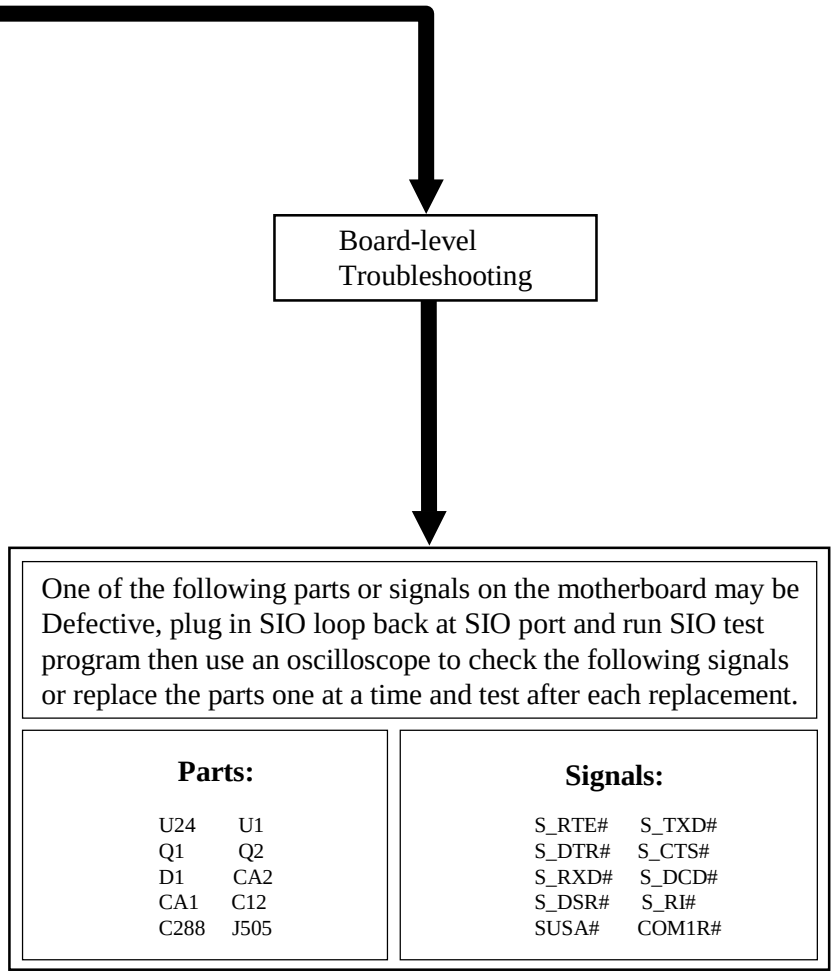
Symptom:
When a SIO device(Such as SIO KB) command is issued, SIO device can not active.



8.13 SIO Port Test Error

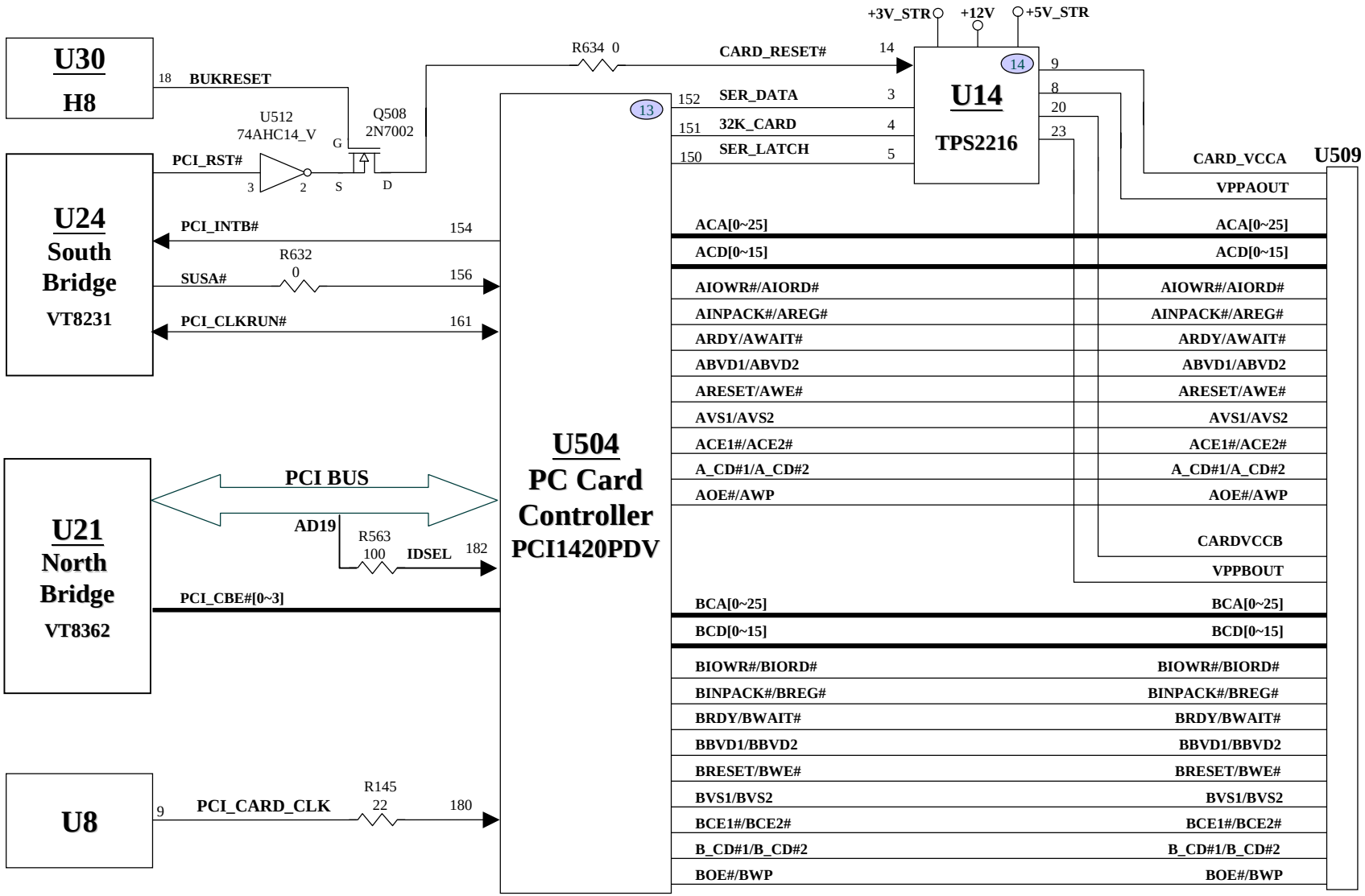
Symptom:
When a SIO device(Such as SIO KB) command is issued, SIO device can not active.





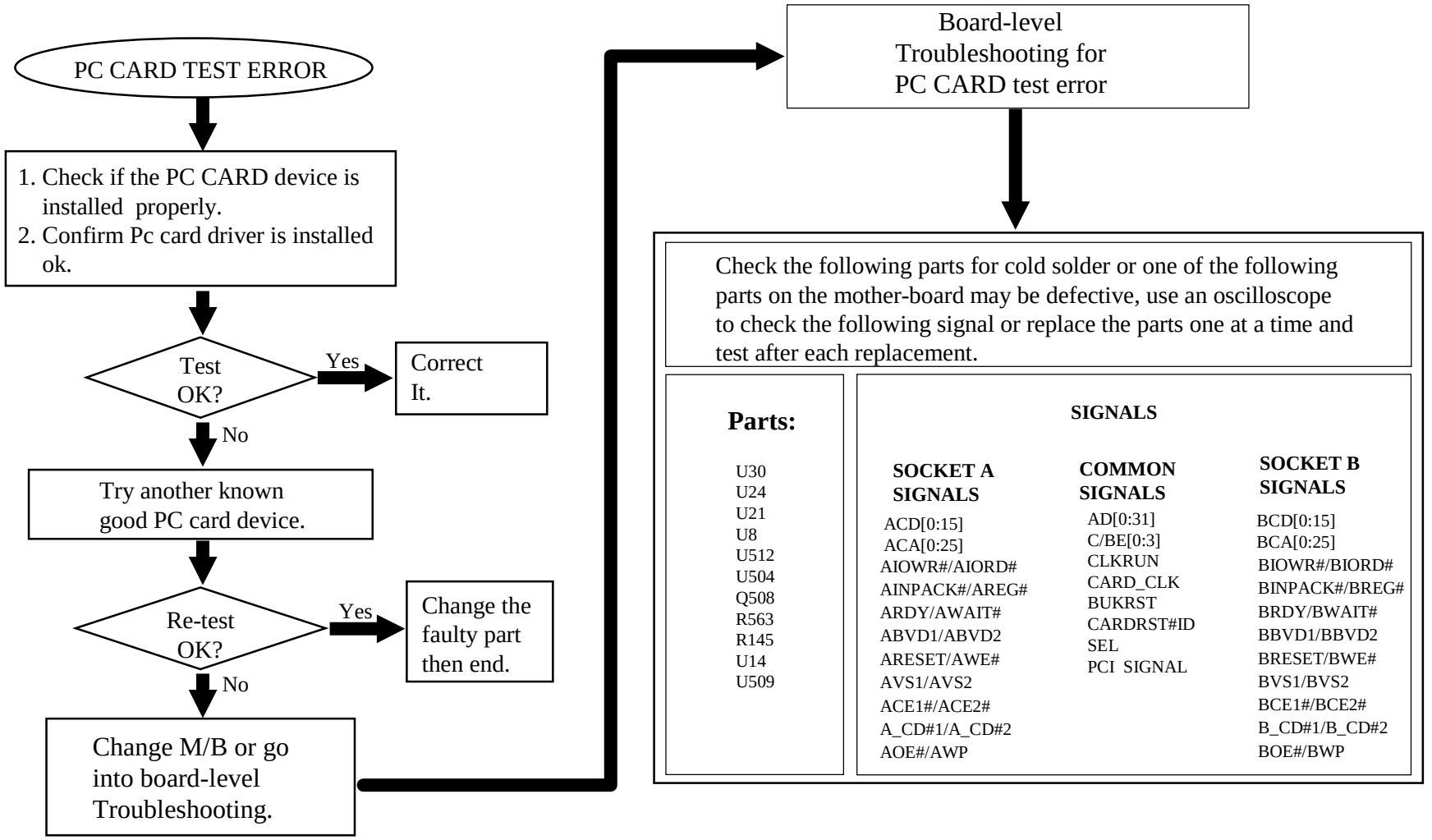
8.14 PC-Card Socket Fail

An error occurs when a PC card device is installed.



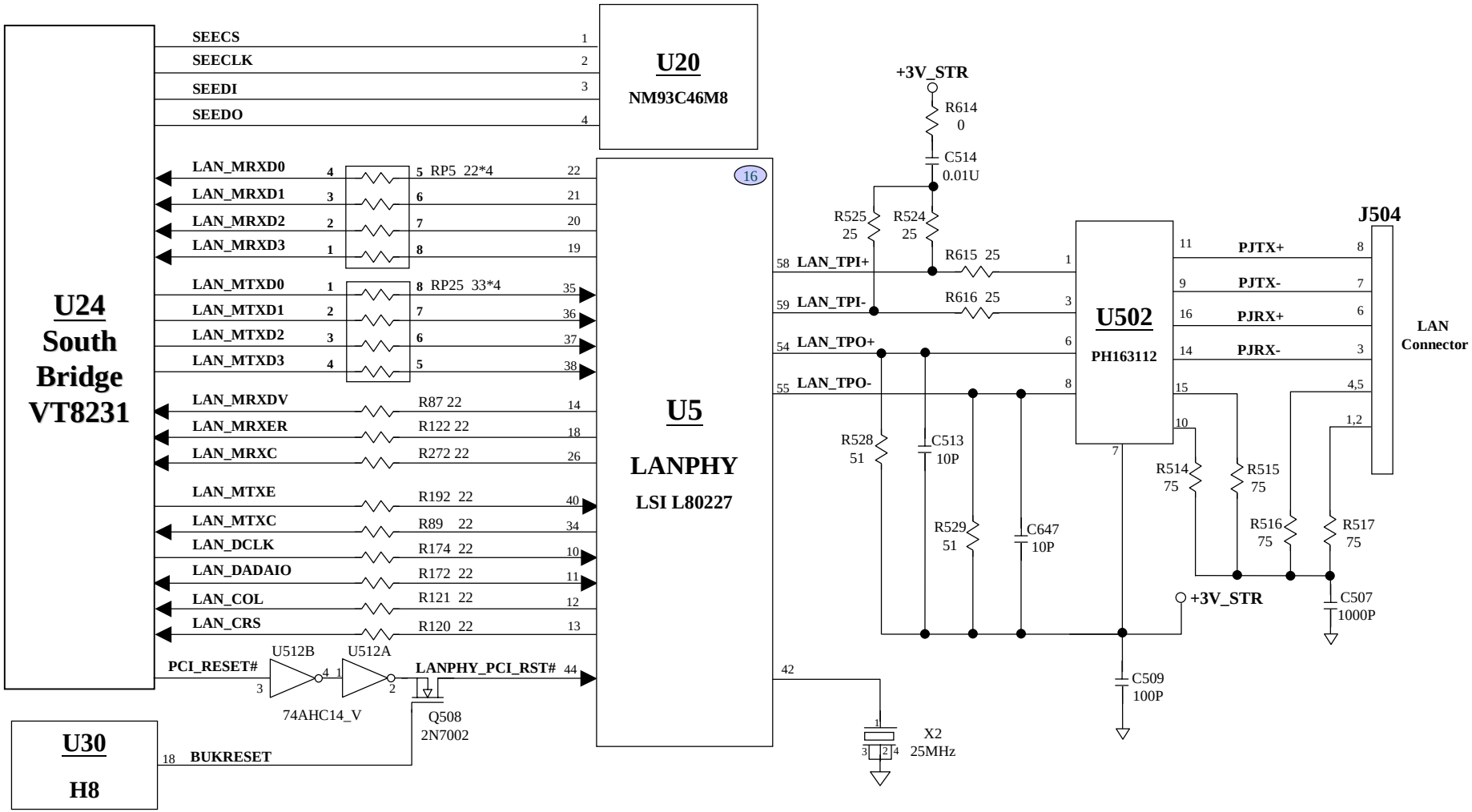
8.14 PC-Card Socket Fail

An error occurs when a PC card device is installed.



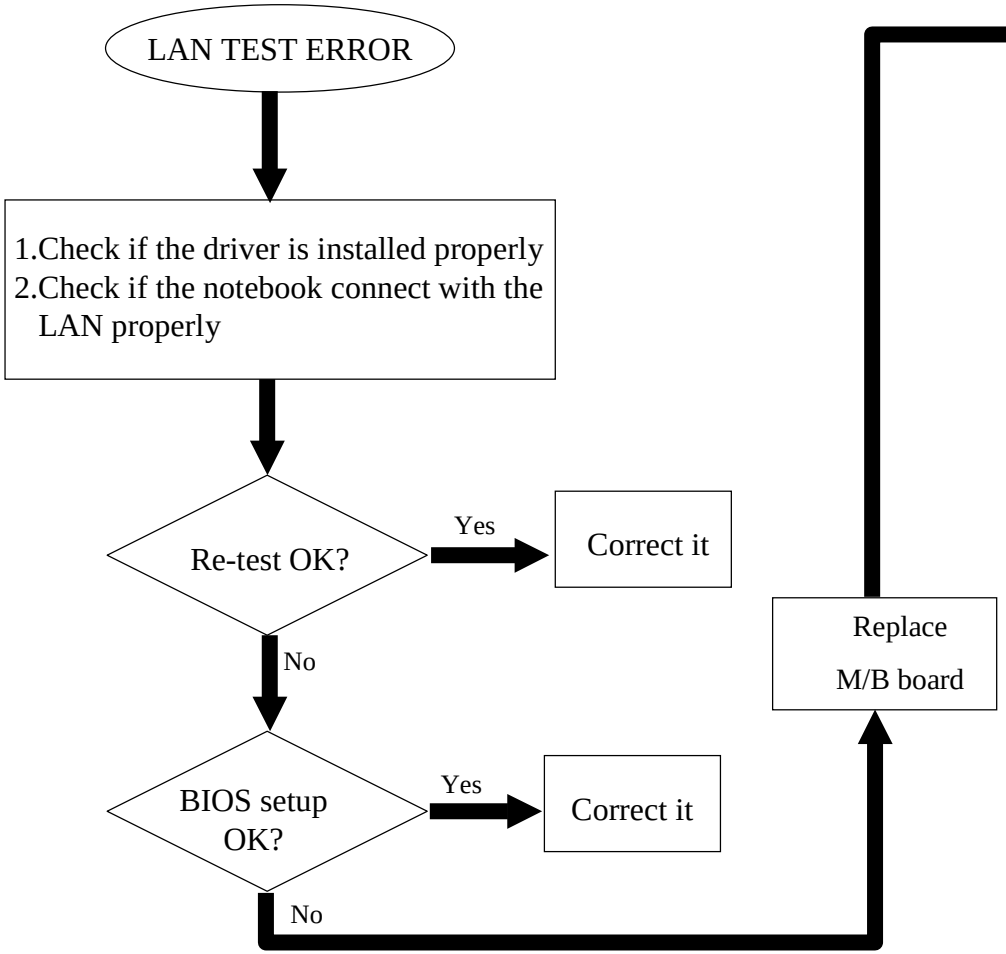
8.15 LAN Test Error

Symptom:
An error occurs when a LAN device is installed.



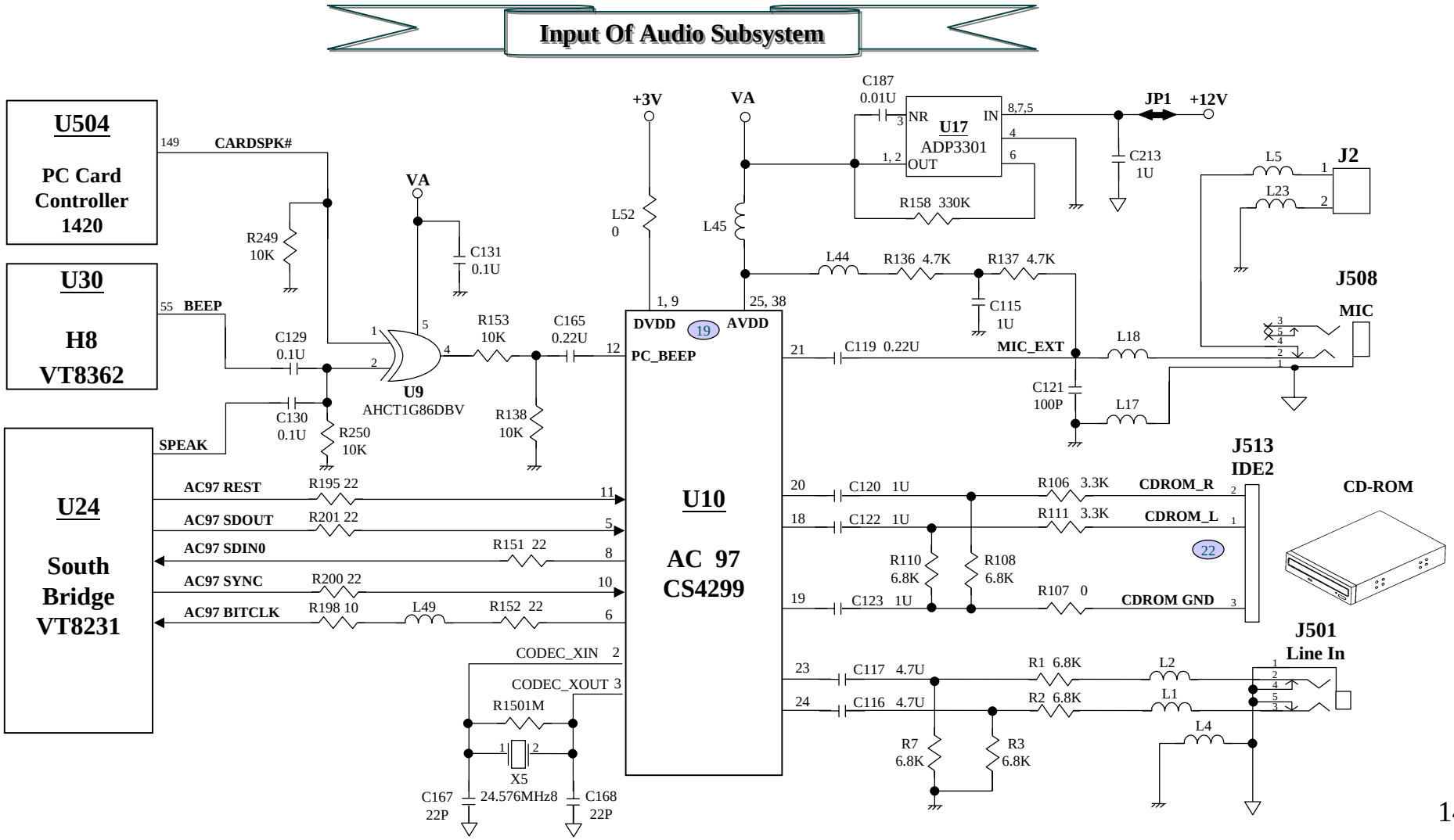
8.15 LAN Test Error

Symptom:
An error occurs when a LAN device is installed.



8.16 Audio Driver Failure

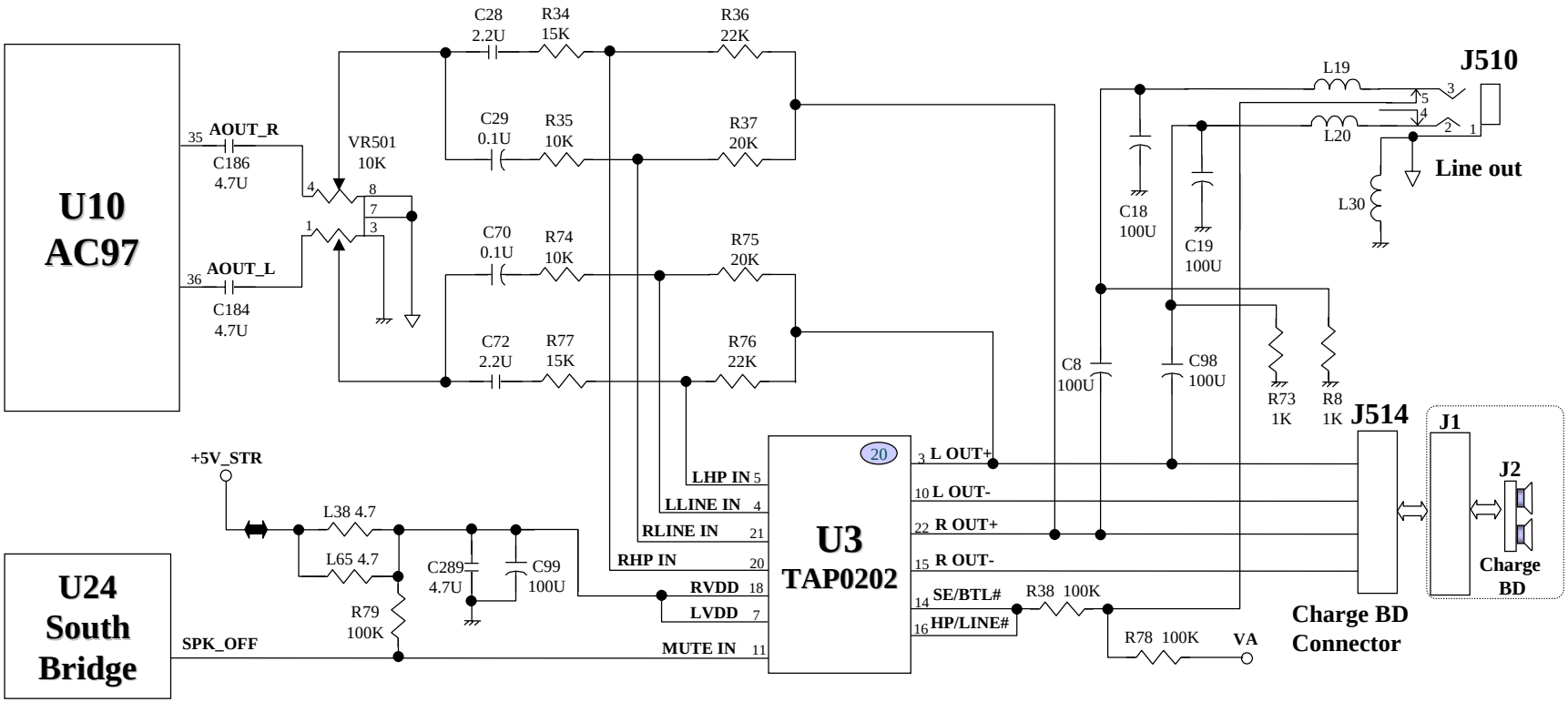
Symptom:
No sound from speaker after audio driver is installed.



8.16 Audio Driver Failure

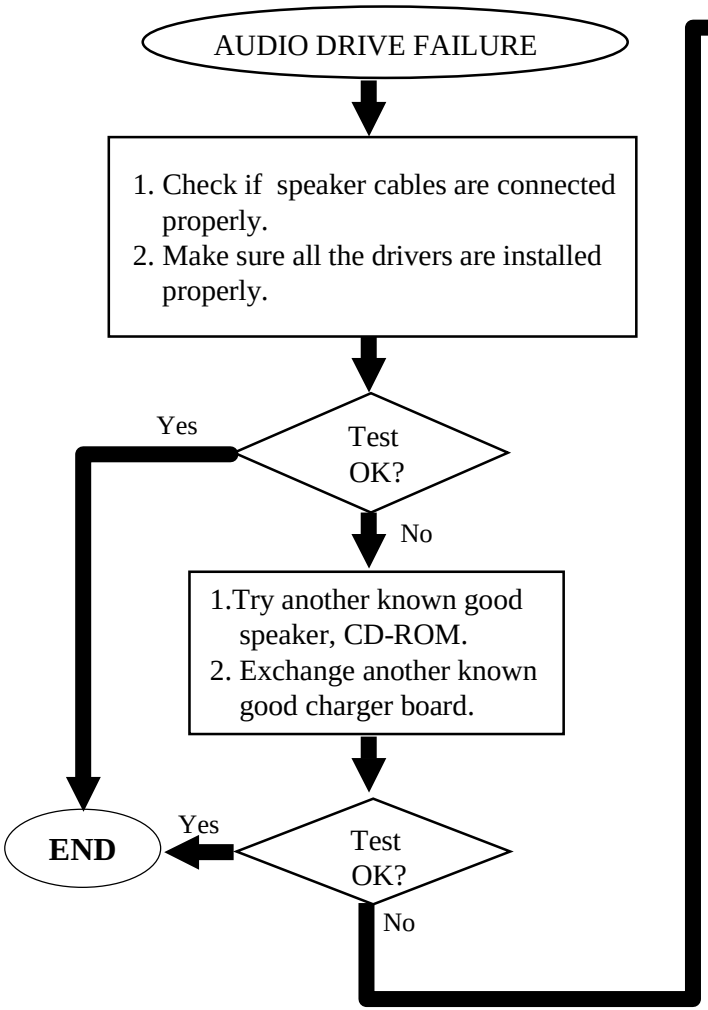
Symptom:
No sound from speaker after audio driver is installed.

Output Of Audio Subsystem



8.16 Audio Driver Failure

Symptom:
No sound from speaker after audio driver is installed.



Replace M/B or go into board-level Troubleshooting.

Check the following parts for cold solder or one of the following parts on the motherboard may be defective,use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

1. If no sound cause of line out, check the following parts & signals:

Parts:		Signals:
U10,	U24	AOUT_R
U3,	J510	AOUT_L
J514	C186	ROUT+
C184	C28,29	ROUT-
C70,72	R[34-37]	LOUT+
R[74-77]	L38	LOUT-
L65	R79	SPK_OFF
R38	L19,20	AC97RESR
L30	C8	PCBEEP
C98	R78	
R150	X5	
C167	C168	

2. If no sound cause of MIC, check the following parts & signals:

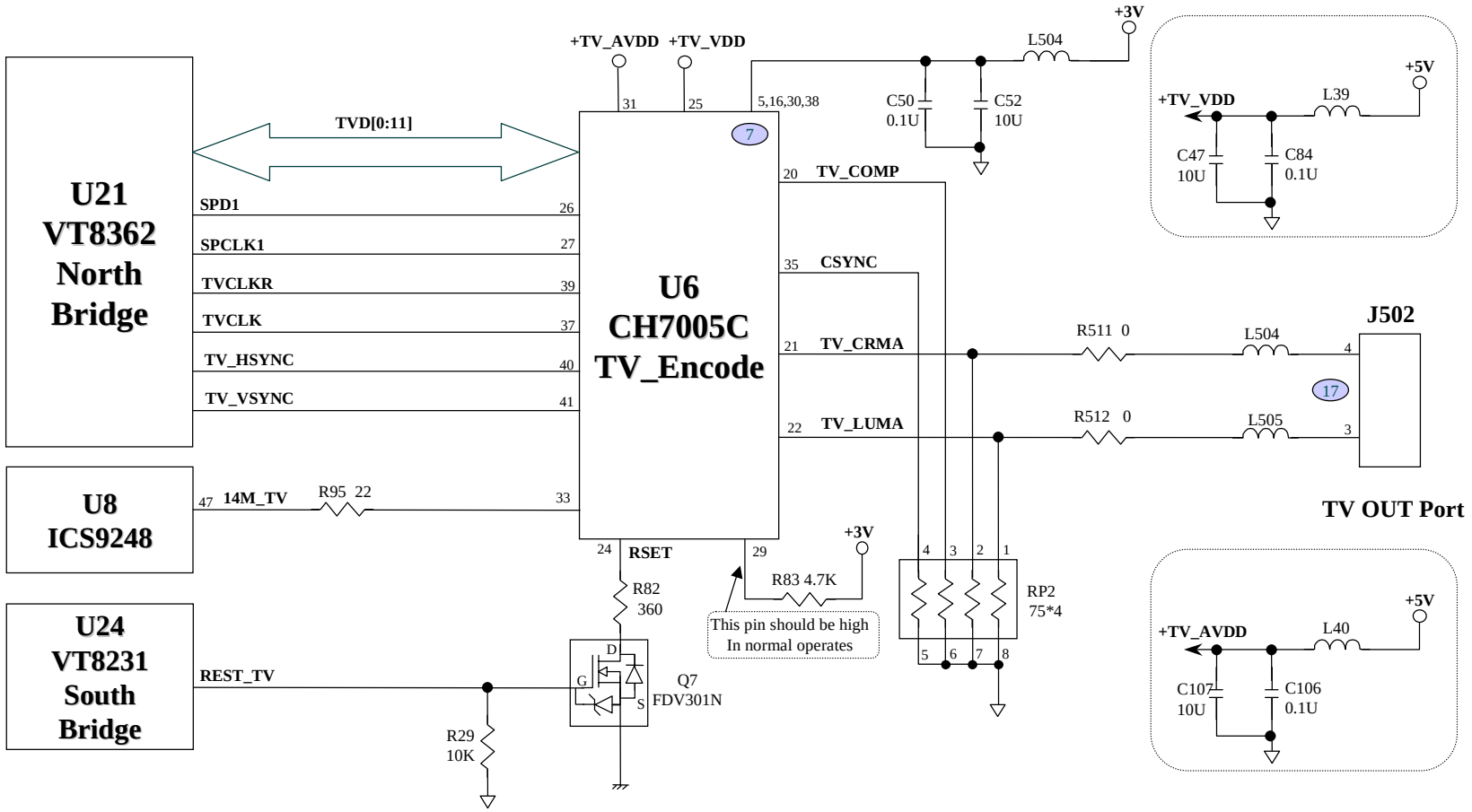
Parts:	Signals:
U17	MIC_EXT
U10	
L45	
L44	
R136	
L17,18	
C121	
C119	
L5,23	
J2,508	

3. If no sound cause of CD-ROM,check the following parts & signals:

Parts:	Signals:
U10	CDROM_L
C120	CDROM_R
C122	CDROM_GND
C123	
R110	
R[106-108]	
R111	
J513	

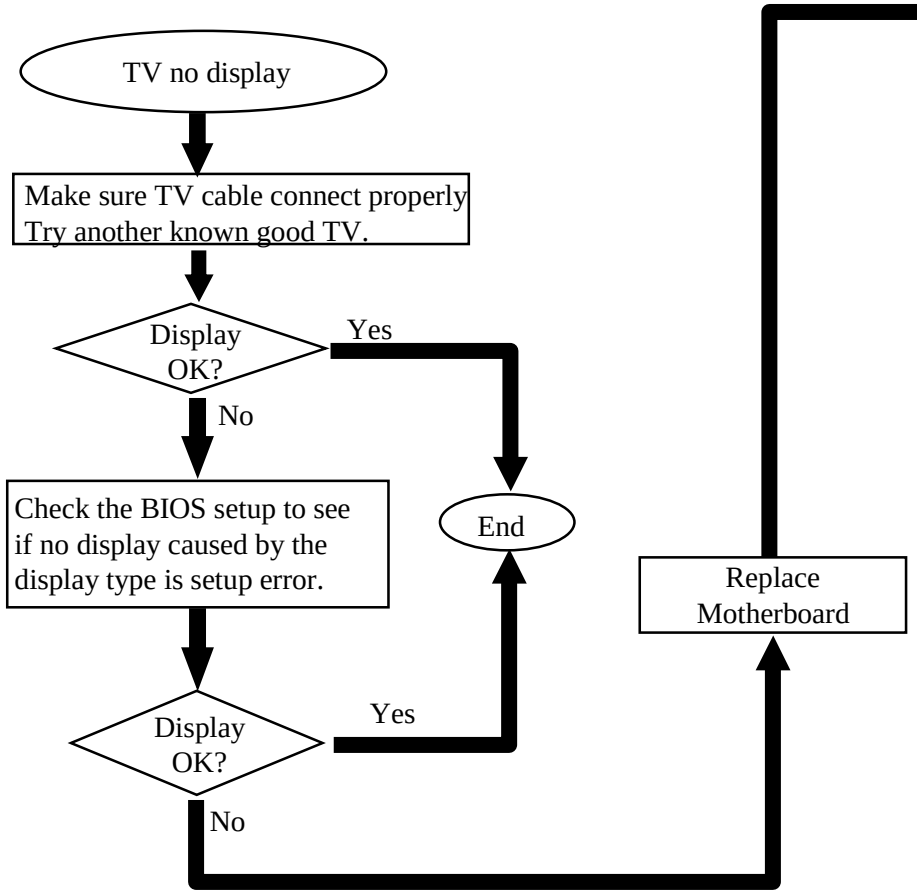
8.17 TV Out Test Failure

Symptom:
No sound from speaker after audio driver is installed.



8.17 TV Out Test Failure

Symptom:
These is no display on TV after power on.



9.Spare parts list(1)

Part Number	Description	Location(s)
442051200001	AC ADPT ASSY;19V/3.16A,DELTA	
541666980001	AK KIT;EN,UTILITY,7321	
541666980026	AK;GR,BOX,7321 CTO	
441999900045	BATT ASSY OPTION;Li-Ion,7321	
442670040002	BATT ASSY;14.8V,3.6AH,LI,PAN,ID2 C,7521	
298000000002	BATTERY HOLDER;FOR CR2032,BH-800.1K	BT501
338530010005	BATTERY;LI,3V/220MAH,CR2032	
340670000012	BEZEL ASSY,DVD-ROM,QUANTA,7521	
221670040001	BOX;AK,7521	
340669600048	BRACKET ASSY-4;I/O,TV-OUT,RACE	
342670000001	BRACKET; LCD,HY14X13,L,7521	
342670000002	BRACKET; LCD,HY14X13,R,7521	
342669600014	BRACKET;CD-ROM,RACE	
342666600002	BRACKET;HDD,TITAN	
344670000005	BUTTON;TOUCH PAD,7521	
421015560001	CABLE ASSY;PHONE LINE,6P2C,W/Z CORE	
332300000115	CABLE;FFC,FDD,6020	
332669600002	CABLE;FFC,IQSB BD,CHARGER BD,REDSEA	
332669600001	CABLE;FFC,TOUCHPAD,REDSEA	
272075103702	CAP;.01U ,50V,+80-20%,0603,SMT	C111,C144,C148,C152,C
272075103401	CAP;.01U ,CR,50V ,10%,0603,X7R,SMT	PC3,4,9,10,502,503
272075104701	CAP;.1U ,50V,+80-20%,0603,SMT	C1,C10,C106,C108,C109,
272075104701	CAP;.1U ,50V,+80-20%,0603,SMT	C2
272075104701	CAP;.1U ,50V,+80-20%,0603,SMT	C503
272075104701	CAP;.1U ,50V,+80-20%,0603,SMT	C1,2,PC5,6,500

Part Number	Description	Location(s)
272072224701	CAP;.22U ,16V ,+80-20%,0603,Y5V,SMT	C119,C165,C516,C517,C
272002474401	CAP;.47U ,CR,16V ,10%,0805,X7R,SMT	C6
272030102401	CAP;1000P,2KV,10%,1808,X7R,SMT	C507
272030102401	CAP;1000P,2KV,10%,1808,X7R,SMT	C1,C2
272075102701	CAP;1000P,50V ,+/-20%,0603,X7R,SMT	C15,C158,C16,C163,C16
272075101701	CAP;100P ,50V ,+ -10%,0603,NPO,SMT	C121,C18,C19
272075101401	CAP;100P ,50V ,10%,0603,COG,SMT	C505,C506,C509
272075100401	CAP;10P ,50V ,10%,0603,COG,SMT	C140,C141,C143,C146,C
272021106501	CAP;10U ,10V ,20%,1210,X7R,SMT	PC34,PC5
272011106701	CAP;10U ,10V,+80-20%,1206,Y5V,SMT	C107,C193,C196,C216,C
272023106501	CAP;10U ,25V ,20%,1210,Y5U,SMT	PC23,PC26,PC27,PC28,P
272075121401	CAP;120P ,CR,50V ,10%,0603,NPO,SMT	PC42
272071105701	CAP;1U ,CR,10V ,80-20%,0603,Y5V	C115,C172,C173,C175,C
272071105701	CAP;1U ,CR,10V ,80-20%,0603,Y5V	C1
272003105701	CAP;1U ,CR,25V ,+80%-20%,0805,Y5V	PC7,8
272013105501	CAP;1U ,CR,25V ,+80-20%,1206,SMT	PC13
272002105701	CAP;1U ,CR,16V ,-20+80%,0805,Y5V,S	C120,C122,C123,C174,C
272002105701	CAP;1U ,CR,16V ,-20+80%,0805,Y5V,S	C1,C2,C3,C4
272002225701	CAP;2.2U ,CR,16V ,+80-20%,0805,Y5V	C161,C203,C204,C28,C3
272012225702	CAP;2.2U ,CR,16V ,+80-20%,1206,Y5V	C137,C202,C622
272075222701	CAP;2200P,50V ,+/-20%,0603,X7R,SMT	C550,C551
272075221302	CAP;220P ,50V ,5% ,0603,NPO,SMT	C14,C23
272431227506	CAP;220U ,2.5V,20%,7343,POSCAP,SMT	PC1,PC33,PC44,PC45,PC
272075220701	CAP;22P ,50V ,+ -10%,0603,NPO,SMT	C167,C168,C266,C279
272021226701	CAP;22U ,10V,+80-20%,1210,Y5V,SMT	C295

9.Spare parts list(2)

Part Number	Description	Location(s)
272075390301	CAP;39P ,50V ,5% ,0603,NPO,SMT	C11,C138,C304,C305,C3(
272001475701	CAP;4.7U ,CR,10V ,+80-20%,0805,Y5V,	C113,C116,C117,C145,C1
272012475701	CAP;4.7U ,CR,16V ,+80-20%,1206,Y5V	C195,C214,C5
272075471401	CAP;470P ,50V,10%,0603,X7R,SMT	PC62,PC63,PC65
272075471401	CAP;470P ,50V,10%,0603,X7R,SMT	PC11,802,803,807
272075470401	CAP;47P ,50V ,10%,0603,COG,SMT	C250,C251,C252,C261,C2
272075681401	CAP;680P ,50V ,10%,0603,X7R,SMT	C562,C563
221670020002	CARTON;NON-BRAND,7521	
431669800002	CASE KIT;14.1",7321,ID3	
342665500008	CFM-SUYIN;S-STANDOFF,#4-40H4.8,NIW	
273000500020	CHOKE COIL;100UH,6X4X4.5,T04020202	L2
273000111002	CHOKE COIL;120OHM/100MHZ,20%,3216	L28,L29
313000020206	CHOKE;1.3UH,+-20%,4.5TS,D0.6X3,TUBE	PL506,PL507
331720015023	CON;D,FM,15P,2.29,R/A,3 ROW,TITAN	J503
331720025012	CON;D,FM,25P,2.77,R/A,TITAN	J506
331720009008	CON;D,MA,9P,2.775,R/A,TITAN	J505
291000151204	CON;FPC/FFC,12P,.5MM,R/A,SMT,REDSEA	J516
291000141402	CON;FPC/FFC,14P,0.5MM,SMT	J500
291000141402	CON;FPC/FFC,14P,0.5MM,SMT	J500
291000152604	CON;FPC/FFC,26P,1MM,R/A,ELCO,SMT	J8
291000152602	CON;FPC/FFC,26P,1MM,R/A,SMT,ELCO	J2
291000023002	CON;HDR,FM,15P*2,0.8MM.H4.4,R/A,SMT	J511
291000023201	CON;HDR,FM,16P*2,1.27MM,R/A,SMT	J514
331030060003	CON;HDR,FM,20P*3,.8MM,ST,DIP	J1
331030044006	CON;HDR,FM,22P*2,2.0MM,ST,SUYIN,DIP	J3

Part Number	Description	Location(s)
291000010604	CON;HDR,FM,6P*1,1.25MM,ST,SMT	J5
291000011411	CON;HDR,FM,7P*2,1.27MM,ST,SMT	J501
291000013010	CON;HDR,MA,15P*2,1.0MM,ST,SMT	J3
331040060003	CON;HDR,MA,20P*3,.8MM,R/A,AMP	J515
291000025006	CON;HDR,MA,25P*2,.8MM,R/A,SMT	J513
291000020202	CON;HDR,MA,2P*1,1.25,R/A,SMT,HIROSE	J2
291000010404	CON;HDR,MA,4P,1.25MM,H=3.6,ST,SMT	J2
331030006018	CON;HDR,MA,6P*1,2.0,ST,GLD,SUYIN	PJ4
291000011410	CON;HDR,MA,7P*2,1.27MM,ST,H3MM,SMT	J4
291000023202	CON;HDR,MA16P*2,1.27MM,R/A,SMT	J1
291000251441	CON;IC CARD,FM,72P*2,.6MM,H3MM,SMT	U509
331870004005	CON;MINI DIN,4P,R/A,W/GROUNDING,F6S	J502
331870006013	CON;MINI DIN,6P,R/A,W/GROUND,73156	J507
331810006010	CON;MODULAR JACK,FM,6P4C,R/A,GR	
291000810204	CON;PHONE JACK,2P,H=8.5,R/A,SMT,FRE	J1
291000810805	CON;PHONE JACK,8P,H=12.59,R/A,RJ45,C100	J504
331910003020	CON;POWER JACK,3P,D=2.5,MARLIN	PJ501
331840005007	CON;STEREO JACK,5P,R/A,W9.1,LGY2313	J501,J508,J510
331000008026	CON;USB,FM,H=13.62,R/A,4P*2,72309-6220B	J509
291000410201	CON;WFR,MA,2P,1.25,ST,SMT/MB	J2
291000410301	CON;WFR,MA,3P,1.25,ST,SMT/MB	J512
346670000005	CONDUCTIVE SHEET; LCD,CONN,7521	
345669800003	CONDUCTIVE TAPE;EASYSTART,7321	
345669600053	CONDUCTIVE TAPE;PCMCIA,RACE	
313000150030	CORE;180OHM/100MH,25.5*23.5*32.5*10	

9.Spare parts list(3)

Part Number	Description	Location(s)
441669800032	COVER ASSY; M/B,14.1",7321,ID3	
340670020009	COVER ASSY;CPU,7521P	
340670000031	COVER ASSY;EASY STAR,ID3,CHAMP,7521	
340669800001	COVER ASSY;ID3,CHAMP,7321	
340670000015	COVER ASSY;LCD,ID2,CHAMP,7521	
344670000051	COVER HINGE;ID2,CHAMP,7521	
344670000013	COVER;MODEM,7521	
272625101401	CP;100P*4,8P,50V ,10%,1206,NPO,SMT	CA1,CA2
272625470401	CP;47P*4 ,8P,50V ,10%,1206,NPO,SMT	CA3,CA4,CA5,CA6,CP2
291006214411	DIMM SOCKET;144P,.8MM,AMP353870,SMT	J7
288100032013	DIODE;BAS32L,VRRM75V,MELF,SOD-80	PD1,PD5,PD6,PD8
288100701002	DIODE;BAV70LT1,70V,225MW,SOT-23	D13,D502
288100056003	DIODE;BAW56,70V,215MA,SOT-23	D1,D8,Q42
288101004024	DIODE;EC10QS04,RECT,40V,1A,CHIP,SMT	PD12,PD14,PD15,PD4
288100805001	DIODE;ESD0805A,1CH,15KV,0805,2P	D3
288100050001	DIODE;RB050L-40,40V,3A,SMT	PD10,PD11,PD13,PD2,P
288104148001	DIODE;RLS4148,200MA,500MW,MELF,SMT	D14,D15,D2,D501
288100020001	DIODE;RLZ20C,ZENER,19.23V,5%,SMT	PD503
288100024002	DIODE;RLZ24D,ZENER,23.63V,5%,SMT	PD501
288100056005	DIODE;UDZ5.6B,ZENER,5.6V,UMD2,SMT	D11
523499999026	DVD ASSY OPTION;8X,7521	
523430061901	DVD DRIVE;8X,SDR-081,H=12.7,QUANTA	
451670000101	DVD ME KIT;8X,SDR-081,7521	
523467000004	DVD ROM ASSY;8X SDR081,7521	
272601107506	EC;100U ,6.3V,M,9.3*3.6,-55~105'C	C8,C98,C99

Part Number	Description	Location(s)
312271006358	EC;100U,25V,RA,M,D6.3*7,SGX,SANYO	PC10
312271005357	EC;10U,25V,20%,RA,6.3*6.8,+105℃,SYO	PC507,PC515,PC516
312272205359	EC;22U ,20V,20%,RA,D6.3*5,OS-CON	PC511
312273306154	EC;330U ,4V ,+-20%,100*5,SP.OS-CON	PC501,PC505,PC508,PC5
312270687161	EC;680U,6.3V,20%D10,FUJITSU-FPCAP	PC502,PC503
227670000001	END CAP;7521	
227670000003	END CAP;AK BOX,7521	
227670000004	END CAP;BATTERY,7521	
227670000002	END CAP;MANUAL,7521	
481669800002	F/W ASSY;KBD CTRL,7321	U30
481669800001	F/W ASSY;SYS/VGA BIOS,7321	U27
523411442048	FD DRIVE;1.44M,3.5",D353G,R69-2015	
523467005001	FDD ASSY;7521 ID3 C	
273000150002	FERRIET CHIP;120OHM/100MHZ,2012,SMT	L1,L3
273000610013	FERRITE ARRAY;120OHM100MHZ,3216,MAG	FA1,FA2,FA3
273000150013	FERRITE CHIP;120OHM/100MHZ,2012,6A	L16,L25,L26,L27,L36,L5
273000150013	FERRITE CHIP;120OHM/100MHZ,2012,6A	PL1-4
273000150031	FERRITE CHIP;120OHM/100MHZ,2012,SMT	L1
273000150031	FERRITE CHIP;120OHM/100MHZ,2012,SMT	L501
273000150031	FERRITE CHIP;120OHM/100MHZ,2012,SMT	L1,2,500
273000130039	FERRITE CHIP;130OHM/100MHZ,1608,SMT	L10,L11,L12,L14,L15,L34
273000130038	FERRITE CHIP;600OHM/100MHZ,1608,SMT	L1,L17,L18,L19,L2,L20,L
346664900010	FILM;LCD PROTEC,.14.2",235*300,5027	
342670010001	FINGER;EMI GROUNDING SMD FINGER,H=5MM,7	TP24,TP501
288003600001	FIR;HSDL3600#007,FRONT VIEW,10P,SMT	U501

9.Spare parts list(4)

Part Number	Description	Location(s)
295000010028	FUSE;0.14A/60V,POLY SWITCH,PTC,SMD	PF1
295000010008	FUSE;1.1A,POLY SWITCH,1812,SMT	F2
295000010105	FUSE;1A,NORMAL,1206,SMT	F4
295000010029	FUSE;FAST,.75A,63V,1206,THIN FILM	PF1
295000010016	FUSE;NORMAL,6.5A/32VDC,3216,SMT	PF501
295000010020	FUSE;NORMAL,7A/24VDC,1206,SMT	PF3
345669600055	GASCKET;TV-OUT,RACE	
345670020010	GASKET;10*1*25,7521P	
345669800001	GASKET;5x5x10,7321	
345669800002	GASKET;7x1x9,7321	
345669600047	GASKET;FDD,LONG,RACE	
345669600048	GASKET;FDD,SHORT,RACE	
345669600006	GASKET;IO-PS2,RACE	
345669600013	GASKET;LAN,RACE	
345669600041	GASKET;LVDS,9X6X10,RACE	
345669600043	GASKET;MIC,5X5X19,RACE	
345669600042	GASKET;USB,10X15X0.3,RACE	
345669600005	GASKET;USB,RACE	
451670040004	HDD ME KIT;7521 ID2 C	
451669800093	HEATSINK ME KIT;7321	
340669800006	HEATSINK ASSY;CPU,7321	
340670000016	HOUSING ASSY;LCD,ID2,CHAMP,7521	
340670020002	HOUSING ASSY;TV-OUT;7521P	
451669800032	HOUSING KIT;14.1",7321,ID3	
344670000054	HOUSING;FDD-HDD,ID2,CHAMP,7521	

Part Number	Description	Location(s)
344600000239	IC CARD CON PART;72P*2,22RRF	
331650046203	IC SOCKET;462P,ZIF,ZIFPGAF	U503
282574014004	IC;74AHC14,HEX INVERTER,TSSOP,14P	U512
282574186002	IC;74AHCT1G86,SINGLE,XOR,SOT23,SMT	U9
282074338402	IC;74CBTD3384,10 BIT BUS SW,TSOP-24	U510
282071338302	IC;74CBTH3383,BUS EXCHG SW,TSSOP-24	U34
282574164002	IC;74VHC164,SIPO REGISTER,TSSOP,14P	U31
284580227001	IC;80227,LAN-PHY,TQFP,64P,SMT	U5
284501022001	IC;ADM1022,TEMPERATURE MTR,SSOP,16P	U508
286203311001	IC;ADM3311E,RS-232,TSSOP,28P	U1
286303301001	IC;ADP3301AR-5,.8%,REG.,SO,8P	U17
286308800001	IC;AME8800,0.3A,1.5%,LDO,SOT89	U505,U517
286308800003	IC;AME8800,0.3A,3.3V,REG,SOT89	U511
284507005001	IC;CH7005C,TV ENCODER,3/5V,PQFP,44P	U6
284504299001	IC;CS4299-JQ,AC97 CODEC,TQFP,48P	U10
283466570001	IC;EEPROM,9346,64*16 BITS,SO8,SMT	U20
283450083001	IC;FLASH,256K*8-70,PLCC32,ST39SF020	
284583437003	IC;H8/F3437S,KBD CTRL,TQFP,100P,HITACHI	
284509248020	IC;ICS9248-189,SYSTEM CLK,SSOP,48P	U8
286300811001	IC;IM811,MICROPWR VOL,SOT23-4	U32
286100393004	IC;LMV393,DUAL COMPARTOR,SSOP,8P	PU2
286302951015	IC;LP2951ACM,VOLTAGE REGULATOR,SO	U19
286317097001	IC;LTC1709EG-7,PWM CTRL,SSOP ,36P	PU11
286301632002	IC;MAX1632CAI,PWM CTRL,SSOP,28P	PU5
286104173001	IC;MAX4173F,I-SENSE AMP,SOT23,6P	PU1

9.Spare parts list(5)

Part Number	Description	Location(s)
284501284002	IC;PACS1284-02Q/T,TERMIN NET,QSOP28	U2
284501420003	IC;PCI1420,PCI/CARDBUS,TQFP,208P	U504
286309701001	IC;RT9701,POWER DISTRI SW,SOT23-5,5P,RI	U33
286300431014	IC;SC431LCSK-.5,.5%,ADJ REG,SOT23	PQ14,PQ4
283766980001	IC;SDRAM,2M*16*4-133,TSOP,54P,7321	U15,U16,U22,U23,U25,U
286300594001	IC;TL594C,PWM CONTROL,SO,16P	PU8
286100202001	IC;TPA0202,AUDIO AMP,2W,TSSOP,24P	U3
286302216001	IC;TPS2216,CARDBUS PWM CTRL,SSOP30P	U14
284508231002	IC;VT8231,PCI/ISA,BGA,376P,SMT	U24
284508362001	IC;VT8362,NORTHBRIOGE,BGA,552P	U21
273000120128	INDUCTOR;10nH,10%,0805,SMT	L512,L513,L514,L515,L5
273000990012	INDUCTOR;10UH,CDRH127,SUMIDA,SMT	PL501
273000990031	INDUCTOR;10UH,CDRH127B,SUMIDA,SMT	PL1
273000990021	INDUCTOR;33uH,CDRH124,SMT	PL504
340669800005	INSULATOR ASSY;CDROM,7321	
346669600054	INSULATOR;DC JACK,RACE	
346669600032	INSULATOR;E-MAIL LED,RACE	
346669600071	INSULATOR;FDD BACK,RACE	
346669600014	INSULATOR;INVERTER,REDSEA	
346669600041	INSULATOR;MEMORY,RACE	
346669800009	INSULATOR;MICROPHONE,7321	
346669800001	INSULATOR;PCMCIA,7321	
346669800007	INSULATOR;QSB,7321	
346670900002	INSULATOR;TP BUTTON,7521T	
531020237255	KBD;87,GR,K982318S1,W/EMI,7521	

Part Number	Description	Location(s)
451669800056	LABEL KIT;N-B,7321,14",MSL	
242600000380	LABEL;10*8MM,BIOS,HI-TEMP 260	
242600000380	LABEL;10*8MM,BIOS,HI-TEMP 260	
242662300009	LABEL;25*10MM,3020F	
242600000385	LABEL;27*10,LAN ID BAR CODE	
242668300017	LABEL;4*3MM,HI-TEMP,260'C,HOPE	
242669800003	LABEL;AGENCY-GLOBAL,MSL,7321	
242600000157	LABEL;BAR CODE,125*65,COMMON	
242600000364	LABEL;BLANK,6*6MM,HI-TEMP	REV LABEL
242600000364	LABEL;BLANK,6*6MM,HI-TEMP	
242600000364	LABEL;BLANK,6*6MM,HI-TEMP	REV LABEL
242600000364	LABEL;BLANK,6*6MM,HI-TEMP	
242664800013	LABEL;CAUTION,INVERT BD,PITCHING	
242600000099	LABEL;MODEL,5M,MITAC	
242600000195	LABEL;SOFTWARE,INSYDE BIOS-M	
242668800033	LABEL;WINDOWS ME,CARTON,ORION2	
242669400013	LABEL;WINDOWS ME,N/B,VILLA	
441669800003	LCD ASSY;TFT,HYUN,14.1",7321,ID3	
451669800003	LCD ME KIT;TFT,HYUN,14.1",7321,ID3	
413000020236	LCD;HT14X13,TFT,14.1",XGA,HYUNDAI	
294011200016	LED;GREEN,H0.8,0603,CL-190G,SMT	D1-6
294011200016	LED;GREEN,H0.8,0603,CL-190G,SMT	D3,4
294011200043	LED;RE/GR,H0.8,L1.9,W1.6,19-22SRVGC	D9
294011200042	LED;ROUND,D5MM,60 ANGLE,GRN/YEL	D8
416266980903	LT PLATFORM OPTION;14.1",7321 ID3	

9.Spare parts list(6)

Part Number	Description	Location(s)
416266980007	LT PLATFORM;TFT,HYUN,14.1",7321,ID3	
561566980011	MANUAL KIT;GR,7321,N-B	
561566980108	MANUAL;USER'S,GR,7321,N-B	
421670000031	MICROPHONE ASSY;LCD,7521,MSL	
412999900007	MODEM OPTION;UNIVERSAL,MDC,7521	
242670000003	NAMEPLATE;N-B,7521	
461670000003	PACKING KIT;N-B,7521	
221670050001	PARTITION;AK BOX,7521	
412155600048	PCB ASSY;MDM,56K,UNIV,W/O Y-CAP,7521	
222600020049	PE BAG;50*70MM,W/SEAL,COMMON	
222667220003	PE BAG;L560XW345,CERES	
222670000001	PE BUBBLE BAG;BATTERY,7521	
273000150033	PHASEOUT;FERRITE CHIP,120OHM/100MHZ	L21,L22,L33,L39,L40,L4
340669600004	PLATE ASSY;TOUCHPAD,REDSEA	
411669800004	PWA;PWA-7321,M/B,ID3,MTC	
411669800003	PWA;PWA-7321,M/B,SMT	
411669800002	PWA;PWA-7321,M/B,T/U	
411670000018	PWA;PWA-7521 ID3 C,QSB TRANS BD	
411670000031	PWA;PWA-7521,CHARGER TRANS BD	
411670000029	PWA;PWA-7521,HDD/FDD BD,SMT	
411670000028	PWA;PWA-7521,HDD/FDD BD,T/U	
411670000011	PWA;PWA-7521,IQSB TRANS BD,SMT	
411670000010	PWA;PWA-7521,IQSB TRANS BD,T/U	
411670800013	PWA;PWA-7521N,INVERTER BD,OZ965,T/U	
411670900005	PWA;PWA-7521T,MDC TRANS BD,SMT	

Part Number	Description	Location(s)
411670900004	PWA;PWA-7521T,MDC TRANS BD,T/U	
332810000034	PWR CORD;250V/2.5A,2P,BLK,EU,175CM	
271045037101	RES;.003 ,1W ,1% ,2512,SMT	PR22,PR59
271045157101	RES;.015 ,1W ,1% ,2512,SMT	PR1,PR14
271045207101	RES;.02 ,1W ,1% ,2512,SMT	PR2,PR31
271002000301	RES;0 ,1/10W,5% ,0805,SMT	L13,L3,L52,L522,L54,R5
271002000301	RES;0 ,1/10W,5% ,0805,SMT	R1-4
271071000002	RES;0 ,1/16W,0603,SMT	L44,L59,PR17,PR20,PR4
271071000002	RES;0 ,1/16W,0603,SMT	R500
271071152302	RES;1.5K ,1/16W,5% ,0603,SMT	R124,R125,R173,R275,R
271071100101	RES;10 ,1/16W,1% ,0603,SMT	PR51
271071100302	RES;10 ,1/16W,5% ,0603,SMT	PR6,R198,R56,R577,R98
271071102211	RES;10.2K,1/16W,1% ,0603,SMT	PR28
271002101301	RES;100 ,1/10W,5% ,0805,SMT	R20,21
271071101101	RES;100 ,1/16W,1% ,0603,SMT	R532,R533,R534,R535,R
271071101301	RES;100 ,1/16W,5% ,0603,SMT	R283,R563
271071104701	RES;100K ,1/16W,.1%,0603,SMT	PR1
271071104101	RES;100K ,1/16W,1% ,0603,SMT	PR9
271071104302	RES;100K ,1/16W,5% ,0603,SMT	PR11,PR25,PR39,PR43,P
271071103101	RES;10K ,1/16W,1% ,0603,SMT	PR29,PR40,PR47,R216,R
271071103302	RES;10K ,1/16W,5% ,0603,SMT	PR15,PR16,PR50,R100,R
271071118271	RES;11.8K,1/16W,0.1%,0603,SMT	PR33
271071121301	RES;120 ,1/16W,5% ,0603,SMT	R157,R166,R167,R168
271071124301	RES;120K ,1/16W,5% ,0603,SMT	PR61
271071141102	RES;140 ,1/16W,1% ,0603,SMT	R165

9.Spare parts list(7)

Part Number	Description	Location(s)
271071143701	RES;14K ,1/16W,0.1% ,0603,SMT	PR13
271071153301	RES;15K ,1/16W,5% ,0603,SMT	R171,R189,R190,R191,R
271071163101	RES;16K ,1/16W,1% ,0603,SMT	R202
271071178311	RES;178K ,1/16W,1% ,0603,SMT	PR507
271002102301	RES;1K ,1/10W,5% ,0805,SMT	PR27
271071102302	RES;1K ,1/16W,5% ,0603,SMT	R22,R236,R255,R289,R3
271071105101	RES;1M ,1/16W,1% ,0603,SMT	PR64
271071105301	RES;1M ,1/16W,5% ,0603,SMT	PR509,PR56,PR63,R142,
271071222302	RES;2.2K ,1/16W,5% ,0603,SMT	R547
271071222302	RES;2.2K ,1/16W,5% ,0603,SMT	R24,25
271071249111	RES;2.49K,1/16W,1% ,0603,SMT	PR42
271071272101	RES;2.7K ,1/16W,1% ,0603,SMT	PR26
271071272301	RES;2.7K ,1/16W,5% ,0603,SMT	R140,R60
271071203701	RES;20K ,1/16W,.1%,0603,SMT	PR500
271071203101	RES;20K ,1/16W,1% ,0603,SMT	PR23,R550
271071203302	RES;20K ,1/16W,5% ,0603,SMT	R37,R75
271071221302	RES;22 ,1/16W,5% ,0603,SMT	R101,R102,R103,R104,R
271071221302	RES;22 ,1/16W,5% ,0603,SMT	R22,23
271071224301	RES;220K ,1/16W,5% ,0603,SMT	R641
271071221311	RES;221K ,1/16W,1% ,0603,SMT	PR67
271071226311	RES;226K ,1/16W,1% ,0603,SMT	PR12
271071223301	RES;22K ,1/16W,5% ,0603,IBM ONLY	R36,R76
271071223302	RES;22K ,1/16W,5% ,0603,SMT	PR21
271071249811	RES;24.9 ,1/16W,1% ,0603,SMT	R524,R525,R615,R616
271071249311	RES;249K ,1/16W,1% ,0603,SMT	PR44

Part Number	Description	Location(s)
271071202102	RES;2K ,1/16W,1% ,0603,SMT	R219,R221
271071332302	RES;3.3K ,1/16W,5% ,0603,SMT	R106,R111
271071301011	RES;301 ,1/16W,1% ,0603,SMT	R536,R82
271071301371	RES;301K ,1/16W,.1%,0603,SMT	PR2
271071330302	RES;33 ,1/16W,5% ,0603,SMT	R10,R209,R9
271071331301	RES;330 ,1/16W,5% ,0603,SMT	R19,11,12
271071334301	RES;330K ,1/16W,5% ,0603,SMT	R158,R33
271071333301	RES;33K ,1/16W,5% ,0603,SMT	PR19,PR506
271071302101	RES;3K ,1/16W,1% ,0603,SMT	PR524,R217
271013478301	RES;4.7 ,1/4W,5% ,1206,SMT	L38,L65,R20,R21
271002472301	RES;4.7K ,1/10W,5% ,0805,SMT	PR5
271071472302	RES;4.7K ,1/16W,5% ,0603,SMT	PR45,PR46,PR8,R129,R1
271071499171	RES;4.99K,1/16W,0.1%,0603,SMT	PR34
271071499171	RES;4.99K,1/16W,0.1%,0603,SMT	PR501
271071402811	RES;40.2 ,1/16W,1% ,0603,SMT	R123,R128
271071433301	RES;43K ,1/16W,5% ,0603,SMT	R160
271071470301	RES;47 ,1/16W,5% ,0603,SMT	R161,R162
271071471302	RES;470 ,1/16W,5% ,0603,SMT	R257
271071471302	RES;470 ,1/16W,5% ,0603,SMT	R7-12
271071474301	RES;470K ,1/16W,5% ,0603,SMT	PR60,R208,R278,R513,R
271071473101	RES;47K ,1/16W,1% ,0603,SMT	PR37,PR504,R290
271071473301	RES;47K ,1/16W,5% ,0603,SMT	R130,R62
271071536101	RES;5.36K,1/16W,1% ,0603,SMT	R569
271071562301	RES;5.6K ,1/16W,5% ,0603,SMT	R234,R261
271071565301	RES;5.6M ,1/16W,5% ,0603,SMT	PR38

9.Spare parts list(8)

Part Number	Description	Location(s)
271071510101	RES;51 ,1/16W,1% ,0603,SMT	PR522,R528,R529
271071560301	RES;56 ,1/16W,5% ,0603,SMT	R543,R544
271071564301	RES;560K ,1/16W,5% ,0603,SMT	R32
271071576311	RES;576K ,1/16W,1% ,0603,SMT	PR36
271071619111	RES;6.19K,1/16W,1% ,0603,SMT	PR41
271071682301	RES;6.8K ,1/16W,5% ,0603,SMT	R1,R108,R110,R2,R3,R7
271071604811	RES;60.4 ,1/16W,1% ,0603,SMT	R537,R538,R558,R567
271071604311	RES;604K ,1/16W,1% ,0603,SMT	PR10
271071681301	RES;680 ,1/16W,5% ,0603,SMT	R109
271071681301	RES;680 ,1/16W,5% ,0603,SMT	R13
271071750101	RES;75 ,1/16W,1% ,0603,SMT	R514,R515,R516,R517
271071822301	RES;8.2K ,1/16W,5% ,0603,SMT	R28,R59
271071806211	RES;80.6K,1/16W,1% ,0603,SMT	PR24
271071976311	RES;976K ,1/16W,1% ,0603,SMT	PR35
271611152301	RP;1.5K*4,8P ,1/16W,5% ,0612,SMT	RP26,RP4,RP58
271571100301	RP;10*8 ,16P ,1/16W,5% ,1606,SMT	RP21,RP23,RP24,RP27,R
271611104301	RP;100K*4,8P ,1/16W,5% ,0612,SMT	RP12
271611103301	RP;10K*4 ,8P ,1/16W,5% ,0612,SMT	RP19,RP44,RP57,RP6,RP
271621103303	RP;10K*8 ,10P,1/16W,5% ,1206,SMT,TF	RP49,RP50,RP509,RP511
271621103302	RP;10K*8 ,10P,1/32W,5% ,1206,SMT	RP37,RP38,RP39,RP46
271611153301	RP;15K*4 ,8P ,1/16W,5% ,0612,SMT	RP1
271621102302	RP;1K*8 ,10P,1/32W,5% ,1206,SMT	RP7
271611220301	RP;22*4 ,8P ,1/16W,5% ,0612,SMT	RP22,RP25,RP5,RP510
271611330301	RP;33*4 ,8P ,1/16W,5% ,0612,SMT	RP55
271571330301	RP;33*8 ,16P ,1/16W,5% ,1606,SMT	RP30,RP35,RP43,RP51,R

Part Number	Description	Location(s)
271611472301	RP;4.7K*4,8P ,1/16W,5% ,0612,SMT	RP11,RP29,RP3,RP31,RP
271621472302	RP;4.7K*8,10P,1/32W,5% ,1206,SMT	RP32,RP36,RP48,RP52
271621433301	RP;43K*8 ,10P,1/16W,5% ,1206,SMT	RP508
271611562301	RP;5.6K*4,8P ,1/16W,5% ,0612,SMT	RP9
271611750301	RP;75*4 ,8P ,1/16W,5% ,0612,SMT	RP18,RP2
271621820302	RP;820*4 ,8P,1/32W,5% ,1206,SMT	RP506,RP507
271621820301	RP;820*8 ,10P,1/32W,5% ,1206,SMT	RP14
345666600003	RUBBER;DOWN,LCD,TITAN	
345669600054	RUBBER;HDD_PCBA,RACE	
565166980001	S/W;CD ROM,SYSTEM DRIVER,7321	
565180626001	S/W;CD*1,DVD,WIN-DVD,INTERVIDEO	
371102030301	SCREW;M2L3,FLT(+),NIB/NLK	
371102030303	SCREW;M2L3,K-HEAD(+),NIW/NLK	
371102030303	SCREW;M2L3,K-HEAD(+),NIW/NLK	
371102030303	SCREW;M2L3,K-HEAD(+),NIW/NLK	
371102030601	SCREW;M2L6,K-HEAD(+),NIB/NLK	
371103030602	SCREW;M3L6,K-HEAD(+),NIB/NLK	
340669600019	SHELDING ASSY;HDD,RACE	
340670020010	SHIELDING ASSY;BOTTOM,7521P	
346669800006	SHIELDING;MB,27x55,7321	
346669800005	SHIELDING;MB,38x70,7321	
561860000022	SINGLE PAGE;GN,NOTE FOR BATTERY&LCD	
361200003025	SOLDER PASTE;RMA-010-FP	
346669600052	SPACER;HDD/FDD PCB,RACE	
346670500008	SPACER;SOCKET 462,TETRA	

9.Spare parts list(9)

Part Number	Description	Location(s)
370102611802	SPC-SCREW;M2.6L18,K-HD,NIB/NLK	
370102610405	SPC-SCREW;M2.6L4,NIW,K-HD,t=0.8,NLK	
370102610405	SPC-SCREW;M2.6L4,NIW,K-HD,t=0.8,NLK	
370102610405	SPC-SCREW;M2.6L4,NIW,K-HD,t=0.8,NLK	
370102610603	SPC-SCREW;M2.6L6,K-HD,NIB/NLK	
370102610603	SPC-SCREW;M2.6L6,K-HD,NIB/NLK	
370102610804	SPC-SCREW;M2.6L8,K-HD,t=0.8,NIB/NLK	
370102610804	SPC-SCREW;M2.6L8,K-HD,t=0.8,NIB/NLK	
370102010204	SPC-SCREW;M2L2,NIW/NLK,K-HD	
370102010256	SPC-SCREW;M2L2.5,K-HD(t0.5) NLK,NIW	
370102010253	SPC-SCREW;M2L2.5,NIW/NLK,HD07	
370102020301	SPC-SCREW;M2L3,NIW,K-HEAD	
370103010405	SPC-SCREW;M3L4,NIW,K-HD,T0.3	
340669600003	SPEAKER ASSY;REDSEA	
345669600007	SPOGE; CPU,RACE	
341670500002	SPRING SCREW;HEATSINK,TETRA	
341670900001	SPRING;MDC TRANS/B,7521T	
342669600011	STANDOFF;M2DP2H4L5,NIW,RACE	
344669600037	STOPPER;CUP SOCKET,RACE	
295000020002	SURGE PROTECTOR;P2600SB,2P,DO-214AA	R2
297120101005	SW;DIP,SPST,8P,50VDC,.1A,SMT,DHS4S	SW3
297030105001	SW;PUSH BUTTON,SPSD,48V/.05A,SMT	SW1
297040101003	SW;PUSH BUTTON,SPST,.1A,30V,2P,SMT	SW1,2
337040100006	SW;PUSH BUTTON,SPST,12V50mA,R/A,RAC	SW3
297040100002	SW;PUSH BUTTON,SPST,4P,15V/20mA,S&T	SW1-5

Part Number	Description	Location(s)
297040100002	SW;PUSH BUTTON,SPST,4P,15V/20mA,S&T	SW500
297030102001	SW;TOGGLE,SPST,5V/0.2mA,H10.7MM,SMT	SW2
346669600006	THERMALPAD;SOCKET,RACE	
340666600018	TILT UNIT;L,TITAN	
340666600017	TILT UNIT;R,TITAN	
442164900006	TOUCH PAD MODULE;TM41PUM220-2	
288227002001	TRANS;2N7002LT1,N-CHANNEL FET	PQ12,PQ17,PQ501,PQ7,(
288227002001	TRANS;2N7002LT1,N-CHANNEL FET	Q1,2
288227002006	TRANS;2N7002LT1,N-CHANNEL FET,ESD	PQ21,PQ22,PQ5
288200144002	TRANS;DTA144WK,PNP,SMT	PQ19
288200144003	TRANS;DTC144TKA,N-MOSFET,SOT-23	Q10,Q37,Q38,Q39,Q41,Q
288200144001	TRANS;DTC144WK,NPN,SOT-23,SMT	PQ11,Q1,Q2,Q23,Q27,Q2
288200301001	TRANS;FDV301N,N-CHANNEL,SOT23	Q3,Q4,Q5,Q6,Q7,Q8,Q9
288207807001	TRANS;IRF7807(A),N-MOS,.025OHM,SO8	PU10,PU14,PU15,PU9
288202222001	TRANS;MMBT2222AL,NPN,TO236AB	PQ18
288203904010	TRANS;MMBT3904L,NPN,Tr35NS,TO236AB	Q29,Q34,Q503,Q504,Q50
288207002001	TRANS;NDC7002N,N-MOSFET,SSOT-6	PQ16
288200352001	TRANS;NDS352P,DMOS,TO-236AB	Q32
288202301001	TRANS;SI2301DS,P-MOSFET,SOT-23	Q21,Q22,Q506
288204416001	TRANS;Si4416DY,N-MOSFET,.028OHM,SO8	PQ2,PQ6
288204788001	TRANS;SI4788CY,P-MOS,5A1.8~5.5V,SO8	U35,U516
288204800001	TRANS;SI4800DY,N-MOS,.0185OHM,SO8	PQ13,Q501
288204832001	TRANS;SI4832DY,N-MOSFET,.028OHM,SO8	PQ1,PQ3,PU12,PU13,PU
288204835001	TRANS;SI4835DY,PMOS,6A/30V,.035,SO8	PQ20,PU18,PU6
288204925001	TRANS;SI4925DY,P-MOSFET,SO-8	PU7

9.Spare parts list(10)

Part Number	Description	Location(s)
273001050020	TRANSFORMER;10/100 BASE,H1102,SMT	U502
373101712351	T-SCREW;B,M1.7,L2.35,K-HD,2,NIB	
271911103902	VR;10K ,20%,.05W,XV0102GPH1N-9391	VR501
346669600015	WASHER;INVERTER,REDSEA	
421669800005	WIRE ASSY;INVERTER,7321	
421669800002	WIRE ASSY;LCD,HY,7321	
274011431408	XTAL;14.318M,50PPM,32PF,7*5,4P,SMT	X4
274011600408	XTAL;16MHZ,16PF,50PPM,8*4.5,2P	X7
274012457406	XTAL;24.576MHZ,16PF,50PPM,8*4.5,2P	X5
274012500401	XTAL;25MHZ,30PPM,18PF,4P,SMT	X2
274013276103	XTAL;32.768KHZ,20PPM,12.5PF,CM200	X6

MODEL : 7321 M/B
Revision : 0B

Power Plane

+VMAIN:	LP2951
VDD5:	H8, IMP811, AME8800 (U511)
VDD5S:	74VHC164, LED, LMV393, MAX4173F
VDD3:	VT8231 Resume Well, RTC, VT8321 MII
+12V:	Card Power Switch, ADP3301, LCD panel MOS, H8 12V
+5V:	CH7005C, MDC, Audio Codec, PIO, HDD, CDROM, FDD, CBTD3384, FAN, SYS BIOS, LED
+5V_STR:	VDD5 Switch Circuit (Q22), AMP, USB, Card Power Switch, Touchpad
+3V:	+2.5V (PQ13), AME8800 (U505), VT8362, VT8231, 1394, LCD Panel, EEPROM, Clock Generator, RS232, FIR, ADM1022, ADM809, Codec (Digital), 244 Buffer
+3V_STR:	AME8800 (U517), Memory, VT8231 USB Interface, U512, MDC, LAN-PHY, Card Power Switch, RS-232, Cardbus Controller
+2.5V:	VT8362, VT8362 (VGA, DAC, PLL...), CPU_VCCA
+2.5V_STR:	VT8362 Resume Well
+CPU_CORE:	CPU, VT8362

PCI Devices Resources

	IDSEL	DEVICE	Bus Master (REQ# & GNT#)	INT#
Cardbus	AD19	D8	0	INTB#
1394	AD22	D11	3	INTC#
LAN		D18, F0	4 (High)	
AUDIO		D17, F5,6		
USB		D17, F2		
N.B.		D0, D1		
S.B.		D17		

M/B Layout Arrangement

Component Layer		Normal Trace Width - Space:	5 - 6
Ground Layer	Ground Plane		
Inner 1 Layer		Trace Impedence:	60 ohm
Inner 2 Layer			
Power Layer	Power Plane		
Solder Layer			

Table of Content

Revision History

Revision	Date	Description
00	01/19/2001	1) Initial schematics release.
0A	03/21/2001	1) Change LAN PHY from ICS1893 to LSI80227. 2) Correct the LVDS PLL power from +3V to +2.5V. 3) GPI0, GPI8 pull high from +VCC_RTC to +VDD3. 4) SMBUS pull high from resistor array to single resistor. 5) Correct internal keyboard matrix from connector. 6) Correct the PS/2 connector shape. 7) Correct internal MIC connector shape. 8) Change cardbus controller GRST# from RC reset to PCIRST#. 9) Change Q502 power on signal from +5V to +3.3V. 10) Change Q20, Q505 from DTC144TKA to MMBT3904 with a 1.5K resistor. 11) Correct CKE pin arrangement from chipset side. 12) Fix cardbus controller pull high arrangement (RP504,505). 13) Change QSB keyboard matrix arrangement. 14) Change Line in Cap. from 1U to 4.7U. 15) Change DDCK, DDDA pull up from +5V to +3V. 16) Add 5 capcitators at screw hole, for EMI. 17) Add a extra 4.7 ohm with a 4.7U for AMP 5V. 18) Add H8_RSMRST at P95, change GREEN_LIGHT to PA2, and delete IQSB1#. 19) Reserve VGA_SUS pull-low.
0B	07/02/2001	1) Resume on 6/8. 2) Phase in STR schematics. 3) Phase in 2 phase CPU power swtiching circuit (LTC1709EG-7). 4) Change Panel ID to VGA Strapping. 5) Change VT8321 & H8 GPIO to follow other model design. 6) Change PowerOK timing for CPU_PWRGOOD faster than SYS_PWRGOOD.

DRAWN	DESIGN	CHECK	ISSUES

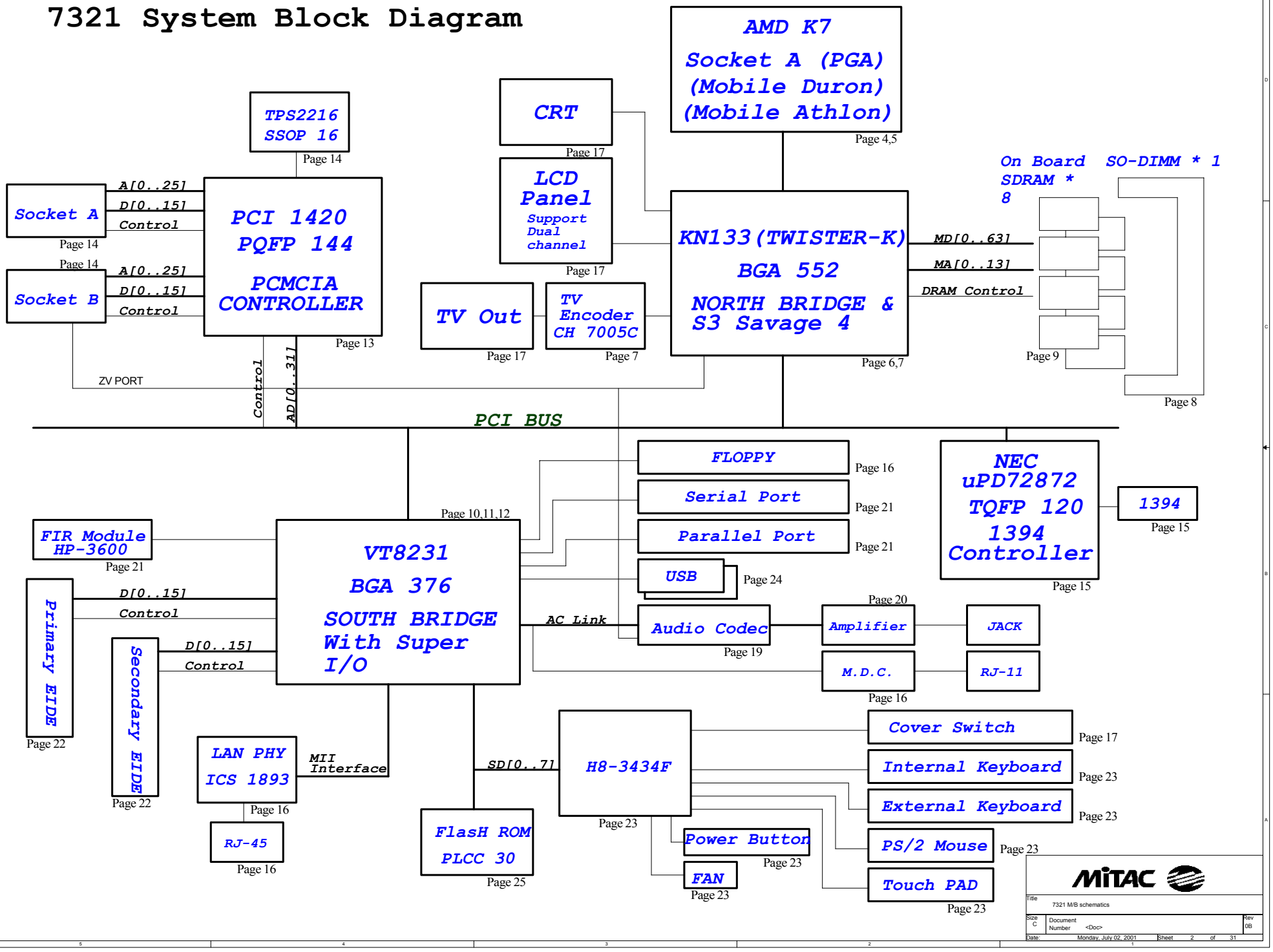
MiTAC

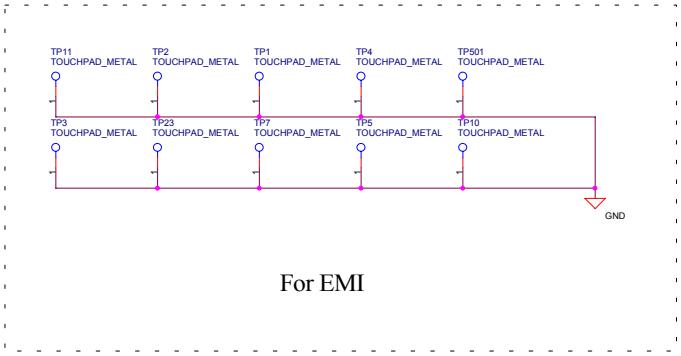
Title: 7321 M/B schematics

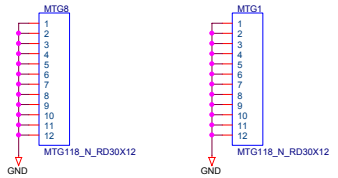
Size: C | Document Number: <Doc> | Rev: 0B

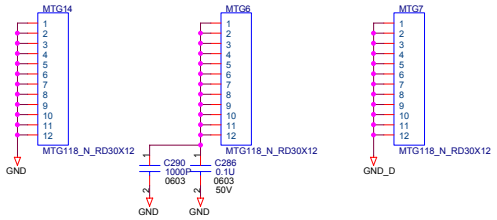
Date: Monday, July 02, 2001 | Sheet 1 of 31

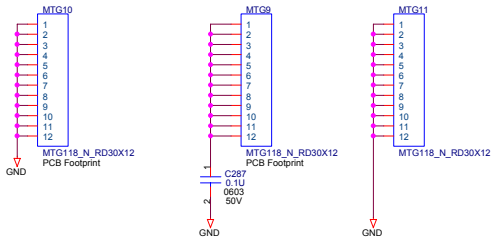
7321 System Block Diagram

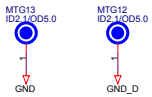


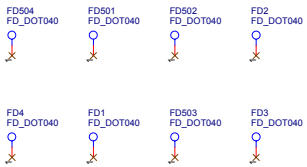












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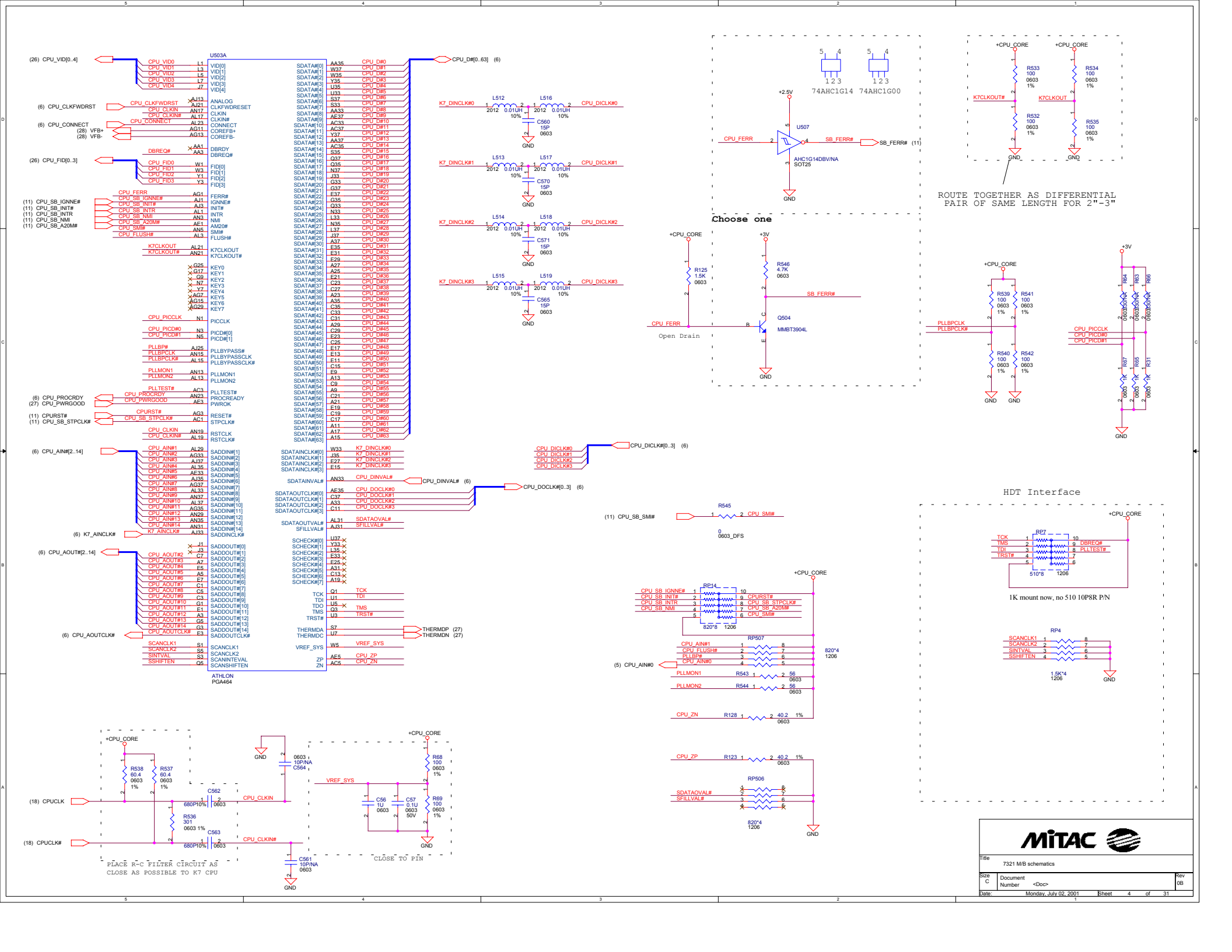
U503A
ATHLON
PGA464
74AHC1G14 74AHC1G00
U507
AHC1G14DBV/NA
SOT25
Choose one
Open Drain
ROUTE TOGETHER AS DIFFERENTIAL
PAIR OF SAME LENGTH FOR 2"-3"
HDT Interface
1K mount now, no 510 10P8R P/N
PLACE R-C FILTER CIRCUIT AS
CLOSE AS POSSIBLE TO K7 CPU
CLOSE TO PIN
MiTAC
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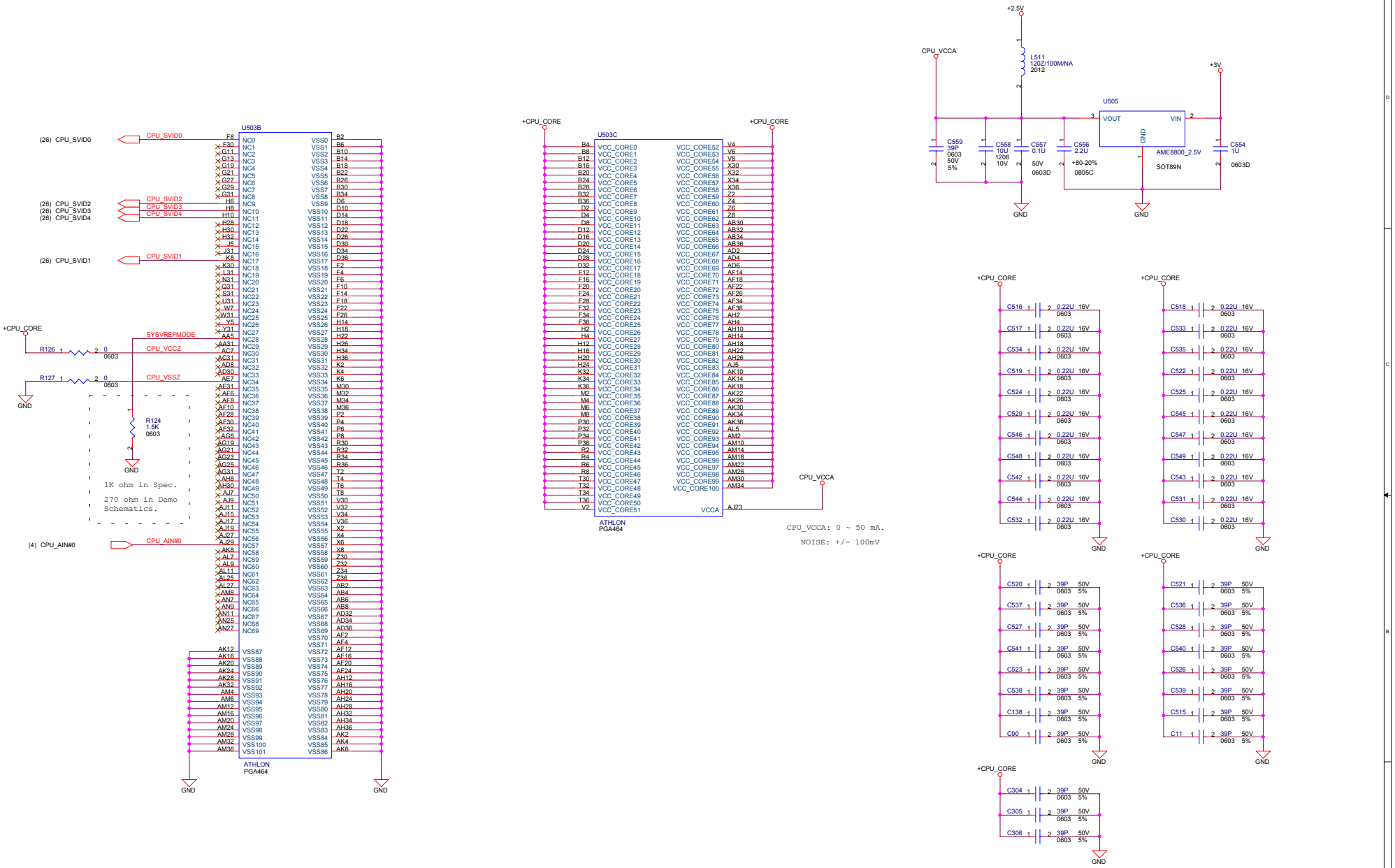

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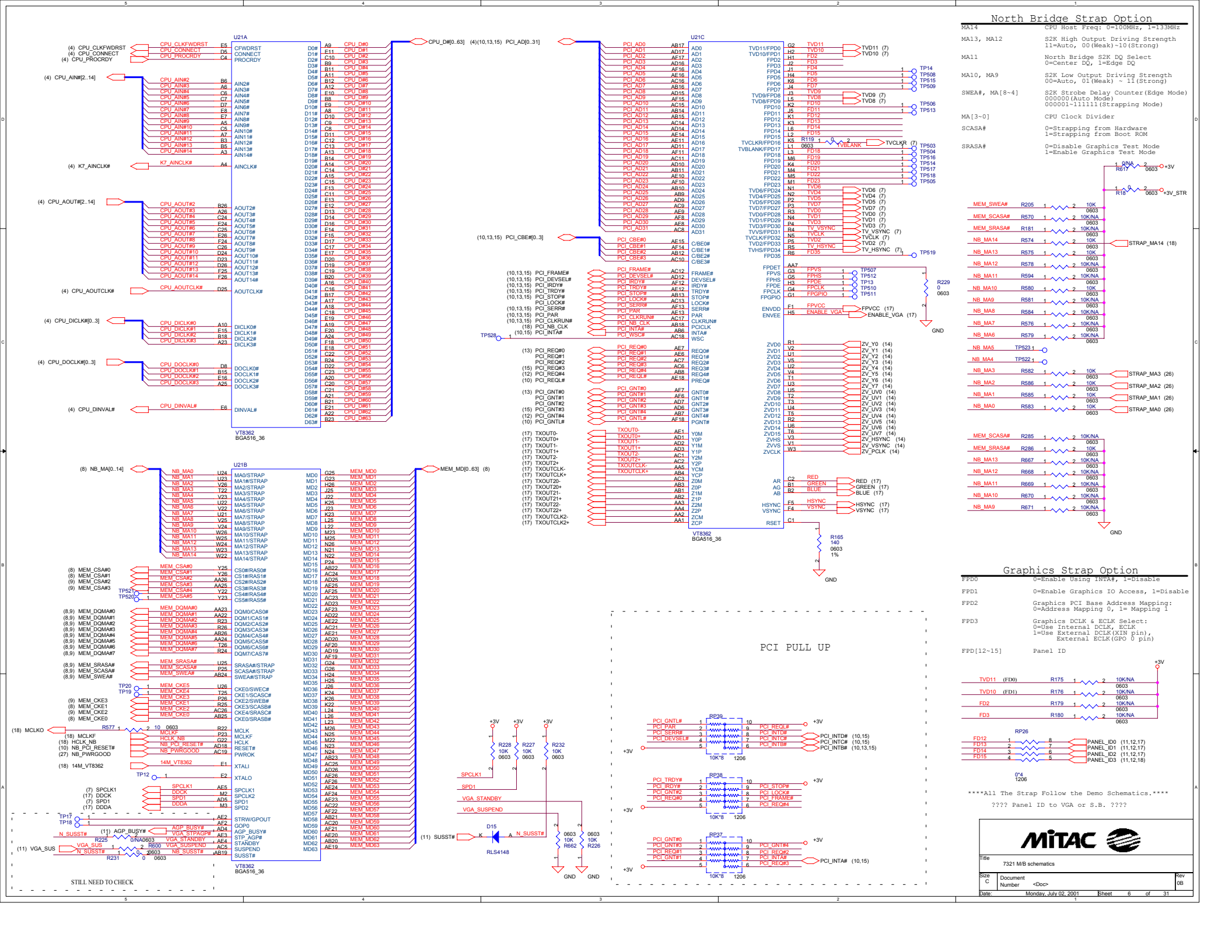
U21A
U21B
U21C
VT8362
BGA516_36
North Bridge Strap Option
MA14 CPU Host Freq: 0=100MHz, 1=133MHz
MA13, MA12 S2K High Output Driving Strength 11=Auto, 00(Weak)~10(Strong)
MA11 North Bridge S2K DQ Select 0=Center DQ, 1=Edge DQ
MA10, MA9 S2K Low Output Driving Strength 00=Auto, 01(Weak) ~ 11(Strong)
SWEA#, MA[8~4] S2K Strobe Delay Counter(Edge Mode) 000000(Auto Mode) 000001~111111(Strapping Mode)
MA[3~0] CPU Clock Divider
SCASA# 0=Strapping from Hardware 1=Strapping from Boot ROM
SRASA# 0=Disable Graphics Test Mode 1=Enable Graphics Test Mode
Graphics Strap Option
FPD0 0=Enable Using INTA#, 1=Disable
FPD1 0=Enable Graphics IO Access, 1=Disable
FPD2 Graphics PCI Base Address Mapping: 0=Address Mapping 0, 1= Mapping 1
FPD3 Graphics DCLK & ECLK Select: 0=Use Internal DCLK, ECLK 1=Use External DCLK(XIN pin), External ECLK(GPO 0 pin)
FPD[12~15] Panel ID
PCI PULL UP
****All The Strap Follow the Demo Schematics.****
???? Panel ID to VGA or S.B. ????
STILL NEED TO CHECK
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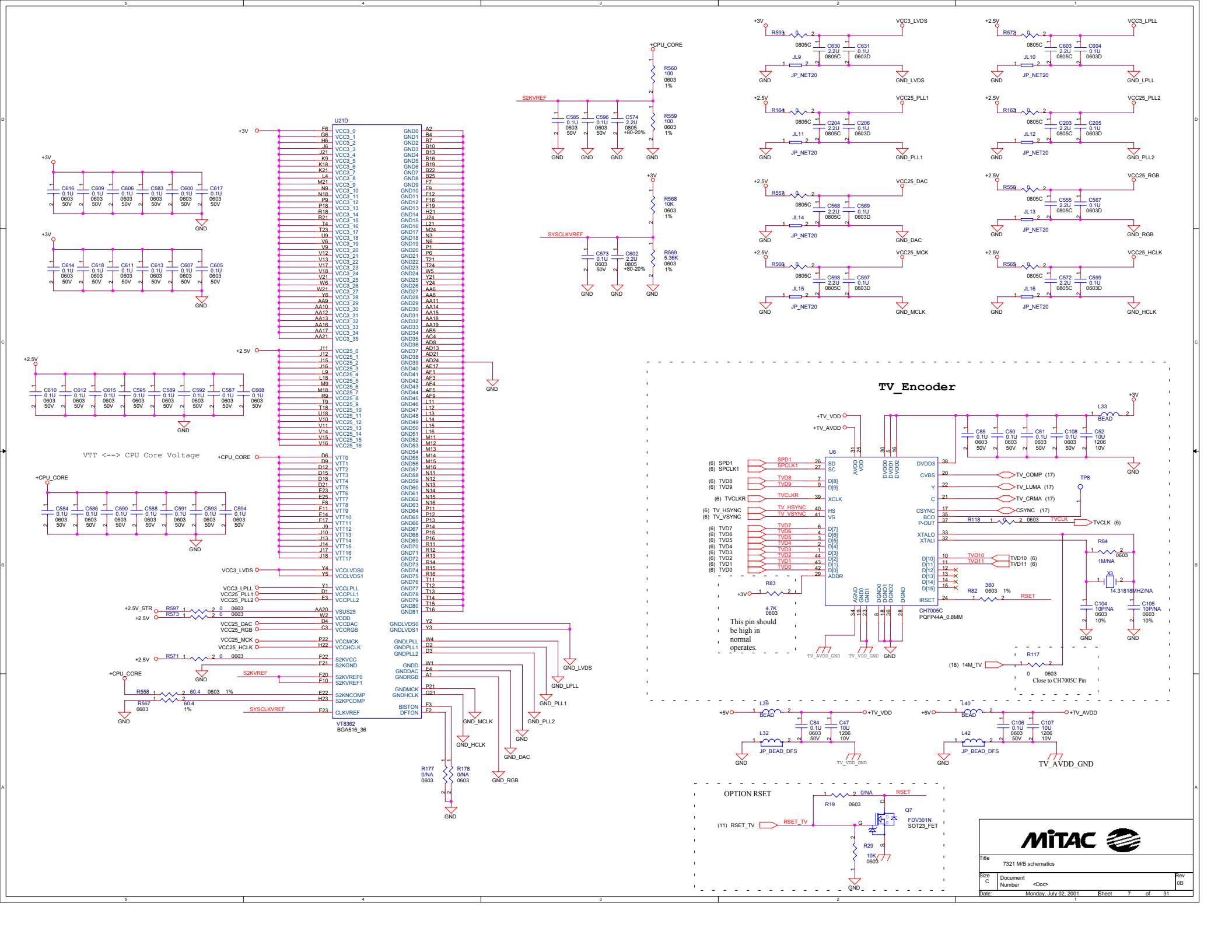
U21D
VTT <--> CPU Core Voltage
TV_Encoder
U6
CH7005C
PQFP44A_0.8MM
This pin should be high in normal operates.
Close to CH7005C Pin
OPTION RSET
VT8362
BGA516_36
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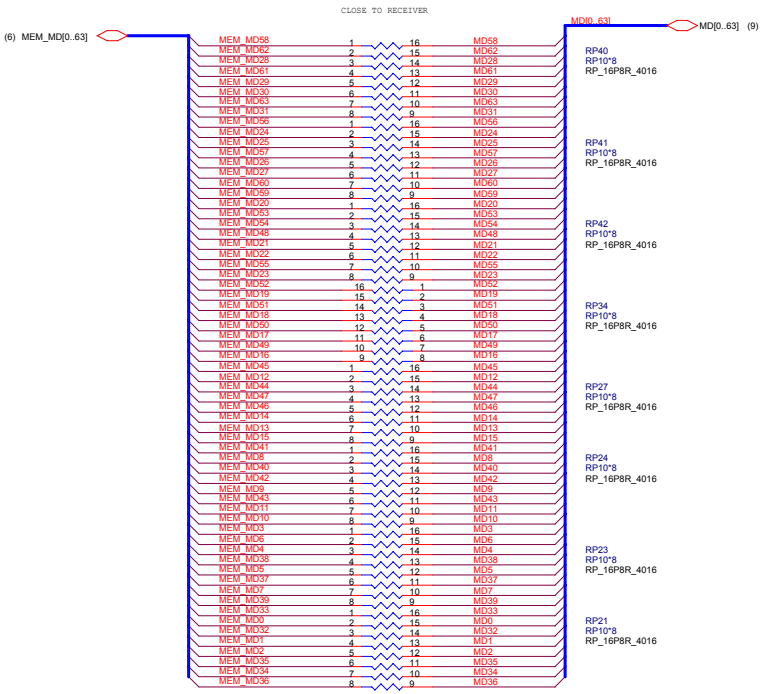
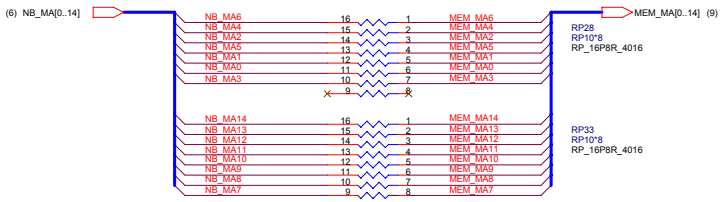
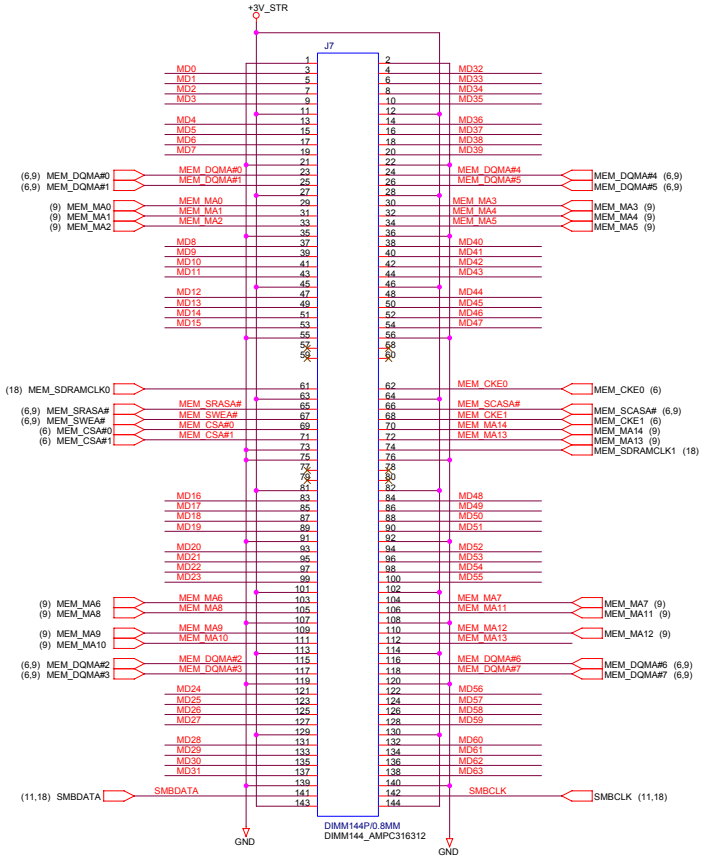
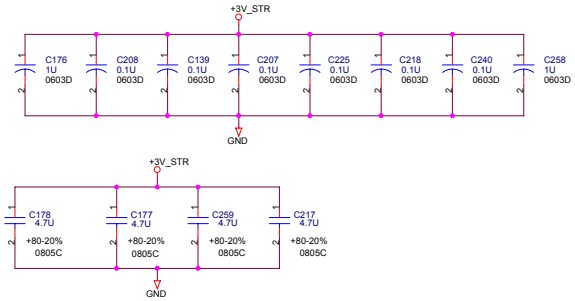
SODIMM





144 PIN SODIMM SOCKET





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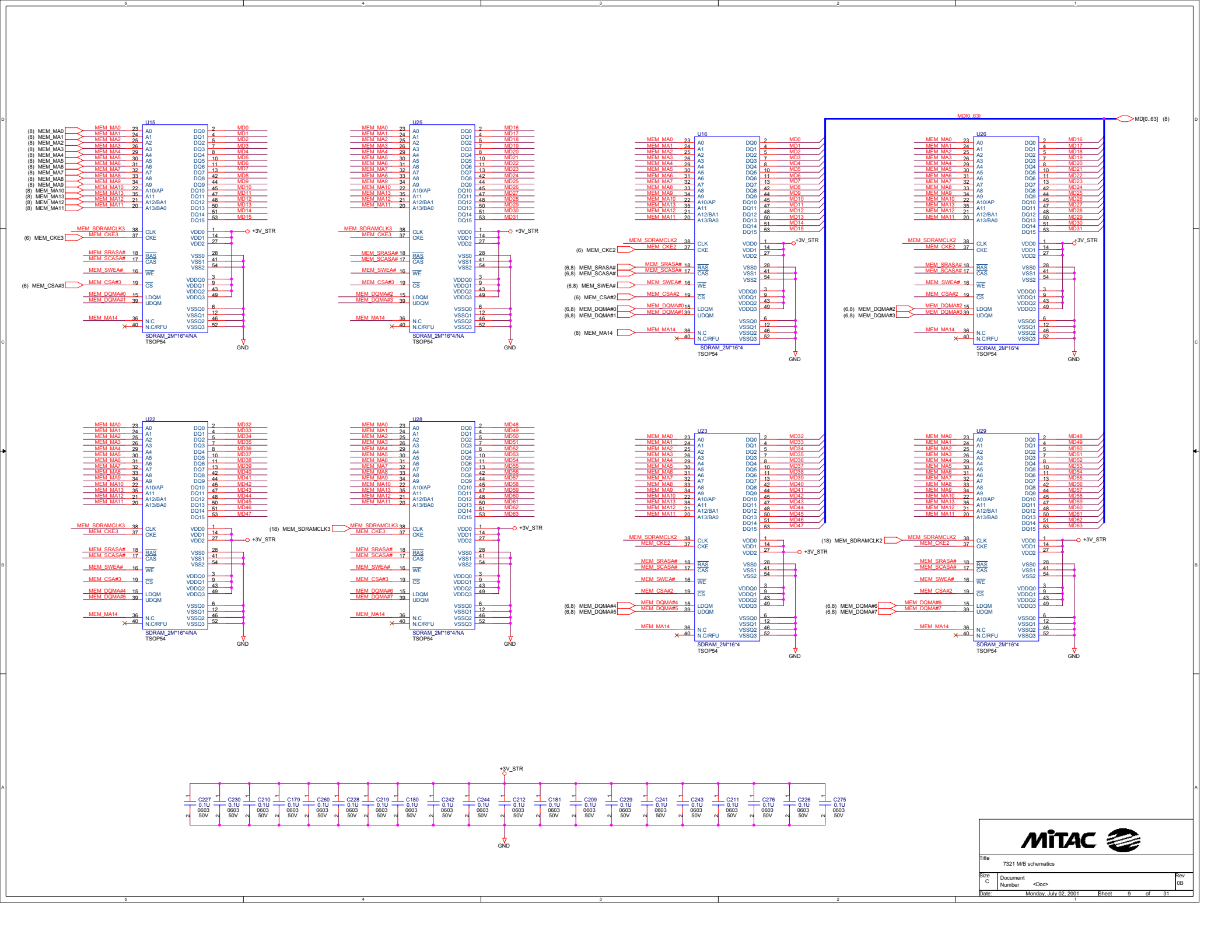
U15
U25
U16
U26
U22
U28
U23
U29
SDRAM_2M*16*4/NA
SDRAM_2M*16*4
TSOP54
+3V_STR
GND
MD[0..63]
C227 0.1U 0603 50V
C230 0.1U 0603 50V
C210 0.1U 0603 50V
C179 0.1U 0603 50V
C260 0.1U 0603 50V
C228 0.1U 0603 50V
C219 0.1U 0603 50V
C180 0.1U 0603 50V
C242 0.1U 0603 50V
C244 0.1U 0603 50V
C212 0.1U 0603 50V
C181 0.1U 0603 50V
C209 0.1U 0603 50V
C229 0.1U 0603 50V
C241 0.1U 0603 50V
C243 0.1U 0603 50V
C211 0.1U 0603 50V
C276 0.1U 0603 50V
C226 0.1U 0603 50V
C275 0.1U 0603 50V
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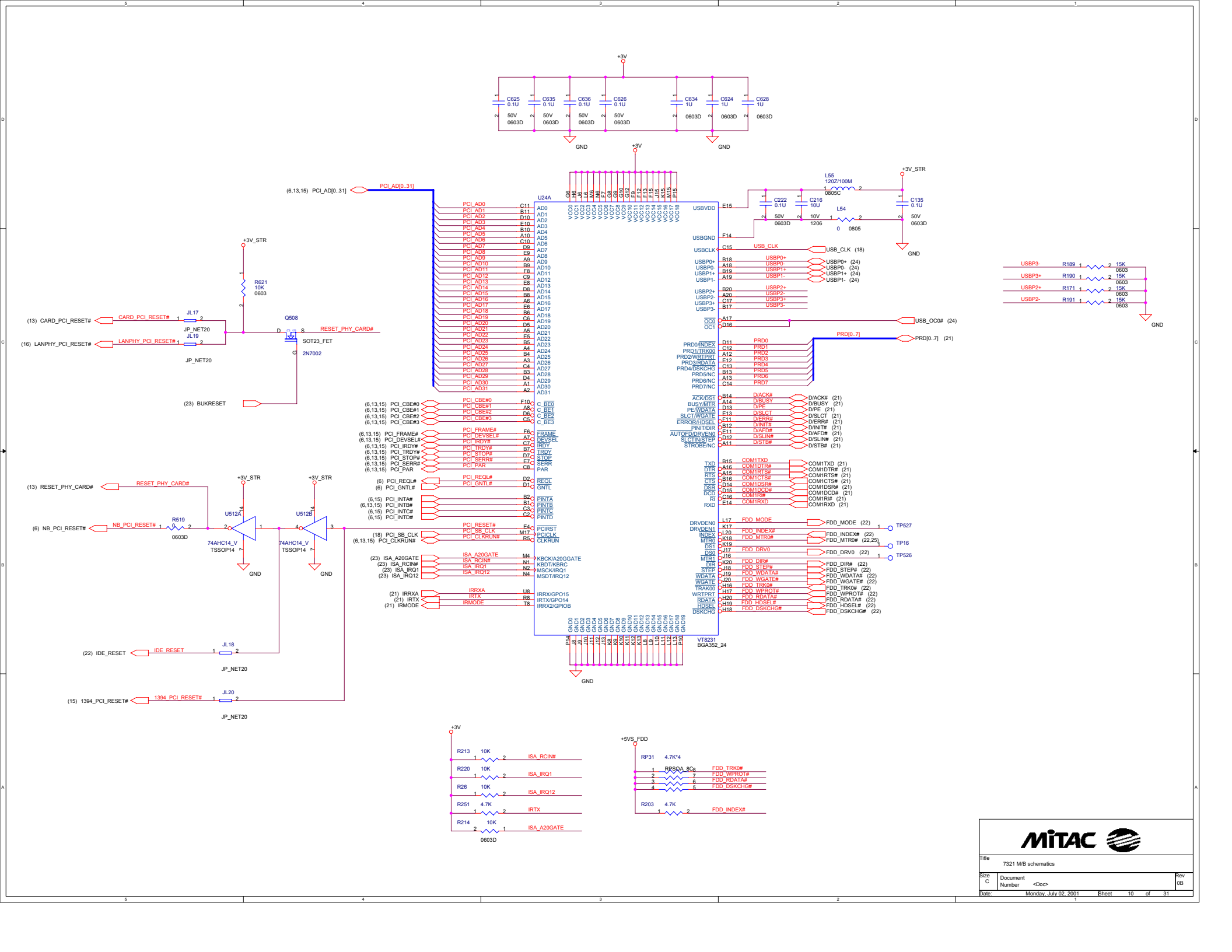
+3V
C625 0.1U 50V 0603D
C635 0.1U 50V 0603D
C636 0.1U 50V 0603D
C626 0.1U 50V 0603D
C634 1U 0603D
C624 1U 0603D
C628 1U 0603D
GND
U24A
VT8231
BGA352_24
PCI_AD[0..31]
(6,13,15) PCI_AD[0..31]
USBVDD
USBGND
USBCLK
USB_CLK
USB_CLK (18)
USBP0+ (24)
USBP0- (24)
USBP1+ (24)
USBP1- (24)
USB_OC0# (24)
PRD[0..7]
PRD[0..7] (21)
L55 120Z/100M 0805C
L54 0 0805
C222 0.1U 50V 0603D
C216 10U 10V 1206
C135 0.1U 50V 0603D
+3V_STR
USBP3- R189 15K 0603
USBP3+ R190 15K 0603
USBP2+ R171 15K 0603
USBP2- R191 15K 0603
R621 10K 0603
Q508 SOT23_FET 2N7002
JL17 JL19 JP_NET20
(13) CARD_PCI_RESET#
(16) LANPHY_PCI_RESET#
(23) BUKRESET
RESET_PHY_CARD#
(6,13,15) PCI_CBE#0
(6,13,15) PCI_CBE#1
(6,13,15) PCI_CBE#2
(6,13,15) PCI_CBE#3
(6,13,15) PCI_FRAME#
(6,13,15) PCI_DEVSEL#
(6,13,15) PCI_IRDY#
(6,13,15) PCI_TRDY#
(6,13,15) PCI_STOP#
(6,13,15) PCI_SERR#
(6,13,15) PCI_PAR
(6) PCI_REQL#
(6) PCI_GNTL#
(6,15) PCI_INTA#
(6,13,15) PCI_INTB#
(6,15) PCI_INTC#
(6,15) PCI_INTD#
(18) PCI_SB_CLK
(6,13,15) PCI_CLKRUN#
(23) ISA_A20GATE
(23) ISA_RCIN#
(23) ISA_IRQ1
(23) ISA_IRQ12
(21) IRRXA
(21) IRTX
(21) IRMODE
D/ACK# (21)
D/BUSY (21)
D/PE (21)
D/SLCT (21)
D/ERR# (21)
D/INIT# (21)
D/AFD# (21)
D/SLIN# (21)
D/STB# (21)
COM1TXD (21)
COM1DTR# (21)
COM1RTS# (21)
COM1CTS# (21)
COM1DSR# (21)
COM1DCD# (21)
COM1RI# (21)
COM1RXD (21)
FDD_MODE (22)
FDD_INDEX# (22)
FDD_MTR0# (22,25)
FDD_DRV0 (22)
FDD_DIR# (22)
FDD_STEP# (22)
FDD_WDATA# (22)
FDD_WGATE# (22)
FDD_TRK0# (22)
FDD_WPROT# (22)
FDD_RDATA# (22)
FDD_HDSEL# (22)
FDD_DSKCHG# (22)
TP527
TP16
TP526
U512A 74AHC14_V TSSOP14
U512B 74AHC14_V TSSOP14
R519 0 0603D
NB_PCI_RESET#
(6) NB_PCI_RESET#
(22) IDE_RESET
JL18 JP_NET20
(15) 1394_PCI_RESET#
JL20 JP_NET20
R213 10K ISA_RCIN#
R220 10K ISA_IRQ1
R26 10K ISA_IRQ12
R251 4.7K IRTX
R214 10K ISA_A20GATE
0603D
+5VS_FDD
RP31 4.7K*4 RPSQA_8C8
R203 4.7K FDD_INDEX#
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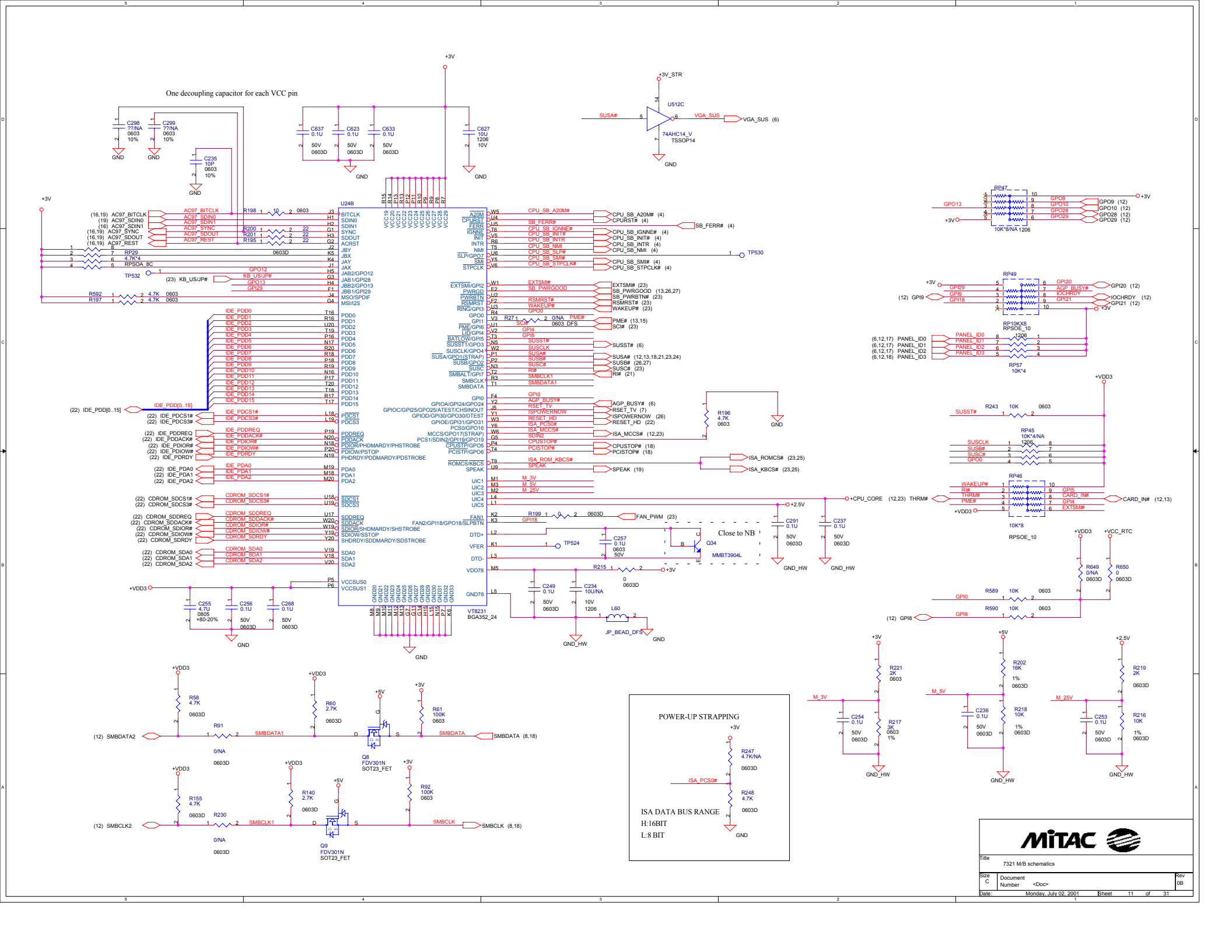
One decoupling capacitor for each VCC pin
U512C
74AHC14_V
TSSOP14
U24B
VT8231
BGA352_24
Close to NB
Q34
MMBT3904L
Q8
FDV301N
SOT23_FET
Q9
FDV301N
SOT23_FET
POWER-UP STRAPPING
ISA DATA BUS RANGE
H:16BIT
L:8 BIT
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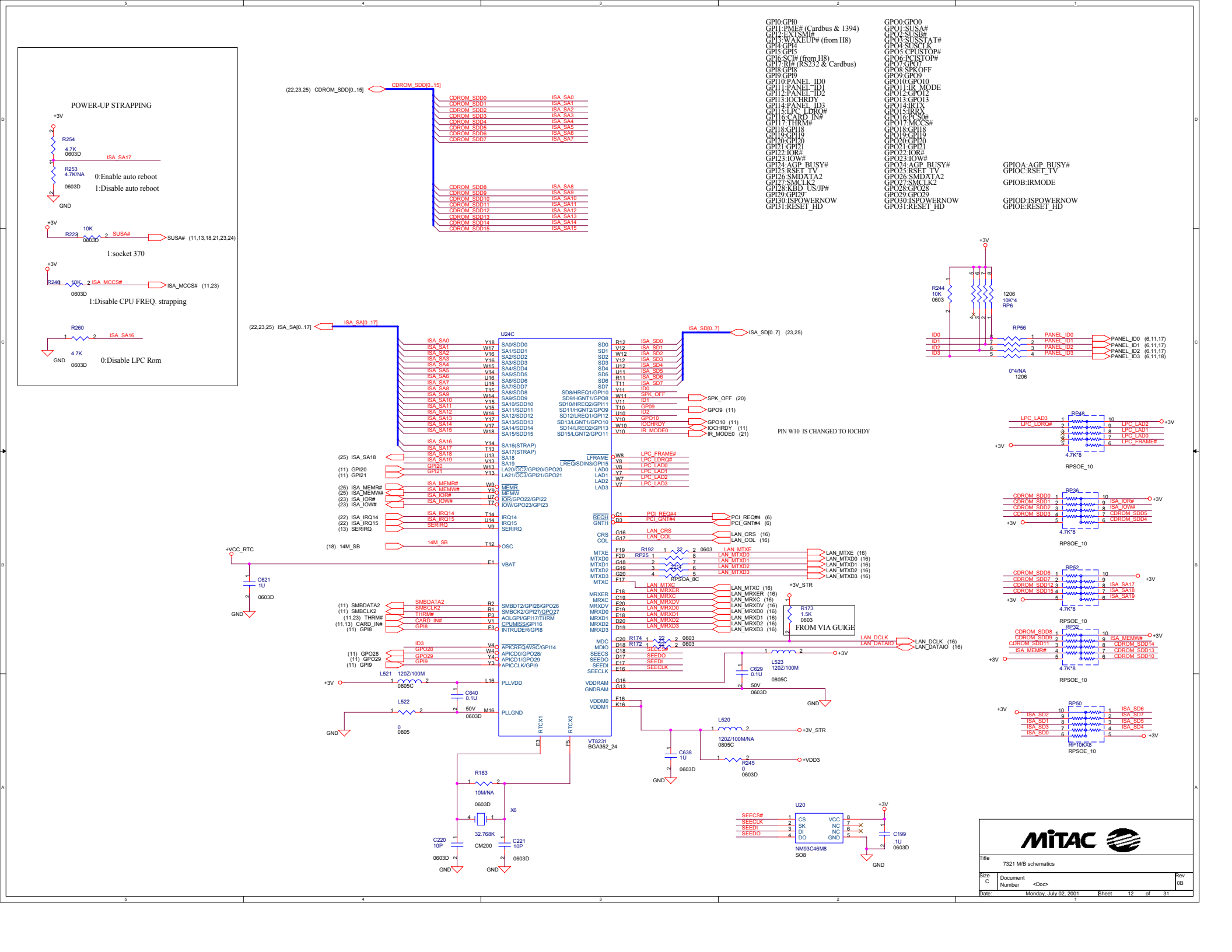
POWER-UP STRAPPING
+3V
R254
4.7K
0603D
ISA_SA17
R253
4.7K/NA
0603D
0:Enable auto reboot
1:Disable auto reboot
GND
+3V
R222
10K
0603D
SUSA#
SUSA# (11,13,18,21,23,24)
1:socket 370
+3V
R249
10K
0603D
ISA_MCCS#
ISA_MCCS# (11,23)
1:Disable CPU FREQ. strapping
R260
4.7K
0603D
ISA_SA16
GND
0:Disable LPC Rom
GPI0:GPI0
GPI1:PME# (Cardbus & 1394)
GPI2:EXTSMI#
GPI3:WAKEUP# (from H8)
GPI4:GPI4
GPI5:GPI5
GPI6:SCI# (from H8)
GPI7:RI# (RS232 & Cardbus)
GPI8:GPI8
GPI9:GPI9
GPI10:PANEL_ID0
GPI11:PANEL_ID1
GPI12:PANEL_ID2
GPI13:IOCHRDY
GPI14:PANEL_ID3
GPI15:LPC_LDRQ#
GPI16:CARD_IN#
GPI17:THRM#
GPI18:GPI18
GPI19:GPI19
GPI20:GPI20
GPI21:GPI21
GPI22:IOR#
GPI23:IOW#
GPI24:AGP_BUSY#
GPI25:RSET_TV
GPI26:SMDATA2
GPI27:SMCLK2
GPI28:KBD_US/JP#
GPI29:GPI29
GPI30:ISPOWERNOW
GPI31:RESET_HD
GPO0:GPO0
GPO1:SUSA#
GPO2:SUSB#
GPO3:SUSSTAT#
GPO4:SUSCLK
GPO5:CPUSTOP#
GPO6:PCISTOP#
GPO7:GPO7
GPO8:SPKOFF
GPO9:GPO9
GPO10:GPO10
GPO11:IR_MODE
GPO12:GPO12
GPO13:GPO13
GPO14:IRTX
GPO15:IRRX
GPO16:PCS0#
GPO17:MCCS#
GPO18:GPI18
GPO19:GPI19
GPO20:GPI20
GPO21:GPI21
GPO22:IOR#
GPO23:IOW#
GPO24:AGP_BUSY#
GPO25:RSET_TV
GPO26:SMDATA2
GPO27:SMCLK2
GPO28:GPO28
GPO29:GPO29
GPO30:ISPOWERNOW
GPO31:RESET_HD
GPIOA:AGP_BUSY#
GPIOC:RSET_TV
GPIOB:IRMODE
GPIOD:ISPOWERNOW
GPIOE:RESET_HD
(22,23,25) CDROM_SDD[0..15]
CDROM_SDD[0..15]
CDROM_SDD0 ISA_SA0
CDROM_SDD1 ISA_SA1
CDROM_SDD2 ISA_SA2
CDROM_SDD3 ISA_SA3
CDROM_SDD4 ISA_SA4
CDROM_SDD5 ISA_SA5
CDROM_SDD6 ISA_SA6
CDROM_SDD7 ISA_SA7
CDROM_SDD8 ISA_SA8
CDROM_SDD9 ISA_SA9
CDROM_SDD10 ISA_SA10
CDROM_SDD11 ISA_SA11
CDROM_SDD12 ISA_SA12
CDROM_SDD13 ISA_SA13
CDROM_SDD14 ISA_SA14
CDROM_SDD15 ISA_SA15
(22,23,25) ISA_SA[0..17]
ISA_SA[0..17]
ISA_SD[0..7]
ISA_SD[0..7] (23,25)
U24C
ISA_SA0 Y18
ISA_SA1 W17
ISA_SA2 V16
ISA_SA3 Y16
ISA_SA4 W15
ISA_SA5 V14
ISA_SA6 U16
ISA_SA7 U15
ISA_SA8 T15
ISA_SA9 W14
ISA_SA10 Y15
ISA_SA11 V15
ISA_SA12 W16
ISA_SA13 Y17
ISA_SA14 V17
ISA_SA15 W18
SA0/SDD0
SA1/SDD1
SA2/SDD2
SA3/SDD3
SA4/SDD4
SA5/SDD5
SA6/SDD6
SA7/SDD7
SA8/SDD8
SA9/SDD9
SA10/SDD10
SA11/SDD11
SA12/SDD12
SA13/SDD13
SA14/SDD14
SA15/SDD15
SD0 R12 ISA_SD0
SD1 V12 ISA_SD1
SD2 W12 ISA_SD2
SD3 Y12 ISA_SD3
SD4 U12 ISA_SD4
SD5 U11 ISA_SD5
SD6 R11 ISA_SD6
SD7 T11 ISA_SD7
SD8/HREQ1/GPI10 Y11 ID0
SD9/HGNT1/GPO8 W11 SPK_OFF (20)
SD10/HREQ2/GPI11 V11 ID1
SD11/HGNT2/GPO9 T10 GPO9 (11)
SD12/LREQ1/GPI12 U10 ID2
SD13/LGNT1/GPO10 Y10 GPO10 (11)
SD14/LREQ2/GPI13 W10 IOCHRDY (11)
SD15/LGNT2/GPO11 V10 IR_MODE0 (21)
PIN W10 IS CHANGED TO IOCHDY
SA16/STRAP)
SA17/STRAP)
SA18
SA19
LA20/OC2/GPI20/GPO20
LA21/OC3/GPI21/GPO21
LFRAME W8 LPC_FRAME#
Y8 LPC_LDRQ#
V8 LPC_LAD0
LAD1 Y7 LPC_LAD1
LAD2 W7 LPC_LAD2
LAD3 V7 LPC_LAD3
LREQ/SDIN3/GPI15
(25) ISA_SA18
(11) GPI20
(11) GPI21
GPI20 W13
GPI21 Y13
(25) ISA_MEMR#
(25) ISA_MEMW#
(23) ISA_IOR#
(23) ISA_IOW#
ISA_MEMR# W9
ISA_MEMW# Y9
ISA_IOR# U7
ISA_IOW# T7
MEMR
MEMW
IOR/GPO22/GPI22
IOW/GPO23/GPI23
(22) ISA_IRQ14
(22) ISA_IRQ15
(13) SERIRQ
ISA_IRQ14 T14
ISA_IRQ15 U14
SERIRQ V9
IRQ14
IRQ15
SERIRQ
REQH C1 PCI_REQ#4
GNTH D3 PCI_GNT#4
PCI_REQ#4 (6)
PCI_GNT#4 (6)
CRS G16 LAN_CRS
COL G17 LAN_COL
LAN_CRS (16)
LAN_COL (16)
(18) 14M_SB
14M_SB T12
OSC
+VCC_RTC
E1
VBAT
C621
1U
0603D
GND
MTXE F19 R192 1 22 2 0603 LAN_MTXE
MTXD0 F20 RP25 1 8 LAN_MTXD0
MTXD1 G18 2 7 LAN_MTXD1
MTXD2 G19 3 6 LAN_MTXD2
MTXD3 G20 4 5 LAN_MTXD3
MTXC F17 RPSOA_8C
LAN_MTXE (16)
LAN_MTXD0 (16)
LAN_MTXD1 (16)
LAN_MTXD2 (16)
LAN_MTXD3 (16)
LAN_MTXC
MRXER F18 LAN_MRXER
MRXC C19 LAN_MRXC
MRXDV E20 LAN_MRXDV
MRXD0 E19 LAN_MRXD0
MRXD1 E18 LAN_MRXD1
MRXD2 D20 LAN_MRXD2
MRXD3 D19 LAN_MRXD3
LAN_MRXER (16)
LAN_MRXC (16)
LAN_MRXDV (16)
LAN_MRXD0 (16)
LAN_MRXD1 (16)
LAN_MRXD2 (16)
LAN_MRXD3 (16)
+3V_STR
R173
1.5K
0603
FROM VIA GUIGE
MDC C20 R174 1 22 2 0603 LAN_DCLK
MDIO D18 R172 1 22 2 0603 LAN_DATAIO
LAN_DCLK (16)
LAN_DATAIO (16)
SEECS C18 SEECS
SEEDO D17 SEEDO
SEEDI F17 SEEDI
SEECLK E16 SEECLK
(11,23) THRM#
(11,13) CARD_IN#
(11) GPI8
SMBDATA2 R2
SMBCLK2 R1
THRM# P3
CARD_IN# V1
GPI8 F3
SMBDT2/GPI26/GPO26
SMBCK2/GPI27/GPO27
AOLGPI/GPI17/THRM
CPUMISS/GPI16
INTRUDER/GPI8
(11) GPO28
(11) GPO29
(11) GPI9
ID3 V4
GPO28 W4
GPO29 Y4
GPI9 Y3
APICREQ/WSC/GPI14
APICD0/GPO28/
APICD1/GPO29
APICCLK/GPI9
L521 120Z/100M
0805C
+3V
C640
0.1U
50V
0603D
L522
0
0805
GND
M16
PLLVDD
PLLGND
RTCX1
RTCX2
E3
F5
VT8231
BGA352_24
VDDRAM G15
GNDRAM G13
VDDM0 F16
VDDM1 K16
L523
120Z/100M
0805C
C629
0.1U
50V
0603D
L520
120Z/100M/NA
0805C
C638
1U
0603D
R245
0
0603D
+VDD3
R183
10M/NA
0603D
X6
32.768K
CM200
C220
10P
0603D
C221
10P
0603D
U20
SEECS#
SEECLK
SEEDI
SEEDO
CS
SK
DI
DO
VCC
NC
NC
GND
NM93C46M8
SO8
C199
1U
0603D
R244
10K
0603
1206
10K*4
RP6
0*4/NA
1206
RP56
ID0
ID1
ID2
ID3
PANEL_ID0
PANEL_ID1
PANEL_ID2
PANEL_ID3
PANEL_ID0 (6,11,17)
PANEL_ID1 (6,11,17)
PANEL_ID2 (6,11,17)
PANEL_ID3 (6,11,18)
RP48
LPC_LAD3
LPC_LDRQ#
LPC_LAD2
LPC_LAD1
LPC_LAD0
LPC_FRAME#
4.7K*8
RPSOE_10
RP36
CDROM_SDD0
CDROM_SDD1
CDROM_SDD2
CDROM_SDD3
ISA_IOR#
ISA_IOW#
CDROM_SDD5
CDROM_SDD4
RP52
CDROM_SDD6
CDROM_SDD7
CDROM_SDD12
CDROM_SDD15
ISA_SA17
ISA_SA18
ISA_SA19
RP32
CDROM_SDD8
CDROM_SDD9
CDROM_SDD11
ISA_MEMR#
ISA_MEMW#
CDROM_SDD4
CDROM_SDD13
CDROM_SDD10
RP50
ISA_SD6
ISA_SD2
ISA_SD1
ISA_SD3
ISA_SD0
ISA_SD7
ISA_SD5
ISA_SD4
RP10K8
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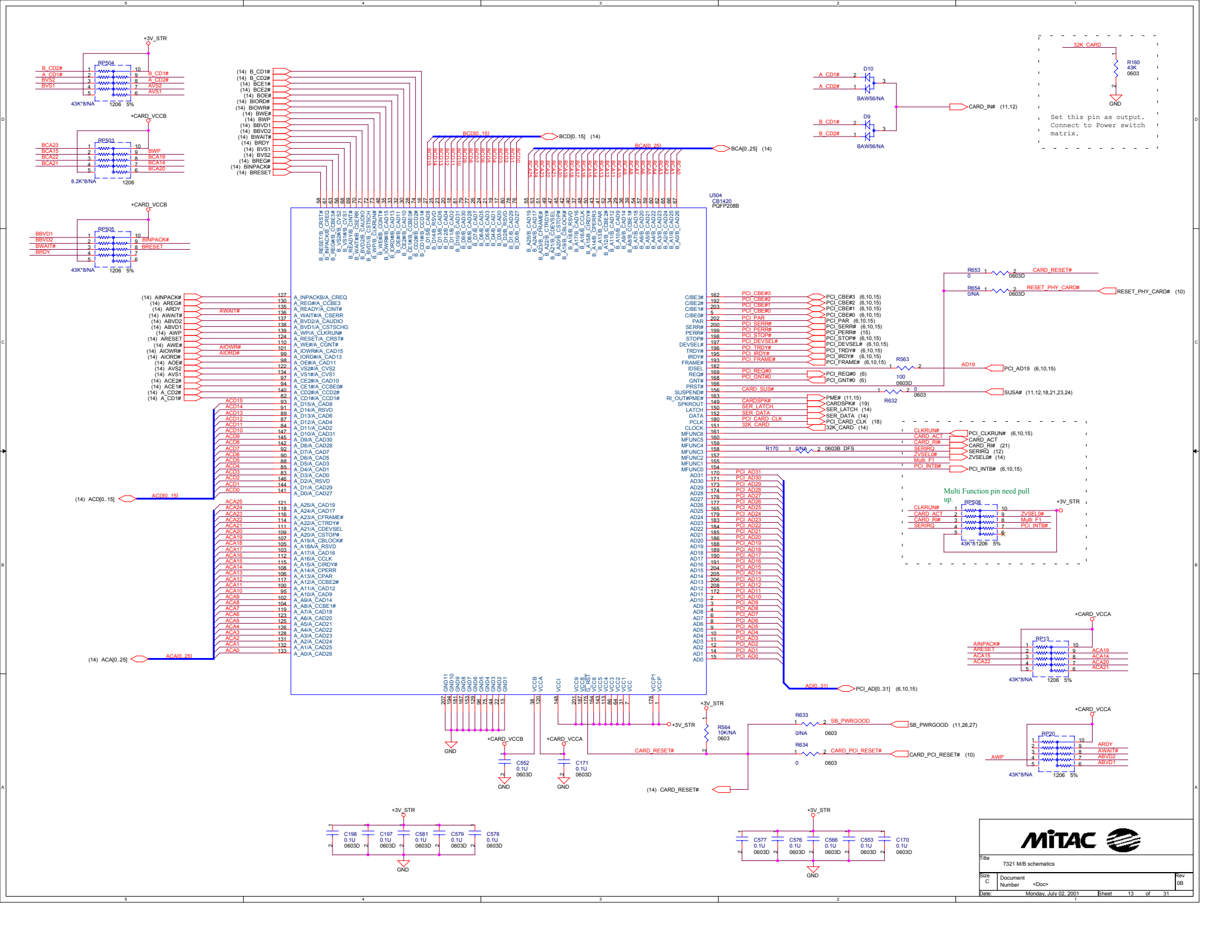
U504
CB1420
PQFP208B
RP504
RP503
RP505
RP508
RP13
RP20
D10
D9
BAW56/NA
R160
43K
0603
32K_CARD
Set this pin as output.
Connect to Power switch
matrix.
R653
R654
R563
R632
R633
R634
R564
10K/NA
CARD_RESET#
RESET_PHY_CARD#
SB_PWRGOOD
CARD_PCI_RESET#
Multi Function pin need pull
up.
C552
C171
C198
C197
C581
C579
C578
C577
C576
C566
C553
C170
0.1U
0603D
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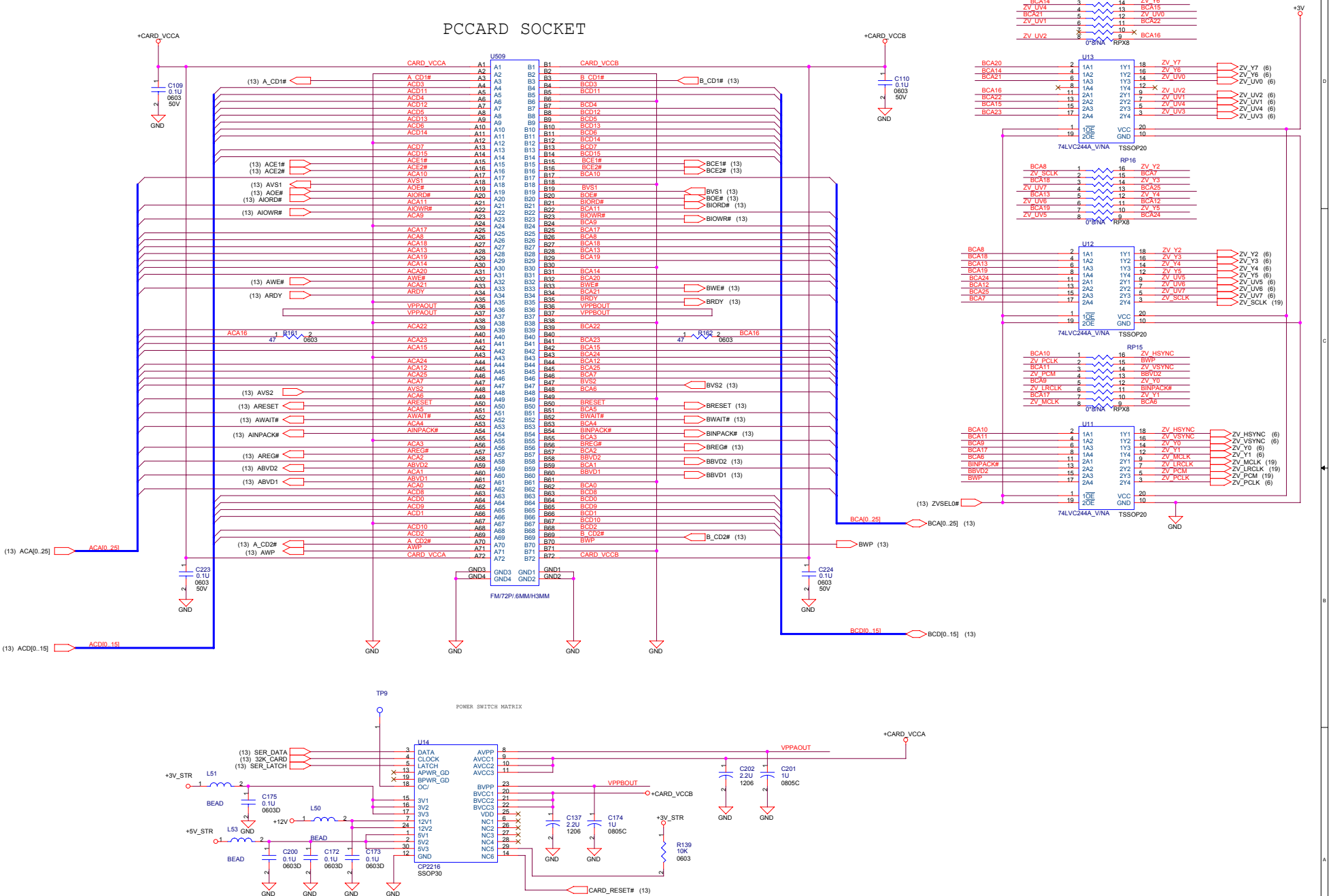
PCCARD SOCKET



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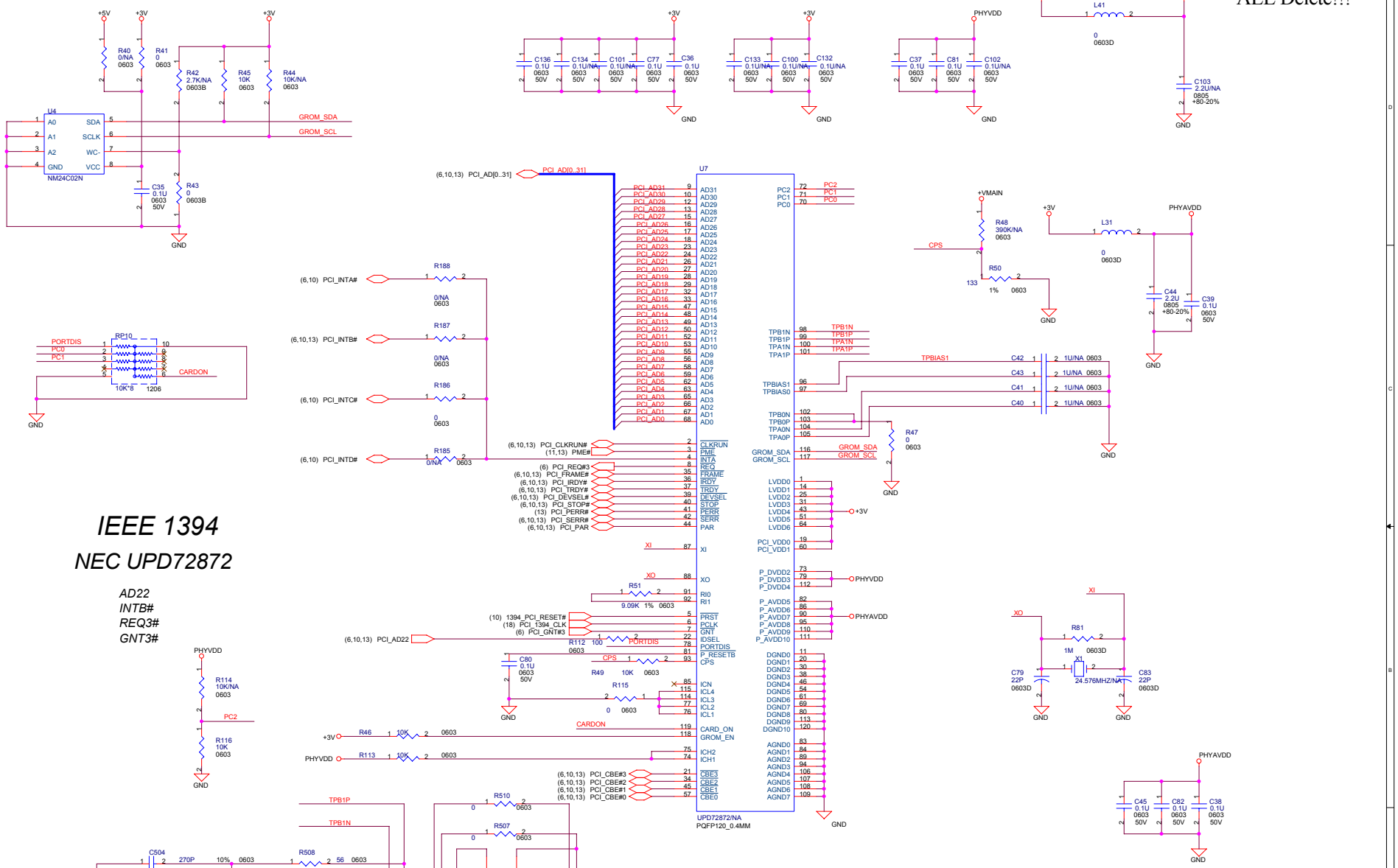
IEEE 1394

NEC UPD72872

AD22
INTB#
REQ3#
GNT3#



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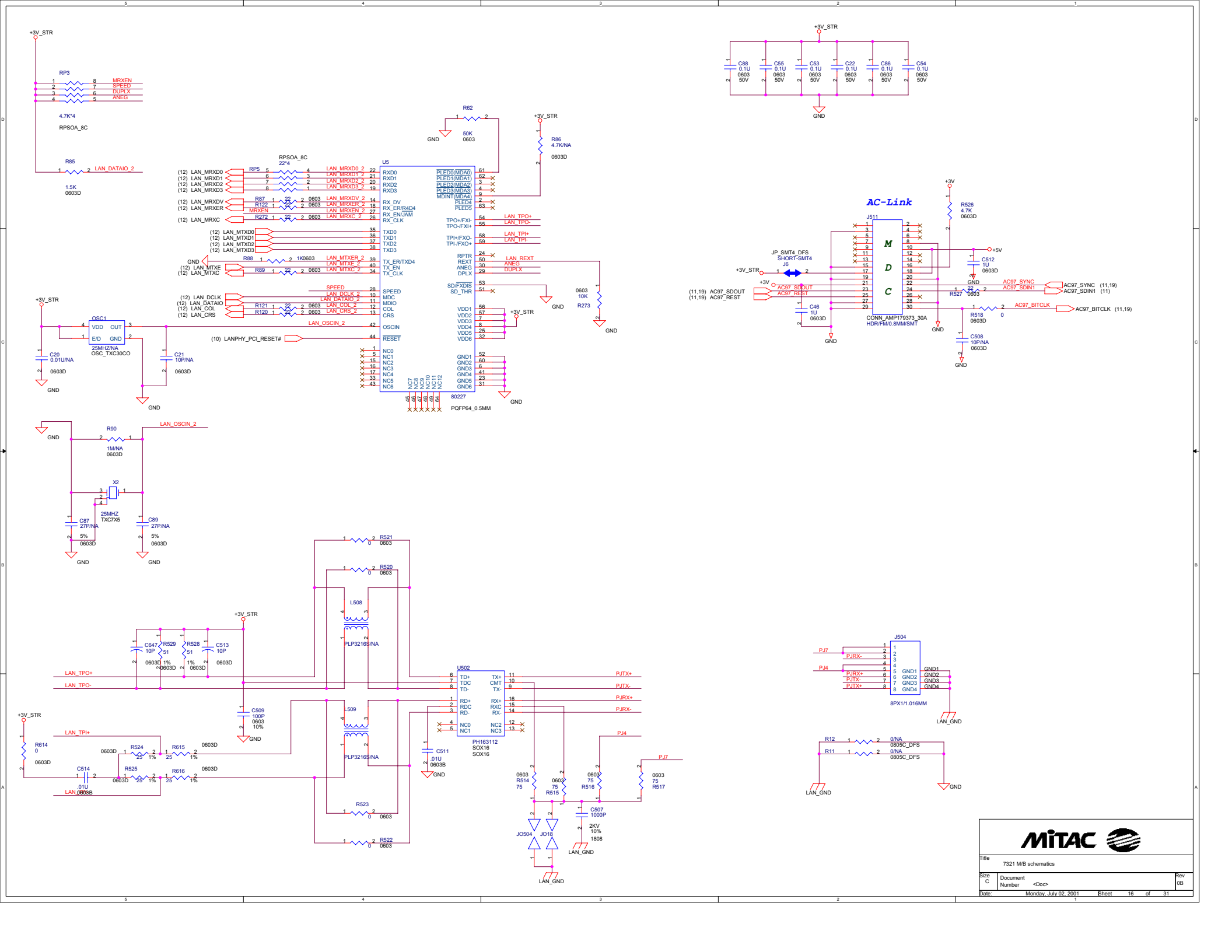
+3V_STR
RP3
MRXEN
SPEED
DUPLX
ANEG
4.7K*4
RPSOA_8C
R85
LAN_DATAIO_2
1.5K
0603D
R62
50K
0603
GND
R86
4.7K/NA
0603D
RPSOA_8C
22*4
U5
(12) LAN_MRXD0
(12) LAN_MRXD1
(12) LAN_MRXD2
(12) LAN_MRXD3
(12) LAN_MRXDV
(12) LAN_MRXER
(12) LAN_MRXC
(12) LAN_MTXD0
(12) LAN_MTXD1
(12) LAN_MTXD2
(12) LAN_MTXD3
(12) LAN_MTXE
(12) LAN_MTXC
(12) LAN_DCLK
(12) LAN_DATAIO
(12) LAN_COL
(12) LAN_CRS
(10) LANPHY_PCI_RESET#
LAN_OSCIN_2
SPEED
RX_DV
RX_ER/R4D4
RX_EN/JAM
RX_CLK
TXD0
TXD1
TXD2
TXD3
TX_ER/TXD4
TX_EN
TX_CLK
MDC
MDIO
COL
CRS
OSCIN
RESET
PLED0(MDA0)
PLED1(MDA1)
PLED2(MDA2)
PLED3(MDA3)
MDINT(MDA4)
PLED4
PLED5
LAN_TPO+
LAN_TPO-
LAN_TPI+
LAN_TPI-
LAN_REXT
ANEG
DUPLX
SD/FXDIS
SD_THR
VDD1
VDD2
VDD3
VDD4
VDD5
VDD6
GND1
GND2
GND3
GND4
GND5
GND6
NC0
NC1
NC2
NC3
NC4
NC5
NC6
NC7
NC8
NC9
NC10
NC11
NC12
80227
PQFP64_0.5MM
0603
10K
R273
OSC1
VDD
OUT
E/D
GND
25MHZ/NA
OSC_TXC30CO
C20
0.01U/NA
C21
10P/NA
R90
1M/NA
X2
25MHZ
TXC7X5
C87
27P/NA
C89
27P/NA
5%
C88
C55
C53
C22
C86
C54
0.1U
50V
AC-Link
J511
CONN_AMP179373_30A
HDR/FM/0.8MM/SMT
JP_SMT4_DFS
SHORT-SMT4
J6
R526
4.7K
C512
1U
C46
1U
R527
R518
0
C508
10P/NA
AC97_SDOUT
AC97_REST
AC97_SYNC
AC97_SDIN1
AC97_BITCLK
(11,19) AC97_SDOUT
(11,19) AC97_REST
AC97_SYNC (11,19)
AC97_SDIN1 (11)
AC97_BITCLK (11,19)
L508
PLP3216S/NA
L509
C647
10P
R529
51
R528
C513
C509
100P
10%
C514
.01U
R524
R525
R615
R616
R523
R521
R520
R522
LAN_TPO+
LAN_TPO-
LAN_TPI+
U502
TD+
TDC
TD-
RD+
RDC
RD-
TX+
CMT
TX-
RX+
RXC
RX-
NC0
NC1
NC2
NC3
PH163112
SOX16
SOX16
PJTX+
PJTX-
PJRX+
PJRX-
PJ4
PJ7
C511
01U
0603B
R614
0
R514
75
R515
R516
R517
C507
1000P
2KV
10%
1808
JO504
JO18
LAN_GND
J504
PJ7
PJRX-
PJ4
PJRX+
PJTX-
PJTX+
GND1
GND2
GND3
GND4
8PX1/1.016MM
R12
R11
0/NA
0805C_DFS
0/NA
0805C_DFS
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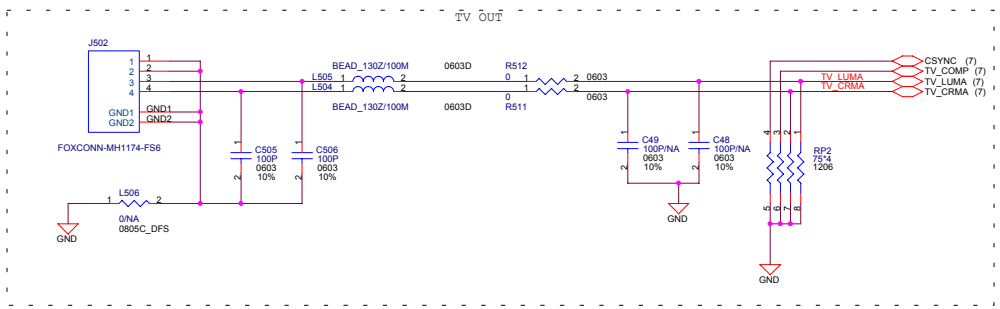
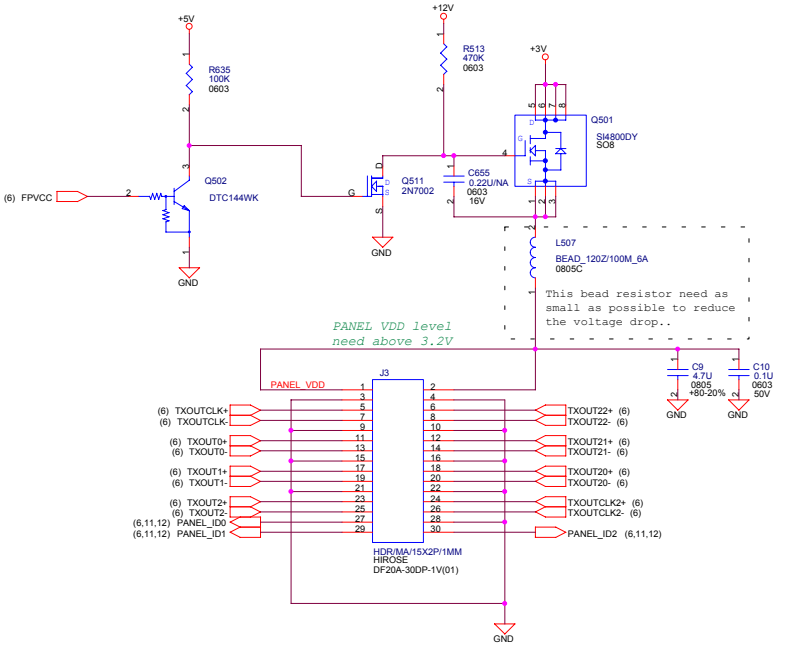
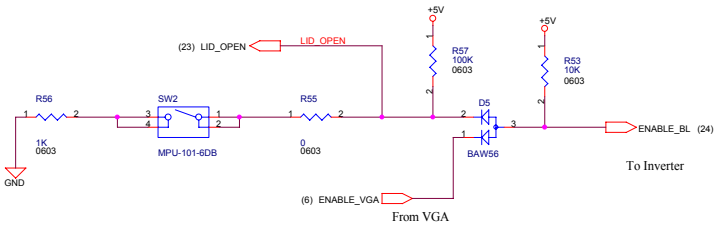
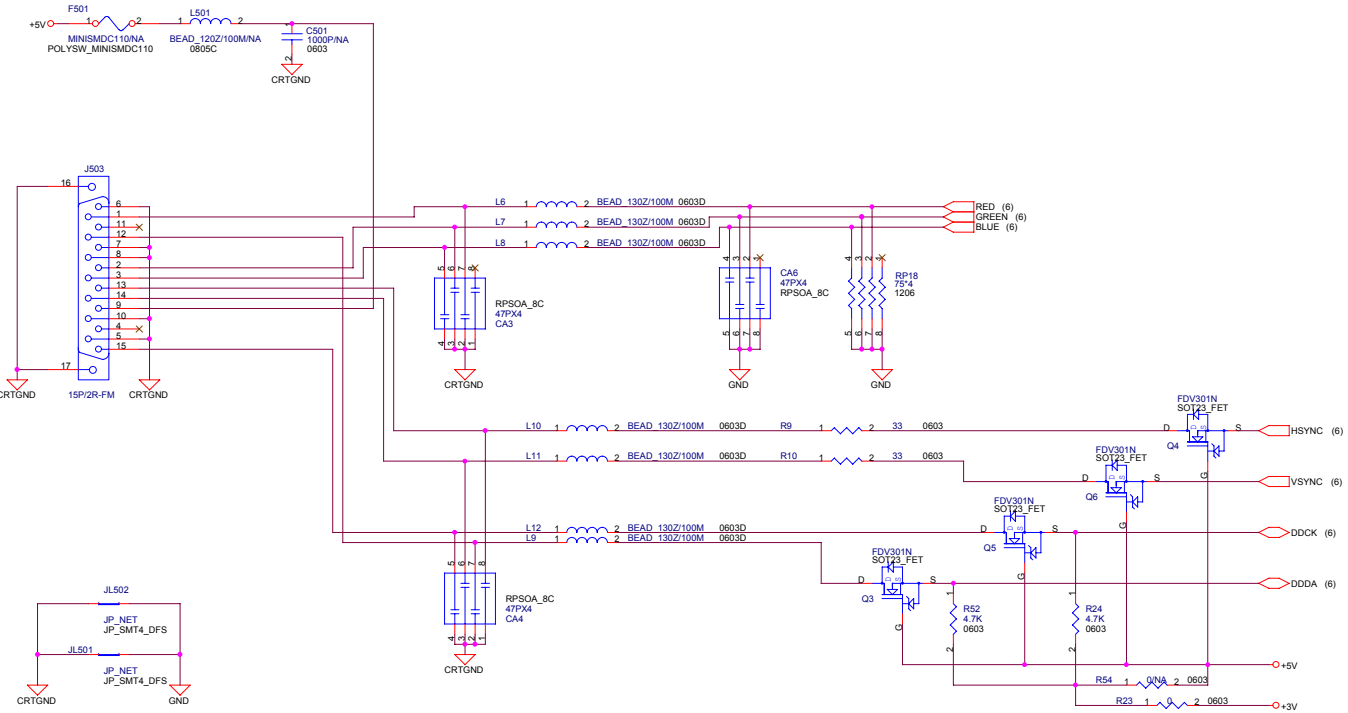
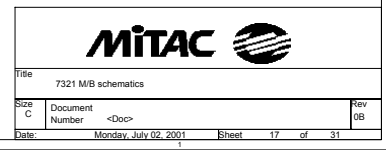

TV OUT
J502
FOXCONN-MH1174-FS6
GND1
GND2
L505
L504
BEAD_130Z/100M
0603D
R512
R511
0603
C505
100P
0603
10%
C506
100P
0603
10%
L506
0/NA
0805C_DFS
C49
100P/NA
0603
10%
C48
100P/NA
0603
10%
RP2
75*4
1206
TV_LUMA
TV_CRMA
CSYNC (7)
TV_COMP (7)
TV_LUMA (7)
TV_CRMA (7)
GND


+5V
R635
100K
0603
Q502
DTC144WK
(6) FPVCC
+12V
R513
470K
0603
Q511
2N7002
C655
0.22U/NA
0603
16V
+3V
Q501
SI4800DY
SO8
L507
BEAD_120Z/100M_6A
0805C
This bead resistor need as small as possible to reduce the voltage drop..
PANEL VDD level need above 3.2V
C9
4.7U
0805
+80-20%
C10
0.1U
0603
50V
PANEL_VDD
J3
HDR/MA/15X2P/1MM
HIROSE
DF20A-30DP-1V(01)
(6) TXOUTCLK+
(6) TXOUTCLK-
(6) TXOUT0+
(6) TXOUT0-
(6) TXOUT1+
(6) TXOUT1-
(6) TXOUT2+
(6) TXOUT2-
(6,11,12) PANEL_ID0
(6,11,12) PANEL_ID1
TXOUT22+ (6)
TXOUT22- (6)
TXOUT21+ (6)
TXOUT21- (6)
TXOUT20+ (6)
TXOUT20- (6)
TXOUTCLK2+ (6)
TXOUTCLK2- (6)
PANEL_ID2 (6,11,12)
GND


(23) LID_OPEN
LID_OPEN
R57
100K
0603
R53
10K
0603
R56
1K
0603
SW2
MPU-101-6DB
R55
0
0603
D5
BAW56
ENABLE_BL (24)
(6) ENABLE_VGA
From VGA
To Inverter
GND


F501
MINISMDC110/NA
POLYSW_MINISMDC110
L501
BEAD_120Z/100M/NA
0805C
C501
1000P/NA
0603
CRTGND
J503
15P/2R-FM
L6
L7
L8
BEAD_130Z/100M
0603D
RED (6)
GREEN (6)
BLUE (6)
RPSOA_8C
47PX4
CA3
CA6
47PX4
RPSOA_8C
RP18
75*4
1206
GND
L10
L11
L12
L9
R9
R10
33
0603
FDV301N
SOT23_FET
Q4
Q6
Q5
Q3
HSYNC (6)
VSYNC (6)
DDCK (6)
DDDA (6)
R52
4.7K
0603
R24
4.7K
0603
R54
0/NA
R23
0
+5V
+3V
JL502
JL501
JP_NET
JP_SMT4_DFS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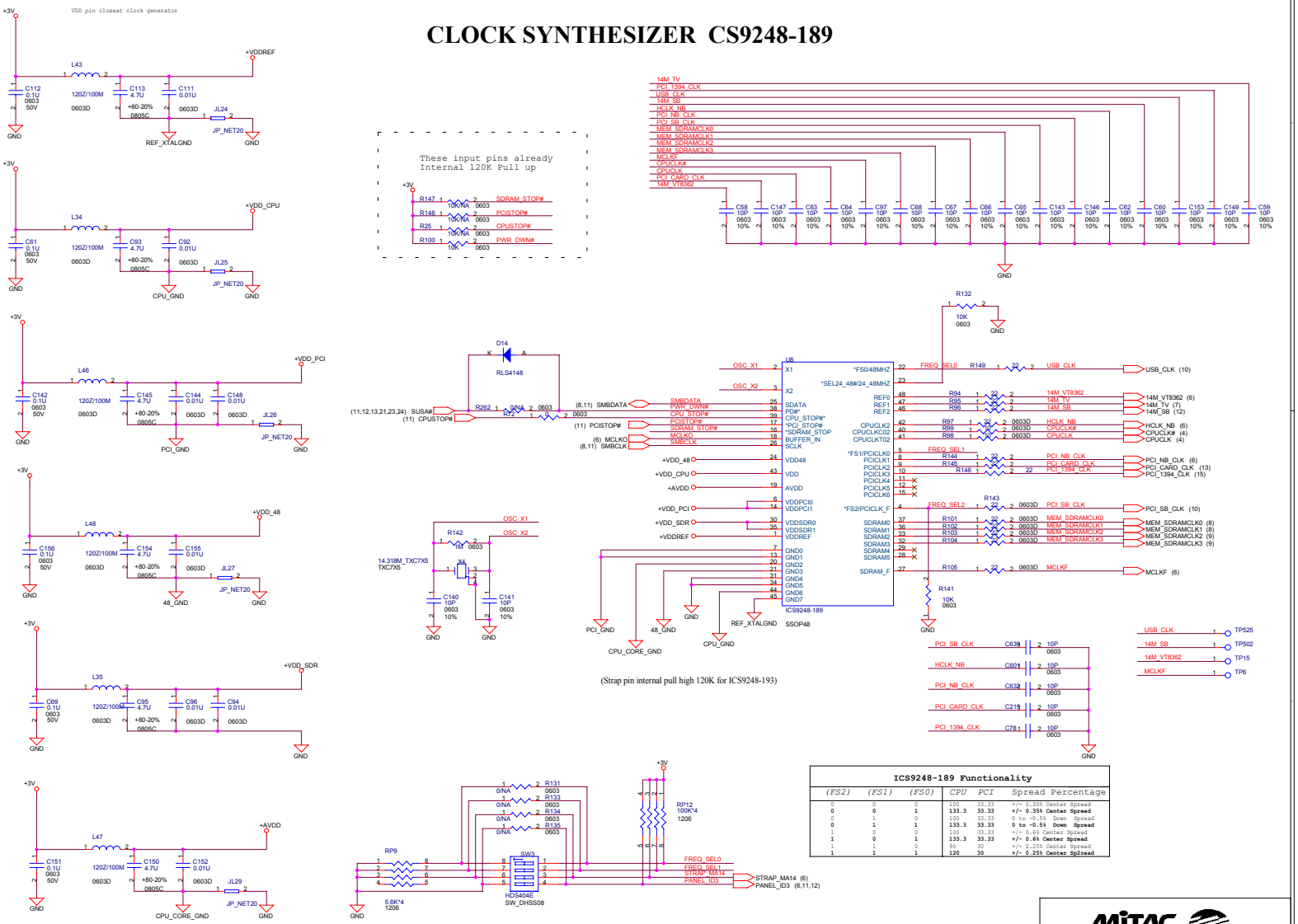
CLOCK SYNTHESIZER CS9248-189



ICS9248-189 Functionality

(FS2)	(FS1)	(FS0)	CPU	PCI	Spread Percentage
0	0	0	100	33.33	+/- 0.35% Center Spread
0	0	1	133.3	33.33	+/- 0.35% Center Spread
0	1	0	100	33.33	0 to -0.5% Down Spread
0	1	1	133.3	33.33	0 to -0.5% Down Spread
1	0	0	100	33.33	+/- 0.6% Center Spread
1	0	1	133.3	33.33	+/- 0.6% Center Spread
1	1	0	90	30	+/- 0.25% Center Spread
1	1	1	120	30	+/- 0.25% Center Spread

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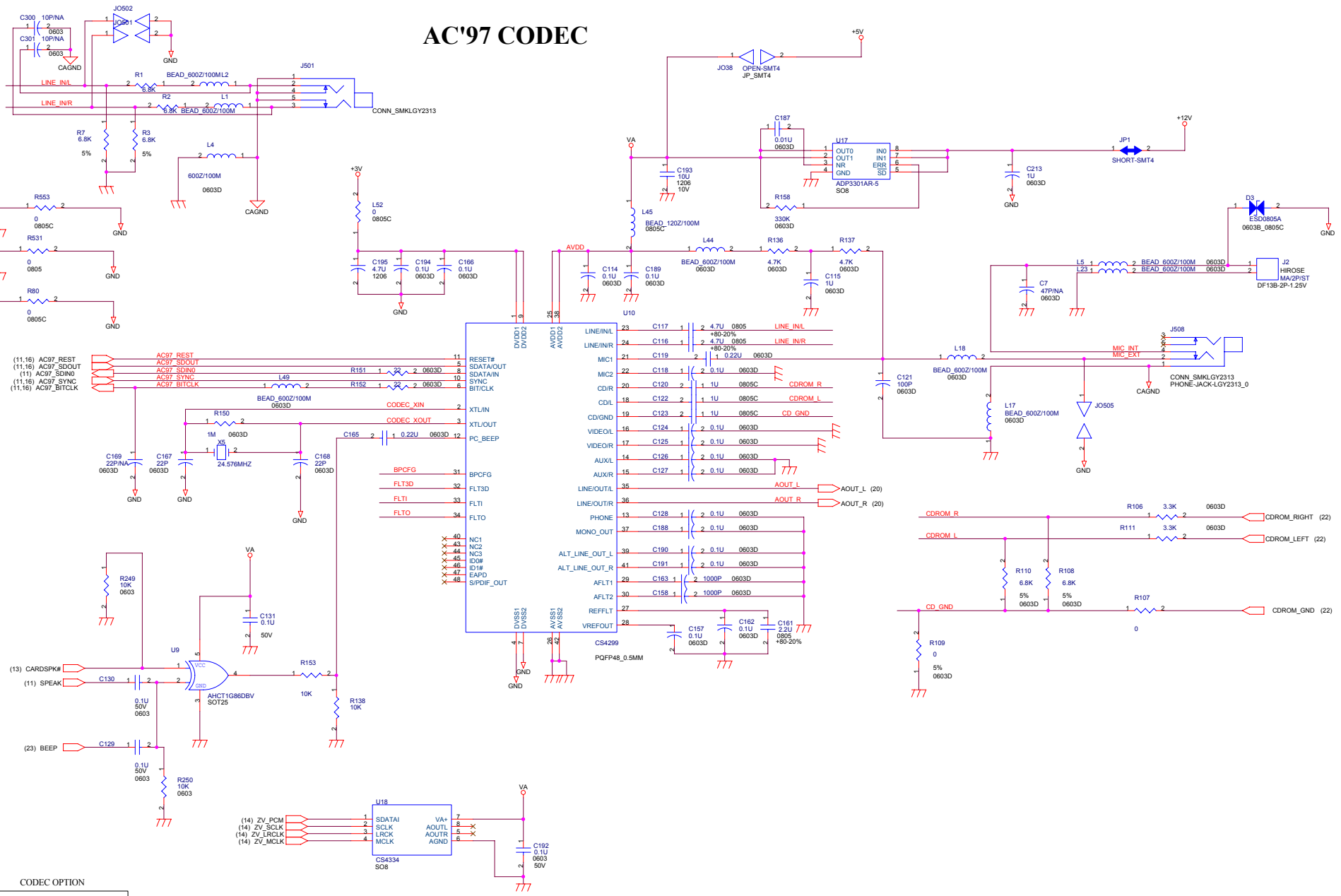
AC'97 CODEC

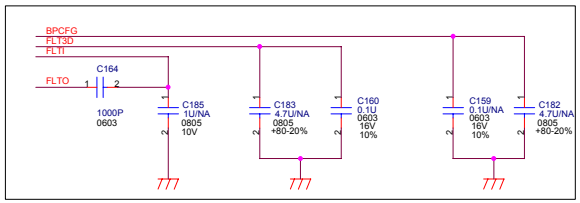


CODEC OPTION

	alc200	ad1881	cs4299
C159	0.1uf	1uf	x
C182	4.7uf	x	x
C160	0.1uf	1uf	0.01uf
C183	4.7uf	x	x
C185	1uf	10p	x
C164	x	4700pf	1000pf

If 4.7UF is remooved then C88,C61 are changed to 1UF

CODEC OPTION



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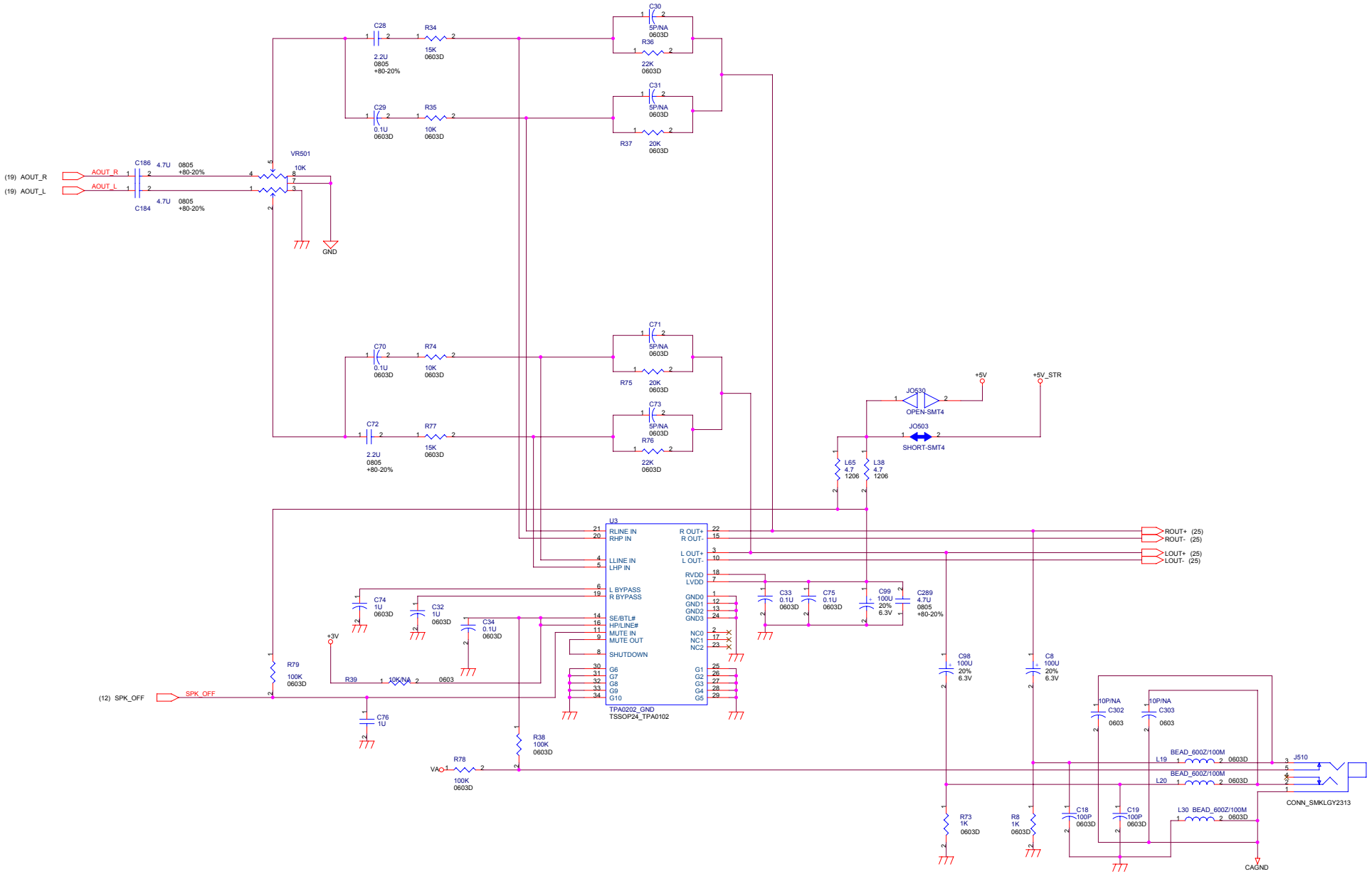
AUDIO AMPLIFIER - TPA0202



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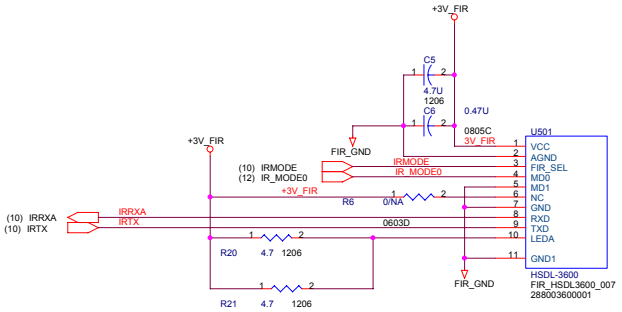
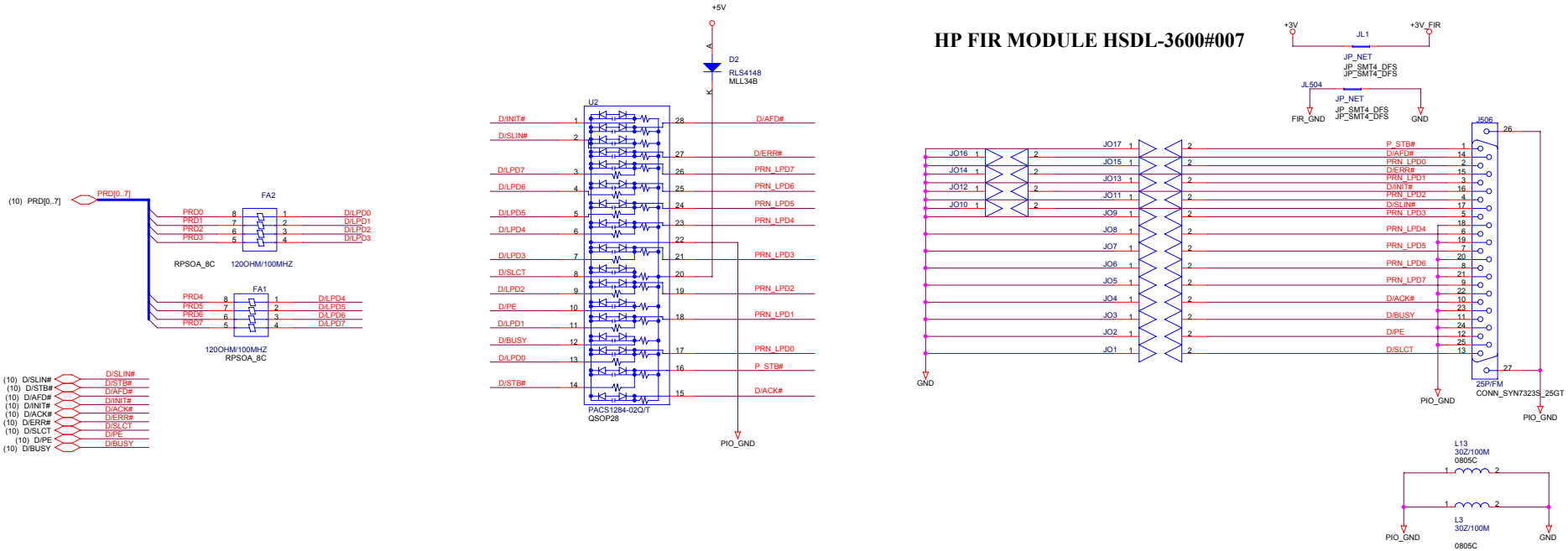
IR Mode Select

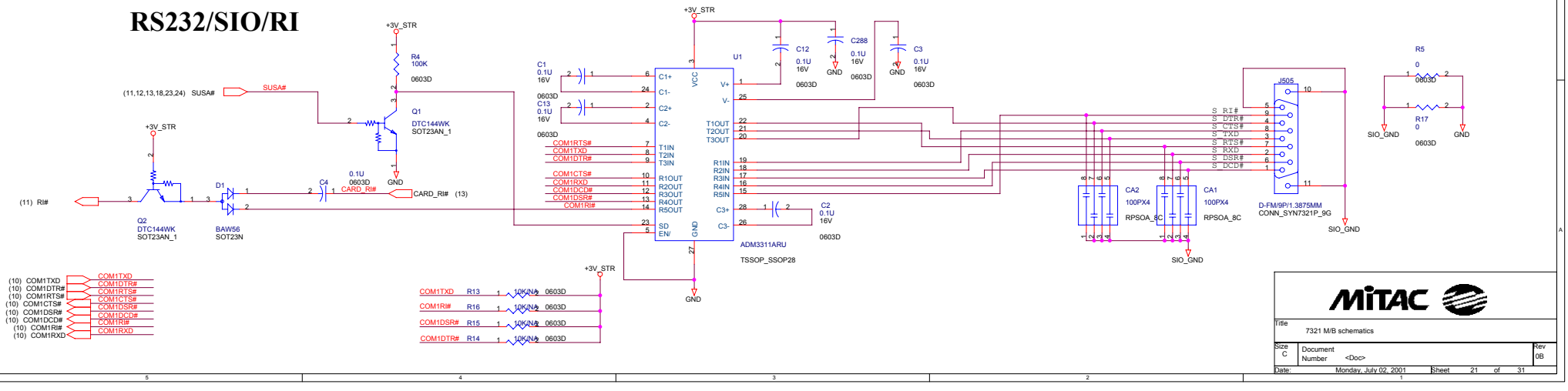
Mode 0	Mode 1	FIR_SEL	RX Function	TX Function
HI	LOW	X	Shutdown	Shutdown
LOW	LOW	LOW	SIR	Full Distance Power
LOW	HI	LOW	SIR	2/3 Distance Power
HI	HI	LOW	SIR	1/3 Distance Power
LOW	LOW	HI	MIR/FIR	Full Distance Power
LOW	HI	HI	MIR/FIR	2/3 Distance Power
HI	HI	HI	MIR/FIR	1/3 Distance Power



HP FIR MODULE HSDL-3600#007



RS232/SIO/RI



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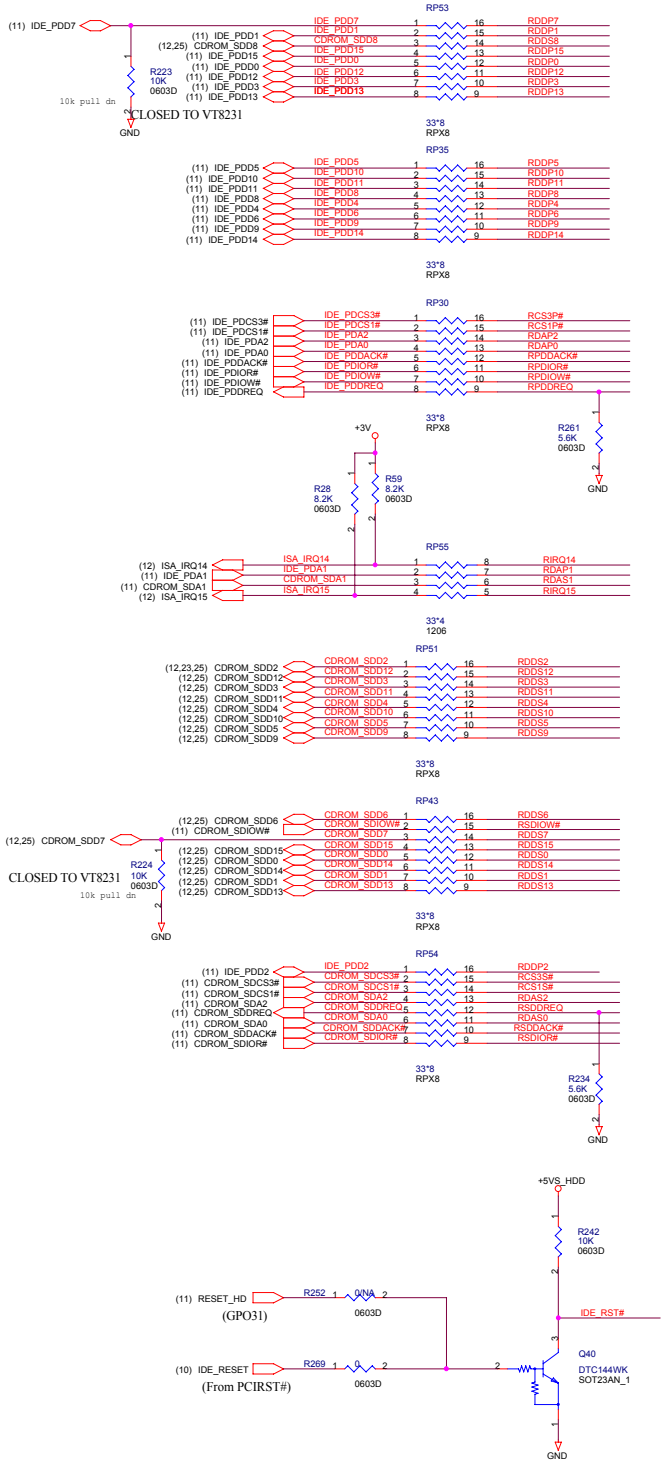
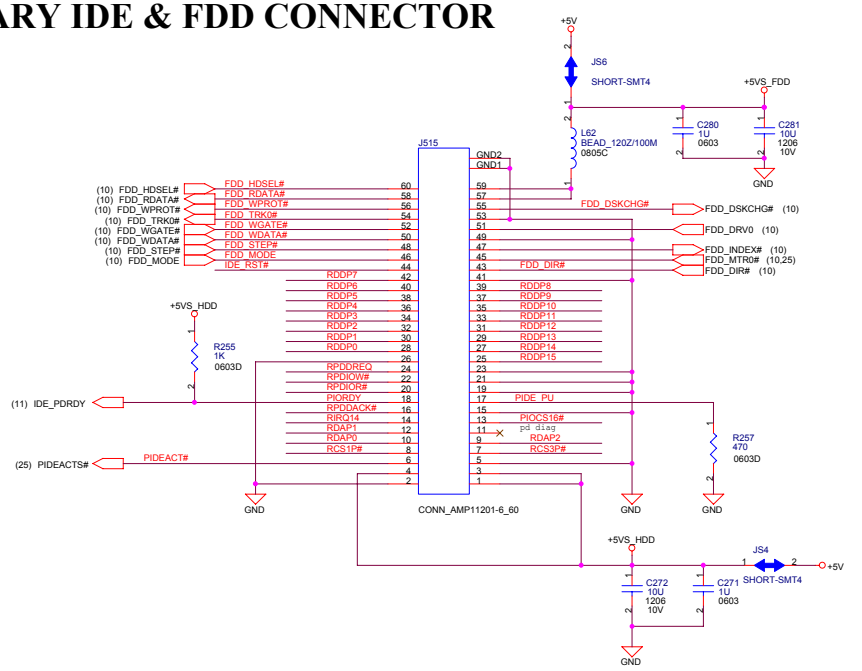
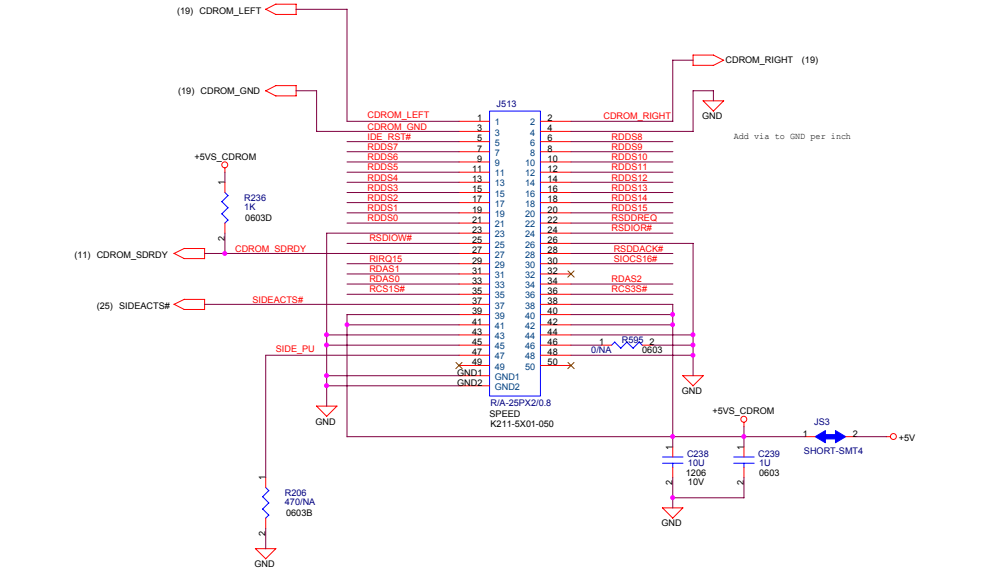
terminating resistors should be place close to South Bridge

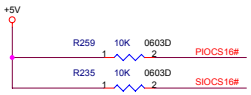


PRIMARY IDE & FDD CONNECTOR



SECONDARY IDE CONNECTOR





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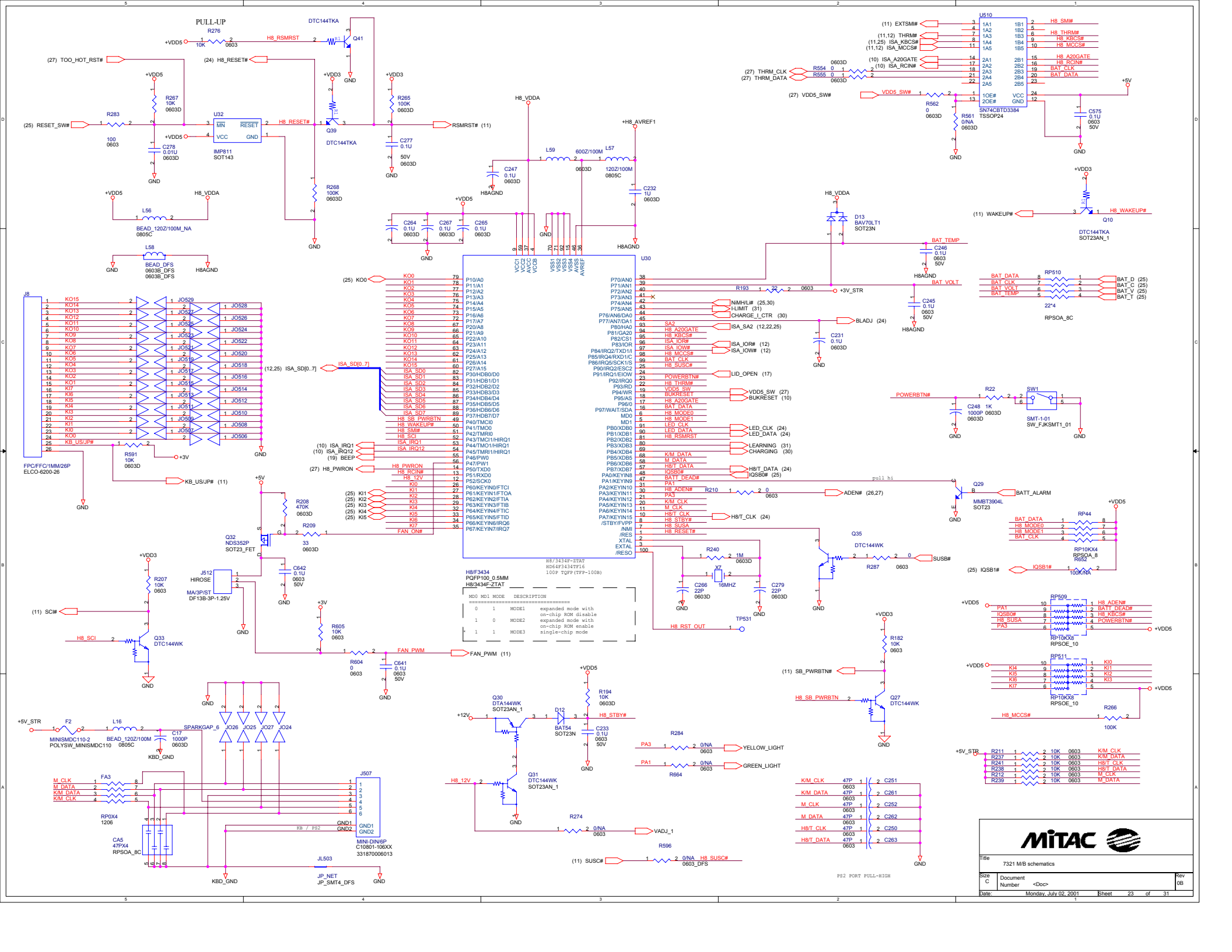
PULL-UP
R276
10K
0603
H8_RSMRST
DTC144TKA
Q41
(27) TOO_HOT_RST#
(24) H8_RESET#
+VDD5
+VDD3
GND
R267
10K
0603D
R265
100K
0603D
RSMRST# (11)
R283
100
0603
(25) RESET_SW#
U32
MIN
RESET
VCC
GND
IMP811
SOT143
H8_RESET#
Q39
DTC144TKA
C278
0.01U
0603D
C277
0.1U
50V
0603D
R268
100K
0603D
H8_VDDA
L56
BEAD_120Z/100M_NA
0805C
L58
BEAD_DFS
0603B_DFS
0603B_DFS
H8AGND
L59
600Z/100M
0603D
L57
120Z/100M
0805C
+H8_AVREF1
C247
0.1U
0603D
C232
1U
0603D
C264
0.1U
0603D
C267
0.1U
0603D
C265
0.1U
0603D
VCC1
VCC2
AVCC
VCCB
VSS1
VSS2
VSS3
VSS4
AVSS
AVREF
U30
H8/3434F-ZTAT
HD64F3434TF16
100P TQFP(TFP-100B)
H8/F3434
PQFP100_0.5MM
H8/3434F-ZTAT
MD0 MD1 MODE DESCRIPTION
0 1 MODE1 expanded mode with on-chip ROM disable
1 0 MODE2 expanded mode with on-chip ROM enable
1 1 MODE3 single-chip mode
(11) EXTSMI#
(11,12) THRM#
(11,25) ISA_KBCS#
(11,12) ISA_MCCS#
(10) ISA_A20GATE
(10) ISA_RCIN#
U510
SN74CBTD3384
TSSOP24
H8_SMI#
H8_THRM#
H8_KBCS#
H8_MCCS#
H8_A20GATE
H8_RCIN#
BAT_CLK
BAT_DATA
(27) THRM_CLK
(27) THRM_DATA
R554
R555
(27) VDD5_SW#
VDD5_SW#
R562
0
0603D
R561
0/NA
0603D
C575
0.1U
0603
50V
+5V
D13
BAV70LT1
SOT23N
BAT_TEMP
C246
0.1U
0603
50V
BAT_VOLT
C245
0.1U
0603
50V
H8AGND
R193
22
0603
+3V_STR
C231
0.1U
0603D
BLADJ (24)
NiMH/Li# (25,30)
LIMIT (31)
CHARGE_I_CTR (30)
SA2
ISA_SA2 (12,22,25)
H8_A20GATE
H8_KBCS#
ISA_IOR# (12)
ISA_IOW# (12)
H8_MCCS#
BAT_CLK
H8_SUSC#
LID_OPEN (17)
POWERBTN#
H8_THRM#
VDD5_SW
BUKRESET
VDD5_SW (27)
BUKRESET (10)
H8_A20GATE
BAT_DATA
H8_MODE0
H8_MODE1
LED_CLK
LED_DATA
H8_RSMRST
LEARNING (31)
CHARGING (30)
K/M_DATA
M_DATA
H8/T_DATA
IQSB0#
H8/T_DATA (24)
IQSB0# (25)
BATT_DEAD#
PA1
H8_ADEN#
PA3
K/M_CLK
M_CLK
H8/T_CLK
H8_STBY#
H8_SUSA
/NMI
H8_RESET#
/RES
XTAL
EXTAL
/RESO
H8/T_CLK (24)
R240
1M
0603D
X7
16MHZ
C266
22P
0603D
C279
22P
0603D
TP531
H8_RST_OUT
R210
0
0603
ADEN# (26,27)
pull hi
Q29
MMBT3904L
SOT23
BATT_ALARM
Q35
DTC144WK
R287
0603
SUSB#
BAT_DATA
BAT_CLK
BAT_VOLT
BAT_TEMP
R510
22*4
RPSOA_8C
BAT_D (25)
BAT_C (25)
BAT_V (25)
BAT_T (25)
POWERBTN#
R22
C248
1K
1000P
0603D
SW1
SMT-1-01
SW_FJKSMT1_01
RP44
H8_MODE0
H8_MODE1
BAT_CLK
RP10KX4
RPSOA_8
R552
100K/NA
IQSB1#
(25) IQSB1#
RP509
H8_ADEN#
BATT_DEAD#
H8_KBCS#
POWERBTN#
PA3
IQSB0#
H8_SUSA
PA1
RP10K8
RPSOE_10
RP511
KI0
KI1
KI2
KI3
KI4
KI5
KI6
KI7
RP10K8
RPSOE_10
R266
100K
H8_MCCS#
R182
10K
0603
(11) SB_PWRBTN#
H8_SB_PWRBTN
Q27
DTC144WK
K/M_CLK
K/M_DATA
M_CLK
M_DATA
H8/T_CLK
H8/T_DATA
47P
0603
C251
C261
C252
C262
C250
C263
R211
R237
R241
R238
R212
R239
10K
0603
K/M_CLK
K/M_DATA
H8/T_CLK
H8/T_DATA
M_CLK
M_DATA
PS2 PORT PULL-HIGH
(11) WAKEUP#
H8_WAKEUP#
Q10
DTC144TKA
SOT23AN_1
J8
FPC/FFC/1MM/26P
ELCO-6200-26
KO0
KO1
KO2
KO3
KO4
KO5
KO6
KO7
KO8
KO9
KO10
KO11
KO12
KO13
KO14
KO15
KI0
KI1
KI2
KI3
KI4
KI5
KI6
KI7
KB_US/JP#
R591
10K
0603D
+3V
KB_US/JP# (11)
JO506
JO507
JO508
JO509
JO510
JO511
JO512
JO513
JO514
JO515
JO516
JO517
JO518
JO519
JO520
JO521
JO522
JO523
JO524
JO525
JO526
JO527
JO528
JO529
(12,25) ISA_SD[0..7]
ISA_SD[0..7]
ISA_SD0
ISA_SD1
ISA_SD2
ISA_SD3
ISA_SD4
ISA_SD5
ISA_SD6
ISA_SD7
H8_SB_PWRBTN
H8_WAKEUP#
H8_SMI#
H8_SCI
ISA_IRQ1
ISA_IRQ12
(10) ISA_IRQ1
(10) ISA_IRQ12
(19) BEEP
(27) H8_PWRON
H8_PWRON
H8_RCIN#
H8_12V
P10/A0
P11/A1
P12/A2
P13/A3
P14/A4
P15/A5
P16/A6
P17/A7
P20/A8
P21/A9
P22/A10
P23/A11
P24/A12
P25/A13
P26/A14
P27/A15
P30/HDB0/D0
P31/HDB1/D1
P32/HDB2/D2
P33/HDB3/D3
P34/HDB4/D4
P35/HDB5/D5
P36/HDB6/D6
P37/HDB7/D7
P40/TMCI0
P41/TMO0
P42/TMRI0
P43/TMCI1/HIRQ1
P44/TMO1/HIRQ1
P45/TMRI1/HIRQ1
P46/PW0
P47/PW1
P50/TXD0
P51/RXD0
P52/SCK0
P60/KEYIN0/FTCI
P61/KEYIN1/FTOA
P62/KEYIN2/FTIA
P63/KEYIN3/FTIB
P64/KEYIN4/FTIC
P65/KEYIN5/FTID
P66/KEYIN6/IRQ6
P67/KEYIN7/IRQ7
P70/AN0
P71/AN1
P72/AN2
P73/AN3
P74/AN4
P75/AN5
P76/AN6/DA0
P77/AN7/DA1
P80/HA0
P81/GA20
P82/CS1
P83/IOR
P84/IRQ2/TXD1/I
P85/IRQ4/RXD1/IC
P86/IRQ5/SCK1/S
P90/IRQ2/ESC2
P91/IRQ1/EIOW
P92/IRQ0
P93/RD
P94/WR
P95/AS
P96/0
P97/WAIT/SDA
MD0
MD1
P80/XDB0
P81/XDB1
P82/XDB2
P83/XDB3
P84/XDB4
P85/XDB5
P86/XDB6
P87/XDB7
PA0/KEYIN8
PA1/KEYIN9
PA2/KEYIN10
PA3/KEYIN11
PA4/KEYIN12
PA5/KEYIN13
PA6/KEYIN14
PA7/KEYIN15
/STBY/FVPP
R208
470K
0603D
R209
33
0603D
Q32
NDS352P
SOT23_FET
C642
0.1U
0603
50V
J512
HIROSE
MA/3P/ST
DF13B-3P-1.25V
(11) SC#
H8_SCI
Q33
DTC144WK
R207
10K
0603
R605
10K
0603
R604
0
0603
C641
0.1U
0603
50V
FAN_PWM
FAN_PWM (11)
FAN_ON#
+5V_STR
F2
MINISMDC110-2
POLYSW_MINISMDC110
L16
BEAD_120Z/100M
0805C
C17
1000P
0603D
KBD_GND
SPARKGAP_6
JO26
JO25
JO27
JO24
FA3
M_CLK
M_DATA
K/M_DATA
K/M_CLK
RP0X4
1206
CA5
47PX4
RPSOA_8C
J507
MINI-DIN/6P
C10801-106XX
331870006013
KB / PS2
GND1
GND2
JL503
JP_NET
JP_SMT4_DFS
Q30
DTA144WK
SOT23AN_1
+12V
D12
BAT54
SOT23N
R194
10K
0603D
C233
0.1U
0603
50V
H8_STBY#
R284
PA3
0/NA
0603
YELLOW_LIGHT
R664
PA1
0/NA
0603
GREEN_LIGHT
Q31
DTC144WK
SOT23AN_1
H8_12V
R274
0/NA
0603
VADJ_1
R596
(11) SUSC#
0/NA
H8_SUSC#
0603_DFS
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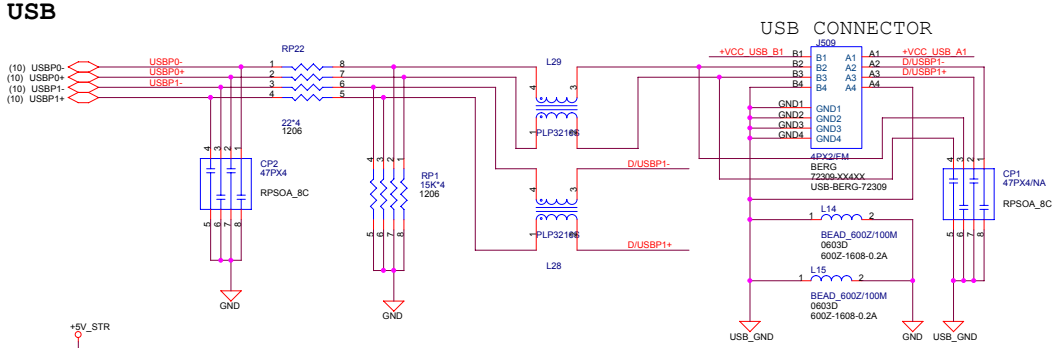
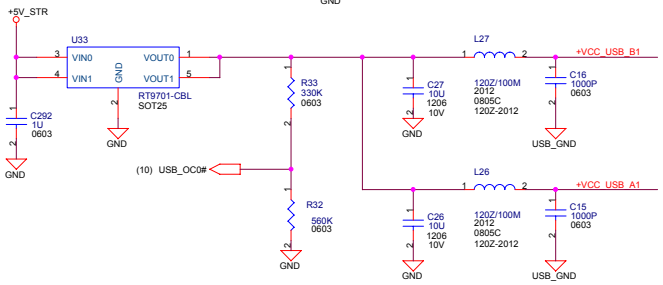
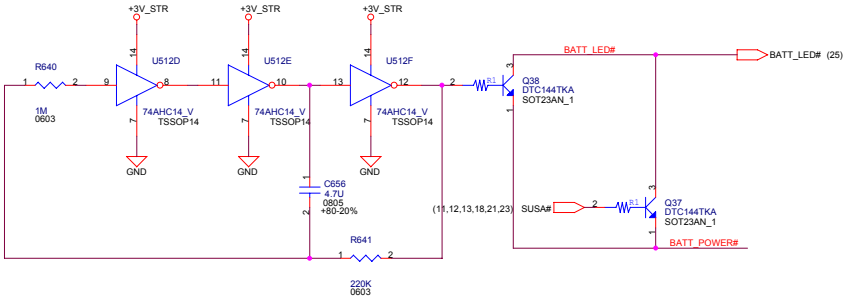
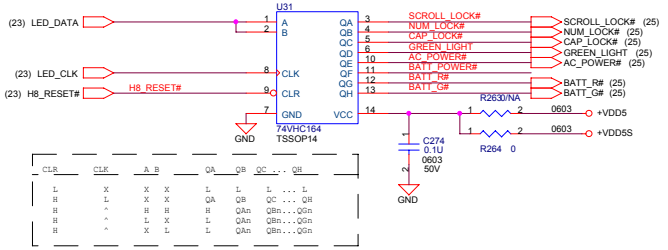
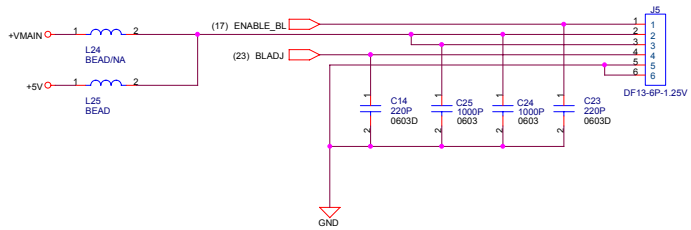
USB

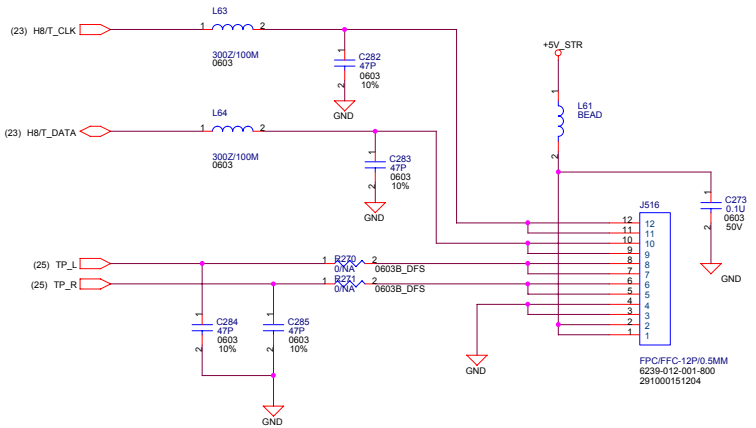












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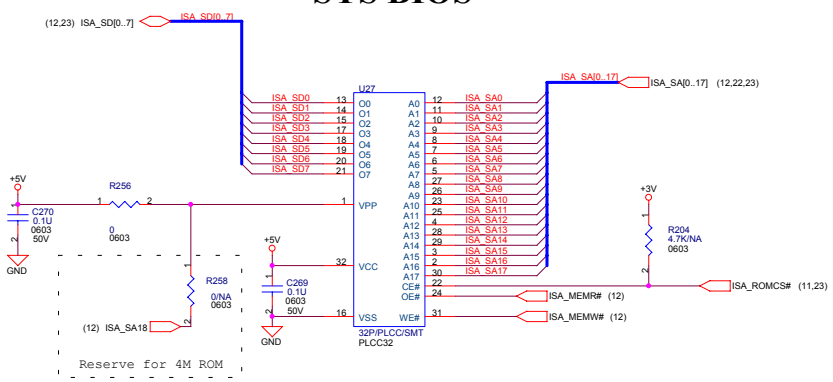
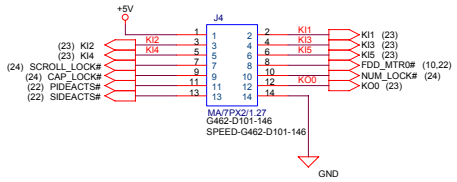
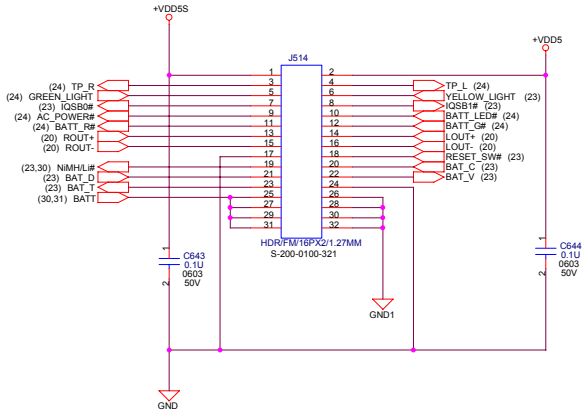
SYS BIOS



QSB & LED connector



Charger board connector



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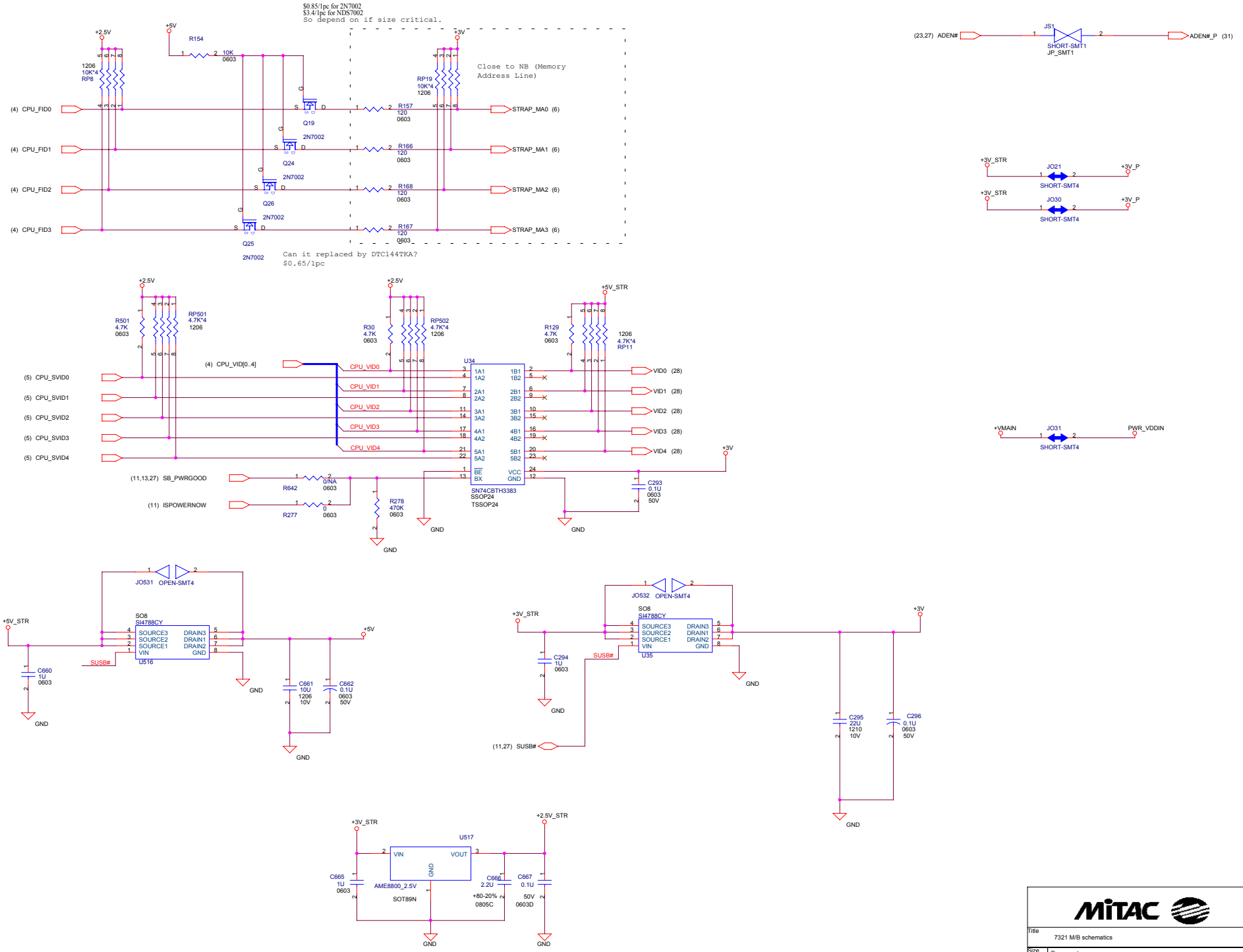
$0.85/1pc for 2N7002
$3.4/1pc for NDS7002
So depend on if size critical.
Close to NB (Memory Address Line)
Can it replaced by DTC144TKA?
$0.65/1pc
(23,27) ADEN#
ADEN#_P (31)
JS1
SHORT-SMT1
JP_SMT1
+3V_STR
+3V_P
JO21
JO30
SHORT-SMT4
+VMAIN
PWR_VDDIN
JO31
(4) CPU_FID0
(4) CPU_FID1
(4) CPU_FID2
(4) CPU_FID3
STRAP_MA0 (6)
STRAP_MA1 (6)
STRAP_MA2 (6)
STRAP_MA3 (6)
R154
10K
0603
RP8
1206
10K*4
RP19
R157
R166
R168
R167
120
Q19
Q24
Q26
Q25
2N7002
(4) CPU_VID[0..4]
(5) CPU_SVID0
(5) CPU_SVID1
(5) CPU_SVID2
(5) CPU_SVID3
(5) CPU_SVID4
R501
4.7K
RP501
4.7K*4
R30
RP502
R129
RP11
CPU_VID0
CPU_VID1
CPU_VID2
CPU_VID3
CPU_VID4
U34
SN74CBTH3383
SSOP24
TSSOP24
VID0 (28)
VID1 (28)
VID2 (28)
VID3 (28)
VID4 (28)
(11,13,27) SB_PWRGOOD
(11) ISPOWERNOW
R642
0/NA
R277
R278
470K
C293
0.1U
50V
GND
JO531 OPEN-SMT4
JO532 OPEN-SMT4
SO8
SI4788CY
SOURCE3
SOURCE2
SOURCE1
VIN
DRAIN3
DRAIN1
DRAIN2
U516
U35
SUSB#
C660
1U
C661
10U
1206
10V
C662
C294
C295
22U
1210
C296
(11,27) SUSB#
U517
AME8800_2.5V
SOT89N
VIN
VOUT
C665
C666
2.2U
+80-20%
0805C
C667
50V
0603D
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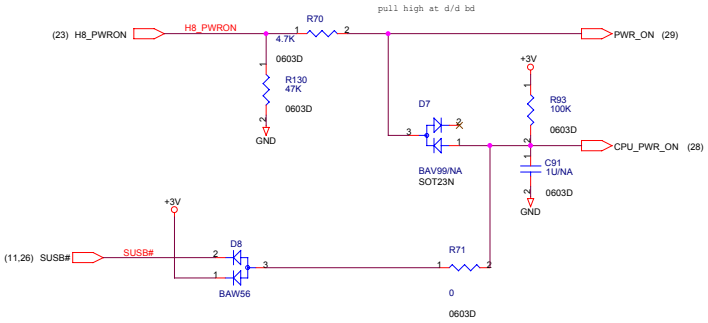
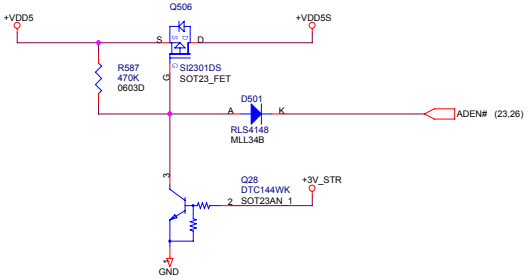
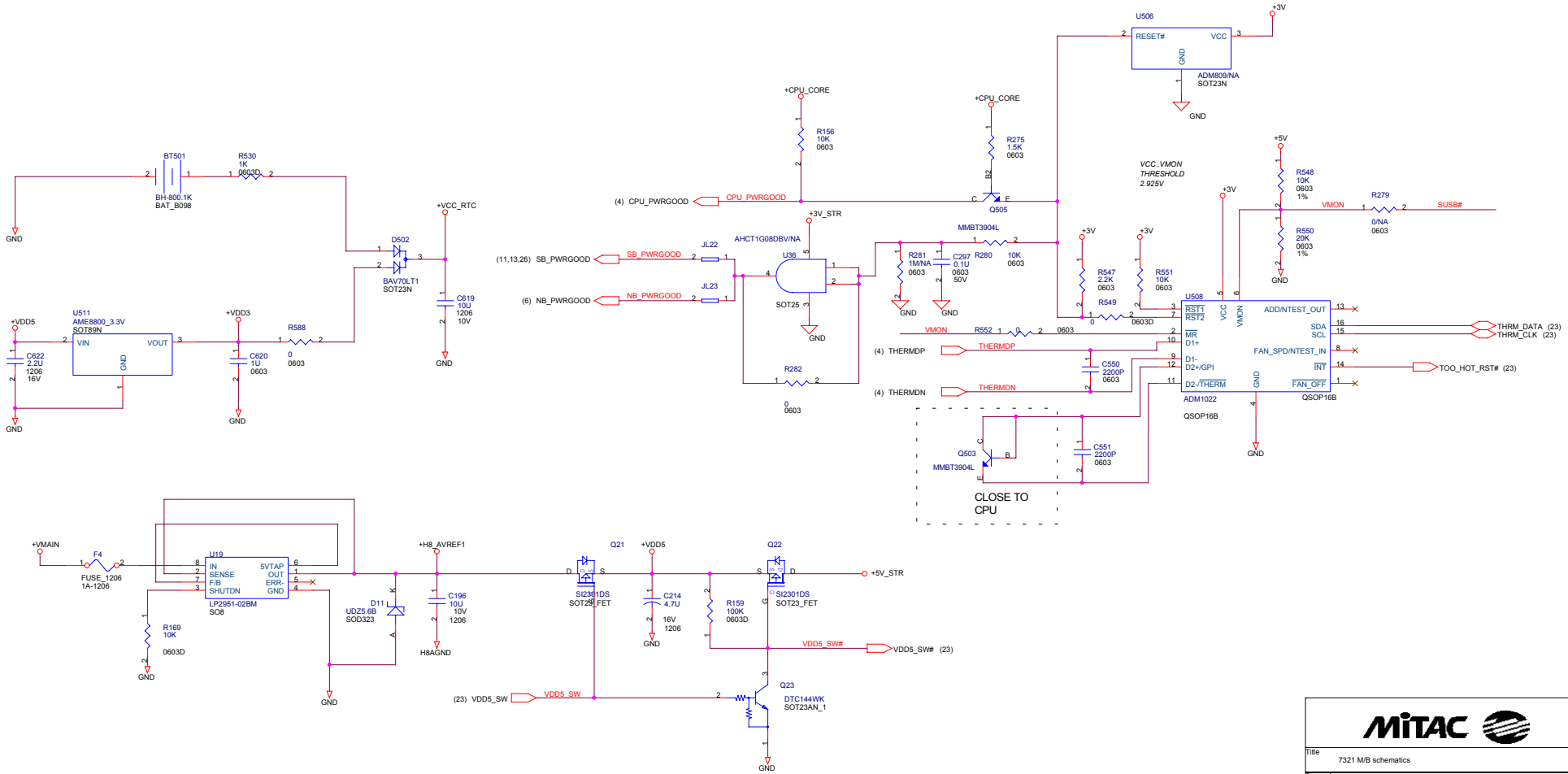


STR worked at cpu power off and others do not.





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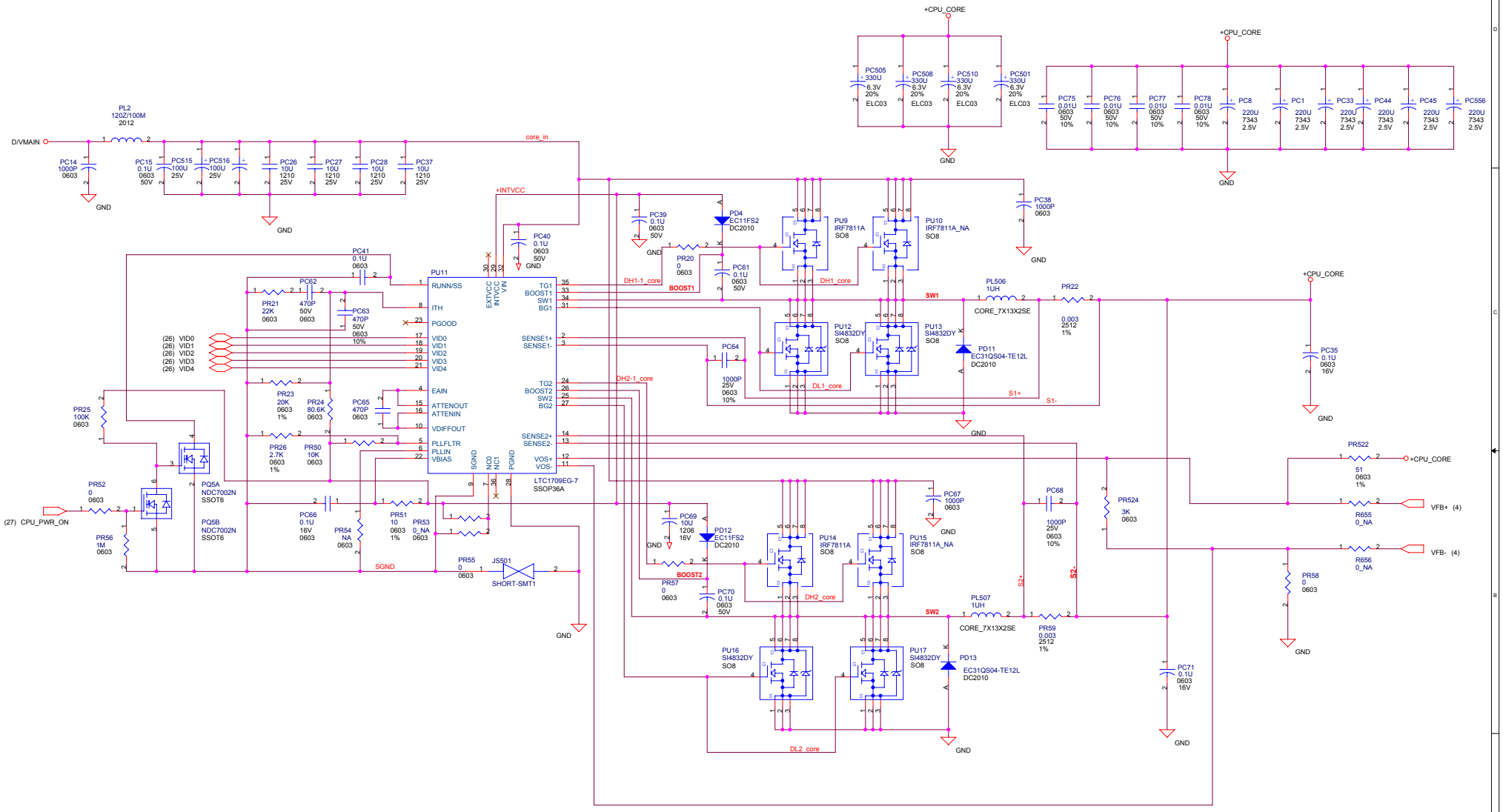

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Title	7321 CPU VCORE POWER	
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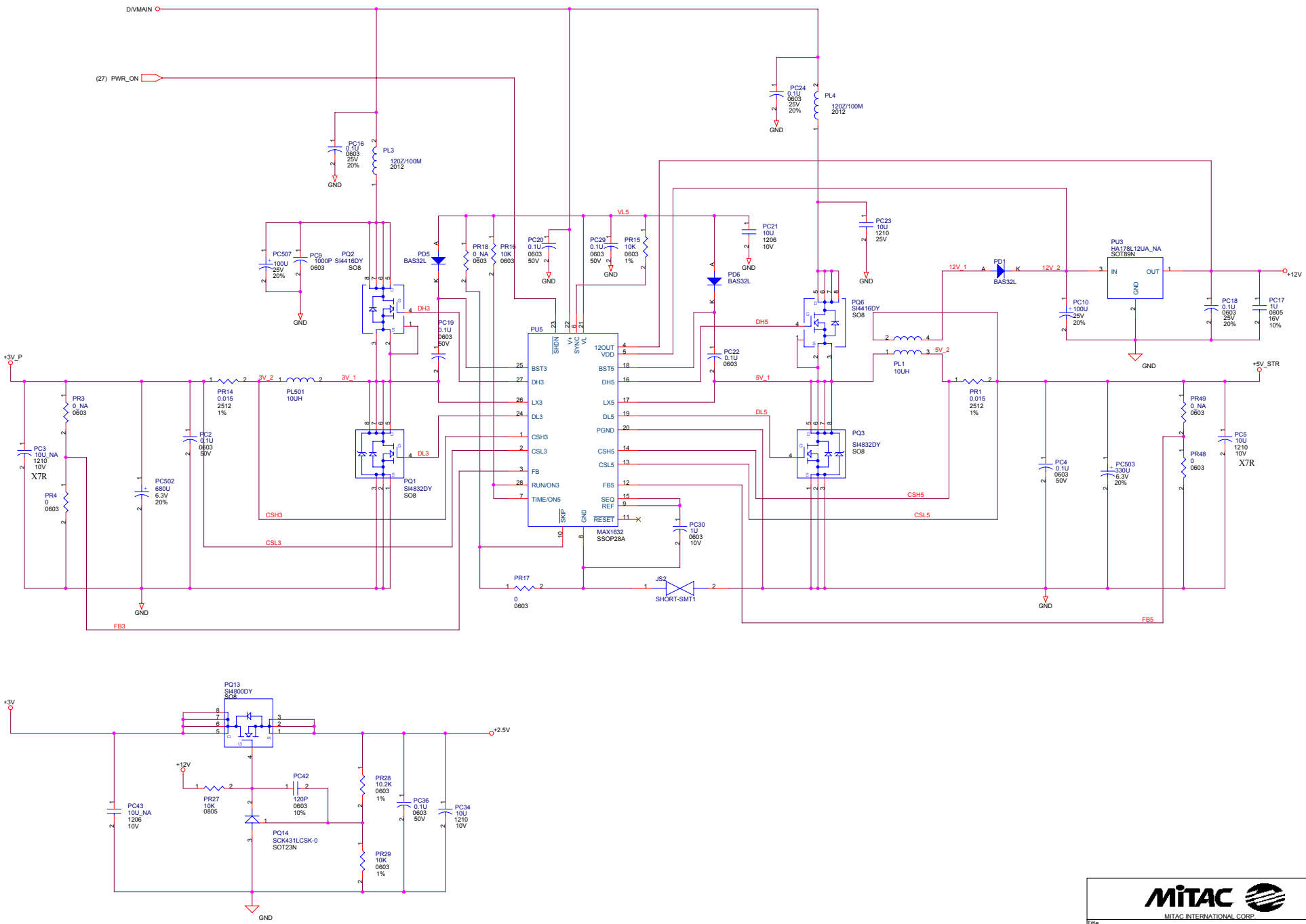

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Title	7321 +3V/+5V/+12V Power	
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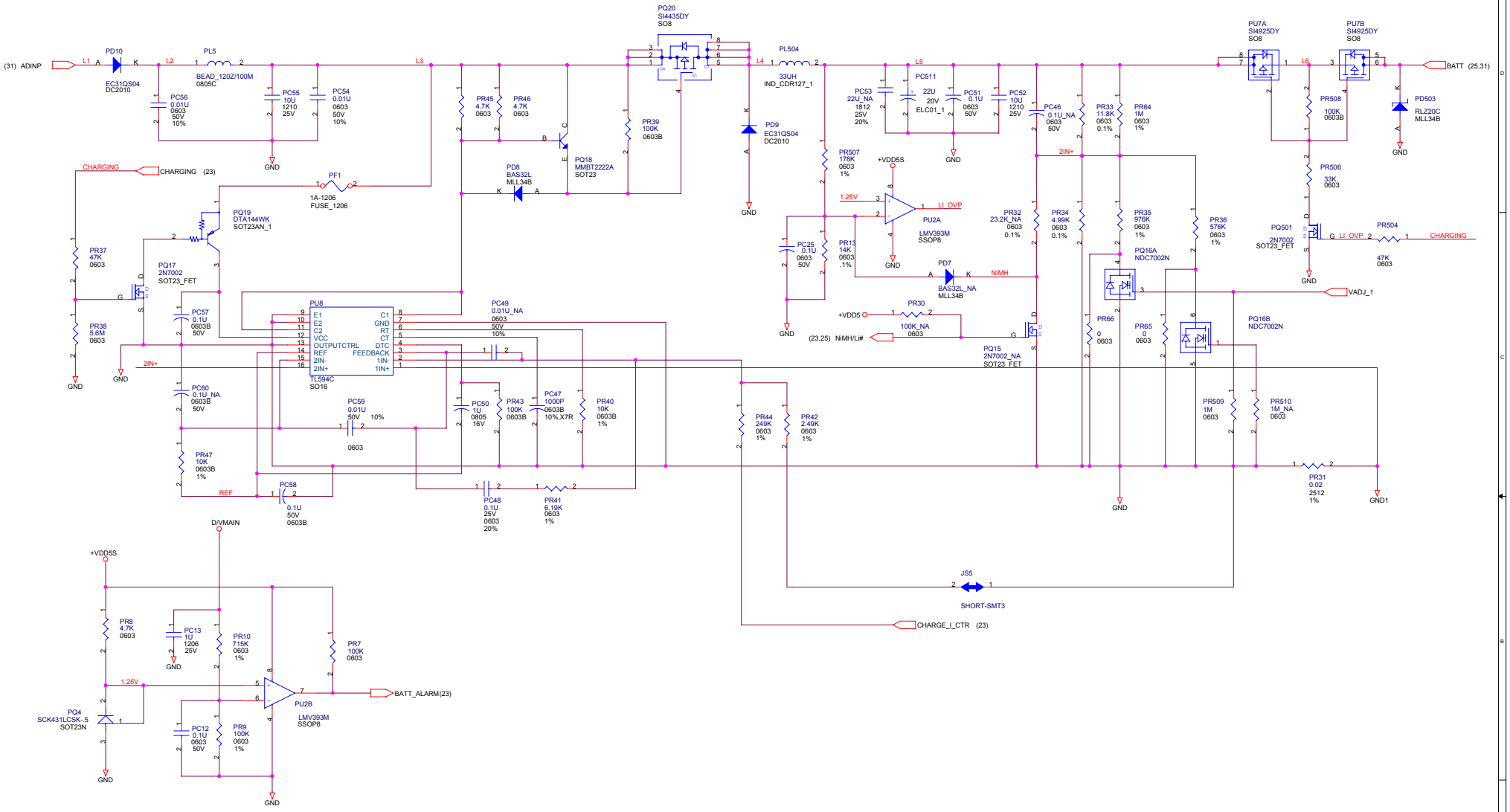

VADJ_1_P

16.7V	0
16.75V	1

MiTAC

Title: 7321 Charger

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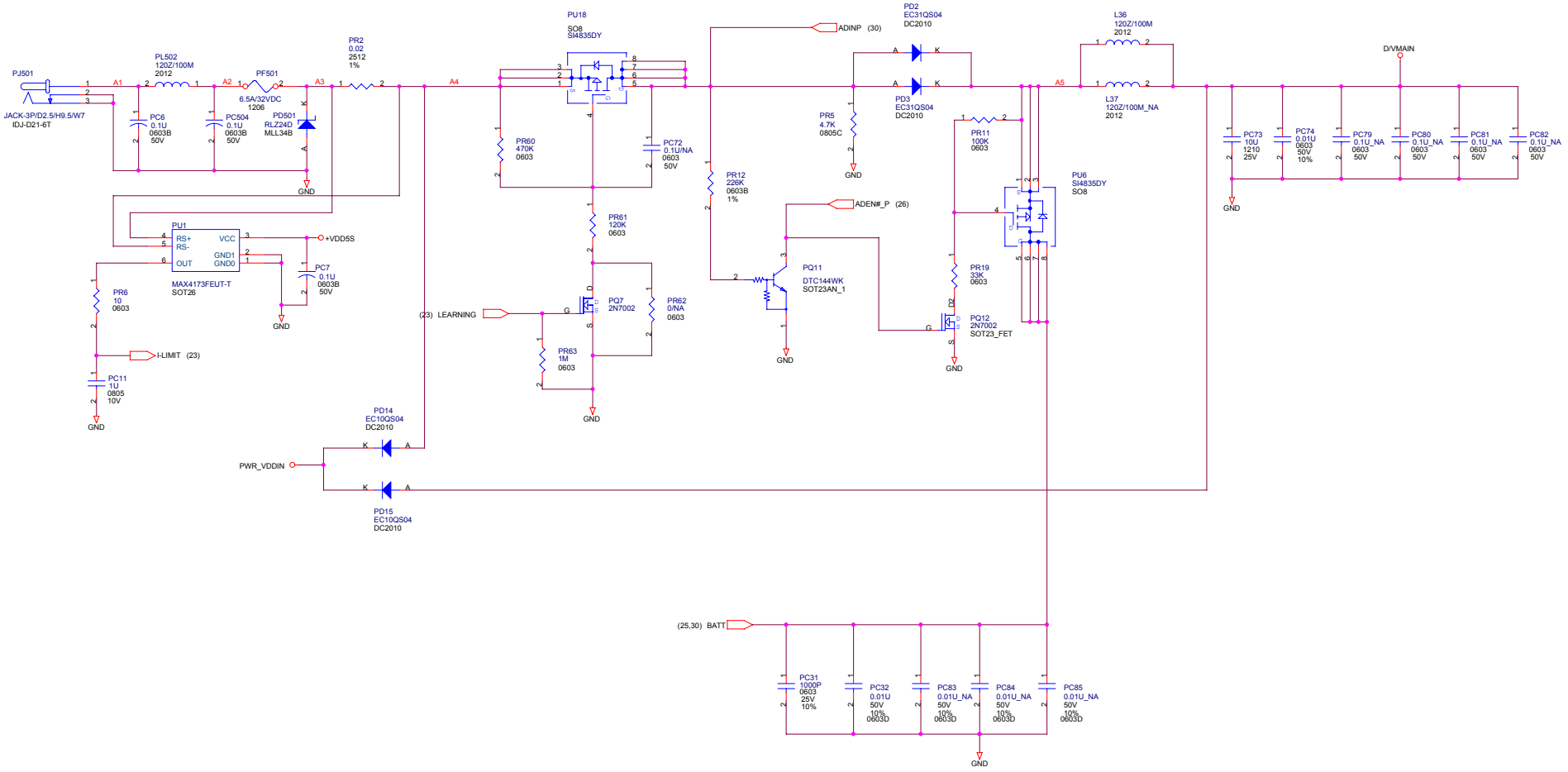

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Title: 7321 ADINP & Discharger

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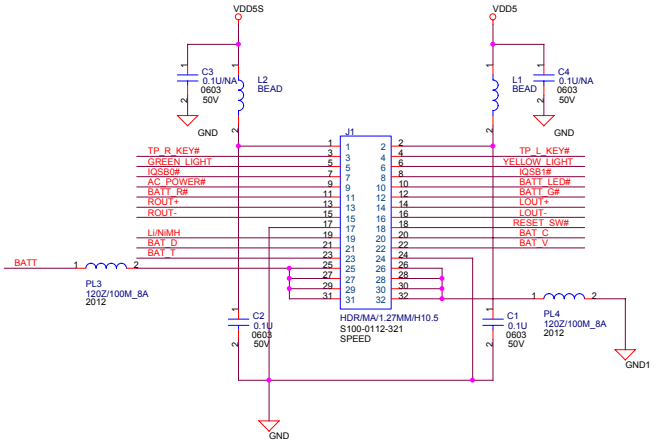
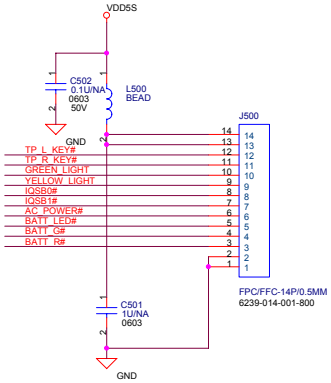
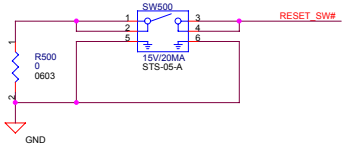
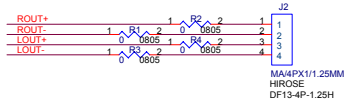
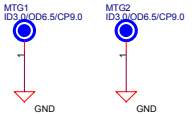
REV	DESCRIPTION OF CHANGE	ECR	DATE
R00			05/26/2000
R0A	1.Relayout base on R00 2.Correcting J1 shape library.		06/16/2000
R0B	1.Relayout base on R0A 2.Add SW1 for H8 RESET function 3.Add PL3 & PL4 for EMI issue 4.Add capacitors for Power issue		07/04/2000
R01	1.Relayout base on R0b 2.Remove one of VDD5S circuit 3.Change PF2 from 6.5A/32V to 125V/5A		08/15/2000
R02	1.Change PF2 from 125V/5A to 7A/24VDC		10/26/2000

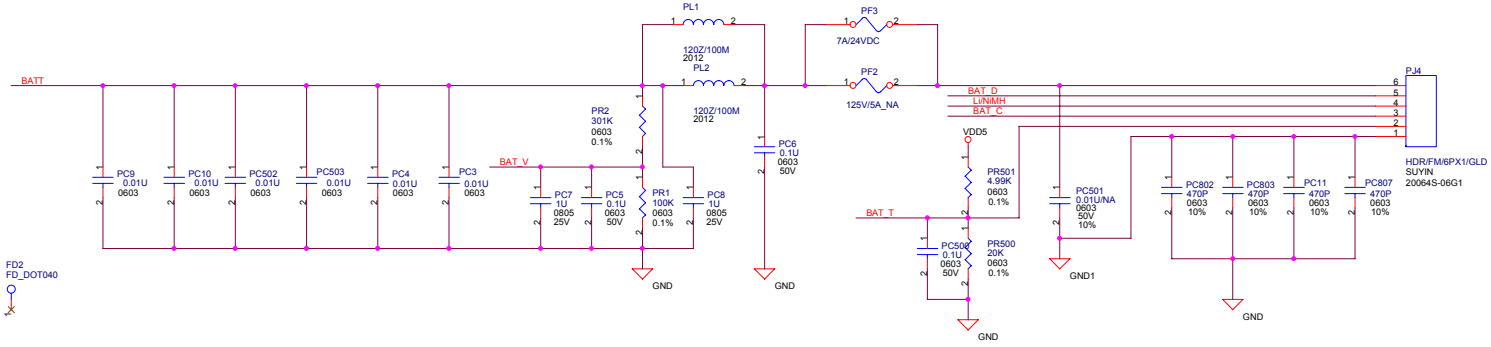


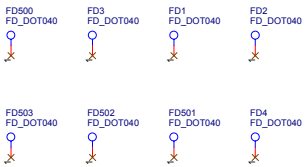












DRAWN	DESIGN	CHECK	ISSUES

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Title: 7521P charger bd

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Reference Material

- **Mobil AMD K7 Processor** ..... ***AMD.INC.***
- **VIA VT8362 North Bridge with S3 Savage4 AGPX4** ..... ***VIA.INC.***
- **VIA VT8231 BGA PCI-LPC/ISA South Bridge** ..... ***VIA.INC.***
- **PC Card Interface controller** ***T1.INC.***
- **7321 Engineer Hardware Specification** ..... ***Technology Corp/MiTAC***
- **7321 Software Engineering Specification** ..... ***Technology Corp/MiTAC***

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Sponsoring Editor : Jesse Jan

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TEL : 886-3- 5645850 Fax : 886-3- 5781245

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E-mail : Willy.Chen @ mic.com.tw

Web : http: //www.mitac.com http: //www.mitacservice.com