7233 N/B MAINTENANCE

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0 Introduction

0.1 General Description

This document describes the engineering specification for 7233 portable notebook computer system.

0.2 System Overview

This system is based on PCI architecture and is fully compatible with IBM PC/AT specification, which have standard hardware peripheral interface and support Intel Pentium family. The power management complies with Advanced Configuration and Power Interface (ACPI) 1.0. It also provides easy configuration through CMOS setup which is built in system BIOS software and can be pop-up by pressing F2 at system start up or warm reset. System also provides icon LEDs to display system status, such as AC Power indicator, FDD, HDD, NUM LOCK, CAP LOCK, SCROLL LOCK, SUSPEND MODE and battery present, capacity & charging status. It also equipped with Zoom Video capture port, FIR, USB port, 3D stereo audio functions.

The 7233 model motherboard will accept Intel Mobile Pentium III / Celeron processors in uPGA2 package operating at 450/500 MHz (Intel Pentium III processor w/o Geyserville technology)and 600/650/700 MHz (Intel Pentium III processor w/ Geyserville technology),450/500/550 MHz(Intel Celeron processor) with a system bus speed of 100 MHz. The integrated L2 cache is designed to help improve performance, it complement the system bus by providing critical data faster and reducing total system power consumption.

The memory subsystem supports 32MB SDRAM on board and one 144-pin SDRAM SO-DIMM module for upgrading up to 128 MB.

The Intel 440BX AGPset brings third important firsts to the mobile PC environment: (1) Concurrent PCI (PCI 2.1) reduces CPU latencies for smoother video and more realistic audio; (2) Universal Serial Bus (USB) technology makes Plug and Play peripheral connections a reality.(3)Accelerated Graphics Port (AGP) specification, Rev 1.0 (4/12/96) support up to 2X. The Intel 440BX AGPset also contains an integrated PCI Bus Mastering IDE controller with two high performance IDE interfaces and supports " Ultra 33 " synchronous DMA mode which transfers up to 33 Mbytes per second. In addition, the 440BX AGPset supports Intel's new Dynamic Power Management Architecture (DPMA) for consuming less power consumption than earlier PCIset designs and supports Advanced Configuration and Power Interface (ACPI) 1.0 for longer battery life in mobile systems.

The ATI 3D RAGE LT PRO VGA controller provides LCD,CRT and supports 2D and 3D acceleration ,ZV port,66MHz SGRAM,DVD, ACPI power management ,integrated LVDS…etc. The TI 1225 cardbus controller supports PCMCIA and CARDBUS. The National Semiconductor PC97338 Super I/O controller integrates the standard PC I/O functions: floppy interface, two FIFO serial ports, one EPP/ECP capable parallel port, and support for an IrDA 1.1, 1.0 and sharp ASK compatible infrared interface. To provide for the increasing number of multimedia applications, an

Maestro-2 audio controller and the CODEC CS4297 is integrated onto the motherboard both. The Maestro-2 provides 16-bit stereo, Sound Blaster Pro and Windows Sound System compatibility and full-duplex capabilities to meet the demands of interactive multimedia applications

A full set of software drivers and utilities are available to allow advanced operating systems such as Windows 95 or Windows 98 to take full advantage of the hardware capabilities. Features such as bus mastering IDE, Windows 95-ready Plug N' Play, Advanced Power Management (APM) with application restart, software-controlled power shutdown.

Following chapters will have more detail description for each individual sub-systems and functions

Hardware System

0.3 System parts

- Central Processing Unit : Intel Mobile Pentium III / Celeron microproceessor in uPGA2 package .
- Intel 440BX AGPset Host bridge with DRAM controller
- PIIX4M: PCI/ISA bridge with IDE/USB/PMU controller
- Video Controller: ATi 3D Rage LT Pro 328-pin BGA
- Super I/O Controller: NS PC97338VJG
- PCMCIA Interface Controller: TI 1225
- Keyboard System: H8(3434) UNIVERSAL KEYBOARD CONTROLLER
- 3D Audio System: EES Maestro-2 PQFP100 AND CODEC CS4297 FIR port: HP HSDL-3600#007 FIR module
- FAX/MODEM:ASKEY 56Kbps Fax Modem , Software Modem

0.4 CPU

The Intel Mobile Pentium III processor will be offered at 450 MHz, 500 MHz with a system bus speed of 100 MHz. The 500 MHz processor will also be offered at a later date to run at higher frequency (600 MHz and 650 MHz) using Geyserville technology , which enables the CPU to switch bus ratios and core speeds without being reset . The Mobile Celeron processor is the first mobile processor with an integrated L2 cache among the Celeron processors. The Mobile Celeron processor will initially be offered at 450 MHz , 500 MHz and 550MHz with a system bus speed of 100 MHz. It consists of a Mobile Pentium III/Celeron processor with an integrated L2 cache and a 64-bit high performance system bus. The integrated L2 cache is designed to help improve performance, it complements the system bus by providing critical data faster and reducing total system power consumption. The Mobile Pentium III/Celeron processor 64-bit wide Low Power Gunning Transceiver Logic (GTL+) system bus is compatible with the 440BX AGPSet, and provides a glue-less, point-to-point interface for an I/O bridge/memory controller.

0.5 Intel 440BX AGPset

0.5.1 Intel 440BX AGPset Host Bridge

- Support Full Symmetric Multiprocessor Protocol for up to two processors
- 64-bit GTL+ based Host Bus Interface
- 32-bit Host address Support
- 64-bit Main Memory Interface with optimized support for SDRAM at 100 and 66/60 MHz
- 32-bit Primary PCI Bus Interface (PCI0) with integrated PCI arbiter
- AGP Interface (PCI1/AGP) with 133 MHz data transfer capability configurable as a Secondary PCI Bus
- Extensive Data Buffering between all interfaces for high throughput and concurrent operations
- Processor/host bus support
  - Optimized for Pentium II processor at 100 MHz host bus frequency; Support for 66 MHz
  - In-order transaction and dynamic deferred transaction support
  - Desktop optimized GTL+ bus driver technology (gated GTL+ receivers for reduced power)
- Integrated DRAM controller
  - 8 to 256Mbytes
  - Supports up to 4 double-sided DIMMs (8 rows memory)
  - 64-bit data interface with ECC support (SDRAM only)
  - Standard and Registered SDRAM (Synchronous) DRAM Support (x-1- 1-1 access @ 66 MHz , x-1-1-1 access @ 100MHz)
  - Enhanced SDRAM Open Page Architecture Support for 16- and 64-Mbit DRAM devices with 2k, 4k and 8k page sizes
- PCI bus interface
  - PCI Rev. 2.1, 5V, 33MHz interface compliant
  - PCI Parity Generation Support
  - Data streaming support from PCI to DRAM
  - Delayed Transaction support for PCI-DRAM Reads
  - Supports concurrent CPU, AGP and PCI transactions to main memory
- AGP interface
  - Supports single AGP compliant device (AGP-66/133 3.3V device)
  - AGP Specification Rev 1.0 compliant
  - AGP-data/transaction flow optimized arbitration mechanism
  - AGP side-band interface for efficient request pipelining without interfering with the data streams
  - AGP-specific data buffering
  - Supports concurrent CPU, AGP and PCI transactions to main memory
  - AGP high-priority transactions (" expedite")support
- Power Management Functions
  - Stop Clock Grant and Halt special cycle translation (host to PCI Bus)
  - Dynamic power down of idle DRAM rows
  - Independent, internal dynamic clock gating reduces average power dissipation
- Packaging/Voltage
  - 492 Pin BGA
  - 3.3V core and mixed 5V,3.3V and GTL I/O
- Supporting I/O Bridge
  - System Management Bus (SMB) with support for DIMM Serial Presence Detect (SPD)
  - PCI-ISA Bridge (PIIX4E)
  - 3.3V core and mixed 5V, 3.3V I/O and interface to the 2.5V CPU signals via open-drain output buffers

0.5.2 Intel PIIX4M (82371MB)

- Supported Kits for both Pentium and Pentium II Microprocessors
  - 82430TX ISA Kit
  - 82440LX ISA/DP Kit
- Multifunction PCI to ISA Bridge
  - Supports PCI at 30 MHz and 33 MHz
  - Supports PCI Rev 2.1 Specification
  - Supports Full ISA or Extended I/O (EIO) Bus
  - Supports full Positive Decode or Subtractive Decode of PCI
  - Supports ISA/EIO at 1/4 of PCI Frequency
- Supports Both Mobile and Desktop Deep Green Environments
  - 3.3V Operation With 5V Tolerant Buffers
  - Ultra-Low Power for Mobile Environments
  - Power-On Suspend and Soft-OFF for Desktop Environment
  - All Registers Readable/Restorable for Proper Resume From 0.V Suspend
- Power Management Logic
  - Global and Local Device Management
  - Suspend and Resume Logic
  - Supports Thermal Alarm
  - Support for External Microcontroller
  - Full Support for Advanced Configuration and Power Interface (ACPI) Revision 1.0 Specification and OS Directed Power Management
- Integrated IDE Controller
  - Independent Timing of Up to 4 Drives
  - PIO Mode 4 Transfers Up to 14 Mbytes/sec
  - Supports " Ultra DMA/33" Synchronous DMA Mode Transfers Up to 33 Mbytes/sec
  - Integrated 16 x 32-Bit Buffer for IDE PCI Burst Transfers
  - Supports Glue-Less " Swap-Bay" Option With Full Electrical Isolation
- Enhanced DMA Controller
  - Two 82C37 DMA Controllers
  - Supports PCI DMA With 3 PC/PCI Channels and Distributed DMA Protocols (Simultaneously)
  - Fast Type-F DMA for Reduced PCI Bus Usage
- Interrupt Controller Based on Two 82C59
  - 15 Interrupt Support
  - Independently Programmable for Edge/Level Sensitivity
  - Supports Optional I/O APIC
  - Serial Interrupt Input
- Timers based on 82C54
  - System Timer, Refresh Request, Speaker Tone Output
- USB
  - Two USB 1.0 Ports for Serial Transfers at 12 or 1.5 Mbit/sec
  - Supports Legacy Keyboard and Mouse Software With USB-Based Keyboard and Mouse Supports UHCI Design Guide Revision 1.1 Interface
- SMBus
  - Host interface Allows CPU to Communicate via SMBus
  - Slave Interface Allows External SMBus Master to Control Resume Events
- Real-Time Clock
  - 256-Byte Battery-Back CMOS SRAM
  - Includes Date Alarm
  - Two 8-Byte Lockout Ranges
- Microsoft Windows* 95 Compliant
- 324 mBGA Package

0.6 VGA Controller: ATI 3D RAGE LT PRO

- Supports AGP 1X and AGP 2X (133 MHz)
  - Supports AGP's pipelined sideband protocol.
  - Support dual CRT controller
  - Dual independent displays (LCD/CRT, CD/TV, CRT/TV).
  - Second triple-DAC for TV allows displays likes CRT+TV/LCD, LCD+TV/CRT, LCD+CRT/TV and the resolutions, refresh rates and display data can be completely independent .
- Primary display path supports:
  - VGA and accelerated modes
  - Video overlay
  - Hardware cursor and hardware icon
  - Palette gamma correction.
- Supports both independent displays at 1024 x 768, 24bpp, 75Hz (see mode tables for details).
- Secondary display path supports:
  - Accelerated modes
  - YUV422 video data
  - 24-bit palette
- Video genlocking supported for both CRTCs.
- Integrated dual 65MHz LVDS interface
  - Up to 10 LVDS channels for power and EMI reduction.
  - Dual pixel SXGA resolution TFT panels
  - XGA resolution DSTN panels.
  - 24bpp TFT (SGA/XGA) using dual pixel LVDS (versus 18 bpp using direct digital interface).
  - 455 Mbps/channel with 65 MHz pixel clock rate.
  - DSTN-120Hz XGA (1024 x 768 60Hz) and 170 Hz SVGA (800 x 600 85Hz)
  - 3 pairs (+1 clock) and 4 pairs (+1 clock) modes for both single and dual pixel LVDS.
  - FPDI-2 compliant; compatible with receivers from National Semiconductor, Texas Instruments, and THine.
  - LVDS eye pattern to improve testability of LVDS module.
- Flat panel power management:
  - Automatic power down panel by programmable internal timer
  - Standby/Suspend pins for hardware Power Management support.
  - Standby/Suspend registers for software Power Management support.
- Flat panel support:
  - Color STN/DSTN/CSTN LCD panels up to XGA (1024 x 768) resolution, up to 16MHz refresh rate, up to 256k colors on an 8-color panel.
  - Color TFT panel up to 1600 x 1280 resolution, up to 24-bit per pixel, single/double pixel per clock.
  - 2/4 levels of frame modulation can be done on 9-bit, 12-bit and 18-bit TFT panels.
  - Hardware Z-buffer support with both DSTN and TFT panels.
  - Integrated LVDS interface support.
  - Support for Panel Link Interface.
  - Support external Panel Link transmitter.
  - Panel ID to allow multiple panel support without swapping BIOS.
  - Five bits allocated for panel ID.
  - DDC support for LCD monitors.
  - General purpose I/O pins available to support DDC on LCD monitor

applications.

- Integrated a floating-point set-up engine
  - processing up to 1.2 million triangles per send.
- Supports 66 MHz SGRAM:
  - 64-bit, 66MHz SGRAM interface
  - 800 MB/s of low-latency frame buffer bandwidth
- ZV Port (PCMCIA compliant with CCIR601 timing)
  - Allows transfer of video data directly into frame buffer without loading down PCI bus.
  - Dedicated video port guarantees video frame rates (30 frames per second)
  - Maximum 40 MHz, 16bpp YUV422 (PCMCIA specs 16 MHz maximum)
- DVD and Video Support
  - Enhanced motion compensation acceleration
  - 4-tap horizontal and 2-tap vertical high quality DVD video scaler.
  - De-interlacing filter, Video on graphics overlay, Multi-stream video
  - Color-space conversion, Scatter-gather bus-master, Planar YUV mode
  - ATI Multimedia Channel (AMC) video input port
  - Zoom Video input port (ZV-port)
  - NTSC and PAL TV- out
  - Improves software DVD/MPEG-2 frame rate by 20 to 30%.
  - Provides full motion MPEG-2 playback on Pentium II processors
- An integrated TV encoder with on-chip triple –DAC allows simultaneous CRT/LCD/TV output with these outstanding TV-out characteristics:
  - Support for Microvision 7.01 copy protection standard (required by DVD players)
  - YUV Direct/Passthrough mode for video/MPEG playback
  - DVD provides the best quality for movie playback
  - Secondary Display support for RGB modes as well as full screen YUV mode.
  - 1024 x 768 24bpp support
  - Line 21 Closed Caption and Extended Data Service support for encoding in Vertical Blanking Interval (VBI) of TV signal.
  - CGMS-A DVD copy management support in VBI through Line-20 and/or Extended Data Service (Line-21 Field 2).
  - UV filtering for a higher quality picture and reduced flicker.
  - TV-out power management support.
  - Proven Y flicker filter with programmable (2,3,4,5,6)taps.
  - Eliminates " Composite Dot Crawl" problem for both NTSC and PAL.
- Varied TV-OUT output formats:
  - NTSC.
  - PAL B, D, G, H, I (PAL B, D, G, H, I are the same for TV-OUT),M(Brazil), N (Uruguay, Paraguay), CN (Argentina).
  - Composite Video (available on the majority of TV's).
  - S-Video(available on Mid to High End TV's, less colour artifacts, better resolution).
  - SCART-RGB connector (direct RGB into the TV-high quality resolution).
  - Output signal is generated at 50+Msamples/sec to virtually eliminate the need for external analogue filtering.
  - Signal is digitally filtered to insure that it does not exceed bandwidth specifications of TV standards, this insures that it can be recorded, can be broadcast, and will comply with FCC regulations when input into poorly shielded TV sets.
  - Can detect whether TV/VCR is connected or not (Power-down/Power-up over-ride via software).
- Supports 3D Acceleration
  - integrated 1 million triangle/s set-up engine

- 4K on-chip texture cache.
- Full screen or window double buffering for smooth animation
- Hidden surface removal using 16-bit Z-buffering
- Edge anti-aliasing
- Sub-pixel and sub-texel accuracy
- Gouraud and specular shaded polygons
- Perspectively correct mip-mapped texturing with chroma-key support.
- Full support of Direct3D texture lighting.

- Extensive 3D mode support:
  - Draw in RGBA32,RGBA16, and RGB16.
  - Texture map modes: RGBA32,RGBA16,RGB8,ARGB4444, YUV444.
  - Compressed texture mode: YUV422, CLUT4 (CI4), CLUT8(CI8), VQ
- Mobile AGP 1.0 and mobile PCI 1.0 support.
- Pin, Register and Timer modes for hardware and software power management.
- Dynamic clock switching.
- Panel bias voltage and digital power control.
- Self-refresh(EDO,SGRAM), and CBR refresh (EDO) in Suspend mode using external 32 KHz source (F32KHz pin).
- Enhanced line buffer allows vertical filtering of native MPEG-2 size (720 x 480) images.
- DVD/MPEG-2 decode assist provides dramatically improved frame rate
- Hardware mirroring for flipping video images in video images in video conferencing systems.
- Smooth video scaling and enhanced YUV to RGB color space conversion
- Front and back end scalers support multi-stream video for video conferencing
- Filtered horizontal/vertical, up/down, scaling enhances playback quality.

0.7 Super IO: NS PC 97338VJG

The PC97338 is a fully ACPI 1.0 and PC97 compliant, ISA based Super I/O. It is functionally compatible with the PC87338. It includes a Floppy Disk Controller (FDC), two Serial Communication Controllers (SCC) for UART and Infrared support, one IEEE1284 compatible Parallel Port, and two general purpose Chip signals for game port support. The device ports power management as well as 3.3V and 5Voperation making it particularly suitable for notebook and sub-notebook applications. The PC87338 and PC97338 are fully compliant to the Plug and Play specifications included in the ware Design Guide for Microsoft Windows 95".

- Meets ACPI 1.0 and PC97 requirements
- Backward compatible with PC87338
- 100% compatibility with Plug and Play requirements specified in the Hardware Design Guide for Microsoft Windows 95″ ISA, EISA, and Micro-mixed Channel architectures
- A special Plug and Play module includes:
  - Flexible IRQs, DMAs and base addresses
  - General Interrupt Requests (IRQs) that can be multi plexed to the ten supported IRQs
- A new, high performance, on-chip Floppy Disk Controller (FDC) provides:
  - Software compatibility with the PC8477, which contains a superset of the floppy disk controller functions in the µDP8473, the NEC µPD765A and the N82077
  - A modifiable 13-bit address
  - Ten IRQ channel options
  - Four 8-bit DMA channel options
  - 16-byte FIFO
  - Burst and non-burst modes
  - Low-power CMOS with enhanced power-down mode

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- A new, high-performance, on-chip, digital data separator without external filter components
- Support for 5.25"/3.5" floppy disk drives
- Automatic media sense support
- Perpendicular recording drive support
- Three mode Floppy Disk Drive (FDD) support
- Full support for IBM? Tape Drive Register (TDR) implementation
- Support for new fast tape drives (2 Mbps) and standard tape drives (1 Mbps, 500 Kbps and 250 Kbps)
- Support for both FM and MFM modes .

- Two Serial Communication Controllers provide:
  - Software compatibility with the 16550A and the 16450
  - A modifiable 13-bit address
  - Ten IRQ channel options
  - MIDI baud rate support
  - Four 8-bit DMA channel options on SCC2
  - Shadow register support UART write-only bits

- A fast universal Infrared interface on SCC2 sup-ports the following:
  - Data rates of up to 115.2 Kbps (SIR)
  - A data rate of 1.152 Mbps (MIR)
  - A data rate of 4.0 Mbps (FIR)
  - Selectable internal or external modulation/de-modulation (Sharp-IR)
  - Consumer Electronic IR mode

- A bidirectional parallel port that includes:
  - A modifiable 13-bit address
  - Ten IRQ channel options
  - Four 8-bit DMA channel options
  - An Enhanced Parallel Port (EPP) compatible with version EPP 1.9 IEEE1284 compliant), that also supports version EPP 1.7 of the Xir-com specification.
  - An Extended Capabilities Port (ECP) that is
  - IEEE1284 compliant, including level 2
  - Bidirectional data transfer under either soft-ware or hardware control
  - Compatibility with ISA, EISA, and MicroChannel parallel ports
  - Multiplexing of additional external FDC signals on parallel port pins that enables use of an external Floppy Disk Drive (FDD)
  - A protection circuit that prevents damage to the parallel port when an external printer powers up or operates at high voltages
  - 14 mA output drivers

- Two general purpose pins for two programmable chip select signals can be programmed for game port control.
- An address decoder that:
  - Selects all primary and secondary ISA ad-dresses, including OM1-4 and LPT1-3
    Decodes up to 16 address bits
- Clock source:
  - An internal clock multiplier generates all required internal frequencies.
  - A clock input source 14.318 MHz, 24 MHz, or 48 MHz may be selected
- Enhanced power management features:
  - Special power-down configuration registers
  - Enhanced programmable FDC command to trigger power down
  - Programmable power-down and wake-up modes
  - Two dedicated pins for FDC power management

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- Low power-down current consumption (typically for PC97338, 400 µA for 3.3V and 600 µA for 5V application)
- Reduced pin leakage current
- Low power CMOS technology
- The ability to shut off clocks to either the entire chip or only to specific modules

- Mixed voltage support provides:
  - Standard 5 V operation
  - Low voltage 3.3 V operation
  - Simultaneous internal 3.3 V operation and reception or transmission to devices that have either 3.3 V or 5 V power supply

- 100-pin TQFP VJG package - PC87338/PC97338
- Standby mode: control by software

Default configuration:

	IO address	IRQx	DRQx
COM1	3F8-3FF	4	-
FIR/MIR/SIR/ SHARP ASK (COM2)	278-27F	3	-
PIO	378-37F	7	-
FDD	3F0-3FF	6	2

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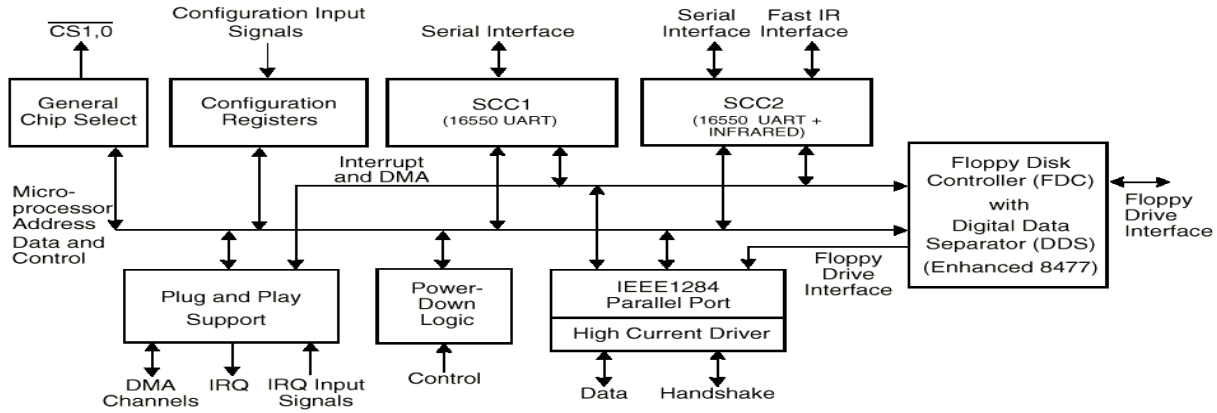
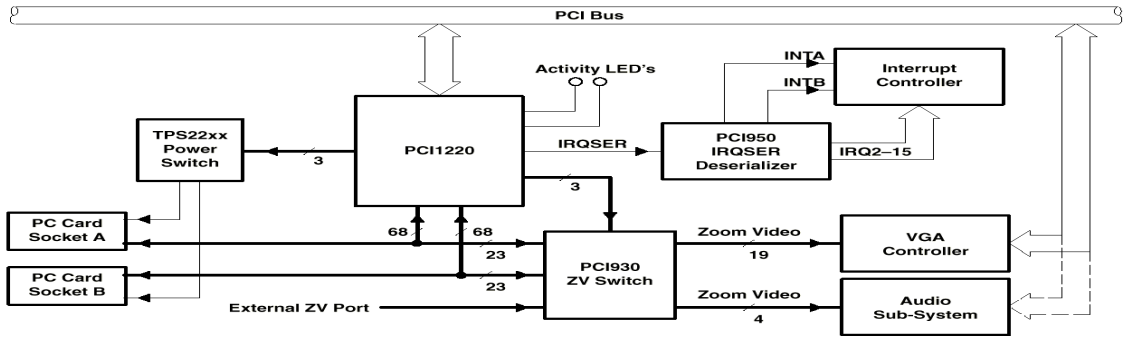
Block Diagram



0.8 PC CARD interface controller: TI1225

- PCI Bus Power Management Interface Specification 1.0 Compliant
- ACPI 1.0 Compliant
- Fully Compatible With the Intel 430TX (Mobile Triton II) Chipset Packaged in 208-Pin TQFP
- PCI Local Bus Specification Revision 2.1 Compliant
- 1995 PC Card Standard Compliant
- 3.3-V Core Logic With Universal PCI Interfaces Compatible With 3.3-V and 5-V PCI Signaling Environments
- Mix-and-Match 5-V/3.3-V PC Card16 Cards and 3.3-V CardBus Cards
- Supports Two PC Card or CardBus Slots With Hot Insertion and Removal
- Uses Serial Interface to TIE TPS2202/2206 Dual-Slot PC Card Power Switch
- Supports Burst Transfers to Maximize Data Throughput
- Supports Parallel PCI Interrupts, Parallel ISA IRQ and Parallel PCI Interrupts, Serial ISA IRQ With Parallel PCI Interrupts, and Serial ISA IRQ and PCI Interrupts
- Serial EEPROM Interface for Loading Subsystem ID and Subsystem Vendor ID
- Pipelined Architecture Allows Greater Than 130M-Bytes-Per-Second Throughput From CardBus to PCI and From PCI to CardBus
- Supports Up to Five General-Purpose I/Os
- Programmable Output Select for CLKRUN
- Multifunction PCI Device With Separate Configuration Space for Each Socket
- Five PCI Memory Windows and Two I/O Windows Available for Each PC Card16 Socket
- Two I/O Windows and Two Memory Windows Available to Each CardBus Socket
- Exchangeable Card Architecture (ExCA) Compatible Registers Are Mapped in Memory and I/O Space
- Intel 82365SL-DF Register Compatible
- Supports Distributed DMA (DDMA) and PC/PCI DMA
- Supports 16-Bit DMA on Both PC Card Sockets
- Supports Ring Indicate, SUSPEND, PCI CLKRUN, and CardBus CCLKRUN
- LED Activity Pins
- Supports PCI Bus Lock (LOCK)
- Advanced Submicron, Low-Power CMOS Technology
- For the Complete Data Sheet for PCI1220, Please See Literature #SCPS016



NOTE: The PC Card interface is 68 pins for CardBus and 16-bit PC Cards. In zoomed-video mode 23 pins are used for routing the zoomed video signals too the VGA controller.

0.9 Keyboard System: H8(3434) Universal Keyboard Controller

CPU

- Two-way general register configuration .
- Eight 16-bit registers or Sixteen 8-bit registers.
- High-speed operation.
- Maximum clock rate : 16Mhz at 5V.

Memory

- Include 32KB ROM and 1KB RAM.

16-bit free-running timer

- One 16-bit free-running counter.
- Two output-compare lines.
- Four input capture lines.

8-bit timer (2 channels)

- each channel has one 8-bit up-counter , two time constant registers

PWM timer (2 channels)

- Resolution : 1/250.
- Duty cycle can be set from 0 to 100%.

I²C bus interface (one channel)

- Include single master mode and slave mode.

Host interface (HIF)

- 8-bit host interface port .
- Three host interrupt requests (HIRQ1,11,12).

- Regular and fast A20 gate output.

Keyboard controller

- Controls a matrix-scan keyboard by providing a keyboard scan function with wake-up interrupts and sense ports.

A/D converter

- 10-bit resolution.
- 8 channels : single or scan mode (selectable).

D/A converter

- 8-bit resolution.
- 2 channels.

Interrupts

- nine external interrupt lines : NMI# , IRQ0 to 7#.
- 26 on-chip interrupt sources.

Power-down modes

- Sleep mode.
- Software standby mode.
- Hardware standby mode.

- A single chip microcomputer.
- On-chip flash memory.
- Maximum 64-kbyte address space.
- Support three PS/2 port for external keyboard ,mouse and internal track pad.
- Support SMI, SCI trigger input.
- Cover switch.
- Battery charging control.
- Smart Battery monitoring .
- Control D/D system on/off.
- Fan control and LED indicator serial interface
- 100pin TQFP

0.9 System BIOS

See software BIOS specification

0.10 Memory System

Main Memory

- NEC uPD4564163/Mitsubishi M2V64S40BTP-7 32 MB SDRAM on board
  - One chip memory size: 4Mx16bit .
  - Standard 54 pin TSOP package.
  - Power supply: 3 ± 0.3V
  - Operating power dissipation: MAX 468mW
- One 144pin S.O. DIMM sockets on Mother Board for expansion
  - Supports JEDEC specification: 144 S.O. DIMM socket.
  - 2 banks on socket.
- Memory bus bandwidth: 64 bits

- Supports 32MB SDRAM on board (can support up to 64MB) and one 144pin SDRAM SO-DIMM memory module upgrading up to 128 MB. Here are some main memory system essential characteristics:

—	4Mx16bit on board	32M
—	144-pin S.O. DIMM socket	1
—	Memory Voltage	3.3V± 0.3V
—	Banks on DIMM	2

0.11 Interface

- Power Supply Jack.
- One Standard Parallel Port With ECP/EPP Functions
- Two Serial Ports, One For COM1/COM2, The Other For FIR/MIR/SIR/SHARP ASK
- One External CRT Connector For CRT Display
- One PS/2 Interface For External KB, Mouse Or Other Devices
- Two Cardbus Sockets
- Connector For Connection Between M/B And Panel.
- Y Connector For Connection Between M/B And LED BD, backlight BD.
- Headphone Out Jack And Microphone Input Jack.
- One MODEM RJ-11 phone jack for PSTN line.

0.12 Audio System :audio controller MAESTRO-2

- 64-voice wavetable synthesizer supporting DLS and 32 independent digital data streams
- Proprietary WaveCache Technology
- 3-D positional audio under DirectX?5.0
- Enhanced effects (reverb, chorus, echo, vibrato, etc.)
- AC-3 decode acceleration
  - — External DSP for hardware AC-3 decode
  - — Active Movie AC-3 filter acceleration option
- 2- or 3-button hardware master volume control
- I ² S/Zoom Video support
- AC97 CODEC interface
- Up to 20-bit ADC/DAC audio resolution
- Complies with Microsoft ACPI rev 1.0 (D0~D3) & Advanced Power Management spec 1.2
- 3.3 V power supply, 5 V - I/O tolerant
- Supports up to 12 GPIO pins
- Secondary AC?7 CODEC interface
- PCI 2.1 bus master with scatter/gather support
- Distributed & PC/PCI DMA, Compaq/Intel serial IRQ support and Transparent DMA

0.13 Audio System: AC' 97 CODEC CS4297

- An AC' 97 CODEC provides a complete high quality audio solution, Feature Include:
  - MIDI port.
  - MODEM
  - CD-ROM
  - User-Defined GPIO
  - Volume Control: Rotary VR
- Stereo BTL 2x1 W Amplifiers (TPA0202) With 8 Ohm Load.
- CD-ROM IDE Interface
- 16 Bit Stereo ADC & DAC For Record And Play Back
- Programmable Sample Rates From 4kHz To 44.1kHz For Record And Playback
- Microphone in * 1 (3.5 mm phone-jack)
- Headphone out * 1: stereo (3.5mm phone-jack)
- Built-in Speaker * 2 (1w, 8 ohm)
- Built-in Microphone * 1
- Note: For Those Input Source Not Using Should Be Set Mute In Order To Reduce Noise. Like Line In

0.14 FAX/MODEM unit

- Made by ASKEY Computer corporation
- Main chip : Pctel PCT789
- Integrated PCI interface
- Host-based ITU V.70 DSVD.
- Video-ready modem interface (VRM) v.80
- Operation support:
  - windows 95 windows NT
- K56flex for internet connection rates approaching 56kbits/s.
- Data Modes capabilities
  - Ultrahigh compress throughput due to parallel access directly to the host PCITU-T V.34 extended rates: 33600 bits/s- 2400 bits/s
  - V.32tero. V.32bis, and fallbacks
  - TIA-EIA 602 standard for AT command set
  - V.42 error correction (LAPM and MNP)
- FAX mode capabilities:
  - ITU-T V.17, V.29, V.27ter, and V.21 CH 2
  - TIA/EIA 578 Class 1 FAX
- SIMULTALK full-duplex speakerphone (FDSP):
  - Adaptive acoustic echo canceler for dynamic speaker/microphone positioning
  - IS-101 AT+ V commands with extensions
- Hardware integrated:
  - Integrated DSP and interface device
  - PCI interface
  - PCI but mastering for EDSP/DSVD/VRM
  - Call progress speaker driver
- High-precision sigma-delta codec STLC7546:
  - Integrated hybrid
- Extensive bit I/Os for homologation and cellular direct connect
- Enhanced voice features;
  - Telephone answering machine (TAM)
  - Business audio (BA)
  - VoiceView
  - Caller identification (caller ID)

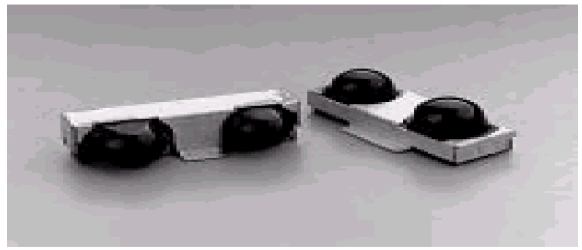
- Internal PLL for low-speed crystal support
- Autoconfiguration
- Enhanced low-power modem
- Support for 5 V or 3.3 V power

0.15 FIR Port

There is a IR port in 7233 system. The IR Port is compliant with IrDA 1.0, IrDA 1.1 and SHARP ASK specification and can support up to 4.0 Mb/s transfer rate.

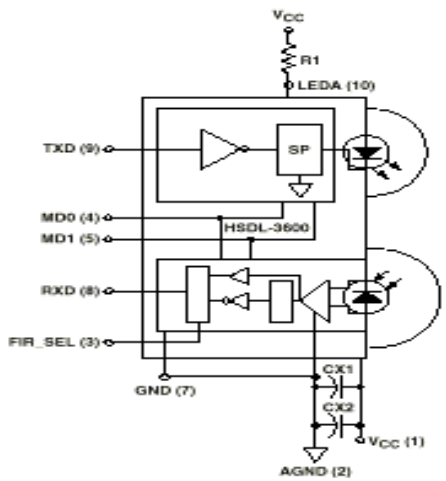
- Fully Compliant to IrDA 1.1 Specifications
  - 9.6 kb/s to 4 Mb/s operation
  - Excellent nose-to-nose operation
- Typical Link Distance > 1.5 m
- Compatible with ASK, HP-SIR, and TV Remote
- IEC825-Class 1 Eye Safe
- Wide Operating Voltage Range
  - 2.7 V to 5.25 V
- Small Module Size
  - 4.0 x 12.2 x 5.1 mm (HxWxD)
- Complete Shutdown
  - TXD, RXD, PIN diode
- Low Shutdown Current
  - 10 nA typical
- Adjustable Optical Power Management
  - Adjustable LED drive-current to maintain link integrity
- Single Rx Data Output
  - FIR Select pin switch to FIR
- Integrated EMI Shield
  - Excellent noise immunity
- Edge Detection Input
  - Prevents the LED from long turn-on time
- Interface to Various Super I/O and Controller Devices
- Designed to Accommodate Light Loss with Cosmetic Window
- Only 2 External Components are Required
- Digital Imaging
  - Digital Still Cameras
  - Photo-Imaging Printers
- Data Communication
  - Notebook Computers
  - Desktop PCs
  - Win CE Handheld Products
  - Personal Digital Assistants (PDAs)
  - Printers
  - Fax Machines, Photocopiers
  - Screen Projectors
  - Auto PCs
  - Dongles
  - Set-Top Box
- Telecommunication Products
  - Cellular Phones
  - Pagers
- Small Industrial & Medical Instrumentation

— General Data Collection Devices



— Patient & Pharmaceutical Data Collection Devices

- IR LANs



0.16 Mass Storage Sub-system

There is one 2.5" , 8.45/9.5mm hard disk drive installed in 7233 system, which can support 3/4/6/9/12 GB, Ultra-DMA33 function.

CD-ROM (24X speed) / DVD-ROM (6X speed)

7233 System has one standard CD-ROM (24 times speed or higher)/DVD-ROM (6 times speed or higher). The hardware interface is compliant with ATAPI IDE specification. The default drive is D. User should install the CD-ROM/DVD-ROM device driver in order to operate this device.

0.17 Special Feature Function

Key Function

Keys Combination	Feature	Meaning
Fn + F5	LCD/external CRT switching	Rotate display mode in LCD only, CRT only and simultaneously display.
Fn + F6	Brightness down	Decreases the LCD brightness / No function in DSTN model
Fn + F7	Brightness up	Increases the LCD brightness / No function in DSTN model
Fn + F8	Contrast down	Decreases the LCD contrast
Fn + F9	Contrast up	Increase the LCD contrast
Fn + F10	Enable/Disable Battery Warning Beep	Toggle Battery Warning on/off
Fn + F11	Panel Off/On	Toggle Panel Off/On
Fn + F12	Suspend to DRAM / HDD	Force the computer into either Suspend to HDD or Suspend to DRAM mode depending on BIOS Setup.

Flash ROM (BIOS)

7233 system utilizes the state-of-the-art Flash EEPROM technology. User can upgrade the system BIOS in the future just running the program from MiTAC.

LED Indicators

System has nine status LED indicators to display system activity which include below LCD panel unit and above keyboard:

1. Three LED indicators below LCD panel unit:

From left to right that indicate AC POWER, BATTERY POWER and BATTERY STATUS

- **AC POWER: This LED lights green when the notebook is being powered by AC, and flash (on 1 second, off 1 second) when Suspend to DRAM is active using AC power. The LED is off when the notebook is off or powered by batteries, or when Suspend to Disk.**

- **BATTERY POWER: This LED lights green when the notebook is being powered by batteries, and flashes (on 1 second, off 1 second) when Suspend to DRAM is active using battery power. The LED is off when the notebook is off or powered by AC, or when Suspend to Disk.**

- **BATTERY STATUS : During normal operation, this LED stays off as long as the battery is charged. When the battery charge drops to 10% of capacity, the LED lights red, flashes per 1 second and beeps per 2 second. When AC is connected, this indicator glows green if the battery pack is fully charged, or orange (amber) if the battery is being charged.**

Six LED indicators above keyboard:

From left to right that indicates CD-ROM/DVD-ROM, HARD DISK DRIVE, FLOPPY DISK DRIVE, NUM LOCK, CAPS LOCK and SCROLL LOCK.

COM port assignment

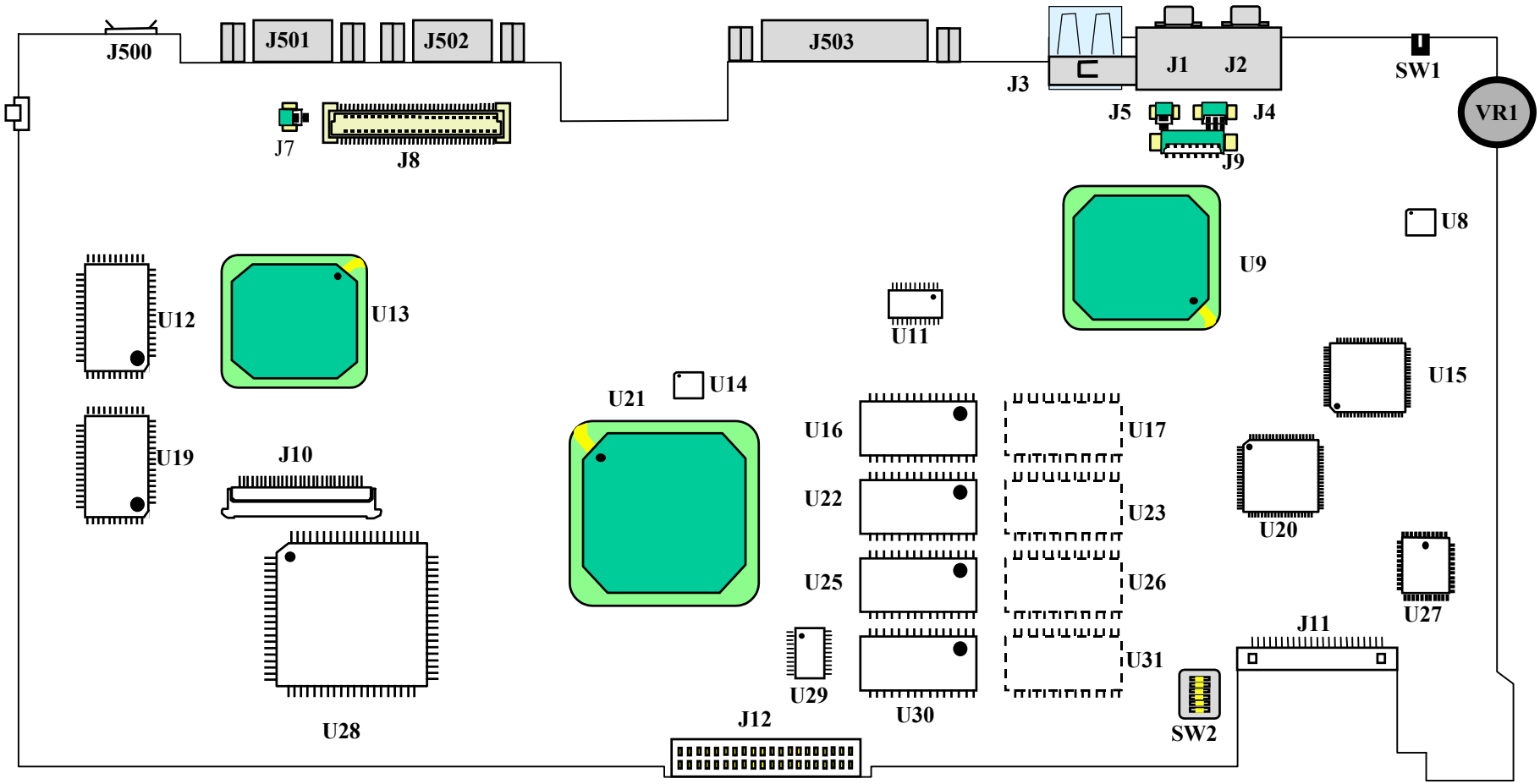
COM1: MODEM / RS-232 / Disable
COM2: IR / RS-232 / Disable

7233 N/B MAINTENANCE

1. Definition & Location of Connectors/ Switches/Components (A)

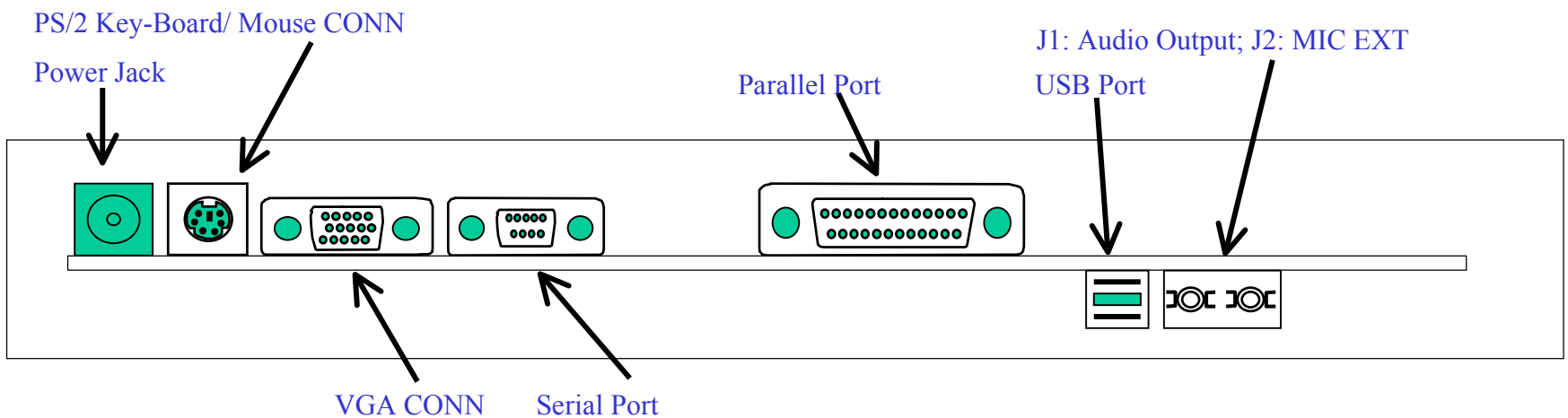
- J1: Audio Output.
- J2: MIC EXT.
- J3: USB Port.
- J4: Internal MIC CONN
- J5/J7: L/R SPK CONN.
- J8: LCD Panel TRANS. BD Connector.
- J9: Inverter BD CONN.
- J10: Keyboard CONN.
- J11: FDD CONN.
- J12: Touch-pad/ HDD CONN.
- SW1: Suspend Switch.
- SW2: LCD ID/ Key Matrix Select.
- VR1: Volume Control VR.
- U8: CS4297 AC′ 97 Compliant Audio Codec.
- U9: PIIX4E(82371MB) South Bridge.
- U11: ICS W137 Frequency Synthesizer.
- U12,U19: SGRAM.
- U13: ATI_RAGE_LT PRO AGP VGA CTRL.
- U14: 72466 Geyserville Speed Step.
- U15: ESS MAESTRO-2E Audio Controller Chip.
- U16,U22,U25,U30: 32MB On-Board Memory.
- U20: NS PC93338VJG Supper I/O Controller.
- U21: FW82443BX Host Bridge Controller.
- U27: 32P/PLCC/SMT SYS BIOS.
- U28: TI 1225 PCI-PCMCIA/CARBUS Controller
- U29: W40S11-02 SDAM Clock Buffer.

2. Definition & Location of Connectors/Switches/Switches(A)

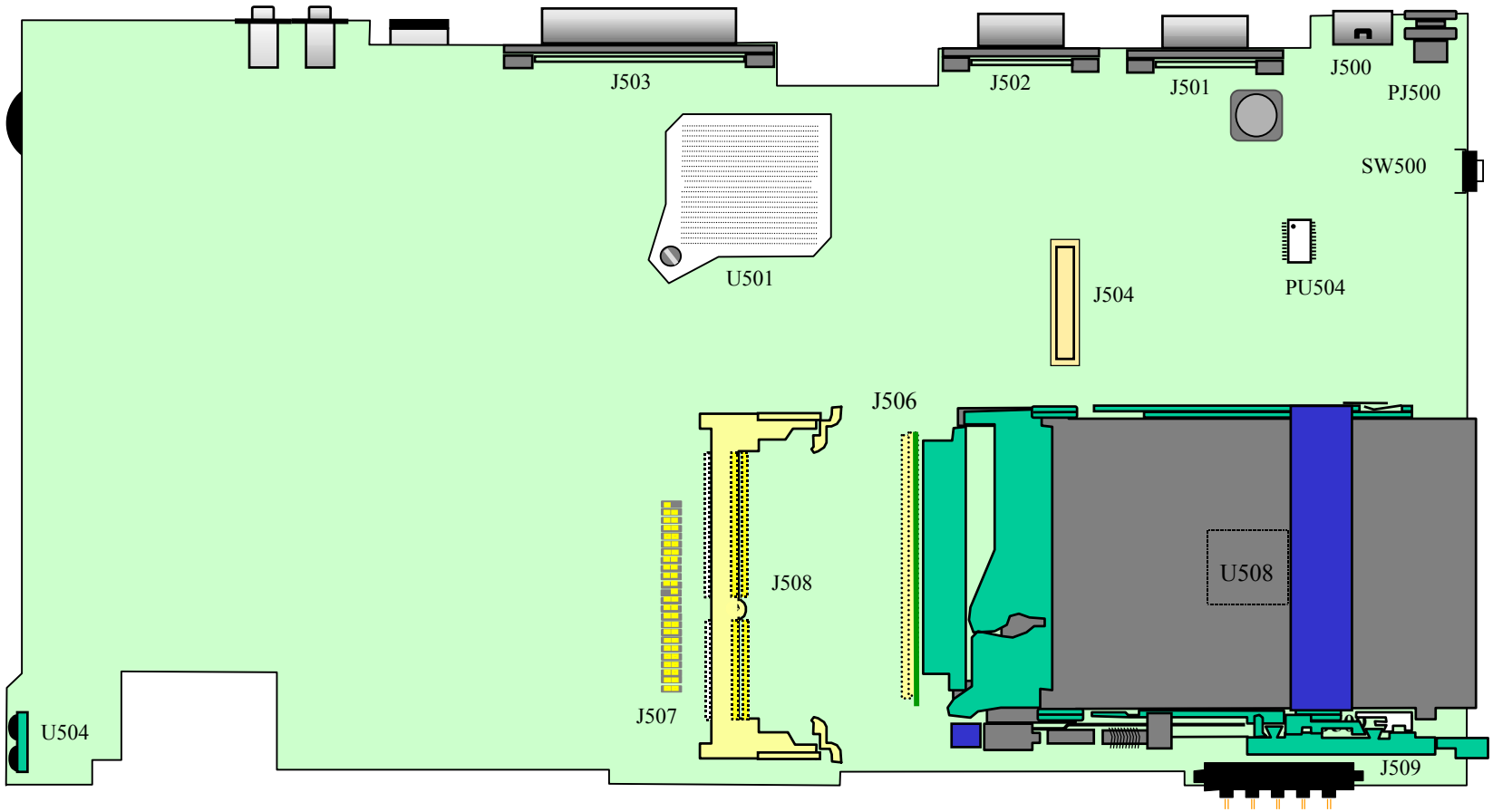


2. Definition & Location Major Components/connectors (Side B)

- PJ500: Power Jack.
- J500: PS/2 Key-Board/ Mouse CONN.
- J501: VGA CONN.
- J502: Serial Port.
- J503: Parallel Port.
- J504: FAX Modem CONN
- J506: PCMCIA CONN
- J507: CO-ROM CONN
- J508: 144 PINS SODIMM Socket.
- J509: Battery Connector.
- SW500: Power Switch.
- U501: uPGAII CPU.
- U504:IR LANs
- U508: H8/F3434 Key-Board Controller.



2. Definition & Location Major Components (Side B)



3. Pin Descriptions of Major Comporents

3.1 Intel µPGAII CPU Processor-1

Alphabetical Signal Reference

Signal Name	I/O	Signal Description
A[35:3]#	I/O GTL+	The A[35:3]# (Address) signals define a 2^{36}-byte physical memory address space. When ADS# is active, these signals transmit the address of a transaction; when ADS# is inactive, these signals transmit transaction information. These signals must be connected to the appropriate pins/balls of both agents on the system bus. The A[35:24]# signals are protected with the AP1# parity signal, and the A[23:3]# signals are protected with the AP0# parity signal. On the active-to-inactive transition of RESET#, each processor bus agent samples A[35:3]# signals to determine its power-on configuration. See Section 4 of this document and the *PentiumII Processor Developer's Manual* for details.
A20M#	I 1.5V Tolerant	If the A20M# (Address-20 Mask) input signal is asserted, the processor masks physical address bit 20 (A20#) before looking up a line in any internal cache and before driving a read/write transaction on the bus. Asserting A20M# emulates the 8086 processor's address wrap-around at the 1-Mbyte boundary. Assertion of A20M# is only supported in Real mode.
ADS#	I/O GTL+	The ADS# (Address Strobe) signal is asserted to indicate the validity of a transaction address on the A[35:3]# signals. Both bus agents observe the ADS# activation to begin parity checking, protocol checking, address decode, internal snoop or deferred reply ID match operations associated with the new transaction. This signal must be connected to the appropriate pins/balls on both agents on the system bus.
AERR#	I/O GTL+	The AERR# (Address Parity Error) signal is observed and driven by both system bus agents, and if used, must be connected to the appropriate pins/balls of both agents on the system bus. AERR# observation is optionally enabled during power-on configuration; if enabled, a valid assertion of AERR# aborts the current transaction. If AERR# observation is disabled during power-on configuration, a central agent may handle an assertion of AERR# as appropriate to the error handling architecture of the system.
AP[1:0]#	I/O GTL+	The AP[1:0]# (Address Parity) signals are driven by the request initiator along with ADS#, A[35:3]#, REQ[4:0]# and RP#. AP1# covers A[35:24]#. AP0# covers A[23:3]#. A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. This allows parity to be high when all the covered signals are high. AP[1:0]# should be connected to the appropriate pins/balls on both agents on the system bus.
BCLK	I 2.5V Tolerant	The BCLK (Bus Clock) signal determines the system bus frequency. Both system bus agents must receive this signal to drive their outputs and latch their inputs on the BCLK rising edge. All external timing parameters are specified with respect to the BCLK signal.

Signal Name	I/O	Signal Description
BERR#	I/O GTL+	The BERR# (Bus Error) signal is asserted to indicate an unrecoverable error without a bus protocol violation. It may be driven by either system bus agent and must be connected to the appropriate pins/balls of both agents, if used. However, the mobile Pentium III processors do not observe assertions of the BERR# signal. BERR# assertion conditions are defined by the system configuration. Configuration options enable the BERR# driver as follows: • Enabled or disabled • Asserted optionally for internal errors along with IERR# • Asserted optionally by the request initiator of a bus transaction after it observes an error • Asserted by any bus agent when it observes an error in a bus transaction
BINIT#	I/O-GTL+	The BINIT# (Bus Initialization) signal may be observed and driven by both system bus agents and must be connected to the appropriate pins/balls of both agents, if used. If the BINIT# driver is enabled during the power-on configuration, BINIT# is asserted to signal any bus condition that prevents reliable future information. If BINIT# is enabled during power-on configuration, and BINIT# is sampled asserted, all bus state machines are reset and any data which was in transit is lost. All agents reset their rotating ID for bus arbitration to the state after reset, and internal count information is lost. The L1 and L2 caches are not affected. If BINIT# is disabled during power-on configuration, a central agent may handle an assertion of BINIT# as appropriate to the Machine Check Architecture (MCA) of the system.
BNR#	I/O-GTL+	The BNR# (Block Next Request) signal is used to assert a bus stall by any bus agent that is unable to accept new bus transactions. During a bus stall, the current bus owner cannot issue any new transactions. Since multiple agents may need to request a bus stall simultaneously, BNR# is a wired-OR signal that must be connected to the appropriate pins/balls of both agents on the system bus. In order to avoid wire-OR glitches associated with simultaneous edge transitions driven by multiple drivers, BNR# is activated on specific clock edges and sampled on specific clock edges.
BP[3:2]#	I/O GTL+	The BP[3:2]# (Breakpoint) signals are the System Support group Breakpoint signals. They are outputs from the processor that indicate the status of breakpoints.
BPM[1:0]#	I/O GTL+	The BPM[1:0]# (Breakpoint Monitor) signals are breakpoint and performance monitor signals. They are outputs from the processor that indicate the status of breakpoints and programmable counters used for monitoring processor performance.

3.1 Intel µPGAII CPU Processor-2

Alphabetical Signal Reference

Signal Name	I/O	Signal Description
BPRI#	I GTL+	The BPRI# (Bus Priority Request) signal is used to arbitrate for ownership of the system bus. It must be connected to the appropriate pins/balls on both agents on the system bus. Observing BPRI# active (as asserted by the priority agent) causes the processor to stop issuing new requests, unless such requests are part of an ongoing locked operation. The priority agent keeps BPRI# asserted until all of its requests are completed and then releases the bus by deasserting BPRI#.
BREQ0#	I/O GTL+	The BREQ0# (Bus Request) signal is a processor Arbitration Bus signal. The processor indicates that it wants ownership of the system bus by asserting the BREQ0# signal. During power-up configuration, the central agent must assert the BREQ0# bus signal. The processor samples BREQ0# on the active-to-inactive transition of RESET#.
BSEL[1:0]	I 1.5V Tolerant	The BSEL[1:0] (Select Processor System Bus Speed) signal is used to configure the processor for the system bus frequency. Table 38 shows the encoding scheme for BSEL[1:0]. The only supported system bus frequency for the mobile Pentium III processor is 100 MHz. If another frequency is used or if the BSEL[1:0] signals are not driven with "1" then the processor is not guaranteed to function properly. **BSEL[1:0] Encoding** **BSEL[1:0] — System Bus Frequency** 00 — 66 MHz 01 — 100 MHz 10 — Reserved 11 — 133 MHz
CLKREF	Analog	The CLKREF (System Bus Clock Reference) signal provides a reference voltage to define the trip point for the BCLK signal. This signal should be connected to a resistor divider to generate 1.25V from the 2.5-V supply.
CMOSREF	Analog	The CMOSREF (CMOS Reference Voltage) signal provides a DC level reference voltage for the CMOS input buffers. A voltage divider should be used to divide a stable voltage plane (e.g., 2.5V or 3.3V). This signal must be provided with a DC voltage that meets the VCMOSREF specification from Table 13.
D[63:0]#	I/O GTL+	The D[63:0]# (Data) signals are the data signals. These signals provide a 64-bit data path between both system bus agents, and must be connected to the appropriate pins/balls on both agents. The data driver asserts DRDY# to indicate a valid data transfer.

Signal Name	I/O	Signal Description
DBSY#	I/O- GTL+	The DBSY# (Data Bus Busy) signal is asserted by the agent responsible for driving data on the system bus to indicate that the data bus is in use. The data bus is released after DBSY# is deasserted. This signal must be connected to the appropriate pins/balls on both agents on the system bus.
DEFER#	I GTL+	The DEFER# (Defer) signal is asserted by an agent to indicate that the transaction cannot be guaranteed in-order completion. Assertion of DEFER# is normally the responsibility of the addressed memory agent or I/O agent. This signal must be connected to the appropriate pins/balls on both agents on the system bus.
DEP[7:0]#	I/O GTL+	The DEP[7:0]# (Data Bus ECC Protection) signals provide optional ECC protection for the data bus. They are driven by the agent responsible for driving D[63:0]#, and must be connected to the appropriate pins/balls on both agents on the system bus if they are used. During power-on configuration, DEP[7:0]# signals can be enabled for ECC checking or disabled for no checking.
DRDY#	I/O GTL+	The DRDY# (Data Ready) signal is asserted by the data driver on each data transfer, indicating valid data on the data bus. In a multi-cycle data transfer, DRDY# can be deasserted to insert idle clocks. This signal must be connected to the appropriate pins/balls on both agents on the system bus.
EDGCTRLP	Analog	The EDGCTRLP (Edge Rate Control) signal is used to configure the edge rate of the GTL+ output buffers. Connect the signal to VSS with a 110-£ ¸[1% resistor.
FERR#	O 1.5V Tolerant Open- drain)	The FERR# (Floating-point Error) signal is asserted when the processor detects an unmasked floating-point error. FERR# is similar to the ERROR# signal on the Intel 387 coprocessor, and it is included for compatibility with systems using DOS-type floating-point error reporting.
FLUSH#	I 1.5V Tolerant	When the FLUSH# (Flush) input signal is asserted, the processor writes back all internal cache lines in the Modified state and invalidates all internal cache lines. At the completion of a flush operation, the processor issues a Flush Acknowledge transaction. The processor stops caching any new data while the FLUSH# signal remains asserted. On the active-to-inactive transition of RESET#, each processor bus agent samples FLUSH# to determine its power-on configuration.

3.1 Intel µPGAII CPU Processor-3

Alphabetical Signal Reference

Signal Name	I/O	Signal Description
GHI#	I 1.5V Tolerant	The GHI# signal controls which operating mode bus ratio is selected in a mobile Pentium III processor featuring Intel SpeedStep technology. On the processor featuring Intel SpeedStep technology, this signal is latched when BCLK restarts in Deep Sleep state and determines which of two bus ratios is selected for operation. This signal is ignored when the processor is not in the Deep Sleep state. This signal is a "Don't Care" on processors that do not feature Intel SpeedStep technology. This signal has an on-die pull-up to VccT and should be driven with an Open-drain driver with no external pull-up.
HIT#, HITM#	I/O GTL+	The HIT# (Snoop Hit) and HITM# (Hit Modified) signals convey transaction snoop operation results, and must be connected to the appropriate pins/balls on both agents on the system bus. Either bus agent can assert both HIT# and HITM# together to indicate that it requires a snoop stall, which can be continued by reasserting HIT# and HITM# together.
IERR#	O 1.5V Tolerant Open-drain	The IERR# (Internal Error) signal is asserted by the processor as the result of an internal error.Assertion of IERR# is usually accompanied by a SHUTDOWN transaction on the system bus. This transaction may optionally be converted to an external error signal (e.g., NMI) by system logic. The processor will keep IERR# asserted until it is handled in software or with the assertion of RESET#, BINIT, or INIT#.
IGNNE#	I 1.5V Tolerant	The IGNNE# (Ignore Numeric Error) signal is asserted to force the processor to ignore a numeric error and continue to execute non-control floating-point instructions. If IGNNE# is deasserted, the processor freezes on a non-control floating-point instruction if a previous instruction caused an error. IGNNE# has no affect when the NE bit in control register 0 (CR0) is set.
INIT#	I 1.5V Tolerant	The INIT# (Initialization) signal is asserted to reset integer registers inside the processor without affecting the internal (L1 or L2) caches or the floating-point registers. The processor begins execution at the power-on reset vector configured during power-on configuration. The processor continues to handle snoop requests during INIT# assertion. INIT# is an asynchronous input. If INIT# is sampled active on RESET#'s active-to-inactive transition, then the processor executes its built-in self test (BIST).

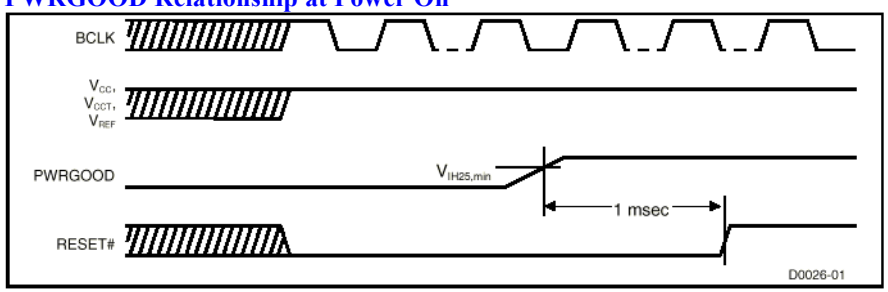
Signal Name	I/O	Signal Description
INTR	I 1.5V Tolerant	The INTR (Interrupt) signal indicates that an external interrupt has been generated. INTR becomes the LINT0 signal when the APIC is enabled. The interrupt is maskable using the IF bit in the EFLAGS register. If the IF bit is set, the processor vectors to the interrupt handler after completing the current instruction execution. Upon recognizing the interrupt request, the processor issues a single Interrupt Acknowledge (INTA) bus transaction. INTR must remain active until the INTA bus transaction to guarantee its recognition.
LINT[1:0]	I 1.5V Tolerant	The LINT[1:0] (Local APIC Interrupt) signals must be connected to the appropriate pins/balls of all APIC bus agents, including the processor and the system logic or I/O APIC component. When APIC is disabled, the LINT0 signal becomes INTR, a maskable interrupt request signal, and LINT1 becomes NMI, a non-maskable interrupt. INTR and NMI are backward compatible with the same signals for the Pentium processor. Both signals are asynchronous inputs. Both of these signals must be software configured by programming the APIC register space to be used either as NMI/INTR or LINT[1:0] in the BIOS. If the APIC is enabled at reset, then LINT[1:0] is the default configuration.
LOCK#	I/O GTL+	The LOCK# (Lock) signal indicates to the system that a sequence of transactions must occur atomically. This signal must be connected to the appropriate pins/balls on both agents on the system bus. For a locked sequence of transactions, LOCK# is asserted from the beginning of the first transaction through the end of the last transaction. When the priority agent asserts BPRI# to arbitrate for bus ownership, it waits until it observes LOCK# deasserted. This enables the processor to retain bus ownership throughout the bus locked operation and guarantee the atomicity of lock.
NMI	I 1.5V Tolerant	The NMI (Non-Maskable Interrupt) indicates that an external interrupt has been generated. NMI becomes the LINT1 signal when the APIC is disabled. Asserting NMI causes an interrupt with an internally supplied vector value of 2. An external interrupt-acknowledge transaction is not generated. If NMI is asserted during the execution of an NMI service routine, it remains pending and is recognized after the IRET is executed by the NMI service routine. At most, one assertion of NMI is held pending. NMI is rising edge sensitive.

3.1 Intel µPGAII CPU Processor-4

Alphabetical Signal Reference

Signal Name	I/O	Signal Description
PICCLK	I 2.5V Tolerant	The PICCLK (APIC Clock) signal is an input clock to the processor and system logic or I/O APIC that is required for operation of the processor, system logic, and I/O APIC components on the APIC bus.
PICD[1:0]	I/O 1.5V Tolerant Open-drain	The PICD[1:0] (APIC Data) signals are used for bi-directional serial message passing on the APIC bus. They must be connected to the appropriate pins/balls of all APIC bus agents, including the processor and the system logic or I/O APIC components. If the PICD0 signal is sampled low on the active-to-inactive transition of the RESET# signal, then the APIC is hardware disabled.
PLL1, PLL2	Analog	The PLL1 and PLL2 signals provide isolated analog decoupling is required for the internal PLL. See Section 3.2.2 for a description of the analog decoupling circuit.
PRDY#	O GTL+	The PRDY# (Probe Ready) signal is a processor output used by debug tools to determine processor debug readiness.
PREQ#	I 1.5V Tolerant	The PREQ# (Probe Request) signal is used by debug tools to request debug operation of the processor.
PWRGOOD	I 2.5V Tolerant	PWRGOOD (Power Good) is a 2.5-V tolerant input. The processor requires this signal to be a clean indication that clocks and the power supplies (Vcc, VccT, etc.) are stable and within their specifications. Clean implies that the signal will remain low, (capable of sinking leakage current) and without glitches, from the time that the power supplies are turned on, until they come within specification. The signal will then transition monotonically to a high (2.5V) state. Figure 26 illustrates the relationship of PWRGOOD to other system signals. PWRGOOD can be driven inactive at any time, but clocks and power must again be stable before the rising edge of PWRGOOD. It must also meet the minimum pulse width specified in Table 17 (Section 3.7) and be followed by a 1 ms RESET# pulse.

PWRGOOD Relationship at Power On



PWRGOOD Relationship at Power On

The PWRGOOD signal, which must be supplied to the processor, is used to protect internal circuits against voltage sequencing issues. The PWRGOOD signal should be driven high throughout boundary scan operation.

Signal Name	I/O	Signal Description
REQ[4:0]#	I/O GTL+	The REQ[4:0]# (Request Command) signals must be connected to the appropriate pins/balls on both agents on the system bus. They are asserted by the current bus owner when it drives A[35:3]# to define the currently active transaction type.
RESET#	I GTL+	Asserting the RESET# signal resets the processor to a known state and invalidates the L1 and L2 caches without writing back Modified (M state) lines. For a power-on type reset, RESET# must stay active for at least 1 msec after Vcc and BCLK have reached their proper DC and AC specifications and after PWRGOOD has been asserted. When observing active RESET#, all bus agents will deassert their outputs within two clocks. RESET# is the only GTL+ signal that does not have on-die GTL+ termination. A 56.2£ [% terminating resistor connected to VccT is required. A number of bus signals are sampled at the active-to-inactive transition of RESET# for the power-on configuration. The configuration options are described in Section 4 and in the *Pentium II Processor Developer's Manual*. Unless its outputs are tri-stated during power-on configuration, after an active-to-inactive transition of RESET#, the processor optionally executes its built-in self-test (BIST) and begins program execution at reset-vector 000FFFF0H or FFFFFFF0H. RESET# must be connected to the appropriate pins/balls on both agents on the system bus.
RP#	I/O GTL+	The RP# (Request Parity) signal is driven by the request initiator and provides parity protection on ADS# and REQ[4:0]#. RP# should be connected to the appropriate pins/balls on both agents on the system bus. A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. This definition allows parity to be high when all covered signals are high.
RS[2:0]#	I GTL+	The RS[2:0]# (Response Status) signals are driven by the response agent (the agent responsible for completion of the current transaction) and must be connected to the appropriate pins/balls on both agents on the system bus.

3.1 Intel µAGPII CPU Processor-5

PWRGOOD Relationship at Power On

Signal Name	I/O	Signal Description
RSP#	I GTL+	The RSP# (Response Parity) signal is driven by the response agent (the agent responsible for completion of the current transaction) during assertion of RS[2:0]#. RSP# provides parity protection for RS[2:0]#. RSP# should be connected to the appropriate pins/balls on both agents on the system bus. A correct parity signal is high if an even number of covered signals are low, and it is low if an odd number of covered signals are low. During Idle state of RS[2:0]# (RS[2:0]#=000), RSP# is also high since it is not driven by any agent guaranteeing correct parity.
RSVD	TBD	The RSVD (Reserved) signal is currently unimplemented but is reserved for future use. Leave this signal unconnected. Intel recommends that a routing channel for this signal be allocated.
RTTIMPEDP	Analog	The RTTIMPEDP (RTT Impedance/PMOS) signal is used to configure the on-die GTL+ termination. Connect the RTTIMPEDP signal to VSS with a 56.2-£ [1% resistor.
SLP#	I 1.5V Tolerant	The SLP# (Sleep) signal, when asserted in the Stop Grant state, causes the processor to enter the Sleep state. During the Sleep state, the processor stops providing internal clock signals to all units, leaving only the Phase-Locked Loop (PLL) still running. The processor will not recognize snoop and interrupts in the Sleep state. The processor will only recognize changes in the SLP#, STPCLK# and RESET# signals while in the Sleep state. If SLP# is deasserted, the processor exits Sleep state and returns to the Stop Grant state in which it restarts its internal clock to the bus and APIC processor units.
SMI#	I 1.5V Tolerant	The SMI# (System Management Interrupt) is asserted asynchronously by system logic. On accepting a System Management Interrupt, the processor saves the current state and enters System Management Mode (SMM). An SMI Acknowledge transaction is issued, and the processor begins program execution from the SMM handler.
STPCLK#	I 1.5V Tolerant	The STPCLK# (Stop Clock) signal, when asserted, causes the processor to enter a low-power Stop Grant state. The processor issues a Stop Grant Acknowledge special transaction and stops providing internal clock signals to all units except the bus and APIC units. The processor continues to snoop bus transactions and service interrupts while in the Stop Grant state. When STPCLK# is deasserted, the processor restarts its internal clock to all units and resumes execution. The assertion of STPCLK# has no affect on the bus clock.
TCK	I 1.5V Tolerant	The TCK (Test Clock) signal provides the clock input for the test bus (also known as the test access port).

Signal Name	I/O	Signal Description
TDI	I 1.5V Tolerant	The TDI (Test Data In) signal transfers serial test data to the processor. TDI provides the serial input needed for JTAG support.
TDO	O 1.5V Tolerant Open-drain	The TDO (Test Data Out) signal transfers serial test data from the processor. TDO provides the serial output needed for JTAG support.
TESTHI	I 1.5V Tolerant	The TESTHI (Test input High) is used during processor test and needs to be pulled high during normal operation.
TESTLO[2:1]	I 1.5V Tolerant	The TESTLO[2:1] (Test input Low) signals are used during processor test and needs to be pulled to ground during normal operation.
TESTP	Analog	The TESTP (Test Point) signals are connected to Vcc and Vss at opposite ends of the die. These signals can be used to monitor the Vcc level on the die. Route the TESTP signals to test points or leave them unconnected. Do not short the TESTP signals together.
THERMDA, THERMDC	Analog	The THERMDA (Thermal Diode Anode) and THERMDC (Thermal Diode Cathode) signals connect to the anode and cathode of the on-die thermal diode.
TMS	I 1.5V Tolerant	The TMS (Test Mode Select) signal is a JTAG support signal used by debug tools.
TRDY#	I GTL+	The TRDY# (Target Ready) signal is asserted by the target to indicate that the target is ready to receive write or implicit write-back data transfer. TRDY# must be connected to the appropriate pins/balls on both agents on the system bus.
TRST#	I 1.5V Tolerant	The TRST# (Test Reset) signal resets the Test Access Port (TAP) logic. The mobile Pentium III processors do not self-reset during power on; therefore, it is necessary to drive this signal low during power-on reset.

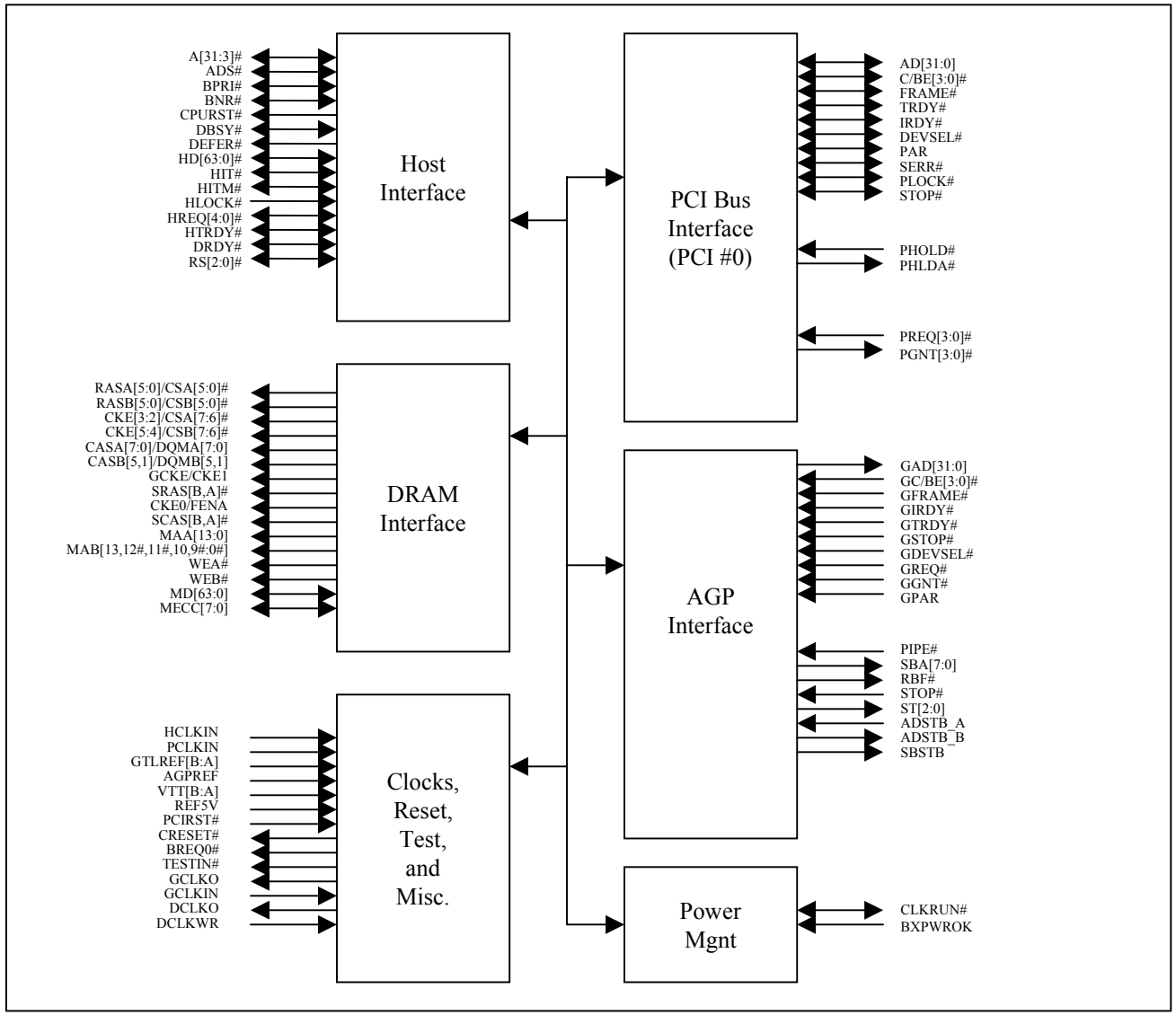
3.1 Intel µPGAII CPU Processor-6

PWRGOOD Relationship at Power On

Signal Name	I/O	Signal Description
VID[4:0]	O - Open-drain	The VID[4:0] (Voltage ID) pins/balls can be used to support automatic selection of power supply voltages. These pins/balls are not signals, they are either an open circuit or a short to VSS on the processor substrate. The combination of opens and shorts encodes the voltage required by the processor. External to pull-ups are required to sense the encoded VID. For processors that have Intel SpeedStep technology enabled, VID[4:0] encode the voltage required in the battery-optimized mode. VID[4:0] are needed to cleanly support voltage specification changes on mobile Pentium III processors. The voltage encoded by VID[4:0] is defined in Table 39. A "1" in this table refers to an open pin/ball and a "0" refers to a short to VSS. The power supply must provide the requested voltage or disable itself. Please note that in order to implement VID on the BGA2 package, some VID[4:0] balls may be depopulated. For the BGA2 package, a "1" in Table 39 implies that the corresponding VID ball is depopulated, while a "0" implies that the corresponding VID ball is not depopulated. But on the Micro-PGA2 package, VID[4:0] pins are not depopulated.

3.2 Intel 440BX Host Bridge Controller-1

- **Intel 82443BX Simplified Block Diagram:**



3.2 Intel 440BX Host Bridge Contrller-2

Table 3.2.1. Host Interface Signals (Sheet 1 of 2)

Name	Type	Description
CPURST#	O GTL+	**CPU Reset.** The CPURST# pin is an output from the 82443ZX. The 82443ZX generates this signal based on the PCIRST# input (from PIIX4E) and also the SUSTAT# pin in mobile mode. The CPURST# allows the CPUs to begin execution in a known state.
A[31:3]#	I/O GTL+	**Address Bus:** A[31:3]# connect to the CPU address bus. During CPU cycles, the A[31:3]# are inputs.
HD[63:0]#	I/O GTL+	**Host Data:** These signals are connected to the CPU data bus. Note that the data signals are inverted on the CPU bus.
ADS#	I/O GTL+	**Address Strobe:** The CPU bus owner asserts ADS# to indicate the first of two cycles of a request phase.
BNR#	I/O GTL+	**Block Next Request:** Used to block the current request bus owner from issuing a new request. This signal is used to dynamically control the CPU bus pipeline depth.
BPRI#	O GTL+	**Priority Agent Bus Request:** The 82443ZX is the only Priority Agent on the CPU bus. It asserts this signal to obtain the ownership of the address bus. This signal has priority over symmetric bus requests and will cause the current symmetric owner to stop issuing new transactions unless the HLOCK# signal was asserted.
BREQ0#	O GTL+	**Symmetric Agent Bus Request:** Asserted by the 82443ZX when CPURST# is asserted to configure the symmetric bus agents. BREQ0# is negated 2 host clocks after CPURST# is negated.
DBSY#	I/O GTL+	**Data Bus Busy:** Used by the data bus owner to hold the data bus for transfers requiring more than one cycle.
DEFER#	O GTL+	**Defer:** The 82443ZX generates a deferred response as defined by the rules of the 82443ZX? dynamic defer policy. The 82443ZX also uses the DEFER# signal to indicate a CPU retry response.
DRDY#	I/O GTL+	**Data Ready:** Asserted for each cycle that data is transferred.
HIT#	I/O GTL+	**Hit:** Indicates that a caching agent holds an unmodified version of the requested line. Also driven in conjunction with HITM# by the target to extend the snoop window.
HITM#	I/O GTL+	**Hit Modified:** Indicates that a caching agent holds a modified version of the requested line and that this agent assumes responsibility for providing the line. Also driven in conjunction with HIT# to extend the snoop window.
HLOCK#	I GTL+	**Host Lock:** All CPU bus cycles sampled with the assertion of HLOCK# and ADS#, until the negation of HLOCK# must be atomic, i.e. no PCI or AGP snoopable access to DRAM is allowed when HLOCK# is asserted by the CPU.
HREQ[4:0]#	I/O GTL+	**Request Command:** Asserted during both clocks of request phase. In the first clock, the signals define the transaction type to a level of detail that is sufficient to begin a snoop request. In the second clock, the signals carry additional information to define the complete transaction type. The transactions supported by the 82443ZX Host Bridge are defined in the Host Interface section of this document.
HTRDY#	I/O GTL+	**Host Target Ready:** Indicates that the target of the CPU transaction is able to enter the data transfer phase.

Table 3.2.1. Host Interface Signals (Sheet 2 of 2)

Name	Type	Description
RS[2:0]#	I/O GTL+	**Response Signals:** Indicates type of response according to the following the table: **RS[2:0] Response type** 000 Idle state 001 Retry response 010 Deferred response 011 Reserved (not driven by 82443ZX) 100 Hard Failure (not driven by 82443ZX) 101 No data response 110 Implicit Writeback 111 Normal data response

Table 3.2.2. Host Signals Not supported by the 82443ZX

Signal	Function	Not Supported By 82443ZX
A[35:32]#	Address	Extended addressing (over 4 GB)
AERR#	Address Parity Error	Parity protection on address bus
AP[1:0]#	Address Parity	Parity protection on address bus
BINIT#	Bus Initialization	Checking for bus protocol violation and protocol recovery mechanism
DEP[7:0]#	Data Bus ECC/Parity	Enhanced data bus integrity
IERR#	Internal Error	Direct internal error observation via IERR# pin
INIT#	Soft Reset	Implemented by PIIX4E, BIST supported by external logic.
BERR#	Bus Error	Unrecoverable error without a bus protocol violation
RP#	Request Parity	Parity protection on ADS# and PREQ[4:0]#
RSP#	Response Parity Signal	Parity protection on RS[2:0]#

Table 3.2.3. DRAM Interface Signals (Sheet 1 of 2)

Name	Type	Description
RASA[3:0]# /CSA[3:0]# RASB[3:0]# /CSB[3:0]#	O CMOS	**Row Address Strobe (EDO):** These signals are used to latch the row address on the MAxx lines into the DRAMs. Each signal is used to select one DRAM row. These signals drive the DRAM array directly without any external buffers. **Chip Select (SDRAM):** For the memory row configured with SDRAM these pins perform the function of selecting the particular SDRAM components during the active state. Note that there are 2 copies of RAS# per physical memory row to improve the loading.
CKE[3:2]	O CMOS	CKE is used to dynamically power down inactive SDRAM rows. Note that there are 2 copies of CS# per physical memory row to reduce the loading.
CASA[7:0]# /DQMA[7:0]	O CMOS	**Column Address Strobe A-side (EDO):** The CASA[7:0]# signals are used to latch the column address on the MA[13:0] lines into the DRAMs of the A half of the memory array. These are active low signals that drive the DRAM array directly without external buffering. **Input/Output Data Mask A-side (SDRAM):** These pins control the A half of the memory array and act as synchronized output enables during read cycles and as a byte enables during write cycles.

3.2 Intel 440BX Host Bridge Controller-3

Table 3.2.3. DRAM Interface Signals (Sheet 2 of 2)

Name	Type	Description
GCKE/CKE1	O CMOS	**Global CKE (SDRAM):** Global CKE is normally used in an 82443BX 4 DIMM configuration requiring power down mode for the SDRAM. External logic must be used to implement this function in an 82443BX. This function is not supportrd in an 82443ZX. **SDRAM Clock Enable (CKE1):** In mobile mode, SDRAM Clock Enable is used to signal a self-refresh or power-down command to an SDRAM array when entering system suspend. CKE is also used to dynamically power down inactive SDRAM rows. The combination of SDRAMPWR (SDRAM register) and MMCONFIG (DRAMC register) determine the functioning of the CKE signals. Refer to the DRAMC register (Section 3.3.15, ? RAMC? RAM Control Register (Device 0)?on page 3-19) for more details.
SRAS[A]#	O CMOS	**SDRAM Row Address Strobe (SDRAM):** The SRAS[A]# signal is a copy of the same logical SRASx signal (for loading purposes) used to generate SDRAM command encoded on SRASx/SCASx/WE signals.
CKE0/FENA	O CMOS	**SDRAM Clock Enable 0 (CKE0).** In mobile mode, CKE0 SDRAM Clock Enable is used to signal a self-refresh or power-down command to an SDRAM array when entering system suspend. CKE is also used to dynamically power down inactive SDRAM rows. **FET Enable (FENA):** In a 4 DIMM configuration. FENA is used to select the proper MD path through the FET switches (refer to Section 4.3, ? RAM Interface on page 4-14 for more details). This function is not supported in the 82443ZX.
SCAS[A]#	O CMOS	**SDRAM Column Address Strobe (SDRAM):** The SCAS[A]# signal is a copy of the same logical SCASx signal (for loading purposes) used to generate SDRAM command encoded on SRASx/SCASx/WE signals.
MAA[13:0] STRAP5 STRAP4 STRAP3 STRAP2 STRAP1 STRAP0	O CMOS	**Memory Address(EDO/SDRAM):** MAA[13:0] are used to provide the row and column address to DRAM. Each MAA[13:0] line has a programmable buffer strength to optimize for different signal loading conditions. STRAP[5:0] are described in Table 2-10, Strapping Options.
WEA#	O CMOS	**Write Enable Signal (EDO/SDRAM):** WE# is asserted during writes to DRAM. The WE# lines have a programmable buffer strength to optimize for different signal loading conditions.
MD [63:0]	I/O CMOS	**Memory Data (EDO/SDRAM):** These signals are used to interface to the DRAM data bus.

Table 3.2.4. Primary PCI Interface Signals (Sheet 1 of 2)

Name	Type	Description
AD[31:0]	I/O PCI	**PCI Address/Data:** These signals are connected to the PCI address/data bus. Address is driven by the 82443ZX with FRAME# assertion, data is driven or received in the following clocks. When the 82443ZX acts as a target on the PCI Bus, the AD[31:0] signals are inputs and contain the address during the first clock of FRAME# assertion and input data (writes) or output data (reads) on subsequent clocks.
DEVSEL#	I/O PCI	**Device Select:** Device select, when asserted, indicates that a PCI target device has decoded its address as the target of the current access. The 82443ZX asserts DEVSEL# based on the DRAM address range or AGP address range being accessed by a PCI initiator. As an input it indicates whether any device on the bus has been selected.
FRAME#	I/O PCI	**Frame:** FRAME# is an output when the 82443ZX acts as an initiator on the PCI Bus. FRAME# is asserted by the 82443ZX to indicate the beginning and duration of an access. The 82443ZX asserts FRAME# to indicate a bus transaction is beginning. While FRAME# is asserted, data transfers continue. When FRAME# is negated, the transaction is in the final data phase. FRAME# is an input when the 82443ZX acts as a PCI target. As a PCI target, the 82443ZX latches the C/BE[3:0]# and the AD[31:0] signals on the first clock edge on which it samples FRAME# active.
IRDY#	I/O PCI	**Initiator Ready:** IRDY# is an output when 82443ZX acts as a PCI initiator and an input when the 82443ZX acts as a PCI target. The assertion of IRDY# indicates the current PCI Bus initiator's ability to complete the current data phase of the transaction.
C/BE[3:0]#	I/O PCI	**Command/Byte Enable:** PCI Bus Command and Byte Enable signals are multiplexed on the same pins. During the address phase of a transaction, C/BE[3:0]# define the bus command. During the data phase C/BE[3:0]# are used as byte enables. The byte enables determine which byte lanes carry meaningful data. PCI Bus command encoding and types are listed below. **C/BE[3:0]# Command Type** 0000 Interrupt Acknowledge 0001 Special Cycle 0010 I/O Read 0011 I/O Write 0100 Reserved 0101 Reserved 0110 Memory Read 0111 Memory Write 1000 Reserved 1001 Reserved 1010 Configuration Read 1011 Configuration Write 1100 Memory Read Multiple 1101 Reserved (Dual Address Cycle) 1110 Memory Read Line 1111 Memory Write and Invalidate

3.2 Intel 440BX Host Bridge Controller-4

Table 3.2.4. Primary PCI Interface Signals (Sheet 2 of 2)

Name	Type	Description
PAR	I/O PCI	**Parity:** PAR is driven by the 82443ZX when it acts as a PCI initiator during address and data phases for a write cycle, and during the address phase for a read cycle. PAR is driven by the 82443ZX when it acts as a PCI target during each data phase of a PCI memory read cycle. Even parity is generated across AD[31:0] and C/BE[3:0]#.
PLOCK#	I/O PCI	**Lock:** PLOCK# indicates an exclusive bus operation and may require multiple transactions to complete. When PLOCK# is asserted, non-exclusive transactions may proceed. The 82443ZX supports lock for CPU initiated cycles only. PCI initiated locked cycles are not supported.
TRDY#	I/O PCI	**Target Ready:** TRDY# is an input when the 82443ZX acts as a PCI initiator and an output when the 82443ZX acts as a PCI target. The assertion of TRDY# indicates the target agent's ability to complete the current data phase of the transaction.

Name	Type	Description
SERR#	I/O PCI	**System Error:** The 82443ZX asserts this signal to indicate an error condition. The SERR# assertion by the 82443ZX is enabled globally via SERRE bit of the PCICMD register. SERR# is asserted under the following conditions: In an ECC configuration, the 82443ZX asserts SERR#, for single bit (correctable) ECC errors or multiple bit (non-correctable) ECC errors if SERR# signaling is enabled via the ERRCMD control register. Any ECC errors received during initialization should be ignored. •The 82443ZX asserts SERR# for one clock when it detects a target abort during 82443ZX initiated PCI cycle. •The 82443ZX can also assert SERR# when a PCI parity error occurs during the address or data phase. •The 82443ZX can assert SERR# when it detects a PCI address or data parity error on AGP. •The 82443ZX can assert SERR# upon detection of access to an invalid entry in the Graphics Aperture Translation Table. •The 82443ZX can assert SERR# upon detecting an invalid AGP master access outside of AGP aperture and outside of main DRAM range (i.e. in the 640k - 1M range or above TOM). •The 82443ZX can assert SERR# upon detecting an invalid AGP master access outside of AGP aperture. •The 82443ZX asserts SERR# for one clock when it detects a target abort during 82443ZX initiated AGP cycle.
STOP#	I/O PCI	**Stop:** STOP# is an input when the 82443ZX acts as a PCI initiator and an output when the 82443ZX acts as a PCI target. STOP# is used for disconnect, retry, and abort sequences on the PCI Bus.

Table 3.2.5. Primary PCI Sideband Interface Signals

Name	Type	Description
PHOLD#	I PCI	**PCI Hold:** This signal comes from the PIIX4E. It is the PIIX4E request for PCI bus ownership. The 82443ZX will flush and disable the CPU-to-PCI write buffers before granting the PIIX4E the PCI bus via PHLDA#. This prevents bus deadlock between PCI and ISA.
PHLDA#	O PCI	**PCI Hold Acknowledge:** This signal is driven by the 82443ZX to grant PCI bus ownership to the PIIX4E after CPU-PCI post buffers have been flushed and disabled.
PREQ[3:0]#	I PCI	**PCI Bus Request:** PREQ[3:0]# are the PCI bus request signals used as inputs by the internal PCI arbiter.
PGNT[3:0]#	O PCI	**PCI Grant: P**GNT[3:0]# are the PCI bus grant output signals generated by the internal PCI arbiter.

Table 3.2.6. AGP Interface Signals(Sheet 1 of 3)

Name	Type	Description
		AGP Sideband Addressing Signals 1
PIPE#	I AGP	**Pipelined Read:** This signal is asserted by the current master to indicate a full width address is to be queued by the target. The master queues one request each rising clock edge while PIPE# is asserted. When PIPE# is deasserted no new requests are queued across the AD bus. PIPE# is a sustained tri-state signal from masters (graphics controller) and is an input to the 82443ZX. Note that initial AGP designs may not use PIPE#.
SBA[7:0]	I AGP	**Sideband Address:** This bus provides an additional bus to pass address and command to the 82443ZX from the AGP master. Note that, when sideband addressing is disabled, these signals are isolated (no external/internal pull-ups are required).
		AGP Flow Control Signals
RBF#	I AGP	**Read Buffer Full.** This signal indicates if the master is ready to accept previously requested low priority read data. When RBF# is asserted the 82443ZX is not allowed to return low priority read data to the AGP master on the first block. RBF# is only sampled at the beginning of a cycle. If the AGP master is always ready to accept return read data then it is not required to implement this signal.

3.2 Intel 440BX Host Bridge Controller-5

Table 3.2.6. AGP Interface Signals(Sheet 2 of 3)

Name	Type	Description
AGP Status Signals		
ST[2:0]	O AGP	**Status Bus:** This bus provides information from the arbiter to a AGP Master on what it may do. ST[2:0] only have meaning to the master when its GGNT# is asserted. When GGNT# is deasserted these signals have no meaning and must be ignored. 000 Indicates that previously requested low priority read data is being returned to the master. 001 Indicates that previously requested high priority read data is being returned to the master. 010 Indicates that the master is to provide low priority write data for a previously queued write command. 011 Indicates that the master is to provide high priority write data for a previously queued write command. 100 Reserved 101 Reserved 110 Reserved 111 Indicates that the master has been given permission to start a bus transaction. The master may queue AGP requests by asserting PIPE# or start a PCI transaction by asserting FRAME#. ST[2:0] are always an output from the 82443ZX and an input to the master.
AGP Clocking Signals – Strobes		
ADSTB_A	I/O AGP	**AD Bus Strobe A:** This signal provides timing for double clocked data on the AD bus. The agent that is providing data drives this signal. This signal requires an 8.2K ohm external pull-up resistor.
ADSTB_B	I/O AGP	**AD Bus Strobe B:** This signal is an additional copy of the AD_STBA signal. This signal requires an 8.2K ohm external pull-up resistor.
SBSTB	I AGP	**Sideband Strobe:** THis signal provides timing for a side-band bus. This signal requires an 8.2K ohm external pull-up resistor.
AGP FRAME# Protocol SIgnals (similar to PCI)2		
GFRAME#	I/O AGP	**Graphics Frame:** Same as PCI. Not used by AGP. GFRAME# remains deasserted by its own pull up resistor.

Table 3.2.6. AGP Interface Signals(Sheet 3 of 3)

Name	Type	Description
GIRDY#	I/O AGP	**Graphics Initiator Ready:** New meaning. GIRDY# indicates the AGP compliant master is ready to provide all write data for the current transaction. Once IRDY# is asserted for a write operation, the master is not allowed to insert wait states. The assertion of IRDY# for reads indicates that the master is ready to transfer to a subsequent block (32 bytes) of read data. The master is never allowed to insert wait states during the initial data transfer (32 bytes) of a read transaction. However, it may insert wait states after each 32 byte block is transferred. (There is no GFRAME# -- GIRDY# relationship for AGP transactions.)
GTRDY#	I/O AGP	**Graphics Target Ready:** New meaning. GTRDY# indicates the AGP compliant target is ready to provide read data for the entire transaction (when the transfer size is less than or equal to 32 bytes) or is ready to transfer the initial or subsequent block (32 bytes) of data when the transfer size is greater than 32 bytes. The target is allowed to insert wait states after each block (32 bytes) is transferred on both read and write transactions.
GSTOP#	I/O AGP	**Graphics Stop:** Same as PCI. Not used by AGP.
GDEVSEL #	I/O AGP	**Graphics Device Select:** Same as PCI. Not used by AGP.
GREQ#	I AGP	**Graphics Request:** Same as PCI. (Used to request access to the bus to initiate a PCI or AGP request.)
GGNT#	O AGP	**Graphics Grant:** Same meaning as PCI but additional information is provided on ST[2:0]. The additional information indicates that the selected master is the recipient of previously requested read data (high or normal priority), it is to provide write data (high or normal priority), for a previously queued write command or has been given permission to start a bus transaction (AGP or PCI).
GAD[31:0]	I/O AGP	**Graphics Address/Data:** Same as PCI.
GC/BE[3:0] #	I/O AGP	**Graphics Command/Byte Enables:** Slightly different meaning. Provides command information (different commands than PCI) when requests are being queued when using PIPE#. Provide valid byte information during AGP write transactions and are not used during the return of read data.
GPAR	I/O AGP	**Graphics Parity:** Same as PCI. Not used on AGP transactions, but used during PCI transactions as defined by the PCI specification.

3.2 Intel 440BX Host Bridge Controller-6

Table 3.2.7. Clocks,Reset,and Miscellaneous

Name	Type	Description
HCLKIN	I CMOS	**Host Clock In:** This pin receives a buffered host clock. This clock is used by all of the 82443ZX logic that is in the Host clock domain.
PCLKIN	I CMOS	**PCI Clock In:** This is a buffered PCI clock reference that is synchronously derived by an external clock synthesizer component from the host clock. This clock is used by all of the 82443ZX logic that is in the PCI clock domain.
DCLKO	O CMOS	**SDRAM Clock Out:** 66 or 100 MHz SDRAM clock reference. It feeds an external buffer clock device that produces multiple copies for the DIMMs.
DCLKWR	I CMOS	**SDRAM Write Clock:** Feedback reference from the external SDRAM clock buffer. This clock is used by the 82443ZX when writing data to the SDRAM array. Note: See the Design Guide for routing constraints.
PCIRST#	I CMOS	**PCI Reset:** When asserted, this signal will reset the 82443ZX logic. All PCI output and bi-directional signals will also tri-state compliant to PCI Rev 2.0 and 2.1 specifications.
GCLKIN	I CMOS	**AGP Clock In:** The GCLKIN input is a feedback reference from the GCLKOUT signal.
GCLKO	O CMOS	**AGP Clock Out:** The frequency is 66 MHz. The GCLKOUT output is used to feed both the reference input pin on the 82443ZX and the AGP compliant device.
CRESET#	O CMOS	**Delayed CPU Reset:** CRESET# is a delayed copy of CPURST#. This signal is used to control the multiplexer for the CPU strap signals. CRESET# is delayed from CPURST# by two host clocks. **Note:** This pin requires an external pull-up resistor. If not used, no pull up is required.
TESTIN#	I CMOS	**Test Input:** This pin is used for manufacturing, and board level test purposes. Note: This pin has an internal 50K ohm pull-up.

Table 3.2.8. Power Management Interface

Name	Type	Description
CLKRUN#	I/OD CMOS	**Primary PCI Clock Run:** The 82443ZX requests the central resource (PIIX4E) to start or maintain the PCI clock by the assertion of CLKRUN#. The 82443ZX tristates CLKRUN# upon deassertion of PCIRST# (since CLK is running upon deassertion of reset). If connected to PIIX4E an external 2.7K Ohm pull-up is required for Desktop, Mobile requires (8.2k?0K) pull-up. Otherwise, a 100 Ohm pull down is required.
BXPWROK	I CMOS	**BX Power OK:** BXPWROK input must be connected to the PWROK signal that indicates valid power is applied to the 82443ZX.

Table 3.2.9. Reference Pins

Name	Description
GTLREF[B:A]	GTL Buffer voltage reference input
VTT[B:A]	GTL Threshold voltage for early clamps
VCC	Power pin @ 3.3V
VSS	Ground
REF5V	PCI 5V reference voltage (for 5V tolerant buffers)
AGPREF	External Input Reference

Table 3.2.10. Strapping Options (Sheet 1 of 2)

Signal	Register Name[bit]	Description
MAB13#		**Reserved**.
STRAP5	NBXCFG[13]	**Host Frequency Select:** If STRAP5 is strapped to 0, the host bus frequency is 60/ 66 MHz. If STRAP5 is strapped to 1, the host bus frequency is 100 MHz. An internal pull-down is used to provide the default setting of 66 MHz.
STRAP4	NBXCFG[2]	**In-Order Queue Depth Enable.** If STRAP4 is strapped to 0 during the rising edge of PCIRST#, then the 82442BX will drive A7# low during the CPURST# deassertion. This forces the CPU bus to be configured for non-pipelined operation. If STRAP4 is strapped to 1 (default), then the 82443ZX does not drive the A7# low during reset, and A7# is sampled in default non-driven state (i.e. pulled-up as far as GTL+ termination is concerned) then the maximum allowable queue depth by the CPU bus protocol is selected (i.e., 8). Note that internal pull-up is used to provide pipelined bus mode as a default.
STRAP3	PMCR[3]	**Quick Start Select.** The value on this pin at reset determines which stop clock mode is used. STRAP3 = 0 (default) for normal stop clock mode. If STRAP3 = 1 during the rising edge of PCIRST#, then the 82443ZX will drive A15# low during CPURST# deassertion. This will configure the CPU for Quick Start mode of operation. Note that internal pull-down is used to provide normal stop clock mode as a default.
STRAP2	PMCR[1]	**AGP Disable:** When strapped to a 1, the AGP interface is disabled, all AGP Signals are tri-stated and isolated. When strapped to a 0 (default), the AGP Interface is enabled. When MMCONFIG is strapped active, we require that AGP_DISABLE is also strapped active. When MMCONFIG is strapped inactive, AGP_DISABLE can be strapped active or inactive but IDSEL_REDIRECT (bit 16 in NBXCFG register) must never be activated. This signal has an internal pull-down resistor.
MAB8#		**Reserved.**

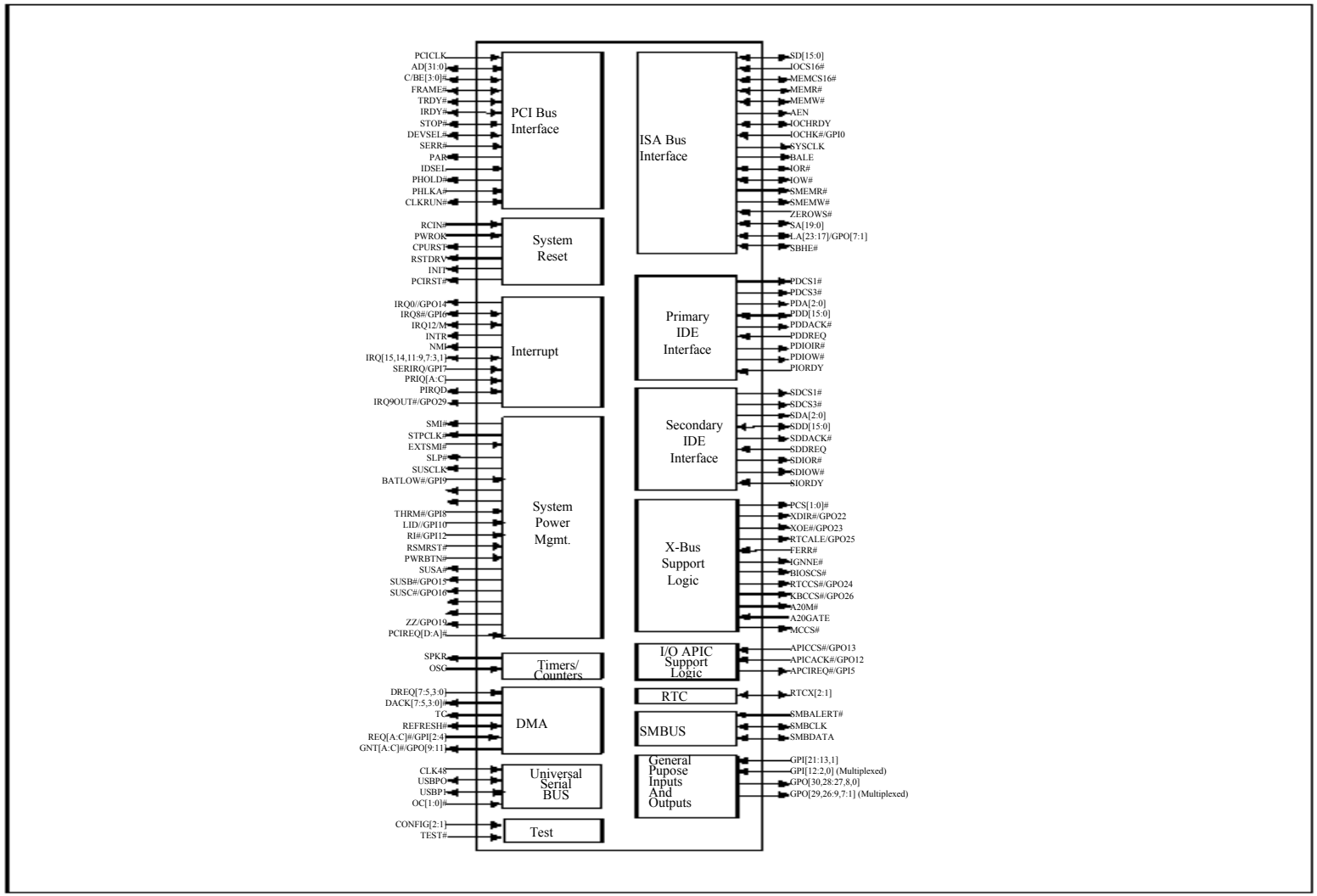
3.2 Intel 440BX Host Bridge Controller-7

Table 3.2.10. Strapping Options (Sheet 2 of 2)

Signal	Register Name[bit]	Description
STRAP 1	DRAMC[5]	**Memory Module Configuration, MMCONFIG:** When strapped to a 1, the 82443ZX configures its DRAM interface in a 430-TX compatible manner. These unused inputs are isolated while unused outputs are tri-stated: RASB[3:0]#/ CSB[3:0]#, CKE[3:2], GCKE/CKE1, MAA[13:0], DCLKO. When strapped to a 0 (default), the 82443ZX DRAM signal are used normally. IDSEL_REDIRECT (bit 16 in NBXCFG register) is programmed by BIOS, before it begins with device enumeration process. The combination of SDRAMPWR (SDRAMC register) and MMCONFIG (DRAMC register) determine the functioning of the CKE signals. Refer to the DRAMC register for more details. Note that internal pull-down is used to set the DRAM interface to a normal Configuration, as a default.
STRAP 0	none	**Host Bus Buffer Mode Select:** When strapped 0, the desktop GTL+ 66 MHz or 100 MHz host bus buffers are used (default). When strapped ?? the mobile Low Power GTL+ 66 MHz host bus buffers are selected. Note that an internal pull-down is used to set the host bus buffers to a desktop configuration as a default in the 82443ZX. An external pull-up therefore is needed for mobile systems using the 82443BX or 82443DX.
A[15]#	none	**Quick Start Select.** The value on A15# sampled at the rising edge of CPURST# will reflect if the quick start/stop clock mode is enabled in the processors.
A7#	none	**In-order Queue Depth Status.** The value on A[7]# sampled at the rising edge of CPURST# reflects if the IOQD is set to 1 or maximum allowable by the CPU bus.

3.3 Intel 82371MB PCI to ISA/IDE Xcelerator (PIIX4M)-1

- **82371MB PCI-TO-ISA / IDE XCELERATOR (PIIX4):**



Simplified Block Diagram

3.3 Intel 82371MB PCI to ISA/IDE Xcelerator (PIIX4M)-2

PIIX4 Signals

3.3.1 PCI BUS INTERFACE (Sheet 1 of 3)

Name	Type	Description
AD[31:0]	I/O	**PCI ADDRESS/DATA.** AD[31:0] is a multiplexed address and data bus. During the first clock of a transaction, AD[31:0] contain a physical byte address (32 bits). During subsequent clocks, AD[31:0] contain data. A PIIX4 Bus transaction consists of an address phase followed by one or more data phases. Little-endian byte ordering is used. AD[7:0] define the least significant byte (LSB) and AD[31:24] the most significant byte (MSB). When PIIX4 is a Target, AD[31:0] are inputs during the address phase of a transaction. During the following data phase(s), PIIX4 may be asked to supply data on AD[31:0] for a PCI read, or accept data for a PCI write. As an Initiator, PIIX4 drives a valid address on AD[31:2] and 0 on AD[1:0] during the address phase, and drives write or latches read data on AD[31:0] during the data phase. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
C/BE#[3:0]	I/O	**BUS COMMAND AND BYTE ENABLES.** The command and byte enable signals are multiplexed on the same PCI pins. During the address phase of a transaction, C/BE[3:0]# define the bus command. During the data phase C/BE[3:0]# are used as Byte Enables. The Byte Enables determine which byte lanes carry meaningful data. C/BE0# applies to byte 0, C/BE1# to byte 1, etc. PIIX4 drives C/BE[3:0]# as an Initiator and monitors C/BE[3:0]# as a Target. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
CLKRUN#	I/O	**CLOCK RUN#.** This signal is used to communicate to PCI peripherals that the PCI clock will be stopped. Peripherals can assert CLKRUN# to request that the PCI clock be restarted or to keep it from stopping. This function follows the protocol described inthe PCI Mobile Design Guide, Revision 1.0. **During Reset:** Low **After Reset:** Low **During POS:** High
DEVSEL#	I/O	**DEVICE SELECT.** PIIX4 asserts DEVSEL# to claim a PCI transaction through positive decoding or subtractive decoding (if enabled). As an output, PIIX4 asserts DEVSEL# when it samples IDSEL active in configuration cycles to PIIX4 configuration registers. PIIX4 also asserts DEVSEL# when an internal PIIX4 address is decoded or when PIIX4 subtractively or positively decodes a cycle for the ISA/EIO bus or IDE device. As an input, DEVSEL# indicates the response to a PIIX4 initiated transaction and is also sampled when deciding whether to subtractively decode the cycle. DEVSEL# is tri-stated from the leading edge of PCIRST#. DEVSEL# remains tri-stated until driven by PIIX4 as a target. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z

3.3.1 PCI BUS INTERFACE (Sheet 2 of 3)

Name	Type	Description
FRAME#	I/O	**CYCLE FRAME.** FRAME# is driven by the current Initiator to indicate the beginning and duration of an access. While FRAME# is asserted data transfers continue. When FRAME# is negated the transaction is in the final data phase. FRAME# is an input to PIIX4 when it is the Target. FRAME# is an output when PIIX4 is the initiator. FRAME# remains tri-stated until driven by PIIX4 as an Initiator. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
IDSEL	I	**INITIALIZATION DEVICE SELECT.** IDSEL is used as a chip select during PCI configuration read and write cycles. PIIX4 samples IDSEL during the address phase of a transaction. If IDSEL is sampled active, and the bus command is a configuration read or write, PIIX4 responds by as serting DEVSEL# on the next cycle.
IRDY#	I/O	**INITIATOR READY.** IRDY# indicates PIIX4• ability, as an Initiator, to complete the current data phase of the transaction. It is used in conjunction with TRDY#. A data phase is completed on any clock both IRDY# and TRDY# are sampled asserted. During a write, IRDY# indicates PIIX4 has valid data present on AD[31:0]. During a read, it indicates PIIX4 is prepared to latch data. IRDY# is an input to PIIX4 when PIIX4 is the Target and an output when PIIX4 is an Initiator. IRDY# remains tri-stated until driven by PIIX4 as a master. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
PAR	O	**CALCULATED PARITY SIGNAL.** PAR is " even" parity and is calculated on 36 bits; AD[31:0] plus C/BE[3:0]#. " Even" parity means that the number of " 1" within the 36 bits plus PAR are counted and the sum is always even. PAR is always calculated on 36 bits regardless of the valid byte enables. PAR is generated for address and data phases and is only guaranteed to be valid one PCI clock after the corresponding address or data phase. PAR is driven and tri-stated identically to the AD[31:0] lines except that PAR is delayed by exactly one PCI clock. PAR is an output during the address phase (delayed one clock) for all PIIX4 initiated transactions. It is also an output during the data phase (delayed one clock) when PIIX4 is the Initiator of a PCI write transaction, and when it is the Target of a read transaction. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z

3.3 Intel 82371MB PCI to ISA/IDE Xcelerator (PIIX4M)-3

3.3.1 PCI BUS INTERFACE (Sheet 3 of 3)

Name	Type	Description
PCIRST#	O	**PCI RESET.** PIIX4 asserts PCIRST# to reset devices that reside on the PCI bus. PIIX4 asserts PCIRST# during power-up and when a hard reset sequence is initiated through the RC register. PCIRST# is driven inactive a minimum of 1 ms after PWROK is driven active. PCIRST# is driven for a minimum of 1 ms when initiated through the RC register. PCIRST# is driven asynchronously relative to PCICLK. **During Reset:** Low **After Reset:** High **During POS:** High
PHOLD#	O	**PCI HOLD.** An active low assertion indicates that PIIX4 desires use of the PCI Bus. Once the PCI arbiter has asserted PHLDA# to PIIX4, it may not negate it until PHOLD# is negated by PIIX4. PIIX4 implements the passive release mechanism by toggling PHOLD# inactive for one PCICLK. **During Reset:** High-Z **After Reset:** High **During POS:** High
PHLDA#	I	**PCI HOLD ACKNOWLEDGE.** An active low assertion indicates that PIIX4 has been granted use of the PCI Bus. Once PHLDA# is asserted, it cannot be negated unless PHOLD# is negated first.
SERR#	I/O	**SYSTEM ERROR.** SERR# can be pulsed active by any PCI device that detects a system error condition. Upon sampling SERR# active, PIIX4 can be programmed to generate a non-maskable interrupt (NMI) to the CPU. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
STOP#	I/O	**STOP.** STOP# indicates that PIIX4, as a Target, is requesting an initiator to stop the current transaction. As an Initiator, STOP# causes PIIX4 to stop the current transaction. STOP# is an output when PIIX4 is a Target and an input when PIIX4 is an Initiator. STOP# is tri-stated from the leading edge of PCIRST#. STOP# remains tri-stated until driven by PIIX4 as a slave. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
TRDY#	I/O	**TARGET READY.** TRDY# indicates PIIX4 ability to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#. A data phase is completed when both TRDY# and IRDY# are sampled asserted. During a read, TRDY# indicates that PIIX4, as a Target, has place valid data on AD[31:0]. During a write, it indicates PIIX4, as a Target is prepared to latch data. TRDY# is an input to PIIX4 when PIIX4 is the Initiator and an output when PIIX4 is a Target. TRDY# is tri-stated from the leading edge of PCIRST#. TRDY# remains tri-stated until driven by PIIX4 as a slave. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z

3.3.2. ISA BUS INTERFACE (Sheet 1 of 4)

Name	Type	Description
AEN	O	**ADDRESS ENABLE.** AEN is asserted during DMA cycles to prevent I/O slaves from misinterpreting DMA cycles as valid I/O cycles. When negated, AEN indicates that an I/O slave may respond to address and I/O commands. When asserted, AEN informs I/O resources on the ISA bus that a DMA transfer is occurring. This signal is also driven high during PIIX4 initiated refresh cycles. **During Reset:** High-Z **After Reset:** Low **During POS:** Low
BALE	O	**BUS ADDRESS LATCH ENABLE.** BALE is asserted by PIIX4 to indicate that the address (SA[19:0], LA[23:17]) and SBHE# signal lines are valid. The LA[23:17] address lines are latched on the trailing edge of BALE. BALE remains asserted throughout DMA and ISA master cycles. **During Reset:** High-Z **After Reset:** Low **During POS:** Low
IOCHK#/	I GPI0	**I/O CHANNEL CHECK.** IOCHK# can be driven by any resource on the ISA bus. When asserted, it indicates that a parity or an uncorrectable error has occurred for a device or memory on the ISA bus. A NMI will be generated to the CPU if the NMI generation is enabled. If the EIO bus is used, this signal becomes a general purposeinput.
IOCHRDY	I/O	**I/O CHANNEL READY.** Resources on the ISA Bus negate IOCHRDY to indicate that wait states are required to complete the cycle. This signal is normally high. IOCHRDY is an input when PIIX4 owns the ISA Bus and the CPU or a PCI agent is accessing an ISA slave, or during DMA transfers. IOCHRDY is output when an external ISA Bus Master owns the ISA Bus and is accessing DRAM or a PIIX4 register. As a PIIX4 output, IOCHRDY is driven inactive (low) from the falling edge of the ISA commands. After data is available for an ISA master read or PIIX4 latches the data for a write cycle, IOCHRDY is asserted for 70 ns. After 70 ns, PIIX4 floats IOCHRDY. The 70 ns includes both the drive time and the time it takes PIIX4 to float IOCHRDY. PIIX4 does not drive this signal when an ISA Bus master is accessing an ISA Bus slave. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
IOCS16#	I	**16-BIT I/O CHIP SELECT.** This signal is driven by I/O devices on the ISA Bus to indicate support for 16-bit I/O bus cycles.
IOR#	I/O	**I/O READ.** IOR# is the command to an ISA I/O slave device that the slave may drive data on to the ISA data bus (SD[15:0]). The I/O slave device must hold the data valid until after IOR# is negated. IOR# is an output when PIIX4 owns the ISA Bus. IOR# isan input when an external ISA master owns the ISA Bus. **During Reset:** High-Z **After Reset:** High **During POS:** High

3.3 Intel 82371MB PCI to ISA/IDE Xcelerator (PIIX4M)-4

3.3.2. ISA BUS INTERFACE (Sheet 2of 4)

Name	Type	Description
IOW#	I/O	**I/O WRITE.** IOW# is the command to an ISA I/O slave device that the slave may latch data from the ISA data bus (SD[15:0]). IOW# is an output when PIIX4 owns the ISA Bus. IOW# is an input when an external ISA master owns the ISA Bus. **During Reset:** High-Z **After Reset:** High **During POS:** High
LA[23:17]/	I/O	**ISA LA[23:17].** LA[23:17] address lines allow accesses to physical memory on the ISA Bus up to 16 Mbytes. LA[23:17] are outputs when PIIX4 owns the ISA Bus. The LA[23:17] lines become inputs whenever an ISA master owns the ISA Bus. If the EIO bus is used, these signals become a general purpose output. **During Reset:** High-Z **After Reset:** Undefined **During POS:** Last LA/GPO
MEMCS16#	I/O	**MEMORY CHIP SELECT 16.** MEMCS16# is a decode of LA[23:17] without any qualification of the command signal lines. ISA slaves that are 16-bit memory devices drive this signal low. PIIX4 ignores MEMCS16# during I/O access cycles and refresh cycles. MEMCS16# is an input when PIIX4 owns the ISA Bus. PIIX4 drives this signal low during ISA master to PCI memory cycles. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
MEMR#	I/O	**MEMORY READ.** MEMR# is the command to a memory slave that it may drive data onto the ISA data bus. MEMR# is an output when PIIX4 is a master on the ISA Bus. MEMR# is an input when an ISA master, other than PIIX4, owns the ISA Bus. This signal is also driven by PIIX4 during refresh cycles. For DMA cycles, PIIX4, as a master, asserts MEMR#. **During Reset:** High-Z **After Reset:** High **During POS:** High
MEMW#	I/O	**MEMORY WRITE.** MEMW# is the command to a memory slave that it may latch data from the ISA data bus. MEMW# is an output when PIIX4 owns the ISA Bus. MEMW# is an input when an ISA master, other than PIIX4, owns the ISA Bus. For DMA cycles, PIIX4, as a master, asserts MEMW#. **During Reset:** High-Z **After Reset:** High **During POS:** High
MEMR#	O	**STANDARD MEMORY READ.** PIIX4 asserts SMEMR# to request an ISA memory slave to drive data onto the data lines. If the access is below the 1-Mbyte range (00000000-00FFFFFh) during DMA compatible, PIIX4 master, or ISA master cycles, PIIX4 asserts SMEMR#. SMEMR# is a delayed version of MEMR#. **During Reset:** High-Z **After Reset:** High **During POS:** High

3.3.2. ISA BUS INTERFACE (Sheet 3 of 4)

Name	Type	Description
REFRESH#	I/O	**REFRESH.** As an output, REFRESH# is used by PIIX4 to indicate when a refresh cycle is in progress. It should be used to enable the SA[7:0] address to the row address inputs of all banks of dynamic memory on the ISA Bus. Thus, when MEMR# is asserted, the entire expansion bus dynamic memory is refreshed. Memory slaves must not drive any data onto the bus during refresh. As an output, this signal is driven directly onto the ISA Bus. This signal is an output only when PIIX4 DMA refresh controller is a master on the bus responding to an internally generated request for refresh. As an input, REFRESH# is driven by 16-bit ISA Bus masters to initiate refresh cycles. **During Reset:** High-Z **After Reset:** High **During POS:** High
RSTDRV	O	**RESET DRIVE.** PIIX4 asserts RSTDRV to reset devices that reside on the ISA/EIO Bus. PIIX4 asserts this signal during a hard reset and during power-up. RSTDRV is asserted during power-up and negated after PWROK is driven active. RSTDRV is also driven active for a minimum of 1 ms if a hard reset has been programmed in the RC register. **During Reset:** High **After Reset:** Low **During POS:** Low
SA[19:0]	I/O	**SYSTEM ADDRESS[19:0].** These bi-directional address lines define the selection with the granularity of 1 byte within the 1-Megabyte section of memory defined by the LA[23:17] address lines. The address lines SA[19:17] that are coincident with LA[19:17] are defined to have the same values as LA[19:17] for all memory cycles. For I/O accesses, only SA[15:0] are used, and SA[19:16] are undefined. SA[19:0] are outputs when PIIX4 owns the ISA Bus. SA[19:0] are inputs when an external ISA Master owns the ISA Bus. **During Reset:** High-Z **After Reset:** Undefined **During POS:** Last SA
SBHE#	I/O	**SYSTEM BYTE HIGH ENABLE.** SBHE# indicates, when asserted, that a byte is being transferred on the upper byte (SD[15:8]) of the data bus. SBHE# is negated during refresh cycles. SBHE# is an output when PIIX4 ownsthe ISA Bus. SBHE# is an input when an external ISA master owns the ISA Bus. **During Reset:** High-Z **After Reset:** Undefined **During POS:** High
SSD[15:0]	I/O	**SYSTEM DATA.** SD[15:0] provide the 16-bit data path for devices residing on the ISA Bus. SD[15:8] correspond to the high order byte and SD[7:0] correspond to the low order byte. SD[15:0] are undefined during refresh. **During Reset:** High-Z **After Reset:** Undefined **During POS:** High-Z

3.3 Intel 82371MB PCI to ISA/IDE Xcelerator (PIIX4M)-5

3.3.2. ISA BUS INTERFACE (Sheet 4 of 4)

Name	Type	Description
SMEMW#	O	**STANDARD MEMORY WRITE.** PIIX4 asserts SMEMW# to request an ISA memory slave to accept data from the data lines. If the access is below the 1-Mbyte range (00000000-00FFFFFh) during DMA compatible, PIIX4 master, or ISA master cycles, PIIX4 asserts SMEMW#. SMEMW# is a delayed version of MEMW#. **During Reset:** High-Z **After Reset:** High **During POS:** High
ZEROWS#	I	**ZERO WAIT STATES.** An ISA slave asserts ZEROWS# after its address and command signals have been decoded to indicate that the current cycle can be shortened. A 16-bit ISA memory cycle can be reduced to two SYSCLKs. An 8-bit memory or I/O cycle can be reduced to three SYSCLKs. ZEROWS# has no effect during 16-bit I/O cycles. If IOCHRDY is negated and ZEROWS# is asserted during the same clock, then. ZEROWS# is ignored and wait states are added as a function of IOCHRDY.

3.3.3. X-BUS INTERFACE(Sheet 1 of3)

Name	Type	Description
A20GATE	I	**ADDRESS 20 GATE.** This input from the keyboard controller is logically combined with bit 1 (FAST_A20) of the Port 92 Register, which is then output via the A20M# signal.
BIOSCS#	O	**BIOS CHIP SELECT.** This chip select is driven active during read or write accesses to enabled BIOS memory ranges. BIOSCS# is driven combinatorially from the ISA addresses SA[16:0] and LA[23:17], except during DMA cycles. During DMA cycles, BIOSCS# is not generated. **During Reset:** High **After Reset:** High **During POS:** High
KBCCS#/ GPO26	O	**KEYBOARD CONTROLLER CHIP SELECT.** KBCCS# is asserted during I/O read or write accesses to KBC locations 60h and 64h. It is driven combinatorially from the ISA addresses SA[19:0] and LA[23:17]. If the keyboard controller does not require a separate chip select, this signal can be programmed to a general purpose output. **During Reset:** High **After Reset:** High **During POS:** High/GPO
MCCS#	O	**MICROCONTROLLER CHIP SELECT.** MCCS# is asserted during I/O read or write accesses to IO locations 62h and 66h. It is driven combinatorially from the ISA addresses SA[19:0] and LA[23:17]. **During Reset:** High **After Reset:** High **During POS:** High

3.3.3. X-BUS INTERFACE(Sheet 2 of3)

Name	Type	Description
PCS0# **PCS1#**	O	**PROGRAMMABLE CHIP SELECTS.** These active low chip selects are asserted for ISA I/O cycles which are generated by PCI masters and which hit the programmable I/O ranges defined in the Power Management section. The X-Bus buffer signals (XOE# and XDIR#) are enabled while the chip select is active. (i.e., it is assumed that the peripheral which is selected via this pin resides on the X-Bus.) **During Reset:** High **After Reset:** High **During POS:** High
RCIN#	I	**RESET CPU.** This signal from the keyboard controller is used to generate an INIT signal to the CPU.
RTCALE/	O	**REAL TIME CLOCK ADDRESS LATCH ENABLE.** RTCALE is used to latch theappropriate memory address into the RTC. A write to port 70h with the appropriate RTC memory address that will be written to or read from causes RTCALE to be asserted. RTCALE is asserted on falling IOW# and remains asserted for two SYSCLKs. If the internal Real Time Clock is used, this signal can be programmed as a general purpose output. **During Reset:** Low **After Reset:** Low **During POS:** Low/GPO
RTCCS#/ GPO24	O	**REAL TIME CLOCK CHIP SELECT.** RTCCS# is asserted during read or write I/O accesses to RTC location 71h. RTCCS# can be tied to a pair of external OR gates to generate the real time clock read and write command signals. If the internal Real Time Clock is used, this signal can be programmed as a general purpose output. **During Reset:** High **After Reset:** High **During POS:** High/GPO
XDIR#/ GPO22	O	**X-BUS TRANSCEIVER DIRECTION.** XDIR# is tied directly to the direction control of a 74?45 that buffers the X-Bus data, XD[7:0]. XDIR# is asserted (driven low) for all I/O read cycles regardless if the accesses is to a PIIX4 supported device. XDIR# is asserted for memory cycles only if BIOS or APIC space has been decoded. For PCI master initiated read cycles, XDIR# is asserted from the falling edge of either IOR# or MEMR# (from MEMR# only if BIOS or APIC space has been decoded), depending on the cycle type. For ISA master-initiated read cycles, XDIR# is asserted from the falling edge of either IOR# or MEMR# (from MEMR# only if BIOS space has been decoded), depending on the cycle type. When the rising edge of IOR# or MEMR# occurs, PIIX4 negates XDIR#. For DMA read cycles from the X-Bus, XDIR# is driven low from DACKx# falling and negated from DACKx# rising. At all other times, XDIR# is negated high. If the X-Bus not used, then this signal can be programmed to be a general purpose output. **During Reset:** High **After Reset:** High **During POS:** High/GPO

3.3 Intel 82371MB PCI to ISA/IDE Xcelerator (PIIX4M)-6

3.3.3. X-BUS INTERFACE(Sheet 3 of3)

Name	Type	Description
XOE#/ GPO23	O	**X-BUS TRANSCEIVER OUTPUT ENABLE.** XOE# is tied directly to the output enable of a 74?45 that buffers the X-Bus data, XD[7:0], from the system data bus, SD[7:0]. XOE# is asserted anytime a PIIX4 supported X-Bus device is decoded, and the devices decode is enabled in the X-Bus Chip Select Enable Register (BIOSCS#, KBCCS#, RTCCS#, MCCS#) or the Device Resource B (PCCS0#) and Device Resource C (PCCS1#). XOE# is asserted from the falling edge of the ISA commands (IOR#, IOW#, MEMR#, or MEMW#) for PCI Master and ISA master-initiated cycles. XOE# is negated from the rising edge of the ISA command signals for PCI Master initiated cycles and the SA[16:0] and LA[23:17] address for ISA master-initiated cycles. XOE# is not generated during any access to an X-Bus peripheral in which its decode space has been disabled. If an X-Bus not used, then this signal can be programmed to be a general purpose output. **During Reset:** High **After Reset:** High **During POS:** High/GPO

3.3.4. DMA SIGNALS (Sheet 1 of 2)

Name	Type	Description
DACK[0,1,2,3]# DACK[55,66,7]#	O	**DMA ACKNOWLEDGE.** The DACK# output lines indicate that a request for DMA service has been granted by PIIX4 or that a 16-bit master has been granted the bus. The active level (high or low) is programmed via the DMA Command Register. These lines should be used to decode the DMA slave device with the IOR# or IOW# line to indicate selection. If used to signal acceptance of a bus master request, this signal indicates when it is legal to assert MASTER#. If the DREQ goes inactive prior to DACK# being asserted, the DACK# signal will not be asserted. **During Reset:** High **After Reset:** High **During POS:** High
DREQ[0,1,2,3] DREQ[5,6,7]	I	**DMA REQUEST.** The DREQ lines are used to request DMA service from PIIX4 DMA controller or for a 16-bit master to gain control of the ISA expansion bus. The active level (high or low) is programmed via the DMA Command Register. All inactive to active edges of DREQ are assumed to be asynchronous. The request must remain active until the appropriate DACKx# signal is asserted.
REQ[A:C]#/ GPI[2:4]	I	**PC/PCI DMA REQUEST.** These signals are the DMA requests for PC/PCI protocol. They are used by a PCI agent to request DMA services and follow the PCI Expansion Channel Passing protocol as defined in the *PCI DMA* section. If the PC/PCI request is not needed, these pins can be used as general-purpose inputs.

3.3.4. DMA SIGNALS (Sheet 2 of 2)

Name	Type	Description
GNT[A:C]#/ GPO[9:11]	O	**PC/PCI DMA ACKNOWLEDGE.** These signals are the DMA grants for PC/PCI protocol. They are used by a PIIX4 to acknowledge DMA services and follow the PCI Expansion Channel Passing protocol as defined in the *PCI DMA* section. If the PC/PCI request is not needed, these pins can be used as general-purpose outputs. **During Reset:** High **After Reset:** High **During POS:** High/GPO
TC	O	**TERMINAL COUNT.** PIIX4 asserts TC to DMA slaves as a terminal count indicator. PIIX4 asserts TC after a new address has been output, if the byte count expires with that transfer. TC remains asserted until AEN is negated, unless AEN is negated during an autoinitialization TC is negated before AEN is negated during an autoinitialization. **During Reset:** Low **After Reset:** Low **During POS:** Low

3.3.5. INTERRUPT CONTROLLER/APIC SIGNALS (Sheet 1 of 3)

Name	Type	Description
APICACK#/ GPO12	O	**APIC ACKNOWLEDGE.** This active low output signal is asserted by PIIX4 after its internal buffers are flushed in response to the APICREQ# signal. When the I/O APIC samples this signal asserted it knows that PIIX4 buffers are flushed and that it can proceed to send the APIC interrupt. The APICACK# output is synchronous to PCICLK. If the external APIC is not used, then this is a general-purpose output. **During Reset:** High **After Reset:** High **During POS:** High/GPO
APICCS#/ GPO13	O	**APIC CHIP SELECT.** This active low output signal is asserted when the APIC Chip Select is enabled and a PCI originated cycle is positively decoded within the programmed I/O APIC address space. If the external APIC is not used, this pin is a general-purpose output. **During Reset:** High **After Reset:** High **During POS:** High/GPO
APICREQ#/ GPI5	I	**APIC REQUEST.** This active low input signal is asserted by an external APIC device prior to sending an interrupt over the APIC serial bus. When PIIX4 samples this pin active it will flush its F-type DMA buffers pointing towards PCI. Once the buffers are flushed, PIIX4 asserts APICACK# which indicates to the external APIC that it can proceed to send the APIC interrupt. The APICREQ# input must be synchronous to PCICLK. If the external APIC is not used, this pin is a general-purpose input.
INTR	OD	**INTERRUPT.** See CPU Interface Signals.

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3.3.5. INTERRUPT CONTROLLER/APIC SIGNALS (Sheet 2 of 3)

Name	Type	Description
IRQ0/ GPO14	O	**INTERRUPT REQUEST 0.** This output reflects the state of the internal IRQ0 signal from the system timer. If the external APIC is not used, this pin is a general-purpose output. **During Reset:** Low **After Reset:** Low **During POS:** IRQ0/GPO
IRQ1	I	**INTERRUPT REQUEST 1.** IRQ1 is always edge triggered and can not be modified by software to level sensitive. A low to high transition on IRQ1 is latched by PIIX4. IRQ1 must remain asserted until after the interrupt is acknowledged. If the input goes inactive before this time, a default IRQ7 is reported in response to the interrupt acknowledge cycle.
IRQ 3:7, 9:11, 14:15	I	**INTERRUPT REQUESTS 3:7, 9:11, 14:15.** The IRQ signals provide both system board components and ISA Bus I/O devices with a mechanism for asynchronously interrupting the CPU. These interrupts may be programmed for either an edge sensitive or a high level sensitive assertion mode. Edge sensitive is the default configuration. An active IRQ input must remain asserted until after the interrupt is acknowledged. If the input goes inactive before this time, a default IRQ7 is reported in response to the interrupt acknowledge cycle.
IRQ8#/ GPI6	I/O	**RQ 8#.** IRQ8# is always an active low edge triggered interrupt and can not be modified by software. IRQ8# must remain asserted until after the interrupt is acknowledged. If the input goes inactive before this time, a default IRQ7 is reported in response to the interrupt acknowledge cycle. If using the internal RTC, then this can be programmed as a general-purpose input. If enabling an APIC, this signal becomes an output and must not be programmed as a general purpose input.
IRQ9OUT#/ GPO29	O	**IRQ9OUT#.** IRQ9OUT# is used to route the internally generated SCI and SMBus interrupts out of the PIIX4 for connection to an external IO APIC. If APIC is disabled, this signal pin is a General Purpose Output. **During Reset:** High **After Reset:** High **During POS:** IRQ9OUT#/GPO
PIRQ[A:D]#	I/OD PCI	**PROGRAMMABLE INTERRUPT REQUEST.** The PIRQx# signals are active low, level sensitive, shareable interrupt inputs. They can be individually steered to ISA interrupts IRQ [3:7,9:12,14:15]. The USB controller uses PIRQD# as its outputsignal.

3.3.5. INTERRUPT CONTROLLER/APIC SIGNALS (Sheet 3 of 3)

Name	Type	Description
IRQ 12/M	I	**INTERRUPT REQUEST 12.** In addition to providing the standard interrupt function as described in the pin description for IRQ[3:7,9:11,14:15], this pin can also be programmed to provide the mouse interrupt function. When the mouse interrupt function is selected, a low to high transition on this signal is latched by PIIX4 and an INTR is generated to the CPU as IRQ12. An internal IRQ12 interrupt continues to be generated until a Reset or an I/O read access to address 60h (falling edge of IOR#) is detected.
SERIRQ/ GPI7	I/O	**SERIAL INTERRUPT REQUEST.** Serial interrupt input decoder, typically used in conjunction with the Distributed DMA protocol. If not using serial interrupts, this pin can be used as a general-purpose input.

3.3.6. CPU INTERFACE SIGNALS (Sheet 1 of 3)

Name	Type	Description
A20M#	OD	**ADDRESS 20 MASK.** PIIX4 asserts A20M# to the CPU based on combination of Port 92 Register, bit 1 (FAST_A20), and A20GATE input signal. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
CPURST	OD	**PU RESET.** PIIX4 asserts CPURST to reset the CPU. PIIX4 asserts CPURST during power-up and when a hard reset sequence is initiated through the RC register. CPURST is driven inactive a minimum of 2 ms after PWROK is driven active. CPURST is driven active for a minimum of 2 ms when initiated through the RC register. The inactive edge of CPURST is driven synchronously to the rising edge of PCICLK. If a hard reset is initiated through the RC register, PIIX4 resets its internal registers (in both core and suspend wells) to their default state. This signal is active high for Pentium processor and active-low for Pentium II processor as determined by CONFIG1 signal. For values **During Reset**, **After Reset**, and **During POS**, see the *Suspend/Resume and Resume Control Signaling* section.

3.3 Intel 82371MB PCI to ISA/IDE Xcelerator (PIIX4M)-8

3.3.6. CPU INTERFACE SIGNALS (Sheet 2 of 3)

Name	Type	Description
FERR#	I	**NUMERIC COPROCESSOR ERROR.** This pin functions as a FERR# signal supporting coprocessor errors. This signal is tied to the coprocessor error signal on the CPU. If FERR# is asserted, PIIX4 generates an internal IRQ13 to its interrupt controller unit. PIIX4 then asserts the INT output to the CPU. FERR# is also used to gate the IGNNE# signal to ensure that IGNNE# is not asserted to the CPU unless FERR# is active.
IGNNE#	OD	**IGNORE NUMERIC EXCEPTION.** This signal is connected to the ignore numeric exception pin on the CPU. IGNNE# is only used if the PIIX4 coprocessor error reporting function is enabled. If FERR# is active, indicating a coprocessor error, a write to the Coprocessor Error Register (F0h) causes the IGNNE# to be asserted. IGNNE# remains asserted until FERR# is negated. If FERR# is not asserted when the Coprocessor Error Register is written, the IGNNE# signal is not asserted. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
INIT	OD	**INITIALIZATION.** INIT is asserted in response to any one of the following conditions. When the System Reset bit in the Reset Control Register is reset to 0 and the Reset CPU bit toggles from 0 to 1, PIIX4 initiates a soft reset by asserting INIT. PIIX4 also asserts INIT if a Shut Down Special cycle is decoded on the PCI Bus, if the RCIN# signal is asserted, or if a write occurs to Port 92h, bit 0. When asserted, INIT remains asserted for approximately 64 PCI clocks before being negated. This signal is active high for Pentium processor and active-low for Pentium II processor as determined by CONFIG1 signal. **Pentium Processor:** **During Reset:** Low **After Reset:** Low **During POS:** Low **Pentium II Processor:** **During Reset:** High **After Reset:** High **During POS:** High
INTR	OD	**CPU INTERRUPT.** INTR is driven by PIIX4 to signal the CPU that an interrupt request is pending and needs to be serviced. It is asynchronous with respect to SYSCLK or PCICLK and is always an output. The interrupt controller must be programmed following PCIRST# to ensure that INTR is at a known state. **During Reset:** Low **After Reset:** Low **During POS:** Low

3.3.6. CPU INTERFACE SIGNALS (Sheet 3 of 3)

Name	Type	Description
NMI	OD	**NON-MASKABLE INTERRUPT.** NMI is used to force a nonmaskable interrupt to the CPU. PIIX4 generates an NMI when either SERR# or IOCHK# is asserted, depending on how the NMI S tatus and Control Register is programmed. The CPU detects an NMI when it detects a rising edge on NMI. After the NMI interrupt routine processes the interrupt, the NMI status bits in the NMI Status and Control Register are cleared by software. The NMI interrupt routine must read this register to determine the source of the interrupt. The NMI is reset by setting the corresponding NMI source enable/disable bit in the NMI Status and Control Register. To enable NMI interrupts, the two NMI enable/disable bits in the register must be set to 0, and the NMI mask bit in the NMI Enable/Disable and Real Time Clock Address Register must be set to 0. Upon PCIRST#, this signal is driven low. **During Reset:** Low **After Reset:** Low **During POS:** Low
SLP#	OD	**SLEEP.** This signal is output to the Pentium II processor in order to put it into Sleep state. For Pentium processor it is a No Connect. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
SMI#	OD	**SYSTEM MANAGEMENT INTERRUPT.** SMI# is an active low synchronous output that is asserted by PIIX4 in response to one of many enabled hardware or software events. The CPU recognizes the falling edge of SMI# as the highest priority interrupt in the system, with the exception of INIT, CPURST, and FLUSH. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
STPCLK#	OD	**STOP CLOCK.** STPCLK# is an active low synchronous output that is asserted by PIIX4 in response to one of many hardware or software events. STPCLK# connects directly to the CPU and is synchronous to PCICLK. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z

3.3.7. CLOCKING SIGNALS (Sheet 1 of 2)

Name	Type	Description
CLK48	I	**48-MHZ CLOCK.** 48-MHz clock used by the internal USB host controller. This signal may be stopped during suspend modes.
OSC	I	**14.31818-MHZ CLOCK.** Clock signal used by the internal 8254 timer. This clock signal may be stopped during suspend modes.

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3.3.7. CLOCKING SIGNALS (Sheet 2 of 2)

Name	Type	Description
PCICLK	I	**FREE-RUNNING PCI CLOCK.** A clock signal running at 30 or 33 MHz, PCICLK provides timing for all transactions on the PCI Bus. All other PCI signals are sampled on the rising edge of PCICLK, and all timing parameters are defined with respect to this edge. Because many of the circuits in PIIX4 run off the PCI clock, this signal MUST be kept active, even if the PCI bus clock is not active.
RTCX1, RTCX2	I/O	**RTC CRYSTAL INPUTS:** These connected directly to a 32.768-kHz crystal. External capacitors are required. These clock inputs are required even if the internal RTC is not being used.
SUSCLK	O	**SUSPEND CLOCK.** 32.768-kHz output clock provided to the Host-to-PCI bridge used for maintenance of DRAM refresh. This signal is stopped during Suspend-to-Disk and Soft Off modes. For values During Reset, After Reset, and During POS, see the *Suspend/Resume and Resume Control Signaling* section.
SYSCLK	O	**ISA SYSTEM CLOCK.** SYSCLK is the reference clock for the ISA bus. It drives the ISA bus directly. The SYSCLK is generated by dividing PCICLK by 4. The SYSCLK frequencies supported are 7.5 MHz and 8.33 MHz. For PCI accesses to the ISA bus, SYSCLK may be stretched low to synchronize BALE falling to the rising edge of SYSCLK. **During Reset:** Running **After Reset:** Running **During POS:** Low

3.3.8. IDE SIGNALS (Sheet 1 of 6)

Name	Type	Description
PDA[2:0]	O	**PRIMARY DISK ADDRESS[2:0].** These signals indicate which byte in either the ATA command block or control block is being addressed. If the IDE signals are configured for Primary and Secondary, these signals are connected to the corresponding signals on the Primary IDE connector. If the IDE signals are configured for Primary 0 and Primary 1, these signals are used for the Primary 0 connector. **During Reset:** High-Z **After Reset:** Undefined[1] **During POS:** PDA

3.3.8. IDE SIGNALS (Sheet 2 of 6)

Name	Type	Description
PDCS1#	O	**PRIMARY DISK CHIP SELECT FOR 1F0H– –1F7H RANGE.** For ATA command register block. If the IDE signals are configured for Primary and Secondary, this output signal is connected to the corresponding signal on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector. **During Reset:** High **After Reset:** High **During POS:** High
PDCS3#	O	**PRIMARY DISK CHIP SELECT FOR 3F0– –3F7 RANGE.** For ATA control register block. If the IDE signals are configured for Primary and Secondary, this output signal is connected to the corresponding signal on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector. **During Reset:** High **After Reset:** High **During POS:** High
PDD[15:0]	I/O	**PRIMARY DISK DATA[15:0].** These signals are used to transfer data to or from the IDE device. If the IDE signals are configured for Primary and Secondary, these signals are connected to the corresponding signals on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector. **During Reset:** High-Z **After Reset:** Undefined[1] **During POS:** PDD
PDDACK#	O	**PRIMARY DMA ACKNOWLEDGE.** This signal directly drives the IDE device DMACK# signal. It is asserted by PIIX4 to indicate to IDE DMA slave devices that a given data transfer cycle (assertion of PDIOR# or PDIOW#) is a DMA data transfer cycle. This signal is used in conjunction with the PCI bus master IDE function. It is not associated with any AT compatible DMA channel. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector. **During Reset:** High **After Reset:** High **During POS:** High

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3.3.8. IDE SIGNALS (Sheet 3 of 6)

Name	Type	Description
PDDREQ	I	**PRIMARY DISK DMA REQUEST.** This input signal is directly driven from the IDE device DMARQ signal. It is asserted by the IDE device to request a data transfer, and used in conjunction with the PCI bus master IDE function. It is not associated with any AT compatible DMA channel. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector.
PDIOR#	O	**PRIMARY DISK IO READ.** In normal IDE this is the command to the IDE device that it may drive data onto the PDD[15:0] lines. Data is latched by PIIX4 on the negation edge of PDIOR#. The IDE device is selected either by the ATA register file chip selects (PDCS1#, PDCS3#) and the PDA[2:0] lines, or the IDE DMA slave arbitration signals (PDDACK#). In an Ultra DMA/33 read cycle, this signal is used as DMARDY# which is negated by the PIIX4 to pause Ultra DMA/33 transfers. In an Ultra DMA/33 write cycle, this signal is used as the STROBE signal, with the drive latching data on rising and falling edges of STROBE. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector. **During Reset:** High **After Reset:** High **During POS:** High
PDIOW#	O	**PRIMARY DISK IO WRITE.** In normal IDE mode, this is the command to the IDE device that it may latch data from the PDD[15:0] lines. Data I s latched by the IDE device on the negation edge of PDIOW#. The IDE device is selected either by the ATA register file chip selects (PDCS1#, PDCS3#) and the PDA[2:0] lines, or the IDE DMA slave arbitration signals (PDDACK#). For Ultra DMA/33 mode, this signal is used as the STOP signal, which is used to terminate an Ultra DMA/33 transaction. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector. **During Reset:** High **After Reset:** High **During POS:** High-Z

3.3.8. IDE SIGNALS (Sheet 4 of 6)

Name	Type	Description
PIORDY	I	**PRIMARY IO CHANNEL READY.** In normal IDE mode, this input signal is directly driven by the corresponding IDE device IORDY signal. In an Ultra DMA/33 read cycle, this signal is used as STROBE, with the PIIX4 latching data on rising and falling edges of STROBE. In an Ultra DMA/33 write cycle, this signal is used as the DMARDY# signal which is negated by the drive to pause Ultra DMA/33 transfers. If the IDE signals are configured for Primary and Secondary, this signal s connected to the corresponding signal on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector. This is a Schmitt triggered input.
SDA[2:0]	O	**SECONDARY DISK ADDRESS[2:0].** These signals indicate which byte in either the ATA command block or control block is being addressed. If the IDE signals are configured for Primary and Secondary, these signals are connected to the corresponding signals on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector. **During Reset:** High-Z **After Reset:** Undefined [1]**During POS:** SDA
SDCS1#	O	**SECONDARY CHIP SELECT FOR 170H– –177H RANGE.** For ATA command register block. If the IDE signals are configured for Primary and Secondary, this output signal is connected to the corresponding signal on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector. **During Reset:** High **After Reset:** High **During POS:** High
SDCS3#	O	**SECONDARY CHIP SELECT FOR 370H– –377H RANGE.** For ATA control register block. If the IDE signals are configured for Primary and Secondary, this output signal is connected to the corresponding signal on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector. **During Reset:** High **After Reset:** High **During POS:** High-Z

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3.3.8. IDE SIGNALS (Sheet 5 of 6)

Name	Type	Description
SDD[15:0]	I/O	**SECONDARY DISK DATA[15:0].** These signals are used to transfer data to or from the IDE device. If the IDE signals are configured for Primary and Secondary, these signals are connected to the corresponding signals on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signalsare used for the Primary Slave connector. **During Reset:** High-Z **After Reset:** Undefined[1] **During POS:** SDD
SDDACK#	O	**SECONDARY DMA ACKNOWLEDGE.** This signal directly drives the IDE device DMACK# signal. It is asserted by PIIX4 to indicate to IDE DMA slave devices that a given data transfer cycle (assertion of SDIOR# or SDIOW#) is a DMA data transfer cycle. This signal is used in conjunction with the PCI bus master IDE function. It is not associated with any AT compatible DMA channel. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector. **During Reset:** High **After Reset:** High **During POS:** High
SDDREQ	I	**SECONDARY DISK DMA REQUEST.** This input signal is directly driven from the IDE device DMARQ signal. It is asserted by the IDE device to request a data transfer, and used in conjunction with the PCI bus master IDE function. It is not associated with any AT compatible DMA channel. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector.
SIORDY	I	**SECONDARY IO CHANNEL READY.** In normal IDE mode, this input signal is directly driven by the corresponding IDE device IORDY signal. In an Ultra DMA/33 read cycle, this signal is used as STROBE, with the PIIX4 latching data on rising and falling edges of STROBE. In an Ultra DMA write cycle, this signal is used as the DMARDY# signal which is negated by the drive to pause Ultra DMA/33 transfers. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector. This is a Schmitt triggered input.

3.3.8. IDE SIGNALS (Sheet 6 of 6)

Name	Type	Description
SDIOR#	O	**SECONDARY DISK IO READ.** In normal IDE mode, this is the command to the IDE device that it may drive data onto the SDD[15:0] lines. Data is latched by the PIIX4 on the negation edge of SDIOR#. The IDE device is selected either by the ATA register file chip selects (SDCS1#, SDCS3#) and the SDA[2:0] lines, or the IDE DMA slave arbitration signals (SDDACK#). In an Ultra DMA/33 read cycle, this signal is used as DMARDY# which is negated by the PIIX4 to pause Ultra DMA/33 transfers. In an Ultra DMA/33 write cycle, this signal is used as the STROBE signal, with the drive latching data on rising and falling edges of STROBE. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector. **During Reset:** High **After Reset:** High **During POS:** High
SDIOW#	O	**SECONDARY DISK IO WRITE.** In normal IDE mode, this is the command to the IDE device that it may latch data from the SDD[15:0] lines. Data is latched by the IDE device on the negation edge of SDIOW#. The IDE device is selected either by the ATA register file chip selects (SDCS1#, SDCS3#) and the SDA[2:0] lines, or the IDE DMA slave arbitration signals (SDDACK#). In read and write cycles this signal is used as the STOP signal, which is used to terminate an Ultra DMA/33 transaction. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector. **During Reset:** High **After Reset:** High **During POS:** High

NOTES:

1. After reset, all undefined signals on the primary channel will default to the same values as the undefined signals on the secondary channel.

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3.3.9. UNIVERSAL SERIAL BUS SIGNALS

Name	Type	Description
OC[1:0]#	I	**OVER CURRENT DETECT.** These signals are used to monitor the status of the USB power supply lines. The corresponding USB port is disabled when its over current signal is asserted.
USBP0+, USBP0	I/O	**SERIAL BUS PORT 0.** This signal pair comprises the differential data signal for USB port 0. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
USBP1+, USBP1	I/O	**SERIAL BUS PORT 1.** This signal pair comprises the differential data signal for USB port 1. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z

3.3.10. POWER MANAGEMENT SIGNALS (Sheet 1 of 4)

Name	Type	Description
BATLOW#/ GPI9	I	**BATTERY LOW.** Indicates that battery power is low. PIIX4 can be programmed to prevent a resume operation when the BATLOW# signal is asserted. If the Battery Low function is not needed, this pin can be used as a general-purposeinput.
CPU_STP#/ GPO17	O	**CPU CLOCK STOP.** Active low control signal to the clock generator used to disable the CPU clock outputs. If this function is not needed, then this signal can be used asa general-purpose output. For values **During Reset**, **After Reset**, and **During POS**, see the *Suspend/Resume and Resume Control Signaling* section.
EXTSMI#	I/OD	**EXTERNAL SYSTEM MANAGEMENT INTERRUPT.** EXTSMI# is a falling edge triggered input to PIIX4 indicating that an external device is requesting the system to enter SMM mode. When enabled, a falling edge on EXTSMI# results in the assertion of the SMI# signal to the CPU. EXTSMI# is an asynchronous input to PIIX4. However, when the setup and hold times are met, it is only required to be asserted for one PCICLK. Once negated EXTSMI# must remain negated for at least four PCICLKs to allow the edge detect logic to reset. EXTSMI# is asserted by PIIX4 in response to SMI# being activated within the Serial IRQ function. An external pull-up should be placed on this signal.

3.3.10. POWER MANAGEMENT SIGNALS (Sheet 2 of 4)

Name	Type	Description
LID/ GPI10	I	**LID INPUT.** This signal can be used to monitor the opening and closing of the display lid of a notebook computer. It can be used to detect both low to high transition or a high to low transition and these transitions will generate an SMI# if enabled. This input contains logic to perform a 16-ms debounce of the input signal. If the LID function is not needed, this pin can be used as a general-purpose input.
PCIREQ [A:D]#	I	**PCI REQUEST.** Power Management input signals used to monitor PCI Master Requests for use of the PCI bus. They are connected to the corresponding REQ[0:3]# signals on the Host Bridge.
PCI_STP#/ GPO18	O	**PCI CLOCK STOP.** Active low control signal to the clock generator used to disable the PCI clock outputs. The PIIX4 free running PCICLK input must remain on. If this function is not needed, this pin can be used as a general-purpose output. For values **During Reset**, **After Reset**, and **During POS**, see the *Suspend/Resume and Resume Control Signaling* section.
PWRBTN#	I	**POWER BUTTON.** Input used by power management logic to monitor external system events, most typically a system on/off button or switch. This input contains logic to perform a 16-ms debounce of the input signal.
RI# GPI12	I	**RING INDICATE.** Input used by power management logic to monitor external system events, most typically used for wake up from a modem. If this function is not needed, then this signal can be individually used as a general-purpose input.
RSMRST#	I	**RESUME RESET.** This signal resets the internal Suspend Well power plane logic and portions of the RTC well logic.
SMBALERT#/ GPI11	I	**SM BUS ALERT.** Input used by System Management Bus logic to generate an interrupt (IRQ or SMI) or power management resume event when enabled. If this function is not needed, this pin can be used as a general-purpose input.
SMBCLK	I/O	**SM BUS CLOCK.** System Management Bus Clock used to synchronize transfer of data on SMBus. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
SMBDATA	I/O	**SM BUS DATA.** Serial data line used to transfer data on SMBus. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z

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3.3.10. POWER MANAGEMENT SIGNALS (Sheet 3 of 4)

Name	Type	Description
SUSA#	O	**SUSPEND PLANE A CONTROL.** Control signal asserted during power management suspend states. SUSA# is primarily used to control the primary power plane. This signal is asserted during POS, STR, and STD suspend states. **During Reset:** Low **After Reset:** High **During POS:** Low
SUSB#/ GPO15	O	**SUSPEND PLANE B CONTROL.** Control signal asserted during power management suspend states. SUSB# is primarily used to control the secondary power plane. This signal is asserted during STR and STD suspend states. If the power plane control is not needed, this pin can be used as a general-purpose output. **During Reset:** Low **After Reset:** High **During POS:** High/GPO
SUSC#/ GPO16	O	**SUSPEND PLANE C CONTROL.** Control signal asserted during power management suspend states, primarily used to control the tertiary power plane. It is asserted only during STD suspend state. If the power plane control is not needed, this pin can be used as a general-purpose output. **During Reset:** Low **After Reset:** High **During POS:** High/GPO
SUS_STAT1#/ GPO20	O	**SUSPEND STATUS 1.** This signal is typically connected to the Host-to-PCI bridge and is used to provide information on host clock status. SUS_STAST1# is asserted when the system may stop the host clock, such as Stop Clock or during POS, STR, and STD suspend states. If this function is not needed, this pin can be used as a general-purpose output. **During Reset:** Low **After Reset:** High **During POS:** Low/GPO
SUS_STAT2#/ GPO21	O	**SUSPEND STATUS 2.** This signal will typically connect to other system peripherals and is used to provide information on system suspend state. It is asserted during POS, STR, and STD suspend states. If this function is not needed, this pin can be used as a general-purpose output. **During Reset:** Low **After Reset:** High **During POS:** Low/GPO
THRM#/ GPI8	I	**THERMAL DETECT.** Active low signal generated by external hardware to start the Hardware Clock Throttling mode. If enabled, the external hardw are can force the system to enter into Hardware Clock Throttle mode by asserting THRM#. This causes PIIX4 to cycle STPCLK# at a preset programmable rate. If this function is not needed, this pin can be used as a general-purpose input.

3.3.10. POWER MANAGEMENT SIGNALS (Sheet 4 of 4)

Name	Type	Description
ZZ/ GPO19	O	**LOW-POWER MODE FOR L2 CACHE SRAM.** This signal is used to power down a cache data SRAMs when the clock logic places the CPU into the Stop Clock. If this function is not needed, this pin can be used as a general-purpose output. **During Reset:** Low **After Reset:** Low **During POS:** Low

3.3.11. GENERAL PURPOSE INPUT AND OUTPUT SIGNALS

Some of the General Purpose Input and Output signals are multiplexed with other PIIX4 signals. The usage is determined by the system configuration.
The default pin usage is shown in Table 1 and Table 2. The configuration can be selected via the General Configuration register and X-Bus Chip Select register.

Name	Type	Description
GPI[21:0]	I	**GENERAL PURPOSE INPUTS.** These input signals can be monitored via the GPIREG register located in Function 3 (Power Management) System IO Space at address PMBase+30h. See Table 1 for details.
GPO[30:0]	O	**GENERAL PURPOSE OUTPUTS.** These output signals can be controlled via the GPIREG register located in Function 3 (Power Management) System IO Space at address PMBase+34h. If a GPO pin is not multiplexed with another signal or defaults to GPO, then its state after reset is the reset condition of the GPOREG register. If the GPO defaults to another signal, then it defaults to that signal state after reset. The GPO pins that default to GPO remain stable after reset. The others may toggle due to system boot or power control sequencing after reset prior to their being programmed as GPOs. The GPO8 signal is driven low upon removal of power from the PIIX4 core power plane. All other GPO signals are invalid (buffers powered off).

3.3 Intel 82371MB PCI to ISA/IDE Xcelerator (PIIX4M)-14

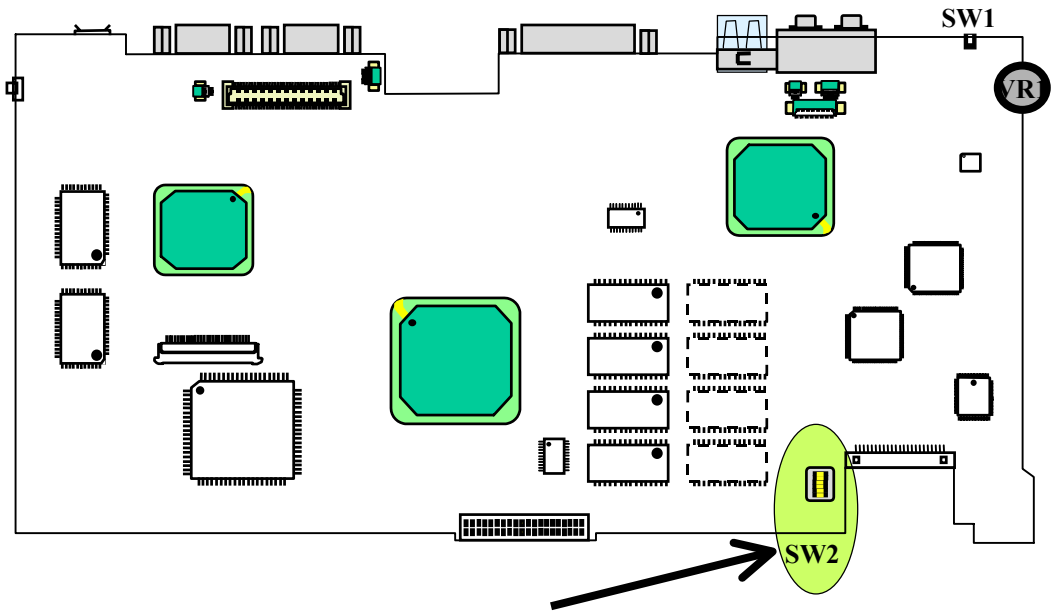
3.3.12. OTHER SYSTEM AND TEST SIGNALS

Name	Type	Description
CONFIG1	I	**CONFIGURATION SELECT 1.** This input signal is used to select the type of microprocessor being used in the system. If CONFIG1=0, the system contains a Pentium microprocessor. If CONFIG1=1, the system contains a Pentium II microprocessor. It is used to control the polarity of INIT and CPURST signals.
CONFIG2	I	**CONFIGURATION SELECT 2.** This input signal is used to select the positive or subtractive decode of FFFF0000h-FFFFFFFh memory address range (top 64 Kbytes). If CONFIG[2]=0, the PIIX4 will positively decode this range. If CONFIG[2]=1, the PIIX4 will decode this range with sub tractive decode timings only. The input value of this pin must be static and may not dynamically change during system operations.
PWROK	I	**POWER OK.** When asserted, PWROK is an indication to PIIX4 that power and PCICLK have been stable for at least 1 ms. PWROK can be driven asynchronously. When PWROK is negated, PIIX4 asserts CPURST, PCIRST# and RSTDRV. When PWROK is driven active (high), PIIX4 negates CPURST, PCIRST#, and RSTDRV.
SPKR	O	**SPEAKER.** The SPKR signal is the output of counter timer 2 and is internally " ANDed with Port 061h bit 1 to provide the Speaker Data Enable. This signal drives an external speaker driver device, which in turn drives the ISA system speaker. **During Reset:** Low **After Reset:** Low **During POS:** Last State
TEST#	I	**TEST MODE SELECT.** The test signal is used to select various test modes of PIIX4. This signal must be pulled up to VCC(SUS) for normal operation.

3.3.13. POWER AND GROUND PINS

Name	Type	Description
VCC	V	**CORE VOLTAGE SUPPLY.** These pins are the primary voltage supply for the PIIX4core and IO periphery and must be tied to 3.3V.
VCC (RTC)	V	**RTC WELL VOLTAGE SUPPLY.** This pin is the supply voltage for the RTC logic and must be tied to 3.3V.
VCC (SUS)	V	**SUSPEND WELL VOLTAGE SUPPLY.** These pins are the primary voltage supply for the PIIX4 suspend logic and IO signals and must be tied to 3.3V.
VCC (USB)	V	**USB VOLTAGE SUPPLY.** This pin is the supply voltage for the USB input/output buffers and must be tied to 3.3V.
VREF	V	**VOLTAGE REFERENCE.** This pin is used to provide a 5V reference voltage for 5V safe input buffers. VREF must be tied to 5V in a system requiring 5V tolerance. In a 5V tolerant system, this signal must power up before or simultaneous to VCC. It must power down after or simultaneous to VCC. In a non-5V tolerant system (3.3V only), this signal can be tied directly to VCC. There are then no sequencing requirements.
VSS	V	**CORE GROUND.** These pins are the primary ground for PIIX4.
VSS (USB)	V	**USB GROUND.** This pin is the ground for the USB input/output buffers.

4.Switch Setting



SW2- 4	Key-Board Type
on	Japaness KeyBoard
off	English KeyBoard

SW2 (LCD TYPE SETTING)

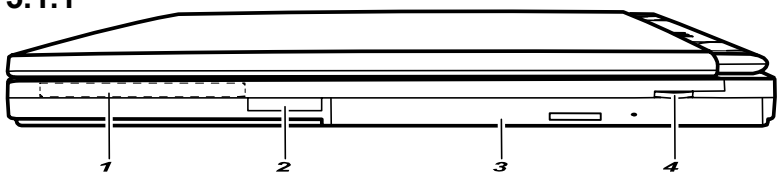
SW2-1	SW2-2	SW2-3	LCD - TYPE
on	on	on	13.3 HitachiTX34D61VC1HAD
off	on	on	12.1 Mitsubishi12.1 AA121SJ03
on	off	on	13.3 HyundaiHT13X14
off	off	on	12.1 Sanyo TM121SV-02L01
on	on	off	12.1 Sanyo TM121SV-02L03(LVDS)
off	on	off	12.1 Sanyo HPA LM-JK63-22NTR
on	off	off	12.1 Sharp LQ 12S1LH12
off	off	off	12.1 DSTN SR120522NTR

5.Assembly & Disassembly

5 System View and Disassembly

5.1 System View

5.1.1

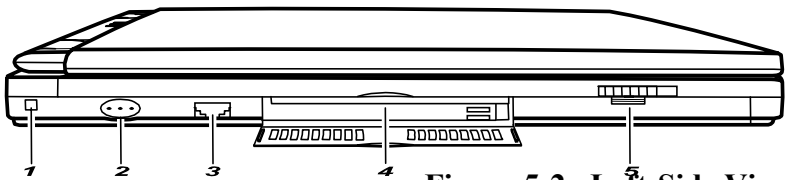


Right-Side View

1. Hard Disk Drive
2. IR Port
3. CD-ROM/DVD-ROM Drive
4. Volume Control

Figure 5-1. Right-Side View

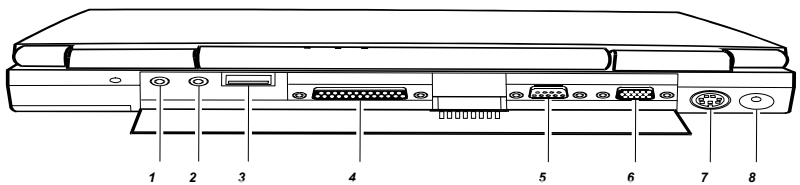
5.1.2 Left-Side View



1. Kensington Lock Anchor
2. Power Button
3. Phone Line Connector (optional)
4. PC Card Slots
5. Battery Pack

Figure 5-2. Left-Side View

5.1.3 Rear View

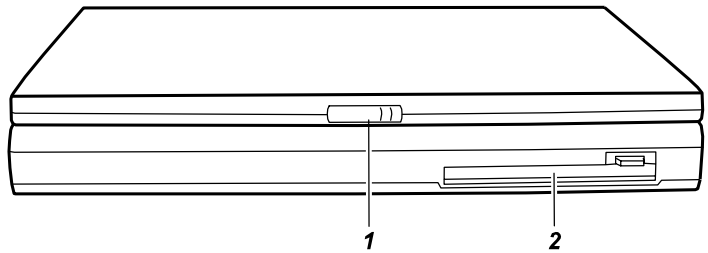


1. Microphone Connector
2. Audio Output Connector
3. USB Port
4. Parallel Port
5. Serial Port
6. VGA Port
7. PS/2 Mouse/Keyboard Port
8. Power Connector

Figure 5-3. Rear View

5.Assembly & Disassembly

5.1.4 Front View

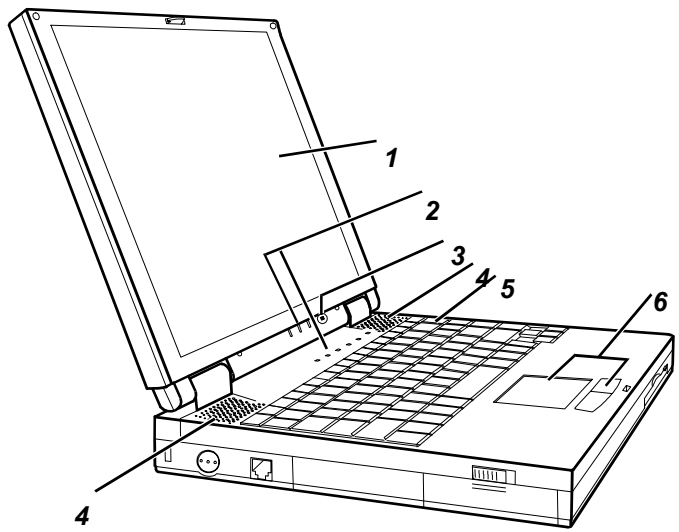


1. **Top Cover Latch**
2. **Floppy Disk Drive**

Figure 5-4. Front View

5.1.5 Top-Open View

To open the cover, press the cover latch toward the right and lift the cover.



1. **LCD Display**
2. **Indicators Panel**
3. **Microphone**
4. **Stereo Speaker Set**
5. **Keyboard**
6. **Touchpad**

Figure 5-5. Top-Open View

5.Assembly & Disassembly

5.2 System Disassembly

The section discusses at length each major component for disassembly/reassembly and show corresponding illustrations. Use the chart below to determine the disassembly sequence for removing components from the notebook.

- **Modular Components**
  - **5.2.1 Battery Pack**
  - **5.2.2 CD-ROM/DVD-ROM Drive**
  - **5.2.3 CPU**
  - **5.2.4 Fax/Modem/Voice Card**
  - **5.2.5 SO-DIMM**
- **LCD Assembly Components**
  - **5.2.6 LCD Assembly**
  - **5.2.7.1 12.1 Inch LCD Panel**
  - **5.2.7.2 13.3 Inch LCD Panel**
  - **5.2.8 Inverter Board/LED Board**
- **Base Unit Components**
  - **5.2.9 Keyboard**
  - **5.2.10 Hard Disk Drive**
  - **5.2.11 Touchpad Board**
  - **5.2.12 System Board**
  - **5.2.13 Floppy Disk Drive**

You can also find details of each component on the exploded charts.

5.Assembly & Disassembly

5.2.1 Battery Pack

Disassembly

1. Place the notebook upside down.
2. First push away the small locking latch (❶) on the battery pack and then slide the locking latch (❷) on the side of the notebook to unlock and lift (❸) the battery pack out of the compartment.

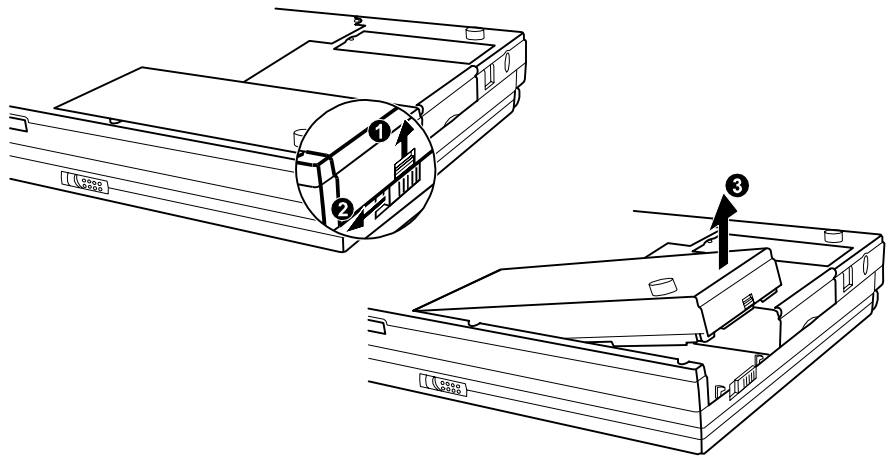


Figure 5-6. Removing the Battery Pack

Reassembly

1. Fit the battery pack into the compartment. Make sure the locking latch is in the locked position. (Refer to Figure 5-6 earlier.)

5.Assembly & Disassembly

5.2.2 CD-ROM/DVD-ROM Drive

Disassembly

1. Place the notebook upside down.
2. Open the CPU compartment cover by removing four screws and lifting up the cover from one side.

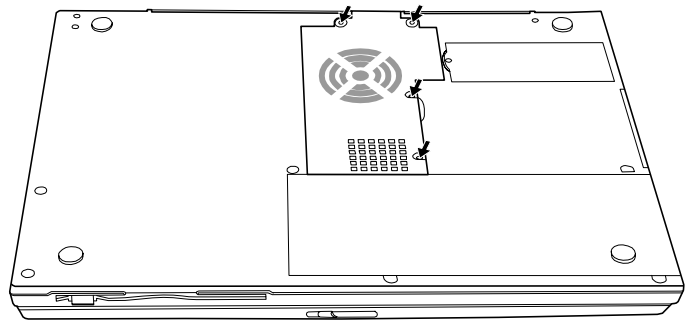


Figure 5-7. Removing the CPU Compartment Cover

3. Unplug the CD-ROM/DVD-ROM drive cable from the system board.

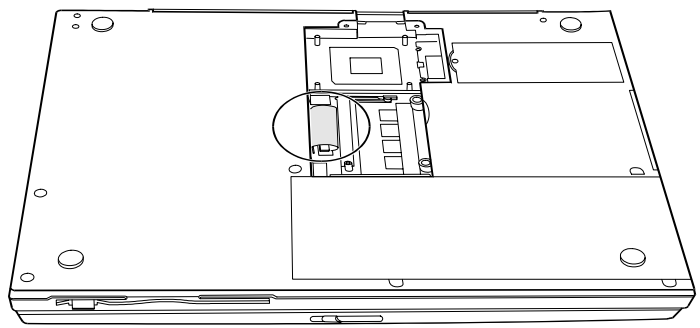


Figure 5-8. Unplugging the CD-ROM/DVD-ROM Drive Cable

5.Assembly & Disassembly

4. Remove one screw and slide the CD-ROM/DVD-ROM drive out of the compartment.

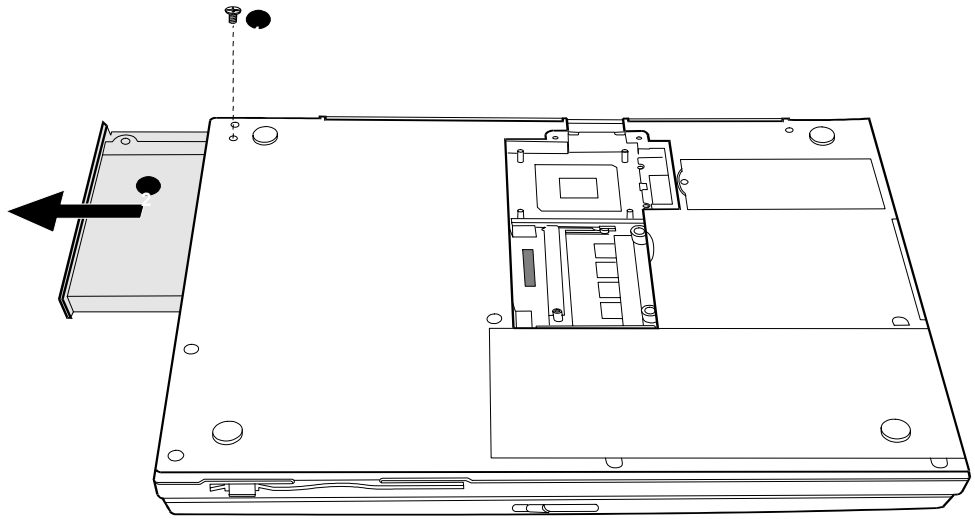


Figure 5-9. Removing the CD-ROM/DVD-ROM Drive

Reassembly

1. Connect one end of the cable to the CD-ROM/DVD-ROM drive.
2. Slide the CD-ROM/DVD-ROM drive into the compartment and secure with one screw. (Refer to Figure 5-9 earlier.)
3. Connect the CD-ROM/DVD-ROM drive cable to the system board. (Refer to Figure 5-8 earlier.)
4. Replace the CPU compartment cover and secure with four screws. (Refer to Figure 5-7 earlier.)

5.Assembly & Disassembly

5.2.3 CPU

Disassembly

1. Place the notebook upside down.
2. Open the CPU compartment cover by removing four screws and lifting up the cover from one side. (See Figure 5-7.)
3. Remove four screws that fasten the fan assembly. Remove the bottom screws (❶) first and then the upper screws (❷).

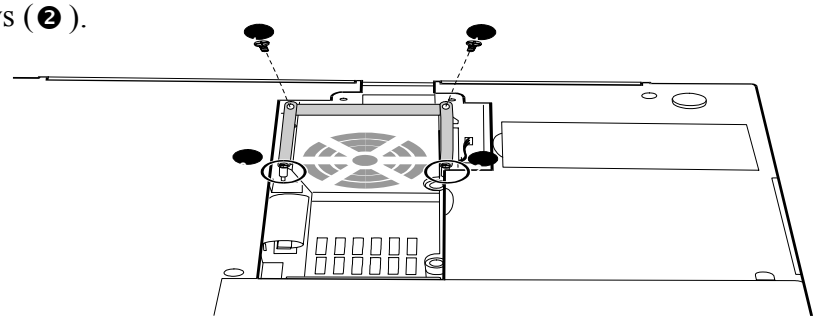


Figure 5-10. Removing the screws

4. Remove the metal plate. Unplug the power cord and remove the fan assembly.

NOTE: When you remove the fan assembly, make sure that the thermal pad is not damaged. If it is damaged, you have to use a new thermal pad.

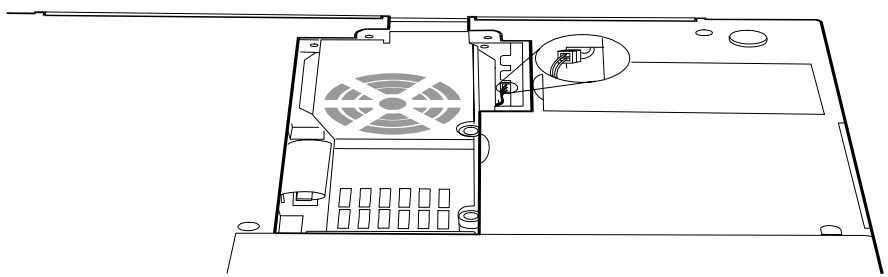


Figure 5-11. Removing the Fan Assembly

5.Assembly & Disassembly

5. Loosen the screw by a flat screwdriver, upraise the CPU socket to unlock the CPU.

   Note: The CPU socket may be different according to the model you purchased.

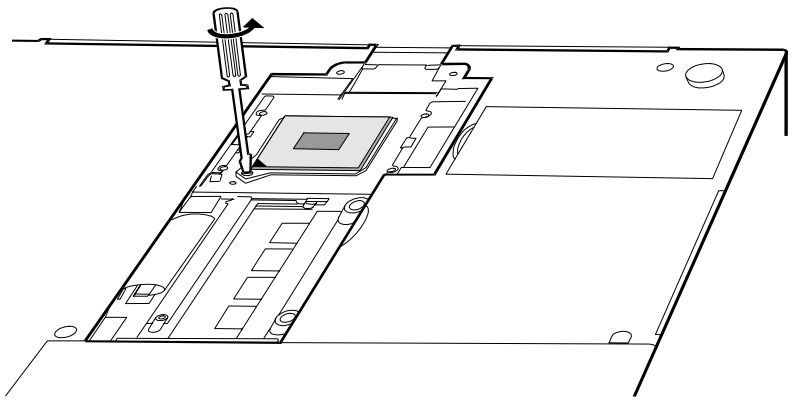


Figure 5-12. Unlocking the screw

6. Remove the CPU gently.

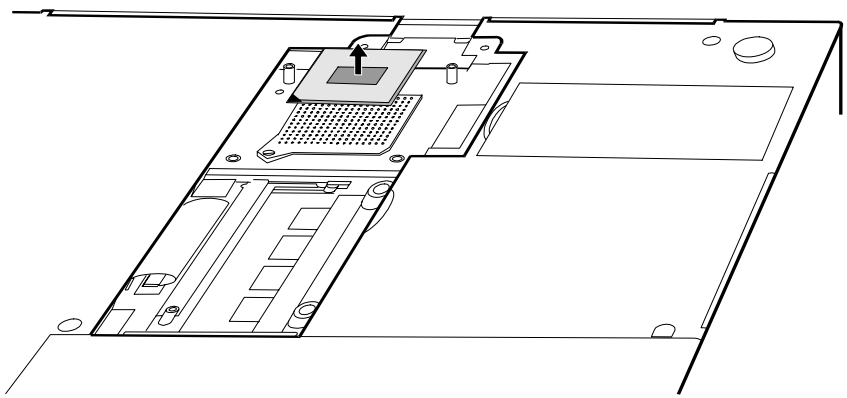


Figure 5-13. Removing the CPU

5.Assembly & Disassembly

Reassembly

1. Align the arrowhead of the uPGA CPU with the arrowhead of the socket and insert the CPU pins into the holes.

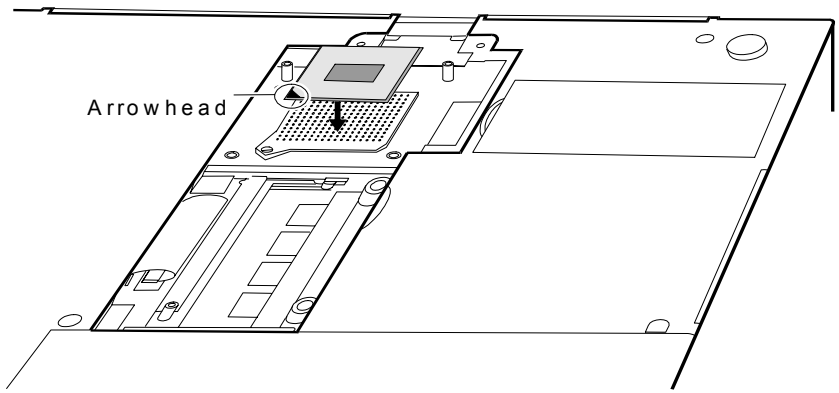


Figure 5-14. Placing the CPU

2. Secure the screw, drop down the CPU socket to lock the CPU.

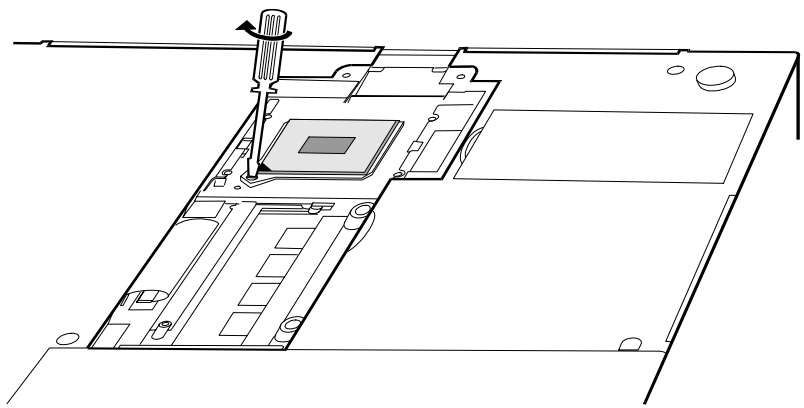


Figure 5-15. Securing the CPU

5.Assembly & Disassembly

5.2.4 Fax/Modem/Voice Card

Disassembly

1. Place the notebook upside down.
2. To remove the compartment cover, remove one screw, then lift up the cover.

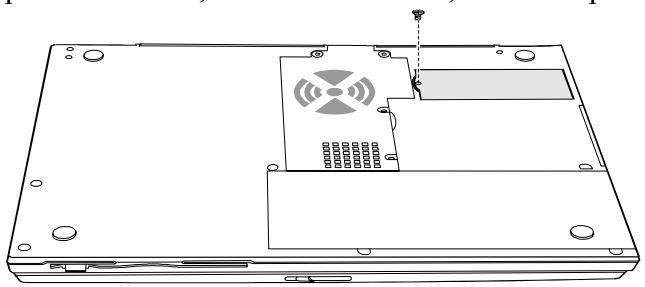


Figure 5-16. Removing the Fax/Modem/Voice Card Compartment Cover

3. Remove one screw. Then, lift up the inner edge of the card to remove the card.

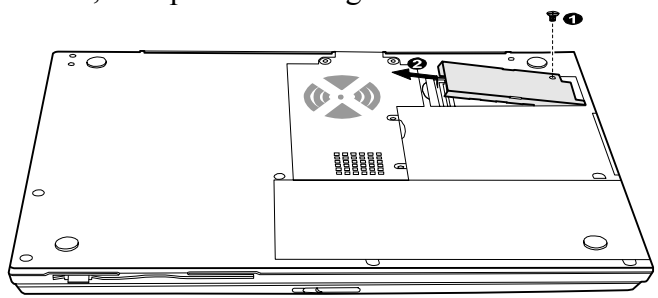


Figure 5-17. Removing the Fax/Modem/Voice Card

Reassembly

1. Hold the Fax/Modem/Voice Card at an angle so that the phone line connector is pointed towards the opening on the notebook. Insert the phone line connector into the opening and press the other end to plug the other connector into the socket on the system board. Then, secure with one screw. (Refer to Figure 5-17 earlier.)

2. Replace the compartment cover and secure with one screw. (Refer to Figure 2-16 earlier.)

2.2.5 SO-DIMM

Disassembly

1. Open the CPU compartment cover by removing four screws and lifting up the cover from one side. (See Figure 5-7.)
2. Pull the retaining clips outwards and remove the SO-DIMM.

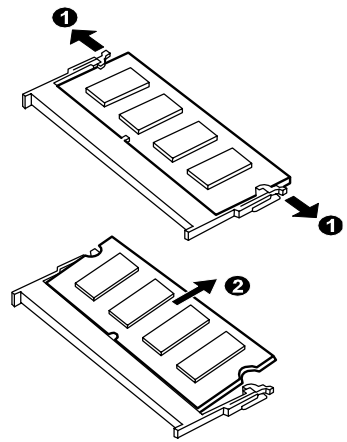


Figure 5-18. Removing the SO-DIMM

Reassembly

1. To install the SO-DIMM, align the SO-DIMM′ s notched part with the socket′ s corresponding part and firmly insert the SO-DIMM into the socket at an angle. Then push down until the retaining clips lock the SO-DIMM into position. (Refer to Figure 2-18 earlier.)
2. Replace the compartment cover and secure with four screws. (Refer to Figure 2-7 earlier.)

5.Assembly & Disassembly

5.2.6 LCD Assembly

Disassembly.

1. Remove six bottom screws.

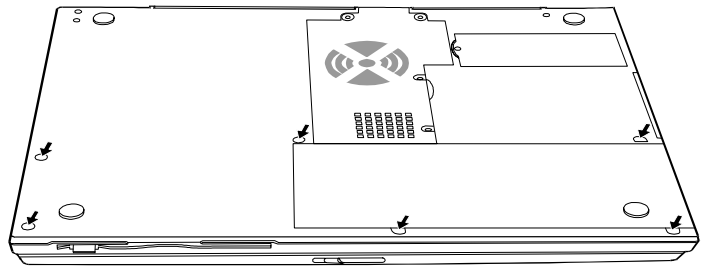


Figure 5-19. Removing Six Bottom Screws

2. Put the notebook back to the upright position and open the top cover. Remove the base unit cover.
3. Disconnect the keyboard cable form the system board.
4. Remove the shield plate by removing 12 screws.

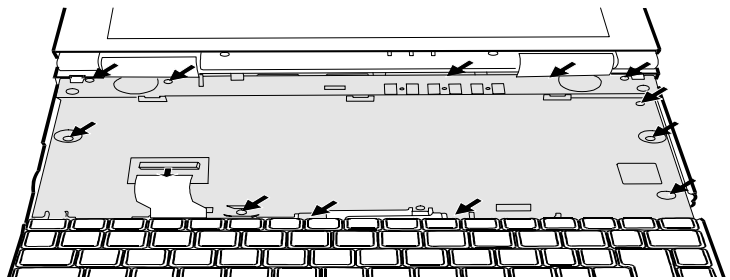


Figure 5-20. Removing the Shield Plate

5. Remove the hinge cover by inserting a flat screwdriver to the rear of the cover and pry the cover out. Repeat the same with the other hinge cover. Note the right and left hinges are not exchangeable.

5.Assembly & Disassembly

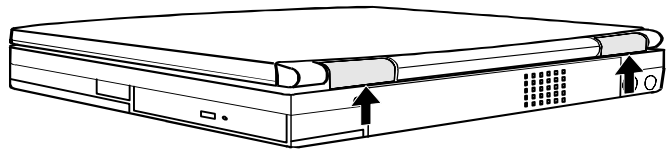


Figure5-21. Removing the Hinge Covers

6. Unplug the three cable connectors coming from the LCD assembly.
7. Remove four screws from the hinges. Now you can separate the LCD assembly from the base unit

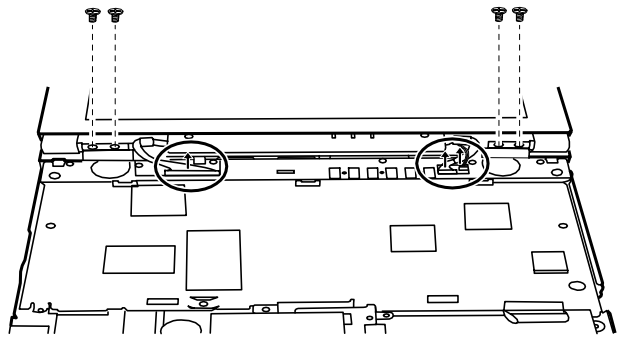


Figure 5-22. Unplugging the Cable Connectors and Removing Four Screws

Reassembly

1. Attach the LCD assembly to the base unit and secure with four screws on the hinges. (Refer to Figure 5-22 earlier.)
2. Reconnect the LCD cable connectors to the system board. (Refer to Figure5-22 earlier.)
3. Replace the two hinge covers. (Refer to Figure 5-21 earlier.)
4. Replace the shield plate and secure with 12 screws. (Refer to Figure 5-20 earlier.)
5. Connect the keyboard cable and replace the keyboard.
6. Replace the base unit cover.
7. Replace the six bottom screws. (Refer to Figure 5-19 earlier.)

5.Assembly & Disassembly

5.2.7.1 12.1 Inch LCD Panel

Disassembly

1. Open the top cover.
2. Remove the four rubber pads and the four screws underneath. Then you can separate the LCD frame from the housing.

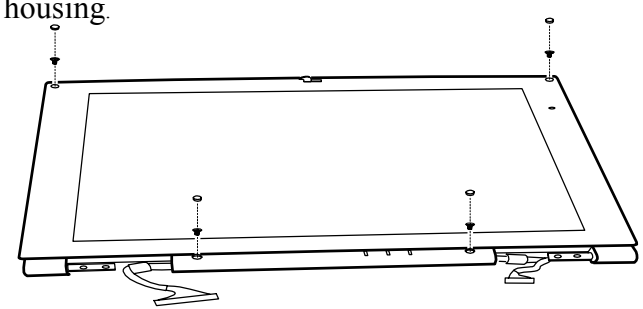


Figure 5-23. Removing the 12.1 Inch LCD Frame

3. To remove the LCD, remove four screws and unplug the cables.

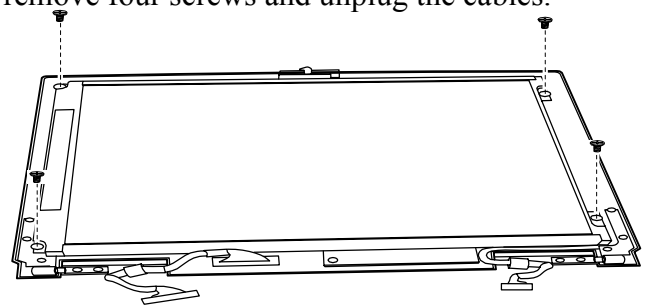


Figure 5-24. Removing the 12.1 Inch LCD

Reassembly

1. Reconnect the cables to the LCD. Fit the LCD back into place and secure with four screws. (Refer to Figure 5-24 earlier.)

5.Assembly & Disassembly

2. Fit the LCD frame back to the housing and replace the four screws and rubber pads. (Refer to Figure 2-23 earlier.)

5.2.7.2 13.3 Inch LCD Panel

Disassembly

1. Open the top cover.
2. Remove the four rubber pads and two screws on the bottom side. Then slightly lift up the bottom part of the frame and gently separate the LCD frame from the housing.

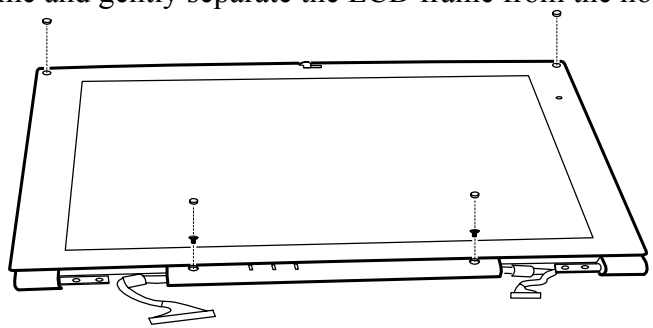


Figure 5-25. Removing the 13.3 Inch LCD Frame

3. To remove the LCD, remove six screws and unplug the cables.

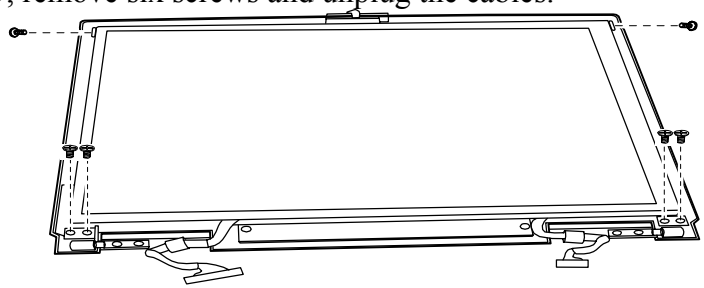


Figure 5-26. Removing the 13.3 Inch LCD

5.Assembly & Disassembly

Reassembly

1. Reconnect the cables to the LCD. Fit the LCD back into place and secure with six screws. (Refer to Figure 5-26 earlier.)
2. Fit the LCD frame back to the housing and replace the two screws and four rubber pads. (Refer to Figure 5-25 earlier.)

5.2.8 Inverter Board/LED Board

Disassembly

1. Detach the LCD frame. (See steps 1 to 2 in section 5.2.7 Disassembly.)
2. For 12.1 inch LCD:
   To remove the LED board at the bottom side of the LCD , remove one screw and unplug the connectors from the board.
   To remove the inverter board at the right side of the LCD , remove two screws and unplug the connectors from the board.

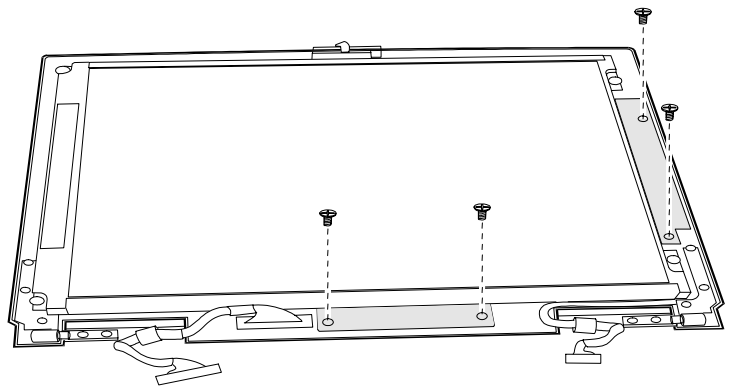


Figure 5-27. Removing the Inverter and LED Board for 12.1 Inch LCD

3. For 13.3 inch LCD:
   To remove the inverter/LED board at the bottom side of the LCD , remove one screw and unplug the connectors from the board.

5.Assembly & Disassembly

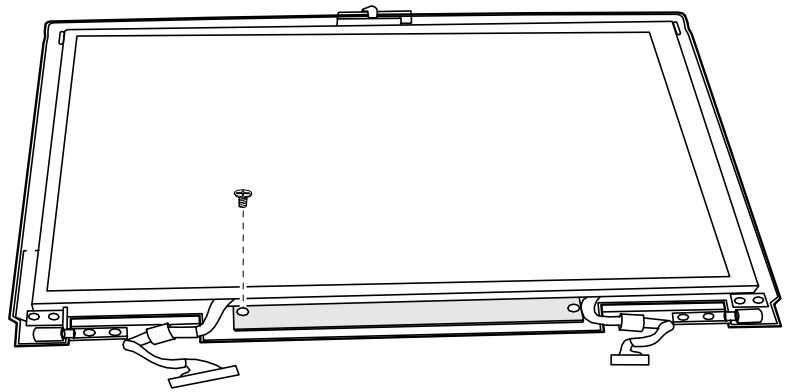


Figure 5-28. Removing the Inverter/LED Board for 13.3 Inch LCD

Reassembly

1. Reconnect the connectors. Fit the inverter/LED board back into place and secure with according number of screws. (Refer to Figure 5-28 and 5-27 earlier.)
2. Place the LCD frame back to the housing. (Refer to Figure 5-25 and 2-23 earlier.)

5.2.9 Keyboard

Disassembly

1. Remove the base unit cover. (See section 5.2.6 Disassembly steps 1 to 2.)
2. Lift the keyboard and unplug the keyboard cable from the system board.

Reassembly

1. Reconnect the keyboard cable and fit the keyboard back into place.
2. Replace the base unit cover. (See section 5.2.6 Reassembly steps 6 to 7.)

5.Assembly & Disassembly

5.2.10 Hard Disk Drive

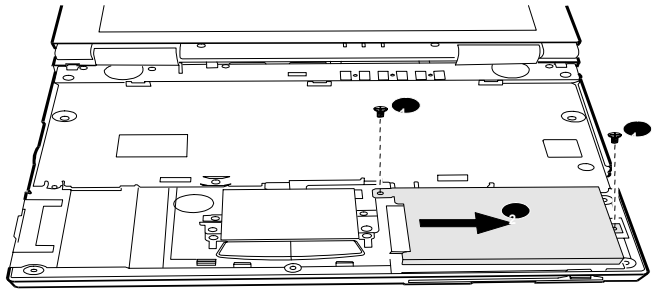


Figure 5-29. Removing the Hard Disk Drive

Disassembly

1. Remove the base unit cover. (See section 5.2.6 Disassembly steps 1 to 2.)
2. Remove two top screws from the hard disk drive bracket and slide the hard disk drive outwards to unplug the connector.

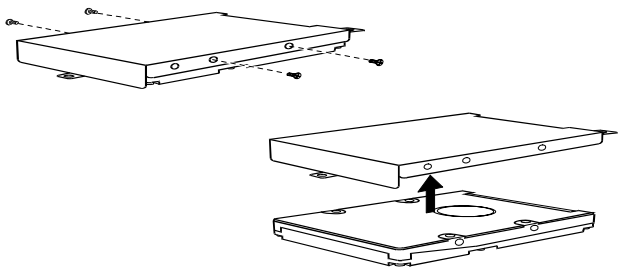


Figure 5-30. Removing the Hard Disk Drive Bracket

3. To separate the hard disk drive from the bracket, remove four side screws from the bracket.

Reassembly

1. Attach the bracket to the hard disk drive and secure with four screws on both sides. (Refer to Figure 5-30 earlier.)
2. Plug the hard disk drive connector to the touchpad board and secure the bracket in place with two screws. (Refer to Figure 5-29 earlier.)
3. Replace the base unit cover. (See section 5.2.6 Reassembly steps 6 to 7.)

5.Assembly & Disassembly

5.2.11 Touchpad Board

Disassembly

1. Remove the shield plate. (See section 5.2.6 Disassembly steps 1 to 4.)
2. Remove the hard disk drive. (See section 5.2.10.)
3. Lift the touchpad board free.

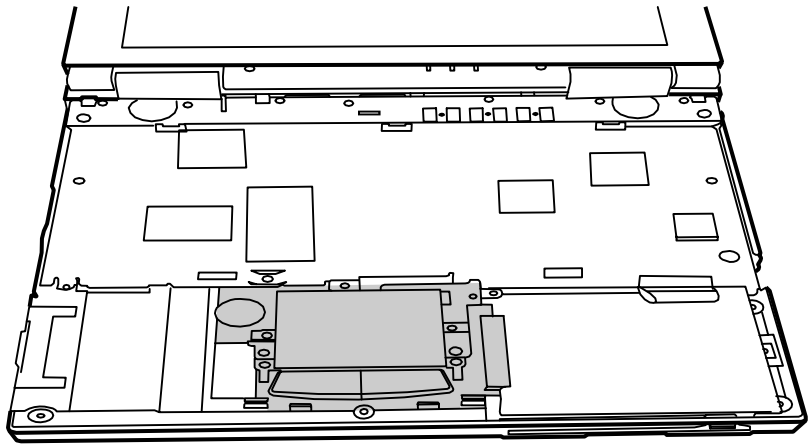


Figure 5-31. Removing the Touchpad Board

Reassembly

1. Fit the touchpad board into place. (Refer to Figure 5-31 earlier.)
2. Replace the hard disk drive. (See section 5.2.10 Reassembly.)
3. Replace the shield plate. (See section 5.2.6 Reassembly steps 4 to 7.)

5.Assembly & Disassembly

5.2.12 System Board

Disassembly

1. Remove all the bottom screws.
2. Remove the battery pack. (See section 5.2.1.)
3. Remove the CD-ROM drive. (See section 5.2.2.)
4. Remove the CPU and cooling fan assembly. (See section 5.2.3.)
5. Remove the Data/Fax/Modem Card if it exists. (See section 5.2.4.)
6. Remove the LCD assembly. (See section 5.2.6.)
7. Remove the hard disk drive. (See section 5.2.10.)
8. Remove the touchpad board. (See section 5.2.11.)
9. Unplug the speaker connectors from the system board.
10. Remove five screws fastening the rear frame.

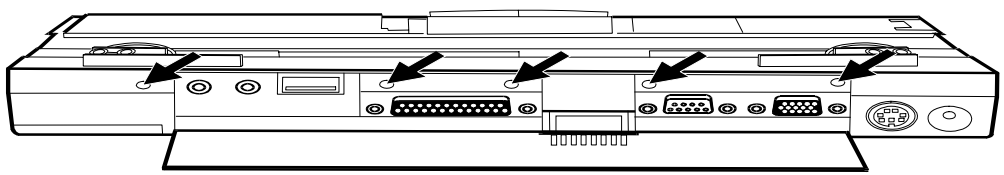


Figure 5-32. Removing Five Rear Screws

11. Gently lift the rear frame free from the housing.

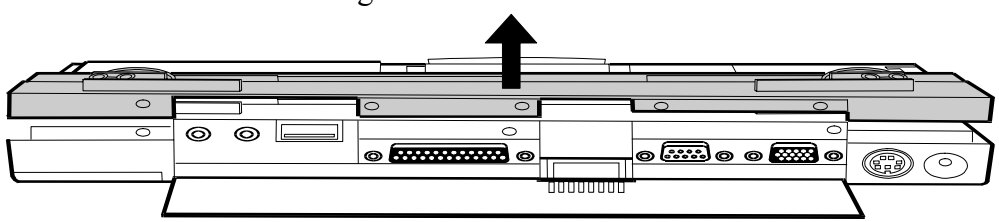


Figure 5-33. Removing the Rear Frame

5.Assembly & Disassembly

12. Remove two bottom screws fastening the system board.

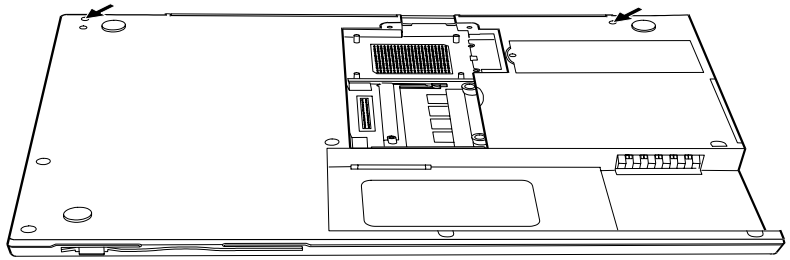


Figure 5-34. Removing Two Bottom Screws

13. Unplug the floppy disk drive cable connector from the system board. Lift the system board free.

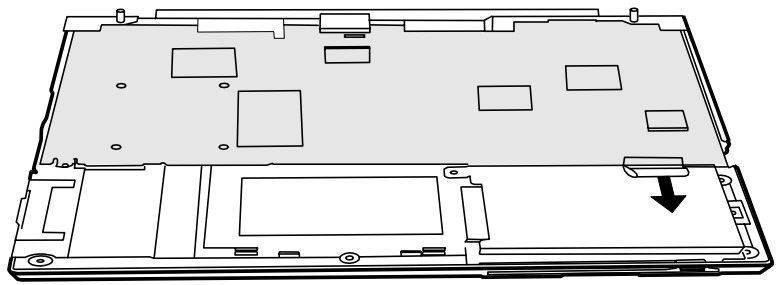


Figure 5-35. Unplugging the Floppy Disk Drive Cable

Reassembly

1. Fit the system board into place.
2. Connect the floppy disk drive cable to the system board. (Refer to Figure 5-35 earlier.)
3. Replace two bottom screws fastening the system board. (Refer to Figure 5-34 earlier.)
4. Replace the rear frame and five rear screws. (Refer to Figure 5-33 and 5-32 earlier.)
5. Replace the touchpad board by plugging the connector. (Refer to Figure 5-31 earlier.)
6. Replace the hard disk drive with its bracket by plugging the connector to the touchpad board and securing with two screws. (Refer to Figure 5-29 earlier.)

5.Assembly & Disassembly

7. Connect the speaker connectors.
8. Attach the LCD assembly to the base unit and secure with four screws. (Refer to Figure 5-22 earlier.)
9. Replace the two hinge covers. (Refer to Figure 5-21 earlier.)
10. Fit the shield plate back into place and secure with 12 screws. (Refer to Figure 5-20 earlier.)
11. Connect the keyboard cable and replace the keyboard.
12. Fit the base unit cover into place and secure with six bottom screws. (Refer to Figure 5-19 earlier.)
13. Replace the CD-ROM drive by sliding it into the compartment, plugging the connector, and secure with one bottom screw. (Refer to Figure 5-9 and 5-8 earlier.)
14. Replace the CPU and fan assembly. (Refer to section 5.2.3 Reassembly.)
15. Replace the CPU compartment cover and secure with four screws. (Refer to Figure 5-7 earlier.)
16. Replace the Data/Fax/Modem Card and secure with one screw. (Refer to Figure 5-17 earlier.)
17. Replace the Data/Fax/Modem Card compartment cover and secure with one screw. (Refer to Figure 5-16 earlier.)
18. Replace the battery pack. (Refer to Figure 5-6 earlier.)

5.2.13 Floppy Disk Drive

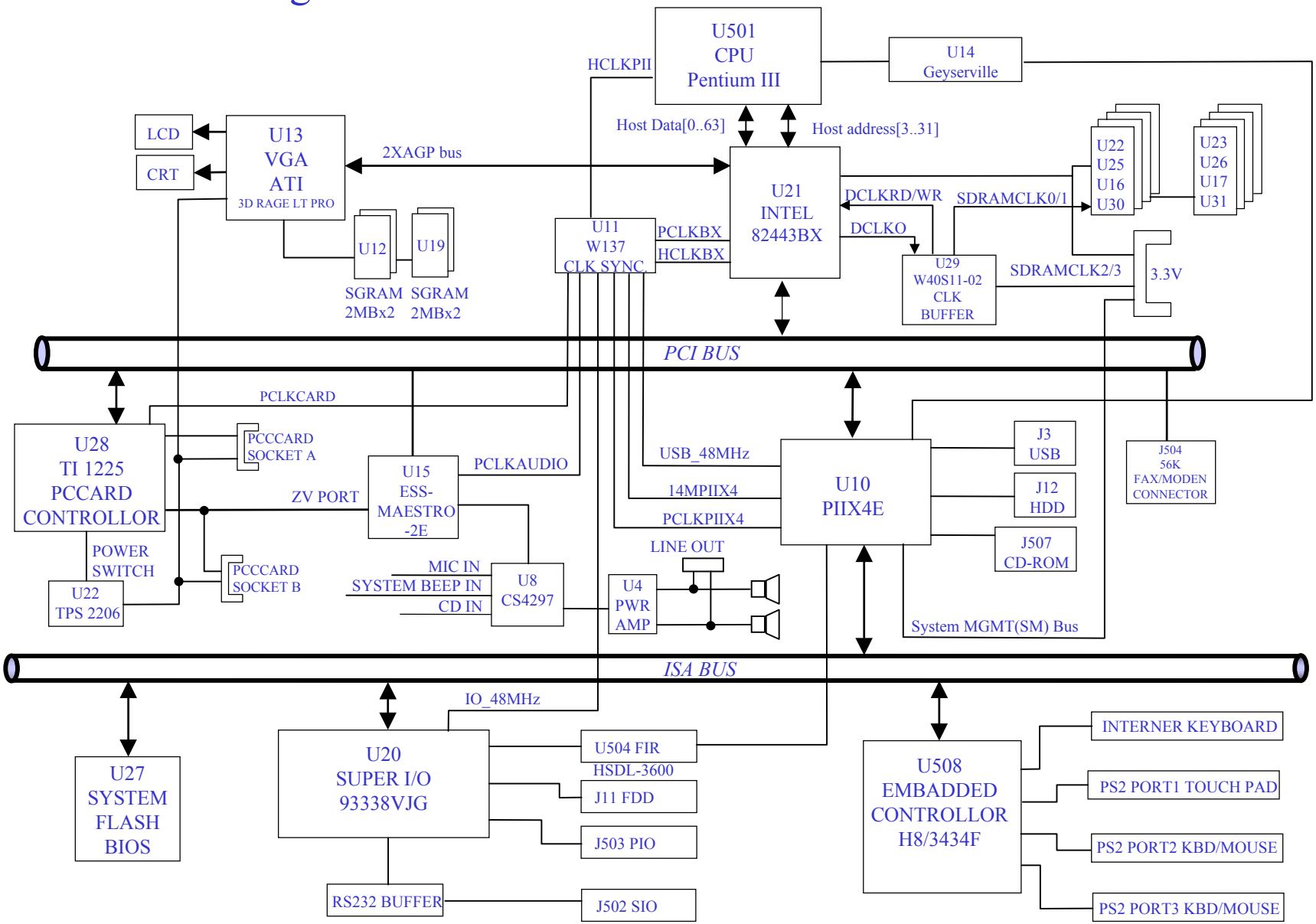
Disassembly

1. Remove the system board. (See section 5.2.12 Disassembly.)
2. Remove the floppy disk drive by first lifting the rear end of the floppy disk drive.

Reassembly

1. Connect the floppy disk drive cable to the floppy disk drive and fit the floppy disk drive into place.
2. Replace the system board. (See section 5.2.12 Reassembly.)

6.7233 Block Diagram-2



7. Maintenance Diagnostics

7.1 Introduction

Every time the computer is turned on ,the system bios runs a series of Internal checks on the hardware. This power-on self test (post) Allows the computer to detect problems as early as the power-on Stage. Error messages of post can alert you to the problems of your Computer.

If an error is detected during these tests, you will see an error Message displayed on the screen. If the error occurs before the Display, then the screen cannot display the error message. Error codes Or system beeps are used to identify a post error that occurs when the Screen is not available.

The value for the diagnostic post(378h) is written at the beginning of The test. Therefore , if the test fail, the user can determine where The problem occurs by reading the last value written to post 378h By the PIO debug board plug at PIO port.

7. Maintenance Diagnostics

7.2 Error Codes : Following is a list of error codes in sequent display on the PIO debug board.

SYSTEM SOFT BIOS:

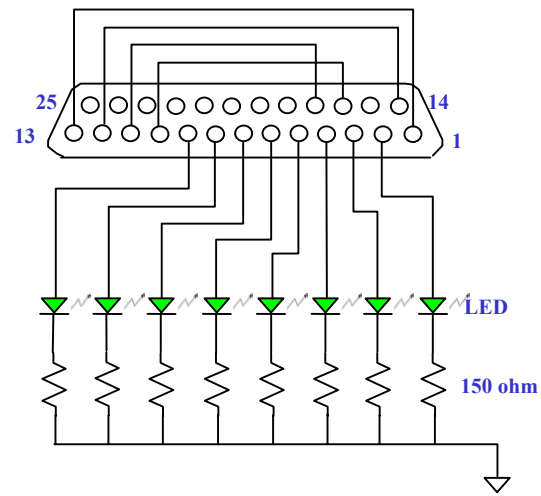
CODE	DESCRIPTION
01h	Start of boot loader sequence.
02h	Initialize chipset.
03h	Memory Sizing.
04h	Perform conventional RAM(1st 640K) test with crossed-
	pattern R/W
05h	Move boot loader to the RAM.
06h	Start point of execution of boot loader in RAM.
07h	Shadow system BIOS.
08h	Initialize clock synthesizer
09h	Initialize audio controller.
0Ah	Detect internal ISA MODEM
0Bh	Proceed with normal boot
0Ch	Proceed with crisis boot
0Fh	DRAM sizing
10h	Initial L1,L2 cache, make stack and diagnose CMOS.
11h	Turn off fast A20 for post. Reset GDT's, 8259s quickly.
12h	Signal power on reset at COMS.
13h	Initialize the chipset, (SDRAM).
14h	Search for ISA bus VGA adapter
15h	Reset counter/timer 1, exite the RAM.
16h	User register config through CMOS
18h	Dispatch to 1st 64K RAM test
19h	Checksum the ROM
1Ah	Reset PIC's(8259s)
1Bh	Initialize video adapter(s)
1Ch	Initialize video (6845 regs)

CODE	DESCRIPTION
1Dh	Initialize color adapter
1Eh	Initialize monochrome adapter
1Fh	Test 8237A page registers
20h	Perform keyboard self test
21h	Test & initialize keyboard controller
22h	Check if CMOS RAM valid
23h	Test battery fail & CMOS X-SUM
24h	Test the DMA controllers
25h	Initialize 8237A controller
26h	Initialize interrupt vectors table.
27h	RAM quick sizing
28h	Protected mode entered safely
29h	RAM test completed
2Ah	Protected mode exit successful
2Bh	Setup shadow
2Ch	Prepare to initialize video
2Dh	Search for monochrome adapter
2Eh	Search for color adapter, VGA initialize.
2Fh	Signon messages displayed
30h	Special init of keyboard ctlr
31h	Test if keyboard present
32h	Test keyboard interrupt
33h	Test keyboard command Byte
34h	Test, blank and count all RAM
35h	Protected mode entered safely (2).
36h	RAM test complete

7. Maintenance Diagnostics

CODE	DESCRIPTION
37h	Protected mode exit successful
38h	Update keyboard output port to disable gate of A20
39h	Setup cache controller
3Ah	Test if 18.2Hz periodic working
3Bh	Initialize BIOS data area at 40:0.
3Ch	Initialize the hardware interrupt vector tabl
3Dh	Search and init the Mouse
3Eh	Update num lock status
3Fh	OEM initialization of COMM and LPT ports
40h	Configure the COMM and LPT ports
41h	Initialize the floppies
42h	Initialize the hard disk
43h	OEM's init of PM with USB
44h	Initialize additional ROMs
45h	Update NUMLOCK status
46h	Test for coprocessor installed
47h	OEM's init of power management, (check SMI)
48h	OEM functions before boot (PCMCIA, CardBus)
49h	Dispatch to operation system boot
4Ah	Jump into bootstrap code

Pio Port (378h) Diagnostic Tools



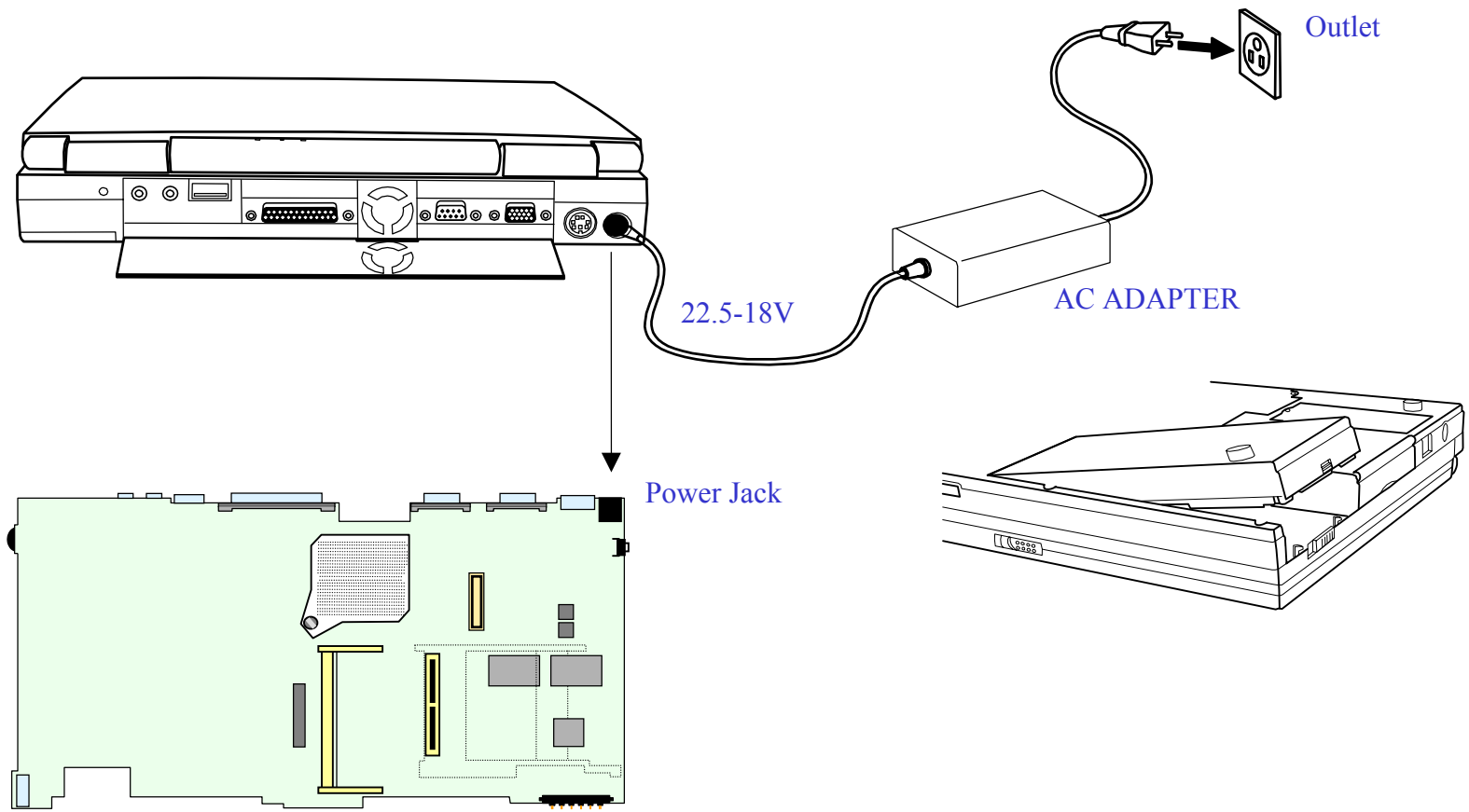
PIN1 : STROBE ⟷ PIN13: SLCT
PIN10: ACK# ⟷ PIN16: INT#
PIN11: BUSY ⟷ PIN17: SELIN#
PIN12:PTERR ⟷ PIN14: AUTOFD#
PIN[9:2]:PD[7:0]

8. Trouble Shooting

8.1 No Power:

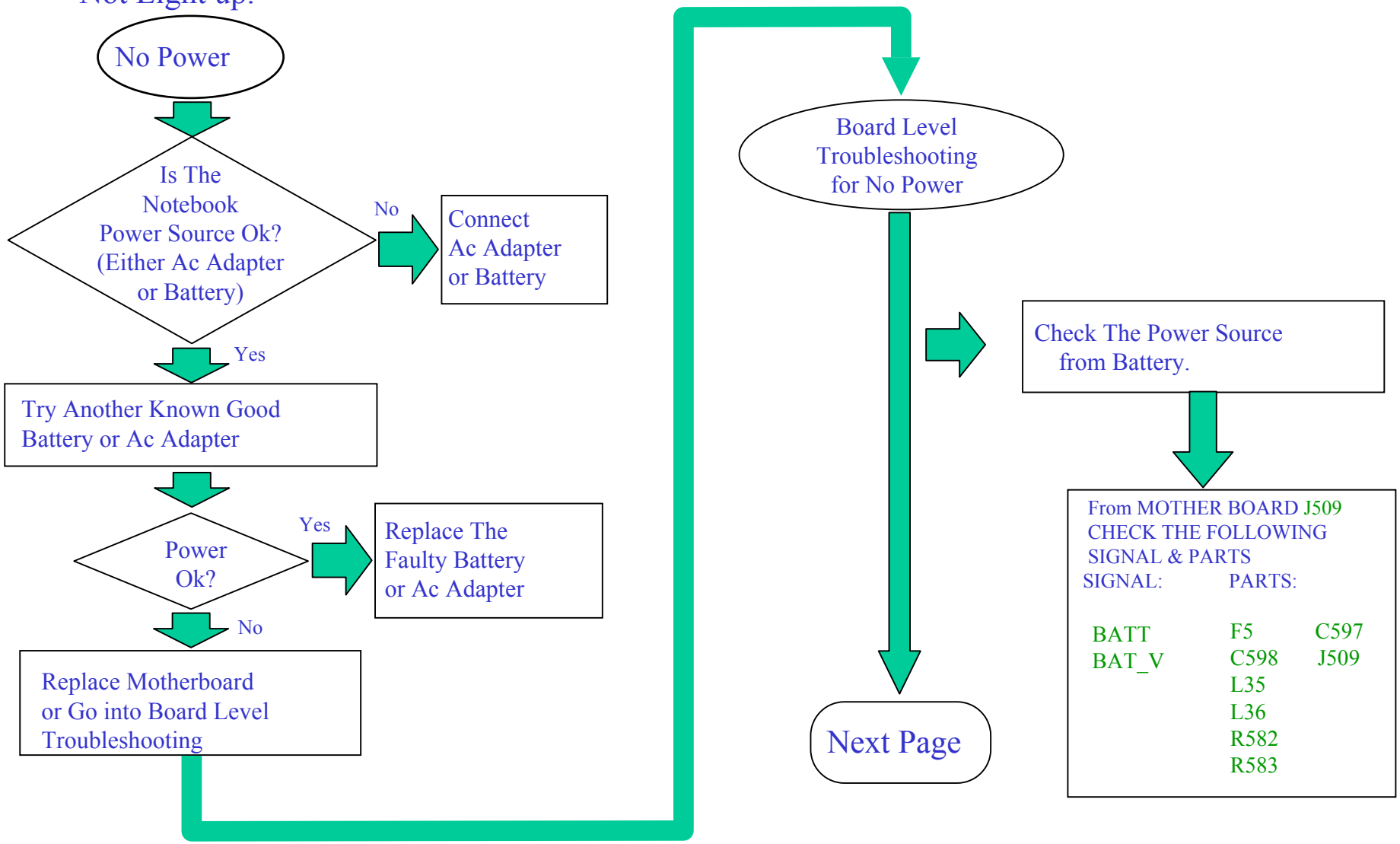
When the Power Button Is Pressed, Nothing Happens ,Power Indicator Does Not Light up.

1. Check Ac Adaptor
2. Check Battery



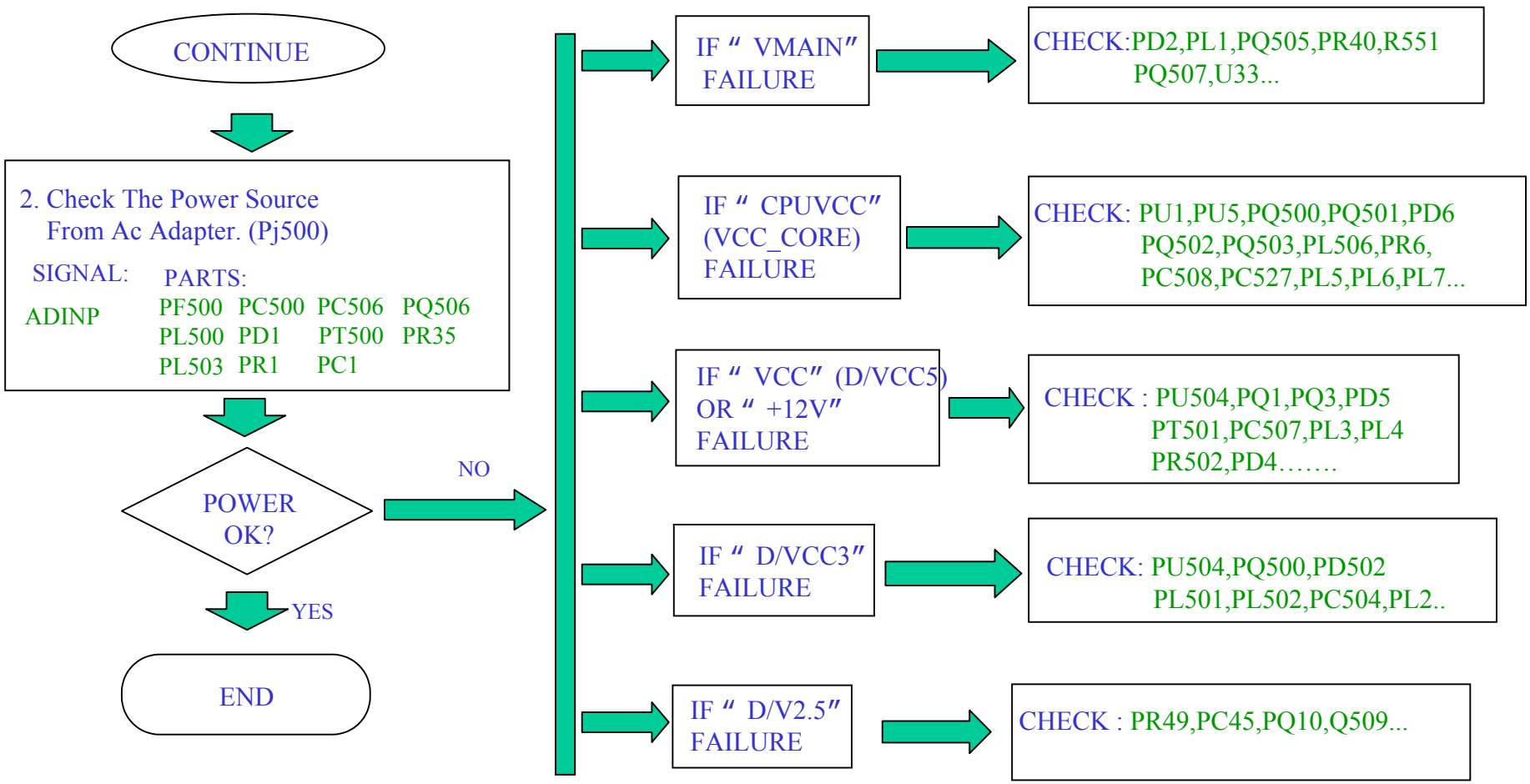
8.1 No Power:

When the Power Button Is Pressed, Nothing Happens ,Power Indicator Does Not Light up.



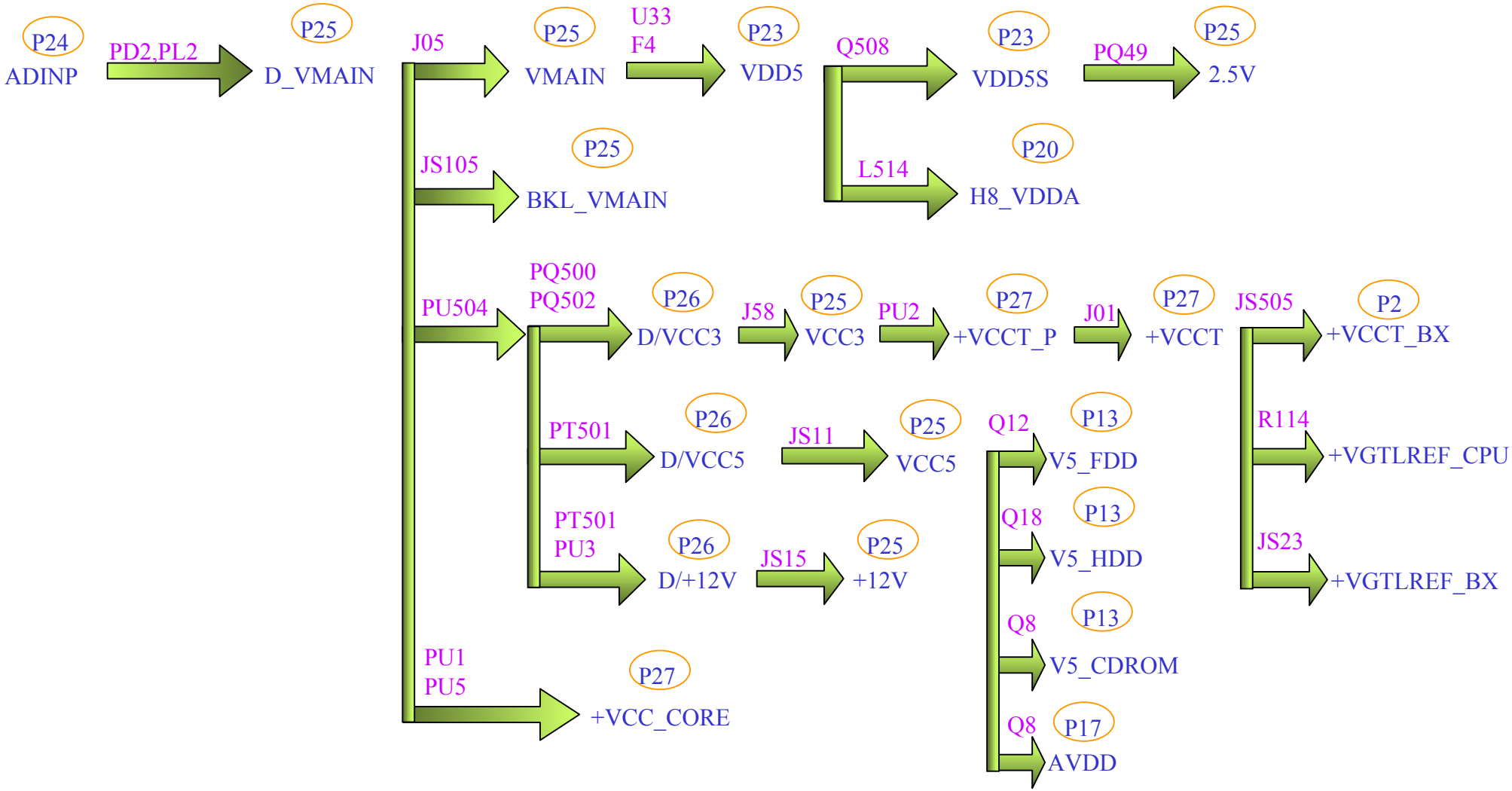
8.1 No Power:

When The Power Button Is Pressed, Nothing Happens ,Power Indicator Does Not Light Up.



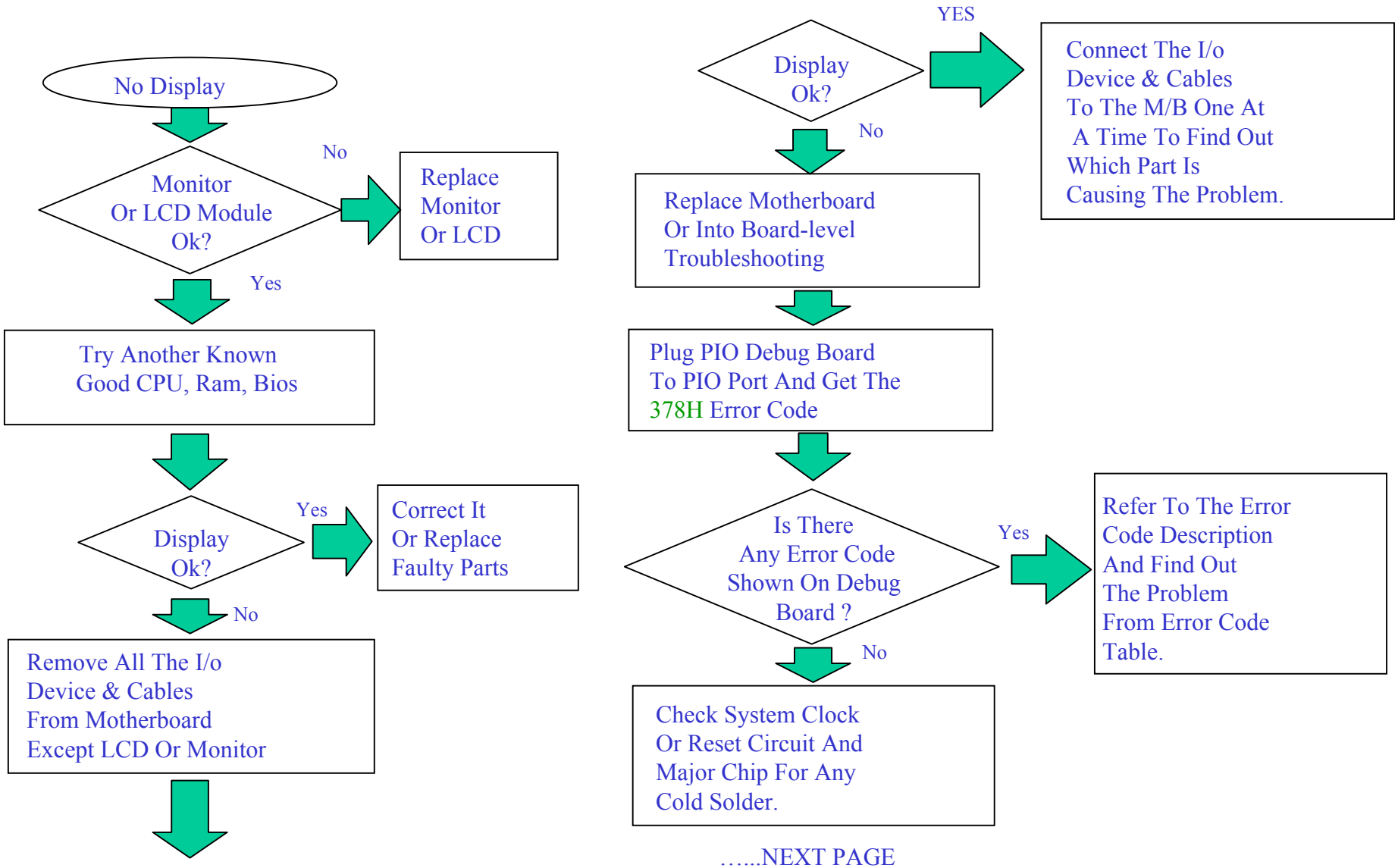
8.1 No Power:

When The Power Button Is Pressed, Nothing Happens ,Power Indicator Does Not Light Up. Please Check The Following Voltage Map.



8.2 No Display

There is no display on both of LCD and monitor



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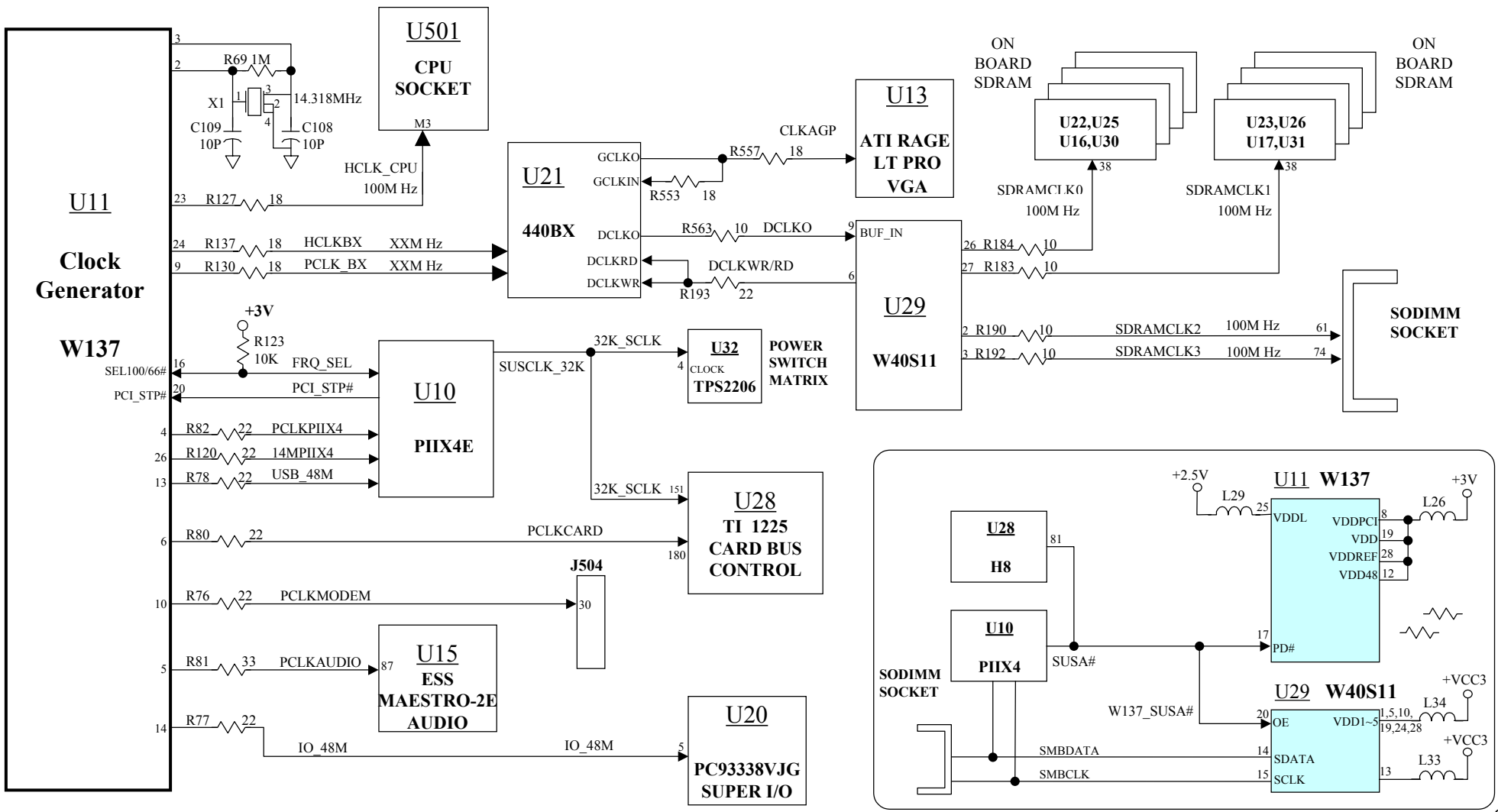
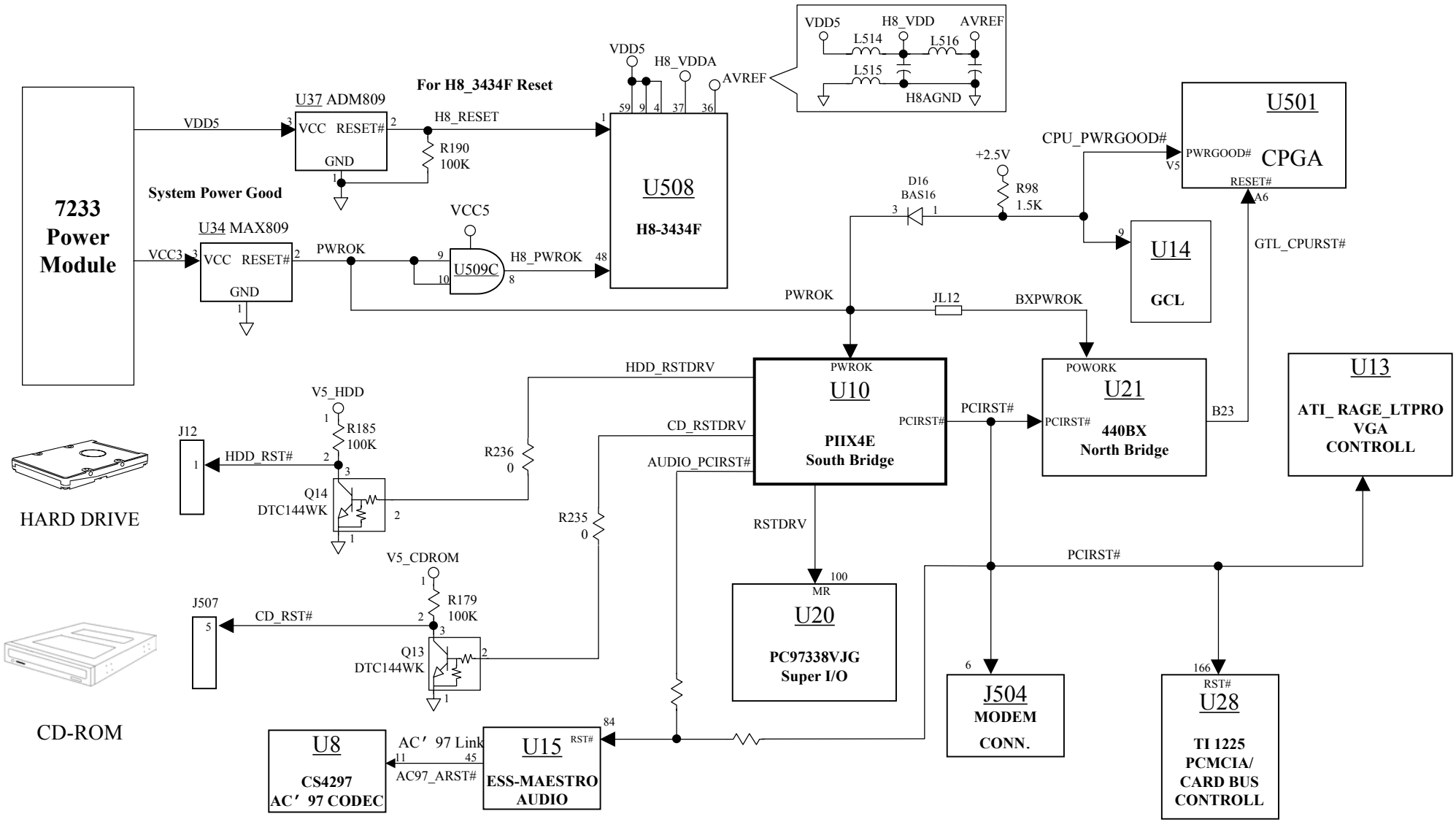
8.2 No Display (System Failure)

******* CLOCK CIRCUIT CHECKING *******



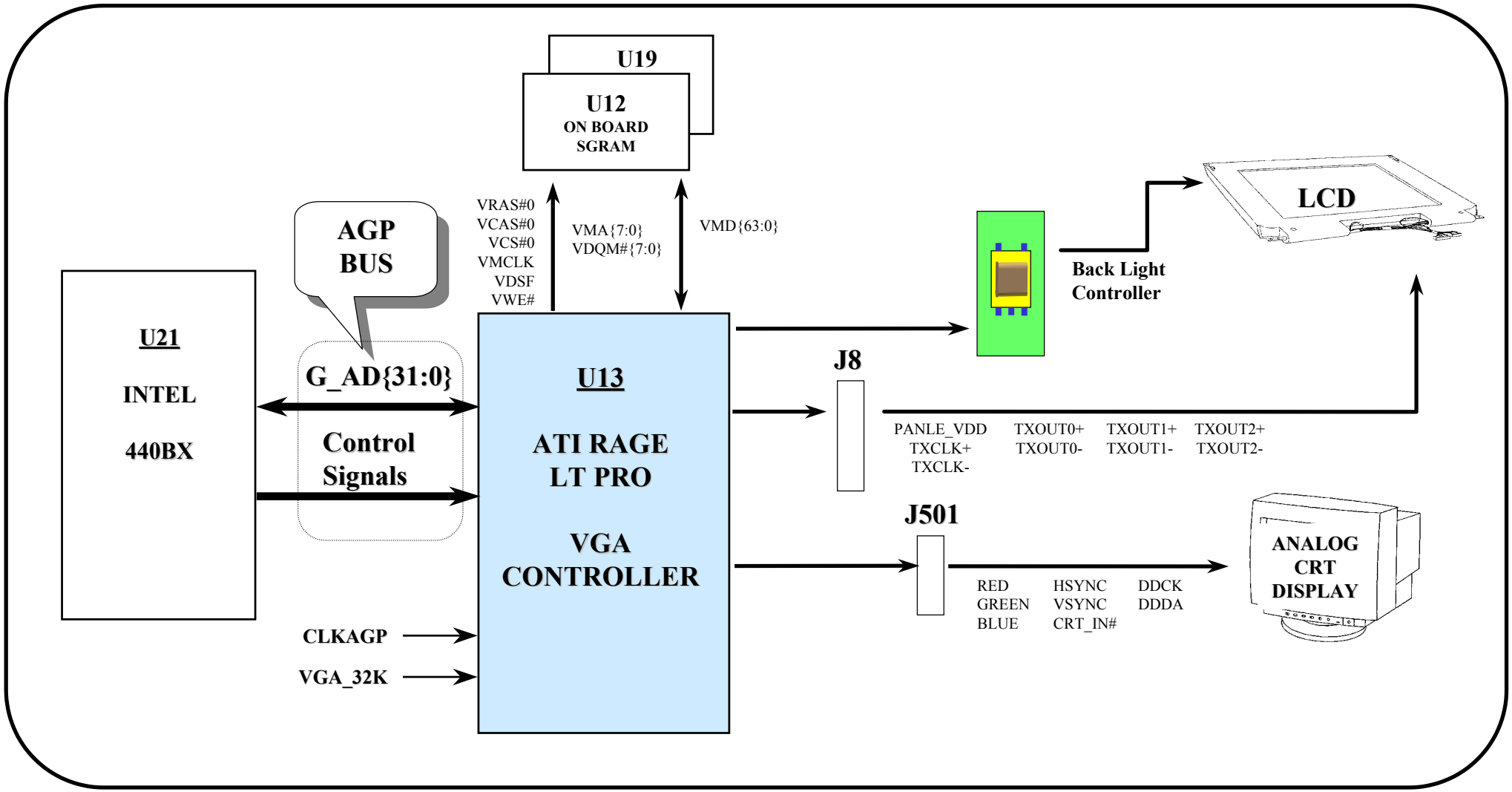
8.2 No Display (System Failure)

********* RESET CIRCUIT CHECKING *********



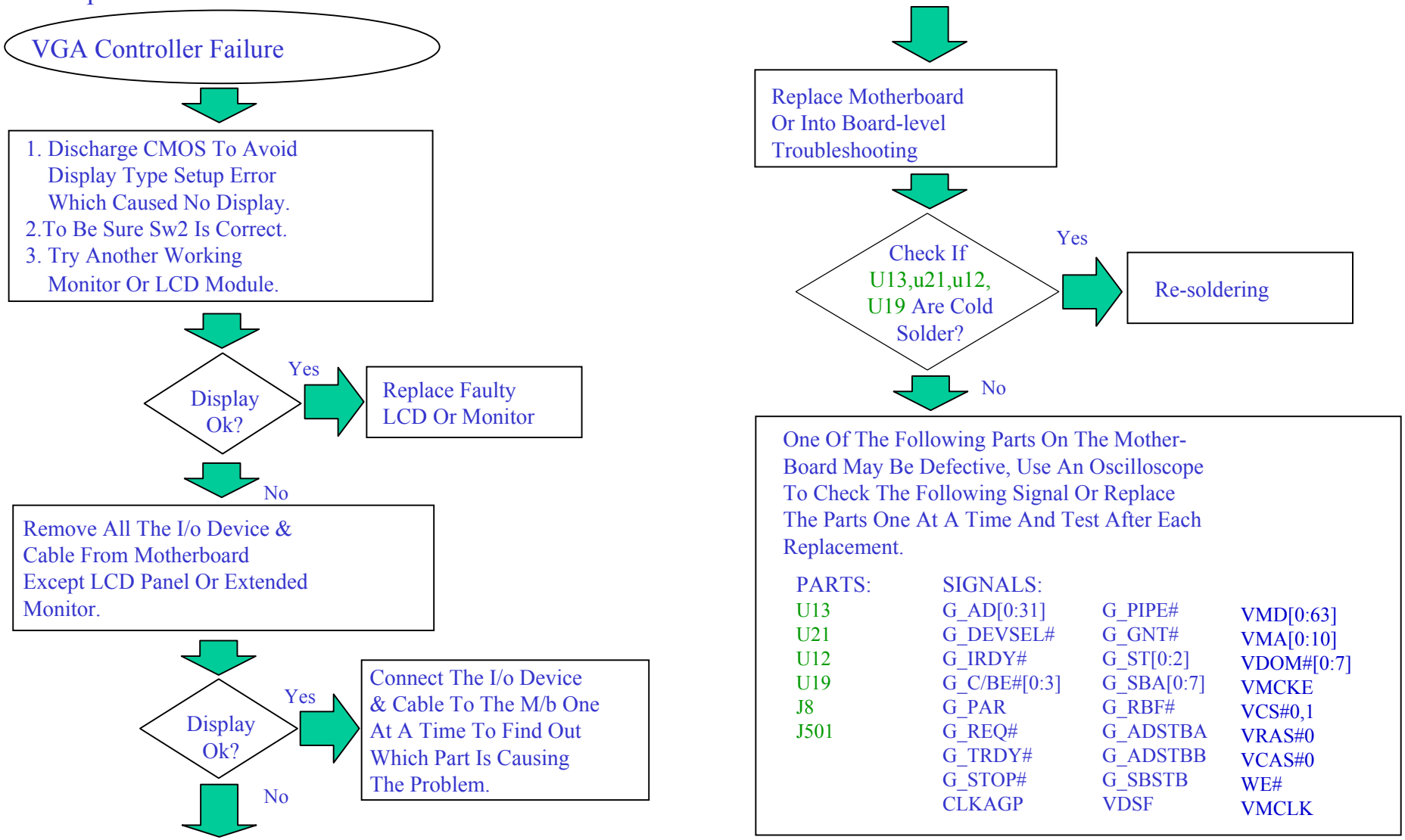
8.3 VGA Controller Failure

Symptom:
There is no display on both LCD and Monitor although power-on-self-test is passed.



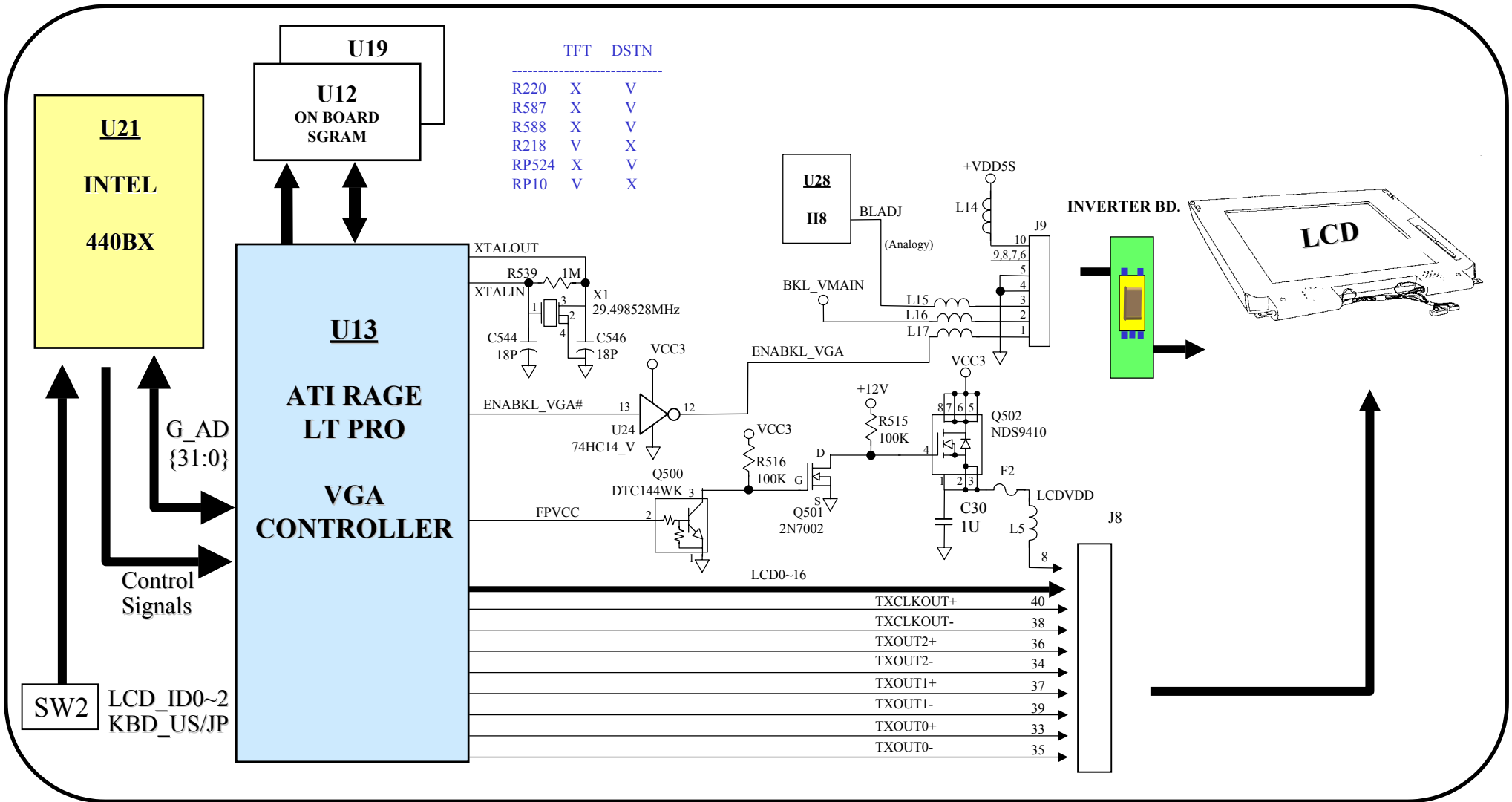
8.3 VGA Controller Failure

There is no display on both LCD and monitor although power-on-self-test Is passed.



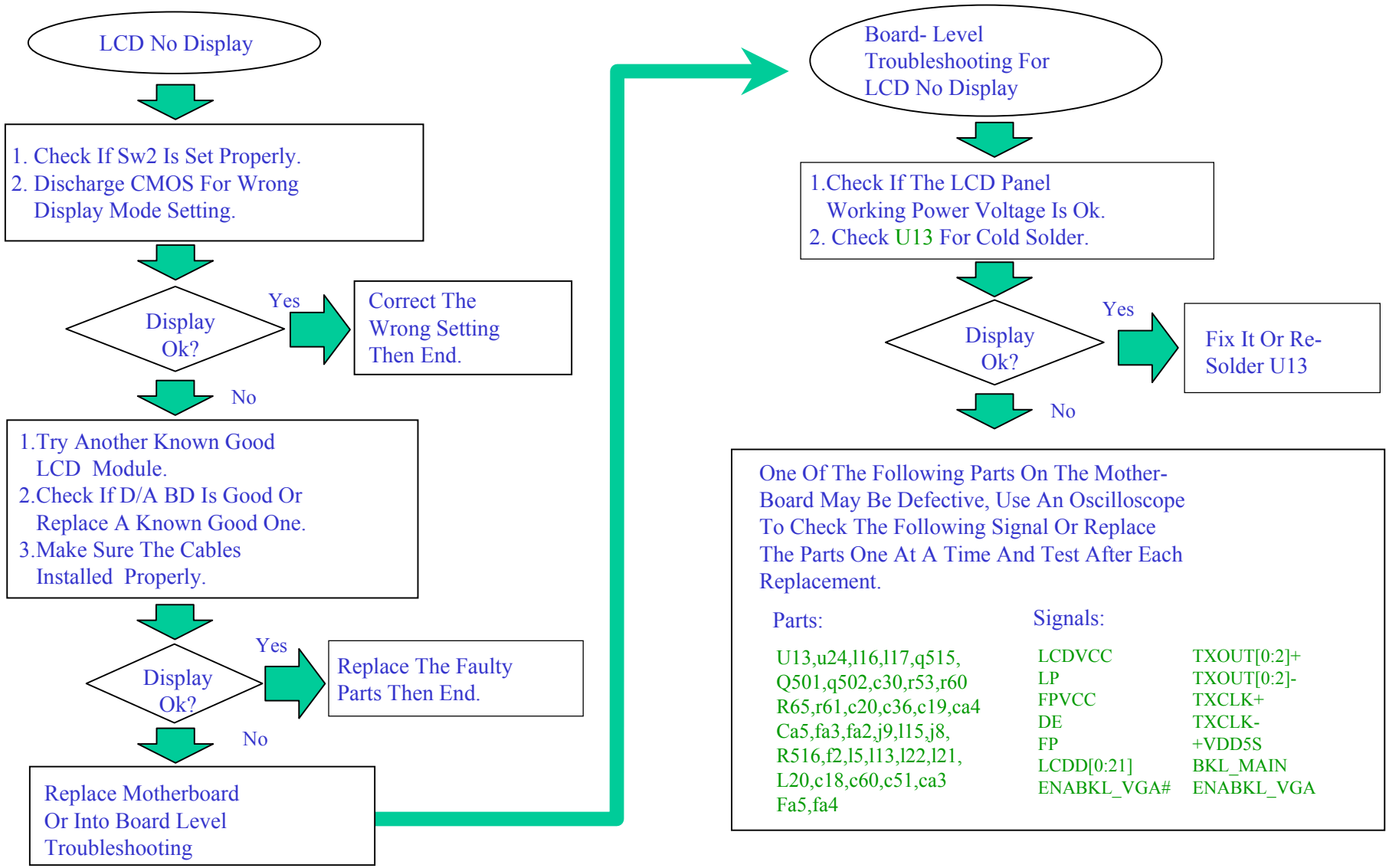
8.4 LCD NO DISPLAY OR PICTURE ABNORMAL

Symptom:
The LCD Shows Nothing or Abnormal Picture, but It Is Ok for External Monitor.



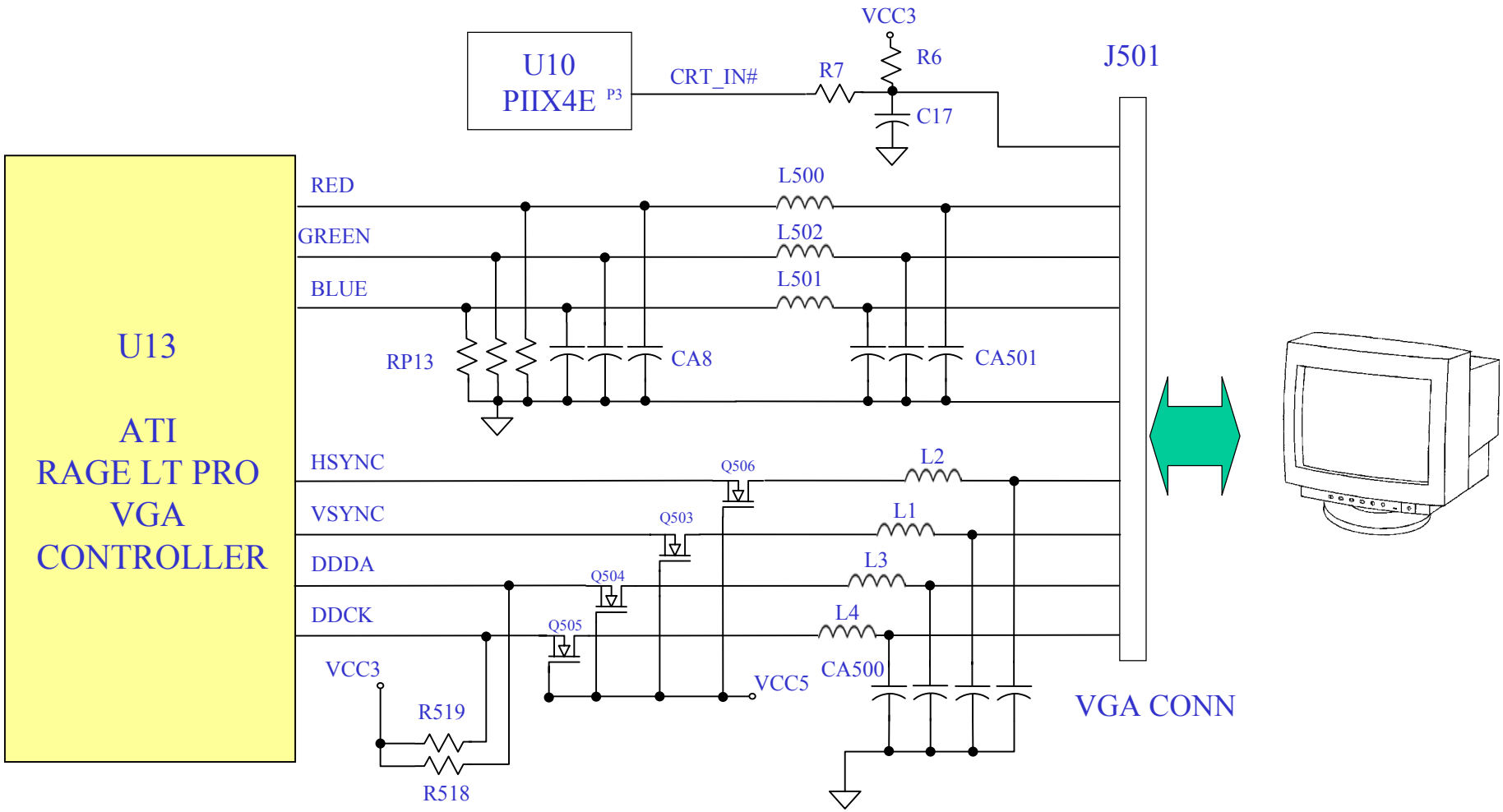
8.4 LCD No Display

The LCD Shows Nothing Or Abnormal Picture , But It Is Ok for External Monitor.



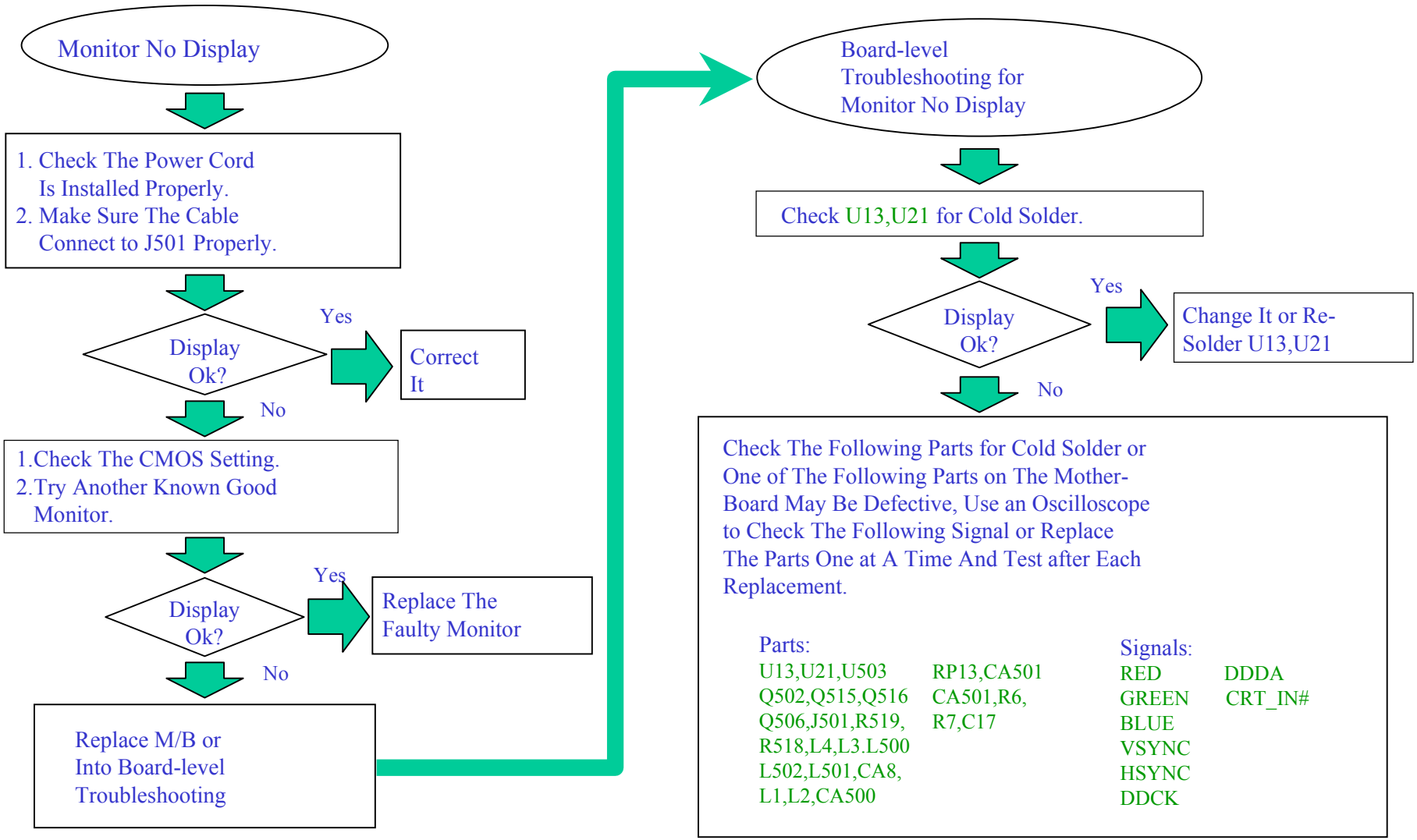
8.5 External Monitor No Display

The CRT Monitor Shows Nothing Or Abnormal Color, But It Is Ok For LCD.



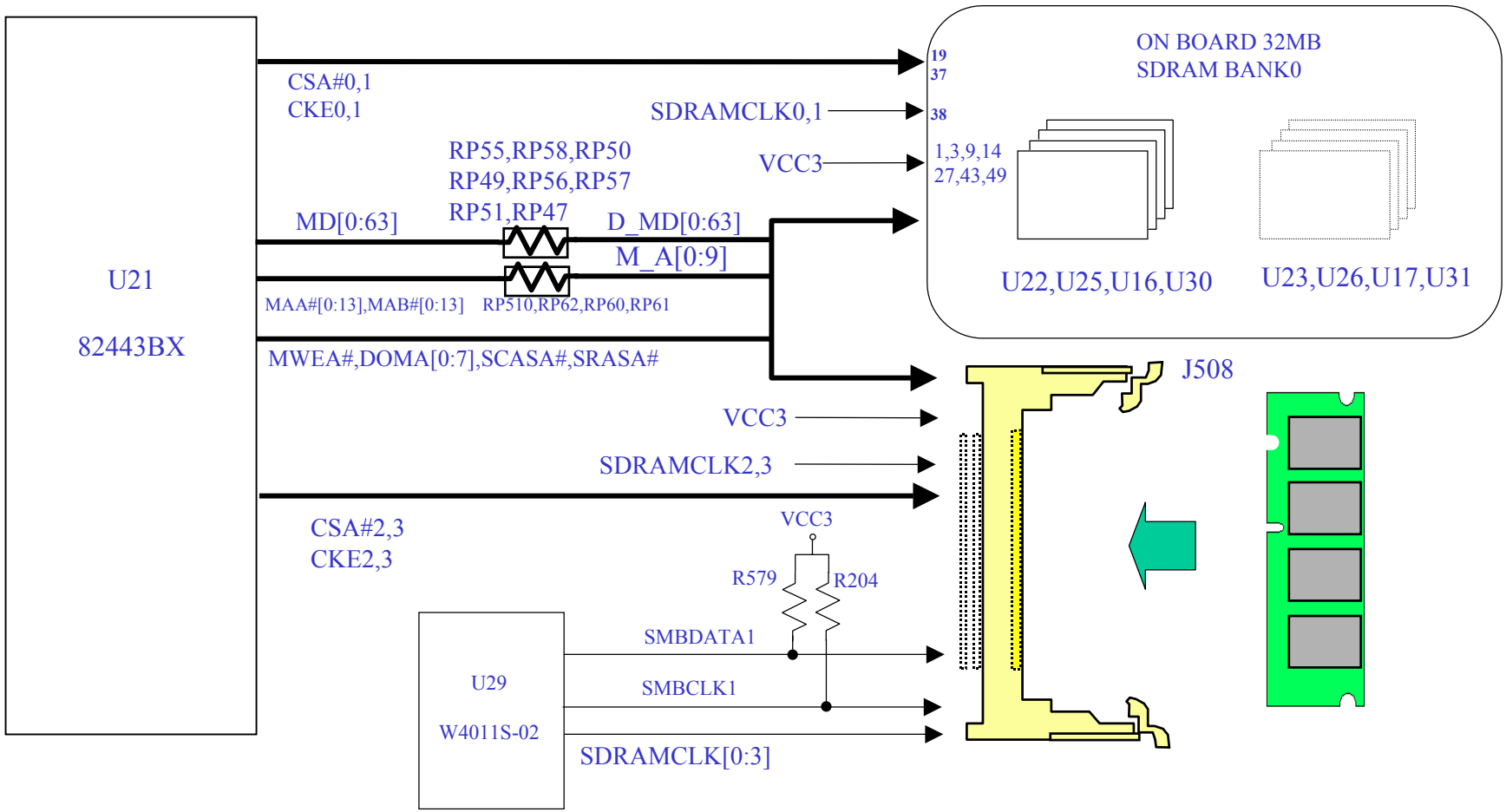
8.5 External Monitor No Display

The CRT Monitor Shows Nothing Or Abnormal Color, But It Is Ok for LCD.



8.6 Memory Test Error

Either on Board or Extend SDRAM ,The Error Code Shown
on The PIO Debug Board Is Mean Memory Error And System Hangs Up.



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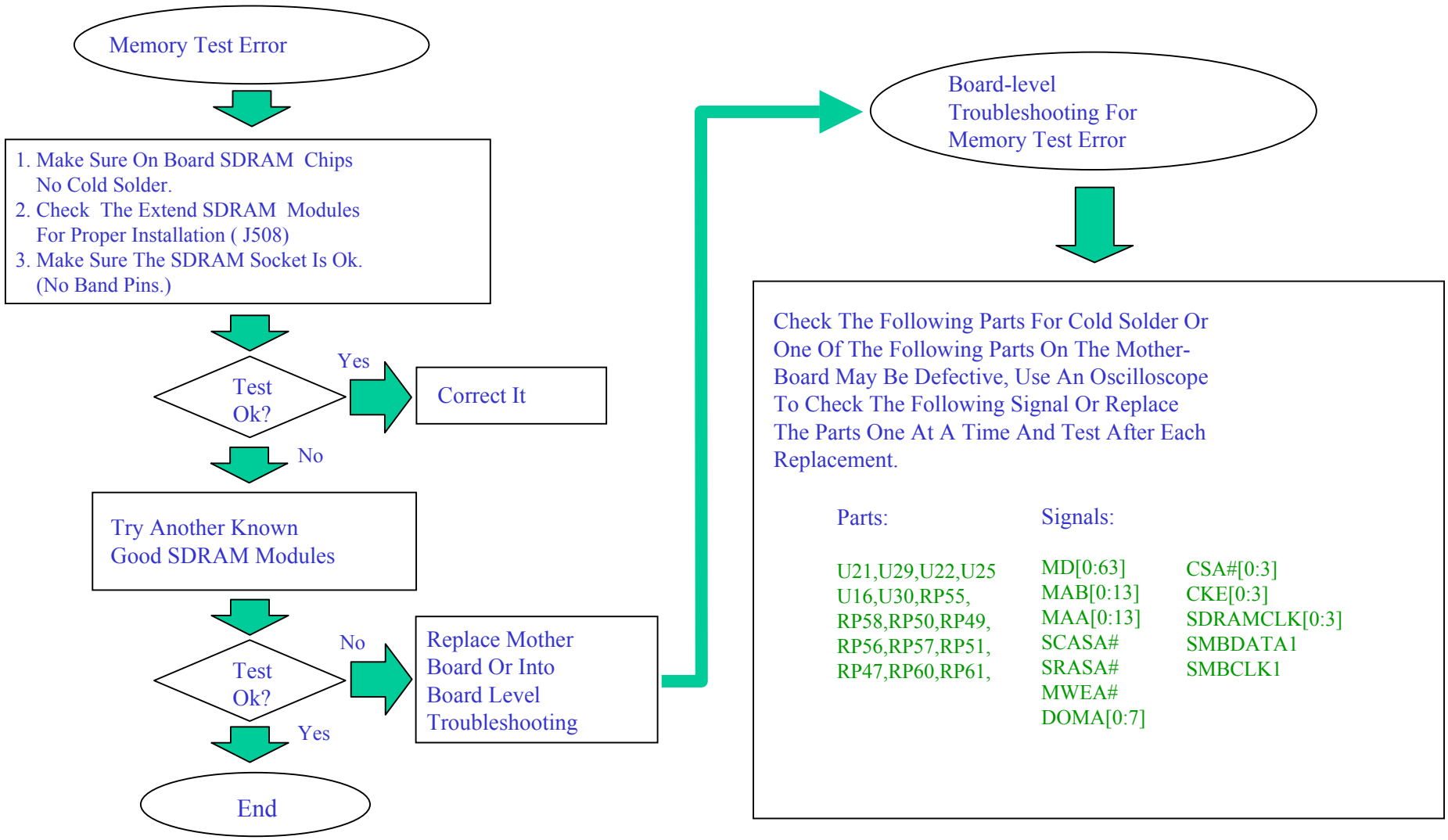
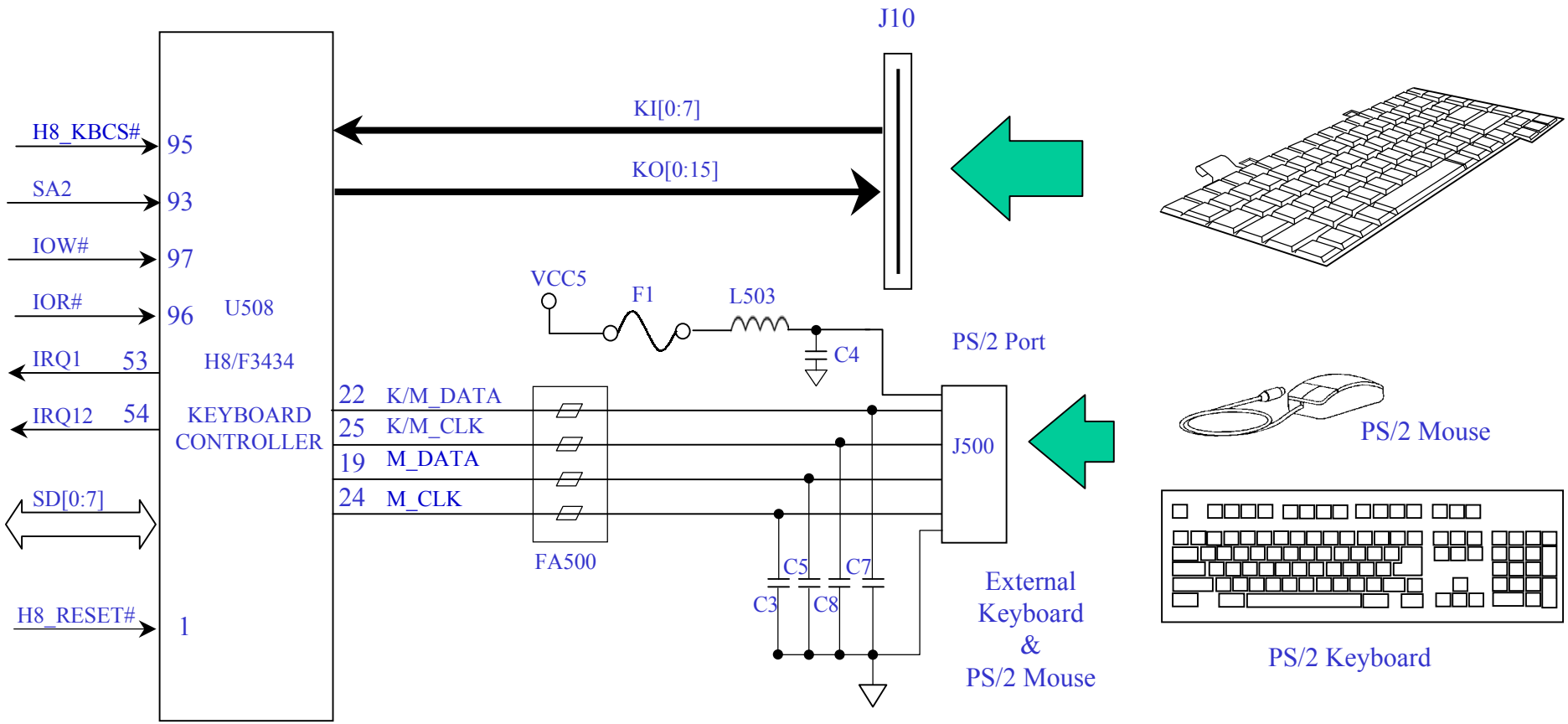


8.7 Keyboard Test Error

Error Message of Keyboard Failure Is Shown or Any Key Doesn't Work.



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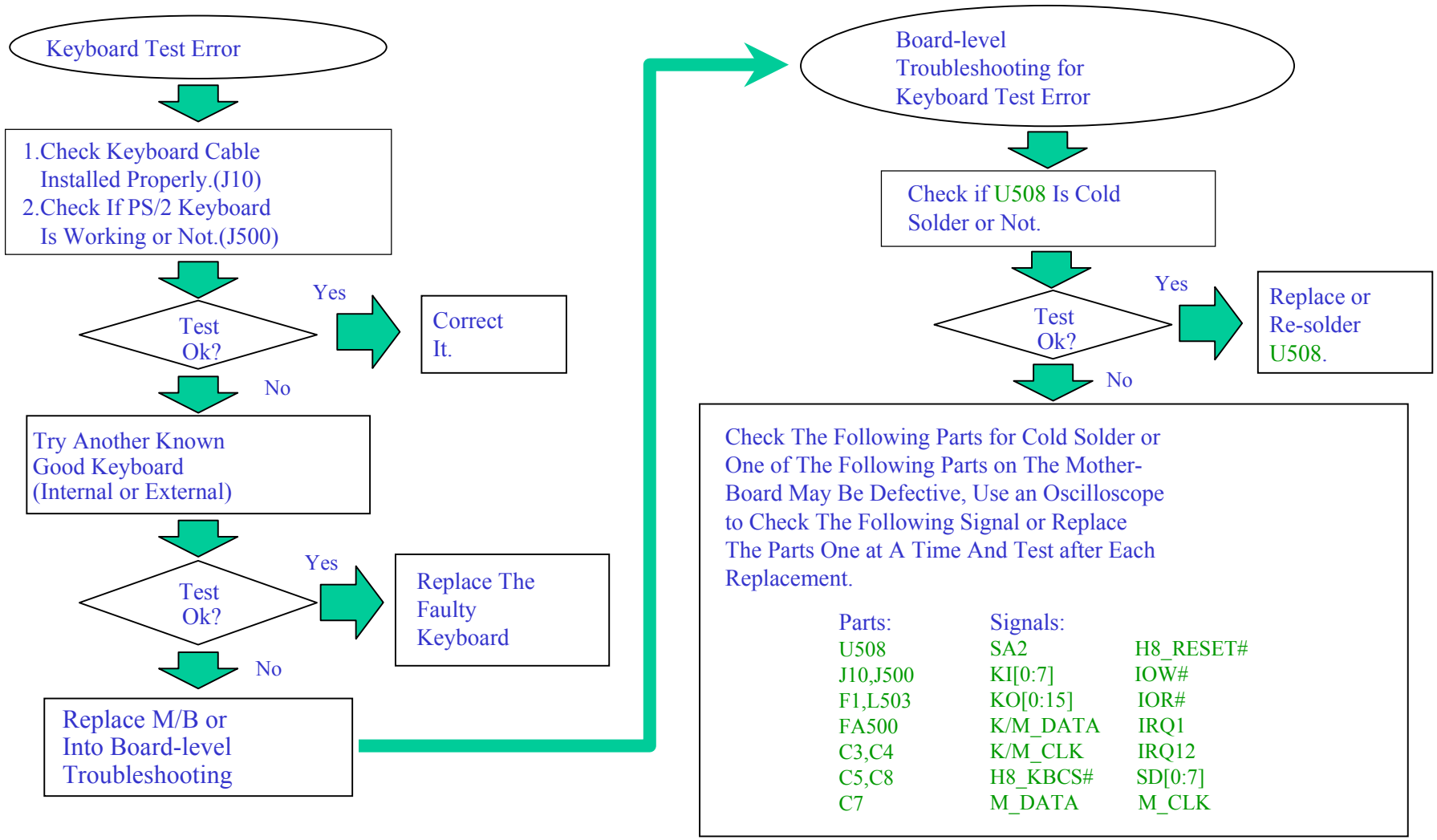
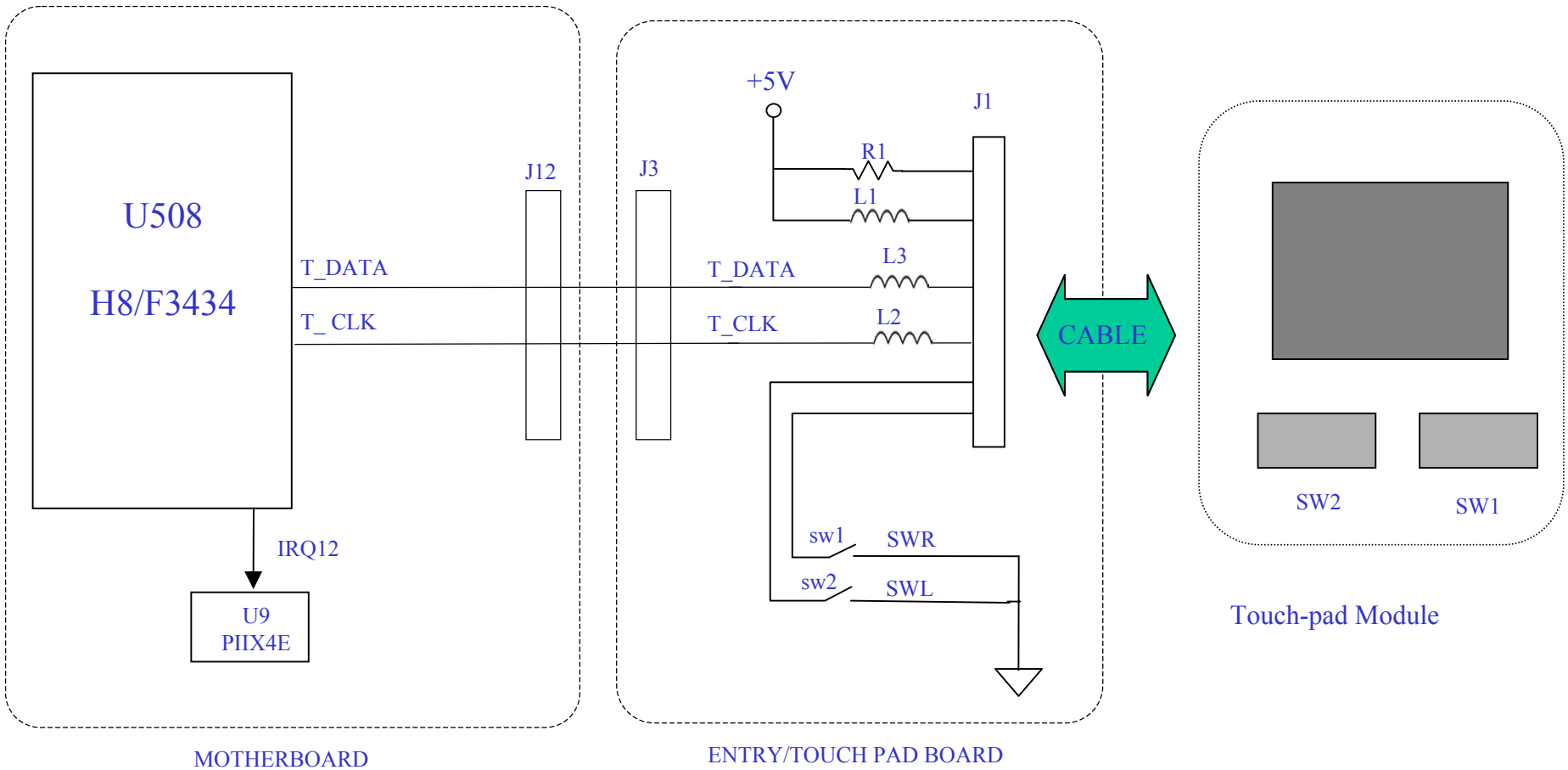


8.8 Track Pad Test Error

An Error Message Is Shown When Touch-pad Is Enabled.



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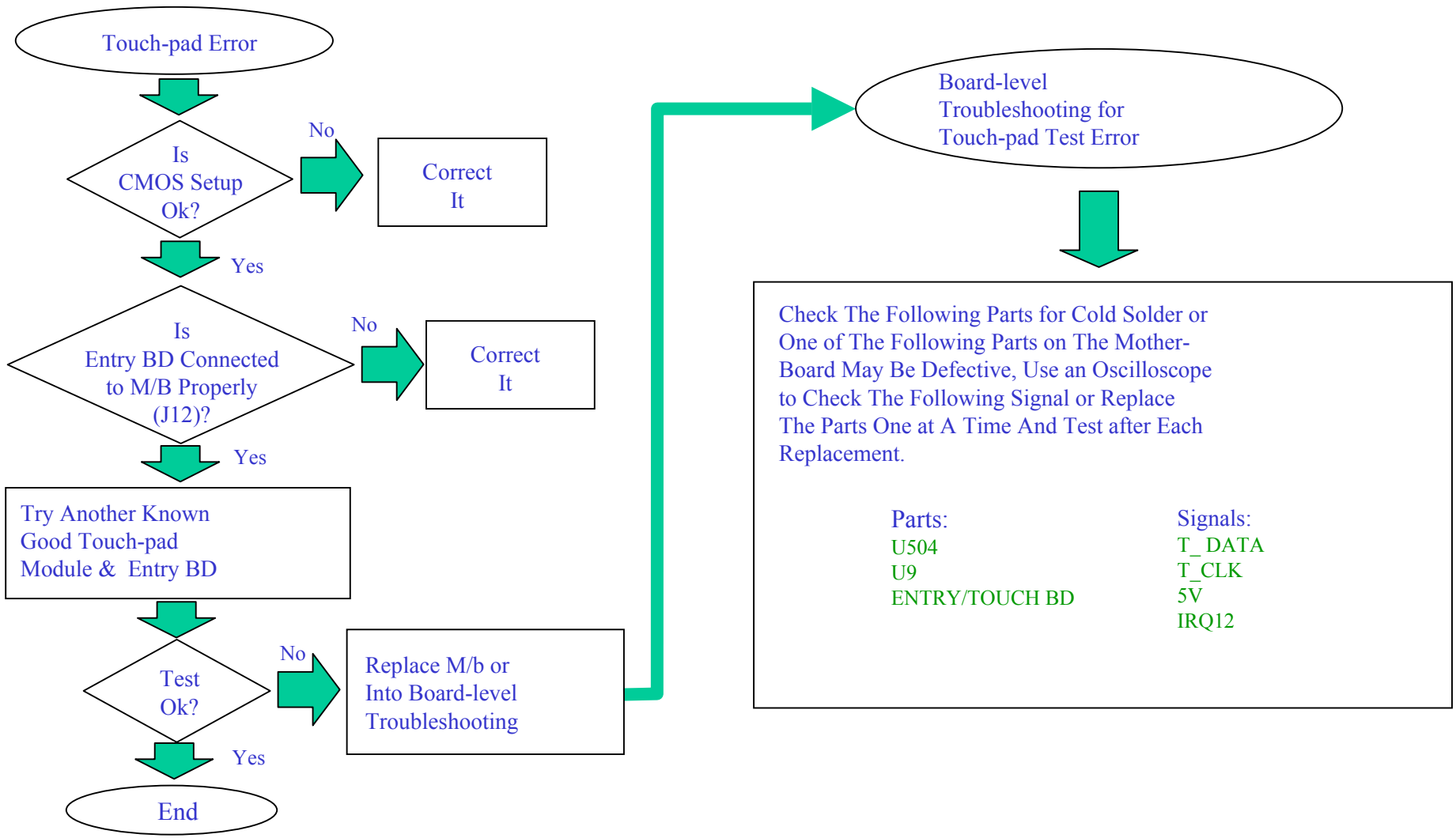
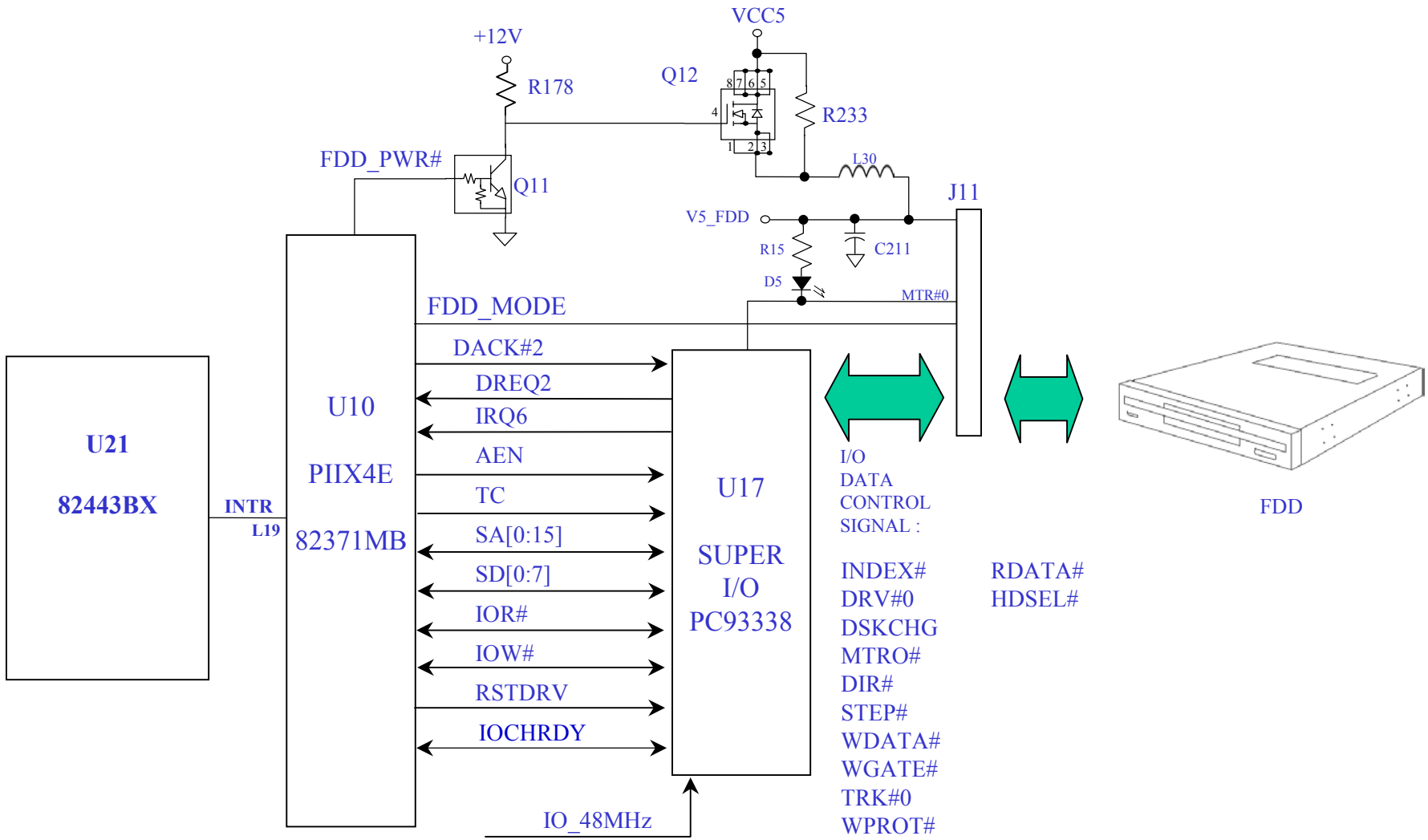


8.9 Diskette Drive Test Error

An Error Message Is Shown When Reading/ Writing Data from/to Diskette Drive.



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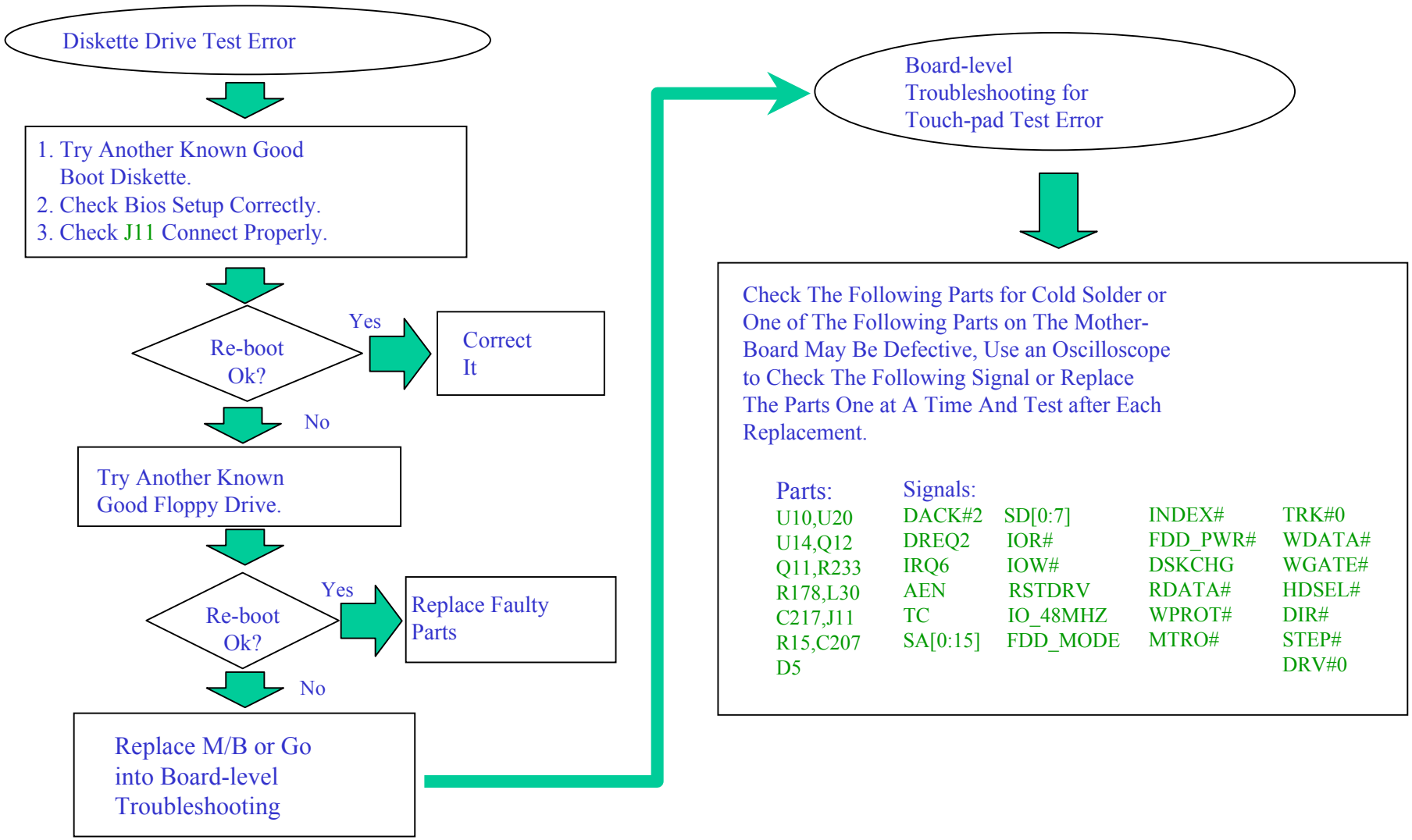
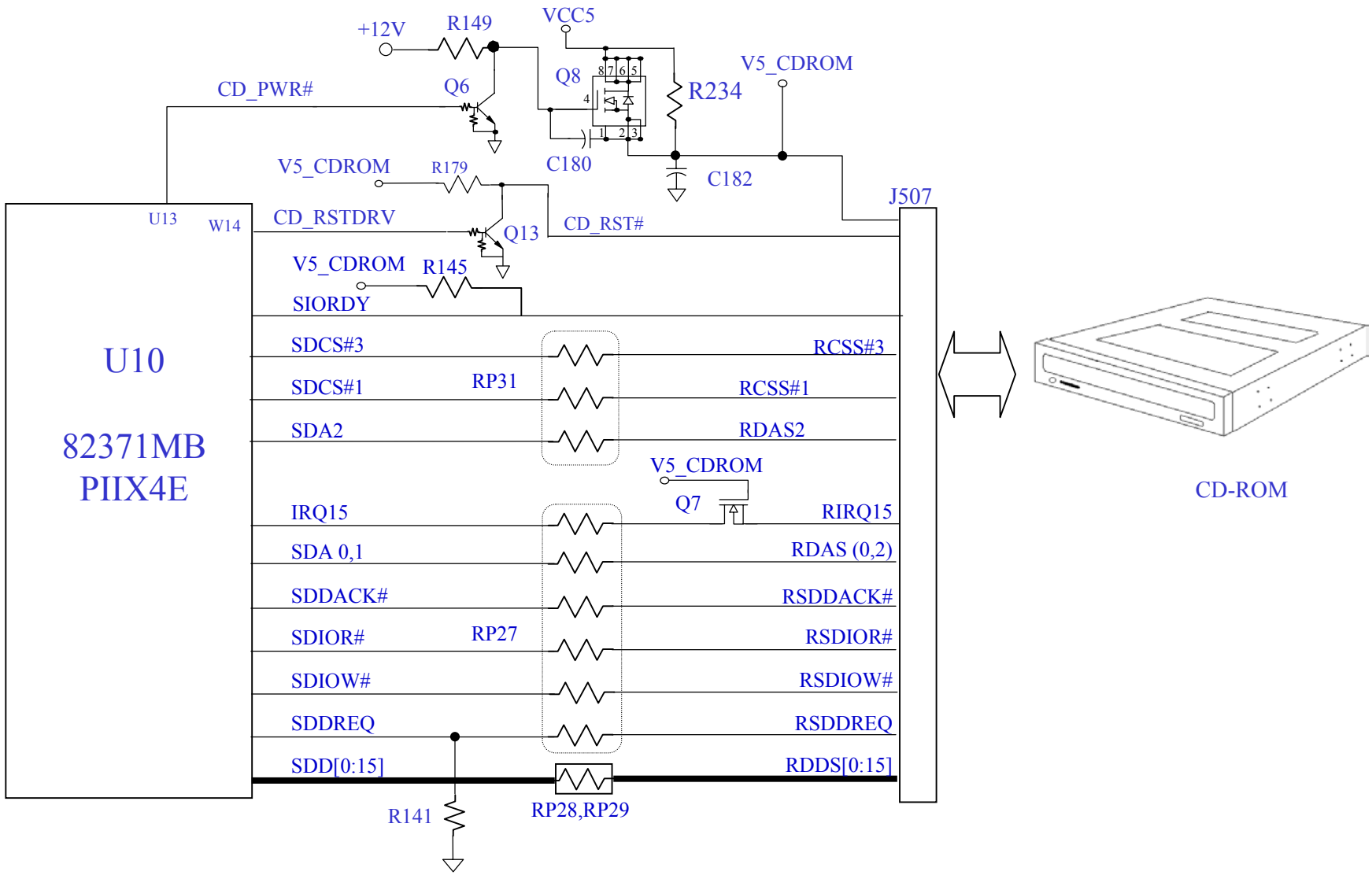
An Error Message Is Shown When Reading/ Writing Data from/to Diskette Drive.



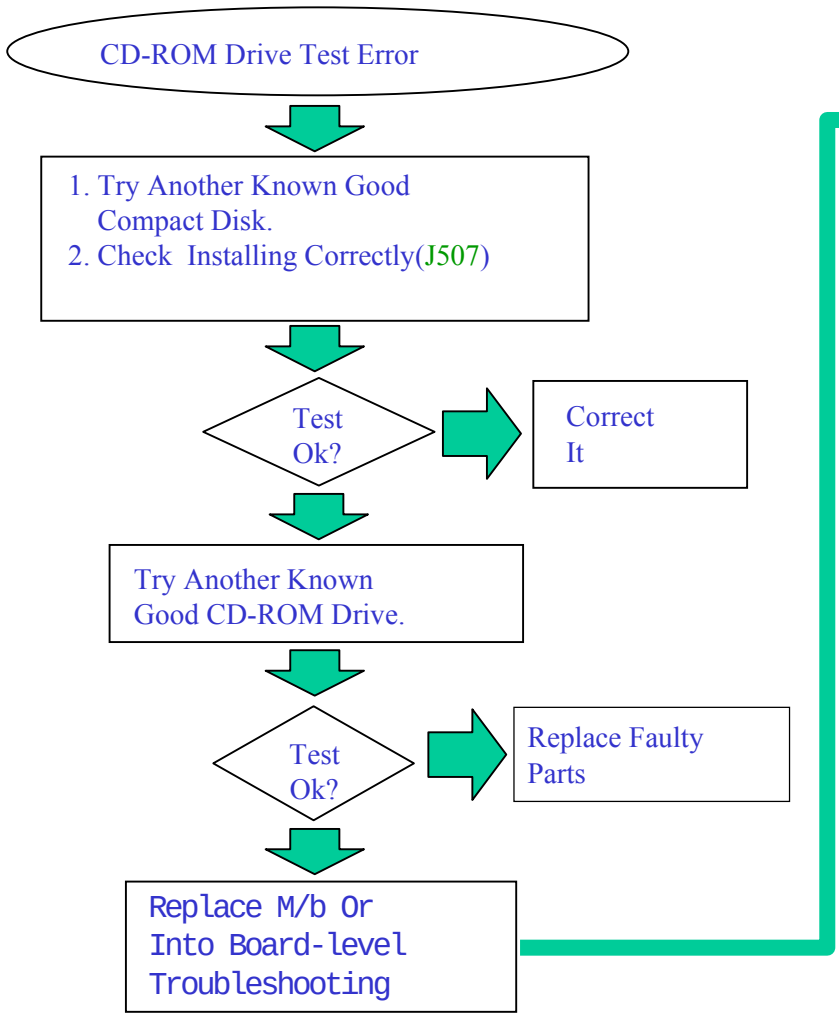
8.10 CD-ROM Drive Test Error

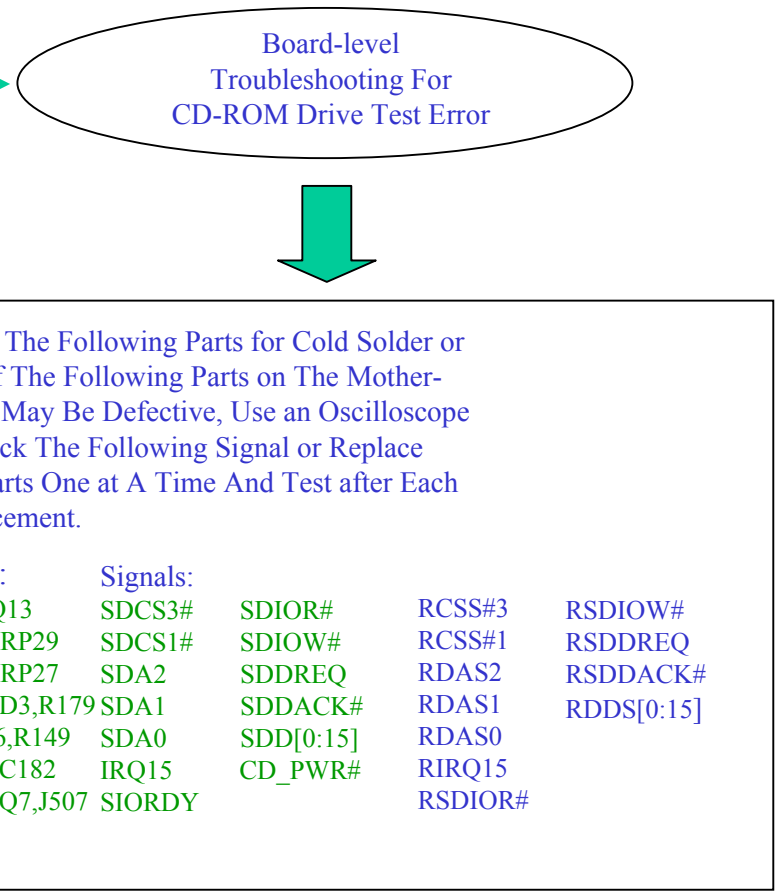
An Error Message Is Shown When Reading Data From CD-ROM Drive.



8.10 CD-ROM Drive Test Error

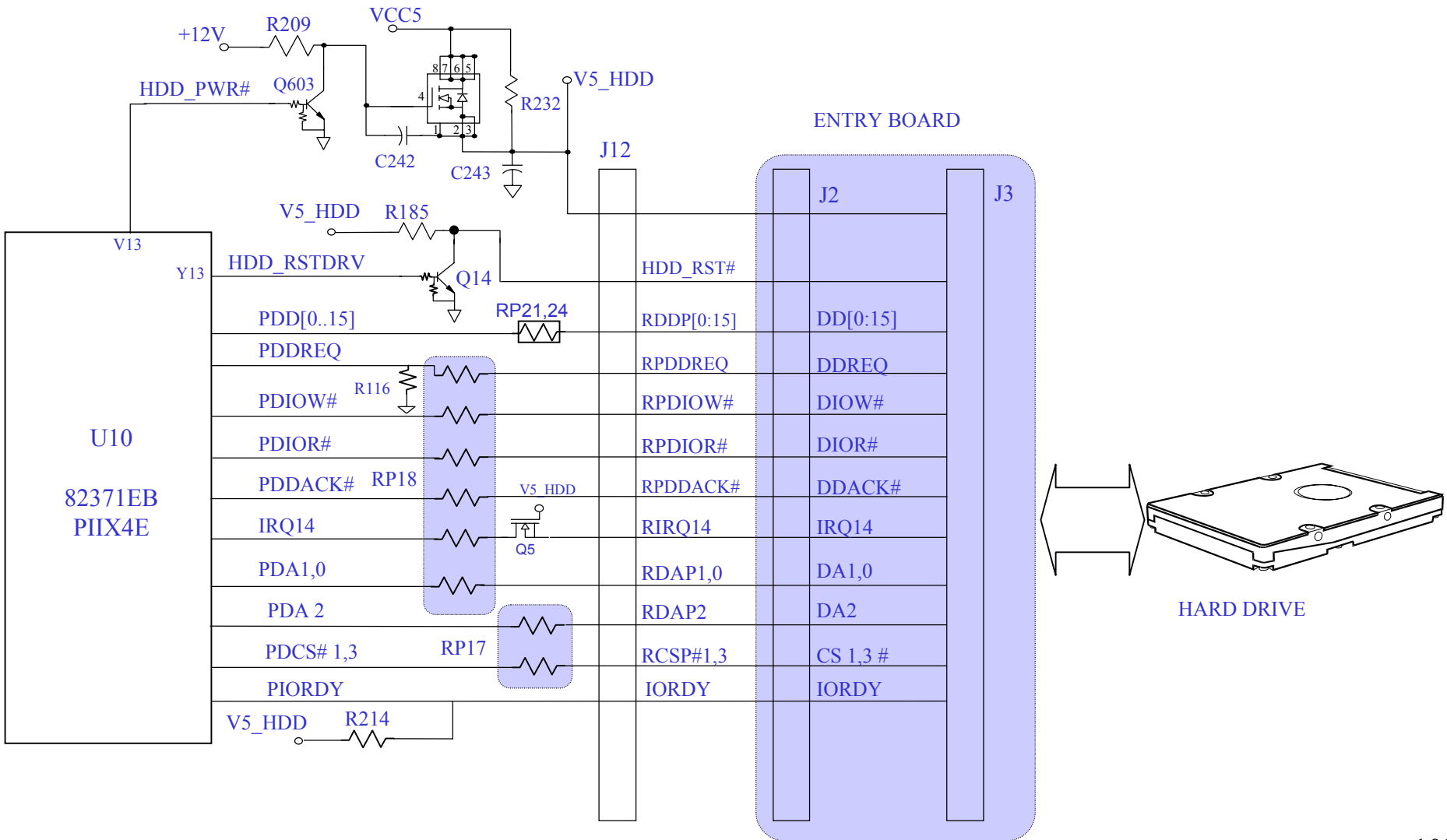
An Error Message Is Shown When Reading Data From CD-ROM Drive.





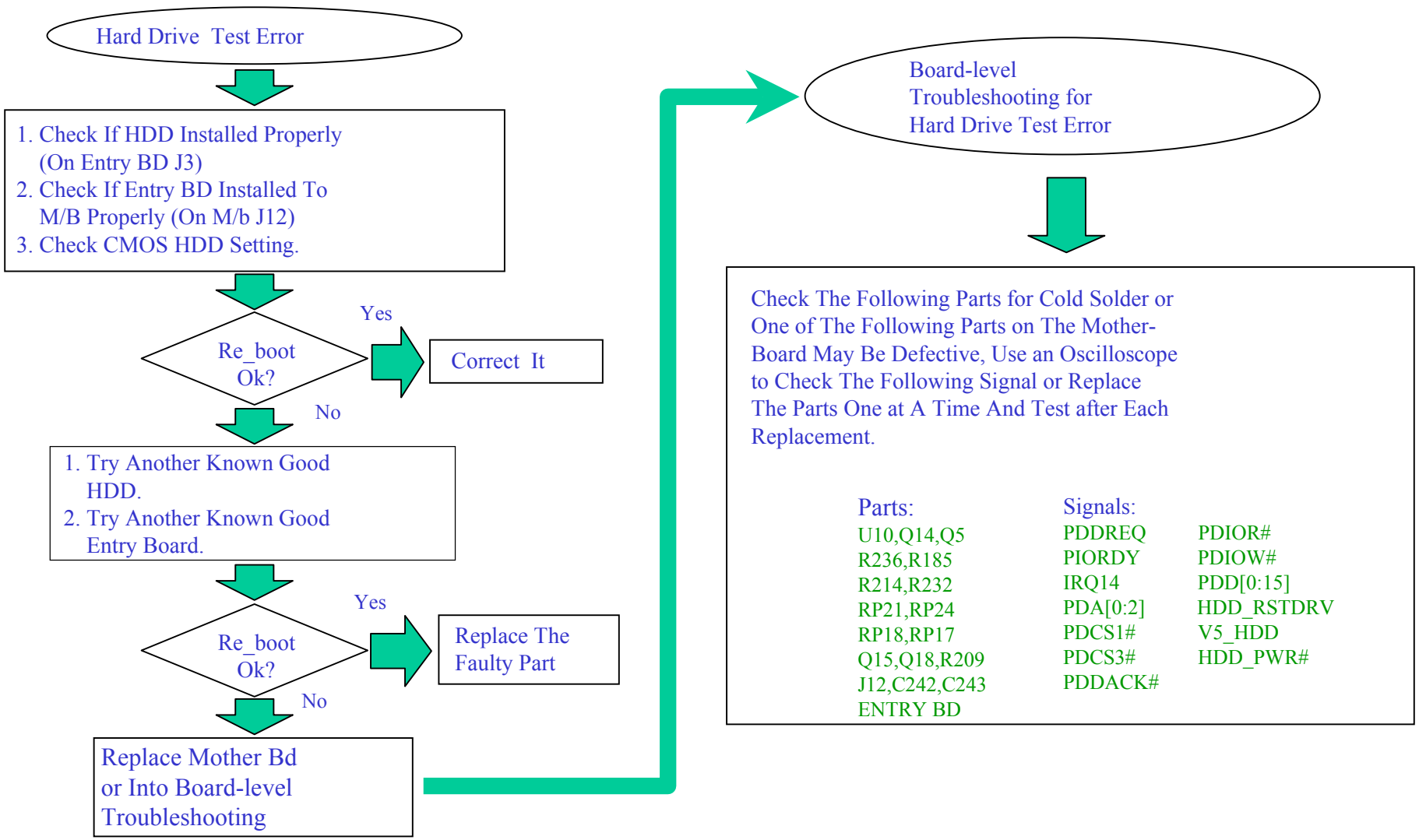
8.11 Hard Drive Test Error

Either an Error Message Is Shown , or The Driver Motor Continues Spinning , While Reading Data Is from/or Writing Data Is to Hard Drive.



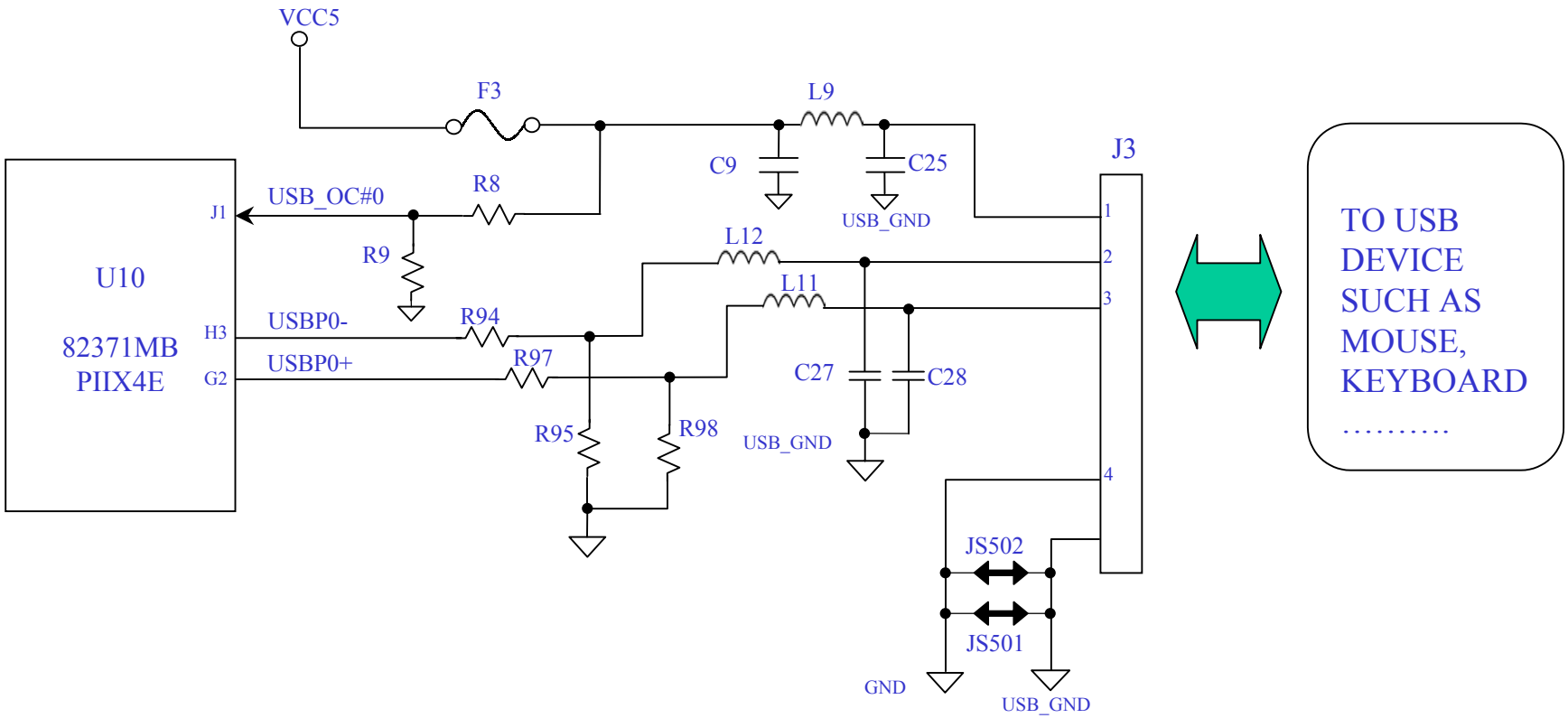
8.11 Hard Drive Test Error

Either An Error Message Is Shown , or The Driver Motor Continues Spinning , While Reading Data Is from \or Writing Data Is to Hard Drive.



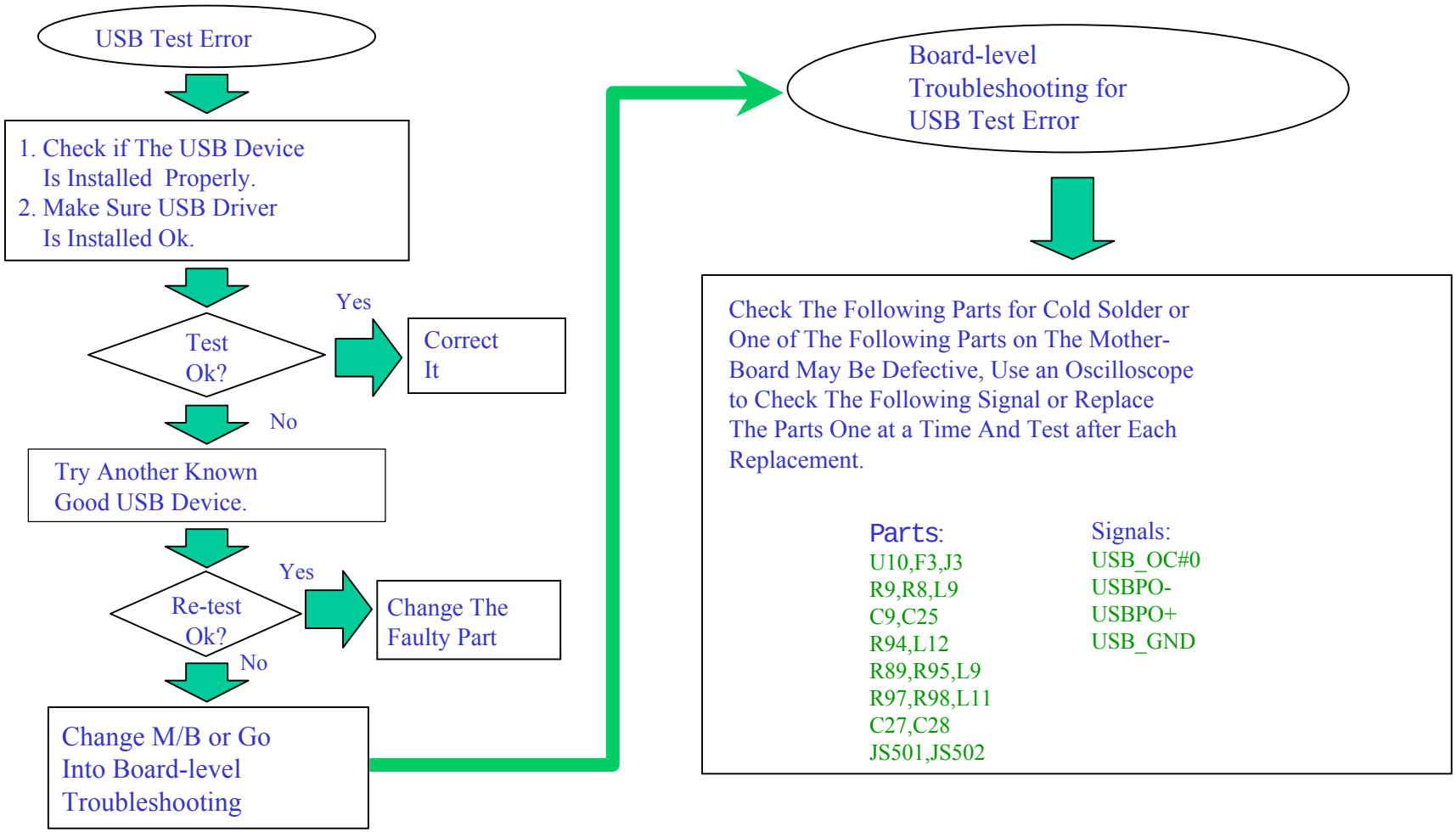
8.12 USB Port Test Error

An Error Occurs When a USB I/O Device Is Installed.



8.12 USB Port Test Error

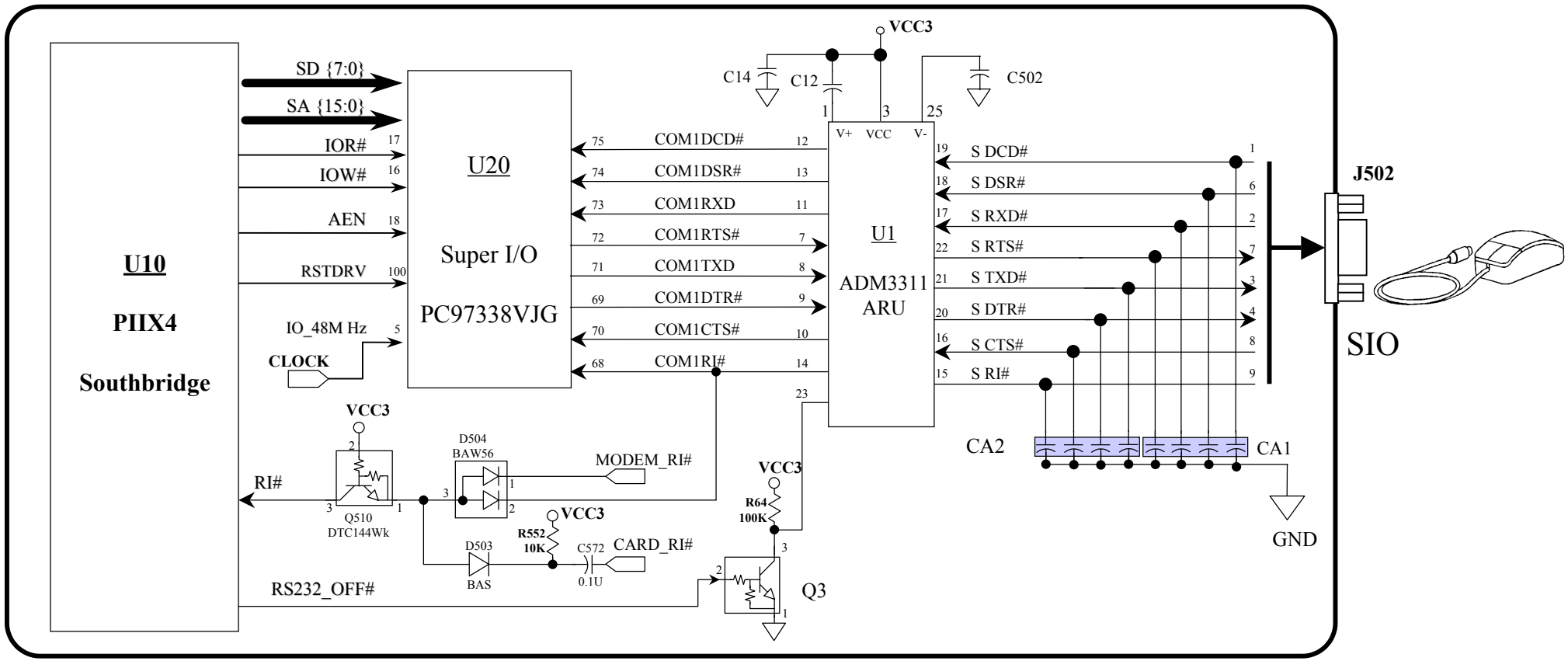
An Error Occurs When A USB I/O Device Is Installed.



8.13 SIO PORT TEST ERROR

Symptom :

An error message occurs when a mouse or other I/O device is installed.



PIN DEFINITION OF SIO PORT:

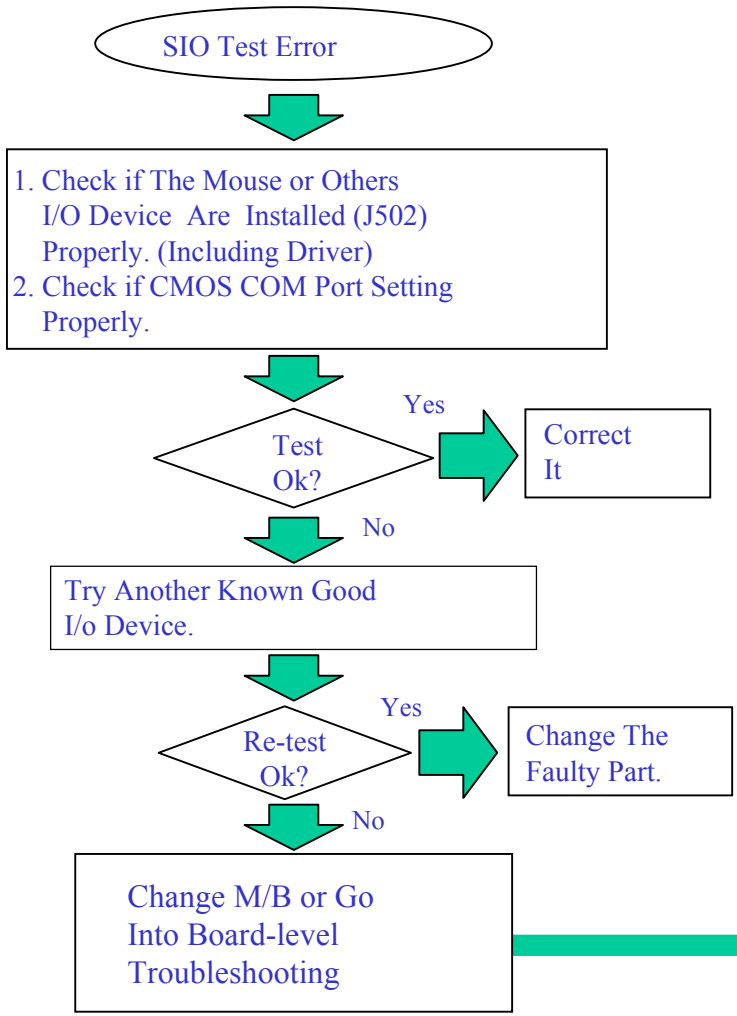
PIN 1 :	DCD-----	Data Carrier Detect	I	PIN 6 :	DSR------	Data Set Ready	I
PIN 2 :	RD-------	Receive Data	I	PIN 7 :	RTS------	Request To Send	O
PIN 3 :	TD-------	Transmit Data	O	PIN 8 :	CTS------	Clear To Send	I
PIN 4 :	DTR-----	Data Terminal Ready	O	PIN 9 :	RI--------	Ring Indicator	I
PIN 5 :	SG--------	Signal Ground	GND				

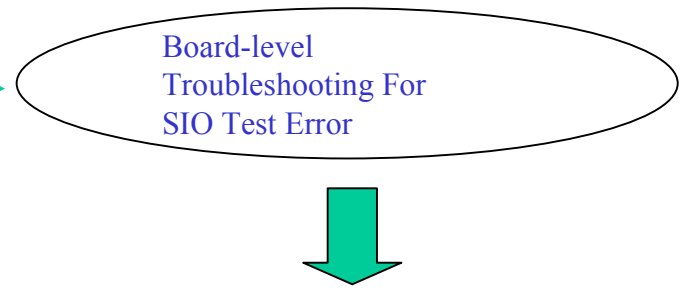
LOOPBACK CONNECTOR FOR SIO TEST:

PIN	1, 4, 6	Short
PIN	2, 3	Short
PIN	7, 8, 9	Short

8.13 SIO Port Test Error

An Error Occurs When a Mouse or Other I/O Device Is Installed.





Check The Following Parts for Cold Solder or One of The Following Parts on The Mother-Board May Be Defective, Use an Oscilloscope to Check The Following Signal or Replace The Parts One at a Time And Test after Each Replacement.

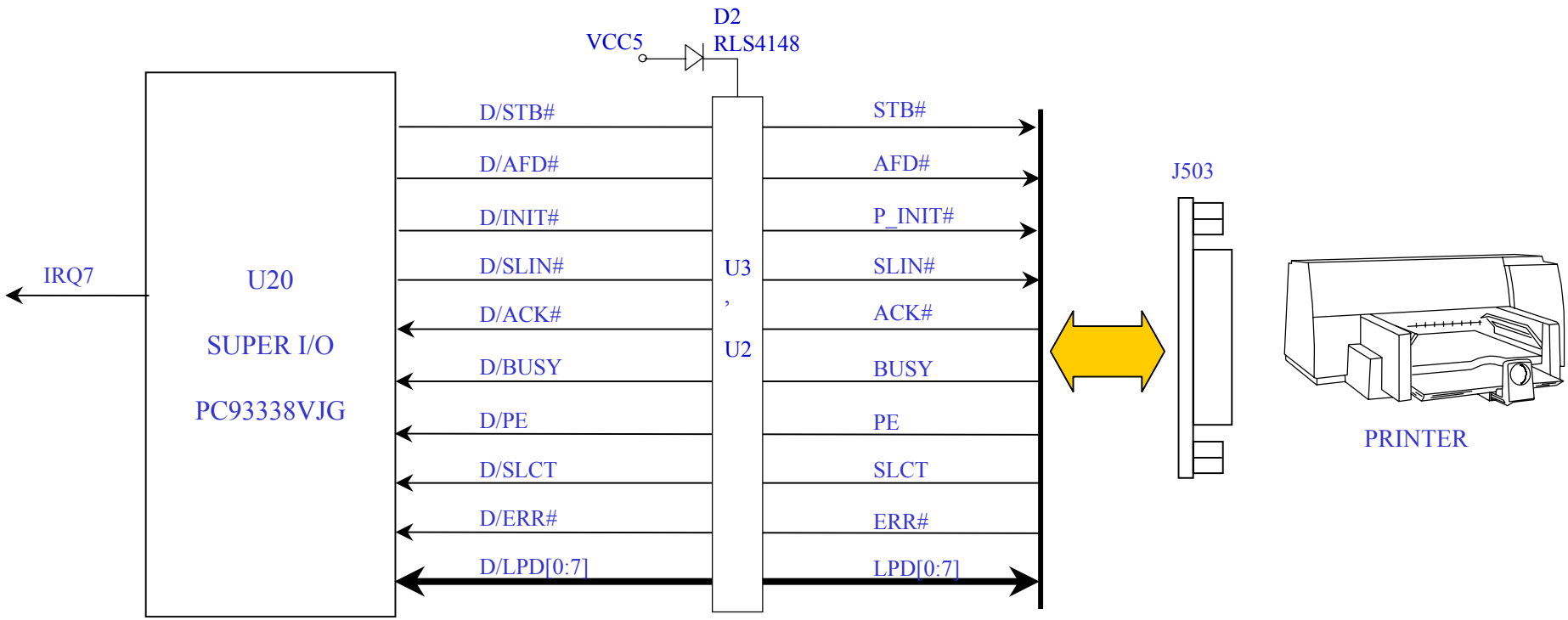
Parts:
U20,U1,U10
Q3,Q510,D503
D504,R64,CA2
CA1,C12,C14,
C502,C503,J502
C501,C13,C572
R552

Signals:

IRQ4	COM1DSR#	S_TXD
RS232_OFF#	COM1RI#	S_RXD
COM1RTS#	S_RTS#	
COM1TXD	S_DTR#	
COM1DTR#	S_DSR#	
COM1CTS#	S_CTS#	
COM1RXD	S_RI#	
COM1DCD#	S_DCD#	

8.14 PIO Port Test Error

When a Print Command Is Issued, Printer Prints Nothing or Garbage.



PIN DEFINITION OF PIO PORT

PIN 1	STB	STROBE SIGNAL	PIN 14	AFD	AUTO LINE FEED
PIN 2-9	D0 -D7	PARALLEL PORT DATA BUS D0 TO D7	PIN 15	ERR	ERROR AT PRINTER
PIN 10	ACK	ACKNOW LEDGE HANDSHANK	PIN 16	INIT	INITIATE OUTPUT
PIN 11	BUSY	BUSY SIGNAL	PIN 17	SLIN	PRINTER SELECT
PIN 12	PE	PAPER END	PIN 18-25:		SIGNAL GROUND
PIN 13	SLCT	PRINTER SELECTED			

LOOPBACK CONNECTOR FOR PIO TEST:

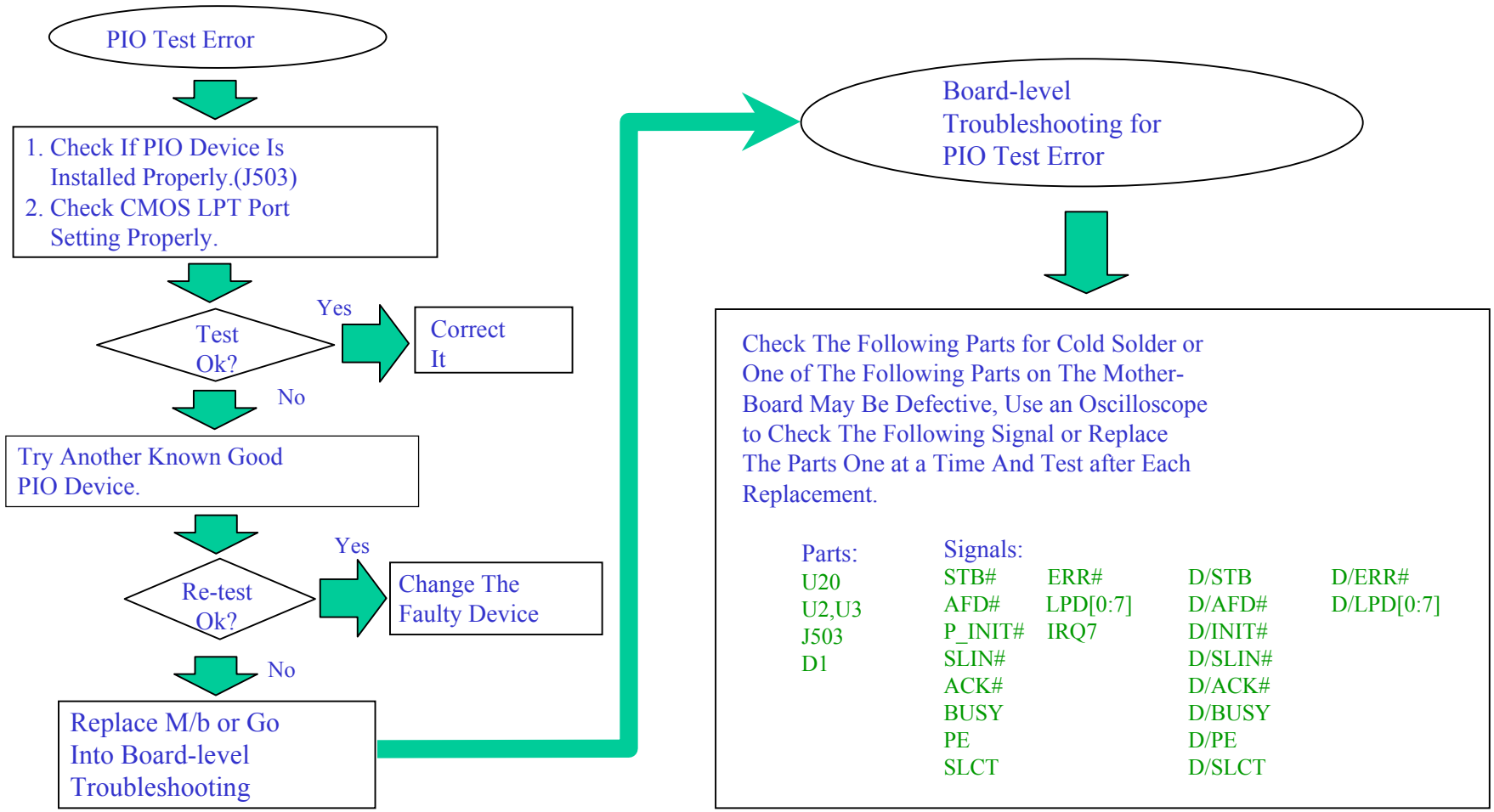
PIN 1,13	SHORT	PIN 10,16	SHORT
PIN 2,15	SHORT	PIN 11,17	SHORT
PIN 12,14	SHORT		

LOOPBACK CONNECTOR FOR EPP TEST:

PIN 1,2,4,6,8	SHORT
PIN 3,5,7,9,16	SHORT
PIN 18,19,20,21,22,23,24,25	SHORT

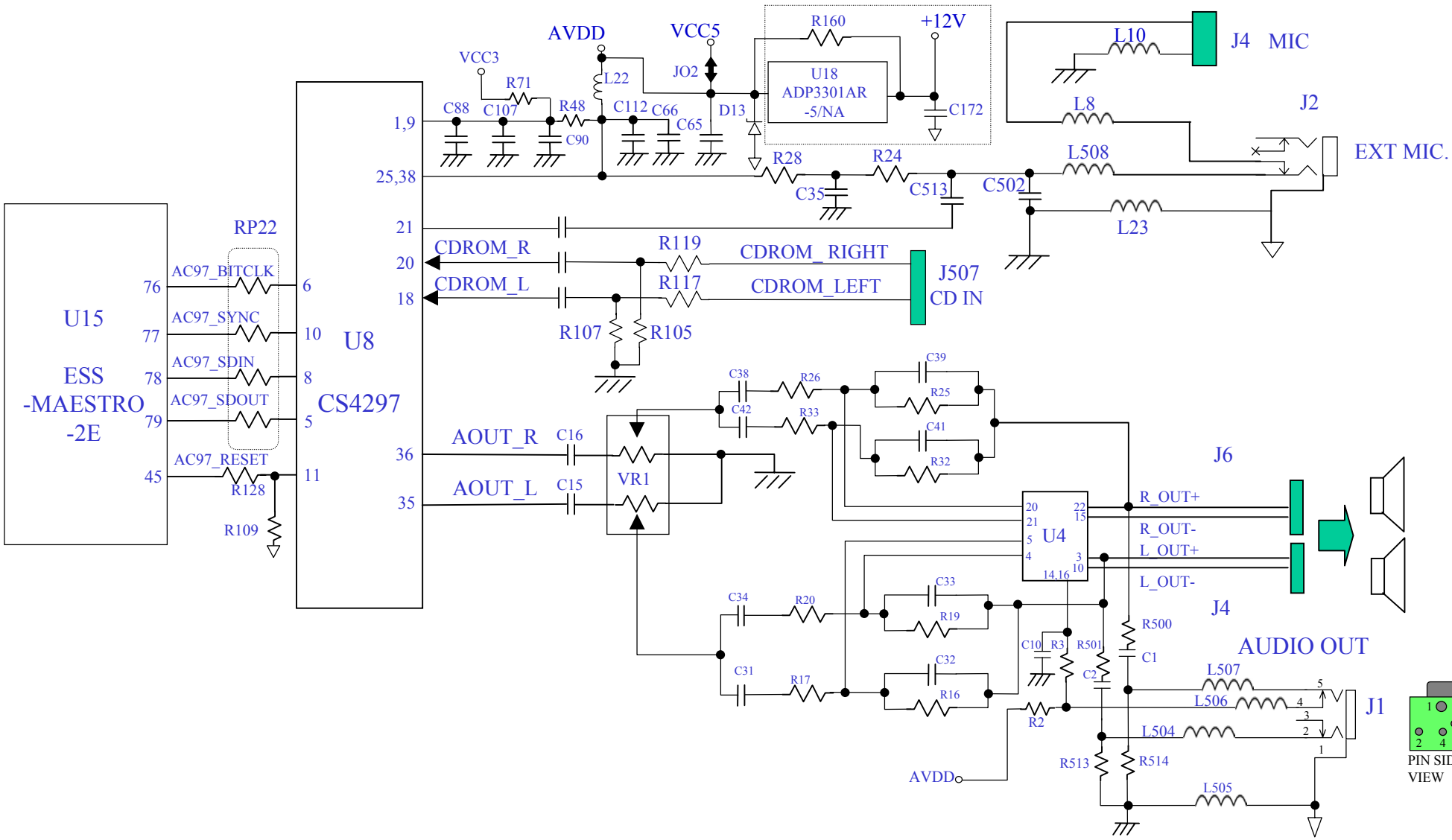
8.14 PIO Port Test Error

When a Print Command Is Issued, Printer Prints Nothing or Garbage.



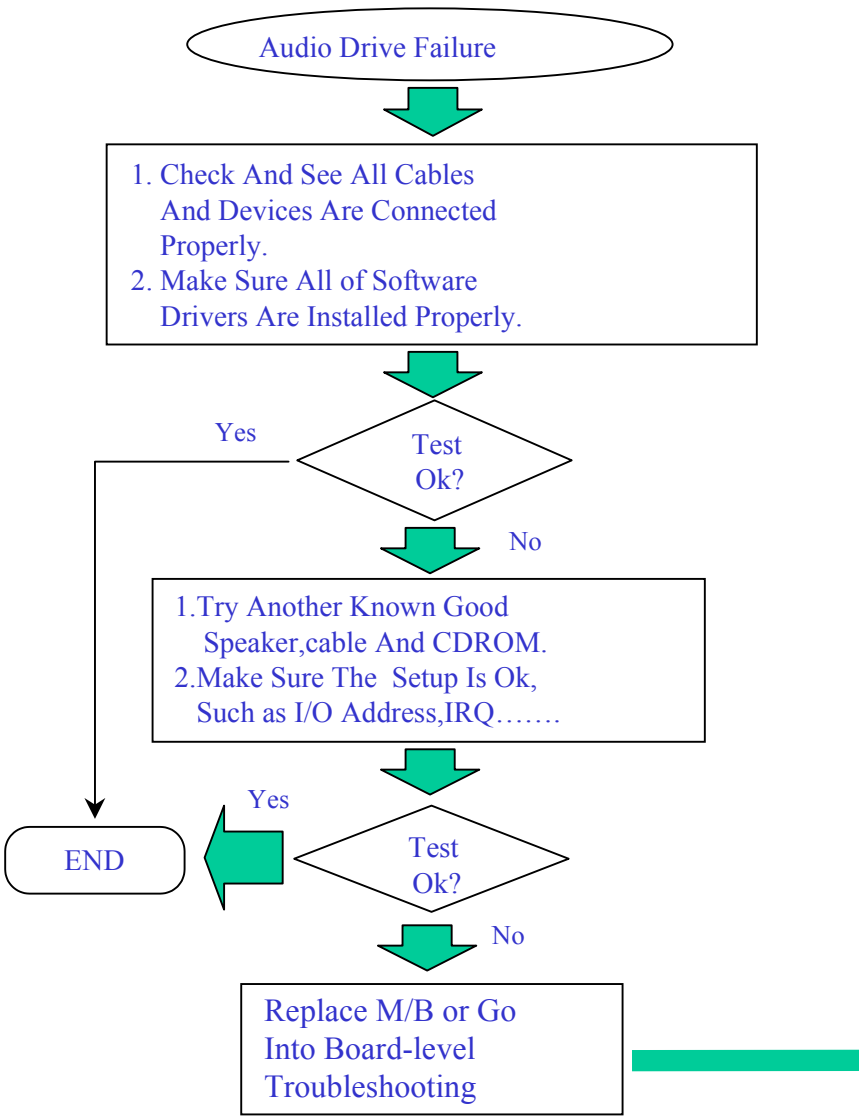
8.15 AUDIO FAILURE

NO SOUND FROM SPEAKER AFTER AUDIO DRIVER IS INSTALLED.



8.15 Audio Failure

No Sound From Speaker After Audio Driver Is Installed.



Board-level Troubleshooting for Audio Test Error

Check The Following Parts for Cold Solder or One of The Following Parts on The Motherboard May Be Defective, Use An Oscilloscope to Check The Following Signal or Replace The Parts One at a Time And Test after Each Replacement.

1.If No Sound Cause of Line Out, Check The Following Parts & Signals:

Parts:	Signals:
U8,U4,U15	AOUT_R
VR1,C16	AOUT_L
C15,C38,C42	HP/LINE
C34,C31,R26	
R33,R20,R17	
R25,R32,R19	
R16,J5,J7,J1	
...	

2.If No Sound CauseOf Mic, Check The Following Parts & Signals:

Parts:	Signals:
U8,U18,L8	MIC1
L10,L508,	
L10,C506	
L509,J4,J2	
…….	

3.If No Sound Cause Of CDROM, Check The Following Parts & Signals:

Parts:	Signals:
U8,R119	CDROM_R
R118,R117	CDROM_L
R105,R106	CD_COMM
R107,C128	
C124,J507	

9. SPARE PARTS LIST-1

Part Number	Description	Location(s)
442999900002	AC ADPT ASSY OPTION;6133	
441600002010	AC ADPT ASSY;PWR-60B,CV/CC-22 MS	
541666810029	ACCESSORY KIT;28-PR,BOX,7233 CTO	
541666810001	ACCESSORY KIT;EN,7233-UTILITY ON	
442665800005	BATT ASSY;12V/4AH,NIMH,TSB,6033,	
340666900008	BEZEL ASSY;CD-ROM,TSB,12A01,6633	
221666140001	BOX;INNER AK,6133	
340666200012	BRACKET ASSY;HDD,NV	
340666200013	BRACKET ASSY;TOUCH PAD,NV	
340666130001	BRKT ASSY;I/O,6133S	
342665500001	BRKT;CD-ROM,5033	
344666710016	BUTTON;T/P,MTC-12A03,6133S	
422600000102	CABLE ASSY;A/D TO CHASSIS,PWR-60	
272075103702	CAP;.01U ,50V,+80-20%,0603,SMT	PC517
272005103401	CAP;.01U ,CR,50V,10%,0805,X7R	PC10
312161002631	CAP;.01U ,PE,100V,5% ,AX	C8
272072473701	CAP;.047U,16V ,+80-20%,0603,Y5V,	C34,42
272072104702	CAP;.1U ,16V,+80-20%,0603,SMT	C1
272072104702	CAP;.1U ,16V,+80-20%,0603,SMT	PC503,515,516
272075104701	CAP;.1U ,50V,+80-20%,0603,SMT	C514,598,602
272072104402	CAP;.1U ,CR,16V,10%,0603,X7R,SM	PC46,47
272003104701	CAP;.1U ,CR,25V ,+80-20%,0805,Y	C218,
272005104701	CAP;.1U ,CR,50V,+80-20%,0805,Y5	C1,9,10,12,17
272072224701	CAP;.22U ,16V ,+80-20%,0603,Y5V,	C513
312263303851	CAP;.33U ,POLY,275V,20%,X2,AX	C6
272002474401	CAP;.47U ,CR,16V ,10%,0805,X7R,S	C596
272075102701	CAP;1000P,50V ,+80-20%,0603,SMT	PC13,523

Part Number	Description	Location(s)
312431001044	CAP;1000P,CR,1KV ,10%,DISK,X7R	C16,20
312431001043	CAP;1000P,CR,1KV ,10%,DISK,Y5P	C5
272075102403	CAP;1000P,CR,50V,10%,0603,X7R,SM	PC22,24,25,37,40
272005102401	CAP;1000P,CR,50V,10%,0805,X7R	C14,18
272075101701	CAP;100P ,50V ,+80-20%,0603,SMT	C3,5,7,8,17,18,21,22
272075100701	CAP;10P ,50V ,+80-20%,0603,SMT	C93,94,95,96,97,98
272021106501	CAP;10U ,10V ,20%,1210,X7R,SMT	PC16,41
272011106701	CAP;10U ,10V,+80-20%,1206,Y5V,S	PC15,
272012106701	CAP;10U ,16V ,+80-20%,1206,Y5U,	PC12,42
272022106701	CAP;10U ,16V,+80-20%,1210,Y5V,S	PC3,6,525
272023106501	CAP;10U ,25V ,20%,1210,Y5U,SMT	PC5,9
272043106501	CAP;10U ,CR,25V ,20%,1812,Y5U,S	PC48
272075122402	CAP;1200P,CR,50V,10%,0603,X7R,SM	PC512
272073152401	CAP;1500P,CR,25V ,10%,0603,X7R,S	PC38
272431157504	CAP;150U ,4V ,20%,7343,POSCAP,SM	C11,52,165,500
272073180401	CAP;18P ,CR,25V ,10%,0603,NPO,S	C87,103,125,173,544
272071105701	CAP;1U ,CR,10V ,80-20%,0603,Y5	PC44
272013105501	CAP;1U ,CR,25V ,+80-20%,1206,S	PC36,43
272002105701	CAP;1U ,CR,16V ,-20+80%,0805,SM	PC17,23,521
272002105701	CAP;1U ,CR,16V ,-20+80%,0805,SM	C15
272002225701	CAP;2.2U ,CR,16V ,+80-20%,0805,Y	C15,16
272012225702	CAP;2.2U ,CR,16V ,+80-20%,1206,Y	C19,151,231,237
272075200302	CAP;20P ,CR,50V ,5% ,0603,SMT	C139,140
272075222701	CAP;2200P,50V ,+80-20%,0603,SMT	C102
272006222401	CAP;2200P,CR,100V,10%,0805,X7R	C2
312262201741	CAP;2200P,POLY,250V,10%,Y1,AX	C23
272005221401	CAP;220P ,CR,50V ,10%,0805,X7R,S	C4

9. SPARE PARTS LIST-2

Part Number	Description	Location(s)
272431227504	CAP;220U ,4V ,20%,7343,POSCAP,SM	PC8,21,26,28,29,502
272075220701	CAP;22P ,50V ,+80-20%,0603,SMT	C621,622
272063226701	CAP;22U ,25V ,+80-20%,2220,Y5U,	PC11
272073330701	CAP;33P ,25V ,+80-20%,0603,SMT	PC18
272075391301	CAP;390P ,CR,50V,5%,0603,NPO,SMT	C120
272012475701	CAP;4.7U ,CR,16V ,+80-20%,1206,Y	C6,101,126,200,240
312434701041	CAP;4700P,CR,1KV ,10%,DISK,Y5P	C22
272075470701	CAP;47P ,50V ,+80-20%,0603,SMT	C2-5
272075470701	CAP;47P ,50V ,+80-20%,0603,SMT	PC31
272005560401	CAP;56P ,CR,50V ,10%,0805,NPO,S	C3
344666710010	CAP;FAX MODEM,MTC-12A01,6133S	
221665820003	CARTON;2 IN 1,6033	
221665720003	CARTON;AC ADAPTER,6020	
221665820001	CARTON;MITAC,6033	
431668100004	CASE KIT;7233,H-R00,12.1	
523466810001	CD ROM DRIVE ASSY;24X,XM-7002B,7	
523499995013	CD ROM DRIVE OPTION;24X,7233	
523400395006	CD ROM DRIVE;24X,XM-7002B,H=12.7	
451668100071	CD ROM ME KIT;24X,XM-7002B,7233	
342665500008	CFM-SUYIN;S-STANDOFF,#4-40H4.8,N	
313000020195	CHOKE COIL;1.3mH(MIN),18.5TS,D.5	T2
313000020190	CHOKE COIL;1.5UH,20%,7.5T,6*8	L1
273000500012	CHOKE COIL;10UH,4.7A,5.7MM,SMT	PL502
313000020191	CHOKE COIL;112UH(MIN),7.5T,2*0.6	T3
313000020192	CHOKE COIL;15mH(MIN),50.5T,D.6	T1
273000500015	CHOKE COIL;50UH(REF),D.4*2,5.5T,	PT500
313000020206	CHOKE;1.3UH,+-20%,4.5TS,D0.6X3,T	PL506

Part Number	Description	Location(s)
313000020148	CHOKE;15UH,D.7*16T/.2*32,55130,T	PT501
313000020153	CHOKE;75uH,20%,D0.6,55130,H=14MM	PL505
331000006002	CON;BATTERY,6P,5MM,GOLD,5010S-06	J509
331720015006	CON;D,FM,15P,2.29,R/A,3ROW	J501
331720025005	CON;D,FM,25P,2.775,R/A	J503
331720009004	CON;D,MA,9P,2.775,R/A	J502
291000151201	CON;FPC/FFC,12P,0.5MM,R/A,SMT	J2
291000152401	CON;FPC/FFC,24P,1MM,R/A,ELCO	J10
291000152602	CON;FPC/FFC,26P,1MM,R/A,SMT,ELCO	J11
291000014801	CON;HDR,FM,24P*2,1.27,ST,SMT	J3
291000016015	CON;HDR,FM,30P*2,.6MM,ST,SMT,613	J504
331040043002	CON;HDR,FM,43P,2MM,R/A,BL4.2,W/O	J1
291000011001	CON;HDR,MA,10P*1,1.25,ST,SMT	J9
291000014003	CON;HDR,MA,20P*2,1.25MM,ST,SMT	J8
291000014802	CON;HDR,MA,24P*2,1.27,ST,H3.58,S	J12
291000020202	CON;HDR,MA,2P*1,1.25,R/A,SMT,HIR	J4
291000014601	CON;HDR,MA,46P,1.27,ST,H1.5,SMT	J507
291000020601	CON;HDR,MA,6P*1,1.25MM,R/A,SMT	J1
331040004011	CON;HDR,SHROUD,4P*1,2,R/A,USB,63	J3
291000251441	CON;IC CARD,FM,72P*2,.6MM,H3MM,S	J506
331870006011	CON;MINI DIN,6P,R/A,W/GROUNDING	J500
331910003003	CON;POWER JACK,3P,16VDC/3A	PJ500
331910002003	CON;PWR PLUG,2P,250V/2.5A,SUPERC	J1
331840005002	CON;STEREO JACK,5P,R/A,D3.6,2 SW	J1,2
291000410201	CON;WFR,MA,2P,1.25,ST,SMT/MB	J5,7
291000410301	CON;WFR,MA,3P,1.25,ST,SMT/MB	J4,505
345665400036	CONDUCTIVE TAPE;TOUCH PAD/166,VE	

9. SPARE PARTS LIST-3

Part Number	Description	Location(s)
340666710005	COVER ASSY;CASE KIT,MTC-A02,6133	
340666710002	COVER ASSY;CPU,MITAC-12A01,6133S	
340666710010	COVER ASSY;LCD-121,MTC-12A02,613	
344665700065	COVER;AC ADAPTER,6020	
344666710009	COVER;FAX MODEM,MITAC-12A01,6133	
344666710014	COVER;L,HINGE,MTC-12A02,6133S	
344666710015	COVER;R,HINGE,MTC-12A02,6133S	
344666900007	COVER;REAR-2,CASE KIT,6633	
272625101401	CP;100P*4,8P,50V ,10%,1206,NPO,S	CA1,2,3,4,5,6,7
272625470401	CP;47P*4 ,8P,50V ,10%,1206,NPO,S	CA8,500,501
345666710004	CUSHION;DOWN,LCD,P-425C,6133S	
345666710003	CUSHION;UPPER,LCD,P-425C,6133S	
291000621445	DIMM SOCKET;144P,.8MM,GOLD,SMT	J508
288100016001	DIODE;BAS16,75V,250MA,SOT-23	D16,503,505
288100032013	DIODE;BAS32L,VRRM75V,MELF,SOD-80	PD7,500,501,502
288100032013	DIODE;BAS32L,VRRM75V,MELF,SOD-80	D3,9
288100701002	DIODE;BAV70LT1,70V,225MW,SOT-23	D500,17
288100099001	DIODE;BAV99,70V,450MA,SOT-23	D501,509
288100056003	DIODE;BAW56,70V,215MA,SOT-23	D12,14,15,504
328100026005	DIODE;BYV26E,FAST,1A,1000V,AX,SO	D8
288100202001	DIODE;DAN202K,80V,SWITCH,SMT	PD503
288101004024	DIODE;EC10QS04,RECT,40V,1A,CHIP,	PD5,6
328101610002	DIODE;F16P10QS,16A,FAST RECOVERY	D1
328100406001	DIODE;PBL406,4A,800V,SIP,4P	D10
288100050001	DIODE;RB050L-40,40V,3A,SMT	PD2,3,504
288104148001	DIODE;RLS4148,200MA,500MW,MELF,S	D2,10,11,18,506
288100024001	DIODE;RLZ2.4B,ZENER,400mW,LL-34	PD8

Part Number	Description	Location(s)
288100024002	DIODE;RLZ24D,ZENER,23.63V,5%,SMT	PD1
288100056001	DIODE;RLZ5.6B,ZENER,5.6V,5%,LL34	PD4
288100016003	DIODE;TZMC16,ZENER,16V,5%,SMT	D4
288100056005	DIODE;UDZ5.6B,ZENER,5.6V,UMD2,SM	D13,502
328114003001	DIODE;UF4003G,200V/1A,PRE./DO-41	D5
344666710004	DOOR;I/O,CASE KIT,MTC-12A01,6133	
344666710005	DOOR;PCMCIA,MITAC-12A01,6133S	
312271006350	EC;100U ,25V,20%,RA,6.3*7,-40~10	PC500,501,508,509
272602107501	EC;100U,16V,M,6.3*5.5,-55+85'C,S	C1,2,9
312271006359	EC;100U,25V,M,D6.3,RA,-40~105',L	C13
312271206951	EC;120U ,400V,20%,RA,D35,-25'~10	C53
312272206152	EC;220U ,4V ,M,RA,D8*5,OS-CON	PC519,524
312273306151	EC;330U ,6.3V,20%,RA,D10,W/OS-CO	PC504,507,526
312274706354	EC;470U ,25V ,20%,RA,D10,-20'~10	C7,C19,C11
227666700001	END CAP;6133S	
227666100003	END CAP;KEYBOARD,6133	
227666100001	END CAP;MIDDLE,AK,6133	
227665700007	END CAP;TOP/BTM,AC ADAPTER,6020	
227666700002	END CAP;TOP/BTM,AK,6133S	
481668100003	F/W ASSY;KBD CTRL,7233	U508
481668100002	F/W ASSY;SYS/VGA BIOS,7233	U27
422665400003	FCC ASSY;CONDUCTION TAPE,VENUS	
523411442008	FD DRIVE;1.44M,3 MODE,D353G	
523466623051	FDD ASSY;1.44M,3.5",W/HD 9.5MM,U	
273000150002	FERRIET CHIP;120OHM/100MHZ,2012,	L26,29,33,34,514,516
273000610008	FERRITE ARRAY;120OHM/100MHZ,TKIN	FA1,2,3,4,5,500

9. SPARE PARTS LIST-4

Part Number	Description	Location(s)
273000130001	FERRITE CHIP;120OHM/100MHZ,1608,	L2,L3
273000130001	FERRITE CHIP;120OHM/100MHZ,1608,	L1,2,11,12,500,501,
273000130019	FERRITE CHIP;120OHM/100MHZ,1608,	L13,18,20,21,22,510
273000150013	FERRITE CHIP;120OHM/100MHZ,2012,	L5,28,35,36
273000150009	FERRITE CHIP;30OHM/100MHZ,2012,S	L6,7,9,16,24,503
273000130006	FERRITE CHIP;600OHM/100MHZ,.2A,1	L3,4,8,10,15,17,504,
273000130002	FERRITE CHIP;80OHM/100MHZ,1608,S	L14,19,511,512,513
313000150019	FERRITE CORE;25OHM/100MHZ,D3	L2
313000150020	FERRITE CORE;25OM100MZ,CORE ONLY	
422666200001	FFC ASSY;TOUCH PAD,CASE KIT,NV	
346600000025	FILM;300MM*500M,PE	
341665500003	FINGER;HEATSINK,5033	
288003600001	FIR;HSDL3600#007,FRONT VIEW,10P,	U504
361200002001	FLUX;3961-E,LOW SOLIDS,NO CLEAN	
421665800032	FPC ASSY;2ND,CD-ROM,EMI,6033	
295000010008	FUSE;1.1A,POLY SWITCH,1812,SMT	F1,3
295000010105	FUSE;1A,NORMAL,1206,SMT	F4
295000010102	FUSE;FAST,3A,32V,1206,SMT,CERAMI	F2
335152000031	FUSE;LAG,4A ,HIBREAK,5*20MM	F1
295000010016	FUSE;NORMAL,6.5A/32VDC,3216,SMT	PF500
295000010020	FUSE;NORMAL,7A/24VDC,1206,SMT	F5
345666700003	GASKET;345665400029,6133S	
345666200012	GASKET;AUDIO-JACK,NV	
345665400032	GASKET;FDD/166,VENUS	
345666200021	GASKET;LCD,HOUSING,5X1.5X10,NV	
345666700006	GASKET;M/B-VR,GTU-5-2-15,6133S	
345665400013	GASKET;USB,VENUS	

Part Number	Description	Location(s)
344600000296	GRAIN;PPO.94V-1,BLACK,PRC	
344600000296	GRAIN;PPO.94V-1,BLACK,PRC	
451666230031	HDD ME KIT;3.2GB,VENUS-U26	
340666900001	HEATSINK ASSY;CPU,6633	
342665700040	HEATSINK;L,AC ADAPTER,6020	HS1
342665700041	HEATSINK;R,AC ADAPTER,6020	HS2
340666200002	HINGE;L,12.1",NV	
340666200001	HINGE;R,12.1",NV	
341666200004	HOLDER;T/P,NV	
344666710025	HOOK;LCD,PANTONE 425C,6133S	
340666710001	HOUSING ASSY;CASE KIT,M-12A01,61	
340666810007	HOUSING ASSY;LCD,SJ03,MTC-A01,62	
451668100032	HOUSING KIT;7233,H-R00	
451600001001	HOUSING KIT;AC 60B	
344665700066	HOUSING;AC ADAPTER,6020	
344600000225	IC CARD CON PART;72P*2,6033	
331650049502	IC SOCKET;495P,ZIF,ZIFuPGA2,FOXC	U501
284500003007	IC;3D RAGE LT PRO,AGP,BGA,328P,J	U13
282574014004	IC;74AHC14,HEX INVERTER,TSSOP,14	U24
282674008001	IC;74AHCT08,2I/P AND GATE,TSSOP,	U509
282074338402	IC;74CBTD3384,10 BIT BUS SW,TSOP	U36
282574164002	IC;74VHC164,SIPO REGISTER,TSSOP,	U35
284501021002	IC;ADM1021,TEMPERATURE MTR,SSOP	U7
286203311001	IC;ADM3311E,RS-232,TSSOP,28P	U1
286300809003	IC;ADM809M,RESET CIRCUIT,4.38V,S	U37
286303410001	IC;ADP3410,PWM,BOOTSTRAP/W,TSSO	PU1
286303421001	IC;ADP3421,GEYSERVILLE CTRL,TSSO	PU5

9. SPARE PARTS LIST-5

Part Number	Description	Location(s)
286300431016	IC;AME431ACFT,1%,ADJ REG,SOT89	Q4
284501918002	IC;ES1918-J,AC 97 CODEC,TQFP,48P	U8
284501978001	IC;ES1978S,AUDIO CHIP,TQFP,100P	U15
283420502004	IC;FLASH,256K*8-15,PLCC,32P,VENU	
284182371005	IC;FW82371EB,PIIX4E,PCI/ISA,BGA3	U10
284582443010	IC;FW82443BX,HOST BRIDG,BGA492,6	U21
284583434001	IC;H8/F3434,KBD CTLR,TQFP,100P	
286317812001	IC;HA178L12UA,VOLT REGULATOR,SC-	PU3
286100358012	IC;LM358,DUAL OP/AMP,SO 8P	U3
286100393004	IC;LMV393,DUAL COMPARTOR,SSOP,8P	PU6,7
286302951015	IC;LP2951ACM,VOLTAGE REGULATOR,S	U33
286300809002	IC;MAX809S,RESET CIRCUIT,2.9V,SO	U34
284501284001	IC;PAC1284-01Q,TERMIN. NETWK,QSO	U2,3
284597338001	IC;PC97338VJG,SUPER I/O,TQFP,100	U20
284501225001	IC;PCI1225PDV,PCI/CARDBUS,LQFP,2	U28
284565837001	IC;PD65837GA-Y03,GCL,TQFP,48P	U14
282153257001	IC;PI5C3257,BUS SWITCH QUAD,QSOP	U9
286303052001	IC;SB3052P,PWM CTRL,SSOP,28P	PU504
286300431011	IC;SC431CSK-.5,.5%,ADJ REG,SOT23	PQ4
286300431010	IC;SC431CSK-1,1%,ADJ REG,SOT23	PQ10
286300431014	IC;SC431LCSK-.5,.5%,ADJ REG,SOT2	PQ6
283766680001	IC;SDRAM,4M*16,TSOP,54P,6233	U16,22,25,30
283866680001	IC;SGRAM,512K*32-100,TQFP,100P,6	U12,19
286300594001	IC;TL594C,PWM CONTROL,SO,16P	PU4
286100202001	IC;TPA0202,AUDIO AMP,2W,TSSOP,24	U4
286302206001	IC;TPS2206,CARDBUS PWR CTLR,SSOP	U32
286303843002	IC;UC3843BD,PWM CTLR,SO,8P,SMT	U2

Part Number	Description	Location(s)
286500137001	IC;W137,CLOCK GENERATOR,SSOP,28P	U11
284104011001	IC;W40S11-02,SDRAM BUFFER,SSOP,2	U29
273000990012	INDUCTOR;10UH,CDRH127,SUMIDA,SMT	PL501
346665700033	INSULATOR;A/D,23MM,MAD-60B,6020	
346665700034	INSULATOR;A/D,65MM,MAD-60B,6020	
346666200007	INSULATOR;AUDIO-JACK,NV	
346665800011	INSULATOR;BATTERY,6033	
346666200010	INSULATOR;HDD CONNECTOR,NV	
346665400009	INSULATOR;I/O PANEL,VENUS	
346666200002	INSULATOR;INVERTER-121,NV	
346665400037	INSULATOR;PCMCIA/200,VENUS	
346665400025	INSULATOR;SW BD CON.,VENUS	
346666200004	INSULATOR;T/P SWITCH BD,NV	
451668100001	LABEL KIT;7233,N-B	
242600000380	LABEL;10*8MM,BIOS,HI-TEMP 260	
242600000380	LABEL;10*8MM,BIOS,HI-TEMP 260	
242662300009	LABEL;25*10MM,3020F	
242662300009	LABEL;25*10MM,3020F	
242600000378	LABEL;27*7MM,HI-TEMP 260'C	
242600000378	LABEL;27*7MM,HI-TEMP 260'C	
242665700017	LABEL;AGENCY,ADPT-22,6020	
242668100001	LABEL;AGENCY-GLOBAL,7233	
242600000088	LABEL;BAR CODE,125*65,COMMON	
242690500078	LABEL;BAR CODE,32*16MM,MD4	
242690500078	LABEL;BAR CODE,32*16MM,MD4	
242600000003	LABEL;BAR CODE,NEW,COMMON	
242600000364	LABEL;BLANK,6*6MM,HI-TEMP	

9. SPARE PARTS LIST-6

Part Number	Description	Location(s)
242600000364	LABEL;BLANK,6*6MM,HI-TEMP	
242600020904	LABEL;BLANK,PAPER 25.4*12.7	
242664800013	LABEL;CAUTION,INVERT BD,PITCHING	
242600000099	LABEL;MODEL,5M,MITAC	
242600000001	LABEL;PAL,20*5MM,COMMON	
242600000001	LABEL;PAL,20*5MM,COMMON	
242600000170	LABEL;PCMCIA CARD WORKS/95 EN	
242600000195	LABEL;SOFTWARE,INSYDE BIOS-M	
242665600006	LABEL;WINDOWS 98,CARTON,5036	
242665600007	LABEL;WINDOWS 98,LCD COVER,5036	
344666710024	LATCH;LCD,MTC-12A03,6133S	
441666800033	LCD ASSY;MIT-SJ03,TFT,12.1",6233	
451666800033	LCD ME KIT;MIT-SJ03,TFT,12.1",62	
413000020160	LCD;AA121SJ03,TFT,12.1",SVGA	
334212000010	LED HOLDER;ROUND,NYLON,LED-18.5	
294011200001	LED;GRN,H1.5,0805,PG1102W,SMT	D1,2,501,502
294011200001	LED;GRN,H1.5,0805,PG1102W,SMT	D3,4,5,6,7,8
294011200006	LED;RE/GR,H1.5,L3,W2.5,BRPG1201W	D3,503
334112000129	LED;ROUND,D3.2,H4.6MM,P2.54,HI,G	D2
416260001002	MAIN UNIT;AC 60B-22V	
561566810001	MANUAL KIT;EN,7233,NON-BRAND	
561566810002	MANUAL;USER'S,EN,7233,NON-BRAND	
421666200031	MICROPHONE ASSY;LCD,NV	3-11-99
344665700053	NAMEPLATE;N-B,6020	
416266810901	NB PLATFORM OPTION;TFT,12.1",723	
416266810005	NB PLATFORM;MIT-SJ03,TFT,12.1",7	
526266810039	NBX;7233/T2XA/XXA/7XX3/N1ENM	

Part Number	Description	Location(s)
328001103001	OPTOCOUPLE;TCET1103,60mA,4P	U1
461600001001	PACKING KIT;AC-60B	
461667100009	PACKING KIT;MITAC,2IN1,6133SX CT	
221665750002	PARTITION;AC ADAPTER,25 IN 1,602	
221666150001	PARTITION;AC ADAPTOR,6133	
412219300024	PCB ASSY;D/A BD,ONLY MTB,12.1,61	
412155600015	PCB ASSY;MDM,56K,SOFT,US,6133	
412155600025	PCB ASSY;MDM,56K,W/O SOFT,6233	
316666200003	PCB;PWA-5033S/LED BD	
316666200002	PCB;PWA-5033S/TOUCH PAD BD	R03
316665700013	PCB;PWA-6020/MAD-60B BD	R01
316665700014	PCB;PWA-6020/MAD-60BI BD	R01
316668100002	PCB;PWA-7233,MOTHER BD,H-R00	R01
222663920008	PE BAG;150*200,FRU,LP486	
222664720001	PE BAG;310*450,T.08,RECY.,5026VO	
222600020049	PE BAG;50*70MM,W/SEAL,COMMON	
222666720001	PE BAG;LCD ASSY,13",6133S	
222665720003	PE BAG;W130*L250,6020	
222665720001	PE BUBBLE BAG;ADAPTOR,6020	
340668100003	PLATE ASSY;SUPPORT,CPU,7233	
411666700007	PWA;PWA-6133S,T/P SW BD	
411668100010	PWA;PWA-7233,MOTHER BD,H8,12.1	
411668100012	PWA;PWA-7233,MOTHER BD,H8,12.1,S	
411668100011	PWA;PWA-7233,MOTHER BD,H8,12.1,T	
411600000114	PWA;PWA-PWR-60B-22,A/D BD,SMT	
411600000115	PWA;PWA-PWR-60B-22,A/D BD,T/U	
411666230004	PWA;PWA-VENUS LED BD,U26	

9. SPARE PARTS LIST-7

Part Number	Description	Location(s)
332810000102	PWR CORD;250V10A,2P,BLK,CHINA,15	
271086057101	RES;.005 ,2W ,1% ,7520,SMT	PR15
271045107101	RES;.01 ,1W ,1% ,2512,SMT	PR2
311100157301	RES;.015 ,MnCu,1/4W,5%,10.2*5.0,	JP1
271045207101	RES;.02 ,1W ,1% ,2512,SMT	PR5,502
271002000301	RES;0 ,1/10W,5% ,0805,SMT	R71,104,232,233,234
271002000301	RES;0 ,1/10W,5% ,0805,SMT	R6
271071000002	RES;0 ,1/16W,0603,SMT	PR6,23,31,513
271012000301	RES;0 ,1/8W,5% ,1206,SMT	R3,4,8,11,14
271013010301	RES;1 ,1/4W,5% ,1206,SMT	R43,R44
271013119301	RES;1.1 ,1/4W,5% ,1206,SMT	R41,42
311121101337	RES;1.1K ,CF,1/4W,5% ,AX	R24
271071152302	RES;1.5K ,1/16W,5% ,0603,SMT	R6,8
271071152302	RES;1.5K ,1/16W,5% ,0603,SMT	R54,56,129,140,148,
271071100302	RES;10 ,1/16W,5% ,0603,SMT	R183,184,190,192,563
271002101301	RES;100 ,1/10W,5% ,0805,SMT	R13
271071101301	RES;100 ,1/16W,5% ,0603,SMT	R142,153,561
271071104101	RES;100K ,1/16W,1% ,0603,SMT	PR45,46,501,514,33
271071104302	RES;100K ,1/16W,5% ,0603,SMT	PR3,7,39,40,41
271012104301	RES;100K ,1/8W,5% ,1206,SMT	R27,28,33,35
271002103301	RES;10K ,1/10W,5% ,0805,SMT	R23,32
271071103101	RES;10K ,1/16W,1% ,0603,SMT	PR10,18,511
271071103302	RES;10K ,1/16W,5% ,0603,SMT	PR13,25,32,34,49,512
271012103301	RES;10K ,1/8W,5% ,1206,SMT	R19
271071118211	RES;11.8K,1/16W,1% ,0603,SMT	PR56
271071111101	RES;110 ,1/16W,1% ,0603,SMT	R589
271071121211	RES;12.1K,1/16W,1% ,0603,SMT	PR48

Part Number	Description	Location(s)
271071121301	RES;120 ,1/16W,5% ,0603,SMT	R502
271071124311	RES;124K ,1/16W,1% ,0603,SMT	PR500
271071137211	RES;13.7K,1/16W,1% ,0603,SMT	PR19
271071151302	RES;150 ,1/16W,5% ,0603,SMT	R508,509
271071153301	RES;15K ,1/16W,5% ,0603,SMT	R16,25,91,95,98,103
271071169311	RES;169K ,1/16W,1% ,0603,SMT	PR28
271002174211	RES;17.4K,1/8W ,1% ,0805,SMT	R16
271071180301	RES;18 ,1/16W,5% ,0603,SMT	R127,137,553,557
271002102301	RES;1K ,1/10W,5% ,0805,SMT	R15
271071102102	RES;1K ,1/16W,1% ,0603,SMT	PR12,503,505
271071102302	RES;1K ,1/16W,5% ,0603,SMT	PR11
271071105101	RES;1M ,1/16W,1% ,0603,SMT	R202,
271071105301	RES;1M ,1/16W,5% ,0603,SMT	PR20,38
271071228301	RES;2.2 ,1/16W,5% ,0603,SMT	PR8
271002221111	RES;2.21K,1/10W,1% ,0805,SMT	R22,12
271071221111	RES;2.21K,1/16W,1% ,0603,SMT	PR508
271071222302	RES;2.2K ,1/16W,5% ,0603,SMT	R518,519
271071232111	RES;2.32K,1/16W,1% ,0603,SMT	R158
271071249111	RES;2.49K,1/16W,1% ,0603,SMT	R102
271071272301	RES;2.7K ,1/16W,5% ,0603,SMT	PR27
271071204101	RES;200K ,1/16W,1% ,0603,SMT	R224
271071205311	RES;205K ,1/16W,1% ,0603,SMT	PR55
271071203101	RES;20K ,1/16W,1% ,0603,SMT	R584
271071203302	RES;20K ,1/16W,5% ,0603,SMT	R89,93
271002220301	RES;22 ,1/10W,5% ,0805,SMT	R39
271071221302	RES;22 ,1/16W,5% ,0603,SMT	R76,77,78,79,80,81,
271071221301	RES;220 ,1/16W,5% ,0603,SMT	R84

9. SPARE PARTS LIST-8

Part Number	Description	Location(s)
271071224301	RES;220K ,1/16W,5% ,0603,SMT	R177
271012224301	RES;220K ,1/8W,5% ,1206,SMT	R37,38
271071223302	RES;22K ,1/16W,5% ,0603,SMT	R17,20,26,33
271071237311	RES;237K ,1/16W,1% ,0603,SMT	PR44
271071249211	RES;24.9K,1/16W,1% ,0603,MST	PR504,515
271071267211	RES;26.7K,1/16W,1% ,0603,SMT	PR507
271071261311	RES;261K ,1/16W,1% ,0603,SMT	PR35,42
271071270301	RES;27 ,1/16W,5% ,0603,SMT	R94,97
271071271301	RES;270 ,1/16W,5% ,0603,SMT	R21,22,23
271002274311	RES;274K ,1/10W,1% ,0805,SMT	R31
271071273301	RES;27K ,1/16W,5% ,0603,SMT	R19,32
271071202102	RES;2K ,1/16W,1% ,0603,SMT	PR26,R110-112,591
271071348111	RES;3.48K,1/16W,1% ,0603,SMT	R157
271071365111	RES;3.65K,1/16W,1% ,0603,SMT	PR509
271071301311	RES;301K ,1/16W,1% ,0603,SMT	R582
271071330302	RES;33 ,1/16W,5% ,0603,SMT	PR16,47,506
271012331301	RES;330 ,1/8W,5% ,1206,SMT	R5
271071333301	RES;33K ,1/16W,5% ,0603,SMT	R551
271071357311	RES;357K ,1/16W,1% ,0603,SMT	PR37
271013478301	RES;4.7 ,1/4W,5% ,1206,SMT	R587,588
271071475112	RES;4.75K,1/16W,1% ,0603,SMT	PR14
271002472301	RES;4.7K ,1/10W,5% ,0805,SMT	PR1,4,510
271002472301	RES;4.7K ,1/10W,5% ,0805,SMT	R26
271071472302	RES;4.7K ,1/16W,5% ,0603,SMT	R24,28,46,72,109,159
271071499111	RES;4.99K,1/16W,1% ,0603,SMT	R212
271071402311	RES;402K ,1/16W,1% ,0603,SMT	PR43
271071412311	RES;412K ,1/16W,1% ,0603,SMT	PR54

Part Number	Description	Location(s)
271071442011	RES;442 ,1/16W,1% ,0603,SMT	R530,535
271071470301	RES;47 ,1/16W,5% ,0603,SMT	R12,34,53,60,61,65,
271071471302	RES;470 ,1/16W,5% ,0603,SMT	R559,213
271071474301	RES;470K ,1/16W,5% ,0603,SMT	R8,207,613,627
271012474301	RES;470K ,1/8W,5% ,1206,SMT	R1,2
271071473301	RES;47K ,1/16W,5% ,0603,SMT	PR21,R228
271071511111	RES;5.11K,1/16W,1% ,0603,SMT	PR53
271012568301	RES;5.6 ,1/10W,5% ,1206,SMT	R18
271071562301	RES;5.6K ,1/16W,5% ,0603,SMT	R116,141
271012562301	RES;5.6K ,1/8W,5% ,1206,SMT	R7
271012510301	RES;51 ,1/8W,5% ,1206,SMT	R9,10
271071523211	RES;52.3K,1/16W,1% ,0603,SMT	PR22
271071560301	RES;56 ,1/16W,5% ,0603,SMT	PR17
271071562831	RES;56.2 ,1/16W,5% ,0603,SMT	R40,506
271071564301	RES;560K ,1/16W,5% ,0603,SMT	R9
271013564301	RES;560K ,1/4W ,5% ,1206,SMT	R29
271071576011	RES;576 ,1/16W,1% ,0603,SMT	PR24
271071622301	RES;6.2K ,1/16W,5% ,0603,SMT	PR9
271002649111	RES;6.49K,1/10W,1% ,0805,SMT	R30
271071681301	RES;680 ,1/16W,5% ,0603,SMT	R1-5,7
271071681301	RES;680 ,1/16W,5% ,0603,SMT	R15,18,134,150
271013683301	RES;680K ,1/4W ,5% ,1206,SMT	R25
271002683301	RES;68K ,1/8W,5% ,0805,SMT	R21
271071787011	RES;787 ,1/16W,1% ,0603,YAGEO,S	PR30
271002822301	RES;8.2K ,1/10W,5% ,0805,SMT	R20
271071976211	RES;97.6K,1/16W,1% ,0603,SMT	PR52
271571000301	RP;0*8 ,16P ,1/16W,5% ,1606,SM	RP60,61

9. SPARE PARTS LIST-9

Part Number	Description	Location(s)
271611152301	RP;1.5K*4,8P ,1/16W,5% ,0612,SMT	RP1
271621152301	RP;1.5K*8,10P,1/32W,5% ,1206,SMT	RP32
271571100301	RP;10*8 ,16P ,1/16W,5% ,1606,SM	RP47,49,50,51,55,56
271611103301	RP;10K*4 ,8P ,1/16W,5% ,0612,SMT	RP4,7,52,518
271621103303	RP;10K*8 ,10P,1/16W,5% ,1206,SMT	RP8,14,19,34,35,41
271611102301	RP;1K*4 ,8P ,1/16W,5% ,0612,SMT	RP6
271611220301	RP;22*4 ,8P ,1/16W,5% ,0612,SMT	RP66
271611330301	RP;33*4 ,8P ,1/16W,5% ,0612,SMT	RP15,17,22,31,501
271571330301	RP;33*8 ,16P ,1/16W,5% ,1606,SM	RP16,18,20,21,23,24
271621472303	RP;4.7K*8,10P,1/16W,5% ,1206,SMT	RP2,3,5,45,54,25
271621433301	RP;43K*8 ,10P,1/16W,5% ,1206,SMT	RP53,63,516
271611470301	RP;47*4 ,8P ,1/16W,5% ,0612,SMT	RP9
271571470301	RP;47*8 ,16P ,1/16W,5% ,1606,SM	RP12
271621473301	RP;47K*8 ,10P,1/16W,5% ,1206,SMT	RP65,520,521
271611750301	RP;75*4 ,8P ,1/16W,5% ,0612,SMT	RP11,13
271621822301	RP;8.2K*8,10P,1/16W,5% ,1206,SMT	RP42,46,64,504
565160000089	S/W;1.44M,PCTEL789,FCC DRIVE,NT4	
565160000086	S/W;1.44M,PCTEL789,FCC DRIVE,WIN	
565166680001	S/W;CD ROM,SYSTEM DRIVER,6233	
371102610401	SCREW;M2.6L4,FLT(+),NIW	
371102610401	SCREW;M2.6L4,FLT(+),NIW	
371102610081	SCREW;M2.6L8,PAN(+),NIB	
371102010010	SCREW;M2L4,FLT(+),NIW	
340668100001	SHIELD ASSY;TOP,CASE KIT,7233	
340666700029	SHIELD ASSY-2;BOTTOM,CASE KIT,61	
341666200011	SHIELD;AUDIO,NV	
343665400009	SHIELD;FDD,VENUS	

Part Number	Description	Location(s)
341666200013	SHIELD;PCMCIA,M/B,NV	
361400003028	SHIN-ETSU;KE45WS RTV SILICON,350	
333050000014	SHRINK TUBE;600V,125',D1.5*20MM,	
561860000022	SINGLE PAGE;GN,NOTE FOR BATTERY&	
561860000029	SINGLE PAGE;PWR-60B-22A	
365250000010	SOLDER BAR;63/37 ALLOY 1KG/BAR	
361200003025	SOLDER PASTE;RMA-010-FP	
365350000002	SOLDER WIRE;63/37FLUX%1.2 DIA.64	
365350000002	SOLDER WIRE;63/37FLUX%1.2 DIA.64	
370102010502	SPC-SCREW;M2 L5,NIB,K-HD,727	
370102610602	SPC-SCREW;M2.6 L6,NIB,K-HD,727	
370102610401	SPC-SCREW;M2.6L4,NIB,727,NLK	
370102610401	SPC-SCREW;M2.6L4,NIB,727,NLK	
370102610401	SPC-SCREW;M2.6L4,NIB,727,NLK	
370102610401	SPC-SCREW;M2.6L4,NIB,727,NLK	
370102010201	SPC-SCREW;M2L2,NIW,K-HD,727	
370102010201	SPC-SCREW;M2L2,NIW,K-HD,727	
370102010253	SPC-SCREW;M2L2.5,NIW/NLK,HD07	
370102010302	SPC-SCREW;M2L3,NIW,K-HD,736	
370102010302	SPC-SCREW;M2L3,NIW,K-HD,736	
370102010404	SPC-SCREW;M2L4,K-HD,NIB	
370103010401	SPC-SCREW;M3L4,K-HD(+),D5.2,NIW,	
370103010505	SPC-SCREW;M3L5,FLNG/PAN(+),HD7,N	
370103010501	SPC-SCREW;M3L5,NIB,K-HD,727	
370103010604	SPC-SCREW;M3L6,NIB,727,NYLOK	
339111100002	SPEAKER ASSY;CASE KIT,VENUS	
345666800001	SPONGE;LCD CABLE,SJ03,6233	

9. SPARE PARTS LIST-10

Part Number	Description	Location(s)
345666200010	SPONGE;LCD/LENS,NV	
345668100001	SPONGE;SPEAKER,7233	
345666200014	SPONGE;WIRE ASSY,BAT,NV	
341666900002	SPRING;CPU,6633	
341666200012	SPRING;DC JACK,NV	
341665400001	SPRING;LATCH,LCD,ENTRY	
343666800003	STANDOFF;M2H12/M2.6,6233	
337120124001	SW;DIP,SPST,2P,25VDC,24MA,HDK632	SW500
297120101005	SW;DIP,SPST,8P,50VDC,.1A,SMT,DHS	SW2
297040102002	SW;PUSH BUTTON,SPST,15V/20MA,H3.	SW1,SW2
337030105013	SW;TOGGLE,SPST,5V/1mA	SW1
225600000013	TAPE;60MM*50M,PP	
225600000012	TAPE;60MM*900M,PP	
225665500001	TAPE;INSULATION,AC04,25M*6MM,503	
225665500001	TAPE;INSULATION,AC04,25M*6MM,503	
225664300001	TAPE;INSULATION,AC04,5024	
346665400019	THERMAL PAD;20*20*.5,VENUS	
346666100005	THERMAL PAD;30*30*.5,6133	
361200002002	THINNER;#111B,KESTER	
441666900001	TOUCH PAD ASSY;41PDG220-2,6633	
442164900004	TOUCH PAD MODULE;TM41PDG220-2	
288227002001	TRANS;2N7002LT1,N-CHANNEL FET	PQ5,8,11,12,13,503,
328222645001	TRANS;2SK2645-01MR,9A,600V,TO-22	Q5
288200144002	TRANS;DTA144WK,PNP,SMT	PQ504
288200144002	TRANS;DTA144WK,PNP,SMT	Q1
288200144003	TRANS;DTC144TKA,N-MOSFET,SOT-23	Q9,10,512,514,515
288200144001	TRANS;DTC144WK,NPN,SOT-23,SMT	PQ9,506,Q511,513

Part Number	Description	Location(s)
288200144001	TRANS;DTC144WK,NPN,SOT-23,SMT	Q2
288202222001	TRANS;MMBT2222AL,NPN,TO236AB	PQ501
288202907001	TRANS;MMBT2907AL,PNP,TO-236AB	PQ7
288203904010	TRANS;MMBT3904L,NPN,Tr35NS,TO236	Q1,4,517
288204401001	TRANS;MMBT4401,NPN,SOT-23,3P	Q3
288202301001	TRANS;SI2301DS,P-MOSFET,SOT-23	Q16,508,516
288204416001	TRANS;Si4416DY,N-MOSFET,.028OHM,	PQ1,500
288204800001	TRANS;SI4800DY,N-MOS,.0185OHM,SO	PU2
288204832001	TRANS;SI4832DY,N-MOSFET,.028OHM,	PQ3,502
288204835001	TRANS;SI4835DY,PMOS,6A/30V,.035,	PQ2,505
288209410001	TRANS;SI9410DY,N-MOSFET,.04OHM,S	Q502
271911103902	VR;10K ,20%,.05W,XV0102GPH1N-93	VR1
421666200009	WIRE ASSY;BATTERY BIOS,NV	
421666200006	WIRE ASSY;BKLIGHT LCD-12.1",NV	
421666700001	WIRE ASSY;LCD-MIT SJ03,6133S	
313001050056	XSFORMER;PQ2620,LP=650uH,38/5/7	T14
274011431408	XTAL;14.318M,50PPM,32PF,7*5,4P,S	X1,4
274011600407	XTAL;16MHZ,30PPM,16PF,7*5,4P,SMT	X501
274012949401	XTAL;29.498928MHZ,30PPM,20PF,4P,	X500
274013276103	XTAL;32.768KHZ,30PPM,12.5PF,CM20	X2
274014915402	XTAL;49.152MHZ,30PPM,16PF,7*5,4P	X3