

# 6120N N/B MAINTENANCE

## CONTENTS

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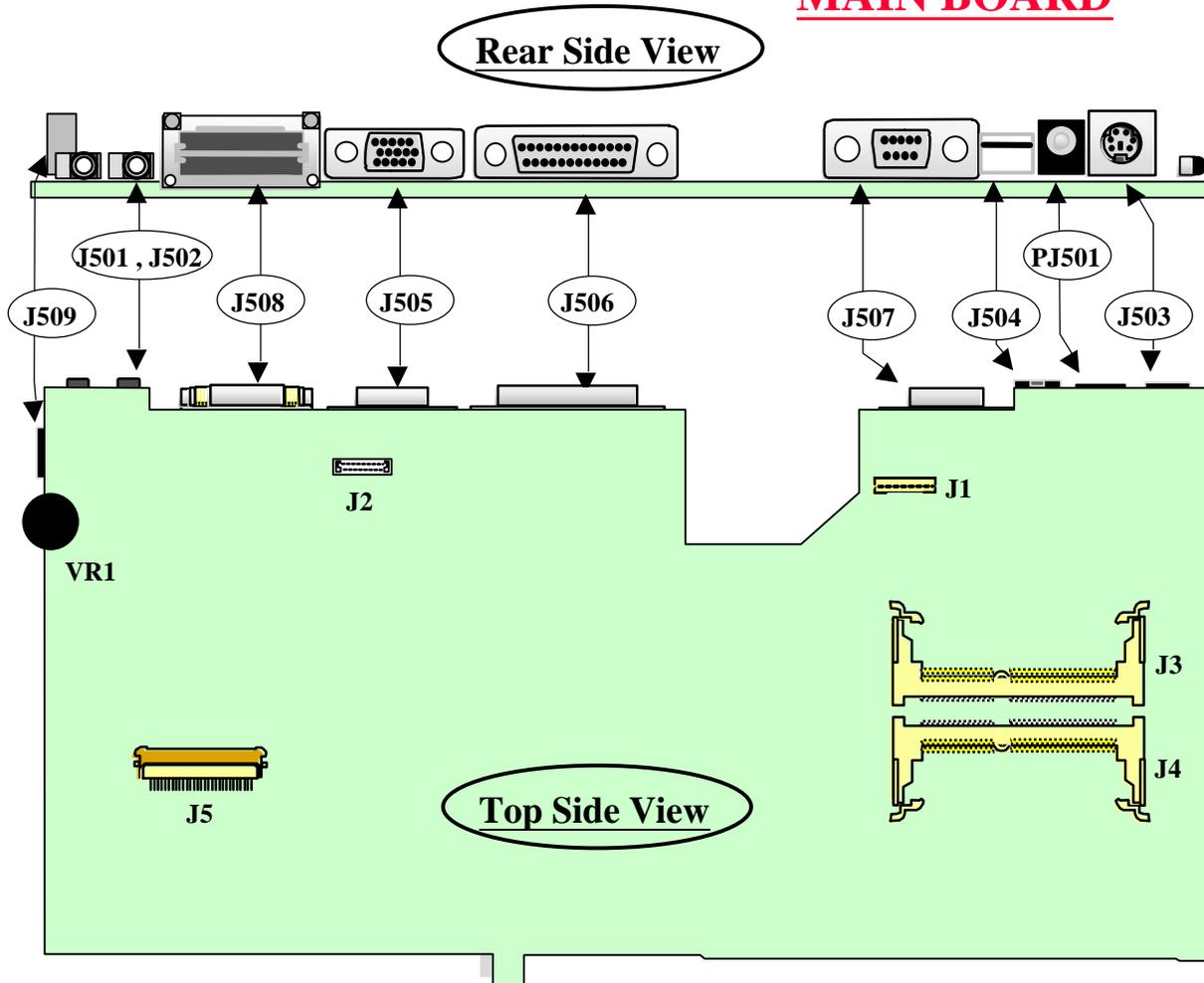
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1. Location Of Connectors & Switches.....	2
2. Location Of Major Components.....	5
3. Pin Descriptions Of Major Components.....	9
4. Major Chips Description.....	28
5. Assembly & Disassembly.....	32
6. Maintenance Diagnostics .....	52
7. System Block Diagram .....	55
8. Trouble Shooting.....	56
9. Spare Parts List.....	99
10. System Block Diagram & Mainboard Schematics.....	109
I/O Board Schematics	
Button Board Schematics	
Trans Board Schematics	

# 6120N N/B MAINTENANCE

## 1. Location Of Connectors & Switches (Main Board Top Side)

### MAIN BOARD



#### Rear Side View

- J501 : External speaker connector.
- J502 : External microphone connector.
- J503 : PS/2 keyboard or mouse connector.
- J504 : USB port connector.
- J505 : External CRT monitor connector.
- J506 : Printer port connector.
- J507 : Serial port Connector.
- J508 : Port replicator connector.
- J509 : TV terminal connector.
- PJ501 : Power jack.

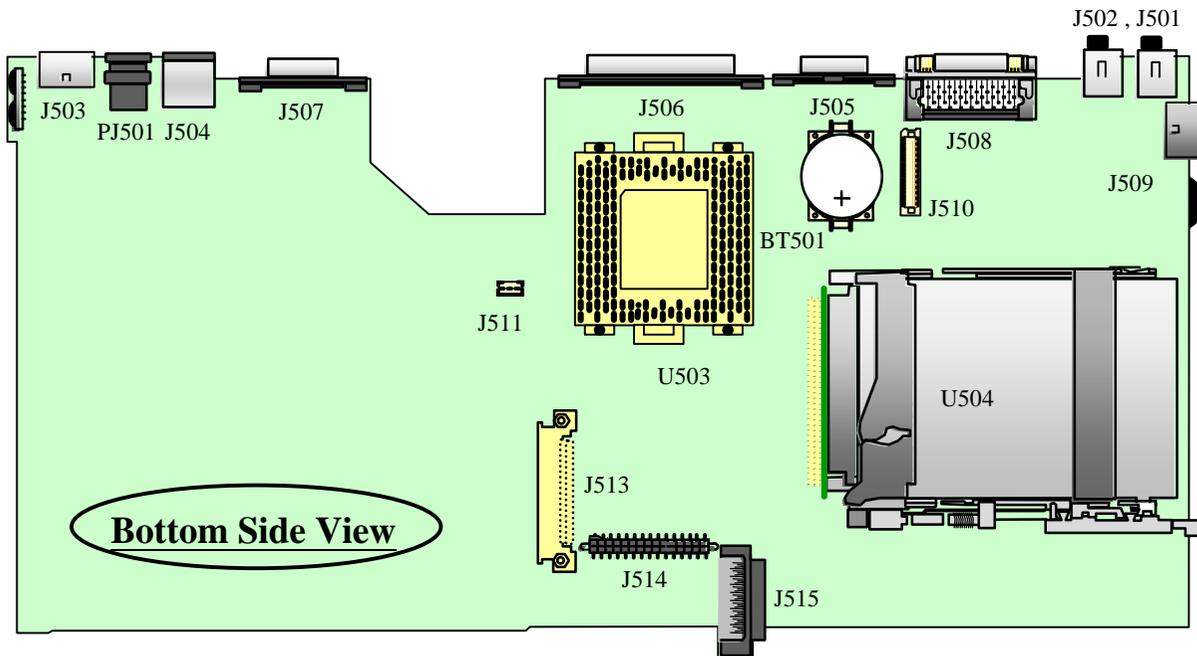
#### Top Side View

- J1 : Backlight and LED indicator connector.
- J2 : LVDS LCD panel connector.
- J3 : 144 pin 3.3V unbuffer expansion DIMM socket.
- J4 : 144 pin 3.3V unbuffer expansion DIMM socket.
- J5 : Internal keyboard connector.

# 6120N N/B MAINTENANCE

## 1 . Location Of Connectors & Switches(Main Board bottom Side)

### MAIN BOARD

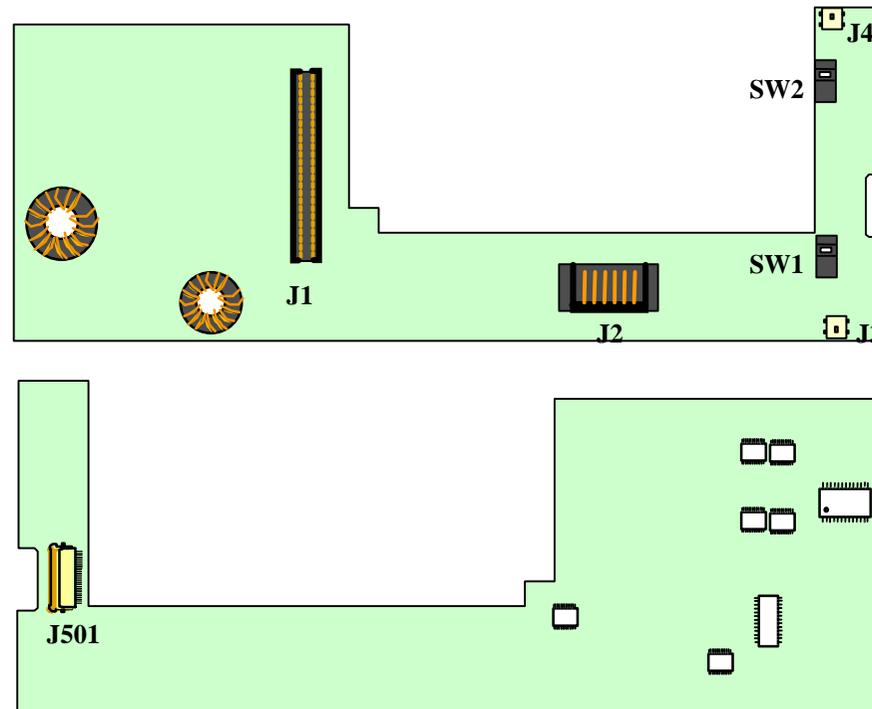


- ✂ J501 : External speaker connector.
- ✂ J502 : External microphone connector.
- ✂ J503 : PS/2 keyboard or mouse connector.
- ✂ J504 : USB port connector.
- ✂ J505 : External CRT monitor connector.
- ✂ J506 : Printer port connector.
- ✂ J507 : Serial port Connector.
- ✂ J508 : Port replicator connector.
- ✂ J509 : TV terminal connector.
- ✂ J510 : Fax/modem/voice card connector.
- ✂ J511 : CPU fan connector.
- ✂ J513 : CD-ROM connector.
- ✂ J514 : Charger & D/D to M/B connector.
- ✂ J515 : FDD and HDD connector.
  
- ✂ PJ501 : Power jack.
- ✂ U503 : PPGA CPU socket.
- ✂ U504 : PCI PCMCIA connector.
- ✂ BT501 : CMOS backup battery.

# 6120N N/B MAINTENANCE

## 1 . Location Of Connectors & Switches

### 7020 D/D & CHARGE BD



✂ J1 : Charger & D/D to M/B connector

✂ J2 : Battery pack connector.

✂ J3 : Left Internal Speaker Out.

✂ J4 : Right Internal Speaker Out.

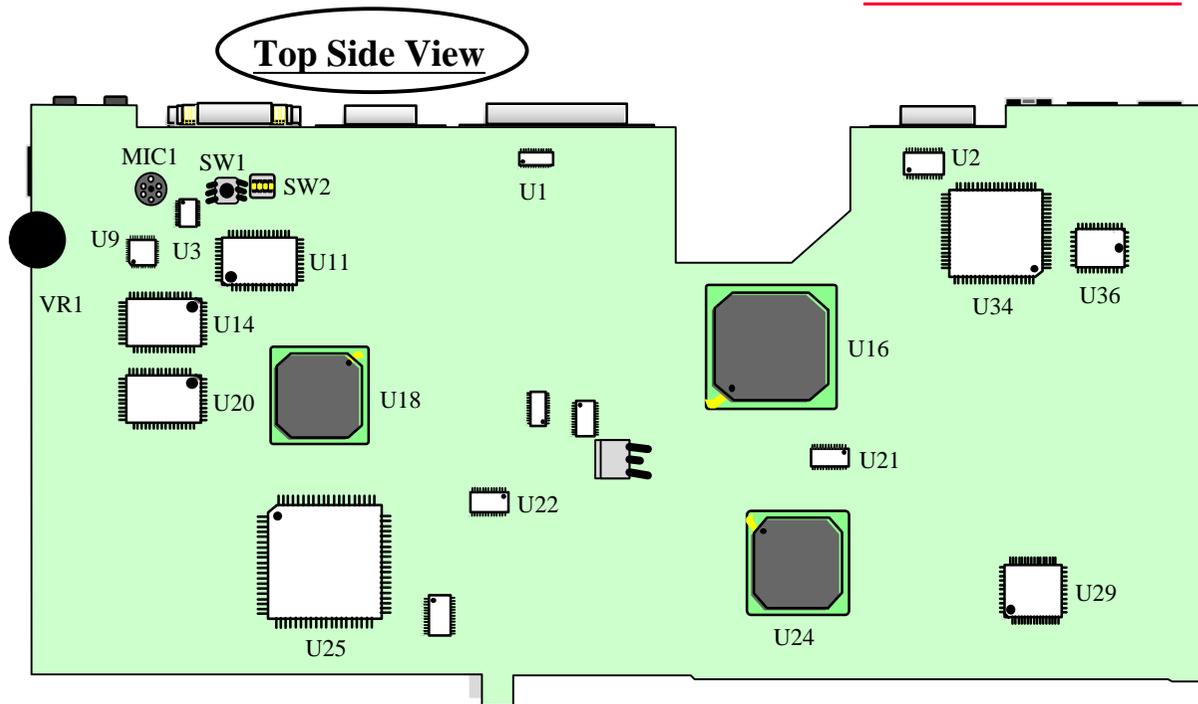
✂ SW1 : Touch pad module left button.

✂ SW2 : Touch pad module right button.

✂ J501 : Touch pad module connector.

# 6120N N/B MAINTENANCE

## 2. Location Of Major Components(Main Board top Side)



- ✂ MIC1 : Internal microphone.
- ✂ SW1 : LCD panel type select.
- ✂ SW2 : Power on/off switch.
- ✂ VR1 : Audio volume adjustment.

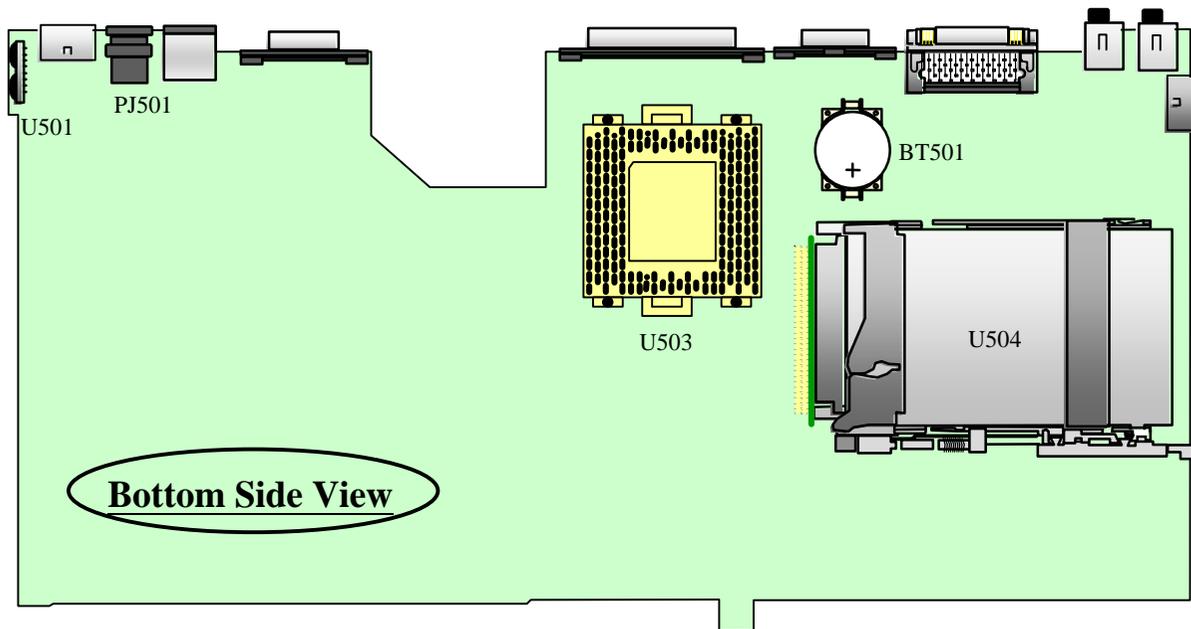
- ✂ U1 : PACS1284
- ✂ U2 : ADM3311 SIO driver.
- ✂ U3 : TPA0202 Audio amplifier.
- ✂ U9 : CS4297 audio AC CODEC device.
- ✂ U11 : CS4280 Audio controller.
- ✂ U14,U20 : On-board 8MB SGRAM .
- ✂ U16 : Intel FW82443BX(ZX) north bridge.
- ✂ U18 : ATI\_RAGE\_LT\_Pro AGP VGA controller.
- ✂ U21 : W40S11-02 SDRAM clock buffer.
- ✂ U22 : W137 Clock synthesizer.
- ✂ U24 : Intel PIIX4 south bridge.
- ✂ U25 : TI1225 PCMCIA Cardbus controller.
- ✂ U29 : PC97338 Super I/O.
- ✂ U34 : PC87570 Keyboard mouse & battery charge controller.
- ✂ U36 : Flashable ROM system BIOS.

*Notice* : When you change the flash ROM, Please remove the CMOS battery for minutes.  
It is to clear the content of CMOS or it would not boot up after change BIOS. \* Page 8.

# 6120N N/B MAINTENANCE

## 2. Location Of Major Components(Main Board bottom Side)

### MAIN BOARD

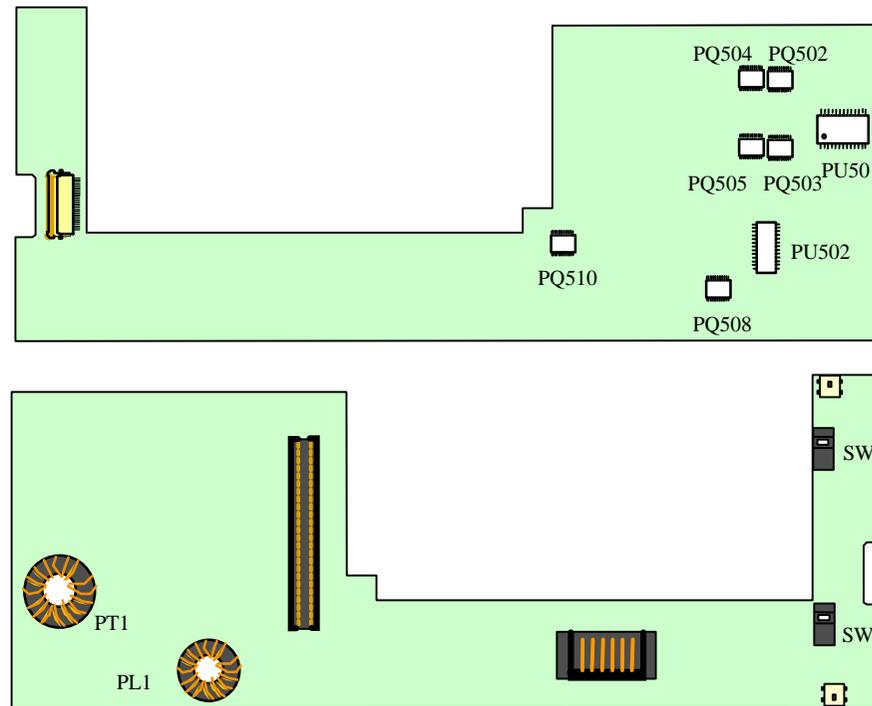


- ✂ U501 : HSDL-3600 Infrared Transceiver.
- ✂ U503 : PPGA 370 CPU socket.
- ✂ U504 : PCI PCMCIA connector.
- ✂ BT501 : CMOS backup battery.

# 6120N N/B MAINTENANCE

## 2. Location Of Major Components

### 7020 D/D CHARGE BD



✂ PU501 : SB3052P +3V,+5V,+12V Generator.

✂ PQ502 : NDS9410 N-Channel Transistor.

✂ PQ503 : FDS6612 N-Channel Power MOSFET.

✂ PQ504 : NDS9410 N-Channel Transistor.

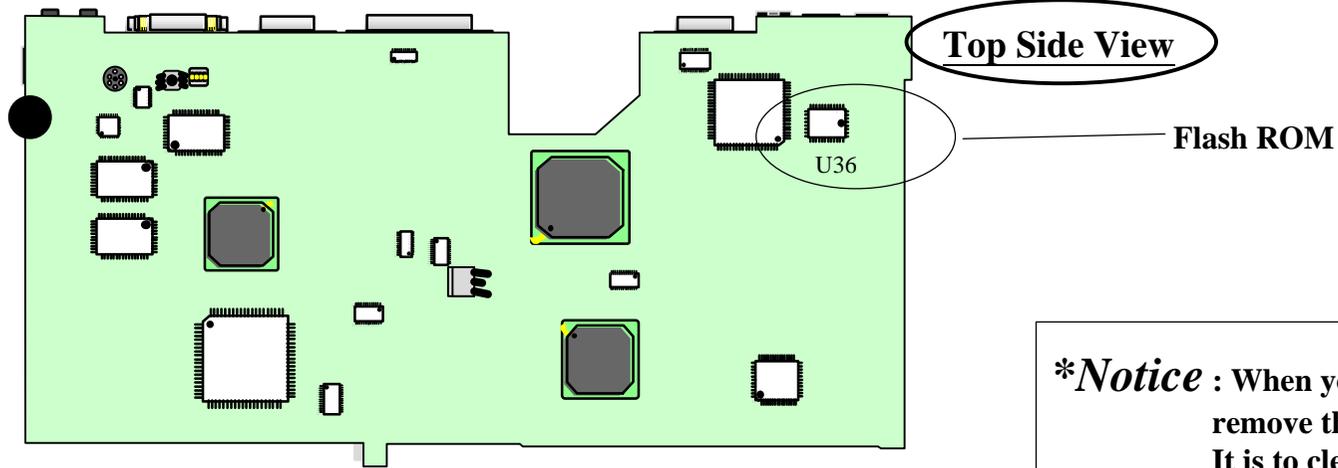
✂ PQ505 : FDS6690 N-Channel Power MOSFET.

✂ PU502 : Pulse-width-modulation Control For Battery Charge.

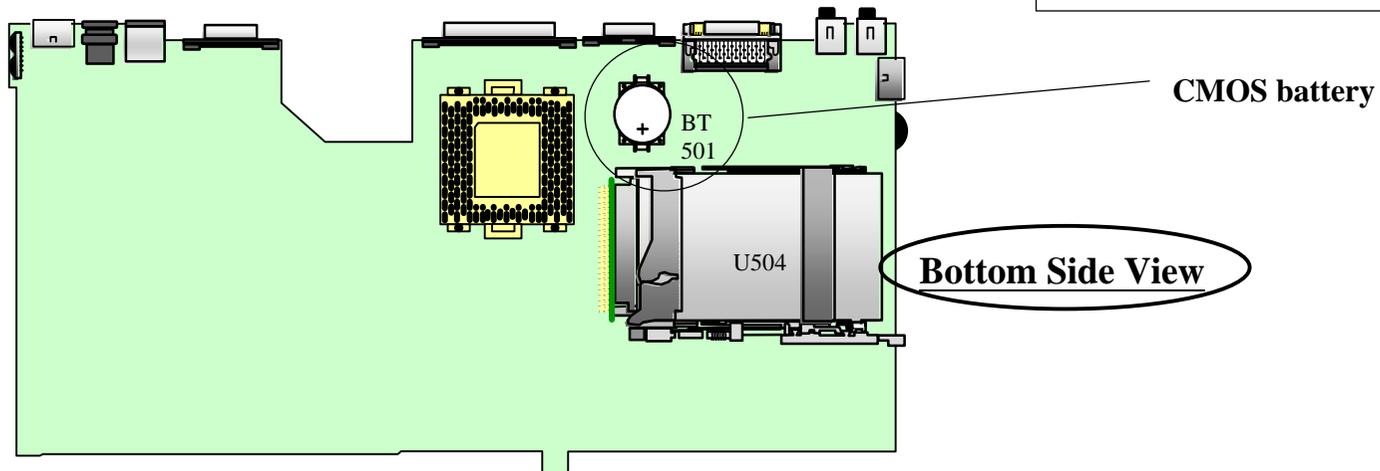
✂ PQ508 : SI4435 P-Channel Power MOSFET.

✂ PQ510 : SI4435 P-Channel Power MOSFET.

# 6120N N/B MAINTENANCE



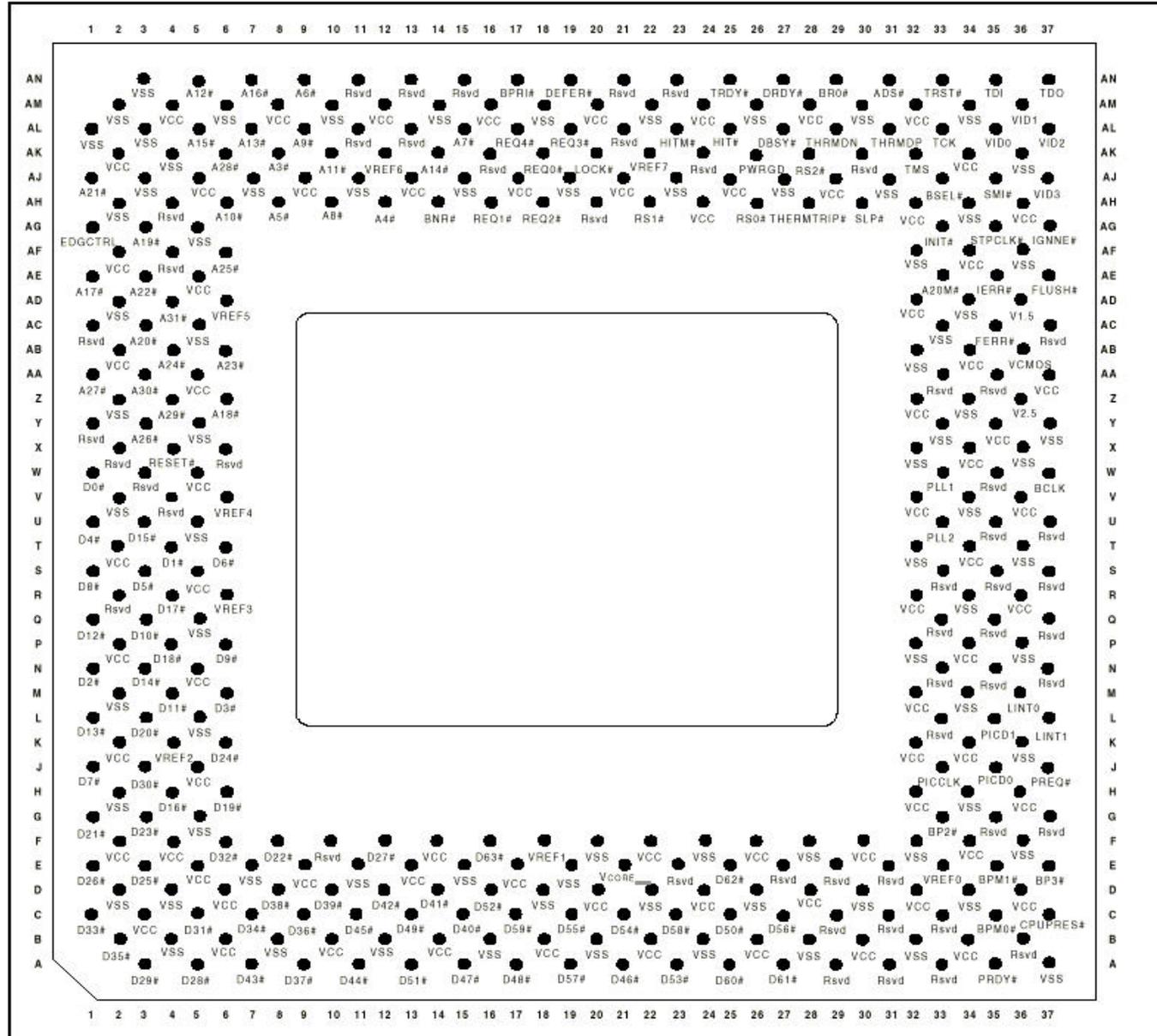
***\*Notice*** : When you change the flash ROM, Please remove the CMOS battery for minutes. It is to clear the content of CMOS . or it would not boot up after change BIOS.



# 6120N N/B MAINTENANCE

## 3. Pin Descriptions Of Major Components

### 3.1 INTEL Celeron Processor



# 6120N N/B MAINTENANCE

## 3. Pin Descriptions Of Major Components

### 3.1 INTEL Celeron Processor

Signal	Type	Description
A[31:3]#	I/O	The A[31:3]# ( <b>Address</b> ) signals define a 2 <sup>32</sup> -byte physical memory address space. When ADS# is active, these pins transmit the address of a transaction; when ADS# is inactive, these pins transmit transaction type information. The A[31:24]# signals are parity-protected by the AP1# parity signal, and the A[23:3]# signals are parity-protected by the AP0# parity signal. On the active-to-inactive transition of RESET#, the processors sample the A[31:3]# pins to determine their power-on configuration.
A20M#	I	If the A20M# ( <b>Address-20 Mask</b> ) input signal is asserted, the Intel Celeron processor masks physical address bit 20 (A20#) before looking up a line in any internal cache and before driving a read/write transaction on the bus. Asserting A20M# emulates the 8086 processor's address wrap-around at the 1 MB boundary. Assertion of A20M# is only supported in real mode. A20M# is an asynchronous signal. However, to ensure recognition of this signal following an I/O write instruction, it must be valid along with the TRDY# assertion of the corresponding I/O Write bus transaction.
ADS#	I/O	The ADS# ( <b>Address Strobe</b> ) signal is asserted to indicate the validity of the transaction address on the A[31:3]# pins. All bus agents observe the ADS# activation to begin parity checking, protocol checking, address decode, internal snoop, or deferred reply ID match operations associated with the new transaction.
BCLK	I	The BCLK ( <b>Bus Clock</b> ) signal determines the bus frequency. All Intel Celeron processor system bus agents must receive this signal to drive their outputs and latch their inputs on the BCLK rising edge. All external timing parameters are specified with respect to the BCLK signal.
BNR#	I/O	The BNR# ( <b>Block Next Request</b> ) signal is used to assert a bus stall by any bus agent who is unable to accept new bus transactions. During a bus stall, the current bus owner cannot issue any new transactions. Since multiple agents might need to request a bus stall at the same time, BNR# is a wire-OR signal which must connect the appropriate pins of all Intel Celeron processor system bus agents. In order to avoid wire-OR glitches associated with simultaneous edge transitions driven by multiple drivers, BNR# is activated on specific clock edges and sampled on specific clock edges.
BP[3:2]#	I/O	The BP[3:2]# ( <b>Breakpoint</b> ) signals are outputs from the processor that indicate the status of breakpoints.
BPM[1:0]#	I/O	( <b>Breakpoint Monitor</b> ) signals are breakpoint and performance monitor signals. They are outputs from the processor which indicate the status of breakpoints and programmable counters used for monitoring processor performance.
BPRI#	I	The BPRI# ( <b>Bus Priority Request</b> ) signal is used to arbitrate for ownership of the Intel Celeron processor system bus. Observing BPRI# active (as asserted by the priority agent) causes all other agents to stop issuing new requests, unless such requests are part of an ongoing locked operation. The priority agent keeps BPRI# asserted until all of its requests are completed, then releases the bus by deasserting BPRI#.
BSEL	I/O	This signal indicates the system bus frequency supported by the processor. A logic low indicates a host bus frequency of 66 MHz.
BR0#	I/O	The BR0# ( <b>Bus Request</b> ) pin drives the BREQ[0]# signal in the system. During power-up configuration, the central agent asserts the BREQ0# bus signal in the system to assign the symmetric agent ID to the processor. The processor samples its BR0# pin on the active-to-inactive transition of RESET# to obtain its symmetric agent ID. The processor asserts BR0# to request the system bus.
CPUPRES# (PPGA only)	O	The CPUPRES# signal provides the ability for a system board to detect the presence of a processor. This pin is a ground on the processor indicating to the system that a processor is installed.

Signal	Type	Description
D[63:0]#	I/O	The D[63:0]# ( <b>Data</b> ) signals are the data signals. These signals provide a 64-bit data path between the Intel Celeron processor system bus agents, and must connect the appropriate pins on all such agents. The data driver asserts DRDY# to indicate a valid data transfer.
DBSY#	I/O	The DBSY# ( <b>Data Bus Busy</b> ) signal is asserted by the agent responsible for driving data on the Intel Celeron processor system bus to indicate that the data bus is in use. The data bus is released after DBSY# is deasserted.
DEFER#	I	The DEFER# signal is asserted by an agent to indicate that a transaction cannot be guaranteed in-order completion. Assertion of DEFER# is normally the responsibility of the addressed memory or I/O agent.
DRDY#	I/O	The DRDY# ( <b>Data Ready</b> ) signal is asserted by the data driver on each data transfer, indicating valid data on the data bus. In a multicycle data transfer, DRDY# may be deasserted to insert idle clocks.
FERR#	O	The FERR# ( <b>Floating-point Error</b> ) signal is asserted when the processor detects an unmasked floating-point error. FERR# is similar to the ERROR# signal on the Intel 387 coprocessor, and is included for compatibility with systems using MS-DOS*-type floating-point error reporting.
FLUSH#	I	When the FLUSH# input signal is asserted, the processor writes back all data in the Modified state from the internal cache and invalidates all internal cache lines. At the completion of this operation, the processor issues a Flush Acknowledge transaction. The processor does not cache any new data while the FLUSH# signal remains asserted. FLUSH# is an asynchronous signal. However, to ensure recognition of this signal following an I/O write instruction, it must be valid along with the TRDY# assertion of the corresponding I/O Write bus transaction. On the active-to-inactive transition of RESET#, the processor samples FLUSH# to determine its power-on configuration.
HIT#, HITM#	I/O	The HIT# ( <b>Snoop Hit</b> ) and HITM# ( <b>Hit Modified</b> ) signals convey transaction snoop operation results. Any such agent may assert both HIT# and HITM# together to indicate that it requires a snoop stall, which can be continued by reasserting HIT# and HITM# together.
IERR#	O	The IERR# ( <b>Internal Error</b> ) signal is asserted by a processor as the result of an internal error. Assertion of IERR# is usually accompanied by a SHUTDOWN transaction on the Intel Celeron processor system bus. This transaction may optionally be converted to an external error signal (e.g., NMI) by system core logic. The processor will keep IERR# asserted until the assertion of RESET#, BINIT#, or INIT#.
IGNNE#	I	The IGNNE# ( <b>Ignore Numeric Error</b> ) signal is asserted to force the processor to ignore a numeric error and continue to execute noncontrol floating-point instructions. If IGNNE# is deasserted, the processor generates an exception on a noncontrol floating-point instruction if a previous floating-point instruction caused an error. IGNNE# has no effect when the NE bit in control register 0 is set. IGNNE# is an asynchronous signal. However, to ensure recognition of this signal following an I/O write instruction, it must be valid along with the TRDY# assertion of the corresponding I/O Write bus transaction.
INIT#	I	The INIT# ( <b>Initialization</b> ) signal, when asserted, resets integer registers inside all processors without affecting their internal (L1) caches or floating-point registers. Each processor then begins execution at the power-on Reset vector configured during power-on configuration. The processor continues to handle snoop requests during INIT# assertion. INIT# is an asynchronous signal and must connect the appropriate pins of all bus agents. If INIT# is sampled active on the active to inactive transition of RESET#, then the processor executes its Built-in Self-Test (BIST).

# 6120N N/B MAINTENANCE

## 3.1 INTEL Celeron Processor

Signal	Type	Description
LINT[1:0]	I	The LINT[1:0] ( <b>Local APIC Interrupt</b> ) signals must connect the appropriate pins of all APIC Bus agents, including all processors and the core logic or I/O APIC component. When the APIC is disabled, the LINT0 signal becomes INTR, a maskable interrupt request signal, and LINT1 becomes NMI, a nonmaskable interrupt. INTR and NMI are backward compatible with the signals of those names on the Pentium processor. Both signals are asynchronous. Both of these signals must be software configured via BIOS programming of the APIC register space to be used either as NMI/INTR or LINT[1:0]. Because the APIC is enabled by default after Reset, operation of these pins as LINT[1:0] is the default configuration.
LOCK#	I/O	The <b>LOCK#</b> signal indicates to the system that a transaction must occur atomically. For a locked sequence of transactions, LOCK# is asserted from the beginning of the first transaction end of the last transaction. When the priority agent asserts BPRI# to arbitrate for ownership of the system bus, it will wait until it observes LOCK# deasserted. This enables symmetric agents to retain ownership of the system bus throughout the bus locked operation and ensure the atomicity of lock.
EDGCTRL	I	The <b>EDGCTRL</b> input provides AGTL+ edge control and should be pulled up to VCC <sub>CORE</sub> with a 51 ± 5% resistor.
PICCLK	I	The <b>PICCLK (APIC Clock)</b> signal is an input clock to the processor and core logic or I/O APIC which is required for operation of all processors, core logic, and I/O APIC components on the APIC bus.
PICD[1:0]	I/O	The <b>PICD[1:0] (APIC Data)</b> signals are used for bidirectional serial message passing on the APIC bus, and must connect the appropriate pins of the Intel Celeron processor for proper initialization.
PLL1, PLL2 (PPGA only)	I	All Intel Celeron processors have internal analog PLL clock generators that require quiet power supplies. PLL1 and PLL2 are inputs to the internal PLL and should be connected to VCC <sub>CORE</sub> through a low-pass filter that minimizes jitter.
PRDY#	O	The <b>PRDY# (Probe Ready)</b> signal is a processor output used by debug tools to determine processor debug readiness.
PREQ#	I	The <b>PREQ# (Probe Request)</b> signal is used by debug tools to request debug operation of the processors.
PWRGOOD	I	The <b>PWRGOOD (Power Good)</b> signal is a 2.5 V tolerant processor input. The processor requires this signal to be a clean indication that the clocks and power supplies (VCC <sub>CORE</sub> , etc.) are stable and within their specifications. Clean implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high (2.5 V) state, illustrates the relationship of PWRGOOD to other system signals. PWRGOOD can be driven inactive at any time, but clocks and power must again be stable before a subsequent rising edge of PWRGOOD. It must also meet the minimum pulse width, and be followed by a 1 ms RESET# pulse. The PWRGOOD signal must be supplied to the processor; it is used to protect internal circuits against voltage sequencing issues. It should be driven high throughout boundary scan operation.
REQ[4:0]#	I/O	The <b>REQ[4:0]# (Request Command)</b> They are asserted by the current bus owner over two clock cycles to define the currently active transaction type.

Signal	Type	Description
RESET#	I	Asserting the <b>RESET#</b> signal resets the processor to a known state and invalidates the L1 cache without writing back any of the contents. RESET# must remain active for one microsecond for a "Warm" Reset; for a power-on Reset, RESET# must stay active for at least one millisecond after VCC <sub>CORE</sub> and CLK have reached their proper specifications. On observing active RESET#, all system bus agents will deassert their outputs within two clocks. A number of bus signals are sampled at the active-to-inactive transition of RESET# for power-on configuration. The processor may have its outputs tristated via power-on configuration. Otherwise, if INIT# is sampled active during the active-to-inactive transition of RESET#, the processor will execute its Built-in Self-Test (BIST). Whether or not BIST is executed, the processor will begin program execution at the power on Reset vector (default 0_FFFh_FFF0h).
RS[2:0]#	I	The <b>RS[2:0]# (Response Status)</b> signals are driven by the response agent (the agent responsible for completion of the current transaction), and must connect the appropriate pins of all processor system bus agents.
SLP#	I	The <b>SLP# (Sleep)</b> signal, when asserted in Stop-Grant state, causes processors to enter the Sleep state. During Sleep state, the processor stops providing internal clock signals to all units, leaving only the Phase-Locked Loop (PLL) still operating. Processors in this state will not recognize snoops or interrupts. The processor will recognize only assertions of the SLP#, STPCLK#, and RESET# signals while in Sleep state. If SLP# is deasserted, the processor exits Sleep state and returns to Stop-Grant state, restarting its internal clock signals to the bus and APIC processor core units.
SMI#	I	The <b>SMI# (System Management Interrupt)</b> signal is asserted asynchronously by system logic. On accepting a System Management Interrupt, processors save the current state and enter System Management Mode (SMM). An SMI Acknowledge transaction is issued, and the processor begins program execution from the SMM handler.
STPCLK#	I	The <b>STPCLK# (Stop Clock)</b> signal, when asserted, causes processors to enter a low power Stop-Grant state. The processor issues a Stop-Grant Acknowledge transaction, and stops providing internal clock signals to all processor core units except the bus and APIC units. The processor continues to snoop bus transactions and service interrupts while in Stop-Grant state. When STPCLK# is deasserted, the processor restarts its internal clock to all units and resumes execution. The assertion of STPCLK# has no effect on the bus clock; STPCLK# is an asynchronous input.
THERMTRIP#	O	The processor protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all execution when the junction temperature exceeds approximately 135 °C. This is signaled to the system by the <b>THERMTRIP# (Thermal Trip)</b> pin. Once activated, the signal remains latched, and the processor stopped, until RESET# goes active. There is no hysteresis built into the thermal sensor itself; as long as the die temperature drops below the trip level, a RESET# pulse will reset the processor and execution will continue. If the temperature has not dropped below the trip level, the processor will reassert THERMTRIP# and remain stopped.
THERMDN	O	Thermal Diode p-n junction. Used to calculate core temperature.
THERMDP	I	Thermal Diode p-n junction. Used to calculate core temperature.
TMS	I	The <b>TMS (Test Mode Select)</b> signal is a JTAG specification support signal used by debug tools.

# 6120N N/B MAINTENANCE

## 3.1 INTEL Celeron Processor

Signal	Type	Description
TRST#	I	The TRST# (Test Reset) signal resets the Test Access Port (TAP) logic. Intel Celeron processors require this signal to be driven low during power on Reset. A 680 ohm resistor is the suggested value for a pull down resistor on TRST#.
TCK	I	The TCK (Test Clock) signal provides the clock input for the Intel Celeron processor Test Access Port.
TDI	I	The TDI (Test Data In) signal transfers serial test data into the processor. TDI provides the serial input needed for JTAG specification support.
TDO	O	The TDO (Test Data Out) signal transfers serial test data out of the processor. TDO provides the serial output needed for JTAG specification support.
TRDY#	I	The TRDY# (Target Ready) signal is asserted by the target to indicate that it is ready to receive a write or implicit writeback data transfer.
V <sub>CC1.5</sub> (PPGA only)	I	The V <sub>CC CMOS</sub> pin provides the CMOS voltage for use by the platform. The 2.5 V must be provided to the V <sub>CC2.5</sub> input and 1.5 V must be provided to the V <sub>CC1.5</sub> input. The processor re-routes the 2.5 V input to the V <sub>CC CMOS</sub> output via the package. Future processors requiring 1.5 V CMOS voltage levels will route the 1.5 V at the V <sub>CC1.5</sub> input to the V <sub>CC CMOS</sub> output.
V <sub>CC2.5</sub> (PPGA only)	I	The V <sub>CC CMOS</sub> pin provides the CMOS voltage for use by the platform. The 2.5 V must be provided to the V <sub>CC2.5</sub> input and 1.5 V must be provided to the V <sub>CC1.5</sub> input. The processor re-routes the 2.5 V input to the V <sub>CC CMOS</sub> output via the package. Future processors requiring 1.5 V CMOS voltage levels will route the 1.5 V at the V <sub>CC1.5</sub> input to the V <sub>CC CMOS</sub> output.
V <sub>CC CMOS</sub> (PPGA only)	O	The V <sub>CC CMOS</sub> pin provides the CMOS voltage for use by the platform. The 2.5 V must be provided to the V <sub>CC2.5</sub> input and 1.5 V must be provided to the V <sub>CC1.5</sub> input. The processor re-routes the 2.5 V input to the V <sub>CC CMOS</sub> output via the package. Future processors requiring 1.5 V CMOS voltage levels will route the 1.5 V at the V <sub>CC1.5</sub> input to the V <sub>CC CMOS</sub> output.
V <sub>CORE DET</sub>	O	The V <sub>CORE DET</sub> signal will float for 2.0 V core processors and will be grounded for future processors with a lower core voltage.
VID[4:0] (S.E.P.P.)  VID[3:0] (PPGA)	O	The VID (Voltage ID) pins can be used to support automatic selection of power supply voltages. These pins are not signals, but are either an open circuit or a short circuit to VSS on the processor. The combination of opens and shorts defines the voltage required by the processor. The VID pins are needed to cleanly support voltage specification variations on Intel Celeron processors. See Table 1 for definitions of these pins. The power supply must supply the voltage that is requested by these pins, or disable itself.
V <sub>REF</sub> [7:0] (PPGA only) I	(PPGA only) I	These input signals are used by the AGTL+ inputs as a reference voltage. AGTL+ inputs are differential receivers and will use this voltage to determine whether the signal is a logic high or logic low.

Table 1. Voltage Identification Definition 1, 2, 3, 5

Processor Pins					
VID4 (S.E.P.P. Only)	VID3	VID2	VID1	VID0	V <sub>CC CMOS</sub>
0	0	0	1	1	1.90
0	0	0	1	0	1.95
0	0	0	0	1	2.00 <sup>2</sup>
0	0	0	0	0	2.05
1	1	1	1	1	No Core
1	1	1	1	0	2.1

**NOTES:**

- 0 = Processor pin connected to VSS.
- 1 = Open on processor; may be pulled up to TTL VIH on motherboard.
- The Intel® Celeron™ processor core will be powered off 2.0 V.
- VID4 applies only to the S.E.P. Package. VID[3:0] applies to both S.E.P. and PPGA packages.
- For PPGA, only the shaded area applies.

Symbol	Parameter	Min	Typ	Max	Units	Notes
V <sub>TT</sub>	Bus Termination Voltage	1.365	1.50	1.635	V	1.5 V ± 9% <sup>2</sup>
R <sub>TT</sub>	Termination Resistor		56		Ω	± 5%
V <sub>REF</sub>	Bus Reference Voltage		<sup>2</sup> / <sub>3</sub> V <sub>TT</sub>		V	± 2% <sup>3</sup>

**NOTES:**

- Unless otherwise noted, all specifications in this table apply to all Intel® Celeron™ processor frequencies.
- V<sub>TT</sub> must be held to 1.5 V ± 9%; dI<sub>CC,VTT</sub>/dt is specified in Table 4. It is recommended that V<sub>TT</sub> be held to 1.5 V ± 3% while the Intel Celeron processor system bus is idle. This is measured at the processor edge fingers.
- V<sub>REF</sub> is generated on the processor substrate to be <sup>2</sup>/<sub>3</sub> V<sub>TT</sub> nominally with the S.E.P. package. It must be created on the motherboard for processors in the PPGA package.



# 6120N N/B MAINTENANCE

## 3.2 INTEL 440ZX AGPSET HOST BRIDGE/CONTROLLER(1)

### Host Interface Signals

Name	Type	Description
CPURST#	O GTL+	<b>CPU Reset.</b> The CPURST# pin is an output from the 82443ZX. The 82443ZX generates this signal based on the PCIRST# input (from PIIX4E) and also the SUSTAT# pin in mobile mode. The CPURST# allows the CPUs to begin execution in a known state.
A[31:3]#	I/O GTL+	<b>Address Bus:</b> A[31:3]# connect to the CPU address bus. During CPU cycles, the A[31:3]# are inputs.
HD[63:0]#	I/O GTL+	<b>Host Data:</b> These signals are connected to the CPU data bus. Note that the data signals are inverted on the CPU bus.
ADS#	I/O GTL+	<b>Address Strobe:</b> The CPU bus owner asserts ADS# to indicate the first of two cycles of a request phase.
BNR#	I/O GTL+	<b>Block Next Request:</b> Used to block the current request bus owner from issuing a new request. This signal is used to dynamically control the CPU bus pipeline depth.
BPRI#	O GTL+	<b>Priority Agent Bus Request:</b> The 82443ZX is the only Priority Agent on the CPU bus. It asserts this signal to obtain the ownership of the address bus. This signal has priority over symmetric bus requests and will cause the current symmetric owner to stop issuing new transactions unless the HLOCK# signal was asserted.
BREQ0#	O GTL+	<b>Symmetric Agent Bus Request:</b> Asserted by the 82443ZX when CPURST# is asserted to configure the symmetric bus agents. BREQ0# is negated 2 host clocks after CPURST# is negated.
DBSY#	I/O GTL+	<b>Data Bus Busy:</b> Used by the data bus owner to hold the data bus for transfers requiring more than one cycle.
DEFER#	O GTL+	<b>Defer:</b> The 82443ZX generates a deferred response as defined by the rules of the 82443ZX's dynamic defer policy. The 82443ZX also uses the DEFER# signal to indicate a CPU retry response.
DRDY#	I/O GTL+	<b>Data Ready:</b> Asserted for each cycle that data is transferred.
HIT#	I/O GTL+	<b>Hit:</b> Indicates that a caching agent holds an unmodified version of the requested line. Also driven in conjunction with HITM# by the target to extend the snoop window.
HITM#	I/O GTL+	<b>Hit Modified:</b> Indicates that a caching agent holds a modified version of the requested line and that this agent assumes responsibility for providing the line. Also driven in conjunction with HIT# to extend the snoop window.
HLOCK#	I GTL+	<b>Host Lock:</b> All CPU bus cycles sampled with the assertion of HLOCK# and ADS#, until the negation of HLOCK# must be atomic, i.e. no PCI or AGP snoopable access to DRAM is allowed when HLOCK# is asserted by the CPU.

Name	Type	Description																		
HREQ[4:0]#	I/O GTL+	<b>Request Command:</b> Asserted during both clocks of request phase. In the first clock, the signals define the transaction type to a level of detail that is sufficient to begin a snoop request. In the second clock, the signals carry additional information to define the complete transaction type. The transactions supported by the 82443ZX Host Bridge are defined in the Host Interface section of this document.																		
HTRDY#	I/O GTL+	<b>Host Target Ready:</b> Indicates that the target of the CPU transaction is able to enter the data transfer phase.																		
RS[2:0]#	I/O GTL+	<b>Response Signals:</b> Indicates type of response according to the following table:  <table style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>RS[2:0]</th> <th>Response type</th> </tr> </thead> <tbody> <tr> <td>000</td> <td>Idle state</td> </tr> <tr> <td>001</td> <td>Retry response</td> </tr> <tr> <td>010</td> <td>Deferred response</td> </tr> <tr> <td>011</td> <td>Reserved (not driven by 82443ZX)</td> </tr> <tr> <td>100</td> <td>Hard Failure (not driven by 82443ZX)</td> </tr> <tr> <td>101</td> <td>No data response</td> </tr> <tr> <td>110</td> <td>Implicit Writeback</td> </tr> <tr> <td>111</td> <td>Normal data response</td> </tr> </tbody> </table>	RS[2:0]	Response type	000	Idle state	001	Retry response	010	Deferred response	011	Reserved (not driven by 82443ZX)	100	Hard Failure (not driven by 82443ZX)	101	No data response	110	Implicit Writeback	111	Normal data response
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### Host Signals Not supported by the 82443ZX

Signal	Function	Not Supported By 82443ZX
A[35:32]#	Address	Extended addressing (over 4 GB)
AERR#	Address Parity Error	Parity protection on address bus
AP[1:0]#	Address Parity	Parity protection on address bus
BINIT#	Bus Initialization	Checking for bus protocol violation and protocol recovery mechanism
DEP[7:0]#	Data Bus ECC/Parity	Enhanced data bus integrity
IEERR#	Internal Error	Direct internal error observation via IEERR# pin
INIT#	Soft Reset	Implemented by PIIX4E, BIST supported by external logic.
BERR#	Bus Error	Unrecoverable error without a bus protocol violation
RP#	Request Parity	Parity protection on ADS# and PREQ[4:0]#
RSP#	Response Parity Signal	Parity protection on RS[2:0]#

# 6120N N/B MAINTENANCE

## 3.2 INTEL 440ZX AGPSET HOST BRIDGE/CONTROLLER (2)

### DRAM Interface Signals

Name	Type	Description
RASA[3:0]# /CSA[3:0]#	O CMOS	<b>Row Address Strobe (EDO):</b> These signals are used to latch the row address on the MAXx lines into the DRAMs. Each signal is used to select one DRAM row. These signals drive the DRAM array directly without any external buffers.
RASB[3:0]# /CSB[3:0]#		<b>Chip Select (SDRAM):</b> For the memory row configured with SDRAM these pins perform the function of selecting the particular SDRAM components during the active state. Note that there are 2 copies of RAS# per physical memory row to improve the loading.
CKE[3:2]	O CMOS	CKE is used to dynamically power down inactive SDRAM rows. Note that there are 2 copies of CS# per physical memory row to reduce the loading.
CASA[7:0]# /DQMA[7:0]	O CMOS	<b>Column Address Strobe A-side (EDO):</b> The CASA[7:0]# signals are used to latch the column address on the MA[13:0] lines into the DRAMs of the A half of the memory array. These are active low signals that drive the DRAM array directly without external buffering. <b>Input/Output Data Mask A-side (SDRAM):</b> These pins control the A half of the memory array and act as synchronized output enables during read cycles and as a byte enables during write cycles.
GCKE/CKE1	O CMOS	<b>Global CKE (SDRAM):</b> Global CKE is normally used in an 82443BX 4 DIMM configuration requiring power down mode for the SDRAM. External logic must be used to implement this function in an 82443BX. This function is not supported in an 82443ZX. <b>SDRAM Clock Enable (CKE1):</b> In mobile mode, SDRAM Clock Enable is used to signal a self-refresh or power-down command to an SDRAM array when entering system suspend. CKE is also used to dynamically power down inactive SDRAM rows. The combination of SDRAMPWR (SDRAM register) and MMCONFIG (DRAMC register) determine the functioning of the CKE signals. Refer to the DRAMC register (Section 3.3.15, "DRAMC-DRAM Control Register (Device 0)" on page 3-19) for more details.
SRAS[A]#	O CMOS	<b>SDRAM Row Address Strobe (SDRAM):</b> The SRAS[A]# signal is a copy of the same logical SRASx signal (for loading purposes) used to generate SDRAM command encoded on SRASx/SCASx/WE signals.
CKE0/FENA	O CMOS	<b>SDRAM Clock Enable 0 (CKE0):</b> In mobile mode, CKE0 SDRAM Clock Enable is used to signal a self-refresh or power-down command to an SDRAM array when entering system suspend. CKE is also used to dynamically power down inactive SDRAM rows. <b>FET Enable (FENA):</b> In a 4 DIMM configuration, FENA is used to select the proper MD path through the FET switches (refer to Section 4.3, "RAM Interface" on page 4-14 for more details). This function is not supported in the 82443ZX.

Name	Type	Description
SCAS[A]#	O CMOS	<b>SDRAM Column Address Strobe (SDRAM):</b> The SCAS[A]# signal is a copy of the same logical SCASx signal (for loading purposes) used to generate SDRAM command encoded on SRASx/SCASx/WE signals.
MAA[13:0] STRAP5 STRAP4 STRAP3 STRAP2 STRAP1 STRAP0	O CMOS	<b>Memory Address(EDO/SDRAM):</b> MAA[13:0] are used to provide the row and column address to DRAM. Each MAA[13:0] line has a programmable buffer strength to optimize for different signal loading conditions. STRAP[5:0] are described in Table 2-10, Strapping Options.
WEA#	O CMOS	<b>Write Enable Signal (EDO/SDRAM):</b> WE# is asserted during writes to DRAM. The WE# lines have a programmable buffer strength to optimize for different signal loading conditions.
MD [63:0]	I/O CMOS	<b>Memory Data (EDO/SDRAM):</b> These signals are used to interface to the DRAM data bus.

### Primary PCI Interface Signals

Name	Type	Description
AD[31:0]	I/O PCI	<b>PCI Address/Data:</b> These signals are connected to the PCI address/data bus. Address is driven by the 82443ZX with FRAME# assertion, data is driven or received in the following clocks. When the 82443ZX acts as a target on the PCI Bus, the AD[31:0] signals are inputs and contain the address during the first clock of FRAME# assertion and input data (writes) or output data (reads) on subsequent clocks.
DEVSEL#	I/O PCI	<b>Device Select:</b> Device select, when asserted, indicates that a PCI target device has decoded its address as the target of the current access. The 82443ZX asserts DEVSEL# based on the DRAM address range or AGP address range being accessed by a PCI initiator. As an input it indicates whether any device on the bus has been selected.
FRAME#	I/O PCI	<b>Frame:</b> FRAME# is an output when the 82443ZX acts as an initiator on the PCI Bus. FRAME# is asserted by the 82443ZX to indicate the beginning and duration of an access. The 82443ZX asserts FRAME# to indicate a bus transaction is beginning. While FRAME# is asserted, data transfers continue. When FRAME# is negated, the transaction is in the final data phase. FRAME# is an input when the 82443ZX acts as a PCI target. As a PCI target, the 82443ZX latches the C/BE[3:0]# and the AD[31:0] signals on the first clock edge on which it samples FRAME# active.
IRDY#	I/O PCI	<b>Initiator Ready:</b> IRDY# is an output when 82443ZX acts as a PCI initiator and an input when the 82443ZX acts as a PCI target. The assertion of IRDY# indicates the current PCI Bus initiator's ability to complete the current data phase of the transaction.

# 6120N N/B MAINTENANCE

## 3.2 INTEL 440ZX AGPSET HOST BRIDGE/CONTROLLER (3)

### Primary PCI Interface Signals

Name	Type	Description																																		
C/BE[3:0]#	I/O PCI	<p><b>Command/Byte Enable:</b> PCI Bus Command and Byte Enable signals are multiplexed on the same pins. During the address phase of a transaction, C/BE[3:0]# define the bus command. During the data phase C/BE[3:0]# are used as byte enables. The byte enables determine which byte lanes carry meaningful data. PCI Bus command encoding and types are listed below.</p> <table border="1"> <thead> <tr> <th>C/BE[3:0]#</th> <th>Command Type</th> </tr> </thead> <tbody> <tr><td>0000</td><td>Interrupt Acknowledge</td></tr> <tr><td>0001</td><td>Special Cycle</td></tr> <tr><td>0010</td><td>I/O Read</td></tr> <tr><td>0011</td><td>I/O Write</td></tr> <tr><td>0100</td><td>Reserved</td></tr> <tr><td>0101</td><td>Reserved</td></tr> <tr><td>0110</td><td>Memory Read</td></tr> <tr><td>0111</td><td>Memory Write</td></tr> <tr><td>1000</td><td>Reserved</td></tr> <tr><td>1001</td><td>Reserved</td></tr> <tr><td>1010</td><td>Configuration Read</td></tr> <tr><td>1011</td><td>Configuration Write</td></tr> <tr><td>1100</td><td>Memory Read Multiple</td></tr> <tr><td>1101</td><td>Reserved (Dual Address Cycle)</td></tr> <tr><td>1110</td><td>Memory Read Line</td></tr> <tr><td>1111</td><td>Memory Write and Invalidate</td></tr> </tbody> </table>	C/BE[3:0]#	Command Type	0000	Interrupt Acknowledge	0001	Special Cycle	0010	I/O Read	0011	I/O Write	0100	Reserved	0101	Reserved	0110	Memory Read	0111	Memory Write	1000	Reserved	1001	Reserved	1010	Configuration Read	1011	Configuration Write	1100	Memory Read Multiple	1101	Reserved (Dual Address Cycle)	1110	Memory Read Line	1111	Memory Write and Invalidate
C/BE[3:0]#	Command Type																																			
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0001	Special Cycle																																			
0010	I/O Read																																			
0011	I/O Write																																			
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0110	Memory Read																																			
0111	Memory Write																																			
1000	Reserved																																			
1001	Reserved																																			
1010	Configuration Read																																			
1011	Configuration Write																																			
1100	Memory Read Multiple																																			
1101	Reserved (Dual Address Cycle)																																			
1110	Memory Read Line																																			
1111	Memory Write and Invalidate																																			
PAR	I/O PCI	<p><b>Parity:</b> PAR is driven by the 82443ZX when it acts as a PCI initiator during address and data phases for a write cycle, and during the address phase for a read cycle. PAR is driven by the 82443ZX when it acts as a PCI target during each data phase of a PCI memory read cycle. Even parity is generated across AD[31:0] and C/BE[3:0]#.</p>																																		
PLOCK#	I/O PCI	<p><b>Lock:</b> PLOCK# indicates an exclusive bus operation and may require multiple transactions to complete. When PLOCK# is asserted, non-exclusive transactions may proceed. The 82443ZX supports lock for CPU initiated cycles only. PCI initiated locked cycles are not supported.</p>																																		
TRDY#	I/O PCI	<p><b>Target Ready:</b> TRDY# is an input when the 82443ZX acts as a PCI initiator and an output when the 82443ZX acts as a PCI target. The assertion of TRDY# indicates the target agent's ability to complete the current data phase of the transaction.</p>																																		

Name	Type	Description
SERR#	I/O PCI	<p><b>System Error:</b> The 82443ZX asserts this signal to indicate an error condition. The SERR# assertion by the 82443ZX is enabled globally via SERRE bit of the PCICMD register. SERR# is asserted under the following conditions:</p> <p>In an ECC configuration, the 82443ZX asserts SERR#, for single bit (correctable) ECC errors or multiple bit (non-correctable) ECC errors if SERR# signaling is enabled via the ERRCMD control register. Any ECC errors received during initialization should be ignored.</p> <ul style="list-style-type: none"> <li>The 82443ZX asserts SERR# for one clock when it detects a target abort during 82443ZX initiated PCI cycle.</li> <li>The 82443ZX can also assert SERR# when a PCI parity error occurs during the address or data phase.</li> <li>The 82443ZX can assert SERR# when it detects a PCI address or data parity error on AGP.</li> <li>The 82443ZX can assert SERR# upon detection of access to an invalid entry in the Graphics Aperture Translation Table.</li> <li>The 82443ZX can assert SERR# upon detecting an invalid AGP master access outside of AGP aperture and outside of main DRAM range (i.e. in the 640k - 1M range or above TOM).</li> <li>The 82443ZX can assert SERR# upon detecting an invalid AGP master access outside of AGP aperture.</li> <li>The 82443ZX asserts SERR# for one clock when it detects a target abort during 82443ZX initiated AGP cycle.</li> </ul>
STOP#	I/O PCI	<p><b>Stop:</b> STOP# is an input when the 82443ZX acts as a PCI initiator and an output when the 82443ZX acts as a PCI target. STOP# is used for disconnect, retry, and abort sequences on the PCI Bus.</p>

### Primary PCI Sideband Interface Signals

Name	Type	Description
PHOLD#	I PCI	<p><b>PCI Hold:</b> This signal comes from the PIIX4E. It is the PIIX4E request for PCI bus ownership. The 82443ZX will flush and disable the CPU-to-PCI write buffers before granting the PIIX4E the PCI bus via PHLDA#. This prevents bus deadlock between PCI and ISA.</p>
PHLDA#	O PCI	<p><b>PCI Hold Acknowledge:</b> This signal is driven by the 82443ZX to grant PCI bus ownership to the PIIX4E after CPU-PCI post buffers have been flushed and disabled.</p>
PREQ[3:0]#	I PCI	<p><b>PCI Bus Request:</b> PREQ[3:0]# are the PCI bus request signals used as inputs by the internal PCI arbiter.</p>
PGNT[3:0]#	O PCI	<p><b>PCI Grant:</b> PGNT[3:0]# are the PCI bus grant output signals generated by the internal PCI arbiter.</p>

# 6120N N/B MAINTENANCE

## 3.2 INTEL 440ZX AGPSET HOST BRIDGE/CONTROLLER (4)

### Primary PCI Sideband Interface Signals

Name	Type	Description
PHOLD#	I PCI	<b>PCI Hold:</b> This signal comes from the PIIX4E. It is the PIIX4E request for PCI bus ownership. The 82443ZX will flush and disable the CPU-to-PCI write buffers before granting the PIIX4E the PCI bus via PHLDA#. This prevents bus deadlock between PCI and ISA.
PHLDA#	O PCI	<b>PCI Hold Acknowledge:</b> This signal is driven by the 82443ZX to grant PCI bus ownership to the PIIX4E after CPU-PCI post buffers have been flushed and disabled.
PREQ[3:0]#	I PCI	<b>PCI Bus Request:</b> PREQ[3:0]# are the PCI bus request signals used as inputs by the internal PCI arbiter.
PGNT[3:0]#	O PCI	<b>PCI Grant:</b> PGNT[3:0]# are the PCI bus grant output signals generated by the internal PCI arbiter.

### AGP Interface Signals

Name	Type	Description
<b>AGP Sideband Addressing Signals 1</b>		
PIPE#	I AGP	<b>Pipelined Read:</b> This signal is asserted by the current master to indicate a full width address is to be queued by the target. The master queues one request each rising clock edge while PIPE# is asserted. When PIPE# is deasserted no new requests are queued across the AD bus. PIPE# is a sustained tri-state signal from masters (graphics controller) and is an input to the 82443ZX. Note that initial AGP designs may not use PIPE#.
SBA[7:0]	I AGP	<b>Sideband Address:</b> This bus provides an additional bus to pass address and command to the 82443ZX from the AGP master. Note that, when sideband addressing is disabled, these signals are isolated (no external/internal pull-ups are required).
<b>AGP Flow Control Signals</b>		
RBF#	I AGP	<b>Read Buffer Full.</b> This signal indicates if the master is ready to accept previously requested low priority read data. When RBF# is asserted the 82443ZX is not allowed to return low priority read data to the AGP master on the first block. RBF# is only sampled at the beginning of a cycle. If the AGP master is always ready to accept return read data then it is not required to implement this signal.

Name	Type	Description
<b>AGP Status Signals</b>		
ST[2:0]	O AGP	<b>Status Bus:</b> This bus provides information from the arbiter to a AGP Master on what it may do. ST[2:0] only have meaning to the master when its GGNT# is asserted. When GGNT# is deasserted these signals have no meaning and must be ignored. 000 Indicates that previously requested low priority read data is being returned to the master. 001 Indicates that previously requested high priority read data is being returned to the master. 010 Indicates that the master is to provide low priority write data for a previously queued write command. 011 Indicates that the master is to provide high priority write data for a previously queued write command. 100 Reserved 101 Reserved 110 Reserved 111 Indicates that the master has been given permission to start a bus transaction. The master may queue AGP requests by asserting PIPE# or start a PCI transaction by asserting FRAME#. ST[2:0] are always an output from the 82443ZX and an input to the master.
<b>AGP Clocking Signals - Strobes</b>		
ADSTB_A	I/O AGP	<b>AD Bus Strobe A:</b> This signal provides timing for double clocked data on the AD bus. The agent that is providing data drives this signal. This signal requires an 8.2K ohm external pull-up resistor.
<b>AGP Clocking Signals - Strobes</b>		
ADSTB_B	I/O AGP	<b>AD Bus Strobe B:</b> This signal is an additional copy of the AD_STBA signal. This signal requires an 8.2K ohm external pull-up resistor.
SBSTB	I AGP	<b>Sideband Strobe:</b> This signal provides timing for a side-band bus. This signal requires an 8.2K ohm external pull-up resistor.
<b>AGP FRAME# Protocol Signals (similar to PCI)2</b>		
GFRAME#	I/O AGP	<b>Graphics Frame:</b> Same as PCI. Not used by AGP. GFRAME# remains deasserted by its own pull up resistor.

# 6120N N/B MAINTENANCE

## 3.2 INTEL 440ZX AGPSET HOST BRIDGE/CONTROLLER (5)

### AGP Interface Signals

Name	Type	Description
GIRDY#	I/O AGP	<b>Graphics Initiator Ready:</b> New meaning. GIRDY# indicates the AGP compliant master is ready to provide all write data for the current transaction. Once IRDY# is asserted for a write operation, the master is not allowed to insert wait states. The assertion of IRDY# for reads indicates that the master is ready to transfer to a subsequent block (32 bytes) of read data. The master is never allowed to insert wait states during the initial data transfer (32 bytes) of a read transaction. However, it may insert wait states after each 32 byte block is transferred. (There is no GFRAME# -- GIRDY# relationship for AGP transactions.)
GTRDY#	I/O AGP	<b>Graphics Target Ready:</b> New meaning. GTRDY# indicates the AGP compliant target is ready to provide read data for the entire transaction (when the transfer size is less than or equal to 32 bytes) or is ready to transfer the initial or subsequent block (32 bytes) of data when the transfer size is greater than 32 bytes. The target is allowed to insert wait states after each block (32 bytes) is transferred on both read and write transactions.
GSTOP#	I/O AGP	<b>Graphics Stop:</b> Same as PCI. Not used by AGP.
GDEVSEL#	I/O AGP	<b>Graphics Device Select:</b> Same as PCI. Not used by AGP.
GREQ#	I AGP	<b>Graphics Request:</b> Same as PCI. (Used to request access to the bus to initiate a PCI or AGP request.)
GGNT#	O AGP	<b>Graphics Grant:</b> Same meaning as PCI but additional information is provided on ST[2:0]. The additional information indicates that the selected master is the recipient of previously requested read data (high or normal priority), it is to provide write data (high or normal priority), for a previously queued write command or has been given permission to start a bus transaction (AGP or PCI).
GAD[31:0]	I/O AGP	<b>Graphics Address/Data:</b> Same as PCI.
GC/BE[3:0]#	I/O AGP	<b>Graphics Command/Byte Enables:</b> Slightly different meaning. Provides command information (different commands than PCI) when requests are being queued when using PIPE#. Provide valid byte information during AGP write transactions and are not used during the return of read data.
GPAR	I/O AGP	<b>Graphics Parity:</b> Same as PCI. Not used on AGP transactions, but used during PCI transactions as defined by the PCI specification.

### Clocks, Reset, and Miscellaneous

Name	Type	Description
HCLKIN	I CMOS	<b>Host Clock In:</b> This pin receives a buffered host clock. This clock is used by all of the 82443ZX logic that is in the Host clock domain.
PCLKIN	I CMOS	<b>PCI Clock In:</b> This is a buffered PCI clock reference that is synchronously derived by an external clock synthesizer component from the host clock. This clock is used by all of the 82443ZX logic that is in the PCI clock domain.
DCLKO	O CMOS	<b>SDRAM Clock Out:</b> 66 or 100 MHz SDRAM clock reference. It feeds an external buffer clock device that produces multiple copies for the DIMMs.
DCLKWR	I CMOS	<b>SDRAM Write Clock:</b> Feedback reference from the external SDRAM clock buffer. This clock is used by the 82443ZX when writing data to the SDRAM array. Note: See the Design Guide for routing constraints.
PCIRST#	I CMOS	<b>PCI Reset:</b> When asserted, this signal will reset the 82443ZX logic. All PCI output and bi-directional signals will also tri-state compliant to PCI Rev 2.0 and 2.1 specifications.
GCLKIN	I CMOS	<b>AGP Clock In:</b> The GCLKIN input is a feedback reference from the GCLKOUT signal.
GCLKO	O CMOS	<b>AGP Clock Out:</b> The frequency is 66 MHz. The GCLKOUT output is used to feed both the reference input pin on the 82443ZX and the AGP compliant device.
CRESET#	O CMOS	<b>Delayed CPU Reset:</b> CRESET# is a delayed copy of CPURST#. This signal is used to control the multiplexer for the CPU strap signals. CRESET# is delayed from CPURST# by two host clocks. Note: This pin requires an external pull-up resistor. If not used, no pull up is required.
TESTIN#	I CMOS	<b>Test Input:</b> This pin is used for manufacturing, and board level test purposes. Note: This pin has an internal 50K ohm pull-up.

### Power Management Interface

Name	Type	Description
CLKRUN#	I/OD CMOS	<b>Primary PCI Clock Run:</b> The 82443ZX requests the central resource (PIIX4E) to start or maintain the PCI clock by the assertion of CLKRUN#. The 82443ZX tristates CLKRUN# upon deassertion of PCIRST# (since CLK is running upon deassertion of reset). If connected to PIIX4E an external 2.7K Ohm pull-up is required for Desktop, Mobile requires (8.2k-10K) pull-up. Otherwise, a 100 Ohm pull down is required.
BXPWROK	I CMOS	<b>BX Power OK:</b> BXPWROK input must be connected to the PWROK signal that indicates valid power is applied to the 82443ZX.

# 6120N N/B MAINTENANCE

## 3.2 INTEL 440ZX AGPSET HOST BRIDGE/CONTROLLER (6)

### Reference Pins

Name	Description
GTLREF[B:A]	GTL Buffer voltage reference input
VTT[B:A]	GTL Threshold voltage for early clamps
VCC	Power pin @ 3.3V
VSS	Ground
REF5V	PCI 5V reference voltage (for 5V tolerant buffers)
AGPREF	External Input Reference

### Strapping Options

Signal	Register Name[bit]	Description
MAB13#		<b>Reserved.</b>
STRAP5	NBXCFC[13]	<b>Host Frequency Select:</b> If STRAP5 is strapped to 0, the host bus frequency is 60/ 66 MHz. If STRAP5 is strapped to 1, the host bus frequency is 100 MHz. An internal pull-down is used to provide the default setting of 66 MHz.
STRAP4	NBXCFC[2]	<b>In-Order Queue Depth Enable.</b> If STRAP4 is strapped to 0 during the rising edge of PCIRST#, then the 82442BX will drive A7# low during the CPURST# deassertion. This forces the CPU bus to be configured for non-pipelined operation. If STRAP4 is strapped to 1 (default), then the 82443ZX does not drive the A7# low during reset, and A7# is sampled in default non-driven state (i.e. pulled-up as far as GTL+ termination is concerned) then the maximum allowable queue depth by the CPU bus protocol is selected (i.e., 8). Note that internal pull-up is used to provide pipelined bus mode as a default.
STRAP3	PMCR[3]	<b>Quick Start Select.</b> The value on this pin at reset determines which stop clock mode is used. STRAP3 = 0 (default) for normal stop clock mode. If STRAP3 = 1 during the rising edge of PCIRST#, then the 82443ZX will drive A15# low during CPURST# deassertion. This will configure the CPU for Quick Start mode of operation. Note that internal pull-down is used to provide normal stop clock mode as a default.
STRAP2	PMCR[1]	<b>AGP Disable:</b> When strapped to a 1, the AGP interface is disabled, all AGP signals are tri-stated and isolated. When strapped to a 0 (default), the AGP interface is enabled. When MMCONFIG is strapped active, we require that AGP_DISABLE is also strapped active. When MMCONFIG is strapped inactive, AGP_DISABLE can be strapped active or inactive but IDSEL_REDIRECT (bit 16 in NBXCFC register) must never be activated. This signal has an internal pull-down resistor.

Signal	Register Name[bit]	Description
MAB8#		<b>Reserved.</b>
STRAP1	DRAMC[5]	<b>Memory Module Configuration, MMCONFIG:</b> When strapped to a 1, the 82443ZX configures its DRAM interface in a 430-TX compatible manner. These unused inputs are isolated while unused outputs are tri-stated: RASB[3:0]#/CSB[3:0]#, CKE[3:2], GCKE/CKE1, MAA[13:0], DCLKO. When strapped to a 0 (default), the 82443ZX DRAM signal are used normally. IDSEL_REDIRECT (bit 16 in NBXCFC register) is programmed by BIOS, before it begins with device enumeration process. The combination of SDRAMPWR (SDRAMC register) and MMCONFIG (DRAMC register) determine the functioning of the CKE signals. Refer to the DRAMC register for more details. Note that internal pull-down is used to set the DRAM interface to a normal configuration, as a default.
STRAP0	none	<b>Host Bus Buffer Mode Select:</b> When strapped 0, the desktop GTL+ 66 MHz or 100 MHz host bus buffers are used (default). When strapped '1' the mobile Low Power GTL+ 66 MHz host bus buffers are selected. Note that an internal pull-down is used to set the host bus buffers to a desktop configuration as a default in the 82443ZX. An external pull-up therefore is needed for mobile systems using the 82443BX or 82443DX.
A[15]#	none	<b>Quick Start Select.</b> The value on A15# sampled at the rising edge of CPURST# will reflect if the quick start/stop clock mode is enabled in the processors.
A7#	none	<b>In-order Queue Depth Status.</b> The value on A[7]# sampled at the rising edge of CPURST# reflects if the IOQD is set to 1 or maximum allowable by the CPU bus.

# 6120N N/B MAINTENANCE

## 3.3 INTEL 82371EB PCI-TO-ISA / IDE XCELERATOR (PIIX4) (1).

SIGNAL	TYPE	DESCRIPTION
AD[31:0]	I/O	<b>PCI ADDRESS/DATA.</b> AD[31:0] is a multiplexed address and data bus. During the first clock of a transaction, AD[31:0] contain a physical byte address (32 bits). During subsequent clocks, AD[31:0] contain data. A PIIX4 Bus transaction consists of an address phase followed by one or more data phases. Little-endian byte ordering is used. AD[7:0] define the least significant byte (LSB) and AD[31:24] the most significant byte (MSB). When PIIX4 is a Target, AD[31:0] are inputs during the address phase of a transaction. During the following data phase(s), PIIX4 may be asked to supply data on AD[31:0] for a PCI read, or accept data for a PCI write. As an Initiator, PIIX4 drives a valid address on AD[31:2] and 0 on AD[1:0] during the address phase, and drives write or latches read data on AD[31:0] during the data phase. <b>During Reset: High-Z After Reset: High-Z During POS: High-Z</b>
C/BE#[3:0]	I/O	<b>BUS COMMAND AND BYTE ENABLES.</b> The command and byte enable signals are multiplexed on the same PCI pins. During the address phase of a transaction, C/BE[3:0]# define the bus command. During the data phase C/BE[3:0]# are used as Byte Enables. The Byte Enables determine which byte lanes carry meaningful data. C/BE0# applies to byte 0, C/BE1# to byte 1, etc. PIIX4 drives C/BE[3:0]# as an Initiator and monitors C/BE[3:0]# as a Target. <b>During Reset: High-Z After Reset: High-Z During POS: High-Z</b>
CLKRUN#	I/O	<b>CLOCK RUN#.</b> This signal is used to communicate to PCI peripherals that the PCI clock will be stopped. Peripherals can assert CLKRUN# to request that the PCI clock be restarted or to keep it from stopping. This function follows the protocol described in the PCI Mobile Design Guide, Revision 1.0. <b>During Reset: Low After Reset: Low During POS: High</b>
DEVSEL#	I/O	<b>DEVICE SELECT.</b> PIIX4 asserts DEVSEL# to claim a PCI transaction through positive decoding or subtractive decoding (if enabled). As an output, PIIX4 asserts DEVSEL# when it samples IDSEL active in configuration cycles to PIIX4 configuration registers. PIIX4 also asserts DEVSEL# when an internal PIIX4 address is decoded or when PIIX4 subtractively or positively decodes a cycle for the ISA/EIO bus or IDE device. As an input, DEVSEL# indicates the response to a PIIX4 initiated transaction and is also sampled when deciding whether to subtractively decode the cycle. DEVSEL# is tri-stated from the leading edge of PCIRST#. DEVSEL# remains tri-stated until driven by PIIX4 as a target. <b>During Reset: High-Z After Reset: High-Z During POS: High-Z</b>
FRAME#	I/O	<b>CYCLE FRAME.</b> FRAME# is driven by the current Initiator to indicate the beginning and duration of an access. While FRAME# is asserted data transfers continue. When FRAME# is negated the transaction is in the final data phase. FRAME# is an input to PIIX4 when it is the Target. FRAME# is an output when PIIX4 is the initiator. FRAME# remains tri-stated until driven by PIIX4 as an Initiator. <b>During Reset: High-Z After Reset: High-Z During POS: High-Z</b>

SIGNAL	TYPE	DESCRIPTION
IRDY#	I/O	<b>INITIATOR READY.</b> IRDY# indicates PIIX4's ability, as an Initiator, to complete the current data phase of the transaction. It is used in conjunction with TRDY#. A data phase is completed on any clock both IRDY# and TRDY# are sampled asserted. During a write, IRDY# indicates PIIX4 has valid data present on AD[31:0]. During a read, it indicates PIIX4 is prepared to latch data. IRDY# is an input to PIIX4 when PIIX4 is the Target and an output when PIIX4 is an Initiator. IRDY# remains tri-stated until driven by PIIX4 as a master.
IDSEL	I	<b>INITIALIZATION DEVICE SELECT.</b> IDSEL is used as a chip select during PCI configuration read and write cycles. PIIX4 samples IDSEL during the address phase of a transaction. If IDSEL is sampled active, and the bus command is a configuration read or write, PIIX4 responds by asserting DEVSEL# on the next cycle. <b>PAR O CALCULATED PARITY SIGNAL.</b> PAR is even parity and is calculated on 36 bits; AD[31:0] plus C/BE[3:0]#. Even parity means that the number of 1's within the 36 bits plus PAR are counted and the sum is always even. PAR is always calculated on 36 bits regardless of the valid byte enables. PAR is generated for address and data phases and is only guaranteed to be valid one PCI clock after the corresponding address or data phase. PAR is driven and tri-stated identically to the AD[31:0] lines except that PAR is delayed by exactly one PCI clock. PAR is an output during the address phase (delayed one clock) for all PIIX4 initiated transactions. It is also an output during the data phase (delayed one clock) when PIIX4 is the Initiator of a PCI write transaction, and when it is the Target of a read transaction. <b>During Reset: High-Z After Reset: High-Z During POS: High-Z</b>
PCIRST#	O	<b>PCI RESET.</b> PIIX4 asserts PCIRST# to reset devices that reside on the PCI bus. PIIX4 asserts PCIRST# during power-up and when a hard reset sequence is initiated through the RC register. PCIRST# is driven inactive a minimum of 1 ms after PWROK is driven active. PCIRST# is driven for a minimum of 1 ms when initiated through the RC register. PCIRST# is driven asynchronously relative to PCICLK. <b>During Reset: Low After Reset: High During POS: High</b>
PHOLD#	O	<b>PCI HOLD.</b> An active low assertion indicates that PIIX4 desires use of the PCI Bus. Once the PCI arbiter has asserted PHLDA# to PIIX4, it may not negate it until PHOLD# is negated by PIIX4. PIIX4 implements the passive release mechanism by toggling PHOLD# inactive for one PCICLK. <b>During Reset: High-Z After Reset: High During POS: High</b>
PHLDA#	I	<b>PCI HOLD ACKNOWLEDGE.</b> An active low assertion indicates that PIIX4 has been granted use of the PCI Bus. Once PHLDA# is asserted, it cannot be negated unless PHOLD# is negated first.
SERR#	I/O	<b>SYSTEM ERROR.</b> SERR# can be pulsed active by any PCI device that detects a system error condition. Upon sampling SERR# active, PIIX4 can be programmed to generate a non-maskable interrupt (NMI) to the CPU. <b>During Reset: High-Z After Reset: High-Z During POS: High-Z</b>

# 6120N N/B MAINTENANCE

## 3.3 INTEL 82371EB PCI-TO-ISA / IDE XCELERATOR (PIIX4) (2).

SIGNAL	TYPE	DESCRIPTION
STOP#	I/O	<b>STOP.</b> STOP# indicates that PIIX4, as a Target, is requesting an initiator to stop the current transaction. As an Initiator, STOP# causes PIIX4 to stop the current transaction. STOP# is an output when PIIX4 is a Target and an input when PIIX4 is an Initiator. STOP# is tri-stated from the leading edge of PCIRST#. STOP# remains tri-stated until driven by PIIX4 as a slave. <b>During Reset: High-Z After Reset: High-Z During POS: High-Z</b>
TRDY#	I/O	<b>TARGET READY.</b> TRDY# indicates PIIX4 ability to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#. A data phase is completed when both TRDY# and IRDY# are sampled asserted. During a read, TRDY# indicates that PIIX4, as a Target, has place valid data on AD[31:0]. During a write, it indicates PIIX4, as a Target is prepared to latch data. TRDY# is an input to PIIX4 when PIIX4 is the Initiator and an output when PIIX4 is a Target. TRDY# is tri-stated from the leading edge of PCIRST#. TRDY# remains tri-stated until driven by PIIX4 as a slave. <b>During Reset: High-Z After Reset: High-Z During POS: High-Z</b>
AEN	O	<b>ADDRESS ENABLE.</b> AEN is asserted during DMA cycles to prevent I/O slaves from misinterpreting DMA cycles as valid I/O cycles. When negated, AEN indicates that an I/O slave may respond to address and I/O commands. When asserted, AEN informs I/O resources on the ISA bus that a DMA transfer is occurring. This signal is also driven high during PIIX4 initiated refresh cycles. <b>During Reset: High-Z After Reset: Low During POS: Low</b> <b>BALE O BUS ADDRESS LATCH ENABLE.</b> BALE is asserted by PIIX4 to indicate that the address (SA[19:0], LA[23:17]) and SBHE# signal lines are valid. The LA[23:17] address lines are latched on the trailing edge of BALE. BALE remains asserted throughout DMA and ISA master cycles. <b>During Reset: High-Z After Reset: Low During POS: Low</b>
IOCHK#/GPIO	I	<b>I/O CHANNEL CHECK.</b> IOCHK# can be driven by any resource on the ISA bus. When asserted, it indicates that a parity or an uncorrectable error has occurred for a device or memory on the ISA bus. A NMI will be generated to the CPU if the NMI generation is enabled. If the EIO bus is used, this signal becomes a general purpose input.
IOCHRDY	I/O	<b>I/O CHANNEL READY.</b> Resources on the ISA Bus negate IOCHRDY to indicate that wait states are required to complete the cycle. This signal is normally high. IOCHRDY is an input when PIIX4 owns the ISA Bus and the CPU or a PCI agent is accessing an ISA slave, or during DMA transfers. IOCHRDY is output when an external ISA Bus Master owns the ISA Bus and is accessing DRAM or a PIIX4 register. As a PIIX4 output, IOCHRDY is driven inactive (low) from the falling edge of the ISA commands. After data is available for an ISA master read or PIIX4 latches the data for a write cycle, IOCHRDY is asserted for 70 ns. After 70 ns, PIIX4 floats IOCHRDY. The 70 ns includes both the drive time and the time it takes PIIX4 to float IOCHRDY. PIIX4 does not drive this signal when an ISA Bus master is accessing an ISA Bus slave. <b>During Reset: High-Z After Reset: High-Z During POS: High-Z</b>

SIGNAL	TYPE	DESCRIPTION
IOCS16#	I	<b>16-BIT I/O CHIP SELECT.</b> This signal is driven by I/O devices on the ISA Bus to indicate support for 16-bit I/O bus cycles.
IOR#	I/O	<b>I/O READ.</b> IOR# is the command to an ISA I/O slave device that the slave may drive data on to the ISA data bus (SD[15:0]). The I/O slave device must hold the data valid until after IOR# is negated. IOR# is an output when PIIX4 owns the ISA Bus. IOR# is an input when an external ISA master owns the ISA Bus. <b>During Reset: High-Z After Reset: High During POS: High</b>
IOW#	I/O	<b>I/O WRITE.</b> IOW# is the command to an ISA I/O slave device that the slave may latch data from the ISA data bus (SD[15:0]). IOW# is an output when PIIX4 owns the ISA Bus. IOW# is an input when an external ISA master owns the ISA Bus. <b>During Reset: High-Z After Reset: High During POS: High</b>
LA[23:17]/GPO[7:1]	I/O	<b>ISA LA[23:17].</b> LA[23:17] address lines allow accesses to physical memory on the ISA Bus up to 16 Mbytes. LA[23:17] are outputs when PIIX4 owns the ISA Bus. The LA[23:17] lines become inputs whenever an ISA master owns the ISA Bus. If the EIO bus is used, these signals become a general purpose output. <b>During Reset: High-Z After Reset: Undefined During POS: Last LA/GPO</b>
MEMCS16#	I/O	<b>MEMORY CHIP SELECT 16.</b> MEMCS16# is a decode of LA[23:17] without any qualification of the command signal lines. ISA slaves that are 16-bit memory devices drive this signal low. PIIX4 ignores MEMCS16# during I/O access cycles and refresh cycles. MEMCS16# is an input when PIIX4 owns the ISA Bus. PIIX4 drives this signal low during ISA master to PCI memory cycles.
MEMR#	I/O	<b>MEMORY READ.</b> MEMR# is the command to a memory slave that it may drive data onto the ISA data bus. MEMR# is an output when PIIX4 is a master on the ISA Bus. MEMR# is an input when an ISA master, other than PIIX4, owns the ISA Bus. This signal is also driven by PIIX4 during refresh cycles. For DMA cycles, PIIX4, as a master, asserts MEMR#. <b>During Reset: High-Z After Reset: High During POS: High</b>
MEMW#	I/O	<b>MEMORY WRITE.</b> MEMW# is the command to a memory slave that it may latch data from the ISA data bus. MEMW# is an output when PIIX4 owns the ISA Bus. MEMW# is an input when an ISA master, other than PIIX4, owns the ISA Bus. For DMA cycles, PIIX4, as a master, asserts MEMW#. <b>During Reset: High-Z After Reset: High During POS: High</b>

# 6120N N/B MAINTENANCE

## 3.3 INTEL 82371EB PCI-TO-ISA / IDE XCELERATOR (PIIX4) (3).

SIGNAL	TYPE	DESCRIPTION
REFRESH#	I/O	<b>REFRESH.</b> As an output, REFRESH# is used by PIIX4 to indicate when a refresh cycle is in progress. It should be used to enable the SA[7:0] address to the row address inputs of all banks of dynamic memory on the ISA Bus. Thus, when MEMR# is asserted, the entire expansion bus dynamic memory is refreshed. Memory slaves must not drive any data onto the bus during refresh. As an output, this signal is driven directly onto the ISA Bus. This signal is an output only when PIIX4 DMA refresh controller is a master on the bus responding to an internally generated request for refresh. As an input, REFRESH# is driven by 16-bit ISA Bus masters to initiate refresh cycles. <b>During Reset: High-Z After Reset: High During POS: High</b>
RSTDRV	O	<b>RESET DRIVE.</b> PIIX4 asserts RSTDRV to reset devices that reside on the ISA/EIO Bus. PIIX4 asserts this signal during a hard reset and during power-up. RSTDRV is asserted during power-up and negated after PWROK is driven active. RSTDRV is also driven active for a minimum of 1 ms if a hard reset has been programmed in the RC register. <b>During Reset: High After Reset: Low During POS: Low</b>
SA[19:0]	I/O	<b>SYSTEM ADDRESS[19:0].</b> These bi-directional address lines define the selection with the granularity of 1 byte within the 1-Megabyte section of memory defined by the LA[23:17] address lines. The address lines SA[19:17] that are coincident with LA[19:17] are defined to have the same values as LA[19:17] for all memory cycles. For I/O accesses, only SA[15:0] are used, and SA[19:16] are undefined. SA[19:0] are outputs when PIIX4 owns the ISA Bus. SA[19:0] are inputs when an external ISA Master owns the ISA Bus. <b>During Reset: High-Z After Reset: Undefined During POS: Last SA</b>
SBHE#	I/O	<b>SYSTEM BYTE HIGH ENABLE.</b> SBHE# indicates, when asserted, that a byte is being transferred on the upper byte (SD[15:8]) of the data bus. SBHE# is negated during refresh cycles. SBHE# is an output when PIIX4 owns the ISA Bus. SBHE# is an input when an external ISA master owns the ISA Bus. <b>During Reset: High-Z After Reset: Undefined During POS: High</b>
SD[15:0]	I/O	<b>SYSTEM DATA.</b> SD[15:0] provide the 16-bit data path for devices residing on the ISA Bus. SD[15:8] correspond to the high order byte and SD[7:0] correspond to the low order byte. SD[15:0] are undefined during refresh. <b>During Reset: High-Z After Reset: Undefined During POS: High-Z</b>
SMEMR#	O	<b>STANDARD MEMORY READ.</b> PIIX4 asserts SMEMR# to request an ISA memory slave to drive data onto the data lines. If the access is below the 1-Mbyte range (0000000h?00FFFFFFh) during DMA compatible, PIIX4 master, or ISA master cycles, PIIX4 asserts SMEMR#. SMEMR# is a delayed version of MEMR#.

SIGNAL	TYPE	DESCRIPTION
AEN	O	<b>ADDRESS ENABLE.</b> AEN is asserted during DMA cycles to prevent I/O slaves from misinterpreting DMA cycles as valid I/O cycles. When negated, AEN indicates that an I/O slave may respond to address and I/O commands. When asserted, AEN informs I/O resources on the ISA bus that a DMA transfer is occurring. This signal is also driven high during PIIX4 initiated refresh cycles. <b>During Reset: High-Z After Reset: Low During POS: Low</b> <b>BALE O BUS ADDRESS LATCH ENABLE.</b> BALE is asserted by PIIX4 to indicate that the address (SA[19:0], LA[23:17]) and SBHE# signal lines are valid. The LA[23:17] address lines are latched on the trailing edge of BALE. BALE remains asserted throughout DMA and ISA master cycles. <b>During Reset: High-Z After Reset: Low During POS: Low</b>
IOCHK#/ GPIO	I	<b>I/O CHANNEL CHECK.</b> IOCHK# can be driven by any resource on the ISA bus. When asserted, it indicates that a parity or an uncorrectable error has occurred for a device or memory on the ISA bus. A NMI will be generated to the CPU if the NMI generation is enabled. If the EIO bus is used, this signal becomes a general purpose input.
IOCHRDY	I/O	<b>I/O CHANNEL READY.</b> Resources on the ISA Bus negate IOCHRDY to indicate that wait states are required to complete the cycle. This signal is normally high. IOCHRDY is an input when PIIX4 owns the ISA Bus and the CPU or a PCI agent is accessing an ISA slave, or during DMA transfers. IOCHRDY is output when an external ISA Bus Master owns the ISA Bus and is accessing DRAM or a PIIX4 register. As a PIIX4 output, IOCHRDY is driven inactive (low) from the falling edge of the ISA commands. After data is available for an ISA master read or PIIX4 latches the data for a write cycle, IOCHRDY is asserted for 70 ns. After 70 ns, PIIX4 floats IOCHRDY. The 70 ns includes both the drive time and the time it takes PIIX4 to float IOCHRDY. PIIX4 does not drive this signal when an ISA Bus master is accessing an ISA Bus slave. <b>During Reset: High-Z After Reset: High-Z During POS: High-Z</b>
IOCS16#	I	<b>16-BIT I/O CHIP SELECT.</b> This signal is driven by I/O devices on the ISA Bus to indicate support for 16-bit I/O bus cycles.
IOR#	I/O	<b>I/O READ.</b> IOR# is the command to an ISA I/O slave device that the slave may drive data on to the ISA data bus (SD[15:0]). The I/O slave device must hold the data valid until after IOR# is negated. IOR# is an output when PIIX4 owns the ISA Bus. IOR# is an input when an external ISA master owns the ISA Bus. <b>During Reset: High-Z After Reset: High During POS: High</b>
IOW#	I/O	<b>I/O WRITE.</b> IOW# is the command to an ISA I/O slave device that the slave may latch data from the ISA data bus (SD[15:0]). IOW# is an output when PIIX4 owns the ISA Bus. IOW# is an input when an external ISA master owns the ISA Bus. <b>During Reset: High-Z After Reset: High During POS: High</b>

# 6120N N/B MAINTENANCE

## 3.3 INTEL 82371EB PCI-TO-ISA / IDE XCELERATOR (PIIX4) (4).

SIGNAL	TYPE	DESCRIPTION
LA[23:17]/GPO[7:1]	I/O	<b>ISA LA[23:17].</b> LA[23:17] address lines allow accesses to physical memory on the ISA Bus up to 16 Mbytes. LA[23:17] are outputs when PIIX4 owns the ISA Bus. The LA[23:17] lines become inputs whenever an ISA master owns the ISA Bus. If the EIO bus is used, these signals become a general purpose output. <b>During Reset: High-Z After Reset: Undefined During POS: Last LA/GPO</b>
MEMCS16#	I/O	<b>MEMORY CHIP SELECT 16.</b> MEMCS16# is a decode of LA[23:17] without any qualification of the command signal lines. ISA slaves that are 16-bit memory devices drive this signal low. PIIX4 ignores MEMCS16# during I/O access cycles and refresh cycles. MEMCS16# is an input when PIIX4 owns the ISA Bus. PIIX4 drives this signal low during ISA master to PCI memory cycles.
MEMR#	I/O	<b>MEMORY READ.</b> MEMR# is the command to a memory slave that it may drive data onto the ISA data bus. MEMR# is an output when PIIX4 is a master on the ISA Bus. MEMR# is an input when an ISA master, other than PIIX4, owns the ISA Bus. This signal is also driven by PIIX4 during refresh cycles. For DMA cycles, PIIX4, as a master, asserts MEMR#. <b>During Reset: High-Z After Reset: High During POS: High</b>
MEMW#	I/O	<b>MEMORY WRITE.</b> MEMW# is the command to a memory slave that it may latch data from the ISA data bus. MEMW# is an output when PIIX4 owns the ISA Bus. MEMW# is an input when an ISA master, other than PIIX4, owns the ISA Bus. For DMA cycles, PIIX4, as a master, asserts MEMW#. <b>During Reset: High-Z After Reset: High During POS: High</b>
REFRESH#	I/O	<b>REFRESH.</b> As an output, REFRESH# is used by PIIX4 to indicate when a refresh cycle is in progress. It should be used to enable the SA[7:0] address to the row address inputs of all banks of dynamic memory on the ISA Bus. Thus, when MEMR# is asserted, the entire expansion bus dynamic memory is refreshed. Memory slaves must not drive any data onto the bus during refresh. As an output, this signal is driven directly onto the ISA Bus. This signal is an output only when PIIX4 DMA refresh controller is a master on the bus responding to an internally generated request for refresh. As an input, REFRESH# is driven by 16-bit ISA Bus masters to initiate refresh cycles. <b>During Reset: High-Z After Reset: High During POS: High</b>
RSTDRV	O	<b>RESET DRIVE.</b> PIIX4 asserts RSTDRV to reset devices that reside on the ISA/EIO Bus. PIIX4 asserts this signal during a hard reset and during power-up. RSTDRV is asserted during power-up and negated after PWROK is driven active. RSTDRV is also driven active for a minimum of 1 ms if a hard reset has been programmed in the RC register. <b>During Reset: High After Reset: Low During POS: Low</b>

SIGNAL	TYPE	DESCRIPTION
SA[19:0]	I/O	<b>SYSTEM ADDRESS[19:0].</b> These bi-directional address lines define the selection with the granularity of 1 byte within the 1-Megabyte section of memory defined by the LA[23:17] address lines. The address lines SA[19:17] that are coincident with LA[19:17] are defined to have the same values as LA[19:17] for all memory cycles. For I/O accesses, only SA[15:0] are used, and SA[19:16] are undefined. SA[19:0] are outputs when PIIX4 owns the ISA Bus. SA[19:0] are inputs when an external ISA Master owns the ISA Bus. <b>During Reset: High-Z After Reset: Undefined During POS: Last SA</b>
SBHE#	I/O	<b>SYSTEM BYTE HIGH ENABLE.</b> SBHE# indicates, when asserted, that a byte is being transferred on the upper byte (SD[15:8]) of the data bus. SBHE# is negated during refresh cycles. SBHE# is an output when PIIX4 owns the ISA Bus. SBHE# is an input when an external ISA master owns the ISA Bus. <b>During Reset: High-Z After Reset: Undefined During POS: High</b>
SD[15:0]	I/O	<b>SYSTEM DATA.</b> SD[15:0] provide the 16-bit data path for devices residing on the ISA Bus. SD[15:8] correspond to the high order byte and SD[7:0] correspond to the low order byte. SD[15:0] are undefined during refresh. <b>During Reset: High-Z After Reset: Undefined During POS: High-Z</b>
SMEMR#	O	<b>STANDARD MEMORY READ.</b> PIIX4 asserts SMEMR# to request an ISA memory slave to drive data onto the data lines. If the access is below the 1-Mbyte range (00000000h?00FFFFFFh) during DMA compatible, PIIX4 master, or ISA master cycles, PIIX4 asserts SMEMR#. SMEMR# is a delayed version of MEMR#.
IGNNE#	OD	<b>IGNORE NUMERIC EXCEPTION.</b> This signal is connected to the ignore numeric exception pin on the CPU. IGNNE# is only used if the PIIX4 coprocessor error reporting function is enabled. If FERR# is active, indicating a coprocessor error, a write to the Coprocessor Error Register (F0h) causes the IGNNE# to be asserted. IGNNE# remains asserted until FERR# is negated. If FERR# is not asserted when the Coprocessor Error Register is written, the IGNNE# signal is not asserted. <b>During Reset: High-Z After Reset: High-Z During POS: High-Z</b>
INIT	OD	<b>INITIALIZATION.</b> INIT is asserted in response to any one of the following conditions. When the System Reset bit in the Reset Control Register is reset to 0 and the Reset CPU bit toggles from 0 to 1, PIIX4 initiates a soft reset by asserting INIT. PIIX4 also asserts INIT if a Shut Down Special cycle is decoded on the PCI Bus, if the RCIN# signal is asserted, or if a write occurs to Port 92h, bit 0. When asserted, INIT remains asserted for approximately 64 PCI clocks before being negated. This signal is active high for Pentium processor and active-low for Pentium II processor as determined by CONFIG1 signal. <b>Pentium Processor:</b> <b>During Reset: Low After Reset: Low During POS: Low</b> <b>Pentium II Processor:</b> <b>During Reset: High After Reset: High During POS: High</b>

# 6120N N/B MAINTENANCE

## 3.3 INTEL 82371EB PCI-TO-ISA / IDE XCELERATOR (PIIX4) (5).

SIGNAL	TYPE	DESCRIPTION
INTR	OD	<b>CPU INTERRUPT.</b> INTR is driven by PIIX4 to signal the CPU that an interrupt request is pending and needs to be serviced. It is asynchronous with respect to SYSCLK or PCICLK and is always an output. The interrupt controller must be programmed following PCIRST# to ensure that INTR is at a known state <b>During Reset: Low After Reset: Low During POS: Low</b>
NMI	OD	<b>NON-MASKABLE INTERRUPT.</b> NMI is used to force a nonmaskable interrupt to the CPU. PIIX4 generates an NMI when either SERR# or IOCHK# is asserted, depending on how the NMI Status and Control Register is programmed. The CPU detects an NMI when it detects a rising edge on NMI. After the NMI interrupt routine processes the interrupt, the NMI status bits in the NMI Status and Control Register are cleared by software. The NMI interrupt routine must read this register to determine the source of the interrupt. The NMI is reset by setting the corresponding NMI source enable/disable bit in the NMI Status and Control Register. To enable NMI interrupts, the two NMI enable/disable bits in the register must be set to 0, and the NMI mask bit in the NMI Enable/Disable and Real Time Clock Address Register must be set to 0. Upon PCIRST#, this signal is driven low. <b>During Reset: Low After Reset: Low During POS: Low</b>
SMI#	OD	<b>SYSTEM MANAGEMENT INTERRUPT.</b> SMI# is an active low synchronous output that is asserted by PIIX4 in response to one of many enabled hardware or software events. The CPU recognizes the falling edge of SMI# as the highest priority interrupt in the system, with the exception of INIT, CPURST, and FLUSH. <b>During Reset: High-Z After Reset: High-Z During POS: High-Z</b>
STPCLK#	OD	<b>STOP CLOCK.</b> STPCLK# is an active low synchronous output that is asserted by PIIX4 in response to one of many hardware or software events. STPCLK# connects directly to the CPU and is synchronous to PCICLK. <b>During Reset: High-Z After Reset: High-Z During POS: High-</b>
RTCX1, RTCX2	I/O	<b>RTC CRYSTAL INPUTS:</b> These connected directly to a 32.768-kHz crystal. External capacitors are required. These clock inputs are required even if the internal RTC is not being used.
CLK48	I	<b>48-MHZ CLOCK.</b> 48-MHz clock used by the internal USB host controller. This signal may be stopped during suspend modes.
PCICLK	I	<b>FREE-RUNNING PCI CLOCK.</b> A clock signal running at 30 or 33 MHz, PCICLK provides timing for all transactions on the PCI Bus. All other PCI signals are sampled on the rising edge of PCICLK, and all timing parameters are defined with respect to this edge. Because many of the circuits in PIIX4 run off the PCI clock, this signal MUST be kept active, even if the PCI bus clock is not active.
OSC	I	<b>14.31818-MHZ CLOCK.</b> Clock signal used by the internal 8254 timer. This clock signal may be stopped during suspend modes.

SIGNAL	TYPE	DESCRIPTION
SUSCLK	O	<b>SUSPEND CLOCK.</b> 32.768-kHz output clock provided to the Host-to-PCI bridge used for maintenance of DRAM refresh. This signal is stopped during Suspend-to-Disk and Soft Off modes. For values During Reset, After Reset, and During POS, see the <i>Suspend/Resume and Resume Control Signaling</i> section.
SYSCLK	O	<b>ISA SYSTEM CLOCK.</b> SYSCLK is the reference clock for the ISA bus. It drives the ISA bus directly. The SYSCLK is generated by dividing PCICLK by 4. The SYSCLK frequencies supported are 7.5 MHz and 8.33 MHz. For PCI accesses to the ISA bus, SYSCLK may be stretched low to synchronize BALE falling to the rising edge of SYSCLK. <b>During Reset: Running After Reset: Running During POS: Low</b>
PDA[2:0]	O	<b>PRIMARY DISK ADDRESS[2:0].</b> These signals indicate which byte in either the ATA command block or control block is being addressed. If the IDE signals are configured for Primary and Secondary, these signals are connected to the corresponding signals on the Primary IDE connector. If the IDE signals are configured for Primary 0 and Primary 1, these signals are used for the Primary 0 connector.
PDCS1#	O	<b>PRIMARY DISK CHIP SELECT FOR 1F0H- 1F7H RANGE.</b> For ATA command register block. If the IDE signals are configured for Primary and Secondary, this output signal is connected to the corresponding signal on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector. <b>During Reset: High After Reset: High During POS: High</b>
PDCS3#	O	<b>PRIMARY DISK CHIP SELECT FOR 3F0- 3F7 RANGE.</b> For ATA control register block. If the IDE signals are configured for Primary and Secondary, this output signal is connected to the corresponding signal on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector. <b>During Reset: High After Reset: High During POS: High</b>
PDD[15:0]	I/O	<b>PRIMARY DISK DATA[15:0].</b> These signals are used to transfer data to or from the IDE device. If the IDE signals are configured for Primary and Secondary, these signals are connected to the corresponding signals on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector.
SDA[2:0]	O	<b>SECONDARY DISK ADDRESS[2:0].</b> These signals indicate which byte in either the ATA command block or control block is being addressed. If the IDE signals are configured for Primary and Secondary, these signals are connected to the corresponding signals on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector.

# 6120N N/B MAINTENANCE

## 3.3 INTEL 82371EB PCI-TO-ISA / IDE XCELERATOR (PIIX4) (6).

SIGNAL	TYPE	DESCRIPTION
IGNNE#	OD	<b>IGNORE NUMERIC EXCEPTION.</b> This signal is connected to the ignore numeric exception pin on the CPU. IGNNE# is only used if the PIIX4 coprocessor error reporting function is enabled. If FERR# is active, indicating a coprocessor error, a write to the Coprocessor Error Register (F0h) causes the IGNNE# to be asserted. IGNNE# remains asserted until FERR# is negated. If FERR# is not asserted when the Coprocessor Error Register is written, the IGNNE# signal is not asserted. <b>During Reset: High-Z After Reset: High-Z During POS: High-Z</b>
INIT	OD	<b>INITIALIZATION.</b> INIT is asserted in response to any one of the following conditions. When the System Reset bit in the Reset Control Register is reset to 0 and the Reset CPU bit toggles from 0 to 1, PIIX4 initiates a soft reset by asserting INIT. PIIX4 also asserts INIT if a Shut Down Special cycle is decoded on the PCI Bus, if the RCIN# signal is asserted, or if a write occurs to Port 92h, bit 0. When asserted, INIT remains asserted for approximately 64 PCI clocks before being negated. This signal is active high for Pentium processor and active-low for Pentium II processor as determined by CONFIG1 signal. <b>Pentium Processor:</b> <b>During Reset: Low After Reset: Low During POS: Low</b> <b>Pentium II Processor:</b> <b>During Reset: High After Reset: High During POS: High</b>
INTR	OD	<b>CPU INTERRUPT.</b> INTR is driven by PIIX4 to signal the CPU that an interrupt request is pending and needs to be serviced. It is asynchronous with respect to SYSCLK or PCICLK and is always an output. The interrupt controller must be programmed following PCIRST# to ensure that INTR is at a known state. <b>During Reset: Low After Reset: Low During POS: Low</b>
NMI	OD	<b>NON-MASKABLE INTERRUPT.</b> NMI is used to force a nonmaskable interrupt to the CPU. PIIX4 generates an NMI when either SERR# or IOCHK# is asserted, depending on how the NMI Status and Control Register is programmed. The CPU detects an NMI when it detects a rising edge on NMI. After the NMI interrupt routine processes the interrupt, the NMI status bits in the NMI Status and Control Register are cleared by software. The NMI interrupt routine must read this register to determine the source of the interrupt. The NMI is reset by setting the corresponding NMI source enable/disable bit in the NMI Status and Control Register. To enable NMI interrupts, the two NMI enable/disable bits in the register must be set to 0, and the NMI mask bit in the NMI Enable/Disable and Real Time Clock Address Register must be set to 0. Upon PCIRST#, this signal is driven low. <b>During Reset: Low After Reset: Low During POS: Low</b>
SMI#	OD	<b>SYSTEM MANAGEMENT INTERRUPT.</b> SMI# is an active low synchronous output that is asserted by PIIX4 in response to one of many enabled hardware or software events. The CPU recognizes the falling edge of SMI# as the highest priority interrupt in the system, with the exception of INIT, CPURST, and FLUSH. <b>During Reset: High-Z After Reset: High-Z During POS: High-Z</b>

SIGNAL	TYPE	DESCRIPTION
STPCLK#	OD	<b>STOP CLOCK.</b> STPCLK# is an active low synchronous output that is asserted by PIIX4 in response to one of many hardware or software events. STPCLK# connects directly to the CPU and is synchronous to PCICLK. <b>During Reset: High-Z After Reset: High-Z During POS: High-</b>
RTCX1, RTCX2	I/O	<b>RTC CRYSTAL INPUTS:</b> These connected directly to a 32.768-kHz crystal. External capacitors are required. These clock inputs are required even if the internal RTC is not being used.
CLK48	I	<b>48-MHZ CLOCK.</b> 48-MHz clock used by the internal USB host controller. This signal may be stopped during suspend modes.
PCICLK	I	<b>FREE-RUNNING PCI CLOCK.</b> A clock signal running at 30 or 33 MHz, PCICLK provides timing for all transactions on the PCI Bus. All other PCI signals are sampled on the rising edge of PCICLK, and all timing parameters are defined with respect to this edge. Because many of the circuits in PIIX4 run off the PCI clock, this signal MUST be kept active, even if the PCI bus clock is not active.
OSC	I	<b>14.31818-MHZ CLOCK.</b> Clock signal used by the internal 8254 timer. This clock signal may be stopped during suspend modes.
SUSCLK	O	<b>SUSPEND CLOCK.</b> 32.768-kHz output clock provided to the Host-to-PCI bridge used for maintenance of DRAM refresh. This signal is stopped during Suspend-to-Disk and Soft Off modes. For values During Reset, After Reset, and During POS, see the <i>Suspend/Resume and Resume Control Signaling</i> section.
SYSCLK	O	<b>ISA SYSTEM CLOCK.</b> SYSCLK is the reference clock for the ISA bus. It drives the ISA bus directly. The SYSCLK is generated by dividing PCICLK by 4. The SYSCLK frequencies supported are 7.5 MHz and 8.33 MHz. For PCI accesses to the ISA bus, SYSCLK may be stretched low to synchronize BALE falling to the rising edge of SYSCLK. <b>During Reset: Running After Reset: Running During POS: Low</b>
PDA[2:0]	O	<b>PRIMARY DISK ADDRESS[2:0].</b> These signals indicate which byte in either the ATA command block or control block is being addressed. If the IDE signals are configured for Primary and Secondary, these signals are connected to the corresponding signals on the Primary IDE connector. If the IDE signals are configured for Primary 0 and Primary 1, these signals are used for the Primary 0 connector.
PDCS1#	O	<b>PRIMARY DISK CHIP SELECT FOR 1F0H-1F7H RANGE.</b> For ATA command register block. If the IDE signals are configured for Primary and Secondary, this output signal is connected to the corresponding signal on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector. <b>During Reset: High After Reset: High During POS: High</b>

# 6120N N/B MAINTENANCE

## 3.3 INTEL 82371EB PCI-TO-ISA / IDE XCELERATOR (PIIX4) (7).

SIGNAL	TYPE	DESCRIPTION
PDCS3#	O	<b>PRIMARY DISK CHIP SELECT FOR 3F0- 3F7 RANGE.</b> For ATA control register block. If the IDE signals are configured for Primary and Secondary, this output signal is connected to the corresponding signal on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector. <b>During Reset: High After Reset: High During POS: High</b>
PDD[15:0]	I/O	<b>PRIMARY DISK DATA[15:0].</b> These signals are used to transfer data to or from the IDE device. If the IDE signals are configured for Primary and Secondary, these signals are connected to the corresponding signals on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector.
SDA[2:0]	O	<b>SECONDARY DISK ADDRESS[2:0].</b> These signals indicate which byte in either the ATA command block or control block is being addressed. If the IDE signals are configured for Primary and Secondary, these signals are connected to the corresponding signals on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector.
SDIOW#	O	<b>SECONDARY DISK IO WRITE.</b> In normal IDE mode, this is the command to the IDE device that it may latch data from the SDD[15:0] lines. Data is latched by the IDE device on the negation edge of SDIOW#. The IDE device is selected either by the ATA register file chip selects (SDCS1#, SDCS3#) and the SDA[2:0] lines, or the IDE DMA slave arbitration signals (SDDACK#). In read and write cycles this signal is used as the STOP signal, which is used to terminate an Ultra DMA/33 transaction. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector. <b>During Reset: High After Reset: High During POS: High</b>
SIORDY	I	<b>SECONDARY IO CHANNEL READY.</b> In normal IDE mode, this input signal is directly driven by the corresponding IDE device IORDY signal. In an Ultra DMA/33 read cycle, this signal is used as STROBE, with the PIIX4 latching data on rising and falling edges of STROBE. In an Ultra DMA write cycle, this signal is used as the DMARDY# signal which is negated by the drive to pause Ultra DMA/33 transfers. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector. This is a Schmitt triggered input.
OC[1:0]#	I	<b>OVER CURRENT DETECT.</b> These signals are used to monitor the status of the USB power supply lines. The corresponding USB port is disabled when its over current signal is asserted.
USBP0+, USBP0?	I/O	<b>SERIAL BUS PORT 0.</b> This signal pair comprises the differential data signal for USB port 0.

SIGNAL	TYPE	DESCRIPTION
USBP1+, USBP1	I/O	<b>SERIAL BUS PORT 1.</b> This signal pair comprises the differential data signal for USB port 1.
BATLOW#/ GPI9	I	<b>BATTERY LOW.</b> Indicates that battery power is low. PIIX4 can be programmed to prevent a resume operation when the BATLOW# signal is asserted. If the Battery Low function is not needed, this pin can be used as a general-purpose input.
CPU_STP#/ GPO17	O	<b>CPU CLOCK STOP.</b> Active low control signal to the clock generator used to disable the CPU clock outputs. If this function is not needed, then this signal can be used as a general-purpose output. For values <b>During Reset, After Reset, and During POS</b> , see the <i>Suspend/Resume and Resume Control Signaling</i> section.
EXTSMI#	I/OD	<b>EXTERNAL SYSTEM MANAGEMENT INTERRUPT.</b> EXTSMI# is a falling edge triggered input to PIIX4 indicating that an external device is requesting the system to enter SMM mode. When enabled, a falling edge on EXTSMI# results in the assertion of the SMI# signal to the CPU. EXTSMI# is an asynchronous input to PIIX4. However, when the setup and hold times are met, it is only required to be asserted for one PCICLK. Once negated EXTSMI# must remain negated for at least four PCICLKs to allow the edge detect logic to reset. EXTSMI# is asserted by PIIX4 in response to SMI# being activated within the Serial IRQ function. An external pull-up should be placed on this signal.
LID/ GPI10	I	<b>LID INPUT.</b> This signal can be used to monitor the opening and closing of the display lid of a notebook computer. It can be used to detect both low to high transition or a high to low transition and these transitions will generate an SMI# if enabled. This input contains logic to perform a 16-ms debounce of the input signal. If the LID function is not needed, this pin can be used as a general-purpose input.
PCIREQ A:D]#	I	<b>PCI REQUEST.</b> Power Management input signals used to monitor PCI Master Requests for use of the PCI bus. They are connected to the corresponding REQ[0:3]# signals on the Host Bridge.
PCI_STP#/ GPO18	O	<b>PCI CLOCK STOP.</b> Active low control signal to the clock generator used to disable the PCI clock outputs. The PIIX4 free running PCICLK input must remain on. If this function is not needed, this pin can be used as a general-purpose output. For values <b>During Reset, After Reset, and During POS</b> , see the <i>Suspend/Resume and Resume Control Signaling</i> section.
PWRBTN#	I	<b>POWER BUTTON.</b> Input used by power management logic to monitor external system events, most typically a system on/off button or switch. This input contains logic to perform a 16-ms debounce of the input signal.
RI# GPI12	I	<b>RING INDICATE.</b> Input used by power management logic to monitor external system events, most typically used for wake up from a modem. If this function is not needed, then this signal can be individually used as a general-purpose input.

# 6120N N/B MAINTENANCE

## 3.3 INTEL 82371EB PCI-TO-ISA / IDE XCELERATOR (PIIX4) (8).

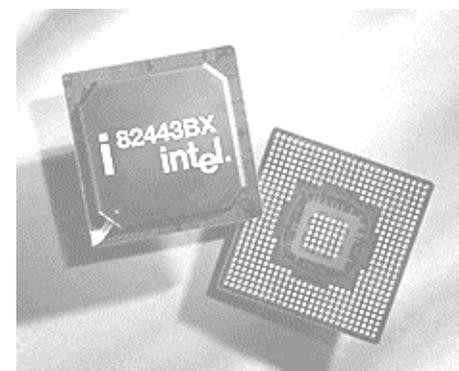
SIGNAL	TYPE	DESCRIPTION
RSMRST#	I	<b>RESUME RESET.</b> This signal resets the internal Suspend Well power plane logic and portions of the RTC well logic.
SMBALERT#/GPI11	I	<b>SM BUS ALERT.</b> Input used by System Management Bus logic to generate an interrupt (IRQ or SMI) or power management resume event when enabled. If this function is not needed, this pin can be used as a general-purpose input.
SMBCLK	I/O	<b>SM BUS CLOCK.</b> System Management Bus Clock used to synchronize transfer of data on SMBus. <b>During Reset: High-Z After Reset: High-Z During POS: High-Z</b>
SMBDATA	I/O	<b>SM BUS DATA.</b> Serial data line used to transfer data on SMBus. <b>During Reset: High-Z After Reset: High-Z During POS: High-Z</b>
SUSA#	O	<b>SUSPEND PLANE A CONTROL.</b> Control signal asserted during power management suspend states. SUSA# is primarily used to control the primary power plane. This signal is asserted during POS, STR, and STD suspend states. <b>During Reset: Low After Reset: High During POS: Low</b>
SUSB#/GPO15	O	<b>SUSPEND PLANE B CONTROL.</b> Control signal asserted during power management suspend states. SUSB# is primarily used to control the secondary power plane. This signal is asserted during STR and STD suspend states. If the power plane control is not needed, this pin can be used as a general-purpose output. <b>During Reset: Low After Reset: High During POS: High/GPO</b>
SUSC#/GPO16	O	<b>SUSPEND PLANE C CONTROL.</b> Control signal asserted during power management suspend states, primarily used to control the tertiary power plane. It is asserted only during STD suspend state. If the power plane control is not needed, this pin can be used as a general-purpose output. <b>During Reset: Low After Reset: High During POS: High/GPO</b>
SUS_STAT1#/GPO20	O	<b>SUSPEND STATUS 1.</b> This signal is typically connected to the Host-to-PCI bridge and is used to provide information on host clock status. SUS_STAT1# is asserted when the system may stop the host clock, such as Stop Clock or during POS, STR, and STD suspend states. If this function is not needed, this pin can be used as a general-purpose output.
SUS_STAT2#/GPO21	O	<b>SUSPEND STATUS 2.</b> This signal will typically connect to other system peripherals and is used to provide information on system suspend state. It is asserted during POS, STR, and STD suspend states. If this function is not needed, this pin can be used as a general-purpose output. <b>During Reset: Low After Reset: High During POS: Low/GPO</b>
THRM#/GPI8	I	<b>THERMAL DETECT.</b> Active low signal generated by external hardware to start the Hardware Clock Throttling mode. If enabled, the external hardware can force the system to enter into Hardware Clock Throttle mode by asserting THRM#. This causes PIIX4 to cycle STPCLK# at a preset programmable rate. If this function is not needed, this pin can be used as a general-purpose input.

SIGNAL	TYPE	DESCRIPTION
ZZ/ GPO19	O	<b>LOW-POWER MODE FOR L2 CACHE SRAM.</b> This signal is used to power down a cache data SRAMs when the clock logic places the CPU into the Stop Clock. If this function is not needed, this pin can be used as a general-purpose output. <b>During Reset: Low After Reset: Low During POS: Low</b>
GPI[21:0]	I	<b>GENERAL PURPOSE INPUTS.</b> These input signals can be monitored via the GPIREG register located in Function 3 (Power Management) System IO Space at address PMBase+30h. See Table 1 for details.
GPO[30:0]	O	<b>GENERAL PURPOSE OUTPUTS.</b> These output signals can be controlled via the GPIREG register located in Function 3 (Power Management) System IO Space at address PMBase+34h. If a GPO pin is not multiplexed with another signal or defaults to GPO, then its state after reset is the reset condition of the GPOREG register. If the GPO defaults to another signal, then it defaults to that signal state after reset. The GPO pins that default to GPO remain stable after reset. The others may toggle due to system boot or power control sequencing after reset prior to their being programmed as GPOs. The GPO8 signal is driven low upon removal of power from the PIIX4 core power plane. All other GPO signals are invalid (buffers powered off).
CONFIG1	I	<b>CONFIGURATION SELECT 1.</b> This input signal is used to select the type of microprocessor being used in the system. If CONFIG1=0, the system contains a Pentium microprocessor. If CONFIG1=1, the system contains a Pentium II microprocessor. It is used to control the polarity of INIT and CPURST signals.
CONFIG2	I	<b>CONFIGURATION SELECT 2.</b> This input signal is used to select the positive or subtractive decode of FFFF0000h FFFFFFFh memory address range (top 64 Kbytes). If CONFIG[2]=0, the PIIX4 will positively decode this range. If CONFIG[2]=1, the PIIX4 will decode this range with subtractive decode timings only. The input value of this pin must be static and may not dynamically change during system operations.
PWROK	I	<b>POWER OK.</b> When asserted, PWROK is an indication to PIIX4 that power and PCICLK have been stable for at least 1 ms. PWROK can be driven asynchronously. When PWROK is negated, PIIX4 asserts CPURST, PCIRST# and RSTDRV. When PWROK is driven active (high), PIIX4 negates CPURST, PCIRST#, and RSTDRV.
SPKR	O	<b>SPEAKER.</b> The SPKR signal is the output of counter timer 2 and is internally "ANDed" with Port 061h bit 1 to provide the Speaker Data Enable. This signal drives an external speaker driver device, which in turn drives the ISA system speaker. <b>During Reset: Low After Reset: Low During POS: Last State</b>
TEST#	I	<b>TEST MODE SELECT.</b> The test signal is used to select various test modes of PIIX4. This signal must be pulled up to VCC(SUS) for normal operation.

# 6120N N/B MAINTENANCE

## 3.3 INTEL 82371EB PCI-TO-ISA / IDE XCELERATOR (PIIX4) (9).

SIGNAL	TYPE	DESCRIPTION
VCC	V	<b>CORE VOLTAGE SUPPLY.</b> These pins are the primary voltage supply for the PIIX4 core and IO periphery and must be tied to 3.3V.
VCC (RTC)	V	<b>RTC WELL VOLTAGE SUPPLY.</b> This pin is the supply voltage for the RTC logic and must be tied to 3.3V.
VCC (SUS)	V	<b>SUSPEND WELL VOLTAGE SUPPLY.</b> These pins are the primary voltage supply for the PIIX4 suspend logic and IO signals and must be tied to 3.3V.
VCC (USB)	V	<b>USB VOLTAGE SUPPLY.</b> This pin is the supply voltage for the USB input/output buffers and must be tied to 3.3V.
VREF	V	<b>VOLTAGE REFERENCE.</b> This pin is used to provide a 5V reference voltage for 5V safe input buffers. VREF must be tied to 5V in a system requiring 5V tolerance. In a 5V tolerant system, this signal must power up before or simultaneous to VCC. It must power down after or simultaneous to VCC. In a non-5V tolerant system (3.3V only), this signal can be tied directly to VCC. There are then no sequencing requirements.
VSS	V	<b>CORE GROUND.</b> These pins are the primary ground for PIIX4.
VSS (USB)	V	<b>USB GROUND.</b> This pin is the ground for the USB input/output buffers.



# 6120N N/B MAINTENANCE

## 4. MAJOR CHIP DESCRIPTION

### INTEL 440ZX AGPSET: 82443ZX HOST BRIDGE/CONTROLLER

- Processor/host bus support
  - ~ Optimized for Pentium? II processor at 100 MHz system bus frequency; Support for 66 MHz
  - ~ In-order transaction and dynamic deferred transaction support
  - ~ Desktop optimized GTL+ bus driver technology (gated GTL+ receivers for reduced power)
- Integrated DRAM controller
  - ~ 8 to 256Mbytes
  - ~ Supports 2 double-sided DIMMs (4 rows memory)
  - ~ 64-bit data interface
  - ~ Unbuffered SDRAM (Synchronous) DRAM Support (x-1-1-1 access @ 66 MHz, x-1-1-1 access @ 100 MHz)
  - ~ Enhanced SDRAM Open Page Architecture Support for 16- and 64-Mbit DRAM devices with 2k, 4k and 8k page sizes
- PCI bus interface
  - ~ PCI Rev. 2.1, 3.3V and 5V, 33MHz interface compliant
  - ~ PCI Parity Generation Support
  - ~ Data streaming support from PCI to DRAM
  - ~ Delayed Transaction support for PCI-DRAM Reads
  - ~ Supports concurrent CPU, AGP and PCI transactions to main memory

# 6120N N/B MAINTENANCE

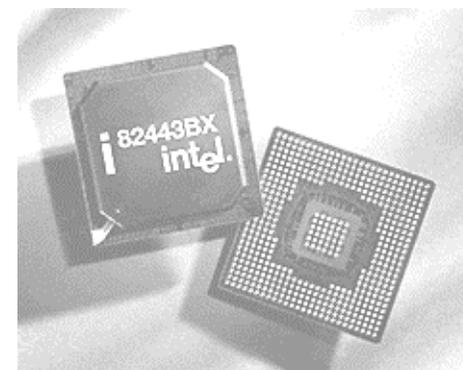
## INTEL 440ZX AGPSET: 82443ZX HOST BRIDGE/CONTROLLER

- AGP interface
  - ~ Supports single AGP compliant device (AGP-66/133 3.3V device)
  - ~ AGP Specification Rev 1.0 compliant
  - ~ AGP-data/transaction flow optimized arbitration mechanism
  - ~ AGP side-band interface for efficient request pipelining without interfering with the data streams
  - ~ AGP-specific data buffering
  - ~ Supports concurrent CPU, AGP and PCI transactions to main memory
  - ~ AGP high-priority transactions (“expedite”) support
- Power Management Functions
  - ~ Stop Clock Grant and Halt special cycle translation (host to PCI Bus)
  - ~ Dynamic power down of idle DRAM rows
  - ~ Independent, internal dynamic clock gating reduces average power dissipation
- Packaging/Voltage
  - ~ 492 Pin BGA
  - ~ 3.3V core and mixed 3.3V and GTL I/O
- Supporting I/O Bridge
  - ~ System Management Bus (SMB) with support for DIMM Serial Presence Detect (SPD)
  - ~ PCI-ISA Bridge (PIIX4E)
  - ~ 3.3V core and mixed 5V, 3.3V I/O and interface to the 2.5V CPU signals via open-drain output buffers

# 6120N N/B MAINTENANCE

## 4.2 Intel 82371EB PCI-to-ISA / IDE accelerator (PIIX4E)

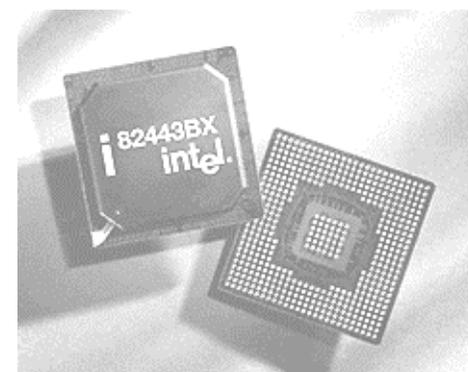
- Supported Kits For Both Pentium And Pentium II Microprocessors
  - ~ 82430TX ISA Kit
  - ~ 82440bx ISA/DP Kit
- Multifunction PCI To ISA Bridge
  - ~ Supports PCI At 30 MHZ And 33 MHZ
  - ~ Supports PCI Rev 2.1 Specification
  - ~ Supports Full ISA Or Extended I/O (EIO) Bus
  - ~ Supports Full Positive Decode Or Subtractive Decode Of PCI
  - ~ Supports ISA And EIO At 1/4 Of PCI Frequency
- Supports Both Mobile And Desktop Deep Green Environments
  - ~ 3.3v Operation With 5v Tolerant Buffers
  - ~ Ultra-low Power For Mobile Environments Support
  - ~ Power-on Suspend, Suspend To Ram, Suspend To Disk, And Soft-off System States
  - ~ All Registers Readable And Restorable For Proper Resume From 0.V Suspend
- Power Management Logic
  - ~ Global And Local Device Management
  - ~ Suspend And Resume Logic
  - ~ Supports Thermal Alarm
  - ~ Support For External Microcontroller
  - ~ Full Support For Advanced Configuration And Power Interface (ACPI) Revision 1.0 Specification And OS Directed Power Management
- Integrated IDE Controller
  - ~ Independent Timing Of Up To 4 Drives
  - ~ PIO Mode 4 And Bus Master IDE Transfers Up To 14 Mbytes/sec
  - ~ Supports Ultra DMA/33 Synchronous DMA Mode Transfers Up To 33 Mbytes/sec
  - ~ Integrated 16 X 32-bit Buffer For IDE PCI Burst Transfers
  - ~ Supports Glue-less Swap-bay Option With Full Electrical Isolation



# 6120N N/B MAINTENANCE

## 4.2 Intel 82371EB PCI-to-ISA / IDE Xcelerator (PIIX4E)

- Enhanced DMA Controller
  - ~ Two 82C37 DMA Controllers
  - ~ Supports PCI DMA With 3 PC/PCI Channels And Distributed DMA Protocols
  - ~ Fast Type-F DMA For Reduced PCI Bus Usage
- Interrupt Controller Based On Two 82C59
  - ~ 15 Interrupt Support
  - ~ Independently Programmable For Edge/level Sensitivity
  - ~ Supports Optional I/O APIC
  - ~ Serial Interrupt Input
- Timers Based On 82C54
  - ~ System Timer, Refresh Request, Speaker Tone Output
- USB
  - ~ Two USB 1.0 Ports For Serial Transfers At 12 Or 1.5 Mbit/sec
  - ~ Supports Legacy Keyboard And Mouse Software With USB-based Keyboard And Mouse
  - ~ Supports UHCI Design Guide
- MBUS
  - ~ Host Interface Allows CPU To Communicate Via SMBUS
  - ~ Slave Interface Allows External SMBUS Master To Control Resume Events
- Real-time Clock
  - ~ 256-byte Battery-back CMOS SRAM
  - ~ Includes Date Alarm
  - ~ Two 8-byte Lockout Ranges
- Microsoft Win95\* Compliant  
324 MBGA Package

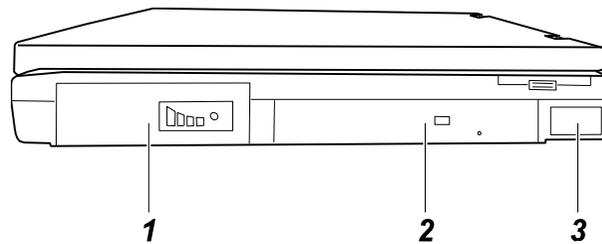


# 6120N N/B MAINTENANCE

## 5. System View And Disassembly

### 5.1 System View

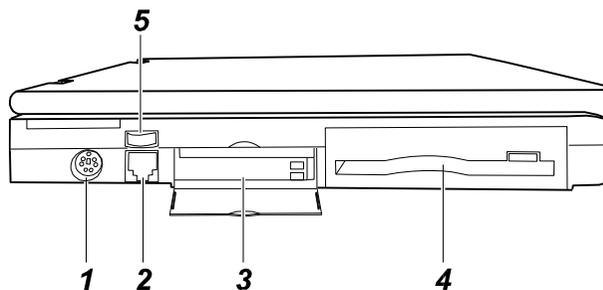
#### 5.1.1 Right-Side View



1. **Battery Pack**
2. **CD-ROM/DVD-ROM Drive**
3. **IR Port**

Figure 5-1. Right-Side View

#### 5.1.2 Left-Side View



1. **S-Video Output Connector**
2. **RJ-45 or RJ-11 Connector**  
(optional)
3. **PC Card Slots**
4. **Floppy Disk Drive**
5. **Volume Control**

Figure 5-2. Left-Side View

# 6120N N/B MAINTENANCE

## 5.1.3 Rear View

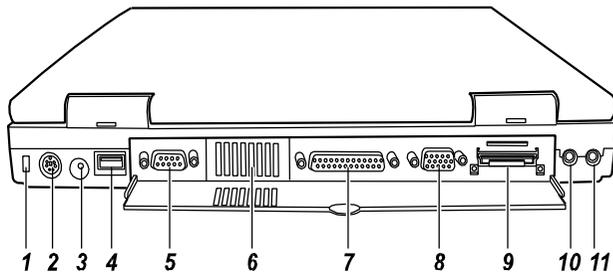


Figure 5-3. Rear View

1. **Kensington Lock Anchor**
2. **PS/2 Mouse/Keyboard Port**
3. **Power Connector**
4. **USB Port**
5. **Serial Port**
6. **Ventilation Opening**
7. **Parallel Port**
8. **VGA Port**
9. **Expansion Connector**
10. **Microphone Connector**
11. **Audio Output Connector**

## 5.1.4 Front View

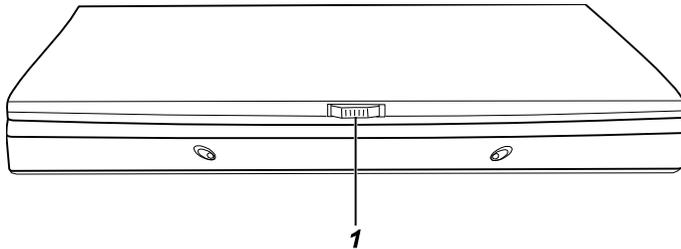
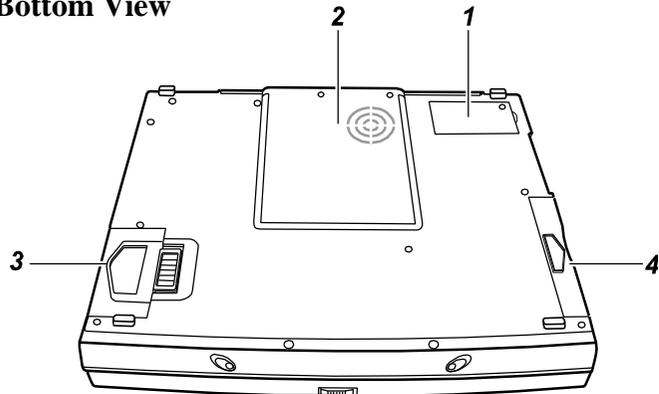


Figure 5-4. Front View

1. **Top Cover Latch**

# 6120N N/B MAINTENANCE

## 5.1.5 Bottom View

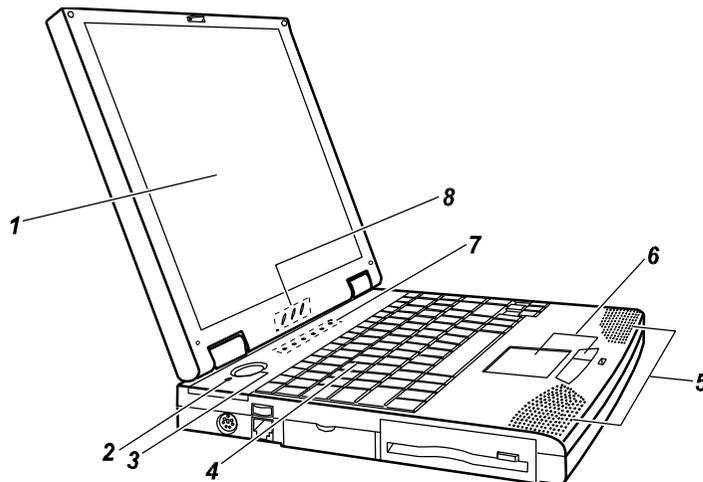


1. Modem Card/LAN Card Cover
2. CPU Card Cover
3. Battery Pack & Locking Latch
4. FDD/HDD Module

Figure 5-5. Bottom View

## 5.1.6 Top-Open View

To open the cover, press the cover latch toward the right and lift the cover.



1. LCD Display
2. Microphone
3. Power Button
4. Keyboard
5. Stereo Speaker Set
6. Touchpad
7. System Indicators
8. Power Indicators

Figure 5-6. Top-Open View

# **6120N N/B MAINTENANCE**

## **5.2 System Disassembly**

The section discusses at length each major component for disassembly/reassembly and show corresponding illustrations. Use the chart below to determine the disassembly sequence for removing components from the notebook.

### **● Modular Components**

- 5.2.1 Battery Pack
- 5.2.2 CD-ROM/DVD-ROM Drive
- 5.2.3 Hard Disk Drive
- 5.2.4 Floppy Disk Drive
- 5.2.5 CPU
- 5.2.6 Modem/LAN Card
- 5.2.7 Keyboard
- 5.2.8 SO-DIMM

### **● LCD Assembly Components**

- 5.2.9 LCD Assembly
- 5.2.10 LCD Panel
- 5.2.11 Inverter/LED Board

### **● Base Unit Components**

- 5.2.12 Battery/Touchpad Board
- 5.2.13 System Board
- 5.2.14 Touchpad Panel

You can also find details such as exploded views and parts lists in Chapter10.

# 6120N N/B MAINTENANCE

## 5.2.1 Battery Pack

### ● Disassembly

1. Put the notebook upside down with care.
2. Press the locking latch outward to unlatch the battery pack and then pull it out of the compartment.

### ● Reassembly

1. Fit the battery pack into the compartment. Make sure the locking latches are in the locked position. (Refer to Figure 5-7 )

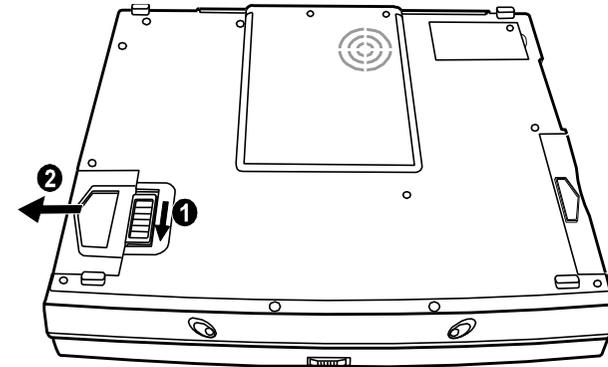


Figure 5-7. Removing the Battery Pack

## 5.2.2 CD-ROM/DVD-ROM Drive

### ● Disassembly

1. Place the notebook upside down with care.
2. Open the CPU compartment cover by removing two screws then sliding the cover toward the rear side to open it. (Refer to Figure 5-8.)

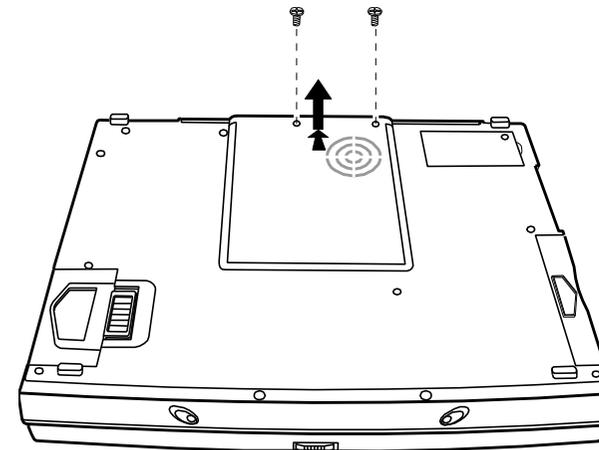


Figure 5-8. Removing the CPU Compartment Cover

# 6120N N/B MAINTENANCE

3. Remove one screw that fastens the CD-ROM/DVD-ROM drive.  
(Refer to Figure 5-9.)
4. Push the rear side of the CD-ROM/DVD-ROM drive to disconnect the drive from the system board, then slide it out of the compartment.

## ● Reassembly

1. Slide the CD-ROM/DVD-ROM drive into the compartment.  
The cable connector on the system board will automatically plug into the rear side of the drive. (Refer to Figure 5-10.)
2. Secure the CD-ROM/DVD-ROM drive with one screw.  
(Refer to Figure 5-9 earlier.)
3. Replace the CPU compartment cover and secure with two screws. (Refer to Figure 5-8 earlier.)

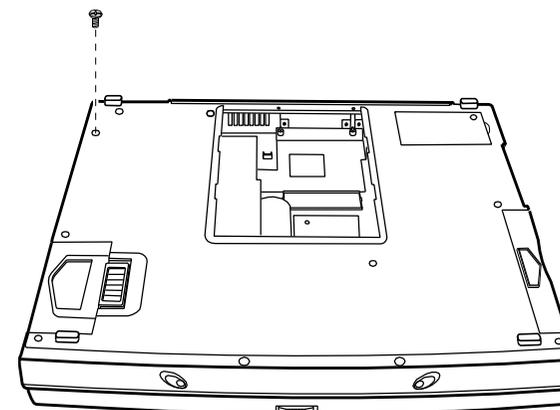


Figure 5-9. Removing One Screw

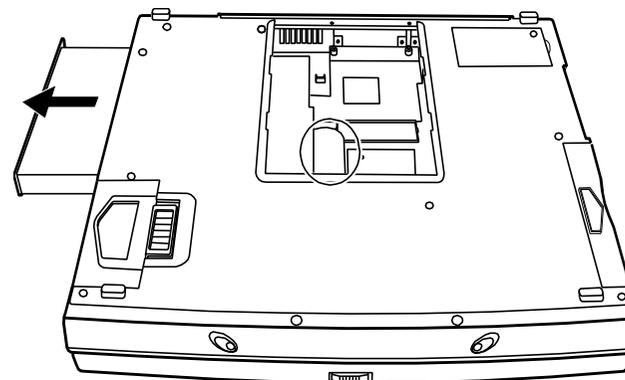


Figure 5-10. Removing the CD-ROM/DVD-ROM Drive

# 6120N N/B MAINTENANCE

## 5.2.3 Hard Disk Drive

### ● Disassembly

1. Put the notebook upside down with care.
2. Remove one screw and slide the FDD/HDD module out of the compartment.
3. Remove four screws and disconnect the hard disk drive from the connector. (Refer to Figure 5-12.)

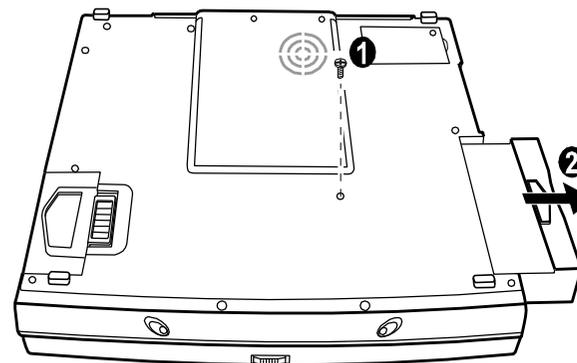


Figure 5-11. Removing the FDD/HDD Module

Note: When securing this screw, the force must be less than 3.5 kg, otherwise the bracket may break.

### ● Reassembly

1. Place the hard disk drive in the bracket and plug in the hard disk drive connector. Then secure the hard disk drive with four screws. (Refer to Figure 5-12 )
2. Slide the HDD/FDD module into the compartment and secure with one screw. (Refer to Figure 5-11 earlier.)

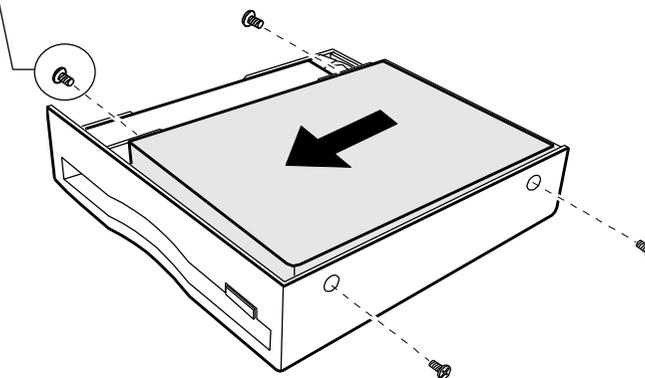


Figure 5-12. Removing the Hard Disk I

# 6120N N/B MAINTENANCE

## 5.2.4 Floppy Disk Drive

### ● Disassembly

1. Remove the hard disk drive. (See section 5.2.3 Disassembly.)
2. Remove four screws to detach the bracket from the floppy disk drive. (Refer to Figure 5-13.)

### ● Reassembly

1. Replace the bracket and secure with four screws. (Refer to Figure 5-13.)
2. Replace the hard disk drive. Slide the HDD/FDD module into the compartment and secure with one screw. (See section 5.2.3 Reassembly.)

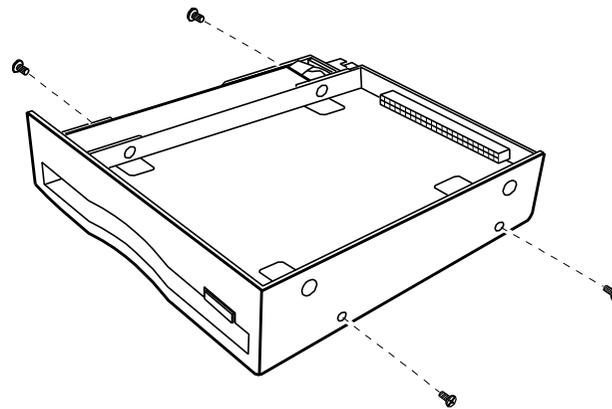


Figure 5-13. Detaching the Bracket From the Floppy Disk Drive

# 6120N N/B MAINTENANCE

## 5.2.5 CPU

### ● Disassembly

1. Place the notebook upside down and remove the CPU compartment cover. (See section 5.2.2 Disassembly step 1 and 2.)
2. Remove four screws fastening the fan assembly. Unplug the fan assembly's power cord and lift it free from the CPU module.

**NOTE:** When you remove the fan assembly, make sure that the thermal pad underneath the fan is not damaged. If it is damaged, you have to replace it with a new thermal pad.

3. Insert a minus screwdriver 101 (JIS standard) to the OPEN (upper) side of the socket and gently push the screwdriver to pry the CPU out of the socket.

**CAUTION:** The maximum force for extraction of the CPU should not exceed 100 lbs (45.5 kg).

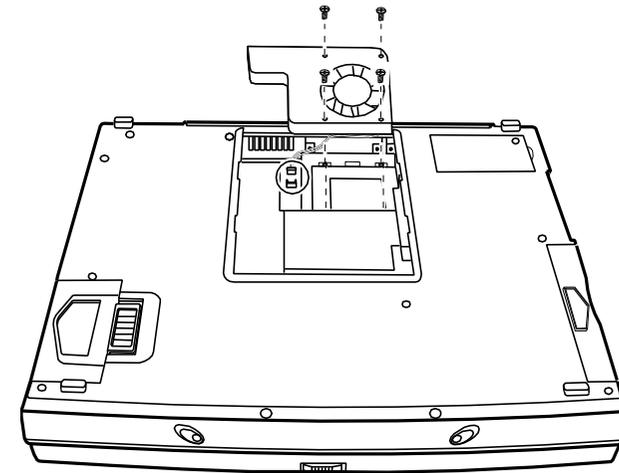


Figure 5-14. Removing the Fan Assem

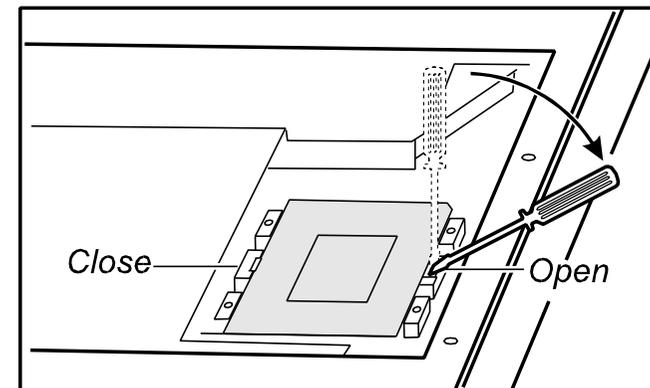


Figure 5-15. Removing the CPU

# 6120N N/B MAINTENANCE

## ● Reassembly

1. Align the beveled corner of the CPU with the beveled corner of the socket and insert the CPU pins into the holes. Insert a minus screwdriver to the CLOSE (lower) side of the socket and push the screwdriver toward the CPU to secure the CPU in place.

**CAUTION:** The maximum force for insertion of the CPU should not exceed 100 lbs (45.5 kg).

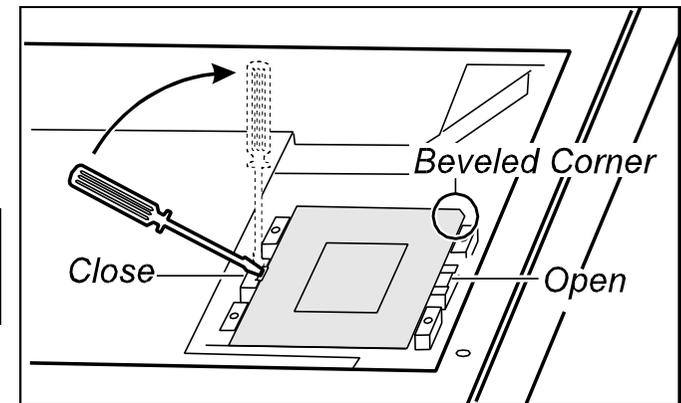


Figure 5-16. Insertion the CPU

2. Place the fan assembly on top of the CPU. Plug in the power cord and secure the fan assembly with four screws. (Refer to Figure 5-14 earlier.)
3. Replace the CPU compartment cover and secure with two screws.

# 6120N N/B MAINTENANCE

## 5.2.6 Modem Card

### ● Disassembly

1. Place the notebook upside down with care.
2. Remove one screw and open the Modem card compartment cover. (Refer to Figure 5-17)
3. Carefully lift up the inner edge of the card to disconnect it from the system board.

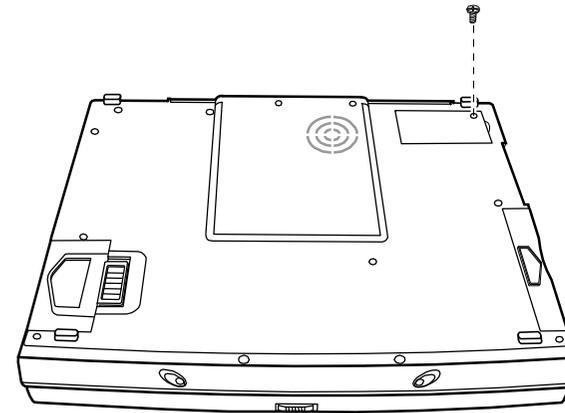


Figure 5-17. Removing the Modem Card Compartment Cover

### ● Reassembly

1. Hold the Modem card at an angle so that the phone line connector is pointed towards the opening on the notebook. Insert the connector into the opening and press the other end to plug the Modem card into the socket on the system board. (Refer to Figure 5-18 earlier.)
2. Replace the compartment cover and secure with one screw. (Refer to Figure 5-17 earlier.)

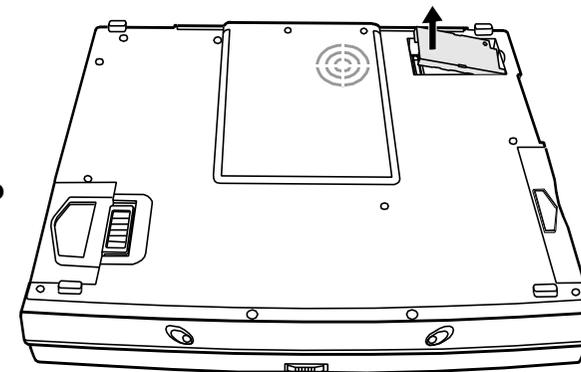


Figure 5-18. Removing the Modem/LAN Card

# 6120N N/B MAINTENANCE

## 5.2.7 Keyboard

### ● Disassembly

1. Open the top cover.
2. Press the locking latch downward to unlatch the LED panel and then push it leftward to remove the panel. (Refer to Figure 5-19.)
3. Slightly lift up the keyboard and disconnect the cable from the system board to detach the keyboard.

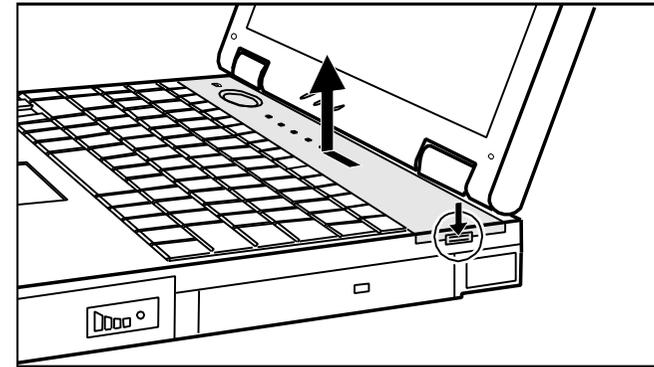


Figure 5-19. Removing the LED Panel

### ● Reassembly

1. Reconnect the keyboard cable and fit the keyboard back into place. (Refer to Figure 5-20 earlier.)
2. Replace the LED panel. (Refer to Figure 5-19 earlier.)

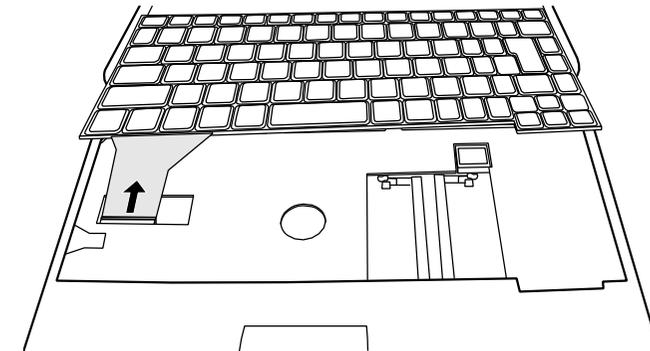


Figure 5-20. Removing the Keyboard

# 6120N N/B MAINTENANCE

## 5.2.8 SO-DIMM

### ● Disassembly

1. Remove the keyboard. (See section 5.2.7 Disassembly.)
2. Pull the retaining clips outwards and remove the SO-DIMM. (Refer to Figure 5-21.)

### ● Reassembly

1. To install the SO-DIMM, align the SO-DIMM's notched part with the socket's corresponding part and firmly insert the SO-DIMM into the socket at an angle. Then push down until the retaining clips lock the SO-DIMM into position. (Refer to Figure 5-21.)
2. Replace the keyboard. (See section 5.2.7 Reassembly.)

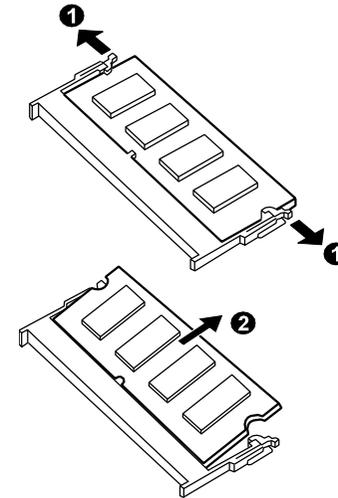


Figure 5-21. Removing the SO-DIMM

# 6120N N/B MAINTENANCE

## 5.2.9 LCD Assembly

### ● Disassembly

1. Remove the hinge cover by inserting a flat screwdriver to the rear of the cover and pry the cover out. Repeat the same with the other hinge cover. (Refer to Figure 5-22).  
\*Note the right and left hinges are not exchangeable.
2. Open the cover and remove the LED panel. (See section 5.2.7 Disassembly step 2.)
3. Disconnect two cables and remove four screws from the hinges. Now you can separate the LCD assembly from the base unit.

### ● Reassembly

1. Attach the LCD assembly to the base unit and secure with four screws on the hinges. Then reconnect the LCD cables to the system board. (Refer to Figure 5-23.)
2. Replace the LED panel.
3. Replace the two hinge covers. (Refer to Figure 5-22 earlier.)

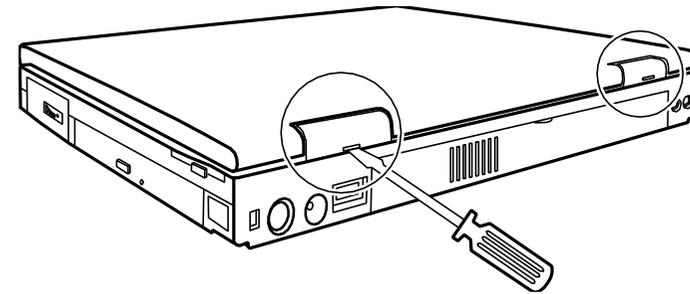


Figure 5-22. Removing the Hinge Covers

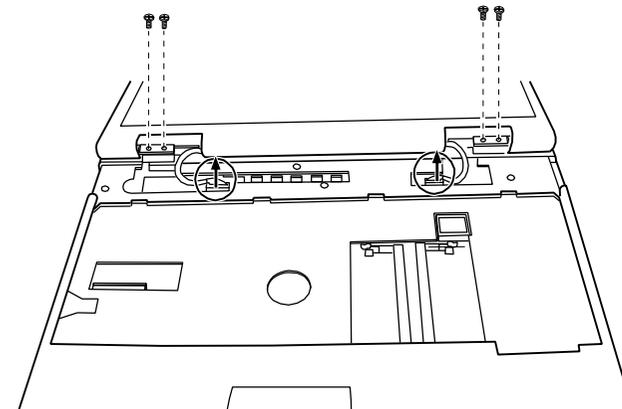


Figure 5-23. Unplugging two Cables and Removing Four Screws

# 6120N N/B MAINTENANCE

## 5.2.10 LCD Panel

### ● Disassembly

1. Open the top cover.
2. Remove the two rubber pads and two screws on the lower part of the panel. Then insert a flat screwdriver to the lower part of the frame and gently pry the frame out. Repeat the process until the frame is completely separated from the housing.
3. To remove the LCD, remove three screws and unplug the inverter cable.

### ● Reassembly

1. Reconnect the cable to the inverter board. Fit the LCD back into place and secure with three screws. (Refer to Figure 5-25.)
2. Fit the LCD frame back to the housing. Replace the two screws and two rubber pads. (Refer to Figure 5-24 earlier.)

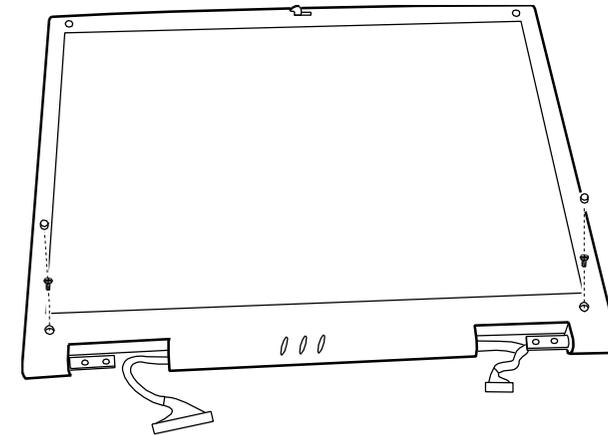


Figure 5-24. Removing the LCD Frame

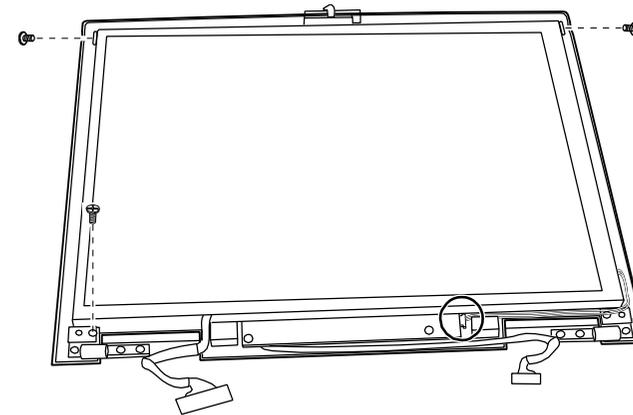


Figure 5-25. Removing the LCD

# 6120N N/B MAINTENANCE

## 5.2.11 Inverter/LED Board

### ● Disassembly

1. Detach the LCD frame. (See section 5.2.10 Disassembly step 1 and 2.)
2. To remove the inverter/LED board at the bottom side of the LCD , remove two screws and unplug the cable from the board.

### ● Reassembly

1. Reconnect the inverter cable. Fit the inverter/LED board back into place and secure with two screws. (Refer to Figure 5-26.)
2. Place the LCD frame back to the housing. (See section 5.2.10 Reassembly step 2.)

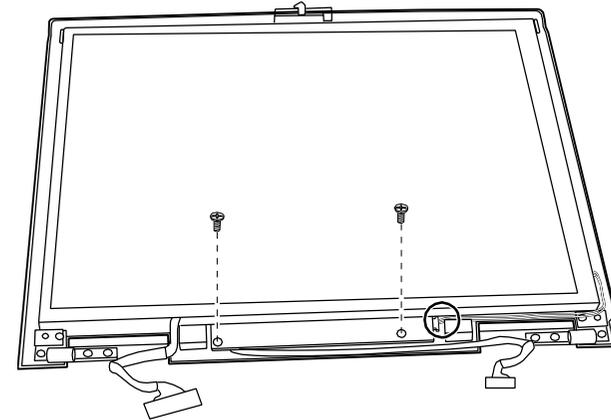


Figure 5-26. Removing the Inverter/LED Board

# 6120N N/B MAINTENANCE

## 5.2.12 Battery/Touchpad Board

### ● Disassembly

1. Remove the battery pack. (See section 5.2.1 Disassembly.)
2. Remove the CD-ROM/DVD-ROM drive. (See section 5.2.2 Disassembly.)
3. Remove the FDD/HDD module. (See section 5.2.3 Disassembly step 1 and 2.)
4. Remove the CPU module. (See section 5.2.5 Disassembly.)
5. Remove the Modem card (if exist). (See section 5.2.6 Disassembly.)
6. Remove nine screws fastening the base unit frame.  
Lift the frame free from the housing. (Refer to Figure 5-27.)
7. Remove seven screws fastening the metal shield. (Refer to Figure 5-28.)
8. After removing the base frame, you will see the battery/touchpad board in between the speakers. To remove the board, first remove three screws and unplug three cables(Refer to Figure 5-29.), then lift it free from the system board.

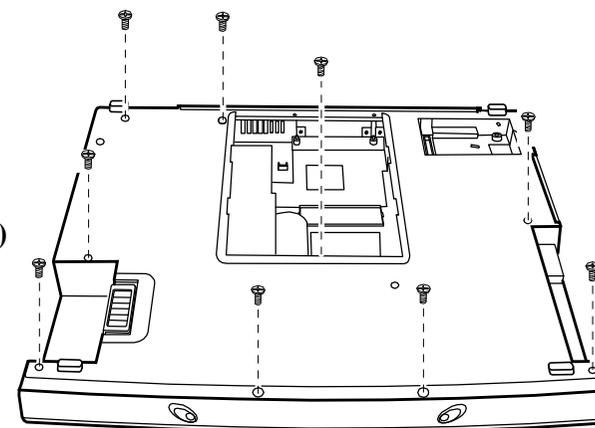


Figure 5-27. Removing the Base Frame Screws

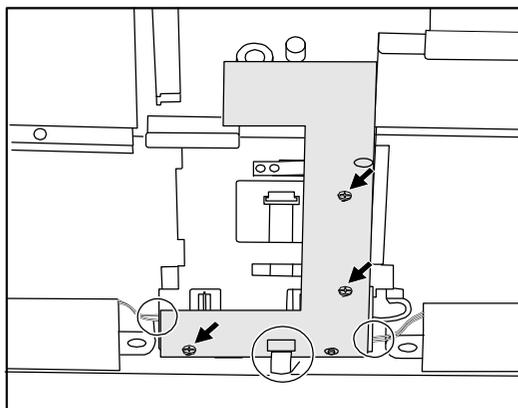


Figure 5-29. Removing the Battery/Touchpad Board

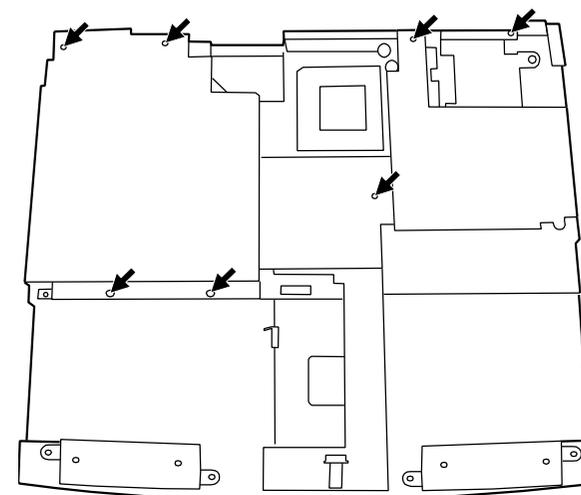


Figure 5-28. Removing the Battery/Touchpad Board

# **6120N N/B MAINTENANCE**

## **5.2.12 Battery/Touchpad Board**

### **● Reassembly**

- 1. Reconnect the battery/touchpad board to the system board. Plug three cables and secure the board with three screws. (Refer to Figure 5-29 earlier.)**
- 2. Replace the metal shield. Secure the shield with seven screws. (Refer to Figure 5-28 earlier.)**
- 3. Replace the base unit frame. Secure the frame with nine screws. (Refer to Figure 5-27 earlier.)**
- 4. Replace the Modem card (if exist). (See section 5.2.6 Reassembly.)**
- 5. Replace the CPU module. (See section 5.2.5 Reassembly.)**
- 6. Replace the FDD/HDD module. (See section 5.2.3 Reassembly step 2.)**
- 7. Replace the CD-ROM/DVD-ROM drive. (See section 5.2.2 Reassembly.)**
- 8. Replace the battery pack. (See section 5.2.1 Reassembly.)**

# 6120N N/B MAINTENANCE

## 5.2.13 System Board

### ● Disassembly

1. Remove the keyboard. (See section 5.2.7 Disassembly.)
2. Remove the LCD assembly. (See section 5.2.9 Disassembly.)
3. Remove one screw fastening the system board.

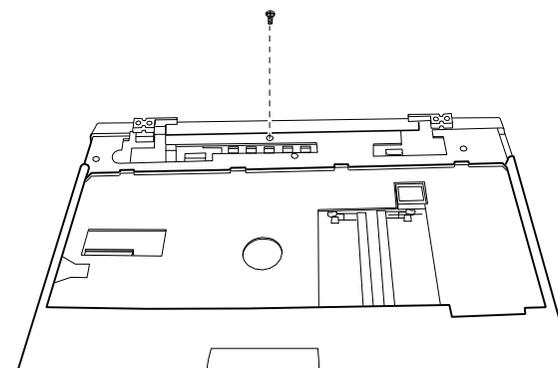


Figure 5-30. Removing One Screw Fastening the System Board

4. Put the notebook upside down with care.
5. Remove the base frame, metal shield, and battery/touchpad board. (See section 5.2.12 Disassembly.)
6. Remove two screws on the rear side.
7. Gently lift the system board free from the housing.

### ● Reassembly

1. Fit the system board into the housing and secure with two screws on the rear side. (Refer to Figure 5-31 earlier.)
2. Replace the battery/touchpad board and other components. (See section 5.2.12 Reassembly.)
3. Put the notebook surface up. Replace the LCD assembly. (See section 5.2.9 Reassembly.)
4. Replace one screw and the keyboard module. (Refer to Figure 5-30 earlier.)

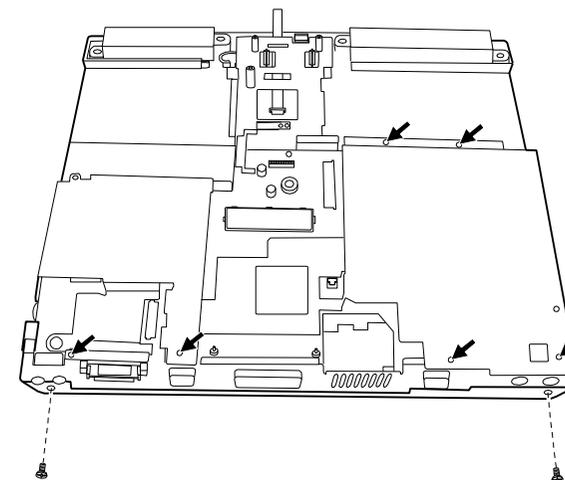


Figure Figure 5-31. Removing One Screw Fastening the System Board

# 6120N N/B MAINTENANCE

## 5.2.14 Touchpad Panel

### ● Disassembly

1. Remove the system board. (See section 5.2.13 Disassembly.)
2. The touchpad panel is located in between the speakers. To remove the panel, unfasten three screws and remove the metal cover, then you can lift the panel free from the housing. (Refer to Figure 5-32.)

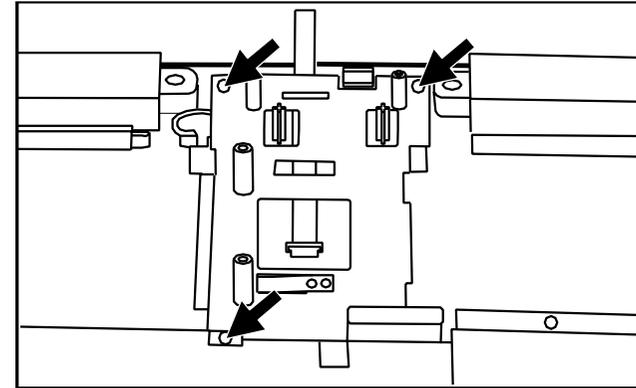


Figure 5-32. Removing Three Screws and Touchpad Panel

### ● Reassembly

1. Fit the touchpad panel back into place. Replace the metal cover and secure with three screws. (Refer to Figure 5-32 earlier.)
2. Replace the system board. (See section 5.2.13 Reassembly.)

# 6120N N/B MAINTENANCE

## 6. MAINTENANCE DIAGNOSTICS

### 6.1 INTRODUCTION

Each time the computer is turned on, the system BIOS runs a series of internal checks on the hardware. This power-on self test (post) allows the computer to detect problems as early as the power-on stage. Error messages of post can alert you to the problems of your computer.

If an error is detected during these tests, you will see an error message displayed on the screen. If the error occurs before the display is initialized, then the screen cannot display the error message. Error codes or system beeps are used to identify a post error that occurs when the screen is not available.

The value for the diagnostic port (378H) is written at the beginning of the test. Therefore, if the test failed, the user can determine where the problem occurred by reading the last value written to port 378H by the PIO debug board plug at PIO port.

# 6120N N/B MAINTENANCE

## 6.2 ERROR CODES

Following is a list of error codes in sequence display on the PIO debug board.

CODE	BEEP	Description
00H		START OF BOOT LOADER SEQUENCE.
01H		DISABLE A20 THROUGH A20, NOT SEND.
02H	.._.	INITIALIZE CHIPSET OR BIOS NOT SHADOWED.
03H		PERFORM CONVENTIONAL RAM TEST WITH CROSSED-PATTERN R/W.
04H	._..	MOVE BOOT LOADER TO THE RAM OR BIOS CHECKSUM BAD.
05H		START POINT OF EXECUTION OF BOOT LOADER IN RAM.
06H		PERFORM PNP INITIALIZATION FOR CRYSTAL AUDIO CHIP OR CHECK OVERRIDE OPTION, NOT SEND.
07H		SHADOW SYSTEM BIOS.
08H		CHECKSUM SYSTEM BIOS ROM, NOT SEND.
09H		PROCEED WITH NORMAL BOOT.
0AH		PROCEED WITH CRISIS BOOT.
0FH	—	NO RAM OR DRAM SIZING.
10H		INITIAL L1, L2 CACHE, MAKE STACK AND DIAGNOSE CMOS.
11H		TURN OFF FAST A20 FOR FOR POST. RESET GDTs, 8259s QUICKLY.
12H		SIGNAL POWER ON RESET AT CMOS.
13H		INITIALIZE THE CHIPSET, (SDRAM)**SOLUTION: TRY TO CLEAR CMOS**
14H		SEARCH FOR ISA BUS VGA ADAPTER.
15H		RESET COUNTER/TIMER 1.
16H		USER REGISTER CONFIG THROUGH CMOS.
18H		DISPATCH TO 1ST 64K RAM TEST.
19H		CHECKSUM THE ROM.
1AH		RESET PICs(8259).
1BH		INITIALIZE VIDEO ADAPTER(S).
1CH		INITIALIZE VIDEO (6845 REGS).
1DH		INITIALIZE COLOR ADAPTER.
1EH		INITIALIZE MONOCHROME ADAPTER.
1FH		TEST 8237A PAGE REGISTERS.
20H		PERFORM KEYBOARD SELF TEST.
21H		TEST & INITIALIZE KEYBOARD CONTROLLER.
22H		CHECK IF CMOS RAM VALID.
23H		TEST BATTER FAIL & CMOS X-SUM.
24H		TEST THE DMA CONTROLLER.
25H		INITIALIZE 8237A CONTROLLER.
26H		INITIALIZE INTERRUPT VECTORS TABLE.
27H		RAM QUICK SIZING.

CODE	BEEP	Description
28H		PROTECTED MODE ENTERED SAFELY.
29H		RAM TEST COMPLETED.
2AH		PROTECTED MODE EXIT SUCCESSFUL .
2BH		SETUP SHADOW.
2CH		PREPARE TO INITIALIZE VIDEO.
2DH		SEARCH FOR MONOCHROME ADAOTER.
2EH		SEARCH FOR COLOR ADAPTER, VGA INITIALIZE.
2FH		SIGN-ON MESSAGES DISPLAYED.
30H		SPECIAL INIT OF KEYBOARD CONTROLLER.
31H		TEST IF KEYBOARD PRESENT.
32H		TEST KEYBOARD INTERRUPT.
33H		TEST KEYBOARD COMMAND BYTE.
34H		TEST, BLANK AND COUNT ALL RAM.
35H		PROTECTED MODE ENTERED SAFELY(2).
36H		RAM TEST COMPLETED.
37H		PROTECTED MODE EXIT SUCCESSFUL .
38H		UPDATE KEYBOARD OUTPUT PORT TO DISABLE GATE OF A20.
39H		SETUP CACHE CONTROLLER.
3AH		TEST IF 18.2HZ PERIODIC WORKING.
3BH		INITIALIZE BIOS DATA AREA AT 40:0.
3CH		INITIALIZE THE HARDWARE INTERRUPT VECTOR.
3DH		SEARCH AND INIT THE MOUSE.
3EH		UPDATE NUMLOCK STATUS.
3FH		OEM INITIALIZATION OF COMM AND LPT PORTS.
40H		CONFIGURE THE COMM AND LPT PORTS.
41H		INITIALIZE THE FLOPPIES.
42H		INITIALIZE THE HARD DISK.
43H		INITIALIZE ADDITIONAL ROMS.
44H		OEM'S INIT OF POWER MANAGEMENT, (CHECK SMD).
45H		UPDATE NUMLOCK STATUS.
46H		TEST FOR COPROCESSOR INSTALLED.
47H		OEM FUNCTIONS BEFORE BOOT(PCMCIA, CARDBUSS).
48H		DISPATCH TO OPERATION SYSTEM BOOT.
49H		JUMP INTO BOOTSTRAP CODE.
4AH		OEM'S INIT OF PM WITH USB.
FO~FIH	....	RMA TEST FAILED.

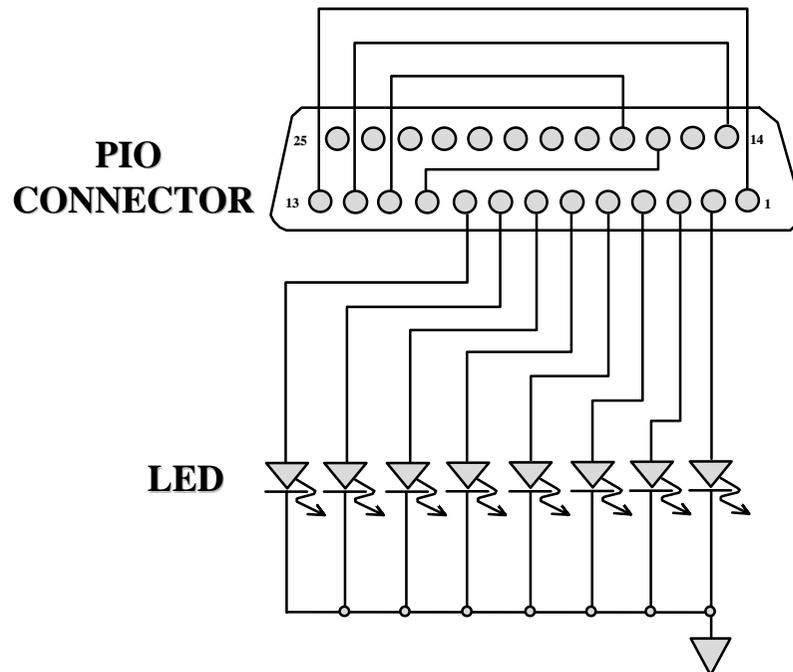
# 6120N N/B MAINTENANCE

## 6.3 PIO PORT (378H) DIAGNOSTIC TOOLS

### 6.3.1 PARTS USED:

- LED \* 8
- PIO CONNECTOR \* 1

### 6.3.2 CIRCUIT:



PIN1 : STROBE ↔ PIN 13 : SLCT

PIN10: ACK# ↔ PIN 16 : INT#

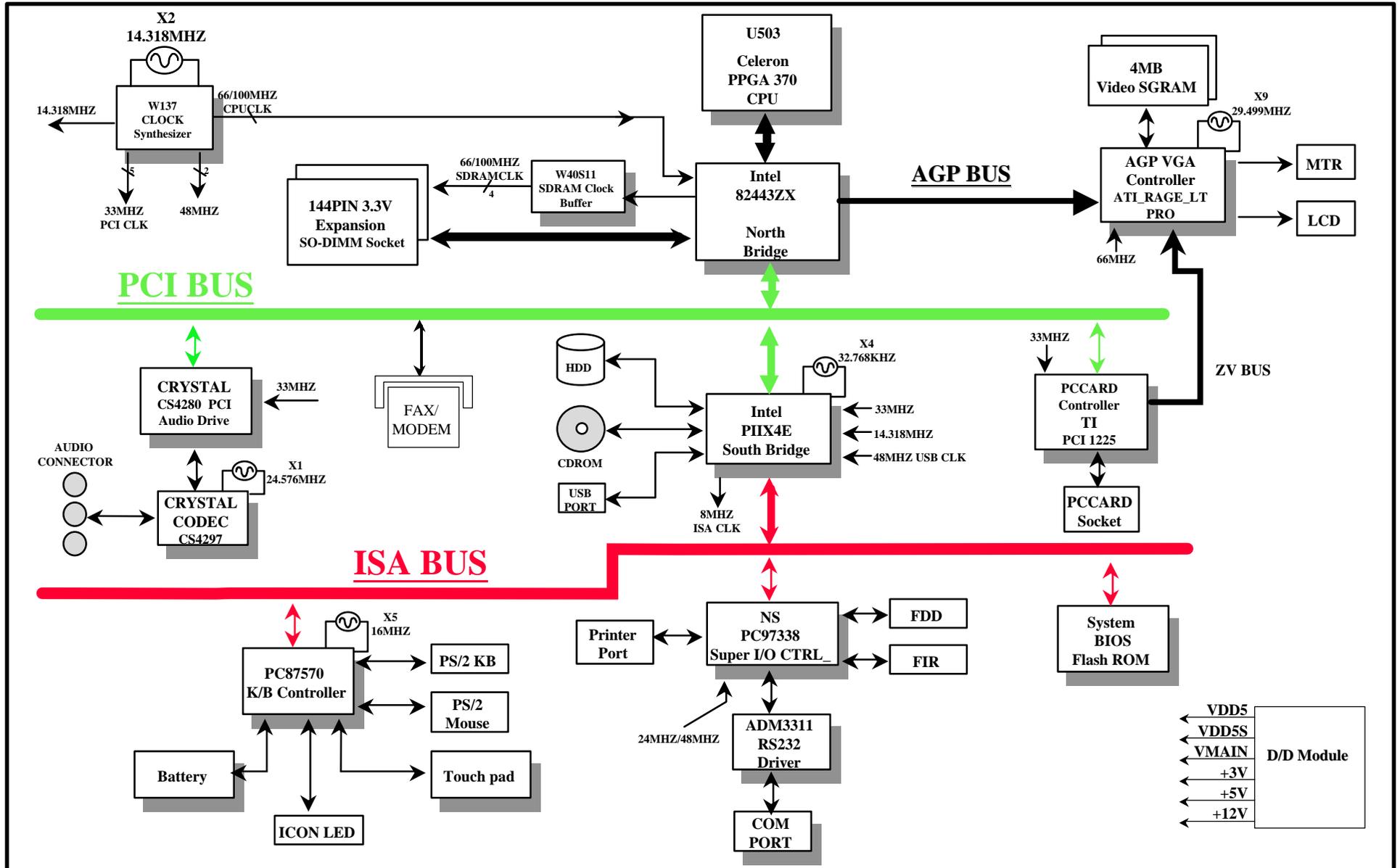
PIN11: BUSY ↔ PIN 17 : SELIN#

PIN12: PTERR ↔ PIN 14 : AUTOFD#

PIN{9:2}: PD{7:0}

# 6120N N/B MAINTENANCE

## 7. System Block Diagram & Schematics



# 6120N N/B MAINTENANCE

## 8. TROUBLE SHOOTING

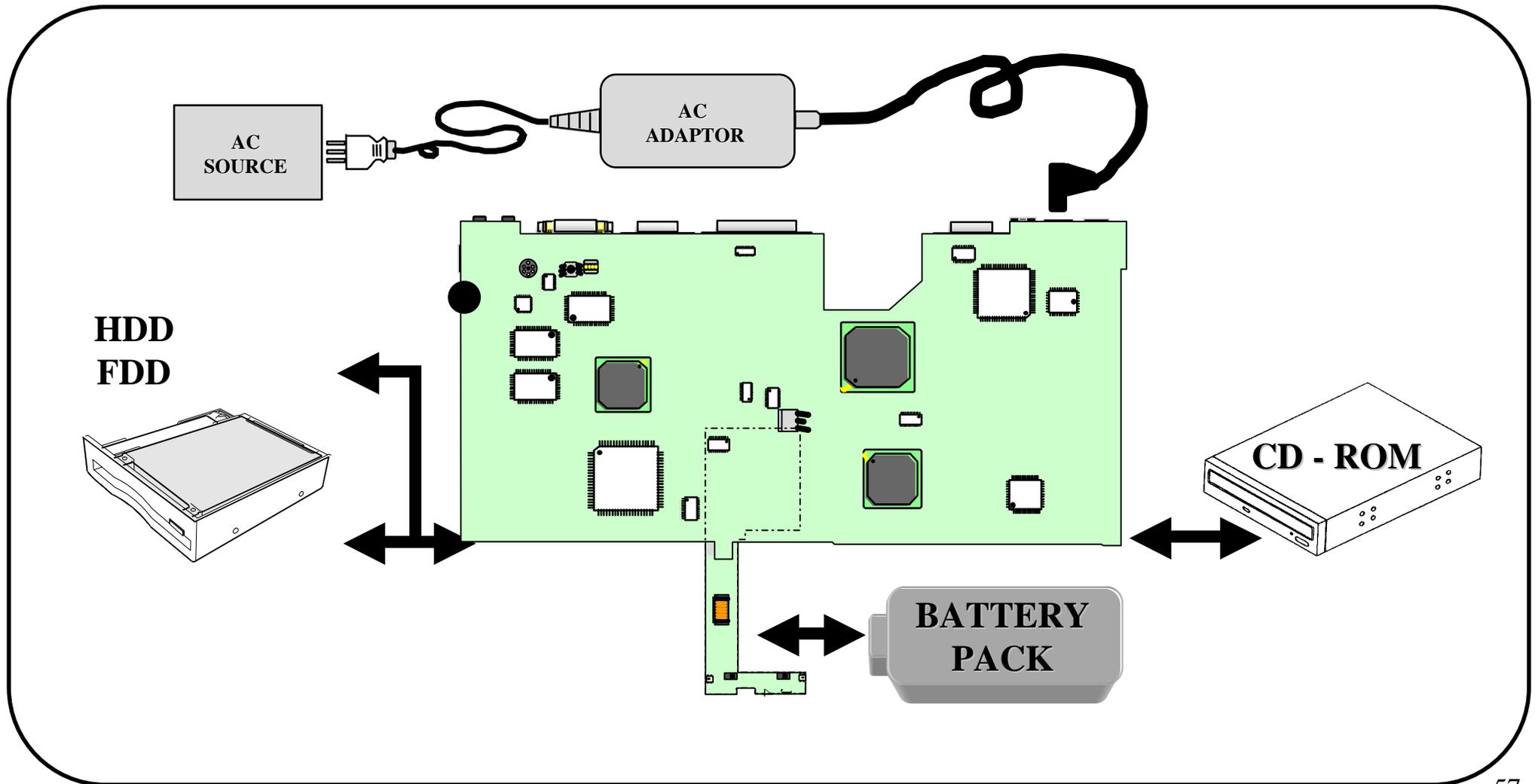
<del>8.1</del> No Power-----57	<del>8.10</del> Hard Disk Drive Test Error-----81
<del>8.2</del> No Display -----61	<del>8.11</del> CD-ROM Test Error-----83
<del>8.3</del> VGA Controller Failure-----65	<del>8.12</del> CMOS Test Error-----85
<del>8.4</del> LCD No Display-----67	<del>8.13</del> SIO Port Test Error-----87
<del>8.5</del> External Monitor No Display-----69	<del>8.14</del> PIO Port Test Error-----89
<del>8.6</del> Memory Test Error-----71	<del>8.15</del> IrDA TEST ERROR-----91
<del>8.7</del> Keyboard Test Error-----73	<del>8.16</del> USB Port Test Error-----93
<del>8.8</del> Track Pad/ball Test Error-----75	<del>8.17</del> Audio Drive Failure-----95
<del>8.9</del> Diskette Drive Test Error-----79	

# 6120N N/B MAINTENANCE

## 8.1 NO POWER

### Symptom:

When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.

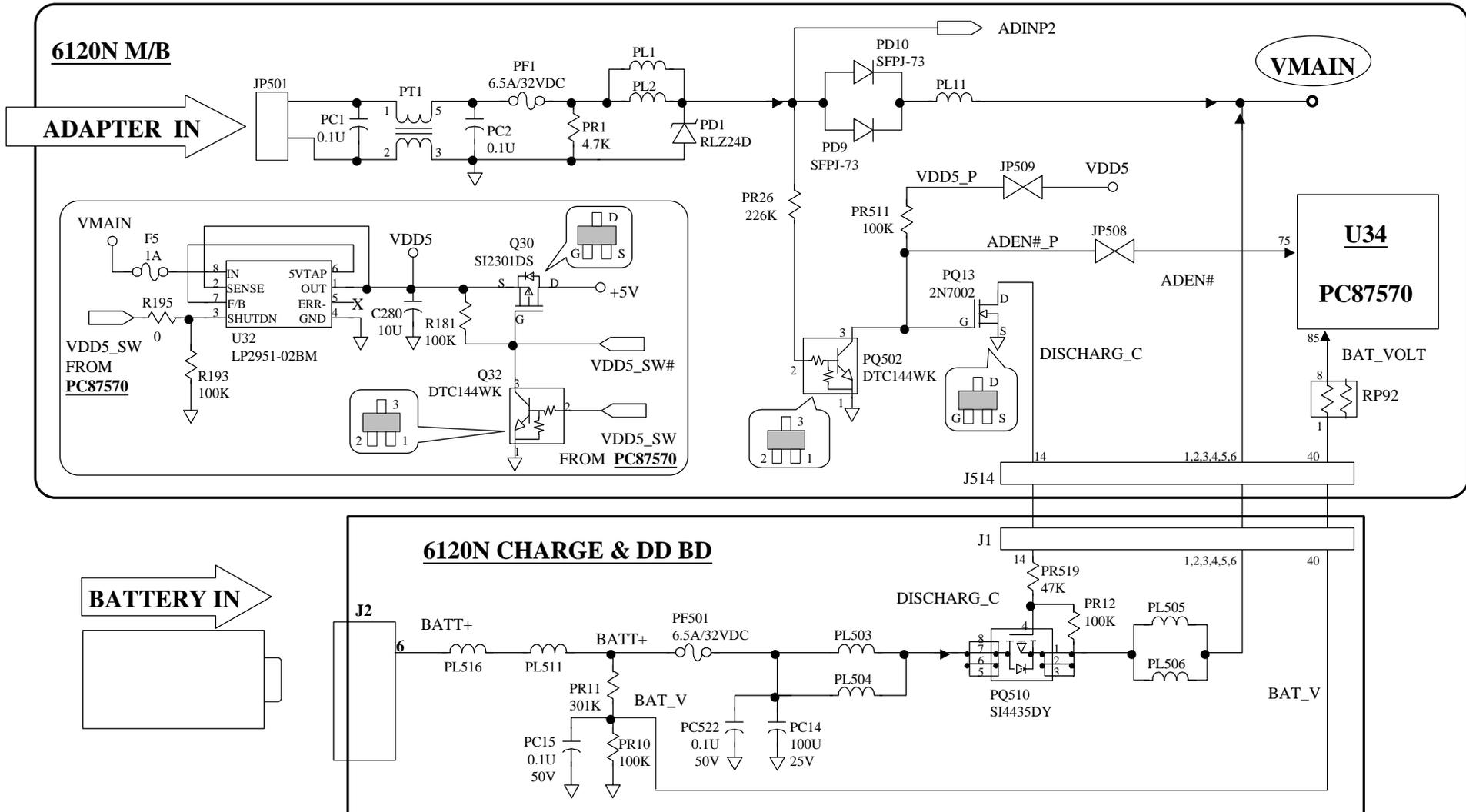


# 6120N N/B MAINTENANCE

## 8.1 NO POWER

### Symptom:

When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.



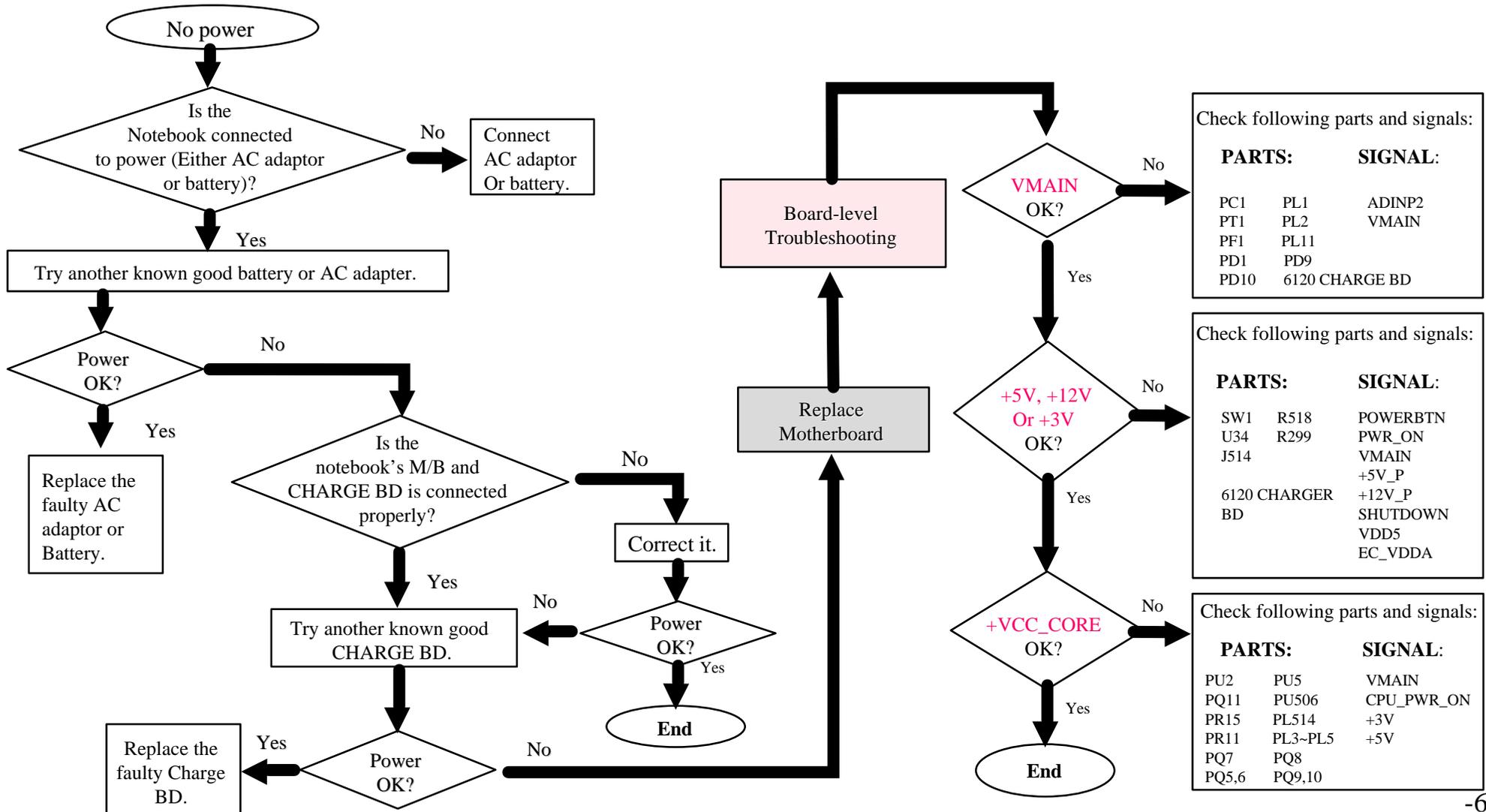


# 6120N N/B MAINTENANCE

## 8.1 NO POWER

### Symptom:

When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.

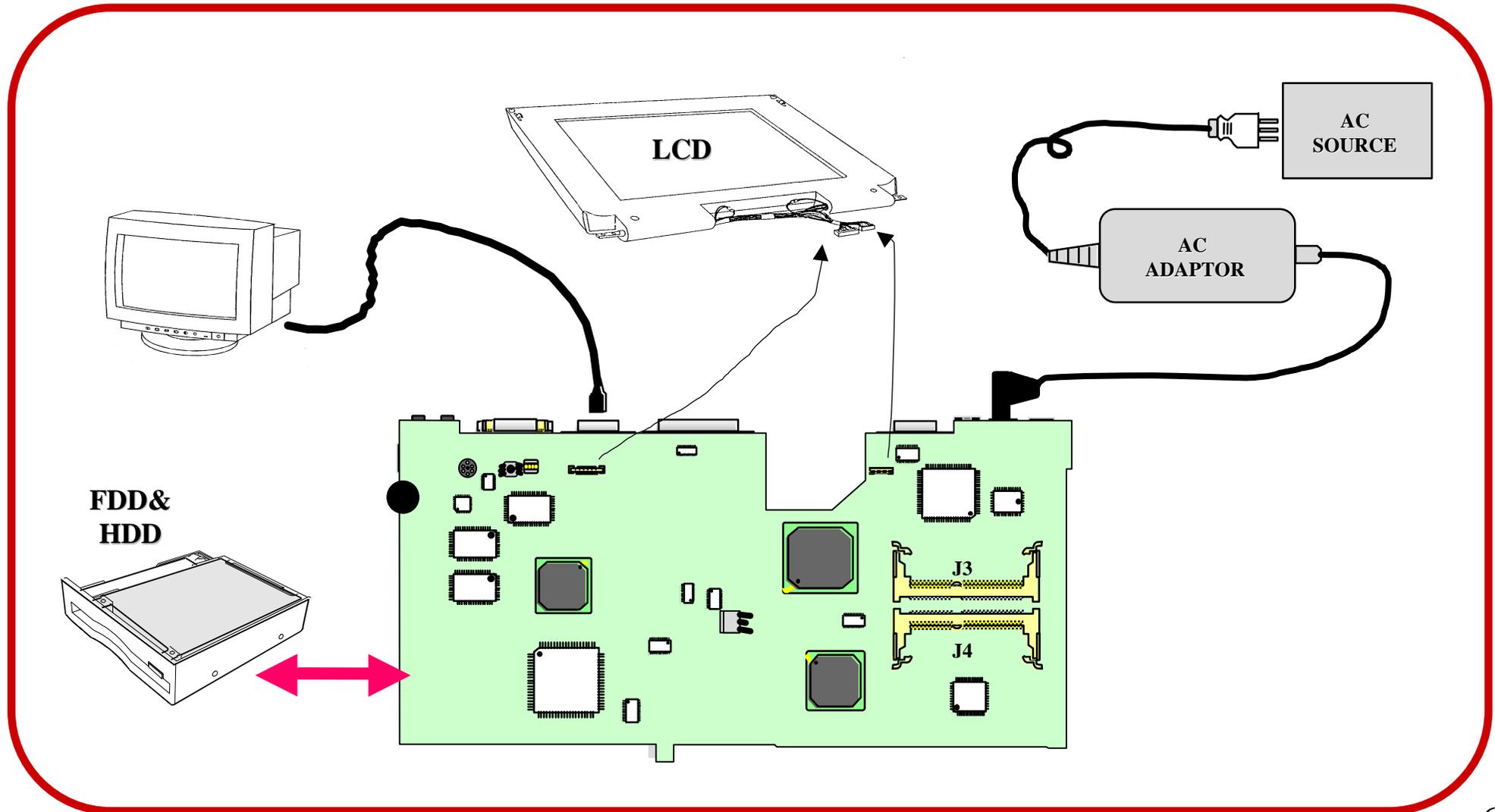


# 6120N N/B MAINTENANCE

## 8.2 NO DISPLAY (SYSTEM FAILURE)

Symptom:

There is no display on both LCD and monitor after power on although the LCD and monitor are known-good.

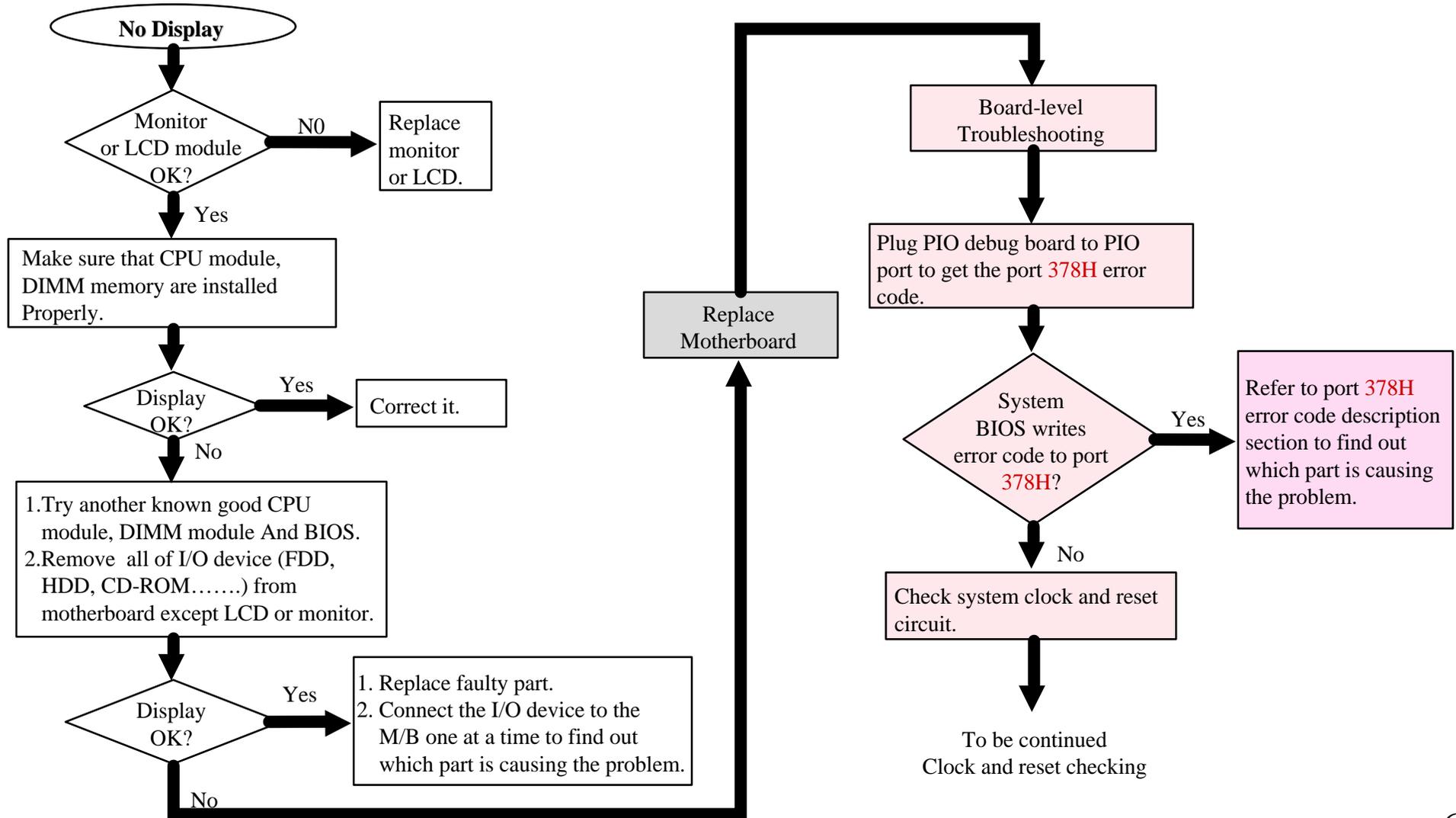


# 6120N N/B MAINTENANCE

## 8.2 NO DISPLAY (SYSTEM FAILURE)

### Symptom:

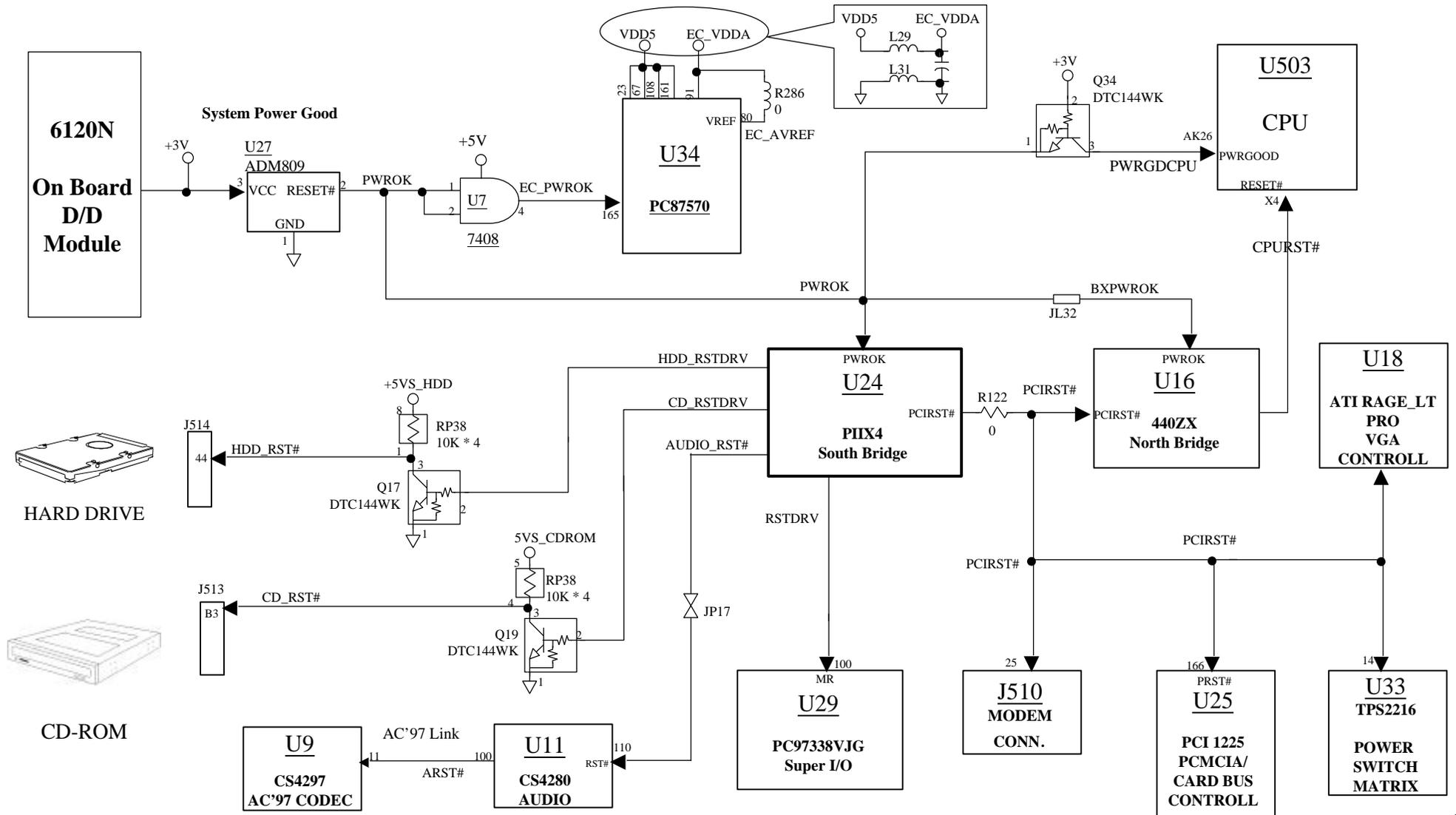
There is no display on both LCD and VGA monitor after power on although the LCD and monitor is known-good.



# 6120N N/B MAINTENANCE

## 8.2 NO DISPLAY (System Failure)

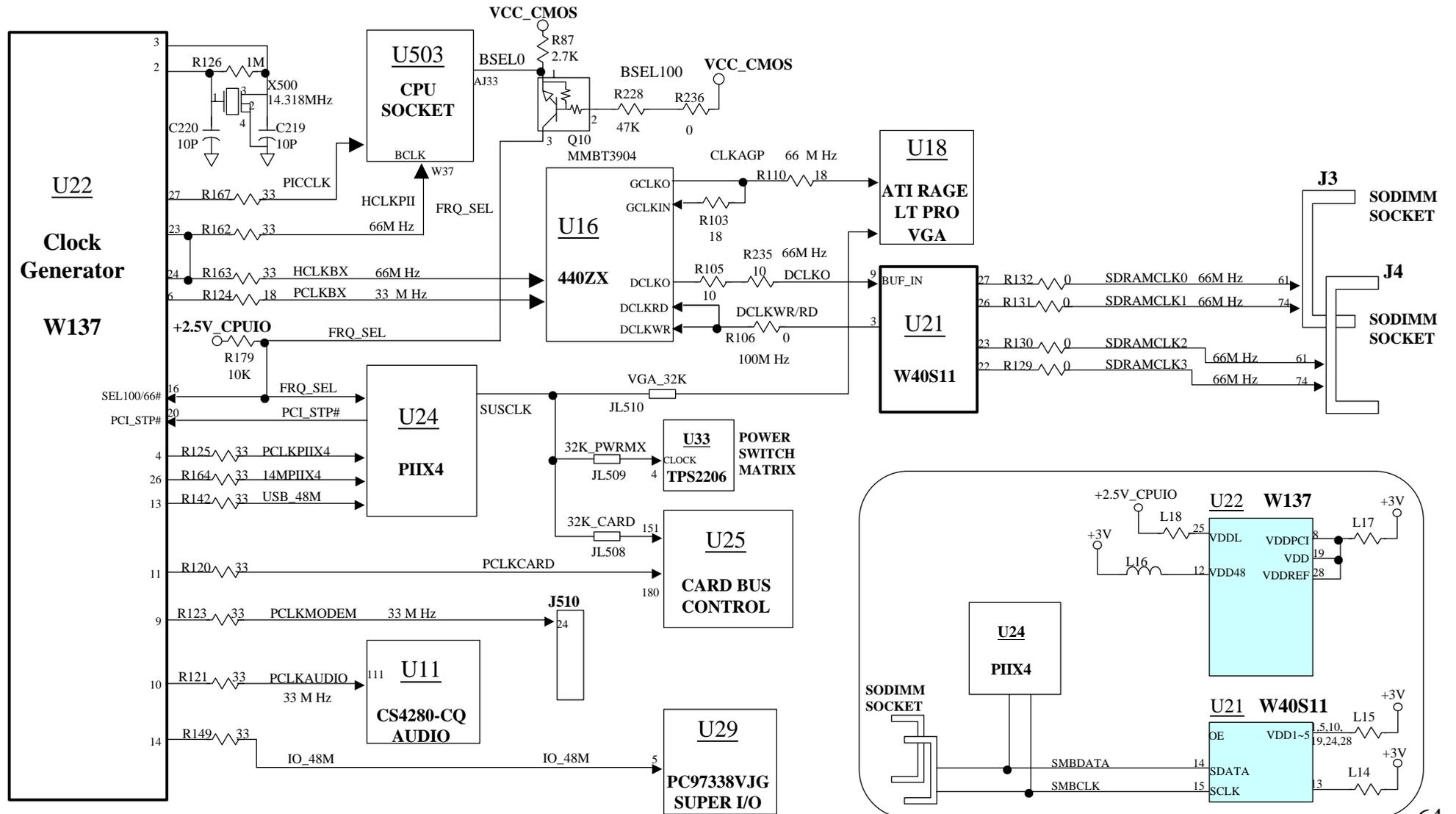
\*\*\*\*\* RESET CIRCUIT CHECKING \*\*\*\*\*



# 6120N N/B MAINTENANCE

## 8.2 NO DISPLAY (System Failure)

\*\*\*\*\* CLOCK CIRCUIT CHECKING \*\*\*\*\*

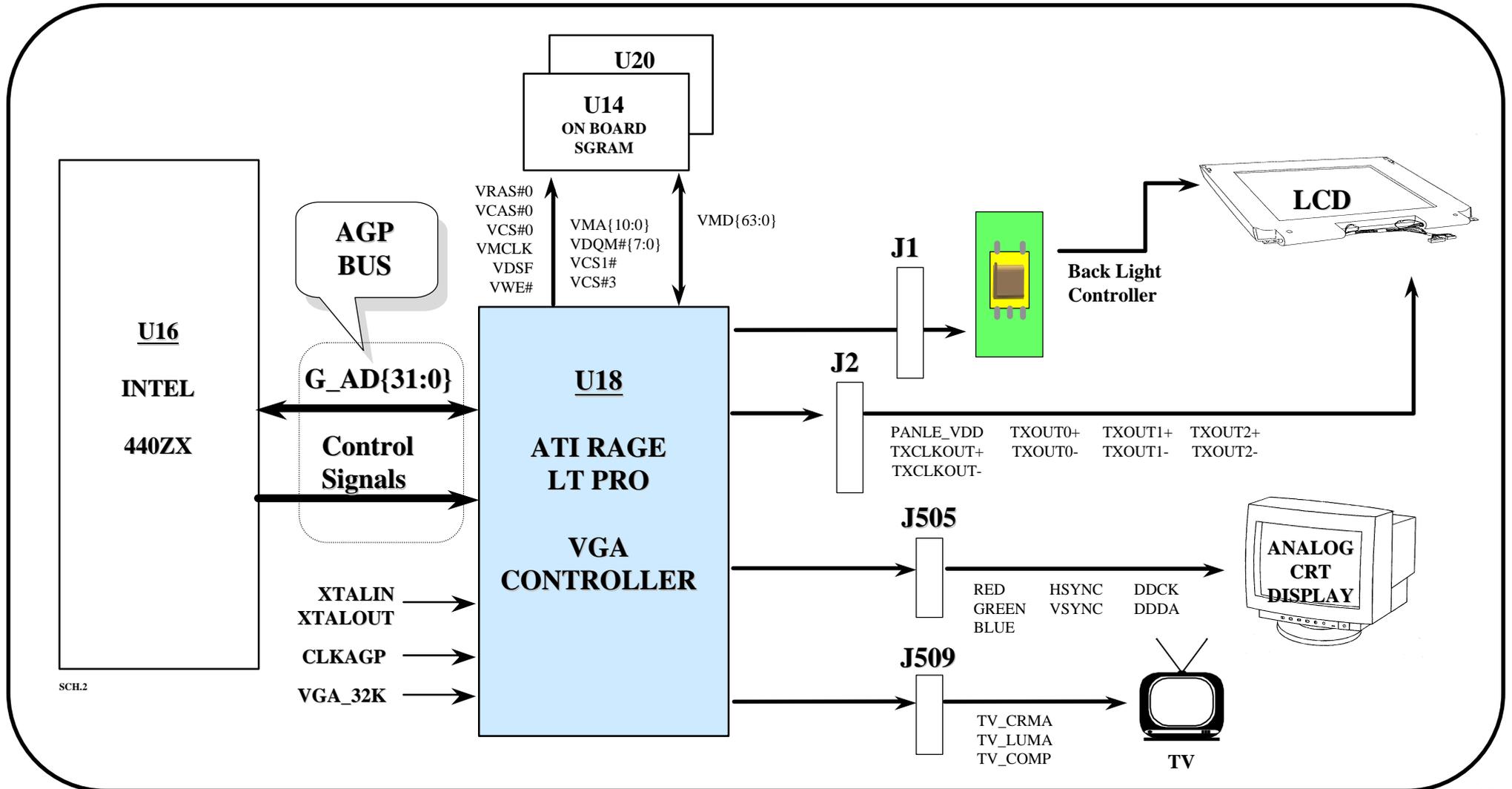


# 6120N N/B MAINTENANCE

## 8.3 VGA CONTROLLER FAILURE

Symptom:

There is no display on both LCD and Monitor although power-on-self-test is passed.

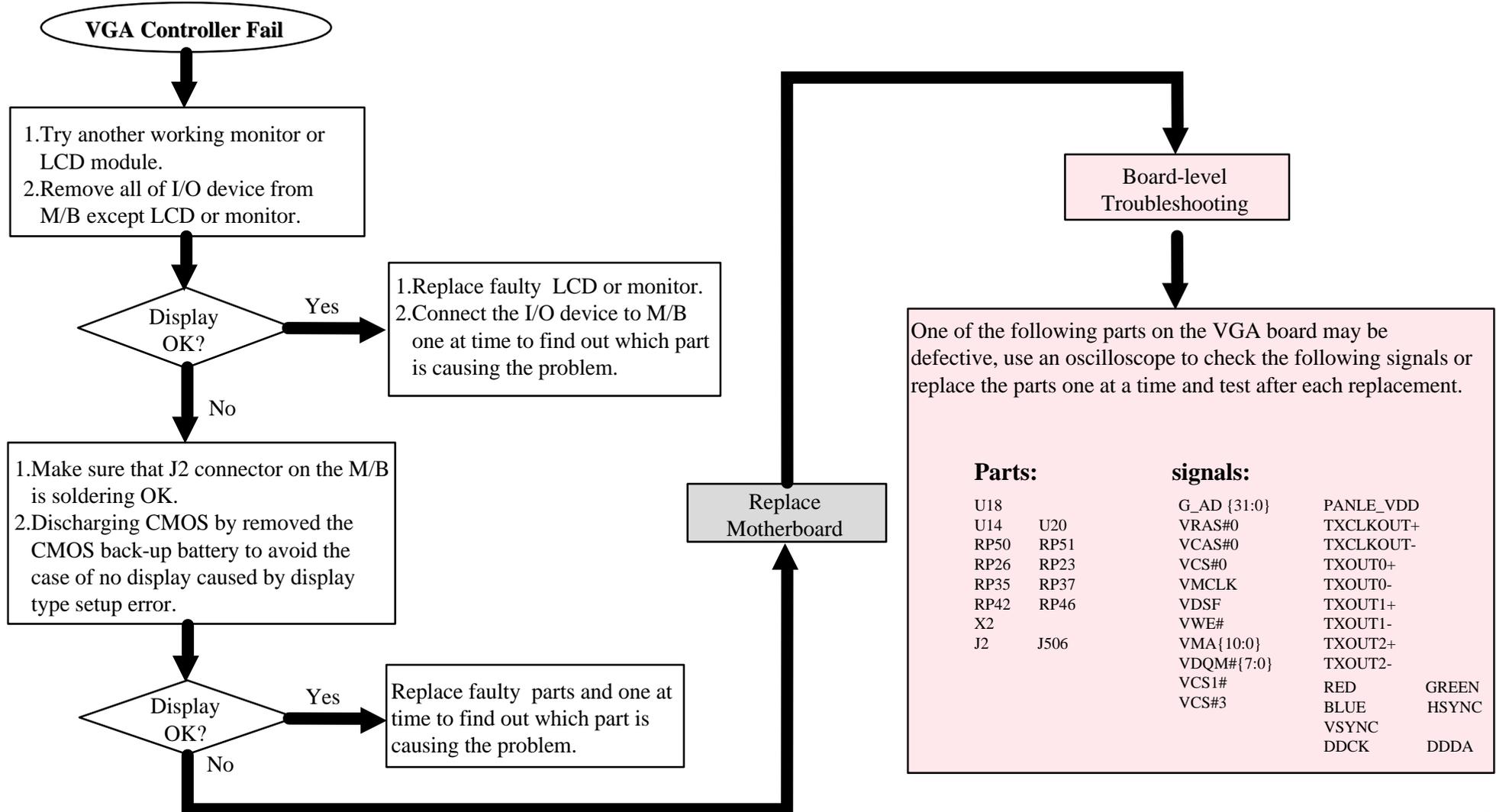


# 6120N N/B MAINTENANCE

## 8.3 VGA CONTROLLER FAILURE

### Symptom:

There is no display on both LCD and monitor although power-on-self-test is passed.

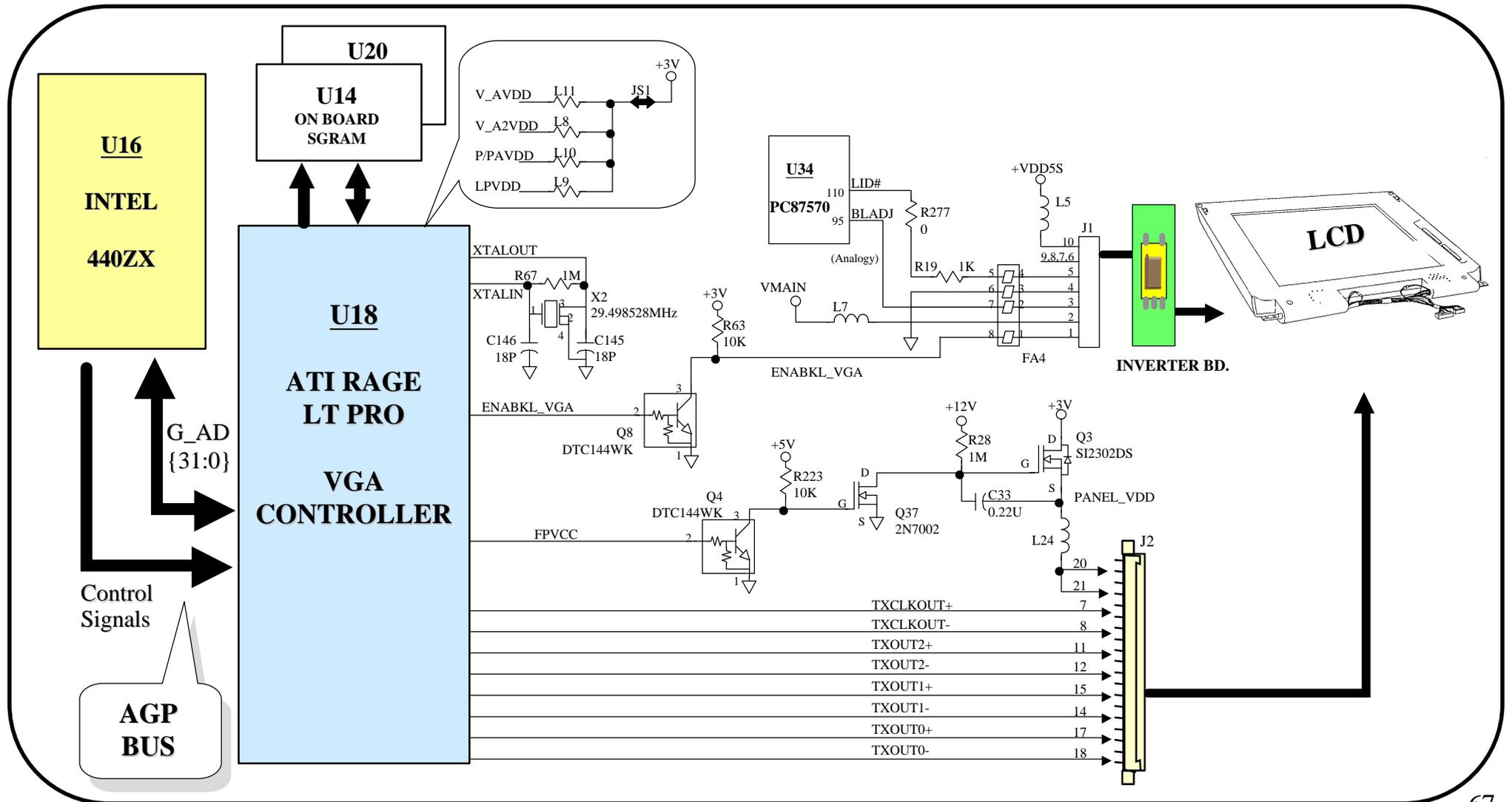


# 6120N N/B MAINTENANCE

## 8.4 LCD NO DISPLAY OR PICTURE ABNORMAL

Symptom:

The LCD shows nothing or abnormal picture, but it is ok for external monitor.

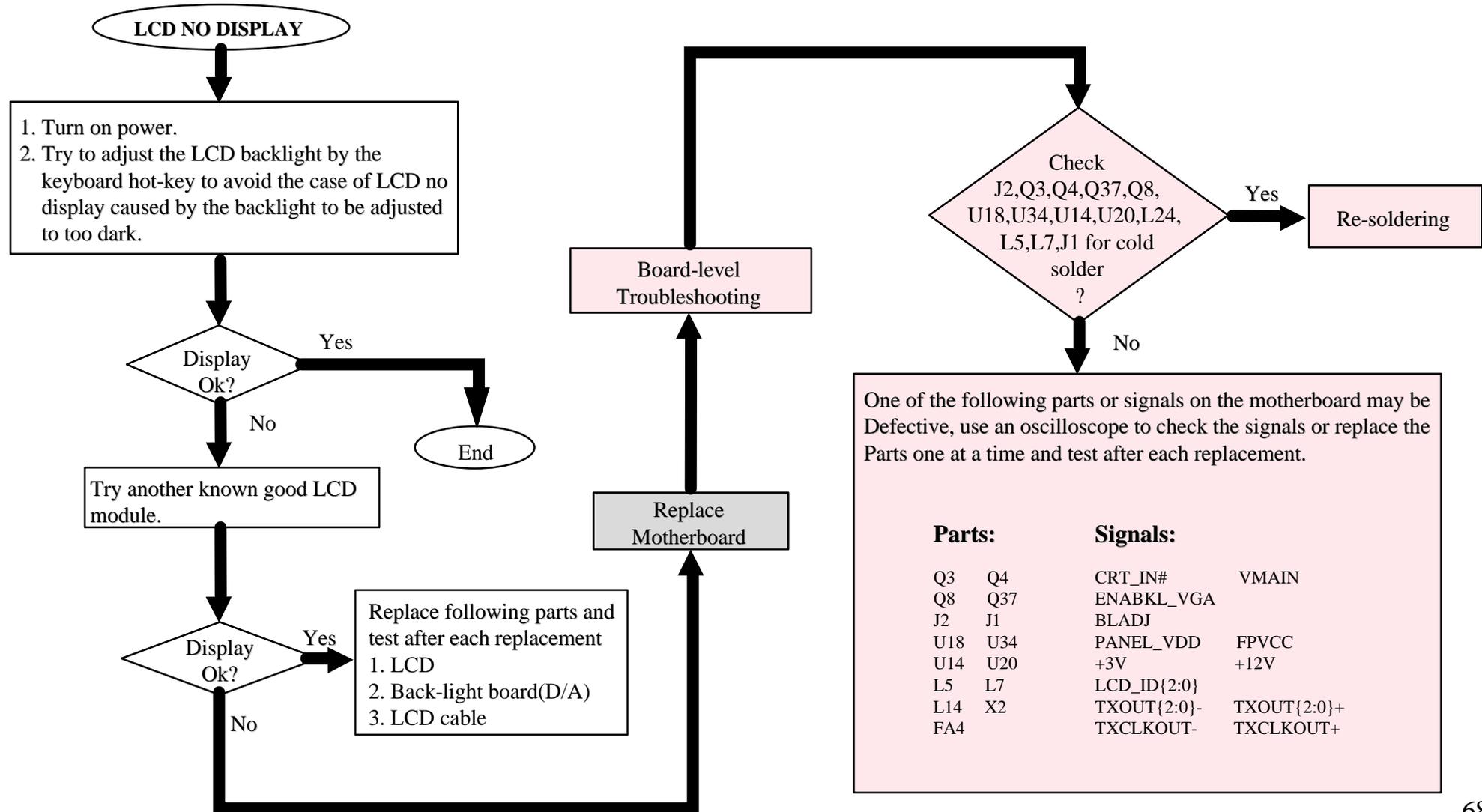


# 6120N N/B MAINTENANCE

## 8.4 LCD NO DISPLAY OR PICTURE ABNORMAL

### Symptom:

The LCD shows nothing or abnormal picture, but it is OK for external monitor.

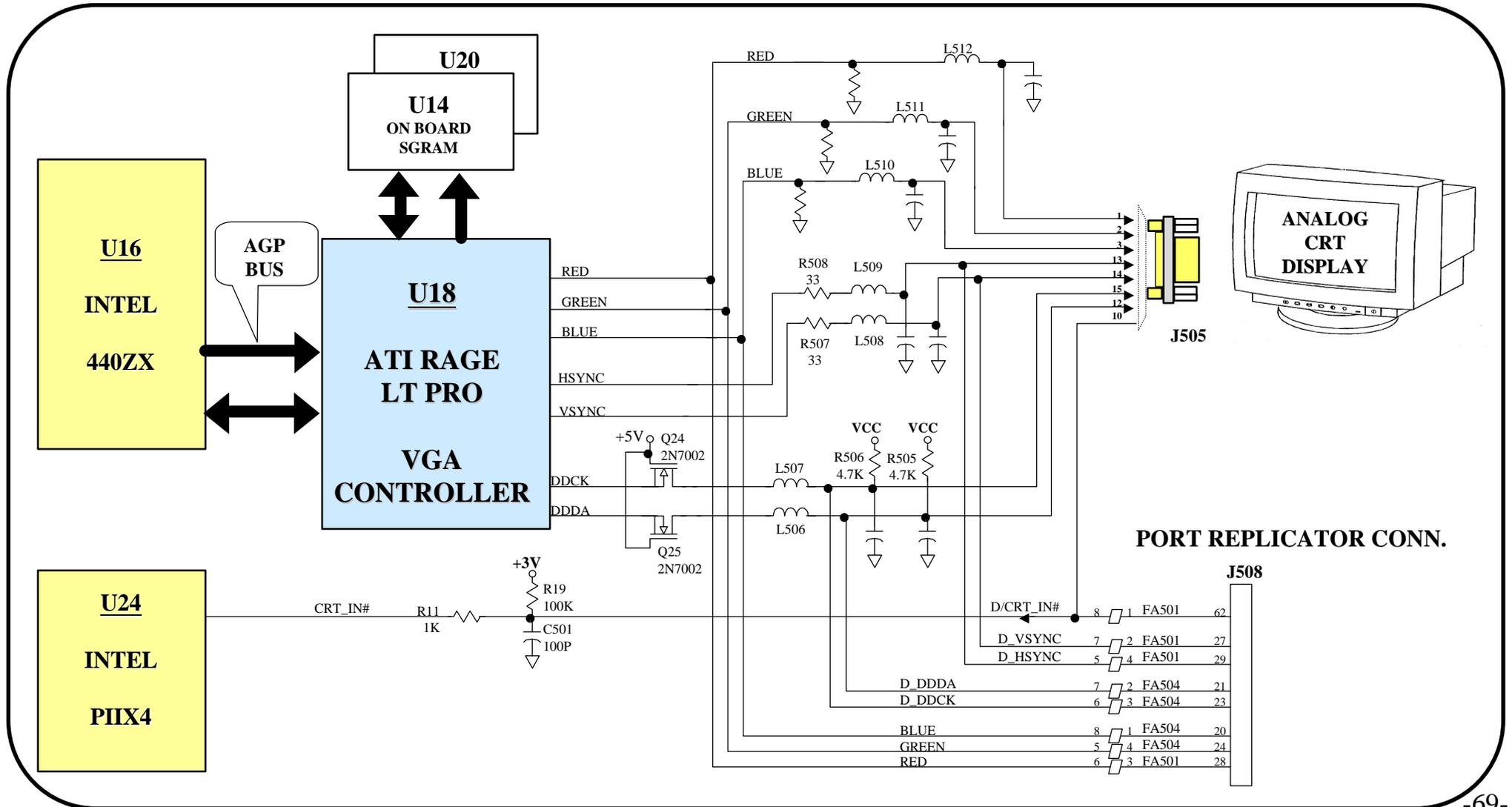


# 6120N N/B MAINTENANCE

## 8.5 EXTERNAL MONITOR NO DISPLAY OR COLOR ABNORMAL

Symptom:

The CRT monitor shows nothing or abnormal color, but it is ok for LCD

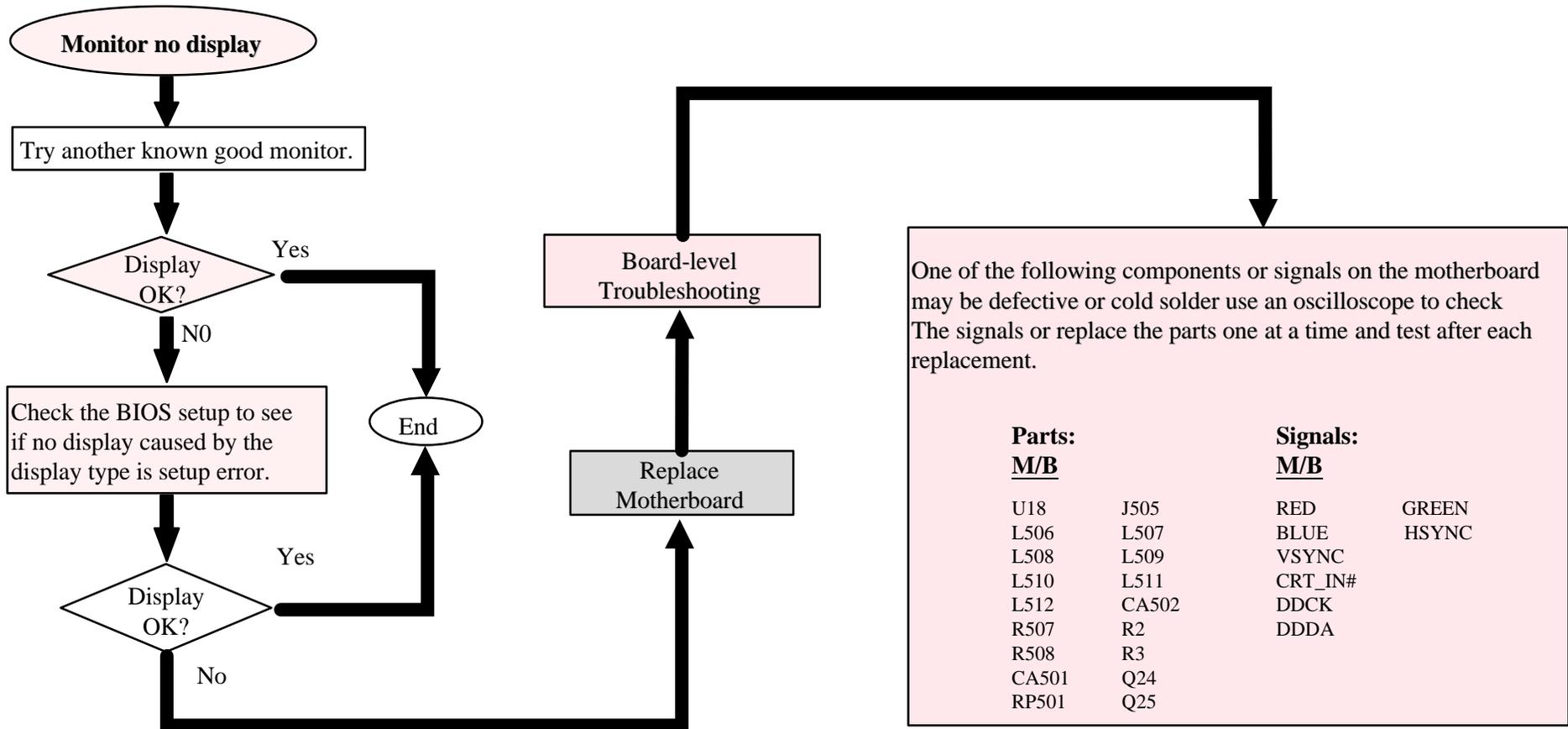


# 6120N N/B MAINTENANCE

## 8.5 EXTERNAL MONITOR NO DISPLAY OR COLOR ABNORMAL

### Symptom:

The CRT monitor shows nothing or abnormal color, but it is OK for LCD.

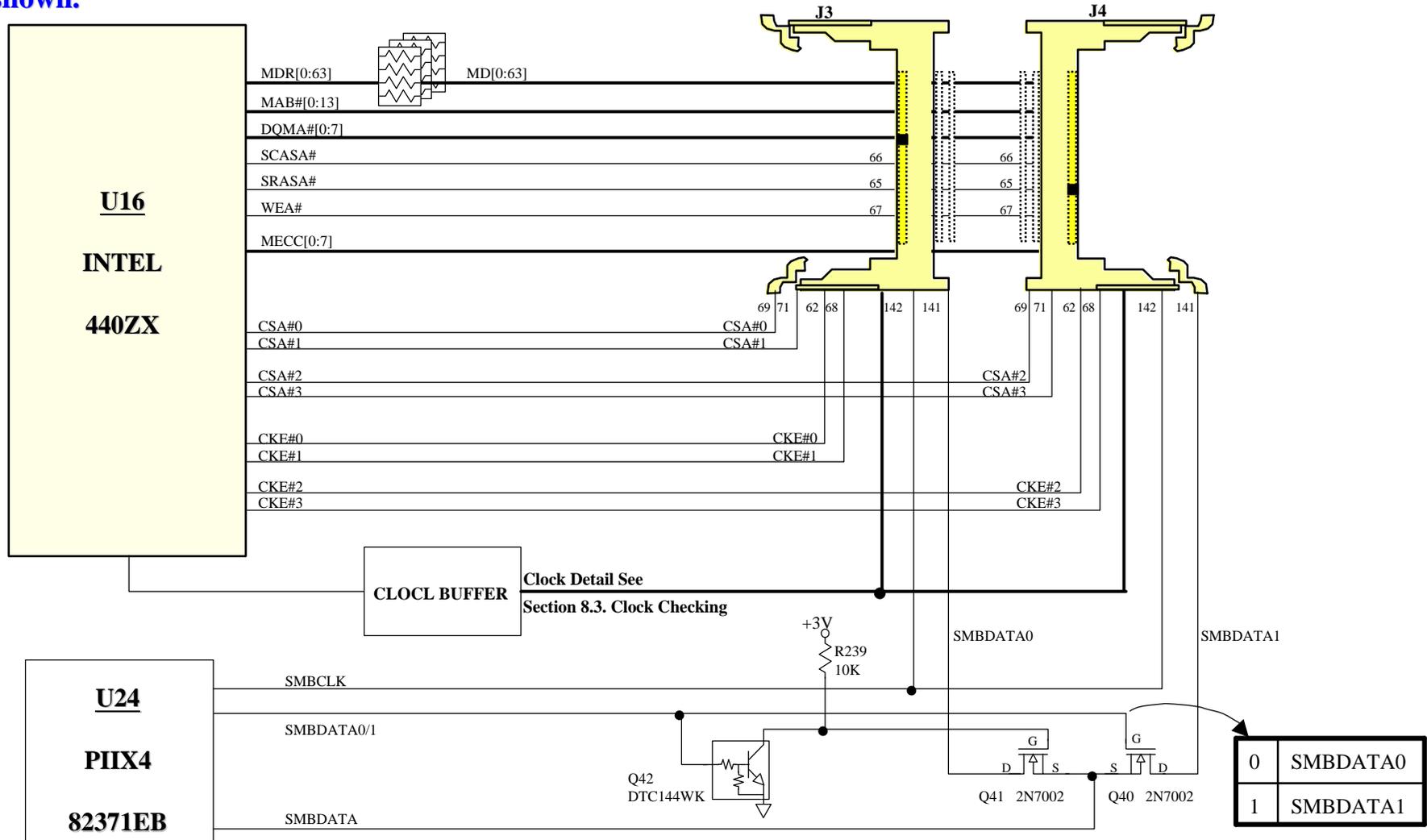


# 6120N N/B MAINTENANCE

## 8.6 MEMORY TEST ERROR

**Symptom:**

**PIO debug board shows the port 378H error code is stopped at 27H, 28H or 29H, or error message of memory failure is shown.**

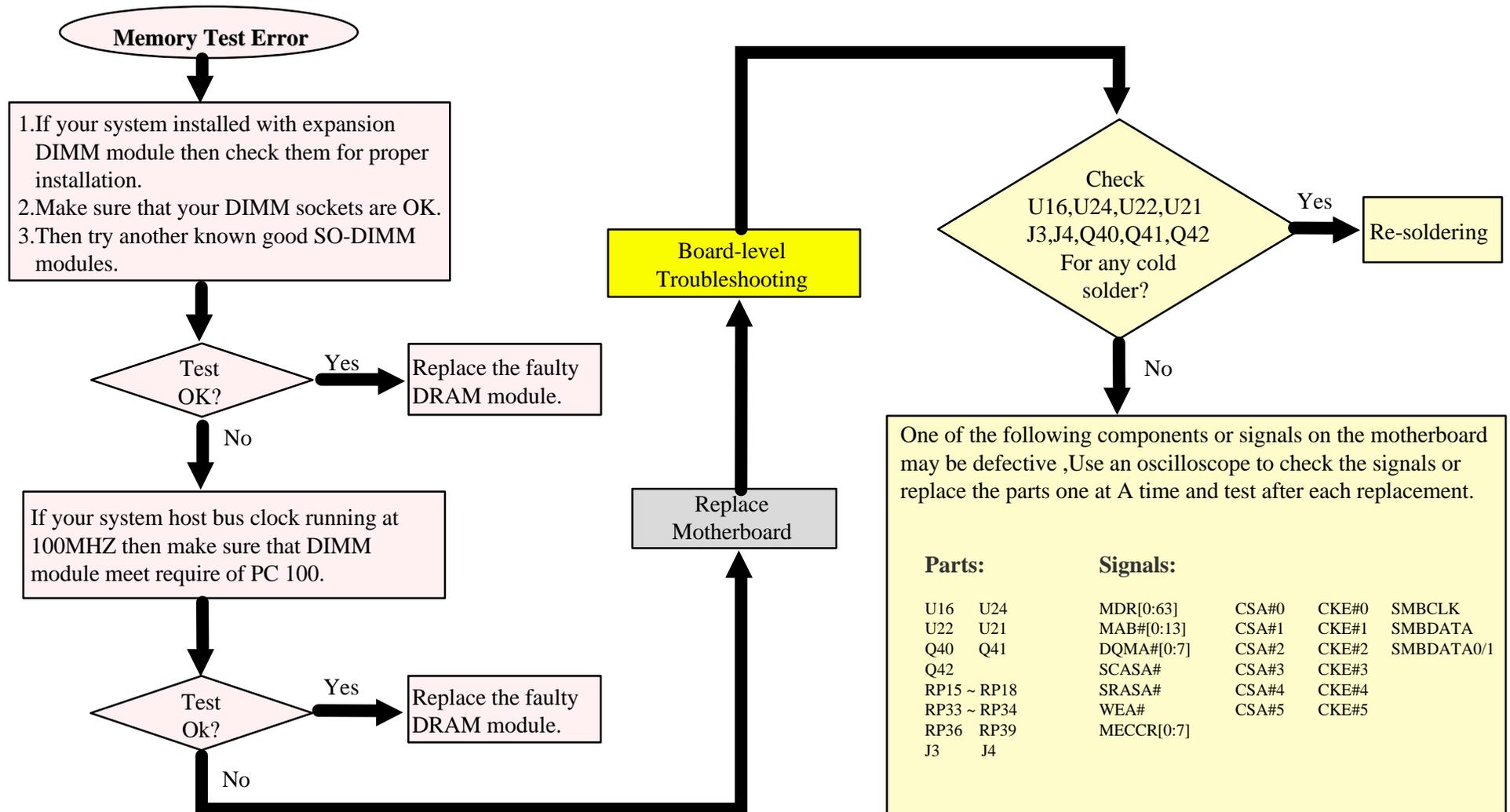


# 6120N N/B MAINTENANCE

## 8.6 MEMORY TEST ERROR

### Symptom:

PIO debug board shows the port **378H** error code is stopped at **27H,28H or 29H**, or error message of memory failure is shown.

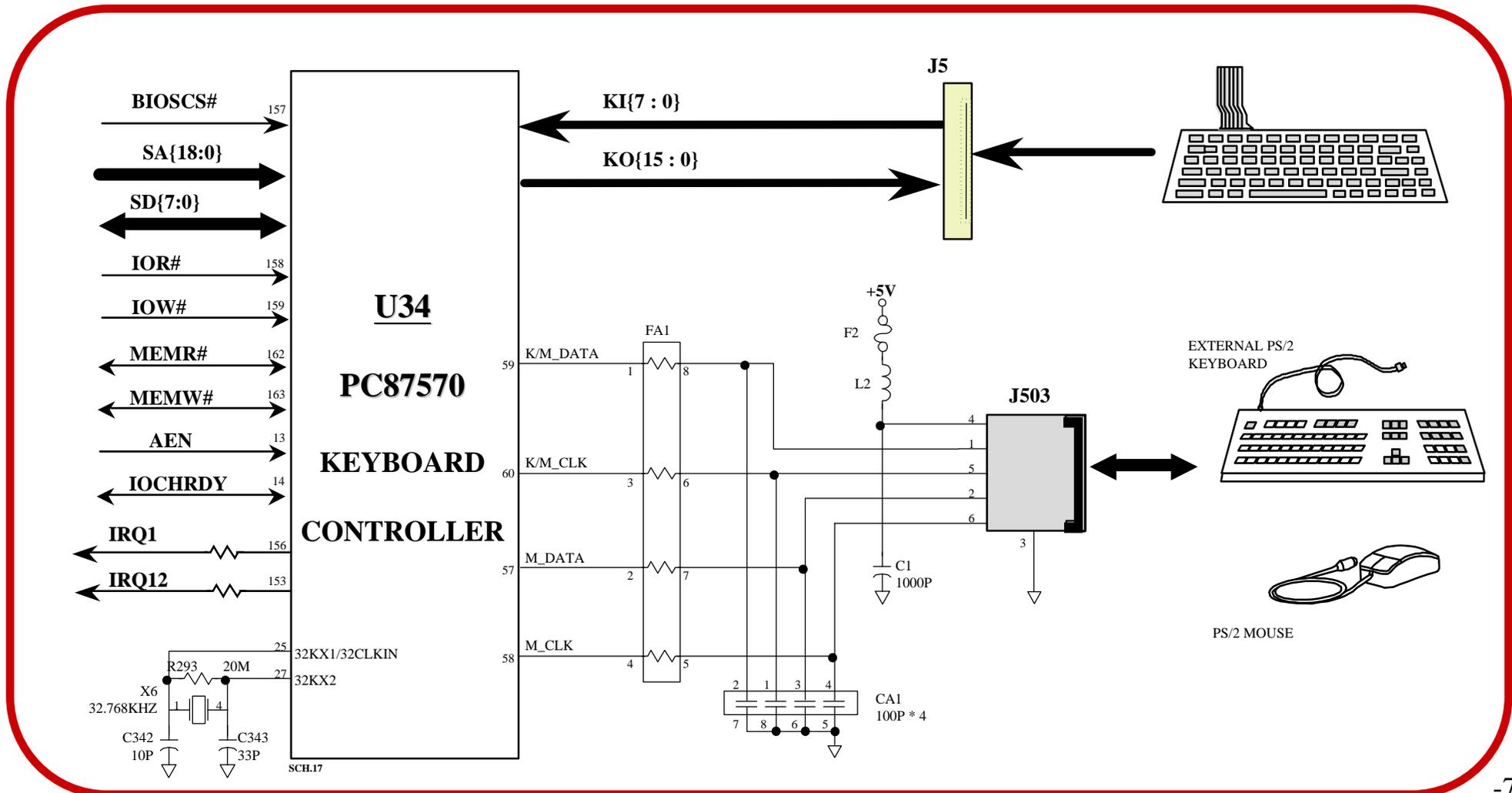


# 6120N N/B MAINTENANCE

## 8.7 KEYBOARD TEST ERROR (INCLUDING EXTERNAL KEYBOARD & PS/2 MOUSE)

Symptom:

1. Error message of keyboard failure is shown or any key doesn't work.
2. PIO debug board shows the port **378H** error code is stopped at **20H,21H,30H or 31H**.

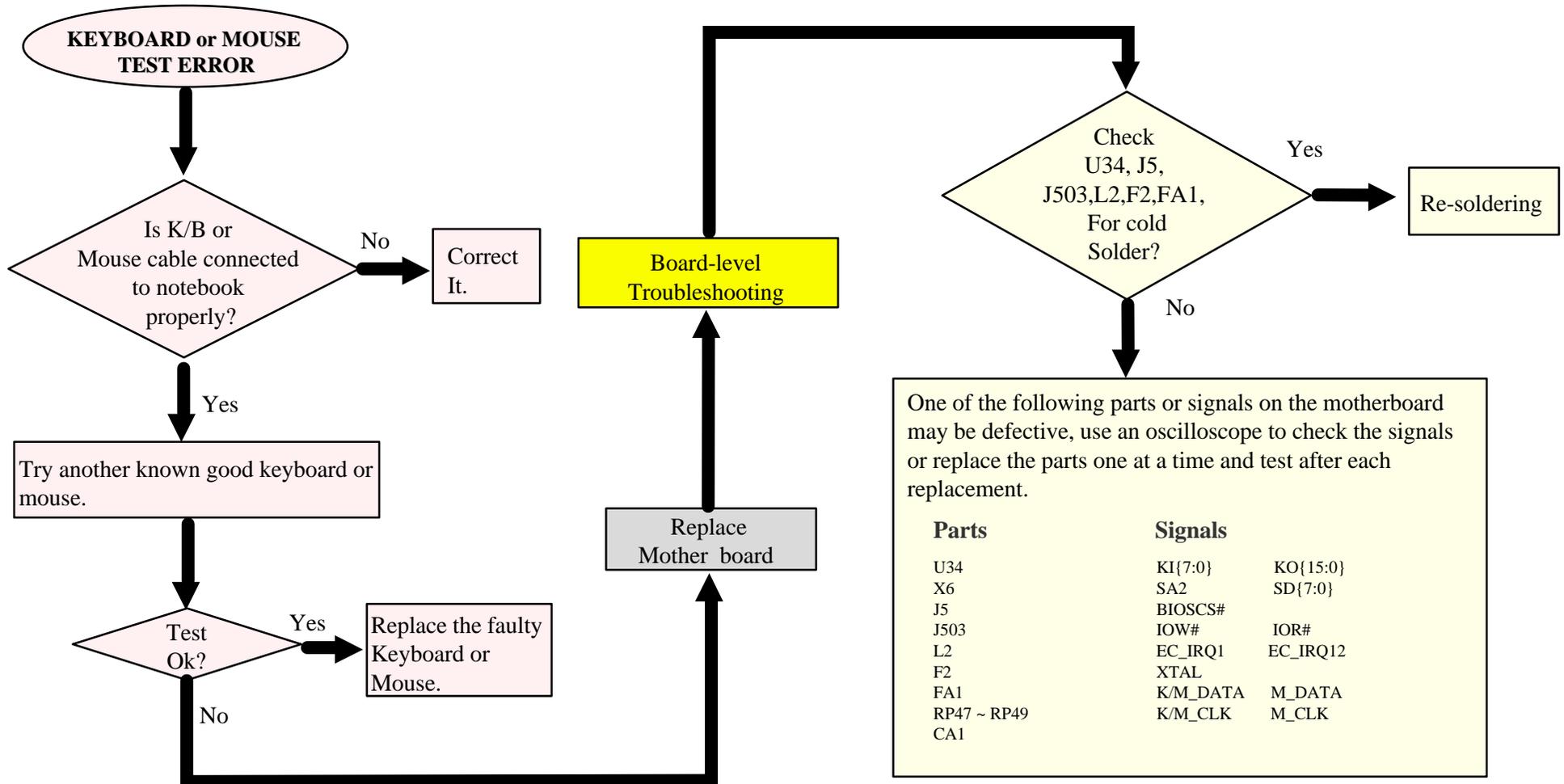


# 6120N N/B MAINTENANCE

## 8.7 KEYBOARD TEST ERROR (INCLUDING EXTERNAL KEYBOARD & PS/2 MOUSE)

Symptom:

1. Error message of keyboard failure is shown or any key doesn't work.
2. PIO debug board shows the port 378H error code is stopped at 20H or 21H, 30H or 31H.

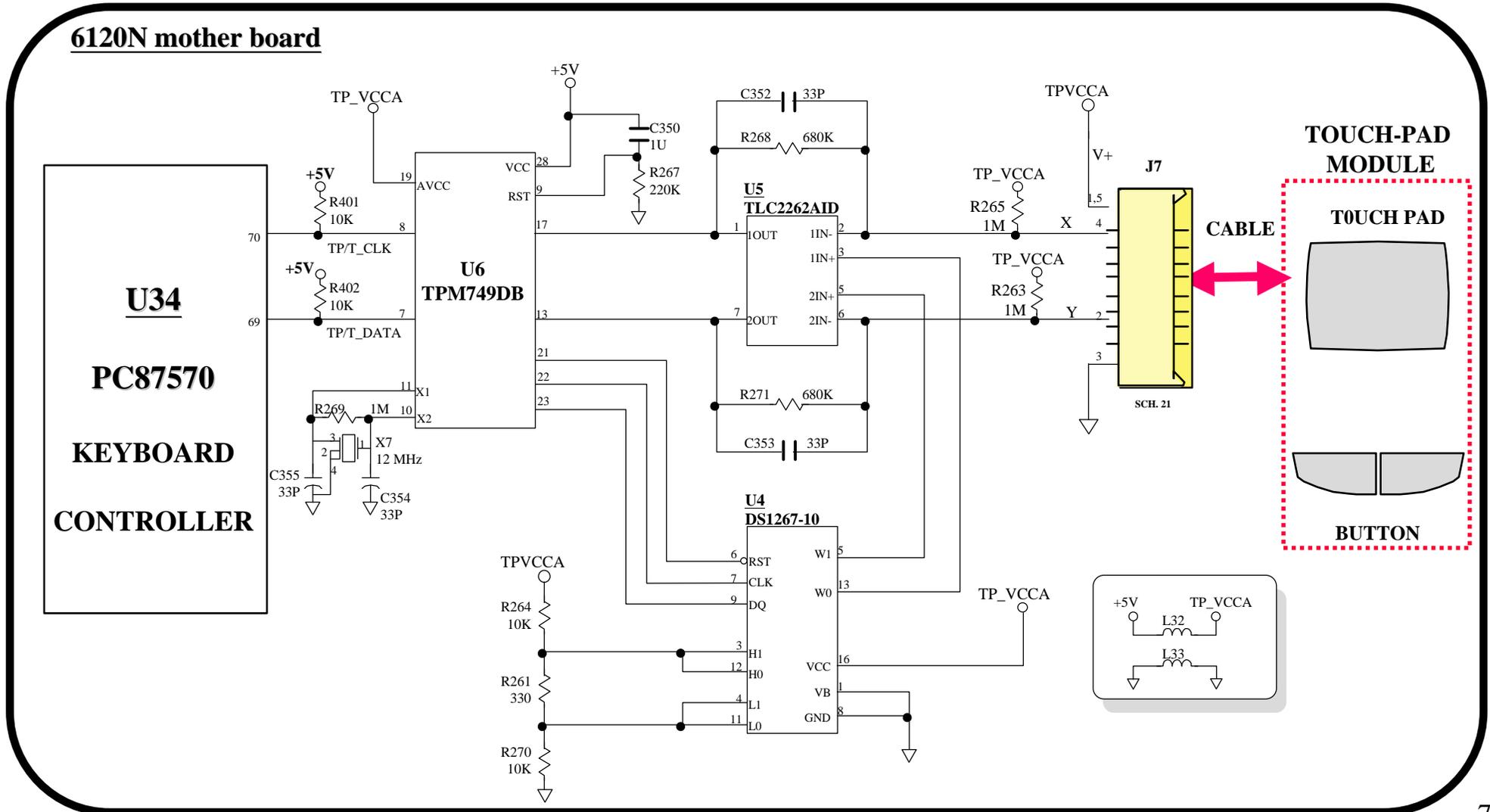


# 6120N N/B MAINTENANCE

## 8.8 TOUCH-PAD TEST ERROR (1)

**Symptom:**

An error message is shown when the touch-pad is enabled.

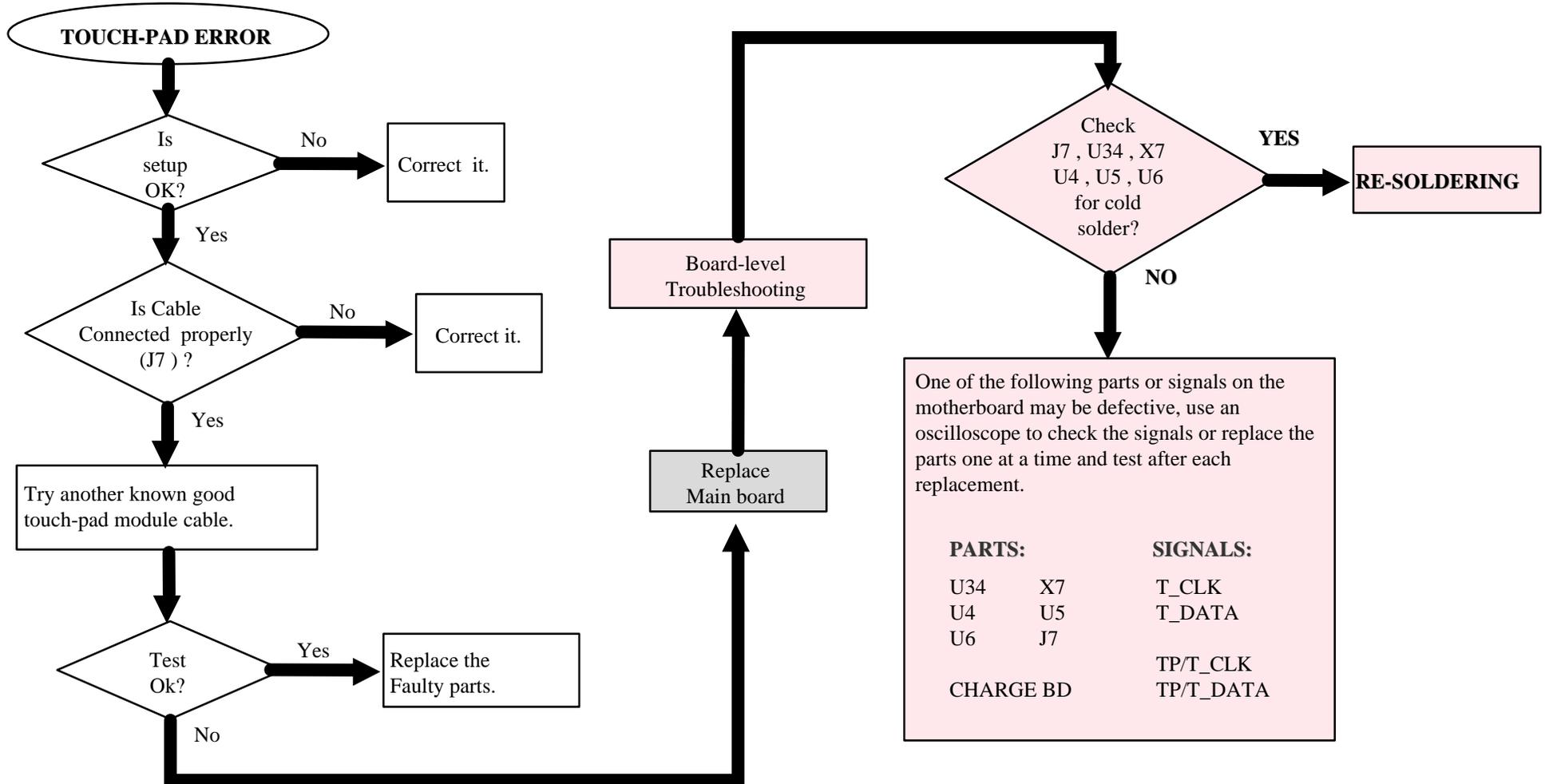


# 6120N N/B MAINTENANCE

## 8.8 TOUCH-PAD TEST ERROR (1)

### Symptom:

An error message is shown when the touch-pad is enabled.

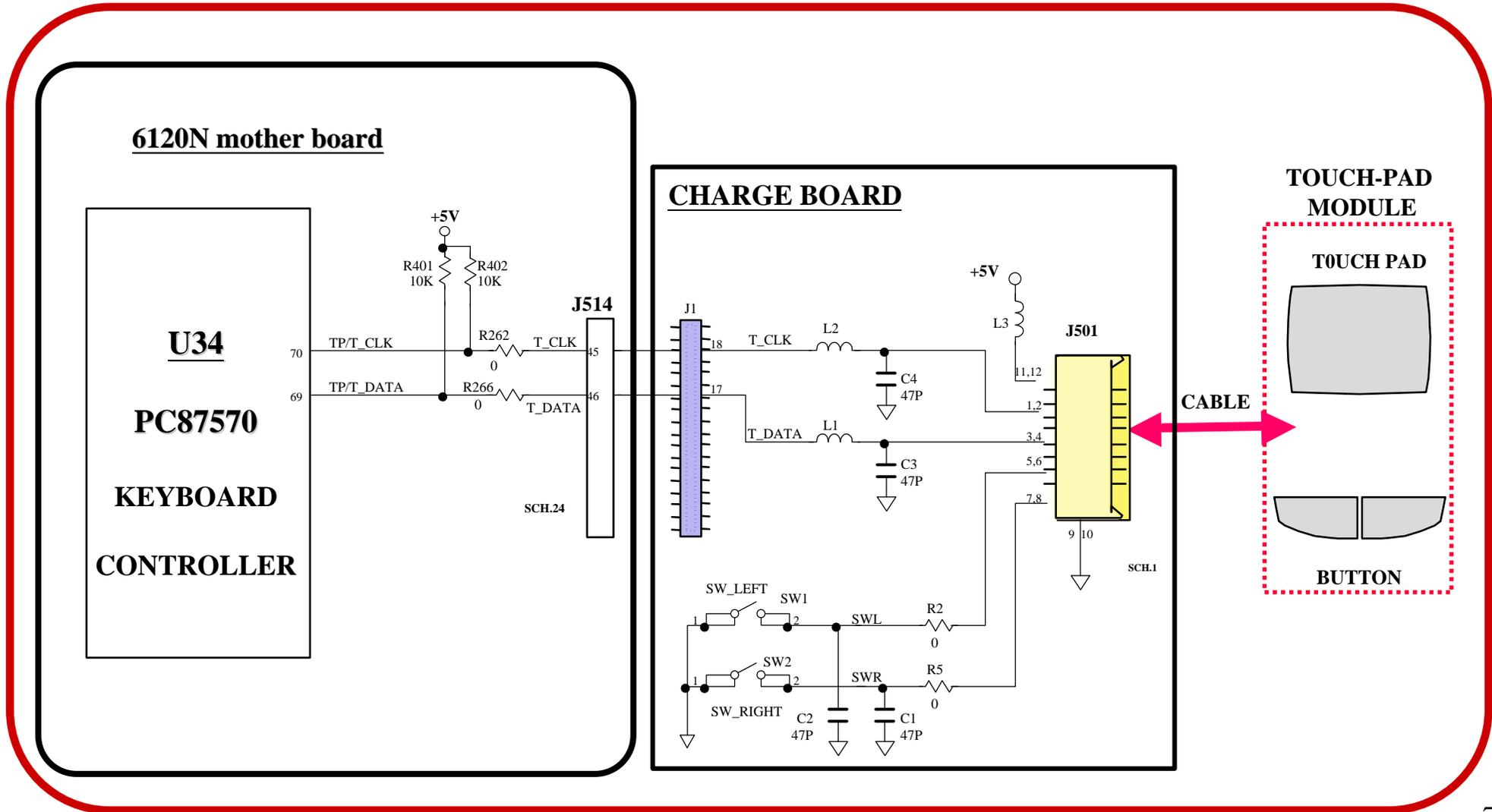


# 6120N N/B MAINTENANCE

## 8.8 TOUCH-PAD TEST ERROR (2)

**Symptom:**

An error message is shown when the touch-pad is enabled.

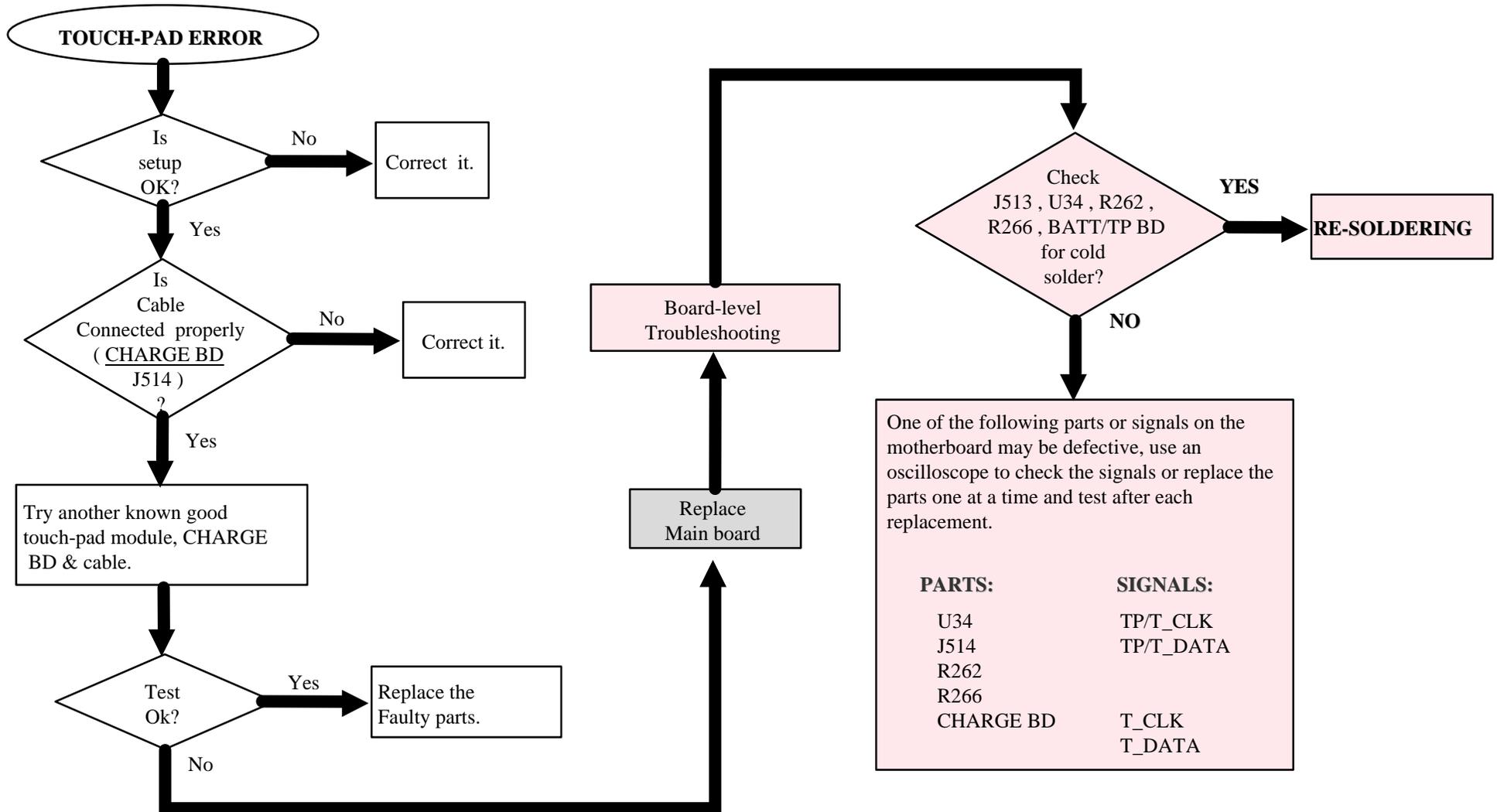


# 6120N N/B MAINTENANCE

## 8.8 TOUCH-PAD TEST ERROR (2)

### Symptom:

An error message is shown when the touch-pad is enabled.

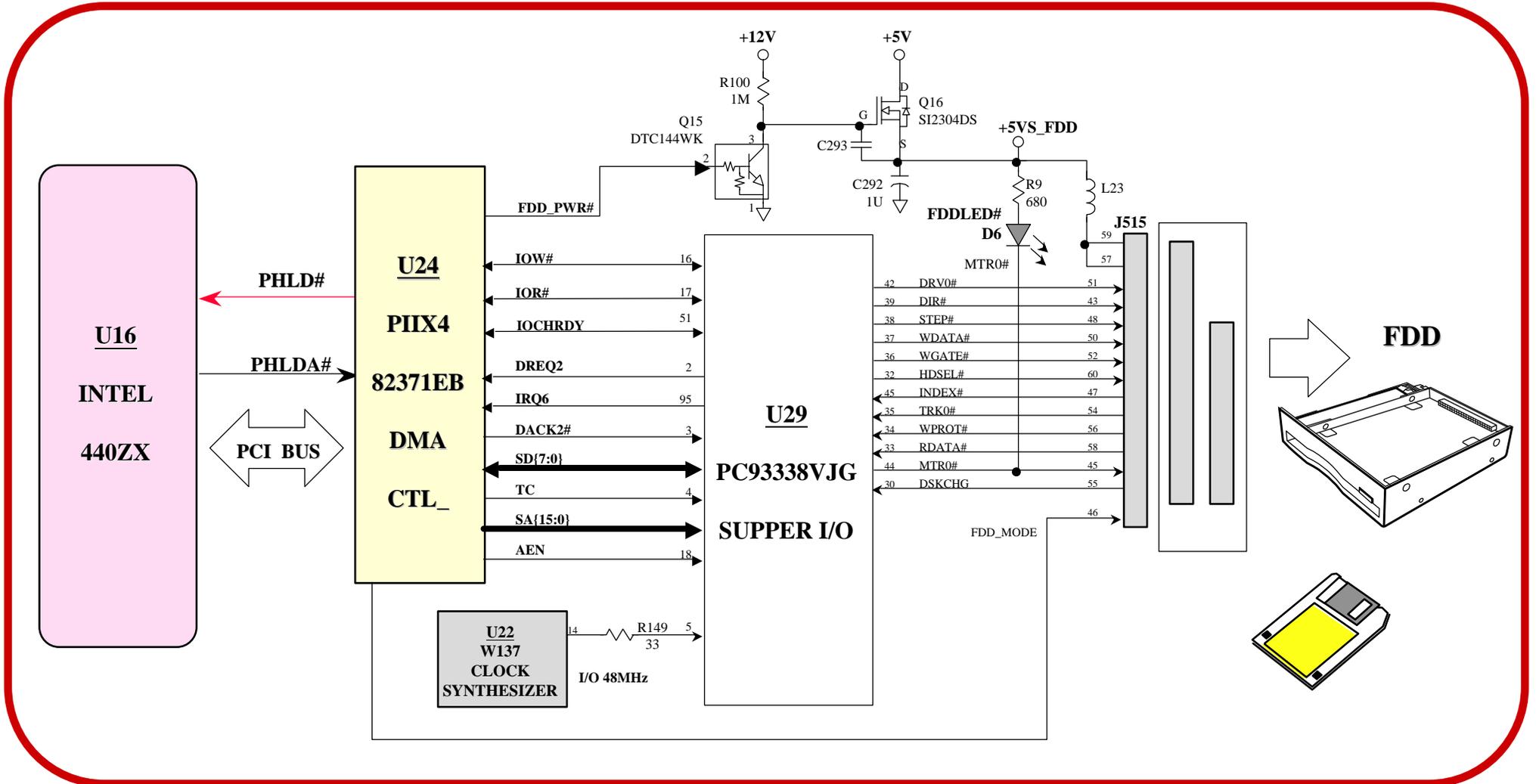


# 6120N N/B MAINTENANCE

## 8.9 DISKETTE DRIVE TEST ERROR

Symptom:

An error message is shown while loading data from disk to system.

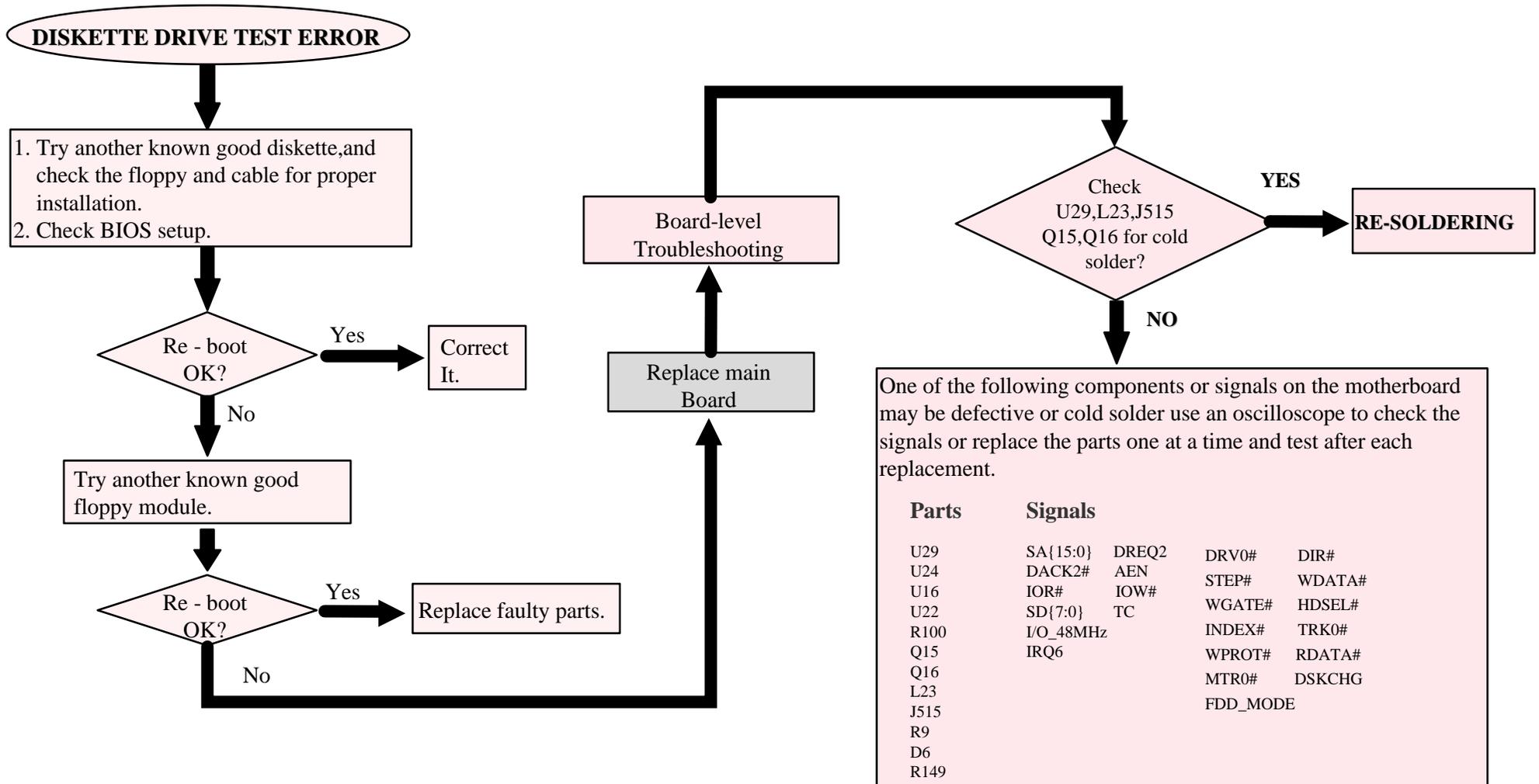


# 6120N N/B MAINTENANCE

## 8.9 DISKETTE DRIVE TEST ERROR

### Symptom:

An error message is shown while loading data from disk to system.



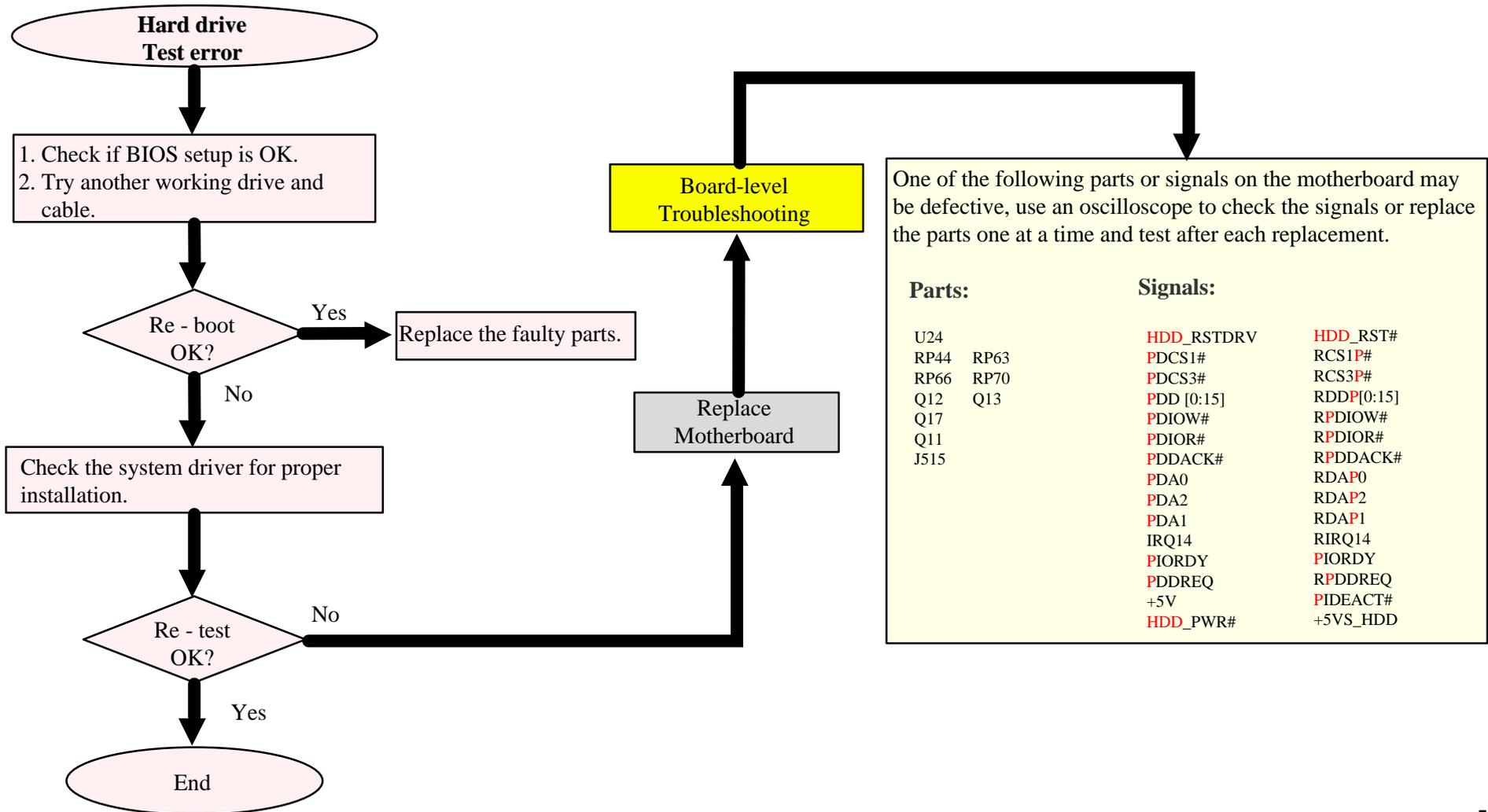


# 6120N N/B MAINTENANCE

## 8.10 HARD DRIVE TEST ERROR

### Symptom:

Either an error message is shown, or the drive motor spins non-stop, while reading data from or writing data to hard-disk.

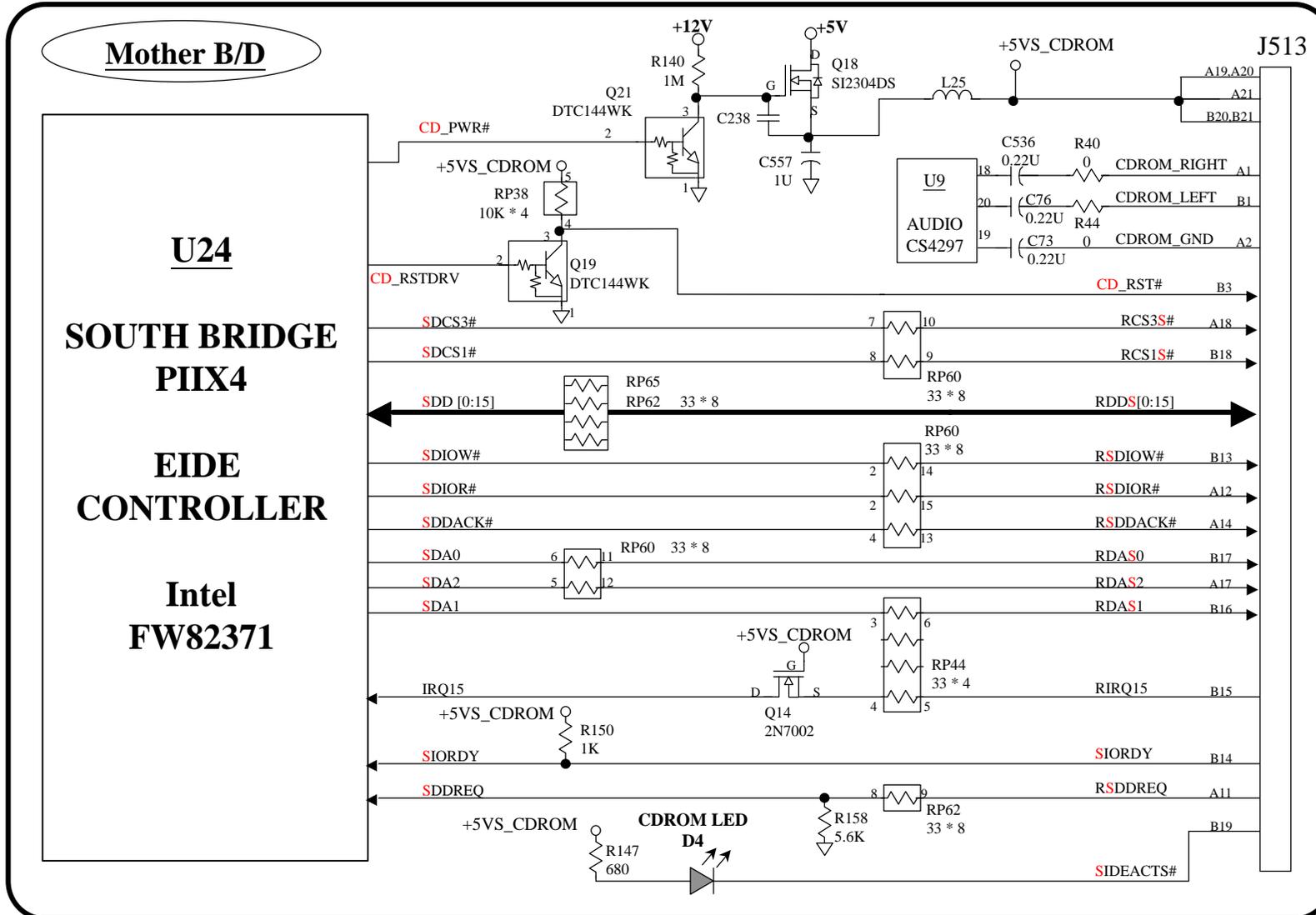


# 6120N N/B MAINTENANCE

## 8.11 CD-ROM TEST ERROR

Symptom:

An error message is shown when reading data from CD-ROM drive.

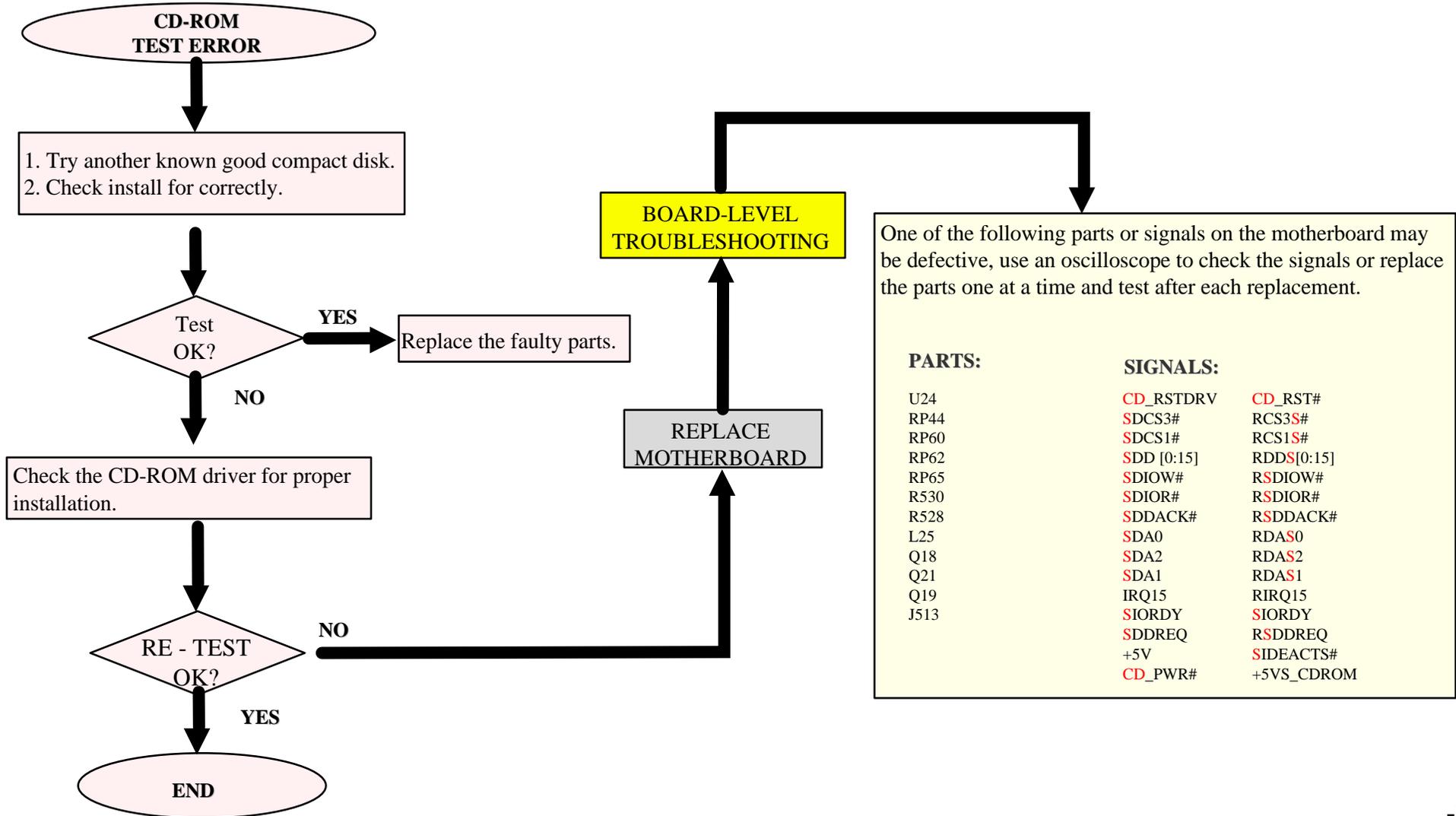


# 6120N N/B MAINTENANCE

## 8.11 CD-ROM TEST ERROR

### Symptom:

An error message is shown when reading data from CD-ROM drive.



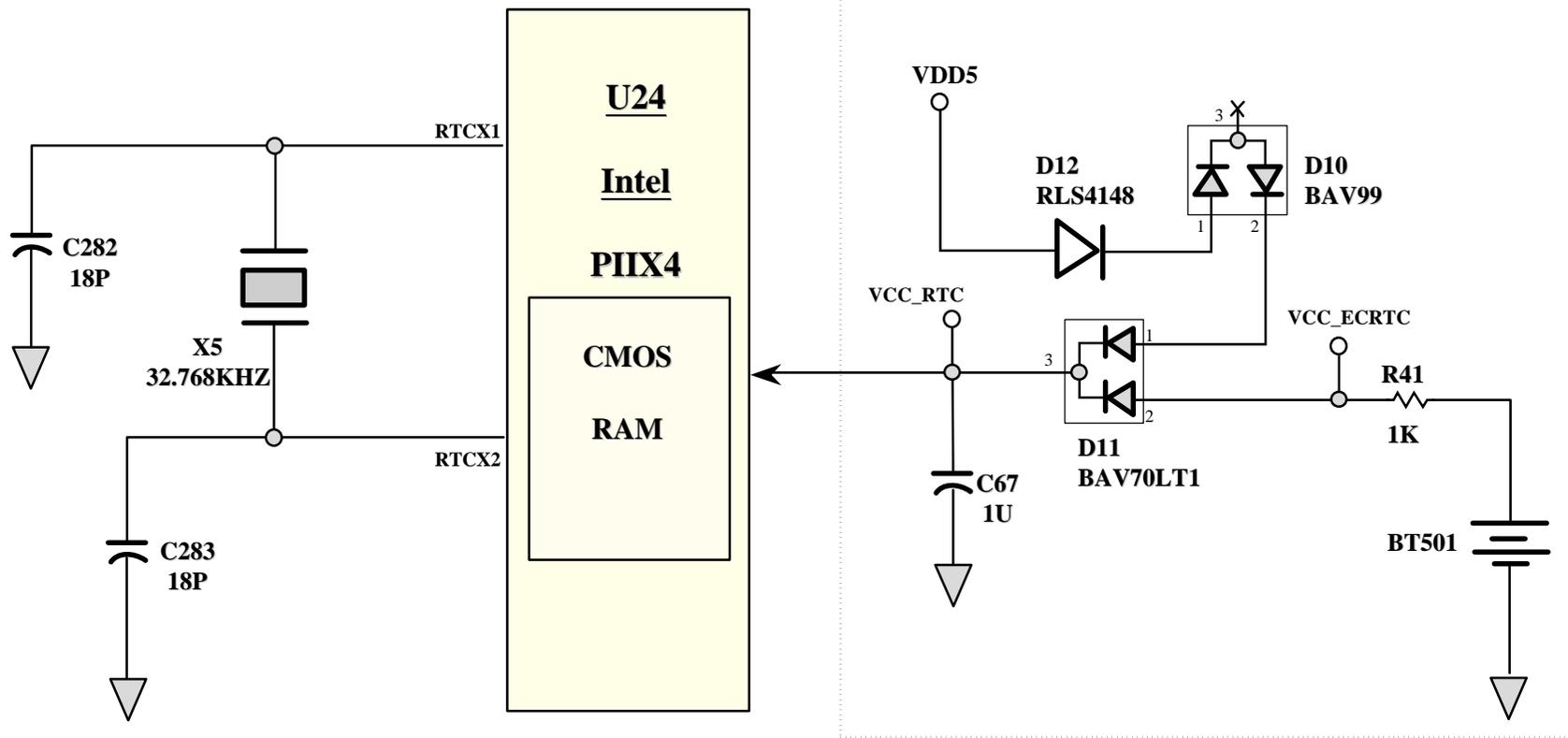
# 6120N N/B MAINTENANCE

## 8.12 CMOS TEST ERROR

Symptom:

1. Error code is stopped at 22H.
2. CMOS data lost, or inaccurate system time & date.

\*\*\*To clear CMOS data, remove battery pack and disconnect AC adapter first, then remove CMOS battery compartment cover on the bottom side of notebook and take off the CMOS back-up battery from it's socket for at least 10 minutes.\*\*\*

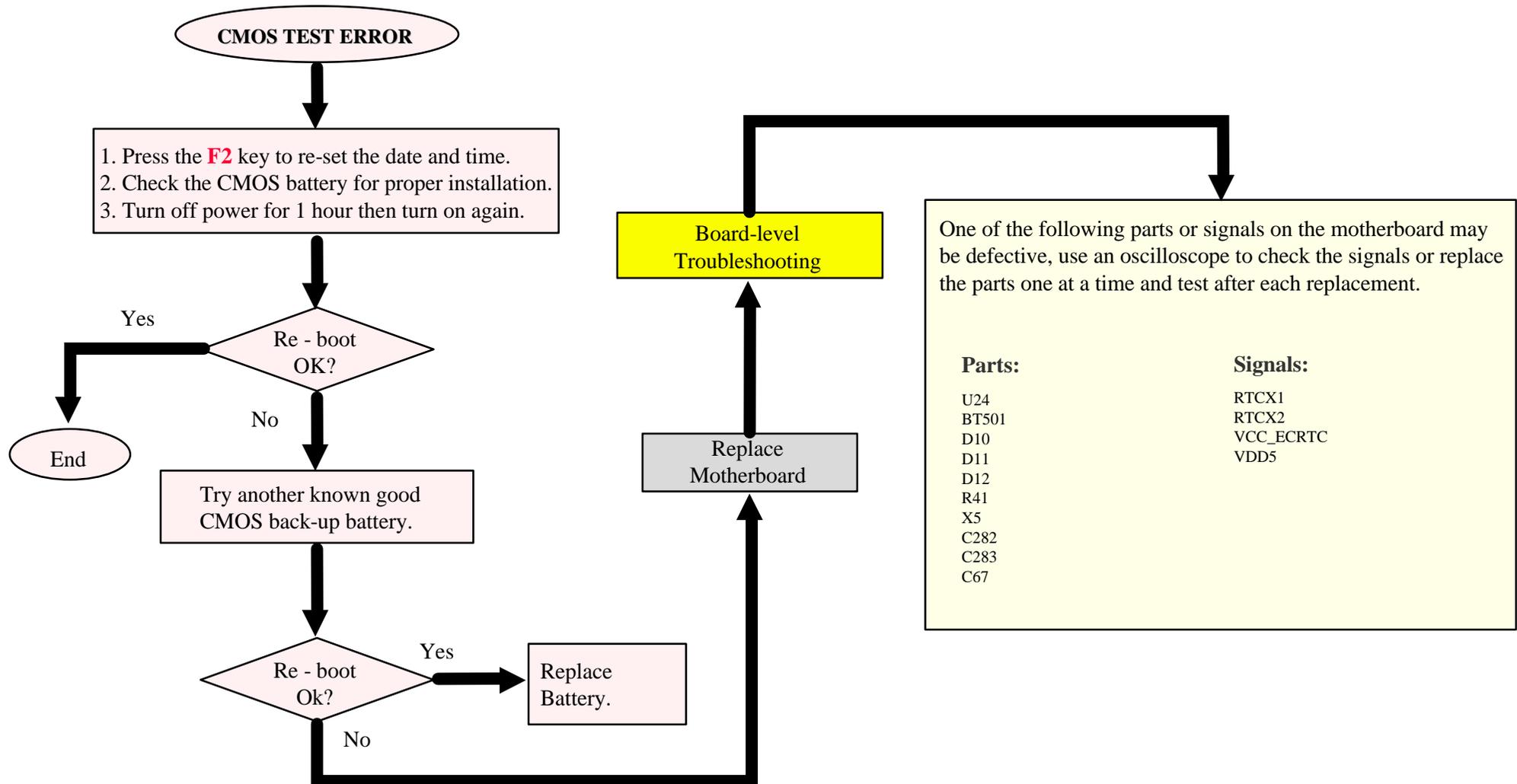


# 6120N N/B MAINTENANCE

## 8.12 CMOS TEST ERROR

Symptom:

1. Error code is stopped at **22H**.
2. CMOS data lost, or inaccurate system time & date.

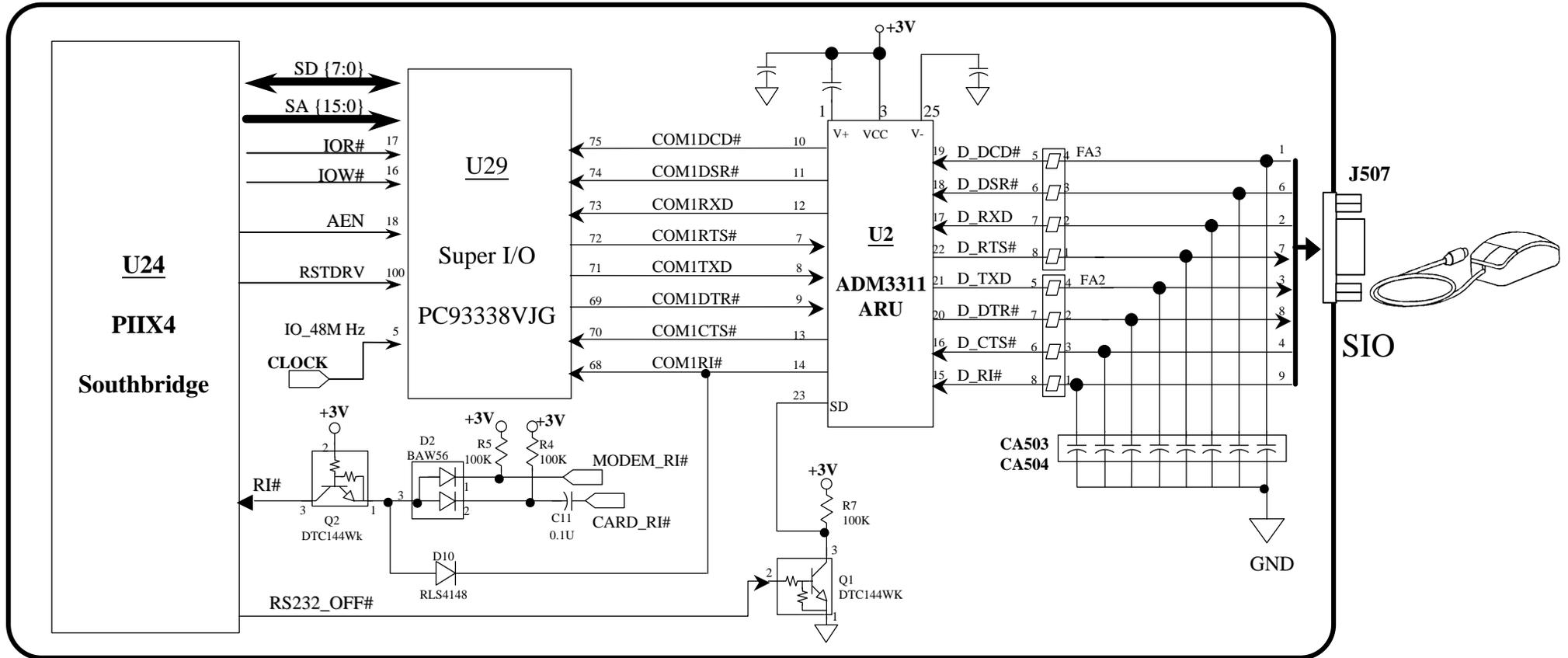


# 6120N N/B MAINTENANCE

## 8.13 SIO PORT TEST ERROR

**Symptom :**

**An error message occurs when a mouse or other I/O device is installed.**



PIN DEFINITION OF SIO PORT:

PIN 1 :	DCD-----	Data Carrier Detect	I	PIN 6 :	DSR-----	Data Set Ready	I
PIN 2 :	RD-----	Receive Data	I	PIN 7 :	RTS-----	Request To Send	O
PIN 3 :	TD-----	Transmit Data	O	PIN 8 :	CTS-----	Clear To Send	I
PIN 4 :	DTR-----	Data Terminal Ready	O	PIN 9 :	RI-----	Ring Indicator	I
PIN 5 :	SG-----	Signal Ground	GND				

LOOPBACK CONNECTOR FOR SIO TEST:

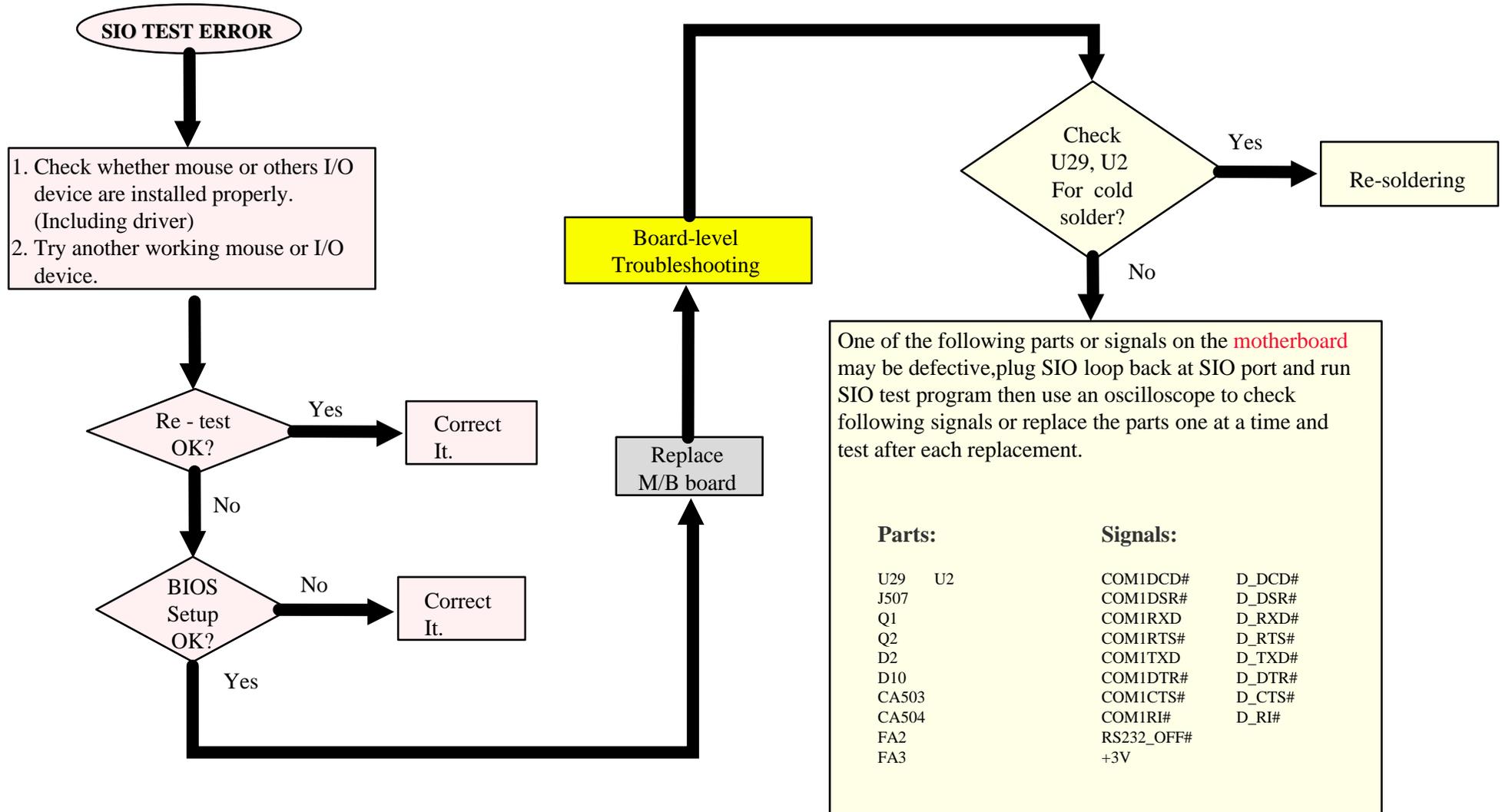
PIN	1, 4, 6	Short
PIN	2, 3	Short
PIN	7, 8, 9	Short

# 6120N N/B MAINTENANCE

## 8.13 SIO PORT TEST ERROR

### Symptom :

An error message occurs when a mouse or other I/O device is installed.

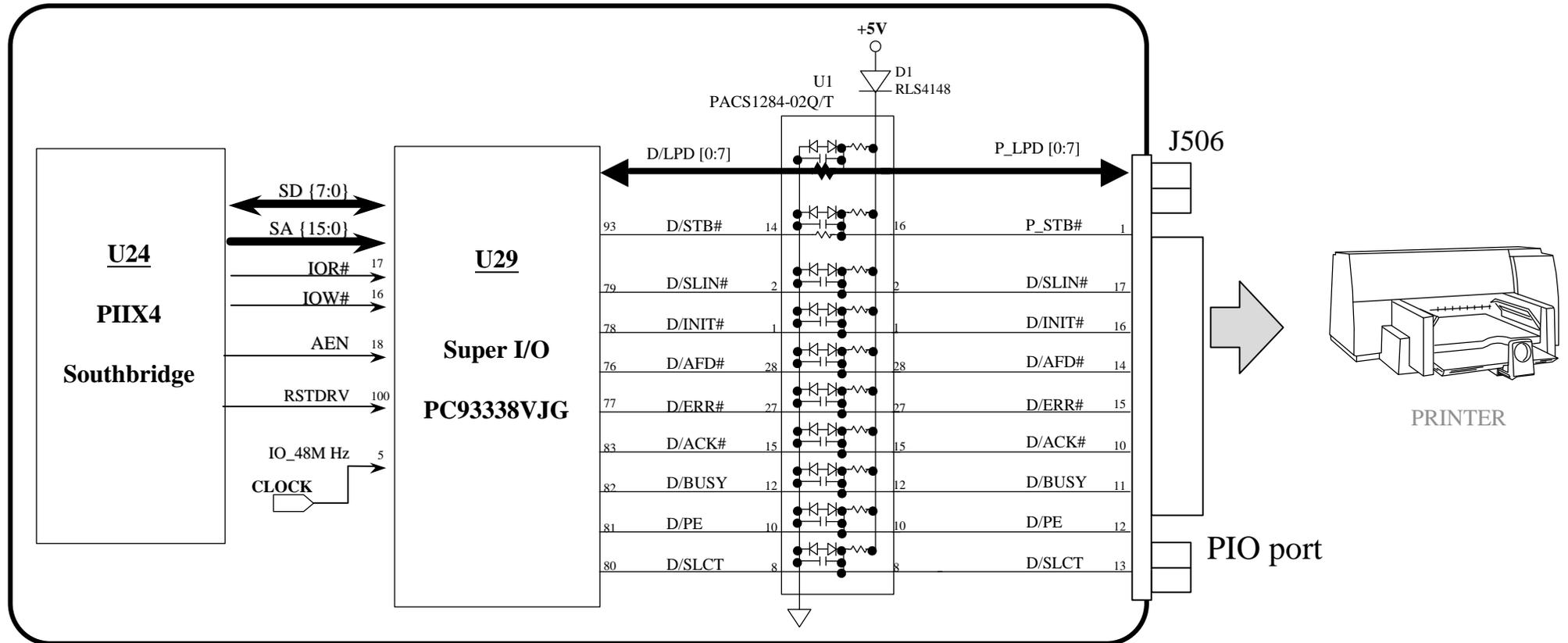


# 6120N N/B MAINTENANCE

## 8.14 PIO PORT TEST ERROR

**Symptom:**

**When a print command is issued, printer prints nothing or garbage.**



PIN DEFINITION OF PIO PORT

PIN 1	STB	STROBE SIGNAL	PIN 14	AFD	AUTO LINE FEED
PIN 2-9	D0 - D7	PARALLEL PORT DATA BUS D0 TO D7	PIN 15	ERR	ERROR AT PRINTER
PIN 10	ACK	ACKNOWLEDGE HANDSHANK	PIN 16	INIT	INITIATE OUTPUT
PIN 11	BUSY	BUSY SIGNAL	PIN 17	SLIN	PRINTER SELECT
PIN 12	PE	PAPER END	PIN 18-25: SIGNAL GROUND		
PIN 13	SLCT	PRINTER SELECTED			

LOOPBACK CONNECTOR FOR PIO TEST:

PIN 1, 13	SHORT	PIN 10,16	SHORT
PIN 2, 15	SHORT	PIN 11,17	SHORT
PIN 12, 14	SHORT		

LOOPBACK CONNECTOR FOR EPP TEST:

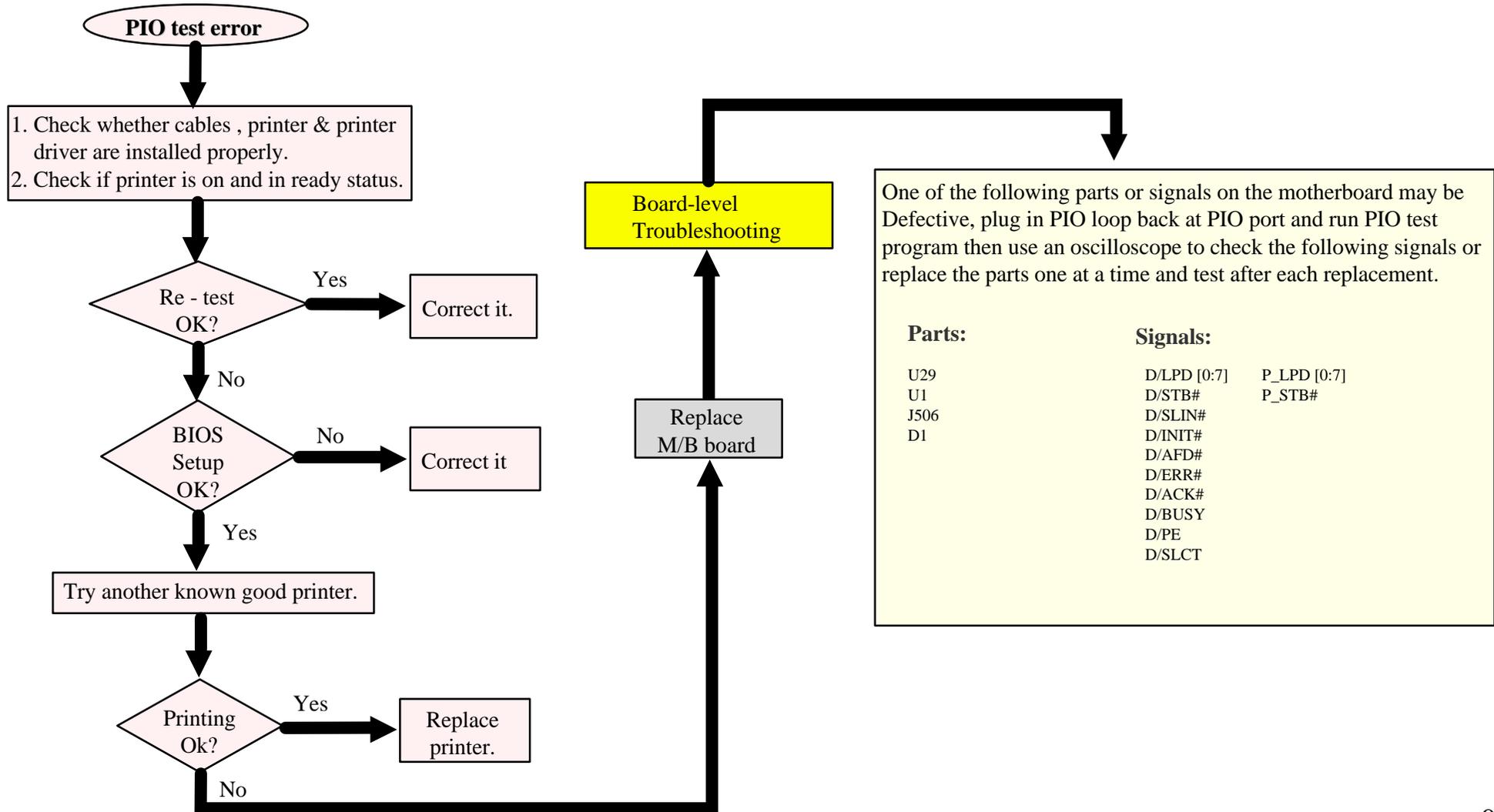
PIN 1, 2, 4, 6, 8	SHORT
PIN 3, 5, 7, 9, 16	SHORT
PIN 18, 19, 20, 21, 22, 23, 24, 25	SHORT

# 6120N N/B MAINTENANCE

## 8.14 PIO PORT TEST ERROR

### Symptom:

When a print command is issued, printer prints nothing or garbage.

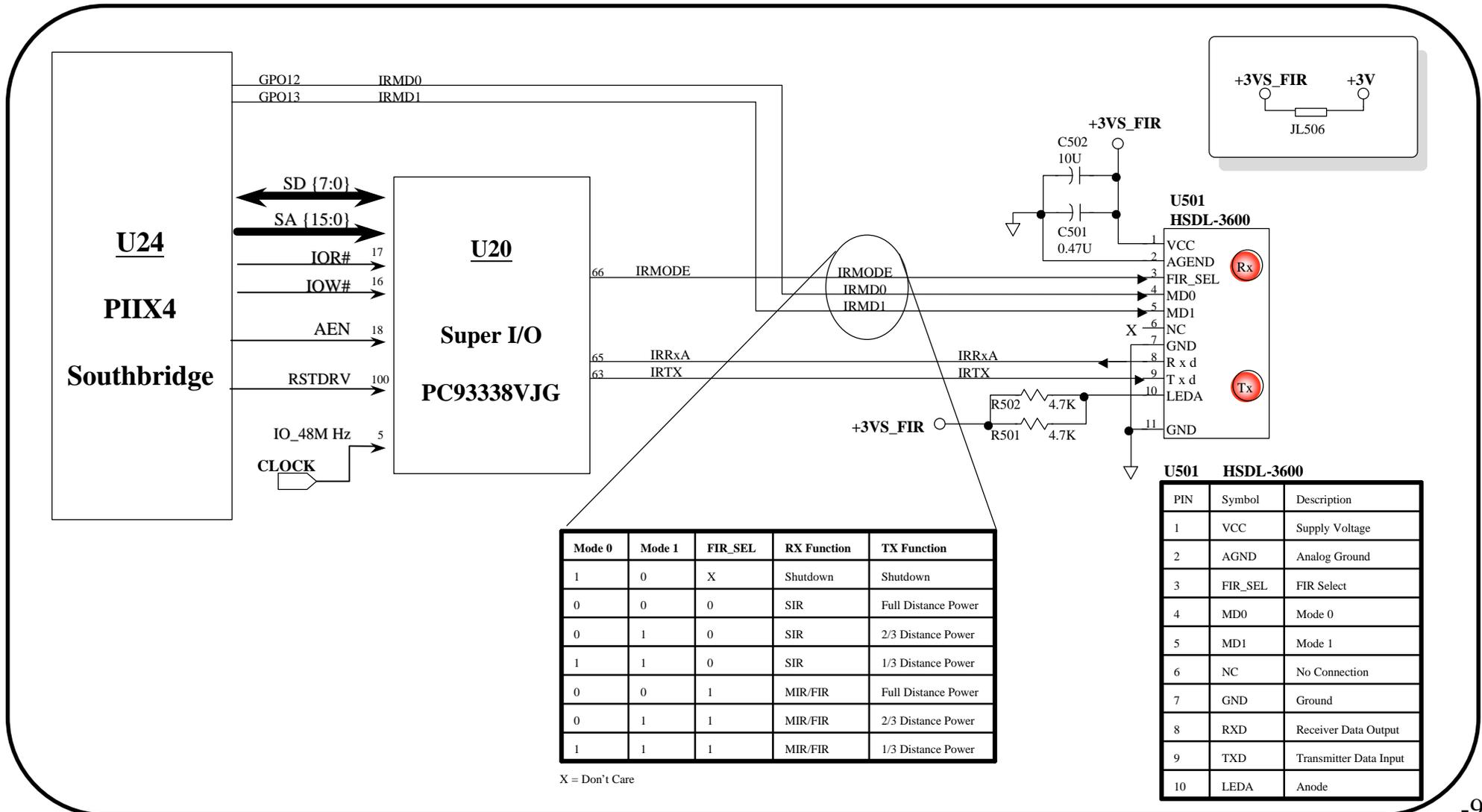


# 6120N N/B MAINTENANCE

## 8.15 IrDA TEST ERROR

Symptom:

The infrared function failure (ex. : can't detect Ir. device or transfer data from Ir.)

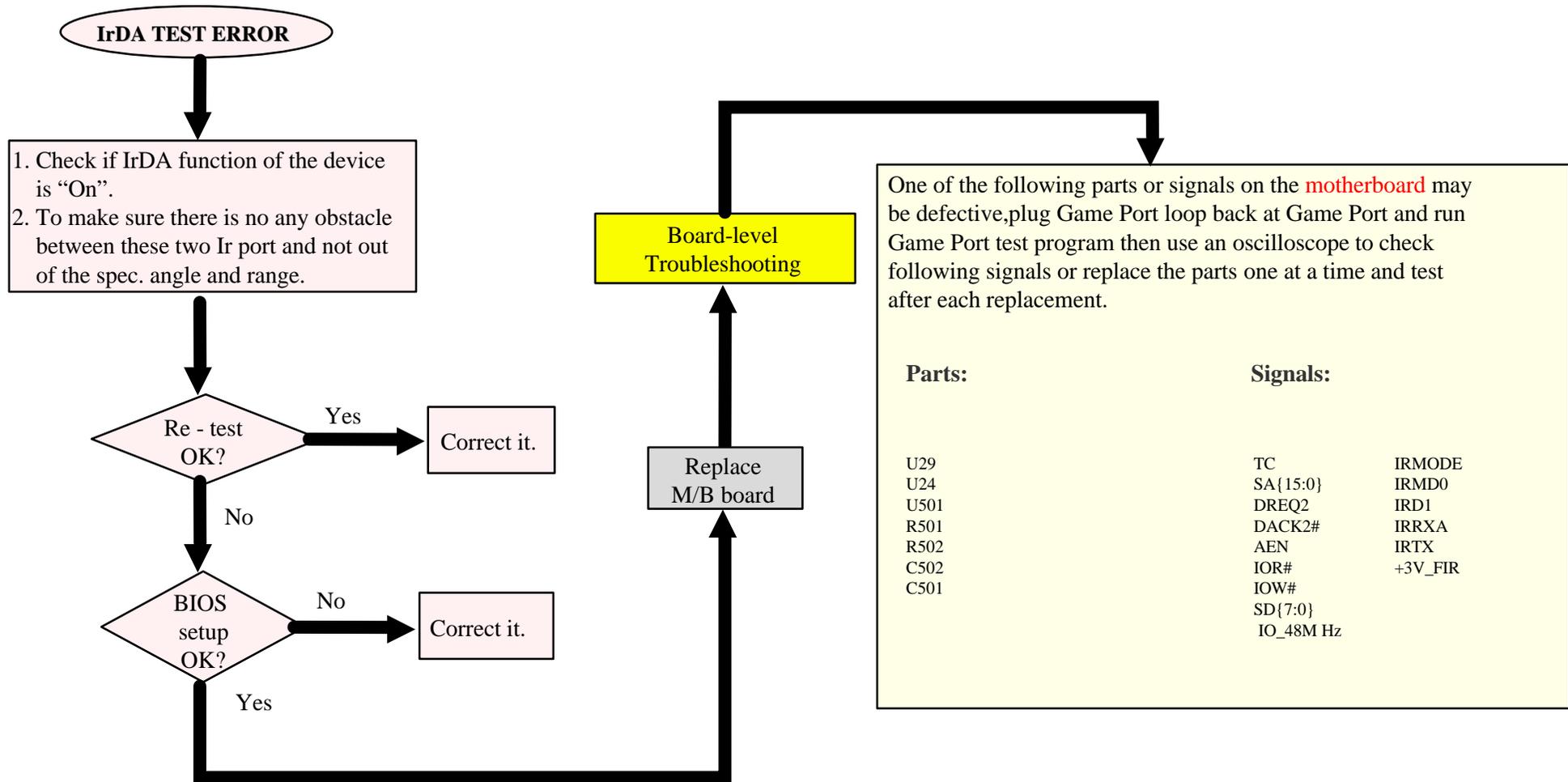


# 6120N N/B MAINTENANCE

## 8.15 IrDA TEST ERROR

### Symptom:

The infrared function failure (ex. : can't detect Ir. device or transfer data from Ir.)

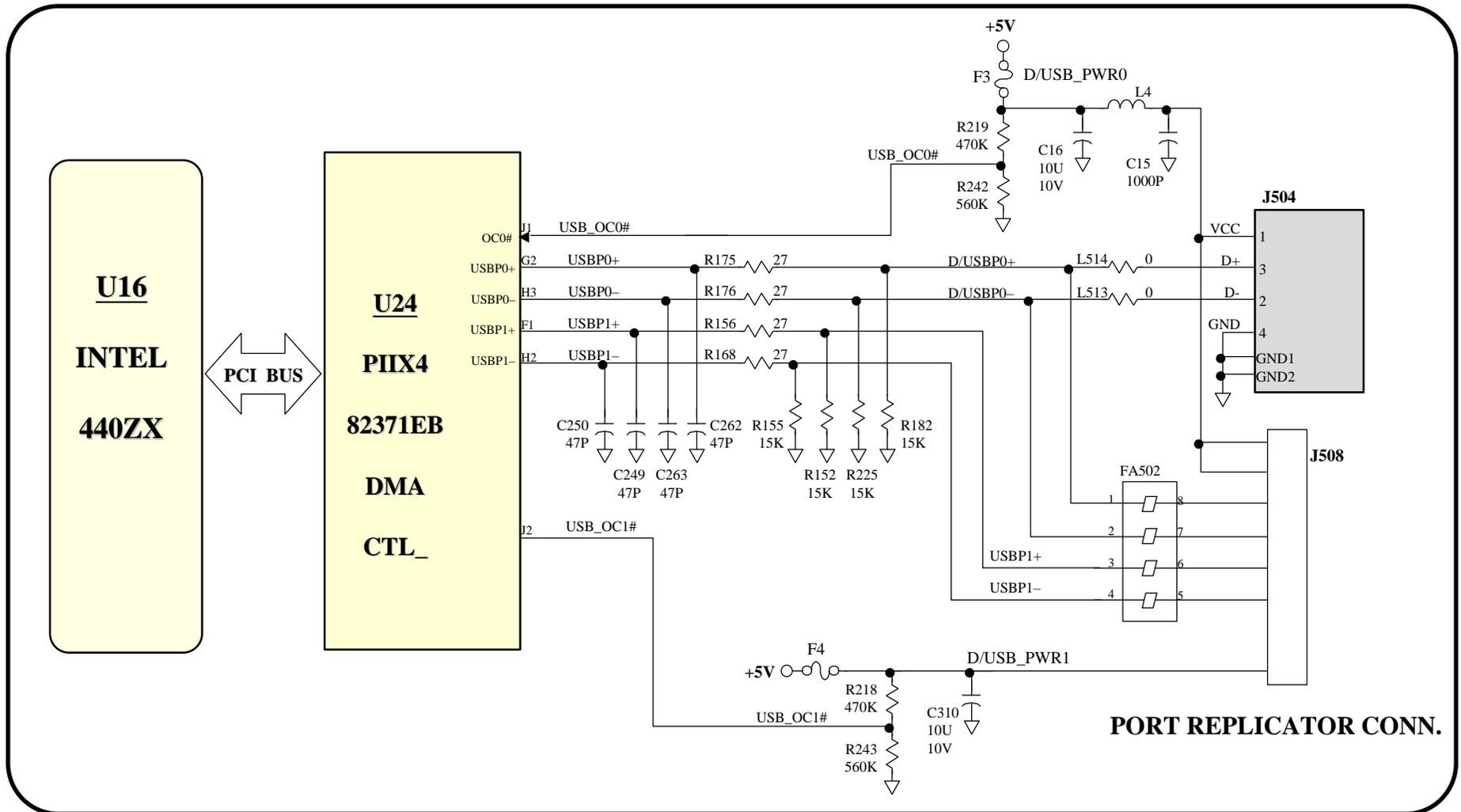


# 6120N N/B MAINTENANCE

## 8.16 USB PORT TEST ERROR

Symptom:

An error occurs when a USB I/O device is installed.

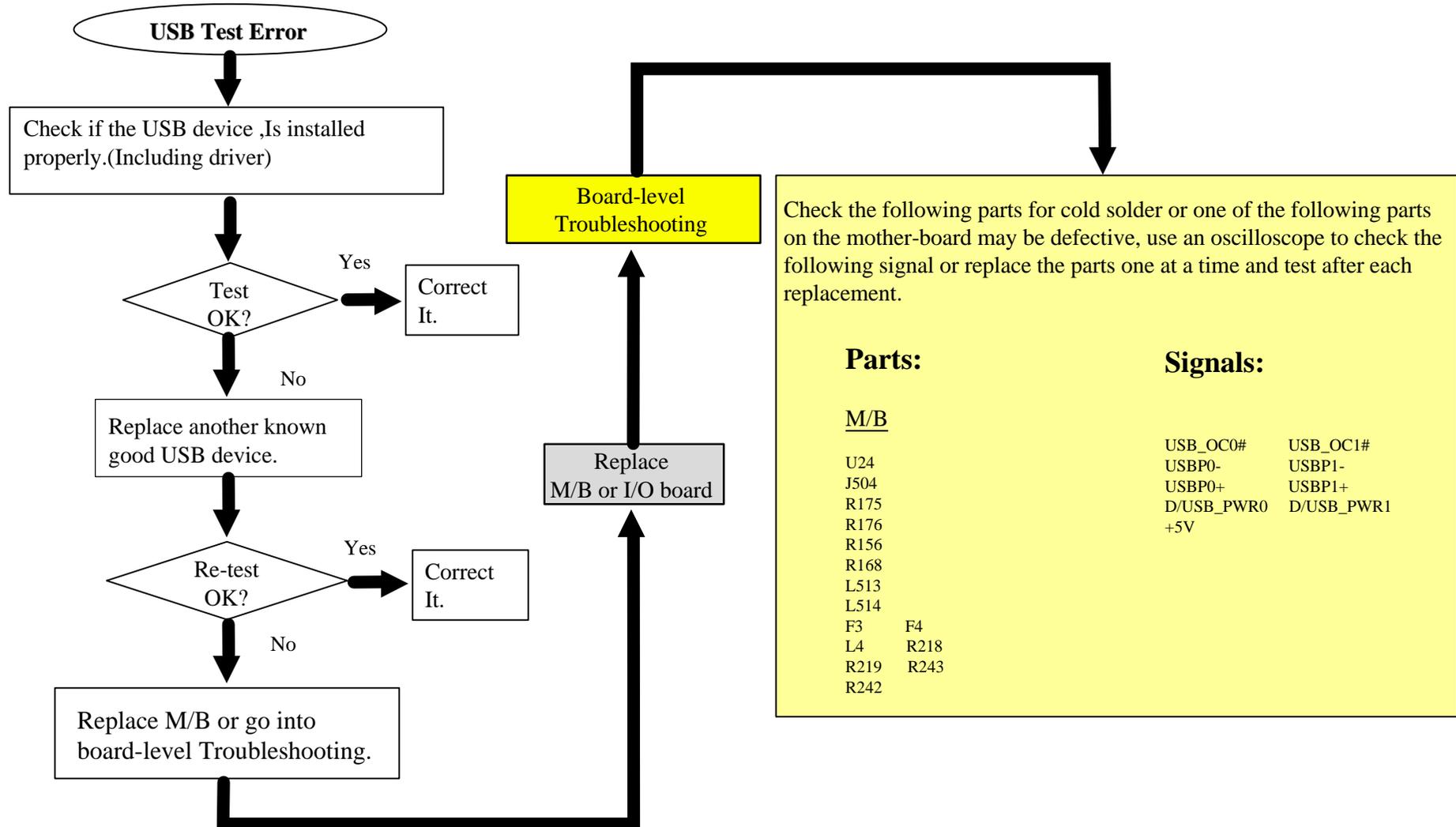


# 6120N N/B MAINTENANCE

## 8.16 USB PORT TEST ERROR

### Symptom:

An error occurs when a USB I/O device is installed.

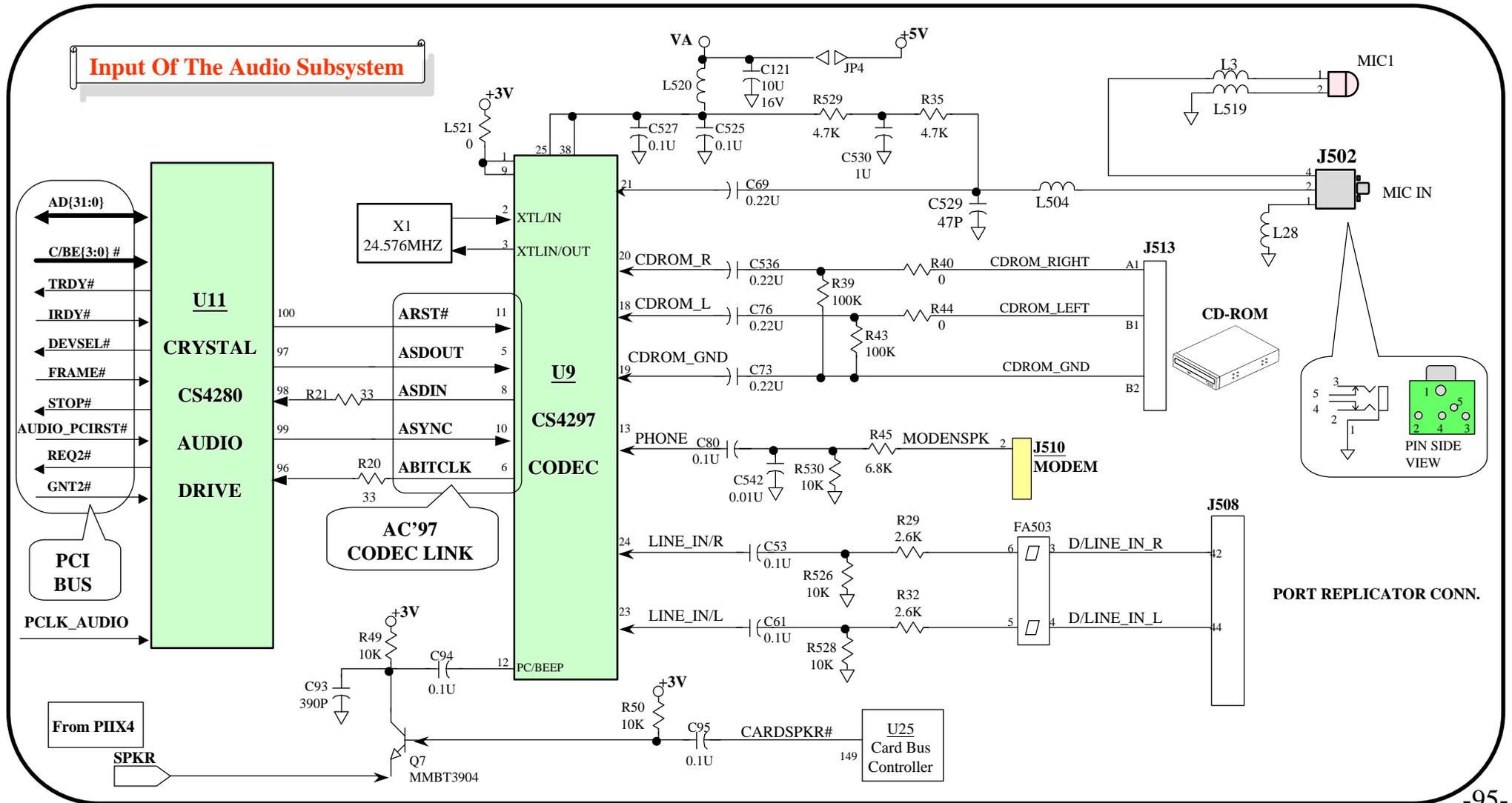


# 6120N N/B MAINTENANCE

## 8.17 AUDIO DRIVE FAILURE

**Symptom:**

**No sound from speaker after audio driver is installed.**

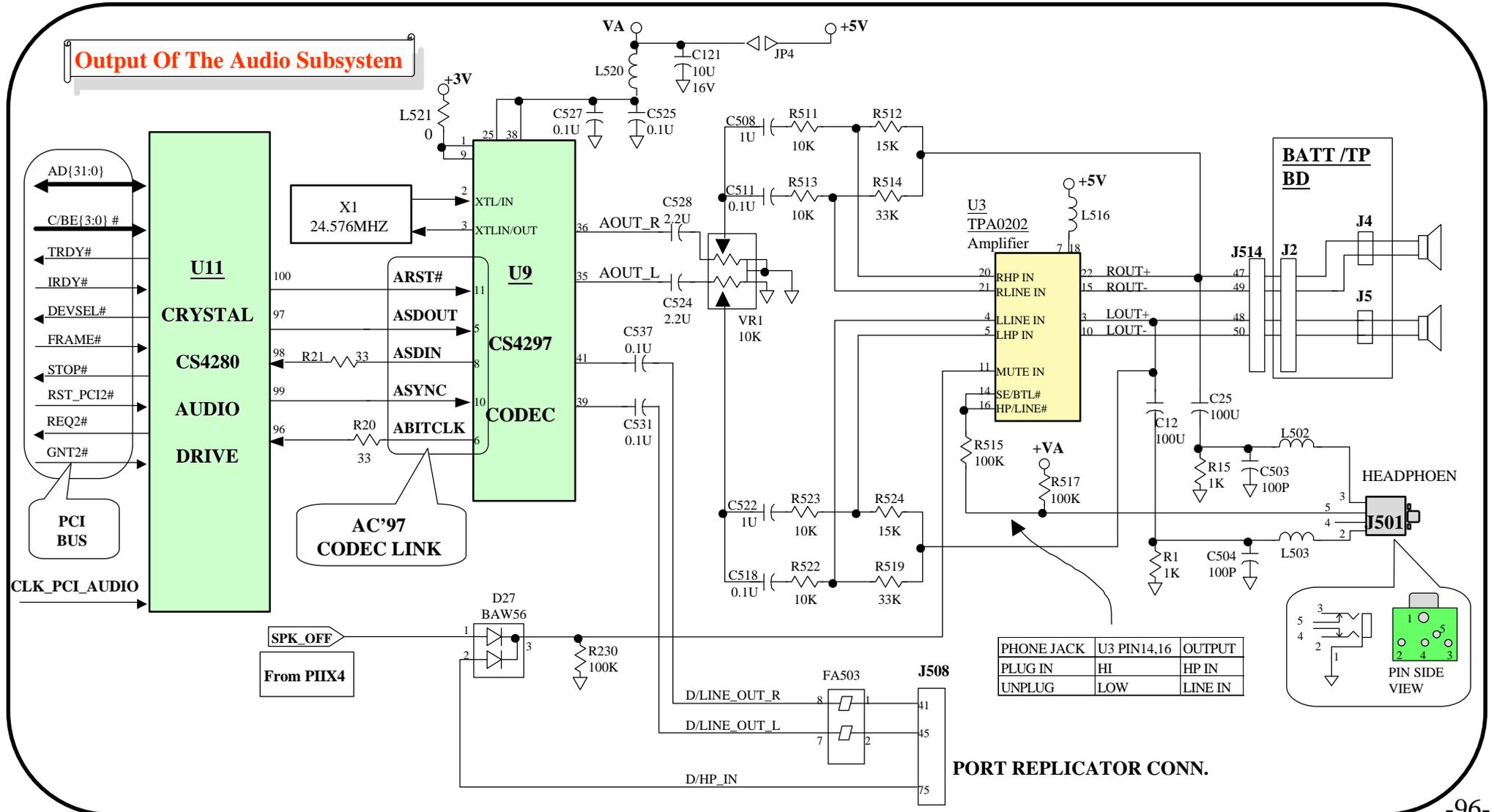


# 6120N N/B MAINTENANCE

## 8.17 AUDIO DRIVE FAILURE

Symptom:

No sound from speaker after audio driver is installed.

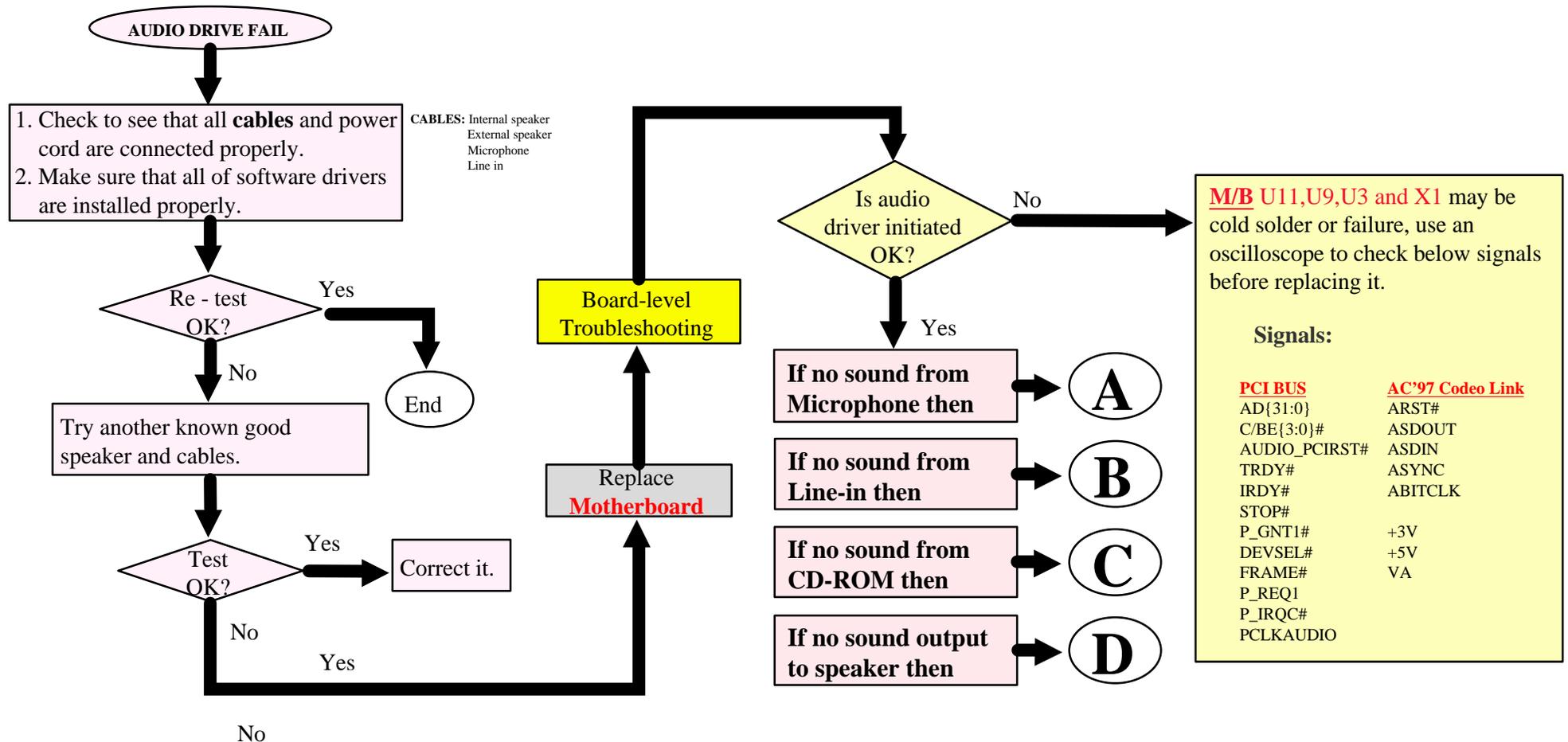


# 6120N N/B MAINTENANCE

## 8.17 AUDIO DRIVE FAILURE

### Symptom:

No sound from speaker after audio driver is installed.

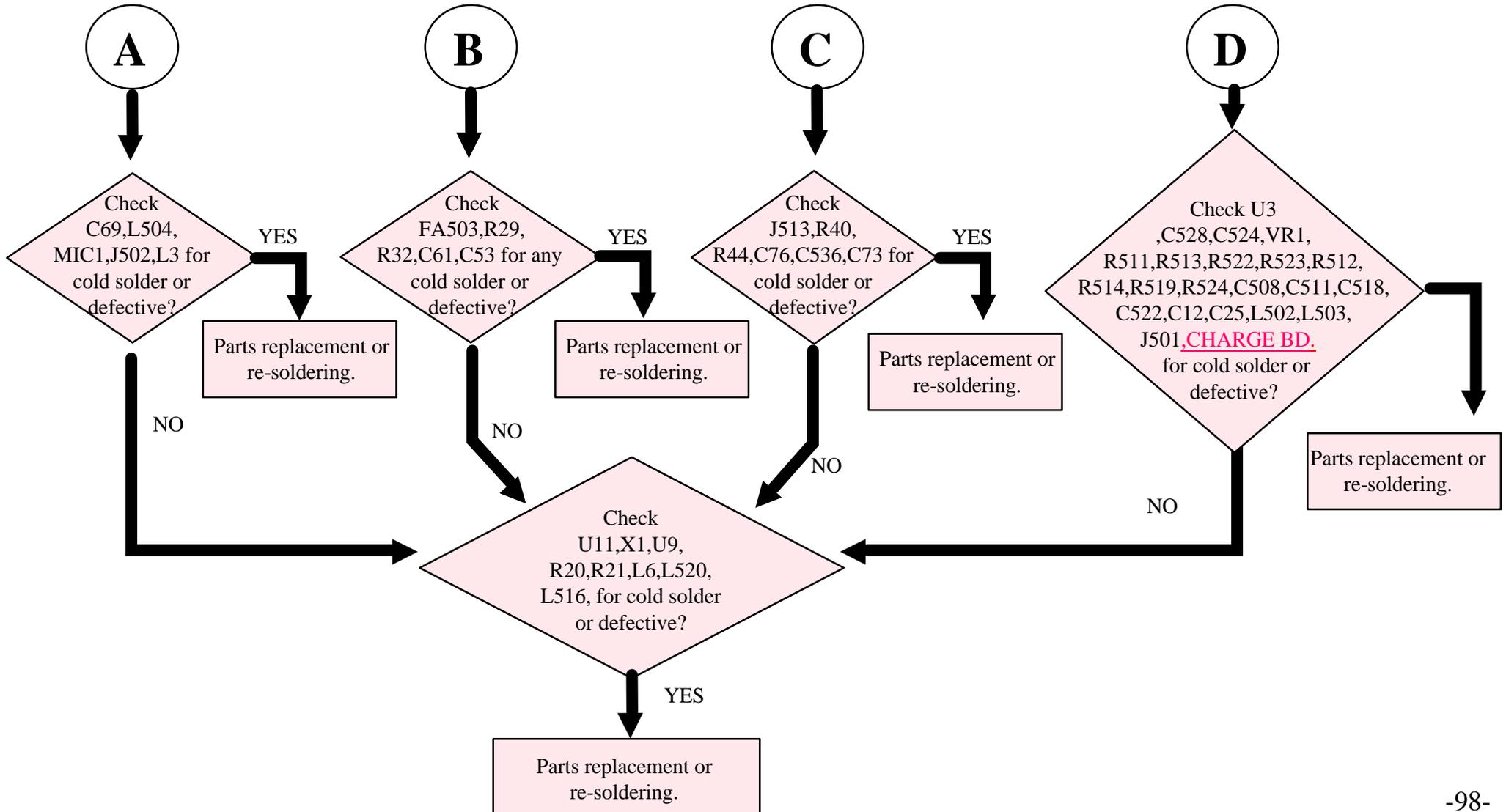


# 6120N N/B MAINTENANCE

## 8.17 AUDIO DRIVE FAILURE

### Symptom:

No sound from speaker after audio driver is installed.



# 6120N N/B MAINTENANCE

## 9. SPARE PARTS LIST(1)

Part Number	Description	Location
442999900006	AC ADPT ASSY OPTION;6120N	
441600002009	AC ADPT ASSY;PWR-60B,CV/CC-19 MS	
541666570003	ACCESSORY KIT;EN,6020-UTILITY ON	
541666570006	ACCESSORY KIT;EU,6020	
541666703004	AK;4-EU,BOX,6020+ CTO	
441999900014	BATT ASSY OPTION;NIMH,4.5/4AH,60	
4416665700012	BATT ASSY;11V/4.5AH,NIMH,SYO,602	
298000000002	BATTERY HOLDER;FOR CR2032,BH-800	BT501
338530010005	BATTERY;LI,3V/220MAH,CR2032	
338712010015	BATTERY;NIMH,1.2V/4.5AH,4/3A,SAN	
340665700011	BEZEL ASSY;TEAC,CDROM,6020	
221666540001	BOX;INNER AK,6120	
342665700045	BRACKET;CD-ROM,6020	
342666600002	BRACKET;HDD,TITAN	
342665700023	BRACKET;HYUNDAI,LCD 2ND,L,6020	
342665700024	BRACKET;HYUNDAI,LCD 2ND,R,6020	
342665700003	BRACKET;IO,6020,PRT	
344665700043	BUTTON;TOUCHPAD 2ND,6020	
422600000101	CABLE ASSY;A/D TO CHASSIS,PWR-60	
422600000103	CABLE ASSY;FAX MODEM,10P,4C,AUST	
332300000115	CABLE;FFC,FDD,6020	
332300000117	CABLE;FFC,TOUCHPAD,12P,6020	
272075103702	CAP;.01U ,50V,+80-20%,0603,SMT	C136,C137,C141,C142
272075103702	CAP;.01U ,50V,+80-20%,0603,SMT	PC7,509,523,511
272005103401	CAP;.01U ,CR,50V,10%,0805,X7R	C2
312161002631	CAP;.01U ,PE,100V,5% ,AX	C8

Part Number	Description	Location
272075104701	CAP;.1U ,50V,+80-20%,0603,SMT	C10,C100,C102,C104
272075104701	CAP;.1U ,50V,+80-20%,0603,SMT	PC4,5,15,501,503,
272003104701	CAP;.1U ,CR,25V ,+80-20%,0805,Y	PC2
272005104701	CAP;.1U ,CR,50V,+80-20%,0805,Y5	C1,9,10,12,17
272072224701	CAP;.22U ,16V ,+80-20%,0603,Y5V,	C33,C338,C536,C69
312263303851	CAP;.33U ,POLY,275V,20%,X2,AX	C6
272002474401	CAP;.47U ,CR,16V ,10%,0805,X7R,S	C501
272075102701	CAP;1000P,50V ,+80-20%,0603,SMT	C1,C103,C15,C172
272075102701	CAP;1000P,50V ,+80-20%,0603,SMT	PC502,506
312431001044	CAP;1000P,CR,1KV ,10%,DISK,X7R	C16,20
312431001043	CAP;1000P,CR,1KV ,10%,DISK,Y5P	C5
272075102403	CAP;1000P,CR,50V,10%,0603,X7R,SM	PC6
272005102401	CAP;1000P,CR,50V,10%,0805,X7R	C14,18
272075101701	CAP;100P ,50V ,+80-20%,0603,SMT	C3,C503,C504,C505
272075100701	CAP;10P ,50V ,+80-20%,0603,SMT	C203,C204,C215,C219
272021106501	CAP;10U ,10V ,20%,1210,X7R,SMT	PC35,PC524,PC533
272012106701	CAP;10U ,16V ,+80-20%,1206,Y5U,	C16,PC16,PC32,PC4
272022106701	CAP;10U ,16V,+80-20%,1210,Y5V,S	PC504
272023106501	CAP;10U ,25V ,20%,1210,Y5U,SMT	PC534,PC535
272043106501	CAP;10U ,CR,25V ,20%,1812,Y5U,S	PC532,PC536
272043106501	CAP;10U ,CR,25V ,20%,1812,Y5U,S	PC1,PC524
272073180401	CAP;18P ,CR,25V ,10%,0603,NPO,S	C145,C146,C282,C283
272071105701	CAP;1U ,CR,10V ,80-20%,0603,Y5	C159,C173,C174,C189
272013105501	CAP;1U ,CR,25V ,+80-20%,1206,S	PC23,PC522
272013105501	CAP;1U ,CR,25V ,+80-20%,1206,S	PC3
272002105701	CAP;1U ,CR,16V ,+20+80%,0805,SM	C101,C109,C115,C116

# 6120N N/B MAINTENANCE

## 9. SPARE PARTS LIST(2)

Part Number	Description	Location
272002105701	CAP;1U ,CR,16V ,-20+80%,0805,SM	PC510,505
272002105701	CAP;1U ,CR,16V ,-20+80%,0805,SM	C15
272012225702	CAP;2.2U ,CR,16V ,+80-20%,1206,Y	C260,C298,C301,C43
272075222701	CAP;2200P,50V ,+80-20%,0603,SMT	C157
312262201741	CAP;2200P,POLY,250V,10%,Y1,AX	C23
272075221302	CAP;220P ,50V ,5% ,0603,SMT	C31,C32,C34,C35
272005221401	CAP;220P ,CR,50V ,10%,0805,X7R,S	C4
272431225501	CAP;220U ,TT,4V,20%,7243,OS-CON,	PC17,PC504,PC505
272075220701	CAP;22P ,50V ,+80-20%,0603,SMT	C91,C99
272041226501	CAP;22U ,CR,10V ,20%,1812,X7R,S	C98,PC28
272073330701	CAP;33P ,25V ,+80-20%,0603,SMT	C343,237,5
272075391301	CAP;390P ,CR,50V,5%,0603,NPO,SMT	C93
272012475701	CAP;4.7U ,CR,16V ,+80-20%,1206,Y	C105,C125,C126,C127
312434701041	CAP;4700P,CR,1KV ,10%,DISK,Y5P	C22
272075470701	CAP;47P ,50V ,+80-20%,0603,SMT	C249,C250,C262,C263
272075470701	CAP;47P ,50V ,+80-20%,0603,SMT	C1-4
272431476502	CAP;47U ,6.3V,20%,SP-CON,7343,S	PC520
272005560401	CAP;56P ,CR,50V ,10%,0805,NPO,S	C3
272431566501	CAP;56U ,TT,4V,20%,SP-CON,7343,	PC521
221665720003	CARTON;AC ADAPTER,6020	
221665720004	CARTON;W/O ROC,N-B,6020	
431667910001	CASE KIT;6120N,ID2	
523466570004	CD ROM DRIVE ASSY;24X,CD-224E,60	
523499995002	CD ROM DRIVE OPTION;24X,6020	
523410295018	CD ROM DRIVE;24X,CD-224E-A92,TEA	
451665700093	CD ROM ME KIT;24X,CD-224E-A92,60	

Part Number	Description	Location
335152000026	CFM-BAT;FUSE,THERMAL,NEC,SF91E	
310131103004	CFM-BAT;NTCR,10K,SEMITEC,103AT-4	
335152000020	CFM-BAT;THERMAL BREAKER,ISUZU,IP	
342665500008	CFM-SUYIN;S-STANDOFF,#4-40H4.8,N	
313000020195	CHOKE COIL;1.3mH(MIN),18.5TS,D.5	T2
313000020190	CHOKE COIL;1.5UH,20%,7.5T,6*8	L1
273000500012	CHOKE COIL;10UH,4.7A,5.7MM,SMT	PT2
313000020191	CHOKE COIL;112UH(MIN),7.5T,2*0.6	T3
273000500016	CHOKE COIL;14UH/13.5T,D.6,55040	PL502
313000020192	CHOKE COIL;15mH(MIN),50.5T,D.6	T1
273000500015	CHOKE COIL;50UH(REF),D.4*2,5.5T,	PT1
313000020180	CHOKE COIL;6UH ,15%,D0.9,9MM,550	PL514
273000500011	CHOKE COIL;80UH/33T,D.30,55040,L	PL1
331720015006	CON;D,FM,15P,2.29,R/A,3ROW	J505
331720025005	CON;D,FM,25P,2.775,R/A	J506
331720009004	CON;D,MA,9P,2.775,R/A	J507
291000151202	CON;FPC/FFC,12P,0.5MM,R/A,UPPER,	J501
291000152604	CON;FPC/FFC,26P,1MM,R/A,ELCO,SMT	J5
291000152602	CON;FPC/FFC,26P,1MM,R/A,SMT,ELCO	J2
331030060003	CON;HDR,FM,20P*3,.8MM,ST,DIP	J1
331030044006	CON;HDR,FM,22P*2,2.0MM,ST,SUYIN,	J3
291000025002	CON;HDR,FM,25P*2,1.27MM,R/A,SMT	J514
291000015202	CON;HDR,FM,26P*2,1.0MM,ST,SMT,HR	J1
291000011001	CON;HDR,MA,10P*1,1.25,ST,SMT	J1
331040060003	CON;HDR,MA,20P*3,.8MM,R/A,AMP	J515
291000012102	CON;HDR,MA,21P,DUAL ROW,1.25,ST,	J2

# 6120N N/B MAINTENANCE

## 9. SPARE PARTS LIST(3)

Part Number	Description	Location
291000015012	CON;HDR,MA,25P*2,.8MM,ST,SMT,KX1	J501
291000025003	CON;HDR,MA,25P*2,1.27MM,R/A,SMT	J1
291000025203	CON;HDR,MA,26P*2,.5MM,R/A,W/NUT,	J513
291000020202	CON;HDR,MA,2P*1,1.25,R/A,SMT,HIR	J3,4
291000026004	CON;HDR,MA,30P*2,.6MM,R/A,SMT,(2	J510
331030006006	CON;HDR,MA,6P*1,2.0,ST,GLD	J2
291000020402	CON;HDR,SHROUD,MA,4P*1,2.0,R/A,U	J504
291000251441	CON;IC CARD,FM,72P*2,.6MM,H3MM,S	U504
331870004005	CON;MINI DIN,4P,R/A,W/GROUNDING,	J509
331870006011	CON;MINI DIN,6P,R/A,W/GROUNDING	J503
331810006010	CON;MODULAR JACK,FM,6P4C,R/A,GR	
331810006009	CON;MODULAR JACK,FM,6P4C,R/A,SW	
331810006014	CON;MODULAR JACK,FM,6P4C,R/A,UK	
331910003003	CON;POWER JACK,3P,16VDC/3A	PJ501
331910002003	CON;PWR PLUG,2P,250V/2.5A,SUPERC	J1
331510080001	CON;RBN,MA,80P,.63MM,R/A	J508
331840005007	CON;STEREO JACK,5P,R/A,W9.1,LGY2	J501,502
291000410301	CON;WFR,MA,3P,1.25,ST,SMT/MB	J511
346667700004	CONDUCTIVE SHEET;S-CONN,7020	
342665700016	CONTACTOR;HDD,6020	
340666500008	COVER ASSY;2ND,6120	
340666530004	COVER ASSY;COL-2,14.1",LCD,6120L	
340666500003	COVER ASSY;CPU,6120	
340665700030	COVER ASSY;LENS,ID2,COL2,6020	
441667910031	COVER ASSY;M/B,6120N,ID2	
344665700065	COVER;AC ADAPTER,6020	

Part Number	Description	Location
344665730004	COVER;HINGE,2ND,6020	
344665700005	COVER;MODEM,6020,PRT	
344665700004	COVER;PCMCIA,6020,PRT	
344665700041	COVER;PHONE JACK,6020	
272625101401	CP;100P*4,8P,50V ,10%,1206,NPO,S	CA1,CA505,CA506
272625470401	CP;47P*4 ,8P,50V ,10%,1206,NPO,S	CA2,CA3,CA501,CA502
272615562501	CP;5600P*4,8P,50V ,20%,0612,X7R,	CA4,CA5
291006214411	DIMM SOCKET;144P,.8MM,AMP353870,	J4
291006214410	DIMM SOCKET;144P,REVERSE,AMP,SMT	J3
288100032013	DIODE;BAS32L,VRRM75V,MELF,SOD-80	PD3,PD6,PD8
288100032013	DIODE;BAS32L,VRRM75V,MELF,SOD-80	PD2,502,503,507
288100032013	DIODE;BAS32L,VRRM75V,MELF,SOD-80	D3,9
288100701002	DIODE;BAV70LT1,70V,225MW,SOT-23	D11,D27,D30
288100099001	DIODE;BAV99,70V,450MA,SOT-23	D10
288100056003	DIODE;BAW56,70V,215MA,SOT-23	D14,D2
328100026005	DIODE;BYV26E,FAST,1A,1000V,AX,SO	D8
288100202001	DIODE;DAN202K,80V,SWITCH,SMT	PD501
288101004024	DIODE;EC10QS04,RECT,40V,1A,CHIP,	PD1,504
328101610002	DIODE;F16P10QS,16A,FAST RECOVERY	D1
328100406001	DIODE;PBL406,4A,800V,SIP,4P	D10
288104148001	DIODE;RLS4148,200MA,500MW,MELF,S	D1,12,13,15,16,28,29
288100020002	DIODE;RLZ2.0B,ZENER,2.02-2.2,5%,	PD5
288100027001	DIODE;RLZ2.7B,ZENER,2.6-2.91,5%,	PD2
288100020001	DIODE;RLZ20C,ZENER,19.23V,5%,SMT	PD508
288100024002	DIODE;RLZ24D,ZENER,23.63V,5%,SMT	PD1
288100024002	DIODE;RLZ24D,ZENER,23.63V,5%,SMT	PD1

# 6120N N/B MAINTENANCE

## 9. SPARE PARTS LIST(4)

Part Number	Description	Location
288100073002	DIODE;SFPJ-73,DC2010,30V,3A,SMT	PD10,PD503,PD9
288100073002	DIODE;SFPJ-73,DC2010,30V,3A,SMT	PD505,506,509
288100016003	DIODE;TZMC16,ZENER,16V,5%,SMT	D4
328114003001	DIODE;UF4003G,200V/1A,PRE./DO-41	D5
312271006350	EC;100U ,25V,20%,RA,6.3*7,-40~10	PC518,519,523
312271006350	EC;100U ,25V,20%,RA,6.3*7,-40~10	PC8,9,14
272602107501	EC;100U,16V,M,6.3*5.5,-55+85°C,S	C12,C21,C25,C310
312271006359	EC;100U,25V,M,D6.3,RA,-40~105°,L	C13
312271206951	EC;120U ,400V,20%,RA,D35,-25~10	C53
312272206152	EC;220U ,4V ,M,RA,D8*5,OS-CON	PC515,516
312272206152	EC;220U ,4V ,M,RA,D8*5,OS-CON	PC12
312272206154	EC;220U ,6.3V,20%,RA,D10*5,OS-CO	PC11
312272205051	EC;22U,20V,M,RA,D6.3,-55+105,OS-	PC13
312273306154	EC;330U ,4V ,+-20%,100*5,SP.OS-	PC513,517
312274706354	EC;470U ,25V ,20%,RA,D10,-20~10	C7,11,19
227666500007	END CAP;MIDDLE,AK,6120	
2276665700001	END CAP;N/B,6020	
2276665700007	END CAP;TOP/BTM,AC ADAPTER,6020	
227666500006	END CAP;TOP/BTM,AK,6120	
481667900001	F/W ASSY;SYS&KBC BIOS,13"/14",61	U36
523411442008	FD DRIVE;1.44M,3 MODE,D353G	
523466570001	FDD/HDD COMBO ASSY;6020	
273000610004	FERRITE ARRAY;120OHM/100MHZ,M TY	FA1,FA2,FA3,FA4,FA5
273000150013	FERRITE CHIP;120OHM/100MHZ,2012,	L10,L11,L13,L16,L2
273000150013	FERRITE CHIP;120OHM/100MHZ,2012,	PL2,501-506,511
273000130010	FERRITE CHIP;130OHM/100MHZ,1608,	L506,L507,L508,L509

Part Number	Description	Location
273000130013	FERRITE CHIP;30OHM/100MHZ,1608	PL6,PL7
273000130013	FERRITE CHIP;30OHM/100MHZ,1608	L1-3,PL507-509
273000130006	FERRITE CHIP;600OHM/100MHZ,.2A,1	L28,L3,L501,L502
313000150019	FERRITE CORE;25OHM/100MHZ,D3	L2
313000150020	FERRITE CORE;25OM100MZ,CORE ONLY	
346600000025	FILM;300MM*500M,PE	
288003600001	FIR;HSDL3600#007,FRONT VIEW,10P,	U501
295000010008	FUSE;1.1A,POLY SWITCH,1812,SMT	F2,F3,F4
295000010105	FUSE;1A,NORMAL,1206,SMT	F5
335152000031	FUSE;LAG,4A ,HIBREAK,5*20MM	F1
295000010016	FUSE;NORMAL,6.5A/32VDC,3216,SMT	PF1
295000010020	FUSE;NORMAL,7A/24VDC,1206,SMT	PF501
345665700010	GASKET;AUDIO,6020	
345666500001	GASKET;IO BRACKET,6120	
345665700019	GASKET;PCMCIA,6020	
345665700012	GASKET;USB,6020	
344600000296	GRAIN;PPO.94V-1,BLACK,PRC	
344600000296	GRAIN;PPO.94V-1,BLACK,PRC	
340666500002	HEATSINK ASSY;CPU,6120	
342665700040	HEATSINK;L,AC ADAPTER,6020	HS1
342665700041	HEATSINK;R,AC ADAPTER,6020	HS2
340667000006	HOUSING ASSY;6020+	
340666530002	HOUSING ASSY;COL-2,ID2,LCD,6120L	
451666540051	HOUSING KIT;6120L,ID2	
451600001001	HOUSING KIT;AC 60B	
344665700066	HOUSING;AC ADAPTER,6020	

# 6120N N/B MAINTENANCE

## 9. SPARE PARTS LIST(5)

Part Number	Description	Location
344665700069	HOUSING-1;HDD,6020	
344600000235	IC CARD CON PART;72P*2,6020	
331650037002	IC SOCKET;370P,ZIF,ZIFPGA370	U503
284500003007	IC;3D RAGE LT PRO,AGP,BGA,328P,J	U18
282574014004	IC;74AHC14,HEX INVERTER,TSSOP,14	U10
282574108002	IC;74AHC1G08,SINGLE AND GATE,SOT	U7
284501021002	IC;ADM1021,TEMPERATURE MTR,SSOP1	U19
286203311001	IC;ADM3311E,RS-232,TSSOP,28P	U2
286300431016	IC;AME431ACFT,1%,ADJ REG,SOT89	Q4
284504280001	IC;CS4280-CQ,PCI AUDIO,TQFP,128P	U11
284504297001	IC;CS4297,AUDIO CODEC,TQFP,48P	U9
283466712001	IC;FLASH,512K*8-90,PLCC,32P,6133	
284182371005	IC;FW82371EB,PIIX4E,PCI/ISA,BGA3	U24
284582443010	IC;FW82443BX,HOST BRIDG,BGA492,6	U16
286317812001	IC;HA178L12UA,VOLT REGULATOR,SC-	PU1
286100358012	IC;LM358,DUAL OP/AMP,SO 8P	U3
286100393004	IC;LMV393,DUAL COMPARTOR,SSOP,8P	PU503,PU504
286302951015	IC;LP2951ACM,VOLTAGE REGULATOR,S	U32
286300809002	IC;MAX809S,RESET CIRCUIT,2.9V,SO	U27
284501284002	IC;PACS1284-02Q/T,TERMIN NET,QSO	U1
284587570001	IC;PC87570,KBD & PWR CTRL,TQFP,1	U34
284597338001	IC;PC97338VJG,SUPER I/O,TQFP,100	U29
284501225001	IC;PCI1225PDV,PCI/CARDBUS,LQFP,2	U25
286303032001	IC;SB3032P,PWM CTRL,SO,16P	PU1,PU2
286303052001	IC;SB3052P,PWM CTRL,SSOP,28P	PU501
286300431011	IC;SC431CSK-.5,.5%,ADJ REG,SOT23	PQ12,PQ4

Part Number	Description	Location
283866700001	IC;SGRAM,1M*32-100,PQFP,100P,602	U14,U20
286300594001	IC;TL594C,PWM CONTROL,SO,16P	PU502
286100202001	IC;TPA0202,AUDIO AMP,2W,TSSOP,24	U3
286302206001	IC;TPS2206,CARDBUS PWR CTRL,SSOP	U33
286303843002	IC;UC3843BD,PWM CTRL,SO,8P,SMT	U2
286500137001	IC;W137,CLOCK GENERATOR,SSOP,28P	U22
284104011001	IC;W40S11-02,SDRAM BUFFER,SSOP,2	U21
273000051001	INDUCTOR;22UH,110mA,3225,SMT	L12
346665700033	INSULATOR;A/D,23MM,MAD-60B,6020	
346665700034	INSULATOR;A/D,65MM,MAD-60B,6020	
346665700012	INSULATOR;FDD BACK,6020	
346665400009	INSULATOR;I/O PANEL,VENUS	
346665700026	INSULATOR;MODEM,6020	
340665700001	IO DOOR ASSY;6020,ASM	
451667900003	LABEL KIT;LOGO,MAXDATA,6120N	
242600000380	LABEL;10*8MM,BIOS,HI-TEMP 260	
242662300009	LABEL;25*10MM,3020F	
242600000378	LABEL;27*7MM,HI-TEMP 260C	
242665700016	LABEL;AGENCY,ADPT-19,6020	
242666500002	LABEL;AGENCY-GLOBAL BCIQ,6120	
242600000088	LABEL;BAR CODE,125*65,COMMON	
242690500078	LABEL;BAR CODE,32*16MM,MD4	
242690500078	LABEL;BAR CODE,32*16MM,MD4	
242600000003	LABEL;BAR CODE,NEW,COMMON	
242600000169	LABEL;BLANK,23.8*5MM,COMMON	
242600000364	LABEL;BLANK,6*6MM,HI-TEMP	

# 6120N N/B MAINTENANCE

## 9. SPARE PARTS LIST(6)

Part Number	Description	Location
242600000364	LABEL;BLANK,6*6MM,HI-TEMP	
242600000099	LABEL;MODEL,5M,MITAC	
242600000001	LABEL;PAL,20*5MM,COMMON	
242600000195	LABEL;SOFTWARE,INSYDE BIOS-M	
242665600006	LABEL;WINDOWS 98,CARTON,5036	
242665600007	LABEL;WINDOWS 98,LCD COVER,5036	
242665700013	LABEL;Y2K,6020	
441666540004	LCD ASSY;TFT,HYUN,14.1",6120L,ID	
451666540033	LCD ME KIT;TFT,HYUN,14.1",6120L,	
413000020138	LCD;HT14X11,TFT14.1,XGA,HYUNDAI	
334212000010	LED HOLDER;ROUND,NYLON,LED-18.5	
294011200017	LED;GREEN,H0.8,0603,CL-190,SMT	D4-9
334112000129	LED;ROUND,D3.2,H4.6MM,P2.54,HI,G	D2
416260001001	MAIN UNIT;AC 60B-19V	
561566570012	MANUAL KIT;EU,6020,NON-BRAND	
561566650018	MANUAL;REF,FR/IT/SP,6020/6120,N-	
561566650015	MANUAL;USER'S,EN,6120/6020NON-BR	
561566570036	MANUAL;USER'S,GR,6020/6120NON-BR	
451665700071	ME KIT;HDD,6020	
339115000008	MICROPHONE;D9.7*H6.7,WM-034BY	MIC1
242666500055	NAMEPLATE;MAXDATA,6120	
416266791901	NB PLATFORM OPTION;14.1",6120N,I	
416266791001	NB PLATFORM;TFT,HT14X11,6120N,ID	
526266791023	NBX;6120N/T4XX/XXA/3XX9/N3DNBA M	
375102030010	NUT-HEX;M2,2,NIW	
328001103001	OPTOCOUPLE;TCET1103,60mA,4P	U1

Part Number	Description	Location
461600001001	PACKING KIT;AC-60B	
461667030003	PACKING KIT;N-B,6020+ CTO	
221665750002	PARTITION;AC ADAPTER,25 IN 1,602	
412665700003	PCB ASSY;FAX MODEM,CTR-21,WIN,60	
412219300019	PCB ASSY;INVERTER BD,14.1",6020	
316665700007	PCB;PWA-6020/CDROM TRANS BD	R0B
316665700013	PCB;PWA-6020/MAD-60B BD	R01
316665700014	PCB;PWA-6020/MAD-60BI BD	R01
316666530002	PCB;PWA-6120L/CHARGER BD	R00
316667900001	PCB;PWA-6120W/M BD	R02
316666600002	PCB;PWA-TITAN,HDD/FDD BD	R02
222664720001	PE BAG;310*450,T.08,RECY.,5026VO	
222600020049	PE BAG;50*70MM,W/SEAL,COMMON	
222665520003	PE BAG;80*200MM,5033	
222665720002	PE BAG;LCD ASSY,14",6020	
222665720003	PE BAG;W130*L250,6020	
340667000005	PLATE ASSY;TP 2nd,6020+	
335512000003	POLYSWITCH;3.8A,LR4-380	
411665700009	PWA;PWA-6020 CD-ROM TRANSLATION	
411666530005	PWA;PWA-6120L,CHARGER BD,SMT	
411666530004	PWA;PWA-6120L,CHARGER BD,T/U	
411667900001	PWA;PWA-6120N,MOTHER BD	
411667900003	PWA;PWA-6120N,V0 MOTHER BD,SMT	
411667900002	PWA;PWA-6120N,V0 MOTHER BD,T/U	
411600000112	PWA;PWA-PWR-60B-19,A/D BD,SMT	
411600000113	PWA;PWA-PWR-60B-19,A/D BD,T/U	

# 6120N N/B MAINTENANCE

## 9. SPARE PARTS LIST(7)

Part Number	Description	Location
411666600001	PWA;PWA-TITAN,HDD/FDD BD,SMT	
411666600005	PWA;PWA-TITAN,HDD/FDD BD,T/U	
332810000034	PWR CORD;250V/2.5A,2P,BLK,EU,175	
271086057101	RES;.005 ,2W ,1% ,7520,SMT	PR11
271045107101	RES;.01 ,1W ,1% ,2512,SMT	PR521,514
311100157301	RES;.015 ,MnCu,1/4W,5%,10.2*5.0,	JP1
271045207101	RES;.02 ,1W ,1% ,2512,SMT	PR13
271045207101	RES;.02 ,1W ,1% ,2512,SMT	PR505
271002000301	RES;0 ,1/10W,5% ,0805,SMT	L14,L15,L17,L18,L513
271002000301	RES;0 ,1/10W,5% ,0805,SMT	R6
271071000002	RES;0 ,1/16W,0603,SMT	PR15,R106,R122,R129
271071000002	RES;0 ,1/16W,0603,SMT	R2,5,PR503,PR5
271012000301	RES;0 ,1/8W,5% ,1206,SMT	R3,4,8,11,14
271013010301	RES;1 ,1/4W,5% ,1206,SMT	R43,R44
271013119301	RES;1.1 ,1/4W,5% ,1206,SMT	R41,R42,R18
311121101337	RES;1.1K ,CF,1/4W,5% ,AX	R24
271071121111	RES;1.21K,1/16W,1% ,0603,SMT	PR513
271071100302	RES;10 ,1/16W,5% ,0603,SMT	R105,R234,R235,R52
271002101301	RES;100 ,1/10W,5% ,0805,SMT	R13
271071101101	RES;100 ,1/16W,1% ,0603,SMT	R112,R136,R55,R56
271071104101	RES;100K ,1/16W,1% ,0603,SMT	PR10,12,508,512,
271071104302	RES;100K ,1/16W,5% ,0603,SMT	PR17,506,511,R193,
271012104301	RES;100K ,1/8W,5% ,1206,SMT	R27,28,33,35
271071102311	RES;102K ,1/16W,1% ,0603,SMT	PR6
271002103301	RES;10K ,1/10W,5% ,0805,SMT	R23,32
271071103101	RES;10K ,1/16W,1% ,0603,SMT	PR5,PR8

Part Number	Description	Location
271071103101	RES;10K ,1/16W,1% ,0603,SMT	PR4,501,502,509
271071103302	RES;10K ,1/16W,5% ,0603,SMT	PR16,R101,R118,R144
271012103301	RES;10K ,1/8W,5% ,1206,SMT	R19
271071111101	RES;110 ,1/16W,1% ,0603,SMT	R282,562
271071118311	RES;118K ,1/16W,1% ,0603,SMT	PR9
271071124301	RES;120K ,1/16W,5% ,0603,SMT	R260
271071124311	RES;124K ,1/16W,1% ,0603,SMT	PR513
271071137211	RES;13.7K,1/16W,1% ,0603,SMT	PR13
271071134101	RES;130K ,1/16W,1% ,0603,SMT	PR509
271002147211	RES;14.7K,1/10W,1% ,0805,SMT	R16
271072151101	RES;150 ,1/10W,1% ,0603,SMT	R111,R13,R284,R285
271071153301	RES;15K ,1/16W,5% ,0603,SMT	R152,R155,R182,R225
271071180301	RES;18 ,1/16W,5% ,0603,SMT	R103,R110,R162,R163
271071184301	RES;180K ,1/16W,5% ,0603,SMT	R24
271002102301	RES;1K ,1/10W,5% ,0805,SMT	R15
271071102102	RES;1K ,1/16W,1% ,0603,SMT	R51
271071102102	RES;1K ,1/16W,1% ,0603,SMT	PR3,507
271071102302	RES;1K ,1/16W,5% ,0603,SMT	PR4,PR507,R1,R114
271071105101	RES;1M ,1/16W,1% ,0603,SMT	PR20,PR22,PR24,PR514
271071105101	RES;1M ,1/16W,1% ,0603,SMT	PR6,7,9
271071105301	RES;1M ,1/16W,5% ,0603,SMT	R100,R126,R140,R25
271002221111	RES;2.21K,1/10W,1% ,0805,SMT	R22,12
271071222302	RES;2.2K ,1/16W,5% ,0603,SMT	PR518
271071225301	RES;2.2M,1/16W,5% ,0603,SMT	PR23,PR510
271071272301	RES;2.7K ,1/16W,5% ,0603,SMT	R61,R71,R87,R166
271071204302	RES;200K ,1/16W,5% ,0603,SMT	R290

# 6120N N/B MAINTENANCE

## 9. SPARE PARTS LIST(8)

Part Number	Description	Location
271071203101	RES;20K ,1/16W,1% ,0603,SMT	PR18,PR512
271071203101	RES;20K ,1/16W,1% ,0603,SMT	PR520
271071206301	RES;20M ,1/16W,5% ,0603,SMT	R293
271002220301	RES;22 ,1/10W,5% ,0805,SMT	R39
271071221302	RES;22 ,1/16W,5% ,0603,SMT	R294,R295,R296
271071221211	RES;22.1K,1/16W,1% ,0603,SMT	PR15
271012224301	RES;220K ,1/8W,5% ,1206,SMT	R37,38
271071226311	RES;226K ,1/16W,1% ,0603,SMT	PR26
271071237311	RES;237K ,1/16W,1% ,0603,SMT	PR7
271071243311	RES;243K ,1/16W,1% ,0603,SMT	PR516
271071249311	RES;249K ,1/16W,1% ,0603,SMT	PR2
271071270301	RES;27 ,1/16W,5% ,0603,SMT	R156,R168,R175,R176
271071271301	RES;270 ,1/16W,5% ,0603,SMT	R10,R11,R12
271002274311	RES;274K ,1/10W,1% ,0805,SMT	R31
271071301211	RES;30.1K,1/16W,1% ,0603,SMT	PR14
271071301311	RES;301K ,1/16W,1% ,0603,SMT	PR11
271071324211	RES;32.4K,1/16W,1% ,0603,SMT	PR508
271071324012	RES;324K ,1/16W,1% ,0603,SMT	PR19
271071330302	RES;33 ,1/16W,5% ,0603,SMT	R120,R121,R123,R124
271071331301	RES;330 ,1/16W,5% ,0603,SMT	R119,220,167,
271012331301	RES;330 ,1/8W,5% ,1206,SMT	R5
271071333301	RES;33K ,1/16W,5% ,0603,SMT	R514,R519
271071392211	RES;39.2K,1% ,1/16W,0603,SMT	PR27
271071305301	RES;3M ,1/16W,5% ,0603,SMT	PR8
271012432301	RES;4.3K ,1/8W,5% ,1206,SMT	R7
271013478301	RES;4.7 ,1/4W,5% ,1206,SMT	R501,R502

Part Number	Description	Location
271002472301	RES;4.7K ,1/10W,5% ,0805,SMT	PR1
271002472301	RES;4.7K ,1/10W,5% ,0805,SMT	R26
271071472302	RES;4.7K ,1/16W,5% ,0603,SMT	R18,
271071472302	RES;4.7K ,1/16W,5% ,0603,SMT	PR510
271071499111	RES;4.99K,1/16W,1% ,0603,SMT	PR505
271071442011	RES;442 ,1/16W,1% ,0603,SMT	R59,R60
271071470301	RES;47 ,1/16W,5% ,0603,SMT	R128,R134,R185,R189
271071471302	RES;470 ,1/16W,5% ,0603,SMT	PR3,R139,R205
271071474301	RES;470K ,1/16W,5% ,0603,SMT	R154,R218,R219,R531
271012474301	RES;470K ,1/8W,5% ,1206,SMT	R1,2
271071473101	RES;47K ,1/16W,1% ,0603,SMT	PR501,PR504
271071473301	RES;47K ,1/16W,5% ,0603,SMT	PR21,R227,R228,R248
271071473301	RES;47K ,1/16W,5% ,0603,SMT	R1,PR511,519
271071487311	RES;487K ,1/16W,1% ,0603,SMT	PR14
271071562301	RES;5.6K ,1/16W,5% ,0603,SMT	R143,R158,R169
271071510301	RES;51 ,1/16W,5% ,0603,SMT	R69
271012510301	RES;51 ,1/8W,5% ,1206,SMT	R9,10
271071514301	RES;510K ,1/16W,5% ,0603,SMT	PR503,PR515
271071560301	RES;56 ,1/16W,5% ,0603,SMT	R84,85
271071564301	RES;560K ,1/16W,5% ,0603,SMT	R242,R243
271013564301	RES;560K ,1/4W ,5% ,1206,SMT	R29
271071593101	RES;59K ,1/16W,1% ,0603,SMT	PR12
271071622301	RES;6.2K ,1/16W,5% ,0603,SMT	PR506
271071682101	RES;6.8K ,1/16W,1% ,0603,SMT	R29,R32,R45
271002698111	RES;6.98K,1/8W ,1% ,0805,SMT	R30
271071681301	RES;680 ,1/16W,5% ,0603,SMT	R113,R147,R8,R9

# 6120N N/B MAINTENANCE

## 9. SPARE PARTS LIST(9)

Part Number	Description	Location
271013683301	RES;680K ,1/4W ,5% ,1206,SMT	R25
271002683301	RES;68K ,1/8W,5% ,0805,SMT	R21
271071750101	RES;75 ,1/16W,1% ,0603,SMT	R14,R76
271002822301	RES;8.2K ,1/10W,5% ,0805,SMT	R20
271071806211	RES;80.6K,1/16W,1% ,0603,SMT	PR25
271071976311	RES;976K ,1/16W,1% ,0603,SMT	PR16
561566570042	REVISED PAGE;EN,6020,NO.1	
271611000301	RP;0*4 ,8P ,1/16W,5% ,0612,SMT	RP87,RP9,RP97
271571000301	RP;0*8 ,16P ,1/16W,5% ,1606,SM	RP11,14,47-49
271571100301	RP;10*8 ,16P ,1/16W,5% ,1606,SM	RP15,RP16,RP17,RP18
271611104301	RP;100K*4,8P ,1/16W,5% ,0612,SMT	RP41,RP81
271611103301	RP;10K*4 ,8P ,1/16W,5% ,0612,SMT	RP38,RP56,RP67
271621103303	RP;10K*8 ,10P,1/16W,5% ,1206,SMT	RP52,RP53,RP55,RP57
271611151301	RP;150*4 ,8P ,1/16W,5% ,0612,SMT	RP25
271611102301	RP;1K*4 ,8P ,1/16W,5% ,0612,SMT	RP59
271611222301	RP;2.2K*4,8P ,1/16W,5% ,0612,SMT	RP8
271611220301	RP;22*4 ,8P ,1/16W,5% ,0612,SMT	RP92
271611330301	RP;33*4 ,8P ,1/16W,5% ,0612,SMT	RP44
271571330301	RP;33*8 ,16P ,1/16W,5% ,1606,SM	RP23,RP26,RP35,RP60
271611472301	RP;4.7K*4,8P ,1/16W,5% ,0612,SMT	RP28,RP7
271621472303	RP;4.7K*8,10P,1/16W,5% ,1206,SMT	RP54,RP58,RP68,RP73
271621433301	RP;43K*8 ,10P,1/16W,5% ,1206,SMT	RP80,RP82,RP83,RP84
271621473301	RP;47K*8 ,10P,1/16W,5% ,1206,SMT	RP90
271621560301	RP;56*8 ,10P,1/16W,5% ,1206,SMT	RP1-3,10,13,19,21
271611750301	RP;75*4 ,8P ,1/16W,5% ,0612,SMT	RP22,RP501
271621822301	RP;8.2K*8,10P,1/16W,5% ,1206,SMT	RP40,RP43,RP45,RP72

Part Number	Description	Location
345667000002	RUBBER;LCD,DOWN,6020+	
345666600011	RUBBER;PCB,FDD/HDD,TITAN	
565166650001	S/W;CD ROM,SYSTEM DRIVER,6120/60	
371102610405	SCREW;M2.6L4,K-HEAD(+),NIW	
371102030303	SCREW;M2L3,K-HEAD(+),NIW/NLK	
371102010601	SCREW;M2L6,FLT(+),NIW	
340666500001	SHIELDING ASSY;BOTTOM,6120	
340665700040	SHIELDING ASSY-1;HDD,6020	
346666500003	SHIELDING;CD ROM,6120	
346666530004	SHIELDING;ESD,VR,6120L	
346666500002	SHIELDING;PCMCIA,6120	
333050000014	SHRINK TUBE;600V,125',D1.5*20MM,	
561866570001	SINGLE PAGE;DOC/EC,6020	
561860000022	SINGLE PAGE;GN,NOTE FOR BATTERY&	
561860000028	SINGLE PAGE;PWR-60B-19A	
361200003025	SOLDER PASTE;RMA-010-FP	
361200003025	SOLDER PASTE;RMA-010-FP	
346667120001	SPACER;FC-PGA CPU,6133XN	
342665700015	SPC-SCREW;M2*L4.9,NIB,K-HD,6020	
370102610602	SPC-SCREW;M2.6 L6,NIB,K-HD,727	
370102610602	SPC-SCREW;M2.6 L6,NIB,K-HD,727	
370102611601	SPC-SCREW;M2.6*L16,NIB,K-HD	
370102610401	SPC-SCREW;M2.6L4,NIB,727,NLK	
370102610801	SPC-SCREW;M2.6L8,NIB,K-HD,NYLOCK	
370102011501	SPC-SCREW;M2L15,NIW,FLT(+),NL,73	
370102010201	SPC-SCREW;M2L2,NIW,K-HD,727	

# 6120N N/B MAINTENANCE

## 9. SPARE PARTS LIST(10)

Part Number	Description	Location
370102020301	SPC-SCREW;M2L3,NIW,K-HEAD	
370102020301	SPC-SCREW;M2L3,NIW,K-HEAD	
370102020301	SPC-SCREW;M2L3,NIW,K-HEAD	
370103010405	SPC-SCREW;M3L4,NIW,K-HD,T0.3	
370103010505	SPC-SCREW;M3L5,FLNG/PAN(+),HD7,N	
370103010604	SPC-SCREW;M3L6,NIB,727,NYLOK	
340665700008	SPEAKER BOX ASSY;L,6020,ASM	
340665700007	SPEAKER BOX ASSY;R,6020,ASM	
346665700018	SUPPORTER;CD-ROM CONN,6020	
297120101005	SW;DIP,SPST,8P,50VDC,.1A,SMT,DHS	SW2
297030105001	SW;PUSH BUTTON,SPSD,48V/.05A,SMT	SW1
297040101003	SW;PUSH BUTTON,SPST,.1A,30V,2P,S	SW1,2
225600000013	TAPE;60MM*50M,PP	
225600000012	TAPE;60MM*900M,PP	
340665700003	TILT UNIT;L,6020,PRT	
340665700002	TILT UNIT;R,6020,PRT	
442164900003	TOUCH PAD MODULE;TM41PDM220-2	
288227002001	TRANS;2N7002LT1,N-CHANNEL FET	PQ13,Q11,14,37,40,41
288227002001	TRANS;2N7002LT1,N-CHANNEL FET	PQ501,507
328222645001	TRANS;2SK2645-01MR,9A,600V,TO-22	Q5
288200144002	TRANS;DTA144WK,PNP,SMT	PQ506
288200144002	TRANS;DTA144WK,PNP,SMT	Q1
288200144001	TRANS;DTC144WK,NPN,SOT-23,SMT	PQ10,PQ5,PQ502,PQ6
288200144001	TRANS;DTC144WK,NPN,SOT-23,SMT	Q2
288206612001	TRANS;FDS6612A,N-MOSFET,.03OHM,S	PQ502,503
288206690001	TRANS;FDS6690A,N-MOSFET,.017OHM,	PQ504,505

Part Number	Description	Location
288202222001	TRANS;MMBT2222AL,NPN,TO236AB	PQ509
288203904010	TRANS;MMBT3904L,NPN,Tr35NS,TO236	PQ501,Q10,44,7,9
288203906018	TRANS;MMBT3906L,PNP,Tr35NS,TO236	Q35
288204401001	TRANS;MMBT4401,NPN,SOT-23,3P	Q3
288207002001	TRANS;NDC7002N,N-MOSFET,SSOT-6	PQ7,PQ8
288207002001	TRANS;NDC7002N,N-MOSFET,SSOT-6	PQ1,2
288200352001	TRANS;NDS352P,DMOS,TO-236AB	Q20,Q502
288202301001	TRANS;SI2301DS,P-MOSFET,SOT-23	Q30
288202302001	TRANS;SI2302DS,N-MOSFET,SOT-23	PQ2,Q12,Q16,Q18,Q3
288204416001	TRANS;Si4416DY,N-MOSFET,.028OHM,	PU3,PU5
288204435001	TRANS;SI4435DY,P-MOSFET,.035OHM,	PQ508,510
288204832001	TRANS;SI4832DY,N-MOSFET,.028OHM,	PU4
288204603001	TRANS;SPB46N03L,30V46A,N-CH,TO26	PQ11
271911103902	VR;10K ,20%,.05W,XV0102GPH1N-93	VR1
346667000009	WASHER;PLATE,TOUCHPAD,6020+	
421666530001	WIRE ASSY;HY14.1,LCD,6120L	
421666500006	WIRE ASSY;INVERTER,LCD,6120	
313001050040	XSFORMER;18U/17.5T/36.5T/8D/.35	PT1
313001050056	XSFORMER;PQ2620,LP=650uH,38/5/7	T14
274011431408	XTAL;14.318M,50PPM,32PF,7*5,4P,S	X500
274012457405	XTAL;24.576M,50PPM,16PF,7*5,4P,S	X1
274012949401	XTAL;29.498928MHZ,30PPM,20PF,4P,	X2
274013276103	XTAL;32.768KHZ,20PPM,12.5PF,CM20	X5,X6



## 6120N N/B MAINTENANCE

### **13. SYSTEM BLOCK DIAGRAM & SCHEMATICS**

**MOTHER-BOARD**

**DC /DC BOARD**