6020 N/B MAINTENANCE

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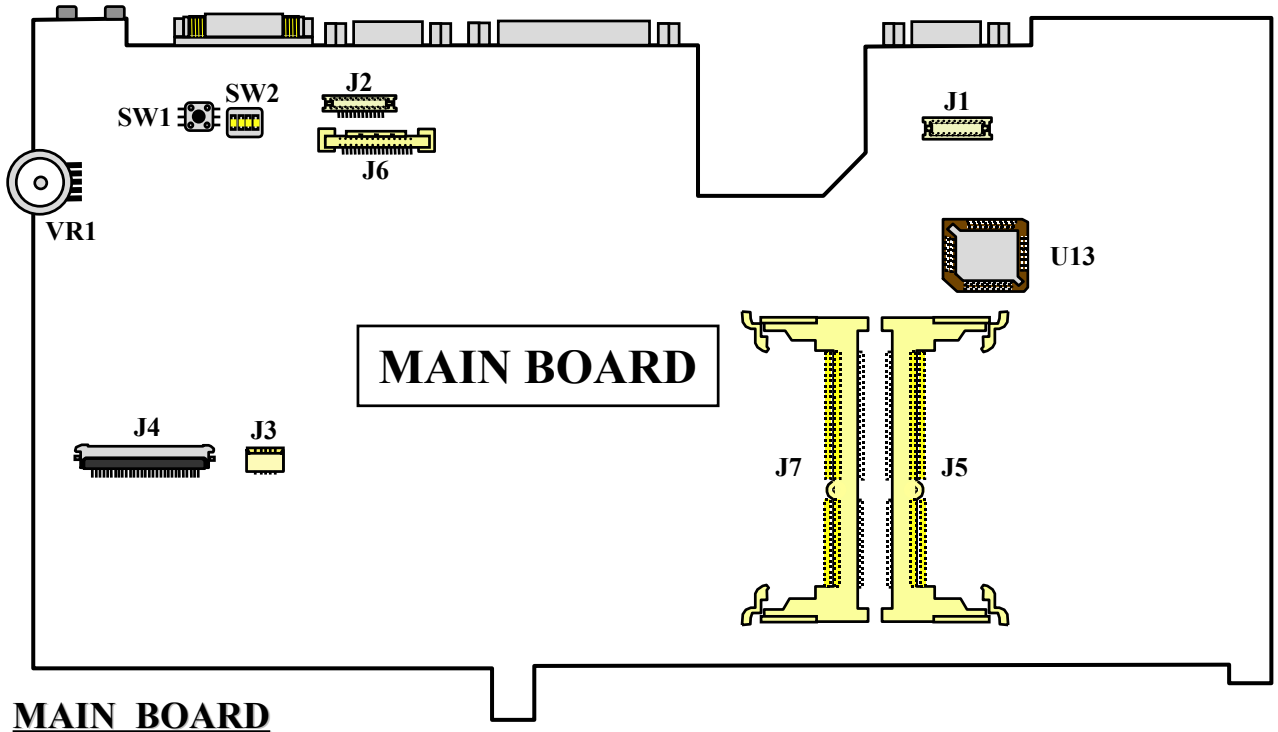
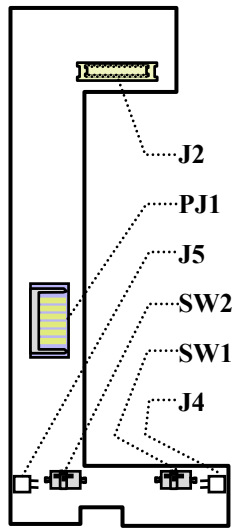
6020 N/B MAINTENANCE

1 . LOCATION OF CONNECTORS & SWITCHES (TOP SIDE)





BATT TP BD

MAIN BOARD

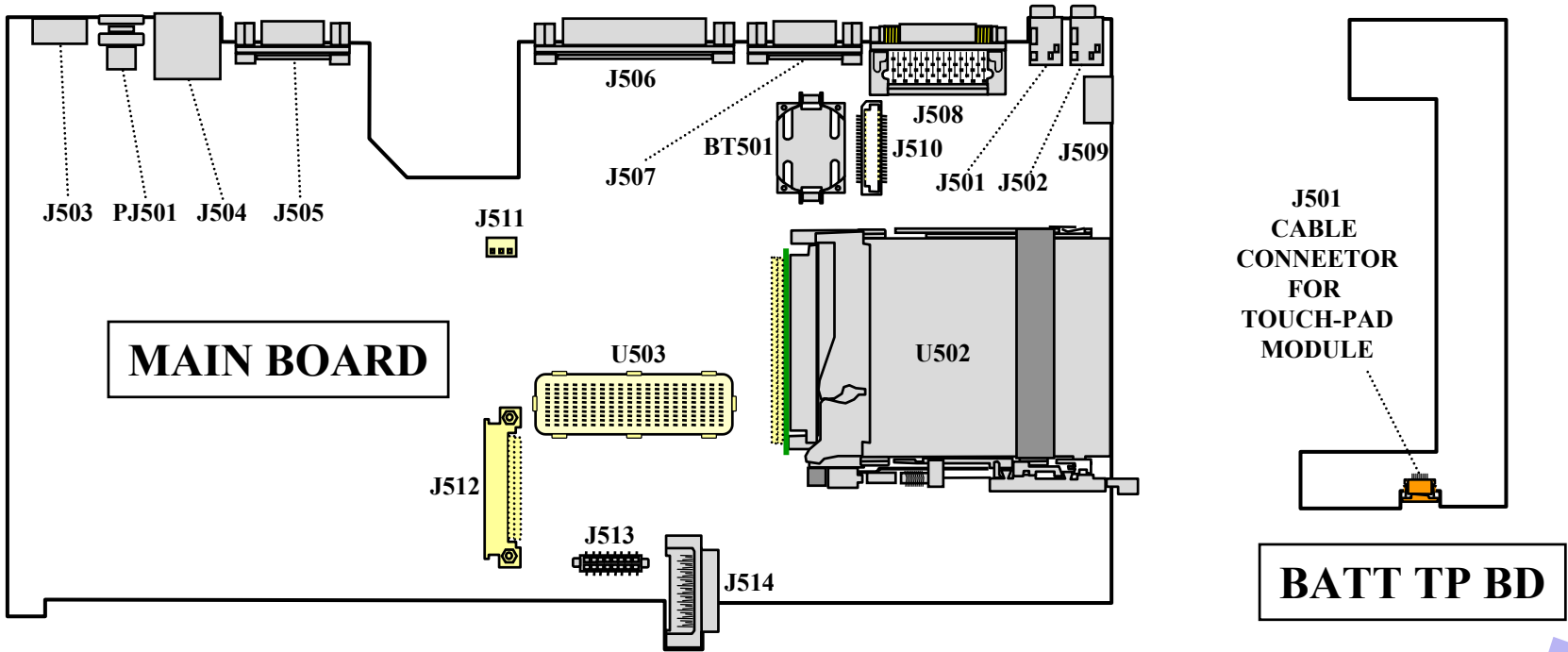
- J1 : BACKLIGHT AND LED INDICATOR CONNECTOR.
- J2 : LVDS LCD PANEL CONNECTOR(REMOVED AFTER R01 OF PCBA).
- J3 : TRACK POINT CONNECTOR (NO ASSEMBLY).
- J4 : INTERNAL KEYBOARD CONNECTOR.
- J5, J7 : 144 PIN 3.3V UNBUFFER EXPANSION DIMM SOCKET.
- J6 : LVDS LCD PANEL CONNECTOR.
- U13 : FLASHABLE SYSTEM BIOS SOCKET.
- SW1 : POWER ON SWITCH.
- SW2 : ID SELECTION FOR LCD PANEL (THE DEFAULT SETTING ARE ON BEFORE THE R02 VERSION OF PCBA).
- VR1 : VOLUME CONTROL FOR AUDIO SYSTEM.

BATT TP BOARD

- J2 : THE CONNECTOR FOR BATT TP BOARD TO CONNECT MAIN BOARD.
- PJ1 : BATTERY PACK CONNECTOR.
- J4, J5 : INTERNAL SPEAKER CONNECTOR.
- SW1, SW1 : TOUCH-PAD BUTTON SWITCH CONNECTOR.

6020 N/B MAINTENANCE

1 . LOCATION OF CONNECTORS & SWITCHES(BOTTOM SIDE)



MAIN BOARD

- J501 : EXTERNAL MICROPHONE CONNECTOR.
- J502 : INTERNAL SPEAKER CONNECTOR.
- J503 : PS/2 KEYBOARD OR MOUSE CONNECTOR.
- J504 : USB PORT CONNECTOR.
- J505 : SERIAL PORT CONNECTOR.
- J506 : PRINTER PORT CONNECTOR.
- J507 : EXTERNAL CRT MONITOR CONNECTOR.
- J508 : PORT REPLICATER CONNECTOR.
- J509 : TV TERMINAL CONNECTOR.
- J510 : FAX/MODEM/VOICE CARD CONNECTOR.
- J511 : CPU FAN CONNECTOR.
- J512 : CD-ROM CONNECTOR.
- J513 : BATT TP BD CONNECTOR.
- J514 : FDD AND HDD CONNECTOR.
- BT501 : COMS BACK-UP BATTERY SOCKET.
- U502 : PCI PCCARD CONNECTOR.
- U503 : MMC2 CPU MODULE CONNECTOR.

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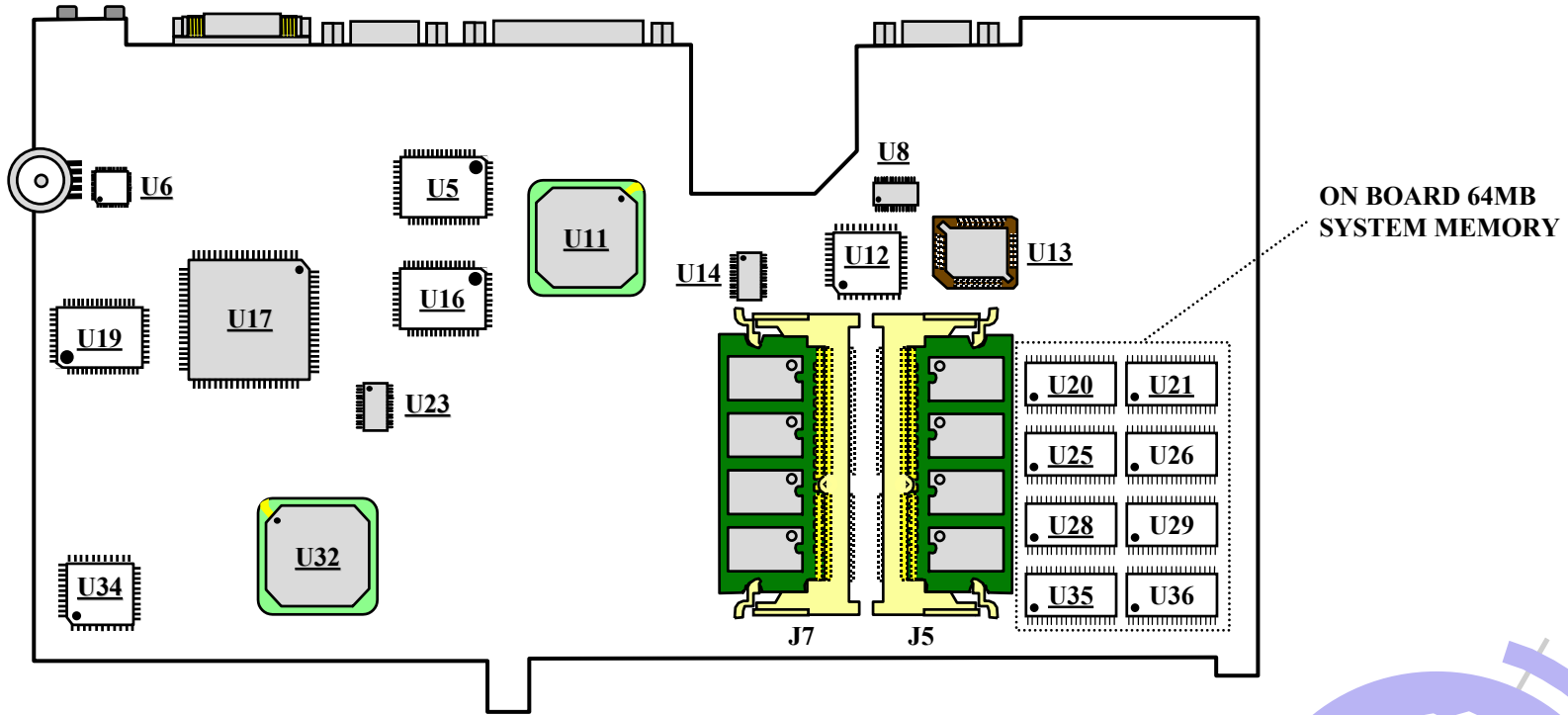
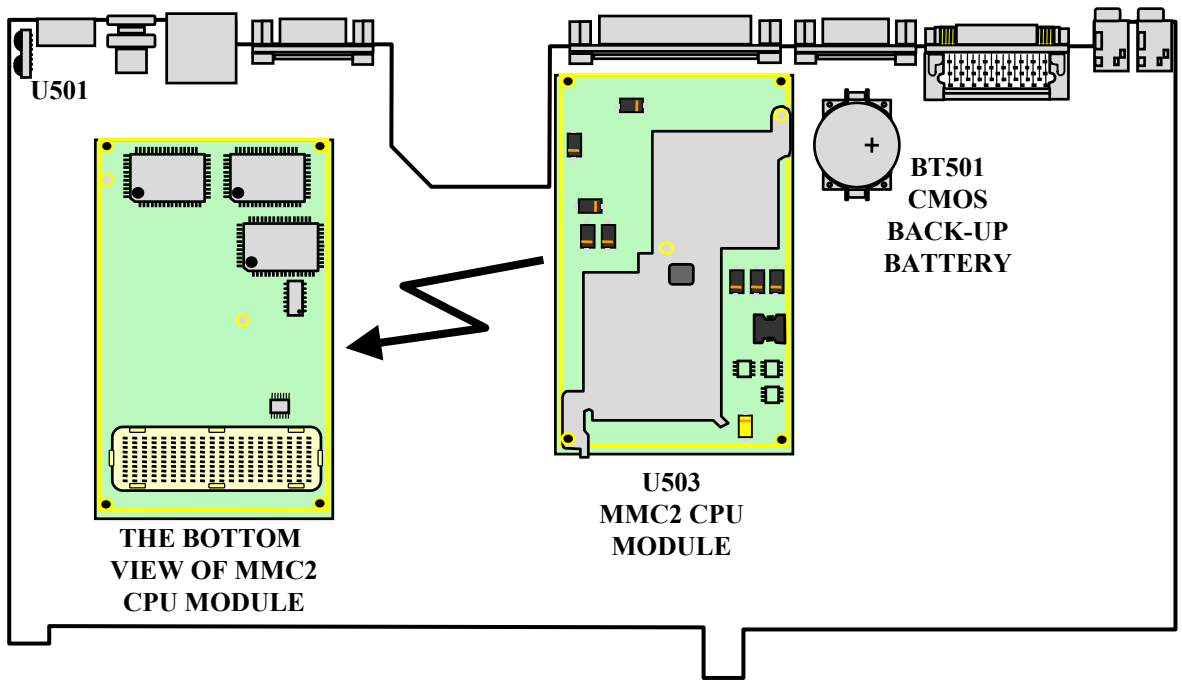
2. LOCATION OF MAJOR COMPONENTS(TOP SIDE)



- U5, U16 : 4MB VIDEO SGRAM.
- U6 : CRYSTAL CS4297 AUDIO CODEC.
- U8 : ADM3311 SIO DRIVE.
- U11 : ATI_RAGE_LTPRO AGP VGA CONTROLLER.
- U12 : PC97338 SUPER I/O CONTROLLER.
- U13 : FLASHABLE SYSTEM BIOS.
- U14 : W40S11 SDRAM CLOCK BUFFER.
- U17 : TI 1225 CARD BUS PCI PCCARD CONTROLLER.
- U19 : CRYSTAL CS4280 PCI AUDIO DRIVE.
- U23 : W137 CLOCK SYNTHESIZER.
- U32 : INTEL PIIX4 FW82371EB PCI/ISA BRIDGE.
- U34 : H8/F3434 KEYBOARD CONTROLLER.
- U20,U21,U25,U26 U28,U29,U35,U36 : ON BOARD 64MB OF SYSTEM MEMORY.
- J5, J7 : 3.3V 144PIN UNBUFFER EXPANSION SDRAM MODULE.

6020 N/B MAINTENANCE

2. LOCATION OF MAJOR COMPONENTS(BOTTOM SIDE)



- U501 : HP FIR MODULE.
- U503 : INTEL MMC2 CPU MODULE.
- UBT501 : CMOS BACK-UP BATTERY.

3. PIN DESCRIPTIONS OF MAJOR COMPONENTS

3.1 INTEL PENTIUM II PROCESSOR MOBILE MODULE (MMC-2) (1).

Memory Signal Descriptions

Name	Type	Description
MECC[7:0]	I/O CMOS	**Memory ECC Data:** These signals carry Memory ECC data during access to DRAM. These pins are implemented by design but not tested on MMC-2.
RASA[5:0]# or CSA[5:0]#	O CMOS	**Row Address Strobe (EDO):** These pins select the DRAM row. **Chip Select (SDRAM):** These pins activate the SDRAMs. SDRAM accepts any command when its CS# pin is active low.
CASA[7:0]# or DQMA[7:0]	O CMOS	**Column Address Strobe (EDO):** These pins select the DRAM column. **Input/Output Data Mask (SDRAM):** These pins act as synchronized output enables during a read cycle and as a byte mask during a write cycle.1
MAB[9:0]# MAB[10] MAB[12:11]# MAB[13]	O CMOS	**Memory Address (EDO/SDRAM):** This is the row and column address for DRAM. The 443BX Host Bridge system controller has two identical sets of address lines (MAA and MAB#). The Pentium®II Processor Mobile Module supports only the MAB set of address lines. For additional addressing features, please refer to the Intel 440BX AGPset datasheet (Order Number 290633-001).2
MWEA#	O CMOS	**Memory Write Enable (EDO/SDRAM):** MWEA# should be used as the write enable for the memory data bus.
SRASA#	O CMOS	**SDRAM Row Address Strobe (SDRAM):** When active low, this signal latches Row Address on the positive edge of the clock. This signal also allows Row access and pre-charge.
SCASA#	O CMOS	**SDRAM Column Address Strobe (SDRAM):** When active low,this signal latches Column Address on the positive edge of the clock. This signal also allows Column access.
CKE[5:0]	O CMOS	**SDRAM Clock Enable (SDRAM):** SDRAM clock enable pin. When these signals are de-asserted, SDRAM enters power-down mode. **Each row is individually controlled by its own clock enable.**
MD[63:0]	I/O CMOS	**Memory Data:** These signals are connected to the DRAM data bus. They are not terminated on the Intel Mobile Module.

NOTES:
1. DQMA signals are non-inverted now. Please refer to 82443BX Spec Update
2. MAB[13] is a non-inverted address signal now. Please refer to 82443BX Spec Update.

AGP Signal Descriptions

Name	Type	Description
GAD[31:0]	I/O AGP	**AGP Address/Data:** The standard AGP address and data lines. This bus functions in the same way as the PCI AD[31:0] bus. The address is driven with FRAME# assertion, and data is driven or received in following clocks.
GC/BE[3:0]#	I/O AGP	**AGP Command/Byte Enable**: This bus carries the command information during AGP cycles when PIPE# is being used. During an AGP write, this bus contains byte enable information. The command is driven with FRAME# assertion, and byte enables corresponding to supplied or requested data are driven on the following clocks.
GFRAME#	I/O AGP	**AGP Frame**: Not used during AGP transactions. Remains deasserted by an internal pullup resistor. Assertion indicates the address phase of a PCI transfer. Negation indicates that one more data transfer is desired by the cycle initiator.
GDEVSEL#	I/O AGP	**AGP Device Select**: Same function as PCI DEVSEL#. Not used during AGP transactions. This signal is driven by the 443BX Host Bridge system controller when a PCI initiator is attempting to access DRAM. DEVSEL# is asserted at medium decode time.
GIRDY#	I/O AGP	**AGP Initiator Ready**: Indicates the AGP compliant target is ready to provide ALL write data for the current transaction. Asserted when the initiator is ready for a data transfer.
GTRDY#	I/O AGP	**AGP Target Ready**: Indicates the AGP compliant master is ready to provide ALL write data for the current transaction. Asserted when the target is ready for a data transfer.
GSTOP#	I/O AGP	**AGP Stop**: Same function as PCI STOP#. Not used during AGP transactions. Asserted by the target to request the master to stop the current transaction.
GREQ#	I AGP	**AGP Request**: AGP master requests for AGP.
GGNT#	O AGP	**AGP Grant**: Same function as on PCI. Additional information is provided on the ST[2:0] bus. PCI Grant: Permission is given to the master to use PCI.

3.1 INTEL PENTIUM II PROCESSOR MOBILE MODULE (MMC-2) (2).

AGP Signal Descriptions

Name	Type	Description
GPAR	I/O AGP	**AGP Parity**: A single parity bit is provided over GAD[31:0] an GC/BE[3:0]. This signal is not used during AGP transactions.
PIPE#	I AGP	**Pipelined Request**: Asserted by the current master to indicate a full width address is to be queued by the target. The master queues one request each rising clock edge while PIPE# is asserted.
SBA[7:0]	I AGP	**Sideband Address**: This bus provides an additional conduit to pass address and commands to the 443BX Host Bridge System Controller from the AGP master.
RBF#	I AGP	**Read Buffer Full**: Indicates if the master is ready to accept previously requested low priority read data.
ST[2:0]	O AGP	**Status Bus**: Provides information from the arbiter to a AGP Master on what it may do. These bits only have meaning when GGNT is asserted.
ADSTB[B:A]	I/O AGP	**AD Bus Strobes**: Provide timing for double clocked data on the GAD bus. The agent that is providing data drives these signals.These are identical copies of each other.
SBSTB	I AGP	**Sideband Strobe**: Provides timing for a side-band bus. It is always driven by the agent driving SBA[7:0], i.e., by the AGP master.

PCI Signal Descriptions

Name	Type	Description
AD[31:0]	I/O PCI	**Address/Data:** The standard PCI address and data lines. The address is driven with FRAME# assertion, and data is driven or received in following clocks.
C/BE[3:0]#	I/O PCI	**Command/Byte Enable:** The command is driven with FRAME# assertion, and byte enables corresponding to supplied or requested data are driven on the following clocks.
FRAME#	I/O PCI	**Frame:** Assertion indicates the address phase of a PCI transfer. Negation indicates that one more data transfers are desired by the cycle initiator.
DEVSEL#	I/O PCI	**Device Select:** This signal is driven by the 443BX Host Bridge when a PCI initiator is attempting to access DRAM. DEVSEL# is asserted at medium decode time.
IRDY#	I/O PCI	**Initiator Ready:** Asserted when the initiator is ready for data transfer.
TRDY#	I/O PCI	**Target Ready:** Asserted when the target is ready for a data transfer.
STOP#	I/OV PCI	**Stop:** Asserted by the target to request the master to stop the current transaction.
PLOCK#	I/O PCI	**Lock:** Indicates an exclusive bus operation and may require multiple transactions to complete. When LOCK# is asserted, non-exclusive transactions may proceed. The 443BX supports lock for CPU initiated cycles only. PCI initiated locked cycles are not supported.
REQ[4:0]#	I PCI	**PCI Request:** PCI master requests for PCI.
GNT[4:0]#	O PCI	**PCI Grant:** Permission is given to the master to use PCI.
PHOLD#	I PCI	**PCI Hold:** This signal comes from the expansion bridge; it is the bridge request for PCI. The 443BX Host Bridge will drain the DRAM write buffers, drain the processor-to-PCI posting buffers, and acquire the host bus before granting the request via PHLDA#. This ensures that GAT timing is met for ISA masters. The PHOLD# protocol has been modified to include support for passive release.
PHLDA#	O PCI	**PCI Hold Acknowledge:** This signal is driven by the 443BX Host Bridge to grant PCI to the expansion bridge. The PHLDA# protocol has been modified to include support for passive release.
PAR	I/O PCI	**Parity:** A single parity bit is provided over AD[31:0] and C/BE[3:0]#

3.1 INTEL PENTIUM II PROCESSOR MOBILE MODULE (MMC-2) (3).

PCI Signal Descriptions

Name	Type	Description
SERR#	I/O PCI	**System Error:** The 443BX asserts this signal to indicate an error condition. Please refer to the Intel 440BX AGPset datasheet (Order Number 290633-001) for further information.
CLKRUN#	I/O D PCI	**Clock Run:** An open-drain output and also an input. The 443BX Host Bridge requests the central resource (PIIX4E) to start or maintain the PCI clock by asserting CLKRUN#. The 443BX Host Bridge tri-states CLKRUN# upon deassertion of Reset (since CLK is running upon deassertion of Reset).
PCI_RST#	I CMOS	**Reset:** When asserted, this signal asynchronously resets the 443BX Host Bridge. The PCI signals also tri-state, compliant with PCI Rev 2.1 specifications.

Processor/PIIX4E Sideband Signal Descriptions

Name	Type	Description
FERR#	O CMOS	**Numeric Coprocessor Error:** This pin functions as a FERR# signal supporting coprocessor errors. This signal is tied to the coprocessor error signal on the processor and is driven by the processor to the PIIX4E.
IGNNE#	I D CMOS	**Ignore Error:** This open drain signal is connected to the ignore error pin on the processor and is driven by the PIIX4E.
INIT#	I D CMOS	**Initialization:** INIT# is asserted by the PIIX4E to the processor for system initialization. This signal is an open drain.
INTR	I D CMOS	**Processor Interrupt:** INTR is driven by the PIIX4E to signal the processor that an interrupt request is pending and needs to be serviced. This signal is an open drain.
NMI	I D CMOS	**Non-Maskable Interrupt:** NMI is used to force a non-maskable interrupt to the processor. The PIIX4E ISA bridge generates an NMI when either SERR# or IOCHK# is asserted, depending on how the NMI Status and Control Register is programmed. This signal is an open drain.
A20M#	I D CMOS	**Address Bit 20 Mask:** When enabled, this open drain signal causes the processor to emulate the address wraparound at one Mbyte which occurs on the Intel 8086 processor.
SMI#	I D CMOS	**System Management Interrupt:** SMI# is an active low synchronous output from the PIIX4E that is asserted in response to one of many enabled hardware or software events. The SMI# open drain signal can be an asynchronous input to the processor. However, in this chip set SMI# is synchronous to PCLK.
STPCLK#	I D CMOS	**Stop Clock:** STPCLK# is an active low synchronous open drain output from the PIIX4E that is asserted in response to one of many hardware or software events. STPCLK# connects directly to the processor and is synchronous to PCICLK. When the processor samples STPCLK# asserted it responds by entering a low power state (Quick Start). The processor will only exit this mode when this signal is de-asserted.

Power Management/Geyserville Signal Descriptions

Name	Type	Description
SUS_STAT1#	I CMOS	**Suspend Status:** This signal connects to the SUS_STAT1# output of PIIX4E. It provides information on host clock status and is asserted during all suspend states.
VR_ON	I CMOS	**VR_ON:** Voltage regulator ON. This 3.3V (5V tolerant) signal controls the operation of the Intel Mobile Module's voltage regulator. VR_ON should be generated as a function of the PIIX4E SUSB# signal which is used for controlling the "Suspend State B" voltage planes.
VR_PWRGD	O	**VR_PWRGD:** This signal is driven high by the Intel Mobile Module to indicate the voltage regulator is stable and is pulled low using a 131.6K resistor when inactive. It can be used in some combination to generate the system PWRGOOD signal.
BXPWROK	I CMOS	**Power OK to BX:** This signal must go active 1mS after the V_3 power rail is stable.
SM_CLK	I/O D CMOS	**Serial Clock:** This clock signal is used on the SMBUS interface to the digital thermal sensor.

3.1 INTEL PENTIUM II PROCESSOR MOBILE MODULE (MMC-2) (4).

Name	Type	Description
SM_DATA	I/O D CMOS	**Serial Data:** Open-drain data signal on the SMBUS interface to the digital thermal sensor.
ATF_INT#	O D CMOS	**ATF Interrupt:** This signal is an open-drain output signal of the digital thermal sensor.
G_SUS_STAT1#	I CMOS	**G_SUS_STAT1#:** The SUS_STST1# signal gated by the Geyserville control logic. G_SUS_STAT1# should be used in place of the SUS_STAT1# signal in the system electronics design. This signal is not implemented on the current Intel Mobile Modules, and is defined for future upgrade ability purposes only.
G_LO/HI#	I CMOS	New signal from a PIIX4E GPIO pin that defines entry into a Geyserville state change to the Geyserville control logic.
G_CPU_STP#	I CMOS	The CPU_STP# signal gated by the Geyserville control logic.
VRChgng#	O CMOS	A Geyserville control logic signal that indicates that the actual state change is in progress. The VR setpoint has changed and the VR is settling. When this signal de-asserts the new state is sent to the processor. System electronics will use this signal to generate an SCI to force a transition out of deep sleep.

NOTE:
* **V**_3ALWAYS: 3.3V voltage supply. It is generated whenever V_DC is available and supplied to PIIX4E resume well.

Miscellaneous Pins

Name	Type	Description
Module ID[3:0]	O CMOS	**Module Revision ID**: These pins track the revision level of the processor module. A 100K pull up resistor to V_3S is required on these signals and to be placed on the system electronics for these signals.
Ground	I	Ground
Reserved	RSVD	Unallocated Reserved pins and should not be connected.

Clock Signal Descriptions

Name	Type	Description
PCLK	I PCI	**PCI Clock In:** PCLK is an input to the module is one of the system's PCI clocks. This clock is used by all of the 443BX Host Bridge logic in the PCI clock domain. This clock is stopped when the PIIX4E PCI_STP# signal is asserted and/or during all suspend states.
HCLK[1:0]	I CMOS	**Host Clock In:** Only HCLK0 is an input to the MMC-2 module from the CK100-M clock source and is used by the processor and 443BX Host Bridge system controller. HCLK0 is the only clock input supplied to the module. This clock is stopped when the PIIX4E CPU_STP# signal is asserted and/or during all suspend states.
DCLKO	O CMOS	**SDRAM Clock Out:** 66 MHz SDRAM clock reference generated internally by the 443BX Host Bridge system controller onboard PLL. It feeds an external buffer that produces multiple copies for the SODIMMs.
DCLKRD	I CMOS	**SDRAM Read Clock:** Feedback reference from the SDRAM clock buffer. This clock is used by 443BX Host Bridge System Controller when reading data from the SDRAM array.
DCLKWR	I CMOS	**SDRAM Write Clock:** Feedback reference from the SDRAM clock buffer. This clock is used by the 443BX Host Bridge system controller when writing data to the SDRAM array.
GCLKIN	I CMOS	**AGP Clock In:** The GCLKIN input is a feedback reference from the GCLKO signal.
GCLKO	O CMOS	**AGP Clock Out:** This signal is generated by the 443BX Host Bridge system controller onboard PLL from the HCLK0 host clock reference. The frequency of GCLKO is 66 MHz. The GCLKO output is used to feed both the PLL reference input pin on the 443BX Host Bridge system controller and the AGP device. The board layout must maintain complete symmetry on loading and trace geometry to minimize AGP clock skew.
FQS	O CMOS	**Frequency Select:** This output indicates the desired host clock frequency for the module. FQS=0 indicates 66 MHz **FQS=1 indicates RESERVED**

3.1 INTEL PENTIUM II PROCESSOR MOBILE MODULE (MMC-2) (5).

Voltage Descriptions

Name	Type	Description
V_DC	I	**DC Input:** 5 - 21V
V_3S	I	**SUSB# controlled 3.3V:** Power-managed 3.3V voltage supply. An output of the voltage regulator on the system electronics. This rail is off during STR, STD, and Soff.
V_5	I	**SUSC# controlled 5V:** Power-managed 5V voltage supply. An output of the voltage regulator on the system electronics. This rail is off during STD and Soff.
V_3	I	**SUSC# controlled 3.3V:** Power-managed 3.3V voltage supply. An output of the voltage regulator on the system electronics. This rail is off during STD and Soff.
VCCAGP	I	**AGP I/O Voltage**: For this revision of the module, this rail must be connected to V_3.
V_CPUPU	O	**Processor I/O Ring:** Driven by the Intel Mobile Module to power processor interface signals such as the PIIX4E open-drain pullups for the processor/PIIX4E sideband signals.
V_CLK	O	**Processor Clock Rail:** Driven by the Intel Mobile Module to power CK100-M VDDCPU rail.

ITP/JTAG Pins

Name	Type	Description
TDO	O	**JTAG Test Data Out:** Serial output port. TAP instructions and data are shifted out of the processor from this port.
TDI	I	**JTAG Test Data In:** Serial input port. TAP instructions and data are shifted into the processor from this port.
TMS	I	**JTAG Test Mode Select:** Controls the TAP controller change sequence.
TCLK	I	**JTAG Test Clock:** Testability clock for clocking the JTAG boundary scan sequence.
TRST#	I	**JTAG Test Reset:** Asynchronously resets the TAP controller in the processor.
FS_RESET#	O	**Processor Reset: Processor** reset status to the ITP.
VTT	O	**GTL+ Termination Voltage:** Used by the POWERON pin on the ITP debug port to determine when target system is on. POWERON pin is pulled up using a 1KΩ resistor to VTT.
FS_PREQ#	I	**Debug Mode Request:** Driven by the ITP - makes request to enter debug mode.
FS_PRDY#	O	**Debug Mode Ready:** Driven by the processor - informs the ITP that the processor is in debug mode.

NOTE:
Recommendation: DBREST# (reset target system) on the ITP debug port can be “logically AND’ed” with the signal VR_PWRGD and connected to the PIIX4E input PWROK.

New Pins in the Mobile Pentium® II Processor

Name	Type	Description
SMBALERT#	O	Thermal sensor attention signal.
SMBCLK	I/O	SMBus clock signal. Refer to the System Management Bus Specification for descriptions and specifications of the three SMBus signals.
SMBDATA	I/O	SMBus data signal. Refer to the System Management Bus Specification for descriptions and specifications of the three SMBus signals.

3.2 INTEL 82371EB PCI-TO-ISA / IDE XCELERATOR (PIIX4) (1).

SIGNAL	TYPE	DESCRIPTION
AD[31:0]	I/O	**PCI ADDRESS/DATA.** AD[31:0] is a multiplexed address and data bus. During the first clock of a transaction, AD[31:0] contain a physical byte address (32 bits).During subsequent clocks, AD[31:0] contain data. A PIIX4 Bus transaction consists of an address phase followed by one or more data phases. Little-endian byte ordering is used. AD[7:0] define the least significant byte (LSB) and AD[31:24] the most significant byte (MSB). When PIIX4 is a Target, AD[31:0] are inputs during the address phase of a transaction. During the following data phase(s), PIIX4 may be asked to supply data on AD[31:0] for a PCI read, or accept data for a PCI write. As an Initiator, PIIX4 drives a valid address on AD[31:2] and 0 on AD[1:0] during the address phase, and drives write or latches read data on AD[31:0] during the data phase. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
C/BE#[3:0]	I/O	**BUS COMMAND AND BYTE ENABLES.** The command and byte enable signals are multiplexed on the same PCI pins. During the address phase of a transaction, C/BE[3:0]# define the bus command. During the data phase C/BE[3:0]# are used as Byte Enables. The Byte Enables determine which byte lanes carry meaningful data. C/BE0# applies to byte 0, C/BE1# to byte 1, etc. PIIX4 drives C/BE[3:0]# as an Initiator and monitors C/BE[3:0]# as a Target. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
CLKRUN#	I/O	**CLOCK RUN#.** This signal is used to communicate to PCI peripherals that the PCI clock will be stopped. Peripherals can assert CLKRUN# to request that the PCI clock be restarted or to keep it from stopping. This function follows the protocol described in the PCI Mobile Design Guide, Revision 1.0. **During Reset:** Low **After Reset:** Low **During POS:** High
DEVSEL#	I/O	**DEVICE SELECT.** PIIX4 asserts DEVSEL# to claim a PCI transaction through positive decoding or subtractive decoding (if enabled). As an output, PIIX4 asserts DEVSEL# when it samples IDSEL active in configuration cycles to PIIX4 configuration registers. PIIX4 also asserts DEVSEL# when an internal PIIX4 address is decoded or when PIIX4 subtractively or positively decodes a cycle for the ISA/EIO bus or IDE device. As an input, DEVSEL# indicates the response to a PIIX4 initiated transaction and is also sampled when deciding whether to subtractively decode the cycle. DEVSEL# is tri-stated from the leading edge of PCIRST#. DEVSEL# remains tri-stated until driven by PIIX4 as a target. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
FRAME#	I/O	**CYCLE FRAME.** FRAME# is driven by the current Initiator to indicate the beginning and duration of an access. While FRAME# is asserted data transfers continue. When FRAME# is negated the transaction is in the final data phase. FRAME# is an input to PIIX4 when it is the Target. FRAME# is an output when PIIX4 is the initiator. FRAME# remains tri-stated until driven by PIIX4 as an Initiator. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
IRDY#	I/O	**INITIATOR READY.** IRDY# indicates PIIX4□ ability, as an Initiator, to complete the current data phase of the transaction. It is used in conjunction with TRDY#. A data phase is completed on any clock both IRDY# and TRDY# are sampled asserted. During a write, IRDY# indicates PIIX4 has valid data present on AD[31:0]. During a read, it indicates PIIX4 is prepared to latch data. IRDY# is an input to PIIX4 when PIIX4 is the Target and an output when PIIX4 is an Initiator. IRDY# remains tri-stated until driven by PIIX4 as a master.

SIGNAL	TYPE	DESCRIPTION
IDSEL	I	**INITIALIZATION DEVICE SELECT.** IDSEL is used as a chip select during PCI configuration read and write cycles. PIIX4 samples IDSEL during the address phase of a transaction. If IDSEL is sampled active, and the bus command is a configuration read or write, PIIX4 responds by asserting DEVSEL# on the next cycle. **PAR O CALCULATED PARITY SIGNAL.** PAR is □ven?parity and is calculated on 36 bits; AD[31:0] plus C/BE[3:0]#. □ven?parity means that the number of ?□ within the 36 bits plus PAR are counted and the sum is always even. PAR is always calculated on 36 bits regardless of the valid byte enables. PAR is generated for address and data phases and is only guaranteed to be valid one PCI clock after the corresponding address or data phase. PAR is driven and tri-stated identically to the AD[31:0] lines except that PAR is delayed by exactly one PCI clock. PAR is an output during the address phase (delayed one clock) for all PIIX4 initiated transactions. It is also an output during the data phase (delayed one clock) when PIIX4 is the Initiator of a PCI write transaction, and when it is the Target of a read transaction. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
PCIRST#	O	**PCI RESET.** PIIX4 asserts PCIRST# to reset devices that reside on the PCI bus. PIIX4 asserts PCIRST# during power-up and when a hard reset sequence is initiated through the RC register. PCIRST# is driven inactive a minimum of 1 ms after PWROK is driven active. PCIRST# is driven for a minimum of 1 ms when initiated through the RC register. PCIRST# is driven asynchronously relative to PCICLK. **During Reset:** Low **After Reset:** High **During POS:** High
PHOLD#	O	**PCI HOLD.** An active low assertion indicates that PIIX4 desires use of the PCI Bus. Once the PCI arbiter has asserted PHLDA# to PIIX4, it may not negate it until PHOLD# is negated by PIIX4. PIIX4 implements the passive release mechanism by toggling PHOLD# inactive for one PCICLK. **During Reset:** High-Z **After Reset:** High **During POS:** High
PHLDA#	I	**PCI HOLD ACKNOWLEDGE.** An active low assertion indicates that PIIX4 has been granted use of the PCI Bus. Once PHLDA# is asserted, it cannot be negated unless PHOLD# is negated first.
SERR#	I/O	**SYSTEM ERROR.** SERR# can be pulsed active by any PCI device that detects a system error condition. Upon sampling SERR# active, PIIX4 can be programmed to generate a non-maskable interrupt (NMI) to the CPU. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
STOP#	I/O	**STOP.** STOP# indicates that PIIX4, as a Target, is requesting an initiator to stop the current transaction. As an Initiator, STOP# causes PIIX4 to stop the current transaction. STOP# is an output when PIIX4 is a Target and an input when PIIX4 is an Initiator. STOP# is tri-stated from the leading edge of PCIRST#. STOP# remains tri-stated until driven by PIIX4 as a slave. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
TRDY#	I/O	**TARGET READY.** TRDY# indicates PIIX4□ ability to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#. A data phase is completed when both TRDY# and IRDY# are sampled asserted. During a read, TRDY# indicates that PIIX4, as a Target, has place valid data on AD[31:0]. During a write, it indicates PIIX4, as a Target is prepared to latch data. TRDY# is an input to PIIX4 when PIIX4 is the Initiator and an output when PIIX4 is a Target. TRDY# is tri-stated from the leading edge of PCIRST#. TRDY# remains tri-stated until driven by PIIX4 as a slave. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z

3.2 INTEL 82371EB PCI-TO-ISA / IDE XCELERATOR (PIIX4) (2).

SIGNAL	TYPE	DESCRIPTION
AEN	O	**ADDRESS ENABLE.** AEN is asserted during DMA cycles to prevent I/O slaves from misinterpreting DMA cycles as valid I/O cycles. When negated, AEN indicates that an I/O slave may respond to address and I/O commands. When asserted, AEN informs I/O resources on the ISA bus that a DMA transfer is occurring. This signal is also driven high during PIIX4 initiated refresh cycles. **During Reset:** High-Z **After Reset:** Low **During POS:** Low
BALE	O	**BUS ADDRESS LATCH ENABLE.** BALE is asserted by PIIX4 to indicate that the address (SA[19:0], LA[23:17]) and SBHE# signal lines are valid. The LA[23:17] address lines are latched on the trailing edge of BALE. BALE remains asserted throughout DMA and ISA master cycles. **During Reset:** High-Z **After Reset:** Low **During POS:** Low
IOCHK#/ GPI0	I	**I/O CHANNEL CHECK.** IOCHK# can be driven by any resource on the ISA bus. When asserted, it indicates that a parity or an uncorrectable error has occurred for a device or memory on the ISA bus. A NMI will be generated to the CPU if the NMI generation is enabled. If the EIO bus is used, this signal becomes a general purpose input.
IOCHRDY	I/O	**I/O CHANNEL READY.** Resources on the ISA Bus negate IOCHRDY to indicate that wait states are required to complete the cycle. This signal is normally high. IOCHRDY is an input when PIIX4 owns the ISA Bus and the CPU or a PCI agent is accessing an ISA slave, or during DMA transfers. IOCHRDY is output when an external ISA Bus Master owns the ISA Bus and is accessing DRAM or a PIIX4 register. As a PIIX4 output, IOCHRDY is driven inactive (low) from the falling edge of the ISA commands. After data is available for an ISA master read or PIIX4 latches the data for a write cycle, IOCHRDY is asserted for 70 ns. After 70 ns, PIIX4 floats IOCHRDY. The 70 ns includes both the drive time and the time it takes PIIX4 to float IOCHRDY. PIIX4 does not drive this signal when an ISA Bus master is accessing an ISA Bus slave. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
IOCS16#	I	**16-BIT I/O CHIP SELECT.** This signal is driven by I/O devices on the ISA Bus to indicate support for 16-bit I/O bus cycles.
IOR#	I/O	**I/O READ.** IOR# is the command to an ISA I/O slave device that the slave may drive data on to the ISA data bus (SD[15:0]). The I/O slave device must hold the data valid until after IOR# is negated. IOR# is an output when PIIX4 owns the ISA Bus. IOR# is an input when an external ISA master owns the ISA Bus. **During Reset:** High-Z **After Reset:** High **During POS:** High
IOW#	I/O	**I/O WRITE.** IOW# is the command to an ISA I/O slave device that the slave may latch data from the ISA data bus (SD[15:0]). IOW# is an output when PIIX4 owns the ISA Bus. IOW# is an input when an external ISA master owns the ISA Bus. **During Reset:** High-Z **After Reset:** High **During POS:** High
LA[23:17]/ GPO[7:1]	I/O	**ISA LA[23:17].** LA[23:17] address lines allow accesses to physical memory on the ISA Bus up to 16 Mbytes. LA[23:17] are outputs when PIIX4 owns the ISA Bus. The LA[23:17] lines become inputs whenever an ISA master owns the ISA Bus. If the EIO bus is used, these signals become a general purpose output. **During Reset:** High-Z **After Reset:** Undefined **During POS:** Last LA/GPO
MEMCS16#	I/O	**MEMORY CHIP SELECT 16.** MEMCS16# is a decode of LA[23:17] without any qualification of the command signal lines. ISA slaves that are 16-bit memory devices drive this signal low. PIIX4 ignores MEMCS16# during I/O access cycles and refresh cycles. MEMCS16# is an input when PIIX4 owns the ISA Bus. PIIX4 drives this signal low during ISA master to PCI memory cycles.

SIGNAL	TYPE	DESCRIPTION
MEMR#	I/O	**MEMORY READ.** MEMR# is the command to a memory slave that it may drive data onto the ISA data bus. MEMR# is an output when PIIX4 is a master on the ISA Bus. MEMR# is an input when an ISA master, other than PIIX4, owns the ISA Bus. This signal is also driven by PIIX4 during refresh cycles. For DMA cycles, PIIX4, as a master, asserts MEMR#. **During Reset:** High-Z **After Reset:** High **During POS:** High
MEMW#	I/O	**MEMORY WRITE.** MEMW# is the command to a memory slave that it may latch data from the ISA data bus. MEMW# is an output when PIIX4 owns the ISA Bus. MEMW# is an input when an ISA master, other than PIIX4, owns the ISA Bus. For DMA cycles, PIIX4, as a master, asserts MEMW#. **During Reset:** High-Z **After Reset:** High **During POS:** High
REFRESH#	I/O	**REFRESH.** As an output, REFRESH# is used by PIIX4 to indicate when a refresh cycle is in progress. It should be used to enable the SA[7:0] address to the row address inputs of all banks of dynamic memory on the ISA Bus. Thus, when MEMR# is asserted, the entire expansion bus dynamic memory is refreshed. Memory slaves must not drive any data onto the bus during refresh. As an output, this signal is driven directly onto the ISA Bus. This signal is an output only when PIIX4 DMA refresh controller is a master on the bus responding to an internally generated request for refresh. As an input, REFRESH# is driven by 16-bit ISA Bus masters to initiate refresh cycles. **During Reset:** High-Z **After Reset:** High **During POS:** High
RSTDRV	O	**RESET DRIVE.** PIIX4 asserts RSTDRV to reset devices that reside on the ISA/EIO Bus. PIIX4 asserts this signal during a hard reset and during power-up. RSTDRV is asserted during power-up and negated after PWROK is driven active. RSTDRV is also driven active for a minimum of 1 ms if a hard reset has been programmed in the RC register. **During Reset:** High **After Reset:** Low **During POS:** Low
SA[19:0]	I/O	**SYSTEM ADDRESS[19:0].** These bi-directional address lines define the selection with the granularity of 1 byte within the 1-Megabyte section of memory defined by the LA[23:17] address lines. The address lines SA[19:17] that are coincident with LA[19:17] are defined to have the same values as LA[19:17] for all memory cycles. For I/O accesses, only SA[15:0] are used, and SA[19:16] are undefined. SA[19:0] are outputs when PIIX4 owns the ISA Bus. SA[19:0] are inputs when an external ISA Master owns the ISA Bus. **During Reset:** High-Z **After Reset:** Undefined **During POS:** Last SA
SBHE#	I/O	**SYSTEM BYTE HIGH ENABLE.** SBHE# indicates, when asserted, that a byte is being transferred on the upper byte (SD[15:8]) of the data bus. SBHE# is negated during refresh cycles. SBHE# is an output when PIIX4 owns the ISA Bus. SBHE# is an input when an external ISA master owns the ISA Bus. **During Reset:** High-Z **After Reset:** Undefined **During POS:** High
SD[15:0]	I/O	**SYSTEM DATA.** SD[15:0] provide the 16-bit data path for devices residing on the ISA Bus. SD[15:8] correspond to the high order byte and SD[7:0] correspond to the low order byte. SD[15:0] are undefined during refresh. **During Reset:** High-Z **After Reset:** Undefined **During POS:** High-Z
SMEMR#	O	**STANDARD MEMORY READ.** PIIX4 asserts SMEMR# to request an ISA memory slave to drive data onto the data lines. If the access is below the 1-Mbyte range (00000000h?00FFFFFh) during DMA compatible, PIIX4 master, or ISA master cycles, PIIX4 asserts SMEMR#. SMEMR# is a delayed version of MEMR#.

3.2 INTEL 82371EB PCI-TO-ISA / IDE XCELERATOR (PIIX4) (3).

SIGNAL	TYPE	DESCRIPTION
SMEMW#	O	**STANDARD MEMORY WRITE.** PIIX4 asserts SMEMW# to request an ISA memory slave to accept data from the data lines. If the access is below the 1-Mbyte range (00000000h?00FFFFFh) during DMA compatible, PIIX4 master, or ISA master cycles, PIIX4 asserts SMEMW#. SMEMW# is a delayed version of MEMW#. **During Reset:** High-Z **After Reset:** High **During POS:** High
ZEROWS#	I	**ZERO WAIT STATES.** An ISA slave asserts ZEROWS# after its address and command signals have been decoded to indicate that the current cycle can be shortened. A 16-bit ISA memory cycle can be reduced to two SYSCLKs. An 8-bit memory or I/O cycle can be reduced to three SYSCLKs. ZEROWS# has no effect during 16-bit I/O cycles. If IOCHRDY is negated and ZEROWS# is asserted during the same clock, then ZEROWS# is ignored and wait states are added as a function of IOCHRDY.
A20GATE	I	**ADDRESS 20 GATE.** This input from the keyboard controller is logically combined with bit 1 (FAST_A20) of the Port 92 Register, which is then output via the A20M# signal.
BIOSCS#	O	**BIOS CHIP SELECT.** This chip select is driven active during read or write accesses to enabled BIOS memory ranges. BIOSCS# is driven combinatorially from the ISA addresses SA[16:0] and LA[23:17], except during DMA cycles. During DMA cycles, BIOSCS# is not generated. **During Reset:** High **After Reset:** High **During POS:** High
KBCCS#/ GPO26	O	**KEYBOARD CONTROLLER CHIP SELECT.** KBCCS# is asserted during I/O read or write accesses to KBC locations 60h and 64h. It is driven combinatorially from the ISA addresses SA[19:0] and LA[23:17]. If the keyboard controller does not require a separate chip select, this signal can be programmed to a general purpose output. **During Reset:** High **After Reset:** High **During POS:** High/GPO
MCCS#	O	**MICROCONTROLLER CHIP SELECT.** MCCS# is asserted during I/O read or write accesses to IO locations 62h and 66h. It is driven combinatorially from the ISA addresses SA[19:0] and LA[23:17]. **During Reset:** High **After Reset:** High **During POS:** High
PCS0# PCS1#	O	**PROGRAMMABLE CHIP SELECTS.** These active low chip selects are asserted for ISA I/O cycles which are generated by PCI masters and which hit the programmable I/O ranges defined in the Power Management section. The X-Bus buffer signals (XOE# and XDIR#) are enabled while the chip select is active. (i.e., it is assumed that the peripheral which is selected via this pin resides on the X-Bus.) **During Reset:** High **After Reset:** High **During POS:** High
RCIN#	I	**RESET CPU.** This signal from the keyboard controller is used to generate an INIT signal to the CPU.
RTCALE/ GPO25	O	**REAL TIME CLOCK ADDRESS LATCH ENABLE.** RTCALE is used to latch the appropriate memory address into the RTC. A write to port 70h with the appropriate RTC memory address that will be written to or read from causes RTCALE to be asserted. RTCALE is asserted on falling IOW# and remains asserted for two SYSCLKs. If the internal Real Time Clock is used, this signal can be programmed as a general purpose output.
RTCCS#/ GPO24	O	**REAL TIME CLOCK CHIP SELECT.** RTCCS# is asserted during read or write I/O accesses to RTC location 71h. RTCCS# can be tied to a pair of external OR gates to generate the real time clock read and write command signals. If the internal Real Time Clock is used, this signal can be programmed as a general purpose output. **During Reset:** High **After Reset:** High **During POS:** High/GPO

SIGNAL	TYPE	DESCRIPTION
XDIR#/ GPO22	O	**X-BUS TRANSCEIVER DIRECTION.** XDIR# is tied directly to the direction control of a 74?45 that buffers the X-Bus data, XD[7:0]. XDIR# is asserted (driven low) for all I/O read cycles regardless if the accesses is to a PIIX4 supported device. XDIR# is asserted for memory cycles only if BIOS or APIC space has been decoded. For PCI master initiated read cycles, XDIR# is asserted from the falling edge of either IOR# or MEMR# (from MEMR# only if BIOS or APIC space has been decoded), depending on the cycle type. For ISA master-initiated read cycles, XDIR# is asserted from the falling edge of either IOR# or MEMR# (from MEMR# only if BIOS space has been decoded), depending on the cycle type. When the rising edge of IOR# or MEMR# occurs, PIIX4 negates XDIR#. For DMA read cycles from the X-Bus, XDIR# is driven low from DACKx# falling and negated from DACKx# rising. At all other times, XDIR# is negated high. If the X-Bus not used, then this signal can be programmed to be a general purpose output. **During Reset:** High **After Reset:** High **During POS:** High/GPO
XOE#/ GPO23	O	**X-BUS TRANSCEIVER OUTPUT ENABLE.** XOE# is tied directly to the output enable of a 74?45 that buffers the X-Bus data, XD[7:0], from the system data bus, SD[7:0]. XOE# is asserted anytime a PIIX4 supported X-Bus device is decoded, and the devices decode is enabled in the X-Bus Chip Select Enable Register (BIOSCS#, KBCCS#, RTCCS#, MCCS#) or the Device Resource B (PCCS0#) and Device Resource C (PCCS1#). XOE# is asserted from the falling edge of the ISA commands (IOR#, IOW#, MEMR#, or MEMW#) for PCI Master and ISA master-initiated cycles. XOE# is negated from the rising edge of the ISA command signals for PCI Master initiated cycles and the SA[16:0] and LA[23:17] address for ISA master-initiated cycles. XOE# is not generated during any access to an X-Bus-peripheral in which its decode space has been disabled. If an X-Bus not used, then this signal can be programmed to be a general purpose output. **During Reset:** High **After Reset:** High **During POS:** High/GPO
DACK[0,1,2,3]# DACK[5,6,7]#	O	**DMA ACKNOWLEDGE.** The DACK# output lines indicate that a request for DMA service has been granted by PIIX4 or that a 16-bit master has been granted the bus. The active level (high or low) is programmed via the DMA Command Register. These lines should be used to decode the DMA slave device with the IOR# or IOW# line to indicate selection. If used to signal acceptance of a bus master request, this signal indicates when it is legal to assert MASTER#. If the DREQ goes inactive prior to DACK# being asserted, the DACK# signal will not be asserted. **During Reset:** High **After Reset:** High **During POS:** High
DREQ[0,1,2,3] DREQ[5,6,7]	I	**DMA REQUEST.** The DREQ lines are used to request DMA service from PIIX4 DMA controller or for a 16-bit master to gain control of the ISA expansion bus. The active level (high or low) is programmed via the DMA Command Register. All inactive to active edges of DREQ are assumed to be asynchronous. The request must remain active until the appropriate DACKx# signal is asserted.
REQ[A:C]#/ GPI[2:4]	I	**PC/PCI DMA REQUEST.** These signals are the DMA requests for PC/PCI protocol. They are used by a PCI agent to request DMA services and follow the PCI Expansion Channel Passing protocol as defined in the *PCI DMA* section. If the PC/PCI request is not needed, these pins can be used as general-purpose inputs.

3.2 INTEL 82371EB PCI-TO-ISA / IDE XCELERATOR (PIIX4) (4).

SIGNAL	TYPE	DESCRIPTION
GNT[A:C]#/ GPO[9:11]	O	**PC/PCI DMA ACKNOWLEDGE.** These signals are the DMA grants for PC/PCI protocol. They are used by a PIIX4 to acknowledge DMA services and follow the PCI Expansion Channel Passing protocol as defined in the *PCI DMA* section. If the PC/PCI request is not needed, these pins can be used as general-purpose outputs. **During Reset:** High **After Reset:** High **During POS:** High/GPO
TC	O	**TERMINAL COUNT.** PIIX4 asserts TC to DMA slaves as a terminal count indicator. PIIX4 asserts TC after a new address has been output, if the byte count expires with that transfer. TC remains asserted until AEN is negated, unless AEN is negated during an autoinitialization. TC is negated before AEN is negated during an autoinitialization. **During Reset:** Low **After Reset:** Low **During POS:** Low
APICACK#/ GPO12	O	**APIC ACKNOWLEDGE.** This active low output signal is asserted by PIIX4 after its internal buffers are flushed in response to the APICREQ# signal. When the I/O APIC samples this signal asserted it knows that PIIX4 buffers are flushed and that it can proceed to send the APIC interrupt. The APICACK# output is synchronous to PCICLK. If the external APIC is not used, then this is a general-purpose output. **During Reset:** High **After Reset:** High **During POS:** High/GPO
APICCS#/ GPO13	O	**APIC CHIP SELECT.** This active low output signal is asserted when the APIC Chip Select is enabled and a PCI originated cycle is positively decoded within the programmed I/O APIC address space. If the external APIC is not used, this pin is a general-purpose output. **During Reset:** High **After Reset:** High **During POS:** High/GPO
APICREQ#/ GPI5	I	**APIC REQUEST.** This active low input signal is asserted by an external APIC device prior to sending an interrupt over the APIC serial bus. When PIIX4 samples this pin active it will flush its F-type DMA buffers pointing towards PCI. Once the buffers are flushed, PIIX4 asserts APICACK# which indicates to the external APIC that it can proceed to send the APIC interrupt. The APICREQ# input must be synchronous to PCICLK. If the external APIC is not used, this pin is a general-purpose input. **INTR** OD **INTERRUPT.** See CPU Interface Signals.
IRQ0/ GPO14	O	**INTERRUPT REQUEST 0.** This output reflects the state of the internal IRQ0 signal from the system timer. If the external APIC is not used, this pin is a general-purpose output. **During Reset:** Low **After Reset:** Low **During POS:** IRQ0/GPO **IRQ1** I **INTERRUPT REQUEST 1.** IRQ1 is always edge triggered and can not be modified by software to level sensitive. A low to high transition on IRQ1 is latched by PIIX4. IRQ1 must remain asserted until after the interrupt is acknowledged. If the input goes inactive before this time, a default IRQ7 is reported in response to the interrupt acknowledge cycle.
IRQ 3:7, 9:11,14:15	I	**INTERRUPT REQUESTS 3:7, 9:11, 14:15.** The IRQ signals provide both system board components and ISA Bus I/O devices with a mechanism for asynchronously interrupting the CPU. These interrupts may be programmed for either an edge sensitive or a high level sensitive assertion mode. Edge sensitive is the default configuration.An active IRQ input must remain asserted until after the interrupt is acknowledged. If the input goes inactive before this time, a default IRQ7 is reported in response to the interrupt acknowledge cycle.

SIGNAL	TYPE	DESCRIPTION
IRQ8#/ GPI6	I/O	**IRQ 8#.** IRQ8# is always an active low edge triggered interrupt and can not be modified by software. IRQ8# must remain asserted until after the interrupt is acknowledged. If the input goes inactive before this time, a default IRQ7 is reported in response to the interrupt acknowledge cycle. If using the internal RTC, then this can be programmed as a general-purpose input. If enabling an APIC, this signal becomes an output and must not be programmed as a general purpose input.
IRQ9OUT#/ GPO29	O	**IRQ9OUT#.** IRQ9OUT# is used to route the internally generated SCI and SMBus interrupts out of the PIIX4 for connection to an external IO APIC. If APIC is disabled, this signal pin is a General Purpose Output. **During Reset:** High **After Reset:** High **During POS:** IRQ9OUT#/GPO
IRQ 12/M	I	**INTERRUPT REQUEST 12.** In addition to providing the standard interrupt function as described in the pin description for IRQ[3:7,9:11,14:15], this pin can also be programmed to provide the mouse interrupt function. When the mouse interrupt function is selected, a low to high transition on this signal is latched by PIIX4 and an INTR is generated to the CPU as IRQ12. An internal IRQ12 interrupt continues to be generated until a Reset or an I/O read access to address 60h (falling edge of IOR#) is detected.
PIRQ[A:D]#	I/OD PCI	**PROGRAMMABLE INTERRUPT REQUEST.** The PIRQx# signals are active low, level sensitive, shareable interrupt inputs. They can be individually steered to ISA interrupts IRQ [3:7,9:12,14:15]. The USB controller uses PIRQD# as its output signal.
SERIRQ/ GPI7	I/O	**SERIAL INTERRUPT REQUEST.** Serial interrupt input decoder, typically used in conjunction with the Distributed DMA protocol. If not using serial interrupts, this pin can be used as a general-purpose input.
A20M#	OD	**ADDRESS 20 MASK.** PIIX4 asserts A20M# to the CPU based on combination of Port 92 Register, bit 1 (FAST_A20), and A20GATE input signal. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
CPURST	OD	**CPU RESET.** PIIX4 asserts CPURST to reset the CPU. PIIX4 asserts CPURST during power-up and when a hard reset sequence is initiated through the RC register. CPURST is driven inactive a minimum of 2 ms after PWROK is driven active. CPURST is driven active for a minimum of 2 ms when initiated through the RC register. The inactive edge of CPURST is driven synchronously to the rising edge of PCICLK. If a hard reset is initiated through the RC register, PIIX4 resets its internal registers (in both core and suspend wells) to their default state. This signal is active high for Pentium processor and active-low for Pentium II processor as determined by CONFIG1 signal. For values **During Reset**, **After Reset**, and **During POS**, see the *Suspend/Resume and Resume Control Signaling* section.
FERR#	I	**NUMERIC COPROCESSOR ERROR.** This pin functions as a FERR# signal supporting coprocessor errors. This signal is tied to the coprocessor error signal on the CPU. If FERR# is asserted, PIIX4 generates an internal IRQ13 to its interrupt controller unit. PIIX4 then asserts the INT output to the CPU. FERR# is also used to gate the IGNNE# signal to ensure that IGNNE# is not asserted to the CPU unless FERR# is active.
SLP#	OD	**SLEEP.** This signal is output to the Pentium II processor in order to put it into Sleep state. For Pentium processor it is a No Connect.

3.2 INTEL 82371EB PCI-TO-ISA / IDE XCELERATOR (PIIX4) (5).

SIGNAL	TYPE	DESCRIPTION
IGNNE#	OD	**IGNORE NUMERIC EXCEPTION.** This signal is connected to the ignore numeric exception pin on the CPU. IGNNE# is only used if the PIIX4 coprocessor error reporting function is enabled. If FERR# is active, indicating a coprocessor error, a write to the Coprocessor Error Register (F0h) causes the IGNNE# to be asserted. IGNNE# remains asserted until FERR# is negated. If FERR# is not asserted when the Coprocessor Error Register is written, the IGNNE# signal is not asserted. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
INIT	OD	**INITIALIZATION.** INIT is asserted in response to any one of the following conditions. When the System Reset bit in the Reset Control Register is reset to 0 and the Reset CPU bit toggles from 0 to 1, PIIX4 initiates a soft reset by asserting INIT. PIIX4 also asserts INIT if a Shut Down Special cycle is decoded on the PCI Bus, if the RCIN# signal is asserted, or if a write occurs to Port 92h, bit 0. When asserted, INIT remains asserted for approximately 64 PCI clocks before being negated. This signal is active high for Pentium processor and active-low for Pentium II processor as determined by CONFIG1 signal. **Pentium Processor:** **During Reset:** Low **After Reset:** Low **During POS:** Low **Pentium II Processor:** **During Reset:** High **After Reset:** High **During POS:** High
INTR	OD	**CPU INTERRUPT.** INTR is driven by PIIX4 to signal the CPU that an interrupt request is pending and needs to be serviced. It is asynchronous with respect to SYSCLK or PCICLK and is always an output. The interrupt controller must be programmed following PCIRST# to ensure that INTR is at a known state. **During Reset:** Low **After Reset:** Low **During POS:** Low
NMI	OD	**NON-MASKABLE INTERRUPT.** NMI is used to force a nonmaskable interrupt to the CPU. PIIX4 generates an NMI when either SERR# or IOCHK# is asserted, depending on how the NMI Status and Control Register is programmed. The CPU detects an NMI when it detects a rising edge on NMI. After the NMI interrupt routine processes the interrupt, the NMI status bits in the NMI Status and Control Register are cleared by software. The NMI interrupt routine must read this register to determine the source of the interrupt. The NMI is reset by setting the corresponding NMI source enable/disable bit in the NMI Status and Control Register. To enable NMI interrupts, the two NMI enable/disable bits in the register must be set to 0, and the NMI mask bit in the NMI Enable/Disable and Real Time Clock Address Register must be set to 0. Upon PCIRST#, this signal is driven low. **During Reset:** Low **After Reset:** Low **During POS:** Low
SMI#	OD	**SYSTEM MANAGEMENT INTERRUPT.** SMI# is an active low synchronous output that is asserted by PIIX4 in response to one of many enabled hardware or software events. The CPU recognizes the falling edge of SMI# as the highest priority interrupt in the system, with the exception of INIT, CPURST, and FLUSH. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
STPCLK#	OD	**STOP CLOCK.** STPCLK# is an active low synchronous output that is asserted by PIIX4 in response to one of many hardware or software events. STPCLK# connects directly to the CPU and is synchronous to PCICLK. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-
RTCX1, RTCX2	I/O	**RTC CRYSTAL INPUTS:** These connected directly to a 32.768-kHz crystal. External capacitors are required. These clock inputs are required even if the internal RTC is not being used.

SIGNAL	TYPE	DESCRIPTION
CLK48	I	**48-MHZ CLOCK.** 48-MHz clock used by the internal USB host controller. This signal may be stopped during suspend modes.
PCICLK	I	**FREE-RUNNING PCI CLOCK.** A clock signal running at 30 or 33 MHz, PCICLK provides timing for all transactions on the PCI Bus. All other PCI signals are sampled on the rising edge of PCICLK, and all timing parameters are defined with respect to this edge. Because many of the circuits in PIIX4 run off the PCI clock, this signal MUST be kept active, even if the PCI bus clock is not active.
OSC	I	**14.31818-MHZ CLOCK.** Clock signal used by the internal 8254 timer. This clock signal may be stopped during suspend modes.
SUSCLK	O	**SUSPEND CLOCK.** 32.768-kHz output clock provided to the Host-to-PCI bridge used for maintenance of DRAM refresh. This signal is stopped during Suspend-to-Disk and Soft Off modes. For values During Reset, After Reset, and During POS, see the *Suspend/Resume and Resume Control Signaling* section.
SYSCLK	O	**ISA SYSTEM CLOCK.** SYSCLK is the reference clock for the ISA bus. It drives the ISA bus directly. The SYSCLK is generated by dividing PCICLK by 4. The SYSCLK frequencies supported are 7.5 MHz and 8.33 MHz. For PCI accesses to the ISA bus, SYSCLK may be stretched low to synchronize BALE falling to the rising edge of SYSCLK. **During Reset:** Running **After Reset:** Running **During POS:** Low
PDA[2:0]	O	**PRIMARY DISK ADDRESS[2:0].** These signals indicate which byte in either the ATA command block or control block is being addressed. If the IDE signals are configured for Primary and Secondary, these signals are connected to the corresponding signals on the Primary IDE connector. If the IDE signals are configured for Primary 0 and Primary 1, these signals are used for the Primary 0 connector.
PDCS1#	O	**PRIMARY DISK CHIP SELECT FOR 1F0H– –1F7H RANGE.** For ATA command register block. If the IDE signals are configured for Primary and Secondary, this output signal is connected to the corresponding signal on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector. **During Reset:** High **After Reset:** High **During POS:** High
PDCS3#	O	**PRIMARY DISK CHIP SELECT FOR 3F0– –3F7 RANGE.** For ATA control register block. If the IDE signals are configured for Primary and Secondary, this output signal is connected to the corresponding signal on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector. **During Reset:** High **After Reset:** High **During POS:** High
PDD[15:0]	I/O	**PRIMARY DISK DATA[15:0].** These signals are used to transfer data to or from the IDE device. If the IDE signals are configured for Primary and Secondary, these signals are connected to the corresponding signals on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector.
SDA[2:0]	O	**SECONDARY DISK ADDRESS[2:0].** These signals indicate which byte in either the ATA command block or control block is being addressed. If the IDE signals are configured for Primary and Secondary, these signals are connected to the corresponding signals on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector.

3.2 INTEL 82371EB PCI-TO-ISA / IDE XCELERATOR (PIIX4) (6).

SIGNAL	TYPE	DESCRIPTION
PDDACK#	O	**PRIMARY DMA ACKNOWLEDGE.** This signal directly drives the IDE device DMACK# signal. It is asserted by PIIX4 to indicate to IDE DMA slave devices that a given data transfer cycle (assertion of PDIOR# or PDIOW#) is a DMA data transfer cycle. This signal is used in conjunction with the PCI bus master IDE function. It is not associated with any AT compatible DMA channel. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector. **During Reset:** High **After Reset:** High **During POS:** High
PDDREQ	I	**PRIMARY DISK DMA REQUEST.** This input signal is directly driven from the IDE device DMARQ signal. It is asserted by the IDE device to request a data transfer, and used in conjunction with the PCI bus master IDE function. It is not associated with any AT compatible DMA channel. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector.
PDIOR#	O	**PRIMARY DISK IO READ.** In normal IDE this is the command to the IDE device that it may drive data onto the PDD[15:0] lines. Data is latched by PIIX4 on the negation edge of PDIOR#. The IDE device is selected either by the ATA register file chip selects (PDCS1#, PDCS3#) and the PDA[2:0] lines, or the IDE DMA slave arbitration signals (PDDACK#). In an Ultra DMA/33 read cycle, this signal is used as DMARDY# which is negated by the PIIX4 to pause Ultra DMA/33 transfers. In an Ultra DMA/33 write cycle, this signal is used as the STROBE signal, with the drive latching data on rising and falling edges of STROBE. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector.
PDIOW#	O	**PRIMARY DISK IO WRITE.** In normal IDE mode, this is the command to the IDE device that it may latch data from the PDD[15:0] lines. Data is latched by the IDE device on the negation edge of PDIOW#. The IDE device is selected either by the ATA register file chip selects (PDCS1#, PDCS3#) and the PDA[2:0] lines, or the IDE DMA slave arbitration signals (PDDACK#). For Ultra DMA/33 mode, this signal is used as the STOP signal, which is used to terminate an Ultra DMA/33 transaction. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector.
PIORDY	I	**PRIMARY IO CHANNEL READY.** In normal IDE mode, this input signal is directly driven by the corresponding IDE device IORDY signal. In an Ultra DMA/33 read cycle, this signal is used as STROBE, with the PIIX4 latching data on rising and falling edges of STROBE. In an Ultra DMA/33 write cycle, this signal is used as the DMARDY# signal which is negated by the drive to pause Ultra DMA/33 transfers.

SIGNAL	TYPE	DESCRIPTION
SDCS1#	O	**SECONDARY CHIP SELECT FOR 170H– –177H RANGE.** For ATA command register block. If the IDE signals are configured for Primary and Secondary, this output signal is connected to the corresponding signal on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector. **During Reset:** High **After Reset:** High **During POS:** High
SDCS3#	O	**SECONDARY CHIP SELECT FOR 370H– –377H RANGE.** For ATA control register block. If the IDE signals are configured for Primary and Secondary, this output signal is connected to the corresponding signal on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector. **During Reset:** High **After Reset:** High **During POS:** High-Z
SDD[15:0]	I/O	**SECONDARY DISK DATA[15:0].** These signals are used to transfer data to or from the IDE device. If the IDE signals are configured for Primary and Secondary, these signals are connected to the corresponding signals on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector.
SDDACK#	O	**SECONDARY DMA ACKNOWLEDGE.** This signal directly drives the IDE device DMACK# signal. It is asserted by PIIX4 to indicate to IDE DMA slave devices that a given data transfer cycle (assertion of SDIOR# or SDIOW#) is a DMA data transfer cycle. This signal is used in conjunction with the PCI bus master IDE function. It is not associated with any AT compatible DMA channel. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector. **During Reset:** High **After Reset:** High **During POS:** High
SDDREQ	I	**SECONDARY DISK DMA REQUEST.** This input signal is directly driven from the IDE device DMARQ signal. It is asserted by the IDE device to request a data transfer, and used in conjunction with the PCI bus master IDE function. It is not associated with any AT compatible DMA channel. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector.
SDIOR#	O	**SECONDARY DISK IO READ.** In normal IDE mode, this is the command to the IDE device that it may drive data onto the SDD[15:0] lines. Data is latched by the PIIX4 on the negation edge of SDIOR#. The IDE device is selected either by the ATA register file chip selects (SDCS1#, SDCS3#) and the SDA[2:0] lines, or the IDE DMA slave arbitration signals (SDDACK#). In an Ultra DMA/33 read cycle, this signal is used as DMARDY# which is negated by the PIIX4 to pause Ultra DMA/33 transfers. In an Ultra DMA/33 write cycle, this signal is used as the STROBE signal, with the drive latching data on rising and falling edges of STROBE. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector.

3.2 INTEL 82371EB PCI-TO-ISA / IDE XCELERATOR (PIIX4) (7).

SIGNAL	TYPE	DESCRIPTION
SDIOW#	O	**SECONDARY DISK IO WRITE.** In normal IDE mode, this is the command to the IDE device that it may latch data from the SDD[15:0] lines. Data is latched by the IDE device on the negation edge of SDIOW#. The IDE device is selected either by the ATA register file chip selects (SDCS1#, SDCS3#) and the SDA[2:0] lines, or the IDE DMA slave arbitration signals (SDDACK#). In read and write cycles this signal is used as the STOP signal, which is used to terminate an Ultra DMA/33 transaction. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector. **During Reset:** High **After Reset:** High **During POS:** High
SIORDY	I	**SECONDARY IO CHANNEL READY.** In normal IDE mode, this input signal is directly driven by the corresponding IDE device IORDY signal. In an Ultra DMA/33 read cycle, this signal is used as STROBE, with the PIIX4 latching data on rising and falling edges of STROBE. In an Ultra DMA write cycle, this signal is used as the DMARDY# signal which is negated by the drive to pause Ultra DMA/33 transfers. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector. This is a Schmitt triggered input.
OC[1:0]#	I	**OVER CURRENT DETECT.** These signals are used to monitor the status of the USB power supply lines. The corresponding USB port is disabled when its over current signal is asserted.
USBP0+, USBP0□	I/O	**SERIAL BUS PORT 0.** This signal pair comprises the differential data signal for USB port 0.
USBP1+, USBP1	I/O	**SERIAL BUS PORT 1.** This signal pair comprises the differential data signal for USB port 1.
BATLOW#/ GPI9	I	**BATTERY LOW.** Indicates that battery power is low. PIIX4 can be programmed to prevent a resume operation when the BATLOW# signal is asserted. If the Battery Low function is not needed, this pin can be used as a general-purpose input.
CPU_STP#/ GPO17	O	**CPU CLOCK STOP.** Active low control signal to the clock generator used to disable the CPU clock outputs. If this function is not needed, then this signal can be used as a general-purpose output. For values **During Reset**, **After Reset**, and **During POS**, see the *Suspend/Resume and Resume Control Signaling* section.
EXTSMI#	I/OD	**EXTERNAL SYSTEM MANAGEMENT INTERRUPT.** EXTSMI# is a falling edge triggered input to PIIX4 indicating that an external device is requesting the system to enter SMM mode. When enabled, a falling edge on EXTSMI# results in the assertion of the SMI# signal to the CPU. EXTSMI# is an asynchronous input to PIIX4. However, when the setup and hold times are met, it is only required to be asserted for one PCICLK. Once negated EXTSMI# must remain negated for at least four PCICLKs to allow the edge detect logic to reset. EXTSMI# is asserted by PIIX4 in response to SMI# being activated within the Serial IRQ function. An external pull-up should be placed on this signal.

SIGNAL	TYPE	DESCRIPTION
LID/ GPI10	I	**LID INPUT.** This signal can be used to monitor the opening and closing of the display lid of a notebook computer. It can be used to detect both low to high transition or a high to low transition and these transitions will generate an SMI# if enabled. This input contains logic to perform a 16-ms debounce of the input signal. If the LID function is not needed, this pin can be used as a general-purpose input.
PCIREQ[A:D]#	I	**PCI REQUEST.** Power Management input signals used to monitor PCI Master Requests for use of the PCI bus. They are connected to the corresponding REQ[0:3]# signals on the Host Bridge.
PCI_STP#/ GPO18	O	**PCI CLOCK STOP.** Active low control signal to the clock generator used to disable the PCI clock outputs. The PIIX4 free running PCICLK input must remain on. If this function is not needed, this pin can be used as a general-purpose output. For values **During Reset**, **After Reset**, and **During POS**, see the *Suspend/Resume and Resume Control Signaling* section.
PWRBTN#	I	**POWER BUTTON.** Input used by power management logic to monitor external system events, most typically a system on/off button or switch. This input contains logic to perform a 16-ms debounce of the input signal.
RI# GPI12	I	**RING INDICATE.** Input used by power management logic to monitor external system events, most typically used for wake up from a modem. If this function is not needed, then this signal can be individually used as a general-purpose input.
RSMRST#	I	**RESUME RESET.** This signal resets the internal Suspend Well power plane logic and portions of the RTC well logic.
SMBALERT#/ GPI11	I	**SM BUS ALERT.** Input used by System Management Bus logic to generate an interrupt (IRQ or SMI) or power management resume event when enabled. If this function is not needed, this pin can be used as a general-purpose input.
SMBCLK	I/O	**SM BUS CLOCK.** System Management Bus Clock used to synchronize transfer of data on SMBus. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
SMBDATA	I/O	**SM BUS DATA.** Serial data line used to transfer data on SMBus. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
SUSA#	O	**SUSPEND PLANE A CONTROL.** Control signal asserted during power management suspend states. SUSA# is primarily used to control the primary power plane. This signal is asserted during POS, STR, and STD suspend states. **During Reset:** Low **After Reset:** High **During POS:** Low
SUSB#/ GPO15	O	**SUSPEND PLANE B CONTROL.** Control signal asserted during power management suspend states. SUSB# is primarily used to control the secondary power plane. This signal is asserted during STR and STD suspend states. If the power plane control is not needed, this pin can be used as a general-purpose output. **During Reset:** Low **After Reset:** High **During POS:** High/GPO
SUSC#/ GPO16	O	**SUSPEND PLANE C CONTROL.** Control signal asserted during power management suspend states, primarily used to control the tertiary power plane. It is asserted only during STD suspend state. If the power plane control is not needed, this pin can be used as a general-purpose output. **During Reset:** Low **After Reset:** High **During POS:** High/GPO
SUS_STAT1#/ GPO20	O	**SUSPEND STATUS 1.** This signal is typically connected to the Host-to-PCI bridge and is used to provide information on host clock status. SUS_STAST1# is asserted when the system may stop the host clock, such as Stop Clock or during POS, STR, and STD suspend states. If this function is not needed, this pin can be used as a general-purpose output.

3.2 INTEL 82371EB PCI-TO-ISA / IDE XCELERATOR (PIIX4) (8).

SIGNAL	TYPE	DESCRIPTION
SUS_STAT2#/ GPO21	O	**SUSPEND STATUS 2.** This signal will typically connect to other system peripherals and is used to provide information on system suspend state. It is asserted during POS, STR, and STD suspend states. If this function is not needed, this pin can be used as a general-purpose output. **During Reset:** Low **After Reset:** High **During POS:** Low/GPO
THRM#/ GPI8	I	**THERMAL DETECT.** Active low signal generated by external hardware to start the Hardware Clock Throttling mode. If enabled, the external hardware can force the system to enter into Hardware Clock Throttle mode by asserting THRM#. This causes PIIX4 to cycle STPCLK# at a preset programmable rate. If this function is not needed, this pin can be used as a general-purpose input.
ZZ/ GPO19	O	**LOW-POWER MODE FOR L2 CACHE SRAM.** This signal is used to power down a cache□ data SRAMs when the clock logic places the CPU into the Stop Clock. If this function is not needed, this pin can be used as a general-purpose output. **During Reset:** Low **After Reset:** Low **During POS:** Low
GPI[21:0]	I	**GENERAL PURPOSE INPUTS.** These input signals can be monitored via the GPIREG register located in Function 3 (Power Management) System IO Space at address PMBase+30h. See Table 1 for details.
GPO[30:0]	O	**GENERAL PURPOSE OUTPUTS.** These output signals can be controlled via the GPIREG register located in Function 3 (Power Management) System IO Space at address PMBase+34h. If a GPO pin is not multiplexed with another signal or defaults to GPO, then its state after reset is the reset condition of the GPOREG register. If the GPO defaults to another signal, then it defaults to that signal□ state after reset. The GPO pins that default to GPO remain stable after reset. The others may toggle due to system boot or power control sequencing after reset prior to their being programmed as GPOs. The GPO8 signal is driven low upon removal of power from the PIIX4 core power plane. All other GPO signals are invalid (buffers powered off).
CONFIG1	I	**CONFIGURATION SELECT 1.** This input signal is used to select the type of microprocessor being used in the system. If CONFIG1=0, the system contains a Pentium microprocessor. If CONFIG1=1, the system contains a Pentium II microprocessor. It is used to control the polarity of INIT and CPURST signals.
CONFIG2	I	**CONFIGURATION SELECT 2.** This input signal is used to select the positive or subtractive decode of FFFF0000h□FFFFFFFh memory address range (top 64 Kbytes). If CONFIG[2]=0, the PIIX4 will positively decode this range. If CONFIG[2]=1, the PIIX4 will decode this range with subtractive decode timings only. The input value of this pin must be static and may not dynamically change during system operations.
PWROK	I	**POWER OK.** When asserted, PWROK is an indication to PIIX4 that power and PCICLK have been stable for at least 1 ms. PWROK can be driven asynchronously. When PWROK is negated, PIIX4 asserts CPURST, PCIRST# and RSTDRV. When PWROK is driven active (high), PIIX4 negates CPURST, PCIRST#, and RSTDRV.
SPKR	O	**SPEAKER.** The SPKR signal is the output of counter timer 2 and is internally "ANDed" with Port 061h bit 1 to provide the Speaker Data Enable. This signal drives an external speaker driver device, which in turn drives the ISA system speaker. **During Reset:** Low **After Reset:** Low **During POS:** Last State TEST# I **TEST MODE SELECT.** The test signal is used to select various test modes of PIIX4. This signal must be pulled up to VCC(SUS) for normal operation.

SIGNAL	TYPE	DESCRIPTION
VCC	V	**CORE VOLTAGE SUPPLY.** These pins are the primary voltage supply for the PIIX4 core and IO periphery and must be tied to 3.3V.
VCC (RTC)	V	**RTC WELL VOLTAGE SUPPLY.** This pin is the supply voltage for the RTC logic and must be tied to 3.3V.
VCC (SUS)	V	**SUSPEND WELL VOLTAGE SUPPLY.** These pins are the primary voltage supply for the PIIX4 suspend logic and IO signals and must be tied to 3.3V.
VCC (USB)	V	**USB VOLTAGE SUPPLY.** This pin is the supply voltage for the USB input/output buffers and must be tied to 3.3V.
VREF	V	**VOLTAGE REFERENCE.** This pin is used to provide a 5V reference voltage for 5V safe input buffers. VREF must be tied to 5V in a system requiring 5V tolerance. In a 5V tolerant system, this signal must power up before or simultaneous to VCC. It must power down after or simultaneous to VCC. In a non-5V tolerant system (3.3V only), this signal can be tied directly to VCC. There are then no sequencing requirements.
VSS	V	**CORE GROUND.** These pins are the primary ground for PIIX4.
VSS (USB)	V	**USB GROUND.** This pin is the ground for the USB input/output buffers.

4. MAJOR CHIP DESCRIPTION

4.1 IMM/MMC-2 CPU MODULE

THE INTEL MOBILE MODULE INCORPORATES AN INTEL MOBILE PENTIUM II PROCESSOR CORE, SECOND LEVEL CACHE WITH TAG RAM, INTEL 443BX HOST BRIDGE " NORTHBRIDGE" SYSTEM CONTROLLER, VOLTAGE REGULATOR, AND A SMBUS THERMAL SENSOR ON A SINGLE PRINTED CIRCUIT BOARD. IT' S A SMALL, HIGHLY INTEGRATED ASSEMBLY CONTAINING THE MOBILE PENTIUM II PROCESSOR CORE WITH INTERNAL/BUS FREQUENCY OF 233/66 OR 266/66 AND ITS IMMEDIATE SYSTEM-LEVEL SUPPORT.

MMC2 INCLUDES A SECOND-LEVEL CACHE OF PIPELINE BURST SRAM WITH SUPPORT UP TO 512KB AND SUPPORTS THE " STOP CLOCK " MODE OF POWER MANAGEMENT FOR THE L2 SRAMS. IN THIS MODE, THE CLOCK SIGNALS TO THE L2 SRAMS ARE STOPPED OR " PARKED " IN A LOW STATE.

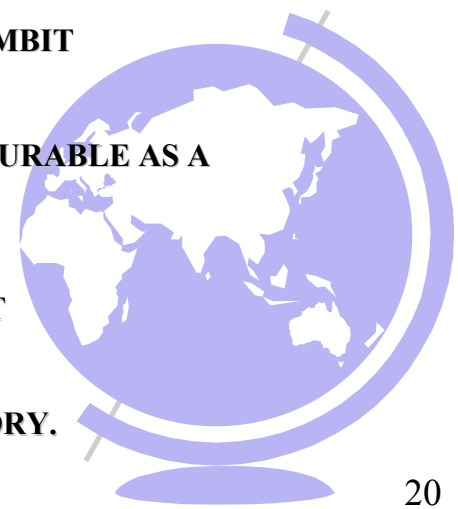
THE INTEL MOBILE MODULE CONTAINS KEY FEATURES OF THE 440BX HOST BRIDGE SYSTEM CONTROLLER. THE DRAM CONTROLLER SUPPORTS EDO AT 3.3V WITH A BURST READ AT 5-2-2-2 (60NS) AND SDRAM AT 3.3V WITH A BURST READ AT 4-1-1-1 (66MHZ, CL=2). PCI, AGP AND DRAM INTERFACE THE MMC2 MICROPROCESSOR CONSUMES 1.7V CORE POWER (VOLTAGE REDUCTION TECHNOLOGY) AND 2.5V FOR I/O INTERFACE.

AN ON BOARD VOLTAGE REGULATOR PROVIDE THE DC CONVERSION FROM THE SYSTEM MANUFACTURER' S SYSTEM DC VOLTAGE TO THE PROCESSOR' S CORE AND I/O VOLTAGE. PROCESSOR CORE VOLTAGE REGULATION SUPPORTS INPUT VOLTAGES FROM 5V TO 21V.

THE INTEL MOBILE MODULAR INCORPORATES ACTIVE THERMAL FEEDBACK (ATF) SENSING, ACPI REV. 1.0 COMPLIANT BY INCLUDING AN INTERNAL A/D-DIGITAL SIGNALING (SMBUS) ACROSS THE MODULE INTERFACE AND A PROGRAMMABLE TRIP POINT INTERRUPT OR POLL MODE FOR READING TEMPERATURE.

4.2 Intel 82443BX AGPset Host bridge

- **PROCESSOR/HOST BUS SUPPORT**
  - ~ OPTIMIZED FOR PENTIUM II PROCESSOR AT 100 MHZ SYSTEM BUS FREQUENCY; SUPPORT FOR 66 MHZ.
  - ~ SUPPORT FOR SINGLE AND DUAL PENTIUM II PROCESSOR CONFIGURATIONS
  - ~ 64-BIT GTL+ BASED HOST BUS INTERFACE
  - ~ 32-BIT HOST ADDRESS SUPPORT
  - ~ SUPPORTS FULL SYMMETRIC MULTIPROCESSOR (SMP) PROTOCOL FOR UP TO TWO PROCESSORS; I/O APIC RELATED BUFFER MANAGEMENT SUPPORT (WSC# SIGNAL).
  - ~ IN-ORDER TRANSACTION AND DYNAMIC DEFERRED TRANSACTION SUPPORT.
  - ~ DESKTOP OPTIMIZED GTL+ BUS DRIVER TECHNOLOGY (GATED GTL+ RECEIVERS FOR REDUCED POWER).
- **INTEGRATED DRAM CONTROLLER**
  - ~ 8 TO 512 MBYTES OR 1GB (WITH REGISTERED DIMMS).
  - ~ SUPPORTS UP TO 4 DOUBLE-SIDED DIMMS (8 ROWS MEMORY).
  - ~ 64-BIT DATA INTERFACE WITH ECC SUPPORT (SDRAM ONLY).
  - ~ UNBUFFERED AND REGISTERED SDRAM (SYNCHRONOUS) DRAM SUPPORT (X-1-1-1 ACCESS @ 66 MHZ,X-1-1-1 ACCESS @ 100 MHZ).
  - ~ ENHANCED SDRAM OPEN PAGE ARCHITECTURE SUPPORT FOR 16- AND 64-MBIT DRAM DEVICES WITH 2K, 4K AND 8K PAGE SIZES
- **PAGP INTERFACE**
  - ~ AGP INTERFACE (AGP) WITH 133 MHZ DATA TRANSFER CAPABILITY CONFIGURABLE AS A SECONDARY PCI BUS (AGP-66/133 3.3V DEVICE).
  - ~ AGP SPECIFICATION REV 1.0 COMPLIANT.
  - ~ AGP-DATA/TRANSACTION FLOW OPTIMIZED ARBITRATION MECHANISM.
  - ~ AGP SIDE-BAND INTERFACE FOR EFFICIENT REQUEST PIPELINING WITHOUT INTERFERING WITH THE DATA STREAMS.
  - ~ AGP-SPECIFIC DATA BUFFERING.
  - ~ SUPPORTS CONCURRENT CPU, AGP AND PCI TRANSACTIONS TO MAIN MEMORY.
  - ~ AGP HIGH-PRIORITY TRANSACTIONS(□EXPEDITE□ SUPPORT)



4.2 Intel 82443BX AGPset Host bridge

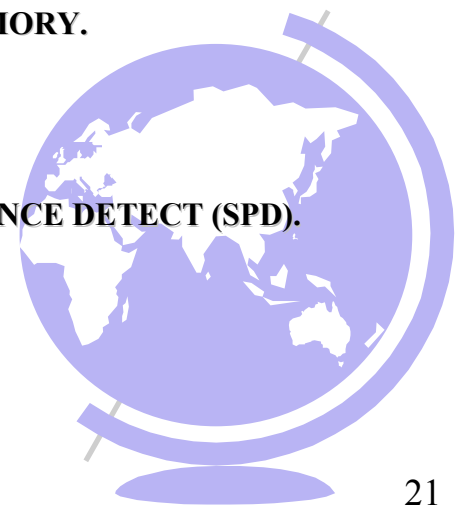
- POWER MANAGEMENT FUNCTIONS
  - ~ STOP CLOCK GRANT AND HALT SPECIAL CYCLE TRANSLATION (HOST TO PCI BUS).
  - ~ MOBILE AND □DEEP GREEN□ DESKTOP SUPPORT FOR SYSTEM SUSPEND/RESUME(I.E., DRAM AND POWER-ON SUSPEND).
  - ~ DYNAMIC POWER DOWN OF IDLE DRAM ROWS.
  - ~ SDRAM SELF-REFRESH POWER DOWN SUPPORT IN SUSPEND MODE.
  - ~ INDEPENDENT, INTERNAL DYNAMIC CLOCK GATING REDUCES AVERAGE POWER DISSIPATION.
  - ~ STATIC STOP CLOCK SUPPORT.
  - ~ POWER-ON SUSPEND MODE.
  - ~ SUSPEND TO DRAM.
  - ~ ACPI COMPLIANT POWER MANAGEMENT.
- CI BUS INTERFACE
  - ~ 32-BIT PRIMARY PCI BUS INTERFACE (PCI) WITH INTEGRATED PCI ARBITER
  - ~ PCI REV. 2.1, 3.3V AND 5V, 33MHZ INTERFACE COMPLIANT.
  - ~ PCI PARITY GENERATION SUPPORT.
  - ~ DATA STREAMING SUPPORT FROM PCI TO DRAM.
  - ~ DELAYED TRANSACTION SUPPORT FOR PCI-DRAM READS.
  - ~ SUPPORTS CONCURRENT CPU, AGP AND PCI TRANSACTIONS TO MAIN MEMORY.

PACKAGING/VOLTAGE

- ~ 492 PIN BGA
- ~ 3.3V CORE AND MIXED 3.3V AND GTL I/O.

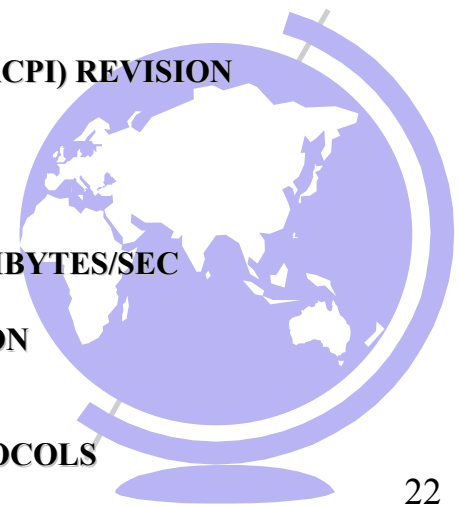
SUPPORTING I/O BRIDGE.

- ~ SYSTEM MANAGEMENT BUS (SMB) WITH SUPPORT FOR DIMM SERIAL PRESENCE DETECT (SPD).
- ~ PCI-ISA BRIDGE (PIIX4E).
- ~ POWER MANAGEMENT SUPPORT.
- ~ 3.3V CORE AND MIXED 5V, 3.3V I/O AND INTERFACE TO THE 2.5V CPU



4.3 INTEL 82371EB PCI-TO-ISA / IDE XCELERATOR (PIIX4E)

- SUPPORTED KITS FOR BOTH PENTIUM AND PENTIUM II MICROPROCESSORS
  - ~ 82430TX ISA KIT
  - ~ 82440BX ISA/DP KIT
- MULTIFUNCTION PCI TO ISA BRIDGE
  - ~ SUPPORTS PCI AT 30 MHZ AND 33 MHZ
  - ~ SUPPORTS PCI REV 2.1 SPECIFICATION
  - ~ SUPPORTS FULL ISA OR EXTENDED I/O (EIO) BUS
  - ~ SUPPORTS FULL POSITIVE DECODE OR SUBTRACTIVE DECODE OF PCI
  - ~ SUPPORTS ISA AND EIO AT 1/4 OF PCI FREQUENCY
- SUPPORTS BOTH MOBILE AND DESKTOP DEEP GREEN ENVIRONMENTS
  - ~ 3.3V OPERATION WITH 5V TOLERANT BUFFERS
  - ~ ULTRA-LOW POWER FOR MOBILE ENVIRONMENTS SUPPORT
  - ~ POWER-ON SUSPEND, SUSPEND TO RAM, SUSPEND TO DISK, AND SOFT-OFF SYSTEM STATES
  - ~ ALL REGISTERS READABLE AND RESTORABLE FOR PROPER RESUME FROM 0.V SUSPEND
- POWER MANAGEMENT LOGIC
  - ~ GLOBAL AND LOCAL DEVICE MANAGEMENT
  - ~ SUSPEND AND RESUME LOGIC
  - ~ SUPPORTS THERMAL ALARM
  - ~ SUPPORT FOR EXTERNAL MICROCONTROLLER
  - ~ FULL SUPPORT FOR ADVANCED CONFIGURATION AND POWER INTERFACE (ACPI) REVISION 1.0 SPECIFICATION AND OS DIRECTED POWER MANAGEMENT
- INTEGRATED IDE CONTROLLER
  - ~ INDEPENDENT TIMING OF UP TO 4 DRIVES
  - ~ PIO MODE 4 AND BUS MASTER IDE TRANSFERS UP TO 14 MBYTES/SEC
  - ~ SUPPORTS ULTRA DMA/33 SYNCHRONOUS DMA MODE TRANSFERS UP TO 33 MBYTES/SEC
  - ~ INTEGRATED 16 X 32-BIT BUFFER FOR IDE PCI BURST TRANSFERS
  - ~ SUPPORTS GLUE-LESS SWAP-BAY OPTION WITH FULL ELECTRICAL ISOLATION
- ENHANCED DMA CONTROLLER
  - ~ TWO 82C37 DMA CONTROLLERS
  - ~ SUPPORTS PCI DMA WITH 3 PC/PCI CHANNELS AND DISTRIBUTED DMA PROTOCOLS
  - ~ FAST TYPE-F DMA FOR REDUCED PCI BUS USAGE



4.3 INTEL 82371EB PCI-TO-ISA / IDE XCELERATOR (PIIX4E)

- INTERRUPT CONTROLLER BASED ON TWO 82C59
  - ~ 15 INTERRUPT SUPPORT
  - ~ INDEPENDENTLY PROGRAMMABLE FOR EDGE/LEVEL SENSITIVITY
  - ~ SUPPORTS OPTIONAL I/O APIC
  - ~ SERIAL INTERRUPT INPUT
- TIMERS BASED ON 82C54
  - ~ SYSTEM TIMER, REFRESH REQUEST, SPEAKER TONE OUTPUT
- USB
  - ~ TWO USB 1.0 PORTS FOR SERIAL TRANSFERS AT 12 OR 1.5 MBIT/SEC
  - ~ SUPPORTS LEGACY KEYBOARD AND MOUSE SOFTWARE WITH USB-BASED KEYBOARD AND MOUSE
  - ~ SUPPORTS UHCI DESIGN GUIDE
- SMBUS

  HOST INTERFACE ALLOWS CPU TO COMMUNICATE VIA SMBUS
  - ~ SLAVE INTERFACE ALLOWS EXTERNAL SMBUS MASTER TO CONTROL RESUME EVENTS
- REAL-TIME CLOCK
  - ~ 256-BYTE BATTERY-BACK CMOS SRAM
  - ~ INCLUDES DATE ALARM
  - ~ TWO 8-BYTE LOCKOUT RANGES
- MICROSOFT WIN95* COMPLIANT
- 324 MBGA PACKAGE

5. SYSTEM VIEW AND DISASSEMBLY

5.1 System View

5.1.1 Right-Side View

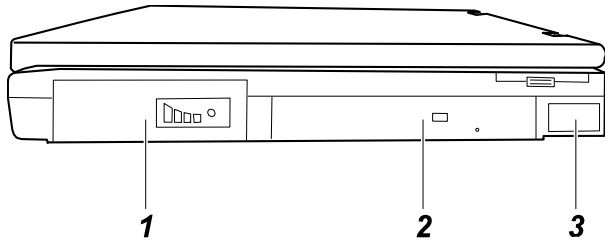


Figure 5-1. Right-Side View

1. **Battery Pack**
2. **CD-ROM/DVD-ROM Drive**
3. **IR Port**

5.1.2 Left-Side View

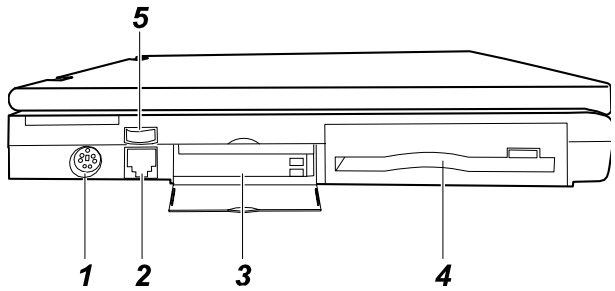


Figure 5-2. Left-Side View

1. **S-Video Output Connector**
2. **RJ-45 or RJ-11 Connector** (optional)
3. **PC Card Slots**
4. **Floppy Disk Drive**
5. **Volume Control**

5.1.3 Rear View

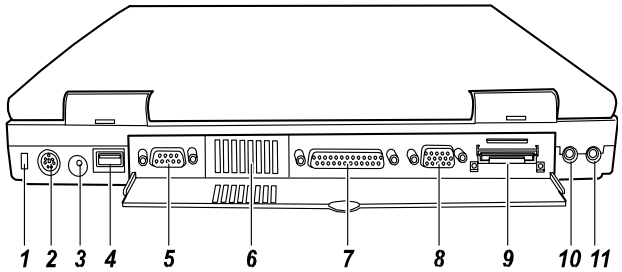


Figure 5-3. Rear View

1. **Kensington Lock Anchor**
2. **PS/2 Mouse/Keyboard Port**
3. **Power Connector**
4. **USB Port**
5. **Serial Port**
6. **Ventilation Opening**
7. **Parallel Port**
8. **VGA Port**
9. **Expansion Connector**
10. **Microphone Connector**
11. **Audio Output Connector**

5.1.4 Front View

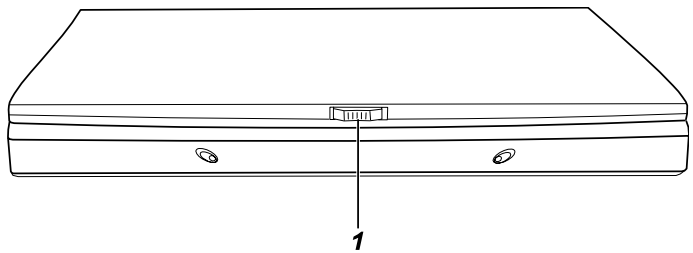
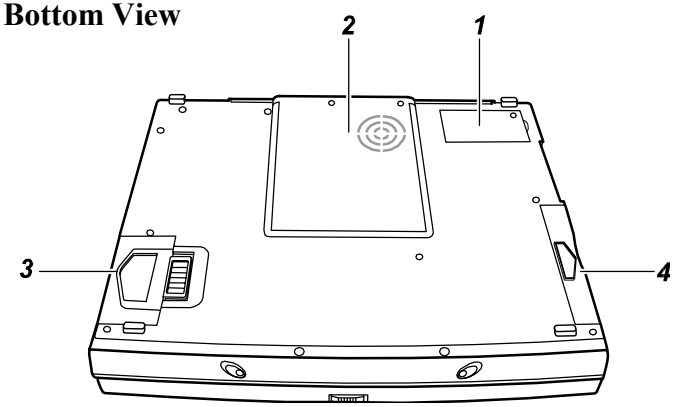


Figure 5-4. Front View

1. **Top Cover Latch**

5.1.5 Bottom View

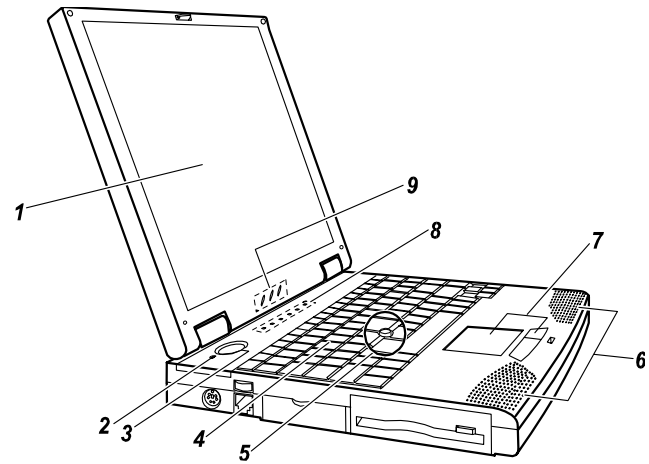


1. **Modem Card/LAN Card Cover**
2. **CPU Card Cover**
3. **Battery Pack & Locking Latch**
4. **FDD/HDD Module**

Figure 5-5. Bottom View

5.1.6 Top-Open View

To open the cover, press the cover latch toward the right and lift the cover.



1. **LCD Display**
2. **Microphone**
3. **Power Button**
4. **Keyboard**
5. **Track Point**
   (select models only)
6. **Stereo Speaker Set**
7. **Touchpad**
8. **System Indicators**
9. **Power Indicators**

Figure 5-6. Top-Open View

5.2 System Disassembly

The section discusses at length each major component for disassembly/reassembly and show corresponding illustrations. Use the chart below to determine the disassembly sequence for removing components from the notebook.

- **Modular Components**

  5.2.1 Battery Pack
  5.2.2 CD-ROM/DVD-ROM Drive
  5.2.3 Hard Disk Drive
  5.2.4 Floppy Disk Drive
  5.2.5 CPU
  5.2.6 Modem/LAN Card
  5.2.7 Keyboard
  5.2.8 SO-DIMM

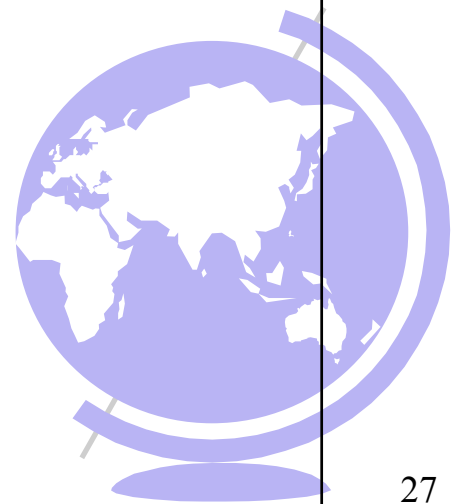
- **LCD Assembly Components**

  5.2.9 LCD Assembly
  5.2.10 LCD Panel
  5.2.11 Inverter/LED Board

- **Base Unit Components**

  5.2.12 Battery/Touchpad Board
  5.2.13 System Board
  5.2.14 Touchpad Panel

You can also find details such as exploded views and parts lists in Chapter 6.



5.2.1 Battery Pack

- **Disassembly**

1. Put the notebook upside down with care.
2. Press the locking latch outward to unlatch the battery pack and then pull it out of the compartment.

- **Reassembly**

1. Fit the battery pack into the compartment. Make sure the locking latches are in the locked position. (Refer to Figure 5-7)

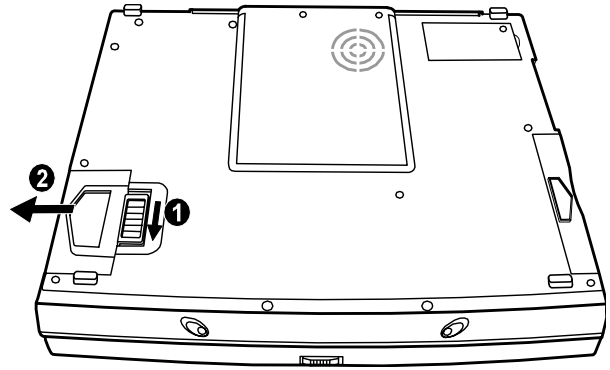


Figure 5-7. Removing the Battery Pack

5.2.2 CD-ROM/DVD-ROM Drive

- **Disassembly**

1. Place the notebook upside down with care.
2. Open the CPU compartment cover by removing two screws then sliding the cover toward the rear side to open it. (Refer to Figure 5-8.)

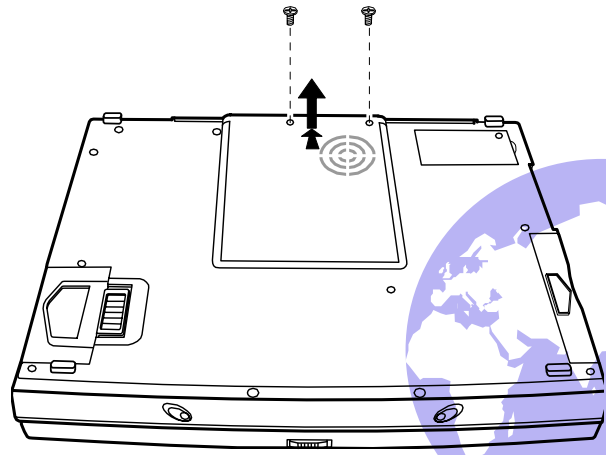


Figure 5-8. Removing the CPU Compartment Cover

3. **Remove one screw that fastens the CD-ROM/DVD-ROM drive. (Refer to Figure 5-9.)**
4. **Push the rear side of the CD-ROM/DVD-ROM drive to disconnect the drive from the system board, then slide it out of the compartment.**

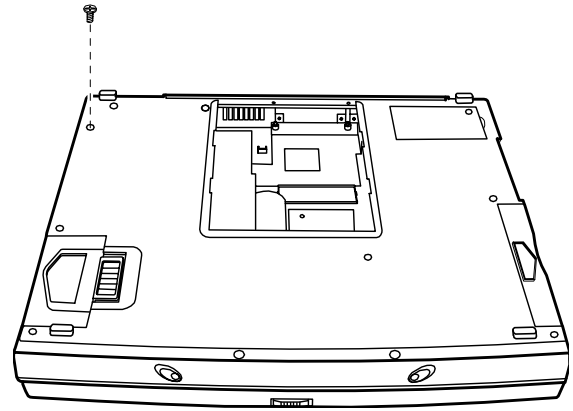


Figure 5-9. Removing One Screw

- **Reassembly**

1. **Slide the CD-ROM/DVD-ROM drive into the compartment. The cable connector on the system board will automatically plug into the rear side of the drive. (Refer to Figure 5-10.)**
2. **Secure the CD-ROM/DVD-ROMdrive with one screw. (Refer to Figure 5-9 earlier.)**
3. **Replace the CPU compartment cover and secure with two screws. (Refer to Figure 5-8 earlier.)**

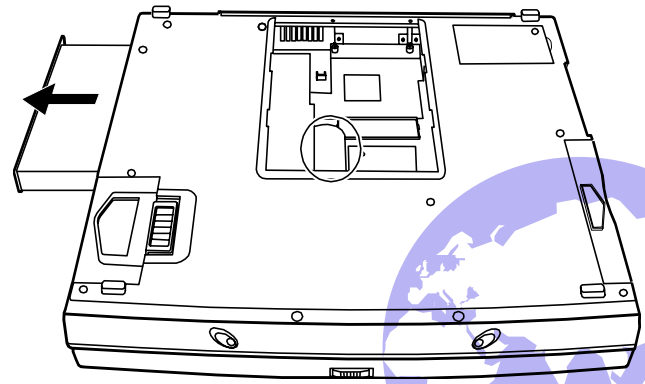


Figure 5-10. Removing the CD-ROM/DVD-ROM Drive

5.2.3 Hard Disk Drive

- **Disassembly**

1. Put the notebook upside down with care.
2. Remove one screw and slide the FDD/HDD module out of the compartment.
3. Remove four screws and disconnect the hard disk drive from the connector. (Refer to Figure 5-12.)

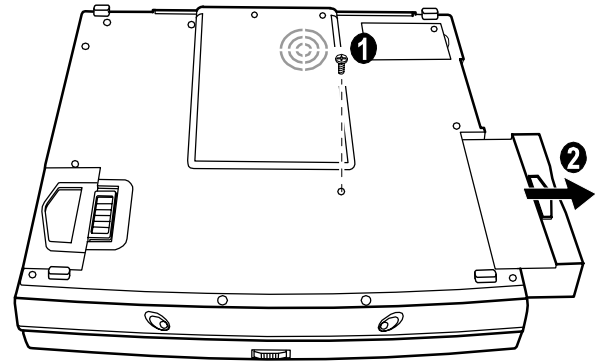


Figure 5-11. Removing the FDD/HDD Module

- **Reassembly**

1. Place the hard disk drive in the bracket and plug in the hard disk drive connector. Then secure the hard disk drive with four screws. (Refer to Figure 5-12)
2. Slide the HDD/FDD module into the compartment and secure with one screw. (Refer to Figure 5-11 earlier.)

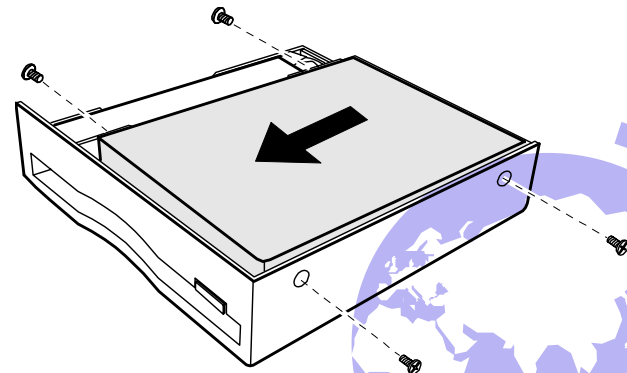


Figure 5-12. Removing the Hard Disk Drive

5.2.4 Floppy Disk Drive

- **Disassembly**

1. **Remove the hard disk drive. (See section 5.2.3 Disassembly.)**
2. **Remove four screws to detach the bracket from the floppy disk drive. (Refer to Figure 5-13.)**

- **Reassembly**

1. **Replace the bracket and secure with four screws. (Refer to Figure 5-13.)**
2. **Replace the hard disk drive. Slide the HDD/FDD module into the compartment and secure with one screw. (See section 5.2.3 Reassembly.)**

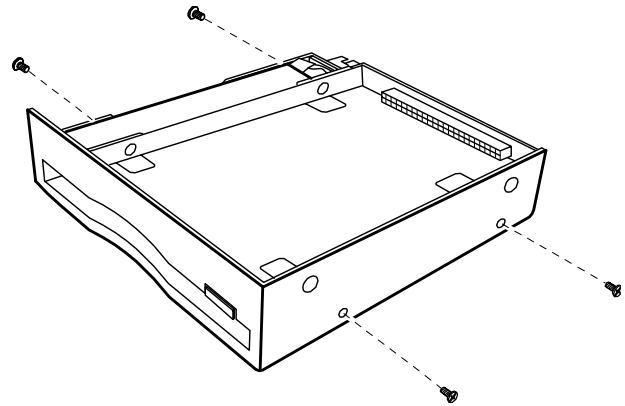


Figure 5-13. Detaching the Bracket From the Floppy Disk Drive

5.2.5 CPU

Disassembly

1. **Place the notebook upside down and remove the CPU compartment cover. (See section 5.2.2 Disassembly step 1 and 2.)**
2. **Remove two screws fastening the fan assembly. Unplug the fan assembly's power cord and lift it free from the CPU module.**
3. **Remove two screw nuts and one screw. (Refer to Figure 5-17.)**
4. **Extract CPU with a tool which provided an application of extraction force under the module' s PCB at left end of the connector. The Figure 5-15 shown the location of the point where pressure should be applied to extract the CPU module.**

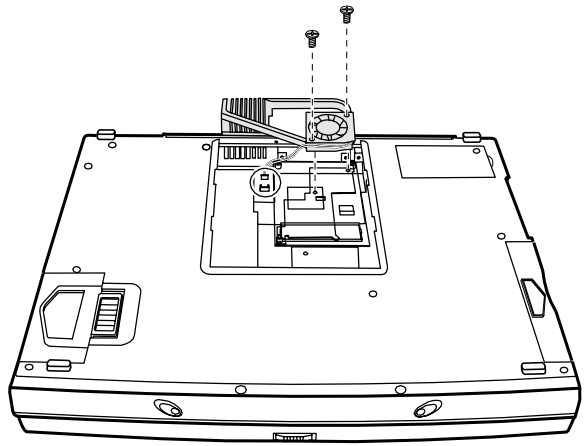


Figure 5-14. Removing the Fan Assembly

> ***NOTE:*** When disconnecting the CPU module, lift the module gently and carefully. If not, the connector of the CPU module may be damaged.

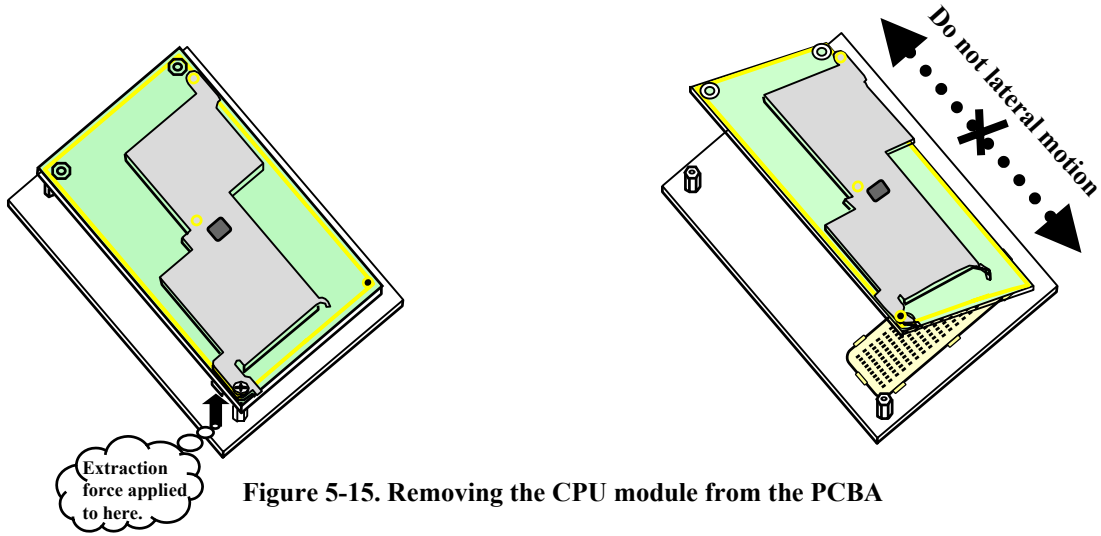


Figure 5-15. Removing the CPU module from the PCBA

● **Reassembly**

1. **Align the three holes on the CPU module with the three screw pillars on the system board.**

2. **Insertion of the MMC-2 CPU module with a two-step method that consists of applying on two areas of the module's Thermal Transfer Plate. Insertion is achieved by pressing one end of the connector first and then by applying pressure on the other end.(Refer to Figure 5-16.)**

3. **Reinstall the two screw nuts and one screw. (Refer to Figure 5-17.)**

4. **Place the fan assembly on top of the CPU module. Plug in the power cord and secure the fan assembly with two screws. (Refer to Figure 5-14 earlier.)**

5. **Replace the CPU compartment cover and secure with two screws.**

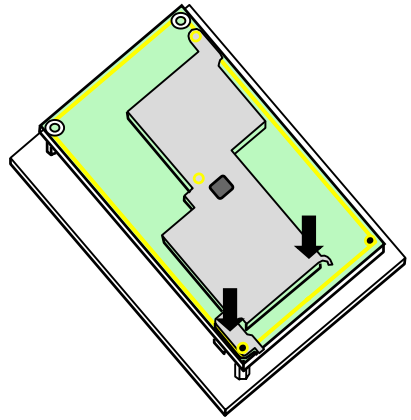


Figure 5-16. Insertion of the MMC-2 CPU Module

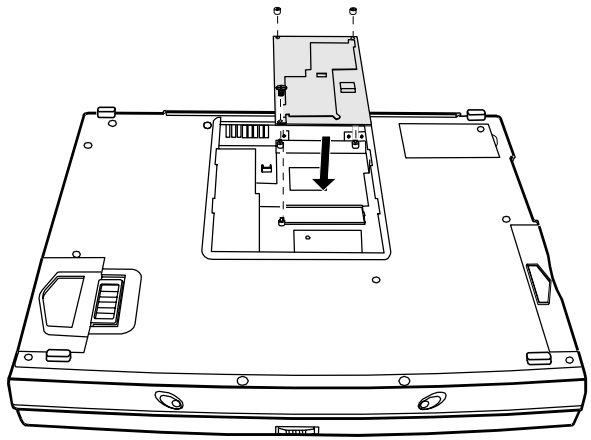


Figure 5-17. Align the CPU Module and two Screw Nuts and one Screw

5.2.6 Modem/LAN Card

- **Disassembly**

1. Place the notebook upside down with care.
2. Remove one screw and open the Modem/LAN card compartment cover. (Refer to Figure 5-18)
3. Carefully lift up the inner edge of the card to disconnect it from the system board.

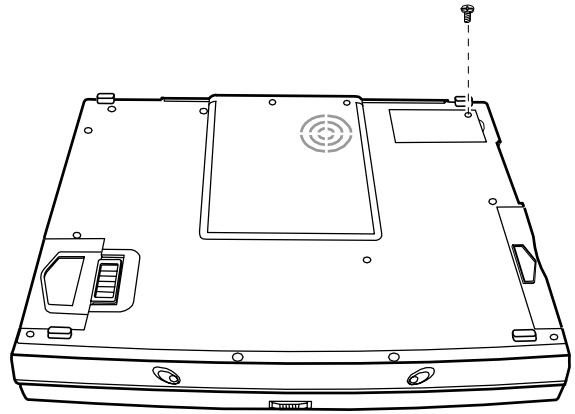


Figure 5-18. Removing the Modem/LAN Card Compartment Cover

- **Reassembly**

1. Hold the Modem/LAN card at an angle so that the phone line connector (or RJ-45 connector if installing a LAN card) is pointed towards the opening on the notebook. Insert the connector into the opening and press the other end to plug the Modem/LAN card into the socket on the system board. (Refer to Figure 5-19)

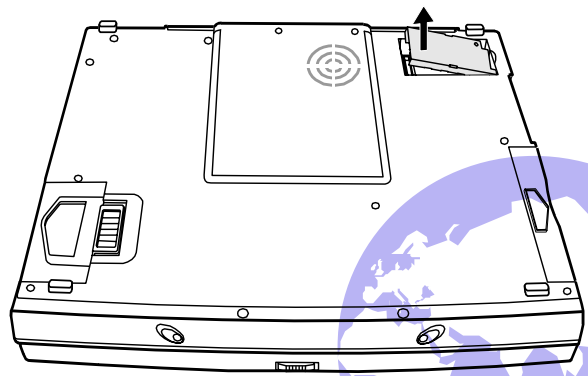


Figure 5-19. Removing the Modem/LAN Card

2. Replace the compartment cover and secure with one screw. (Refer to Figure 5-18 earlier.)

5.2.7 Keyboard

- **Disassembly**

1. Open the top cover.
2. Press the locking latch downward to unlatch the LED panel and then push it leftward to remove the panel. (Refer to Figure 5-20.)
3. Slightly lift up the keyboard and disconnect the cable from the system board to detach the keyboard.

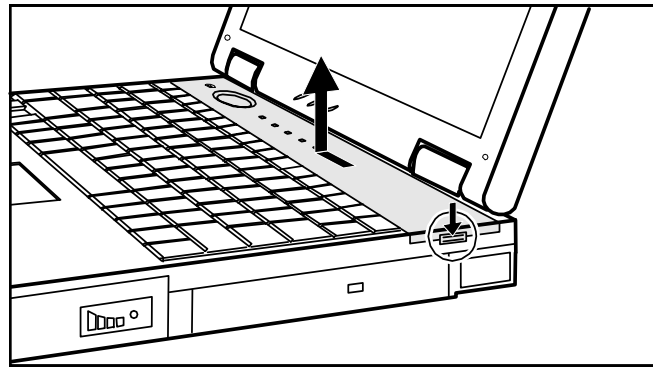


Figure 5-20. Removing the LED Panel

- **Reassembly**

1. Reconnect the keyboard cable and fit the keyboard back into place. (Refer to Figure 5-21 earlier.)
2. Replace the LED panel. (Refer to Figure 5-20 earlier.)

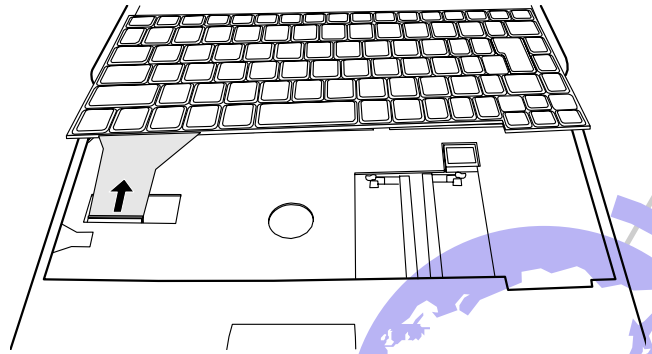


Figure 5-21. Removing the Keyboard

5.2.8 SO-DIMM

- **Disassembly**

1. Remove the keyboard. (See section 5.2.7 Disassembly.)
2. Pull the retaining clips outwards and remove the SO-DIMM. (Refer to Figure 5-22.)

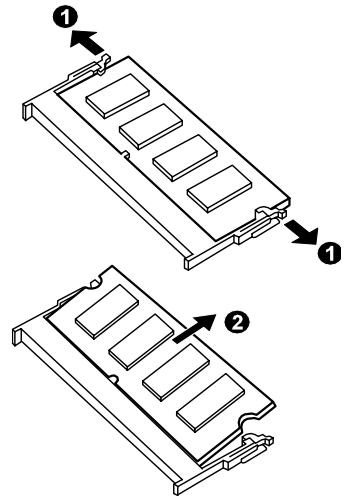


Figure 5-22. Removing the SO-DIMM

- **Reassembly**

1. To install the SO-DIMM, align the SO-DIMM's notched part with the socket's corresponding part and firmly insert the SO-DIMM into the socket at an angle. Then push down until the retaining clips lock the SO-DIMM into position. (Refer to Figure 5-22.)
2. Replace the keyboard. (See section 5.2.7 Reassembly.)

5.2.9 LCD Assembly

- **Disassembly**

1. Remove the hinge cover by inserting a flat screwdriver to the rear of the cover and pry the cover out. Repeat the same with the other hinge cover. (Refer to Figure 5-23).
   *Note the right and left hinges are not exchangeable.
2. Open the cover and remove the LED panel. (See section 5.2.7 Disassembly step 2.)
3. Disconnect two cables and remove four screws from the hinges. Now you can separate the LCD assembly from the base unit.

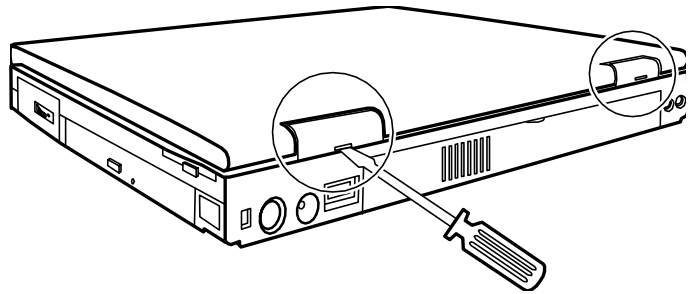


Figure 5-23. Removing the Hinge Covers

- **Reassembly**

1. Attach the LCD assembly to the base unit and secure with four screws on the hinges. Then reconnect the LCD cables to the system board. (Refer to Figure 5-24.)
2. Replace the LED panel.
3. Replace the two hinge covers. (Refer to Figure 5-23 earlier.)

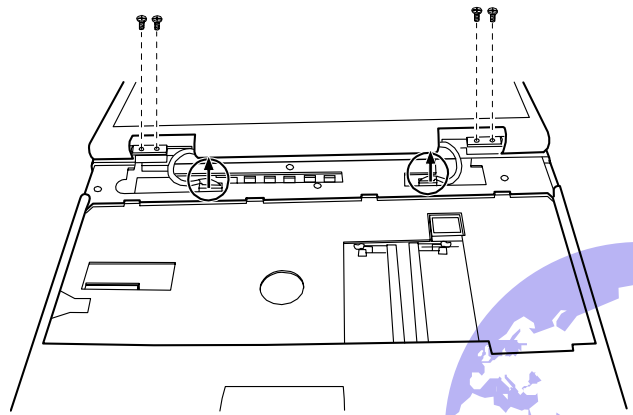


Figure 5-24. Unplugging two Cables and Removing Four Screws

5.2.10 LCD Panel

- **Disassembly**

1. Open the top cover.
2. Remove the two rubber pads and two screws on the lower part of the panel. Then insert a flat screwdriver to the lower part of the frame and gently pry the frame out. Repeat the process until the frame is completely separated from the housing.
3. To remove the LCD, remove three screws and unplug the inverter cable.

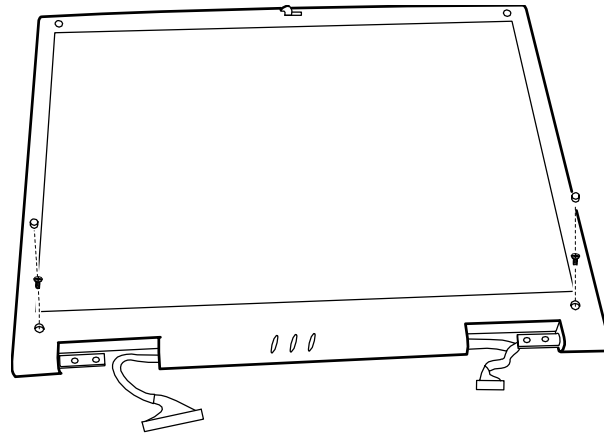


Figure 5-25. Removing the LCD Frame

- **Reassembly**

1. Reconnect the cable to the inverter board. Fit the LCD back into place and secure with three screws. (Refer to Figure 5-26.)
2. Fit the LCD frame back to the housing. Replace the two screws and two rubber pads. (Refer to Figure 5-25 earlier.)

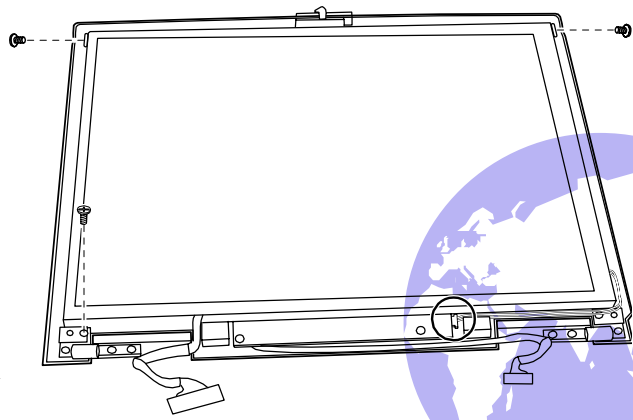


Figure 5-26. Removing the LCD

5.2.11 Inverter/LED Board

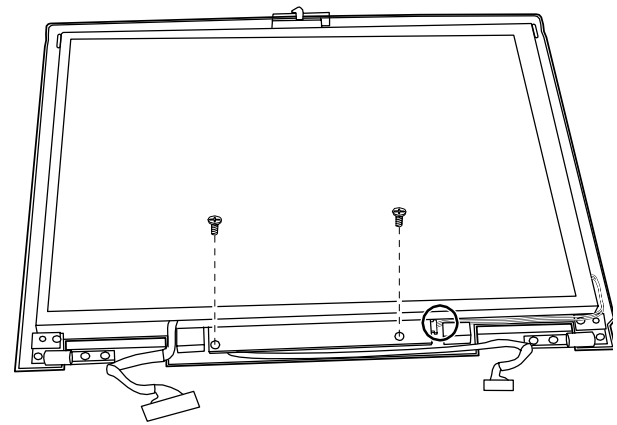


Figure 5-27. Removing the Inverter/LED Board

- **Disassembly**

1. Detach the LCD frame. (See section 5.2.10 Disassembly step 1 and 2.)
2. To remove the inverter/LED board at the bottom side of the LCD , remove two screws and unplug the cable from the board.

- **Reassembly**

1. Reconnect the inverter cable. Fit the inverter/LED board back into place and secure with two screws. (Refer to Figure 5-27.)
2. Place the LCD frame back to the housing. (See section 5.2.10 Reassembly step 2.)

5.2.12 Battery/Touchpad Board

- **Disassembly**

1. Remove the battery pack. (See section 5.2.1 Disassembly.)
2. Remove the CD-ROM/DVD-ROM drive. (See section 5.2.2 Disassembly.)
3. Remove the FDD/HDD module. (See section 5.2.3 Disassembly step 1 and 2.)

4. Remove the CPU module. (See section 5.2.5 Disassembly.)
5. Remove the Modem/LAN card (if exist). (See section 5.2.6 Disassembly.)
6. Remove nine screws fastening the base unit frame. Lift the frame free from the housing. (Refer to Figure 5-28.)
7. After removing the base frame, you will see the battery/touchpad board in between the speakers. To remove the board, first remove three screws and unplug three cables(Refer to Figure 5-29.), then lift it free from the system board.

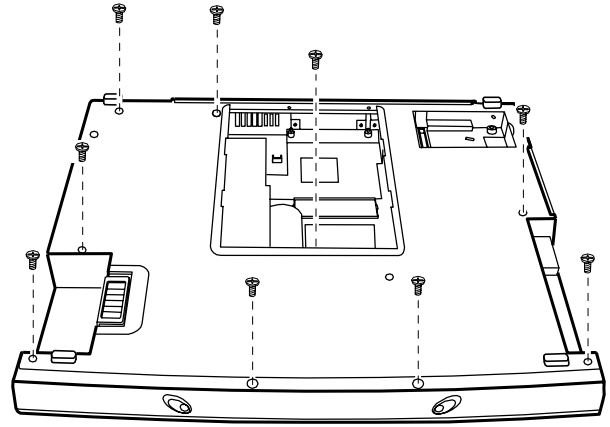


Figure 5-28. Removing the Base Frame Screws

Reassembly

1. Fit the battery/touchpad board into place. Plug three cables and secure the board with three screws. (Refer to Figure 5-29.)
2. Replace the base unit frame. Secure the frame with nine screws. (Refer to Figure 5-28 earlier.)
3. Replace the Modem/LAN card (if exist). (See section 5.2.6 Reassembly.)
4. Replace the CPU module. (See section 5.2.5 Reassembly.)
5. Replace the FDD/HDD module. (See section 5.2.3 Reassembly step 2.)
6. Replace the CD-ROM/DVD-ROM drive. (See section 5.2.2 Reassembly.)
7. Replace the battery pack. (See section 5.2.1 Reassembly.)

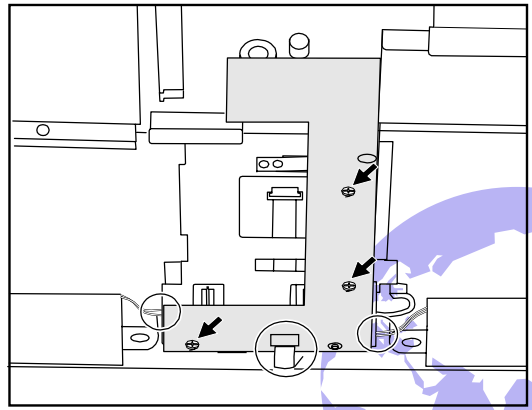


Figure 5-29. Removing the Battery/Touchpad Board

5.2.13 System Board

● **Disassembly**

1. Remove the keyboard. (See section 5.2.7 Disassembly.)
2. Remove one screw fastening the system board. Refer to Figure 5-30.)
3. Put the notebook upside down with care.
4. Remove the battery/touchpad board. (See section 5.2.12 Disassembly.)
5. Remove two screws on the rear side, as well as six screws fastening the metal shield. (Refer to Figure 5-31.)
6. Remove the metal shield. Then you can lift the system board free from the housing.

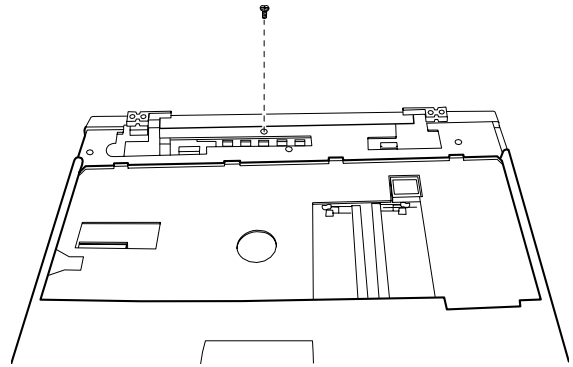


Figure 5-30. Removing One Screw Fastening the System Board

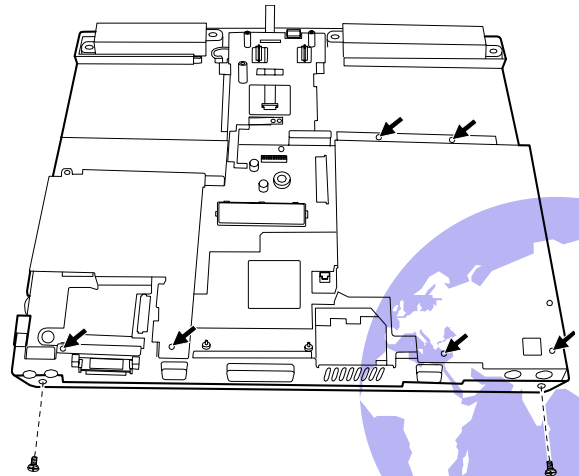


Figure 5-31. Removing Eight Screws Fastening Metal Shield and System Board

● **Reassembly**

1. Fit the system board into the housing and secure with two screws on the rear side. (Refer to Figure 5-31.)
2. Replace the metal shield and secure with six screws. (Refer to Figure 5-31.)
3. Replace the battery/touchpad board. (See section 5.2.12 Reassembly.)
4. Put the notebook surface up. Replace one screw and the keyboard module. (Refer to Figure 5-30 earlier.)

5.2.14 Touchpad Panel

- **Disassembly**

1. Remove the system board. (See section 5.2.13 Disassembly.)
2. The touchpad panel is located in between the speakers. To remove the panel, unfasten three screws and remove the metal cover, then you can lift the panel free from the housing. (Refer to Figure 5-32.)

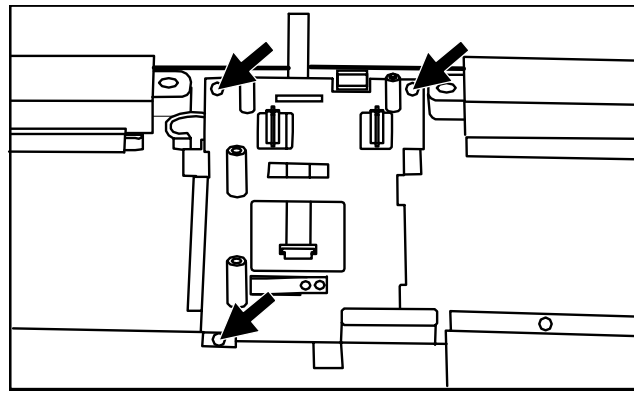


Figure 5-32. Removing Three Screws and Touchpad Panel

- **Reassembly**

1. Fit the touchpad panel back into place. Replace the metal cover and secure with three screws. (Refer to Figure 5-32 earlier.)
2. Replace the system board. (See section 5.2.13 Reassembly.)

6. MAINTENANCE DIAGNOSTICS

6.1 INTRODUCTION

EACH TIME THE COMPUTER IS TURNED ON, THE SYSTEM BIOS RUNS A SERIES OF INTERNAL CHECKS ON THE HARDWARE. THIS POWER-ON SELF TEST (POST) ALLOWS THE COMPUTER TO DETECT PROBLEMS AS EARLY AS THE POWER-ON STAGE. ERROR MESSAGES OF POST CAN ALERT YOU TO THE PROBLEMS OF YOUR COMPUTER.

IF AN ERROR IS DETECTED DURING THESE TESTS, YOU WILL SEE AN ERROR MESSAGE DISPLAYED ON THE SCREEN. IF THE ERROR OCCURS BEFORE THE DISPLAY IS INITIALIZED,THEN THE SCREEN CANNOT DISPLAY THE ERROR MESSAGE. ERROR CODES OR SYSTEM BEEPS ARE USED TO IDENTIFY A POST ERROR THAT OCCURS WHEN THE SCREEN IS NOT AVAILABLE.

THE VALUE FOR THE DIAGNOSTIC PORT (378H) IS WRITTEN AT THE BEGINNING OF THE TEST. THEREFORE, IF THE TEST FAILED, THE USER CAN DETERMINE WHERE THE PROBLEM OCCURRED BY READING THE LAST VALUE WRITTEN TO PORT 378H BY THE PIO DEBUG BOARD PLUG AT PIO PORT.

6.2 ERROR CODES

FOLLOWING IS A LIST OF ERROR CODES IN SEQUENCE DISPLAY ON THE PIO DEBUG BOARD.

CODE	BEEP	Description
00H		START OF BOOT LOADER SECQUENCE.
01H		DISABLE A20 THROUGH A20, NOT SEND.
02H	.._.	INITIALIZE CHIPSET OR BIOS NOT SHADOWED.
03H		PERFORM CONVENTIONAL RAM TEST WITH CROSSED-PATTERN R/W.
04H	._..	MOVE BOOT LOADER TO THE RAM OR BIOS CHECKSUM BAD.
05H		START POINT OF EXECUTION OF BOOT LOADER IN RAM.
06H		PERFORM PNP INITIALIZATION FOR CRYSTAL AUDIO CHIP OR CHECK
		OVERRIDE OPTION, NOT SEND.
07H		SHADOW SYSTEM BIOS.
08H		CHECKSUM SYSTEM BIOS ROM, NOT SEND.
09H		PROCEED WITH NORMAL BOOT.
0AH		PROCEED WITH CRISIS BOOT.
0FH	——	NO RAM OR DRAM SIZING.
10H		INITIAL L1, L2 CACHE, MAKE STACK AND DIAGNOSE CMOS.
11H		TURN OFF FAST A20 FOR FOR POST. RESET GDTS, 8259S QUICKLY.
12H		SIGNAL POWER ON RESET AT CMOS.
13H		INITIALIZE THE CHIPSET, (SDRAM).***SOLUTION: TRY TO CLEAR CMOS***
14H		SEARCH FOR ISA BUS VGA ADAPTER.
15H		RESET COUNTER/TIMER 1.
16H		USER REGISTER CONFIG THROUGH CMOS.
18H		DISPATCH TO 1ST 64K RAM TEST.
19H		CHECKSUM THE ROM.
1AH		RESET PIC'S(8259).
1BH		INITIALIZE VIDEO ADAPTER(S).
1CH		INITIALIZE VIDEO (6845 REGS).
1DH		INITIALIZE COLOR ADAPTER.
1EH		INITIALIZE MONOCHROME ADAPTER.
1FH		TEST 8237A PAGE REGISTERS.
20H		PERFORM KEYBOARD SELF TEST.
21H		TEST & INITIALIZE KEYBOARD CONTROLLER.
22H		CHECK IF CMOS RAM VALID.
23H		TEST BATTER FAIL & CMOS X-SUM.
24H		TEST THE DMA CONTROLLER.
25H		INITIALIZE 8237A CONTROLLER.
26H		INITIALIZE INTERRUPT VECTORS TABLE.
27H		RAM QUICK SIZING.

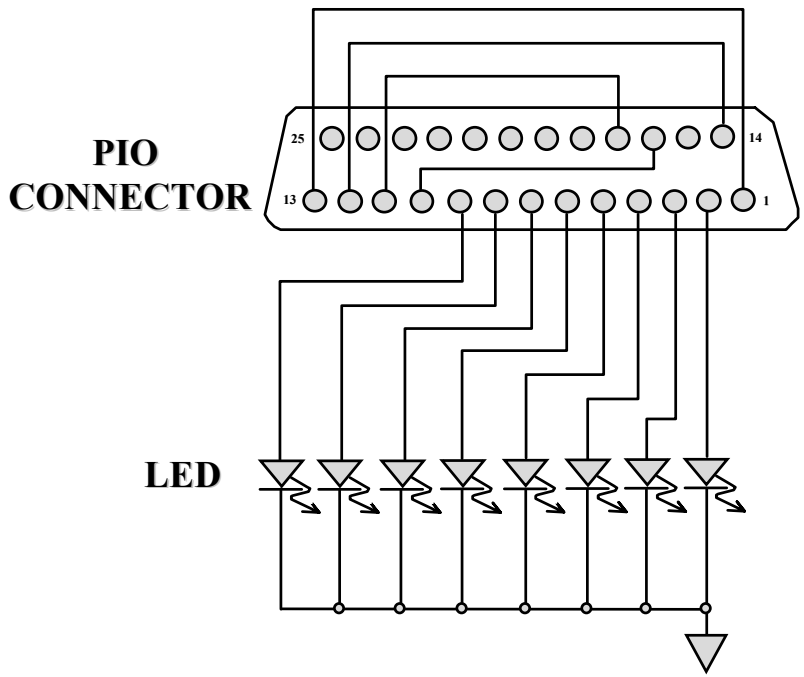
CODE	BEEP	Description
28H		PROTECTED MODE ENTERED SAFELY.
29H		RAM TEST COMPLETED.
2AH		PROTECTED MODE EXIT SUCCESSFUL .
2BH		SETUP SHADOW.
2CH		PREPARE TO INITIALIZE VIDEO.
2DH		SEARCH FOR MONOCHROME ADAOTER.
2EH		SEARCH FOR COLOR ADAPTER, VGA INITIALIZE.
2FH		SIGN-ON MESSAGES DISPLAYED.
30H		SPECIAL INIT OF KEYBOARD CONTROLLER.
31H		TEST IF KEYBOARD PRESENT.
32H		TEST KEYBOARD INTERRUPT.
33H		TEST KEYBOARD COMMAND BYTE.
34H		TEST, BLANK AND COUNT ALL RAM.
35H		PROTECTED MODE ENTERED SAFELY(2).
36H		RAM TEST COMPLETED.
37H		PROTECTED MODE EXIT SUCCESSFUL .
38H		UPDATE KEYBOARD OUTPUT PORT TO DISABLE GATE OF A20.
39H		SETUP CACHE CONTROLLER.
3AH		TEST IF 18.2HZ PERIODIC WORKING.
3BH		INITIALIZE BIOS DATA AREA AT 40:0.
3CH		INITIALIZE THE HARDWARE INTERRUPT VECTOR.
3DH		SEARCH AND INIT THE MOUSE.
3EH		UPDATE NUMLOCK STATUS.
3FH		OEM INITIALIZATION OF COMM AND LPT PORTS.
40H		CONFIGURE THE COMM AND LPT PORTS.
41H		INITIALIZE THE FLOPPIES.
42H		INITIALIZE THE HARD DISK.
43H		INITIALIZE ADDITIONAL ROMS.
44H		OEM'S INIT OF POWER MANAGEMENT, (CHECK SMI).
45H		UPDATE NUMLOCK STATUS.
46H		TEST FOR COPROCESSOR INSTALLED.
47H		OEM FUNCTIONS BEFORE BOOT(PCMCIA, CARDBUSS).
48H		DISPATCH TO OPERATION SYSTEM BOOT.
49H		JUMP INTO BOOTSTRAP CODE.
4AH		OEM'S INIT OF PM WITH USB.
FO~F1H	....	RMA TEST FAILED.

6.3 PIO PORT (378H) DIAGNOSTIC TOOLS

6.3.1 PARTS USED:

- LED * 8
- PIO CONNECTOR * 1

6.3.2 CIRCUIT:



PIN1 : STROBE ⟷ PIN 13 : SLCT

PIN10: ACK# ⟷ PIN 16 : INT#

PIN11: BUSY ⟷ PIN 17 : SELIN#

PIN12: PTERR ⟷ PIN 14 : AUTOFD#

PIN{9:2}: PD{7:0}

7. TROUBLE SHOOTING

7.1 NO POWER

7.2 NO DISPLAY

7.3 VGA CONTROLLER FAILURE

7.4 LCD NO DISPLAY

7.5 EXTERNAL MONITOR NO DISPLAY

7.6 MEMORY TEST ERROR

7.7 KEYBOARD TEST ERROR

7.8 TRACK PAD/BALL TEST ERROR

7.9 DISKETTE DRIVE TEST ERROR

7.10 HARD DRIVE OR CD-ROM TEST ERROR

7.11 CMOS TEST ERROR

7.12 SIO PORT TEST ERROR

7.13 PIO PORT TEST ERROR

7.14 AUDIO DRIVE FAILURE

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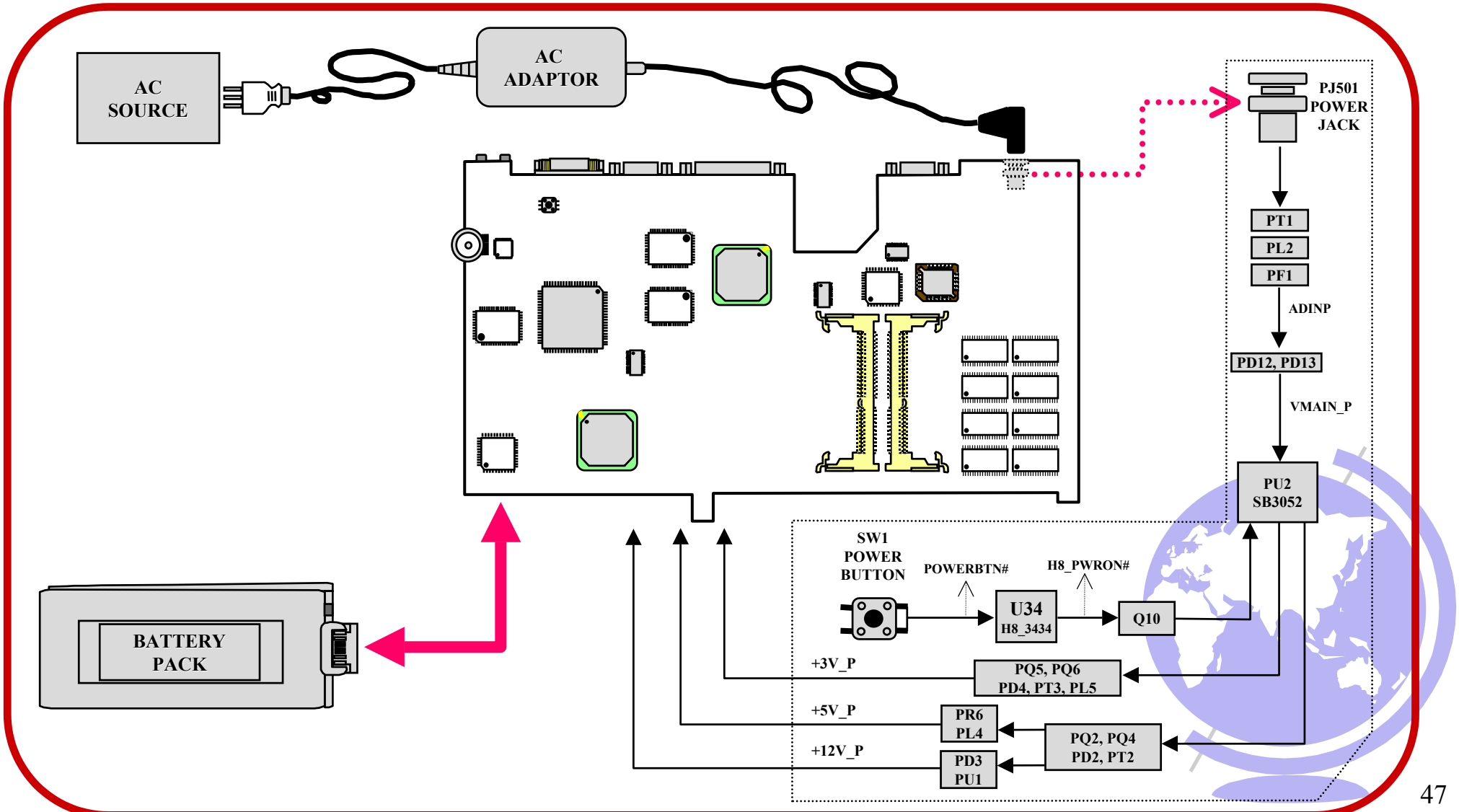
7.1 NO POWER

SYMPTOM:

WHEN THE POWER BUTTON IS PRESSED, NOTHING HAPPENS, POWER INDICATOR IS NOT LIGHT UP.



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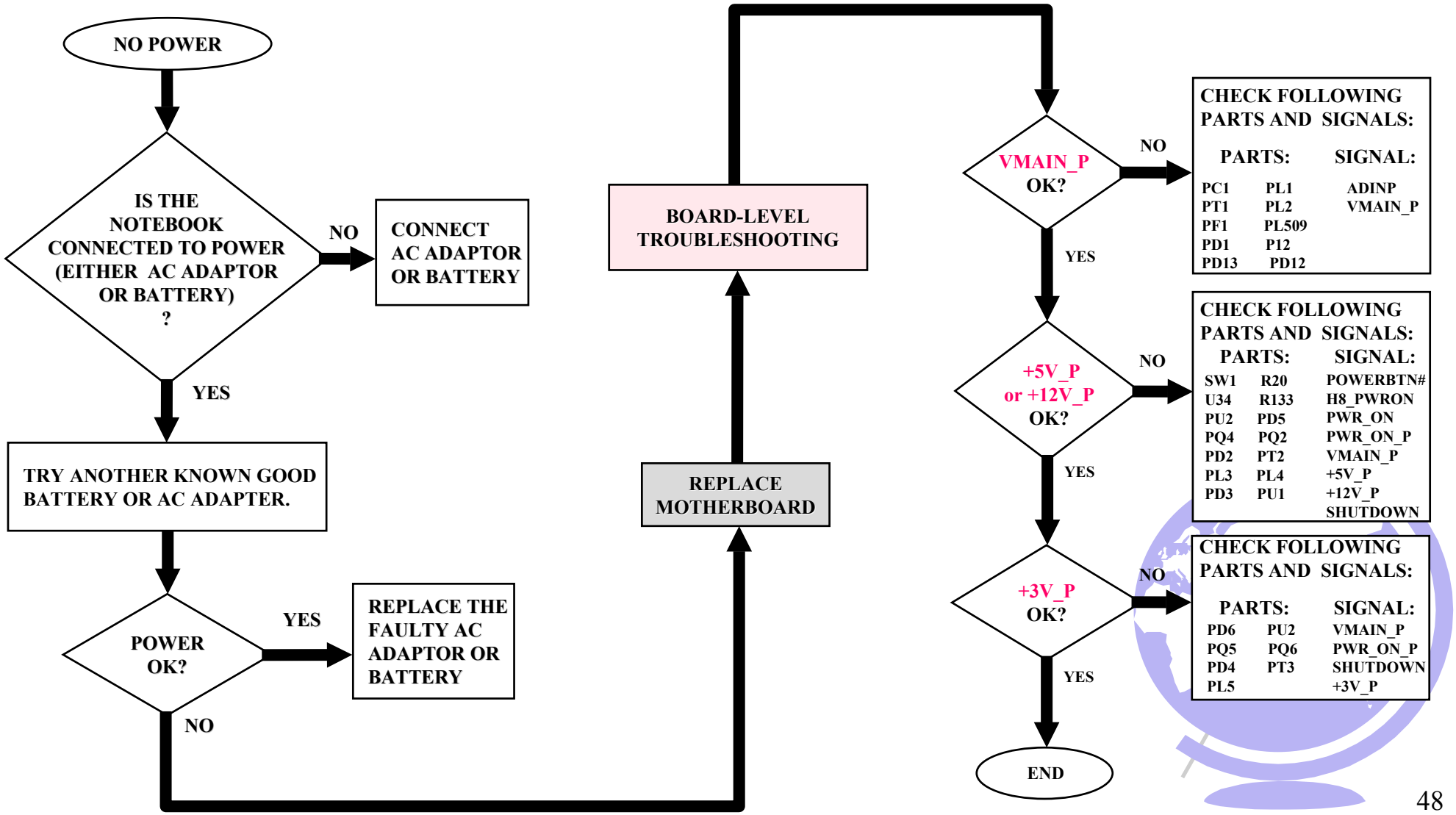
SYMPTOM:

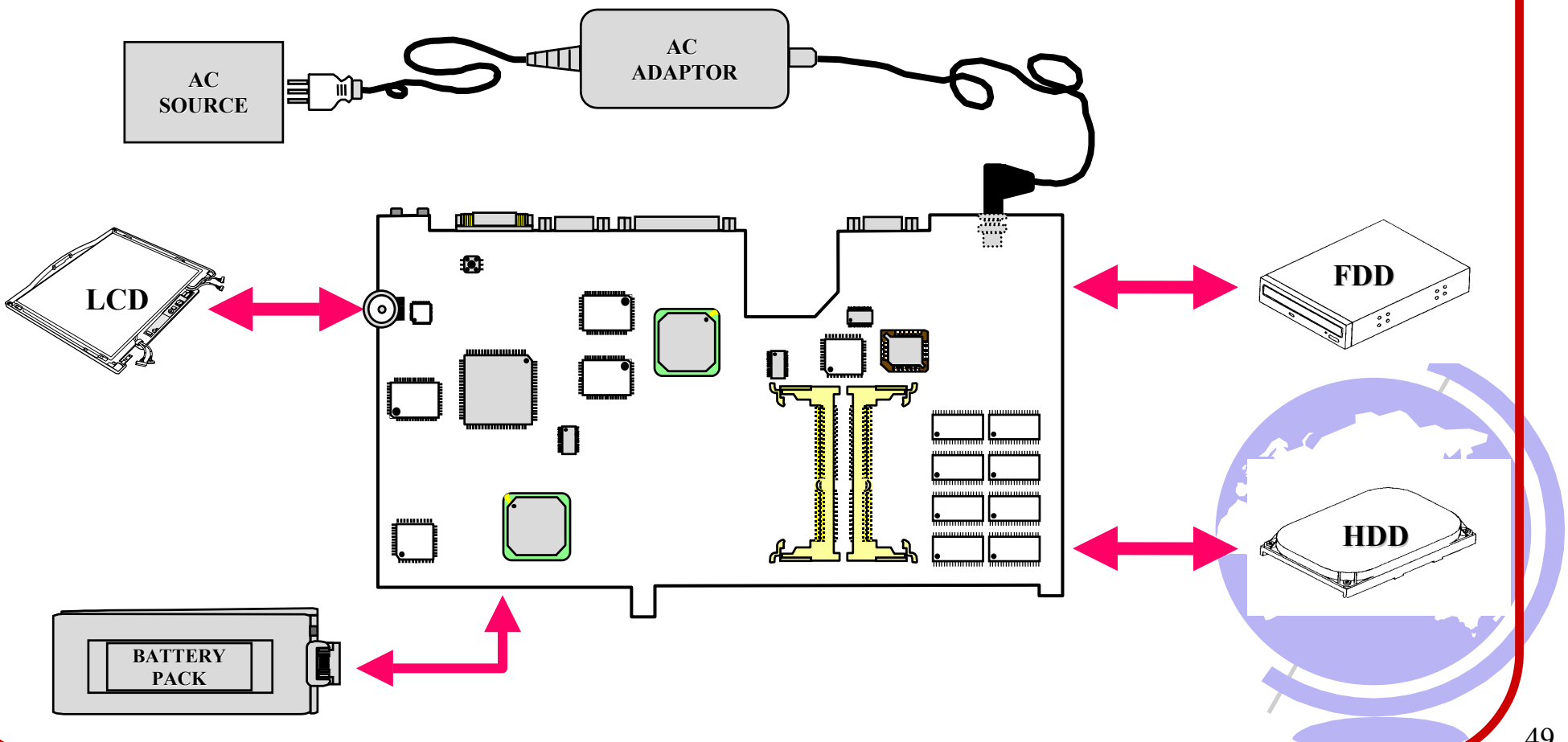
WHEN THE POWER BUTTON IS PRESSED, NOTHING HAPPENS, POWER INDICATOR IS NOT LIGHT UP.



7.2 NO DISPLAY (SYSTEM FAILURE)

SYMPTOM:

THERE IS NO DISPLAY ON BOTH LCD AND MONITOR AFTER POWER ON ALTHOUGH THE LCD AND MONITOR ARE KNOWN-GOOD.



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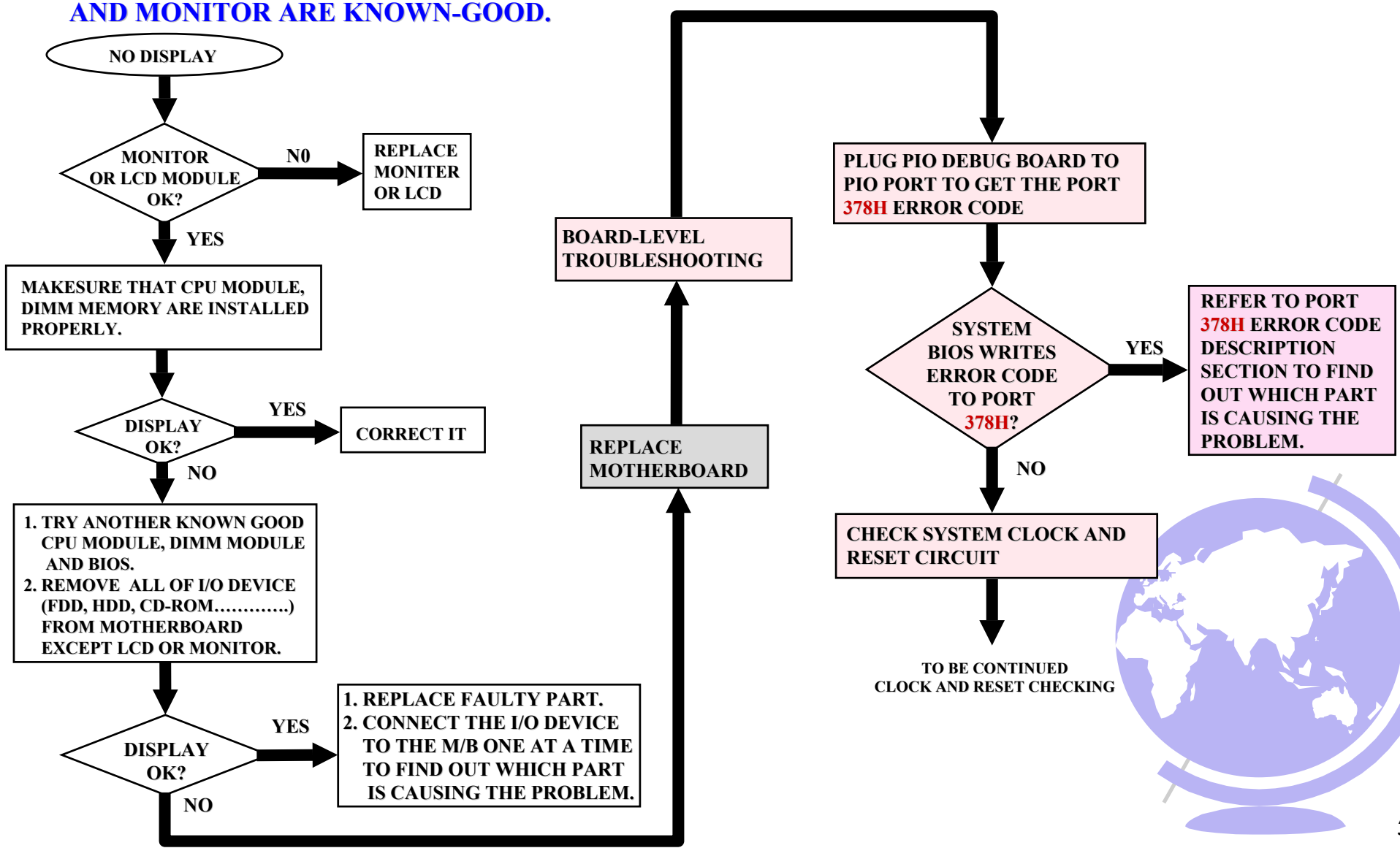

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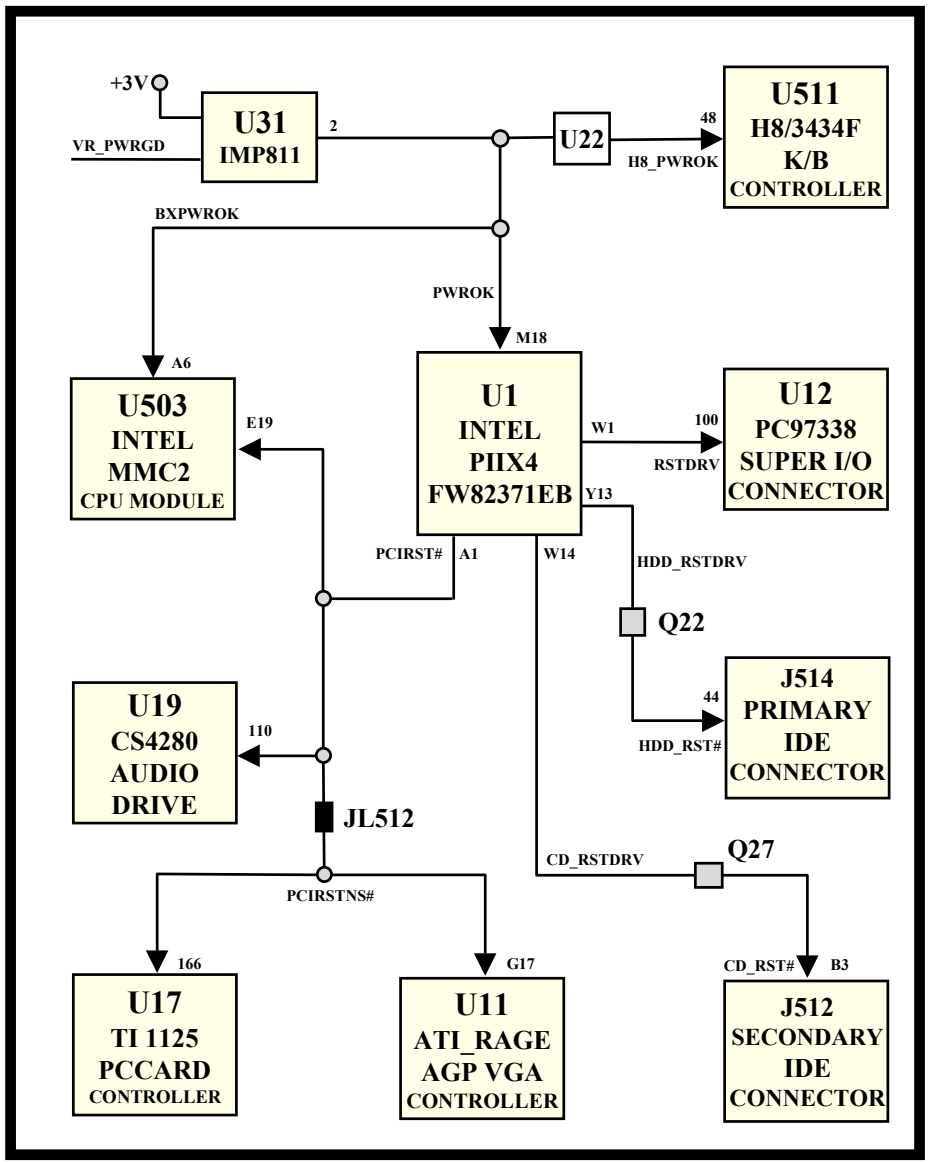
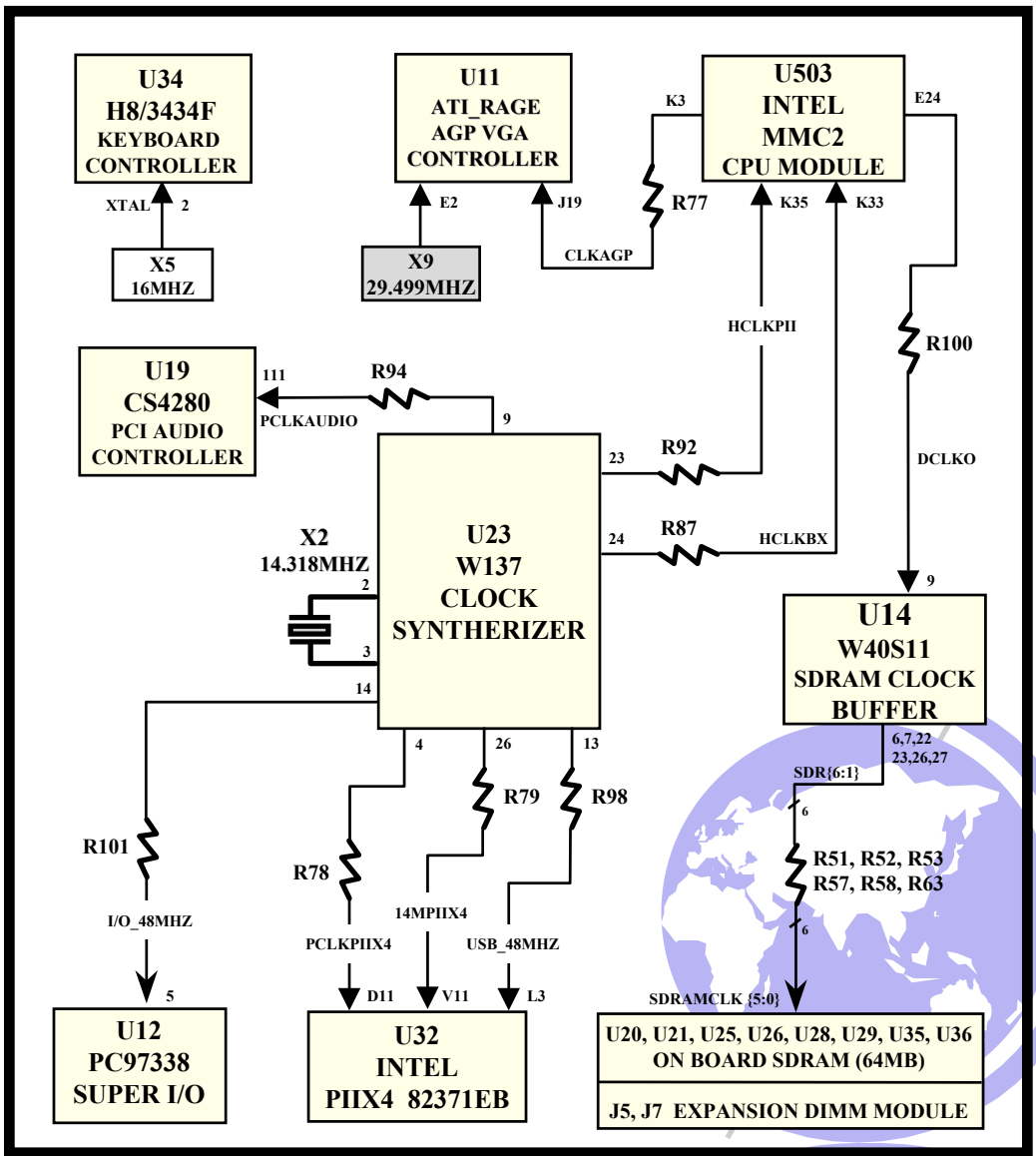
7.2 NO DISPLAY (SYSTEM FAILURE)

*******CLOCK AND RESET CIRCUIT CHECKING*******

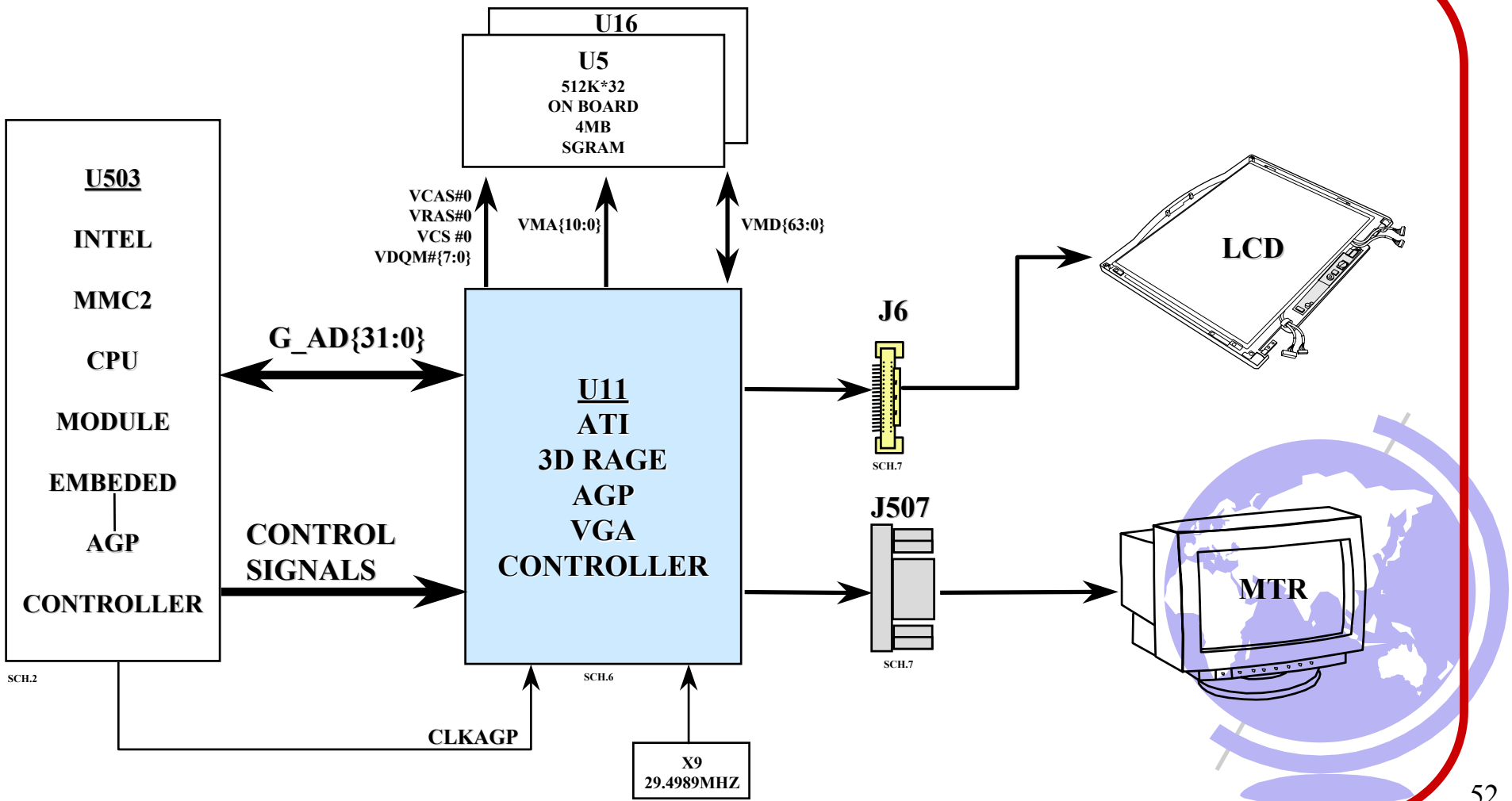




7.3 VGA CONTROLLER FAILURE

SYMPTOM:

THERE IS NO DISPLAY ON BOTH LCD AND MONITOR ALTHOUGH POWER-ON-SELF-TEST IS PASSED OR THE PIO DEBUG BOARD SHOWS THE PORT 378H ERROR CODE IS STOPPED AT 2CH.



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SYMPTOM:

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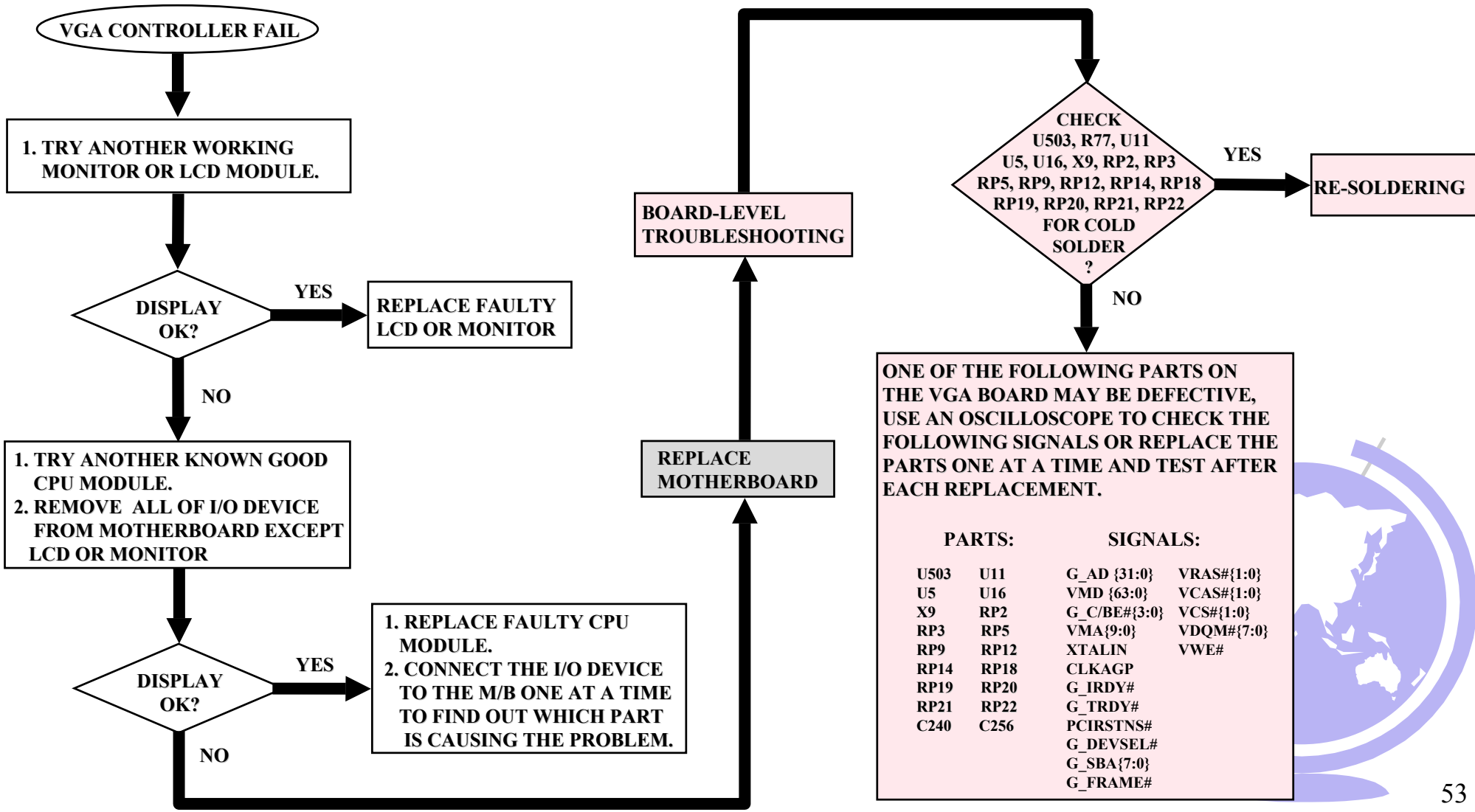
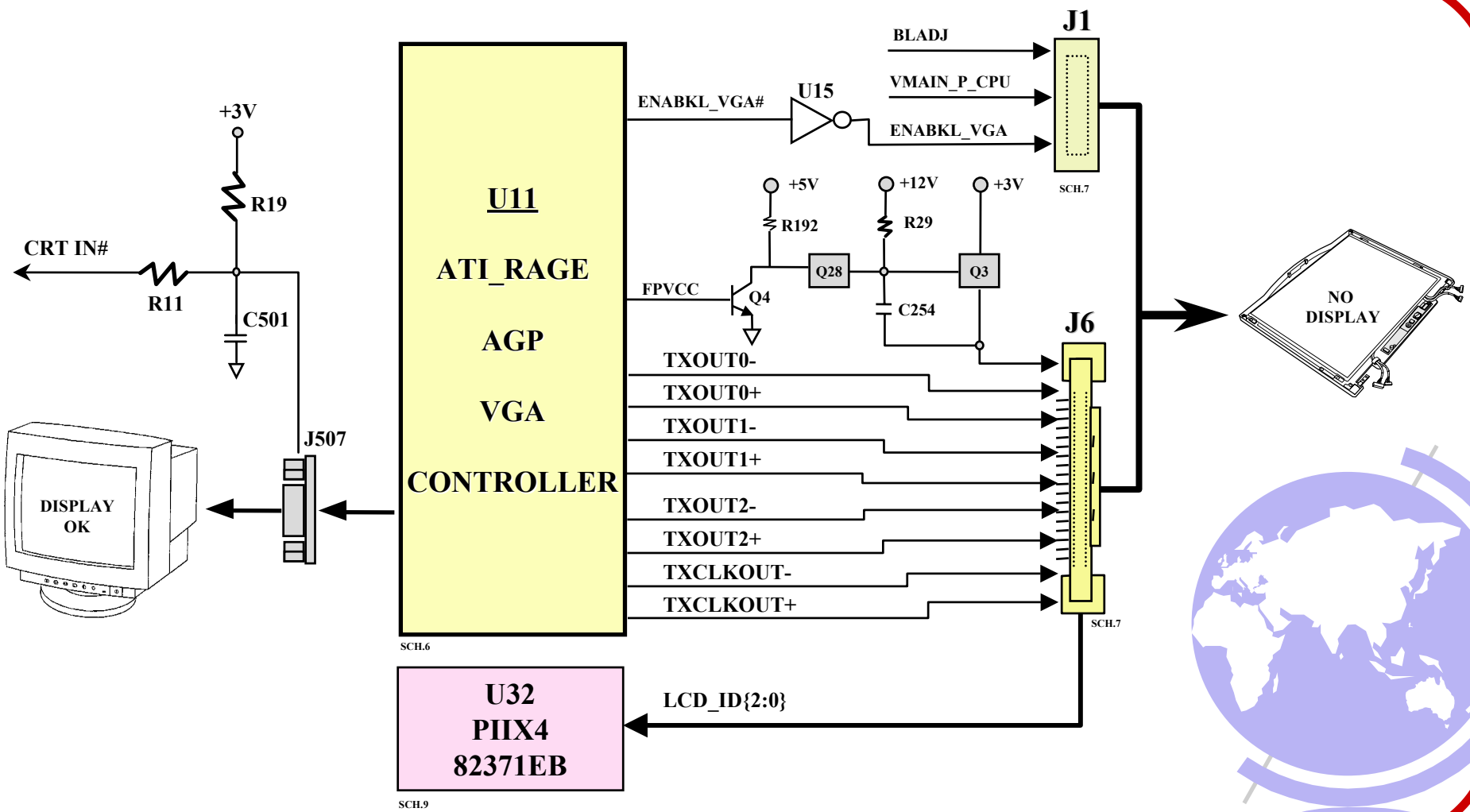


7.4 LCD NO DISPLAY OR PICTURE ABNORMAL

SYMPTOM:

THE LCD SHOWS NOTHING OR ABNORMAL PICTURE, BUT IT IS OK FOR EXTERNAL MONITOR.

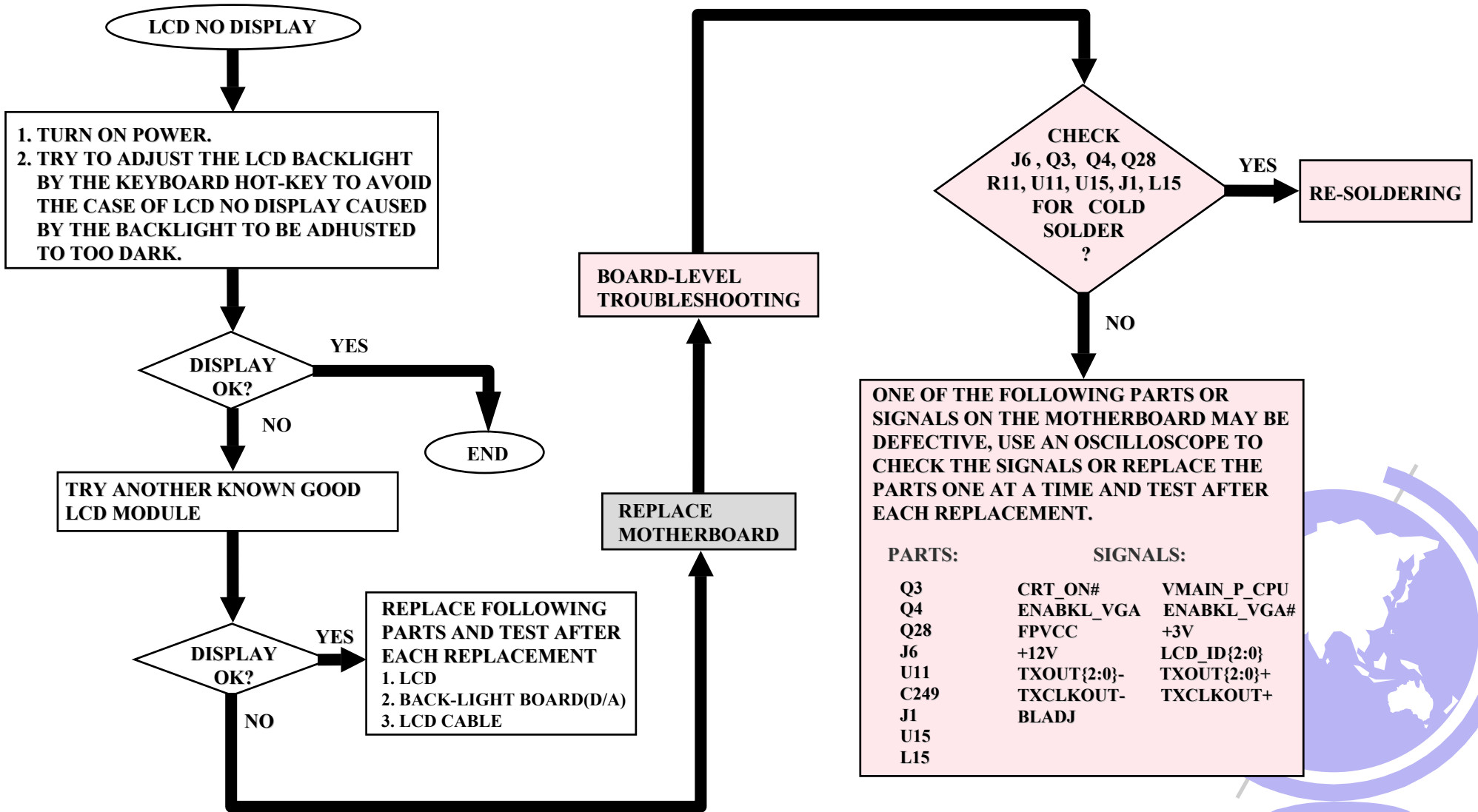


6020 N/B MAINTENANCE

7.4 LCD NO DISPLAY OR PICTURE ABNORMAL

SYMPTOM:

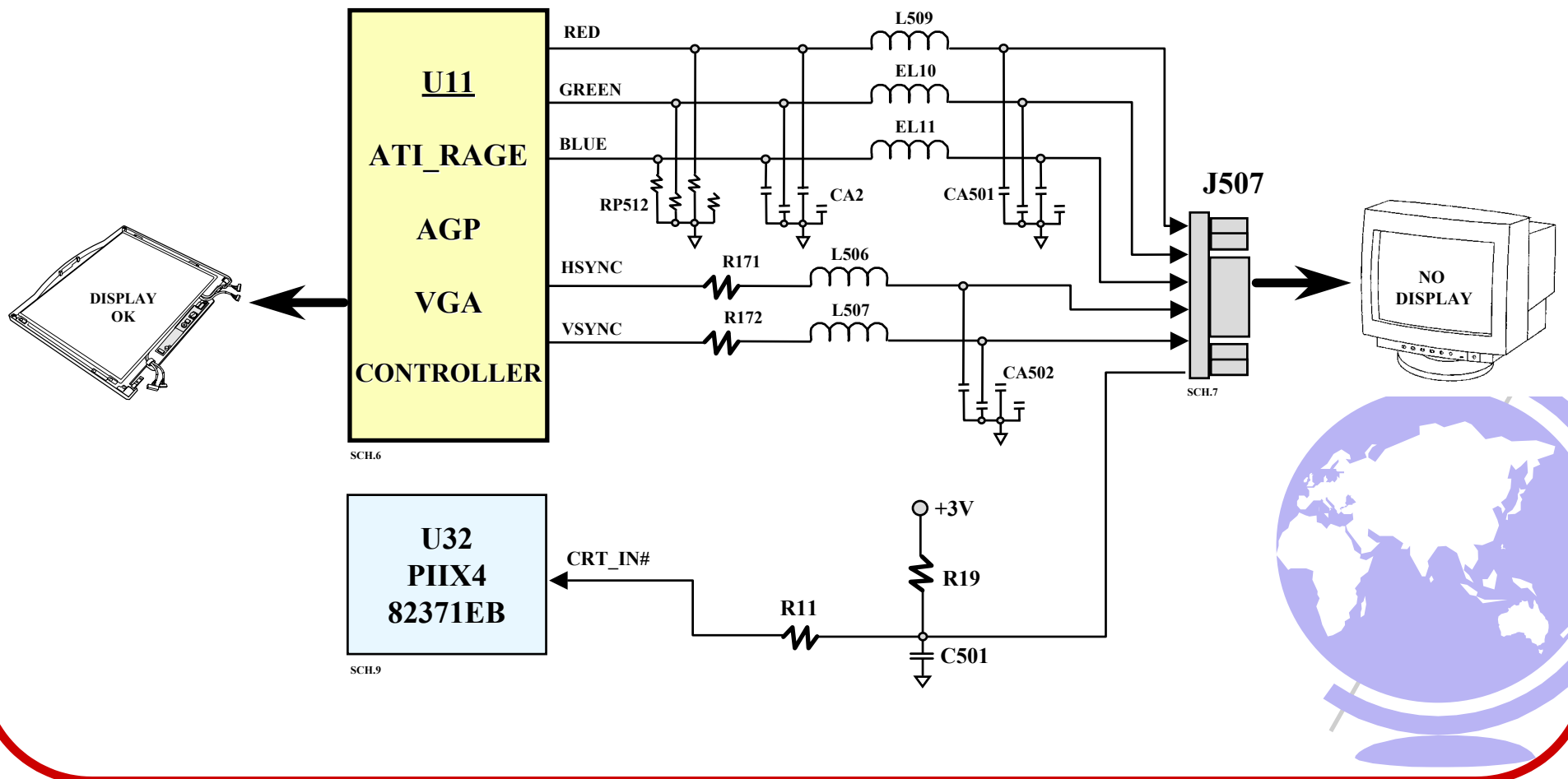
THE LCD SHOWS NOTHING OR ABNORMAL PICTURE, BUT IT IS OK FOR EXTERNAL MONITOR.



7.5 EXTERNAL MONITOR NO DISPLAY OR COLOR ABNORMAL

SYMPTOM:

THE CRT MONITOR SHOWS NOTHING OR ABNORMAL COLOR, BUT IT IS OK FOR LCD.



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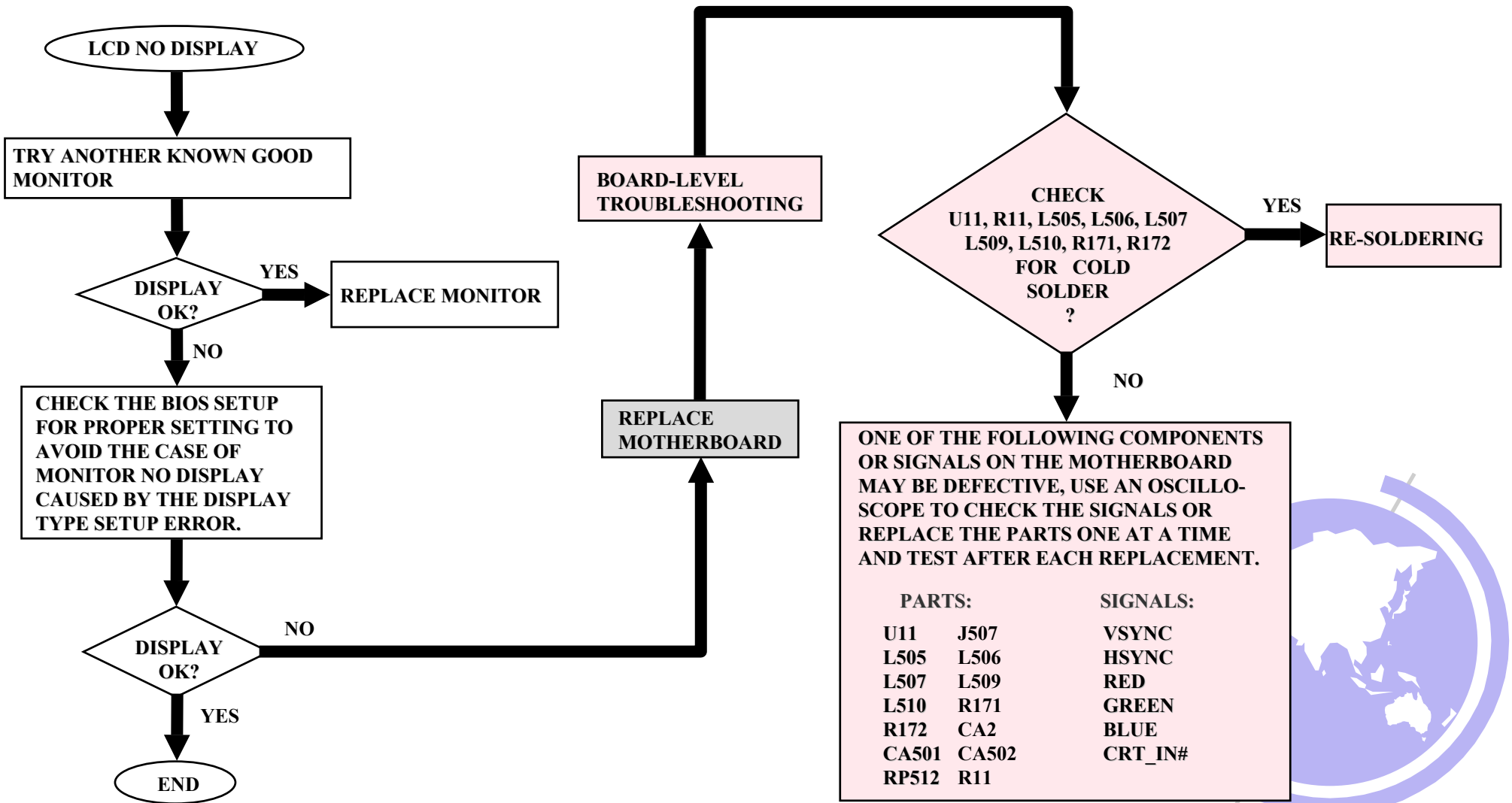
7.5 EXTERNAL MONITOR NO DISPLAY OR COLOR ABNORMAL

SYMPTOM:

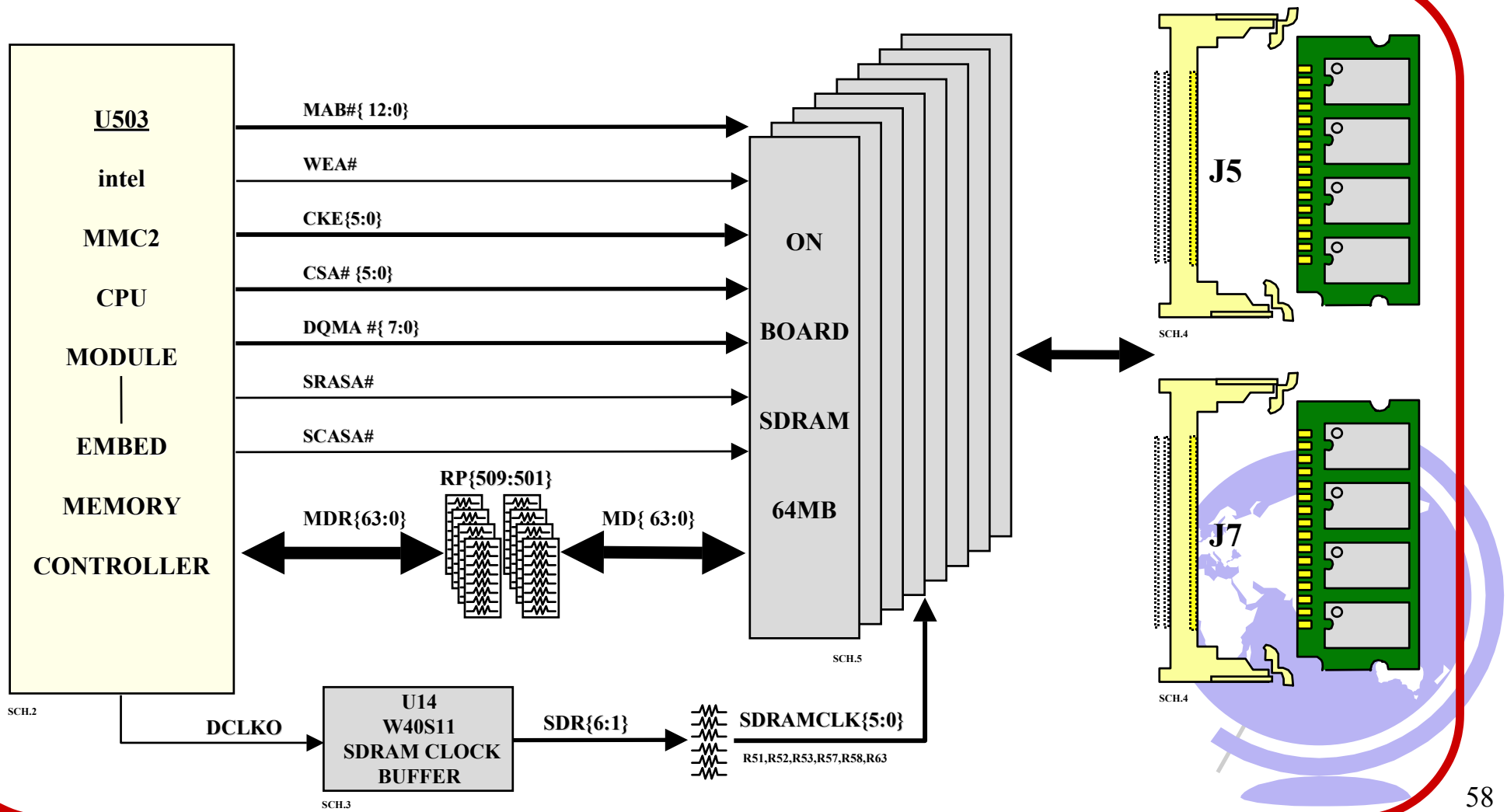
THE CRT MONITOR SHOWS NOTHING OR ABNORMAL COLOR, BUT IT IS OK FOR LCD.



7.6 MEMORY TEST ERROR

SYMPTOM:

PIO DEBUG BOARD SHOWS THE PORT 378H ERROR CODE IS STOPPED AT 0FH OR ERROR MESSAGE OF MEMORY FAILURE IS SHOWN.



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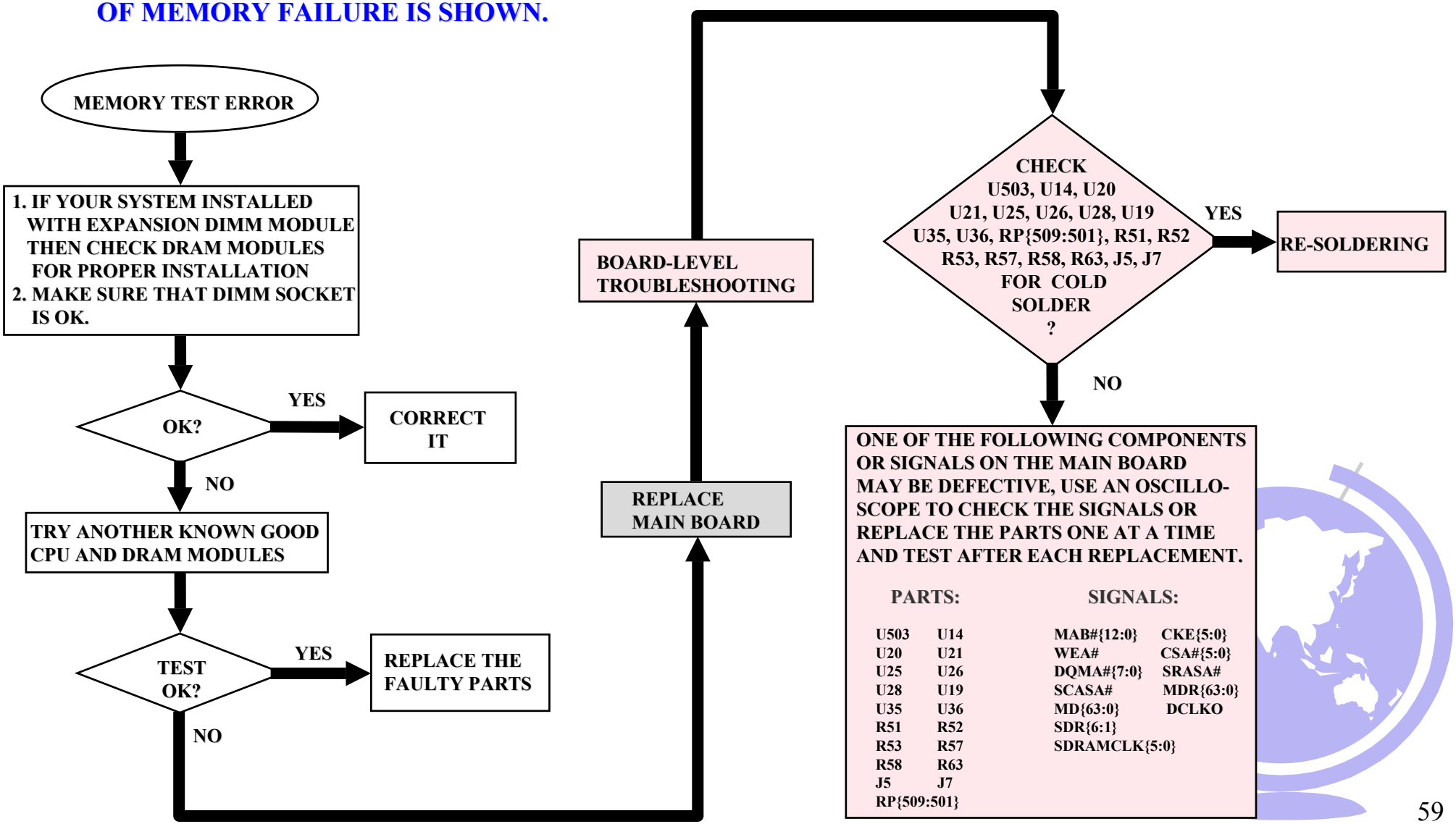
SYMPTOM:

PIO DEBUG BOARD SHOWS THE PORT 378H ERROR CODE IS STOPPED AT 0FH OR ERROR MESSAGE OF MEMORY FAILURE IS SHOWN.



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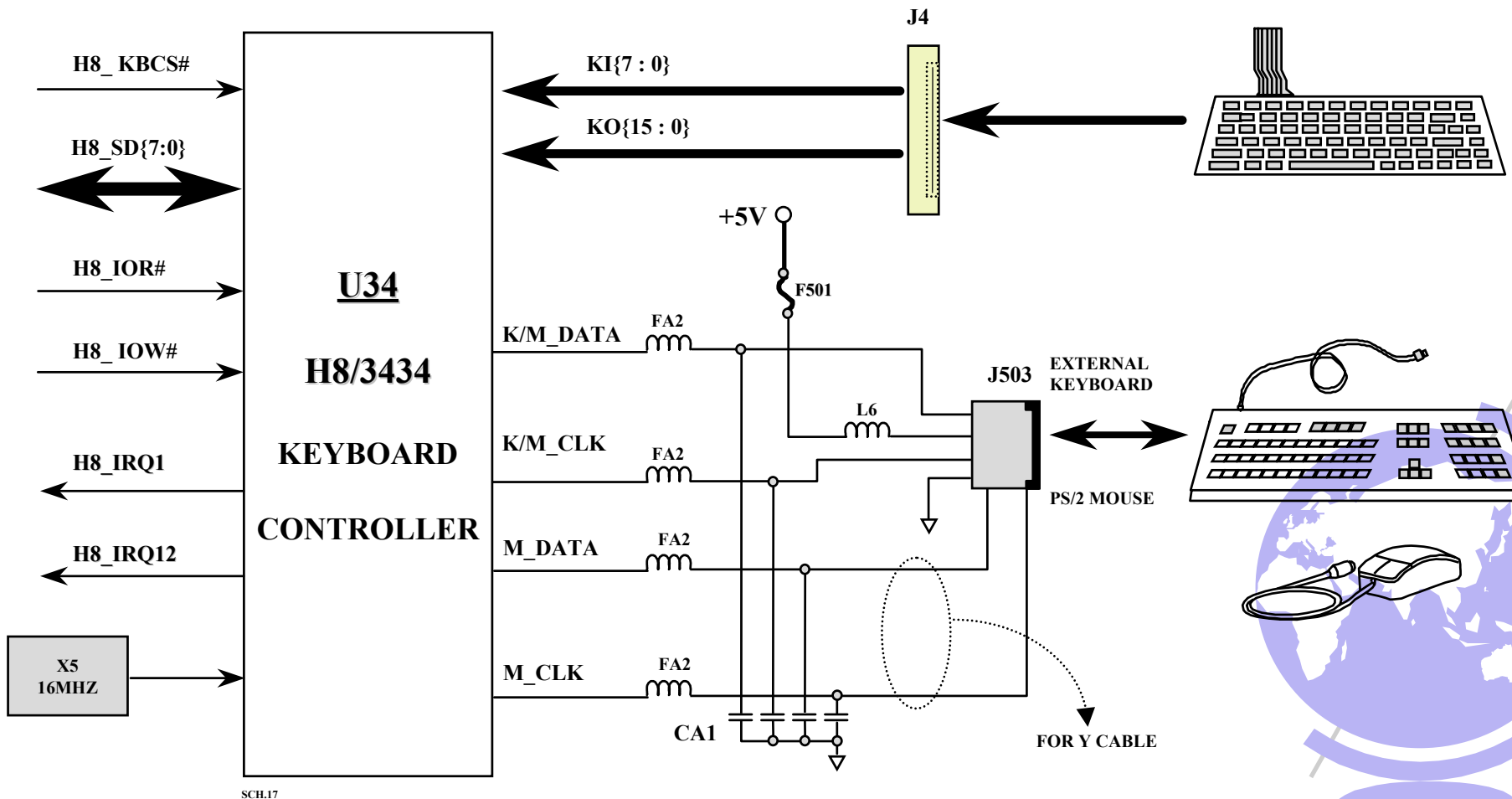
7.7 KEYBOARD TEST ERROR (INCLUDING EXTERNAL KEYBOARD & PS/2 MOUSE)

SYMPTOM:

1. ERROR MESSAGE OF KEYBOARD FAILURE IS SHOWN OR ANY KEY DOESN'T WORK.
2. PIO DEBUG BOARD SHOWS THE PORT 378H ERROR CODE IS STOPPED AT 20H OR 21H.



6020 N/B MAINTENANCE

7.7 KEYBOARD TEST ERROR (INCLUDING EXTERNAL KEYBOARD & PS/2 MOUSE)

SYMPTOM:

1. ERROR MESSAGE OF KEYBOARD FAILURE IS SHOWN OR ANY KEY DOESN'T WORK.
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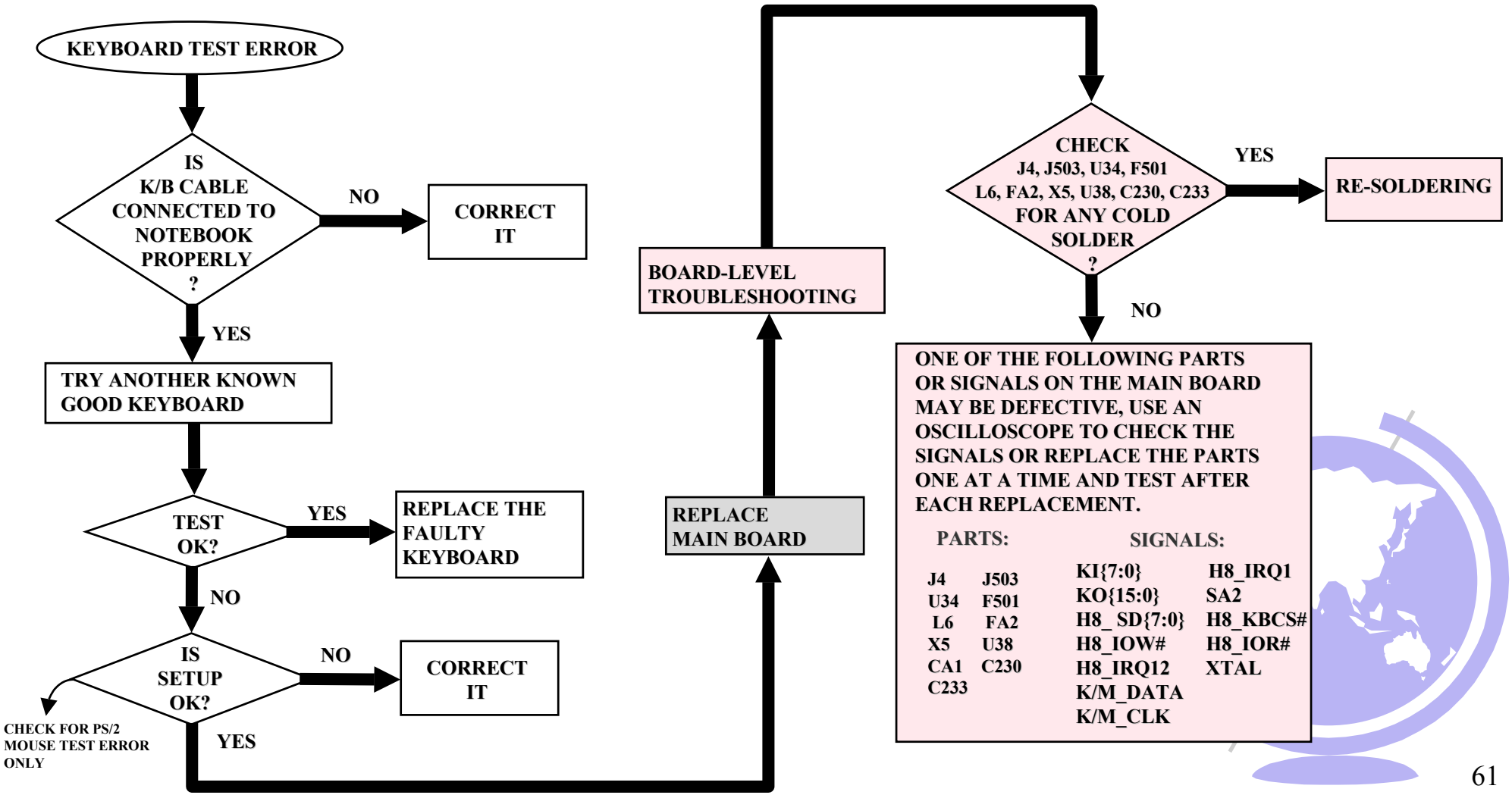
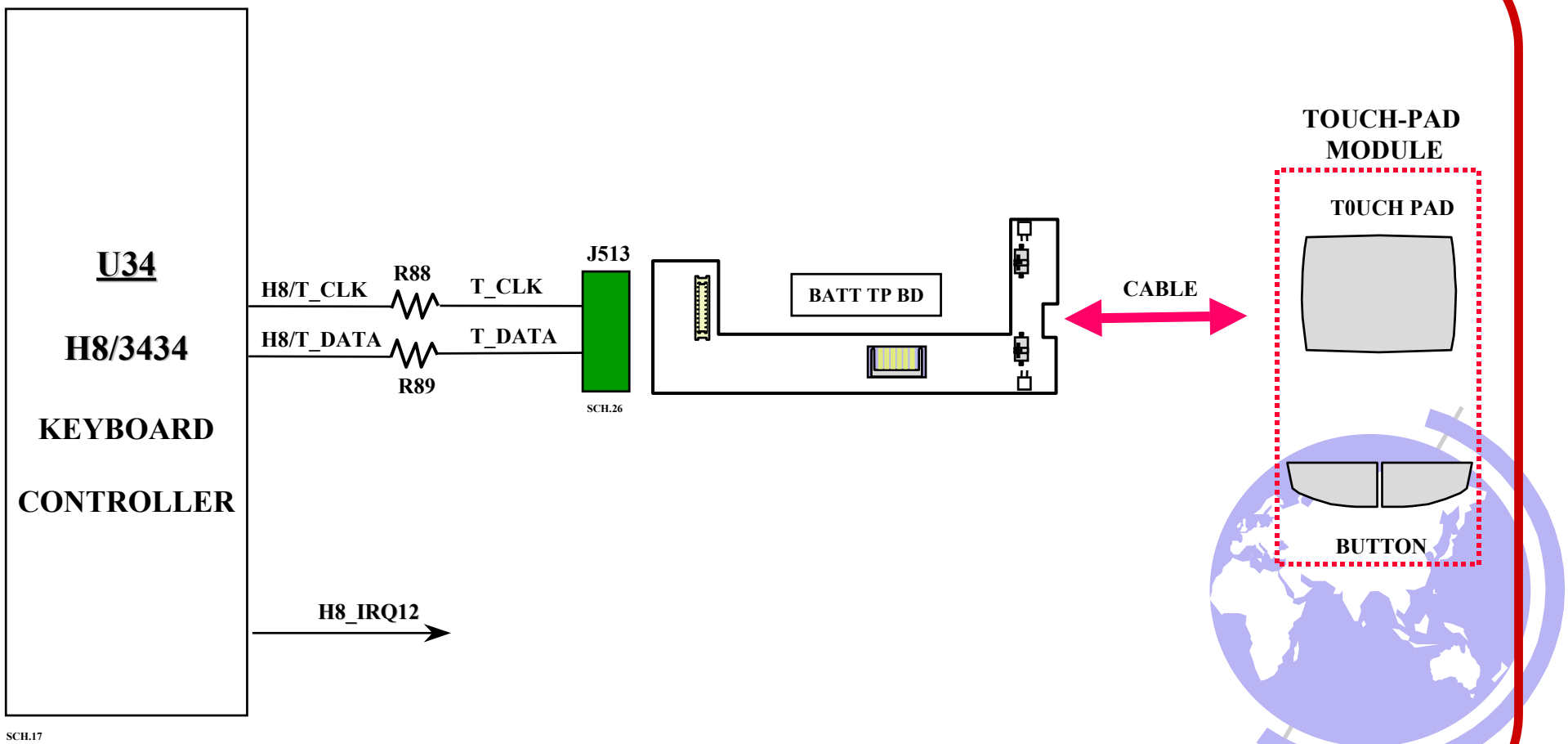


7.8 TOUCH-PAD TEST ERROR

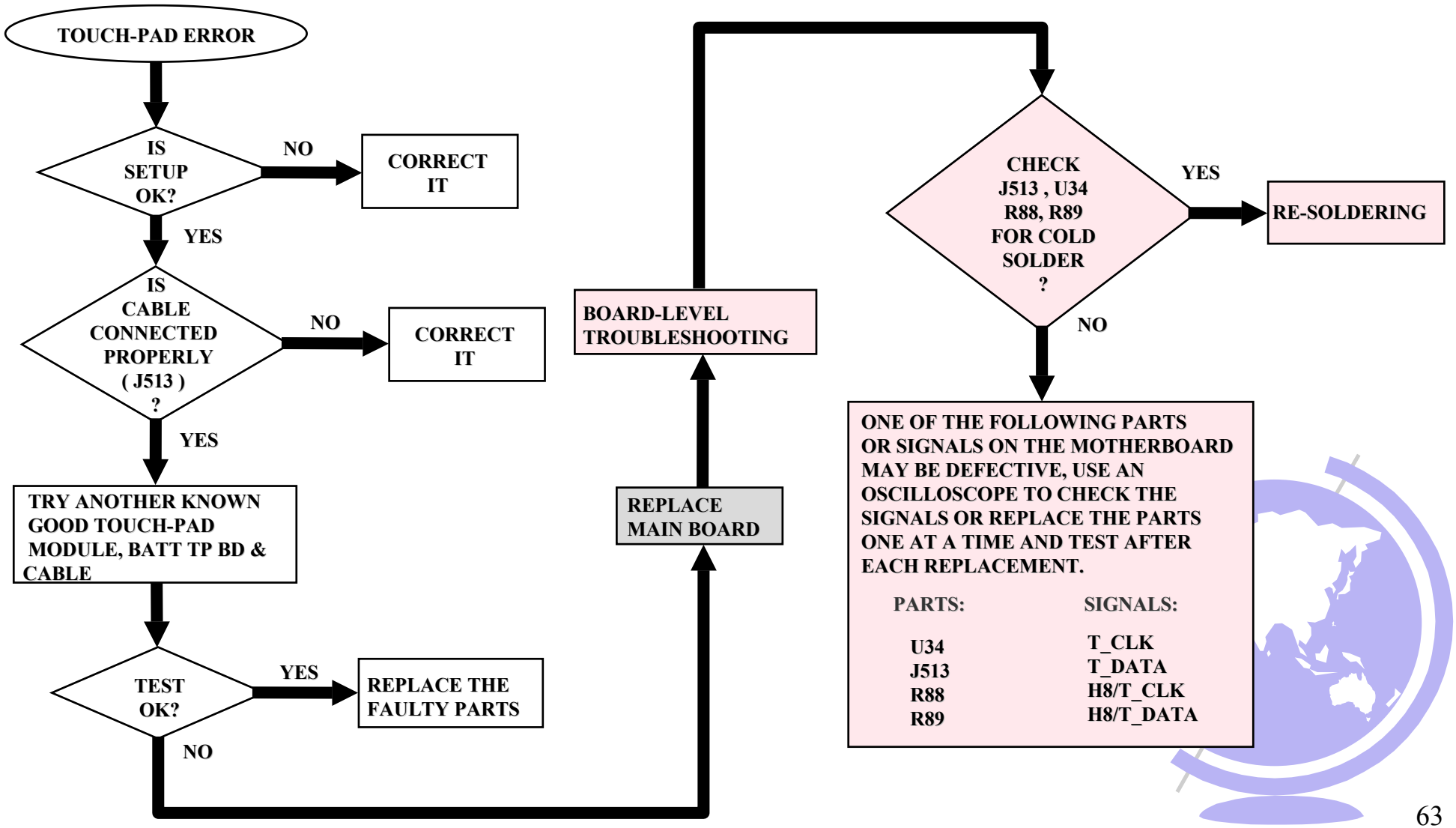
SYMPTOM:
AN ERROR MESSAGE IS SHOWN WHEN THE TOUCH-PAD IS ENABLED.



6020 N/B MAINTENANCE

7.8 TOUCH-PAD TEST ERROR

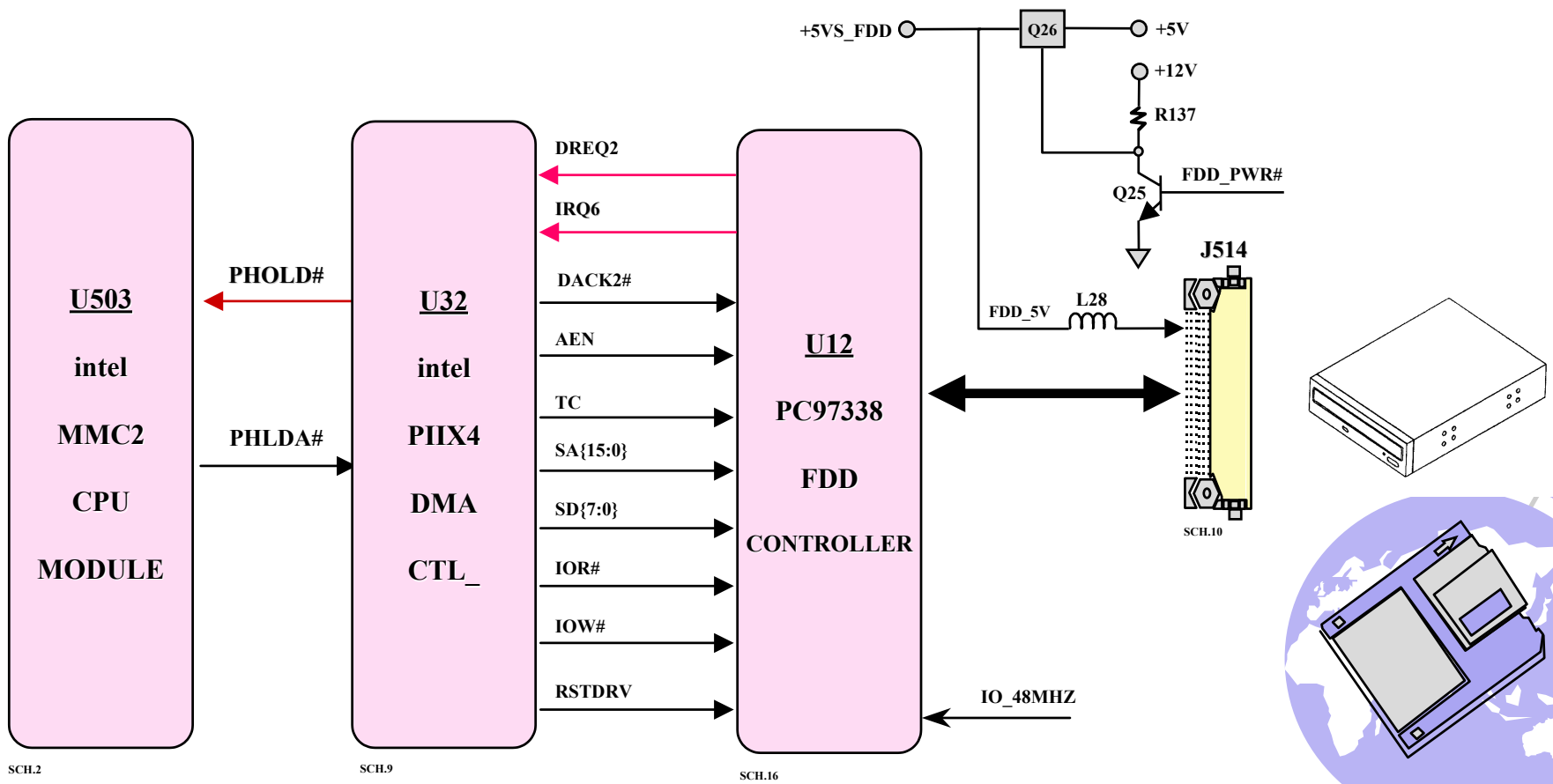
SYMPTOM:
AN ERROR MESSAGE IS SHOWN WHEN THE TOUCH-PAD IS ENABLED.



7.9 DISKETTE DRIVE TEST ERROR

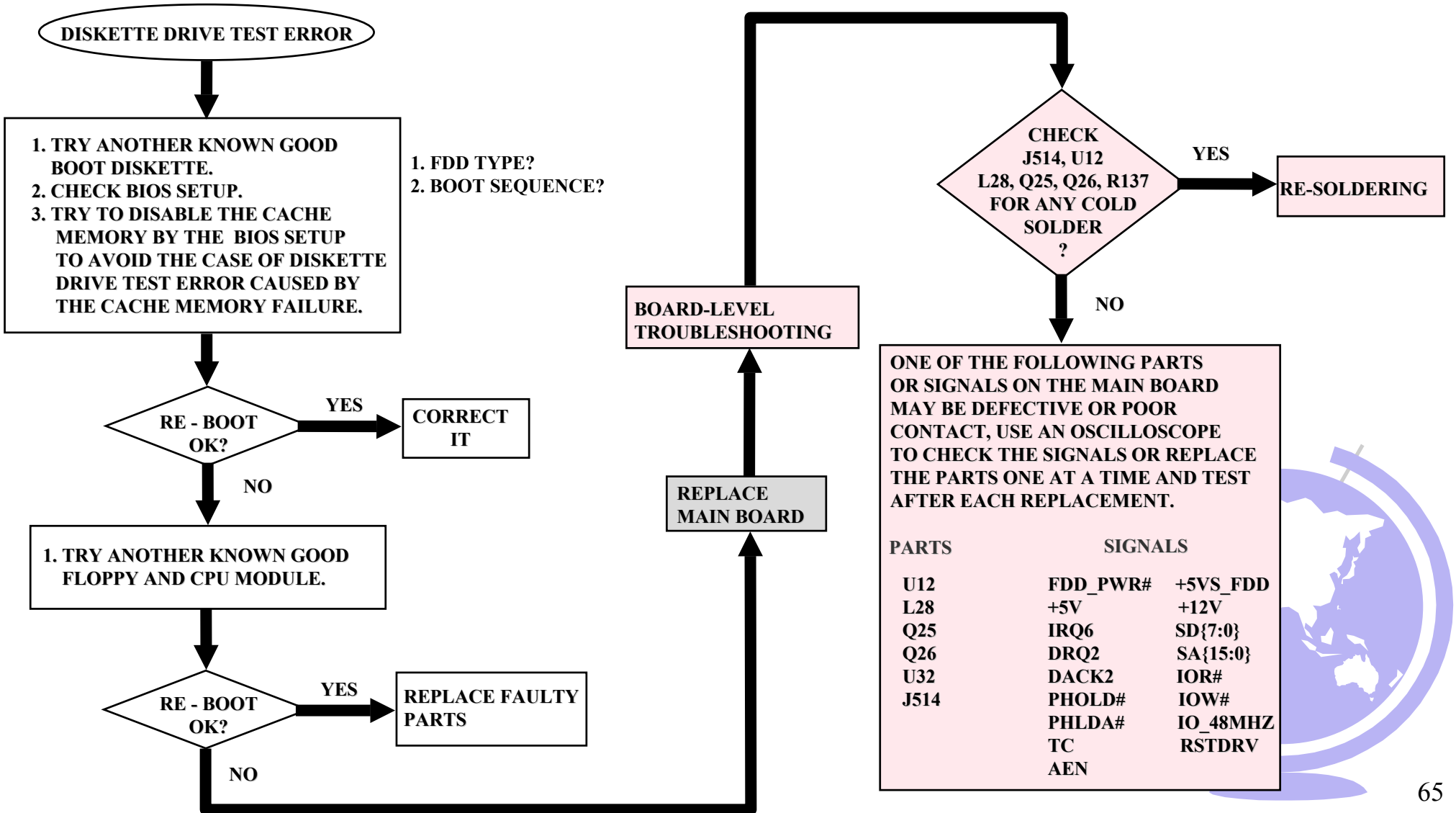
SYMPTOM:

AN ERROR MESSAGE IS SHOWN WHILE LOADING DATA FROM DISK TO SYSTEM.



7.9 DISKETTE DRIVE TEST ERROR

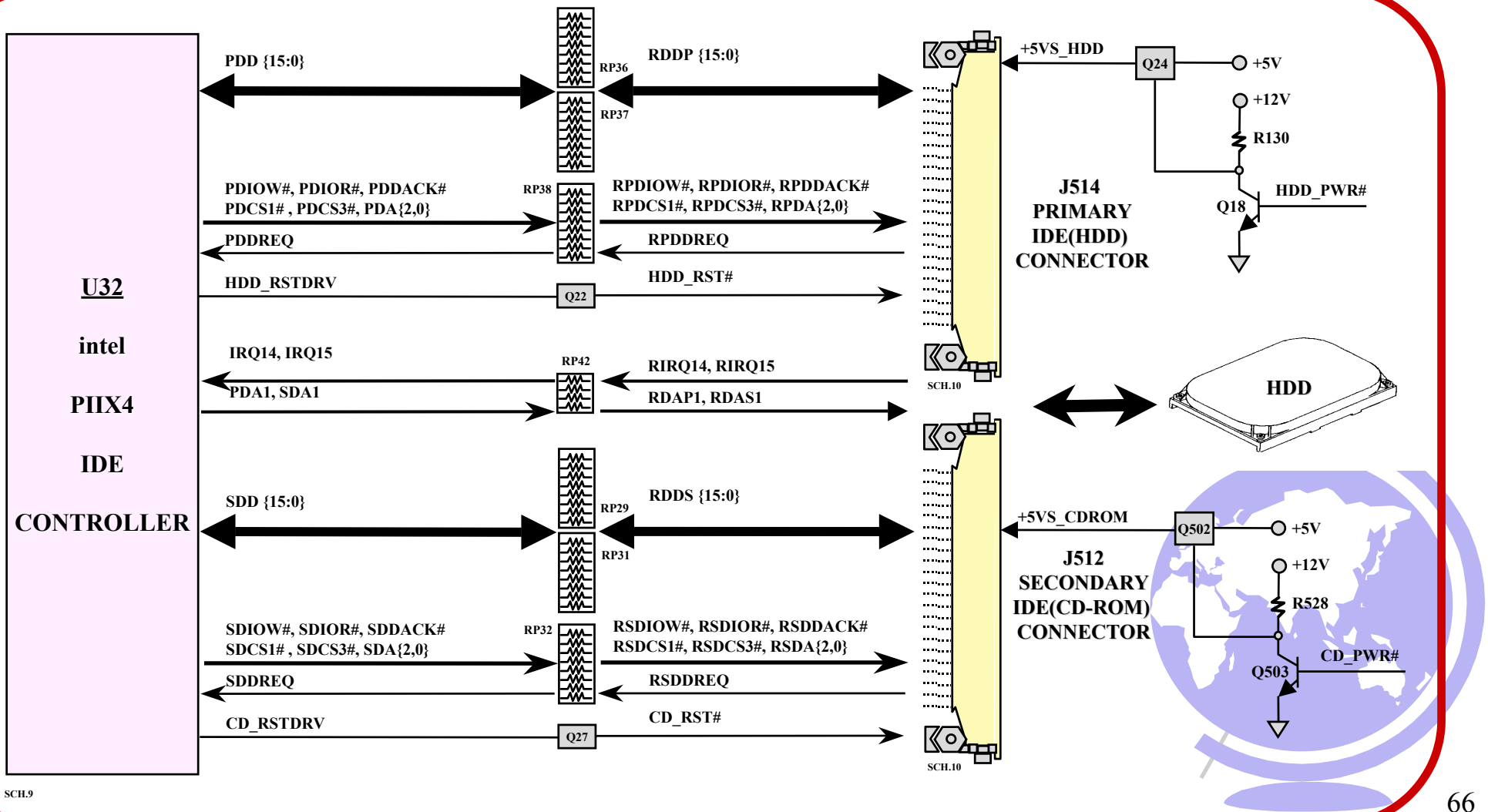
SYMPTOM:
AN ERROR MESSAGE IS SHOWN WHILE LOADING DATA FROM DISK TO SYSTEM.



7.10 HARD DRIVE TEST ERROR

SYMPTOM:

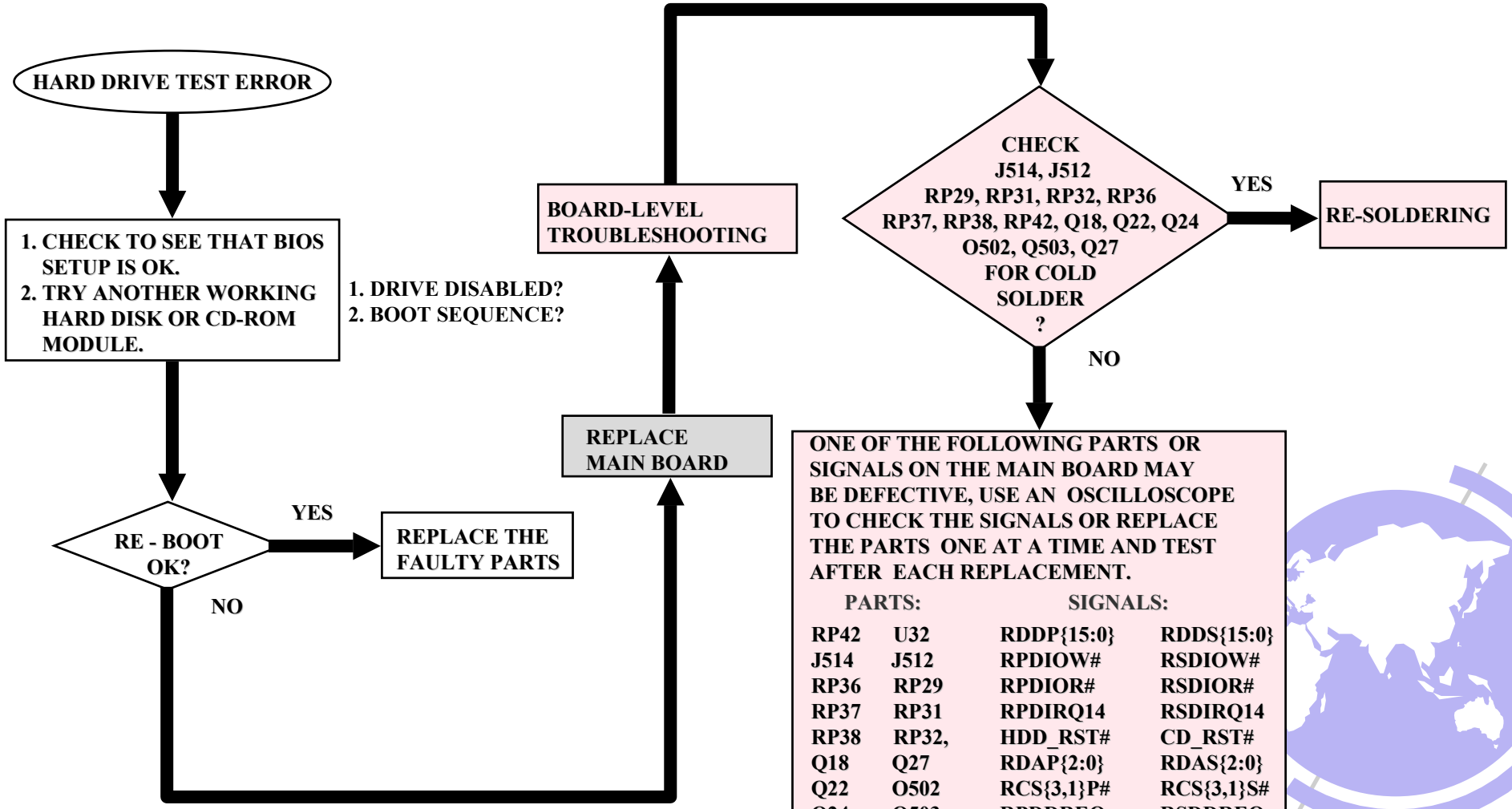
EITHER AN ERROR MESSAGE IS SHOWN, OR THE DRIVE MOTOR SPINS NON-STOP, WHILE READING DATA FROM OR WRITING DATA TO HARD-DISK.



7.10 HARD DRIVE TEST ERROR

SYMPTOM:

EITHER AN ERROR MESSAGE IS SHOWN, OR THE DRIVE MOTOR SPINS NON-STOP, WHILE READING DATA FROM OR WRITING DATA TO HARD-DISK.



6020 N/B MAINTENANCE

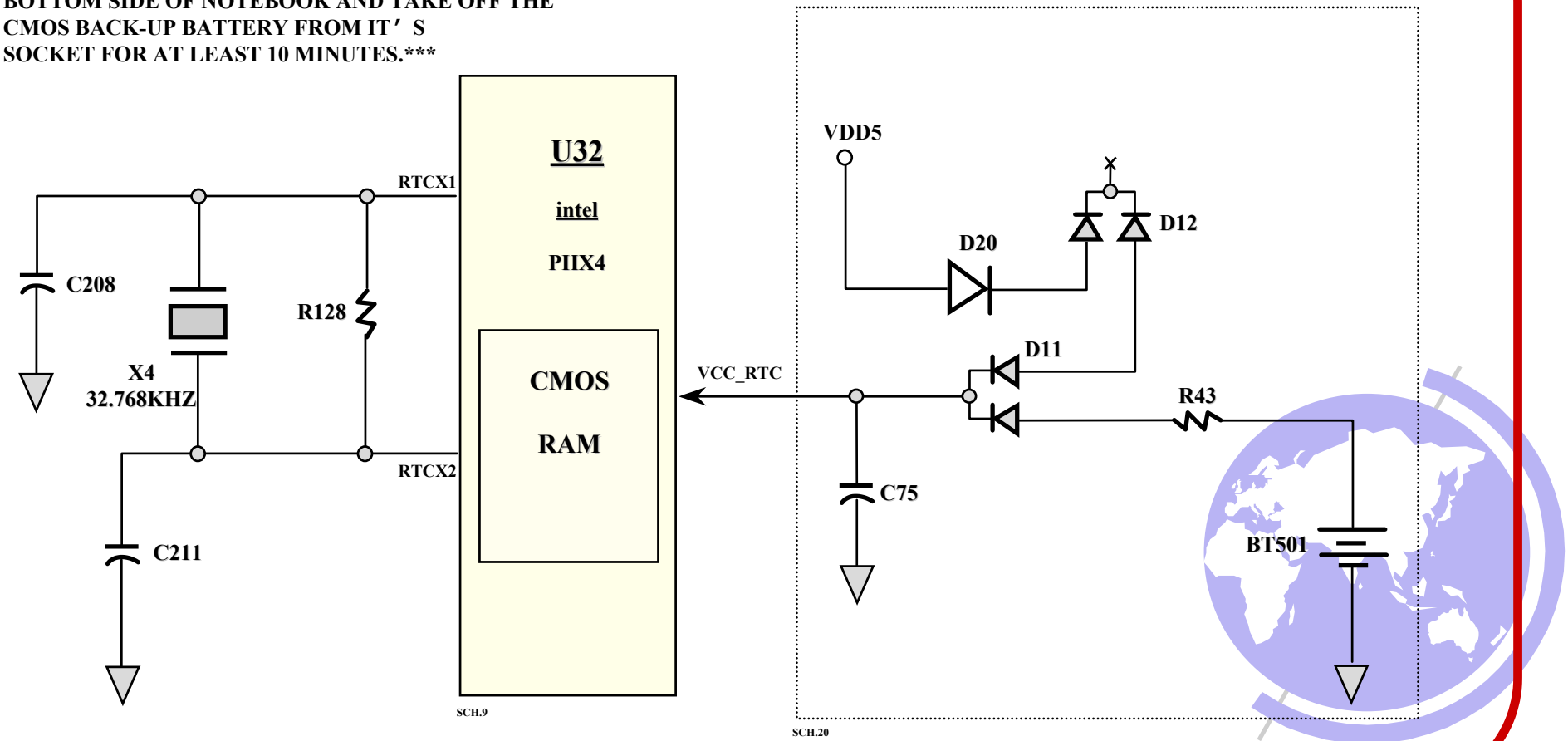
7.11 CMOS TEST ERROR

SYMPTOM:

1. ERROR CODE IS STOPEED AT 22H.

2. CMOS DATA LOST, OR INACCURATE SYSTEM TIME & DATE.

TO CLEAR CMOS DATA, REMOVE BATTERY PACK AND DISCONNECT AC ADAPTER FIRST, THEN REMOVE CMOS BATTERY COMPARTMENT COVER ON THE BOTTOM SIDE OF NOTEBOOK AND TAKE OFF THE CMOS BACK-UP BATTERY FROM IT' S SOCKET FOR AT LEAST 10 MINUTES.



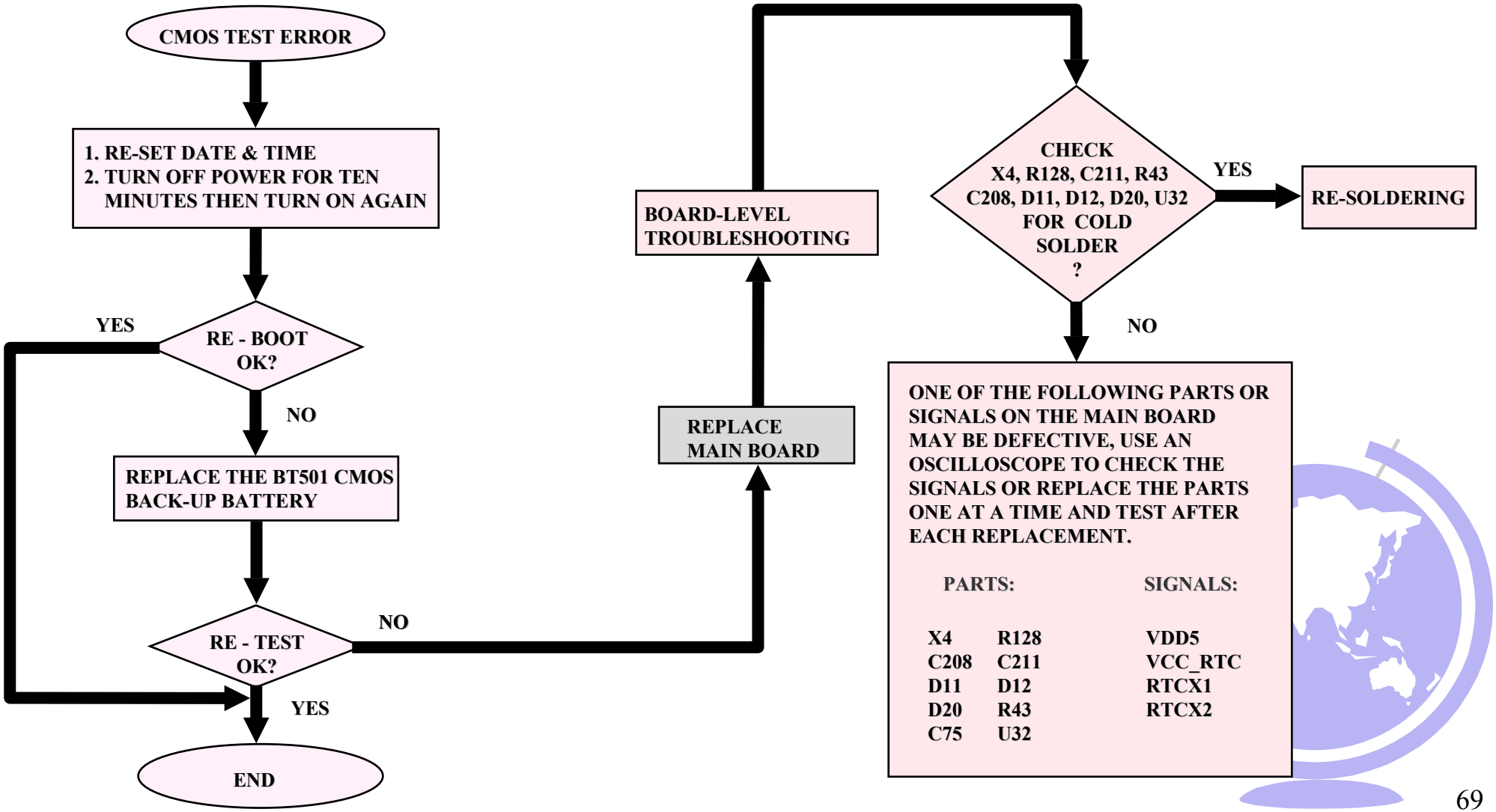
6020 N/B MAINTENANCE

7.11 CMOS TEST ERROR

SYMPTOM:

1. ERROR CODE IS STOPEED AT 22H.

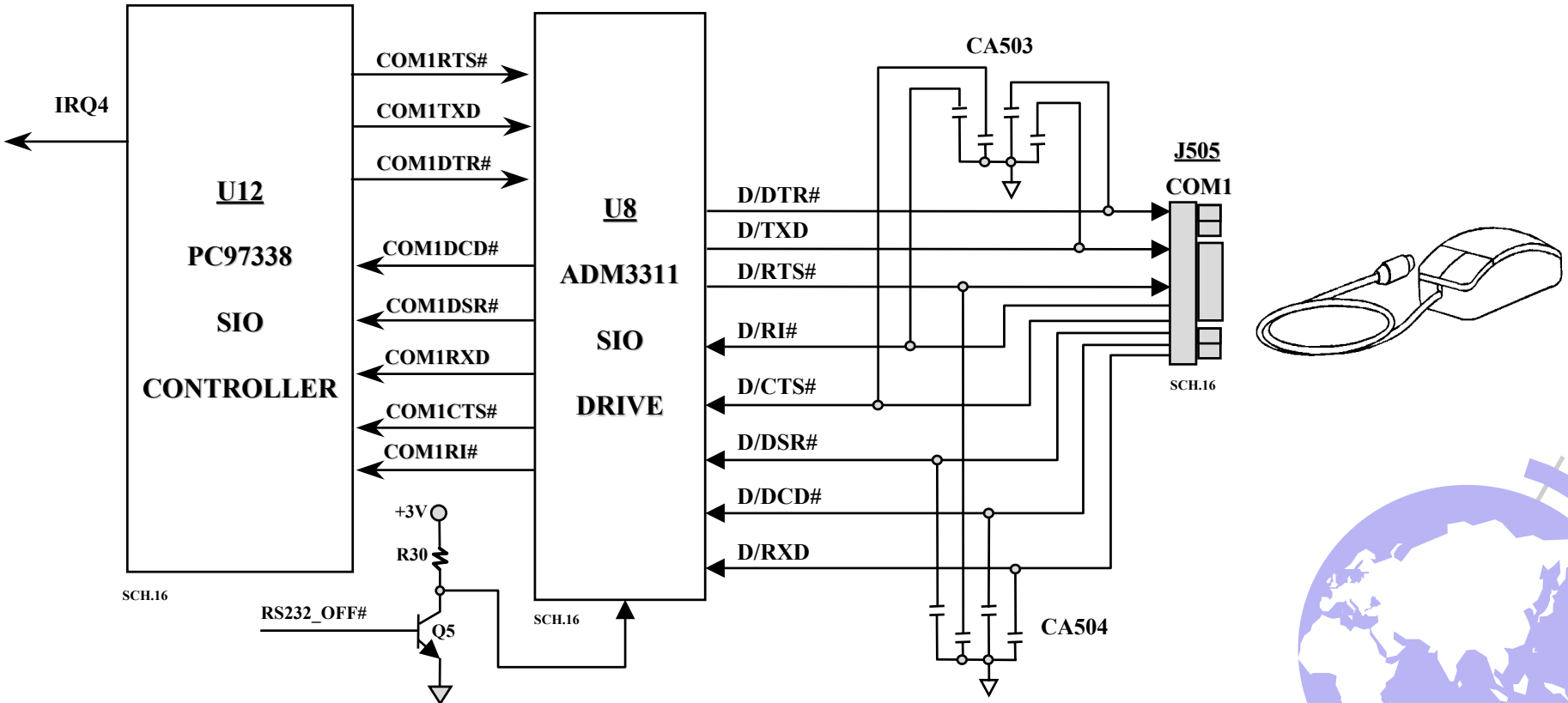
2. CMOS DATA LOST, OR INACCURATE SYSTEM TIME & DATE.



7.12 SIO PORT TEST ERROR

SYMPTON:

ERROR OCCURS WHEN A MOUSE OR OTHER I/O SERIAL DEVICE IS INSTALLED.



PIN DEFINITION OF SIO PORT:

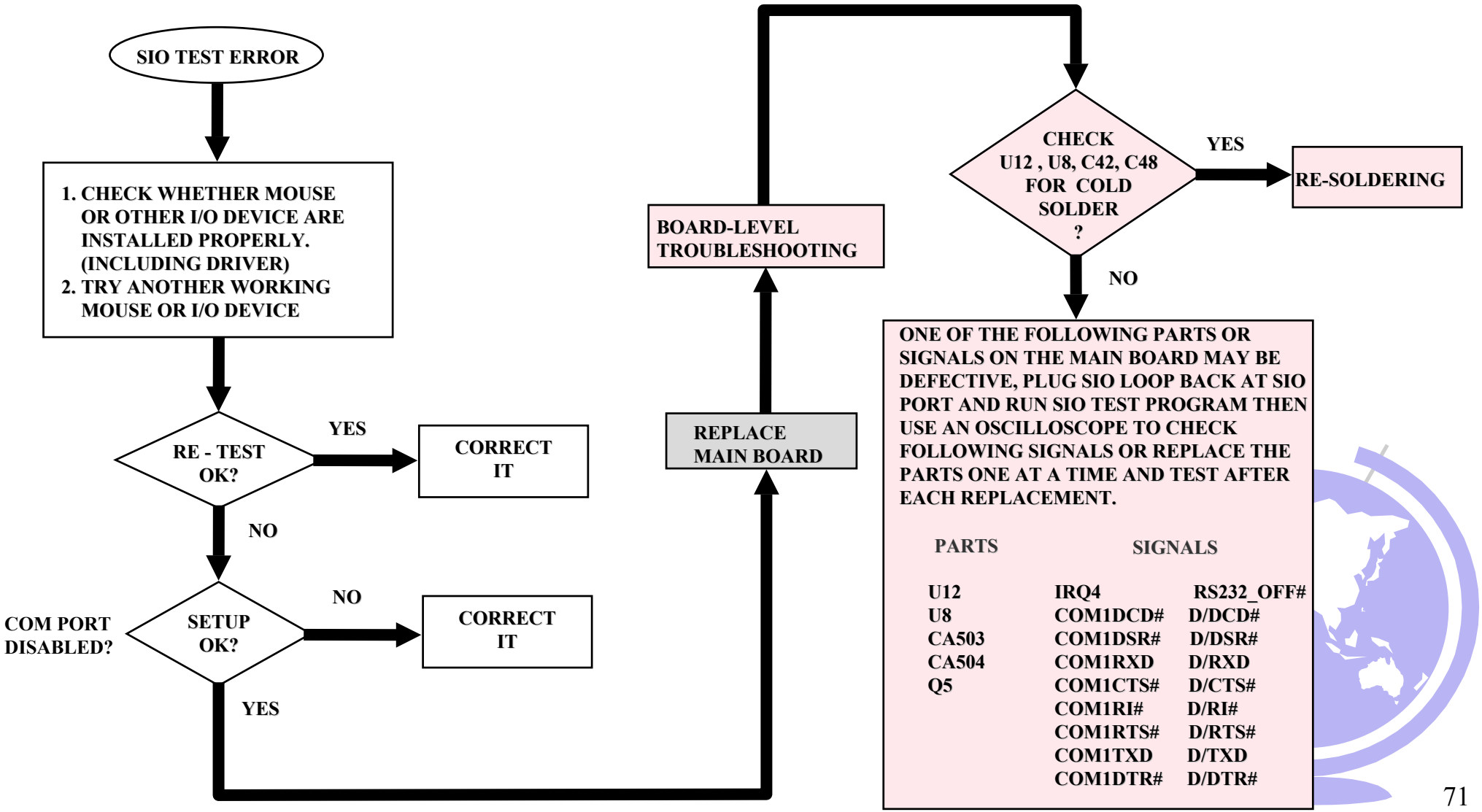
PIN 1	DCD	DATA CARRIER DETECT	PIN 6	DSR	DATA SET READY
PIN 2	RD	RECEIVE DATA	PIN 7	RTS	REQUEST TO SEND
PIN 3	TD	TRANSMIT DATA	PIN 8	CTS	CLEAR TO SEND
PIN 4	DTR	DATA TERMINAL READY	PIN 9	RI	RING INDICATOR
PIN 5	SG	SIGNAL GROUND			

LOOPBACK CONNECTOR FOR SIO TEST:

PIN 1,4,6	SHORT
PIN 2,3	SHORT
PIN 7,8,9	SHORT

7.12 SIO PORT TEST ERROR

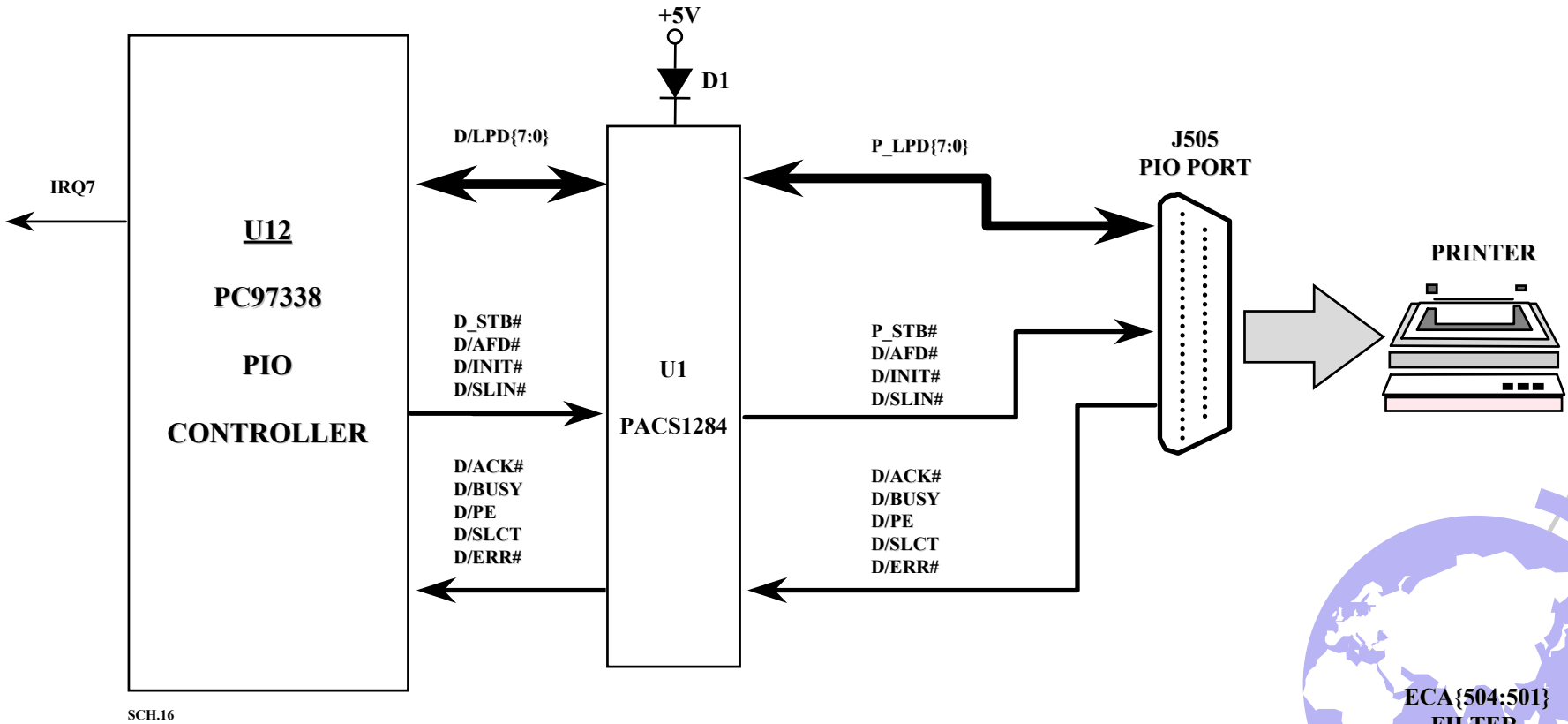
SYMPTON:
ERROR OCCURS WHEN A MOUSE OR OTHER I/O SERIAL DEVICE IS INSTALLED.



7.13 PIO PORT TEST ERROR

SYMPTON:

WHEN A PRINT COMMAND IS ISSUED, PRINTER PRINTS NOTHING OR GARBAGE.



PIN DEFINITION OF PIO PORT

PIN 1	STB	STROBE SIGNAL	PIN 14	AFD	AUTO LINE FEED
PIN 2-9	D0 -D7	PARALLEL PORT DATA BUS D0 TO D7	PIN 15	ERR	ERROR AT PRINTER
PIN 10	ACK	ACKNOW LEDGE HANDSHANK	PIN 16	INIT	INITIATE OUTPUT
PIN 11	BUSY	BUSY SIGNAL	PIN 17	SLIN	PRINTER SELECT
PIN 12	PE	PAPER END	PIN 18-25:		SIGNAL GROUND
PIN 13	SLCT	PRINTER SELECTED			

LOOPBACK CONNECTOR FOR PIO TEST:

PIN 1,13	SHORT	PIN 10,16	SHORT
PIN 2,15	SHORT	PIN 11,17	SHORT
PIN 12,14	SHORT		

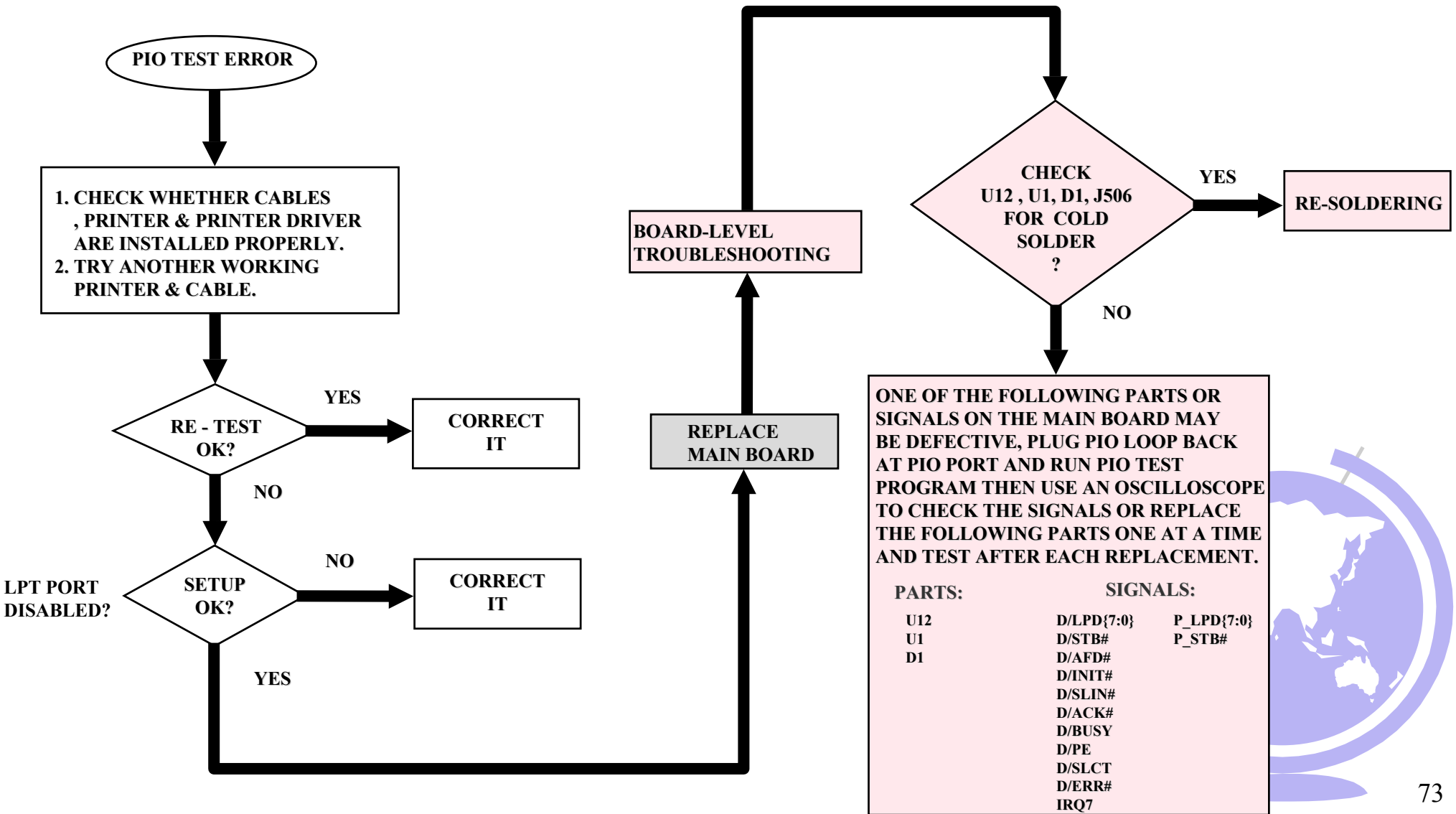
LOOPBACK CONNECTOR FOR EPP TEST:

PIN 1,2,4,6,8	SHORT
PIN 3,5,7,9,16	SHORT
PIN 18,19,20,21,22,23,24,25	SHORT

ECA{504:501}
FILTER
CAPACITOR

7.13 PIO PORT TEST ERROR

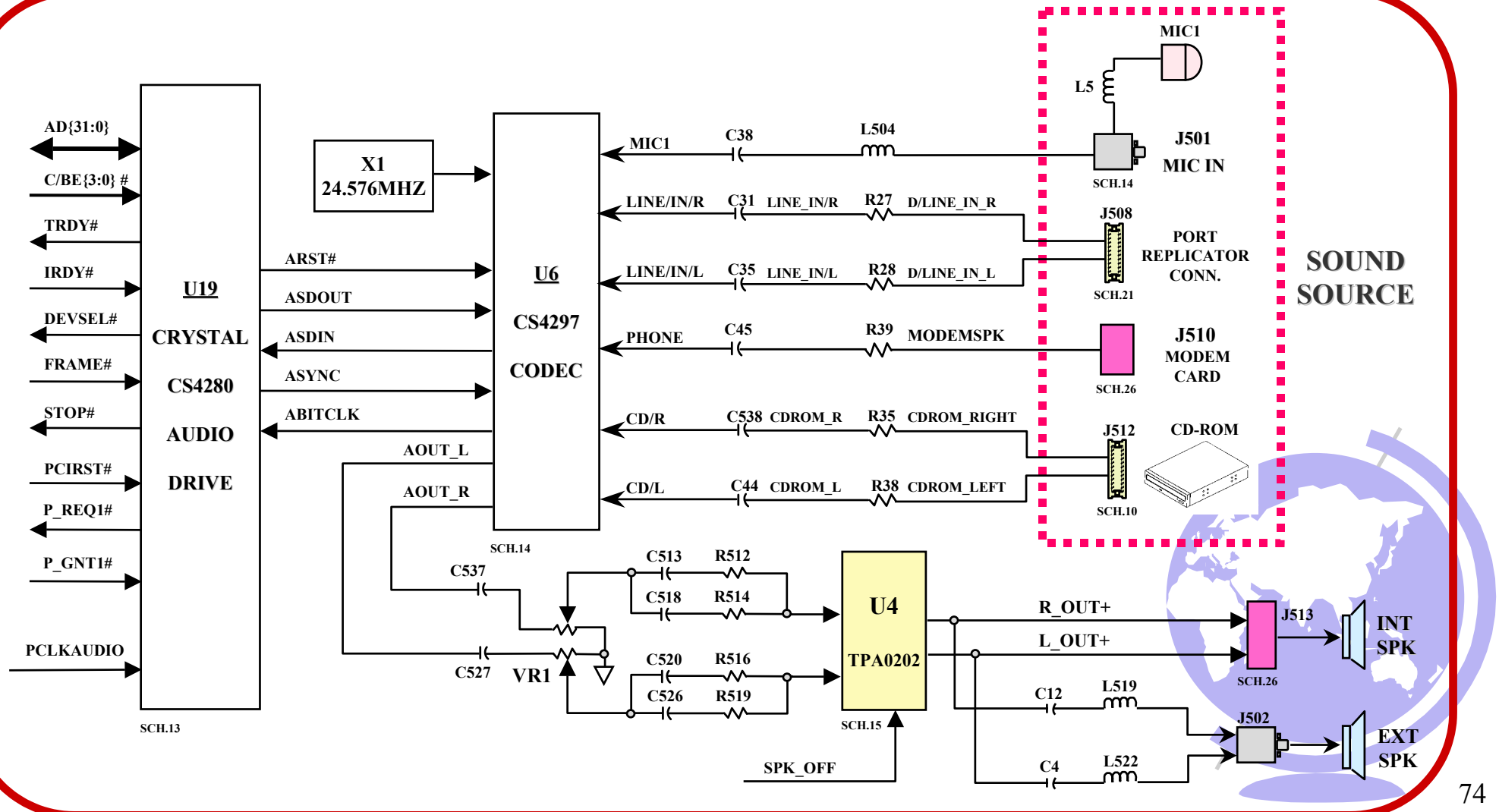
SYMPTON:
WHEN A PRINT COMMAND IS ISSUED, PRINTER PRINTS NOTHING OR GARBAGE.



7.14 AUDIO DRIVE FAILURE

SYMPTON:

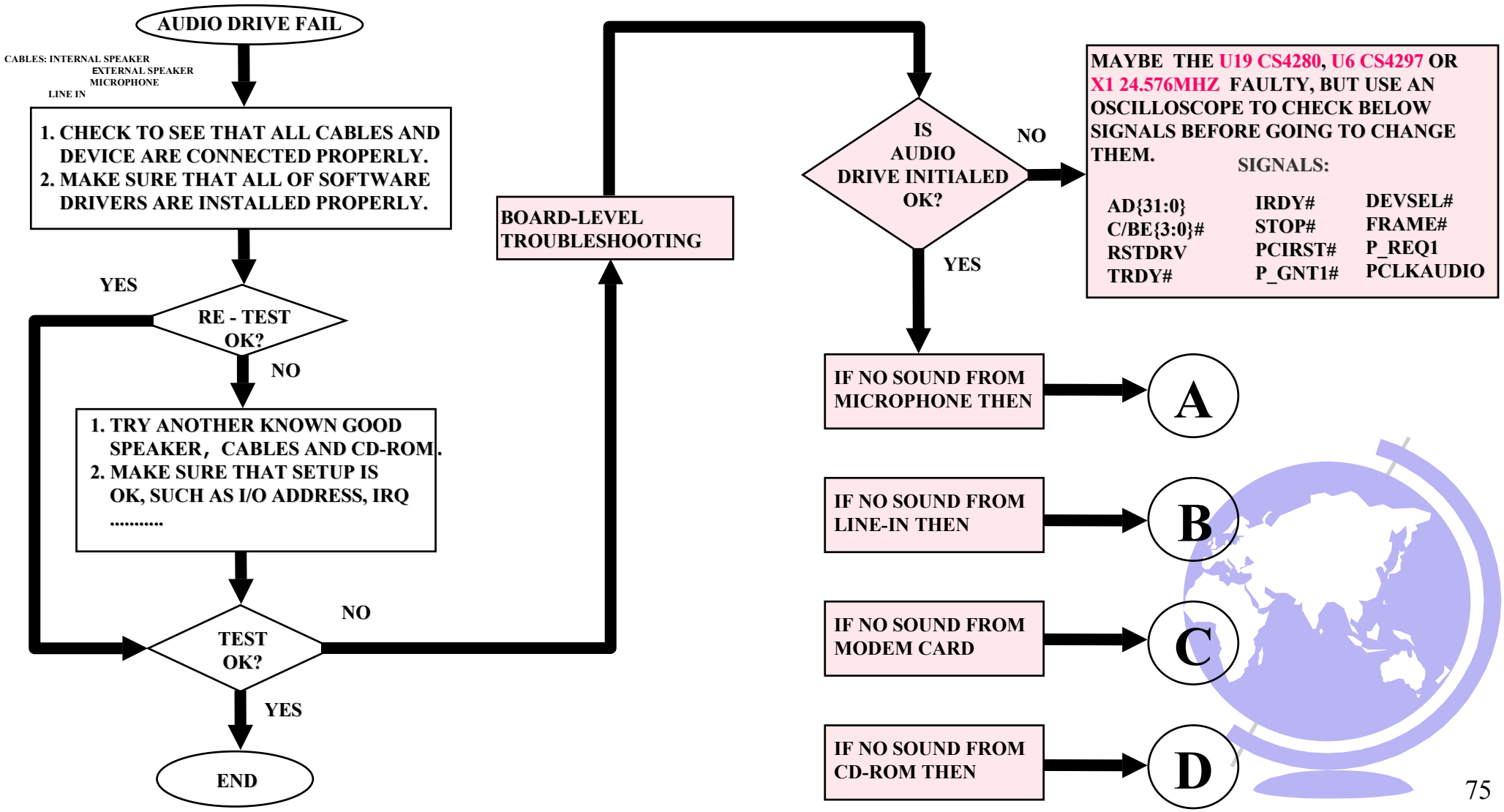
NO SOUND FROM SPEAKER AFTER AUDIO DRIVE IS INSTALLED OR NO SOUND FROM CD-ROM, MICROPHONE AND MODEM VOICE.



7.14 AUDIO DRIVE FAILURE

SYMPTON:

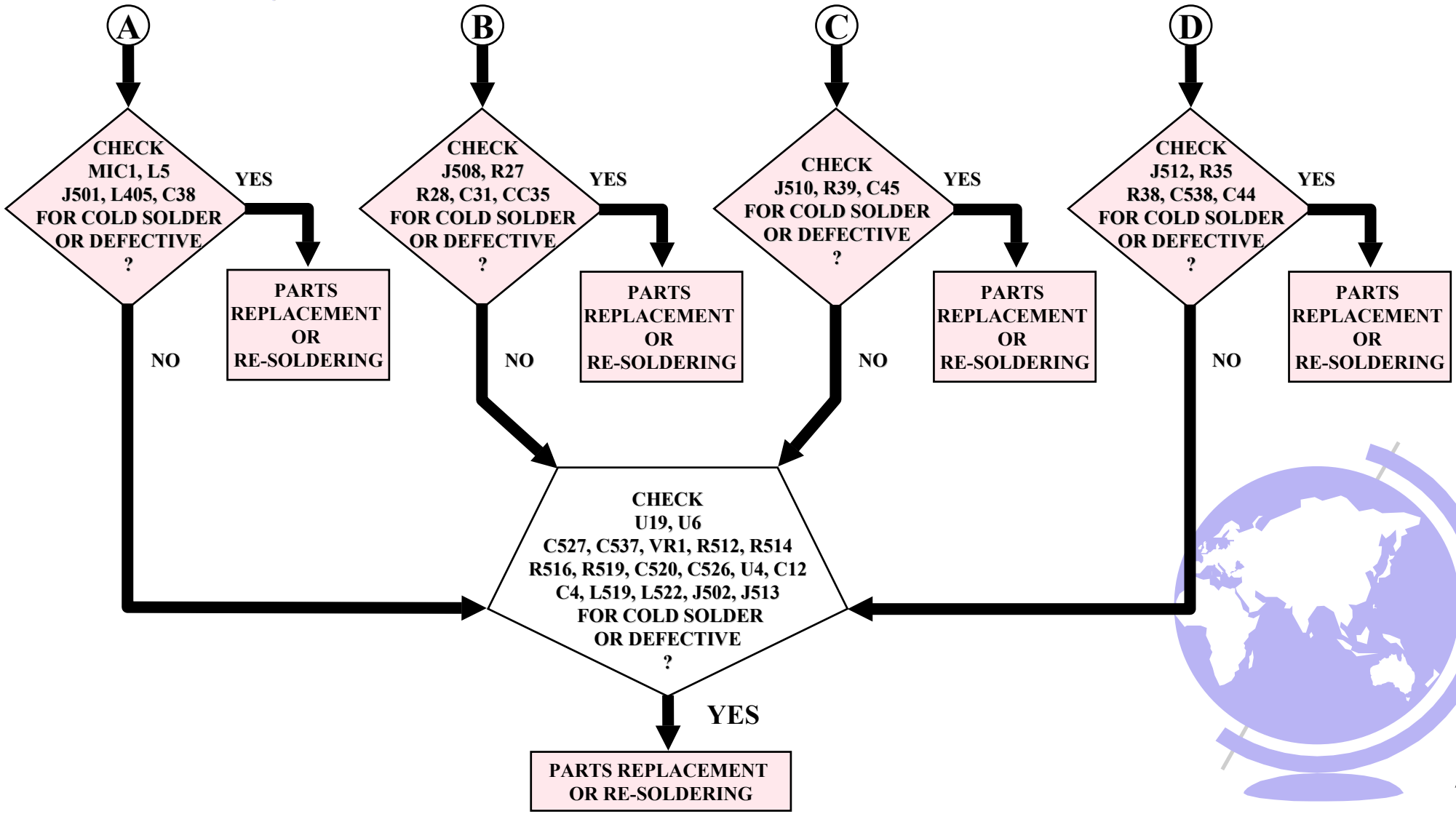
NO SOUND FROM SPEAKER AFTER AUDIO DRIVE IS INSTALLED OR NO SOUND FROM CD-ROM, MICROPHONE AND MODEM VOICE.



7.14 AUDIO DRIVE FAILURE

SYMPTON:

NO SOUND FROM SPEAKER AFTER AUDIO DRIVE IS INSTALLED OR NO SOUND FROM CD-ROM, MICROPHONE AND MODEM VOICE.



8. EXPLOED VIEWS(1)

8. EXPLOED VIEWS(2)

8. EXPLOED VIEWS(3)

8. EXPLOED VIEWS(4)

8. EXPLOED VIEWS(5)

9. SPARE PARTS LIST(1)

PART_NO	DESCRIPTION	LOCATION
526266570001	NB;6020/TMAA/43A/1EN1/A1CB1	
523400390013	HD DRIVE;4.3GB,2.5",MK4309MAT	
324000000011	CPU MODULE;PII/MMC2,233,DESCHUTE	
531013890137	KBD;86,US,K980218E,6020	
416266570001	NB PLATFORM;TFT,MTB,14.1",6020	
340665700002	TILT UNIT;R,6020,PRT	
340665700003	TILT UNIT;L,6020,PRT	
344665700015	HOOK;SLIDE,LATCH,LCD,6020,PRT	
342665700006	BRACKET;LCD,L,6020,PRT	
344665700018	LATCH;LCD,6020,PRT	
421665700032	WIRE ASSY;INVERTER/LCD,6020,PRT	
340665700015	COVER ASSY;LCD,6020	
340665700016	HOUSING ASSY;LCD,6020	
342665700007	BRACKET;LCD,R,6020N,PRT	
421665700031	WIRE ASSY;LCD,6020,ASM	
346665700003	INSULATOR;LCD COVER,6020	
345665700004	SPONGE;LCD,6020	
345665700001	RUBBER;LCD,DOWN,6020,PRT	
341665700004	SPRING;LCD,6020,PRT	
370102010404	SPC-SCREW;M2L4,K-HD,NIB	
371102610405	SCREW;M2.6L4,K-HEAD(+),NIW	
370102610602	SPC-SCREW;M2.6 L6,NIB,K-HD,727	
370102510302	SPC-SCREW;M2.5L3,NIB,K-HD,727	
413000020136	LCD;AA141XB01,TFT14.1,XGA,ADI	
412219300019	PCB ASSY;INVERTER BD,14.1",6020	
523411442008	FD DRIVE;1.44M,3 MODE,D353G	
344665700001	HOUSING;HDD,6020,PRT	
340665700013	SHIELDING ASSY;HDD,6020	
342665700002	BRACKET;HDD,6020,PRT	

PART_NO	DESCRIPTION	LOCATION
332300000115	CABLE;FFC,FDD,6020	
371103010403	SCREW;M3L4,K-HEAD(+),NIW	
371102030303	SCREW;M2L3,K-HEAD(+),NIW/NLK	
411665700006	PWA;PWA-6020 HDD/FDD TRANSLATION	
291000152602	CON;FPC/FFC,26P,1MM,R/A,SMT,ELCO	J2
331030044006	CON;HDR,FM,22P*2,2.0MM,ST,SUYIN,	J3
331030060003	CON;HDR,FM,20P*3,.8MM,ST,DIP	J1
344665700005	COVER;MODEM,6020,PRT	
340665700001	IO DOOR ASSY;6020,ASM	
344665700004	COVER;PCMCIA,6020,PRT	
342665700003	BRACKET;IO,6020,PRT	
344665700006	BUTTON;TOUCHPAD,6020,PRT	
344665700007	COVER;CPU,6020,PRT	
344665700008	COVER;HINGE,6020,PRT	
421665700001	CABLE ASSY;CD ROM,6020,ASM	
370102020301	SPC-SCREW;M2L3,NIW,K-HEAD	
340665700005	COVER ASSY;6020,ASM	
340665700006	HOUSING ASSY;6020,ASM	
340665700012	SHIELDING ASSY;BOTTOM,6020	
332300000116	CABLE;FFC,TOUCHPAD,6020	
340665700007	SPEAKER BOX ASSY;R,6020,ASM	
340665700008	SPEAKER BOX ASSY;L,6020,ASM	
342665700010	SHIELDING;CPU,COVER,6020,PRT	
342665700011	SHIELDING;MODEM,6020,PRT	
340665700009	CPU HEATSINK ASSY;6020,ASM	
370102630502	SPC-SCREW;M2.6L5,K-HEAD(+),NIB	
370102610602	SPC-SCREW;M2.6 L6,NIB,K-HD,727	
371103030602	SCREW;M3L6,K-HEAD(+),NIB/NLK	
371102610405	SCREW;M2.6L4,K-HEAD(+),NIW	

9. SPARE PARTS LIST(2)

PART_NO	DESCRIPTION	LOCATION
340665700014	PLATE ASSY;TOUCHPAD,6020	
411665700001	PWA;PWA-6020 MOTHER BD	
242600000195	LABEL;PENTIUM-BP,SYSTEMSOFT BIOS	
312271006350	EC;100U ,25V,20%,RA,6.3*7,-40~10	PC3,504,507,508
312272206154	EC;220U ,6.3V,20%,RA,D10*5,OS-CO	PC4,5
331040060003	CON;HDR,MA,20P*3,.8MM,R/A,AMP	J514
331510080001	CON;RBN,MA,80P,.63MM,R/A	J508
331720009004	CON;D,MA,9P,2.775,R/A	J505
331720015006	CON;D,FM,15P,2.29,R/A,3ROW	J507
331720025005	CON;D,FM,25P,2.775,R/A	J506
331840005007	CON;STEREO JACK,5P,R/A,W9.1,LGY2	J501,502
331870004002	CON;MINI DIN,4P,R/A,W/GROUNDING	J509
331870006011	CON;MINI DIN,6P,R/A,W/GROUNDING	J503
331910005001	CON;POWER JACK,5P,42VDC/5A	PJ501
339115000008	MICROPHONE;D9.7*H6.7,WM-034BY	MIC1
411665700005	PWA;PWA-6020 SMT V0 MOTHER BD	
271002000301	RES;0 ,1/10W,5% ,0805,SMT	L3,4,17,19,20
271002103301	RES;10K ,1/10W,5% ,0805,SMT	PR8
271002472301	RES;4.7K ,1/10W,5% ,0805,SMT	PR4
271003228101	RES;2.2 ,1/4W,1% ,0805,SMT	R2
271071202102	RES;2K ,1/16W,1% ,0603,SMT	R7
271013150301	RES;15 ,1/4W,5% ,1206,SMT	R17
271045107101	RES;.01 ,1W ,1% ,2512,SMT	PR6
271045207101	RES;.02 ,1W ,1% ,2512,SMT	PR47
271045257101	RES;.025 ,1W ,1% ,2512,SMT	PR3
271071000002	RES;0 ,1/16W,0603,SMT	PR25,31,35
271071101301	RES;100 ,1/16W,5% ,0603,SMT	R75,86,90
271071102102	RES;1K ,1/16W,1% ,0603,SMT	PR43,45
271071102302	RES;1K ,1/16W,5% ,0603,SMT	R1,5,11,20,43

PART_NO	DESCRIPTION	LOCATION
271071103101	RES;10K ,1/16W,1% ,0603,SMT	PR59,61
271071103302	RES;10K ,1/16W,5% ,0603,SMT	PR18,24,40,49,52
271071104101	RES;100K ,1/16W,1% ,0603,SMT	PR7,10,504
271071104302	RES;100K ,1/16W,5% ,0603,SMT	PR1,14,16,17,21
271071184301	RES;180K ,1/16W,5% ,0603,SMT	R50
271071105101	RES;1M ,1/16W,1% ,0603,SMT	PR11,15,22,27,30
271071105301	RES;1M ,1/16W,5% ,0603,SMT	R29,45,49,74,91
271071124311	RES;124K ,1/16W,1% ,0603,SMT	PR9
271071137211	RES;13.7K,1/16W,1% ,0603,SMT	PR56
271071153301	RES;15K ,1/16W,5% ,0603,SMT	R108,111,122,125
271071180301	RES;18 ,1/16W,5% ,0603,SMT	R77,82,87,92
271071203101	RES;20K ,1/16W,1% ,0603,SMT	PR36,54,506
271071203302	RES;20K ,1/16W,5% ,0603,SMT	PR2,R513,515
271071204101	RES;200K ,1/16W,1% ,0603,SMT	PR20
271071205101	RES;2M ,1/16W,1% ,0603,SMT	R124
271071221211	RES;22.1K,1/16W,1% ,0603,SMT	PR503,34
271071221301	RES;220 ,1/16W,5% ,0603,SMT	R71
271071222302	RES;2.2K ,1/16W,5% ,0603,SMT	PR60
271071224301	RES;220K ,1/16W,5% ,0603,SMT	R104
271071225301	RES;2.2M,1/16W,5% ,0603,SMT	PR12,19,63
271071243311	RES;243K ,1/16W,1% ,0603,SMT	PR5
271071249211	RES;24.9K,1/16W,1% ,0603,MST	PR42,48
271071270301	RES;27 ,1/16W,5% ,0603,SMT	R112,118,120,126
271071287311	RES;287K ,1/16W,1% ,0603,SMT	PR29
271071301311	RES;301K ,1/16W,1% ,0603,SMT	PR505
271071330302	RES;33 ,1/16W,5% ,0603,SMT	R24,36,46,47,59
271071331301	RES;330 ,1/16W,5% ,0603,SMT	R504,110
271071334301	RES;330K ,1/16W,5% ,0603,SMT	R54
271071357111	RES;3.57K,1/16W,1% ,0603,SMT	PR50

9. SPARE PARTS LIST(3)

PART_NO	DESCRIPTION	LOCATION
271071365311	RES;365K ,1/16W,1% ,0603,SMT	PR32
271071442011	RES;442 ,1/16W,1% ,0603,SMT	R25,26
271071470301	RES;47 ,1/16W,5% ,0603,SMT	R70,72
271071471302	RES;470 ,1/16W,5% ,0603,SMT	R16,22,23,139,529
271071472302	RES;4.7K ,1/16W,5% ,0603,SMT	R4,31,55,64-66
271071473301	RES;47K ,1/16W,5% ,0603,SMT	PR13,33,R96
271071474301	RES;470K ,1/16W,5% ,0603,SMT	R67,130,137,525,528
271071487311	RES;487K ,1/16W,1% ,0603,SMT	PR57
271071499111	RES;4.99K,1/16W,1% ,0603,SMT	PR41,507
271071562301	RES;5.6K ,1/16W,5% ,0603,SMT	R102,117
271071564301	RES;560K ,1/16W,5% ,0603,SMT	R9
271071622301	RES;6.2K ,1/16W,5% ,0603,SMT	PR62
271071681101	RES;680 ,1/16W,1% ,0603,SMT	R8
271071681301	RES;680 ,1/16W,5% ,0603,SMT	R10,12,13
271071682101	RES;6.8K ,1/16W,1% ,0603,SMT	R27,28,35,38,39
271071684301	RES;680K ,1/16W,5% ,0603,SMT	R106,115
271071750302	RES;75 ,1/16W,5% ,0603,SMT	R505,507,509
271071806211	RES;80.6K,1/16W,1% ,0603,SMT	PR37
271071909211	RES;90.9K,1/16W,1% ,0603,SMT	PR38
271071976311	RES;976K ,1/16W,1% ,0603,SMT	PR55
271571000301	RP;0*8 ,16P ,1/16W,5% ,1606,SM	RP1,9,12,
271571100301	RP;10*8 ,16P ,1/16W,5% ,1606,SM	RP501-509
271571330301	RP;33*8 ,16P ,1/16W,5% ,1606,SM	RP29,31,32,36-38
271611102301	RP;1K*4 ,8P ,1/16W,5% ,0612,SMT	RP45,30
271611103301	RP;10K*4 ,8P ,1/16W,5% ,0612,SMT	RP17,49,50,510
271611104301	RP;100K*4,8P ,1/16W,5% ,0612,SMT	RP35
271611220301	RP;22*4 ,8P ,1/16W,5% ,0612,SMT	RP39
271611222301	RP;2.2K*4,8P ,1/16W,5% ,0612,SMT	RP8
271611330301	RP;33*4 ,8P ,1/16W,5% ,0612,SMT	RP42

PART_NO	DESCRIPTION	LOCATION
271611472301	RP;4.7K*4,8P ,1/16W,5% ,0612,SMT	RP7,40
271621103303	RP;10K*8 ,10P,1/16W,5% ,1206,SMT	RP13,26-28,33,41
271621433301	RP;43K*8 ,10P,1/16W,5% ,1206,SMT	RP4,6,11,15,25
271621472303	RP;4.7K*8,10P,1/16W,5% ,1206,SMT	RP34,44,48,51,52
271621822301	RP;8.2K*8,10P,1/16W,5% ,1206,SMT	RP10,23,24
271911103901	VR;10K ,.05W,20%,XV0102GPH1N-93	VR1
272002105701	CAP;1U ,CR,16V ,-20+80%,0805,SM	C43,54,PC8,26,506
272002334401	CAP;.33U ,CR,16V ,10%,0805,SMT	PC32,35
272002474401	CAP;.47U ,CR,16V ,10%,0805,X7R,S	C5
272011106701	CAP;10U ,10V,+80-20%,1206,Y5V,S	C8,11,16,17,129
272012105702	CAP;1U ,CR,16V ,+80-20%,1206,Y	PC18
272012225702	CAP;2.2U ,CR,16V ,+80-20%,1206,Y	C46,55,121,237
272012475701	CAP;4.7U ,CR,16V ,+80-20%,1206,Y	C22,63,70,119
272021106501	CAP;10U ,10V ,20%,1210,X7R,SMT	C13,PC17
272022106701	CAP;10U ,16V,+80-20%,1210,Y5V,S	C57,PC13
272041226501	CAP;22U ,CR,10V ,20%,1812,X7R,S	PC19
272043106501	CAP;10U ,CR,25V ,20%,1812,Y5U,S	C125,PC14
272071105701	CAP;1U ,CR,10V ,80-20%,0603,Y5	C75,77,104,111
272072104702	CAP;.1U ,16V,+80-20%,0603,SMT	C10,14,21,29,508
272072224701	CAP;.22U ,16V ,+80-20%,0603,Y5V,	C38,40,44,538
272073180401	CAP;18P ,CR,25V ,10%,0603,NPO,S	C25,208,211
272073330701	CAP;33P ,25V ,+80-20%,0603,SMT	C169,170,181,192
272075100701	CAP;10P ,50V ,+80-20%,0603,SMT	C72,84,108,116
272075101701	CAP;100P ,50V ,+80-20%,0603,SMT	C1,6,24,501,502
272075102403	CAP;1000P,CR,50V,10%,0603,X7R,SM	PC39
272075102701	CAP;1000P,50V ,+80-20%,0603,SMT	C2,3,15,23,88
272075103702	CAP;.01U ,50V,+80-20%,0603,SMT	C19,27,28,30,49
272075104701	CAP;.1U ,50V,+80-20%,0603,SMT	PC1,11,15,23,33
272075220701	CAP;22P ,50V ,+80-20%,0603,SMT	C52,53,230,233

9. SPARE PARTS LIST(4)

PART_NO	DESCRIPTION	LOCATION
272075221302	CAP;220P ,50V ,5% ,0603,SMT	C18,20,80,81
272075391301	CAP;390P ,CR,50V,5%,0603,NPO,SMT	C51
272075470701	CAP;47P ,50V ,+80-20%,0603,SMT	C190,194,195,199
272431225501	CAP;220U ,TT,4V,20%,7243,OS-CON,	PC6,7,9,C122
272601566501	EC;56U ,6.3V,20%,OS-CON,SMT	PC501,503
272602107501	EC;100U,16V,M,6.3*5.5,-55+85'C,S	C4,9,12
272615562501	CP;5600P*4,8P,50V ,20%,0612,X7R,	CA6,7
272625101401	CP;100P*4,8P,50V ,10%,1206,NPO,S	CA1,3,5,505
272625470401	CP;47P*4 ,8P,50V ,10%,1206,NPO,S	CA2,4,8,9,501,502
273000130006	FERRITE CHIP;600OHM/100MHZ,.2A,1	L1,2,5,7,515
273000130010	FERRITE CHIP;130OHM/100MHZ,1608,	L501,502,505-512
273000150013	FERRITE CHIP;120OHM/100MHZ,2012,	L8,10,14-16
273000500006	CHOKE COIL;7UH,7TS,T6*4*2,VENUS,	PT1
273000500011	CHOKE COIL;80UH/33T,D.30,55040,L	PL501
273000500012	CHOKE COIL;10UH,4.7A,5.7MM,SMT	PT3
273000610004	FERRITE ARRAY;120OHM/100MHZ,M TY	FA1-5
273001050016	XFMR;25UH,.3*2*12T/.25*24T,ER14.	PT2
274011431408	XTAL;14.318M,50PPM,32PF,7*5,4P,S	X2
274011600407	XTAL;16MHZ,30PPM,16PF,7*5,4P,SMT	X5
274012457405	XTAL;24.576M,50PPM,16PF,7*5,4P,S	X1
274013276103	XTAL;32.768KHZ,30PPM,12.5PF,CM20	X4
274042949401	OSC;29.498928M,50PPM,15PF,SMALL,	X8
282074338402	IC;74CBTD3384,10 BIT BUS SW,TSOP	U38
282574014004	IC;74AHC14,HEX INVERTER,TSSOP,14	U15
282574164002	IC;74VHC164,SIPO REGISTER,TSSOP,	U2
282674008001	IC;74AHCT08,2I/P AND GATE,TSSOP,	U22
283766570001	IC;SDRAM,1M*16*4-100,TSOP,54P,60	U20,25,28,35
283866570001	IC;SGRAM,512K*32-100,PQFP,100P,6	U5,16
284104011001	IC;W40S11-02,SDRAM BUFFER,SSOP,2	U14

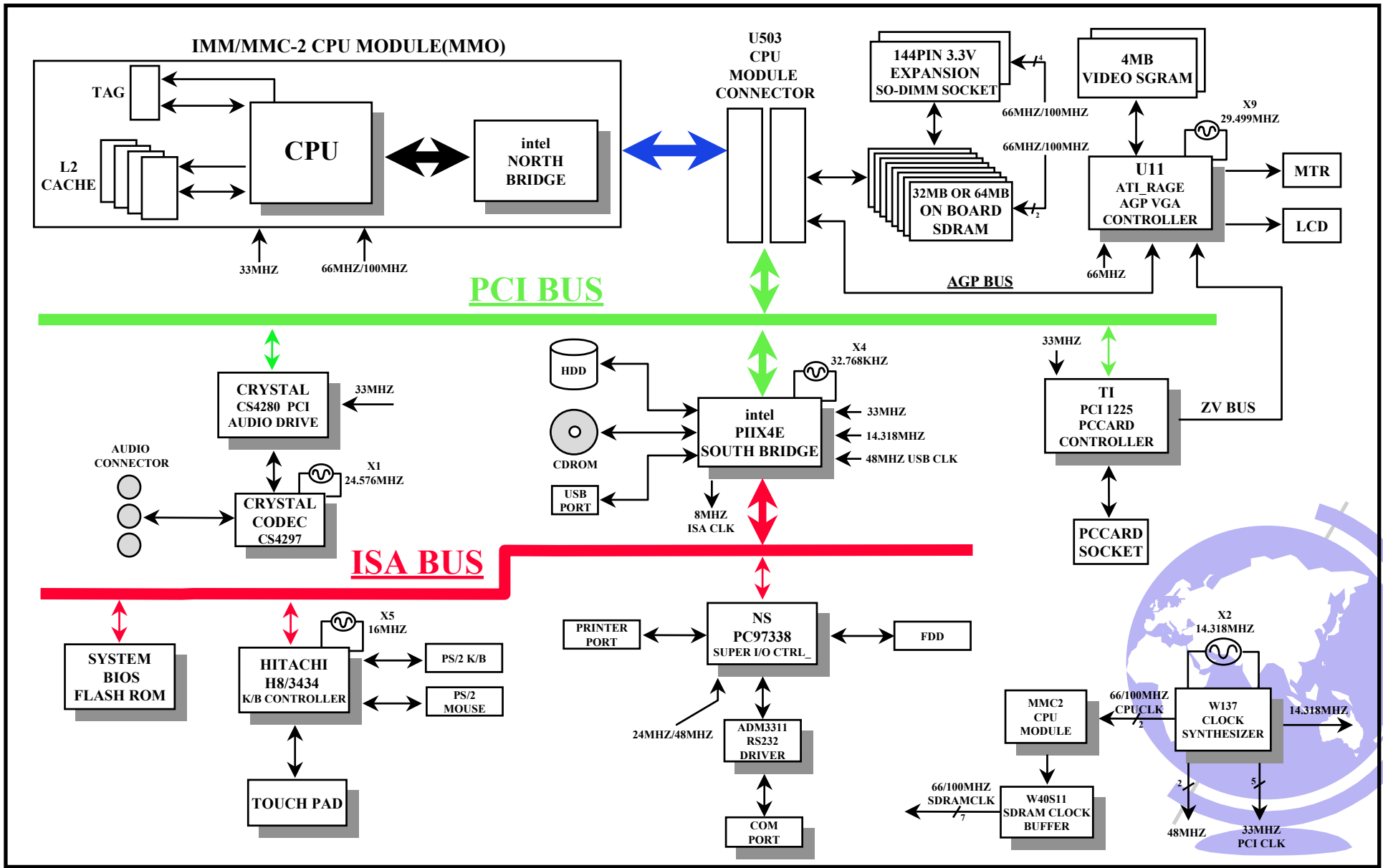
PART_NO	DESCRIPTION	LOCATION
284182371005	IC;FW82371EB,PIIX4E,PCI/ISA,BGA3	U32
284500003002	IC;3D,RAGE LT PRO,AGP,BGA,328P	U11
284501225001	IC;PCI1225PDV,PCI/CARDBUS,LQFP,2	U17
284501284002	IC;PACS1284-02Q/T,TERMIN NET,QSO	U1
284504280001	IC;CS4280-CQ,PCI AUDIO,TQFP,128P	U19
284504297001	IC;CS4297,AUDIO CODEC,TQFP,48P	U6
282153257001	IC;PI5C3257,BUS SWITCH QUAD,QSOP	U18
286500137001	IC;W137,CLOCK GENERATOR,SSOP,28P	U23
284597338001	IC;PC97338VJG,SUPER I/O,TQFP,100	U12
286100202001	IC;TPA0202,AUDIO AMP,2W,TSSOP,24	U4
286100358001	IC;LMV358M,DUAL AMP.,LOW VOLT.,S	PU6
286100393004	IC;LMV393,DUAL COMPARTOR,SSOP,8P	PU3,4
286203311002	IC;ADM3311ARU,RS-232,+-3KV,TSSOP	U8
286300431010	IC;SC431CSK-1,1%,ADJ REG,SOT23	Q1,PQ9,501
286300594001	IC;TL594C,PWM CONTROL,SO,16P	PU5
286302206001	IC;TPS2206,CARDBUS PWR CTLR,SSOP	U7
286302951015	IC;LP2951ACM,VOLTAGE REGULATOR,S	U37
286303052001	IC;SB3052P,PWM CTRL,SSOP,28P	PU2
286303301001	IC;ADP3301AR-5,.8%,REG.,SO,8P	U9
286303823001	IC;TPS3823-33,MICROPWR VOL,SOT23	U33
286317812001	IC;HA178L12UA,VOLT REGULATOR,SC-	PU1
288003600001	FIR;HSDL3600#007,FRONT VIEW,10P,	U501
288100020001	DIODE;RLZ20C,ZENER,19.23V,5%,SMT	PD502
288100024002	DIODE;RLZ24D,ZENER,23.63V,5%,SMT	PD1
288100032013	DIODE;BAS32L,VRRM75V,MELF,SOD-80	PD5,6,8-10,501
288100056003	DIODE;BAW56,70V,215MA,SOT-23	D9,14
288100073002	DIODE;SFPJ-73,DC2010,30V,3A,SMT	PD2,11
288100099001	DIODE;BAV99,70V,450MA,SOT-23	D12
288100202001	DIODE;DAN202K,80V,SWITCH,SMT	PD7

9. SPARE PARTS LIST(5)

PART_NO	DESCRIPTION	LOCATION
288100701002	DIODE;BAV70LT1,70V,225MW,SOT-23	D11,19
288101004024	DIODE;EC10QS04,RECT,40V,1A,CHIP,	PD3,4
288104148001	DIODE;RLS4148,200MA,500MW,MELF,S	D1,8,10,13,15
288200144001	TRANS;DTC144WK,NPN,SOT-23,SMT	PQ10,Q4-6,10
288200144002	TRANS;DTA144WK,PNP,SMT	Q15
288200144003	TRANS;DTC144TKA,N-MOSFET,SOT-23	Q8,9
288200352001	TRANS;NDS352P,DMOS,TO-236AB	Q11,501
288202222001	TRANS;MMBT2222AL,NPN,TO236AB	PQ16
288202301001	TRANS;SI2301DS,P-MOSFET,SOT-23	Q19
288202302001	TRANS;SI2302DS,N-MOSFET,SOT-23	Q3,24,26,502
288203904010	TRANS;MMBT3904L,NPN,Tr35NS,TO236	Q7,23
288203906018	TRANS;MMBT3906L,PNP,Tr35NS,TO236	PQ12
288204435001	TRANS;SI4435DY,P-MOSFET,.035OHM,	PQ1,8,15
288206612001	TRANS;FDS6612A,N-MOSFET,.03OHM,S	PQ2
288206690001	TRANS;FDS6690A,N-MOSFET,.017OHM,	PQ4
288209410001	TRANS;SI9410DY,N-MOSFET,.04OHM,S	PQ5,6
288209430001	TR;NDS9430,P-FET,.06OHM,SO,8P	PQ13
288227002001	TRANS;2N7002LT1,N-CHANNEL FET	PQ3,7,11,14,17
291000011001	CON;HDR,MA,10P*1,1.25,ST,SMT	J1
291000012001	CON;HDR,MA,10P*2,1.25MM,ST,SMT	J2
291000022401	CON;HDR,FM,12P*2,1.27MM,R/A,SMT	J513
291000014803	CON;HDR,MA,24P*2,1.27,ST,H1.5,SM	J512
291000020402	CON;HDR,SHROUD,MA,4P*1,2.0,R/A,U	J504
291000026001	CON;HDR,MA,30P*2,.6MM,R/A,SMT	J510
291000140503	CON;FPC/FFC,5P,1MM,ST,SMT,6020	J3
291000152603	CON;FPC/FFC,26P,1MM,R/A,KBD,SMT	J4
291000251441	CON;IC CARD,FM,72P*2,.6MM,H3MM,S	U502
291000410301	CON;WFR,MA,3P,1.25,ST,SMT/MB	J511
291000610032	IC SOCKET;32P,PLCC,TIN,W/O PEGS,	U13

PART_NO	DESCRIPTION	LOCATION
291000614003	IC SOCKET;400P,1.27,MMC2,MEG-ARR	U503
291006214410	DIMM SOCKET;144P,REVERSE,AMP,SMT	J5
291006214411	DIMM SOCKET;144P,.8MM,AMP353870,	J7
294011200017	LED;GREEN,H0.8,0603,CL-190,SMT	D2-7
295000010008	FUSE;1.1A,POLY SWITCH,SMT	F1,2,501
295000010016	FUSE;NORMAL,6.5A/32VDC,3216,SMT	PF1,2
297030105001	SW;PUSH BUTTON,SPSD,48V/.05A,SMT	SW1
298000000002	BATTERY HOLDER;FOR CR2032,BH-800	BT501
284583434001	IC;H8/F3434,KBD CTLR,TQFP,100P	
242600000145	LABEL;10*10,BLANK,COMMON	
242600000158	LABEL;10*10,BLANK,COMMON,HI-TEMP	
283420402003	IC;FLASH,256K*8-120,5V,PLCC32,BT	
411665700007	PWA;PWA-6020 BATT/TP TRANSLATION	
271071000002	RES;0 ,1/16W,0603,SMT	R2,3
272075470701	CAP;47P ,50V ,+80-20%,0603,SMT	C1,2
291000012406	CON;HDR,SHROUD,MA,12P*2,1.27,ST,	J2
291000140601	CON;FPC/FFC,6P,1MM,ST,SMT	J511
291000020202	CON;HDR,MA,2P*1,1.25,R/A,SMT,HIR	J1,3
297040101003	SW;PUSH BUTTON,SPST,.1A,30V,2P,S	SW1,2
331030006006	CON;HDR,MA,6P*1,2.0,ST,GLD	PJ1
442110500009	TOUCH PAD MODULE;904255-0002,602	
442665700002	BATT ASSY;11V/1.6AH,LI,SANYO,602	
412155600011	PCB ASSY;FAX MODEM,US,SOFT,6020	
523410295017	BFM-SHP;CD ROM DRIVE,24X,CD-224E	
342665700005	BRACKET;CDROM-P,PRT	
340665700011	BEZEL ASSY;TEAC,CDROM,6020	
370102630502	SPC-SCREW;M2.6L5,K-HEAD(+),NIB	
442665700001	AC ADPT ASSY;19V/2.64A,6020	
340665700004	COVER ASSY;LENS,6020,ASM	

10. SYSTEM BLOCK DIAGRAM & SCHEMATICS



10. SYSTEM BLOCK DIAGRAM & SCHEMATICS

MOTHER-BOARD

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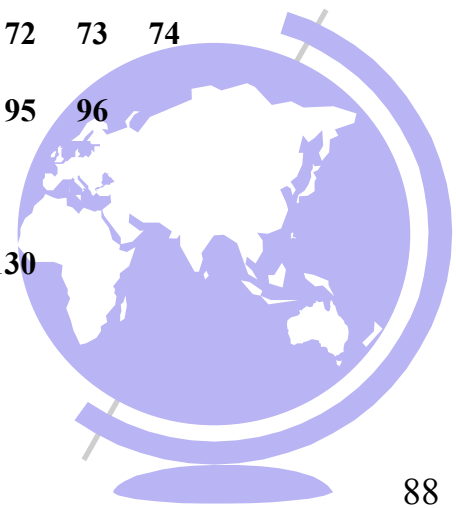

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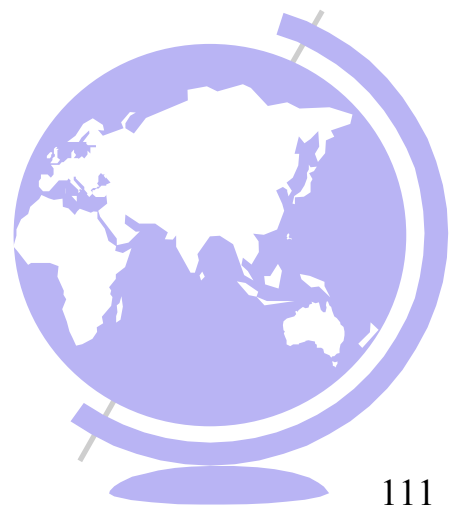

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