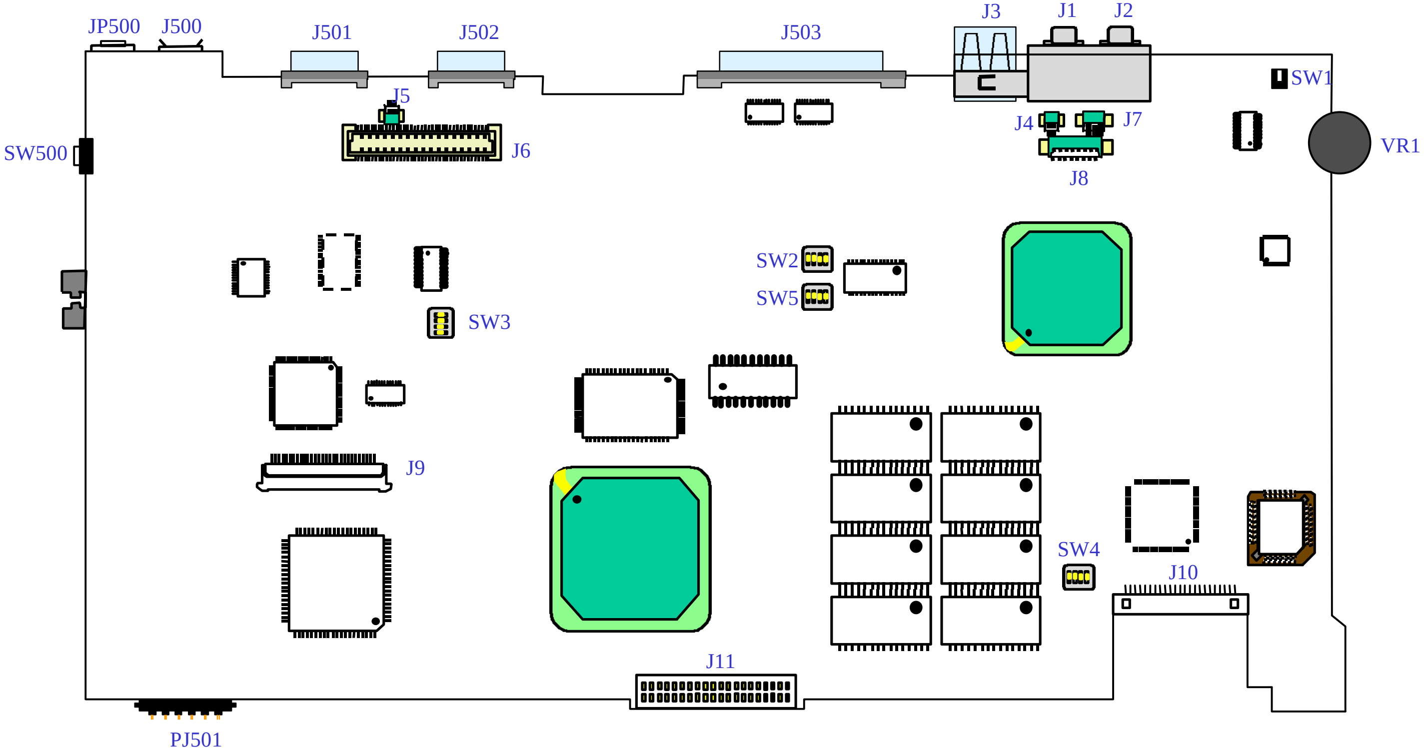
5133S M/B Maintenance

5133S M/B Maintenance

1. Definition & location of connectors/switchs (side A)

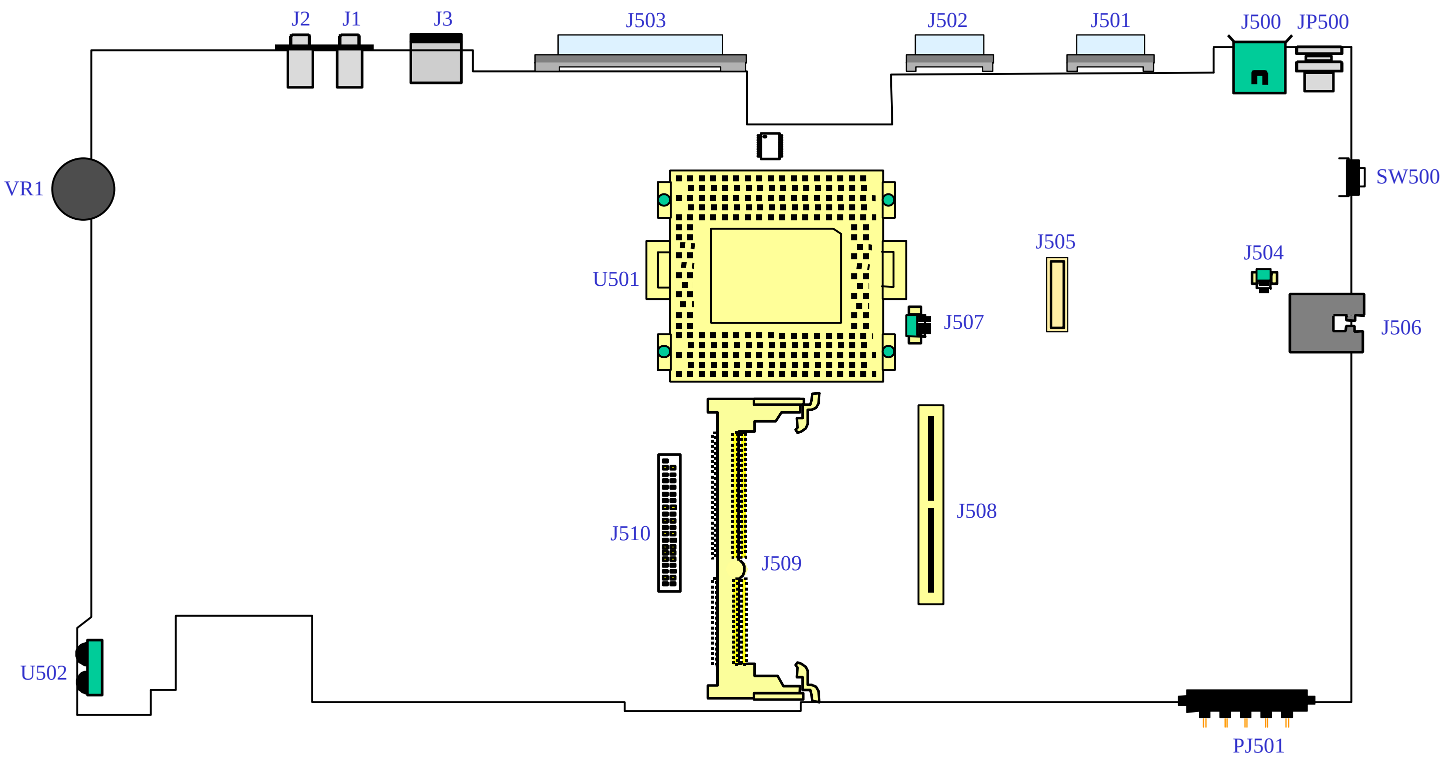
- J1: Line out phone jack.
- J2: External micro phone jack.
- J3: USB port.
- J4,J5: R/L speaker connector.
- J6: LCD flat panel connector.
- J7: Internal micro phone connector.
- J8:Inverter BD. connector.
- J9: Internal keyboard connector.
- J10: FDD connector.
- J11: Touch pad/ HDD connector.
- SW1:Cover switch.
- SW2: Bus fraction switch.
- SW3: Vcore voltage select.
- SW4: LCD ID key matrix select.
- SW5:CPU front bus Clock select.
- VR1: Volume control VR.



5133S M/B Maintenance

1. Definition & location of connectors/switchs (side B)

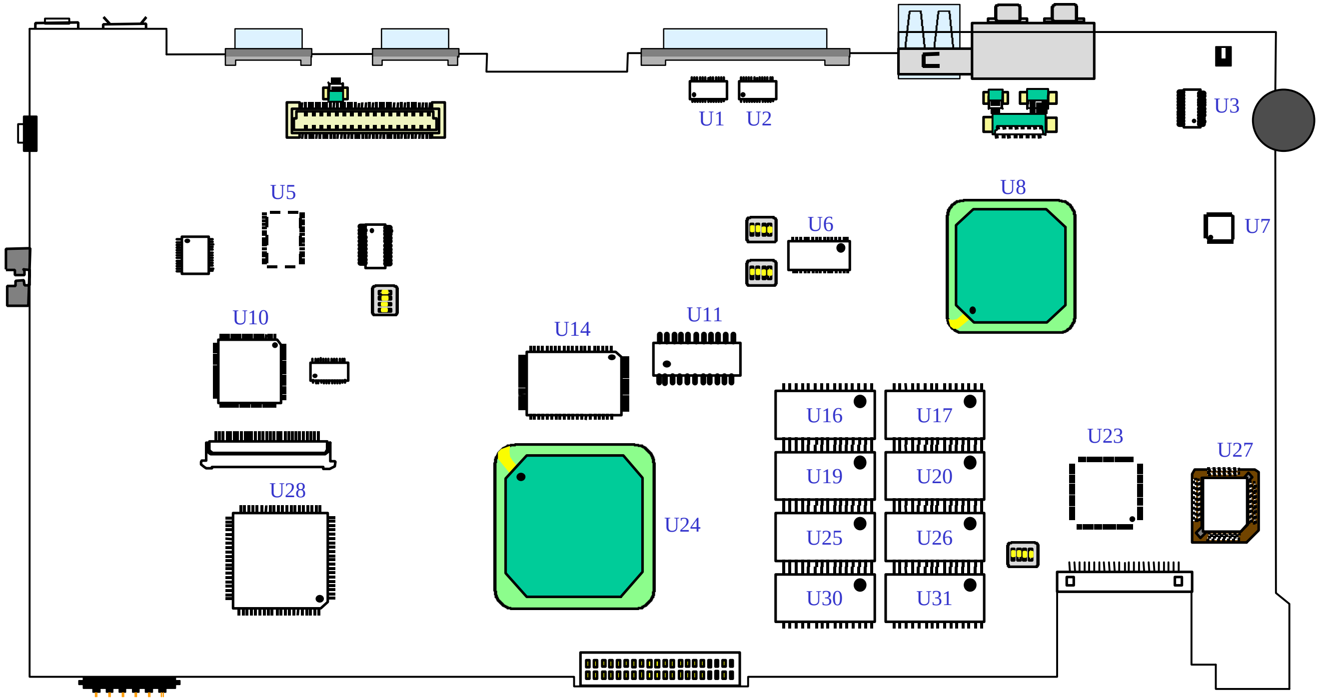
- J500: PS/2 connector.
- PJ500: Power jack.
- PJ501: Battery connector.
- J501: External VGA connector.
- J502: Serial Port connector.
- J503: Parallel Port connector.
- J504:Modem Daughter Board to RJ11connect.
- J505:Modem daughter board connector AC-link.
- J506:RJ11 Phone Jack.
- J507: CPU FAN.
- J508: PCMCIA connector.
- J509:144 Pins SODIMM socket.
- J510: CO-ROM connector.
- SW500: Power button.



5133S M/B Maintenance

2. Definition & location of major components (side A)

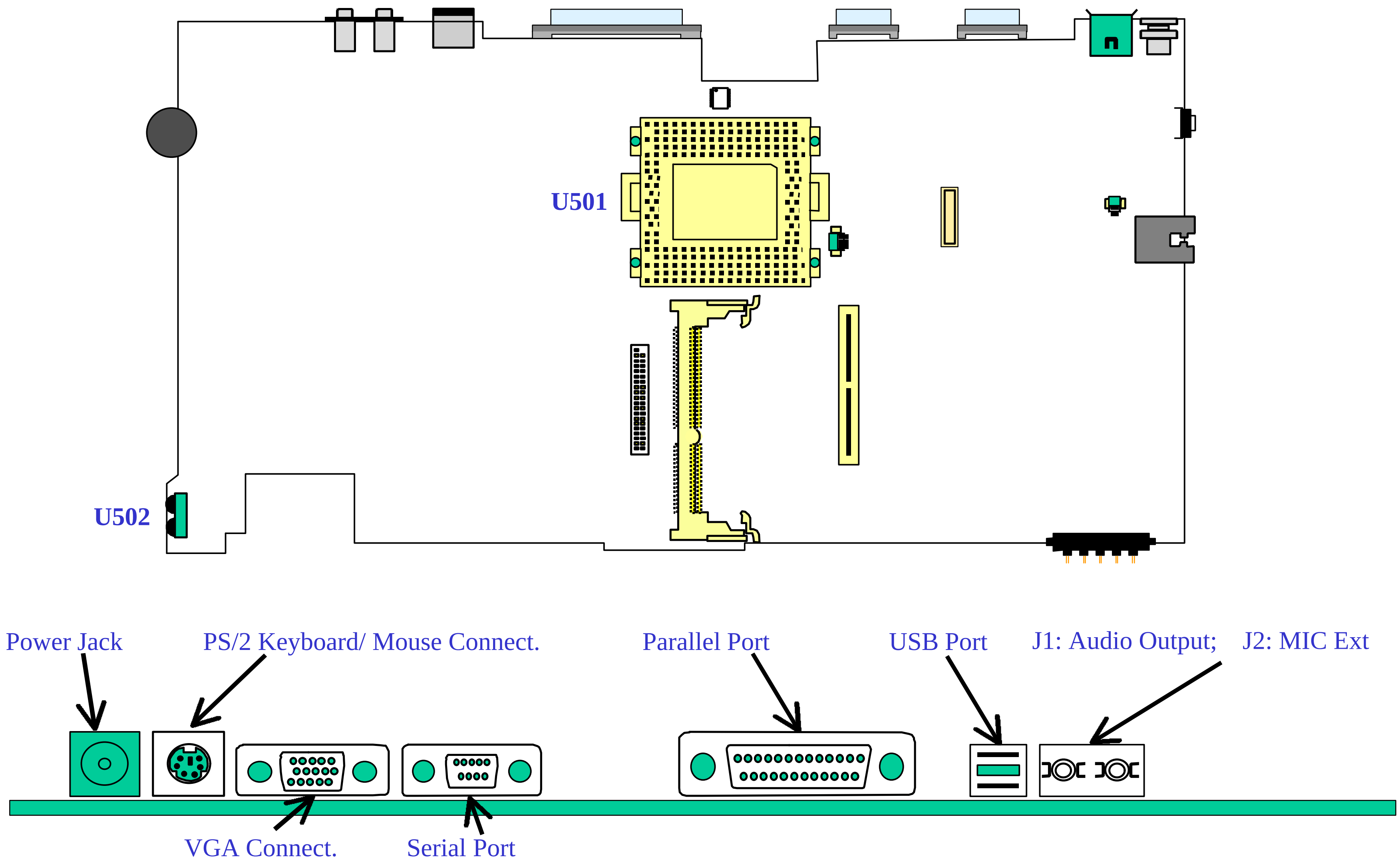
- U3: TPA0202 Amplifier.
- U5: LVDS Transmitter.
- U6: ICS9248-101 clock generator.
- U7: AD1881 Audio codec.
- U8: VT82C686A Super South Bridge.
- U10: H8/F3434 keyboard controller.
- U11: TAG.
- U14: PBSRAM.
- U16,U19,U25,U30: 32MB on-board memory.
- U17,U20,U26,U31:32MB on-board memory.
- U23: PC97338VJG Super I/O controller.
- U24: CBI-7 North Bridge.
- U27: Flash ROM BIOS.
- U28: PCI1221 PQFP PCMCIA controller.



5133S M/B Maintenance

2. Definition & location of major components (side B)

- U501: Socket 7.
- U502:HSDL-3600 SIR port.



5133S M/B Maintenance

3. Pin descriptions of major components

3.1 AMD-K6-2 Processor-1

Signal Name	I/O	Signal Description
A20M# **(Address Bit 20 Mask)**	I	A20M# is used to simulate the behavior of the 8086 when running in Real mode. The assertion of A20M# causes the processor to force bit 20 of the physical address to 0 prior to accessing the cache or driving out a memory bus cycle. The clearing of address bit 20 maps addresses that extend above the 8086 1-Mbyte limit to below 1 Mbyte.
A[31:3] **(Address Bus)**	**O**	A[31:3] contain the physical address for the current bus cycle. The processor drives addresses on A[31:3] during memory and I/O cycles, and cycle definition information during special bus cycles. The processor samples addresses on A[31:5] during inquire cycles.
ADS# **(Address Strobe)**	**O**	The assertion of ADS# indicates the beginning of a new bus cycle. The address bus and all cycle definition signals corresponding to this bus cycle are driven valid off the same clock edge as ADS#.
ADSC# **(Address Strobe Copy)**	**I**	ADSC# has the identical function and timing as ADS#. In the event ADS# becomes too heavily loaded due to a large fanout in a system, ADSC# can be used to split the load across two outputs, which can improve system timing.
AHOLD **(Address Hold)**	**I**	AHOLD can be asserted by the system to initiate one or more inquire cycles. To allow the system to drive the address bus during an inquire cycle, the processor floats A[31:3] and AP off the clock edge on which AHOLD is sampled asserted. The data bus and all other control and status signals remain under the control of the processor and are not floated. This allows a bus cycle that is in progress when AHOLD is sampled asserted to continue to completion. The processor resumes driving the address bus off the clock edge on which AHOLD is sampled negated. If AHOLD is sampled asserted, ADS# is only asserted in order to perform a writeback cycle due to an inquire cycle that hits a modified cache line.
AP **(Address Parity)**	**I/O**	AP contains the even parity bit for cache line addresses driven and sampled on A[31:5]. Even parity means that the total number of 1 bits on AP and A[31:5] is even. (A4 and A3 are not used for the generation or checking of address parity because these bits are not required to address a cache line.) AP is driven by the processor during processor-initiated cycles and is sampled by the processor during inquire cycles. If AP does not reflect even parity during an inquire cycle, the processor asserts APCHK# to indicate an address bus parity check. The processor does not take an internal exception as the result of detecting an address bus parity check, and system logic must respond appropriately to the assertion of this signal.

Signal Name	I/O	Signal Description
APCHK# **(Address Parity Check)**	**O**	If the processor detects an address parity error during an inquire cycle, APCHK# is asserted for one clock. The processor does not take an internal exception as the result of detecting an address bus parity check, and system logic must respond appropriately to the assertion of this signal. The processor ensures that APCHK# does not glitch, enabling the signal to be used as a clocking source for system logic.
BE[7:0]# **(Byte Enables)**	**I**	BE[7:0]# are used by the processor to indicate the valid data bytes during a write cycle and the requested data bytes during a read cycle. The byte enables can be used to derive address bits A[2:0], which are not physically part of the processor's address bus. The processor checks and generates valid data parity for the data bytes that are valid as defined by the byte enables. The eight byte enables correspond to the eight bytes of the data bus as follows: BE7#: D[63:56] BE3#: D[31:24] BE6#: D[55:48] BE2#: D[23:16] BE5#: D[47:40] BE1#: D[15:8] BE4#: D[39:32] BE0#: D[7:0] The processor expects data to be driven by the system logic on all eight bytes of the data bus during a burst cache-line read cycle, independent of the byte enables that are asserted. The byte enables are also used to distinguish between special bus cycles as defined in Table 23 on page 122.
BF[2:0] **(Bus requency)**	**I**	BF[2:0] determine the internal operating frequency of the processor. The frequency of the CLK input signal is multiplied internally by a ratio determined by the state of these signals as defined in Table 16. BF[2:0] have weak internal pullups and default to the 3.5 multiplier if left unconnected. **Processor-to-Bus Clock Ratios** **State of BF[2:0] Inputs** — **Processor-Clock to Bus-Clock Ratio** 110b — 2.0x 100b — 2.5x 101b — 3.0x 111b — 3.5x 010b — 4.0x 000b — 4.5x 001b — 5.0x 011b — 5.5x

3.1 AMD-K6-2 Processor-2

Signal Name	I/O	Signal Description
BOFF# **(Backoff)**	**I**	If BOFF# is sampled asserted, the processor unconditionally aborts any cycles in progress and transitions to a bus hold state by floating the following signals: A[31:3], ADS#, ADSC#, AP, BE[7:0]#, CACHE#, D[63:0], D/C#, DP[7:0], LOCK#, M/IO#, PCD, PWT, SCYC, and W/R#. These signals remain floated until BOFF# is sampled negated. This allows an alternate bus master or the system to control the bus. When BOFF# is sampled negated, any processor cycle that was aborted due to the assertion of BOFF# is restarted from the beginning of the cycle, regardless of the number of transfers that were completed. If BOFF# is sampled asserted on the same clock edge as BRDY# of a bus cycle of any length, then BOFF# takes precedence over the BRDY#. In this case, the cycle is aborted and restarted after BOFF# is sampled negated.
BRDY# **(Burst Ready)**	**I**	BRDY# is asserted to the processor by system logic to indicate either that the data bus is being driven with valid data during a read cycle or that the data bus has been latched during a write cycle. If necessary, the system logic can insert bus cycle wait states by negating BRDY# until it is ready to continue the data transfer. BRDY# is also used to indicate the completion of special bus cycles.
BRDYC# **(Burst Ready Copy)**	**I**	BRDYC# has the identical function as BRDY#. In the event BRDY# becomes too heavily loaded due to a large fanout or loading in a system, BRDYC# can be used to reduce this loading, which improves timing. In addition, BRDYC# is sampled when RESET is negated to configure the drive strength of A[20:3], ADS#, HITM#, and W/R#. If BRDYC# is 0 during the falling transition of RESET, these particular outputs are configured using higher drive strengths than the standard strength. If BRDYC# is 1 during the falling transition of RESET, the standard strength is selected.
BREQ **(Bus Request)**	**O**	BREQ is asserted by the processor to request the bus in order to complete an internally pending bus cycle. The system logic can use BREQ to arbitrate among the bus participants. If the processor does not own the bus, BREQ is asserted until the processor gains access to the bus in order to begin the pending cycle or until the processor no longer needs to run the pending cycle. If the processor currently owns the bus, BREQ is asserted with ADS#. The processor asserts BREQ for each assertion of ADS# but does not necessarily assert ADS# for each assertion of BREQ.

Signal Name	I/O	Signal Description
CACHE# **(Cacheable Access)**	**O**	For reads, CACHE# is asserted to indicate the cacheability of the current bus cycle. In addition, if the processor samples KEN# assert ed, which i ndicates the driven address is cacheable, the cycle is a 32-byte burst read cycle. For write cycles, CACHE# is asserted to indicate the current bus cycle is a modified cache-line writeback. KEN# is ignored during writebacks. If CACHE# is not asserted, or if KEN# is sampled negated during a read cycle, the cycle is not cacheable and defaults to a single-transfer cycle.
CLK **(Clock)**	**I**	The CLK signal is the bus clock for the processor and is the reference for all signal timings under normal operation (except for TDI, TDO, TMS, and TRST#). BF[2:0] determine the internal frequency multiplier applied to CLK to obtain the processor's core operating frequency. See "BF[2:0] (Bus Frequency)"on page 88 for a list of the processor-to-bus clock ratios.
D/C# **(Data/Code)**	**O**	The processor drives D/C # during a memory bus cycle to indicate whether it is addressing data or executable code. D/C# is also used to define other bus cycles, including interrupt acknowledge and special cycles. See Table 23 on page 122 for more details.
D[63:0] **(Data Bus)**	I/O	D[63:0] represent the processor's 64-bit data bus. Each of the eight bytes of data that comprise this bus is qualified as valid by its corresponding byte enable. See "BE[7:0]# (Byte Enables)"on page 87.
DP[7:0] **(Data Parity)**	I/O	DP[7:0] are even parity bits for each valid byte of data--as defined by BE[7:0]#--driven and sampled on the D[63:0] data bus. Even parity means that the total number of 1 bits within each byte of data and its respective data parity bit is an even number. DP[7:0] are driven by the processor during write cycles and sampled by the processor during read cycles. If the processor detects bad parity on any valid byte of data during a read cycle, PCHK# is asserted for one clock beginning the clock edge after BRDY# is sampled asserted. The processor does not take an internal exception as the result of detecting a data parity check, and system logic must respond appropriately to the assertion of this signal. The eight data parity bits correspond to the eight bytes of the data bus as follows: DP7: D[63:56] DP3: D[31:24] DP6: D[55:48] DP2: D[23:16] DP5: D[47:40] DP1: D[15:8] DP4: D[39:32] DP0: D[7:0] For systems that do not support data parity, DP[7:0] should be connected to Vcc3 through pullup resistors.

3.1 AMD-K6-2 Processor-3

Signal Name	I/O	Signal Description
EADS# **(External Address Strobe)**	I	System logic asserts EADS# during a cache inquire cycle to indicate that the address bus contains a valid address. EADS# can only be driven after the system logic has taken control of the address bus by asserting AHOLD or BOFF# or by receiving HLDA. The processor responds to the sampling of EADS# and the address bus by driving HIT#, which indicates if the inquired cache line exists in the processor 's cache, and HITM#, which indicates if it is in the modified state.
EWBE# **(External Write Buffer Empty)**	I	The system logic can negate EWBE# to the processor to indicate that its external write buffers are full and that additional data cannot be stored at this time. This causes the processor to delay the following activities until EWBE# is sampled asserted: ▪ The commitment of write hit cycles to cache lines in the modified state or exclusive state in the processor 's cache ▪ The decode and execution of an instruction that follows a currently-executing serializing instruction ▪ The assertion or negation of SMIACT# ▪ The entering of the Halt state and the Stop Grant state Negating EWBE# does not prevent the completion of any type of cycle that is currently in progress.
FERR# **(Floating-Point Error)**	O	The assertion of FERR # indicates the occurrence of an unmasked fl oati ng-point exception resulting from the execution of a floating-point instruction. This signal is provided to allow the system logic to handle this exception in a manner consistent with IBM-compatible PC/AT systems. See "Handling Floating-Point Exceptions" on page 191 for a system logic implementation that supports floating-point exceptions. The state of the numeric error (NE) bit in CR0 does not affect the FERR# signal. The processor ensures that FERR# does not glitch, enabling the signal to be used as a clocking source for system logic.
FLUSH# **(Cache Flush)**	I	In response to sampling FLUSH# asserted, the processor writes back any data cache lines that are in the modified state, invalidates all lines in the instruction and data caches, and then executes a flush acknowledge special cycle. See Table 23 on page 122 for the bus definition of special cycles. In addition, FLUSH# is sampled when RESET is negated to determine if the processor enters the Tri-State Test mode. If FLUSH# is 0 during the falling transition of RESET, the processor enters the Tri-State Test mode instead of performing the normal RESET functions.

Signal Name	I/O	Signal Description
HIT# **(Inquire Cycle Hit)**	O	The processor asserts HIT# during an inquire cycle to indicate that the cache line is valid within the processor's instruction or data cache (also known as a cache hit). The cache line can be in the modified, exclusive, or shared state.
HITM# **(Inquire Cycle Hit To Modified Line)**	O	The processor asserts HITM# during an inquire cycle to indicate that the cache line exists in the processor data cache in the modified state. The processor's performs a writeback cycle as a result of this cache hit. If an inquire cycle hits a cache line that is currently being written back, the processor asserts HITM# but does not execute another writeback cycle. The system logic must not expect the processor to assert ADS# each time HITM# is asserted.
HLDA **(Hold Acknowledge)**	O	When HOLD is sampled asserted, the processor completes the current bus cycles, floats the processor bus, and asserts HLDA in an acknowledgment that these events have been completed. The processor does not assert HLDA until the completion of a locked sequence of cycles. While HLDA is asserted, another bus master can drive cycles on the bus, including inquire cycles to the processor. The following signals are floated when HLDA is asserted: A[31:3], ADS #, ADSC#, AP, BE[7:0]#, CACHE#, D[63:0], D/C#, DP[7:0], LOCK#, M/IO#, PCD, PWT, SCYC, and W/R#. The processor ensures that HLDA does not glitch.
HOLD **(Bus Hold Request)**	I	The system logic can assert HOLD to gain control of the processor's bus. When HOLD is sampled asserted, the processor completes the current bus cycles, floats the processor bus, and asserts HLDA in an acknowledgment that these events have been completed.

3.1 AMD-K6-2 Processor-4

Signal Name	I/O	Signal Description
IGNNE# (Ignore Numeric Exception)	I	IGNNE#, in conjunction with the numeric error (NE) bit in CR0, is used by the system logic to control the effect of an unmasked floating-point exception on a previous floating-point instruction during the execution of a floating-point instruction, MMX instruction, 3DNow! instruction, or the WAIT instruction-- hereafter referred to as the target instruction. If an unmasked floating-point exception is pending and the target instruction is considered error-sensitive, then the relationship between NE and IGNNE# is as follows: ☐ If NE = 0, then: ▪ If IGNNE# is sampled asserted, the processor ignores the floating-point exception and continues with the execution of the target instruction. ▪ If IGNNE# is sampled negated, the processor waits until it samples IGNNE#, INTR, SMI#, NMI, or INIT asserted. ▪ If IGNNE# is sampled asserted while waiting, the processor ignores the floating-point exception and continues with the execution of the target instruction. ▪ If INTR, SMI#, NMI, or INIT is sampled asserted while waiting, the processor handles its assertion appropriately. ☐ If NE = 1, the processor invokes the INT 10h exception handler. If an unmasked floating-point exception is pending and the target instruction is considered error-insensitive, then the processor ignores the floating-point exception and continues with the execution of the target instruction. FERR# is not affected by the state of the NE bit or IGNNE#. FERR# is always asserted at the instruction boundary of the target instruction that follows the floating-point instruction that caused the unmasked floating-point exception. This signal is provided to allow the system logic to handle exceptions in a manner consistent with IBM-compatible PC/AT systems.
INIT (Initialization)	I	The assertion of INIT causes the processor to empty its pipelines, to initialize most of its internal state, and to branch to address FFFF_FFF0h--he same instruction execution starting point used after RESET. Unlike RESET, the processor preserves the contents of its caches, the floating-point state, the MMX state, Model-Specific Registers, the CD and NW bits of the CR0 register, and other specific internal resources. INIT can be used as an accelerator for 80286 code that requires a reset to exit from Protected mode back to Real mode.

Signal Name	I/O	Signal Description
INTR (Maskable Interrupt)	I	INTR is the system's maskable interrupt input to the processor. When the processor samples and recognizes INTR asserted, the processor executes a pair of interrupt acknowledge bus cycles and then jumps to the interrupt service routine specified by the interrupt number that was returned during the interrupt acknowledge sequence. The processor only recognizes INTR if the interrupt flag (IF) in the EFLAGS register equals 1.
INV (Invalidation Request)	I	During an inquire cycle, the state of INV determines whether an addressed cache line that is found in the processor instruction or data cache transitions to the invalid state or the shared state. If INV is sampled asserted during an inquire cycle, the processor's transitions the cache line (if found) to the invalid state, regardless of its previous state. If INV is sampled negated during an inquire cycle, the processor transitions the cache line (if found) to the shared state. In either case, if the cache line is found in the modified state, the processor writes it back to memory before changing its state.
KEN# (Cache Enable)	I	If KEN# is sampled asserted, it indicates that the address presented by the processor is cacheable. If KEN# is sampled asserted and the processor intends to perform a cache-line fill (signified by the assertion of CACHE#), the processor executes a 32-byte burst read cycle and expects to sample BRDY# asserted a total of four times. If KEN# is sampled negated during a read cycle, a single-transfer cycle is executed and the processor does not cache the data. For write cycles, CACHE# is asserted to indicate the current bus cycle is a modified cache-line writeback. KEN# is ignored during writebacks. If PCD is asserted during a bus cycle, the processor does not cache any data read during that cycle, regardless of the state of KEN#. See "PCD (Page Cache Disable)" on page 109 for more details. If the processor has sampled the state of KEN# during a cycle, and that cycle is aborted due to the sampling of BOFF# asserted, the system logic must ensure that KEN# is sampled in the same state when the processor restarts the aborted cycle.

3.1 AMD-K6-2 Processor-5

Signal Name	I/O	Signal Description
LOCK# **(Bus Lock)**	O	The processor asserts LOCK# during a sequence of bus cycles to ensure that the cycles are completed without allowing other bus masters to intervene. Locked operations consist of two to five bus cycles. LOCK# is asserted during the following operations: ▪ An interrupt acknowledge sequence ▪ Descriptor Table accesses ▪ Page Directory and Page Table accesses ▪ XCHG instruction ▪ An instruction with an allowable LOCK prefix In order to ensure that locked operations appear on the bus and are visible to the entire system, any data operands addressed during a locked cycle that reside in the processor's cache are flushed and invalidated from the cache prior to the locked operation. If the cache line is in the modified state, it is written back and invalidated prior to the locked operation. Likewise, any data read during a locked operation is not cached. The processor ensures that LOCK# does not glitch.
M/IO# **(Memory or I/O)**	O	The processor drives M/IO# during a bus cycle to indicate whether it is addressing the memory or I/O space. If M/IO# = 1, the processor is addressing memory or a memory-mapped I/O port as the result of an instruction fetch or an instruction that loads or stores data. If M/IO# = 0, the processor is addressing an I/O port during the execution of an I/O instruction. In addition, M/IO# is used to define other bus cycles, including interrupt acknowledge and special cycles. See Table 23 on page 122 for more details.
NA# **(Next Address)**	I	System logic asserts NA# to indicate to the processor that it is ready to accept another bus cycle pipelined into the previous bus cycle. ADS#, along with address and status signals, can be asserted as early as one clock edge after NA# is sampled asserted if the processor is prepared to start a new cycle. Because the processor allows a maximum of two cycles to be in progress at a time, the assertion of NA# is sampled while two cycles are in progress but ADS# is not asserted until the completion of the first cycle.
NMI **(Non-Maskable Interrupt)**	I	When NMI is sampled asserted, the processor jumps to the interrupt service routine defined by interrupt number 02h. Unlike the INTR signal, software cannot mask the effect of NMI if it is sampled asserted by the processor. However, NMI is temporarily masked upon entering System Management Mode (SMM). In addition, an interrupt acknowledge cycle is not executed because the interrupt number is predefined. If NMI is sampled asserted while the processor is executing the interrupt service routine for a previous NMI, the subsequent NMI remains pending until the completion of the execution of the IRET instruction at the end of the interrupt service routine.

Signal Name	I/O	Signal Description
PCD **(Page Cache Disable)**	O	The processor drives PCD to indicate the operating system's specification of cacheability for the page being addressed. System logic can use PCD to control external caching. If PCD is asserted, the addressed page is not cached. If PCD is negated, the cacheability of the addressed page depends upon the state of CACHE# and KEN#. The state of PCD depends upon the processor's operating mode and the state of certain bits in its control registers and TLB as follows: ☐ In Real mode, or in Protected and Virtual-8086 modes while paging is disabled (PG bit in CR0 set to 0): PCD output = CD bit in CR0 ☐ In Protected and Virtual-8086 modes while caching is enabled (CD bit in CR0 set to 0) and paging is enabled (PG bit in CR0 set to 1): ▪ For accesses to I/O space, page directory entries, and other non-paged accesses: PCD output = PCD bit in CR3 ▪ For accesses to 4-Kbyte page table entries or 4-Mbyte pages: PCD output = PCD bit in page directory entry ▪ For accesses to 4-Kbyte pages: PCD output = PCD bit in page table entry
PCHK# **(Parity Check)**	O	The processor asserts PCHK# during read cycles if it detects an even parity error on one or more valid bytes of D[63:0] during a read cycle. (Even parity means that the total number of 1 bits within each byte of data and its respective data parity bit is even.) The processor checks data parity for the data bytes that are valid, as defined by BE[7:0]#, the byte enables. PCHK# is always driven but is only asserted for memory and I/O read bus cycles and the second cycle of an interrupt acknowledge sequence. PCHK# is not driven during any type of write cycles or special bus cycles. The processor does not take an internal exception as the result of detecting a data parity error, and system logic must respond appropriately to the assertion of this signal. The processor ensures that PCHK# does not glitch, enabling the signal to be used as a clocking source for system logic.

3.1 AMD-K6-2 Processor-6

Signal Name	I/O	Signal Description
PWT (Page Writethrough)	O	The processor drives PWT to indicate the operating system's specification of the writeback state or writethrough state for the page being addressed. PWT, together with WB/ WT#, specifies the data cache-line state during cacheable read misses and write hits to shared cache lines. See "WB/WT# (Writeback or Writethrough)" on page 119 for more details. The state of PWT depends upon the processor's operating mode and the state of certain bits in its control registers and TLB as follows: ☐ In Real mode, or in Protected and Virtual-8086 modes while paging is disabled (PG bit in CR0 set to 0): PWT output = 0 (writeback state) ☐ In Protected and Virtual-8086 modes while paging is enabled (PG bit in CR0 set to 1): ▪ For accesses to I/O space, page directory entries, and other non-paged accesses: PWT output = PWT bit in CR3 ▪ For accesses to 4-Kbyte page table entries or 4-Mbyte pages: PWT output = PWT bit in page directory entry ▪ For accesses to 4-Kbyte pages: PWT output = PWT bit in page table entry
RESET (Reset)	I	When the processor samples RESET asserted, it immediately flushes and initializes all internal resources and its internal state including its pipelines and caches, the floating-point state, the MMX state, the 3DNow! state, and all registers, and then the processor jumps to address FFFF_FFF0h to start instruction execution. The signals BRDYC# and FLUSH# are sampled during the falling transition of RESET to select the drive strength of selected output signals and to invoke the Tri-State Test mode, respectively. See these signal descriptions for more details.
RSVD (Reserved)	R	Reserved signals are a special class of pins that can be treated in one of the following ways: ▪ As no-connect (NC) pins, in which case these pins are left unconnected ▪ As pins connected to the system logic as defined by the industry-standard Pentium interface (Socket 7) ▪ Any combination of NC and Socket 7 pins In any case, if the RSVD pins are treated accordingly, the normal operation of the AMD-K6-2 processor is not adversely affected in any manner. See "Pin Designations" on page 271 for a list of the locations of the RSVD pins.

Signal Name	I/O	Signal Description
SCYC (Split Cycle)	O	The processor asserts SCYC during misaligned, locked transfers on the D[63:0] data bus. The processor generates additional bus cycles to complete the transfer of misaligned data. For purposes of bus cycles, the term *aligned* means: ▪ Any 1-byte transfers ▪ 2-byte and 4-byte transfers that lie within 4-byte address boundaries ▪ 8-byte transfers that lie within 8-byte address boundaries
SMI# (System Management Interrupt)	I	The assertion of SMI# causes the processor to enter System Management Mode (SMM). Upon recognizing SMI#, the processor performs the following actions, in the order shown: 1. Flushes its instruction pipelines 2. Completes all pending and in-progress bus cycles 3. Acknowledges the interrupt by asserting SMIACT# after sampling EWBE# asserted 4. Saves the internal processor state in SMM memory 5. Disables interrupts by clearing the interrupt flag (IF) in EFLAGS and disables NMI interrupts 6. Jumps to the entry point of the SMM service routine at the SMM base physical address which defaults to 0003_8000h in SMM memory See "System Management Mode (SMM)" on page 195 for more details regarding SMM.
SMIACT# (System Management Interrupt Active)	O	The processor acknowledges the assertion of SMI# with the assertion of SMIACT# to indicate that the processor has entered System Management Mode (SMM). The system logic can use SMIACT# to enable SMM memory. See "SMI# (System Management Interrupt)" on page 113 for more details. See "System Management Mode (SMM)" on page 195 for more details regarding SMM.

3.1 AMD-K6-2 Processor-7

Signal Name	I/O	Signal Description
STPCLK# (Stop Clock)	I	The assertion of STPCLK# causes the processor to enter the Stop Grant state, during which the processor's internal clock is stopped. From the Stop Grant state, the processor can subsequently transition to the Stop Clock state, in which the bus clock CLK is stopped. Upon recognizing STPCLK#, the processor performs the following actions, in the order shown: 1. Flushes its instruction pipelines 2. Completes all pending and in-progress bus cycles 3. Acknowledges the STPCLK# assertion by executing a Stop Grant special bus cycle (see Table 23 on page 122) 4. Stops its internal clock after BRDY# of the Stop Grant special bus cycle is sampled asserted and after EWBE# is sampled asserted 5. Enters the Stop Clock state if the system logic stops the bus clock CLK (optional) See "Clock Control" on page 225 for more details regarding clock control.
TCK (Test Clock)	I	TCK is the clock for boundary-scan testing using the Test Access Port (TAP). See "Boundary-Scan Test Access Port (TAP)" on page 207 for details regarding the operation of the TAP controller.
TDI (Test Data Input)	I	TDI is t he ser i al test data and instruction input for boundary-scan testing using the Test Access Port (TAP). See "Boundary-Scan Test Access Port (TAP)" on page 207 for details regarding the operation of the TAP controller.
TDO (Test Data Output)	O	TDO is the serial test data and instruction output for boundary-scan testing using the Test Access Port (TAP). See "Boundary-Scan Test Access Port (TAP)" on page 207 for details regarding the operation of the TAP controller.
TMS (Test Mode Select)	I	TMS specifies the test function and sequence of state changes for boundary-scan testing using the Test Access Port (TAP). See "Boundary-Scan Test Access Port (TAP)" on page 207 for details regarding the operation of the TAP controller.
TRST# (Test Reset)	I	The assertion of TRST# initializes the Test Access Port (TAP) by resetting its state machine to the Test-Logic-Reset state. See 'Boundary-Scan Test Access Port (TAP)" on page 207 for details regarding the operation of the TAP controller.
VCC2DET (Vcc2 Detect)	O	VCC2DET is internally tied to Vss (logic level 0) to indicate to the system logic that it must supply the specified dual-voltage requirements to the Vcc2 and Vcc3 pins. The Vcc2 pins supply voltage to the processor core, independent of the voltage supplied to the I/O buffers on the Vcc3 pins. Upon sampling VCC2DET Low, system logic should sample VCC2H/L# to identify core voltage requirements.

Signal Name	I/O	Signal Description
VCC2H/L# (Vcc2 High/Low)	O	VCC2DET is internally tied to Vss (logic level 0) to indicate to the system logic that it must supply the specified dual-voltage requirements to the Vcc2 and Vcc3 pins. The Vcc2 pins supply voltage to the processor core, independent of the voltage supplied to the I/O buffers on the Vcc3 pins. Upon sampling VCC2DET Low, system logic should sample VCC2H/L# to identify core voltage requirements.
VCC2H/L# (Vcc2 High/Low)	O	VCC2H/L# is internally tied to Vss (logic level 0) to indicate to the system logic that it must supply the specified processor core voltage to the Vcc2 pins. The Vcc2 pins supply voltage to the processor core, independent of the voltage supplied to the I/O buffers on the V3 pins. Upon sampling VCC2DET Low to identify dual-voltage processor requirements, system logic should sample VCC2H/L# to identify the core vol tage requirements for 2.9 V and 3.2 V products (High) and 2.2V products (Low).
W/R# (Write/Read)	O	The processor drives W/R# to indicate whether it is performing a write or a read cycle on the bus. In addition, W/R# is used to define other bus cycles, including interrupt acknowledge and special cycles. See Table 23 on page 122 for more details.
WB/WT# (Writeback or Writethrough)	I	WB/WT#, together with PWT, specifies the data cache-line state during cacheable read misses and write hits to shared cache lines. If WB/WT# = 0 or PWT = 1 during a cacheable read miss or write hit to a shared cache line, the accessed line is cached in the shared state. This is referred to as the writethrough state because all write cycles to this cache line are driven externally on the bus. If WB/WT# = 1 and PWT = 0 during a cacheable read miss or a write hit to a shared cache line, the accessed line is cached in the exclusive state. Subsequent write hits to the same line cause its state to transition from exclusive to modified. This is referred to as the writeback state because the data cache can contain modified cache lines that are subject to be written back--referred to as a writeback cycle--as the result of an inquire cycle, an internal snoop, a flush operation, or the WBINVD instruction.

5133S M/B Maintenance

3.2 VIA North Bridge and Super South Bridge Feature:

. VIA VT8501 Apollo MVP4 Feature:

- Supports all Socket 7 Host Interface
- Support Advanced L2 Cache
- Internal Accelerated Graphics Port (AGP) Controller
- Support Concurrent PCI Bus Controller
- High-Performance DRAM Controller
- Sophisticated Power Management Features
- General Graphic Capabilities
- High Performance rCADE3DTM Accelerator
- Support DVD
- Support Video Processor on-chip
- Digital Flat Panel (DFP) Interface
- Build-in NAND-tree scan test capability

. VIA VT82C686A Super South Bridge Feature:

- Inter-operable with VIA and other Host-to-PCI Bridges
- PCI to ISA Bridge
- UltraDMA-33 / 66 Master Mode PCI EIDE Controller
- Integrated Super IO Controller
- SoundBlaster Pro Hardware and Direct Sound Ready AC97 Digital Audio Controller
- Voltage, Temperature, Fan Speed Monitor and Controller
- Universal Serial Bus Controller
- System Management Bus Interface
- Sophisticated PC99-Compatible Mobile Power Management
- Plug and Play Controller
- Built-in NAND-tree pin scan test capability
- 0.35um, 3.3V, low power CMOS process
- Single chip 27x27 mm, 352 pin BGA

3.3 VIA VT8501 Apollo MVP4 North Bridge-1

CPU Interface

Signal Name	Pin #	I/O	Signal Description
HD[63:0]	(see pinout tables)	IO	**Host CPU Data.** These signals are connected to the CPU data bus.
BE[7:0]#	B23, A23, C22, B22, A22, D22, E21, D21	I	**Byte Enables.** The CPU byte enables indicate which byte lane the current CPU cycle is accessing.
HA[31:3]	(see pinout tables)	IO	**Host Address Bus.** HA[31:3] connect to the address bus of the host CPU. During CPU cycles HA[31:3] are inputs. These signals are driven by the MVP4 during cache snooping operations.
ADS#	H23	I	**Address Strobe.** The CPU asserts ADS# in T1 of the CPU bus cycle to initiate a command
M/IO#	F22	I	**Memory / IO Command Indicator**
W/R#	J22	I	**Write / Read Command Indicator**
D/C#	J24	I	**Data / Control Command Indicator**
BRDY#	G26	O	**Bus Ready.** The MVP4 asserts BRDY# to indicate to the CPU that data is available on reads or has been received on writes.
EADS#	J23	O	**External Address Strobe.** Asserted by the MVP4 to inquire the L1 cache when serving PCI master accesses to main memory.
KEN# / INV	G22	O	**Cache Enable / Invalidate.** KEN# / INV functions as both the KEN# signal during CPU read cycles and the INV signal during L1 cache snoop cycles.
HITM#	J25	I	**Hit Modified.** Asserted by the CPU to indicate that the address presented with the last assertion of EADS# is modified in the L1 cache and needs to be written back.
HLOCK#	H22	I	**Host Lock.** All CPU cycles sampled with the assertion of HLOCK# and ADS# until the negation of HLOCK# must be atomic.
CACHE#	G23	I	**Cacheable Indicator.** Asserted by the CPU during a read cycle to indicate the CPU can perform a burst line fill. Asserted by the CPU during a write cycle to indicate that the CPU will perform a burst write-back cycle.
AHOLD	G24	O	**Address Hold.** The MVP4 asserts AHOLD when a PCI master is accessing main memory. AHOLD is held for the duration of the PCI burst transfer.
NA#	G25	O	**Next Address Indicator.**
BOFF#	H25	O	**Back Off.** Asserted by the MVP4 when required to terminate a CPU cycle that was in progress.

Signal Name	Pin #	I/O	Signal Description
SMIACT#	H26	I	**System Management Interrupt Active.** This is asserted by the CPU when it is in system management mode as a result of SMI.

Note: Clocking of the CPU and cache interfaces is performed with HCLK; see the clock pin group at the end of the pin descriptions section for descriptions of the clock input pins.
Note: All signals above require 4.7K pullups to VCC3 except EADS#, HITM#, AHOLD, HA, and HD.
Note: All signals above connect directly to the host CPU except HA and HD which connect directly to the L2 cache SRAMs and connect to the host CPU through 22 ohm series resistors (see the "Apollo MVP4 Design Guide" for more information).

L2 Cache Control

Signal Name	Pin #	I/O	Signal Description
CADS#	C21	O	**Cache Address Strobe.** Assertion causes the burst SRAM to load the address register from address pins. Connected to all cache SRAMs.
CADV#	C20	O	**Cache Advance.** Assertion causes the burst SRAM to advance to the next Quadword in the cache line. Connected to all cache SRAMs.
COE#	B21	O	**Cache Output Enable.** Typically connected to all cache SRAMs.
CCS#	A21	O	**Cache Chip Select.** Typically connected to all cache SRAMs.
TA[7:0]	C26, C25, C24, B26, B25, A25, B24, A24	IO	**Tag Address.** TA0-7 are inputs during CPU accesses and outputs during L2 cache line fills and L2 line invalidates during inquire cycles.
TWE#	C23	O	**Tag Write Enable.** When asserted, new state and tag addresses are written into the external tag. Connected to all cache SRAMs.
GWE#	B20	O	**Global Write Enable.** Connected to all cache SRAMs.
BWE#	A20	O	**Byte Write Enable.** Connected to all cache SRAMs.

Note: VT8501 pinouts were defined for optimum use with the ATX PCB form factor (shown in simplified form below). The general component layout shown may be used as a guide for ATX PCB component placement. For more detailed PCB layout and design information and layout recommendations for other PCB form factors, refer to the "Apollo MVP4 Design Guide"

3.3 VIA VT8501 Apollo MVP4 North Bridge-2

DRAM Interface

Signal Name	Pin #	I/O	Signal Description
MD[63:0]	(see pinout tables)	IO	**Memory Data.** These signals are connected to the DRAM data bus. Note: MD0 is internally pulled up for use in EDO memory type detection.
MECC[7-0]	AE22, AF23, V26, V23, AD22, AE23, V24, U23	IO	**DRAM ECC or EC Data.** Note: These pins are powered by VSUS
MA[13:0] / Strap Options	AF25, AE25, AE26, AD25, AD26, AC24, AC25, AC26, AB23, AB24, AB25, AB26, AA24	O /I	**Memory Address.** DRAM address lines. These pins are also used for power-up strapping options (sampled on the rising edge of RESET#): MA13-12 Rx68[1-0] Host CPU Bus Frequency (0=Auto, 1=100, 2=66) MA11 SERR Pin Function (0=SERR, 1=PWRGD) MA10-9 North Bridge Clock Delay (0-3 Clocks) MA8 -reserved-AA23, MA7 Graphics Test Mode (0 =Normal, 1 = Test Mode) MA6 LCD Output (0 = Off, 1 = On) MA5-3 Panel Type (0-3 = TFT, 4-7 = DSTN) MA2 -reserved- MA1-0 Graphics Clock Delay (0-3 Clocks) All pins have internal pull-downs for default low (0). Strap 1 using 4.7KW.
RAS5# / CS5# / CKE1#, RAS4# / CS4# / CKE0#, RAS3# / CS3#, RAS2# / CS2#, RAS1# / CS1#, RAS0# / CS0#	AA25, AA26, Y23, Y24, Y25, Y26	O	**Multifunction Pins** 1. FPG/EDO DRAM: Row Address Strobe of each bank. 2. Synchronous DRAM: Chip select of each bank. 3. Clock Enable: Clock enables 1-0 (see SCASC# & SRASC# for CKE[3-2]#). CKE[3-0]# may be connected to the DRAM modules in any order. Each DRAM module requires 2 clock enables, so CKE[3-0]# may only be used to implement Suspend to RAM with the first 2 modules. Note: These pins are powered by VSUS.
CAS#[7:0] / DQM#[7:0]	AD23, AE24, W26, V22, AF24, AD24, W25, V25	O	**Multifunction Pins** 1. FPG/EDO DRAM: Column Address Strobe of each byte lane. 2. Synchronous DRAM: Data mask of each byte lane. Note: These pins are powered by VSUS.

Signal Name	Pin #	I/O	Signal Description
SRASA#, SRASB#, SRASC# / CKE3#	U25, U26, U22	O	**Row Address Command Indicator.** For support of up to three Synchronous DRAM DIMM slots (these are not copies as each DIMM slot may have separate timing). "A"controls banks 0-1 (module 0), "B"controls banks 2-3 (module 1), and "C"controls banks 4-5 (module 2). See RAS[5-4]# for an explanation of CKE3#.
SCASA#, SCASB#, SCASC# / CKE2#	T26, T22, U24	O	**Column Address Command Indicator.** For support of up to three Synchronous DRAM DIMM slots (these are not copies as each DIMM slot may have separate timing). "A"controls banks 0-1 (module 0), "B"controls banks 2-3 (module 1), and "C"controls banks 4-5 (module 2). See RAS[5- 4]# for an explanation of CKE2#.
SWEA# / MWEA#, SWEB# / MWEB#, SWEC# / MWEC#	W23, W22, Y22	O	**Write Enable Command Indicator.** For support of up to three Synchronous DRAM DIMM slots (these are not copies as each DIMM slot may have separate timing). Multifunction pins, used as MWE# pins for FPG/EDO memory. "A"controls banks 0-1 (module 0), "B"controls banks 2-3 (module 1), and "C"controls banks 4-5 (module 2). Note: These pins are powered by VSUS.

Note: Clocking of the memory subsystem uses memory clock (MCLK); see the clock pin group at the end of the pin descriptions section for descriptions of the clock pins.

Note: Connect all memory interface pins except MD and MECC to the DRAM modules through 22W series resistors (see the Apollo MVP4 Design Guide?for more specific connection details and PCB layout recommendations).

3.3 VIA VT8501 Apollo MVP4 North Bridge-3

PCI Bus Interface

Signal Name	Pin #	I/O	Signal Description
AD[31:0]	(see pinout tables)	IO	**Address/Data Bus.** The standard PCI address and data lines. The address is driven with FRAME# assertion and data is driven or received in following cycles.
CBE[3:0]#	AC5, AD7, AD9,AB10	IO	**Command/Byte Enables.** Commands are driven with FRAME# assertion. Byte enables corresponding to supplied or requested data are driven on following clocks.
PAR	AC8	IO	**Parity.** A single parity bit is provided over AD[31:0] and C/BE[3:0].
FRAME#	AF7	IO	**Frame.** Assertion indicates the address phase of a PCI transfer. Negation indicates that one more data transfer is desired by the cycle initiator. 10KW pullup to VCC3.
IRDY#	AE7	IO	**Initiator Ready.** Asserted when initiator is ready for data transfer. 10KW pullup to VCC3.
TRDY#	AB7	IO	**Target Ready.** Asserted when target is ready for data transfer. 10KW pullup to VCC3.
STOP#	AE8	IO	**Stop.** Asserted by the target to request the master to stop the current transaction. 10KW pullup to VCC3.
DEVSEL#	AC7	IO	**Device Select.** This signal is driven by the MVP4 when a PCI initiator is attempting to access main memory. It is an input when the MVP4 is acting as a PCI initiator. 10KW pullup to VCC3.
LOCK#	AF8	IO	**Lock.** Used to establish, maintain, and release resource lock. 10KW pullup to VCC3.
SERR# / PWRGD	AB8	IO /I	**System Error.** The MVP4 will pulse this signal when it detects a system error condition (10KW pullup to VCC3). May optionally be configured as a PWRGD input (see strapping pin MA11).
PREQ#	AF12	I	**South Bridge Request.** This signal comes from the South Bridge. PREQ# is the South Bridge request for the PCI bus. 10KW pullup to VCC3.
PGNT#	AC12	O	**South Bridge Grant.** This signal driven by the MVP4 to grant PCI access to the South Bridge. 10KW pullup to VCC3.
REQ[3:0]#	AC1, AC3, AD2,AE1	I	**PCI Master Request.** PCI master requests for use of the PCI bus. 2.2KW pullup to VCC5.
GNT[3:0]#	AB5, AC2, AD1,AD3	O	**PCI Master Grant.** Permission is given to the master to use the PCI bus. 2.2KW pullup to VCC3.
REQX#	AB4	I	**High Priority PCI Master Request.** VIA special high priority master request for use of the PCI bus. 4.7KW pullup to VCC3 if not used.
GNTX#	AB3	O	**High Priority PCI Master Grant.** Permission is given to the VIA high priority master to use the PCI bus.
INTA#	Y5	O	**PCI Interrupt Out.** INTA# is an asynchronous active low output used to signal an event that requires handling. It is driven by the integrated graphics controller.

Note: Clocking of the PCI interface is performed with PCLK; see the clock pin group at the end of the pin descriptions section for descriptions of the clock input pins.

Clock / Reset Control

Signal Name	Pin #	I/O	Signal Description
HCLK	AC21	I	**Host Clock.** This pin receives the host CPU clock. This clock is used by all logic in the host CPU domain. It is driven by the external clock synthesizer.
MCLKI	AF22	I	**Memory Clock In.** This clock is used by internal clock logic to maintain the proper phase relationship with MCLKO. It is driven by the external clock synthesizer.
MCLKO	AB21	O	**Memory Clock Out.** Created on-chip from MCLKI and used by the memory controller as a timing reference for creation of all memory timing sequences. It is connected to the external clock chip for use in maintaining proper phase relationships.
PCLK	AB12	I	**PCI Clock.** This clock is used by all on-chip logic in the PCI clock domain. This input must be 33 MHz maximum to comply with PCI specification requirements and must be synchronous with the host CPU clock (HCLK) with an HCLK:PCLK frequency ratio of 2:1 (66MHz CPU clock) or 3:1 (100 MHz CPU clock). The PCI clock needs to be controlled to within 1.5 ?0.5 nsec relative to the host CPU clock (CPU leads).
PCKRUN#	AC13	IO	**PCI Clock Run**. For implementation of PCI bus clock control for low-power PCI bus operation. Refer to the "PCI Mobile Design Guidelines" and "Apollo MVP4 Design Guide" documents for additional information.
XLTI	AA4	I	**Crystal Input.** 14.31818 MHz for the video clock synthesizer reference. Connect to a 14.31818 MHz clock source if a crystal not used. Connect to main ground plane GND with 10pF if using a crystal.

3.3 VIA VT8501 Apollo MVP4 North Bridge-4

Clock / Reset Control

Signal Name	Pin #	I/O	Signal Description
XLTO	AA5	O	**Crystal Output.** 14.31818 MHz for the video clock synthesizer reference. Leave open if a clock source is used instead of a crystal. Connect to main ground plane GND with 10pF if using a crystal.
RESET#	AF13	I	**Reset.** Driven from the South Bridge RESET signal through an inverter. When asserted (low), this signal resets the MVP4 and sets all register bits to the default value. This signal also connects to the PCI bus (South Bridge RESET drives the ISA bus if implemented). The rising edge of this signal is used to sample all power-up strap options (see memory interface MA pins).
PWROK	AE13	I	**Power OK.** Connect to South Bridge and Power Good circuitry.
SUST#	AC22	I	**Suspend Status.** For implementation of the Suspend-to-DRAM feature. Input logic for this pin is powered by VSUS. Connect to the South Bridge SUST# pin or to a 10KW pullup to VSUS if not used.
SUSP	F5	I	**Suspend.** For implementation of the Suspend-to-DRAM feature. Input logic for this pin is powered by VSUS. Connect to South Bridge GPO pin or to a 10KW pullup to VSUS if not used.

Miscellaneous

Signal Name	Pin #	I/O	Signal Description
ENTST#	F4	I	**Test Mode Enable.** 4.7KW pullup to VCC3 for normal operation.
IMIO	N2	O	**IMI Out.** Leave open.
IMIIN	N4	I	**IMI In.** 4.7KW pullup to VCC3.

CRT Interface

Signal Name	Pin #	I/O	Signal Description
RED	C2	A	**Red.** Red analog output to the CRT. Connect 75W load resistor to GNDR (RGB Return) and connect to VGA connector through a series ferrite bead and 10pF capacitors to GNDR on both input and output sides of the bead (see "Apollo MVP4 Design Guide").

Signal Name	Pin #	I/O	Signal Description
GRN	D3	A	**Green.** Green analog output to the CRT. Connect same as RED.
BLUE	D2	A	**Blue.** Blue analog output to the CRT. Connect same as RED.
HSYNC	E2	O	**Horizontal Sync.** Digital horizontal sync output to the CRT. Also used (with VSYNC) to signal power management state information to the CRT per the VESADPMS™ standard. Connect to VGA connector through a series 47W resistor and 120pF capacitor to ground (see "Apollo MVP4 Design Guide").
VSYNC	E1	O	**Vertical Sync.** Digital vertical sync output to the CRT. Also used (with HSYNC) to signal power management state information to the CRT per the VESA™ DPMS ™ standard. Connect to VGA connector through a series 47W resistor and 120pF capacitor to ground (see "Apollo MVP4 Design Guide").
SDA	F2	IO	**DDC Data/Address.** Serial I²C protocol for VESA™ DDC2B signaling to the CRT. Connect this pin to VCC5 through a 4.7KW pullup. Connect to the VGA connector only (pin 12 of the connector). Connect through a ferrite bead and 120pF capacitor to ground (on the output side of the bead). Refer to the "Apollo MVP4 Design Guide" for additional information.
SCL	F3	IO	**DDC Clock.** Serial I²C protocol for VESA™ DDC2B signaling to the CRT. Connect this pin to VCC5 through a 4.7KW pullup. Connect to the VGA connector only (pin 15 of the VGA connector). Connect through a ferrite bead and 120pF capacitor to ground (on the output side of the bead). Refer to the "Apollo MVP4 Design Guide" for additional information.

DFP Interface

Signal Name	Pin #	I/O	Signal Description
PD[23-0]	(see pin list)	O	**Panel Data.** Digital monitor pixel data outputs.
SHFCLK	H5	O	**Shift Clock.** Clock for transferring digital pixel data.
DE	H4	O	**Data Enable.** Indicates valid data on PD[23-0].
LP	G4	O	**Line Pulse.** Digital monitor equivalent of HSYNC.
FLM	G5	O	**First Line Marker.** Digital monitor equivalent of VSYNC.
ENPVDD	F1	O	**Enable Panel VDD Power.**
ENPVEE	G1	O	**Enable Panel VEE Power.**
ENPBLT	G3	O	**Enable Panel Backlight.**

Note: Connect SHFCLK, DE, LP, and FLM to external TMDS transmitters through series 22W resistors. See the "Apollo MVP4 Design Guide" for DFP interface design examples and additional information.

3.3 VIA VT8501 Apollo MVP4 North Bridge-5

TV Input / Video Interface

Signal Name	Pin #	I/O	Signal Description
VIDD[15-0]	(see pin list)	IO	**Video Capture / Playback Data.** Connect to TV decoder if used.
VIDHS	U4	IO	**Video Horizontal Sync.** Connect to TV decoder if used.
VIDVS	U3	IO	**Video Vertical Sync.** Connect to TV decoder if used.
VIDCLK	V3	IO	**Video Clock.** Connect to TV decoder through a series 22W resistor.

Note: Refer to the "Apollo MVP4 Design Guide " for video interface design examples.

TV Output Interface

Signal Name	Pin #	I/O	Signal Description
TVD[7-0]	V2, U5, V1, V5, V4, W5, W2, W1	O	**TV Output Data.** Connect to TV encoder if used.
TVHS	W4	O	**TV Horizontal Sync.** Connect to TV encoder if used.
TVVS	Y3	O	**TV Vertical Sync.** Connect to TV encoder if used.
TVCLK	Y4	O	**TV Clock.** Connect to TV encoder through a series 22W resistor.

Note: Refer to the "Apollo MVP4 Design Guide " for TV interface design examples.

Digital Power and Ground

Signal Name	Pin #	I/O	Signal Description
VCC5	U6	P	**Power** for **Display / Video Interfaces** (5V ¡Ó5%). Power for CRT H/VSYNC, DFP interface, video interface, and TV interface. Used to provide adequate output voltage swing for driving external video devices. Also used to provide 5V input tolerance from those interfaces.
VCC3	C8, C19, F7, F8, F19, F20, G6, G21, H3, H6, H21, H24, L12, L15, M11, M16, R11, R16, T12, T15, W3, W6, W21, W24, Y6, Y21, AA7, AA8, AA19, AA20, AD8, AD19	P	**Power** for **On-Board Interfaces** (2.5V to 3 .3V ¡Ó5%). Power for host CPU / L2 Cache interface, PCI bus interface, and memory interface (except pins listed below under VSUS).
VSUS3	U21, AB19	P	**Suspend Power** (3.3V ¡Ó5%). Power for memory interface signals SRASC#, SCASC#, SWEC#, SWEB#, RAS[5-0]#, CAS[7-0]#, and MECC[7-0] as well as SUSTAT# and SUSCLK. Connect to VCC3 if suspend functions are not implemented.

Signal Name	Pin #	I/O	Signal Description
VSUS2	AA22	P	**Suspend Power** (2.5V ¡Ó5%). Connect to VCCI if suspend functions are not implemented.
VCCI	F9, F18, J6, J21, V6, V21, AA9, AA18	P	**Power** for **On-Chip Internal Logic** (2.5V ¡Ó5%).
VCCD	Y1	P	**Power** for **Video Clock Synthesizer Digital Logic** (2.5V ¡Ó5%). Connect to VCCI through a ferrite bead and decouple to main ground plane GND with 0.001uF and 0.1uF ceramic and 10uF tantalum capacitors (see "Apollo MVP4 Design Guide").
VCCR	D1	P	**Power** for **RAMDAC Video Output Digital Logic** (2.5V ¡Ó5%). Connect to VCCI through a ferrite bead and decouple to main ground plane GND with 0.001uF and 0.1uF ceramic and 10uF tantalum capacitors (see "Apollo MVP4 Design Guide").
GND	A13, A26, C14, D4, D23, E13, E14, F6, F21, L11, L13, L14, L16, M12-M15, N3, N5, N11-N16, N22, N26, P1, P5, P11-P16, P22, R12-R15, T11, T13, T14, T16, AA6, AA21, AB13, AB14, AC4, AC23, AD13, AF14, AF26	P	**Ground.** Connect to primary PCB ground plane.

Commonly Used Prefix / Suffix Letters in Signal Names:

I = Internal Logic	V1 = Video Clock Synthesizer PLL1
M = Memory (SDRAM) Interface	V2 = Video Clock Synthesizer PLL2
H = Host CPU Interface	D = Video Clocks Digital Data Path
P = PCI Bus Interface	R = RAMDAC Digital Data Path
G = AGP Bus Interface (internal in MVP4)	S = RAMDAC Current Source
U (or USB) = USB (Universal Serial Bus)	RGB = Analog Video Out Return
H (or HWM) = Hardware Monitoring	TV = TV Out
SUS = Suspend Power	VID = TV In
A = North Bridge Clock Synthesizer	

3.3 VIA VT8501 Apollo MVP4 North Bridge-6

Clock Power / Ground and Filtering

Signal Name	Pin #	I/O	Signal Description
VCCA	AB16, AC16	P	**Power** for **North Bridge Clock Circuitry** (2.5V ¡Ó 5 %). Connect to VCCI through a ferrite bead and decouple to GNDA with 0.001uF and 0.1uF ceramic and 10uF tantalum capacitors (see "Apollo MVP4 Design Guide").
GNDA	AA17, AB17	P	**Ground** for **North Bridge Clock Circuitry.** Connect to main ground plane GND through a ferrite bead. (see Apollo MVP4 Design Guide").
VCCV1	Y2	P	**Power** for **Video Clock Synthesizer 1 Analog Circuitry** (2.5V ¡Ó 5%). Connect to VCCI through a ferrite bead and decouple to GNDV1 with 0.001uF and 0.1uF ceramic and 10uF tantalum capacitors (see "Apollo MVP4 Design Guide").
GNDV1	AA1	P	**Ground** for **Video Clock Synthesizer 1.** Connect to main ground plane through a ferrite bead.
VLF1	AA3	A	**Low Pass Filter Capacitor** for **Video Clock Synthesizer 1.** Connect to GNDV1 through a 560pF capacitor.
VCCV2	AA2	P	**Power** for **Video Clock Synthesizer 2 Analog Circuitry** (2.5V ¡Ó 5%). Connect to VCCI through a ferrite bead and decouple to GNDV2 with 0.001uF and 0.1uF ceramic and 10uF tantalum capacitors (see "Apollo MVP4 Design Guide").
GNDV2	AB1	P	**Ground** for **Video Clock Synthesizer 2.** Connect to main ground plane through a ferrite bead.
VLF2	AB2	A	**Low Pass Filter Capacitor** for **Video Clock Synthesizer 2.** Connect to GNDV2 through a 560pF capacitor.

RAMDAC Output Power / Ground and Analog Control

Signal Name	Pin #	I/O	Signal Description
VCCS	C1	P	**Power** for **RAMDAC Current Source Circuitry** (2.5V ¡Ó 5 %). Connect to VCCI through a ferrite bead and decouple to GNDS with 0.001uF and 0.1uF ceramic and 10Uf tantalum capacitors (see "Apollo MVP4 Design Guide").
GNDS	B1	P	**Ground** for **RAMDAC Current Source Circuitry.** Connect to main ground plane through a ferrite bead.
COMP	E4	A	**Compensation Capacitor.** RAMDAC analog control. Connect to VCCS using a 0.1 uF capacitor.
IRSET	E3	A	**RAMDAC Current Set Point Resistor.** RAMDAC analog control. Connect to GNDS through a 360W 1% resistor.
GNDRGB	A1	P	**RGB Video Output Return.** Connection point for the RGB load resistors. Also used as a shield for the RGB video output traces to the VGA display connector. Connects to RGB return pins 6, 7, and 8 of the VGA connector. Connect to main ground plane through a ferrite bead. Refer to the"Apollo MVP4 Design Guide" for more specific connection and PCB layout details.

3.4 VIA VT82C686A Super South Bridge-1

PCI Bus Interface

Signal Name	Pin #	I/O	Signal Description
AD[31:0]	(see pin list)	IO	**Address/Data Bus.** The standard PCI address and data lines. The address is driven with FRAME# assertion and data is driven or received in following cycles.
C/BE[3:0]#	C19, F17, G20, J19	IO	**Command/Byte Enable.** The command is driven with FRAME# assertion. Byte enables corresponding to supplied or requested data are driven on following clocks.
FRAME#	F18	IO	**Frame.** Assertion indicates the address phase of a PCI transfer. Negation indicates that one more data transfer is desired by the cycle initiator.
IRDY#	F19	IO	**Initiator Ready.** Asserted when the initiator is ready for data transfer.
TRDY#	F20	IO	**Target Ready.** Asserted when the target is ready for data transfer.
STOP#	G17	IO	**Stop.** Asserted by the target to request the master to stop the current transaction.
DEVSEL#	G16	IO	**Device Select.** The VT82C686A asserts this signal to claim PCI transactions through positive or subtractive decoding. As an input, DEVSEL# indicates the response to a VT82C686A-initiated transaction and is also sampled when decoding whether to subtractively decode the cycle.
PAR	G19	IO	**Parity.** A single parity bit is provided over AD[31:0] and C/BE[3:0]#.
SERR#	G18	I	**System Error.** SERR# can be pulsed active by any PCI device that detects a system error condition. Upon sampling SERR# active, the VT82C686A can be programmed to generate an NMI to the CPU.
IDSEL	C20	I	**Initialization Device Select.** IDSEL is used as a chip select during configuration read and write cycles. Connect this pin to AD18 using a 100 W resistor.
PIRQA-D#	A16, D17, C17, B17	I	**PCI Interrupt Request**. These pins are typically connected to the PCI bus INTA#-INTD# pins as follows: PIRQA# PIRQB# PIRQC# PIRQD# PCI Slot 1 INTA# INTB# INTC# INTD# PCI Slot 2 INTB# INTC# INTD# INTA# PCI Slot 3 INTC# INTD# INTA# INTB# PCI Slot 4 INTD# INTA# INTB# INTC#
PREQ#	L18	O	**PCI Request.** This signal goes to the North Bridge to request the PCI bus.
PGNT#	L19	I	**PCI Grant.** This signal is driven by the North Bridge to grant PCI access to the VT82C686A.

Signal Name	Pin #	I/O	Signal Description
PCLK	E16	I	**PCI Clock.** PCLK provides timing for all transactions on the PCI Bus.
PCKRUN#	W12	IO	**PCI Bus Clock Run.** This signal indicates whether the PCI clock is or will be stopped (high) or running (low). The VT82C686A drives this signal low when the PCI clock is running (default on reset) and releases it when it stops the PCI clock. External devices may assert this signal low to request that the PCI clock be restarted or prevent it from stopping. Connect this pin to ground using a 100 £ [resistor if the function is not used. Refer to the "PCI Mobile Design Guide" and the VIA "Apollo MVP4 Design Guide" for more details.

CPU Interface

Signal Name	Pin #	I/O	Signal Description
CPURST	V8	OD	**CPU Reset.** The VT82C686A asserts CPURST to reset the CPU during power-up.
INTR	W8	OD	**CPU Interrupt.** INTR is driven by the VT82C686A to signal the CPU that an interrupt request is pending and needs service.
NMI	U7	OD	**Non-Maskable Interrupt.** NMI is used to force a non-maskable interrupt to the CPU. The VT82C686A generates an NMI when either SERR# or IOCHK# is asserted.
INIT	T6	OD	**Initialization.** The VT82C686A asserts INIT if it detects a shut-down special cycle on the PCI bus or if a soft reset is initiated by the register.
STPCLK#	W7	OD	**Stop Clock.** STPCLK# is asserted by the VT82C686A to the CPU to throttle the processor clock.
SMI#	U6	OD	**System Management Interrupt.** SMI# is asserted by the VT82C686A to the CPU in response to different Power-Management events.
FERR#	V7	I	**Numerical Coprocessor Error.** This signal is tied to the coprocessor error signal on the CPU. Internally generates interrupt 13 if active.
IGNNE#	Y8	OD	**Ignore Numeric Error.** This pin is connected to the "gnore error" pin on the CPU.
SLP# / GPO7	T7	OD	**Sleep** (Rx75[7] = 0). Used to put the CPU to sleep. Used with slot-1 CPUs only. Not currently used with socket-7 CPUs.
A20M#	Y7	OD	**A20 Mask.** Connect to A20 mask input of the CPU to control address bit-20 generation. Logical combination of the A20GATE input (from internal or external keyboard controller) and Port 92 bit-1 (Fast_A20).

Note: Connect each of the above signals to 4.7K W pullup resistors to VCC3

3.4 VIA VT82C686A Super South Bridge-2

Advanced Programmable Interrupt Controller (APIC) Interface

Signal Name	Pin #	I/O	Signal Description
APICREQ# / GPI3 / LID	U10	I / I / I	**APIC Request.** Rx74[7] = 1. Asserted by external APIC synchronous to PCLK prior to sending an interrupt over the APIC serial bus. This signals the VT82C686A to flush its internal buffers.
APICACK# / GPO1 / SUSA#	V9	O / O / O	**APIC Acknowledge.** Rx74[7] = 1. Asserted by the VT82C686A to indicate that its internal buffers have been flushed (in response to APICREQ#). This indicates to the external APIC that the VT82C686A's internal buffers have been flushed and that it is OK for the APIC to send its interrupt.
APICCS# / GPO2 / SUSB#	W9	O / O / O	**APIC Chip Select.** Rx74[7] = 1. The VT82C686A drives this signal active to select an external APIC (if used). This occurs if the external APIC is enabled and a PCI cycle is detected within the programmed APIC address range.
SCIOUT# / GPO13 / SOE# **(CD/CE)**	U5	O / O / O	**SCI Out.** Used to route the internally generated SCI and SMBus interrupts out of the South Bridge for connection to an external APIC (if used). Defined as SCI Out if function 0 Rx74[7] = 1 (APIC Enabled).
SCIOUT# / GPIOD / GPI11 / GPO11 / MCCS# **(CF)**	U8	O / IO / I / O / O	**SCI Out.** Used to route the internally generated SCI and SMBus interrupts out of the South Bridge for connection to an external APIC (if used). Defined as SCI Out if function 0 Rx74[7] = 1 (APIC Enabled).

Universal Serial Bus Interface

Signal Name	Pin #	I/O	Signal Description
USBP0+	A3	IO	**USB Port 0 Data +**
USBP0-	B3	IO	**USB Port 0 Data -**
USBP1+	C4	IO	**USB Port 1 Data +**
USBP1-	D4	IO	**USB Port 1 Data -**
USBP2+	A4	IO	**USB Port 2 Data +**
USBP2-	B4	IO	**USB Port 2 Data -**
USBP3+	B5	IO	**USB Port 3 Data +**
USBP3-	E6	IO	**USB Port 3 Data -**
USBCLK	C3	I	**USB Clock.** 48MHz clock input for the USB interface
USBOC0#/ GPI13 / GPO25/DACK2#/ FDCIRQ	G5	I / I / O O / I	**USB Port 0 Over Current Detect.** Port 0 is disabled if low.
USBOC1# / GPI12 / GPO24/DRQ2/ DCDRQ/ SERIRQ	H3	I / I / O I / I / I	**USB Port 1 Over Current Detect.** Port 1 is disabled if this input is low. Direct inputs are provided for overcurrent protection for ports 0 and 1 which may be used if the alternate functions of these two pins are not required. If overcurrent protection is desired on all four ports (or it is desired to use the alternate functions of these two pins), an external buffer may be used to drive the state of USBOC[3-0]# onto SD[3-0] during ISA bus refresh cycles (i.e., while ISA bus RFSH# is low, so that RFSH# may be used as the buffer enable).
USBOC0# (SD2 & RFSH#)	(W2)	I	**USB Port 0 Over Current Detect**
USBOC1# (SD1 & RFSH#)	(Y2)	I	**USB Port 1 Over Current Detect**
USBOC2# (SD0 & RFSH#)	(Y1)	I	**USB Port 2 Over Current Detect**
USBOC3# (SD3 & RFSH#)	(Y3)	I	**USB Port 3 Over Current Detect**
USBIRQA / DACK6#	M3	O	**USB Interrupt Request A.** Output of internal block.
USBIRQB / DACK7#	N2	O	**USB Interrupt Request B.** Output of internal block.

System Management Bus (SMB) Interface (I 2 C Bus)

Signal Name	Pin #	I/O	Signal Description
SMBCLK	U9	IO	**SMB / I 2 C Clock.**
SMBDATA	T9	IO	**SMB / I 2 C Data.**
SMBALRT# / GPI6	W10	I	**SMB Alert.** (System Management Bus I/O space Rx08[3] = 1) When the chip is enabled to allow it, assertion generates an IRQ or SMI interrupt or a power management resume event. The same pin is used as General Purpose Input 6 whose value is reflected in Rx48[6] of function 4 I/O space

3.4 VIA VT82C686A Super South Bridge-3

UltraDMA-33 / 66 Enhanced IDE Interface

Signal Name	Pin #	I/O	Signal Description
PDRDY / PDDMARDY / PDSTROBE	N16	I	EIDE Mode: **Primary I/O Channel Ready.** Device ready indicator UltraDMA Mode: **Primary Device DMA Ready**. Output flow control. The device may assert DDMARDY to pause output transfers **Primary Device Strobe**. Input data strobe (both edges). The device may stop DSTROBE to pause input data transfers
SDRDY / SDDMARDY / SDSTROBE	V20	I	EIDE Mode: **Secondary I/O Channel Ready.** Device ready indicator UltraDMA Mode: **Secondary Device DMA Ready**.Output flow control. The device may assert DDMARDY to pause output transfers **Secondary Device Strobe**. Input data strobe (both edges). The device may stop DSTROBE to pause input data transfers
PDIOR / PHDMARDY / PHSTROBE	N17	O	EIDE Mode: **Primary Device I/O Read.** Device read strobe UltraDMA Mode: **Primary Host DMA Ready**. Primary channel input flow control. The host may assert HDMARDY to pause input transfers **Primary Host Strobe**. Output data strobe (both edges). The host may stop HSTROBE to pause output data transfers
SDIOR / SHDMARDY / SHSTROBE	W19	O	EIDE Mode: **Secondary Device I/O Read.** Device read strobe UltraDMA Mode: **Secondary Host DMA Ready**. Input flow control. The host may assert HDMARDY to pause input transfers **Host Strobe B**. Output strobe (both edges). The host may stop HSTROBE to pause output data transfers
PDIOW# / PSTOP	N18	O	EIDE Mode: **Primary Device I/O Write.** Device write strobe UltraDMA Mode: **Primary Stop**. Stop transfer: Asserted by the host prior to initiation of an UltraDMA burst; negated by the host before data is transferred in an UltraDMA burst. Assertion of STOP by the host during or after data transfer in UltraDMA mode signals the termination of the burst.
SDIOW# / SSTOP	W20	O	EIDE Mode: **Secondary Device I/O Write.** Device write strobe UltraDMA Mode: **Secondary Stop**. Stop transfer: Asserted by the host prior to initiation of an UltraDMA burst; negated by the host before data is transferred in an UltraDMA burst. Assertion of STOP by the host during or after data transfer in UltraDMA mode signals the termination of the burst.

UltraDMA-33 / 66 Enhanced IDE Interface

Signal Name	Pin #	I/O	Signal Description
PDDRQ	N19	I	**Primary Device DMA Request.** Primary channel DMA request
SDDRQ	Y20	I	**Secondary Device DMA Request.** Secondary channel DMA request
PDDACK#	M20	O	**Primary Device DMA Acknowledge.** Primary channel DMA acknowledge
SDDACK#	V19	O	**Secondary Device DMA Acknowledge.** Secondary channel DMA acknowledge

UltraDMA-33 / 66 Enhanced IDE Interface (continued)

Signal Name	Pin #	I/O	Signal Description
PDCS1#	L20	O	**Primary Master Chip Select.** This signal corresponds to CS1FX# on the primary IDE connector.
PDCS3#	M16	O	**Primary Slave Chip Select.** This signal corresponds to CS3FX# on the primary IDE connector.
SDCS1#	U17	O	**Secondary Master Chip Select.** This signal corresponds to CS17X# on the secondary IDE connector.
SDCS3#	U18	O	**Secondary Slave Chip Select.** This signal corresponds to CS37X# on the secondary IDE connector.
PDA[2-0]	M18, M19,M17	O	**Primary Disk Address.** PDA[2:0] are used to indicate which byte in either the ATA command block or control block is being accessed.
SDA[2-0]	U20, V18,U19	O	**Secondary Disk Address.** SDA[2:0] are used to indicate which byte in either the ATA command block or control block is being accessed.
PDD[15-0]	N20, P17,P19, R16,R18, R20, T17, T19,T20, T18,T16, R19, R17, P20,P18, P16	IO	**Primary Disk Data**
SDD[15-0] / SA[15-0]	P5, R1-R5, T1-T4, U1-U3, V1, V2, W1	IO	**Secondary Disk Data** muxed with ISA Bus Address (Audio Enabled) **ISA Bus Address only** (Audio Disabled / Dedicated Secondary IDE Data) Note: Audio is enabled by strapping the SPKR pin high with 4.7K ohms and disabled by strapping the SPKR pin low with 4.7K ohms.

3.4 VIA VT82C686A Super South Bridge-4

UltraDMA-33 / 66 Enhanced IDE Interface (continued)

Signal Name	Pin #	I/O	Signal Description
			Secondary Disk Data (SPKR strap = 0) **or AC-Link/Game Ports** (SPKR strap = 1)
SDD[15] / **MSI**,	Y19,	IO / I	**Secondary Disk Data 15 / Midi Serial In**
SDD[14] / **MSO**,	Y18,	IO / O	**Secondary Disk Data 14 / Midi Serial Out**
SDD[13] / **JBB1** / PDRQB,	W17,	IO / I	**Secondary Disk Data 13 / Game Port Joystick B Button 1**
SDD[12] / **JBB2** / PGNTB,	U16,	IO / I	**Secondary Disk Data 12 / Game Port Joystick B Button 2**
SDD[11] / **JAB1** / PDRQA,	W16,	IO / I	**Secondary Disk Data 11 / Game Port Joystick A Button 1**
SDD[10] / **JAB2** / PGNTA,	T15,	IO / I	**Secondary Disk Data 10 / Game Port Joystick A Button 2**
SDD[9] / **JAX** / GPO23,	V15,	IO / I	**Secondary Disk Data 9 / Game Port Joystick A X-axis**
SDD[8] / **JAY** / GPO22,	Y15,	IO / I	**Secondary Disk Data 8 / Game Port Joystick A Y-axis**
SDD[7] / **JBX** / GPI23,	U14,	I O / I	**Secondary Disk Data 7 / Game Port Joystick B X-axis**
SDD[6] / **JBY** / GPI22,	W15,	IO / I	**Secondary Disk Data 6 / Game Port Joystick B Y-axis**
SDD[5] / **ACRST**,	U15,	IO / O	**Secondary Disk Data 5 / AC97 Reset**
SDD[4] / **SDOUT**,	Y16,	IO / O	**Secondary Disk Data 4 / AC97 Serial Data Out**
SDD[3] / **SYNC**,	V16,	IO / O	**Secondary Disk Data 3 / AC97 Sync**
SDD[2] / **SDIN2**,	Y17,	IO / I	**Secondary Disk Data 2 / AC97 Serial Data In 2**
SDD[1] / **SDIN**,	V17,	IO / I	**Secondary Disk Data 1 / AC97 Serial Data In**
SDD[0] / **BITCLK**	W18	IO / I	**Secondary Disk Data 0 / AC97 Bit Clock**
Signal Name	**Pin #**	**I/O**	**Signal Description**
IDEIRQA / DACK0#	L2	O	**IDE Interrupt Request A.** Output of internal block.
IDEIRQB / DACK1#	E1	O	**IDE Interrupt Request B.** Output of internal block.

MIDI Interface

Signal Name	Pin #	I/O	Signal Description
MSI / SDD[15]	Y19	I / IO	**MIDI Serial In** / Secondary Disk Data 15 (SPKR strap = 1)
MSO / SDD[14]	Y18	O / IO	**MIDI Serial Out** / Secondary Disk Data 14 (SPKR strap = 1)

AC97 Audio / Modem Interface

Signal Name	Pin #	I/O	Signal Description
ACRST / SDD[5]	U15	O / IO	**AC97 Reset** / Secondary Disk Data 5 (SPKR strap = 1)
SDOUT/ SDD[4]	Y16	O / IO	**AC97 Serial Data Out** / Secondary Disk Data 4 (SPKR strap = 1)
SYNC / SDD[3]	V16	O / IO	**AC97 Sync** / Secondary Disk Data 3 (SPKR strap = 1)
SDIN2 / SDD[2]	Y17	I / IO	**AC97 Serial Data In 2** / Secondary Disk Data 2 (SPKR strap = 1)
SDIN / SDD[1]	V17	I / IO	**AC97 Serial Data In** / Secondary Disk Data 1 (SPKR strap = 1)
BITCLK / SDD[0]	W18	I / IO	**AC97 Bit Clock** / Secondary Disk Data 0 (SPKR strap = 1)
AC97IRQ / DACK3#	D2	O	**AC97 Interrupt Request.** Output of internal block.
MC97IRQB / DACK5#	L4	O	**MC97 Interrupt Request.** Output of internal block.

Game Port Interface

Signal Name	Pin #	I/O	Signal Description
JAB1/ SDD[11]/ PDRQA	W16	I / IO / I	**Joystick A Button 1** / Secondary Disk Data 11 (SPKR strap = 1)
JAB2/ SDD[10]/ GNTA	T15	I / IO / O	**Joystick A Button 2** / Secondary Disk Data 10 (SPKR strap = 1)
JBB1/ SDD[13]/PDRQB	W17	I / IO / I	**Joystick B Button 1** / Secondary Disk Data 13 (SPKR strap = 1)
JBB2/ SDD[12]/ PGNTB	U16	I / IO / O	**Joystick B Button 2** / Secondary Disk Data 12 (SPKR strap = 1)
JAX/ SDD[9]/ GPO23	V15	I / IO / O	**Joystick A X-axis** / Secondary Disk Data 9 (SPKR strap = 1)
JAY/ SDD[8]/ GPO22	Y15	I / IO / O	**Joystick A Y-axis** / Secondary Disk Data 8 (SPKR strap = 1)
JBX/ SDD[7]/ GPI23	U14	I / IO / I	**Joystick B X-axis** / Secondary Disk Data 7 (SPKR strap = 1)
JBY/ SDD[6]/ GPI22	W15	I / IO / I	**Joystick B Y-axis** / Secondary Disk Data 6 (SPKR strap = 1)

5133S M/B Maintenance

3.4 VIA VT82C686A Super South Bridge-5

PDRQ / PGNT Interface

Signal Name	Pin #	I/O	Signal Description
PDRQA / SDD[11] JAB1	W16	I / IO / I	
PGNTA/ SDD[10]/ JAB2	T15	O / IO / I	
PDRQB/ SDD[13]/ JBB1	W17	I / IO / I	
PGNTB/ SDD[12]/ JBB2	U16	O / IO / I	

Floppy Disk Interface

Signal Name	Pin #	I/O	Signal Description
DRVDEN0	D9	OD	**Drive Density Select 0.**
DRVDEN1	D6	OD	**Drive Density Select 1.**
MTR0#	E9	OD	**Motor Control 0.** Select motor on drive 0.
MTR1#	C8	OD	**Motor Control 1.** Select motor on drive 1
DS0#	B8	OD	**Drive Select 0.** Select drive 0.
DS1#	A8	OD	**Drive Select 1.** Select drive 1
DIR#	D8	OD	**Direction.** Direction of head movement (0 = inward motion, 1 = outward motion)
STEP#	E8	OD	**Step.** Low pulse for each track-to-track movement of the head.
INDEX#	D7	I	**Index.** Sense to detect that the head is positioned over the beginning of a track
HDSEL#	C7	OD	**Head Select.** Selects the side for R/W operations (0 = side 1, 1 = side 0)
TRK00#	E7	I	**Track 0.** Sense to detect that the head is positioned over track 0.
RDATA#	B6	I	**Read Data.** Raw serial bit stream from the drive for read operatrions.
WDATA#	A7	OD	**Write Data.** Encoded data to the drive for write operations.

Floppy Disk Interface

Signal Name	Pin #	I/O	Signal Description
WGATE#	B7	OD	**Write Gate.** Signal to the drive to enable current flow in the write head.
DSKCHG#	C6	I	**Disk Change.** Sense that the drive door is open or the diskette has been changed since the last drive selection.
WRTPRT#	A6	I	**Write Protect.** Sense for detection that the diskette is write protected (causes write commands to be ignored)
FDCIRQ / DACK2#	G5	I	**FDC Interrupt Request.** Rx75[3] = 1.
FDCDRQ / DRQ2	H3	I	**FDC DMA Request.** Rx75[3] = 1.

Parallel Port Interface

Signal Name	Pin #	I/O	Signal Description
PINIT# / DIR#	C15	IO / O	**Initialize.** Initialize printer. Output in standard mode, I/O in ECP/EPP mode.
STROBE# / nc	D16	IO / -	**Strobe.** Output used to strobe data into the printer. I/O in ECP/EPP mode.
AUTOFD# / DRVEN0	C16	IO / O	**Auto Feed.** Output used to cause the printer to automatically feed one line after each line is printed. I/O pin in ECP/EPP mode.
SLCTIN# / STEP#	E15	IO / O	**Select In.** Output used to select the printer. I/O pin in ECP/EPP mode.
SLCT / WGATE#	E13	I / O	**Select.** Status output from the printer. High indicates that it is powered on.
ACK# / DS1#	B13	I / O	**Acknowledge.** Status output from the printer. Low indicates that it has received the data and is ready to accept new data
ERROR# / HDSEL#	A15	I / O	**Error.** Status output from the printer. Low indicates an error condition in the printer.
BUSY / MTR1#	C13	I / O	**Busy.** Status output from the printer. High indicates not ready to accept data.
PE / WDATA#	D13	I / O	**Paper End.** Status output from the printer. High indicates that it is out of paper.
PD7 / nc, **PD6** / nc, **PD5** / nc, **PD4** / DSKCHG#, **PD3** / RDATA#, **PD2** / WRTPRT#, **PD1** / TRK00#, **PD0** / INDEX#	A13, E14, D14, C14, B14, A14, D15, B15	IO / - IO/ - IO/ - IO/ I IO / I IO / I IO / I IO / I	**Parallel Port Data.**

3.4 VIA VT82C686A Super South Bridge-6

Serial Ports and Infrared Interface

Signal Name	Pin #	I/O	Signal Description
TXD1	A11	O	**Transmit Data 1.** Serial port 1 transmit data out.
TXD2	D10	O	**Transmit Data 2.** Serial port 2 transmit data out.
IRTX / GPO14	E12	O	**Infrared Transmit.** IR transmit data out (Rx76[5] = 0) selectable from serial port 1, 2, or 3. General Purpose Output 14 if Rx76[5] = 1
RXD1	B12	I	**Receive Data 1.** Serial port 1 receive data in.
RXD2	B10	I	**Receive Data 2.** Serial port 2 receive data in.
IRRX / GPO15	D12	IO	**Infrared Receive.** IR receive data in (Rx76[5] = 0) selectable to serial port 1, 2, or 3. General Purpose Output 15 if Rx76[5] = 1
RTS1#	B11	O	**Request To Send 1.** Indicator that serial output port 1 is ready to transmit data. Typically used as hardware handshake with CTS1# for low level flow control. Designed for direct input to external RS-232C driver.
RTS2##	E10	O	**Request To Send 2.** Indicator that serial output port 2 is ready to transmit data. Typically used as hardware handshake with CTS2# for low level flow control. Designed for direct input to external RS-232C driver.
CTS1#	C11	I	**Clear To Send 1.** Indicator to serial port 1 that external communications device is ready to receive data. Typically used as hardware handshake with RTS1# for low level flow control. Designed for input from external RS-232C receiver.
CTS2#	A9	I	**Clear To Send 2.** Indicator to serial port 2 that external communications device is ready to receive data. Typically used as hardware handshake with RTS2# for low level flow control. Designed for input from external RS-232C receiver.
DTR1#	D11	O	**Data Terminal Ready 1.** Serial port 1 indicator that port is powered, initialized, and ready. Typically used as hardware handshake with DSR1# for overall readiness to communicate. Designed for direct input to external RS-232C driver.
DTR2#	B9	O	**Data Terminal Ready 2.** Serial port 2 indicator that port is powered, initialized, and ready. Typically used as hardware handshake with DSR2# for overall readiness to communicate. Designed for direct input to external RS-232C driver.

Serial Ports and Infrared Interface

Signal Name	Pin #	I/O	Signal Description
DSR1#	C12	I	**Data Set Ready 1.** Indicator to serial port 1 that external serial communications device is powered, initialized, and ready. Typically used as hardware handshake with DTR1# for overall readiness to communicate. Designed for direct input from external RS-232C receiver.
DSR2#	C10	I	**Data Set Ready 2.** Indicator to serial port 2 that external serial communications device is powered, initialized, and ready. Typically used as hardware handshake with DTR2# for overall readiness to communicate. Designed for direct input from external RS-232C receiver.
DCD1#	A12	I	**Data Carrier Detect 1.** Indicator to serial port 1 that external modem is detecting a carrier signal (i.e., a communications channel is currently open). In direct connect environments, this input will typically be driven by DTR1# as part of the DTR/DSR handshake. Designed for direct input from external RS-232C receiver.
DCD2#	A10	I	**Data Carrier Detect 2.** Indicator to serial port 2 that external modem is detecting a carrier signal (i.e., a communications channel is currently open). In direct connect environments, this input will typically be driven by DTR2# as part of the DTR/DSR handshake. Designed for direct input from external RS-232C receiver.
RI1#	E11	I	**Ring Indicator 1.** Indicator to serial port 1 that external modem is detecting a ring condition. Used by software to initiate operations to answer and open the communications channel. Designed for direct input from external RS-232C receiver (whose input is typically not connected in direct connect environments).
RI2#	C9	I	**Ring Indicator 2.** Indicator to serial port 2 that external modem is detecting a ring condition. Used by software to initiate operations to answer and open the communications channel. Designed for direct input from external RS-232C receiver (whose input is typically not connected in direct connect environments).

3.4 VIA VT82C686A Super South Bridge-7

ISA Bus Interface

Signal Name	Pin #	I/O	Signal Description
SA[19:16], **SA[15-0]** / SDD[15-0]	K1, K2, P3, P4, P5, R1, R2, R3, R4, R5, T1, T2, T3, T4, U1, U2, U3, V1, V2, W1	IO IO	**System Address Bus**. SA[19-16] are connected to ISA bus SA[19-16] directly. SA[19-17] are also connected to LA[19-17] of the ISA bus. If the audio interface is disabled (SPKR pin strapped low), SA[15-0] are connected directly to ISA address bus pins SA[15-0] (the audio interface pins are used for the IDE secondary data bus). If the audio interface is enabled (SPKR pin strapped high), SA[15-0] are multiplexed with the IDE Secondary Data Bus. In this case, SA[15-0] may be connected to both SDD[15-0] and ISA bus SA[15-0]. However, if ISA address bus loading is a concern, 74F245 transceivers may be used to externally drive ISA address bus pins SA[15-0]. In this case, these pins would connect directly to the IDE secondary data bus and to the transceiver "A" pins and the ISA address bus would connect to the transceiver "B" pins. SOE# would be used to control the transceiver output enables and the ISA bus MASTER# signal would drive the transceiver direction controls.
LA[23:20]	J2, J3, J4, J5	IO	**System "Latched" Address Bus**: The LA[23:20] address lines are bi-directional. These address lines allow accesses to physical memory on the ISA bus up to 16Mbytes. LA[19-17] on the ISA bus are connected to SA[19-17] (see notes above).
SD[15:0]	P2, P1, N5, N3, N1, M4, M2, L5, W4, Y4, V3, W3, Y3, W2, Y2, Y1	IO	**System Data.** SD[15:0] provide the data path for devices residing on the ISA bus. X-Bus data signals XD[7:0] may be derived if needed from SD[7:0] using an external 74F245-type transceiver (see the XDIR pin description for transceiver connection details). SD7:4 are strap options for keyboard inputs 6:3 (see Function 0 Rx5A)
SBHE#	F2	IO	**System Byte High Enable.** SBHE# indicates, when asserted, that a byte is being transferred on the upper byte (SD[15:8]) of the data bus. SBHE# is negated during refresh cycles.
IOR#	D1	IO	**I/O Read.** IOR# is the command to an ISA I/O slave device that the slave may drive data on to the ISA data bus.

ISA Bus Interface

Signal Name	Pin #	I/O	Signal Description
IOW#	C2	IO	**I/O Write.** IOW# is the command to an ISA I/O slave device that the slave may latch data from the ISA data bus.
MEMR#	U4	IO	**Memory Read.** MEMR# is the command to a memory slave that it may drive data onto the ISA data bus.
MEMW#	V4	IO	**Memory Write.** MEMW# is the command to a memory slave that it may latch data from the ISA data bus.
SMEMR#	A1	O	**Standard Memory Read.** SMEMR# is the command to a memory slave, under 1MB, which indicates that it may drive data onto the ISA data bus.
SMEMW#	B1	O	**Standard Memory Write.** SMEMW# is the command to a memory slave, under 1MB, which indicates that it may latch data from the ISA data bus.
BALE	H2	O	**Bus Address Latch Enable.** BALE is an active high signal asserted by the VT82C686A to indicate that the address (SA[19:0], LA[23:17] and the SBHE# signal) is valid
IOCS16#	F3	I	**16-Bit I/O Chip Select.** This signal is driven by I/O devices on the ISA Bus to indicate that they support 16-bit I/O bus cycles.
MCS16#	F1	I	**Memory Chip Select 16.** ISA slaves that are 16-bit memory devices drive this line low to indicate they support 16-bit memory bus cycles.
IOCHCK# / GPI0	F4	I	**I/O Channel Check** (Rx74[0] = 1). When this signal is asserted, it indicates that a parity or an uncorrectable error has occurred for an I/O or memory device on the ISA Bus. The same pin may optionally be used as General Purpose Input 0.
IOCHRDY	A2	I	**I/O Channel Ready** (Rx74[0] = 1). This signal is normally high. Devices on the ISA Bus assert IOCHRDY low to indicate that additional time (wait states) is required to complete the cycle.
RFSH#	E3	IO	**Refresh.** As an output RFSH# indicates when a refresh cycle is in progress. RFSH# is also driven by 16-bit ISA Bus masters to indicate a refresh cycle.
AEN	B2	O	**Address Enable.** AEN is asserted during DMA cycles to prevent I/O slaves from misinterpreting DMA cycles as valid I/O cycles.
IRQ1 / MSCK	D5	I / IO	**Interrupt Request 1** (Rx5A[1] = 0)
IRQ3	G4	I	**Interrupt Request 3.**
IRQ4	G3	I	**Interrupt Request 4.**
IRQ5	G2	I	**Interrupt Request 5.**

3.4 VIA VT82C686A Super South Bridge-8

ISA Bus Interface

Signal Name	Pin #	I/O	Signal Description
IRQ6 / GPI4 / SLPBTN#	G1	I / I / I	**Interrupt Request 6.**
IRQ7	F5	I	**Interrupt Request 7.**
IRQ8# / GPI1	W11	I / I	**Interrupt Request 8** from ext RTC if int RTC disabled (Rx5A[2] = 0)
IRQ9	H4	I	**Interrupt Request 9.**
IRQ10	K3	I	**Interrupt Request 10.**
IRQ11	K4	I	**Interrupt Request 11.**
IRQ12 / MSDT	C5	I / IO	**Interrupt Request 12.** (Rx5A[1] = 0)
IRQ14	L1	I	**Interrupt Request 14.**
IRQ15	K5	I	**Interrupt Request 15.**
DRQ7 / GPI21, **DRQ6** / GPI20, **DRQ5** / GPI19, **DRQ3** / GPI18, **DRQ2** / FDCDRQ / SERIRQ / GPI12 / GPO24 / USBOC1#, **DRQ1** / GPI17, **DRQ0** / GPI16	N4, M5, M1, D3, H3, E2, L3	I / I I / I I / I I / I I / I / I I / O / I I / I I / I	**DMA Request.** Used to request DMA services from the internal DMA controller. DRQ2: Rx68[3] = 0 & Rx75[3] = 0 & Rx75[1] = 0 See also Function 0 Rx77[7]
DACK7# / USBIRQB / GPO21, **DACK6#** / USBIRQA / GPO20, **DACK5#** / MC97IRQ / GPO19 / SERIRQ, **DACK3#** / AC97IRQ / GPO18, **DACK2#** / USBOC0# / GPO25 / GPI13 / FDCIRQ, **DACK1#** / IDEIRQB / GPO17, **DACK0#** / IDEIRQA / GPO16	N2, M3, L4, D2, G5, E1, L2	O / O / O O / O / O O / O / O / I O / O / O O / I / O / I / I O / O / O O / O / O	**Acknowledge.** Used by the internal DMA controller to indicate that a request for DMA service has been granted. DACK5#: Rx68[3] = 0 DACK2#: Rx68[3] = 0 & Rx75[3] = 0 & Rx75[2] = 0 See also Function 0 Rx77[7]
TC	H1	O	**Terminal Count.** Asserted to DMA slaves as a terminal count indicator.
SPKR / strap	V5	O / I	**Speaker Drive.** Output of internal timer/counter 2. Also functions as a **strap input** sampled at reset to determine the function of the Audio /Game interface pins: 0=Disable Audio / Game interface (pins used for IDE Secondary Data Bus SDD[15-0] and ISA SA[15-0] pins used for ISA bus only), 1=Enable Audio / Game interface (pins used for Audio/Game functions and SDD[15-0] are multiplexed with ISA SA[15-0]).

ISA Bus Interface

Signal Name	Pin #	I/O	Signal Description
SOE# (default pin function) / GPO13/ SCIOUT# **(CD/CE only)**/ MCCS# **(CF only)**	U5	O / O / O / O	**ISA Address (SA) Output Enable.** Asserted low when ISA address (SA) is valid (deasserted when SDD is valid) when SA and SDD are multiplexed on SA pins 15-0 (i.e., when SPKR is strapped low to enable the audio interface pins). SOE# is tied directly to the output enable of 74F245 transceivers that buffer IDE Secondary Bus data and ISA-address (see SA pins for more information).

Serial IRQ

Signal Name	Pin #	I/O	Signal Description
SERIRQ / DRQ2/ GPI12 / GPO24/ FDCDRQ / USBOC1#	H3	I	**Serial IRQ** (Rx68[3] = 1 and Rx74[6] = 0)
SERIRQ / DACK5#/ GPO19 / MC97IRQ	L4	I	**Serial IRQ** (Rx68[3] = 1 and Rx74[6] = 1)

Internal Keyboard Controller

Signal Name	Pin #	I/O	Signal Description
MSCK / IRQ1	D5	IO / I	**MultiFunction Pin** (Internal mouse controller enabled by Rx5A[1]) Rx5A[1]=1 **Mouse Clock.** From internal mouse controller. Rx5A[1]=0 **Interrupt Request 1**. Interrupt input 1.
MSDT / IRQ12	C5	IO / I	**MultiFunction Pin** (Internal mouse controller enabled by Rx5A[1]) Rx5A[1]=1 **Mouse Data.** From internal mouse controller. Rx5A[1]=0 **Interrupt Request 12**. Interrupt input 12.
KBCK / A20GATE	E5	IO / I	**MultiFunction Pin** (Internal keyboard controller enabled by Rx5A[0]) Rx5A[0]=1 **Keyboard Clock.** From internal keyboard controller Rx5A[0]=0 **Gate A20.** Input from external keyboard controller.
KBDT / KBRC	A5	IO / I	**MultiFunction Pin** (Internal keyboard controller enabled by Rx5A[0]) Rx5A[0]=1 **Keyboard Data.** From internal keyboard controller. Rx5A[0]=0 **Keyboard Reset.** From external keyboard controller (KBC) for CPURST# generation
KBCS# / ROMCS# / **strap**	C1	O / O / I	**Keyboard Chip Select** (Rx5A[0]=0). To external keyboard controller chip. **Power-Up Configuration Strap (Sampled At Reset)**: 4.7K to GND = Socket-7, 4.7K to VCC3 = Socket-370 / Slot-1

3.4 VIA VT82C686A Super South Bridge-9

Internal Keyboard Controller

Signal Name	Pin #	I/O	Signal Description
KBIN[6-3] / SD[7-4]	W4, Y4, V3, W3	I / IO	**Keyboard Inputs 6-3.** Sampled at reset on SD[7-4] and latched into Rx5A[7-4].

Chip Selects

Signal Name	Pin #	I/O	Signal Description
ROMCS# / KBCS# / **strap**	C1	O / O / I	**ROM Chip Select** (Rx5A[0]=1). Chip Select to the BIOS ROM. **Power-Up Configuration Strap (Sampled At Reset)**: 4.7K to GND = Socket-7, 4.7K to VCC3 = Socket-370 / Slot-1
PCS0# / GPO12 / XDIR	T5	O / IO / IO	**Programmable Chip Select 0** (Rx76[1] = 1 and Rx76[4] =1 (CD/CE) or Rx8B[0] = 1 (CF)). Asserted during I/O cycles to programmable read or write ISA I/O port ranges. Addressed devices drive data to the SD pins (XDIR is disabled and the X-Bus is not implemented). See also Rx59[3] and Rx77[2].
MCCS# / GPIOD / GPIO11	U8	O / IO / IO	**Microcontroller Chip Select** (Rx74[5] = 1, Rx74[7] = 0, Rx76[3] = 1, Rx76[4] = 1). Asserted during read or write accesses to I/O ports 62h or 66h.
MCCS# / GPO13 / SOE# **(CF)**	U5	O / IO / IO	**Microcontroller Chip Select** (Rx76[3] = 1, Rx76[4] = 0, Rx77[0] = 1). Asserted during read or write accesses to I/O ports 62h or 66h.

General Purpose Inputs

Signal Name	Pin #	I/O	Signal Description
GPI0 / IOCHCK#	F4	I	**General Purpose Input 0** (Rx74[0] = 0)
GPI1 / IRQ8#	W11	I	**General Purpose Input 1** (Rx5A[2] = 1)
GPI2 / BATLOW#	U11	I	**General Purpose Input 2**
GPI3 / LID / APICREQ#	U10	I	**General Purpose Input 3**
GPI4 / IRQ6 / SLPBTN#	G1	I	**General Purpose Input 4**
GPI5 / THRM / PME#	T11	I	**General Purpose Input 5** (Read pin state at function 4 Rx48[5])
GPI6 / SMBALRT#	W10	I	**General Purpose Input 6**
GPI7 / RING#	V11	I	**General Purpose Input 7**
GPI8 / GPO8 / GPIOA / GPOWE#	T14	I	**General Purpose Input 8** (Rx74[2] = 0)
GPI9 / GPO9 / GPIOB / FAN2 / DTEST	U12	I	**General Purpose Input 9+** (Rx74[3] = 0)
GPI10 / GPO10 / GPIOC / CHAS / ATEST	V14	I	**General Purpose Input 10** (Rx74[4] = 0)
GPI11 / GPO11 / GPIOD	U8	I	**General Purpose Input 11** (Rx74[5] = 0)
GPI12 / GPO24 / DRQ2 / FDCDRQ/ USBOC1# / SERIRQ	H3	I	**General Purpose Input 12** (Rx75[3] = 1 & 75[1]=0 & 68[3]=0)
GPI13 / GPO25 / DACK2# / FDCIRQ / USBOC0#	G5	I	**General Purpose Input 13** (Rx75[3] = 1 & 75[2]=0)
GPI16 / DRQ0 **(CF)**	L3	I	**General Purpose Input 16** (Rx77[7] = 1). Read at PMU IO 44[2]
GPI17 / DRQ1 **(CF)**	E2	I	**General Purpose Input 17** (Rx77[7] = 1). Read at PMU IO 44[3]
GPI18 / DRQ3 **(CF)**	D3	I	**General Purpose Input 18** (Rx77[7] = 1)
GPI19 / DRQ5 **(CF)**	M1	I	**General Purpose Input 19** (Rx77[7] = 1)
GPI20 / DRQ6 **(CF)**	M5	I	**General Purpose Input 20** (Rx77[7] = 1)
GPI21 / DRQ7 **(CF)**	N4	I	**General Purpose Input 21** (Rx77[7] = 1)
GPI22 / SDD6 **(CF)**	W15	I	**General Purpose Input 22** (Rx77[6] = 1, audio ena, game disa)
GPI23 / SDD7 **(CF)**	U14	I	**General Purpose Input 23** (Rx77[6] = 1, audio ena, game disa)
GPI[23-16] (SD[7-0] & RFSH#)	n/a	I	**General Purpose Inputs 16-23** (enabled on SD[7-0] by RFSH# active) (Rx77[7] = 0)

3.4 VIA VT82C686A Super South Bridge-10

General Purpose Outputs

Signal Name	Pin #	I/O	Signal Description
GPO0 / SLOWCLK	T8	O	**General Purpose Output 0** (Function 4 Rx54[1-0] = 00). Output value determined by PMU I/O Rx4C[
GPO1 / SUSA# / APICACK#	V9	O	**General Purpose Output 1** (Rx74[7] = 0 and Function 4 Rx54[2] = 1)
GPO2 / SUSB# / APICCS#	W9	O	**General Purpose Output 2** (Rx74[7] = 0 and Function 4 Rx54[3] = 1)

Signal Name	Pin #	I/O	Signal Description
GPO24 / DRQ2 / GPI12 / FDCDRQ/ USBOC1# / SERIRQ	H3	O	**General Purpose Output 24** (Rx75[3] = 1 & Rx75[1]=1 & Rx68[3]=0)
GPO[23-16] (latched from SD[7-0])	n/a	O	**General Purpose Output 23-16** (Rx74[7]=0) latched by GPOWE# rising
GPOWE# / GPIOA / GPI8 / GPO8	T14	O	**General Purpose Output Write Enable** (Rx74[2] = 1 and Rx76[0] = 1).

General Purpose Outputs

Signal Name	Pin #	I/O	Signal Description
GPO3 / SUSST1#	V10	O	**General Purpose Output 3** (Function 4 Rx54[4] = 1)
GPO4 / CPUSTP#	Y12	O	**General Purpose Output 4** (Rx75[4] = 1)
GPO5 / PCISTP#	V12	O	**General Purpose Output 5** (Rx75[5] = 1)
GPO7 / SLP#	T7	O	**General Purpose Output 7** (Rx75[7] = 1)
GPO8 / GPI8 / GPIOA / GPOWE#	T14	O	**General Purpose Output 8** (Rx74[2] = 1 and Rx76[0] = 0)
GPO9 / GPI9 / GPIOB / FAN2	U12	O	**General Purpose Output 9** (Rx74[3] = 1)
GPO10 / GPI10 / GPIOC / CHAS	V14	O	**General Purpose Output 10** (Rx74[4] = 1 and Rx76[2] = 0)
GPO11 / GPI11 / GPIOD	U8	O	**General Purpose Output 11** (Rx74[5] = 1 and Rx76[3] = 0)
GPO12 / XDIR / PCS0#	T5	O	**General Purpose Output 12** (Rx76[1] = 1 and Rx76[4] = 0)
GPO13 / SOE# / SCIOUT# **(CD/CE)** / MCCS# **(CF)**	U5	O	**General Purpose Output 13** (Rx77[0] = 1 and Rx74[7] = 0)
GPO14 / IRTX	E12	O	**General Purpose Output 14** (Rx76[5] = 1)
GPO15 / IRRX	D12	O	**General Purpose Output 15** (Rx76[5] = 1)
GPO16 / DACK0# **(CF)**	L2	O	**General Purpose Output 16** (Rx77[7] = 1 and Rx77[3] = 0)
GPO17 / DACK1# **(CF)**	E1	O	**General Purpose Output 17** (Rx77[7] = 1 and Rx77[3] = 0)
GPO18 / DACK3# **(CF)**	D2	O	**General Purpose Output 18** (Rx77[7] = 1 and Rx77[3] = 0)
GPO19 / DACK5# **(CF)**	L4	O	**General Purpose Output 19** (Rx77[7] = 1 and Rx77[3] = 0)
GPO20 / DACK6# **(CF)**	M3	O	**General Purpose Output 20** (Rx77[7] = 1 and Rx77[3] = 0)
GPO21 / DACK7# **(CF)**	N2	O	**General Purpose Output 21** (Rx77[7] = 1 and Rx77[3] = 0)
GPO22 / SDD8 **(CF)**	Y15	O	**General Purpose Output 22** (Rx77[6] = 1, audio enabled, game disabled)
GPO23 / SDD9 **(CF)**	V15	O	**General Purpose Output 23** (Rx77[6] = 1, audio enabled, game disabled)

General Purpose I/Os

Signal Name	Pin #	I/O	Signal Description
GPIOA / GPI8 / GPO8 / GPOWE#	T14	IO	**General Purpose I/O A / 8** (Rx76[0] = 0). GPOWE# if Rx76[0] = 1. See also Rx74[2]
GPIOB / GPI9 / GPO9 / FAN2 / DTEST	U12	IO	**General Purpose I/O B / 9.** See also Rx74[3]
GPIOC / GPI10 / GPO10 / CHAS/ ATEST	V14	IO	**General Purpose I/O C / 10.** (Rx76[2] = 0). See also Rx74[4]
GPIOD / GPI11 / GPO11 (default)/ MCCS#/ SCIOUT# **(CF)**	U8	IO	**General Purpose I/O D / 11.** (Rx76[3] = 0). See also Rx74[5]

Hardware Monitoring

Signal Name	Pin #	I/O	Signal Description
VSENS1	U13	I	**Voltage Sense 2.0V.** Monitor for CPU core voltage.
VSENS2	V13	I	**Voltage Sense 2.5V.** Monitor for North Bridge core voltage.
VSENS3	W14	I	**Voltage Sense 5V.**
VSENS4	Y14	I	**Voltage Sense 12V.** Connect +12V through a resistive voltage divider to insure 5V max to the input pin (see MVP4 Design Guide for details).
VREF	T13	P	**Voltage Reference for Thermal Sensing** (5V ¡ Ó 5%)
TSENS1	W13	I	**Temperature Sense 1.**
TSENS2	Y13	I	**Temperature Sense 2.**
FAN1	T12	I	**Fan Speed Monitor 1.** (3.3V only)
FAN2 / GPIOB/9 / DTEST	U12	I	**Fan Speed Monitor 2.**
CHAS / GPIOC/10 / ATEST	V14	I	**Chassis Intrusion Detect** (Rx76[2] = 1 and Rx74[4] = 1). Used for system security purposes.
DTEST / FAN2 / GPIOB/9	U12	O	**Hardware Monitor Digital Test Out**
ATEST / CHAS / GPIOC/10	V14	O	**Hardware Monitor Analog Test Out**

3.4 VIA VT82C686A Super South Bridge-11

XD Interface

Signal Name	Pin #	I/O	Signal Description
XDIR / PCS0# / GPO12	T5	O	**X-Bus Data Direction.** (Rx76[1]=0) Asserted low for all I/O read cycles and for memory read cycles to the programmed BIOS address space. XDIR is tied directly to the direction control of a 74F245 transceiver that buffers the X-Bus data and ISA-Bus data. The transceiver output enable may be grounded. SD0-7 connect to the "A"side of the transceiver and XD0-7 connect to the "B"side. XDIR high indicates that SD0-7 drives XD0-7.

Power Management

Signal Name	Pin #	I/O	Signal Description
THRM / GPI5 / PME#	T11	I	**Thermal Alarm Monitor** (Rx74[1] = 1)
PWRBTN#	Y11	I	**Power Button.** Used by the Power Management subsystem to monitor an external system on/off button or switch. The VT82C686A performs a 200us debounce of this input if Function 4 Rx40[5] is set to 1. (3.3V only)
SLPBTN# / IRQ6 / GPI4	G1	I / I / I	**Sleep Button.** Used by the Power Management subsystem to monitor an external system sleep button or switch. (Function 4 Rx40[6]=1) (10K PU to VCC if not used)
RSMRST#	V6	I	**Resume Reset.** Resets the internal logic connected to the VCCS power plane and also resets portions of the internal RTC logic.
EXTSMI#	Y10	IOD	**External System Management Interrupt.** When enabled to allow it, a falling edge on this input causes an SMI# to be generated to the CPU to enter SMI mode. (10K PU to VCCS if not used) (3.3V only)
PME# / GPI5 / THRM	T11	I	**Power Management Event.** (Rx74[1]=0) (1K PU to VCCS if not used)
SMBALRT# / GPI6	W10	I	**SMB Alert** (System Management Bus I/O space Rx08[3] = 1). When the chip is enabled to allow it, assertion generates an IRQ or SMI or power management event. (10K PU to VCCS if not used)
LID / GPI3	U10	I	**Notebook Computer Display Lid Open / Closed Monitor.** Used by the Power Management subsystem to monitor the opening and closing of the display lid of notebook computers. Can be used to detect either low-to-high and/or high-to-low transitions to generate an SMI#. The VT82C686A performs a 200 usec debounce of this input if Function 4 Rx40[5] is set to 1. (10K PU to VCCS if not used)

Signal Name	Pin #	I/O	Signal Description
RING# / GPI7	V11	I	**Ring Indicator.** May be connected to external modem circuitry to allow the system to be re-activated by a received phone call. (10K PU to VCCS if not used)
BATLOW# / GPI2	U11	I	**Battery Low Indicator.** (10K PU to VCCS if not used) (3.3V only)
CPUSTP# / GPO4	Y12	O	**CPU Clock Stop** (Rx75[4] = 0). Signals the system clock generator to disable the CPU clock outputs. Not connected if not used.
PCISTP# / GPO5	V12	O	**PCI Clock Stop** (Rx75[5] = 0). Signals the system clock generator to disable the PCI clock outputs. Not connected if not used.
SUSA# / GPO1 / APICACK#	V9	O	**Suspend Plane A Control** (Rx74[7]=0 and Function 4 Rx54[2]=0). Asserted during power management POS, STR, and STD suspend states. Used to control the primary power plane. (10K PU to VCCS if not used)
SUSB# / GPO2 / APICCS#	W9	O	**Suspend Plane B Control** (Rx74[7]=0 and Function 4 Rx54[3]=0). Asserted during power management STR and STD suspend states. Used to control the secondary power plane. (10K PU to VCCS if not used)
SUSC#	Y9	O	**Suspend Plane C Control.** Asserted during power management STD suspend state. Used to control the tertiary power plane. Also connected to ATX power-on circuitry.
SUSST1# / GPO3	V10	O	**Suspend Status 1** (Func4 Rx54[4] = 0 for GPO3). Typically connected to the North Bridge to provide information on host clock status. Asserted when the system may stop the host clock, such as Stop Clock or during POS, STR, or STD suspend states. Connect 10K PU to VCCS.
SUSCLK	T10	O	**Suspend Clock.** 32.768 KHz output clock for use by the North Bridge (e.g., Apollo MVP3 or MVP4) for DRAM refresh purposes. Stopped during Suspend-to-Disk and Soft-Off modes. Connect 10K PU to VCCS.

5133S M/B Maintenance

3.4 VIA VT82C686A Super South Bridge-12

Power and Ground

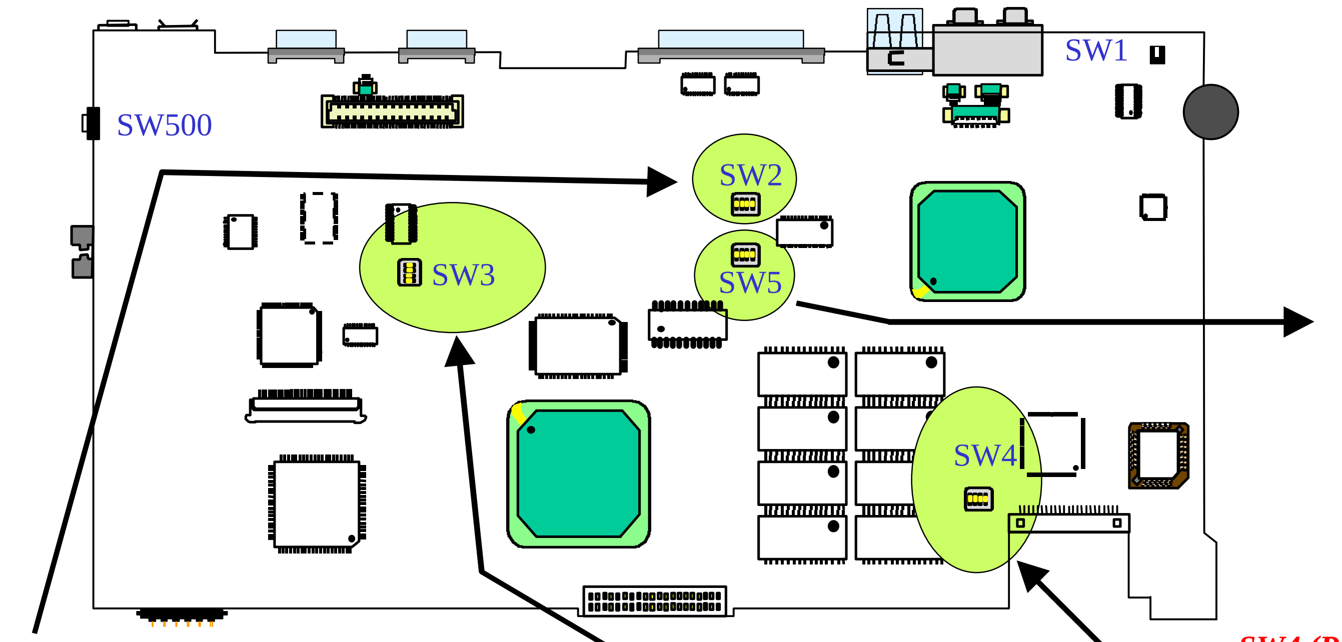
Signal Name	Pin #	I/O	Signal Description
VCC	F7, F10, F12-F14, H6, H15, J6, J15, K6, K15, M6, M15, N6, N15, R7-R8, R11, R14	P	**Core Power.** 3.3V nominal (3.15V to 3.45V). This supply is turned on only when the mechanical switch on the power supply is turned on and the PWRON signal is conditioned high. This pin should be connected to the same voltage as the CPU I/O circuitry. Internally connected to hardware monitoring system voltage detection circuitry for 3.3V monitoring.
GND	F6, F11, F15, G6, G15, J9-J12, K9-K12, L6, L9-L12, L15, M9-M12, P6, P15, R6, R15	P	**Ground.** Connect to primary motherboard ground plane.
VCCS	R9-R10	P	**Suspend Power.** Always available unless the mechanical switch of the power supply is turned off. If the "soft-off" state is not implemented, then this pin can be connected to VCC. Signals powered by or referenced to this plane are: PWRGD, RSMRST#, PWRBTN#, SMBCLK, SMBDATA, SUSCLK, SUSA# / GPO1, SUSB# / GPO2, SUSC#, SUSST1# / GPO6, GPI1 / IRQ8#, GPI2 / BATLOW#, GPI3 / LID, GPI5 / PME#, GPI6 / SMBALRT#, GPI7 / RING#, GPO0
VBAT	Y6	P	**RTC Battery.** Battery input for internal RTC (RTCX1, RTCX2)
VREF	T13	P	**Voltage Reference** (5V ¡ Ó5%). For thermal sensing and 5V input tolerance.
VCCH	R12	P	**Hardware Monitor Power.** Power for hardware monitoring subsystem (voltage monitoring, temperature monitoring, and fan speed monitoring). Connect to VCC through a ferrite bead.
GNDH	R13	P	**Hardware Monitor Ground.** Connect to GND through a ferrite bead.
VCCU	F9	P	**USB Differential Output Power.** Power for USB differential outputs (USBP0+, P0-, P1+, P1-, P2+, P2-, P3+, P3-). Connect to VCC through a ferrite bead.
GNDU	F8	P	**USB Differential Output Ground.** Connect to GND through a ferrite bead.

Resets and Clocks

Signal Name	Pin #	I/O	Signal Description
PWRGD	W6	I	**Power Good.** Connected to the PWRGOOD signal on the Power Supply.
PCIRST#	B16	O	**PCI Reset.** Active low reset signal for the PCI bus. The VT82C686A will assert this pin during power-up or from the control register.
RSTDRV	J1	O	**Reset Drive.** Reset signal to the ISA bus. Connect through an inverter to the chipset north bridge RESET# input and to PCI bus RESET#.
BCLK	H5	O	**Bus Clock.** ISA bus clock.
OSC	E4	I	**Oscillator.** 14.31818 MHz clock signal used by the internal Timer.
RTCX1	Y5	I	**RTC Crystal Input**: 32.768 KHz crystal or oscillator input. This input is used for the internal RTC and for power-well power management logic.
RTCX2	W5	O	**RTC Crystal Output**: 32.768 KHz crystal output
SLOWCLK / GPO0	T8	O	**Slow Clock.** .Frequency selectable if PMU function 4 Rx54[1-0] is nonzero (set to 01, 10, or 11).

5133S M/B Maintenance

4. Switch setting



SW5 (Frequency Select)

SW1-8	SW2-7	SW3-6	SW4-5	Host Frequency
ON	ON	ON	ON	124MHz
OFF	ON	ON	ON	120MHz
ON	OFF	ON	ON	114.99MHz
OFF	OFF	ON	ON	109.99MHz
ON	ON	OFF	ON	105MHz
OFF	ON	OFF	ON	83.31MHz
ON	OFF	OFF	ON	137MHz
OFF	OFF	OFF	ON	75MHz
ON	**ON**	**ON**	**OFF**	**100MHz**
OFF	**ON**	**ON**	**OFF**	**95.19MHz**
ON	OFF	ON	OFF	83.31MHz
OFF	OFF	ON	OFF	133.33MHz
ON	ON	OFF	OFF	90MHz
OFF	**ON**	**OFF**	**OFF**	**96.22MHz**
ON	OFF	OFF	OFF	66.82MHz
OFF	OFF	OFF	OFF	91.5MHz

SW2(Bus Ratio Select)

Pin 1-8	Pin 2-7	Pin 3-6	Bus Ratio
BF0	BF1	BF2	
ON	ON	OFF	2.5X
OFF	ON	OFF	3.0X
ON	OFF	OFF	2.0X
OFF	OFF	OFF	3.5X
ON	ON	ON	4.5X
OFF	ON	ON	5.0X
ON	OFF	ON	4.0X
OFF	OFF	ON	5.5X

SW3 (Core Voltage Select)

Pin 4-5	Pin 3-6	Vcore Voltage
ON	ON	2.20V
OFF	ON	2.00V
ON	OFF	2.10V
OFF	OFF	1.90V

(MDC Select)

Pin 2-7	Function
ON	With MDC
OFF	Without MDC

(Key Board Type Select)

Pin 1-8	Function
ON	US Keyboard
OFF	Japan Keyboard

SW4 (Panel ID Select)

Pin 4-5	Pin 3-6 (MAA5)	Pin 2-7 (MAA4)	Pin 1-8 (MAA3)	Panel Type
X	ON	ON	ON	HYUNDAI HT13x13-201 1024*768 (13.3” TFT)
X	ON	ON	OFF	
X	ON	OFF	ON	SANYO TM121SV-02L01 800*600 (12.1” TFT)
X	ON	OFF	OFF	
X	OFF	ON	ON	MITSUBISHI AA121SJ03 800*600(12.1” TFT)
X	OFF	ON	OFF	Sanyo (12.1” HPA)
X	OFF	OFF	ON	Sanyo (12.1” DSTN)
X	OFF	OFF	OFF	

** X : Don't Care.

5133S M/B Maintenance

5. Assembly & disassembly

5.1 System view

5.1.1 Right-side view
5.1.2 Left-side view
5.1.3 Rear view
5.1.4 Front view
5.1.5 Top-open view

5.2 System disassembly

Modular components

5.2.1 Battery pack
5.2.2 CD-ROM drive
5.2.3 CPU
5.2.4 Fax/ modem/data card
5.2.5 SO-DIMM
5.2.6 Keyboard

LCD assembly components

5.2.7 LCD assembly
5.2.8 LCD panel
5.2.8.1 12.1 inch LCD panel
5.2.8.2 13.3 inch LCD panel
5.2.9 inverter board

Base unit components

5.2.10 Hard disk drive
5.2.11 Touch pad board
5.2.12 System board
5.2.13 Floppy disk drive

5. Assembly & disassembly

5.1 System view

5.1.1 Right-side view

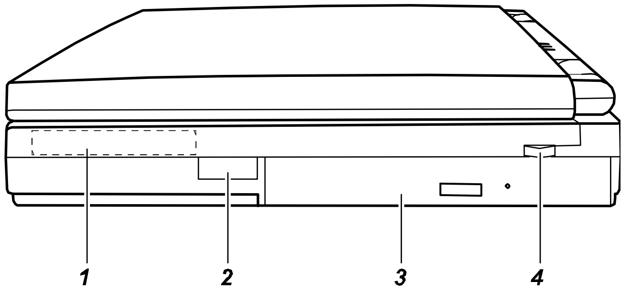


Figure 5-1. Right-Side View

1. **Hard Disk Drive**
2. **IR Port**
3. **CD-ROM/DVD-ROM Drive**
4. **Volume Control**

5.1.2 Left-side view

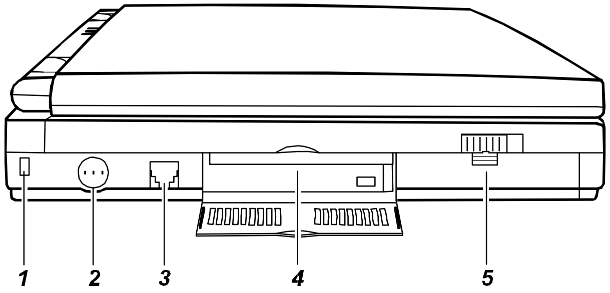
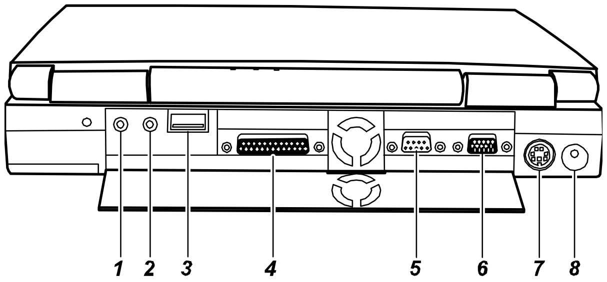


Figure 5-2. Left-Side View

1. **Kensington Lock Anchor**
2. **Power Button**
3. **Phone Line Connector** (optional)
4. **PC Card Slot**
5. **Battery Pack**

5. Assembly & disassembly

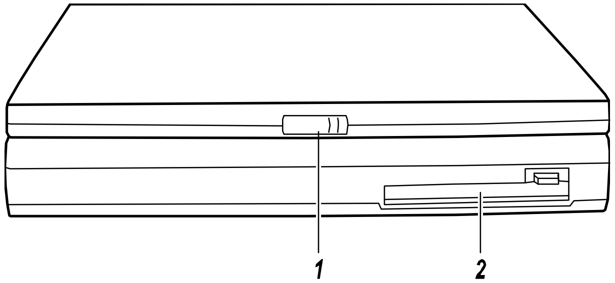
5.1.3 Rear view



1. **Microphone Connector**
2. **Audio Output Connector**
3. **USB Port**
4. **Parallel Port**
5. **Serial Port**
6. **VGA Port**
7. **PS/2 Mouse/Keyboard Port**
8. **Power Connector**

Figure 5-3. Rear View

5.1.4 Front view



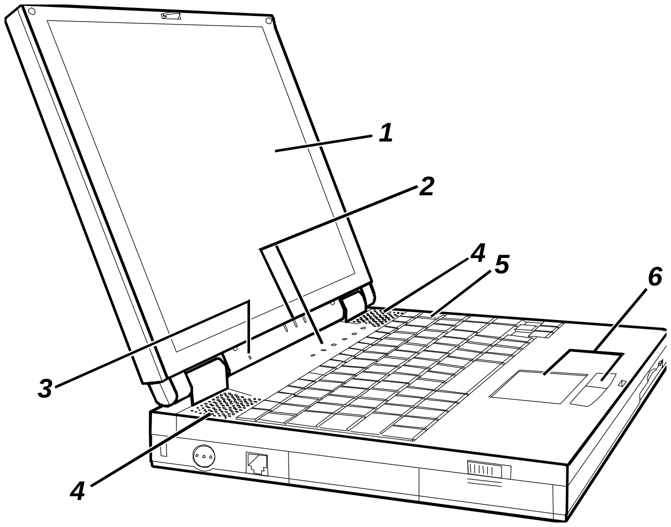
1. **Top Cover Latch**
2. **Floppy Disk Drive**

Figure 5-4. Front View

5. Assembly & disassembly

5.1.5 Top-open view

To open the cover, press the cover latch toward the right and lift the cover.



1. **LCD Display**
2. **Indicators Panel**
3. **Microphone**
4. **Stereo Speaker Set**
5. **Keyboard**
6. **Touchpad**

Figure 5-5. Top-Open View

5. Assembly & disassembly

5.2 System disassembly

The section discusses at length each major component for disassembly/reassembly and show corresponding illustrations. Use the chart below to determine the disassembly sequence for removing components from the notebook.

Modular Components
- 2.2.1 Battery Pack
- 2.2.2 CD-ROM/DVD-ROM Drive
- 2.2.3 CPU
- 2.2.4 Fax/Modem/Voice Card
- 2.2.5 SO-DIMM
- 2.2.6 Keyboard

LCD Assembly Components
- 2.2.7 LCD Assembly
- 2.2.8.1 12.1 Inch LCD Panel
- 2.2.8.2 13.3 Inch LCD Panel
- 2.2.9 Inverter Board/LED Board

Base Unit Components
- 2.2.10 Hard Disk Drive
- 2.2.11 Touchpad Board
- 2.2.12 System Board
- 2.2.13 Floppy Disk Drive

♦ You can also find details of each component on the exploded charts.

5. Assembly & disassembly

5.2.1 Battery pack

Disassembly

1.Place the notebook upside down.

2.First push away the small locking latch (❶) on the battery pack and then slide the locking latch (❷) on the side of the notebook to unlock and lift (❸) the battery pack out of the compartment.

Reassembly

1.Fit the battery pack into the compartment.
Make sure the locking latch is in the locked position.
(Refer to Figure 5-6 earlier.)

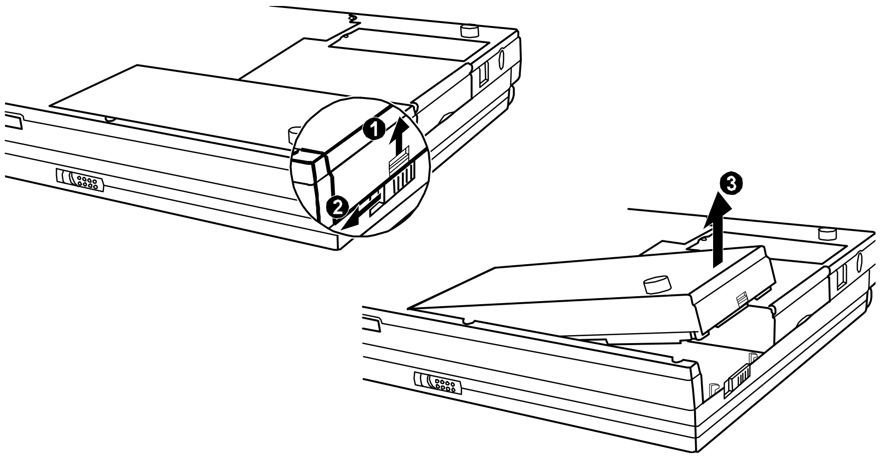


Figure 5-6. Removing the Battery Pack

5. Assembly & disassembly

5.2.2 CD-ROM/DVD-ROM DRIVE

Disassembly

1. Place the notebook upside down.
2. Open the CPU compartment cover by removing four screws and lifting up the cover from one side. (Refer to Figure 5-7)
3. Unplug the CD-ROM/DVD-ROM drive cable from the system board. (Refer to Figure 5-8)
4. Remove one screw and slide the CD-ROM/DVD-ROM drive out of the compartment. (Refer to Figure 5-9)

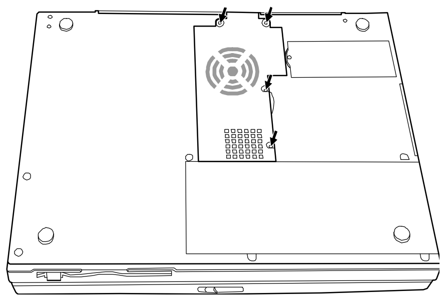


Figure 5-7. Removing the CPU Compartment Cover

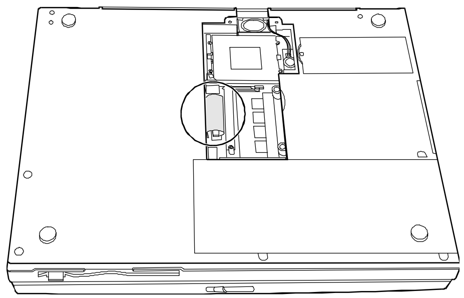


Figure 5-8. Unplugging the CD-ROM Drive Cable

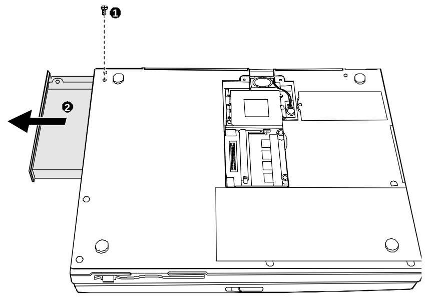


Figure 5-9. Removing the CD-ROM Drive

Reassembly

1. Connect one end of the cable to the CD-ROM/DVD-ROM drive.
2. Slide the CD-ROM/DVD-ROM drive into the compartment and secure with one screw. (Refer to Figure 5-9 earlier.)
3. Connect the CD-ROM/DVD-ROM drive cable to the system board. (Refer to Figure 5-8 earlier.)
4. Replace the CPU compartment cover and secure with four screws. (Refer to Figure 5-7 earlier.)

5. Assembly & disassembly

5.2.3 CPU

Disassembly

1. Place the notebook upside down.
2. Open the CPU compartment cover by removing four screws and lifting up the cover from one side.
3. Remove four screws that fasten the fan assembly. Unplug the fan assembly's power cord from the system board. Then lift the fan assembly free from the housing. (Refer to Figure 5-10)
4. Gently remove the thermal pad and the metal shield around the CPU. (Refer to Figure 5-11)

NOTE: When you remove the CPU heatsink, make sure that the thermal pad is not damaged. If it is damaged, you have to use a new thermal pad.

5. Insert a minus screwdriver 101 (JIS standard) to the OPEN side of the socket and gently push the screwdriver to pry the CPU out of the socket. (Refer to Figure 5-12)

CAUTION: The maximum force for extraction of the CPU should not exceed 100 lbs (45.5 kg).

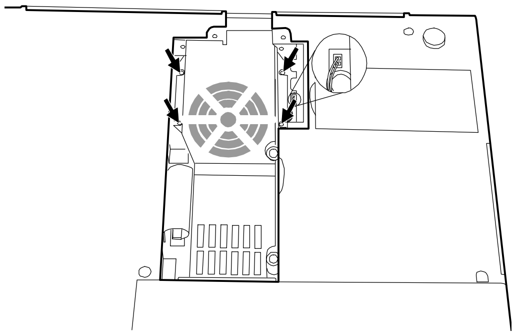


Figure 5-10. Removing the screws and the fan power cord

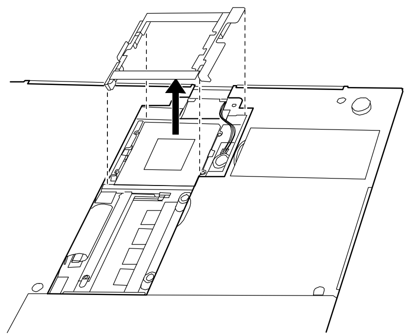


Figure 5-11. Unplug the thermal pad and the metal

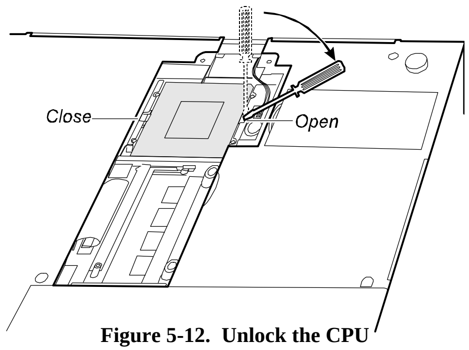


Figure 5-12. Unlock the CPU

5. Assembly & disassembly

5.2.3 CPU

Reassembly

1. Align the beveled corner of the CPU with the beveled corner of the socket and insert the CPU pins into the holes. Insert a minus screwdriver to the CLOSE side of the socket and push the screwdriver toward the CPU to secure the CPU in place.

> ***CAUTION:*** The maximum force for insertion of the CPU should not exceed 100 lbs (45.5 kg).

2. Align the metal shield with the CPU socket. Gently place the shield into the housing around the CPU.
3. Attach the thermal pad to the surface of the heatsink.
4. Connect the power cord of the fan assembly and fit it into place. First secure the two screws on the CLOSE side and then the two screws on the OPEN side.
5. Replace the CPU compartment cover and secure with four screws.

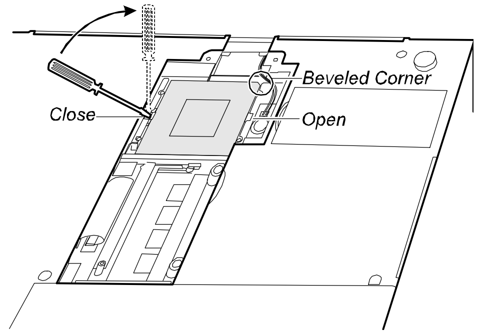


Figure 5-13. Placing the CPU and securing the CPU

5. Assembly & disassembly

5.2.4 Fax/ Modem/ Voice card

Disassembly

1. Place the notebook upside down.   Remove one screw and lift up the cover. (Refer to Figure 5-14)
2. Remove two screws and lift up the metal shield. (Refer to Figure 5-15)
3. Unplug the modem cable and gently lift up the modem card. (Refer to Figure 5-16)

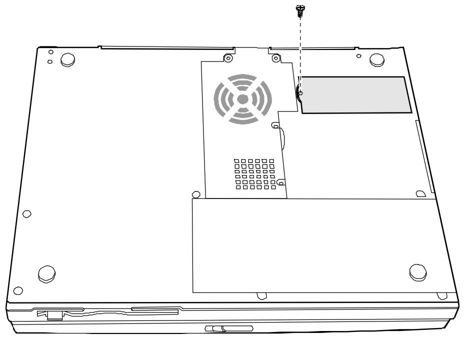


Figure 5-14. Remove one screw and lift up the cover.

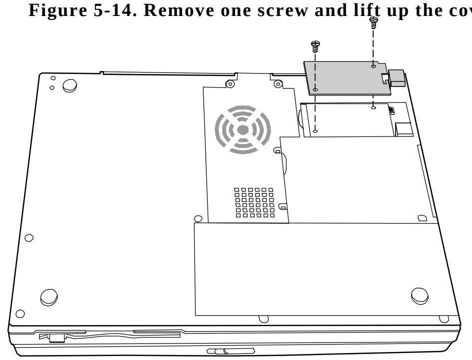


Figure 5-15. Remove two screws and lift up the metal shield.

Reassembly

1. Plug the cable connector to the system board and the card connector into the socket.
2. Fold the transparent plastic cover into the housing.
3. Place the metal shield on top of the modem card and secure with two screws.
4. Replace the compartment cover and secure with one screw.

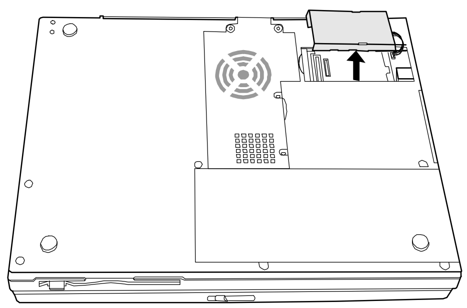


Figure 5-16. Remove Fax/ Modem/ Voice card

5. Assembly & disassembly

5.2.5 SO-DIMM

Disassembly

1. Open the CPU compartment cover by removing four screws and lifting up the cover from one side.
2. Pull the retaining clips outwards and remove the SO-DIMM. (Refer to Figure 5-18)

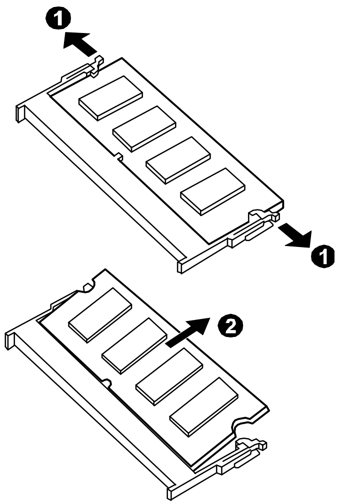


Figure 5-18. Removing the SO-DIMM

Reassembly

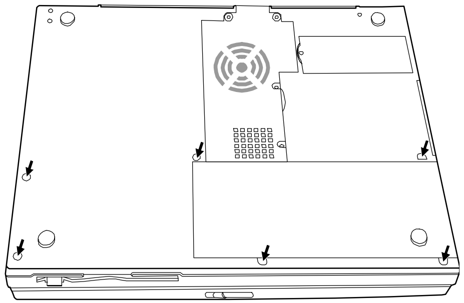
1. To install the SO-DIMM, align the SO-DIMM's notched part with the socket's corresponding part and firmly insert the SO-DIMM into the socket at an angle. Then push down until the retaining clips lock the SO-DIMM into position.
2. Replace the compartment cover and secure with four screws.

Assembly & disassembly

5.2.6

Disassembly

1. Remove six bottom screws. (Refer to Figure 5-19)
2. Put the notebook back to the upright position and open the top cover. Remove the base unit cover.
3. Lift the keyboard and unplug the keyboard cable from the system board. (Refer to Figure 5-20)



Reassembly

1. Reconnect the keyboard cable and fit the keyboard back into place.
2. Replace the base unit cover.
3. Replace the six bottom screws.

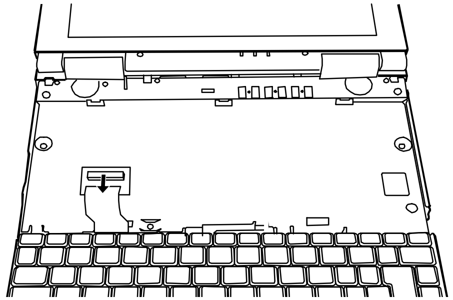


Figure 5-20. Removing the keyboard cable

5. Assembly & disassembly

5.2.7 LCD assembly

Disassembly

1. Remove the keyboard. (See section 5.2.6.)
2. Remove the shield plate by removing 12 screws. (Refer to Figure 5-21)
3. Remove the hinge cover by inserting a flat screwdriver to the rear of the cover and pry the cover out. Repeat the same with the other hinge cover. Note the right and left hinges are not exchangeable. (Refer to Figure 5-22)
4. Unplug the three cable connectors coming from the LCD assembly.
5. Remove four screws from the hinges. Now you can separate the LCD assembly from the base unit. (Refer to Figure 5-23)

Reassembly

Attach the LCD assembly to the base unit and secure with four screws on the hinges.

2. Reconnect the LCD cable connectors to the system board.
3. Replace the two hinge covers.
4. Replace the shield plate and secure with 12 screws.
5. Connect the keyboard cable and replace the keyboard.
6. Replace the base unit cover.
7. Replace the six bottom screws.

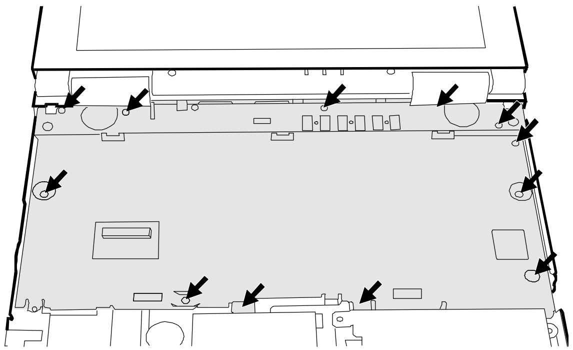


Figure 5-21. Removing the shield plate.

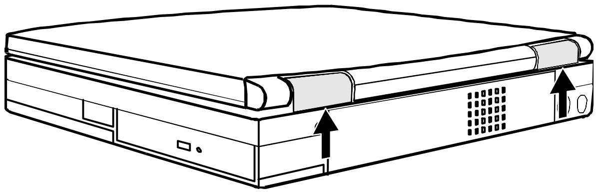


Figure 5-22. Removing the hinge covers.

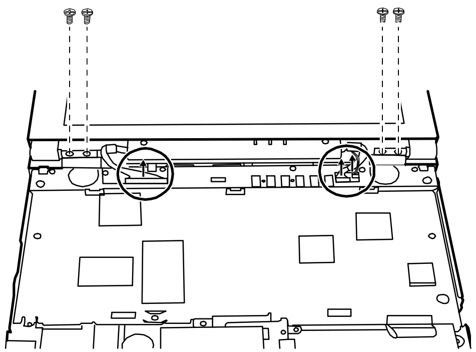


Figure 5-23. Unplugging the cable connectors and removing four screws

5. Assembly & disassembly

5.2.8.1 12.1 inch LCD panel

Disassembly

1. Open the top cover.
2. Remove the four rubber pads and the four screws underneath. Then you can separate the LCD frame from the housing. (Refer to Figure 5-24)
3. To remove the LCD, remove four screws and unplug the cables. (Refer to Figure 5-25)

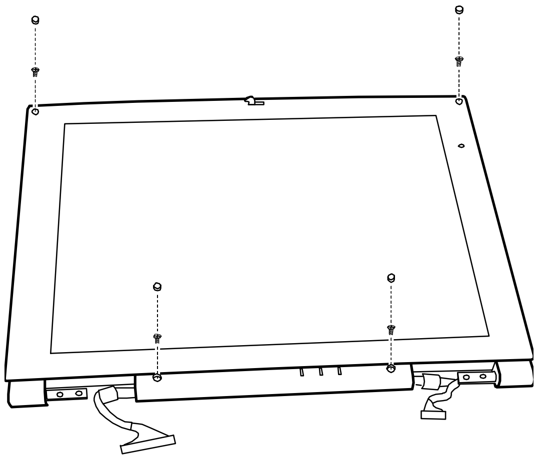
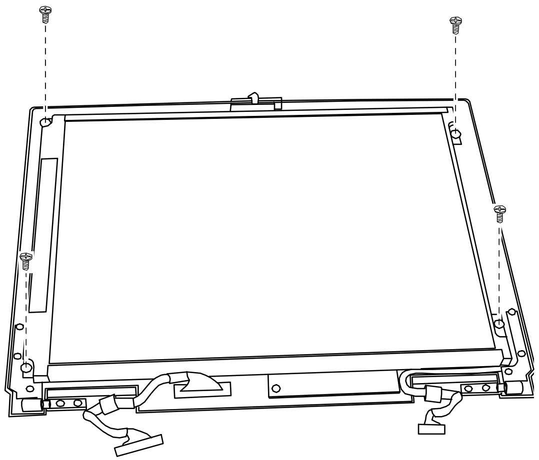


Figure 5-24. Removing the 12.1 inch LCD frame.

Reassembly

1. Reconnect the cables to the LCD. Fit the LCD back into place and secure with four screws.
2. Fit the LCD frame back to the housing and replace the four screws and rubber pads.



5. Assembly & disassembly

5.2.8.2 13.3 inch LCD panel

Disassembly

1. Open the top cover.
2. Remove the four rubber pads and two screws on the bottom side. Then slightly lift up the bottom part of the frame and gently separate the LCD frame from the housing. (Refer to Figure 5-26)
3. To remove the LCD, remove six screws and unplug the cables. (Refer to Figure 5-27)

Reassembly

1. Reconnect the cables to the LCD. Fit the LCD back into place and secure with six screws.
2. Fit the LCD frame back to the housing and replace the two screws and four rubber pads.

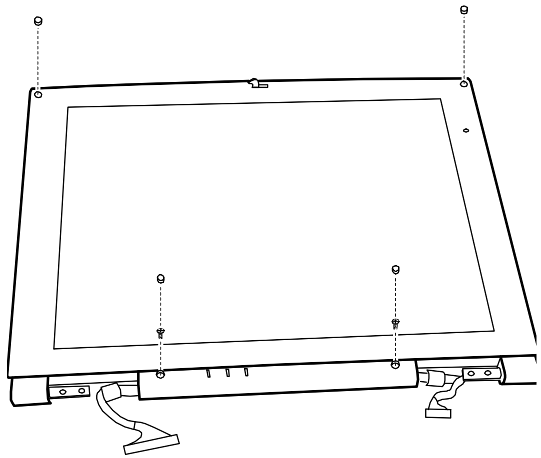


Figure 5-26. Removing the 13.3 inch LCD frame.

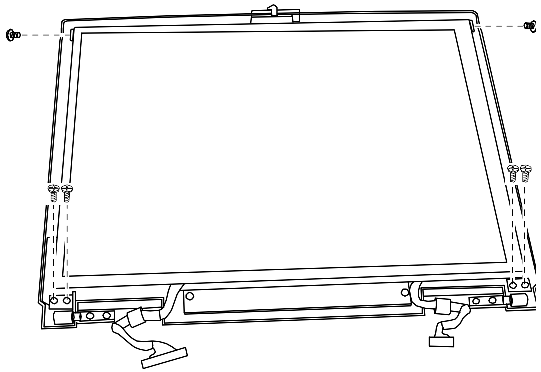


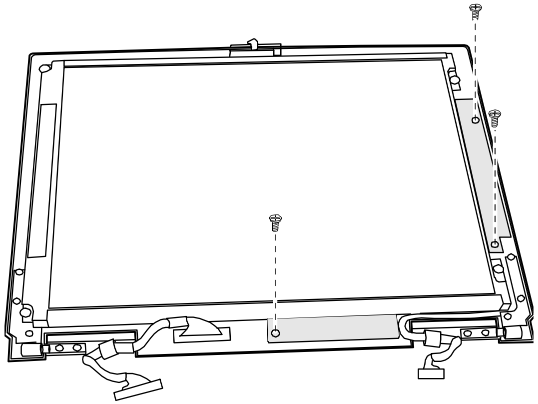
Figure 5-27. Removing the 13.3 inch LCD.

Assembly & disassembly

5.2.9 Inverter board / LED board

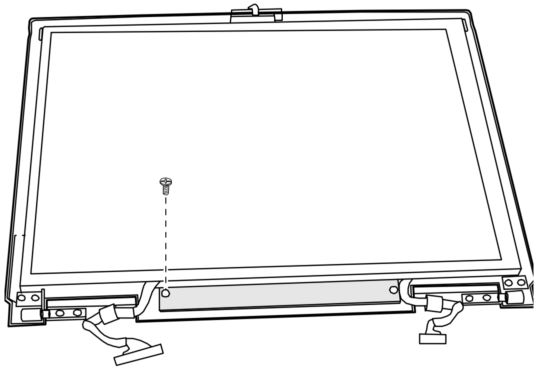
Disassembly

1. Detach the LCD frame. (See steps 1 to 2 in section 5.2.8 Disassembly.)
2. For 12.1 inch LCD:
   To remove the LED board at the bottom side of the LCD , remove one screw and unplug the connectors from the board.
   To remove the inverter board at the right side of the LCD , remove two screws and unplug the connectors from the board. (Refer to Figure 5-28)
3. For 13.3 inch LCD:
   To remove the inverter/LED board at the bottom side of the LCD , remove one screw and unplug the connectors from the board. (Refer to Figure 5-29)



Removing the Inverter and LED board for 12.1 inch LCD.

1. Reconnect the connectors. Fit the inverter/LED board back into place and secure with according number of screws.
2. Place the LCD frame back to the housing.



Removing the Inverter and LED board for the 13.3 inch LCD.

5. Assembly & disassembly

5.2.10 Hard disk drive

Disassembly

Remove the keyboard. (See section 5 .2.6.)
Remove two top screws from the hard disk drive bracket and slide the hard disk drive
30)
To separate the hard disk drive from the bracket, remove fou
bracket. (Refer to Figure 5-31)

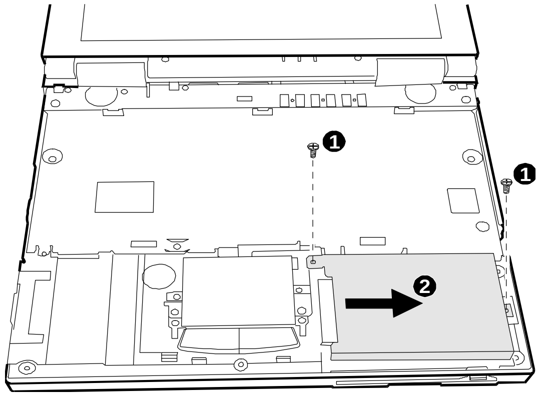


Figure 5-30. Removing the Hard disk drive.

Reassembly

1.
2.
place with two screws.
Replace the base unit cover.

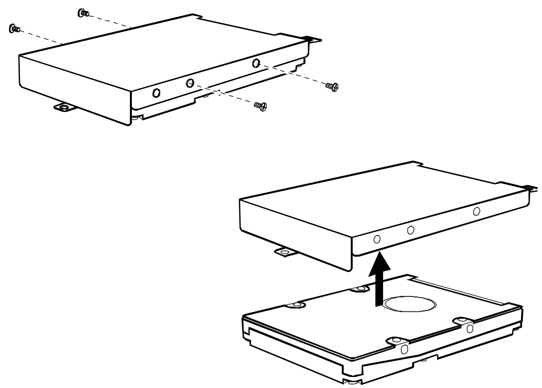


Figure 5-31. Removing the Hard disk drive bracket.

5. Assembly & disassembly

5.2.11 Touch Pad board

Disassembly

1. Remove the keyboard and shield plate. (See section 5.2.6 and 5.2.7.)
2. Remove the hard disk drive. (See section 5.2.10.)
3. Lift the touchpad board free. (Refer to Figure 5-32)

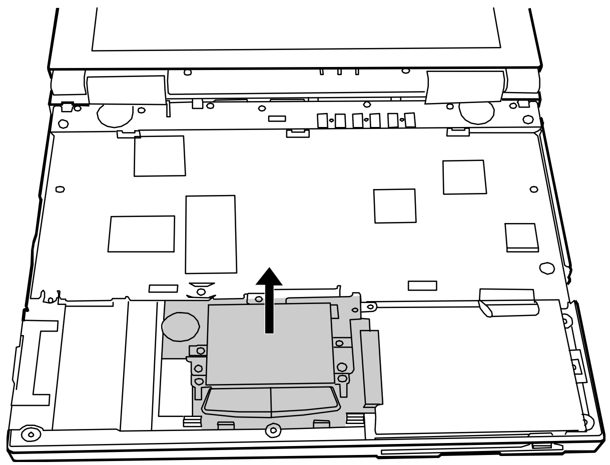


Figure 5-32. Removing the Touch pad board.

Reassembly

1. Fit the touchpad board into place.
2. Replace the hard disk drive.
3. Replace the shield plate and keyboard.

5. Assembly & disassembly

5.2.12 System board

Disassembly

1.
2.
3.
4. CPU and cooling fan assembly. (See section 5.2.3.)
Remove the Data/Fax/Modem Card if it exists. (See sectio
6.
7.
8. touchpad board. (See section 5.2.11.)
Unplug the speaker connectors from the system board.
Remove five screws fastening the (Refer to Figure 5- 3
11. (Refer to Figure 5-3)
5
13. Unplug the floppy disk drive cable connector from the system board. (Refer to Figure 5-3)

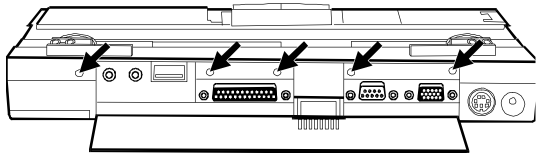


Figure 5-33. Removing five rear screws.

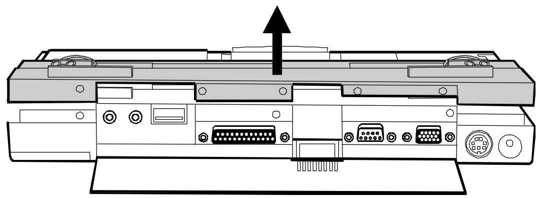


Figure 5-34. Removing the rear frame.

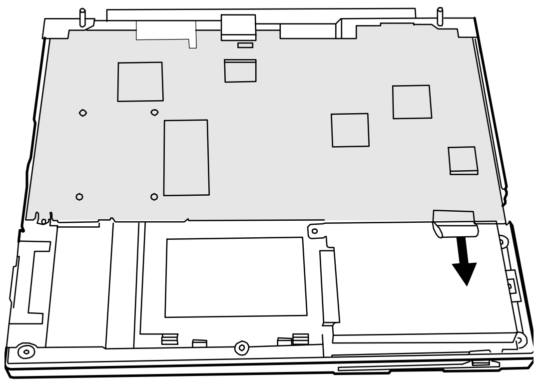


Figure 5-36. Unplugging the floppy disk drive cable.

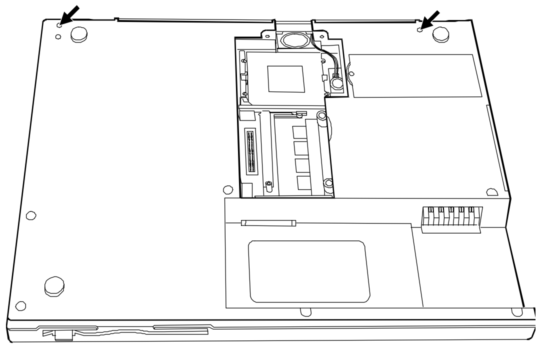


Figure 5-35. Removing two bottom screws.

5. Assembly & disassembly

5.2.12 System board

Reassembly

1. Fit the system board into place.
2. Connect the floppy disk drive cable to the system board.
3. Replace two bottom screws fastening the system board.
4. Replace the rear frame and five rear screws.
5. Replace the touchpad board by plugging the connector.
6. Replace the hard disk drive with its bracket by plugging the connector to the touchpad board and securing with two screws.
7. Connect the speaker connectors.
8. Attach the LCD assembly to the base unit and secure with four screws.
9. Replace the two hinge covers.
10. Fit the shield plate back into place and secure with 12 screws.
11. Connect the keyboard cable and replace the keyboard.
12. Fit the base unit cover into place and secure with six bottom screws.
13. Replace the CD-ROM drive by sliding it into the compartment, plugging the connector, and secure with one bottom screw.
14. Replace the CPU and fan assembly. Secure the fan assembly with four screws.
15. Replace the CPU compartment cover and secure with four screws.
16. Replace the Data/Fax/Modem Card and metal shield, then secure with two screws.
17. Replace the Data/Fax/Modem Card compartment cover and secure with one screw.
18. Replace the battery pack.

5. Assembly & disassembly

5.2.13 Floppy disk drive

Disassembly

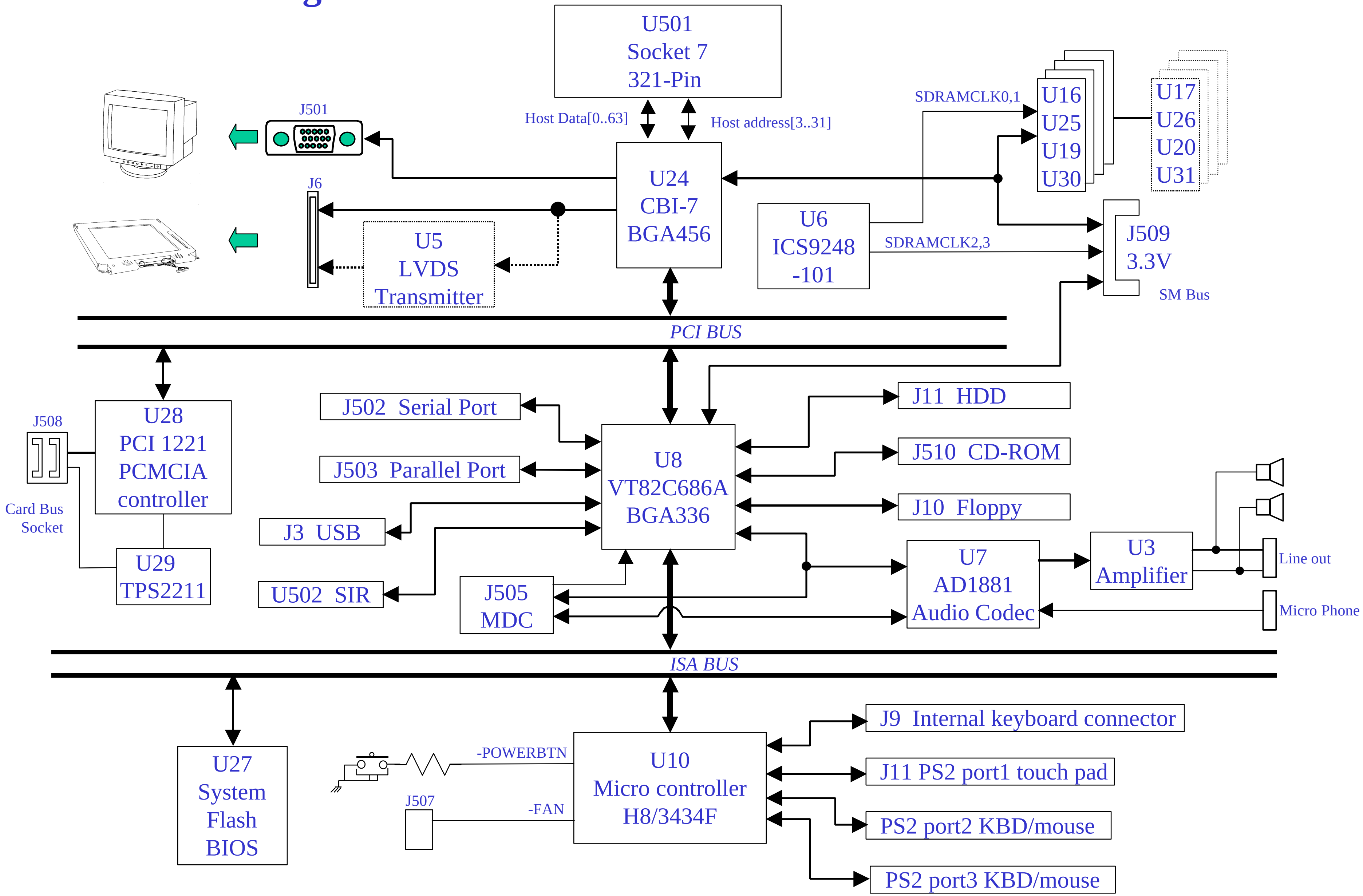
1. Remove the system board. (See section 5.2.12 Disassembly.)
2. Remove the floppy disk drive by first lifting the rear end of the floppy disk drive.

Reassembly

1. Connect the floppy disk drive cable to the floppy disk drive and fit the floppy disk drive into place.
2. Replace the system board. (See section 5.2.12 Reassembly.)

5133S M/B Maintenance

6. 5133S Block Diagram



7. Maintenance diagnostics

7.1 Introduction

Every time the computer is turned on ,the system bios runs a series of internal checks on the hardware. This power-on self test (post) allows the computer to detect problems as early as the power-on stage. Error messages of post can alert you to the problems of your computer.

If an error is detected during these tests, you will see an error message displayed on the screen. If the error occurs before the display, then the screen cannot display the error message. Error codes or system beeps are used to identify a post error that occurs when the screen is not available.

The value for the diagnostic post(378H) is written at the beginning of the test. Therefore , if the test fail, the user can determine where the problem occurs by reading the last value written to post 378H by the PIO debug board plug at PIO port.

7. Maintenance diagnostics

7.2 error codes : Following is a list of error codes in sequent display on the pio debug board.

System soft BIOS:

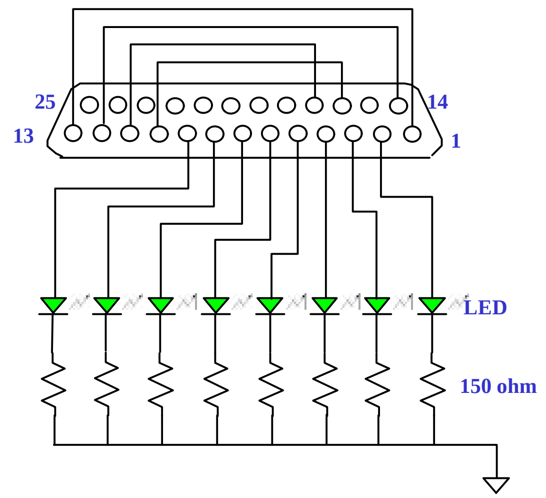
CODE	DESCRIPTION
01h	Start of boot loader sequence.
02h	Initialize chipset.
03h	Memory Sizing.
04h	Perform conventional RAM(1st 640K) test with crossed-pattern R/W
05h	Move boot loader to the RAM.
06h	Start point of execution of boot loader in RAM.
07h	Shadow system BIOS.
08h	Initialize clock synthesizer
09h	Initialize audio controller.
0Ah	Detect internal ISA MODEM
0Bh	Proceed with normal boot
0Ch	Proceed with crisis boot
0Fh	DRAM sizing
10h	Initial L1,L2 cache, make stack and diagnose CMOS.
11h	Turn off fast A20 for post. Reset GDT's, 8259s quickly.
12h	Signal power on reset at COMS.
13h	Initialize the chipset, (SDRAM).
14h	Search for ISA bus VGA adapter
15h	Reset counter/timer 1, exite the RAM.
16h	User register config through CMOS
18h	Dispatch to 1st 64K RAM test
19h	Checksum the ROM
1Ah	Reset PIC's(8259s)
1Bh	Initialize video adapter(s)
1Ch	Initialize video (6845 regs)

CODE	DESCRIPTION
1Dh	Initialize color adapter
1Eh	Initialize monochrome adapter
1Fh	Test 8237A page registers
20h	Perform keyboard self test
21h	Test & initialize keyboard controller
22h	Check if CMOS RAM valid
23h	Test battery fail & CMOS X-SUM
24h	Test the DMA controllers
25h	Initialize 8237A controller
26h	Initialize interrupt vectors table.
27h	RAM quick sizing
28h	Protected mode entered safely
29h	RAM test completed
2Ah	Protected mode exit successful
2Bh	Setup shadow
2Ch	Prepare to initialize video
2Dh	Search for monochrome adapter
2Eh	Search for color adapter, VGA initialize.
2Fh	Signon messages displayed
30h	Special init of keyboard ctlr
31h	Test if keyboard present
32h	Test keyboard interrupt
33h	Test keyboard command Byte
34h	Test, blank and count all RAM
35h	Protected mode entered safely (2).
36h	RAM test complete

7. Maintenance diagnostics

CODE	DESCRIPTION
37h	Protected mode exit successful
38h	Update keyboard output port to disable gate of A20
39h	Setup cache controller
3Ah	Test if 18.2Hz periodic working
3Bh	Initialize BIOS data area at 40:0.
3Ch	Initialize the hardware interrupt vector tabl
3Dh	Search and init the Mouse
3Eh	Update num lock status
3Fh	OEM initialization of COMM and LPT ports
40h	Configure the COMM and LPT ports
41h	Initialize the floppies
42h	Initialize the hard disk
43h	OEM's init of PM with USB
44h	Initialize additional ROMs
45h	Update NUMLOCK status
46h	Test for coprocessor installed
47h	OEM's init of power management, (check SMI)
48h	OEM functions before boot (PCMCIA, CardBus)
49h	Dispatch to operation system boot
4Ah	Jump into bootstrap code

PIO PORT (378H) DIAGNOSTIC TOOLS



PIN1 : STROBE ⟷ PIN13: SLCT
PIN10: ACK# ⟷ PIN16: INT#
PIN11: BUSY ⟷ PIN17: SELIN#
PIN12:PTERR ⟷ PIN14: AUTOFD#
PIN[9:2]:PD[7:0]

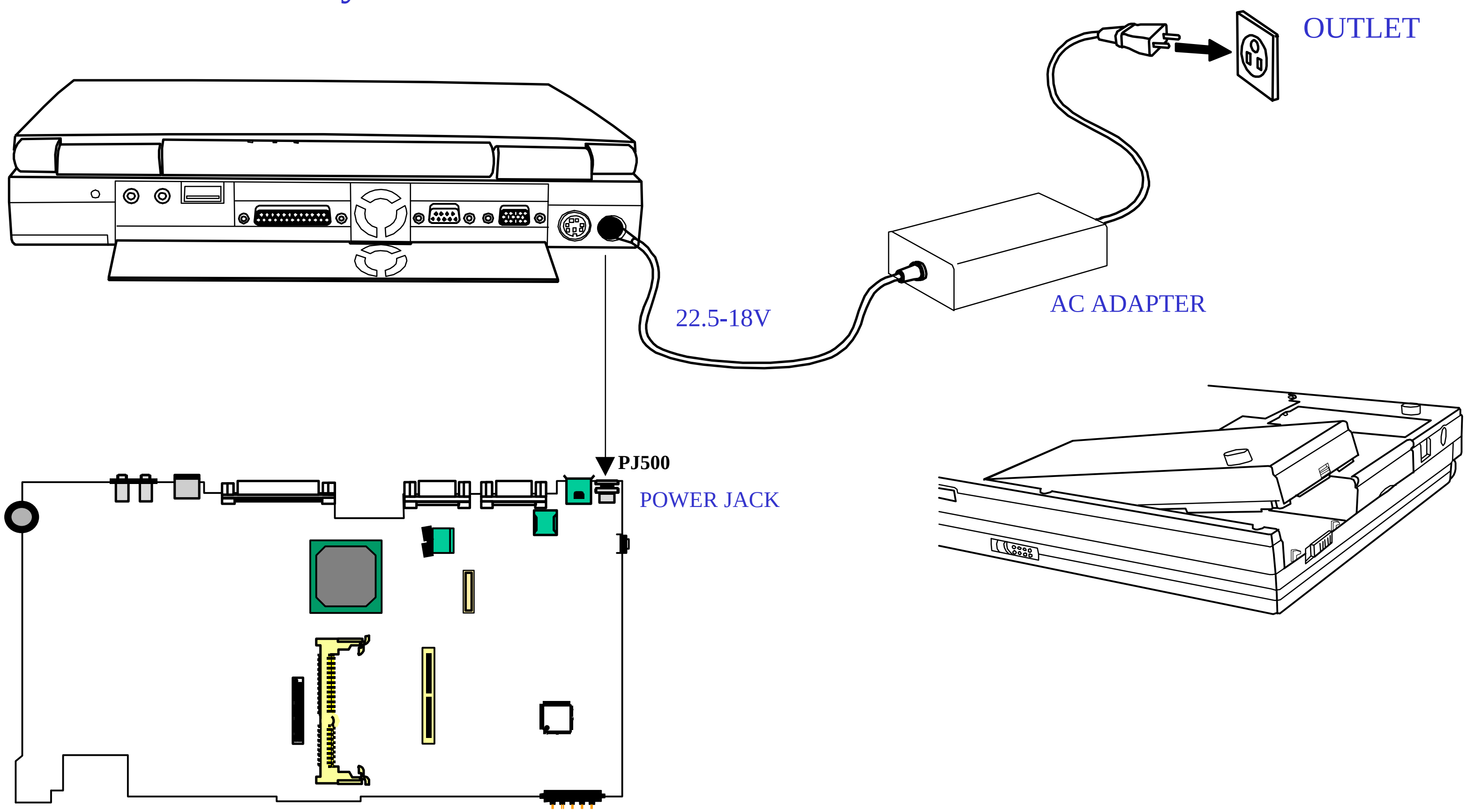
8. Trouble shooting

5133S M/B Maintenance

8.1 No power:

When the power button is pressed, nothing happens ,power indicator does not light up.

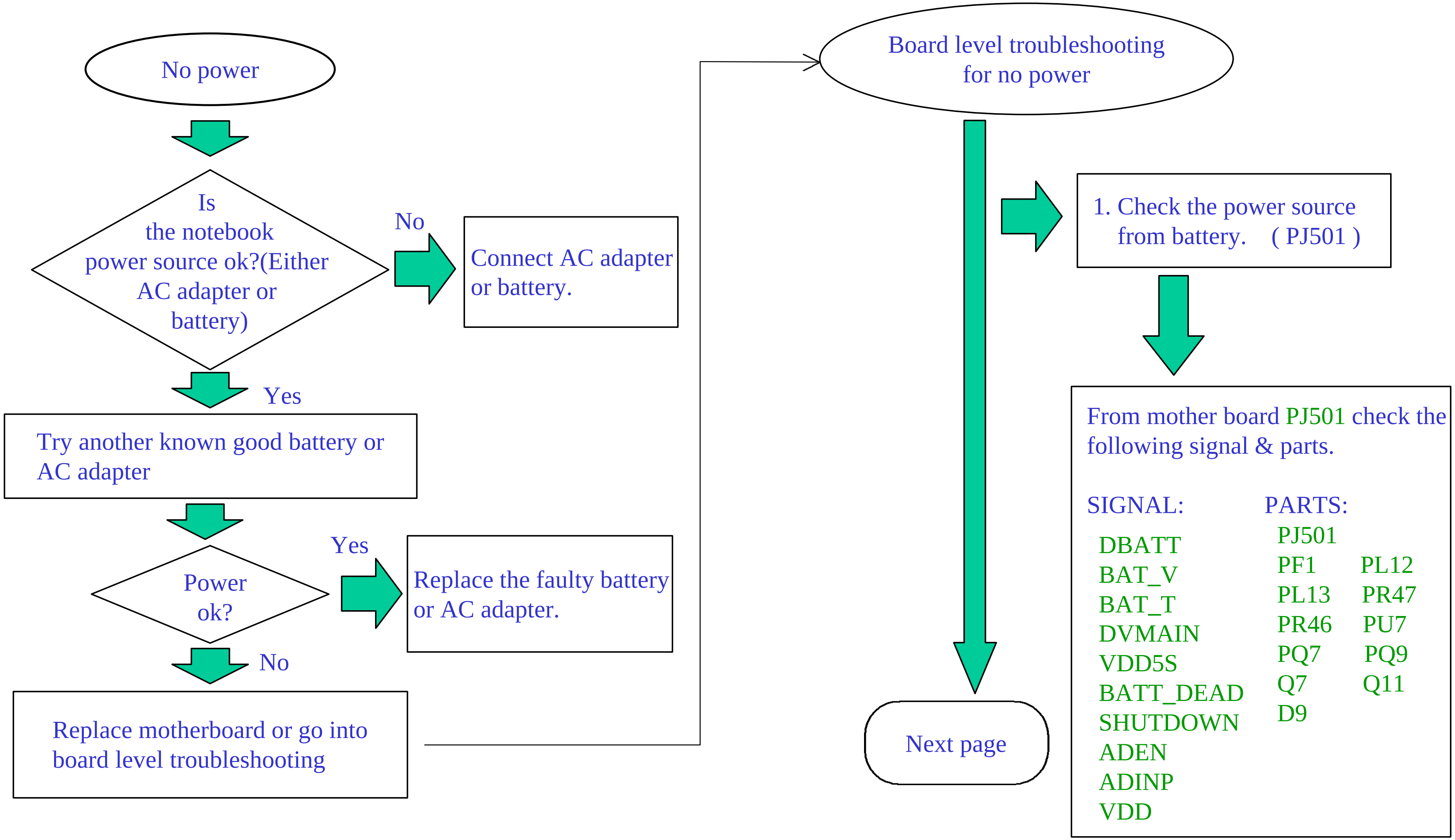
1. Check ac adaptor
2. Check battery



5133S M/B Maintenance

8.1 No power:

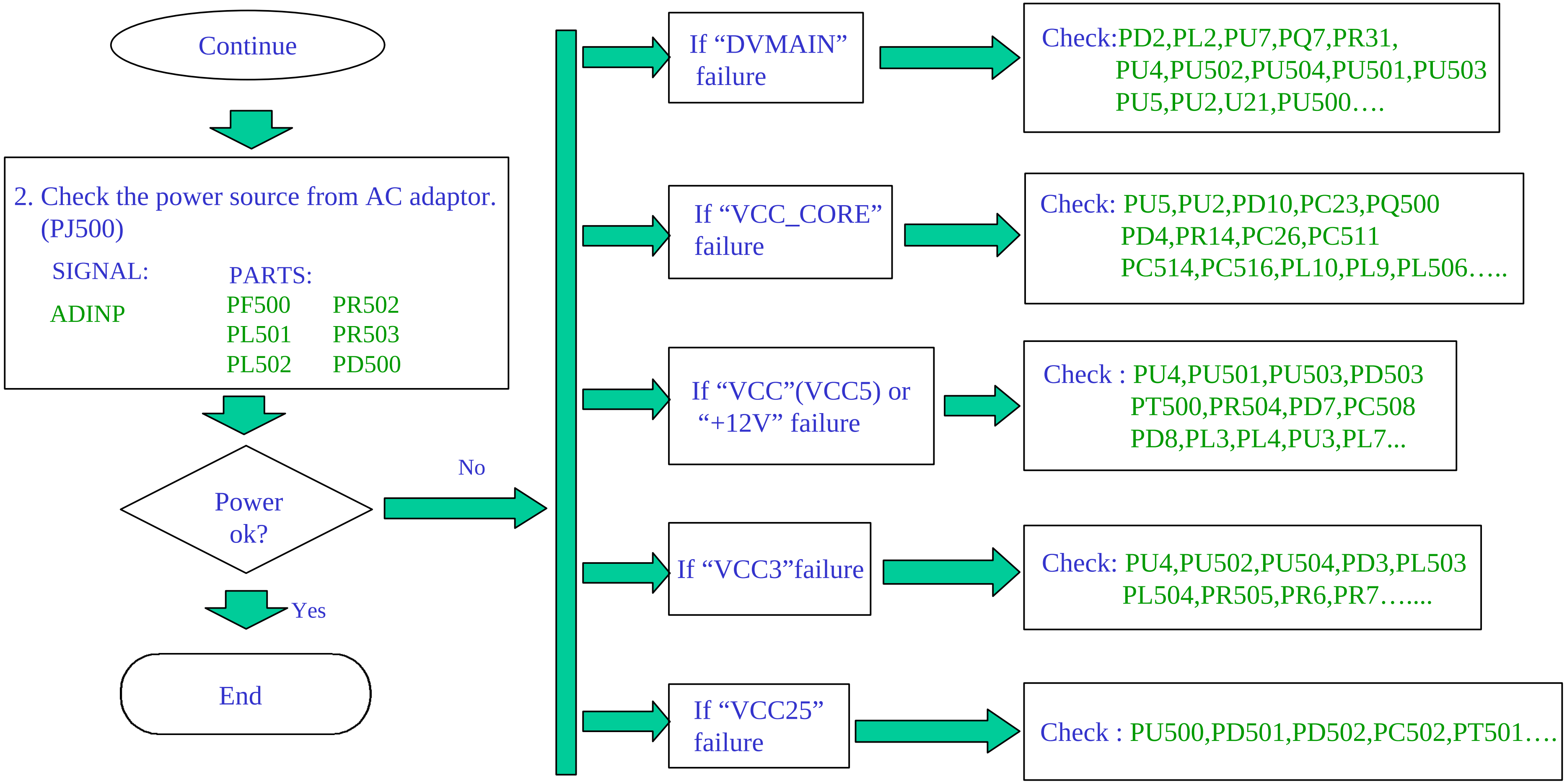
When the power button is pressed, nothing happens ,power indicator does not light up.



5133S M/B Maintenance

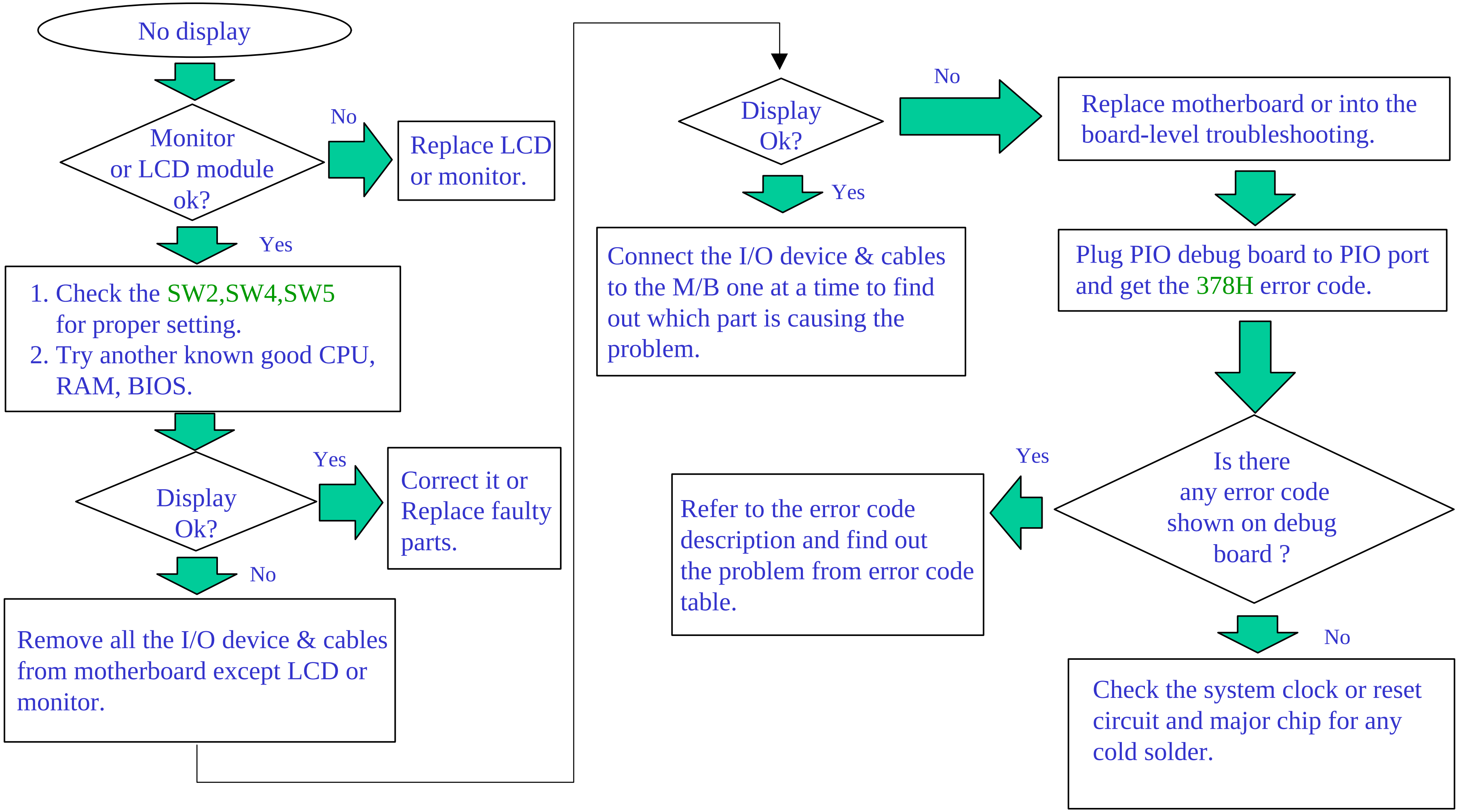
8.1 No power:

When the power button is pressed, nothing happens ,power indicator does not light up.



8.2 No display:

There is no display on both LCD and monitor.

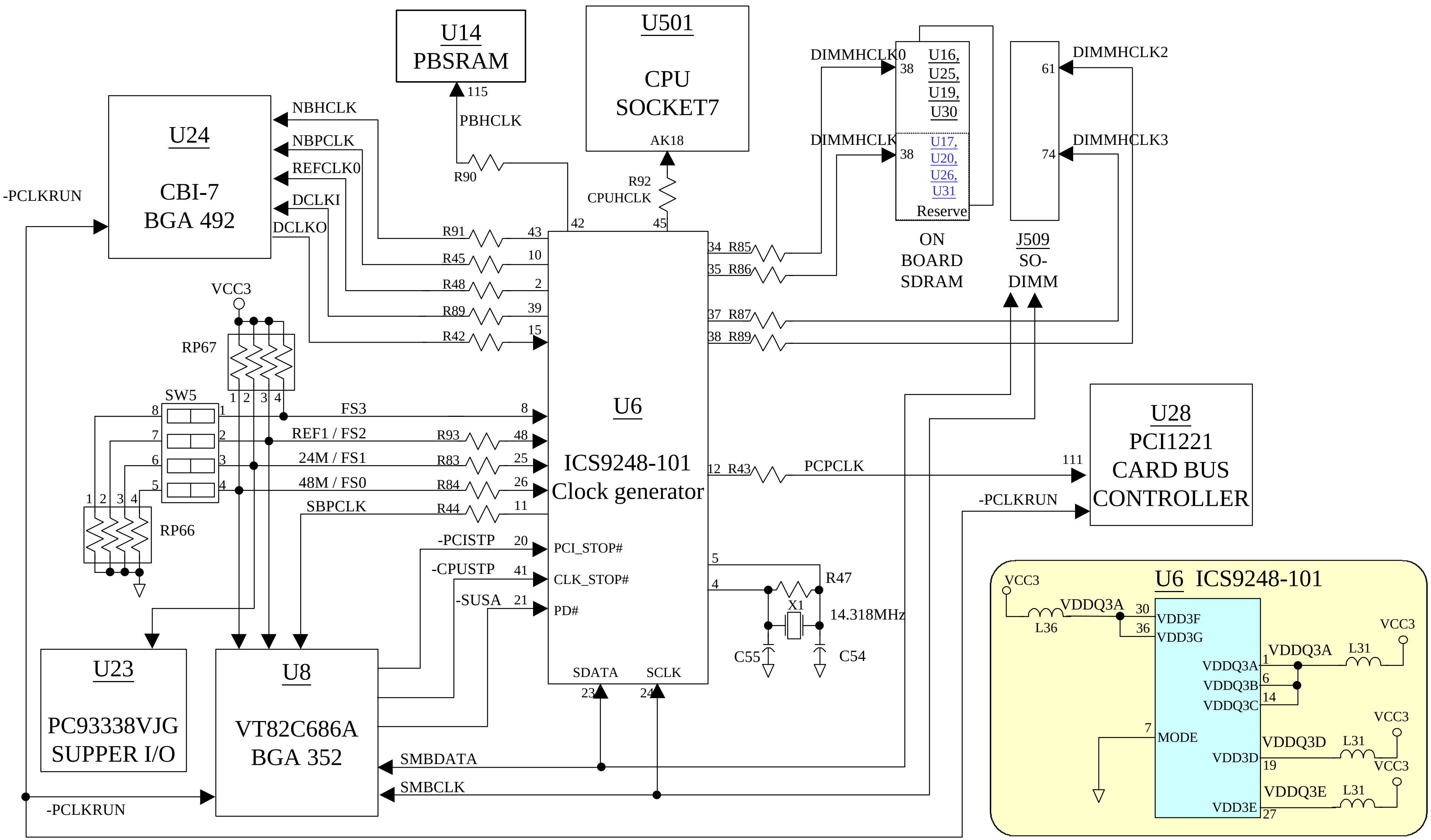


……Next page

5133S M/B Maintenance

8.2 No display:

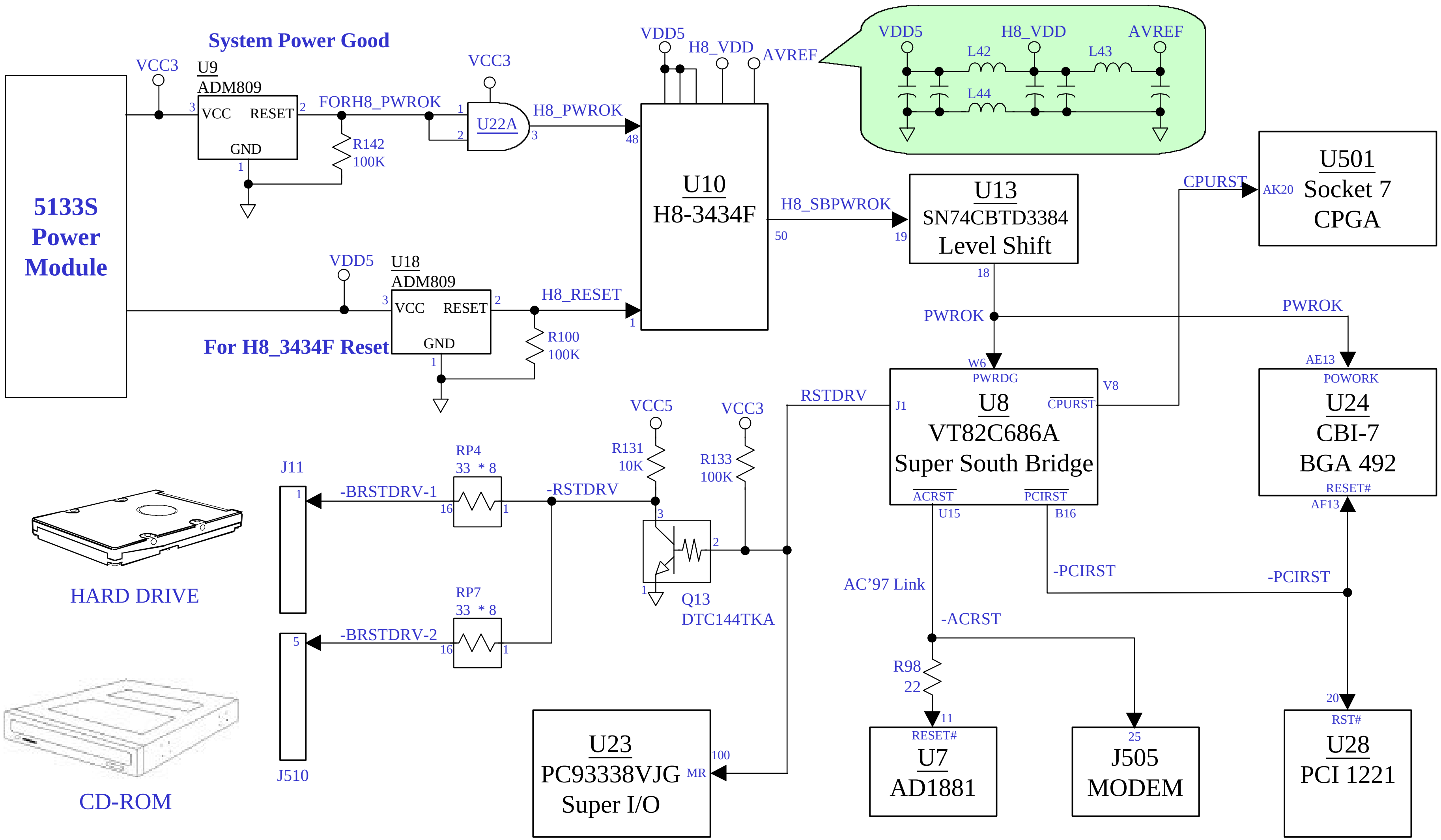
******System clock check ******



5133S M/B Maintenance

8.2 No display:

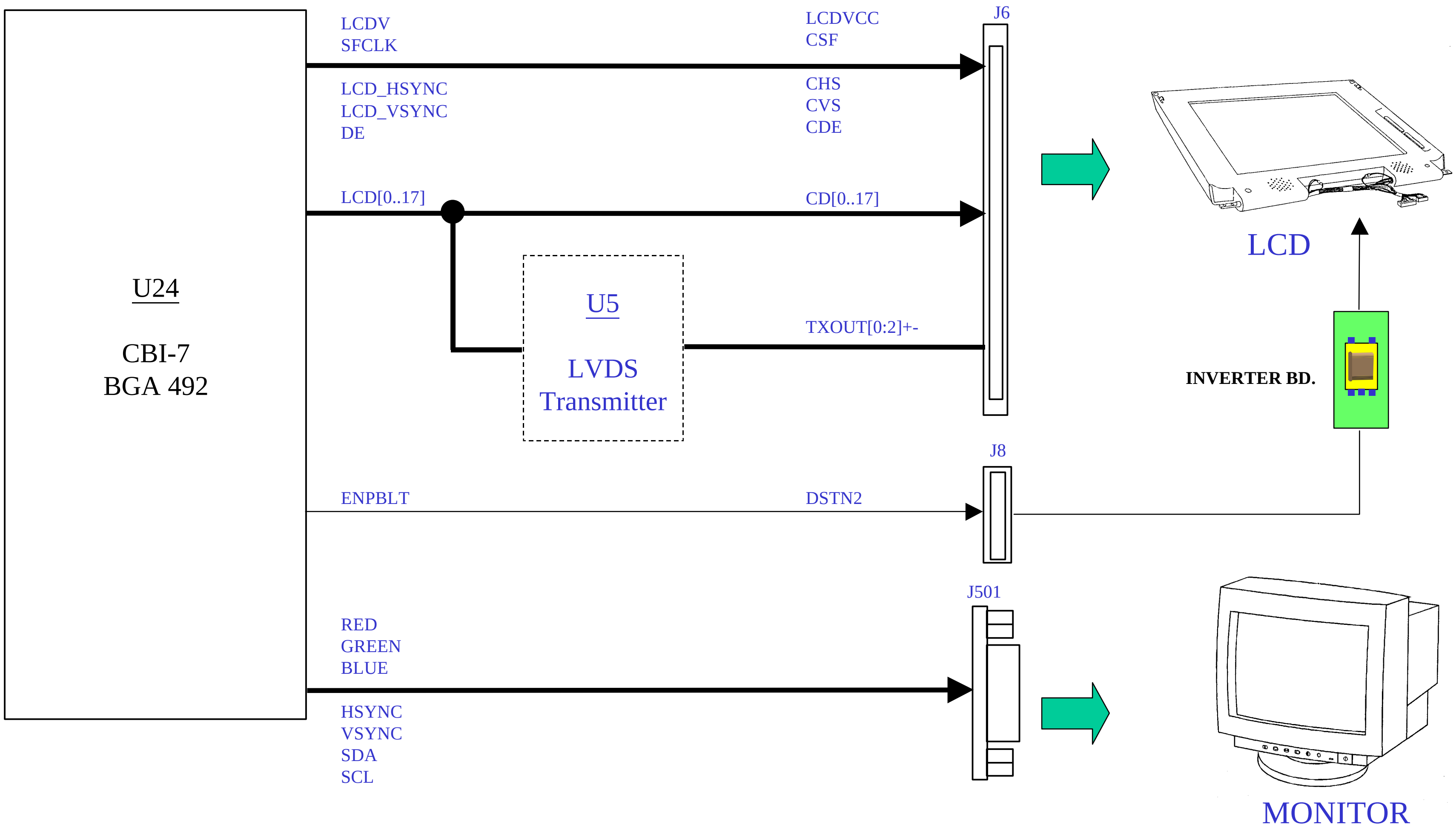
****** Reset system check ******



5133S M/B Maintenance

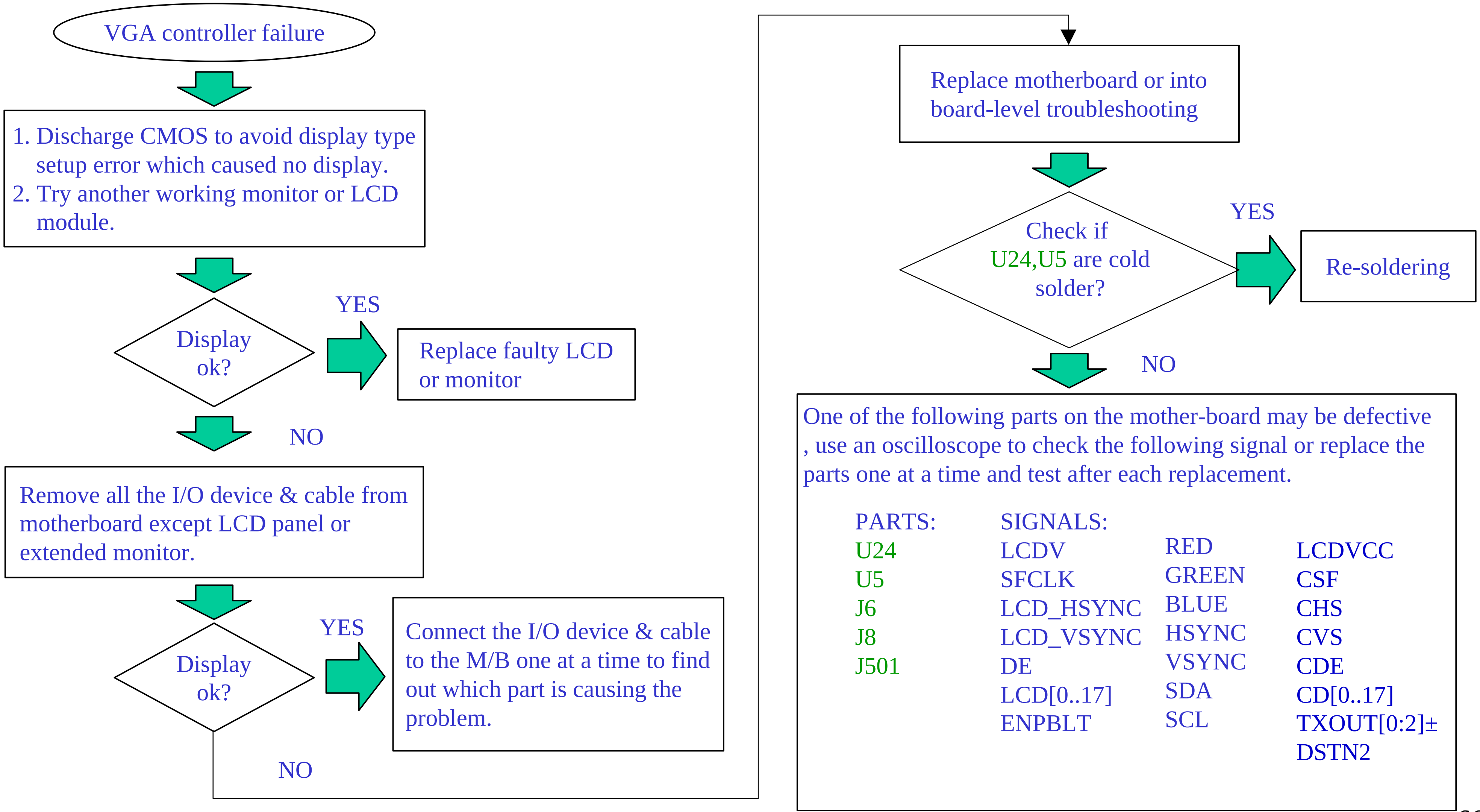
8.3 VGA controller failure

There is no display on both LCD and monitor although power-on-self-test is passed.



8.3 VGA controller failure

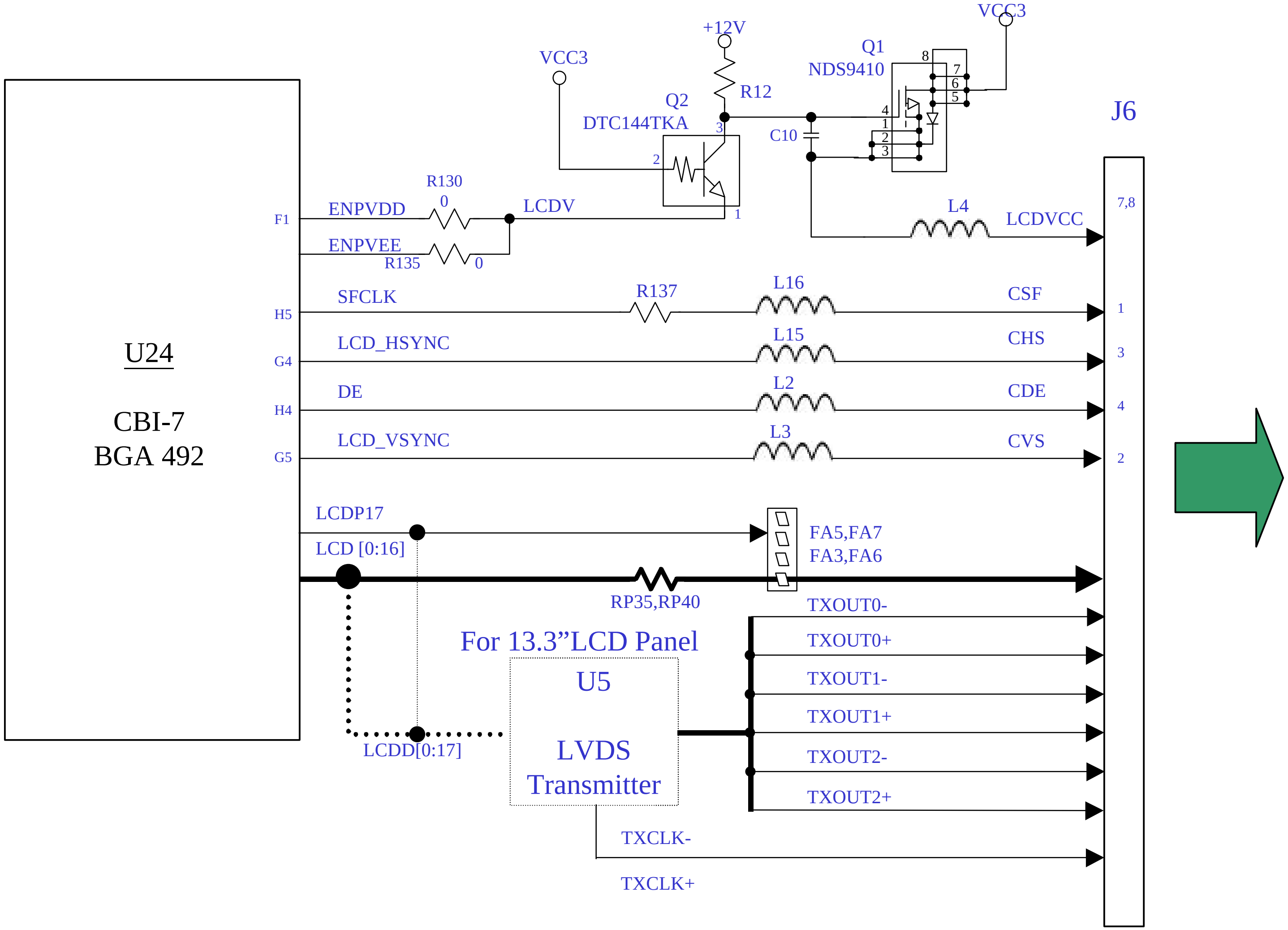
There is no display on both LCD and monitor although power-on-self-test is passed.

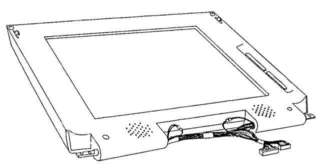


5133S M/B Maintenance

8.4 LCD no display

The LCD shows nothing or abnormal picture , but it is ok for external monitor.

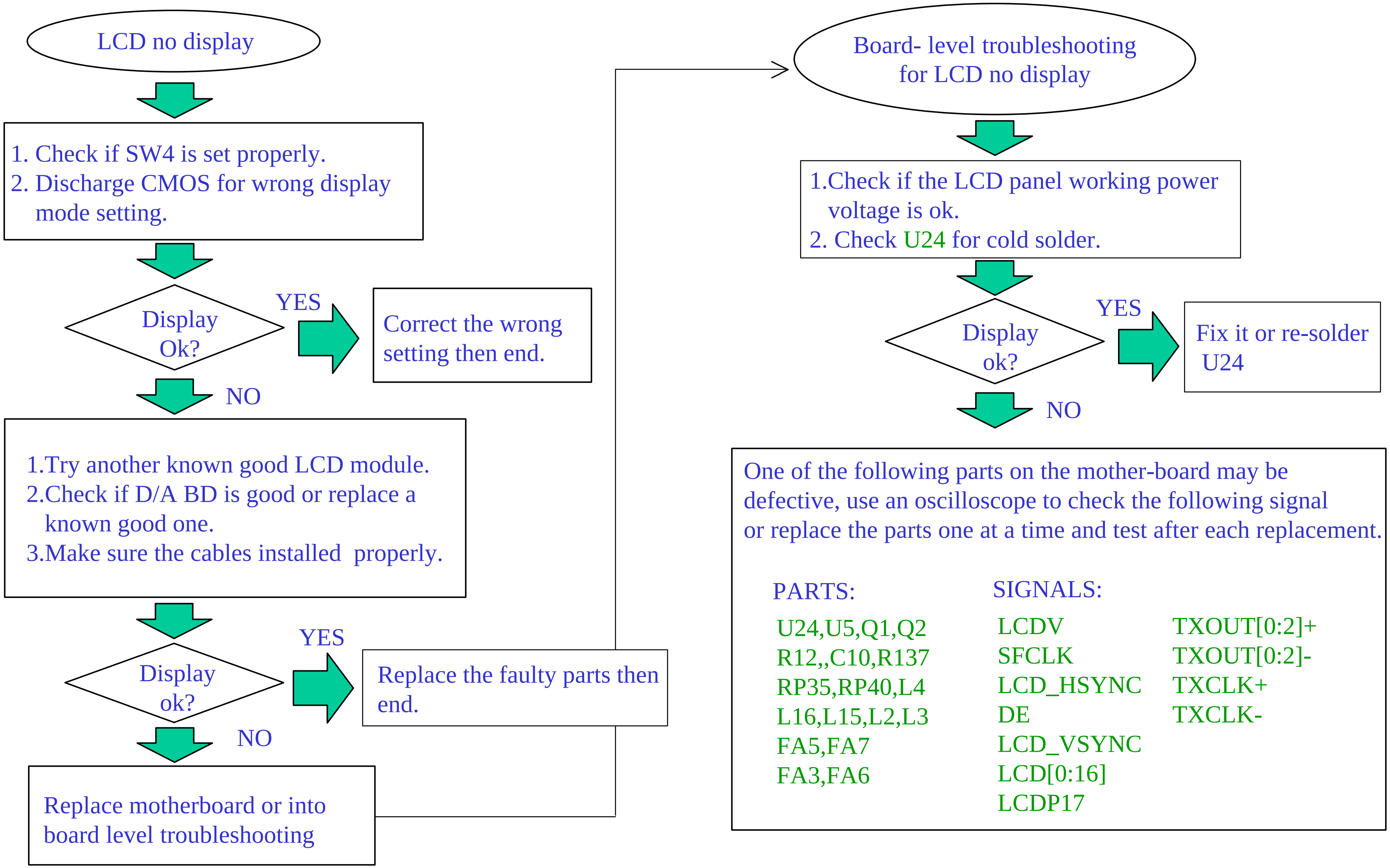




5133S M/B Maintenance

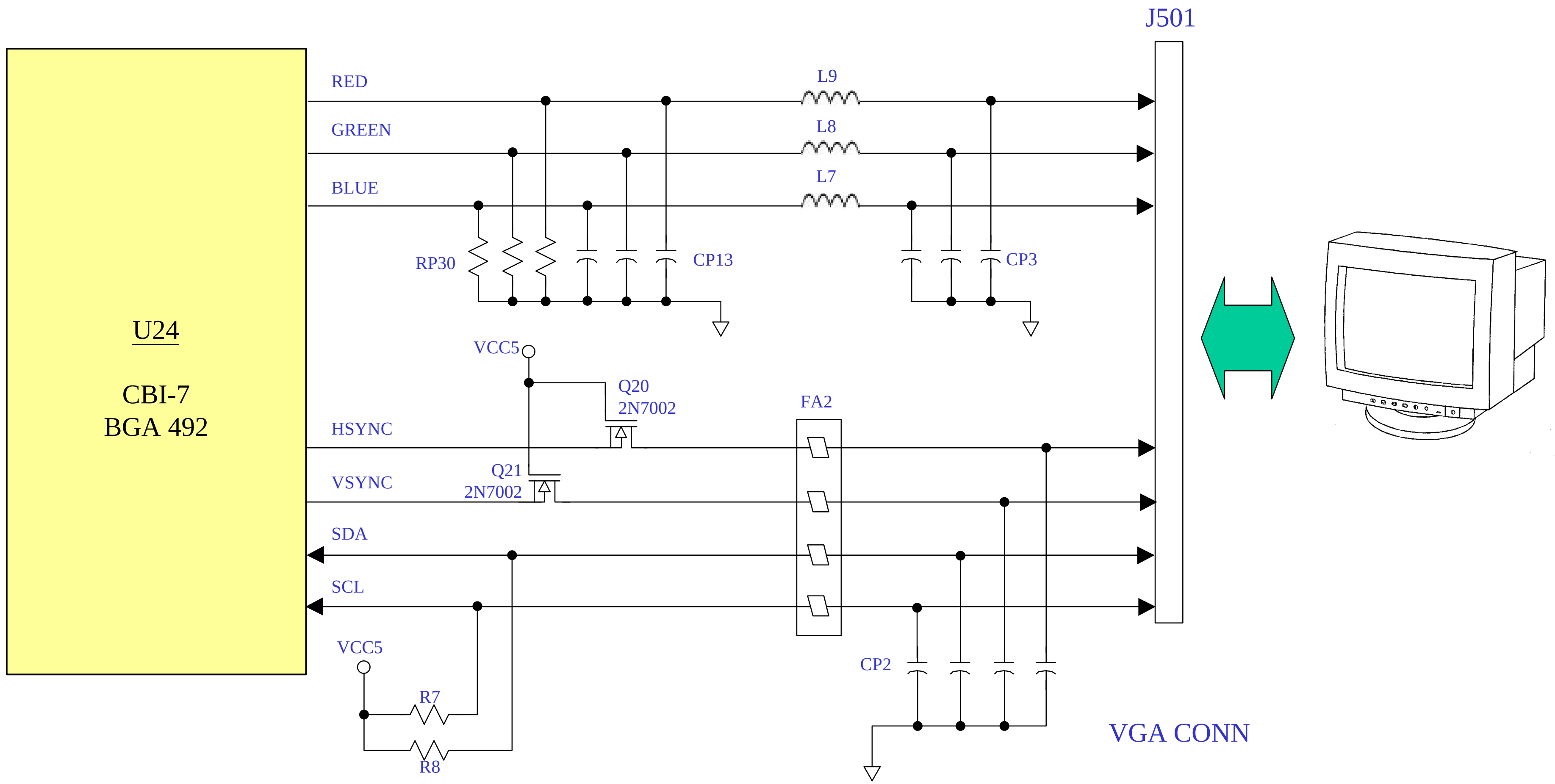
8.4 LCD no display

The LCD shows nothing or abnormal picture , but it is ok for external monitor.



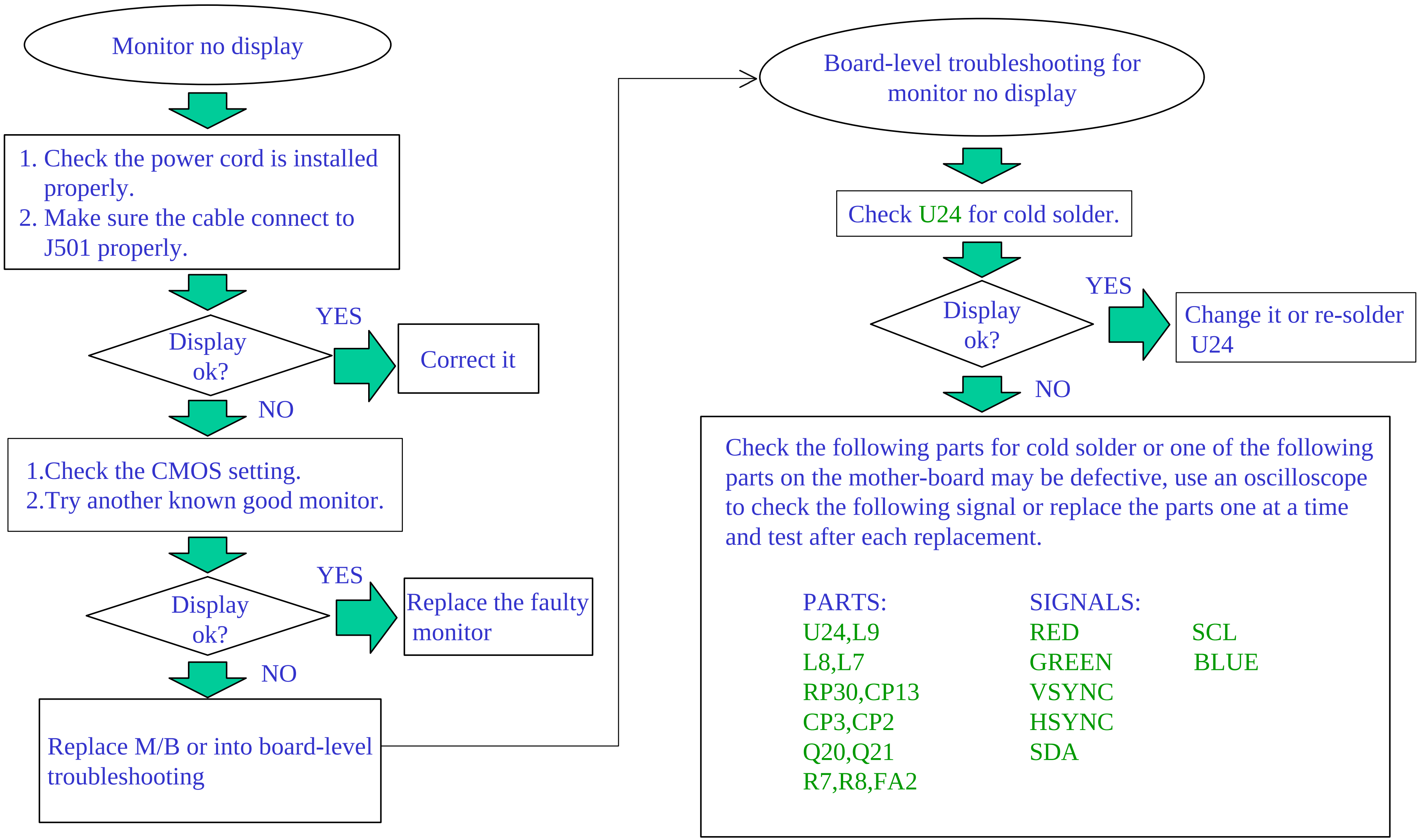
8.5 External monitor no display

The CRT monitor shows nothing or abnormal color, but it is ok for LCD.



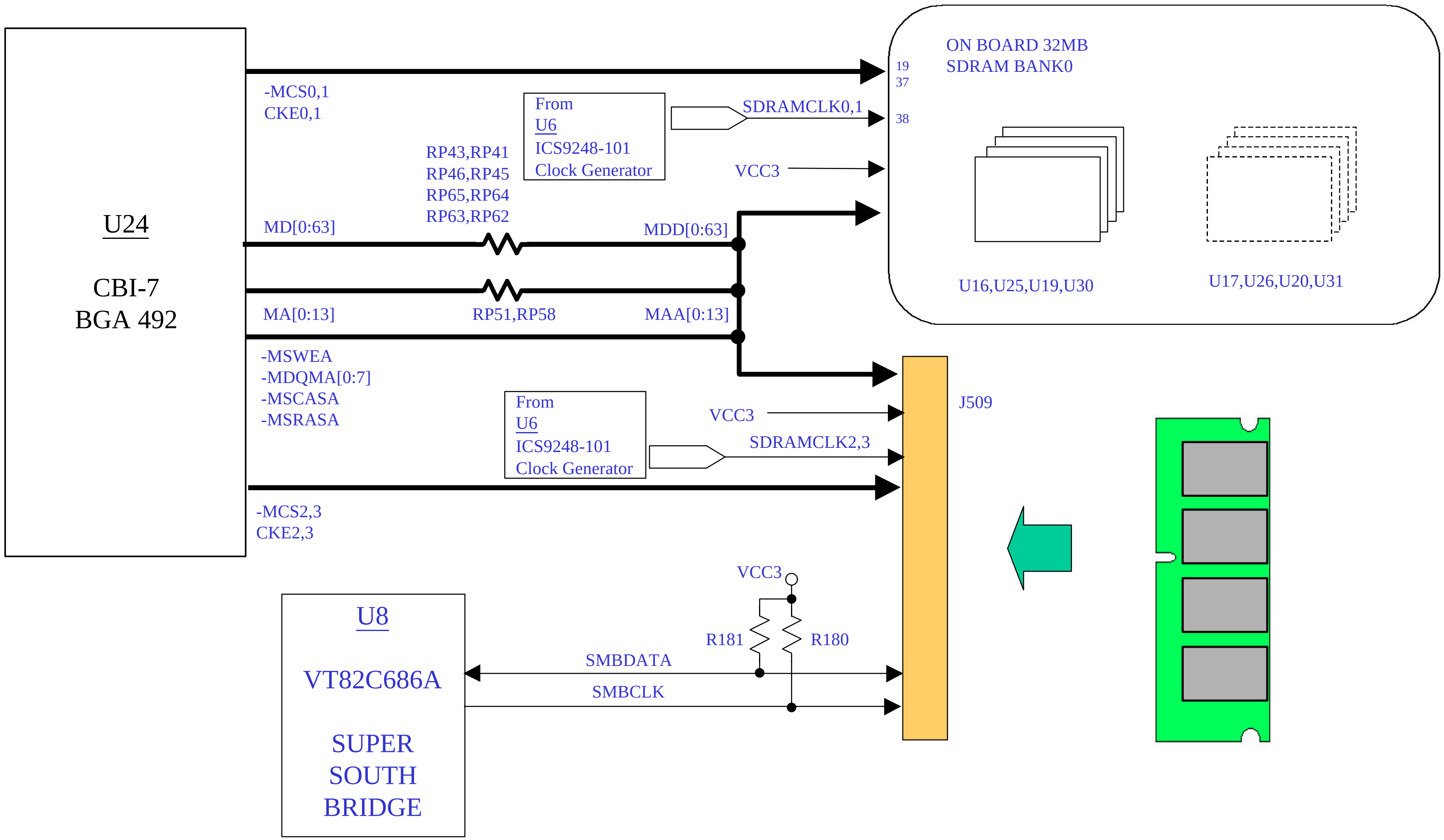
8.5 External monitor no display

The CRT monitor shows nothing or abnormal color, but it is ok for LCD.



8.6 Memory test error

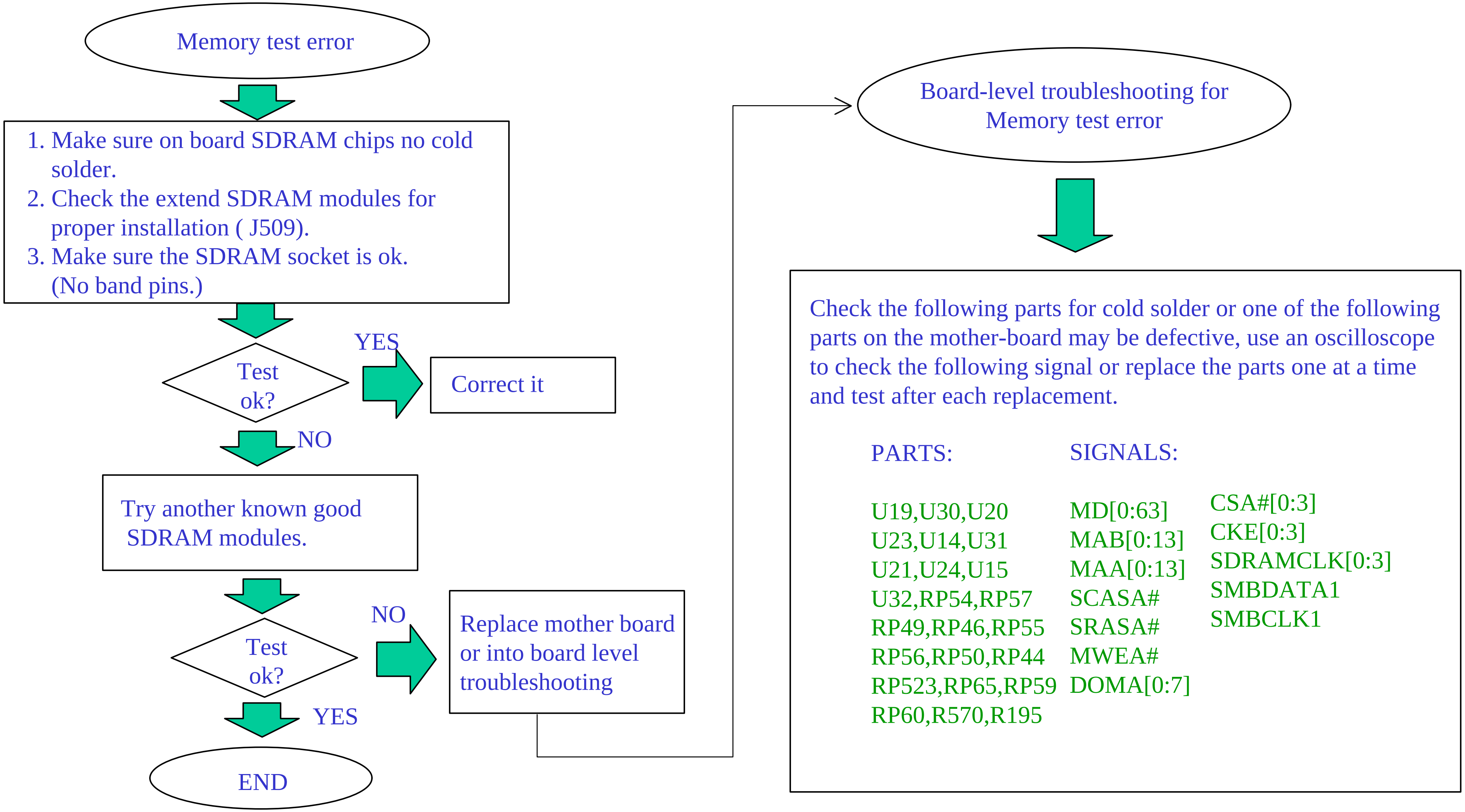
Either on board or extend SDRAM ,the error code shown on the PIO debug board is mean memory error and system hangs up.



5133S M/B Maintenance

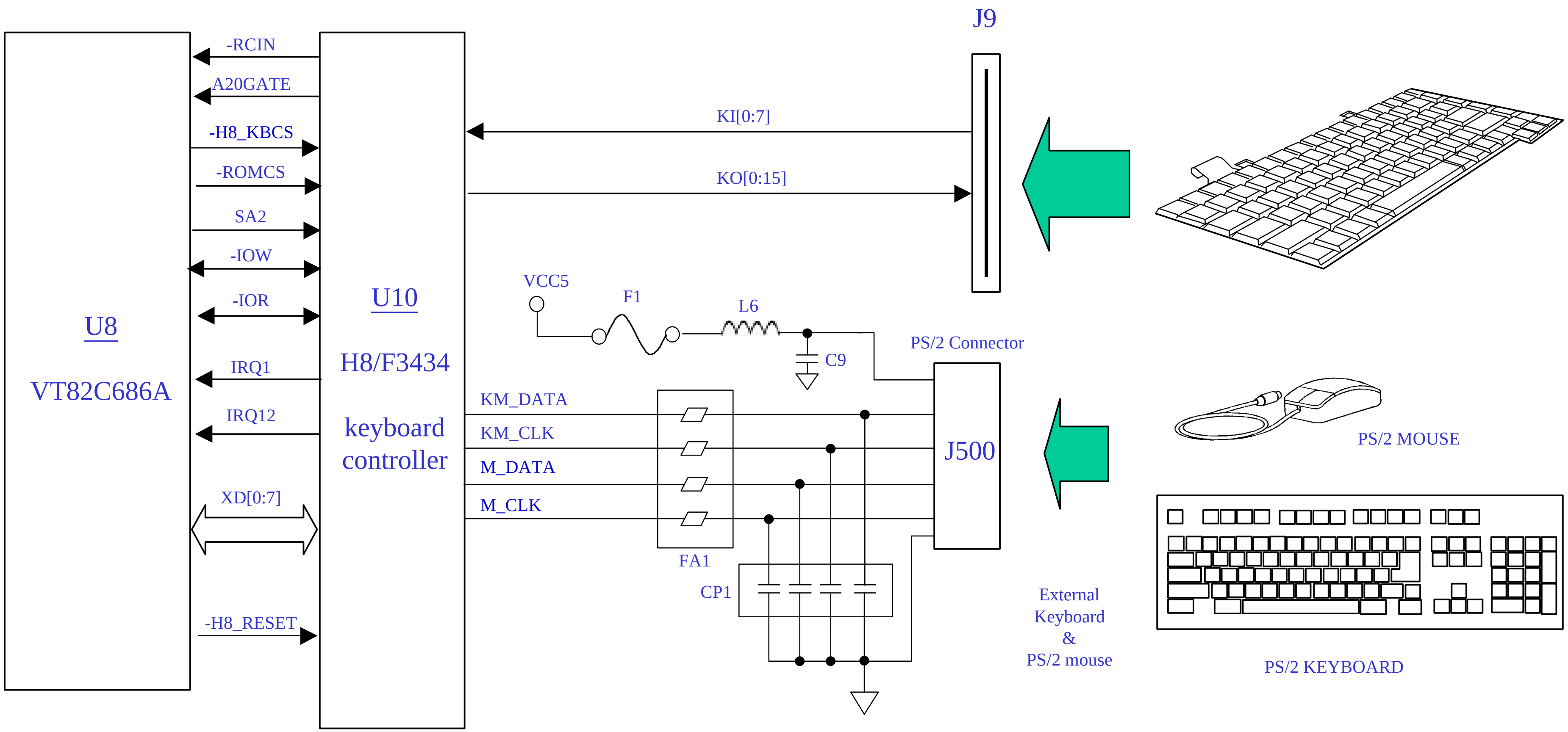
8.6 Memory test error

Either on board or extend SDRAM ,the error code shown on the PIO debug board is mean memory error and system hangs up.



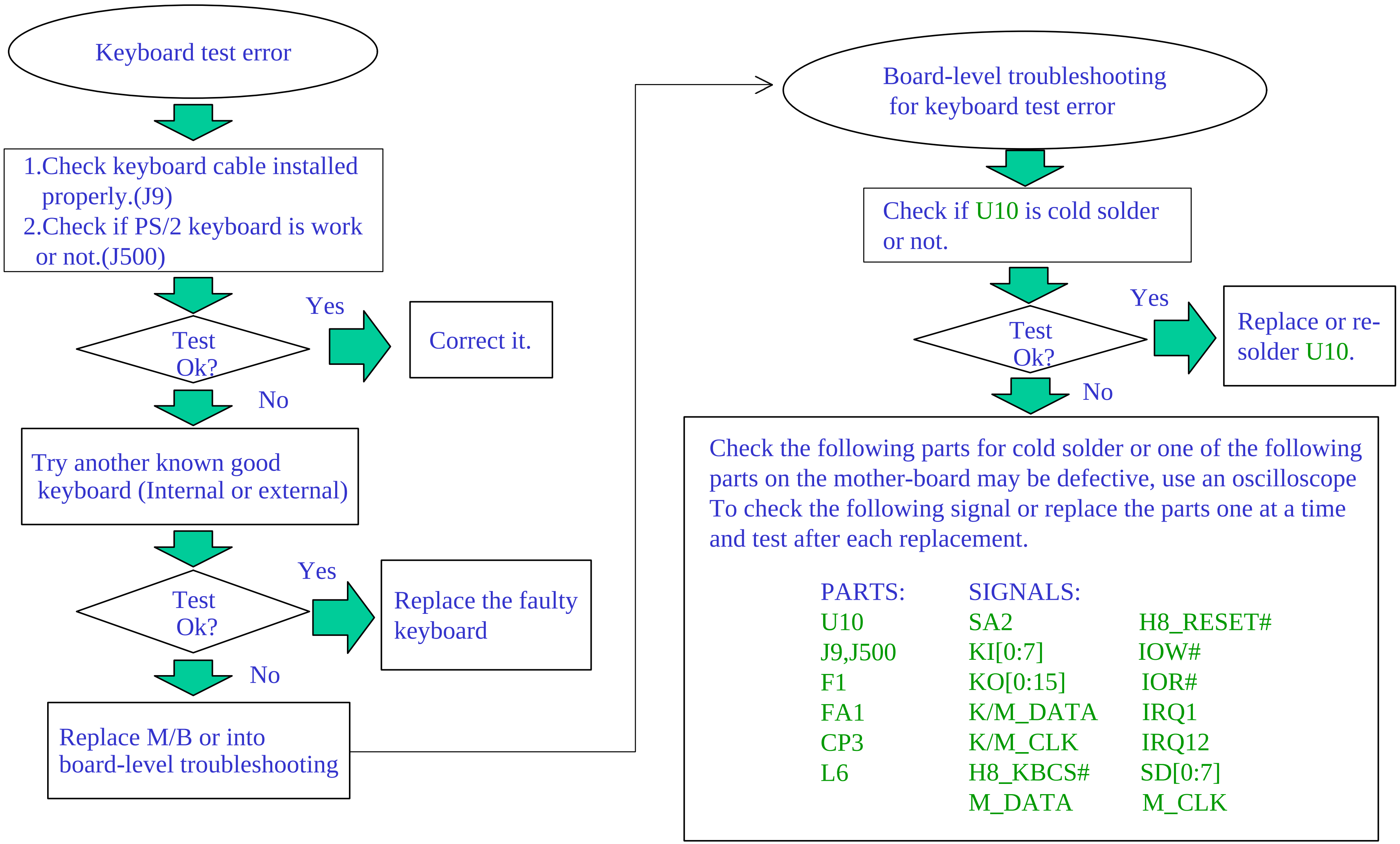
8.7 Keyboard test error

Error message of keyboard failure is shown or any key doesn't work.



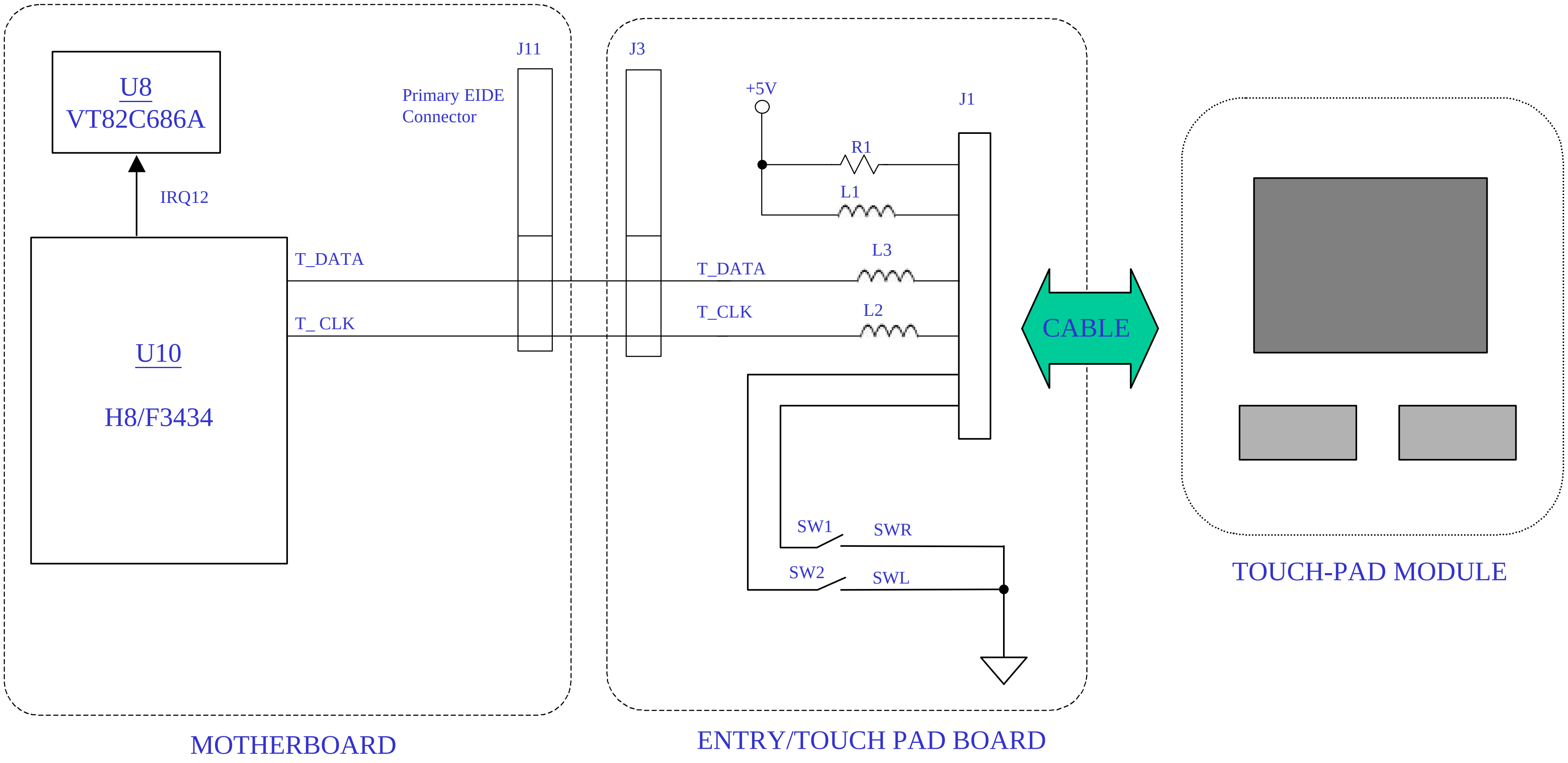
8.7 Keyboard test error

Error message of keyboard failure is shown or any key doesn’t work.



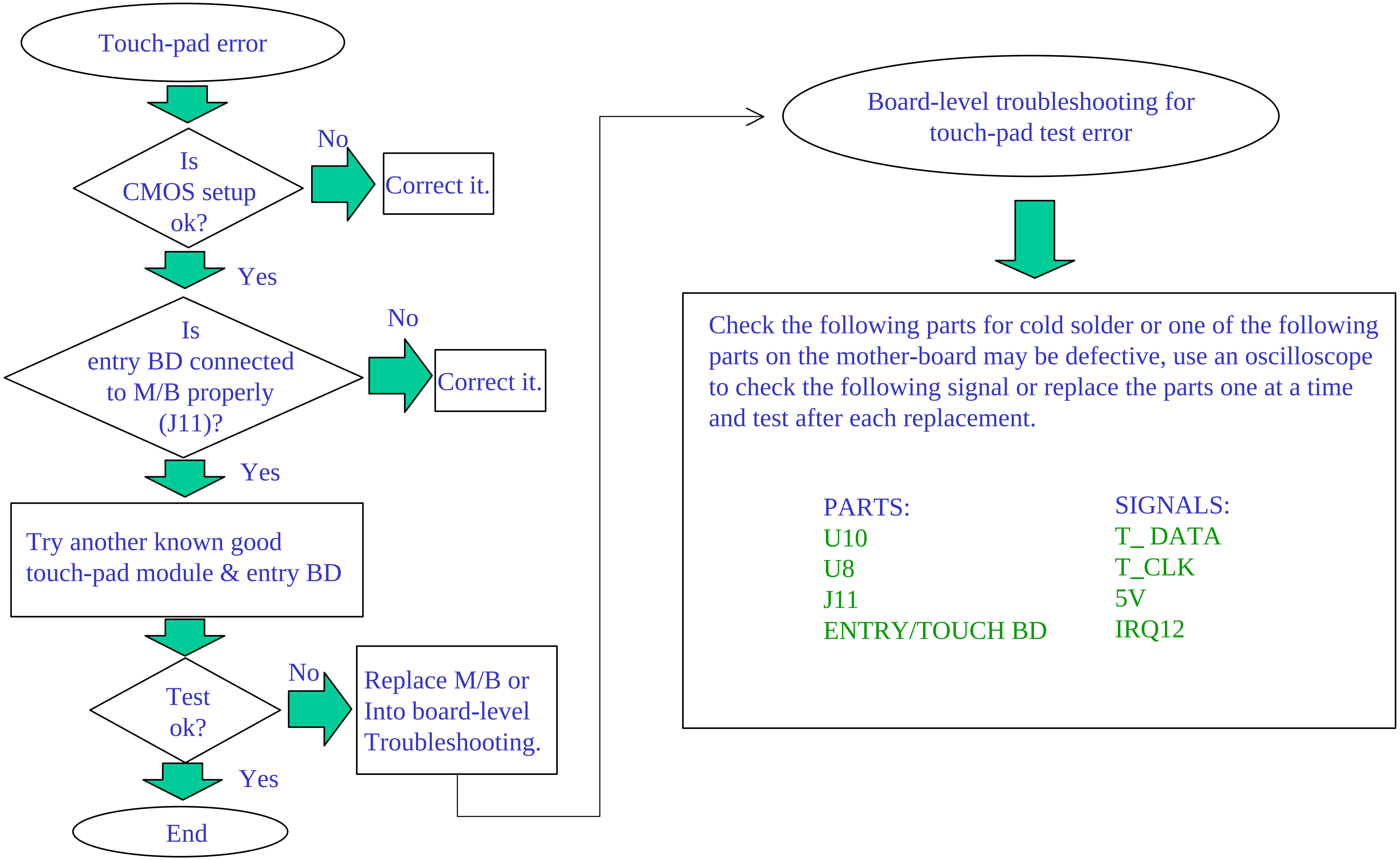
8.8 Track pad test error

An error message is shown when touch-pad is enabled.



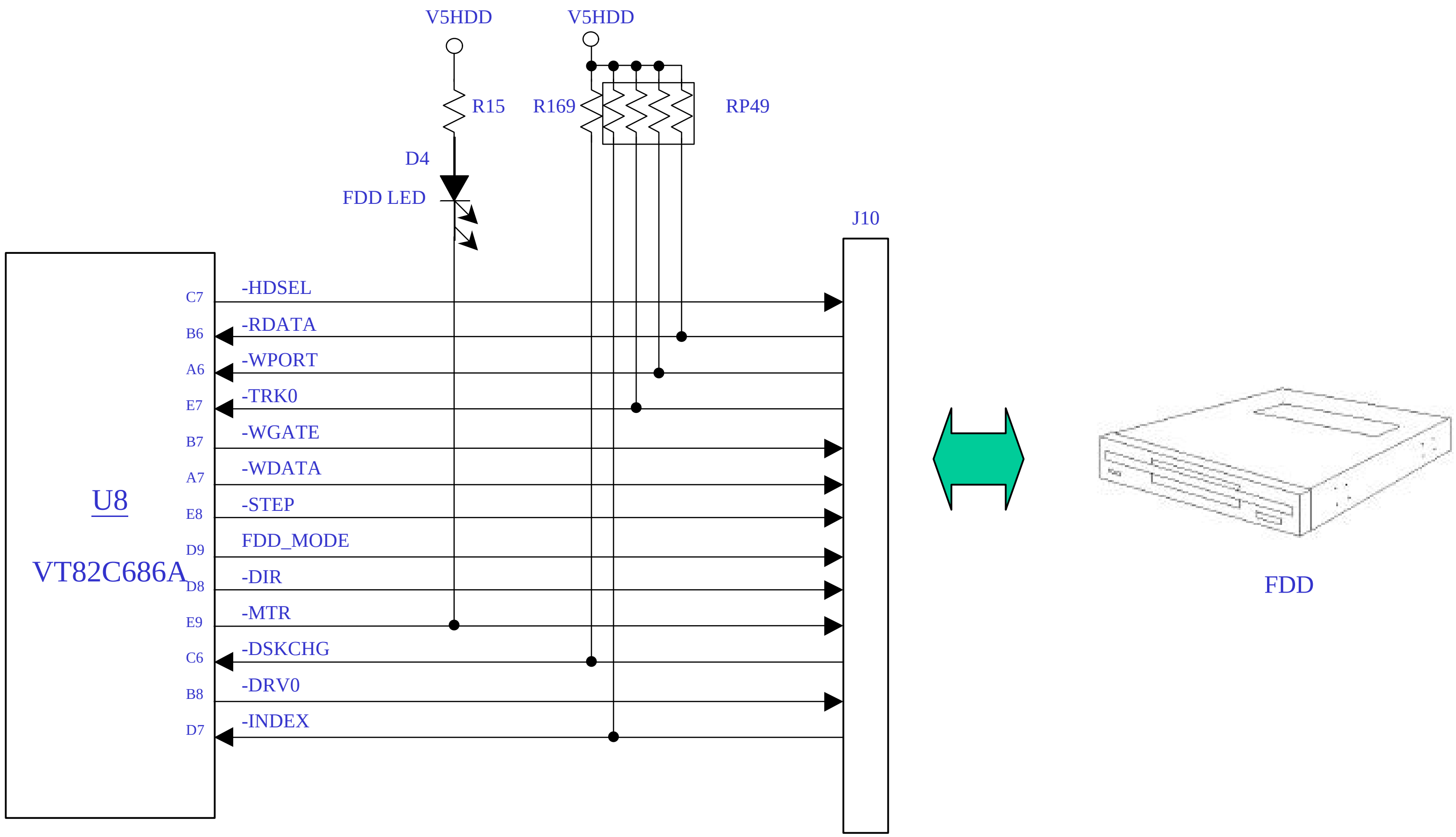
8.8 Track pad test error

An error message is shown when touch-pad is enabled.



8.9 Diskette drive test error

An error message is shown when reading/ writing data from/to diskette drive.



8.9 Diskette drive test error

An error message is shown when reading/ writing data from/to diskette drive.

Diskette drive test error

1. Try another known good boot diskette.
2. Check BIOS setup correctly.
3. Check J10 connect properly.

Re-boot ok?

Yes → Correct it.

No ↓

Try another known good floppy drive.

Re-boot ok?

Yes → Replace faulty parts.

No ↓

Replace M/B or go into board-level troubleshooting

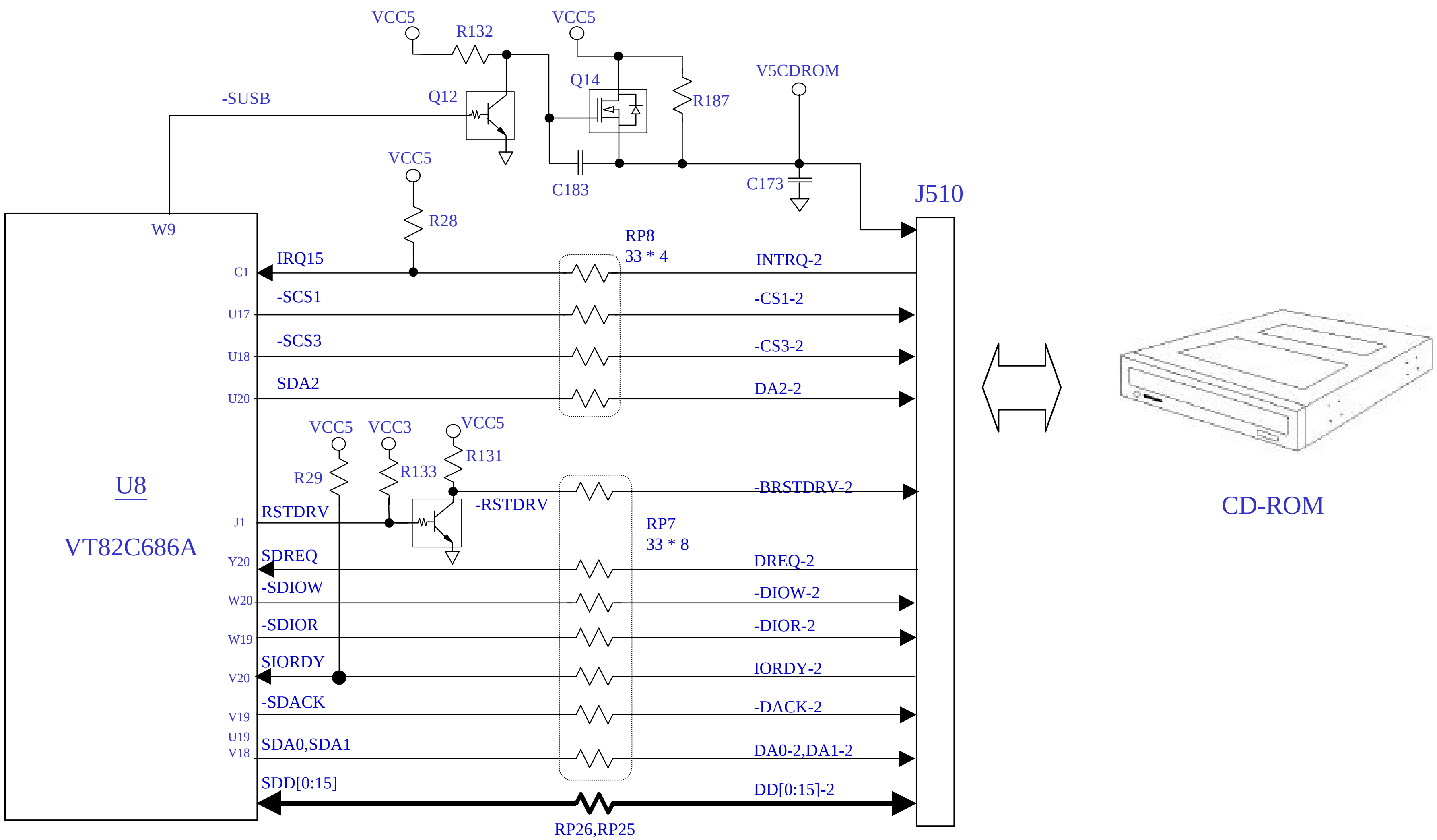
Board-level troubleshooting for touch-pad test error

Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

PARTS:	SIGNALS:	
U8	V5HDD	-STEP
J10	-HDSEL	FDD_MODE
RP49	-RDATA	-DIR
R15,R169	-WPORT	-MTR
D4	-TRK0	-DSKCHG
	-WGATE	-DRV0
	-WDATA	-INDEX

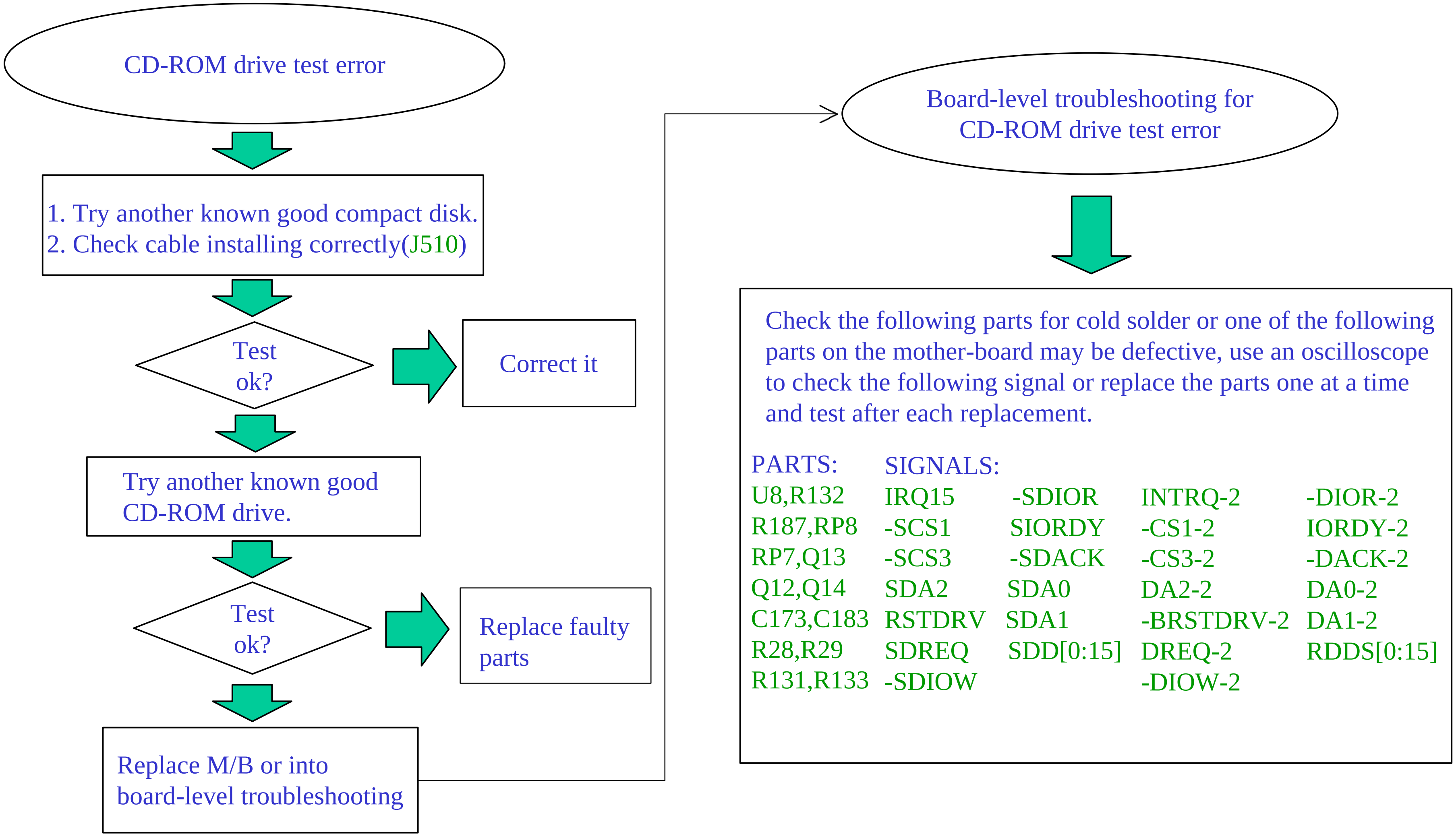
8.10 CD-ROM drive test error

An error message is shown when reading data from CD-ROM drive.



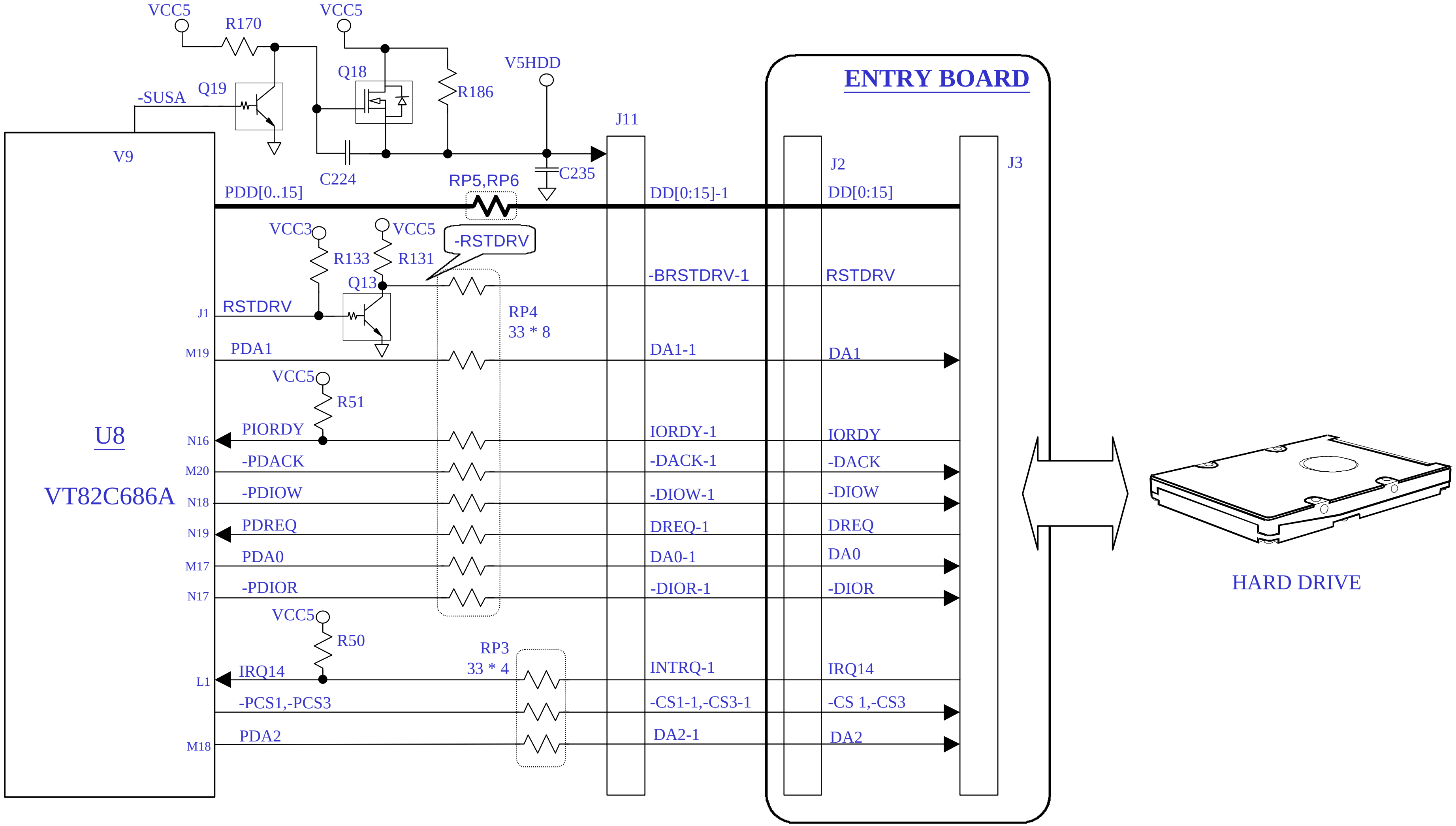
8.10 CD-ROM drive test error

An error message is shown when reading data from CD-ROM drive.



8.11 Hard drive test error

Either an error message is shown ,or the driver motor continues spinning ,while reading data is from or writing data is to hard drive.



8.11 Hard drive test error

Either an error message is shown ,or the driver motor continues spinning ,while reading data is from or writing data is to hard drive.

Hard drive test error

1. Check if HDD installed properly. (On entry BD J3)
2. Check if entry BD installed to M/B properly. (on M/B J11)
3. Check CMOS HDD setting.

Re_boot ok?

Yes → Correct it.

No ↓

1. Try another known good HDD.
2. Try another known good entry board.

Re_boot ok?

Yes → Replace the faulty part.

No ↓

Replace mother BD or into board-level troubleshooting.

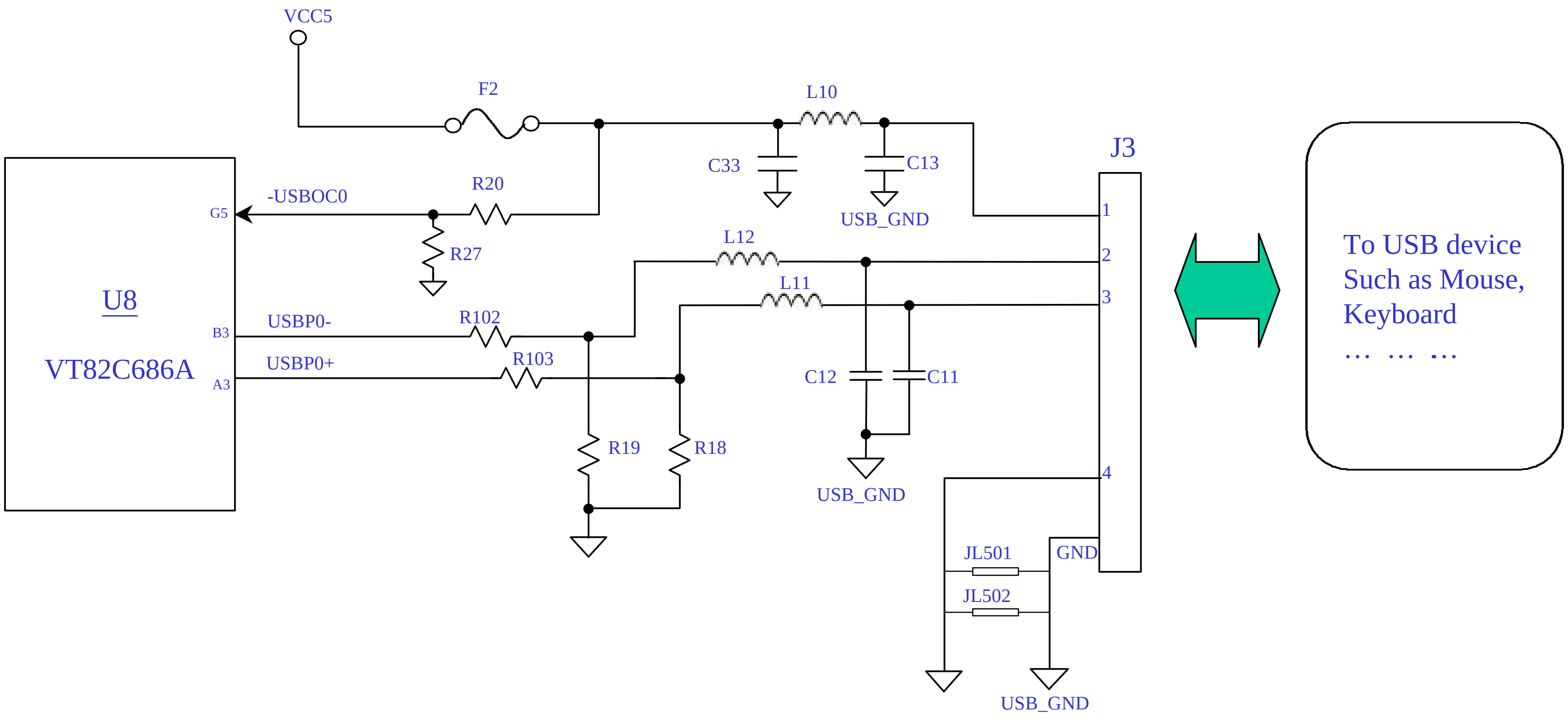
→ Board-level troubleshooting for Hard drive test error

Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope To check the following signal or replace the parts one at a time and test after each replacement.

PARTS:	SIGNALS:	
U8,Q18,Q19	PDD[0:15]	PDREQ
R170,R186	RSTDRV	PDIOR
C224,C235	PDA[0:2]	IRQ14
R131,R133	PIORDY	-PCS1,-PCS3
RP5,RP6	-PDACK	
RP3,RP4	PDIOW	
Q13,R51	-SUSA	
J11	VCC5	
ENTRY BD	V5HDD	

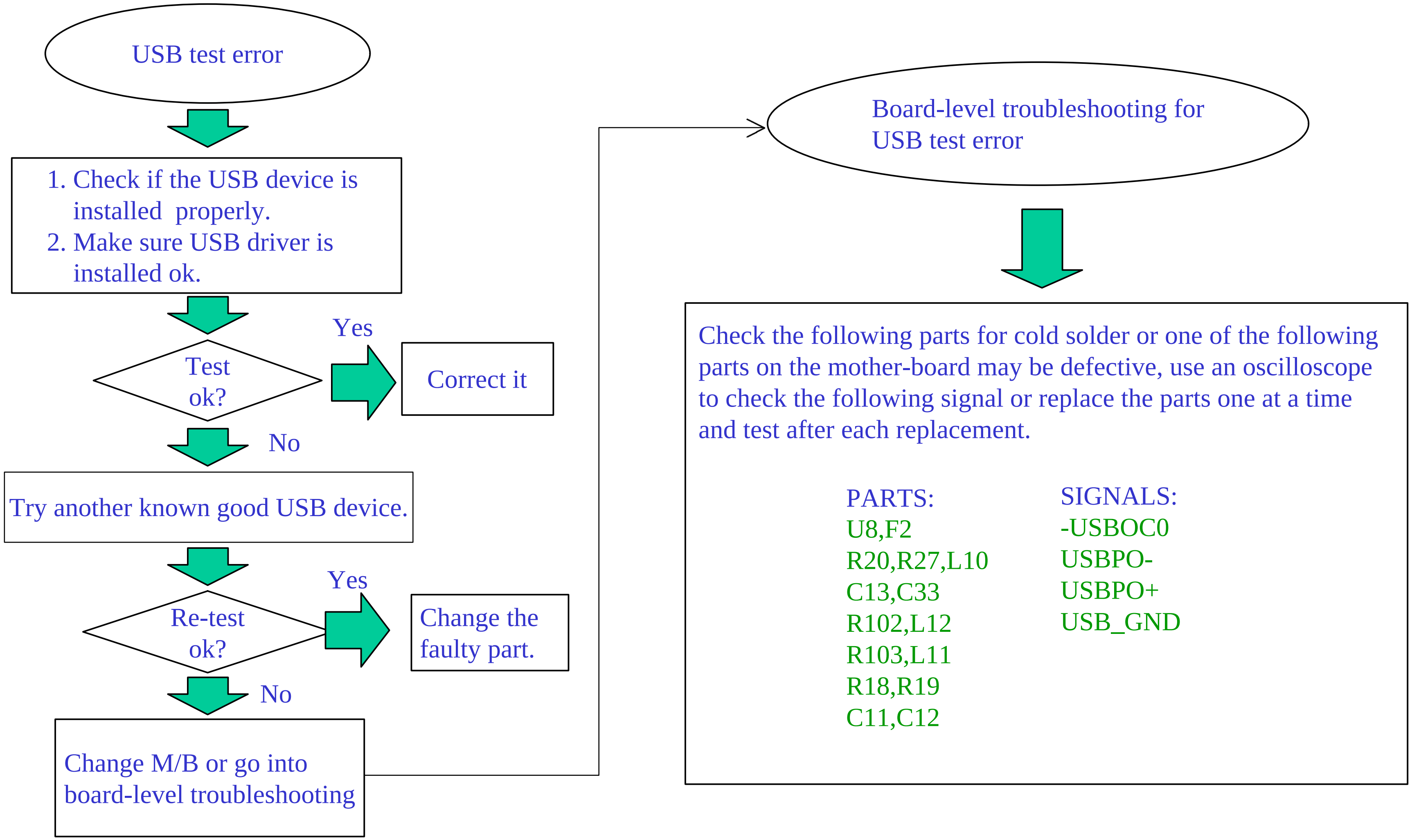
8.12 USB port test error

An error occurs when a USB I/O device is installed.



8.12 USB port test error

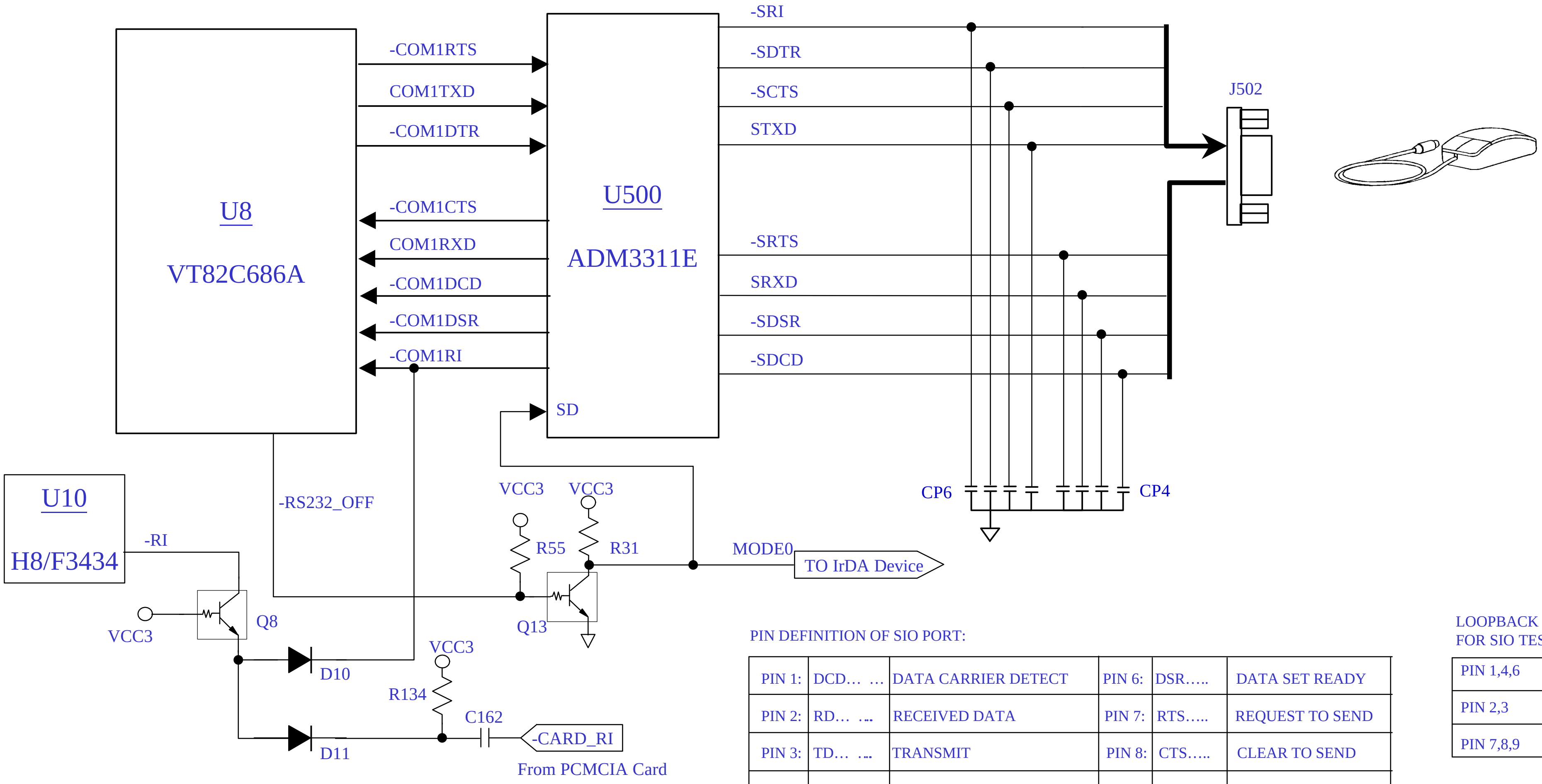
An error occurs when a USB I/O device is installed.



5133S M/B Maintenance

8.13 SIO port test error

An error occurs when a mouse or other I/O device is installed.



PIN DEFINITION OF SIO PORT:

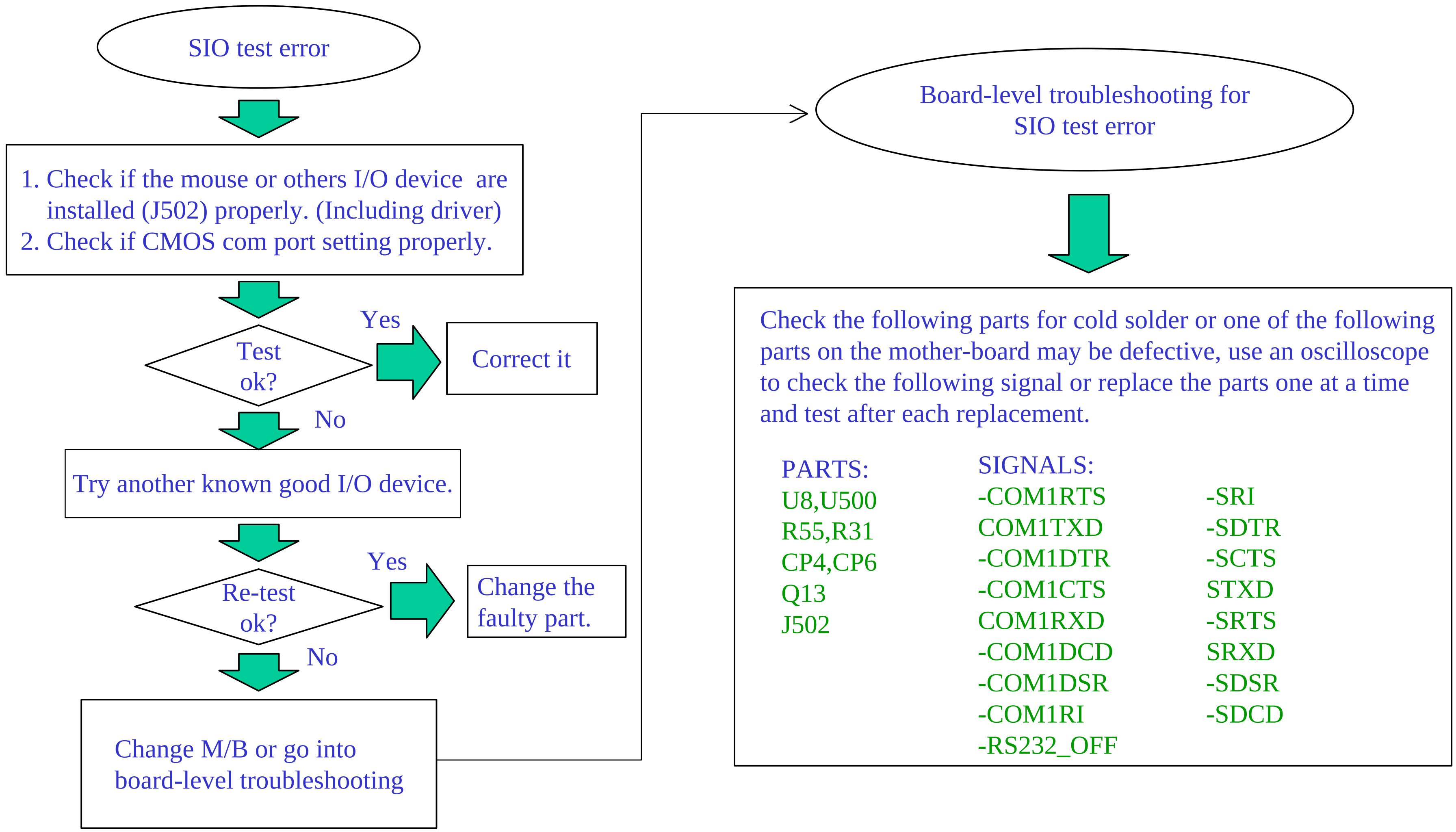
PIN 1:	DCD… …	DATA CARRIER DETECT	PIN 6:	DSR…..	DATA SET READY
PIN 2:	RD… …	RECEIVED DATA	PIN 7:	RTS…..	REQUEST TO SEND
PIN 3:	TD… …	TRANSMIT	PIN 8:	CTS…..	CLEAR TO SEND
PIN 4:	DTR… …	DATA TERMINAL READY	PIN9:	RI… …	RING INDICATOR
PIN 5:	SG… …	SIGNAL GROUND			

LOOPBACK CONNECTOR
FOR SIO TEST

PIN 1,4,6	SHORT
PIN 2,3	SHORT
PIN 7,8,9	SHORT

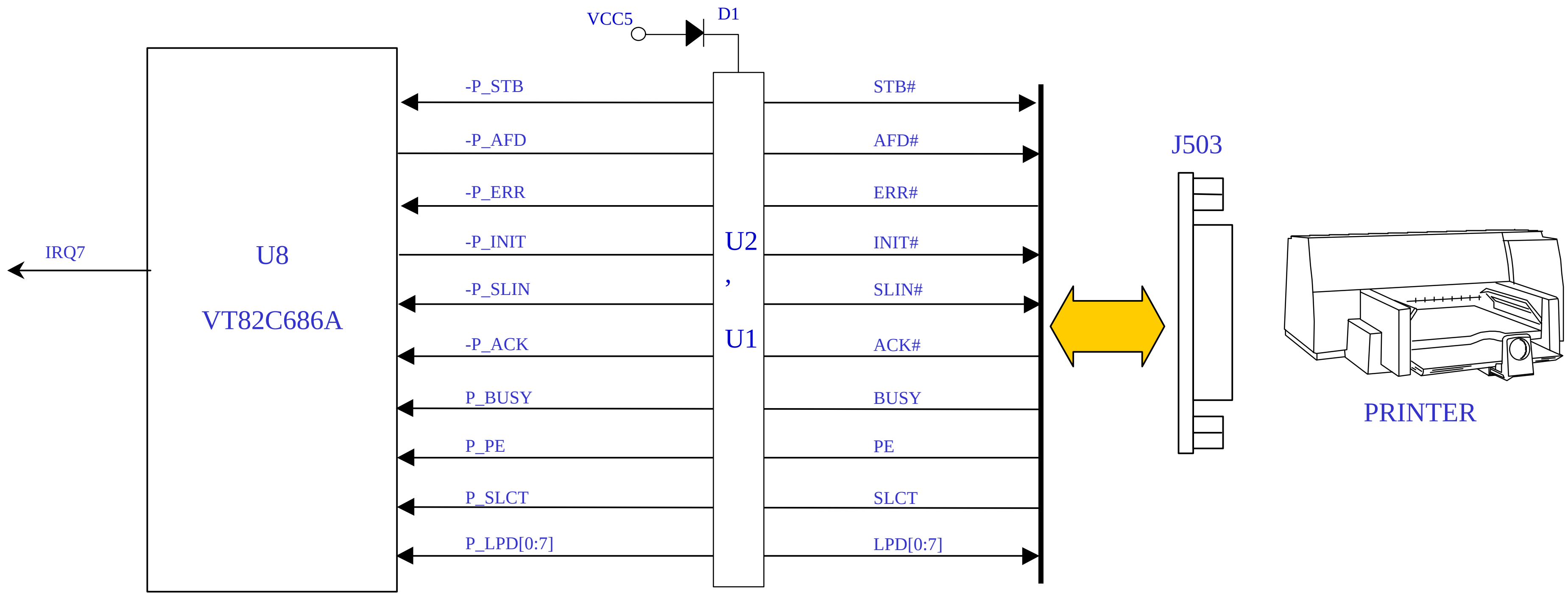
8.13 SIO port test error

An error occurs when a mouse or other I/O device is installed.



8.14 PIO port test error

When a print command is issued, printer prints nothing or garbage.



PIN DEFINITION OF PIO PORT

PIN 1	STB	STROBE SIGNAL	PIN 14	AFD	AUTO LINE FEED
PIN 2-9	D0 - D7	PARALLEL PORT DATA BUS D0 TO D7	PIN 15	ERR	ERROR AT PRINTER
PIN 10	ACK	ACKNOWLEDGE HANDSHANK	PIN 16	INIT	INITIATE OUTPUT
PIN 11	BUSY	BUSY SIGNAL	PIN 17	SLIN	PRINTER SELECT
PIN 12	PE	PAPER END	PIN 18-25:	SIGNAL GROUND	
PIN 13	SLCT	PRINTER SELECTED			

LOOPBACK CONNECTOR FOR PIO TEST:

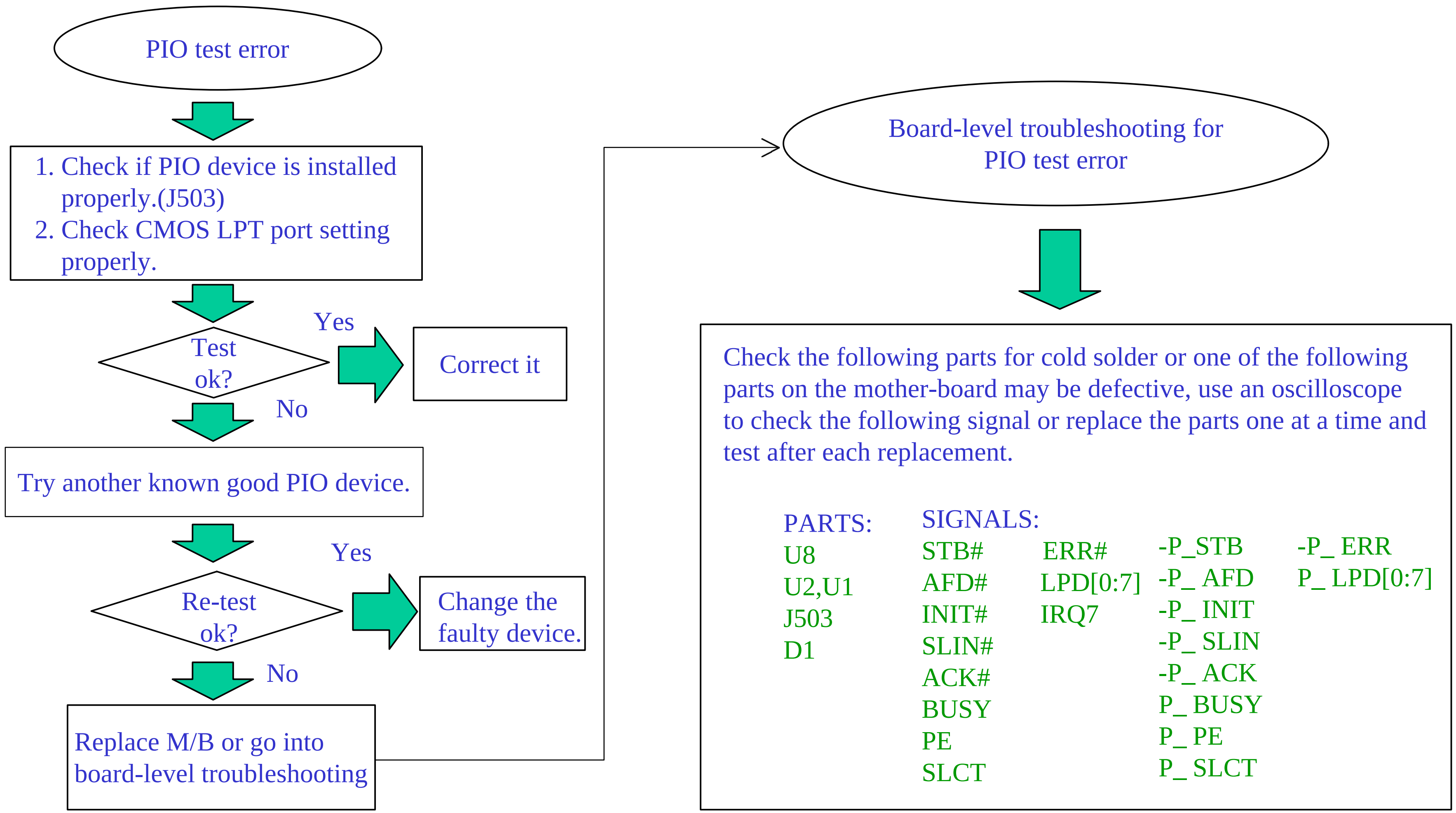
PIN 1, 13	SHORT	PIN 10,16	SHORT
PIN 2, 15	SHORT	PIN 11,17	SHORT
PIN 12, 14	SHORT		

LOOPBACK CONNECTOR FOR EPP TEST:

PIN 1, 2, 4, 6, 8	SHORT
PIN 3, 5, 7, 9, 16	SHORT
PIN 18, 19, 20, 21, 22, 23, 24, 25	SHORT

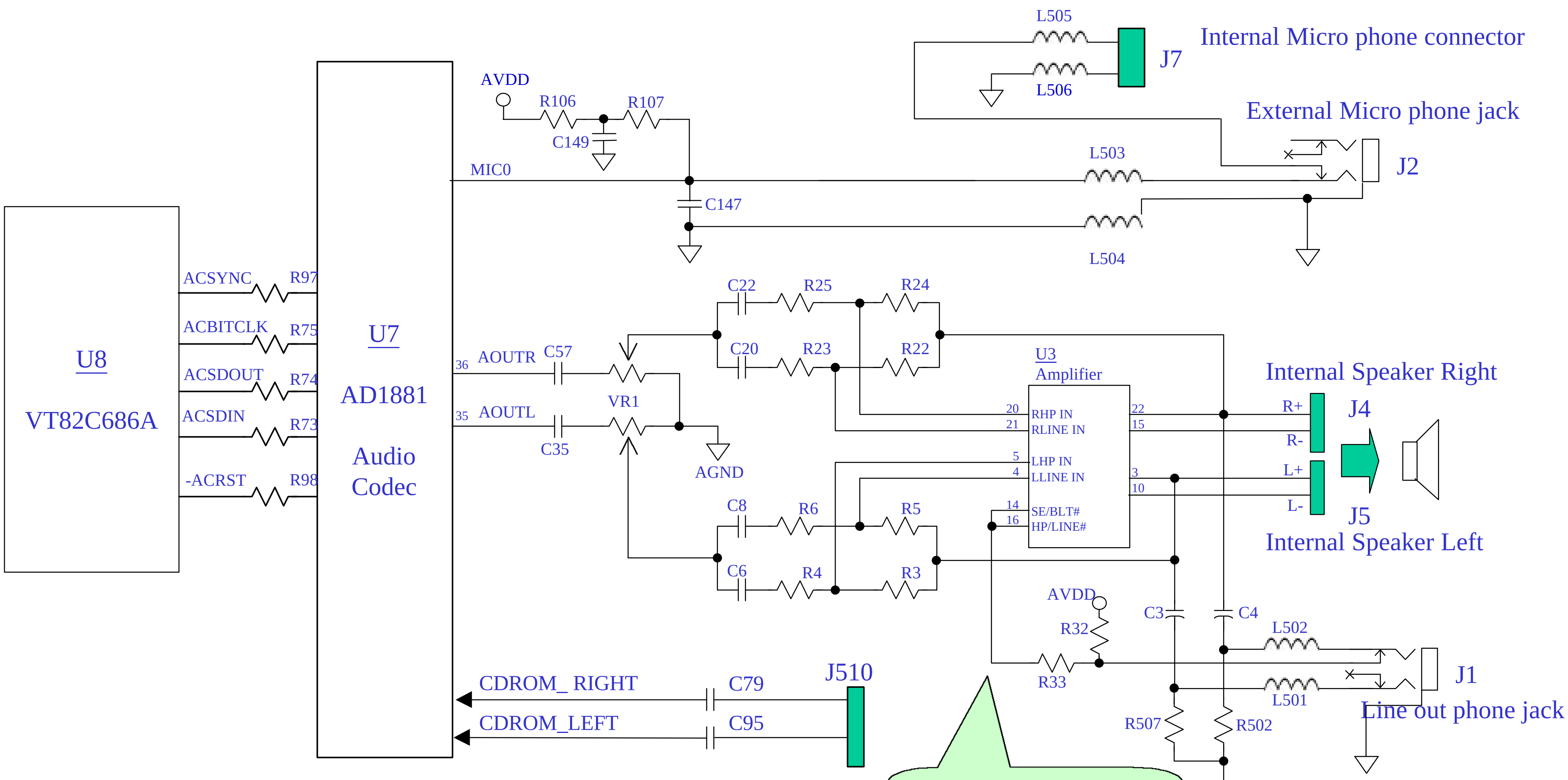
8.14 PIO port test error

When a print command is issued, printer prints nothing or garbage.



8.15 Audio failure

No sound from speaker after audio driver is installed.



PHONE JACK	U3 PIN14,16	OUTPUT
PLUG IN	HI	HP IN
UNPLUG	LOW	LINR IN

8.15 Audio failure

No sound from speaker after audio driver is installed.

Audio drive failure

1. Check and see all cables and devices are connected properly.
2. Make sure all of software drivers are installed properly.

Test ok?

Yes → End

No

1.Try another known good speaker,cable and CD-ROM.
2.Make sure the setup is ok,such as I/O address,IRQ… ….

Test ok?

Yes → End

No

Replace M/B or go into board-level troubleshooting

Board-level troubleshooting for Audio test error

Check the following parts for cold solder or one of the following parts on the motherboard may be defective,use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

1.If no sound cause of line out, check the following parts & signals:

2.If no sound cause of MIC, check the following Parts & signals:

3.If no sound cause of CD-ROM,check the following parts & signals:

PARTS:	SIGNALS:	PARTS:	SIGNALS:	PARTS:	SIGNALS:
U7,U8,U3	AOUTR	U7,U8,U3	MIC0	U3,U7,U8	CDROM_RIGHT
R502,R507	AOUTL	L505,L506		C79,C95	CDROM_LEFT
L501,L502		L503,L504		R98,R97	
C3,C4,C5		C149,R107		R75,R74	
R3,C7,R5		… … …		R73	
VR1				J510	
C4,C6					
...					

9. Spare parts list-1

Part Number	Description	Location
272075103702	CAP;.01U ,50V,+80-20%,0603,SMT	PC12,16,27,37,46
272072473401	CAP;.047U,16V ,10%,0603,Y5V,SMT	C20,8
272075104701	CAP;.1U ,50V,+80-20%,0603,SMT	PC3,4,5,7,8,14,15,18
272003104701	CAP;.1U ,CR,25V ,+80-20%,0805,Y	C68,70,110,111,112,
272075102403	CAP;1000P,CR,50V,10%,0603,X7R,SM	PC13,1,2,32,504,513,
272075101701	CAP;100P ,50V ,+80-20%,0603,SMT	C508,507,23
272075100701	CAP;10P ,50V ,+80-20%,0603,SMT	C54,55,116,119,144,
272012106701	CAP;10U ,16V ,+80-20%,1206,Y5U,	PC6,10,21,24,25,C184
272043106501	CAP;10U ,CR,25V ,20%,1812,Y5U,S	PC9,29,43,502
272071105701	CAP;1U ,CR,10V ,80-20%,0603,Y5	PC17,22,33,C135
272012475701	CAP;4.7U ,CR,16V ,+80-20%,1206,Y	C2,36,93,155,229
272075470701	CAP;47P ,50V ,+80-20%,0603,SMT	C11,12,142,143
272075561701	CAP;560P ,CR,50V ,+80-20%,0603,S	C39,60,225,226
272431566501	CAP;56U ,TT,4V,20%,SP-CON,7343,	PC510,C517,518
272075680302	CAP;68P ,50V ,5% ,0603,SMT	C139,140
342665500008	CFM-SUYIN;S-STANDOFF,#4-40H4.8,N	
273000500020	CHOKE COIL;100UH,6X4X4.5,T040202	L508
273000500015	CHOKE COIL;50UH(REF),D.4*2,5.5T,	PL500
313000020181	CHOKE COIL;8UH,12.5TS,D1.0,55130	PL506
313000020153	CHOKE;75uH,20%,D0.6,55130,H=14MM	PL505
331000006002	CON;BATTERY,6P,5MM,GOLD,5010S-06	PJ501
331720015006	CON;D,FM,15P,2.29,R/A,3ROW	J501
331720025005	CON;D,FM,25P,2.775,R/A	J503
331720009004	CON;D,MA,9P,2.775,R/A	J502
291000153006	CON;FPC/FFC,15P*2,.8MM,BD/BD,ST,	J505
291000152401	CON;FPC/FFC,24P,1MM,R/A,ELCO	J9

Part Number	Description	Location
291000152602	CON;FPC/FFC,26P,1MM,R/A,SMT,ELCO	J10
291000011001	CON;HDR,MA,10P*1,1.25,ST,SMT	J8
291000014003	CON;HDR,MA,20P*2,1.25MM,ST,SMT	J6
291000014802	CON;HDR,MA,24P*2,1.27,ST,H3.58,S	J11
291000014601	CON;HDR,MA,46P,1.27,ST,H1.5,SMT	J510
291000020404	CON;HDR,SHROUD,4P*1,2,R/A,USB,BE	J3
291000251441	CON;IC CARD,FM,72P*2,.6MM,H3MM,S	J508
331870006011	CON;MINI DIN,6P,R/A,W/GROUNDING	J500
331810006016	CON;PHONE JACK,6P,17*13.2*11.5,R	J506
331910003003	CON;POWER JACK,3P,16VDC/3A	PJ500
331840005008	CON;STEREO JACK,5P,R/A,D3.6,2H7.	J1,J2
291000410201	CON;WFR,MA,2P,1.25,ST,SMT/MB	J4,5,504
291000410301	CON;WFR,MA,3P,1.25,ST,SMT/MB	J7,507
345665400036	CONDUCTIVE TAPE;TOUCH PAD/166,VE	
272625101401	CP;100P*4,8P,50V ,10%,1206,NPO,S	CP1,4,5,6,7,8,9,10,
272625470401	CP;47P*4 ,8P,50V ,10%,1206,NPO,S	CP2,3,13
Part Number	Description	Location
291000621445	DIMM SOCKET;144P,.8MM,GOLD,SMT	J509
288100032013	DIODE;BAS32L,VRRM75V,MELF,SOD-80	D1,8,9,10,11,13,14,
288100701002	DIODE;BAV70LT1,70V,225MW,SOT-23	PD11,D12
288101004024	DIODE;EC10QS04,RECT,40V,1A,CHIP,	PD3,8,501,503
288100024002	DIODE;RLZ24D,ZENER,23.63V,5%,SMT	PD500
288100056001	DIODE;RLZ5.6B,ZENER,5.6V,5%,LL34	PD7
288100073002	DIODE;SFPJ-73,DC2010,30V,3A,SMT	PD1,2,4,13,14
312271006350	EC;100U ,25V,20%,RA,6.3*7,-40~10	PC500,PC501,PC506
272602107501	EC;100U,16V,M,6.3*5.5,-55+85'C,S	C3,4

5133S M/B Maintenance

9. Spare parts list-2

Part Number	Description	Location
312273306151	EC;330U ,6.3V,20%,RA,D10,W/OS-CO	PC508,PC509,PC511
481666410002	F/W ASSY;KBD CTRL,5133S	U10
481666410001	F/W ASSY;SYS/VGA BIOS,5133S	U27
273000610008	FERRITE ARRAY;120OHM/100MHZ,TKIN	FA1,2,3,4,5,6,7
273000130013	FERRITE CHIP;30OHM/100MHZ,1608	L2,3,6,7,8,9,10,11,
273000150009	FERRITE CHIP;30OHM/100MHZ,2012,S	L4,5,17,19,28,507,
273000130006	FERRITE CHIP;600OHM/100MHZ,.2A,1	L501,502,503
341666400002	FINGER;M/B,TOP-SHIELD,5133S	E1,2,3,4
288003600001	FIR;HSDL3600#007,FRONT VIEW,10P,	U502
295000010014	FUSE;1.1A/6V,POLY SWITCH,PTC,SMD	F1,2
295000010016	FUSE;NORMAL,6.5A/32VDC,3216,SMT	PF1,500
345666700003	GASKET;345665400029,6133S	
345666200012	GASKET;AUDIO-JACK,NV	
345666700006	GASKET;M/B-VR,GTU-5-2-15,6133S	
345665400013	GASKET;USB,VENUS	
344600000286	IC CARD CON PART;72P*2,5133S	
331650032107	IC SOCKET;321P,ZIF,ZIFPGAF8	U501
282574008005	IC;74AHC08,QUAD 2-I/P AND,TSSOP,	U22
282574014004	IC;74AHC14,HEX INVERTER,TSSOP,14	U15
282074338402	IC;74CBTD3384,10 BIT BUS SW,TSOP	U13
282574164002	IC;74VHC164,SIPO REGISTER,TSSOP,	U4
286203311001	IC;ADM3311E,RS-232,TSSOP,28P	U500
286300809003	IC;ADM809M,RESET CIRCUIT,4.38V,S	U9
284500007001	IC;CBI7,NORTH BRIDGE,BGA,492P	U24
283420502004	IC;FLASH,256K*8-15,PLCC,32P,VENU	U27
284583434001	IC;H8/F3434,KBD CTLR,TQFP,100P	U10

Part Number	Description	Location
286317812001	IC;HA178L12UA,VOLT REGULATOR,SC-	PU3
284509248005	IC;ICS9248-101,CLOCK GEN,SSOP,48	U6
286302675002	IC;LM2675-ADJ,REGULATOR,1A,SO,8P	PU500
286100393004	IC;LMV393,DUAL COMPARTOR,SSOP,8P	PU9,8
286302951015	IC;LP2951ACM,VOLTAGE REGULATOR,S	U21
286300809002	IC;MAX809S,RESET CIRCUIT,2.9V,SO	U18
284501284001	IC;PAC1284-01Q,TERMIN. NETWK,QSO	U2,1
283666640001	IC;PBSRAM,64*64-5,TQFP,128P,5133	U14
284501211001	IC;PCI1211,PCI/CARDBUS,PQFP,144P	U28
286303032001	IC;SB3032P,PWM CTLR,SO,16P	PU5
286303052001	IC;SB3052P,PWM CTRL,SSOP,28P	PU4
286300431010	IC;SC431CSK-1,1%,ADJ REG,SOT23	PQ5,11
283766641001	IC;SDRAM,1M*16*4-100,TSOP,54P,51	U16,19,25,30
283666640002	IC;SRAM,32K*8,8NS,3.3V,SOJ,28P,5	U11
286300594001	IC;TL594C,PWM CONTROL,SO,16P	PU6
286100202001	IC;TPA0202,AUDIO AMP,2W,TSSOP,24	U3
286302211001	IC;TPS2211,POWER DISTRI SW,SSOP1	U29
284501611001	IC;VT1611A,AUDIO CODEC,TQFP,48P	U7
284582686006	IC;VT82C686A,SOUTH BRIDGE,BGA,35	U8
273000990023	INDUCTOR;10UH,CDRH125B,SUMIDA,SM	PT500
273000990012	INDUCTOR;10UH,CDRH127,SUMIDA,SMT	PL503
273000990015	INDUCTOR;22UH,CD54,SUMIDA,SMT	PT501
346666200007	INSULATOR;AUDIO-JACK,NV	
346666100006	INSULATOR;I/O PANEL,6133	
346666400005	INSULATOR;MDC,M/B,5133S	
346665400037	INSULATOR;PCMCIA/200,VENUS	

9. Spare parts list-3

Part Number	Description	Location
346665400025	INSULATOR;SW BD CON.,VENUS	
242600000380	LABEL;10*8MM,BIOS,HI-TEMP 260	
242600000380	LABEL;10*8MM,BIOS,HI-TEMP 260	
242662300009	LABEL;25*10MM,3020F	
242600000378	LABEL;27*7MM,HI-TEMP 260'C	
242600000364	LABEL;BLANK,6*6MM,HI-TEMP	
242600000170	LABEL;PCMCIA CARD WORKS/95 EN	
242600000195	LABEL;SOFTWARE,INSYDE BIOS-M	
294011200001	LED;GRN,H1.5,0805,PG1102W,SMT	D2,3,4,5,6,7
375102030010	NUT-HEX;M2,2,NIW	
316666410003	PCB;PWA-5133S/M BD,R01	
411666410010	PWA;PWA-5133S,M/BD,W/32MB,12.1",	
411666410011	PWA;PWA-5133S,MBD,W/32M,121,R01,	
411666410012	PWA;PWA-5133S,MBD,W/32M,121,R01,	R0B
271086057101	RES;.005 ,2W ,1% ,7520,SMT	PR14
271045207101	RES;.02 ,1W ,1% ,2512,SMT	PR2,504,505
271071000002	RES;0 ,1/16W,0603,SMT	PR21,50,R1,42,49
271071121111	RES;1.21K,1/16W,1% ,0603,SMT	PR3,32
271071152101	RES;1.5K ,1/16W,1% ,0603,SMT	PR8
271071100302	RES;10 ,1/16W,5% ,0603,SMT	R43,44,45,48,153
271071107211	RES;10.7K,1/16W,1% ,0603,SMT	PR501
271071104101	RES;100K ,1/16W,1% ,0603,SMT	PR7,33,35,43,46
271071104302	RES;100K ,1/16W,5% ,0603,SMT	PR1,19,37,R31,32,33,
271071103101	RES;10K ,1/16W,1% ,0603,SMT	PR18,500,502,503,506
271071103302	RES;10K ,1/16W,5% ,0603,SMT	PR4,5,15,24,26,34,R4
271071106301	RES;10M ,1/16W,5% ,0603,SMT	R104
271071118211	RES;11.8K,1/16W,1% ,0603,SMT	PR41
271071115411	RES;115K ,1/16W,1% ,0603,SMT	PR6
271071153301	RES;15K ,1/16W,5% ,0603,SMT	R18,19
271071169311	RES;169K ,1/16W,1% ,0603,SMT	PR44
271071191211	RES;19.1K,1/16W,1% ,0603,SMT	PR507
271071102102	RES;1K ,1/16W,1% ,0603,SMT	PR11,12
271071102302	RES;1K ,1/16W,5% ,0603,SMT	R2,161,29,51,81,150,
271071105101	RES;1M ,1/16W,1% ,0603,SMT	PR40
271071221111	RES;2.21K,1/16W,1% ,0603,SMT	PR9,R7,8,26
271071204101	RES;200K ,1/16W,1% ,0603,SMT	PR27
271071203101	RES;20K ,1/16W,1% ,0603,SMT	PR49,R505
271071203302	RES;20K ,1/16W,5% ,0603,SMT	R24,22,5,3
271071221302	RES;22 ,1/16W,5% ,0603,SMT	R73,74,75,97,98,102,
271071224301	RES;220K ,1/16W,5% ,0603,SMT	R126
271071226311	RES;226K ,1/16W,1% ,0603,SMT	PR36
271071249211	RES;24.9K,1/16W,1% ,0603,MST	PR10,13
271071301211	RES;30.1K,1/16W,1% ,0603,SMT	PR511
271071301311	RES;301K ,1/16W,1% ,0603,SMT	PR47
271071361101	RES;360 ,1/16W,1% ,0603,SMT	R136,504
271071472302	RES;4.7K ,1/16W,5% ,0603,SMT	PR22,28,R28,30,50,52
271071499111	RES;4.99K,1/16W,1% ,0603,SMT	PR48,R188
271071402311	RES;402K ,1/16W,1% ,0603,SMT	PR39
271071412311	RES;412K ,1/16W,1% ,0603,SMT	PR29
271071471302	RES;470 ,1/16W,5% ,0603,SMT	R13,14,15,16,17,21,
271071474301	RES;470K ,1/16W,5% ,0603,SMT	R12,20,141
271071473301	RES;47K ,1/16W,5% ,0603,SMT	R106,107,101,PR25

9. Spare parts list-4

Part Number	Description	Location
271071511111	RES;5.11K,1/16W,1% ,0603,SMT	PR30
271071514301	RES;510K ,1/16W,5% ,0603,SMT	PR17
271071576311	RES;576K ,1/16W,1% ,0603,SMT	PR42,R27
271071593101	RES;59K ,1/16W,1% ,0603,SMT	PR508
271071634211	RES;63.4K,1/16W,1% ,0603,SMT	PR509
271023918301	RES;9.1 ,1/4W,5% ,1210,SMT	R184,185
271571100301	RP;10*8 ,16P ,1/16W,5% ,1606,SM	RP35,40
271611103301	RP;10K*4 ,8P ,1/16W,5% ,0612,SMT	RP10,20,67
271621103303	RP;10K*8 ,10P,1/16W,5% ,1206,SMT	RP13,15,16
271611102301	RP;1K*4 ,8P ,1/16W,5% ,0612,SMT	RP22,27,49,66
271611330301	RP;33*4 ,8P ,1/16W,5% ,0612,SMT	RP3,8,58
271571330301	RP;33*8 ,16P ,1/16W,5% ,1606,SM	RP4,5,6,7,25,26
271611472301	RP;4.7K*4,8P ,1/16W,5% ,0612,SMT	RP9,50,53,54,59,60,
271621472303	RP;4.7K*8,10P,1/16W,5% ,1206,SMT	RP18,1,2,11,12,14,17
271611473301	RP;47K*4 ,8P ,1/16W,5% ,0612,SMT	RP52
271621473301	RP;47K*8 ,10P,1/16W,5% ,1206,SMT	RP44,19
271611750301	RP;75*4 ,8P ,1/16W,5% ,0612,SMT	RP30
371102610401	SCREW;M2.6L4,FLT(+),NIW	
340666400001	SHIELD ASSY;BOTTOM,CASE KIT,5133	
341666200011	SHIELD;AUDIO,NV	
341666900003	SHIELD;PCMCIA,6633	
361400003028	SHIN-ETSU;KE45WS RTV SILICON,350	
365350000002	SOLDER WIRE;63/37FLUX%1.2 DIA.64	
370102610401	SPC-SCREW;M2.6L4,NIB,727,NLK	
370102010302	SPC-SCREW;M2L3,NIW,K-HD,736	
341666200012	SPRING;DC JACK,NV	

Part Number	Description	Location
341666400001	STANDOFF;MDC MODEM,5133S	
337120124001	SW;DIP,SPST,2P,25VDC,24MA,HDK632	SW500
297120101005	SW;DIP,SPST,8P,50VDC,.1A,SMT,DHS	SW2,3,4,5
337030105013	SW;TOGGLE,SPST,5V/1mA	SW1
225665500001	TAPE;INSULATION,AC04,25M*6MM,503	
346665400019	THERMAL PAD;20*20*.5,VENUS	
310111103006	THERMISTOR;10K,1%,DISK,103JT-025	RT500
288227002001	TRANS;2N7002LT1,N-CHANNEL FET	PQ2,4,6,7,8,10,13
288200144003	TRANS;DTC144TKA,N-MOSFET,SOT-23	PQ12,Q2,3,4,6,8,9
288200144001	TRANS;DTC144WK,NPN,SOT-23,SMT	PQ9
288207030003	TRANS;FDB7030BL,60A30V,NMOS,TO26	PQ500
288202222001	TRANS;MMBT2222AL,NPN,TO236AB	PQ1
288203906018	TRANS;MMBT3906L,PNP,Tr35NS,TO236	PQ3,Q5
288202301001	TRANS;SI2301DS,P-MOSFET,SOT-23	Q7,15,500
288204416001	TRANS;Si4416DY,N-MOSFET,.028OHM,	PU2
288204435001	TRANS;SI4435DY,P-MOSFET,.035OHM,	PU1,7
288209410001	TRANS;SI9410DY,N-MOSFET,.04OHM,S	Q1,PU501,502,503,504
270140000003	VARISTOR;280V,5.6X3.8MM,TVB280-0	S1
311801002193	VR;10K,20%,.05W,CCE,D16MM,-15C10	VR1
274011431409	XTAL;14.318MHZ,16PF,50PPM,8*4.5,	X1
274011600408	XTAL;16MHZ,16PF,50PPM,8*4.5,2P	X2
274012457406	XTAL;24.576MHZ,16PF,50PPM,8*4.5,	X3
274013276103	XTAL;32.768KHZ,30PPM,12.5PF,CM20	X4
**** s¹ P¬ § Æ	ù p- â µ § *****	