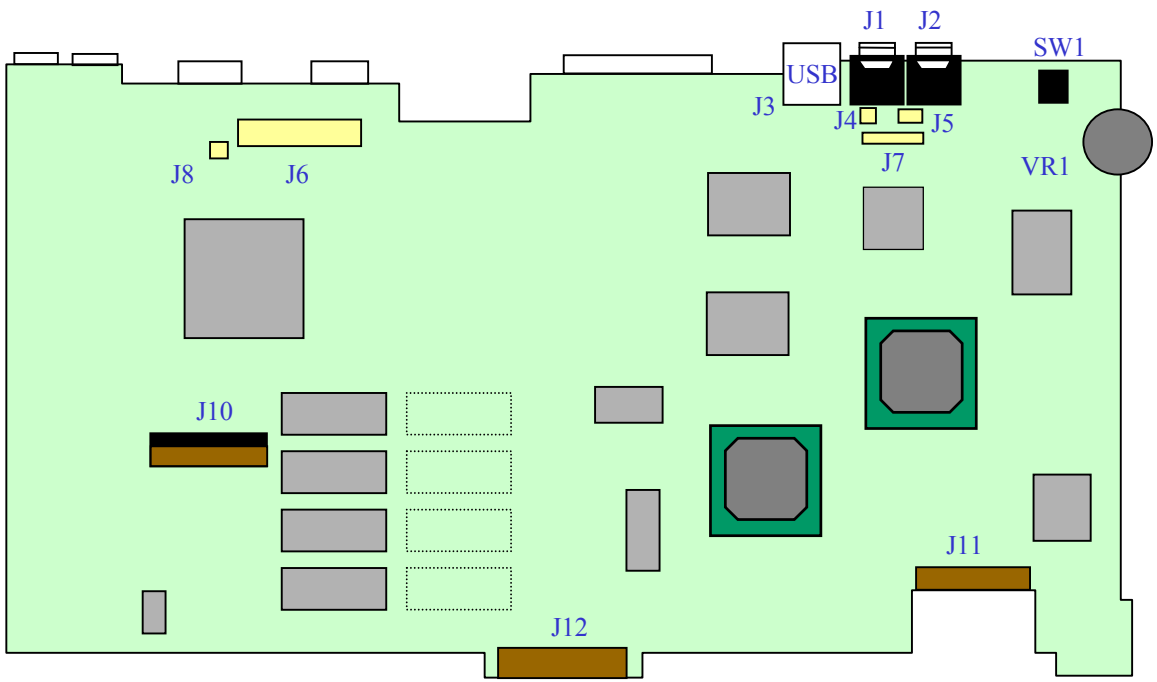
MITAC
5033T MAINTENANCE

5033 M/B MAINTENANCE

5033 M/B MAINTENANCE

1. DEFINITION & LOCATION OF CONNECTORS / SWITCHES (A)

J1: AUDIO OUTPUT
J2: MIC IN
J3: USB PORT
J4,J8: R/L SPK CONN.
J5: INTERNAL MIC
J6: LCD CONN.
J7: INVERTER BD CONN
J10: KEYBOARD CONN.
J11: FDD CONN.
J12: TOUCHPAD CONN.
SW1: SUSPAND SWITCH

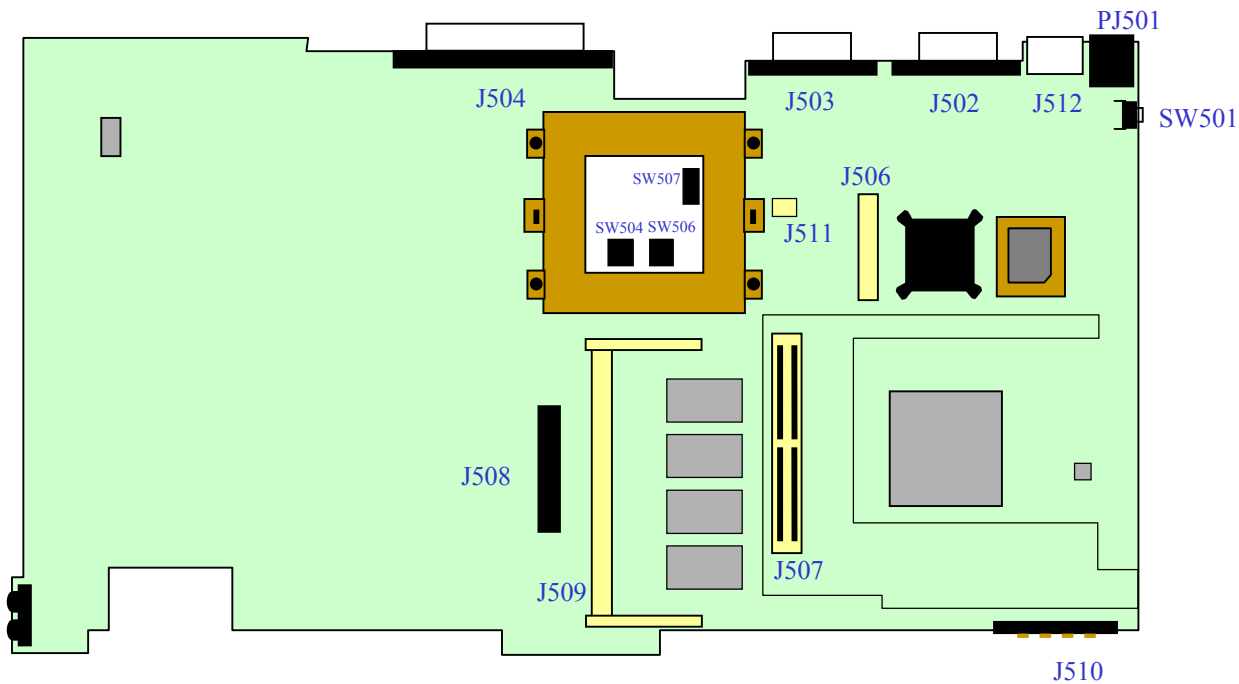


5033 M/B MAINTENANCE

2. DEFINITION & LOCATION OF CONNECTORS / SWITCHES (B)

PJ501: POWER JACK
J512: PS/2 KEYBOARD/
MOUSE CONN.
J502: VGA CONN.
J503: SERIAL PORT
J504: PARALLEL PORT
J506: FAX/MODEM CONN
J511: CPU FAN CONN

J507: PCMCIA CONN.
J508: CO-ROM CONN.
J509: 114 PINS SODIMM SOCKET
J510: BATTERY CONN.
J506: INTERNAL MODEM CONN
SW501: POWER SWITCH
SW504: SELECTING CPU SPEED
SW506: SELECTING CPU CORE VCC

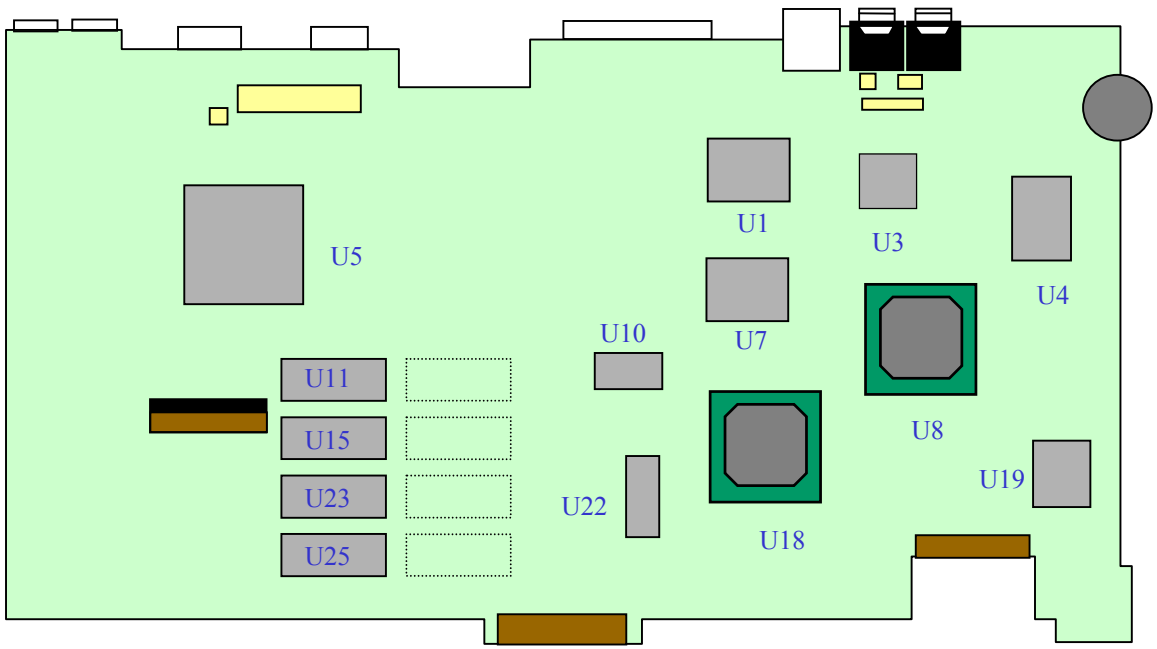


5033 M/B MAINTENANCE

2. DEFINITION & LOCATION OF MAJOR COMPONENTS(A)

U1,U7:256K L2 CACHE SRAM
U3: NS PC97338VJC
SUPER I/O CONTROLLER
U4: ES1869F AUDIO CONTROLLER
U5: TRIDENT 9385T VGA CTRL.
U8: PIIX4(82371AB) SOUTH BRIDGE
U10: CLOCK SYNTHESIZER.

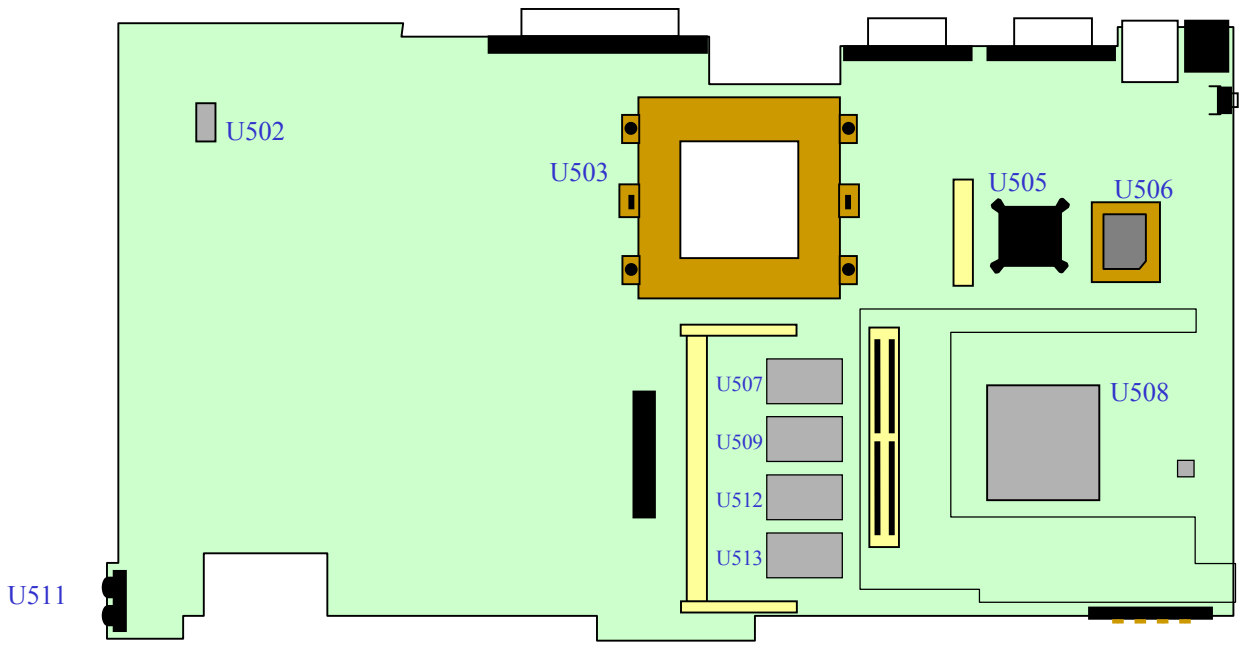
U11,15,U23,U25:2MB VIDEO MEMORY
U18: MTXC(82439TX)
U19: 29F002 SYSTEM BIOS



5033 M/B MAINTENANCE

2. DEFINITION & LOCATION OF MAJOR COMPONENTS(A)

U503: CPU
U505: 80C51 UNIVERSAL KEYBOARD CONTROLLER.
U506: 256K FLASH KEYBOARD BIOS
U508: TI1220 CARD BUS CONTROLLER.
U507,U509,U512,U513: ON BOARD MEMORY 32MB EDO RAM.



3. PIN DESCRIPTIONS OF MAJOR COMPONENTS

3.2 PENTIUM MICROPROCESSOR (P55C)-1

Symbol	Type	Name and Function
A20M#	I	When the **address bit 20 mask** pin is asserted, the Pentium ?processor with MMX™ technology emulates the address wraparound at 1 Mbyte which occurs on the 8086 by masking physical address bit 20 (A20) before performing a lookup to the internal caches or driving a memory cycle on the bus. The effect of A20M# is undefined in protected mode. A20M# must be asserted only when the processor is in real mode. A20M# is internally masked by the Pentium processor with MMX technology when configured as a Dual processor.
A31-A3	I/O	As outputs, the **address** lines of the processor along with the byte enables define the physical area of memory or I/O accessed. The external system drives the inquire address to the processor on A31-A5.
ADS#	O	The **address strobe** indicates that a new valid bus cycle is currently being driven by the Pentium processor with MMX technology.
ADSC#	O	The **address strobe (copy)** is functionally identical to ADS#.
AHOLD	I	In response to the assertion of **address hold**, the Pentium processor with MMX technology will stop driving the address lines (A31-A3) and AP in the next clock. The rest of the bus will remain active so data can be returned or driven for previously issued bus cycles.
AP	I/O	**Address parity** is driven by the Pentium processor with MMX technology with even parity information on all Pentium processor with MMX technology generated cycles in the same clock that the address is driven. Even parity must be driven back to the Pentium processor with MMX technology during inquire cycles on this pin in the same clock as EADS# to ensure that correct parity check status is indicated by the Pentium processor with MMX technology.
APCHK#	O	The **address parity check** status pin is asserted two clocks after EADS# is sampled active if the Pentium processor with MMX technology has detected a parity error on the address bus during inquire cycles. APCHK# will remain active for one clock each time a parity error is detected (including during dual processing private snooping).
[APICEN] PICD1	I	**Advanced Programmable Interrupt Controller Enable** enables or disables the on-chip APIC interrupt controller. If sampled high at the falling edge of RESET, the APIC is enabled. APICEN shares a pin with the PICD1 signal.

Symbol	Type	Name and Function
BE7#-E4# BE3#-E0#	O I/O	The **byte enable** pins are used to determine which bytes must be written to external memory or which bytes were requested by the CPU for the current cycle. The byte enables are driven in the same clock as the address lines (A31-3). Additionally, the lower 4-byte enables (BE3#-BE0#) are used on the Pentium processor with MMX technology as APIC ID inputs and are sampled at RESET. In dual processing mode, BE4# is used as an input during Flush cycles.
BF[1:0]	I	The **bus frequency** pins determine the bus-to-core frequency ratio. BF[1:0] are sampled at RESET, and cannot be changed until another non-warm (1 ms) assertion of RESET. Additionally, BF[1:0] must not change values while RESET is active. See Table 3 for Bus Frequency Selections.
BOFF#	I	The **backoff** input is used to abort all outstanding bus cycles that have not yet completed. In response to BOFF#, the Pentium processor with MMX technology will float all pins normally floated during bus hold in the next clock. The processor remains in bus hold until BOFF# is negated, at which time the Pentium processor with MMX technology restarts the aborted bus cycle(s) in their entirety.
BP[3:2] PM/BP[1:0]	O	The **breakpoint** pins (BP3-0) correspond to the debug registers, DR3-DR0 These pins externally indicate a breakpoint match when the debug registers are programmed to test for breakpoint matches.
		BP1 and BP0 are multiplexed with the **performance monitoring** pins (PM1 and PM0). The PB1 and PB0 bits in the Debug Mode Control Register determine if the pins are configured as breakpoint or performance monitoring pins. The pins come out of RESET configured for performance monitoring.
BRDY#	I	The **burst ready** input indicates that the external system has presented valid data on the data pins in response to a read or that the external system has accepted the Pentium processor with MMX technology data in response to a write request. This signal is sampled in the T2, T12 and T2P bus states.
BRDYC#	I	The **burst ready (copy)** is functionally identical to BRDY#.
BREQ	O	The **bus request** output indicates to the external system that the Pentium processor with MMX technology has internally generated a bus request. This signal is always driven whether or not the Pentium processor with MMX technology is driving its bus.

3.2 PENTIUM MICROPROCESSOR (P55C)-2

Symbol	Type	Name and Function
BUSCHK#	I	The **bus check** input allows the system to signal an unsuccessful completion of a bus cycle. If this pin is sampled active, the Pentium processor with MMX technology will latch the address and control signals in the machine check registers. If, in addition, the MCE bit in CR4 is set, the Pentium processor with MMX technology will vector to the machine check exception. **NOTE:** To assure that BUSCHK# will always be recognized, STPCLK# must be deasserted any time BUSCHK# is asserted by the system, before the system allows another external bus cycle. If BUSCHK# is asserted by the system for a snoop cycle while STPCLK# remains asserted, usually (if MCE=1) the processor will vector to the exception after STPCLK# is deasserted. But if another snoop to the same line occurs during STPCLK# assertion, the processor can lose the BUSCHK# request.
CACHE#	O	For Pentium processor with MMX technology-initiated cycles the **cache** pin indicates internal cacheability of the cycle (if a read), and indicates a burst write back cycle (if a write). If this pin is driven inactive during a read cycle, the Pentium processor with MMX technology will not cache the returned data, regardless of the state of the KEN# pin. This pin is also used to determine the cycle length (number of transfers in the cycle).
CLK	I	The **clock** input provides the fundamental timing for the Pentium processor with MMX technology. Its frequency is the operating frequency of the Pentium processor with MMX technology external bus, and requires TTL levels. All external timing parameters except TDI, TDO, TMS, TRST#, and PICD0-1 are specified with respect to the rising edge of CLK. This pin is 3.3V-tolerant-only on the Pentium processor with MMX technology. Please refer to the Pentium ?Processor Family Developer• Manual (Order Number 241428) for the CLK and PICCLK signal quality specification. **NOTE:** It is recommended that CLK begin toggling within 150 ms after VCC reaches its proper operating level. This recommendation is to ensure long-term reliability of the device.
CPUTYP	I	**CPU type** distinguishes the Primary processor from the Dual processor. In a single processor environment, or when the Pentium processor with MMX technology is acting as the Primary processor in a dual processing system, CPUTYP should be strapped to VSS. The Dual processor should have CPUTYP strapped to VCC3.
D/C#	O	The **data/code** output is one of the primary bus cycle definition pins. It is driven valid in the same clock as the ADS# signal is asserted. D/C# distinguishes between data and code or special cycles.

Symbol	Type	Name and Function
D/P#	O	The **dual/primary** processor indication. The Primary processor drives this pin low when it is driving the bus, otherwise it drives this pin high. D/P# is always driven. D/P# can be sampled for the current cycle with ADS# (like a status pin). This pin is defined only on the Primary processor. Dual processing is supported in a system only if both processors are operating at identical core and bus frequencies. Within these restrictions, two processors of different steppings may operate together in a system.
D63-D0	I/O	These are the 64 **data lines** for the processor. Lines D7-D0 define the least significant byte of the data bus; lines D63-D56 define the most significant byte of the data bus. When the CPU is driving the data lines, they are driven during the T2, T12, or T2P clocks for that cycle. During reads, the CPU samples the data bus when BRDY# is returned.
DP7-DP0	I/O	These are the **data parity** pins for the processor. There is one for each byte of the data bus. They are driven by the Pentium processor with MMX technology with even parity information on writes in the same clock as write data. Even parity information must be driven back to the Pentium processor with MMX technology on these pins in the same clock as the data to ensure that the correct parity check status is indicated by the Pentium processor with MMX technology. DP7 applies to D63-56, DP0 applies to D7-0.
[DPEN#] PICD0	I/O	**Dual processing enable** is an output of the Dual processor and an input of the Primary processor. The Dual processor drives DPEN# low to the Primary processor at RESET to indicate that the Primary processor should enable dual processor mode. DPEN# may be sampled by the system at the falling edge of RESET to determine if the dual-processor socket is occupied. DPEN# is multiplexed with PICD0.
EADS#	I	This signal indicates that a valid **external address** has been driven onto the Pentium processor with MMX technology address pins to be used for an inquire cycle.
EWBE#	I	The **external write buffer empty** input, when inactive (high), indicates that a write cycle is pending in the external system. When the Pentium processor with MMX technology generates a write, and EWBE# is sampled inactive, the Pentium processor with MMX technology will hold off all subsequent writes to all E- or M-state lines in the data cache until all write cycles have completed, as indicated by EWBE# being active.
FERR#	O	The **floating-point error** pin is driven active when an unmasked **floating-point** error occurs. FERR# is similar to the ERROR# pin on the Intel387?math coprocessor. FERR# is included for compatibility with systems using DOS type **floating-point** error reporting. FERR# is never driven active by the Dual processor.

3.2 PENTIUM MICROPROCESSOR (P55C)-3

Symbol	Type	Name and Function
FLUSH#	I	When asserted, the **cache flush** input forces the Pentium processor with MMX technology to write back all modified lines in the data cache and invalidate its internal caches. A Flush Acknowledge special cycle will be generated by the Pentium processor with MMX technology indicating completion of the write back and invalidation. If FLUSH# is sampled low when RESET transitions from high to low, tristate test mode is entered. If two Pentium processors with MMX technology are operating in dual processing mode and FLUSH# is asserted, the Dual processor will perform a flush first (without a flush acknowledge cycle), then the Primary processor will perform a flush followed by a flush acknowledge cycle. **NOTE:** If the FLUSH# signal is asserted in dual processing mode, it must be deasserted at least one clock prior to BRDY# of the FLUSH Acknowledge cycle to avoid DP arbitration problems.
FRCMC#	I	Functional Redundancy Checking is not supported on the Pentium processor with MMX technology. The FRCMC# pin is not defined for the Pentium processor with MMX technology. This pin should be left as a • C?or tied to VCC3 via an external pull-up resistor.
HIT#	O	The **hit** indication is driven to reflect the outcome of an inquire cycle. If an inquire cycle hits a valid line in either the Pentium processor with MMX technology data or instruction cache, this pin is asserted two clocks after EADS# is sampled asserted. If the inquire cycle misses the Pentium processor with MMX technology cache, this pin is negated two clocks after EADS#. This pin changes its value only as a result of an inquire cycle and retains its value between the cycles.
HITM#	O	The **hit to a modified line** output is driven to reflect the outcome of an inquire cycle. It is asserted after inquire cycles which resulted in a hit to a modified line in the data cache. It is used to inhibit another bus master from accessing the data until the line is completely written back.
HLDA	O	The **bus hold acknowledge** pin goes active in response to a hold request driven to the processor on the HOLD pin. It indicates that the Pentium processor with MMX technology has floated most of the output pins and relinquished the bus to another local bus master. When leaving bus hold, HLDA will be driven inactive and the Pentium processor with MMX technology will resume driving the bus. If the Pentium processor with MMX technology has a bus cycle pending, it will be driven one clock cycle after HLDA is de-asserted.

Symbol	Type	Name and Function
HOLD	I	In response to the **bus hold request**, the Pentium processor with MMX technology will float most of its output and input/output pins and assert HLDA after completing all outstanding bus cycles. The Pentium processor with MMX technology will maintain its bus in this state until HOLD is de-asserted. HOLD is not recognized during LOCK cycles. The Pentium processor with MMX technology will recognize HOLD during reset.
IERR#	O	The **internal error** pin is used to indicate internal parity errors. If a parity error occurs on a read from an internal array, the Pentium processor with MMX technology will assert the IERR# pin for one clock and then shutdown.
IGNNE#	I	This is the **ignore numeric error** input. This pin has no effect when the NE bit in CR0 is set to 1. When the CR0.NE bit is 0, and the IGNNE# pin is asserted, the Pentium processor with MMX technology will ignore any pending unmasked numeric exception and continue executing floating-point instructions for the entire duration that this pin is asserted. When the CR0.NE bit is 0, IGNNE# is not asserted, a pending unmasked numeric exception exists (SW.ES = 1), and the floating-point instruction is one of FINIT, FCLEX, FSTENV, FSAVE, FSTSW, FSTCW, FENI, FDISI, or FSETPM, the Pentium processor with MMX technology will execute the instruction in spite of the pending exception. When the CR0.NE bit is 0, IGNNE# is not asserted, a pending unmasked numeric exception exists (SW.ES = 1), and the floating-point instruction is one other than FINIT, FCLEX, FSTENV, FSAVE, FSTSW, FSTCW, FENI, FDISI, or FSETPM,the Pentium processor with MMX technology will stop execution and wait for an external interrupt. IGNNE# is internally masked when the Pentium processor with MMX technology is configured as a Dual processor.
INIT	I	The Pentium processor with MMX technology **initialization** input pin forces the Pentium processor with MMX technology to begin execution in a known state. The processor state after INIT is the same as the state after RESET except that the internal caches, write buffers, and floating-point registers retain the values they had prior to INIT. INIT may NOT be used in lieu of RESET after power-up. If INIT is sampled high when RESET transitions from high to low, the Pentium processor with MMX technology will perform built-in self test prior to the start of program execution.
INTR/LINT0	I	An active **maskable interrupt** input indicates that an external interrupt has been generated. If the IF bit in the EFLAGS register is set, the Pentium processor with MMX technology will generate two locked interrupt acknowledge bus cycles and vector to an interrupt handler after the current instruction execution is completed. INTR must remain active until the first interrupt acknowledge cycle is generated to assure that the interrupt is recognized. If the local APIC is enabled, this pin becomes LINT0.

3.2 PENTIUM MICROPROCESSOR (P55C)-4

Symbol	Type	Name and Function
INV	I	The **invalidation** input determines the final cache line state (S or I) in case of an inquire cycle hit. It is sampled together with the address for the inquire cycle in the clock EADS# is sampled active.
KEN#	I	The **cache enable** pin is used to determine whether the current cycle is cacheable or not and is consequently used to determine cycle length. When the Pentium processor with MMX technology generates a cycle that can be cached (CACHE# asserted) and KEN# is active, the cycle will be transformed into a burst line fill cycle.
LINT0/INTR	I	If the APIC is enabled, this pin is **local interrupt 0**. If the APIC is disabled, this pin is INTR.
LINT1/NMI	I	If the APIC is enabled, this pin is **local interrupt 1**. If the APIC is disabled, this pin is NMI.
LOCK#	O	The **bus lock** pin indicates that the current bus cycle is locked. The Pentium processor with MMX technology will not allow a bus hold when LOCK# is asserted (but AHOLD and BOFF# are allowed). LOCK# goes active in the first clock of the first locked bus cycle and goes inactive after the BRDY# is returned for the last locked bus cycle. LOCK# is guaranteed to be de-asserted for at least one clock between back-to-back locked cycles.
M/IO#	O	The **memory/input-output** is one of the primary bus cycle definition pins. It is driven valid in the same clock as the ADS# signal is asserted. M/IO# distinguishes between memory and I/O cycles.
NA#	I	An active **next address** input indicates that the external memory system is ready to accept a new bus cycle although all data transfers for the current cycle have not yet completed. The Pentium processor with MMX technology will issue ADS# for a pending cycle two clocks after NA# is asserted. The Pentium processor with MMX technology supports up to 2 outstanding bus cycles.
NMI/LINT1	I	The **non-maskable interrupt** request signal indicates that an external non-maskable interrupt has been generated. If the local APIC is enabled, this pin becomes LINT1.
PBGNT#	I/O	**Private bus grant** is the grant line that is used when two Pentium processors with MMX technology are configured in dual processing mode, in order to perform private bus arbitration. PBGNT# should be left unconnected if only one Pentium processor with MMX technology exists in a system.

Symbol	Type	Name and Function
PBREQ#	I/O	**Private bus request** is the request line that is used when two Pentium processor with MMX technology are configured in dual processing mode, in order to perform private bus arbitration. PBREQ# should be left unconnected if only one Pentium processor with MMX technology exists in a system.
PCD	O	The **page cache disable** pin reflects the state of the PCD bit in CR3, the Page Directory Entry, or the Page Table Entry. The purpose of PCD is to provide an external cacheability indication on a page by page basis.
PCHK#	O	The **parity check** output indicates the result of a parity check on a data read. It is driven with parity status two clocks after BRDY# is returned. PCHK# remains low one clock for each clock in which a parity error was detected. Parity is checked only for the bytes on which valid data is returned. When two Pentium processors with MMX technology are operating in dual processing mode, PCHK# may be driven two or three clocks after BRDY# is returned.
PEN#	I	The **parity enable** input (along with CR4.MCE) determines whether a machine check exception will be taken as a result of a data parity error on a read cycle. If this pin is sampled active in the clock a data parity error is detected, the Pentium processor with MMX technology will latch the address and control signals of the cycle with the parity error in the machine check registers. If, in addition, the machine check enable bit in CR4 is set to ?? the Pentium processor with MMX technology will vector to the machine check exception before the beginning of the next instruction.
PHIT#	I/O	**Private hit** is a hit indication used when two Pentium processors with MMX technology are configured in dual processing mode, in order to maintain local cache coherency. PHIT# should be left unconnected if only one Pentium processor with MMX technology exists in a system.
PHITM#	I/O	**Private modified hit** is a hit on a modified cache line indication used when two Pentium processors with MMX technology are configured in dual processing mode, in order to maintain local cache coherency. PHITM# should be left unconnected if only one Pentium processor with MMX technology exists in a system.
PICCLK	I	The APIC interrupt controller serial data bus clock is driven into the **programmable interrupt controller clock** input of the Pentium processor with MMX technology. This pin is 3.3V-tolerant-only on the Pentium processor with MMX technology. Please refer to the Pentium ?Processor Family Developer• Manual (Order Number 241428) for the CLK and PICCLK signal quality specification.

3.2 PENTIUM MICROPROCESSOR (P55C)-5

Symbol	Type	Name and Function
PICD0-1 [DPEN#] [APICEN]	I/O	**Programmable interrupt controller data lines 0-1** of the Pentium processor with MMX technology comprise the data portion of the APIC 3-wire bus. They are open-drain outputs that require external pull-up resistors. These signals are multiplexed with DPEN# and APICEN respectively.
PM/BP[1:0]	O	These pins function as part of the performance monitoring feature. The breakpoint 1-0 pins are multiplexed with the **performance monitoring 1-0** pins. The PB1 and PB0 bits in the Debug Mode Control Register determine if the pins are configured as breakpoint or performance monitoring pins. The pins come out of RESET configured for performance monitoring.
PRDY	O	The **probe ready** output pin is provided for use with the Intel debug port. Please refer to the Pentium?Processor Family Developer• Manual (Order Number 241428) for more details.
PWT	O	The **page write through** pin reflects the state of the PWT bit in CR3, the page directory entry, or the page table entry. The PWT pin is used to provide an external write back indication on a page-by-page basis.
R/S#	I	The **run/stop** input is provided for use with the Intel debug port. Please refer to the Pentium?Processor Family Developer• Manual (Order Number 241428) for more details.
RESET	I	**RESET** forces the Pentium processor with MMX technology to begin execution at a known state. All the Pentium processor with MMX technology internal caches will be invalidated upon the RESET. Modified lines in the data cache are not written back. FLUSH# and INIT are sampled when RESET transitions from high to low to determine if tristate test mode or checker mode will be entered, or if Built-In Self-Test (BIST) will be run.
SCYC	O	The **split cycle** output is asserted during misaligned LOCKed transfers to indicate that more than two cycles will be locked together. This signal is defined for locked cycles only. It is undefined for cycles which are not locked.
SMI#	I	The **system management interrupt** causes a system management interrupt request to be latched internally. When the latched SMI# is recognized on an instruction boundary, the processor enters System Management Mode.
SMIACT#	O	An active **system management interrupt active** output indicates that the processor is operating in System Management Mode.

Symbol	Type	Name and Function
STPCLK#	I	Assertion of the **stop clock** input signifies a request to stop the internal clock of the Pentium processor with MMX technology, thereby causing the core to consume less power. When the CPU recognizes STPCLK#, the processor will stop execution on the next instruction boundary, unless superseded by a higher priority interrupt, and generate a stop grant acknowledge cycle. When STPCLK# is asserted, the Pentium processor with MMX technology will still respond to interprocessor and external snoop requests.
TCK	I	The **testability clock** input provides the clocking function for the Pentium processor with MMX technology boundary scan in accordance with the IEEE Boundary Scan interface (Standard 1149.1). It is used to clock state information and data into and out of the Pentium processor with MMX technology during boundary scan.
TDI	I	The **test data input** is a serial input for the test logic. TAP instructions and data are shifted into the Pentium processor with MMX technology on the TDI pin on the rising edge of TCK when the TAP controller is in an appropriate state.
TDO	O	The **test data output** is a serial output of the test logic. TAP instructions and data are shifted out of the Pentium processor with MMX technology on the TDO pin on TCK′s falling edge when the TAP controller is in an appropriate state.
TMS	I	The value of the **test mode select** input signal sampled at the rising edge of TCK controls the sequence of TAP controller state changes.
TRST#	I	When asserted, the **test reset** input allows the TAP controller to be asynchronously initialized.
VCC2 VCC3	I I	The Pentium processor with MMX technology has 25 2.8V **power** inputs. The Pentium processor with MMX technology has 28 3.3V **power** inputs.
VCC2DET#	O	**VCC2 detect** is used in flexible motherboard implementations to configure the voltage output set-point appropriately for the VCC2 inputs of the processor.
VSS	I	The Pentium processor with MMX technology has 53 **ground** inputs.
W/R#	O	**Write/read** is one of the primary bus cycle definition pins. It is driven valid in the same clock as the ADS# signal is asserted. W/R# distinguishes between write and read cycles.
WB/WT#	I	The **write back/write through** input allows a data cache line to be defined as write back or write through on a line-by-line basis. As a result, it determines whether a cache line is initially in the S or E state in the data cache.

3.3 INTEL FW82439TX MEMORY/PCI/CACHE CONTROLLER (MTXC)-1

2.1. MTXC Signals 2.1.1.HOST INTERFACE

Name	Type	Description
A[31:3]	I/O 3.3V/2.5V	**Address Bus.** A[31:3] connects to the address bus of the CPU. During CPU cycles A[31:3] are inputs. The MTXC drives A[31:3] during inquire cycles on behalf of PCI initiators. Bits A[31:26] act as inputs when RST# is active
BE[7:0]#	I 3.3V/2.5V	**Byte Enables.** The CPU byte enables indicate which byte lane the current CPU cycle is accessing. All eight byte lanes must be provided to the CPU if the cycle is a cacheable read regardless of the state of BE[7:0]#.
ADS#	I 3.3V/2.5V	**Address Status.** CPU asserts ADS# in T1 of the CPU bus cycle.
BRDY#	O 3.3V/2.5V	**Bus Ready.** The MTXC asserts BRDY# to indicate to the CPU that data is available on reads or has been received on writes
NA#	O 3.3V/2.5V	**Next Address.** This signal is asserted by the MTXC to indicate to the Processor that it is ready to process a second cycle.
AHOLD	O 3.3V/2.5V	**Address Hold.** The MTXC asserts AHOLD when a PCI initiator is performing a cycle to DRAM. AHOLD is held for the duration of the PCI burst transfer. The MTXC will negate AHOLD when the completion of the PCI to DRAM read or write cycles complete and during PCI peer transfers. AHOLD is kept asserted while PHLDA# is asserted (i.e., duration of PIIX4 granting).
EADS#	O 3.3V/2.5V	**External Address Strobe.** Asserted by the MTXC to inquire the first level cache when servicing PCI master references of DRAM.
BOFF#	O 3.3V/2.5V	**Back Off.** Asserted by the MTXC when required to terminate a CPU cycle that was in progress.
HITM#	I 3.3V/2.5V	**Hit Modified.** Asserted by the CPU to indicate that the address presented with the last assertion of EADS# is modified in the first level cache and needs to be written back.
M/IO#, D/C#, W/R#	I 3.3V/2.5V	**Memory/IO; Data/Control; Write/Read.** Asserted by the CPU with ADS# to indicate the type of cycle that the system needs to perform.
HLOCK#	I 3.3V/2.5V	**Host Lock.** All CPU cycles sampled with the assertion of HLOCK# and ADS#, until the negation of HLOCK# must be atomic, i.e. no PCI activity to DRAM is allowed.
CACHE#	I 3.3V/2.5	**Cache.** Asserted by the CPU during a read cycle to indicate the CPU will Vperform a burst line fill. Asserted by the CPU during a write cycle to indicate the CPU will perform a burst writeback cycle. If CACHE# is asserted to indicate cacheability, the MTXC will assert KEN# either with the first BRDY#, or with NA# if NA# is asserted before the first BRDY#.
KEN#/INV	O 3.3V/2.5V	**Ken/Invalidate.** KEN#/INV functions as both the KEN# signal during CPU read cycles, and the INV signal during L1 snoop cycles. During CPU cycles, KEN#/INV is normally low. KEN#/INV is driven high during the 1st BRDY# or NA# assertion of a non-L1-cacheable CPU read cycle. KEN#/INV is driven high(low) during the EADS# assertion of a PCI master DRAM write(read) snoop cycle. Note that KEN#/INV operation during snoop cycles is independent of the FLCE bit programming.
SMIACT#	I 3.3V/2.5V	**System Management Interrupt Active.** This is asserted by the CPU when it is in system management mode as a result of an SMI. This signal must be sampled active with ADS# for the processor to access the SMM space of DRAM, located at A0000h, after SMM space has been loaded and locked by BIOS at system boot.
HD[63:0]	I/O 3.3V/2.5V	**Host Data.** These signals are connected to the CPU data bus. These signals have internal pull-down resistors.

NOTES:
All of the signals in the host interface are described in the Pentium Processor data sheet. The preceding table highlights MTXC specific uses of these signals.

2.1.2. DRAM INTERFACE

Name	Type	Description
RAS[3:0]# Or CS[3:0]#, RAS4#/CS4#/ BA1, RAS5#/CS5#/ MA13	O 3.3V	**Row Address Strobe• ASx# (EDO/FPM).** These pins select the DRAM row. **Chip Select-CSx# (SDRAM).** These pins activate the SDRAMs. SDRAM accepts any command when its CS# pin is active low. Note: For 64Mbit SDRAM support, BA1/MA12 and MA13 are muxed with the RAS4# and RAS5# signals, respectively. When SDRAMC[bit 1]=1, BA1 and MA13 are driven out on these lines.
CAS[7:0]# or DQM[7:0]	O 3.3V	**Column Address Strobe (EDO/FPM).** These pins select the DRAM column. **Input/Output Data Mask SDRAM).** These pins act as synchronized output enables during a read cycle and a byte mask during a write cycle. The read cycles require Tdqz clock latency before the functions are actually performed. In case of a write cycle, word mask functions are performed in the same cycle (0 cycle latency).
MA[11:0]	O 3.3 V	**Memory Address (EDO/FPM/SDRAM).** This is the row and column address for DRAM. These buffers now include programmable size selection, as controlled by the DRAMEC[MAD] bit. For 64-Mbit SDRAM support BA1/MA12 and MA13 are muxed with the RAS4# and RAS5# signals, respectively.

3.3 INTEL FW82439TX MEMORY/PCI/CACHE CONTROLLER (MTXC)-2

Name	Type	Description
MWEB#	O 3.3 V	**Memory Write Enable (second copy) (EDO/FPM/SDRAM).** MWE# should be used as the write enable for the memory data bus. This signal has programmable buffer size selection.
MWE#	O 3.3 V	**Memory Write Enable (EDO/FPM/SDRAM).** MWE# should be used as the write enable for the memory data bus. This signal has programmable buffer size selection.
SRAS[A,B]#	O 3.3 V	**SDRAM Row Address Strobe (SDRAM).** When asserted, this signal latches Row Address on the positive edge of the clock. This signal also allows Row access and precharge. Two copies are provided for loading purpose. These signals have programmable buffer size selection.
SCAS[A,B]#	O 3.3 V	**SDRAM Column Address Strobe (SDRAM).** When asserted, this signal latches Column Address on the positive edge of the clock. This signal also allows Column access. Two copies provided for loading purpose. These signals have programmable buffer size selection.
CKE/MAA0	O 3.3 V	**SDRAM Clock Enable (SDRAM).** SDRAM clock enable pin. When this signal is negated, SDRAM enters power down mode. This signal is also muxed to provide a second copy of memory address MA0 (MAA0). The MA function is selected via DRT[bit2] (offset 67h). MTXC negates CKE (and CKEB) when SUSSTAT1# is asserted. Note that MTXC asserts CKE (and CKEB) for all rows (i.e., CKE and CKEB cannot be selectively asserted for certain rows and negated for other rows).
CKEB/MAA1	O 3.3 V	**SDRAM Clock Enable (SDRAM) (second copy).** SDRAM clock enable pin. When this signal is negated, SDRAM enters into power down mode. Note that this signal is not implemented in the • uspend Well?and should not be used if suspend to RAM (STR) is implemented. This signal is also muxed to provide a second copy of memory address MA1 (MAA1). The MA function is selected via DRT[bit2] (offset 67h). MTXC negates CKE (and CKEB) when SUSSTAT1# is asserted. Note that MTXC asserts CKE (and CKEB) for all rows (i.e., CKE and CKEB cannot be selectively asserted for certain rows and negated for other rows).
MD[63:0] 3.3V/5V	I/O	**Memory Data.** These signals are connected to the DRAM data bus. These signals have internal pull-down resistors

2.1.3. SECONDARY CACHE INTERFACE

Name	Type	Description
CADV#	O 3.3V	**Cache Advance.** Assertion causes the PBSRAM in the secondary cache to advance to the next QWord in the cache line.
CADS#	O 3.3V	**Cache Address Strobe.** Assertion causes the PBSRAM in the secondary cache to load the PBSRAM address register from the PBSRAM address pins.
CCS#	O 3.3V	**Cache Chip Select (CCS#).** The second level cache will power up, if necessary, and perform an access if this signal is asserted when CADS# is asserted. The second level cache will power down if this signal is negated when CADS# is asserted. When CCS# is negated the second level cache will ignore ADS#. If CCS# is asserted when ADS# is asserted, the second level cache will power up, if necessary, and perform an access.
COE#	O 3.3V	**Cache Output Enable.** The secondary cache data RAMs drive the CPUs data bus when COE# is asserted.
GWE#	O 3.3V	**Global Write Enable.** GWE# assertion causes all the byte lanes to be written into the secondary cache data RAMs, if they are powered up.
BWE#	O 3.3V	**Byte Write Enable.** Asserted low with GWE#=HIGH to enable using host• BE[7:0]# to be used to control byte lanes to pipeline burst SRAM cache.
TIO[7:0]	I/O 3.3V/5V	**Tag Address.** These are inputs during CPU accesses and outputs during second level cache line fills and second level cache line invalidates due to inquire cycles. These signals have internal pull-down resistors.
TWE#	O 3.3V	**Tag Write Enable.** When asserted, new state and tag addresses are written into the external tag.
KRQAK/ CS4_64#	I/O 3.3V	**KRQAK/Chip Select 4 (for 64-Mb Technology).** This pin is a dual-function signal. KRQAK is used in a DRAM Cache L2 implementation and is a bi-directional refresh request/acknowledge. The CS4_64# function is used to generate the fifth chip select line in a SDRAM L2 Cache implementation that supports five rows of 64-Mbit SDRAM. During a hard reset, this signal is sampled to determine if DRAM cache is in the system (see MTXC Strapping options). This signal has a weak internal pull-down. If SDRAMC[bit 1]=1 and DRAM cache is not present in the system (indicated by CEC[bit 5]=0, offset 53h), the CS4_64# function is selected. If DRAM cache is in the system or SDRAMC[bit 1] (offset 54h)=0, then KRQAK is used to drive the KRQAK function.

3.3 INTEL FW82439TX MEMORY/PCI/CACHE CONTROLLER (MTXC)-3

2.1.4. PCI INTERFACE

Name	Type	Description
AD[31:0]	I/O 3.3/5V	**Address/Data.** The standard PCI address and data lines. Address is driven with FRAME# assertion, data is driven or received in following clocks.
C/BE[3:0]#	I/O 3.3/5V	**Command/Byte Enable.** The command is driven with FRAME# assertion, byte enables corresponding to supplied or requested data is driven on following clocks
FRAME#	I/O 3.3/5V	**Frame.** Assertion indicates the address phase of a PCI transfer. Negation indicates that one more data transfer is desired by the cycle initiator.
DEVSEL#	I/O 3.3/5V	**Device Select.** This signal is driven by the MTXC when a PCI initiator is attempting to access DRAM. DEVSEL# is asserted at medium decode time.
IRDY#	I/O 3.3/5V	**Initiator Ready.** Asserted when the initiator is ready for a data transfer.
TRDY#	I/O 3.3/5V	**Target Ready.** Asserted when the target is ready for a data transfer.
STOP#	I/O 3.3/5V	**Stop.** Asserted by the target to request the master to stop the current transaction.
LOCK#	I/O 3.3/5V	**Lock.** Used to establish, maintain, and release resource locks on PCI.
REQ[3:0]#	I 3.3/5V	**PCI Request.** PCI master requests for PCI bus.
GNT[3:0]#	O 3.3V	**PCI Grant.** Permission is given to the master to use PCI.
PHLD#	I 3.3/5V	**PCI Hold.** This signal comes from the expansion bridge. It is the bridge request for PCI. The MTXC will drain the DRAM write buffers, drain the CPU-to-PCI posting buffers, and acquire the host bus before granting via PHLDA#.
PHLDA#	O 3.3V	**PCI Hold Acknowledge.** This signal is driven by the MTXC to grant PCI to the expansion bridge. PHLDA# protocol has been modified to include support for passive release.
PAR	I/O 3.3/5V	**Parity.** A single parity bit is provided over AD[31:0] and C/BE[3:0]. This signal should be pulled high through a weak external pull-up resistor.
CLKRUN#	I/O 3.3/5V	**CLOCK RUN.** An open drain output and also an input. MTXC requests the central resource (PIIX4) to start, or maintain the PCI clock by the assertion of CLKRUN#. MTXC will tri-state CLKRUN# upon negation of reset (since CLK is running upon negation of reset). External pull-up is required. Note: This signal should be connected to the PIIX4 CLKRUN# pin. However, if it is left as a no connect on the MTXC, it must be pulled low through a 100**W** (pull-down resistor.
RST#	I 3.3/5V	**Reset.** When asserted this signal asynchronously resets the MTXC. The PCI signals also tri-state compliant to PCI Rev 2.0 and 2.1 specifications.

2.1.5. TEST AND CLOCK

Name	Type	Description
TEST#	I 3.3/5V	**Test In.** NAND tree mode is activated by driving this pin low. The test mode selected depends on the state of REQ[3:0]#. This pin should be pulled high with an external pull-up during normal operation.
HCLKIN	I 3.3/2.5V	**Host Clock In.** This pin receives a buffered host clock. This clock is used by all of the MTXC logic that is in the Host clock domain.
PCLKIN	I 3.3/5V	**PCI Clock In.** This pin receives a buffered divide-by-2 host clock. This clock is used by all of the MTXC logic that is in the PCI clock domain.

2.1.6. POWER MANAGEMENT

Name	Type	Description
SUSCLK	I 3.3V	**Suspend Clock.** The signal is a 32 KHz input for DRAM refresh circuitry and clocking events in suspend state. The DRAM refresh during suspend and non-suspend states is performed based on this clock. This signal has an internal pull-down resistor.
SUSSTAT1#	I 3.3V	**Suspend Status.** SUSSTAT1# indicates MTXC• power plane status during suspend mode. SUSSTAT1#, along with SUSCLK and RST#, define the suspend protocol between MTXC and PIIX4. This signal has an internal pull-up resistor.

2.1.7. POWER AND GROUND PINS

Name	Type	Description
VCC	3.3V	**Main voltage supply.** These pins are the primary voltage supply for the MTXC core and I/O periphery and must be connected to 3.3V.
VCC (CPU)	3.3V or 2.5V	**CPU Interface Voltage Supply.** These pins are the primary voltage supply for the MTXC Host periphery and must be connected to either 2.5V or 3.3V, depending on the oltage level of the CPU interface. Refer to the Power sequencing requirements section for additional details.
VCC (SUS)	3.3V	**Suspend Well Voltage Supply.** These pins are the primary voltage supply for the MTXC suspend logic and I/O. If suspend to RAM is supported, these pins should be on an isolated power plane; otherwise, they can be connected to the same 3.3V source used for the VCC pins.
VCC5REF	3.3V or 5V	**Voltage Reference.** This pin is tied to 5V through a small external power sequencing circuit, if MTXC signals are required to be 5V Tolerant. In a non 5V tolerant system (i.e. 3.3V only system), this signal can be tied directly to VCC. Refer to the Power sequencing requirements section for additional details.
VSS	0V	**Ground.** These pins are the ground for the MTXC.

3.3 INTEL FW82439TX MEMORY/PCI/CACHE CONTROLLER (MTXC)-4

2.2. MTXC Strapping Options

Name	Type	Description
SCS	A[31:30]	**Secondary Cache Size.** Described in the Cache Control Register bits 7:6.
L2RAMT	A[29:28]	**Initial L2 RAM Type.** Described in the Cache Control Register bits 5:4.
DRAM Cache	KRQAK	**DRAM Cache L2 Present Upon Reset Negation.** This bit is sampled to detect DRAM L2 cache. If sampled high, a DRAM Cache is present. A weak pulldown is provided internally. A DRAM cache module should implement a pull-up on this pin that overrides the weak pulldown. BIOS does not have to be aware of this, this information is used by the MTXC to maintain optimal Pburst timings.
25VD	A26	**2.5V Voltage Detection.** This bit is used to determine the voltage level (3.3V or 2.5V)of the host clock connected to the host clock pin and the voltage on the VCC(CPU)pins. An external pull-down or pull-up resistor is required on this pin (pulled down for 2.5V and pulled up for 3.3V).
HFD	A27	**Frequency Detection.** BIOS can use this bit to determine if the system is 60 MHz (external pull-up) or 66 MHz (no strapping is present) as described in the DRTH Register, bit 7. DRTH[bit 7] register is initialized with the inverted value of pin A27 upon reset negation. The A27 input buffer includes a weak pulldown resistor which will force DRTH[bit 7] to default to 1 if no strapping is present.

3.4 INTEL FW82371AB PCI/ISA BRIDGE (PIIX4)-1

PIIX4 Signals PCI BUS INTERFACE

Name	Type	Description
AD[31:0]	I/O	**PCI ADDRESS/DATA.** AD[31:0] is a multiplexed address and data bus. During the first clock of a transaction, AD[31:0] contain a physical byte address (32 bits). During subsequent clocks, AD[31:0] contain data. A PIIX4 Bus transaction consists of an address phase followed by one or more data phases. Little-endian byte ordering is used. AD[7:0] define the least significant byte (LSB) and AD[31:24] the most significant byte (MSB). When PIIX4 is a Target, AD[31:0] are inputs during the address phase of a transaction. During the following data phase(s), PIIX4 may be asked to supply data on AD[31:0] for a PCI read, or accept data for a PCI write. As an Initiator, PIIX4 drives a valid address on AD[31:2] and 0 on AD[1:0] during the address phase, and drives write or latches read data on AD[31:0] during the data phase. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
C/BE#[3:0]	I/O	**BUS COMMAND AND BYTE ENABLES.** The command and byte enable signals are multiplexed on the same PCI pins. During the address phase of a transaction, C/BE[3:0]# define the bus command. During the data phase C/BE[3:0]# are used as Byte Enables. The Byte Enables determine which byte lanes carry meaningful data. C/BE0# applies to byte 0, C/BE1# to byte 1, etc. PIIX4 drives C/BE[3:0]# as an Initiator and monitors C/BE[3:0]# as a Target. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
CLKRUN#	I/O	**CLOCK RUN#.** This signal is used to communicate to PCI peripherals that the PCI clock will be stopped. Peripherals can assert CLKRUN# to request that the PCI clock be restarted or to keep it from stopping. This function follows the protocol described in the PCI Mobile Design Guide, Revision 1.0. **During Reset:** Low **After Reset:** Low **During POS:** High
DEVSEL#	I/O	**DEVICE SELECT.** PIIX4 asserts DEVSEL# to claim a PCI transaction through positive decoding or subtractive decoding (if enabled). As an output, PIIX4 asserts DEVSEL# when it samples IDSEL active in configuration cycles to PIIX4 configuration registers. PIIX4 also asserts DEVSEL# when an internal PIIX4 address is decoded or when PIIX4 subtractively or positively decodes a cycle for the ISA/EIO bus or IDE device. As an input, DEVSEL# indicates the response to a PIIX4 initiated transaction and is also sampled when deciding whether to subtractively decode the cycle. DEVSEL# is tri-stated from the leading edge of PCIRST#. DEVSEL# remains tri-stated until driven by PIIX4 as a target. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
FRAME#	I/O	**CYCLE FRAME.** FRAME# is driven by the current Initiator to indicate the beginning and duration of an access. While FRAME# is asserted data transfers continue. When FRAME# is negated the transaction is in the final data phase. FRAME# is an input to PIIX4 when it is the Target. FRAME# is an output when PIIX4 is the initiator. FRAME# remains tri-stated until driven by PIIX4 as an Initiator. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z

Name	Type	Description
IDSEL	I	**INITIALIZATION DEVICE SELECT.** IDSEL is used as a chip select during PCI configuration read and write cycles. PIIX4 samples IDSEL during the address phase of a transaction. If IDSEL is sampled active, and the bus command is a configuration read or write, PIIX4 responds by asserting DEVSEL# on the next cycle.
IRDY#	I/O	**INITIATOR READY.** IRDY# indicates PIIX4• ability, as an Initiator, to complete the current data phase of the transaction. It is used in conjunction with TRDY#. A data phase is completed on any clock both IRDY# and TRDY# are sampled asserted. During a write, IRDY# indicates PIIX4 has valid data present on AD[31:0]. During a read, it indicates PIIX4 is prepared to latch data. IRDY# is an input to PIIX4 when PIIX4 is the Target and an output when PIIX4 is an Initiator. IRDY# remains tri-stated until driven by PIIX4 as a master. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
PAR	O	**CALCULATED PARITY SIGNAL.** PAR is • ven?parity and is calculated on 36 bits; AD[31:0] plus C/BE[3:0]#. • ven?parity means that the number of ?• within the 36 bits plus PAR are counted and the sum is always even. PAR is always calculated on 36 bits regardless of the valid byte enables. PAR is generated for address and data phases and is only guaranteed to be valid one PCI clock after the corresponding address or data phase. PAR is driven and tri-stated identically to the AD[31:0] lines except that PAR is delayed by exactly one PCI clock. PAR is an output during the address phase (delayed one clock) for all PIIX4 initiated transactions. It is also an output during the data phase (delayed one clock) when PIIX4 is the Initiator of a PCI write transaction, and when it is the Target of a read transaction. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
PCIRST#	O	**PCI RESET.** PIIX4 asserts PCIRST# to reset devices that reside on the PCI bus. PIIX4 asserts PCIRST# during power-up and when a hard reset sequence is initiated through the RC register. PCIRST# is driven inactive a minimum of 1 ms after PWROK is driven active. PCIRST# is driven for a minimum of 1 ms when initiated through the RC register. PCIRST# is driven asynchronously relative to PCICLK. **During Reset:** Low **After Reset:** High **During POS:** High
PHOLD#	O	**PCI HOLD.** An active low assertion indicates that PIIX4 desires use of the PCI Bus. Once the PCI arbiter has asserted PHLDA# to PIIX4, it may not negate it until PHOLD# is negated by PIIX4. PIIX4 implements the passive release mechanism by toggling PHOLD# inactive for one PCICLK. **During Reset:** High-Z **After Reset:** High **During POS:** High
PHLDA#	I	**PCI HOLD ACKNOWLEDGE.** An active low assertion indicates that PIIX4 has been granted use of the PCI Bus. Once PHLDA# is asserted, it cannot be negated unless PHOLD# is negated first.
SERR#	I/O	**SYSTEM ERROR.** SERR# can be pulsed active by any PCI device that detects a system error condition. Upon sampling SERR# active, PIIX4 can be programmed to generate a non-maskable interrupt (NMI) to the CPU. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z

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Name	Type	Description
STOP#	I/O	**STOP.** STOP# indicates that PIIX4, as a Target, is requesting an initiator to stop the current transaction. As an Initiator, STOP# causes PIIX4 to stop the current transaction. STOP# is an output when PIIX4 is a Target and an input when PIIX4 is an Initiator. STOP# is tri-stated from the leading edge of PCIRST#. STOP# remains tri-stated until driven by PIIX4 as a slave. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
TRDY#	I/O	**TARGET READY.** TRDY# indicates PIIX4• ability to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#. A data phase is completed when both TRDY# and IRDY# are sampled asserted. During a read, TRDY# indicates that PIIX4, as a Target, has place valid data on AD[31:0]. During a write, it indicates PIIX4, as a Target is prepared to latch data. TRDY# is an input to PIIX4 when PIIX4 is the Initiator and an output when PIIX4 is a Target. TRDY# is tri-stated from the leading edge of PCIRST#. TRDY# remains tri-stated until driven by PIIX4 as a slave. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z

NOTES:
All of the signals in the host interface are described in the Pentium Processor data sheet. The preceding table highlights PIIX4 specific uses of these signals.

2.1.2. ISA BUS INTERFACE

Name	Type	Description
AEN	O	**ADDRESS ENABLE.** AEN is asserted during DMA cycles to prevent I/O slaves from misinterpreting DMA cycles as valid I/O cycles. When negated, AEN indicates that an I/O slave may respond to address and I/O commands. When asserted, AEN informs I/O resources on the ISA bus that a DMA transfer is occurring. This signal is also driven high during PIIX4 initiated refresh cycles. **During Reset:** High-Z **After Reset:** Low **During POS:** Low
BALE	O	**BUS ADDRESS LATCH ENABLE.** BALE is asserted by PIIX4 to indicate that the address (SA[19:0], LA[23:17]) and SBHE# signal lines are valid. The LA[23:17] address lines are latched on the trailing edge of BALE. BALE remains asserted throughout DMA and ISA master cycles. **During Reset:** High-Z **After Reset:** Low **During POS:** Low
IOCHK#/I GPI0	**I/O**	**CHANNEL CHECK.** IOCHK# can be driven by any resource on the ISA bus. When asserted, it indicates that a parity or an uncorrectable error has occurred for a device or memory on the ISA bus. A NMI will be generated to the CPU if the NMI generation is enabled. If the EIO bus is used, this signal becomes a general purpose input.

Name	Type	Description
IOCHRDY	I/O	**I/O CHANNEL READY.** Resources on the ISA Bus negate IOCHRDY to indicate that wait states are required to complete the cycle. This signal is normally high. IOCHRDY is an input when PIIX4 owns the ISA Bus and the CPU or a PCI agent is accessing an ISA slave, or during DMA transfers. IOCHRDY is output when an external ISA Bus Master owns the ISA Bus and is accessing DRAM or a PIIX4 register. As a PIIX4 output, IOCHRDY is driven inactive (low) from the falling edge of the ISA commands. After data is available for an ISA master read or PIIX4 latches the data for a write cycle, IOCHRDY is asserted for 70 ns. After 70 ns, PIIX4 floats IOCHRDY. The 70 ns includes both the drive time and the time it takes PIIX4 to float IOCHRDY. PIIX4 does not drive this signal when an ISA Bus master is accessing an ISA Bus slave. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
IOCS16#	I	**16-BIT I/O CHIP SELECT.** This signal is driven by I/O devices on the ISA Bus to indicate support for 16-bit I/O bus cycles.
IOR#	I/O	**I/O READ.** IOR# is the command to an ISA I/O slave device that the slave may drive data on to the ISA data bus (SD[15:0]). The I/O slave device must hold the data valid until after IOR# is negated. IOR# is an output when PIIX4 owns the ISA Bus. IOR# is an input when an external ISA master owns the ISA Bus. **During Reset:** High-Z **After Reset:** High **During POS:** High
IOW#	I/O	**I/O WRITE.** IOW# is the command to an ISA I/O slave device that the slave may latch data from the ISA data bus (SD[15:0]). IOW# is an output when PIIX4 owns the ISA Bus. IOW# is an input when an external ISA master owns the ISA Bus. **During Reset:** High-Z **After Reset:** High **During POS:** High
LA[23:17]/ GPO[7:1]	I/O	**ISA LA[23:17].** LA[23:17] address lines allow accesses to physical memory on the ISA Bus up to 16 Mbytes. LA[23:17] are outputs when PIIX4 owns the ISA Bus. The LA[23:17] lines become inputs whenever an ISA master owns the ISA Bus. If the EIO bus is used, these signals become a general purpose output. **During Reset:** High-Z **After Reset:** Undefined **During POS:** Last LA/GPO
MEMCS16#	I/O	**MEMORY CHIP SELECT 16.** MEMCS16# is a decode of LA[23:17] without any qualification of the command signal lines. ISA slaves that are 16-bit memory devices drive this signal low. PIIX4 ignores MEMCS16# during I/O access cycles and refresh cycles. MEMCS16# is an input when PIIX4 owns the ISA Bus. PIIX4 drives this signal low during ISA master to PCI memory cycles. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
MEMR#	I/O	**MEMORY READ.** MEMR# is the command to a memory slave that it may drive data onto the ISA data bus. MEMR# is an output when PIIX4 is a master on the ISA Bus. MEMR# is an input when an ISA master, other than PIIX4, owns the ISA Bus. This signal is also driven by PIIX4 during refresh cycles. For DMA cycles, PIIX4, as a master, asserts MEMR#. **During Reset:** High-Z **After Reset:** High **During POS:** High

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Name	Type	Description
MEMW#	I/O	**MEMORY WRITE.** MEMW# is the command to a memory slave that it may latch data from the ISA data bus. MEMW# is an output when PIIX4 owns the ISA Bus. MEMW# is an input when an ISA master, other than PIIX4, owns the ISA Bus. For DMA cycles, PIIX4, as a master, asserts MEMW#. **During Reset:** High-Z **After Reset:** High **During POS:** High
REFRESH#	I/O	**REFRESH.** As an output, REFRESH# is used by PIIX4 to indicate when a refresh cycle is in progress. It should be used to enable the SA[7:0] address to the row address inputs of all banks of dynamic memory on the ISA Bus. Thus, when MEMR# is asserted, the entire expansion bus dynamic memory is refreshed. Memory slaves must not drive any data onto the bus during refresh. As an output, this signal is driven directly onto the ISA Bus. This signal is an output only when PIIX4 DMA refresh controller is a master on the bus responding to an internally generated request for refresh. As an input, REFRESH# is driven by 16-bit ISA Bus masters to initiate refresh cycles. **During Reset:** High-Z **After Reset:** High **During POS:** High
RSTDRV	O	**RESET DRIVE.** PIIX4 asserts RSTDRV to reset devices that reside on the ISA/EIO Bus. PIIX4 asserts this signal during a hard reset and during power-up. RSTDRV is asserted during power-up and negated after PWROK is driven active. RSTDRV is also driven active for a minimum of 1 ms if a hard reset has been programmed in the RC register. **During Reset:** High **After Reset:** Low **During POS:** Low
SA[19:0]	I/O	**SYSTEM ADDRESS[19:0].** These bi-directional address lines define the selection with the granularity of 1 byte within the 1-Megabyte section of memory defined by the LA[23:17] address lines. The address lines SA[19:17] that are coincident with LA[19:17] are defined to have the same values as LA[19:17] for all memory cycles. For I/O accesses, only SA[15:0] are used, and SA[19:16] are undefined. SA[19:0] are outputs when PIIX4 owns the ISA Bus. SA[19:0] are inputs when an external ISA Master owns the ISA Bus. **During Reset:** High-Z **After Reset:** Undefined **During POS:** Last SA
SBHE#	I/O	**SYSTEM BYTE HIGH ENABLE.** SBHE# indicates, when asserted, that a byte is being transferred on the upper byte (SD[15:8]) of the data bus. SBHE# is negated during refresh cycles. SBHE# is an output when PIIX4 owns the ISA Bus. SBHE# is an input when an external ISA master owns the ISA Bus. **During Reset:** High-Z **After Reset:** Undefined **During POS:** High
SD[15:0]	I/O	**SYSTEM DATA.** SD[15:0] provide the 16-bit data path for devices residing on the ISA Bus. SD[15:8] correspond to the high order byte and SD[7:0] correspond to the low order byte. SD[15:0] are undefined during refresh. **During Reset:** High-Z **After Reset:** Undefined **During POS:** High-Z
SMEMR#	O	**STANDARD MEMORY READ.** PIIX4 asserts SMEMR# to request an ISA memory slave to drive data onto the data lines. If the access is below the 1-Mbyte range (00000000h?00FFFFFh) during DMA compatible, PIIX4 master, or ISA master cycles, PIIX4 asserts SMEMR#. SMEMR# is a delayed version of MEMR#. **During Reset:** High-Z **After Reset:** High **During POS:** High

Name	Type	Description
SMEMW#	O	**STANDARD MEMORY WRITE.** PIIX4 asserts SMEMW# to request an ISA memory slave to accept data from the data lines. If the access is below the 1-Mbyte range (00000000h?00FFFFFh) during DMA compatible, PIIX4 master, or ISA master cycles, PIIX4 asserts SMEMW#. SMEMW# is a delayed version of MEMW#. **During Reset:** High-Z **After Reset:** High **During POS:** High
ZEROWS#	I	**ZERO WAIT STATES.** An ISA slave asserts ZEROWS# after its address and command signals have been decoded to indicate that the current cycle can be shortened. A 16-bit ISA memory cycle can be reduced to two SYSCLKs. An 8-bit memory or I/O cycle can be reduced to three SYSCLKs. ZEROWS# has no effect during 16-bit I/O cycles. If IOCHRDY is negated and ZEROWS# is asserted during the same clock, then ZEROWS# is ignored and wait states are added as a function of IOCHRDY.

2.1.3. X-BUS INTERFACE

Name	Type	Description
A20GATE	I	**ADDRESS 20 GATE.** This input from the keyboard controller is logically combined with bit 1 (FAST_A20) of the Port 92 Register, which is then output via the A20M# signal.
BIOSCS#	O	**BIOS CHIP SELECT.** This chip select is driven active during read or write accesses to enabled BIOS memory ranges. BIOSCS# is driven combinatorially from the ISA addresses SA[16:0] and LA[23:17], except during DMA cycles. During DMA cycles, BIOSCS# is not generated. **During Reset:** High **After Reset:** High **During POS:** High
KBCCS#/ GPO26	O	**KEYBOARD CONTROLLER CHIP SELECT.** KBCCS# is asserted during I/O read or write accesses to KBC locations 60h and 64h. It is driven combinatorially from the ISA addresses SA[19:0] and LA[23:17]. If the keyboard controller does not require a separate chip select, this signal can be programmed to a general purpose output. **During Reset:** High **After Reset:** High **During POS:** High/GPO
MCCS#	O	**MICROCONTROLLER CHIP SELECT.** MCCS# is asserted during I/O read or write accesses to IO locations 62h and 66h. It is driven combinatorially from the ISA addresses SA[19:0] and LA[23:17]. **During Reset:** High **After Reset:** High **During POS:** High
PCS0# **PCS1#**	O	**PROGRAMMABLE CHIP SELECTS.** These active low chip selects are asserted for ISA I/O cycles which are generated by PCI masters and which hit the programmable I/O ranges defined in the Power Management section. The X-Bus buffer signals (XOE# and XDIR#) are enabled while the chip select is active. (i.e., it is assumed that the peripheral which is selected via this pin resides on the X-Bus.) **During Reset:** High **After Reset:** High **During POS:** High
RCIN#	I	**RESET CPU.** This signal from the keyboard controller is used to generate an INIT signal to the CPU.

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Name	Type	Description
RTCALE/	O	**REAL TIME CLOCK ADDRESS LATCH ENABLE.** RTCALE is used to latch the GPO25appropriate memory address into the RTC. A write to port 70h with the appropriate RTC memory address that will be written to or read from causes RTCALE to be asserted. RTCALE is asserted on falling IOW# and remains asserted for two SYSCLKs. If the internal Real Time Clock is used, this signal can be programmed as a general purpose output. **During Reset:** Low **After Reset:** Low **During POS:** Low/GPO
RTCCS#/ GPO24	O	**REAL TIME CLOCK CHIP SELECT.** RTCCS# is asserted during read or write I/O accesses to RTC location 71h. RTCCS# can be tied to a pair of external OR gates to generate the real time clock read and write command signals. If the internal Real Time Clock is used, this signal can be programmed as a general purpose output. **During Reset:** High **After Reset:** High **During POS:** High/GPO
XDIR#/ GPO22	O	**X-BUS TRANSCEIVER DIRECTION.** XDIR# is tied directly to the direction control of a 74?45 that buffers the X-Bus data, XD[7:0]. XDIR# is asserted (driven low) for all I/O read cycles regardless if the accesses is to a PIIX4 supported device. XDIR# is asserted for memory cycles only if BIOS or APIC space has been decoded. For PCI master initiated read cycles, XDIR# is asserted from the falling edge of either IOR# or MEMR# (from MEMR# only if BIOS or APIC space has been decoded), depending on the cycle type. For ISA master-initiated read cycles, XDIR# is asserted from the falling edge of either IOR# or MEMR# (from MEMR# only if BIOS space has been decoded), depending on the cycle type. When the rising edge of IOR# or MEMR# occurs, PIIX4 negates XDIR#. For DMA read cycles from the X-Bus, XDIR# is driven low from DACKx# falling and negated from DACKx# rising. At all other times, XDIR# is negated high. If the X-Bus not used, then this signal can be programmed to be a general purpose output. **During Reset:** High **After Reset:** High **During POS:** High/GPO
XOE#/ GPO23	O	**X-BUS TRANSCEIVER OUTPUT ENABLE.** XOE# is tied directly to the output enable of a 74?45 that buffers the X-Bus data, XD[7:0], from the system data bus, SD[7:0]. XOE# is asserted anytime a PIIX4 supported X-Bus device is decoded, and the devices decode is enabled in the X-Bus Chip Select Enable Register (BIOSCS#, KBCCS#, RTCCS#, MCCS#) or the Device Resource B (PCCS0#) and Device Resource C (PCCS1#). XOE# is asserted from the falling edge of the ISA commands (IOR#, IOW#, MEMR#, or MEMW#) for PCI Master and ISA master-initiated cycles. XOE# is negated from the rising edge of the ISA command signals for PCI Master initiated cycles and the SA[16:0] and LA[23:17] address for ISA master-initiated cycles. XOE# is not generated during any access to an X-Bus peripheral in which its decode space has been disabled. If an X-Bus not used, then this signal can be programmed to be a general purpose output. **During Reset:** High **After Reset:** High **During POS:** High/GPO

2.1.4. DMA SIGNALS

Name	Type	Description
DACK[0,1,2,3]# DACK[5,6,7]#	O	**DMA ACKNOWLEDGE.** The DACK# output lines indicate that a request for DMA service has been granted by PIIX4 or that a 16-bit master has been granted the bus. The active level (high or low) is programmed via the DMA Command Register. These lines should be used to decode the DMA slave device with the IOR# or IOW# line to indicate selection. If used to signal acceptance of a bus master request, this signal indicates when it is legal to assert MASTER#. If the DREQ goes inactive prior to DACK# being asserted, the DACK# signal will not be asserted. **During Reset:** High **After Reset:** High **During POS:** High
DREQ[0,1,2,3] DREQ[5,6,7]	I	**DMA REQUEST.** The DREQ lines are used to request DMA service from PIIX4 DMA controller or for a 16-bit master to gain control of the ISA expansion bus. The active level (high or low) is programmed via the DMA Command Register. All inactive to active edges of DREQ are assumed to be asynchronous. The request must remain active until the appropriate DACKx# signal is asserted.
REQ[A:C]#/ GPI[2:4]	I	**PC/PCI DMA REQUEST.** These signals are the DMA requests for PC/PCI protocol. They are used by a PCI agent to request DMA services and follow the PCI Expansion Channel Passing protocol as defined in the *PCI DMA* section. If the PC/PCI request is not needed, these pins can be used as general-purpose inputs.
GNT[A:C]#/ GPO[9:11]	O	**PC/PCI DMA ACKNOWLEDGE.** These signals are the DMA grants for PC/PCI protocol. They are used by a PIIX4 to acknowledge DMA services and follow the PCI Expansion Channel Passing protocol as defined in the *PCI DMA* section. If the PC/PCI request is not needed, these pins can be used as general-purpose outputs. **During Reset:** High **After Reset:** High **During POS:** High/GPO
TC	O	**TERMINAL COUNT.** PIIX4 asserts TC to DMA slaves as a terminal count indicator. PIIX4 asserts TC after a new address has been output, if the byte count expires with that transfer. TC remains asserted until AEN is negated, unless AEN is negated during an autoinitialization. TC is negated before AEN is negated during an autoinitialization. **During Reset:** Low **After Reset:** Low **During POS:** Low

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2.1.5. INTERRUPT CONTROLLER/APIC SIGNALS

Name	Type	Description
APICACK#/ GPO12	O	**APIC ACKNOWLEDGE.** This active low output signal is asserted by PIIX4 after its internal buffers are flushed in response to the APICREQ# signal. When the I/O APIC samples this signal asserted it knows that PIIX4• buffers are flushed and that it can proceed to send the APIC interrupt. The APICACK# output is synchronous to PCICLK. If the external APIC is not used, then this is a general-purpose output. **During Reset:** High **After Reset:** High **During POS:** High/GPO
APICCS#/ GPO13	O	**APIC CHIP SELECT.** This active low output signal is asserted when the APIC Chip Select is enabled and a PCI originated cycle is positively decoded within the programmed I/O APIC address space. If the external APIC is not used, this pin is a general-purpose output. **During Reset:** High **After Reset:** High **During POS:** High/GPO
APICREQ#/ GPI5	I	**APIC REQUEST.** This active low input signal is asserted by an external APIC device prior to sending an interrupt over the APIC serial bus. When PIIX4 samples this pin active it will flush its F-type DMA buffers pointing towards PCI. Once the buffers are flushed, PIIX4 asserts APICACK# which indicates to the external APIC that it can proceed to send the APIC interrupt. The APICREQ# input must be synchronous to PCICLK. If the external APIC is not used, this pin is a general-purpose input. **INTR** OD **INTERRUPT.** See CPU Interface Signals.
IRQ0/	O	**INTERRUPT REQUEST 0.** This output reflects the state of the internal IRQ0 signal GPO14 from the system timer. If the external APIC is not used, this pin is a general-purpose output. **During Reset:** Low **After Reset:** Low **During POS:** IRQ0/GPO
IRQ1	I	**INTERRUPT REQUEST 1.** IRQ1 is always edge triggered and can not be modified by software to level sensitive. A low to high transition on IRQ1 is latched by PIIX4. IRQ1 must remain asserted until after the interrupt is acknowledged. If the input goes inactive before this time, a default IRQ7 is reported in response to the interrupt acknowledge cycle.
IRQ 3:7, 9:11, 14:15	I	**INTERRUPT REQUESTS 3:7, 9:11, 14:15.** The IRQ signals provide both system board components and ISA Bus I/O devices with a mechanism for asynchronously interrupting the CPU. These interrupts may be programmed for either an edge sensitive or a high level sensitive assertion mode. Edge sensitive is the default configuration. An active IRQ input must remain asserted until after the interrupt is acknowledged. If the input goes inactive before this time, a default IRQ7 is reported in response to the interrupt acknowledge cycle.

Name	Type	Description
IRQ8#/ GPI6	I/O	**IRQ 8#.** IRQ8# is always an active low edge triggered interrupt and can not be modified by software. IRQ8# must remain asserted until after the interrupt is acknowledged. If the input goes inactive before this time, a default IRQ7 is reported in response to the interrupt acknowledge cycle. If using the internal RTC, then this can be programmed as a general-purpose input. If enabling an APIC, this signal becomes an output and must not be programmed as a general purpose input.
IRQ9OUT#/ GPO29	O	**IRQ9OUT#.** IRQ9OUT# is used to route the internally generated SCI and SMBus interrupts out of the PIIX4 for connection to an external IO APIC. If APIC is disabled, this signal pin is a General Purpose Output. **During Reset:** High **After Reset:** High **During POS:** IRQ9OUT#/GPO
IRQ 12/M	I	**INTERRUPT REQUEST 12.** In addition to providing the standard interrupt function as described in the pin description for IRQ[3:7,9:11,14:15], this pin can also be programmed to provide the mouse interrupt function. When the mouse interrupt function is selected, a low to high transition on this signal is latched by PIIX4 and an INTR is generated to the CPU as IRQ12. An internal IRQ12 interrupt continues to be generated until a Reset or an I/O read access to address 60h (falling edge of IOR#) is detected.
PIRQ[A:D]#	I/OD PCI	**PROGRAMMABLE INTERRUPT REQUEST.** The PIRQx# signals are active low, level sensitive, shareable interrupt inputs. They can be individually steered to ISA interrupts IRQ [3:7,9:12,14:15]. The USB controller uses PIRQD# as its output signal.
SERIRQ/ GPI7	I/O	**SERIAL INTERRUPT REQUEST.** Serial interrupt input decoder, typically used in conjunction with the Distributed DMA protocol. If not using serial interrupts, this pin can be used as a general-purpose input.

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2.1.6. CPU INTERFACE SIGNALS

Name	Type	Description
A20M#	OD	**ADDRESS 20 MASK.** PIIX4 asserts A20M# to the CPU based on combination of Port 92 Register, bit 1 (FAST_A20), and A20GATE input signal. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
CPURST	OD	**CPU RESET.** PIIX4 asserts CPURST to reset the CPU. PIIX4 asserts CPURST during power-up and when a hard reset sequence is initiated through the RC register. CPURST is driven inactive a minimum of 2 ms after PWROK is driven active. CPURST is driven active for a minimum of 2 ms when initiated through the RC register. The inactive edge of CPURST is driven synchronously to the rising edge of PCICLK. If a hard reset is initiated through the RC register, PIIX4 resets its internal registers (in both core and suspend wells) to their default state. This signal is active high for Pentium processor and active-low for Pentium II processor as determined by CONFIG1 signal. For values **During Reset**, **After Reset**, and **During POS**, see the *Suspend/Resume and Resume Control Signaling* section.
FERR#	I	**NUMERIC COPROCESSOR ERROR.** This pin functions as a FERR# signal supporting coprocessor errors. This signal is tied to the coprocessor error signal on the CPU. If FERR# is asserted, PIIX4 generates an internal IRQ13 to its interrupt controller unit. PIIX4 then asserts the INT output to the CPU. FERR# is also used to gate the IGNNE# signal to ensure that IGNNE# is not asserted to the CPU unless FERR# is active.
IGNNE#	OD	**IGNORE NUMERIC EXCEPTION.** This signal is connected to the ignore numeric exception pin on the CPU. IGNNE# is only used if the PIIX4 coprocessor error reporting function is enabled. If FERR# is active, indicating a coprocessor error, a write to the Coprocessor Error Register (F0h) causes the IGNNE# to be asserted. IGNNE# remains asserted until FERR# is negated. If FERR# is not asserted when the Coprocessor Error Register is written, the IGNNE# signal is not asserted. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
INIT	OD	**INITIALIZATION.** INIT is asserted in response to any one of the following conditions. When the System Reset bit in the Reset Control Register is reset to 0 and the Reset CPU bit toggles from 0 to 1, PIIX4 initiates a soft reset by asserting INIT. PIIX4 also asserts INIT if a Shut Down Special cycle is decoded on the PCI Bus, if the RCIN# signal is asserted, or if a write occurs to Port 92h, bit 0. When asserted, INIT remains asserted for approximately 64 PCI clocks before being negated. This signal is active high for Pentium processor and active-low for Pentium II processor as determined by CONFIG1 signal. **Pentium Processor:** **During Reset:** Low **After Reset:** Low **During POS:** Low **Pentium II Processor:** **During Reset:** High **After Reset:** High **During POS:** High
INTR	OD	**CPU INTERRUPT.** INTR is driven by PIIX4 to signal the CPU that an interrupt request is pending and needs to be serviced. It is asynchronous with respect to SYSCLK or PCICLK and is always an output. The interrupt controller must be programmed following PCIRST# to ensure that INTR is at a known state. **During Reset:** Low **After Reset:** Low **During POS:** Low

Name	Type	Description
NMI	OD	**NON-MASKABLE INTERRUPT.** NMI is used to force a nonmaskable interrupt to the CPU. PIIX4 generates an NMI when either SERR# or IOCHK# is asserted, depending on how the NMI Status and Control Register is programmed. The CPU detects an NMI when it detects a rising edge on NMI. After the NMI interrupt routine processes the interrupt, the NMI status bits in the NMI Status and Control Register are cleared by software. The NMI interrupt routine must read this register to determine the source of the interrupt. The NMI is reset by setting the corresponding NMI source enable/disable bit in the NMI Status and Control Register. To enable NMI interrupts, the two NMI enable/disable bits in the register must be set to 0, and the NMI mask bit in the NMI Enable/Disable and Real Time Clock Address Register must be set to 0. Upon PCIRST#, this signal is driven low. **During Reset:** Low **After Reset:** Low **During POS:** Low
SLP#	OD	**SLEEP.** This signal is output to the Pentium II processor in order to put it into Sleep state. For Pentium processor it is a No Connect. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
SMI#	OD	**SYSTEM MANAGEMENT INTERRUPT.** SMI# is an active low synchronous output that is asserted by PIIX4 in response to one of many enabled hardware or software events. The CPU recognizes the falling edge of SMI# as the highest priority interrupt in the system, with the exception of INIT, CPURST, and FLUSH. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
STPCLK#	OD	**STOP CLOCK.** STPCLK# is an active low synchronous output that is asserted by PIIX4 in response to one of many hardware or software events. STPCLK# connects directly to the CPU and is synchronous to PCICLK. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z

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2.1.7. CLOCKING SIGNALS

Name	Type	Description
CLK48	I	**48-MHZ CLOCK.** 48-MHz clock used by the internal USB host controller. This signal may be stopped during suspend modes.
PCICLK	I	**FREE-RUNNING PCI CLOCK.** A clock signal running at 30 or 33 MHz, PCICLK provides timing for all transactions on the PCI Bus. All other PCI signals are sampled on the rising edge of PCICLK, and all timing parameters are defined with respect to this edge. Because many of the circuits in PIIX4 run off the PCI clock, this signal MUST be kept active, even if the PCI bus clock is not active.
OSC	I	**14.31818-MHZ CLOCK.** Clock signal used by the internal 8254 timer. This clock signal may be stopped during suspend modes.
RTCX1, RTCX2	I/O	**RTC CRYSTAL INPUTS:** These connected directly to a 32.768-kHz crystal. External capacitors are required. These clock inputs are required even if the internal RTC is not being used.
SUSCLK	O	**SUSPEND CLOCK.** 32.768-kHz output clock provided to the Host-to-PCI bridge used for maintenance of DRAM refresh. This signal is stopped during Suspend-to-Disk and Soft Off modes. For values During Reset, After Reset, and During POS, see the *Suspend/Resume and Resume Control Signaling* section.
SYSCLK	O	**ISA SYSTEM CLOCK.** SYSCLK is the reference clock for the ISA bus. It drives the ISA bus directly. The SYSCLK is generated by dividing PCICLK by 4. The SYSCLK frequencies supported are 7.5 MHz and 8.33 MHz. For PCI accesses to the ISA bus, SYSCLK may be stretched low to synchronize BALE falling to the rising edge of SYSCLK. **During Reset:** Running **After Reset:** Running **During POS:** Low

2.1.8. IDE SIGNALS

Name	Type	Description
PDA[2:0]	O	**PRIMARY DISK ADDRESS[2:0].** These signals indicate which byte in either the ATA command block or control block is being addressed. If the IDE signals are configured for Primary and Secondary, these signals are connected to the corresponding signals on the Primary IDE connector. If the IDE signals are configured for Primary 0 and Primary 1, these signals are used for the Primary 0 connector. **During Reset:** High-Z **After Reset:** Undefined **During POS:** PDA
PDCS1#	O	**PRIMARY DISK CHIP SELECT FOR 1F0H- -1F7H RANGE.** For ATA command register block. If the IDE signals are configured for Primary and Secondary, this output signal is connected to the corresponding signal on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector. **During Reset:** High **After Reset:** High **During POS:** High
PDCS3#	O	**PRIMARY DISK CHIP SELECT FOR 3F0- -3F7 RANGE.** For ATA control register block. If the IDE signals are configured for Primary and Secondary, this output signal is connected to the corresponding signal on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector. **During Reset:** High **After Reset:** High **During POS:** High
PDD[15:0]	I/O	**PRIMARY DISK DATA[15:0].** These signals are used to transfer data to or from the IDE device. If the IDE signals are configured for Primary and Secondary, these signals are connected to the corresponding signals on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector. **During Reset:** High-Z **After Reset:** Undefined**During POS:** PDD
PDDACK#	O	**PRIMARY DMA ACKNOWLEDGE.** This signal directly drives the IDE device DMACK# signal. It is asserted by PIIX4 to indicate to IDE DMA slave devices that a given data transfer cycle (assertion of PDIOR# or PDIOW#) is a DMA data transfer cycle. This signal is used in conjunction with the PCI bus master IDE function. It is not associated with any AT compatible DMA channel. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector. **During Reset:** High **After Reset:** High **During POS:** High
PDDREQ	I	**PRIMARY DISK DMA REQUEST.** This input signal is directly driven from the IDE device DMARQ signal. It is asserted by the IDE device to request a data transfer, and used in conjunction with the PCI bus master IDE function. It is not associated with any AT compatible DMA channel. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector.

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Name	Type	Description
PDIOR#	O	**PRIMARY DISK IO READ.** In normal IDE this is the command to the IDE device that it may drive data onto the PDD[15:0] lines. Data is latched by PIIX4 on the negation edge of PDIOR#. The IDE device is selected either by the ATA register file chip selects (PDCS1#, PDCS3#) and the PDA[2:0] lines, or the IDE DMA slave arbitration signals (PDDACK#). In an Ultra DMA/33 read cycle, this signal is used as DMARDY# which is negated by the PIIX4 to pause Ultra DMA/33 transfers. In an Ultra DMA/33 write cycle, this signal is used as the STROBE signal, with the drive latching data on rising and falling edges of STROBE. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector. **During Reset:** High **After Reset:** High **During POS:** High
PDIOW#	O	**PRIMARY DISK IO WRITE.** In normal IDE mode, this is the command to the IDE device that it may latch data from the PDD[15:0] lines. Data is latched by the IDE device on the negation edge of PDIOW#. The IDE device is selected either by the ATA register file chip selects (PDCS1#, PDCS3#) and the PDA[2:0] lines, or the IDE DMA slave arbitration signals (PDDACK#). For Ultra DMA/33 mode, this signal is used as the STOP signal, which is used to terminate an Ultra DMA/33 transaction. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector. **During Reset:** High **After Reset:** High **During POS:** High-Z
PIORDY	I	**PRIMARY IO CHANNEL READY.** In normal IDE mode, this input signal is directly driven by the corresponding IDE device IORDY signal. In an Ultra DMA/33 read cycle, this signal is used as STROBE, with the PIIX4 latching data on rising and falling edges of STROBE. In an Ultra DMA/33 write cycle, this signal is used as the DMARDY# signal which is negated by the drive to pause Ultra DMA/33 transfers. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector. This is a Schmitt triggered input.

Name	Type	Description
SDA[2:0]	O	**SECONDARY DISK ADDRESS[2:0].** These signals indicate which byte in either the ATA command block or control block is being addressed. If the IDE signals are configured for Primary and Secondary, these signals are connected to the corresponding signals on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector. **During Reset:** High-Z **After Reset:** Undefined **During POS:** SDA
SDCS1#	O	**SECONDARY CHIP SELECT FOR 170H- -177H RANGE.** For ATA command register block. If the IDE signals are configured for Primary and Secondary, this output signal is connected to the corresponding signal on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector. **During Reset:** High **After Reset:** High **During POS:** High
SDCS3#	O	**SECONDARY CHIP SELECT FOR 370H- -377H RANGE.** For ATA control register block. If the IDE signals are configured for Primary and Secondary, this output signal is connected to the corresponding signal on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector. **During Reset:** High **After Reset:** High **During POS:** High-Z
SDD[15:0]	I/O	**SECONDARY DISK DATA[15:0].** These signals are used to transfer data to or from the IDE device. If the IDE signals are configured for Primary and Secondary, these signals are connected to the corresponding signals on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector. **During Reset:** High-Z **After Reset:** Undefined **During POS:** SDD
SDDACK#	O	**SECONDARY DMA ACKNOWLEDGE.** This signal directly drives the IDE device DMACK# signal. It is asserted by PIIX4 to indicate to IDE DMA slave devices that a given data transfer cycle (assertion of SDIOR# or SDIOW#) is a DMA data transfer cycle. This signal is used in conjunction with the PCI bus master IDE function. It is not associated with any AT compatible DMA channel. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector. **During Reset:** High **After Reset:** High **During POS:** High

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Name	Type	Description
SDDREQ	I	**SECONDARY DISK DMA REQUEST.** This input signal is directly driven from the IDE device DMARQ signal. It is asserted by the IDE device to request a data transfer, and used in conjunction with the PCI bus master IDE function. It is not associated with any AT compatible DMA channel. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector.
SDIOR#	O	**SECONDARY DISK IO READ.** In normal IDE mode, this is the command to the IDE device that it may drive data onto the SDD[15:0] lines. Data is latched by the PIIX4 on the negation edge of SDIOR#. The IDE device is selected either by the ATA register file chip selects (SDCS1#, SDCS3#) and the SDA[2:0] lines, or the IDE DMA slave arbitration signals (SDDACK#). In an Ultra DMA/33 read cycle, this signal is used as DMARDY# which is negated by the PIIX4 to pause Ultra DMA/33 transfers. In an Ultra DMA/33 write cycle, this signal is used as the STROBE signal, with the drive latching data on rising and falling edges of STROBE. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector. **During Reset:** High **After Reset:** High **During POS:** High
SDIOW#	O	**SECONDARY DISK IO WRITE.** In normal IDE mode, this is the command to the IDE device that it may latch data from the SDD[15:0] lines. Data is latched by the IDE device on the negation edge of SDIOW#. The IDE device is selected either by the ATA register file chip selects (SDCS1#, SDCS3#) and the SDA[2:0] lines, or the IDE DMA slave arbitration signals (SDDACK#). In read and write cycles this signal is used as the STOP signal, which is used to terminate an Ultra DMA/33 transaction. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector. **During Reset:** High **After Reset:** High **During POS:** High
SIORDY	I	**SECONDARY IO CHANNEL READY.** In normal IDE mode, this input signal is directly driven by the corresponding IDE device IORDY signal. In an Ultra DMA/33 read cycle, this signal is used as STROBE, with the PIIX4 latching data on rising and falling edges of STROBE. In an Ultra DMA write cycle, this signal is used as the DMARDY# signal which is negated by the drive to pause Ultra DMA/33 transfers. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector. This is a Schmitt triggered input.

2.1.9. UNIVERSAL SERIAL BUS SIGNALS

Name	Type	Description
OC[1:0]#	I	**OVER CURRENT DETECT.** These signals are used to monitor the status of the USB power supply lines. The corresponding USB port is disabled when its over current signal is asserted.
USBP0+, USBP0-	I/O	**SERIAL BUS PORT 0.** This signal pair comprises the differential data signal for USB port 0. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
USBP1+, USBP1	I/O	**SERIAL BUS PORT 1.** This signal pair comprises the differential data signal for USB port 1. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z

2.1.10. POWER MANAGEMENT SIGNALS

Name	Type	Description
BATLOW#/ GPI9	I	**BATTERY LOW.** Indicates that battery power is low. PIIX4 can be programmed to prevent a resume operation when the BATLOW# signal is asserted. If the Battery Low function is not needed, this pin can be used as a general-purpose input.
CPU_STP#/ GPO17	O	**CPU CLOCK STOP.** Active low control signal to the clock generator used to disable the CPU clock outputs. If this function is not needed, then this signal can be used as a general-purpose output. For values **During Reset**, **After Reset**, and **During POS**, see the *Suspend/Resume and Resume Control Signaling* section.
EXTSMI#	I/OD	**EXTERNAL SYSTEM MANAGEMENT INTERRUPT.** EXTSMI# is a falling edge triggered input to PIIX4 indicating that an external device is requesting the system to enter SMM mode. When enabled, a falling edge on EXTSMI# results in the assertion of the SMI# signal to the CPU. EXTSMI# is an asynchronous input to PIIX4. However, when the setup and hold times are met, it is only required to be asserted for one PCICLK. Once negated EXTSMI# must remain negated for at least four PCICLKs to allow the edge detect logic to reset. EXTSMI# is asserted by PIIX4 in response to SMI# being activated within the Serial IRQ function. An external pull-up should be placed on this signal.
LID/ GPI10	I	**LID INPUT.** This signal can be used to monitor the opening and closing of the display lid of a notebook computer. It can be used to detect both low to high transition or a high to low transition and these transitions will generate an SMI# if enabled. This input contains logic to perform a 16-ms debounce of the input signal. If the LID function is not needed, this pin can be used as a general-purpose input.

3.4 INTEL FW82371AB PCI/ISA BRIDGE (PIIX4)-10

Name	Type	Description
PCIREQ[A:D]#	I	**PCI REQUEST.** Power Management input signals used to monitor PCI Master Requests for use of the PCI bus. They are connected to the corresponding REQ[0:3]# signals on the Host Bridge.
PCI_STP#/	O	**PCI CLOCK STOP.** Active low control signal to the clock generator used to disable GPO18the PCI clock outputs. The PIIX4 free running PCICLK input must remain on. If this function is not needed, this pin can be used as a general-purpose output. For values **During Reset**, **After Reset**, and **During POS**, see the *Suspend/Resume and Resume Control Signaling* section.
PWRBTN#	I	**POWER BUTTON.** Input used by power management logic to monitor external system events, most typically a system on/off button or switch. This input contains logic to perform a 16-ms debounce of the input signal.
RI# GPI12	I	**RING INDICATE.** Input used by power management logic to monitor external system events, most typically used for wake up from a modem. If this function is not needed, then this signal can be individually used as a general-purpose input.
RSMRST#	I	**RESUME RESET.** This signal resets the internal Suspend Well power plane logic and portions of the RTC well logic.
SMBALERT#/	I	**SM BUS ALERT.** Input used by System Management Bus logic to generate an GPI11interrupt (IRQ or SMI) or power management resume event when enabled. If this function is not needed, this pin can be used as a general-purpose input.
SMBCLK	I/O	**SM BUS CLOCK.** System Management Bus Clock used to synchronize transfer of data on SMBus. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
SMBDATA	I/O	**SM BUS DATA.** Serial data line used to transfer data on SMBus. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
SUSA#	O	**SUSPEND PLANE A CONTROL.** Control signal asserted during power management suspend states. SUSA# is primarily used to control the primary power plane. This signal is asserted during POS, STR, and STD suspend states. **During Reset:** Low **After Reset:** High **During POS:** Low
SUSB#/ GPO15	O	**SUSPEND PLANE B CONTROL.** Control signal asserted during power management suspend states. SUSB# is primarily used to control the secondary power plane. This signal is asserted during STR and STD suspend states. If the power plane control is not needed, this pin can be used as a general-purpose output. **During Reset:** Low **After Reset:** High **During POS:** High/GPO

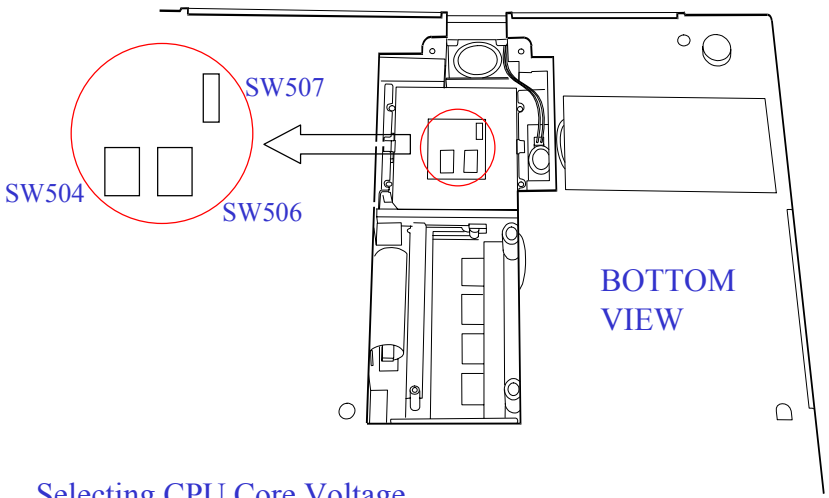
Name	Type	Description
SUSC#/	O	**SUSPEND PLANE C CONTROL.** Control signal asserted during power GPO16management suspend states, primarily used to control the tertiary power plane. It is asserted only during STD suspend state. If the power plane control is not needed, this pin can be used as a general-purpose output. **During Reset:** Low **After Reset:** High **During POS:** High/GPO
SUS_STAT1#/	O	**SUSPEND STATUS 1.** This signal is typically connected to the Host-to-PCI bridge GPO20and is used to provide information on host clock status. SUS_STAST1# is asserted when the system may stop the host clock, such as Stop Clock or during POS, STR,and STD suspend states. If this function is not needed, this pin can be used as a general-purpose output. **During Reset:** Low **After Reset:** High **During POS:** Low/GPO
SUS_STAT2#/	O	**SUSPEND STATUS 2.** This signal will typically connect to other system peripherals GPO21and is used to provide information on system suspend state. It is asserted during POS, STR, and STD suspend states. If this function is not needed, this pin can be used as a general-purpose output. **During Reset:** Low **After Reset:** High **During POS:** Low/GPO
THRM#/	I	**THERMAL DETECT.** Active low signal generated by external hardware to start the GPI8Hardware Clock Throttling mode. If enabled, the external hardware can force the system to enter into Hardware Clock Throttle mode by asserting THRM#. This causes PIIX4 to cycle STPCLK# at a preset programmable rate. If this function is not needed, this pin can be used as a general-purpose input.
ZZ/	O	**LOW-POWER MODE FOR L2 CACHE SRAM.** This signal is used to power down a GPO19cache• data SRAMs when the clock logic places the CPU into the Stop Clock. If this function is not needed, this pin can be used as a general-purpose output. **During Reset:** Low **After Reset:** Low **During POS:** Low

2.1.11. GENERAL PURPOSE INPUT AND OUTPUT SIGNALS

Some of the General Purpose Input and Output signals are multiplexed with other PIIX4 signals. The usage is determined by the system configuration.
The default pin usage is shown in Table 1 and Table 2. The configuration can be selected via the General Configuration register and X-Bus Chip Select register.

Name	Type	Description
GPI[21:0]	I	**GENERAL PURPOSE INPUTS.** These input signals can be monitored via the GPIREG register located in Function 3 (Power Management) System IO Space at address PMBase+30h. See Table 1 for details.

4.SWITCH & JUMPERS SETTING



Selecting CPU Core Voltage

Voltage	SW506			
	Pin1	Pin2	Pin3	Pin4
1.8V	OFF	OFF	OFF	OFF
1.9V	OFF	OFF	OFF	ON
2.0V	OFF	OFF	ON	OFF
2.1V	OFF	OFF	ON	ON
2.2V	OFF	ON	OFF	OFF
2.3V	OFF	ON	OFF	ON
2.4V	OFF	ON	ON	OFF
2.5V	OFF	ON	ON	ON
2.6V	ON	OFF	OFF	OFF
2.7V	ON	OFF	OFF	ON
2.8V	ON	OFF	ON	OFF
2.9V	ON	OFF	ON	ON
3.0V	ON	ON	OFF	OFF
3.1V	ON	ON	OFF	ON
3.2V	ON	ON	ON	OFF
3.3V	ON	ON	ON	ON

Selecting CPU Speed

INTEL CPU Speed	SW504			
	Pin1	Pin2	Pin3	Pin4
100MHz	OFF	OFF	OFF	ON
120MHz	ON	ON	OFF	ON
133MHz	OFF	ON	OFF	ON
150MHz	ON	ON	ON	ON
166MHz	OFF	ON	ON	ON
180MHz	ON	OFF	ON	ON
200MHz	OFF	OFF	ON	ON
233MHz	OFF	OFF	OFF	ON
266Mhz	OFF	ON	ON	OFF

AMD CPU Speed	SW501			
	Pin1	Pin2	Pin3	Pin4
150MHz	ON	ON	ON	OFF
166MHz	OFF	ON	ON	OFF
180MHz	ON	OFF	ON	OFF
200MHz	OFF	OFF	ON	OFF
233MHz	OFF	OFF	OFF	OFF
266Mhz	OFF	ON	OFF	ON

5033 M/B MAINTENANCE

5.ASSEMBLY & DISASSEMBLY

5.1 SYSTEM VIEW

5.1.1 RIGHT-SIDE VIEW
5.1.2 LEFT-SIDE VIEW
5.1.3 REAR VIEW
5.1.4 FRONT VIEW
5.1.5 TOP-OPEN VIEW

5.2 SYSTEM DISASSEMBLY

MODULAR COMPONENTS

5.2.1 BATTERY PACK
5.2.2 CD-ROM DRIVE
5.2.3 CPU
5.2.4 FAX/ MODEM/ VOICE CARD
5.2.5 SO-DIMM

LCD ASSEMBLY COMPONENTS

5.2.6 LCD ASSEMBLY
5.2.7 LCD PANEL
5.2.8 INVERTER BOARD

BASE UNIT COMPONENTS

5.2.9 KEYBOARD
5.2.10 HARD DISK DRIVE
5.2.11 TOUCHPAD BOARD
5.2.12 SYSTEM BOARD
5.2.13 FLOPPY DISK DRIVE

5.ASSEMBLY & DISASSEMBLY

5.1 SYSTEM VIEW

5.1.1 RIGHT-SIDE VIEW

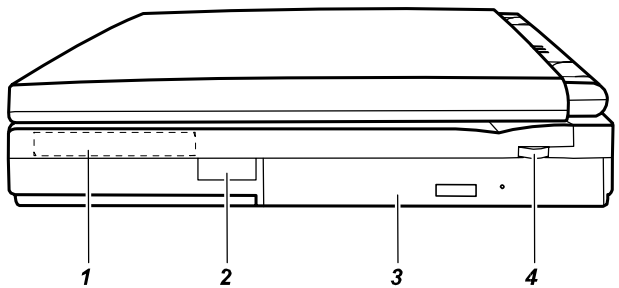


Figure 5-1. Right-Side View

1. **Hard Disk Drive**
2. **IR Port**
3. **CD-ROM Drive**
4. **Volume Control**

5.1.2 LEFT-SIDE VIEW

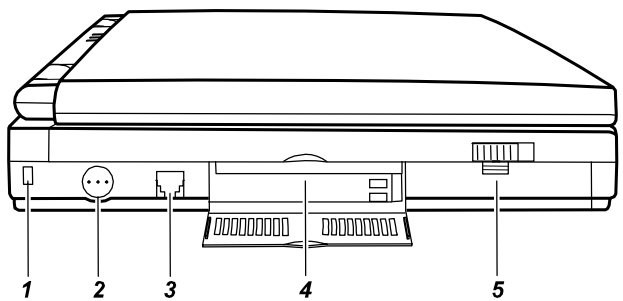


Figure 5-2. Left-Side View

1. **Kensington Lock Anchor**
2. **Power Button**
3. **Phone Line Connector** (optional)
4. **PC Card Slots**
5. **Battery Pack**

5.ASSEMBLY & DISASSEMBLY

5.1.3 REAR VIEW

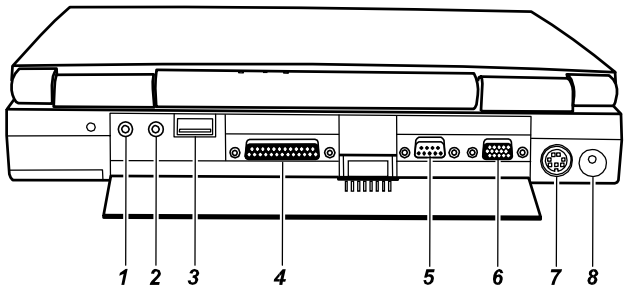


Figure 5-3. Rear View

1. **Microphone Connector**
2. **Audio Output Connector**
3. **USB Port**
4. **Parallel Port**
5. **Serial Port**
6. **VGA Port**
7. **PS/2 Mouse/Keyboard Port**
8. **Power Connector**

5.1.4 FRONT VIEW

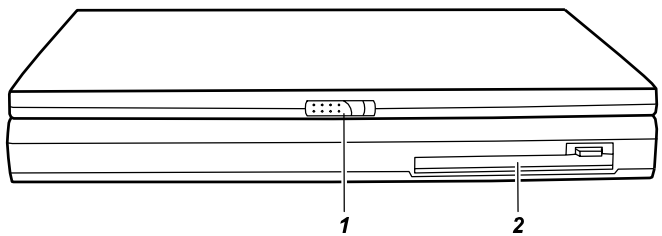


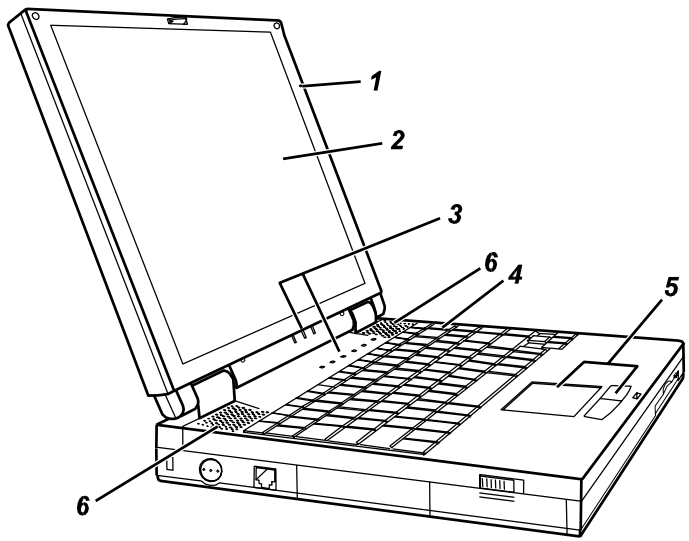
Figure 5-4. Front View

1. **Top Cover Latch**
2. **Floppy Disk Drive**

5.ASSEMBLY & DISASSEMBLY

5.1.5 TOP-OPEN VIEW

To open the cover, press the cover latch toward the right and lift the cover.



1. **Microphone**
2. **LCD Display**
3. **Indicators Panel**
4. **Keyboard**
5. **Touchpad**
6. **Stereo Speaker Set**

Figure 5-5. Top-Open View

5.ASSEMBLY & DISASSEMBLY

5.2 SYSTEM DISASSEMBLY

The section discusses at length each major component for disassembly/reassembly and shows corresponding illustrations. Use the chart below to determine the disassembly sequence for removing components from the notebook.

5.2.1 BATTERY PACK

DISASSEMBLY

1. Place the notebook upside down.
2. First push away the small locking latch(❶) on the battery pack and then slide the locking latch (❷) on the side of the notebook to unlock and lift (❸) the battery pack out of the compartment.

REASSEMBLY

1. Fit the battery pack into the compartment. Make sure the lock latches are in the locked position. (fig 7-6)

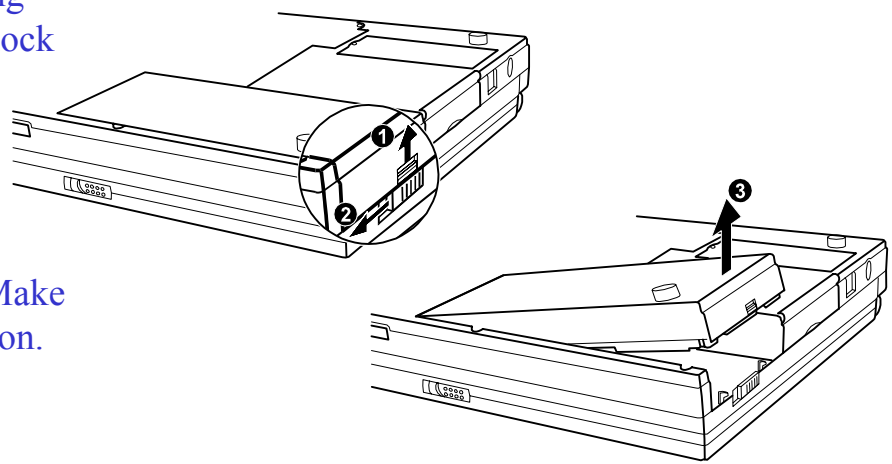


Figure 5-6. Removing the Battery Pack

5.ASSEMBLY & DISASSEMBLY

5.2.2 CD-ROM DRIVE

DISASSEMBLY

1. Place the notebook upside down.
2. Open the CPU compartment cover by removing four screws and lifting up the cover from one side.
3. Unplug the CD-ROM drive cable from the system board.
4. Remove one screw and slide the CD-ROM drive out of the compartment.

REASSEMBLY

1. Connect one end of the CD-ROM drive cable to the CD-ROM drive.
2. Slide the CD-ROM drive into the compartment and secure with one screw.
3. Connect the CD-ROM drive cable to the system board.
4. Replace the CPU compartment cover and secure with four screws.

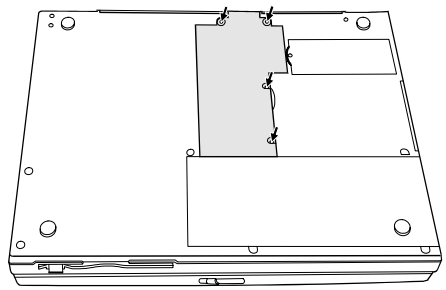


Figure 5-7. Removing the CPU Compartment Cover

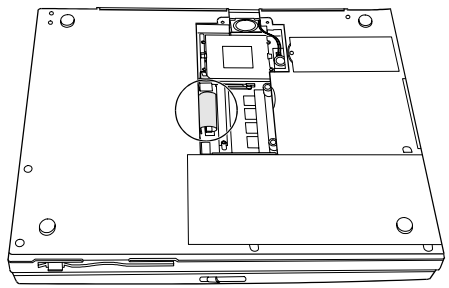


Figure 5-8. Unpluging the CD-ROM Drive Cable

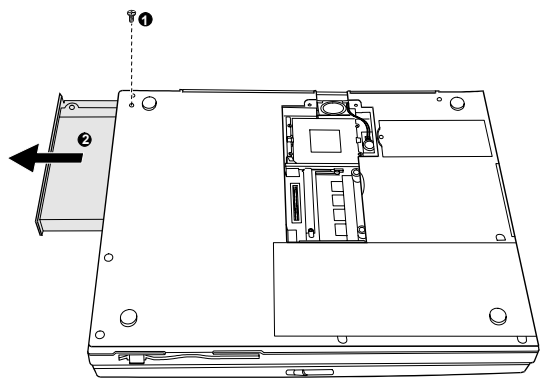


Figure 5-9. Removing the CD-ROM Drive

5.ASSEMBLY & DISASSEMBLY

5.2.3 CPU

DISASSEMBLY

1. Place the notebook upside down.
2. Open the CPU compartment cover by removing four screws and lifting up the cover from one side.
3. To remove the CPU cooling fan assembly, follow these steps:
   a. Remove the four screws.
   b.Unplug the fan power cord.
4. To remove the CPU, insert a flat screwdrive to the OPEN side of the socket and push the screwdriver toward the CPU to loosen the CPU.

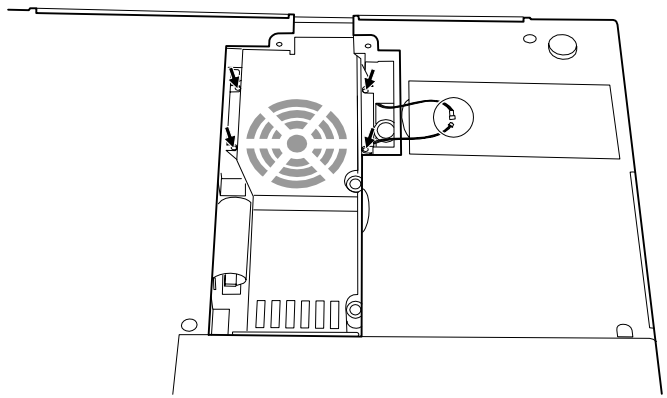


Figure 5-10. Removing the CPU Cooling Fan

REASSEMBLY

1. To install the CPU, align the beveled corner on the CPU with the beveled corner of the socket and insert the CPU pins into the holes.insert a flat screwdriver to the CLOSE side of the socket and push the screwdriver toward the CPU to secure the CPU in place.
2. Make sure SW504 and SW506 are set correctly(referring to jumper setting)
3. Reconnect the fan power cord. Then , attach the CPU cooling fan to CPU and secure with four screws.
4. Replace the compartment cover and secure with four screws.

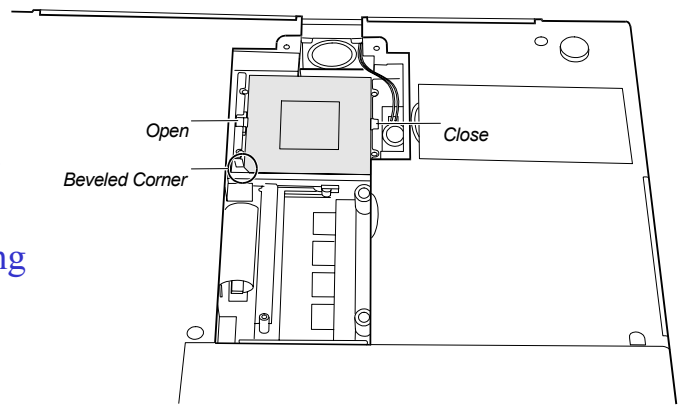


Figure 5-11. Removing the CPU

5.ASSEMBLY & DISASSEMBLY

5.2.4 FAX/ MODEM/ VOICE CARD

DISASSEMBLY

1. Place the notebook upside down.
2. To remove the compartment cover, remover one screw, then lift up the cover.
3. Lift up the inner edge of the card and remove the card.

REASSEMBLY

1. Hold the Fax/ Modem/Voice Card at an angle so that the phone line connector is pointed towards the opening on the notebook. Insert the phone line connector into the opening and press the other end to plug the other connector into the socket on the system board.
2. Replace the compartment cover and secure with one screw.

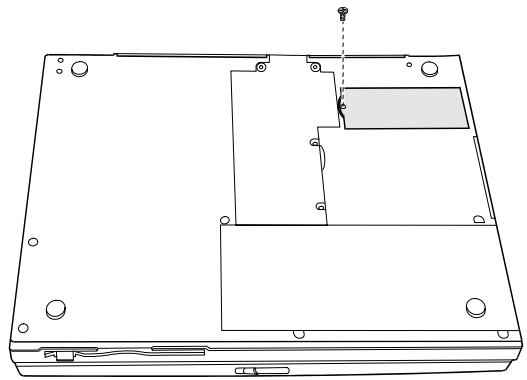


Figure 5-12. Removing the Fax/Modem/Voice Card Compartment Cover

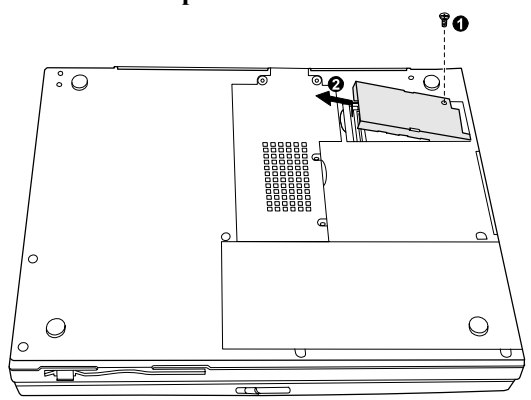


Figure 5-13. Removing the Fax/Modem/Voice Card

5.ASSEMBLY & DISASSEMBLY

5.2.5 SO-DIMM

DISASSEMBLY

1. Open the CPU compartment cover by removing four screws and lifting up the cover from one side.
2. Remove the CPU cooling fan assembly.
3. Pull the retaining clips outward and remove the SO-DIMM.

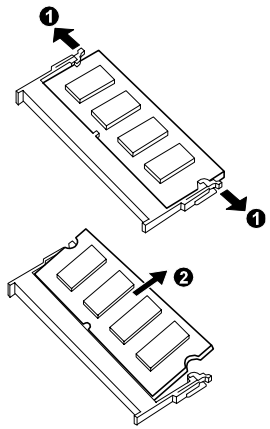


Figure 2-14. Removing the SO-DIMM

REASSEMBLY

1. To install the SO-DIMM ,align the SO-DIMM notched part with the socket corresponding part and family insert the SO-DIMM into the socket at an angle. Then push down until the retaining clips lock the SO-DIMM into position
2. Replace the CPU cooling fan assembly.
3. Replace the compartment cover and secure with four screws.

5.ASSEMBLY & DISASSEMBLY

5.2.6 LCD ASSEMBLY

DISASSEMBLY

1. Remove six bottom screws.
2. Put the notebook back to the upright position and open the top cover. Remove the base unit cover.
3. Disconnect the keyboard cable from the system board.
4. Remove the shield plate by removing 13 screws.
5. Remove the hinge cover by inserting a flat screwdriver to the rear of cover and pry the cover out. Repeat the same with the other hinge cover. Note the right and left hinges are not exchangeable.
6. Unplug the three cable connectors coming from the LCD assembly.
7. Remove four screws from the hinges. Now you can separate the LCD assembly from the base unit.

REASSEMBLY

1. Attach the LCD assembly to base unit and secure with four screws on the hinges.
2. Reconnect the Lcd cable connectors to the system board.
3. Replace the two hinge covers.
4. Replace the shield plate and secure with 13 screws.
5. Connect the keyboard cable and replace the keyboard.
6. Replace the base unit cover.
7. Replace the six bottom screws.

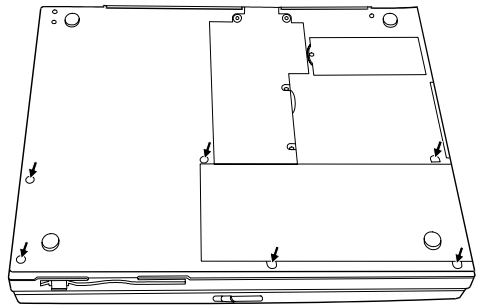


Figure 5-15. Removing Six Bottom Screws

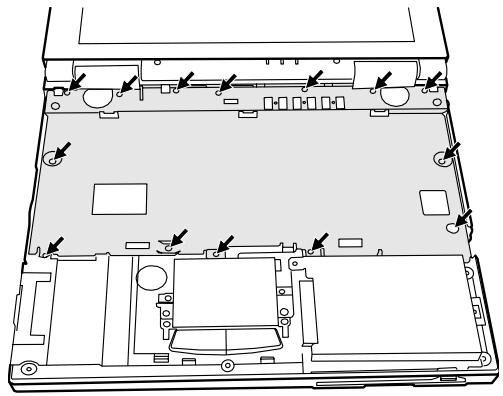


Figure 5-16. Removing the Shield Plate

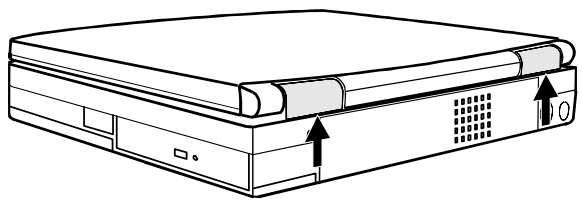


Figure 5-17. Removing the Hinge Covers

5.ASSEMBLY & DISASSEMBLY

5.2.7 LCD PANEL

DISASSEMBLY

1. Open the top cover.
2. Remove the four rubber pads and four screws underneath. Now you can separate the LCD frame from the housing.
3. To remove the LCD, remove four screws and unplug the cables.

REASSEMBLY

1. Reconnect the cables to LCD. Fit the LCD back into place and secure with four screws.
2. Fit the LCD frame back to the housing and replace the four screws and rubber pads.

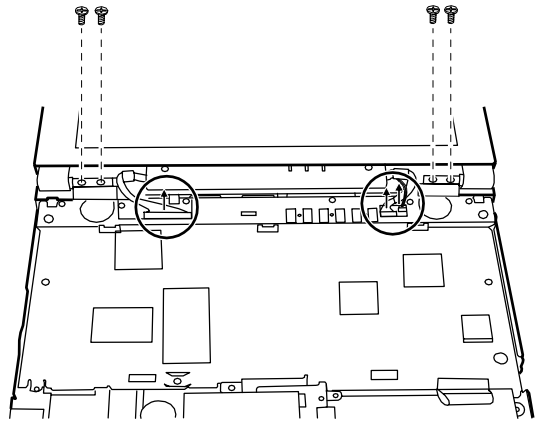


Figure 5-18. Unplugging the Cable Connectors and Removing Four Screws

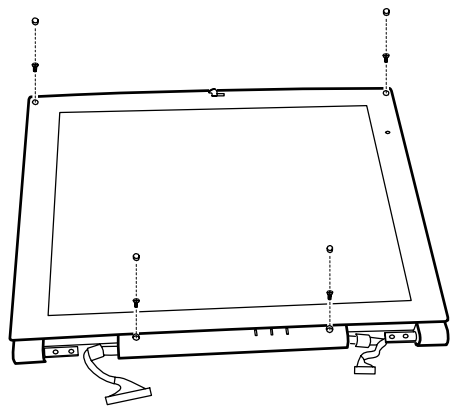


Figure 2-19. Removing the LCD Frame

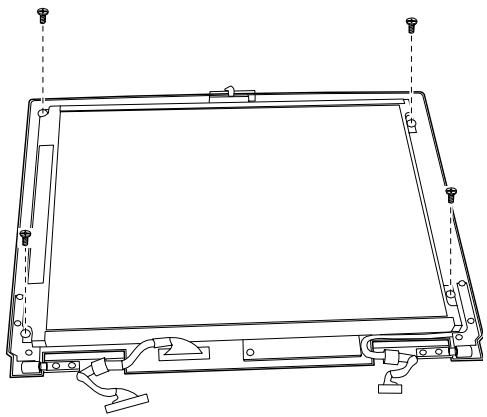


Figure 2-20. Removing the Flat Panel Screen

5.ASSEMBLY & DISASSEMBLY

5.2.8 INVERTER BOARD

DISASSEMBLY

1. Detach the LCD frame.
2. To remove the inverter board, remove one screw and unplug the connectors from the board.

REASSEMBLY

1. Reconnect the connector . Fit the inverter board back into place and secure with one screw.
2. Fit the LCD frame back to the housing and replace the four scrtews and rubber pads.

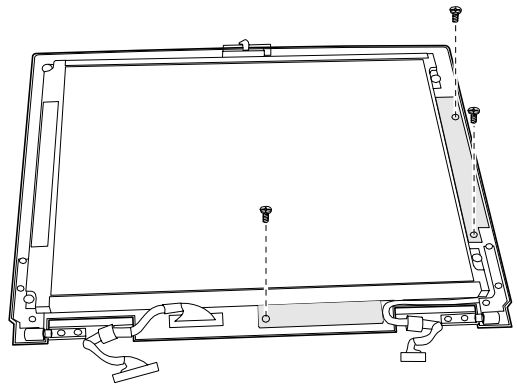


Figure 5-21. Removing the Inverter Board

5.2.9 KEYBOARD

DISASSEMBLY

1. Remove the base unit cover.
2. Lift the keyboard and unplug the keyboard cable from the system board.

REASSEMBLY

1. Reconnect the keyboard cable and fit the keyboard back into place.
2. Replace the base unit cover.

5.ASSEMBLY & DISASSEMBLY

5.2.10 HARD DISK DRIVE

DISASSEMBLY

1. Remove the base unit cover.
2. Remove two top screws from the hard disk drive bracket and slide the hard disk drive outwards to unplug the connector.
3. To separate the hard disk drive from the backet, remove four side screws from the bracket.

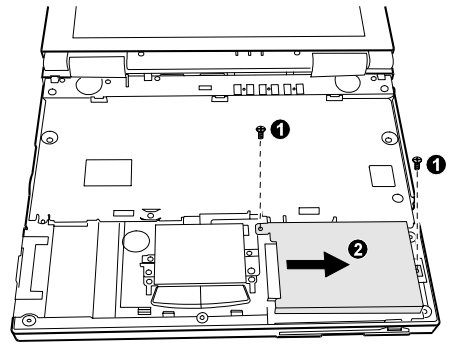


Figure 5-22. Removing the Hard Disk Drive

REASSEMBLY

1. Attach the bracket to the hard disk drive and secure with four screws on both sides.
2. Plug the hard disk drive connector to the touchpad board and secure the bracket in place with two screws.
3. Replace the base unit cover.

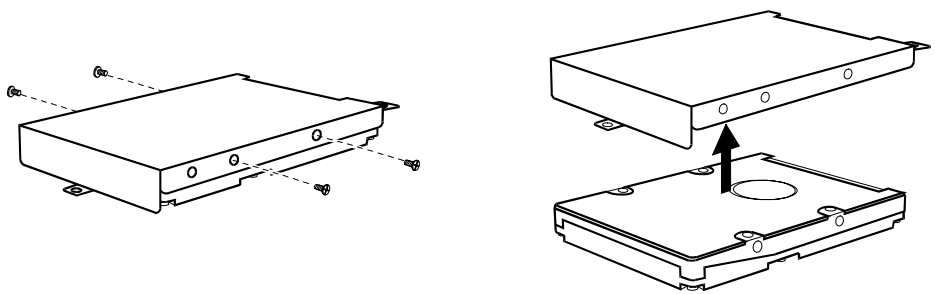


Figure 5-23. Removing the Hard Disk Drive Bracket

5.ASSEMBLY & DISASSEMBLY

5.2.11 TOUCHPAD BOARD

DISASSEMBLY

1. Remove the shield plate.
2. Remove the hard disk drive
3. Lift the touchpad board free.

REASSEMBLY

1. Fit the touchpad board into place.
2. Replace the hard disk drive.
3. Replace the Shield plate.

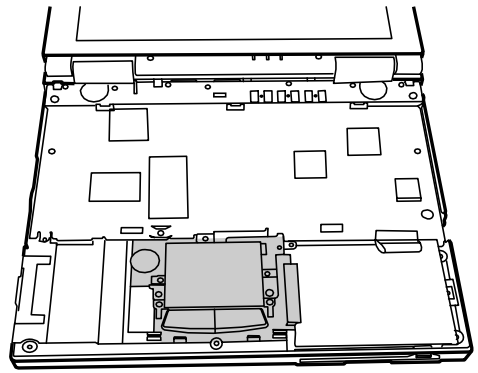


Figure 5-24. Removing the Touchpad Board

5.2.12 SYSTEM BOARD

DISASSEMBLY

1. Remove all the bottom screws.
2. Remove the battery pack.
3. Remove the CD-ROM drive.
4. Remove the CPU cooling fan assembly.
5. Remove the Fax/ Modem/ Voice Card if it exists.
6. Remove the LCD assembly.
7. Remove the hard disk drive .
8. Remove the touchpad board.
9. Unplug the speaker connectors from the system board.
10. Remove the base unit rear cover by removing two rear panel screws.

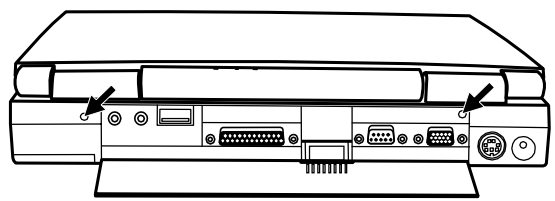


Figure 5-25. Removing Two Rear Panel Screws

5.ASSEMBLY & DISASSEMBLY

11. Remove the remaining four screws that secure the system board to the base unit.
12. Unplug the floppy disk drive cable connector from the system board.
13. Lift the system board free.

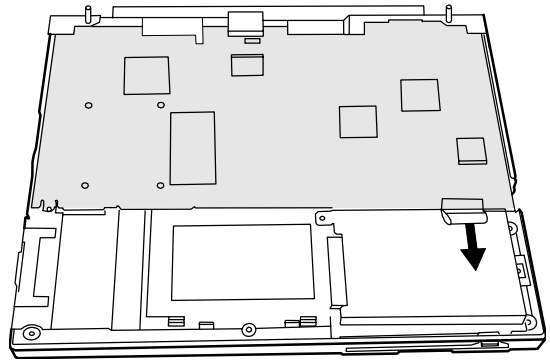


Figure 5-26. Removing System Board Screws and Unpluging the Floppy Disk Drive Cable

REASSEMBLY

1. Fit the system board into place and the four screws
2. Connect the floppy disk drive cable to the system board.
3. Replace the touchpad board by plugging the connector.
4. Replace the hard disk drive with its bracket by plugging the connector to the touchpad board and securing with two screws.
5. Fit the base unit rear cover into place and secure with two rear screws.
6. Connect the speaker connector.
7. Attach the LCD assembly to the base unit and secure with our screws.
8. Replace two hinge covers.
9. Fit the shield plate back into place and secure with 13 screws.
10. Connector the keyboard cable and replace the keyboard.
11. Fit the base unit cover into place and secure with six bottom screws.
12. Replace the CD-ROM drive by sliding it into the compartment , plugging the connector, and secure with one bottom screw.
13. Reconnect the fan power cord. Then , attach the CPU cooling fan to the CPU and secure with four screws.
14. Replace the CPU compartment cover and secure with four screws.
15. Replace the Fax/ Modem/ Voice card and secure with one screw.
16. Replace the Fax/ Modem/ Voice card compartment cover and secure with one screw.
17. Replace the battery pack.

5.ASSEMBLY & DISASSEMBLY

5.2.13 FLOPPY DISK DRIVE

DISASSEMBLY

1. Remove the system board.
2. Remove the floppy disk drive by first lifting the rear end of the floppy disk drive.

REASSEMBLY

1. Connect the floppy disk drive cable to the floppy disk drive and fit the floppy disk drive into place.
2. Replace the system board.

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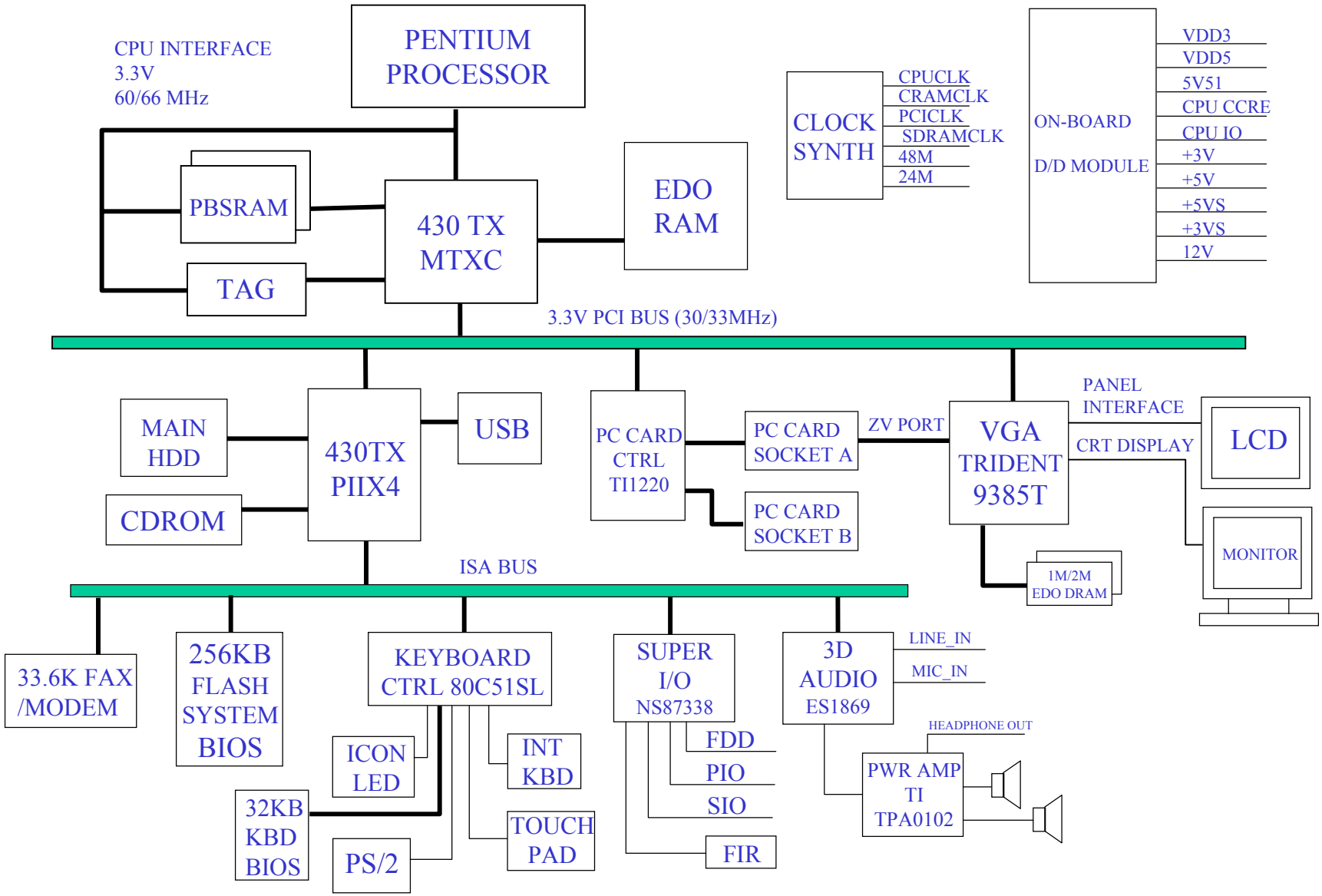
6. 5033 BLOCK DIAGRAM



7. MAINTENANCE DIAGNOSTICS

7.1 INTRODUCTION

EVERY TIME THE COMPUTER IS TURNED ON ,THE SYSTEM BIOS RUNS A SERIES OF INTERNAL CHECKS ON THE HARDWARE. THIS POWER-ON SELF TEST (POST) ALLOWS THE COMPUTER TO DETECT PROBLEMS AS EARLY AS THE POWER-ON STAGE. ERROR MESSAGES OF POST CAN ALERT YOU TO THE PROBLEMS OF YOUR COMPUTER.

IF AN ERROR IS DETECTED DURING THESE TESTS, YOU WILL SEE AN ERROR MESSAGE DISPLAYED ON THE SCREEN. IF THE ERROR OCCURS BEFORE THE DISPLAY, THEN THE SCREEN CANNOT DISPLAY THE ERROR MESSAGE. ERROR CODES OR SYSTEM BEEPS ARE USED TO IDENTIFY A POST ERROR THAT OCCURS WHEN THE SCREEN IS NOT AVAILABLE.

THE VALUE FOR THE DIAGNOSTIC POST(378H) IS WRITTEN AT THE BEGINNING OF THE TEST. THEREFORE , IF THE TEST FAIL, THE USER CAN DETERMINE WHERE THE PROBLEM OCCURS BY READING THE LAST VALUE WRITTEN TO POST 378H BY THE PIO DEBUG BOARD PLUG AT PIO PORT.

7. MAINTENANCE DIAGNOSTICS

7.2 ERROR CODES : FOLLOWING IS A LIST OF ERROR CODES IN SEQUENT DISPLAY ON THE PIO DEBUG BOARD.

Code	Description
00H	Start of BootLoader sequence.
01H	Disable A20 through A20, not send.
02H	Initialize ChipSet.
03H	Perform conventional RAM(1st 640K) test with crossed-pattern R/W.
04H	Move BootLoader to the RAM.
05H	Start point of execution of BootLoader in RAM.
06H	Perform PnP initialization for Crystal audio chip.
06H	Check OVERRIDE option, not send.
07H	Shadow System BIOS.
08H	Checksum System BIOS ROM, not send.
09H	Proceed with Normal Boot
0AH	Proceed with Crisis Boot
0FH	DRAM Sizing
10H	Initial L1,L2 cache, make stack and diagnose CMOS.
11H	Turn off FASTA20 for POST. Reset GDTs, 8259s guickly.
12H	Signal Power On Reset at COMS.
13H	Initialize the Chipset, (SDRAM).
14H	Search For ISA Bus VGA Adapter
15H	Reset Counter/Timer 1, exite the RAM.
16H	User register config through CMOS
18H	Dispatch to 1st 64K RAM Test
19H	Checksum the ROM
1AH	Reset PIC's(8259s)
1BH	Initialize Video Adapter(s)
1CH	Initialize Video (6845 Regs)
1DH	Initialize Color Adapter
1EH	Initialize Monochrome Adapter
1FH	Test 8237A Page Registers
20H	Perform Keyboard self test
21H	Test & Initialize Keyboard Controller

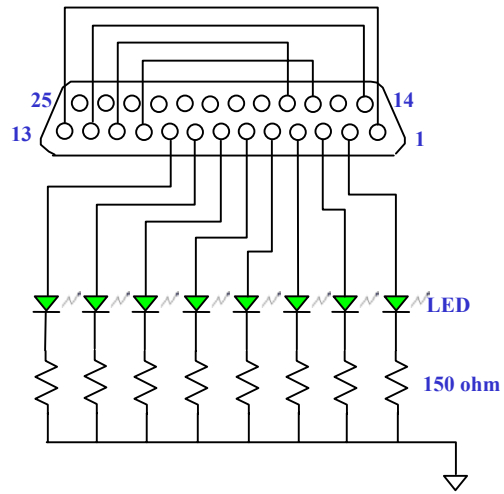
Code	Description
22H	Check If CMOS Ram Valid
23H	Test Battery Fail & CMOS X-SUM
24H	Test the DMA controllers
25H	Initialize 8237A Controller
26H	Initialize Interrupt Vectors Table.
27H	RAM Quick Sizing
28H	Protected mode entered safely
29H	RAM test completed
2AH	Protected mode exit successful
2BH	Setup Shadow
2CH	Prepare To Initialize Video
2DH	Search For Monochrome Adapter
2EH	Search For Color Adapter, VGA Initialize.
2FH	Signon messages displayed
30H	Special init of keyboard ctlr
31H	Test If Keyboard Present
32H	Test Keyboard Interrupt
33H	Test Keyboard Command Byte
34H	TEST, Blank and count all RAM
35H	Protected mode entered safely (2).
36H	RAM test complete
37H	Protected mode exit successful
38H	Update Keyboard output port to disable gate of A20
39H	Setup Cache Controller
3AH	Test If 18.2Hz Periodic Working
3BH	Initialize BIOS Data Area at 40:0.
3CH	Initialize the hardware interrupt vector table
3DH	Search and Init the Mouse
3EH	Update NumLock status
3FH	OEM initialization of COMM and LPT ports

7. MAINTENANCE DIAGNOSTICS

Code	Description
40H	Configure the COMM and LPT ports
41H	Initialize the floppies
42H	Initialize the hard disk
43H	Initialize additional ROMs
44H	OEM's init of Power Management, (check SMI)
45H	Update NUMLOCK status
46H	Test For Coprocessor Installed
47H	OEM functions before boot (PCMCIA, CardBus)
48H	Dispatch To Operation System Boot
49H	Jump Into Bootstrap Code
4AH	OEM's init of PM with USB

Code	Beeps	Description
0F0h	....	No RAM
0F1h	..._	RAM test failed
002h	.._.	BIOS is not shadowed
004h	._..	BIOS Checksum BAD
00Ah	_._.	No CR code/CR bad

PIO PORT (378H) DIAGNOSTIC TOOLS



PIN1 : STROBE ⟷ PIN13: SLCT
PIN10: ACK# ⟷ PIN16: INT#
PIN11: BUSY ⟷ PIN17: SELIN#
PIN12:PTERR ⟷ PIN14: AUTOFD#
PIN[9:2]:PD[7:0]

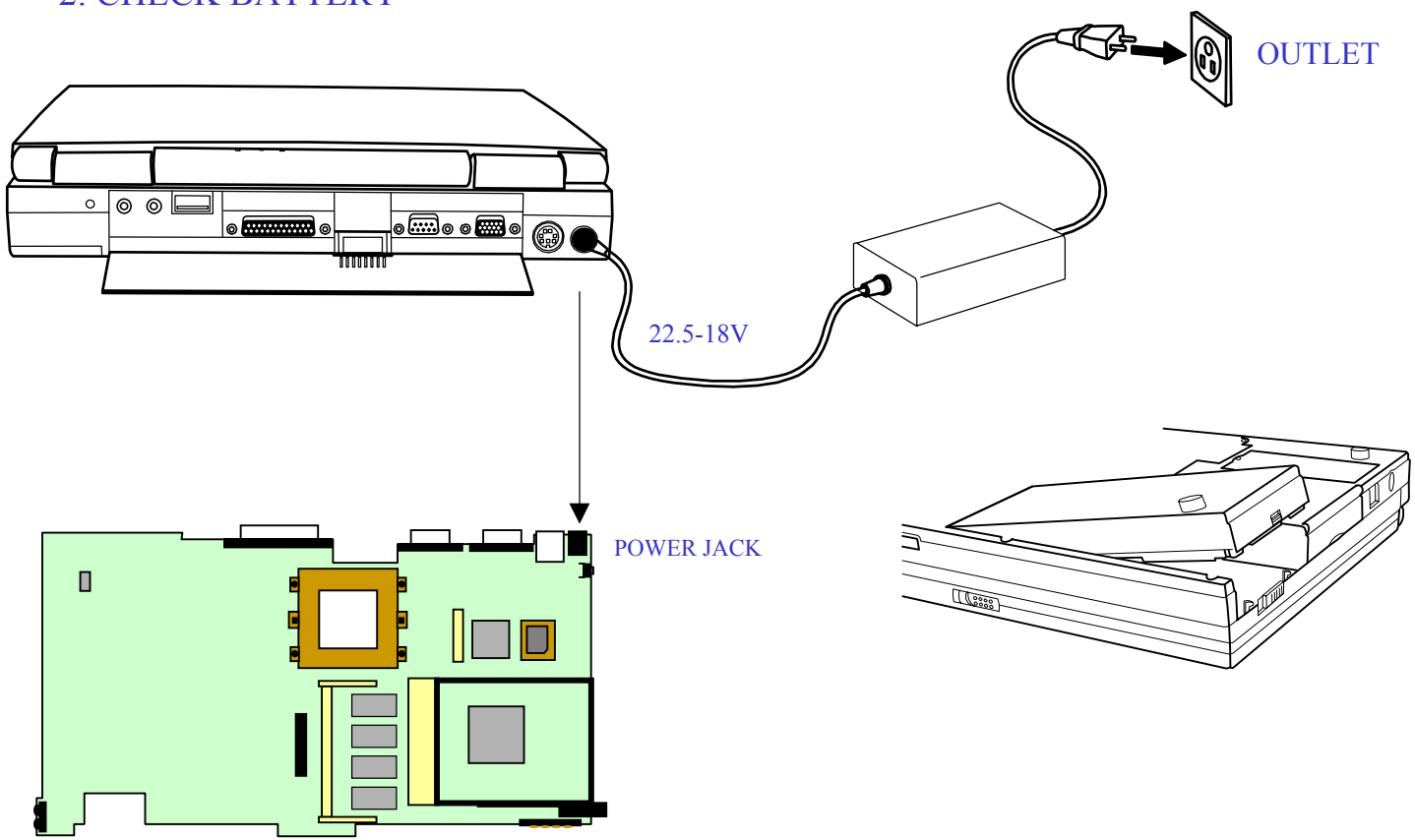
8. TROUBLE SHOOTING

5033 M/B MAINTENANCE

8.1 NO POWER:

WHEN THE POWER BUTTON IS PRESSED, NOTHING HAPPENS ,POWER INDICATOR DOES NOT LIGHT UP.

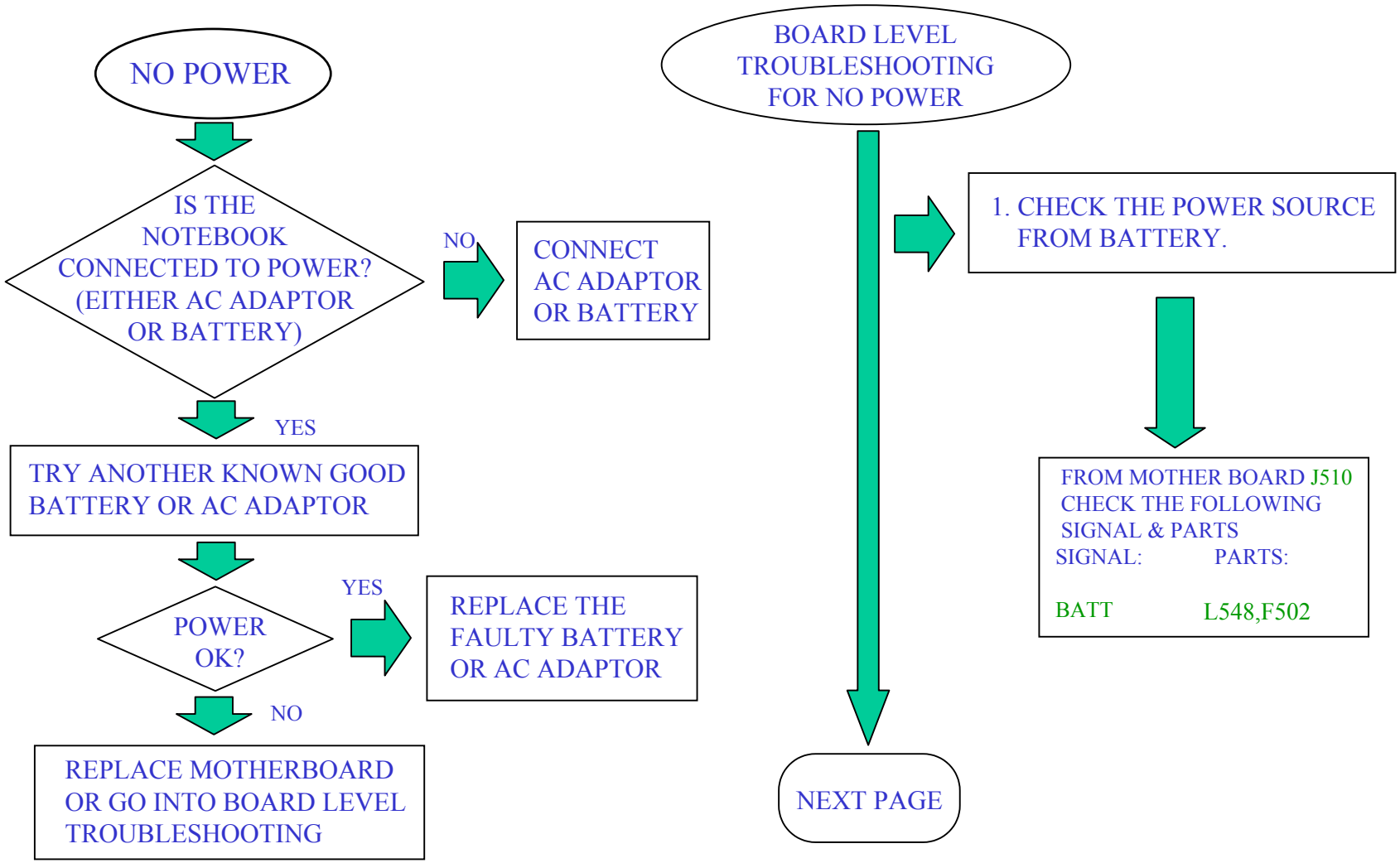
1. CHECK AC ADAPTOR
2. CHECK BATTERY



5033 M/B MAINTENANCE

8.1 NO POWER:

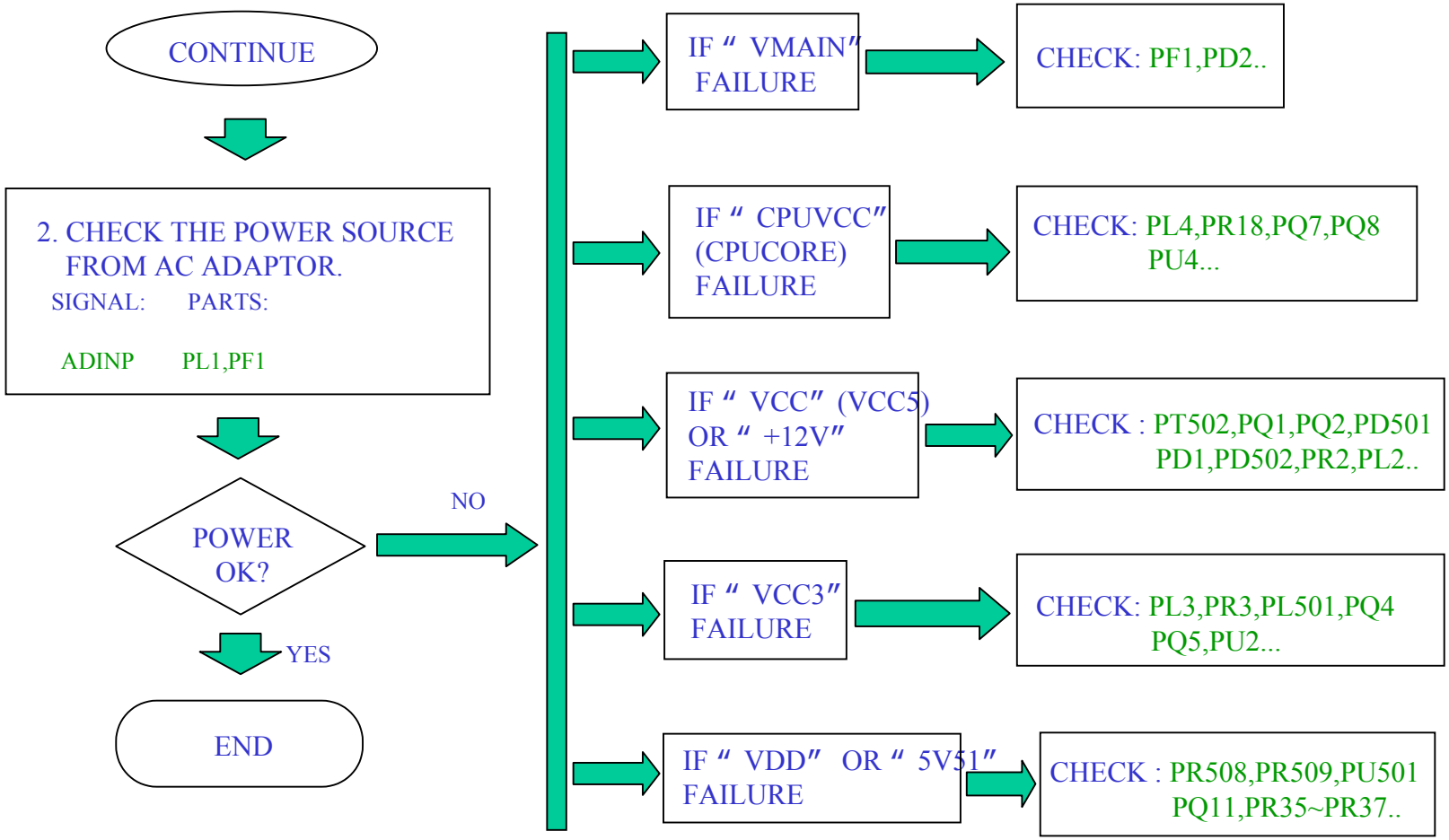
WHEN THE POWER BUTTON IS PRESSED, NOTHING HAPPENS ,POWER INDICATOR DOES NOT LIGHT UP.



5033 M/B MAINTENANCE

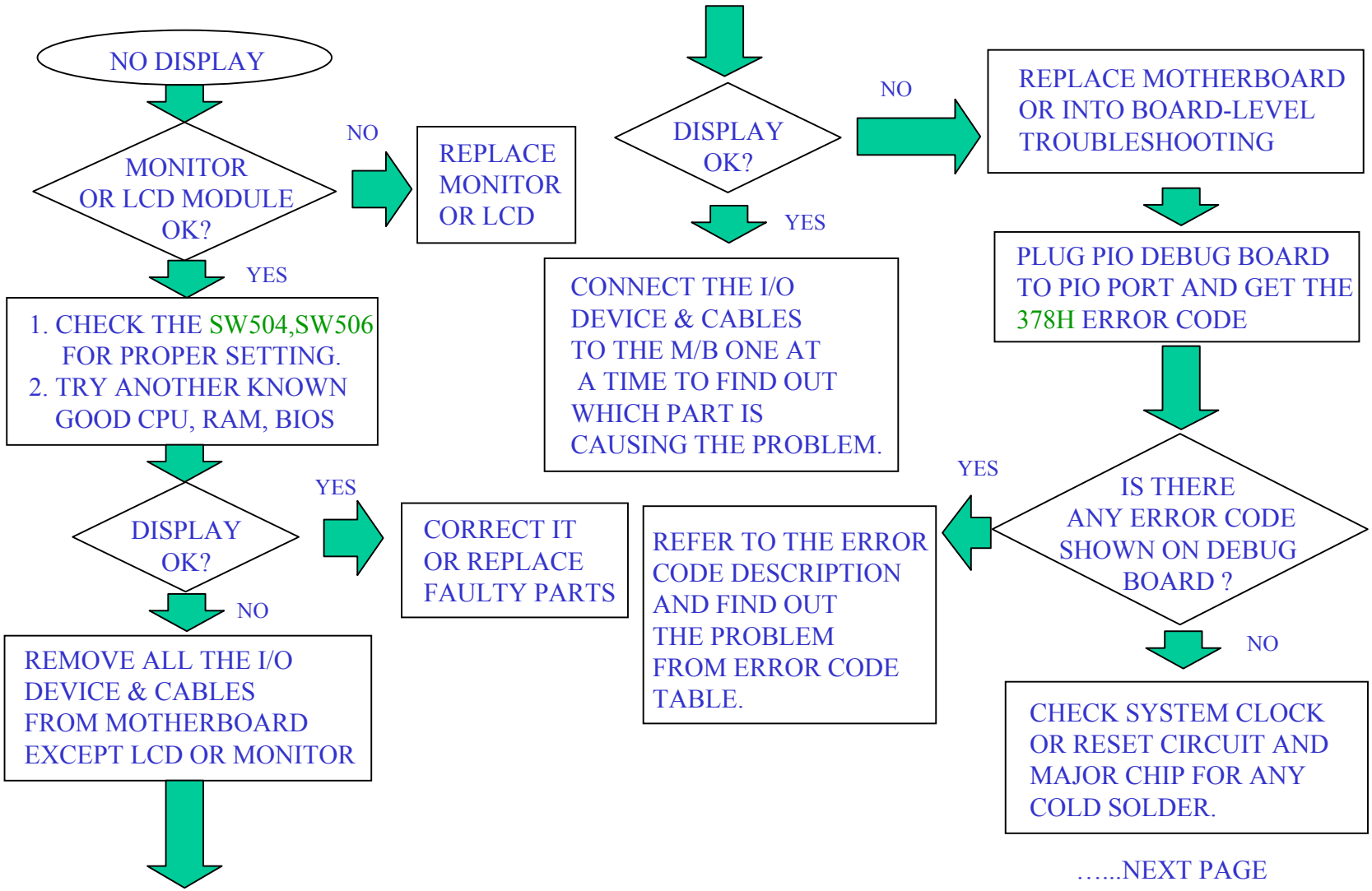
8.1 NO POWER:

WHEN THE POWER BUTTON IS PRESSED, NOTHING HAPPENS ,POWER INDICATOR DOES NOT LIGHT UP.



8.2 NO DISPLAY

THERE IS NO DISPLAY ON BOTH LCD AND MONITOR



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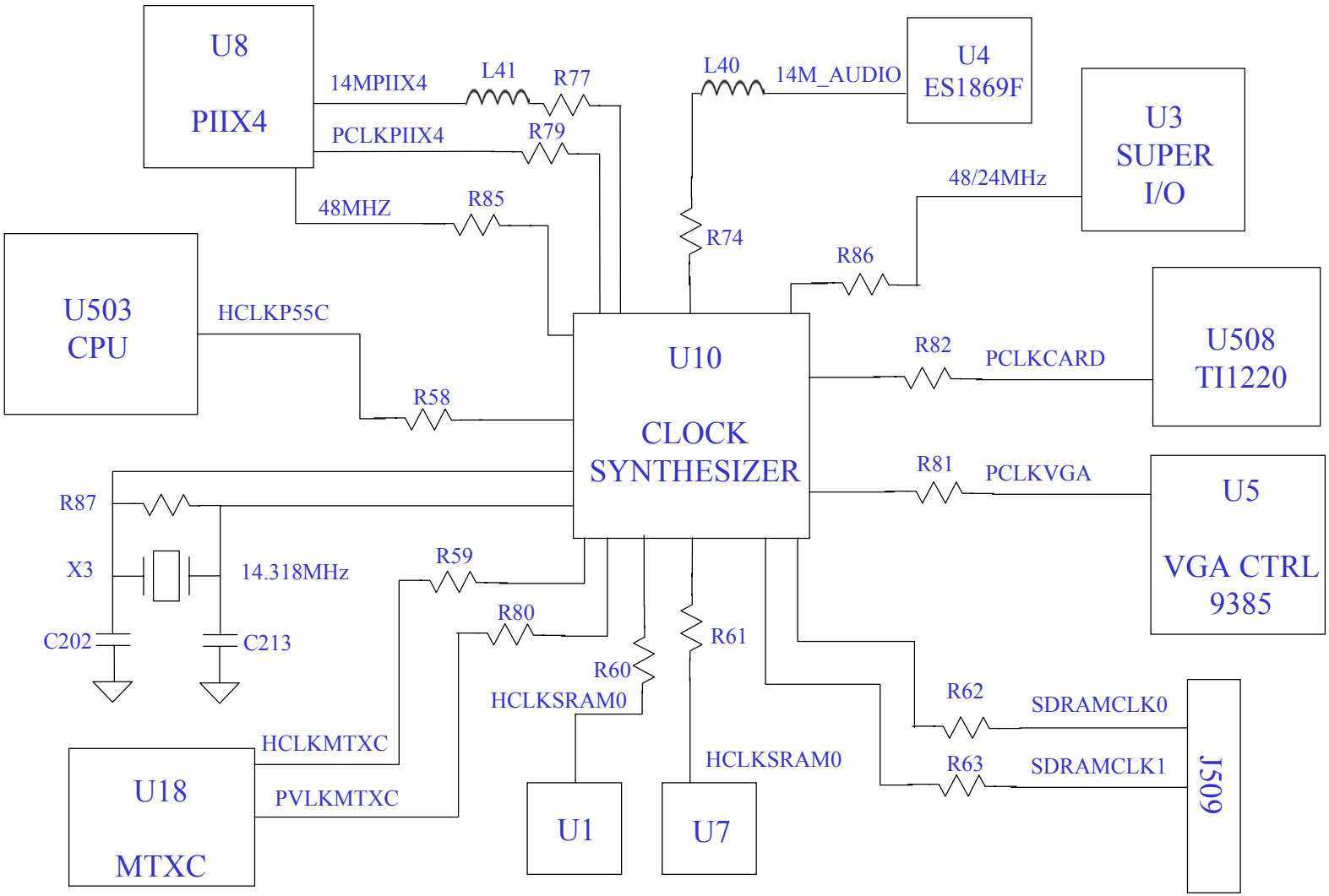
5033 M/B MAINTENANCE

8.2 NO DISPLAY

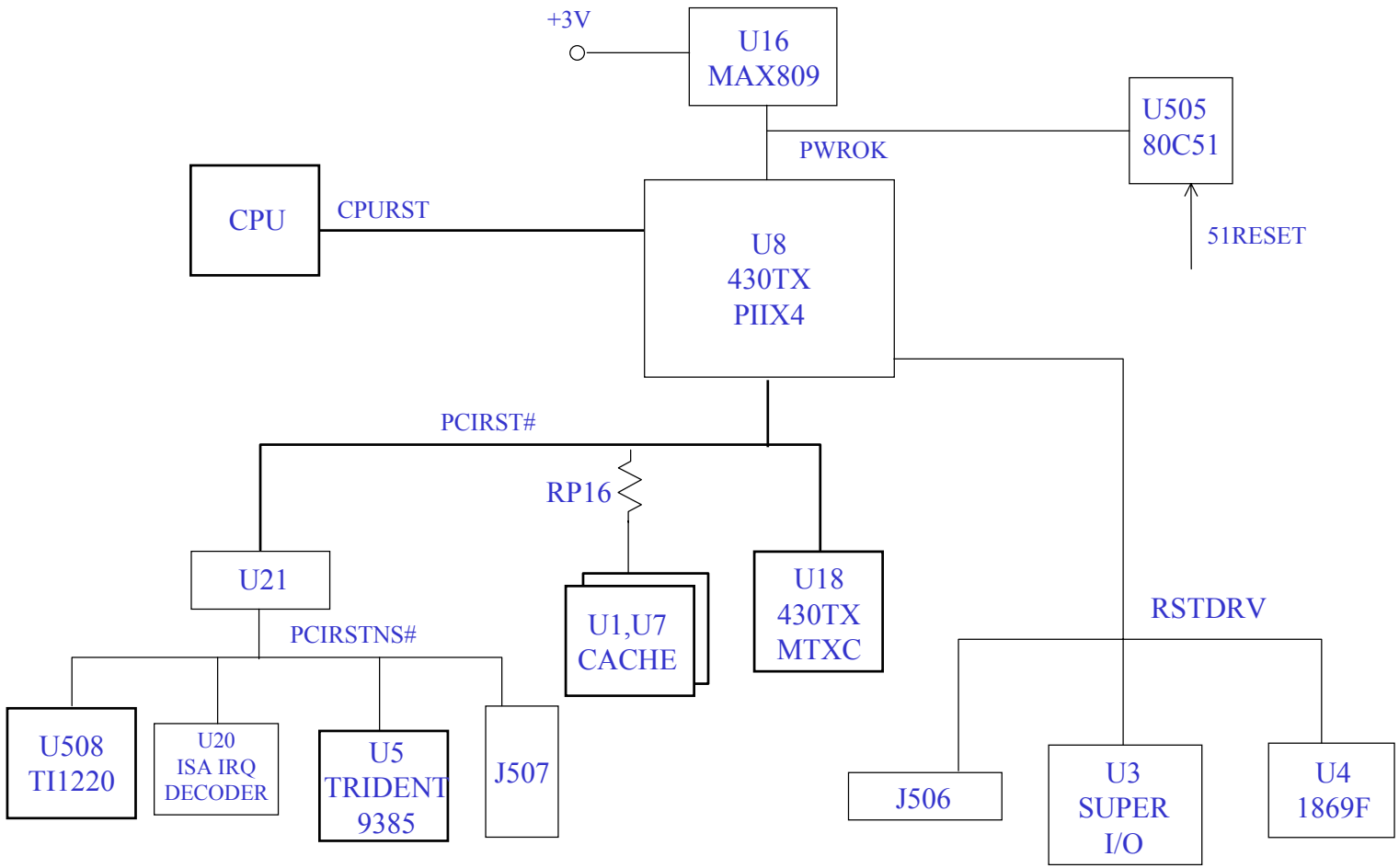
******SYSTEM CLOCK CHECK ******



5033 M/B MAINTENANCE

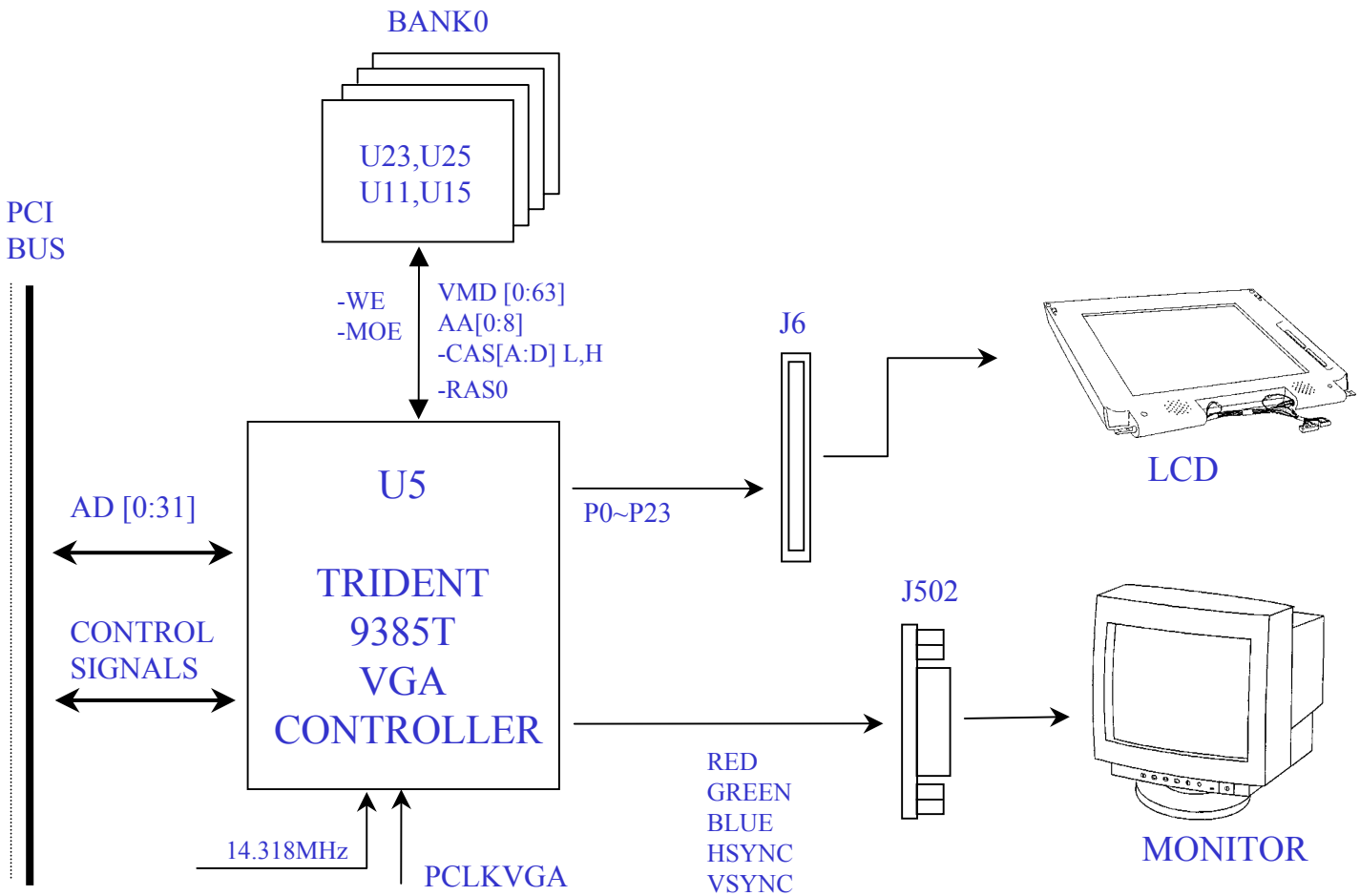
8.2 NO DISPLAY

******RESET SYSTEM ******



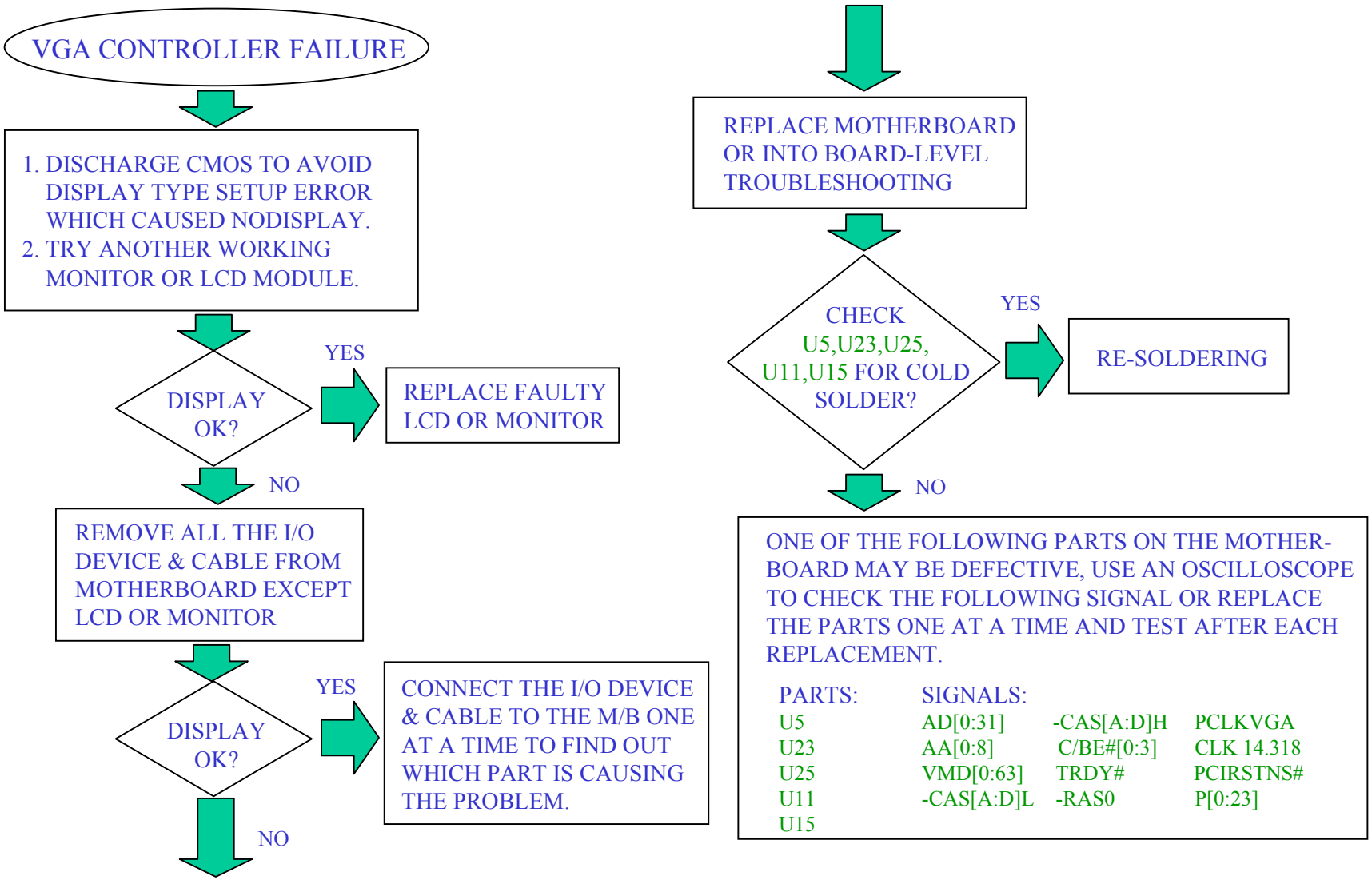
8.3 VGA CONTROLLERFAILURE

THERE IS NO DISPLAY ON BOTH LCD AND MONITOR ALTHOUGH POWER-ON-SELF-TEST IS PASSED.



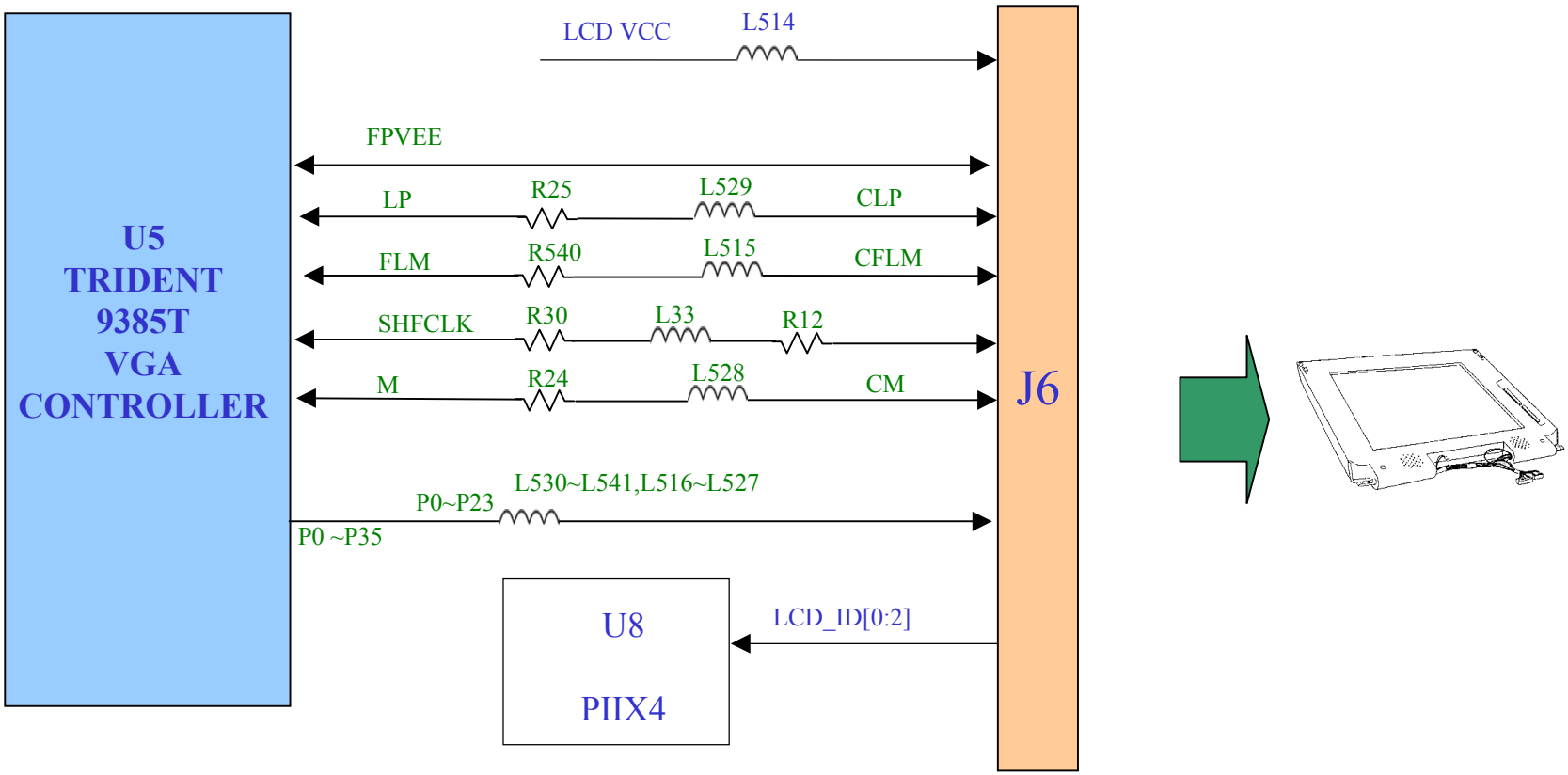
8.3 VGA CONTROLLERFAILURE

THERE IS NO DISPLAY ON BOTH LCD AND MONITOR ALTHOUGH POWER-ON-SELF-TEST IS PASSED.



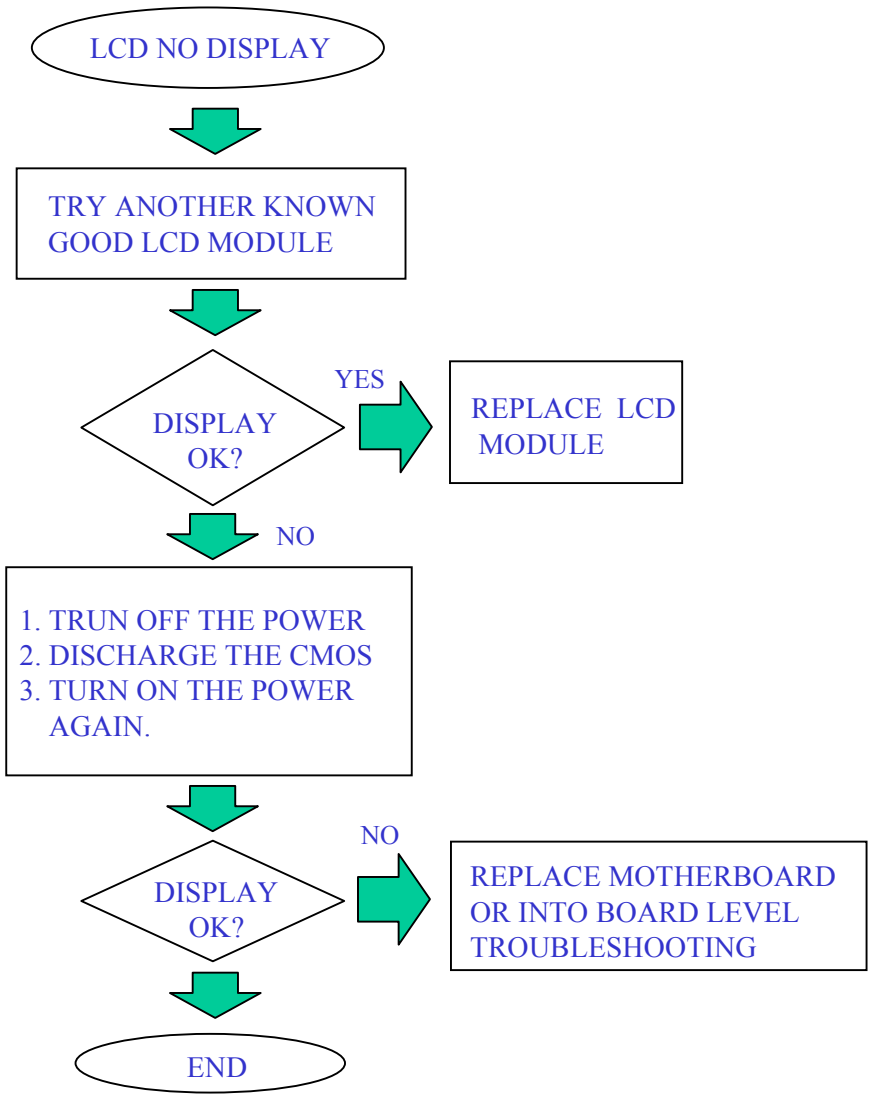
8.4 LCD NO DISPLAY

THE LCD SHOWS NOTHING OR ABNORMAL PICTURE , BUT IT IS OK FOR EXTERNAL MONITOR.



8.4 LCD NO DISPLAY

THE LCD SHOWS NOTHING OR ABNORMAL PICTURE , BUT IT IS OK FOR EXTERNAL MONITOR.



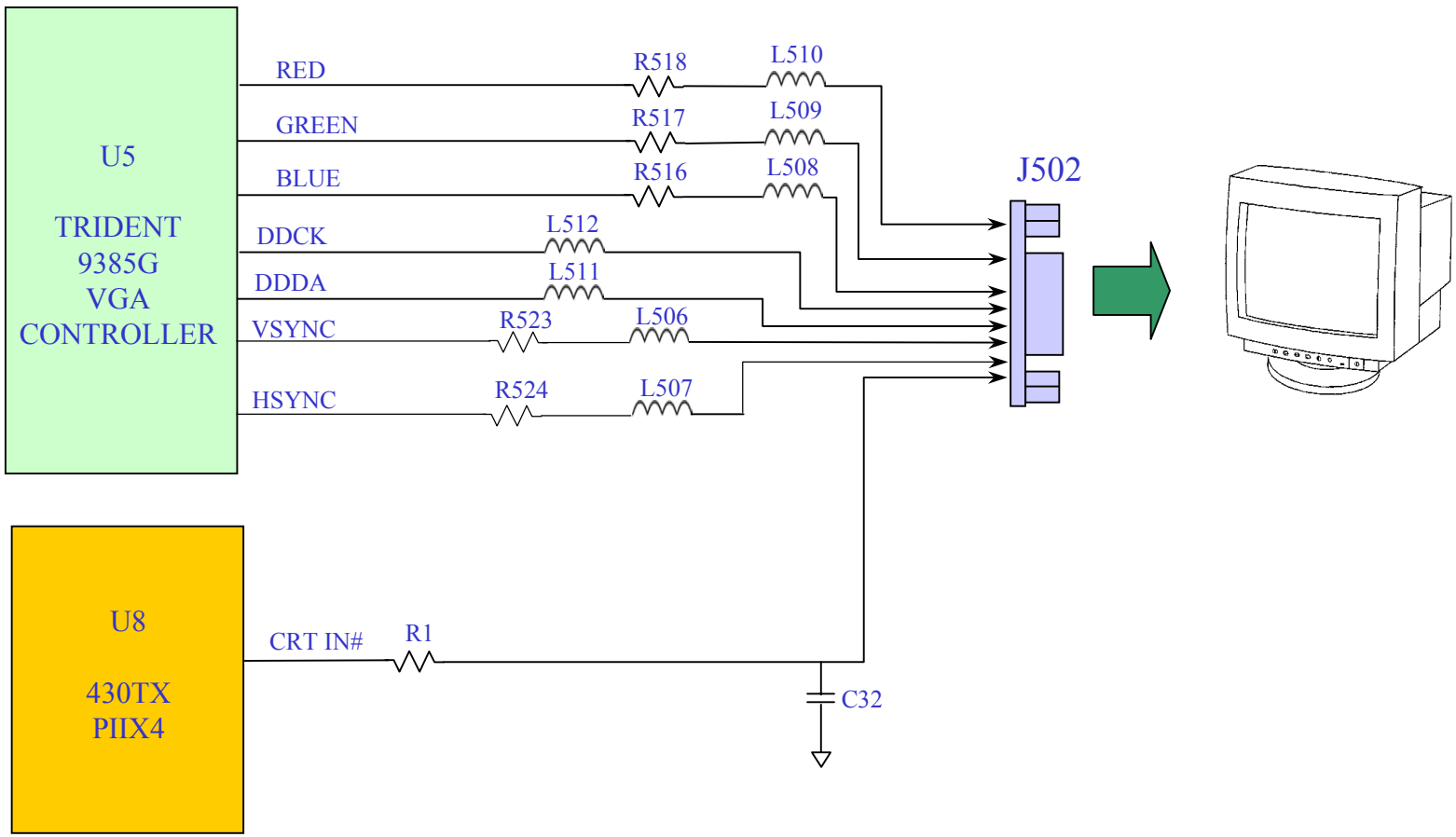
BOARD- LEVEL TROUBLESHOOTING

ONE OF THE FOLLOWING PARTS ON THE MOTHER-BOARD MAY BE DEFECTIVE, USE AN OSCILLOSCOPE TO CHECK THE FOLLOWING SIGNAL OR REPLACE THE PARTS ONE AT A TIME AND TEST AFTER EACH REPLACEMENT.

PARTS:	SIGNALS:	
U5,U8	FPVEE	M
L529~L541	P0~P23	VEEADJ
L515~L528	LP	LCD_ID[0:2]
R25,R30,L33	FLM	LCD_VCC
R24,R12,L514	SHFCLK	

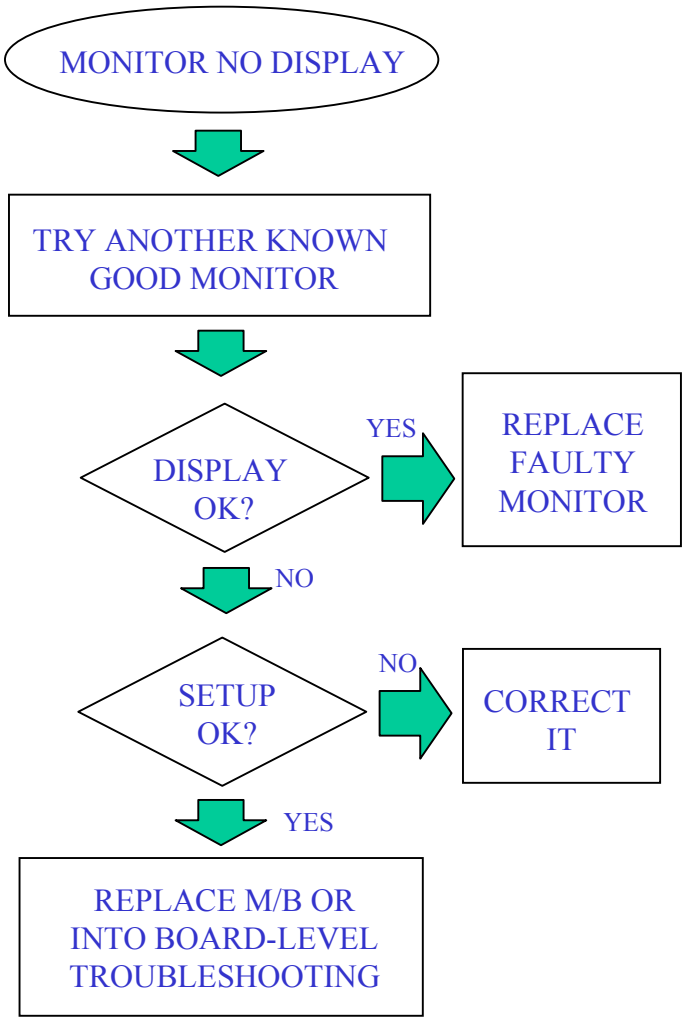
8.5 EXTERNAL MONITOR NO DISPLAY

THE CRT MONITOR SHOWS NOTHING OR ABNORMAL COLOR, BUT IT IS OK FOR LCD.



8.5 EXTERNAL MONITOR NO DISPLAY

THE CRT MONITOR SHOWS NOTHING OR ABNORMAL COLOR, BUT IT IS OK FOR LCD.



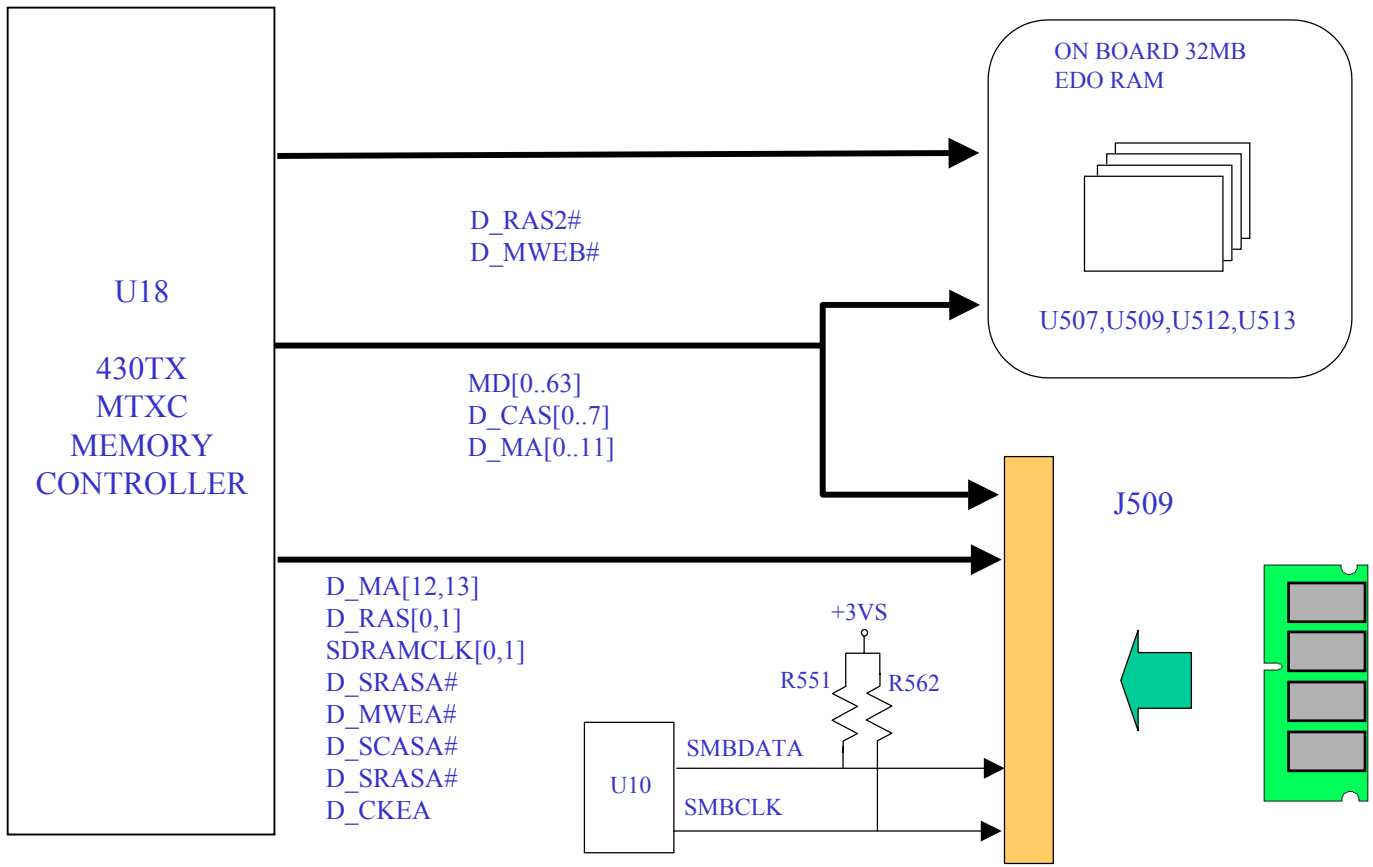
BOARD-LEVEL TROUBLESHOOTING FOR MONITOR NO DISPLAY

CHECK THE FOLLOWING PARTS FOR COLD SOLDER OR ONE OF THE FOLLOWING PARTS ON THE MOTHER-BOARD MAY BE DEFECTIVE, USE AN OSCILLOSCOPE TO CHECK THE FOLLOWING SIGNAL OR REPLACE THE PARTS ONE AT A TIME AND TEST AFTER EACH REPLACEMENT.

PARTS:	SIGNALS:	
U5,U8	RED	DDDA
L506~L510	GREEN	CRT_IN#
R1,R523,R524	BLUE	
R516~R518	VSYNC	
	HSYNC	
	DDCK	

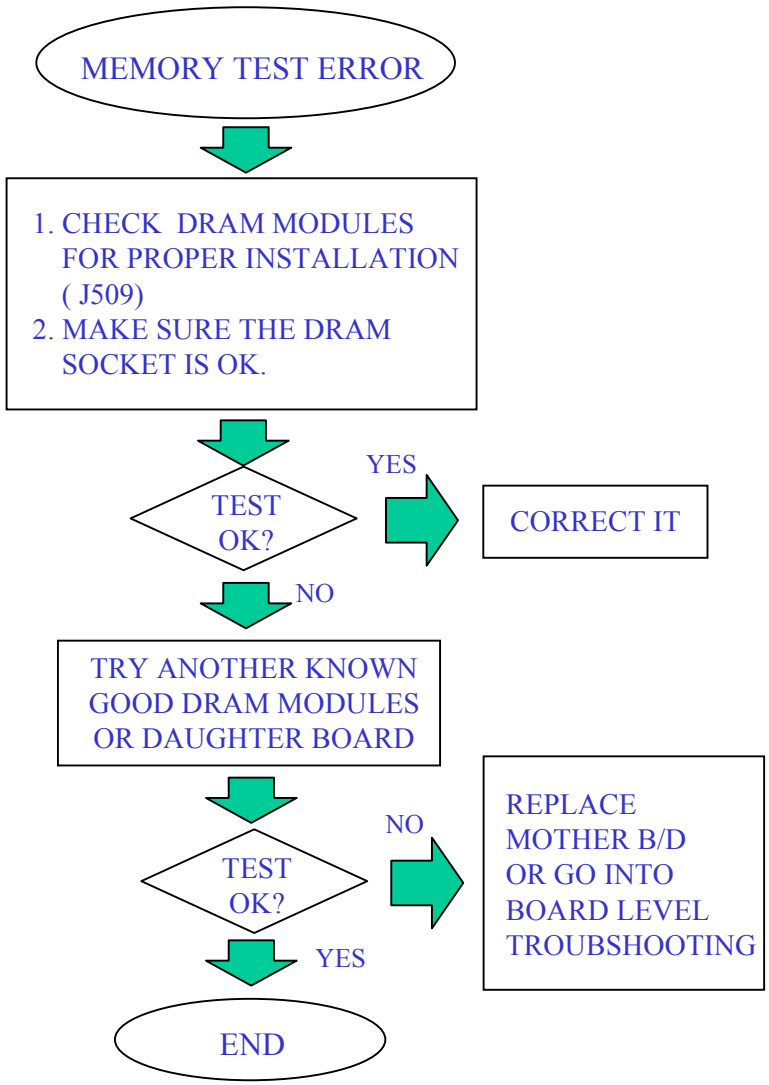
8.6 MEMORY TEST ERROR

THE ERROR CODE SHOWN ON THE PIO DEBUG BOARD IS 0FH, 13H,18H OR 27H AND SYSTEM HANGS UP.



8.6 MEMORY TEST ERROR

THE ERROR CODE SHOWN ON THE PIO DEBUG BOARD IS 0FH, 13H,18H OR 27H AND SYSTEM HANGS UP.



BOARD-LEVEL TROUBLESHOOTING FOR MEMORY TEST ERROR

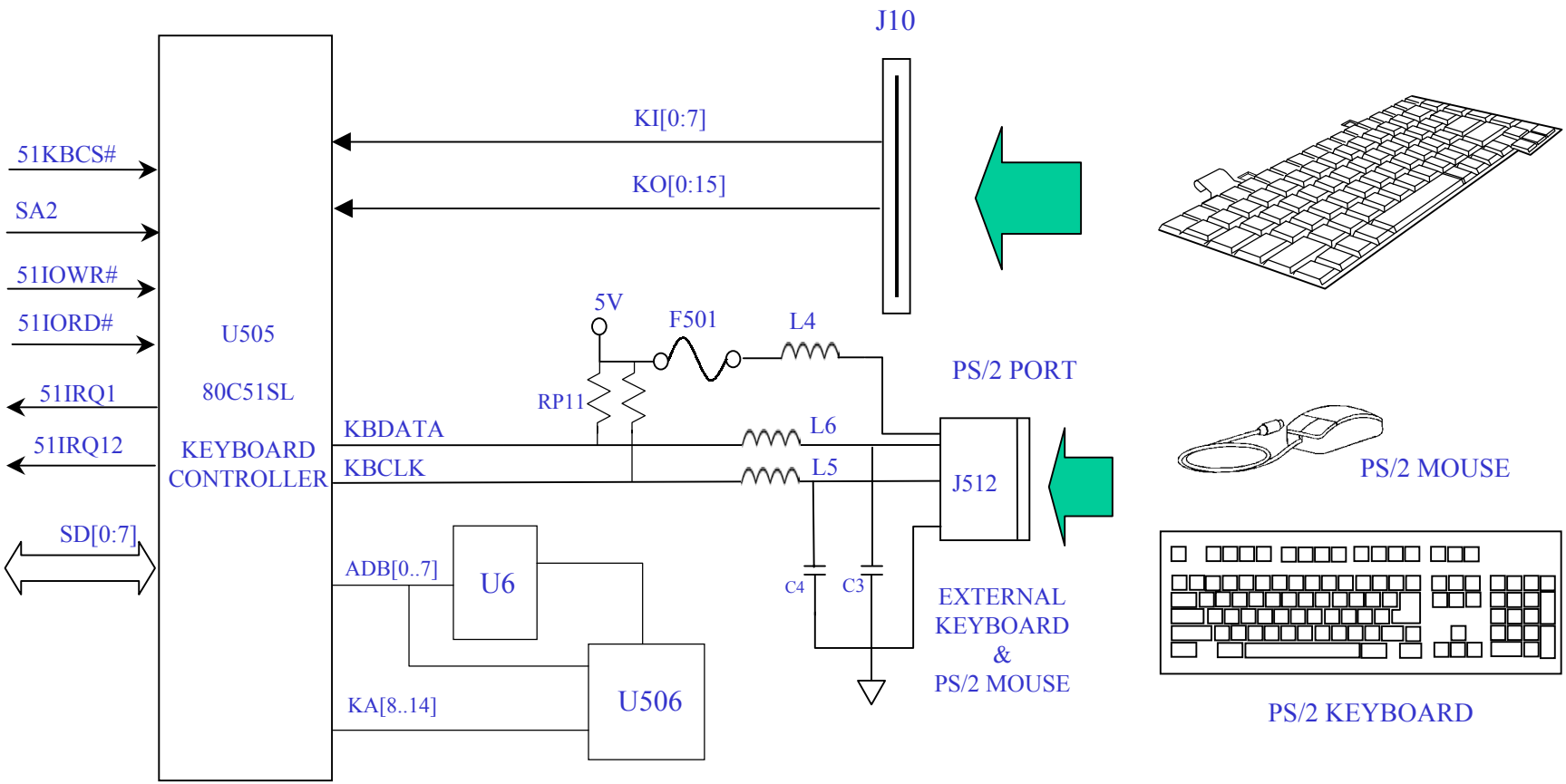
CHECK THE FOLLOWING PARTS FOR COLD SOLDER OR ONE OF THE FOLLOWING PARTS ON THE MOTHER-BOARD MAY BE DEFECTIVE, USE AN OSCILLOSCOPE TO CHECK THE FOLLOWING SIGNAL OR REPLACE THE PARTS ONE AT A TIME AND TEST AFTER EACH REPLACEMENT.

PARTS:	SIGNALS:	
U507,U509	MD[0:63]	D_SCASA#
U512,U513	D_CAS[0:7]#	D_SRASA#
U18,U10	D_RAS[0:2]#	D_CKEA
RP31,RP33	D_MA[0:13]	SDRAMCLK[0:1]
RP34~RP39	D_MWEA#	SMBCLK
RP1251,RP1161	D_MWEB#	SMBDATA
RP1281,RP1141		

5033 M/B MAINTENANCE

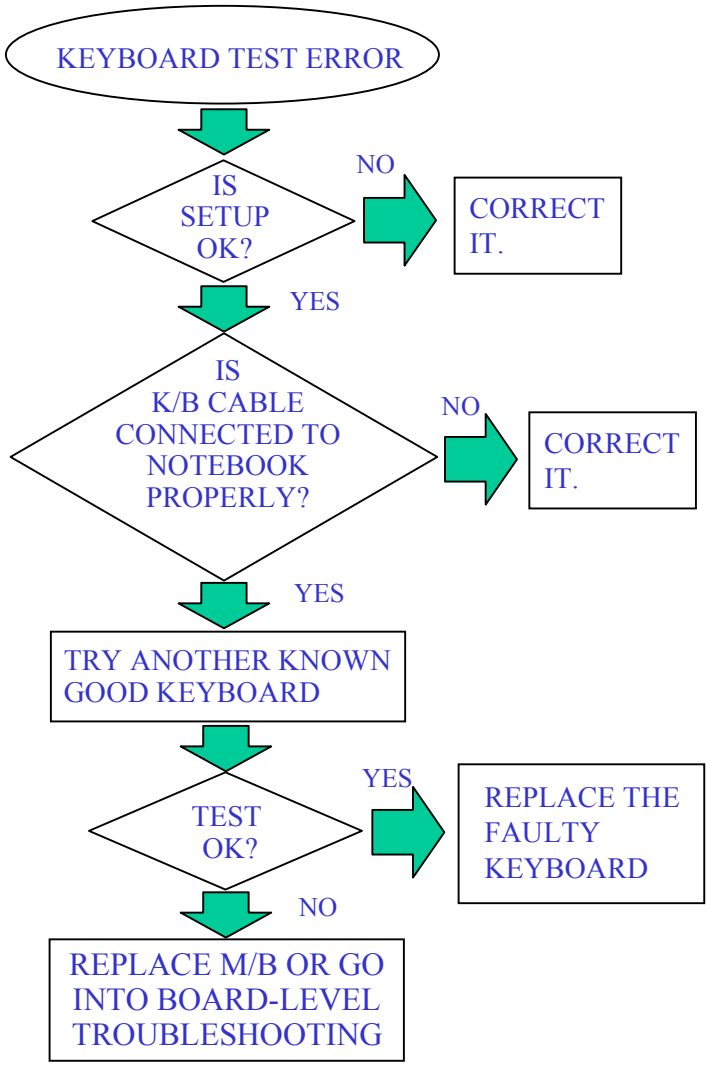
8.7 KEYBOARD TEST ERROR

1. ERROR MESSAGE OF KEYBOARD FAILURE IS SHOWN OR ANY KEY DOESN′ T WORK.
2. PIO DEBUG BOARD SHOWS THAT THE PORT 378H ERROR CODE IS STOPPED AT 30H,31H, 32H OR 33H



8.7 KEYBOARD TEST ERROR

1. ERROR MESSAGE OF KEYBOARD FAILURE IS SHOWN OR ANY KEY DOESN′ T WORK.
2. PIO DEBUG BOARD SHOWS THE PORT 378H ERROR CODE IS STOPPED AT 30H,31H,32H,33H



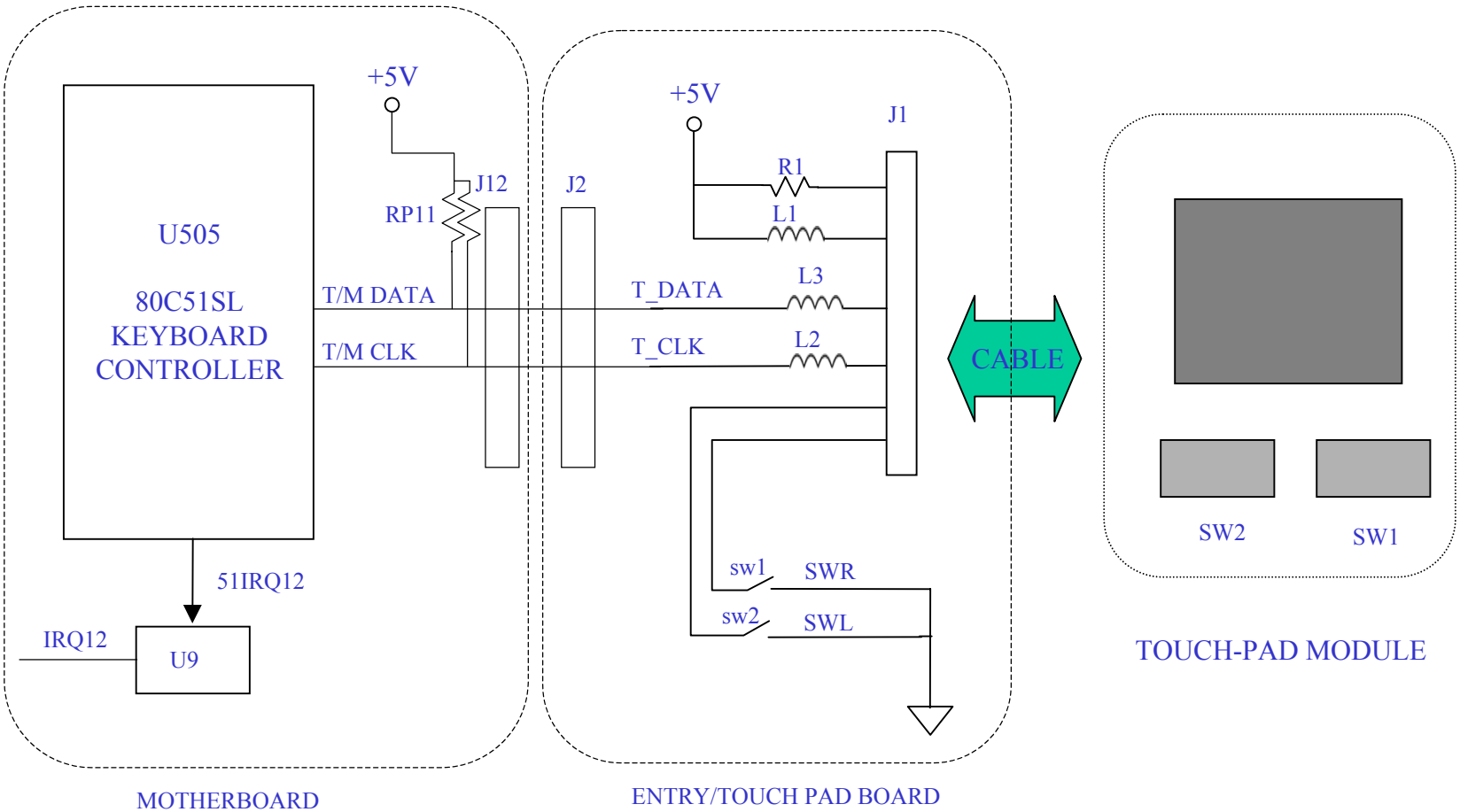
BOARD-LEVEL TROUBLESHOOTING FOR KEYBOARD TEST ERROR

CHECK THE FOLLOWING PARTS FOR COLD SOLDER OR ONE OF THE FOLLOWING PARTS ON THE MOTHER-BOARD MAY BE DEFECTIVE, USE AN OSCILLOSCOPE TO CHECK THE FOLLOWING SIGNAL OR REPLACE THE PARTS ONE AT A TIME AND TEST AFTER EACH REPLACEMENT.

PARTS:	SIGNALS:		
U505	ADB[0..7]	SA2	51RESET
U506	KI[0:7]	51IOWR#	16MHz
U6	KO[0:15]	51IORD#	KA[8..14]
U8	KBDATA	51IRQ1	
	KBCLK	51IRQ12	
	51KBCS#	SD[0:7]	

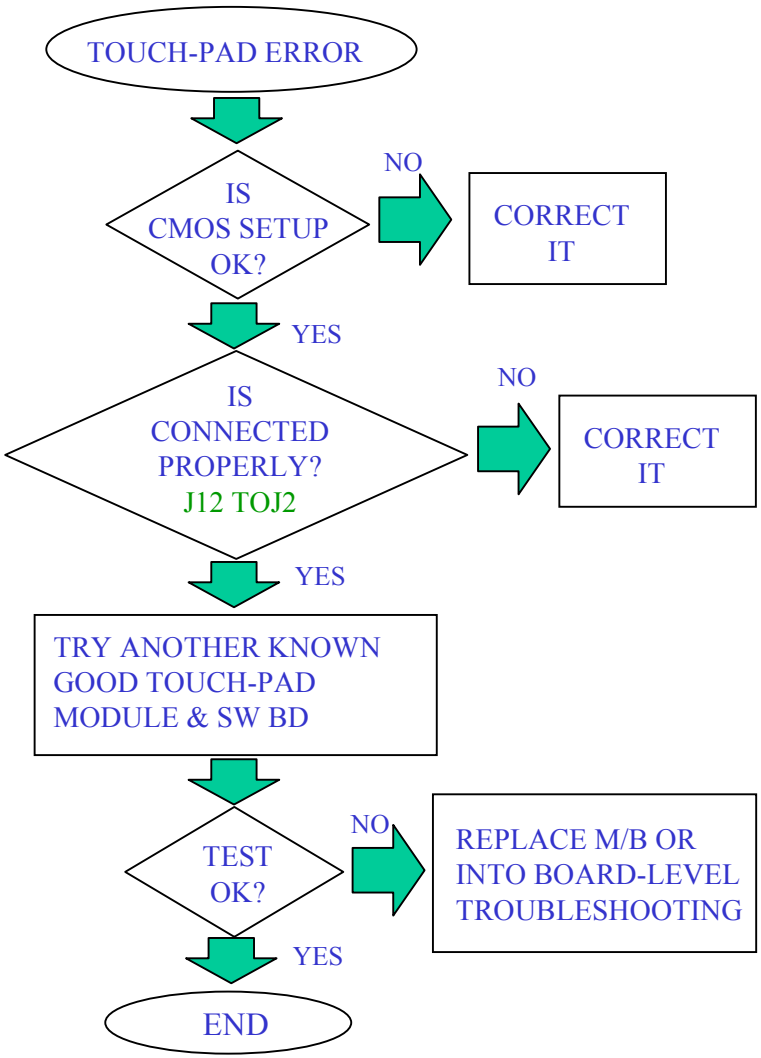
8.8 TRACK PAD TEST ERROR

AN ERROR MESSAGE IS SHOWN WHEN TOUCH-PAD IS ENABLED.



8.8 TRACK PAD TEST ERROR

AN ERROR MESSAGE IS SHOWN WHEN TOUCH-PAD IS ENABLED.



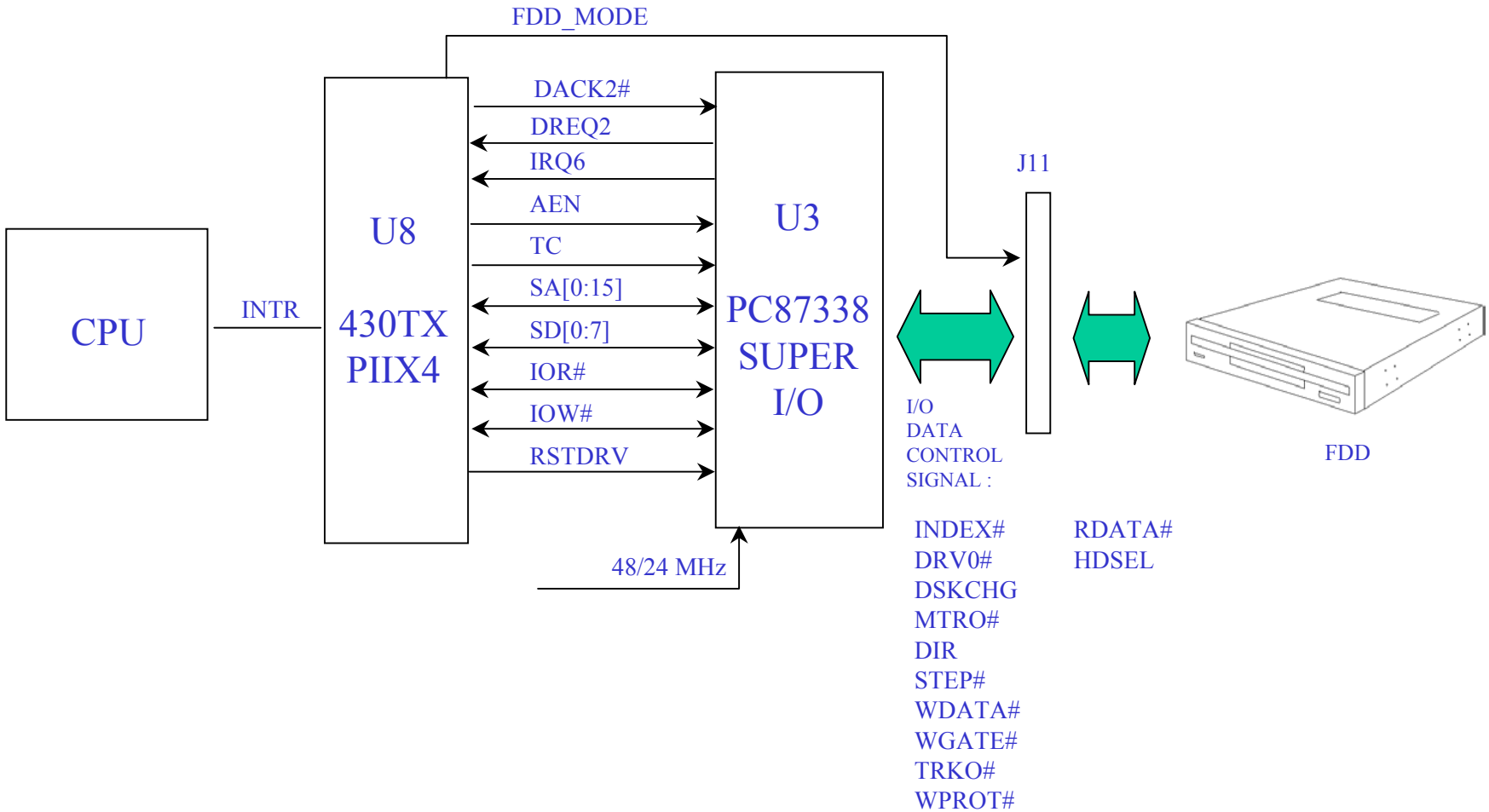
BOARD-LEVEL TROUBLESHOOTING FOR TOUCH-PAD TEST ERROR

CHECK THE FOLLOWING PARTS FOR COLD SOLDER OR ONE OF THE FOLLOWING PARTS ON THE MOTHER-BOARD MAY BE DEFECTIVE, USE AN OSCILLOSCOPE TO CHECK THE FOLLOWING SIGNAL OR REPLACE THE PARTS ONE AT A TIME AND TEST AFTER EACH REPLACEMENT.

PARTS:	SIGNALS:	
RP11	T/M DATA	51IRQ12
U505	T/M CLK	
U9	5V	
ENTRY/TOUCH BD		

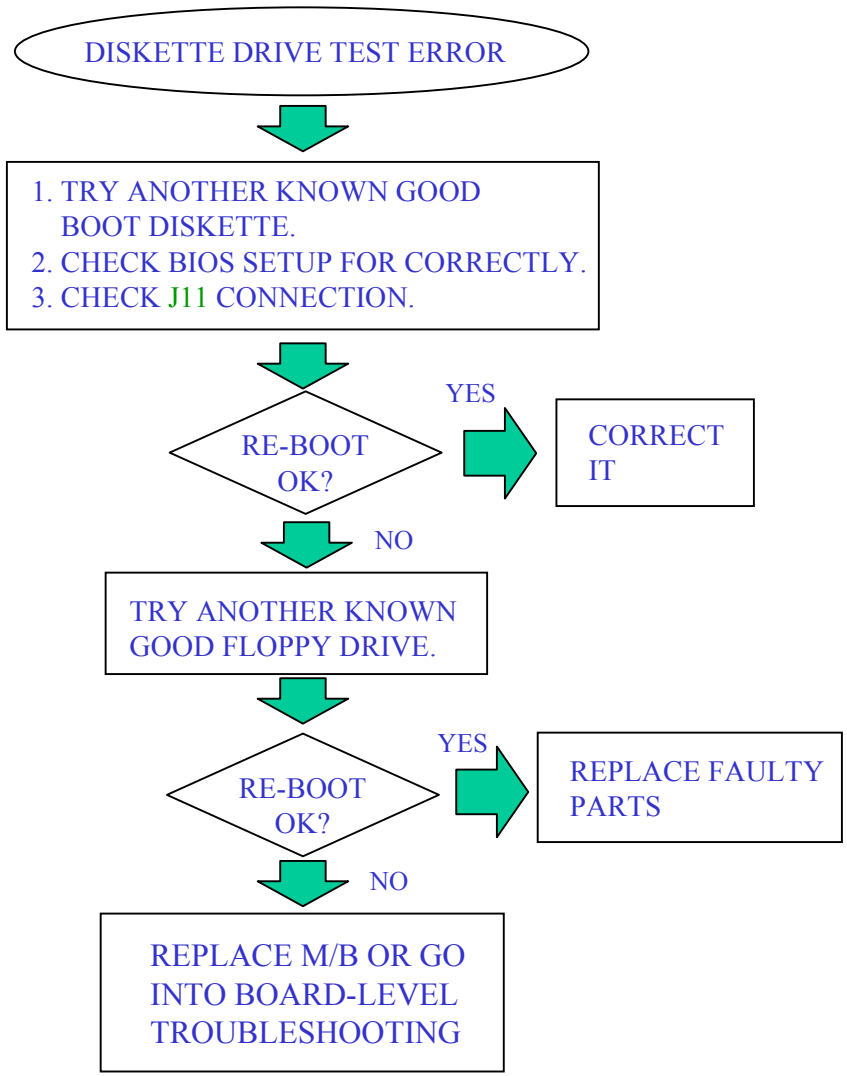
8.9 DISKETTE DRIVE TEST ERROR

AN ERROR MESSAGE IS SHOWN WHEN READING/ WRITING DATA FROM/TO DISKETTE DRIVE.



8.9 DISKETTE DRIVE TEST ERROR

AN ERROR MESSAGE IS SHOWN WHEN READING/ WRITING DATA FROM/TO DISKETTE DRIVE.



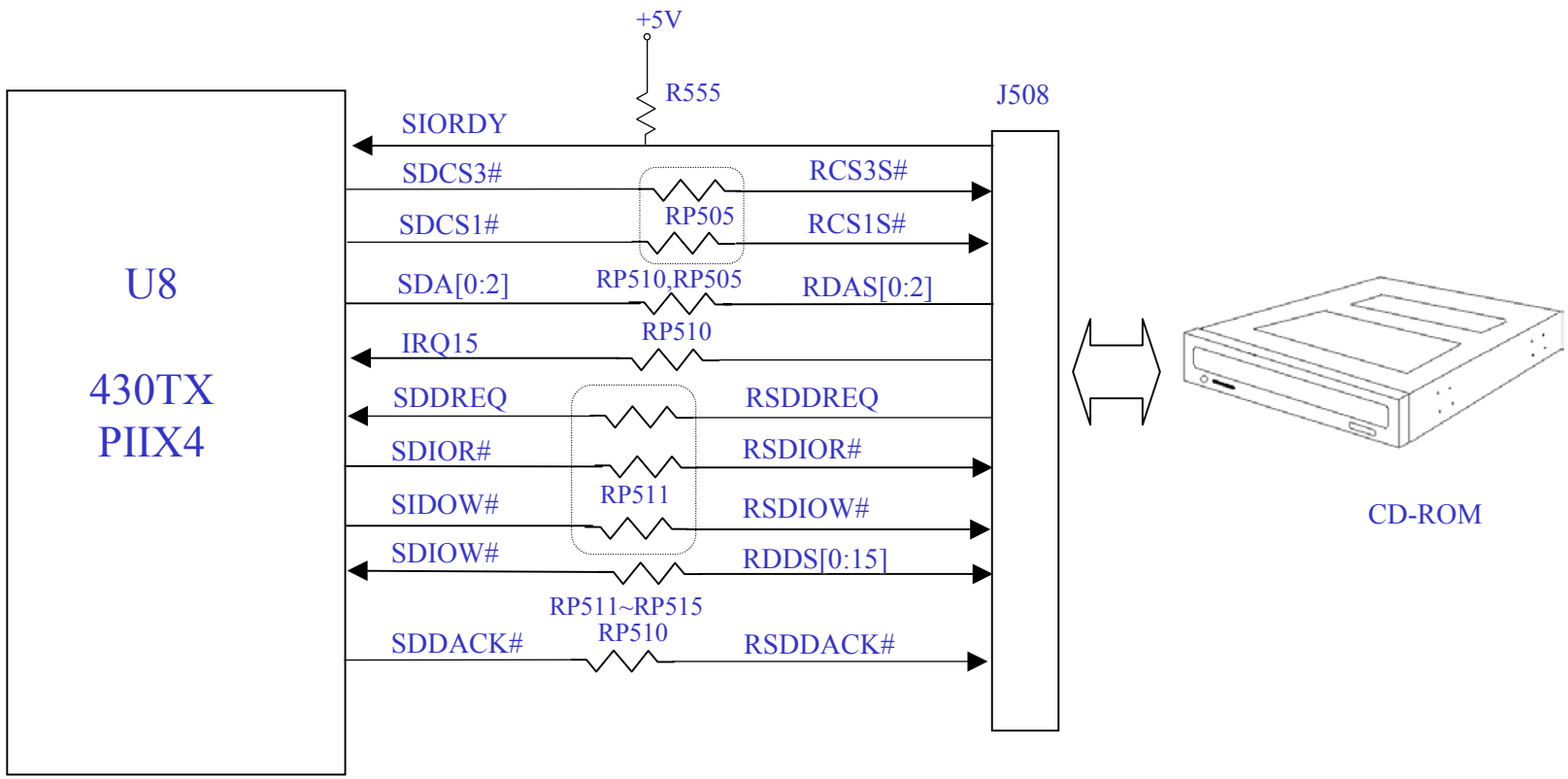
BOARD-LEVEL TROUBLESHOOTING FOR TOUCH-PAD TEST ERROR

CHECK THE FOLLOWING PARTS FOR COLD SOLDER OR ONE OF THE FOLLOWING PARTS ON THE MOTHER-BOARD MAY BE DEFECTIVE, USE AN OSCILLOSCOPE TO CHECK THE FOLLOWING SIGNAL OR REPLACE THE PARTS ONE AT A TIME AND TEST AFTER EACH REPLACEMENT.

PARTS:	SIGNALS:			
U3	DACK2#	SD[0:7]	INDEX#	TRKO#
U8	DREQ2	IOR#	FDD_MODE	RDATA#
RP40	IRQ6	IOW#	DSKCHG	WDATA#
L44	AEN	RSTDRV	RDATA#	WGATE#
R7	TC	24MHz	WPROT#	HDSEL#
D4	SA[0:15]		MTRO#	DIR#
FA[1..3]				STEP#
				DRVO#

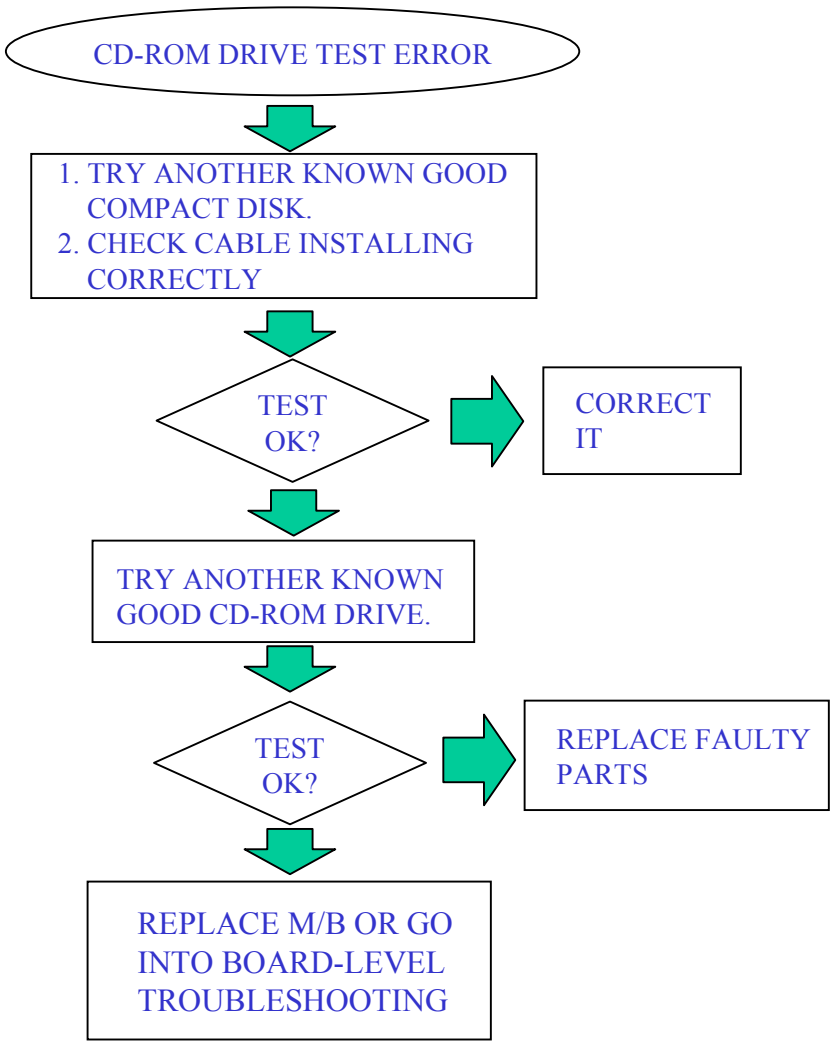
8.10 CD-ROM DRIVE TEST ERROR

AN ERROR MESSAGE IS SHOWN WHEN READING DATA FROM CD-ROM DRIVE.



8.10 CD-ROM DRIVE TEST ERROR

AN ERROR MESSAGE IS SHOWN WHEN READING GATA FROM CD-ROM DRIVE.



BOARD-LEVEL TROUBLESHOOTING FOR CD-ROM DRIVE TEST ERROR

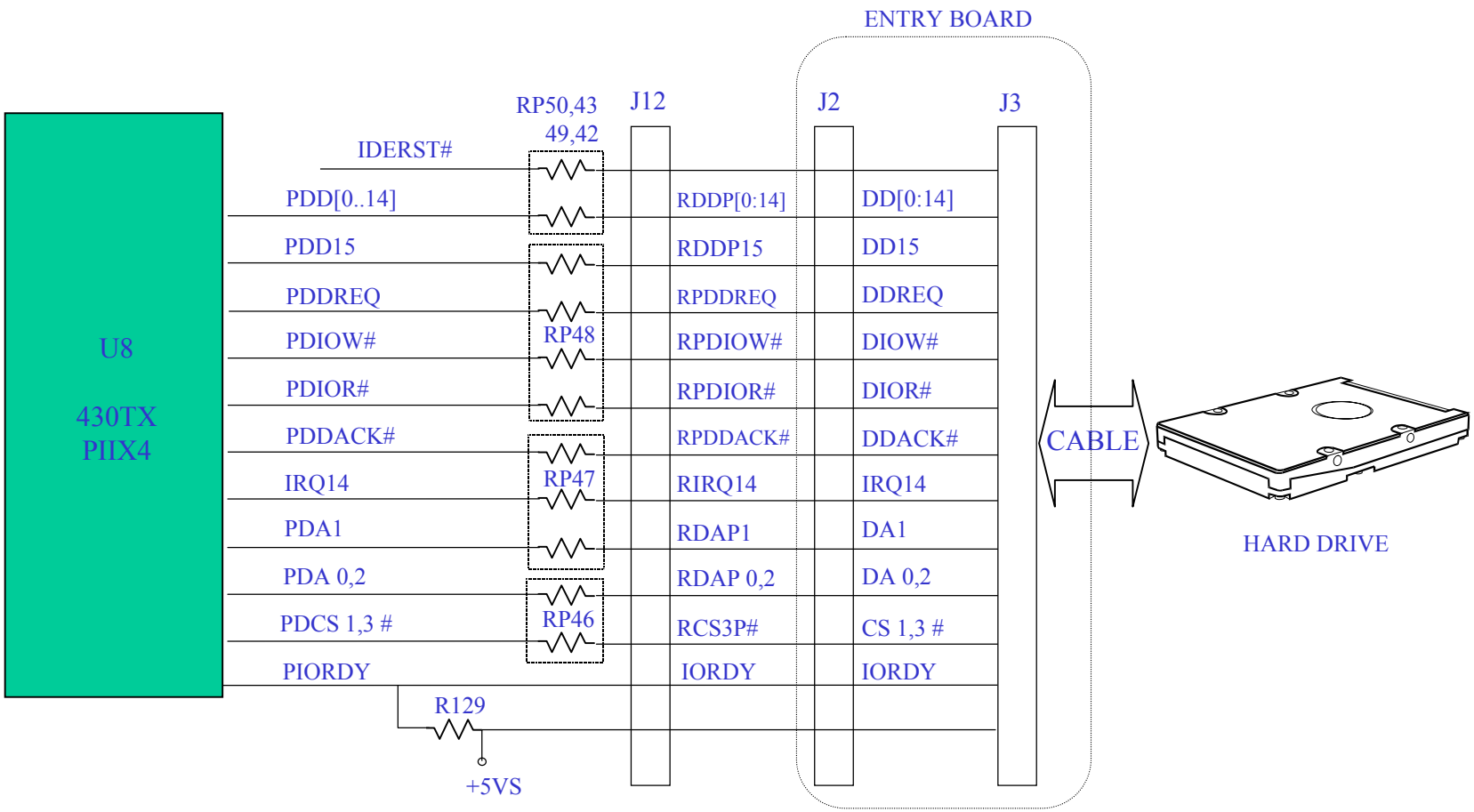
CHECK THE FOLLOWING PARTS FOR COLD SOLDER OR ONE OF THE FOLLOWING PARTS ON THE MOTHER-BOARD MAY BE DEFECTIVE, USE AN OSCILLOSCOPE TO CHECK THE FOLLOWING SIGNAL OR REPLACE THE PARTS ONE AT A TIME AND TEST AFTER EACH REPLACEMENT.

PARTS:	SIGNALS:			
U8	SDCS3#	SDIOR#	RCS3S#	RSDIOP#
RP10~RP15	SDCS1#	SDIOW#	RSC1S#	RSDIOW#
RP505	SDA2	SDDREQ	RDAS2	RSDDREQ
	SDA1	SDDACK#	RDAS1	RSDDACK#
	SDA0	SDD[0:15]	RDAS0	RDDS[0:15]
	IRQ15		RIRQ15	
	SIORDY		RSDIOR#	

5033 M/B MAINTENANCE

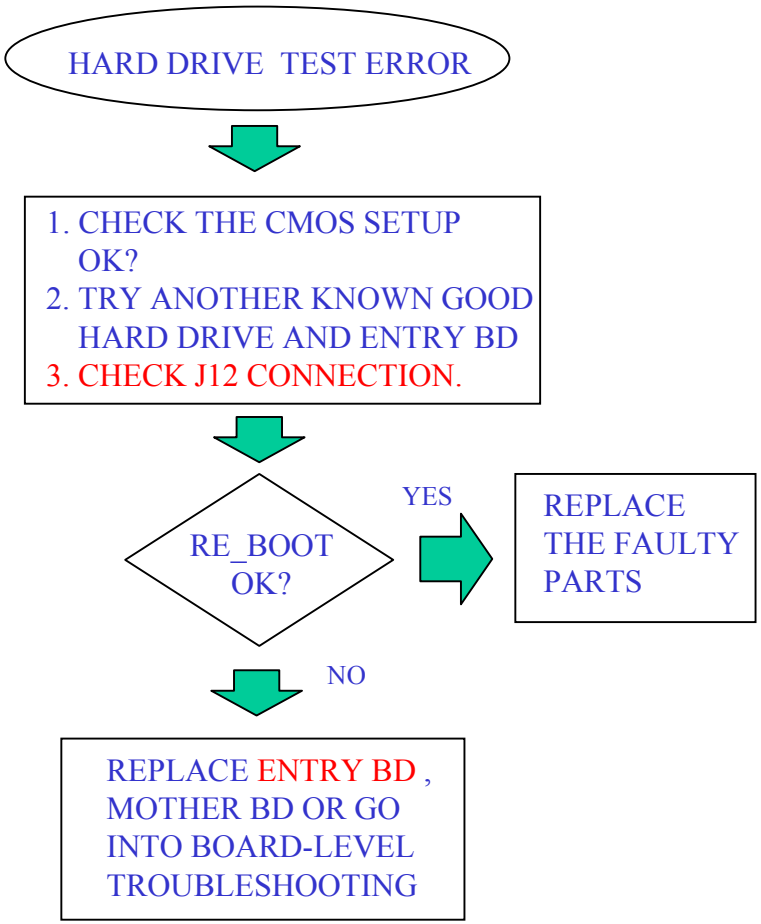
8.11 HARD DRIVE TEST ERROR

EITHER AN ERROR MESSAGE IS SHOWN , OR THE DRIVER MOTOR CONTINUES SPINNING , WHILE READING DATA IS FROM OR WRITING DATA IS TO HARD-DISK.



8.11 HARD DRIVE TEST ERROR

EITHER AN ERROR MESSAGE IS SHOWN , OR THE DRIVER MOTOR CONTINUES SPINNING , WHILE READING DATA IS FROM OR WRITING DATA IS TO HARD-DISK.



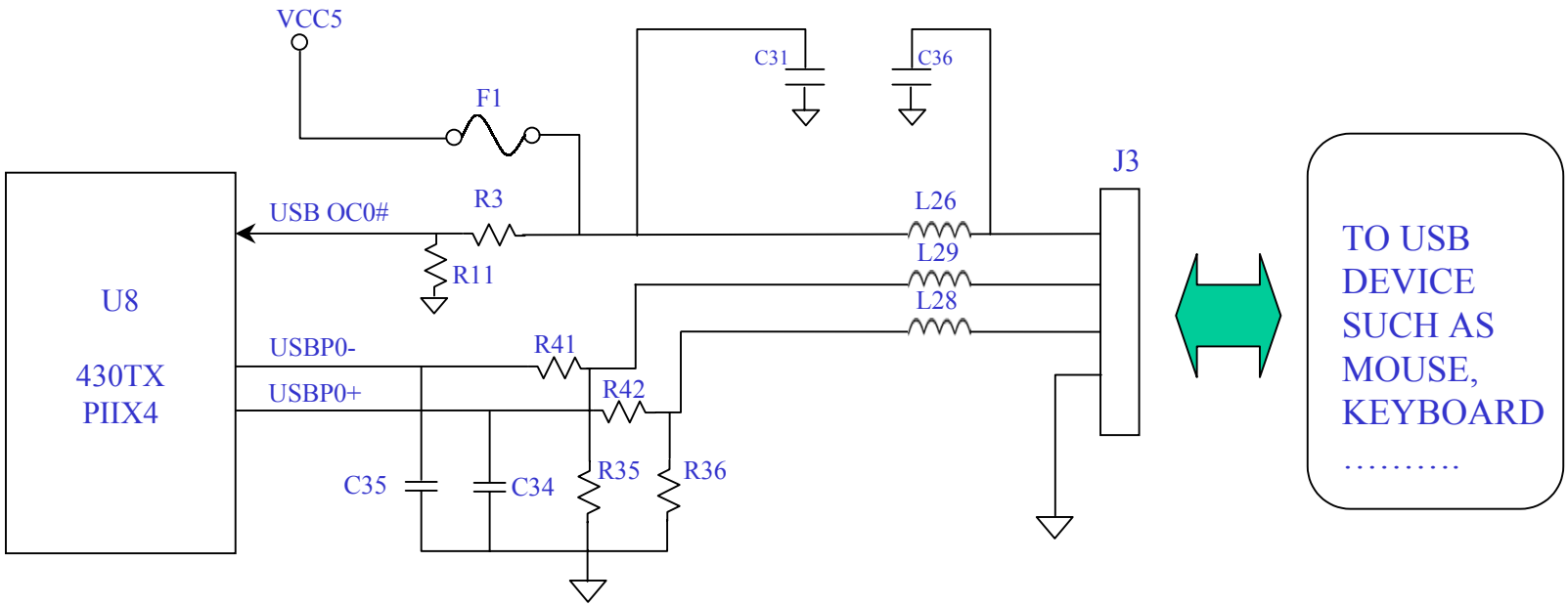
BOARD-LEVEL TROUBLESHOOTING FOR HARD DRIVE TEST ERROR

CHECK THE FOLLOWING PARTS FOR COLD SOLDER OR ONE OF THE FOLLOWING PARTS ON THE MOTHER-BOARD MAY BE DEFECTIVE, USE AN OSCILLOSCOPE TO CHECK THE FOLLOWING SIGNAL OR REPLACE THE PARTS ONE AT A TIME AND TEST AFTER EACH REPLACEMENT.

PARTS:	SIGNALS:	
U8,R554	PDDREQ	PDIOR#
RP42	PIORDY	PDIOW#
RP43	IRQ14	PDD[0:15]
RP46~RP50	PDA[0:2]	IDERST#
ENTRY BD	PDCS1#	5VS
	PDCS3#	
	PDDACK#	

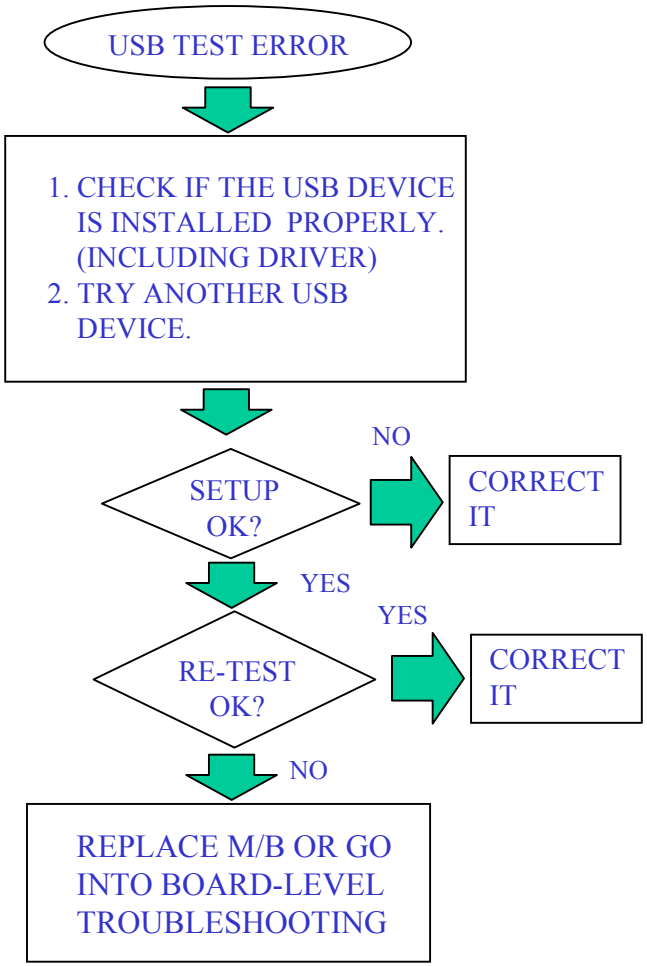
8.12 USB PORT TEST ERROR

AN ERROR OCCURS WHEN A USB I/O DEVICE IS INSTALLED.



8.12 USB PORT TEST ERROR

AN ERROR OCCURS WHEN A USB I/O DEVICE IS INSTALLED.



BOARD-LEVEL TROUBLESHOOTING FOR USB TEST ERROR

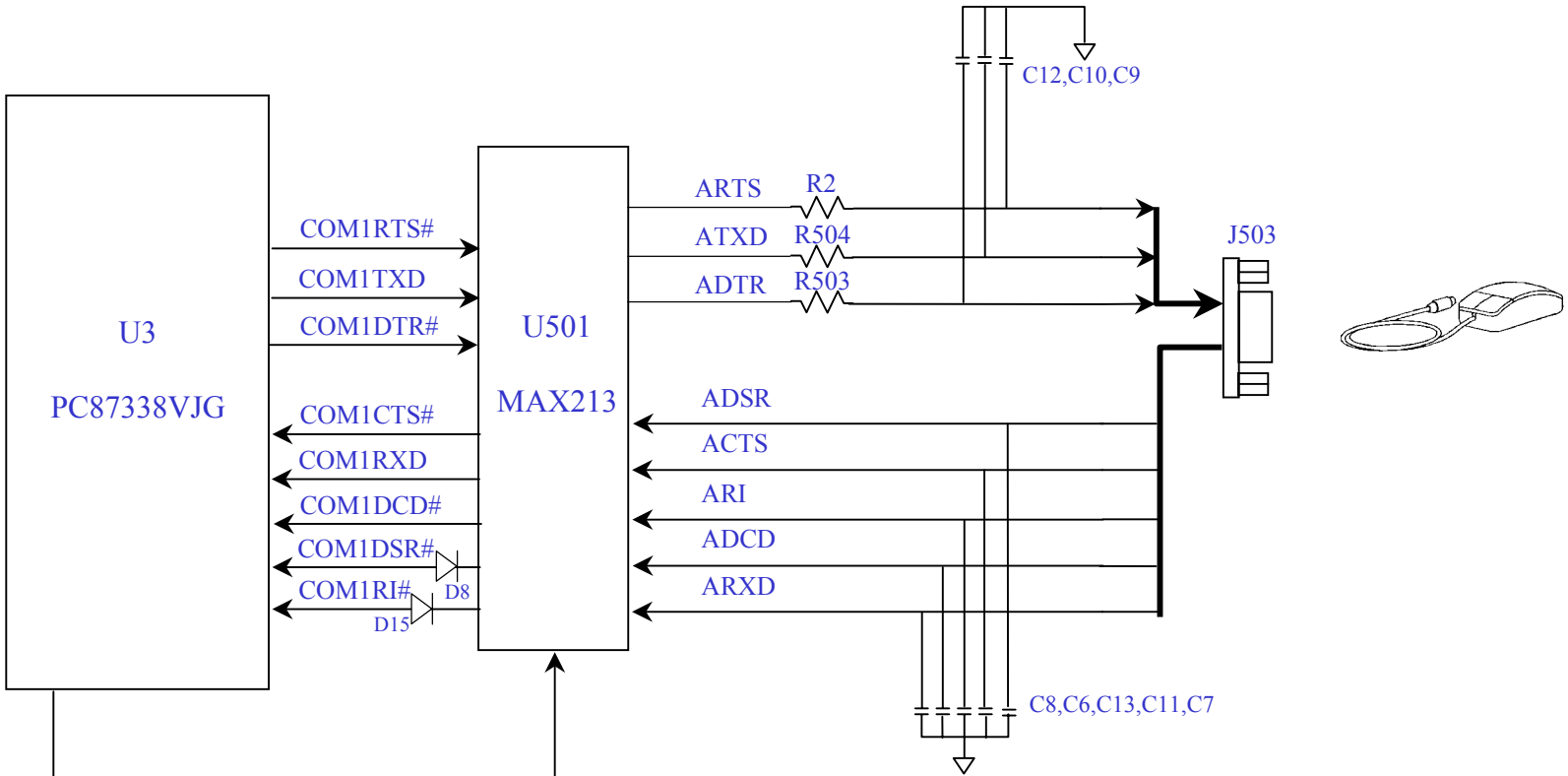
CHECK THE FOLLOWING PARTS FOR COLD SOLDER OR ONE OF THE FOLLOWING PARTS ON THE MOTHER-BOARD MAY BE DEFECTIVE, USE AN OSCILLOSCOPE TO CHECK THE FOLLOWING SIGNAL OR REPLACE THE PARTS ONE AT A TIME AND TEST AFTER EACH REPLACEMENT.

PARTS:
U8
F1
L26,R3,R11
J3,R41,R35
R42,R36
L28,L29
C34,C35

SIGNALS:
USB_OC0#
USBPO-
USBPO+

8.13 SIO PORT TEST ERROR

AN ERROR OCCURS WHEN A MOUSE OR OTHER I/O DEVICE IS INSTALLED.



PIN DEFINITION OF SIO PORT:

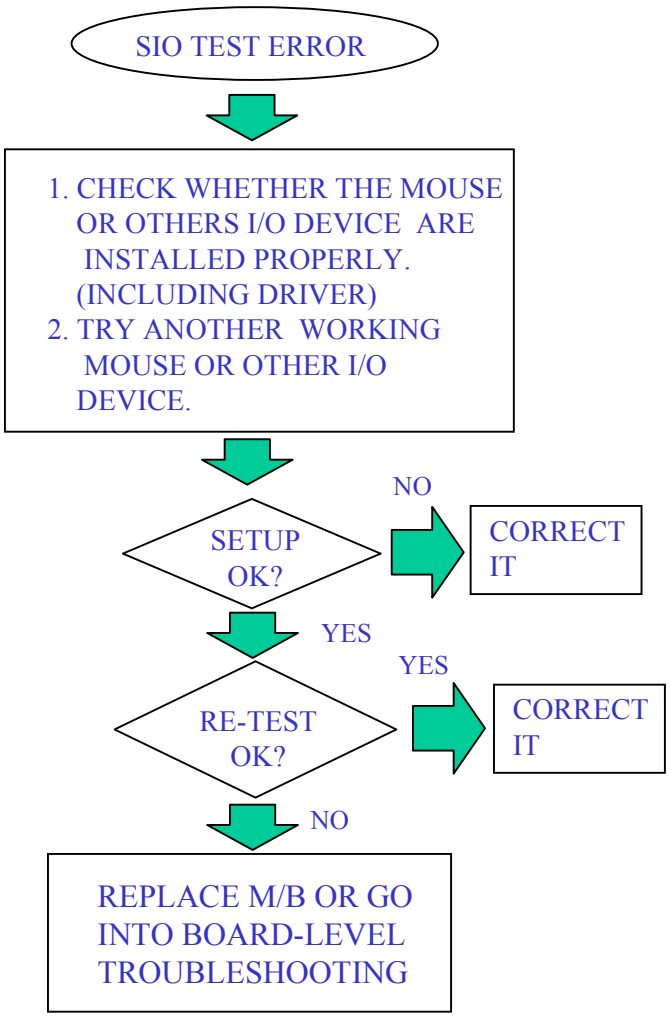
PIN 1 :	DCD-----	DATA CARRIER DETECT	PIN 6 :	DSR------	DATA SET READY
PIN 2 :	RD-------	RECEIVE DATA	PIN 7 :	RTS------	REQUEST TO SEND
PIN 3 :	TD-------	TRANSMIT DATA	PIN 8 :	CTS------	CLEAR TO SEND
PIN 4 :	DTR-----	DATA TERMINAL READY	PIN 9 :	RI--------	RING INDICATOR
PIN 5 :	SG--------	SIGNAL GROUND			

LOOPBACK CONNECTOR FOR SIO TEST:

PIN 1, 4, 6	SHORT
PIN 2, 3	SHORT
PIN 7, 8, 9	SHORT

8.13 SIO PORT TEST ERROR

AN ERROR OCCURS WHEN A MOUSE OR OTHER I/O DEVICE IS INSTALLED.



BOARD-LEVEL TROUBLESHOOTING FOR SIO TEST ERROR

CHECK THE FOLLOWING PARTS FOR COLD SOLDER OR ONE OF THE FOLLOWING PARTS ON THE MOTHER-BOARD MAY BE DEFECTIVE, USE AN OSCILLOSCOPE TO CHECK THE FOLLOWING SIGNAL OR REPLACE THE PARTS ONE AT A TIME AND TEST AFTER EACH REPLACEMENT.

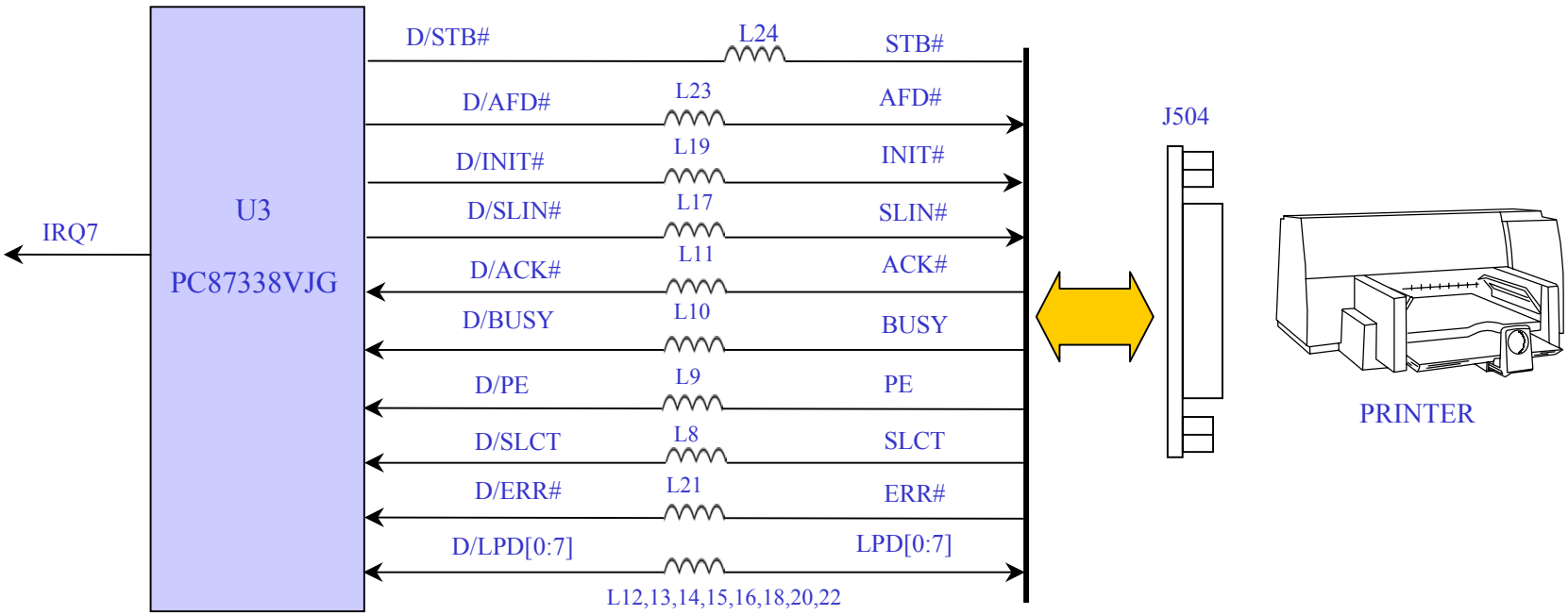
PARTS:
U3,U8
U501
R2,R504
R503,D8
D15
C6~C13
J503

SIGNALS:

IRQ4	COM1DSR#	ATXD
IO_OFF#	COM1RI#	ARXD
COM1RTS#	ARTS	
COMETXD	ADTR	
COM1DTR#	ADSR	
COM1CTS#	ACTS	
COM1RXD	ARI	
COM1DCD#	ADCD	

8.14 PIO PORT TEST ERROR

WHEN A PRINT COMMAND IS ISSUED, PRINTER PRINTS NOTHING OR GARBAGE.



PIN DEFINITION OF PIO PORT

PIN 1	STB	STROBE SIGNAL	PIN 14	AFD	AUTO LINE FEED
PIN 2-9	D0-D7	PARALLEL PORT DATA BUS D0 TO D7	PIN 15	ERR	ERROR AT PRINTER
PIN 10	ACK	ACKNOWLEDGE HANDSHANK	PIN 16	INIT	INITIATE OUTPUT
PIN 11	BUSY	BUSY SIGNAL	PIN 17	SLIN	PRINTER SELECT
PIN 12	PE	PAPER END	PIN 18-25:		SIGNAL GROUND
PIN 13	SLCT	PRINTER SELECTED			

LOOPBACK CONNECTOR FOR PIO TEST:

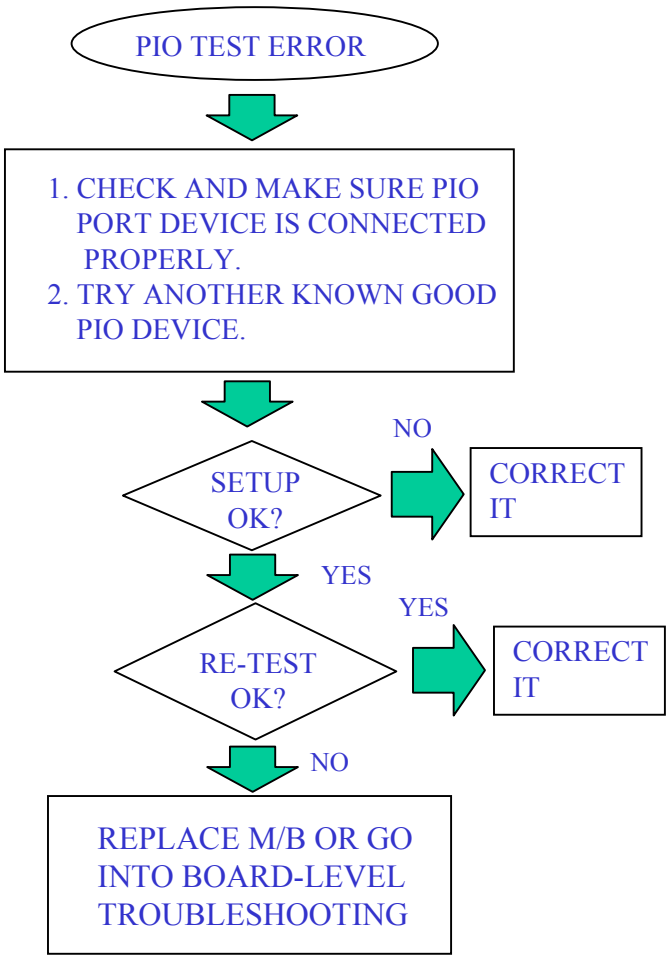
PIN 1,13	SHORT	PIN 10,16	SHORT
PIN 2,15	SHORT	PIN 11,17	SHORT
PIN 12,14	SHORT		

LOOPBACK CONNECTOR FOR EPP TEST:

PIN 1,2,4,6,8	SHORT
PIN 3,5,7,9,16	SHORT
PIN 18,19,20,21,22,23,24,25	SHORT

8.14 PIO PORT TEST ERROR

WHEN A PRINT COMMAND IS ISSUED, PRINTER PRINTS NOTHING OR GARBAGE.



BOARD-LEVEL TROUBLESHOOTING FOR PIO TEST ERROR

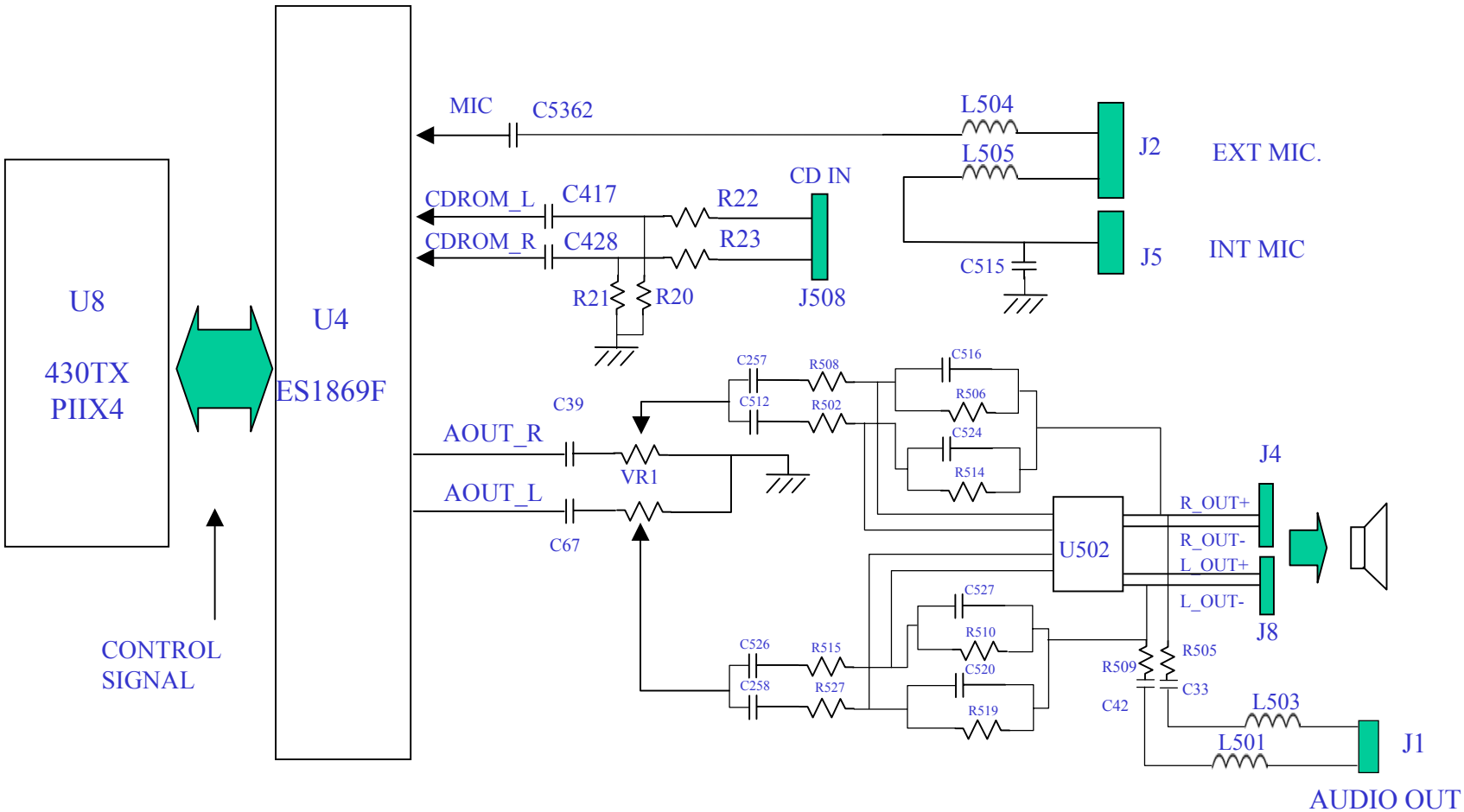
CHECK THE FOLLOWING PARTS FOR COLD SOLDER OR ONE OF THE FOLLOWING PARTS ON THE MOTHER-BOARD MAY BE DEFECTIVE, USE AN OSCILLOSCOPE TO CHECK THE FOLLOWING SIGNAL OR REPLACE THE PARTS ONE AT A TIME AND TEST AFTER EACH REPLACEMENT.

PARTS:
U3
U8
L8~L24
J504

SIGNALS:
STB#
AFD#
INIT#
SLIN#
ACK#
BUSY
PE
SLCT
ERR#
LPD[0:7]
IRQ7

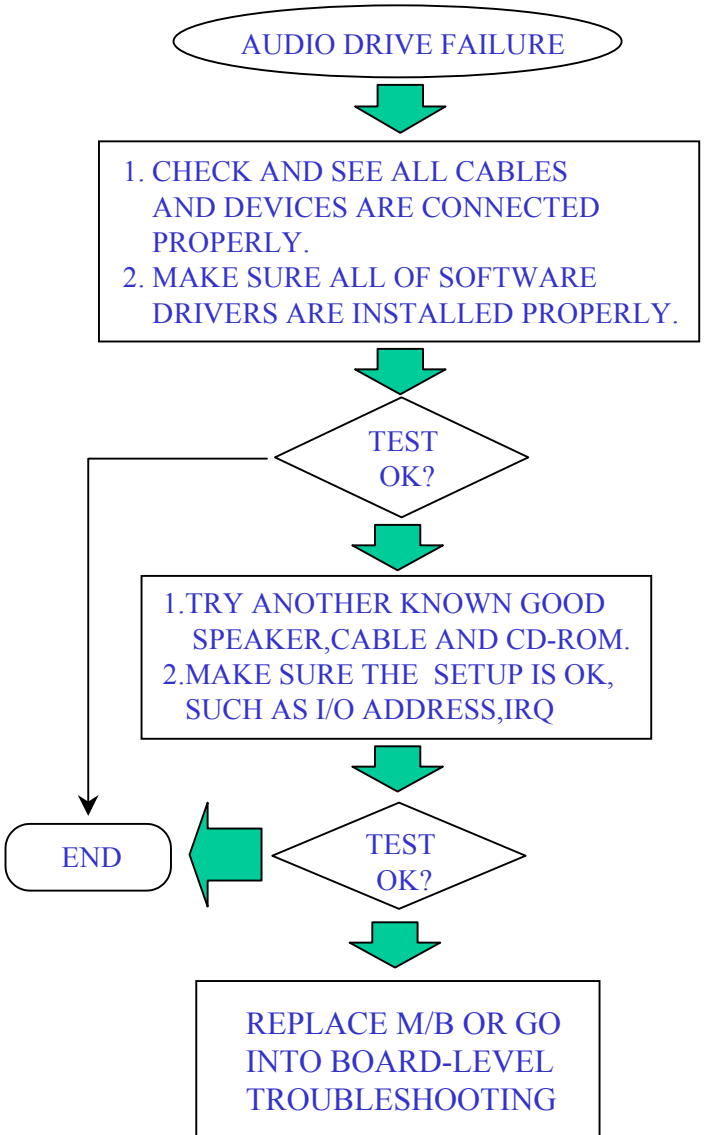
8.15 AUDIO FAILURE

NO SOUND FROM SPEAKER AFTER AUDIO DRIVER IS INSTALLED.



8.15 AUDIO FAILURE

NO SOUND FROM SPEAKER AFTER AUDIO DRIVER IS INSTALLED.



BOARD-LEVEL TROUBLESHOOTING FOR AUDIO TEST ERROR

CHECK THE FOLLOWING PARTS FOR COLD SOLDER OR ONE OF THE FOLLOWING PARTS ON THE MOTHERBOARD MAY BE DEFECTIVE, USE AN OSCILLOSCOPE TO CHECK THE FOLLOWING SIGNAL OR REPLACE THE PARTS ONE AT A TIME AND TEST AFTER EACH REPLACEMENT.

1.IF NO SOUND CAUSE OF LINE OUT, CHECK THE FOLLOWING PARTS & SIGNALS:

PARTS:	SIGNALS:
C39,C67	AOUT_L
VR1,U502	AOUT_R
L3,L501	
L503	
R509,R505	
C42,C33	
...	

2.IF NO SOUND CAUSE OF MIC, CHECK THE FOLLOWING PARTS & SIGNALS:

PARTS:	SIGNALS:
J2	MIC
J5	
L505,L513	
L504,L2	
C515,C5326	
R501,R513	
R521,U4	

3.IF NO SOUND CAUSE OF CD-ROM, CHECK THE FOLLOWING PARTS & SIGNALS:

PARTS:	SIGNALS:
J508	CDROM_L
R20,r22	CDROM_R
R21,r23	
C1022	
C1032	
U4	

9. SPARE PARTS LIST-1

***** PC;5033L/TL-F11-M/EN-1A/1M Spare Parts List *****

PART_NO	DESCRIPTION	LOCATION
526266550002	PC;5033L/TL-F11-M/EN-1A/1M	
324180586060	IC;CPU,P55C,133MHZ,2.45V,PPGA	
412665500001	PCB ASSY;MDM,33.6K,SOFT,FCC,5033	
416266550002	NB PLATFORM;TFT,GSTAR,12.1,5033,	
431665500001	CASE KIT;5033,US	
411665500003	PWA;PWA-5033 MOTHER BD,US	
242600000001	LABEL;PAL,20*5MM,COMMON	
242600000145	LABEL;10*10,BLANK,COMMON	
242600000158	LABEL;10*10,BLANK,COMMON,HI-TEMP	
242600000169	LABEL;BLANK,23.8*5MM,COMMON	
242600000170	LABEL;PCMCIA CARD WORKS/95 EN	
242600000195	LABEL;PENTIUM-BP,SYSTEMSOFT BIOS	
242901300011	LABEL;BAR CODE,IB,BBU	
341665400004	SHIELDING;PCMCIA,VENUS	
341665400005	SPRING;DC JACK,VENUS	
341665400006	SHIELD;AUDIO,VENUS	
344600000214	IC CARD CON PART;156P,REV,ST,HIR	
346665400015	INSULATOR;PCMCIA,VENUS	
346665400023	INSULATOR;M/BD,VENUS	
346665400025	INSULATOR;SW BD CON.,VENUS	
371102011501	SCREW;M2L15,FLT(+),NIW	
411665500004	PWA;PWA-5033 T/U V1 MOTHER BD,US	
312271006152	EC;100U ,10V,M,RA,D6.3*9.8,OS-CO	PC505
312271006350	EC;100U ,25V,20%,RA,6.3*7,-40~10	PC503,504,511,501
312272206152	EC;220U ,4V ,M,RA,D8*5,OS-CON	C569
312273306151	EC;330U ,6.3V,20%,RA,D10,W/OS-CO	PC502,PC517
313000020078	CHOKE COIL;15UH,D.7*16T/.2*32,55	PT502
313000020110	CHOKE COIL;8uH,12.5TS,D0.8,55130	PL501
313000020114	CHOKE COIL;15uH,16.5TS,D0.8,5513	PL503
313000020127	CHOKE COIL;30uH,23.5T,55130,TUBE	PL502
331000005001	CON;BATTERY,5P,5MM,SPRING,5010S0	J510

PART_NO	DESCRIPTION	LOCATION
331650029606	IC SOCKET;296P,ZIF,ZIFPGAFC	U503
331720009004	CON;D,MA,9P,2.775,R/A	J503
331720015006	CON;D,FM,15P,2.29,R/A,3ROW	J502
331720025005	CON;D,FM,25P,2.775,R/A	J504
331840005002	CON;STEREO JACK,5P,R/A,D3.6,2 SW	J2,1
331870006008	CON;DIN,SKT,6P,MINI,R/A,W/SHIELD	J501
331910003003	CON;POWER JACK,3P,16VDC/3A	PJ501
337030105013	SW;TOGGLE,SPST,5V/1mA	SW1
337120124001	SW;DIP,SPST,2P,25VDC,24MA,HDK632	SW501
346665200036	INSULATOR;D/D CHOKE,PITCHING3	PL503
411665500005	PWA;PWA-5033 SMT V1 MOTHER BD,US	
271002000301	RES;0 ,1/10W,5% ,0805,SMT	L546,JP3,JP501
271002100301	RES;10 ,1/10W,5% ,0805,SMT	PR29
271002472301	RES;4.7K ,1/10W,5% ,0805,SMT	PR1,21
271012202301	RES;2K ,1/8W,5% ,1206,SMT	R141
271012561301	RES;560 ,1/8W,5% ,1206,SMT	R140
271013100301	RES;10 ,1/4W,5% ,1206,SMT	R144,145,146
271045107101	RES;.01 ,1W ,1% ,2512,SMT	PR2,18
271045207101	RES;.02 ,1W ,1% ,2512,SMT	PR501
271045257101	RES;.025 ,1W ,1% ,2512,SMT	PR3
271071000002	RES;0 ,1/16W,0603,SMT	R2,R25,R12
271071100302	RES;10 ,1/16W,5% ,0603,SMT	R59,74,R62,R63
271071101301	RES;100 ,1/16W,5% ,0603,SMT	R40,93,548,557
271071102302	RES;1K ,1/16W,5% ,0603,SMT	R1,32,33,121,124
271071103302	RES;10K ,1/16W,5% ,0603,SMT	PR6,PR10,
271071104101	RES;100K ,1/16W,1% ,0603,SMT	PR4,7,16,28,37,
271071104302	RES;100K ,1/16W,5% ,0603,SMT	R3,PR11,PR24,R45
271071105101	RES;1M ,1/16W,1% ,0603,SMT	R73,PR41
271071105301	RES;1M ,1/16W,5% ,0603,SMT	PR23,R87,R89,R102
271071111101	RES;110 ,1/16W,1% ,0603,SMT	R27
271071121211	RES;12.1K,1/16W,1% ,0603,SMT	PR43

9. SPARE PARTS LIST-2

PART_NO	DESCRIPTION	LOCATION
271071124311	RES;124K ,1/16W,1% ,0603,SMT	PR5,PR9,R66
271071137311	RES;137K ,1/16W,1% ,0603,SMT	PR14
271071153301	RES;15K ,1/16W,5% ,0603,SMT	R35,36,525,526,
271071203101	RES;20K ,1/16W,1% ,0603,SMT	R135
271071203302	RES;20K ,1/16W,5% ,0603,SMT	R514,510
271071204101	RES;200K ,1/16W,1% ,0603,SMT	PR513,27
271071221302	RES;22 ,1/16W,5% ,0603,SMT	R60,61,77,79-82
271071222302	RES;2.2K ,1/16W,5% ,0603,SMT	R53,57,537
271071224301	RES;220K ,1/16W,5% ,0603,SMT	R46,113,123,520,559
271071226311	RES;226K ,1/16W,1% ,0603,SMT	PR22
271071249311	RES;249K ,1/16W,1% ,0603,SMT	R70
271071255311	RES;255K ,1/16W,1% ,0603,SMT	PR13
271071270301	RES;27 ,1/16W,5% ,0603,SMT	R41,42
271071274311	RES;274K ,1/16W,1% ,0603,SMT	PR36
271071301311	RES;301K ,1/16W,1% ,0603,SMT	R574,PR507
271071309211	RES;30.9K,1/16W,1% ,0603,SMT	R52
271071330302	RES;33 ,1/16W,5% ,0603,SMT	R24,58,71,76
271071332302	RES;3.3K ,1/16W,5% ,0603,SMT	R28
271071332311	RES;332K ,1/16W,1% ,0603,SMT	PR20
271071333301	RES;33K ,1/16W,5% ,0603,SMT	PR17
271071392311	RES;392K ,1/16W,1% ,0603,SMT	PR26
271071412311	RES;412K ,1/16W,1% ,0603,SMT	PR35
271071470301	RES;47 ,1/16W,5% ,0603,SMT	R524,523
271071471302	RES;470 ,1/16W,5% ,0603,SMT	R139,558
271071472302	RES;4.7K ,1/16W,5% ,0603,SMT	R13,14,95,544
271071473301	RES;47K ,1/16W,5% ,0603,SMT	R50,97,104,111,565
271071474301	RES;470K ,1/16W,5% ,0603,SMT	PR30,R31,R47,R122
271071499111	RES;4.99K,1/16W,1% ,0603,SMT	R130
271071499211	RES;49.9K,1/16W,1% ,0603,SMT	PR19
271071499311	RES;499K ,1/16W,1% ,0603,SMT	R69
271071562301	RES;5.6K ,1/16W,5% ,0603,SMT	R554,563

PART_NO	DESCRIPTION	LOCATION
271071562311	RES;562K ,1/16W,1% ,0603,SMT	PR42
271071564301	RES;560K ,1/16W,5% ,0603,SMT	R11
271071619211	RES;61.9K,1/16W,1% ,0603,SMT	R67
271071681301	RES;680 ,1/16W,5% ,0603,SMT	R4-9
271071682101	RES;6.8K ,1/16W,1% ,0603,SMT	R22-23
271071750101	RES;75 ,1/16W,1% ,0603,SMT	R17-19
271071752101	RES;7.5K ,1/16W,1% ,0603,SMT	R513
271071787311	RES;787K ,1/16W,1% ,0603,SMT	PR25
271071976211	RES;97.6K,1/16W,1% ,0603,SMT	PR15,44
271611100301	RP;10*4 ,8P ,1/16W,5% ,0612,SMT	RP31,33-39
271611102301	RP;1K*4 ,8P ,1/16W,5% ,0612,SMT	RP15
271611103301	RP;10K*4 ,8P ,1/16W,5% ,0612,SMT	RP10,21,23,26,27
271611104301	RP;100K*4,8P ,1/16W,5% ,0612,SMT	RP44,11
271611220301	RP;22*4 ,8P ,1/16W,5% ,0612,SMT	RP45
271611330301	RP;33*4 ,8P ,1/16W,5% ,0612,SMT	RP3-8,20,25
271611472301	RP;4.7K*4,8P ,1/16W,5% ,0612,SMT	RP2
271611822301	RP;8.2K*4,8P ,1/16W,5% ,0612,SMT	RP9
271621102303	RP;1K*8 ,10P,1/16W,5% ,1206,SMT	RP1
271621103303	RP;10K*8 ,10P,1/16W,5% ,1206,SMT	RP12-14,19,
271621472303	RP;4.7K*8,10P,1/16W,5% ,1206,SMT	RP18,22,40,41
271911103901	VR;10K ,.05W,20%,XV0102GPH1N-93	VR1
272002105701	CAP;1U ,CR,16V ,-20+80%,0805,SM	PC15,24,C40,47
272012105702	CAP;1U ,CR,16V ,+80-20%,1206,Y	PC3
272012225702	CAP;2.2U ,CR,16V ,+80-20%,1206,Y	C39,67,192,210
272012475701	CAP;4.7U ,CR,16V ,+80-20%,1206,Y	C78,189,544,546
272015474501	CAP;.47U ,CR,50V,20%,1206,Z5U	C260,C261
272021106501	CAP;10U ,10V ,20%,1210,X7R,SMT	PC7
272022106701	CAP;10U ,16V,+80-20%,1210,Y5V,S	PC23,507,516,C259
272041226501	CAP;22U ,CR,10V ,20%,1812,X7R,S	PC5,21
272043106501	CAP;10U ,CR,25V ,20%,1812,Y5U,S	PC512
272072104702	CAP;.1U ,16V,+80-20%,0603,SMT	PC2,4,9,10

9. SPARE PARTS LIST-3

PART_NO	DESCRIPTION	LOCATION
272072221301	CAP;220P ,16V,5% ,-30+85'C,0603,	C269
272072224701	CAP;.22U ,16V ,+80-20%,0603,Y5V,	C98,99,102,103,536
272072473701	CAP;.047U,16V ,+80-20%,0603,Y5V,	C100,512,526
272073180401	CAP;18P ,CR,25V ,10%,0603,NPO,S	C206,207,533,
272075100701	CAP;10P ,50V ,+80-20%,0603,SMT	C116,151-154,193
272075101701	CAP;100P ,50V ,+80-20%,0603,SMT	C3,4,6-13,32,79
272075102701	CAP;1000P,50V ,+80-20%,0603,SMT	C1,PC12,C36,C38
272075103702	CAP;.01U ,50V,+80-20%,0603,SMT	PC18,20,C73,114
272075104701	CAP;.1U ,50V,+80-20%,0603,SMT	PC8,11,13,22,510
272075121401	CAP;120P ,CR,50V ,10%,0603,NPO,S	C503,502
272075181301	CAP;180P ,50V ,5% ,0603,SMT	C14-30
272075222701	CAP;2200P,50V ,+80-20%,0603,SMT	C271
272075331701	CAP;330P ,50V, +80-20%,0603,SMT	C212
272075470701	CAP;47P ,50V ,+80-20%,0603,SMT	C34,35,104-106
272075471401	CAP;470P ,50V,10%,0603,SMT	C563,524,527
272075472701	CAP;4700P,50V ,+80-20%,0603,SMT	PC515
272075561701	CAP;560P ,CR,50V ,+80-20%,0603,S	C113,117,520,516
272075681401	CAP;680P ,50V ,10%,0603,NPO,SMT	C75,76
272601227501	EC;220U ,10V,M,6.3*7.7,-15+105',	C2
272601476501	EC;47U ,6.3V,M,5*5.5,-40+85',SM	C66,511
272602107501	EC;100U,16V,M,6.3*5.5,-55+85'C,S	C31,5,33,42
273000010003	FERRITE CHIP;36OHM/100MHZ,4332	PL1-4
273000053228	INDUCTOR;2.2UH,5%,3225,SMT	L27,544
273000130001	FERRITE CHIP;120OHM/100MHZ,1608,	L5,6,506-510,44
273000130003	FERRITE CHIP;40OHM/100MHZ,1608,S	L40,41
273000130006	FERRITE CHIP;600OHM/100MHZ,.2A,1	L2,8-24,501-505
273000130010	FERRITE CHIP;130OHM/100MHZ,1608,	L515-541,33
273000150002	FERRIET CHIP;120OHM/100MHZ,2012,	L3,28-30,543
273000150009	FERRITE CHIP;30OHM/100MHZ,2012,S	L7,25,26,31,514
273000250005	FERRITE CHIP;160OHM/100MHZ,6A,45	L548
273000500006	CHOKE COIL;7UH,7TS,T6*4*2,VENUS,	PT501

PART_NO	DESCRIPTION	LOCATION
273000610004	FERRITE ARREY;120OHM/100MHZ,M TY	FA1,2,3
274011431406	XTAL;14.318MHZ,30PPM,32PF,H2.5,S	X1,X3
274011600405	XTAL;16MHZ,30PPM,16PF,SMT	X501
274013276103	XTAL;32.768KHZ,30PPM,12.5PF,CM20	X2
282074338401	IC;74CBT3384DBQ,Q SWITCH,QSOP,24	U9
282574074004	IC;74AHC74,DUAL D F/F,TSSOP,14P	U21
282574123003	IC;74VHC123,RETRI. M/RESET,SSOP,	U510
282574373004	IC;74AHC373,OCT D-TRAN,TSSOP,20P	U6
283603000002	IC;SRAM,32K*32,8NS,TQFP,100P	U1,7
283605003011	IC;SRAM,32K*8,12NS,SOJ,28P,PURE,	U22
283766540002	IC;DRAM,4M*16-60,EDO,TSOP,50P,VE	U507,U509,U512,U513
283766540005	IC;DRAM,256K*16-60,EDO,SOJ40,VEN	U11,15,23,25
284100430001	IC;FW82439TX,MTXC,CPU/PCI,BGA,32	U18
284100430002	IC;FW82371AB,PIIX4,PCI/ISA,BGA,3	U8
284500045001	IC;LM45B,TEMPERATURE SENSORS,SOT	U504
284501869001	IC;ES1869F,AUDIO DRIVE,PQFP,100P	U4
284506701002	IC;OZ6701-G-CL,PC CARD COMPAN.,S	U20
284506832004	IC;OZ6832TC2,PCI/CARDBUS,TQFP,20	U508
284509385004	IC;CYBER9385,VGA CTRL,TQFP,256P	U5
284580051001	IC;80C51SL-BG,KBD CTLR,PQFP,100P	U505
284587338002	IC;PC87338VJG,SUPER I/O,TQFP,100	U3
286100102001	IC;TPA0102,AUDIO AMP,1.5W,TSSOP,	U502
286100393002	IC;LM393A,DUAL,COMPARTOR,SO,8P	PU5,501
286200213001	IC;MAX213,RS-232,SSOP,28P	U501
286300055001	IC;TC55,3.3V,250mA,REG.,SOT89	U13
286300431004	IC;AIC431,.5%,ADJ SHUNT REG,SOT-	PQ12
286300745001	IC;MAX745EAP,PWM CTRL,SSOP,20P	PU3
286300786001	IC;MAX786CAI,PWM CTLR,DUAL,SSOP,	PU2
286300798001	IC;MAX798ESE,PWM CTLR,SO,16P	PU4
286300809002	IC;MAX809,RESET CIRCUIT,2.9V,SOT	U16
286302206001	IC;TPS2206,CARDBUS PWR CTLR,SSOP	U27

9. SPARE PARTS LIST-4

PART_NO	DESCRIPTION	LOCATION
286302951015	IC;LP2951ACM,VOLTAGE REGULATOR,S	U28
286305200001	IC;MIC5200-5BS,VOL REG,SOT-223	U14
286317812001	IC;HA178L12UA,VOLT REGULATOR,SC-	PU1
286505265001	IC;PLL52C65-02,CLOCK GEN.,SSOP,4	U10
288001100001	FIR;HSDL-1100,TRANSCEIVER,X07,SM	U511
288100018002	DIODE;RLZ18B,ZENER,18V,LL34,SMT	PD5
288100024002	DIODE;RLZ24D,ZENER,23.63V,5%,SMT	PD509
288100032013	DIODE;BAS32L,VRRM75V,MELF,SOD-80	PD4,504,506,508
288100056001	DIODE;RLZ5.6B,ZENER,5.6V,5%,LL34	PD502
288100056003	DIODE;BAW56,70V,215MA,SOT-23	D13,11
288100202001	DIODE;DAN202K,80V,SWITCH,SMT	PD3,D16
288101004024	DIODE;EC10QS04,RECT,40V,1A,CHIP,	PD1,501,503,505
288104148001	DIODE;RLS4148,200MA,500MW,MELF,S	D1,8,9,10,12
288106004001	DIODE;EA60Q04-F,RECT,40V,80W,SMT	PD6,2
288200144001	TRANS;DTC144WK,NPN,SMT	PQ9,
288200352001	TRANS;NDS352P,DMOS,TO-236AB	Q3,13
288203105001	TRANS;TM3105,N-MOSFET,SOP-8	PQ1,2,7,8
288203904010	TRANS;MMBT3904L,NPN,Tr35NS,TO236	Q8,505,507,508,PQ13
288203906018	TRANS;MMBT3906L,PNP,Tr35NS,TO236	Q504
288204410001	TRANS;SI4410DY,N-MOSFET,.02OHM,S	PQ3,6
288204435001	TRANS;SI4435DY,P-MOSFET,.035OHM,	PQ501
288209410001	TRANS;SI9410DY,N-MOSFET,.04OHM,S	Q502
288227002001	TRANS;2N7002LT1,N-CHANNEL FET	Q6,PQ10,11,Q501,506
291000011001	CON;HDR,MA,10P*1,1.25,ST,SMT	J7
291000014003	CON;HDR,MA,20P*2,1.25MM,ST,SMT	J6
291000014802	CON;HDR,MA,24P*2,1.27,ST,H3.58,S	J12
291000014803	CON;HDR,MA,24P*2,1.27,ST,H1.5,SM	J508
291000015008	CON;HDR,MA/FM,25P*2,.8,ST,SPEEDT	J506
291000020404	CON;HDR,SHROUD,4P*1,2,R/A,USB,BE	J3
291000152401	CON;FPC/FFC,24P,1MM,R/A,ELCO	J10
291000152602	CON;FPC/FFC,26P,1MM,R/A,SMT	J11

PART_NO	DESCRIPTION	LOCATION
291000251564	CON;IC CARD,78P*2,FM,.6MM,SMT,VE	J507
291000410201	CON;WFR,MA,2P,1.25,ST,SMT/MB	J4,8,13
291000410301	CON;WFR,MA,3P,1.25,ST,SMT/MB	J5
291000610032	IC SOCKET;32P,PLCC,TIN,W/O PEGS,	U506
291000621445	DIMM SOCKET;144P,.8MM,GOLD,SMT	J509
294011200001	LED;GRN,H1.5,0805,PG1102W,SMT	D2-7
295000010008	FUSE;1.1A,POLY SWITCH,SMT	F1,501
295000010016	FUSE;NORMAL,6.5A/32VDC,3216,SMT	PF1,F502
295000010105	FUSE;1A,NORMAL,1206,SMT	F2
297120101005	SW;DIP,SPST,8P,50VDC,.1A,SMT,DHS	SW504,SW506
316665400001	PCB;PWA-VENUS/M BD	R03
481665500001	F/W ASSY;SYS/VGA BIOS,US,5033	
242600000158	LABEL;10*10,BLANK,COMMON,HI-TEMP	
283420402005	IC;FLASH,256K*8-12,PLCC-32,PL540	
481665500003	F/W ASSY;KBD CTRL,5033	
451665500051	HOUSING KIT;5033	
339111100002	SPEAKER ASSY;CASE KIT,VENUS	
340665400012	HDD BRKT ASSY;VENUS	
340665400014	COVER SHIELD ASSY;VENUS	
340665400015	BRKT ASSY;TOUCH PAD,VENUS	
340665400016	HOUSING SHIELD ASSY;VENUS	
340665400017	HEATSINK ASSY;VENUS	
340665500002	COVER ASSY;CASE KIT,5033	
340665500008	HOUSING ASSY;CASE KIT,5033	
340665500009	COVER ASSY;CPU,5033	
341665400007	HOLDER;TOUCH PAD,VENUS	
341665400010	FINGERS;I/O BRKT,VENUS	
341665400011	CONTACE;FAN,VENUS	
342665400001	BRKT;I/O,CASE KIT,ENTRY	
344665500015	COVER;L,HINGE,CASE KIT,5033	
344665500016	COVER;R,HINGE,CASE KIT,5033	

9. SPARE PARTS LIST-5

PART_NO	DESCRIPTION	LOCATION
344665500018	COVER;REAR,CASE KIT,5033	
344665500019	COVER;MODEM,HOUSING,CASE KIT,503	
344665500023	DOOR;PCMCIA,CASE KIT,5033	
344665500024	DOOR;I/O,CASE KIT,5033	
344665500025	BUTTON;TOUCH PAD,CASE KIT,5033	
344665500027	LEVER;I/O BRACKET,CASE KIT,5033	
345665400013	GASKET;USB,VENUS	
345665400025	GASKET;AUDIO,VENUS	
346665200005	THERMAL PAD;DOWN,CPU,PITCHING3	
346665400006	INSULATOR;T/P SWITCH BD,VENUS	
346665400009	INSULATOR;I/O PANEL,VENUS	
346665400016	INSULATOR;BATTERY,VENUS	
346665400019	THERMAL PAD;20*20*.5,VENUS	
370102010201	SPC-SCREW;M2L2,NIB,K-HD,727	
370102010402	SPC-SCREW;M2L4,NIW,K-HD(+),731	
370102010501	SPC-SCREW/W;M2L5,NIW,NYLOK	
370102610401	SPC-SCREW;M2.6L4,NIB,727,NLK	
370102610602	SPC-SCREW;M2.6 L6,NIB,K-HD,727	
370103010604	SPC-SCREW;M3L6,NIB,727,NYLOK	
371102010010	SCREW;M2L4,FLT(+),NIW	
371102010801	SCREW;M2L8,FLT(+),NIW	
371102610081	SCREW;M2.6L8,PAN(+),NIB	
371102610401	SCREW;M2.6L4,FLT(+),NIW	
411665400005	PWA;PWA-ENTRY T/P SW BD	
271071103302	RES;10K ,1/16W,5% ,0603,SMT	R1
272072104702	CAP;.1U ,16V,+80-20%,0603,SMT	C1,4
272075470701	CAP;47P ,50V ,+80-20%,0603,SMT	C2,3,5,6
273000130001	FERRITE CHIP;120OHM/100MHZ,1608,	L1,2,3
291000014801	CON;HDR,FM,24P*2,1.27,ST,SMT	J2
291000150804	CON;FPC/FFC,8P,1MM,R/A,2CONTAC,E	J1
297040101003	SW;PUSH BUTTON,SPST,.1A,30V,2P,S	SW1,2

PART_NO	DESCRIPTION	LOCATION
316665400003	PCB;PWA-VENUS/TOUCH PAD BD	R04
331040044003	CON;HDR,FM,22P*2,2MM,R/A,SUYIN	J3
338530010005	BATTERY;LI,3V/220MAH,CR2032	
298000000002	BATTERY HOLDER;FOR CR2032,BH-800	BT1
421665400006	FAN ASSY;CASE KIT,VENUS	
422665400002	FFC ASSY;TOUCH PAD,CASE KIT,VENU	
442110500005	TOUCH PAD MODULE;904236-0000,502	
451665400071	HDD ME KIT;ENTRY	
370103010401	SPC-SCREW;M3L4,K-HD(+),D5.2,NIW,	
370102610401	SPC-SCREW;M2.6L4,NIB,727,NLK	
340665400012	HDD BRKT ASSY;VENUS	
451665500031	CD ROM ME KIT;SR200S,5033	
340665500001	BEZEL ASSY;CD ROM,MITSUMI,20X,50	
342665500001	BRKT;CD-ROM,5033	
370102010201	SPC-SCREW;M2L2,NIB,K-HD,727	
421665400005	FPC ASSY;CD ROM,VENUS	
441665500002	LCD ASSY;TFT,LG,12.1",5033	
411665400004	PWA;PWA-ENTRY LED BD	
271071152302	RES;1.5K ,1/16W,5% ,0603,SMT	R4
271071681301	RES;680 ,1/16W,5% ,0603,SMT	R1,2,3
291000020601	CON;HDR,MA,6P*1,1.25MM,R/A,SMT	J1
294011200001	LED;GRN,H1.5,0805,PG1102W,SMT	D1,2,501,502
294011200006	LED;RE/GR,H1.5,L3,W2.5,BRPG1201W	D3,503
316665400004	PCB;PWA-VENUS/LED BD	R01
412219300005	PCB ASSY;D/A BD,ONLY L/G PANEL,5	
413000020078	LCD;LP121S1,TFT,12.1",SVGA	
421665400003	WIRE ASSY;BKLGHT,MB/INVRT/LED,VE	
421665500032	FPC ASSY;LG,12.1",TFT,5033	
421665500051	CABLE ASSY;MB/FPC,12.1",TFT,5033	
451665500002	LCD ME KIT;TFT,LG,12.1",5033	
242664800013	LABEL;CAUTION,INVERT BD,PITCHING	

9. SPARE PARTS LIST-6

PART_NO	DESCRIPTION	LOCATION
339115100001	MICROPHONE ASSY;LCD,VENUS	
340665400001	TILT UNIT;R,ENTRY	
340665400002	TILT UNIT;L,ENTRY	
340665500003	COVER ASSY;12.1",LCD,5033	
340665500004	HOUSING ASSY;LG,TFT,12.1",LCD,50	
345665200005	CUSHION;TOP,LCD,PITCHING3	
345665500001	CUSHION;LCD,5033	
345665500003	CUSHION;DOWN,LCD,5033	
346665500001	INSULATOR;INV./BD,5033	
370102010502	SPC-SCREW;M2 L5,NIB,K-HD,727	
370102610401	SPC-SCREW;M2.6L4,NIB,727,NLK	
371103010615	SPC-SCREW;M3L6,FLNG(+),NIW.NLK	
523411442506	CD ROM DRIVE;8-20X,SR200S	
523466540041	FDD ASSY;1.44M,3.5",ENTRY	
523411442008	FD DRIVE;1.44M,3 MODE,D353G	
422665400003	FFC ASSY;FDD,CONDUCTIVE TAPE,VEN	
345665400025	GASKET;AUDIO,VENUS	
343665400009	SHIELD;FDD,VENUS	
345665400024	SPONGE;FDD,PORON,L,VENUS	
441665500031	BATT ASSY;12V/3.5AH,NIMH,SANYO,5	
310131103004	CFM-BAT;NTCR,10K,SEMITEC,103AT-4	
335152000026	CFM-BAT;FUSE,THERMAL,NEC,SF91E	
335152000027	CFM-BAT;THERMAL BREAKER,TI,4MM75	
338712010010	BATTERY;NIMH,1.2V/3.5AH,4/3A,SAN	
442665500001	AC ADPT ASSY;5033	
451665500071	LABEL KIT;5033	
242665500003	LABEL;AGENCY-GLOBAL,CASE KIT,503	
343664710001	NAMEPLATE;LOGO,1,5026	
461665500001	PACKING KIT;5033	
221665520004	CARTON;PC,5033	
221665540003	BOX;INNER AK,5033	

PART_NO	DESCRIPTION	LOCATION
222663920008	PE BAG;150*200,FRU,LP486	
222664920001	PE BAG;340*475,T0.08,5027	
222665520003	PE BAG;80*200MM,5033	
227665500004	END CAP;N/B,5033	
227665500005	END CAP;TOP/BTM,AK,5033	
227665500006	END CAP;MIDDLE,AK,5033	
523415780002	HD DRIVE;1.6GB,2.5",M2724TAM	
531013890101	KBD;87,US,K950418A-4,5033	
541666550001	ACCESSORY KIT;EN,5033	
332810000033	PWR CORD;125V/7A,2P,BLACK,AMERIC	
561566550001	MANUAL;USER'S,EN,5033	
561566550002	MANUAL;QUICK,REF,EN,5033	
541666550010	ACCESSORY KIT;5033-UTILITY ONLY	
565166550003	S/W;1.44M,UTILITY,5033	
222600050108	ENVELOPE;3.5" FD,PVC,COMMON	
242661900008	LABEL;3.5",EN,ALL COMMON	
551103200013	FLOPPY DISKETTE;3.5",1.44MB,2HD	
565166550004	S/W;1.44M,AUDIO DRIVER,5033	
222600050108	ENVELOPE;3.5" FD,PVC,COMMON	
242661900008	LABEL;3.5",EN,ALL COMMON	
551103200013	FLOPPY DISKETTE;3.5",1.44MB,2HD	
565166490003	S/W;1.44M,VGA DRIVER,5027	
222600050108	ENVELOPE;3.5" FD,PVC,COMMON	
242661900008	LABEL;3.5",EN,ALL COMMON	
551103200013	FLOPPY DISKETTE;3.5",1.44MB,2HD	
565166510004	S/W;1.44M,PCMCIA DRIVER,5031/603	
222600050108	ENVELOPE;3.5" FD,PVC,COMMON	
242661900008	LABEL;3.5",EN,ALL COMMON	
551103200013	FLOPPY DISKETTE;3.5",1.44MB,2HD	