5031 M/B MAINTENANCE

5031 M/B MAINTENANCE

1. DEFINITION OF CONNECTORS & SWITCHS

J1 . POWER CONNECTOR

J2 . VGA CONNECT

J3 . RS232/SIO

J4 . PIO CONNECTOR

J6 . USB PORT CONNECTOR

J7 . DOCKINK STATION CONNECTOR

J8 . INTERNAL LEFT SPEAKER CONNECTOR

J9 . INTERNAL RIGHT SPEAKER CONNECTOR

J10.INTERNAL MICROPHONE CONNECTOR

J11.UPPER LED CARD CONNECTOR

J12.COVER SW CONNECTOR

J13.BACKLIGHT CONNECTOR

J14.LOWER LED CONNECTOR

J15.LVDS CARD CONNECTOR

J16.LEGACY LCD PANEL CONNECTOR

J18.INTERNAL KEYBOARD CONNECTOR

J19.TOUCHPADE CONNECTOR

J20,J21.144-PIN DIMM SOCKETS

J22.PCCARD CONNECTOR

J23.INTERNAL CAMERA CONNECTOR

J1000.D/D BOARD CONNECTOR

J1001.PS/2 KEYBOARD/MOUSE CONNECTOR

J1003,J1015.FDD/MO/HDD2 CONNECTORS

J1005.EXTERNAL MICROPHONE CONNECTOR

J1007.LINE-IN CONNECTOR

J1008.TV IN/OUT TRANSLATION CARD CONNECTOR

J1009.LINE-OUT CONNECTOR

J1010.LEFT BATTERY CONNECTOR

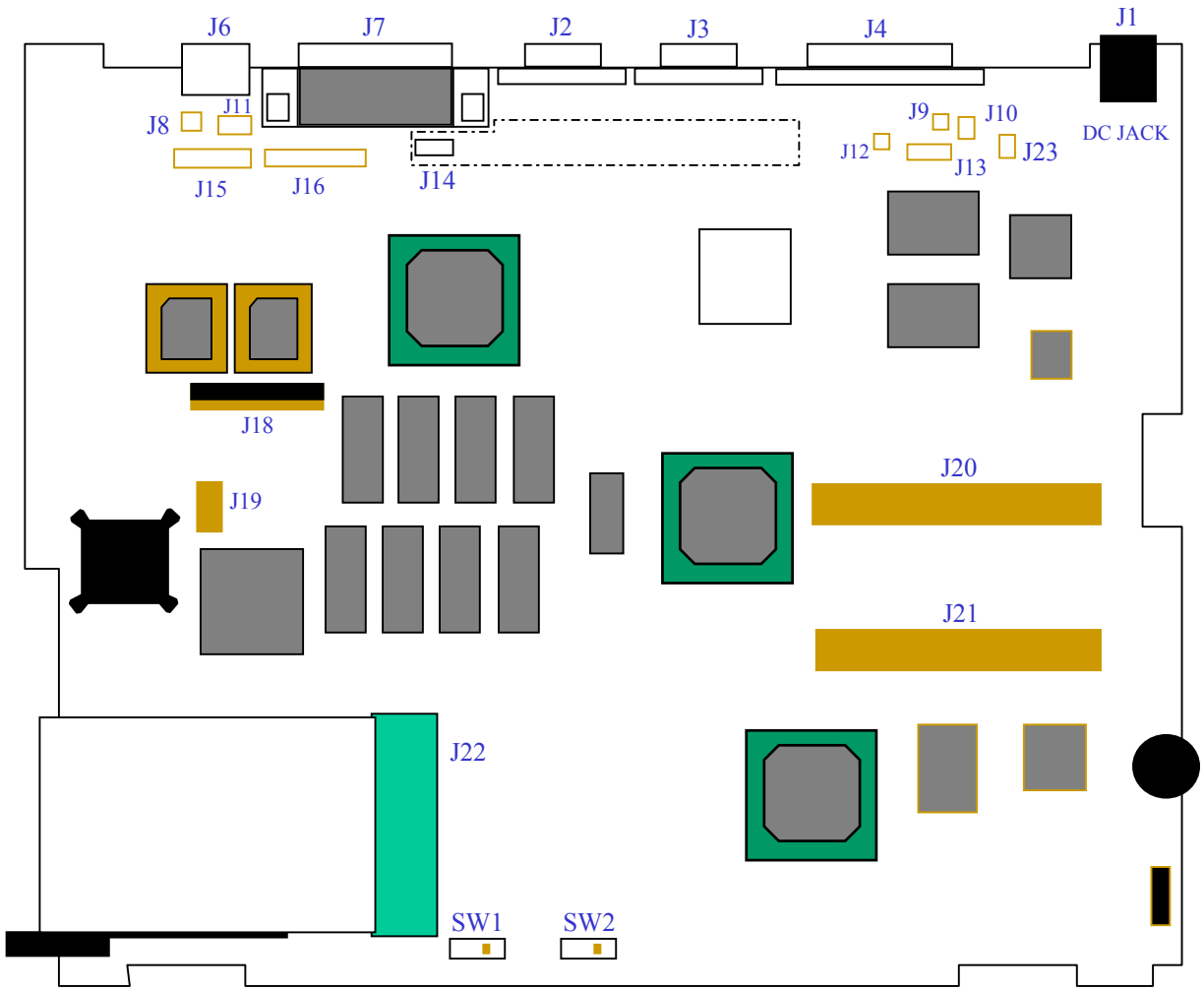
J1012.FAX/MODEM/VOICE CONNECTOR

J1013.RIGHT BATTERY CONNECTOR

J1016.PRIMARY HDD CONNECTOR

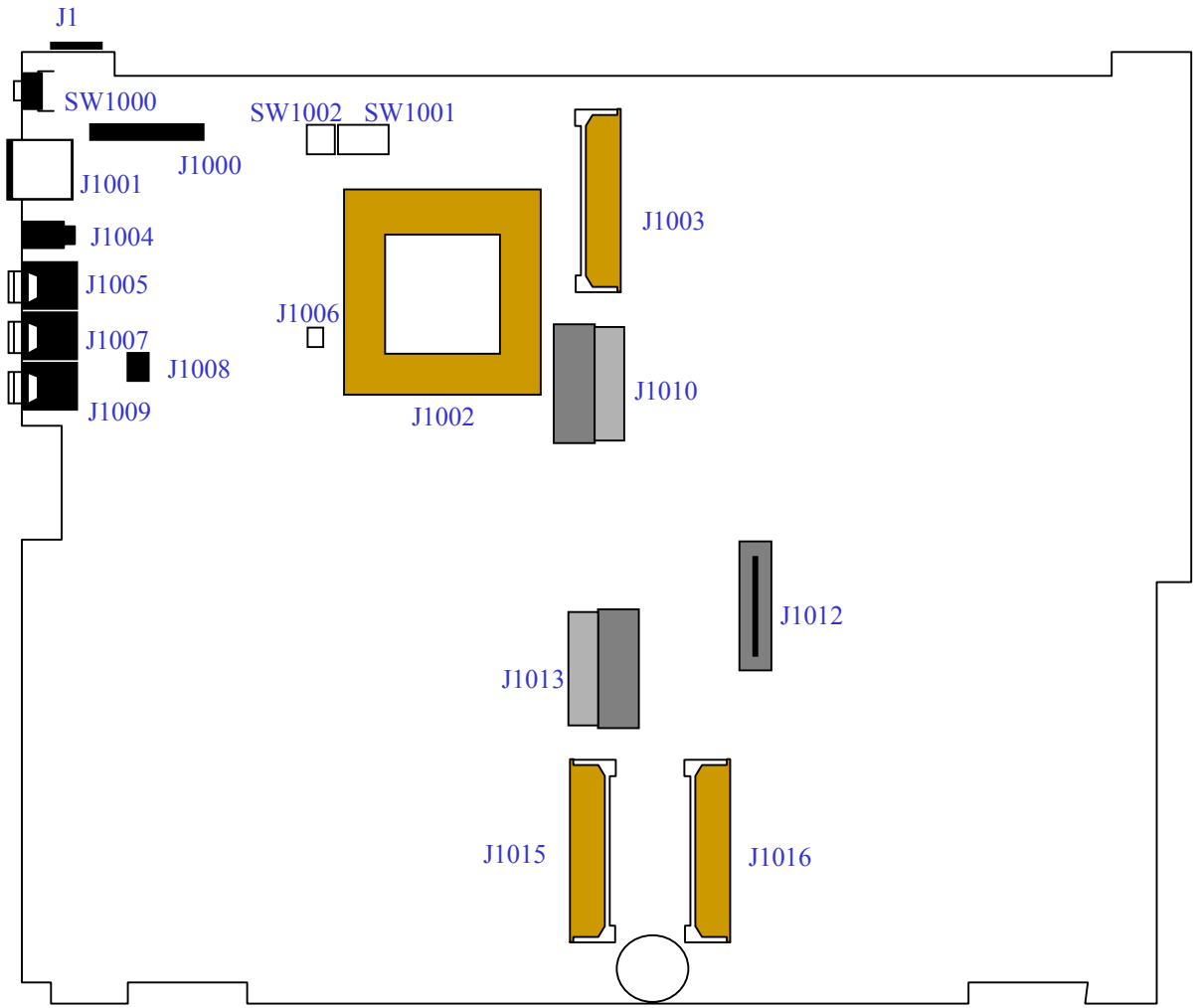
5031 M/B MAINTENANCE

2. LOCATION OF CONNECTORS & SWITCHES (A)



5031 M/B MAINTENANCE

2. LOCATION OF CONNECTORS & SWITCHES (B)



3. MAJOR COMPONENTS

1. U9 SUPER I/O CONTROLLER (PC87338VJG)

2. U10 LCD CRT & TV 64 BIT MUL-TIMEDIA FLAT PANEL CONTROLLER (CYBER9385/2)

3. U6,U13 512K L2 CACHE

4. U14 KEYBOARD BIOS (27C256)
5. U15 256K FLASH ROM (281020)
6. U20~U23,U33~U36 4MB VIDEO MEMORY (416C256)
7. U31 MTXC (82439TX)
8. U32 KEYBOARD CONTROLLER(80C51SL)

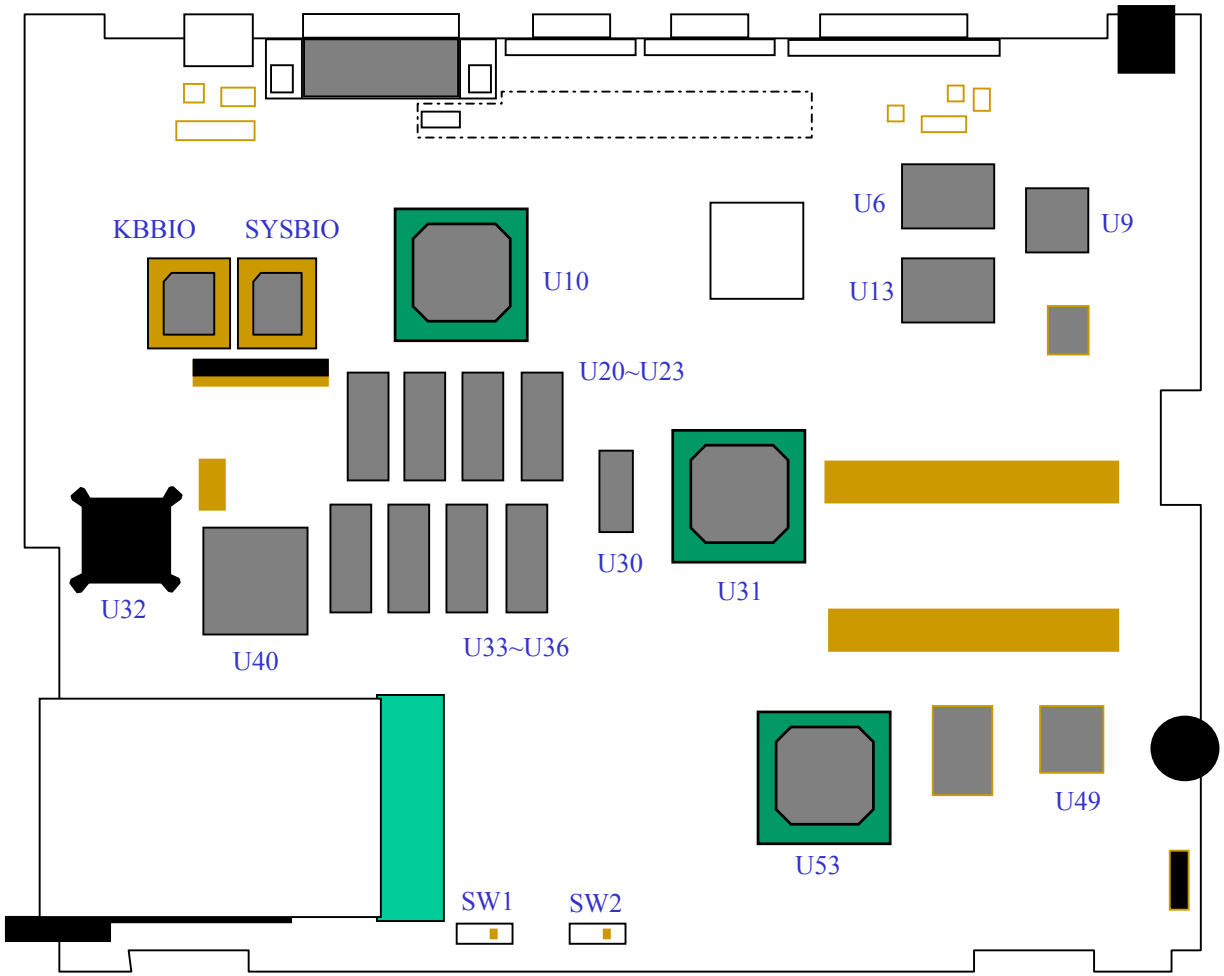
9. U38 CARDBUS CONTROLLER (OZ6832)

10. U45 CLOCK SYNTHESIZER(W48S67-02)

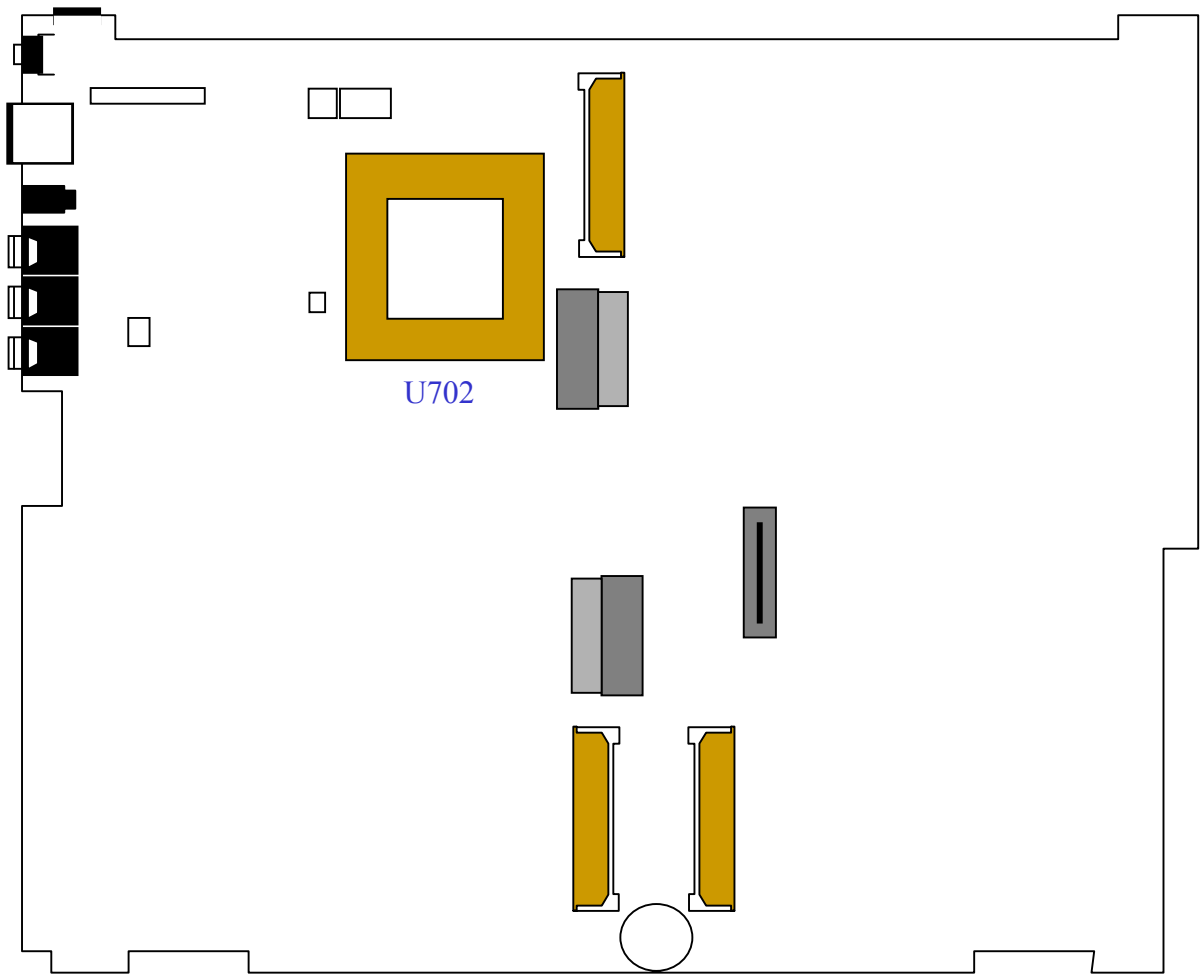
11. U49 AUDIO CONTROLLER (CS4237B)
12. U53 PIIX4 (82371AB)

13. U702 CPU (P55CLM ,TILLAMOOK, OR COMPATIBLE CPU)

4. LOCATION OF MAJOR COMPONENTS (A)



4. LOCATION OF MAJOR COMPONENTS (B)



5. PIN DESCRIPTIONS OF MAJOR COMPONENTS

5.1 PENTIUM MICROPROCESSOR (P54LM)-1

SYMBOL	TYPE	DESCRIPTION
A20M#	I	WHEN THE ADDRESS BIT 20 MASK PIN IS ACTIVE, THE 20 (A20) PENTIUNM MICORPROCESSOR MASKS PHYSICAL ADDRES BIT BEFORE PERFORMING A LOOKUP TO THE INTERNAL CACHE OR EMULATES THE ADDRESS WRAPAROUND AT THE AMB DRIVING A MEMORY BUS CYCLE ONTO THE BUSES. A20M# BOUNDARY THAT OCCUS ON THE 8086/8088.
A31:A5 A4:A3	I/O O	A31:A3 COMPRISE THR PENTIUME, ICROPROCESSOR'S ADDRES BUS.
ADS#	I/O	WHEN ACTIVE, THE ADDRESS STATUS OUTPUT INDICCATES THAT A VALID BUS CYCLE DEFINITION AND ADDRESS ARE AVAILABLE ON THE BUS CYCLE DEFINITION AND BUS LINES.
AHOLD	I	THE ADDRESS HOLD REQUEST INPUT ALLOWS ANOTHER BUS MASTER ACCESS TO PENTIUM MICROPROCESSOR'S ADDRESS BUS FOR A CACHE INVALIDATION, BACK INVALIDATION, OR INQUIRE CYCLE.
AP	I/O	THE PENTIUM PROCESS GENERATES ADDRESS PARITY DURING MEMORY WRITE OPERATIONS AND CHECK ADDRESS PARITY DURING CACHE INVALIDATION CYCLES (ADDRESS BUS SNOOPING).
APCHK#	O	THE PENTIUM PROCESS ASSERTS THE ADDRES PARITY CHECK OUTPUT WHEN AN ADDRES BUS PARITY ERROD IS DETECTED APCHK# IS ASSERTED 2 CLOCK CYCLES AFTER EADS# IS SAMPLE ACTIVE. APCHK$ REMAIN ACTIVE FOR ON CLOCK CYCLE.
[APICHEN] OR PICD1	I/O	APIC ENABLE.
BE0#	O	BYTE ENABLE, PATH0 (D7:D0).
BE1#	O	BYTE ENABLE, PATH1 (D15:D8).
BE2#	O	BYTE ENABLE, PATH 2 (D23:D16).
BE3#	O	BYTE ENABLE, PATH3 (D31:D24).
BE4#	O	BYTE ENABLE, PATH4 (D39:D32).
BE5#	O	BYTE ENABLE, PATH5 (D47:D40).
BE6#	O	BYTE ENABLE, PATH6 (D55:D48).
BE7#	O	BYTE ENABLE, PATH7 (D63:D56).

SYMBOL	TYPE	DESCRIPTION
BF	I	THE BUS FREQUENCY SIGNAL (BF) DETERMINES THE I/O BUS TO PROCESSOR CORE FREQUENCY RATIO.
BOFF#	I	ENSURE THAT THE PROCESSOR DOESN'T FETCH STALE DATA FROM MAIN MEMORY.
BP3:2	O	THE BREAK POINT OUTPUTS INDICATE THAT A BREAKPOINT MATCH HAS BEEN DETECTED THROUGH THE BRESKPOINT REGISTER.
BP/PM1:0	O	BREAKPOINT AND PERFORMANCE MONITORING PINS.
BRDY#	I	THE BURS READY INPUT INDICATES THAT THE CURRENTLY ADDRESSED DEVICE HAS PRESENTED VALID DATA ON THE DATA BUS PINS IN RESPONSE TO A READ OR THAT CURRENTLY ADDRESSED DEVICE HAS ACCEPTED DATA FROM THE PENTIUM CPU IN RESPONSE TO A WRITE.
BRDCY#	I	THE BURS READY INPUT INDICATES THAT THE LEVEL 2 CACHE HAS PRESENTED VALID DATA ON THE DATA BUS PINS IN RESPONSE TO A READ OR THAT THE LEVEL 2 CACHE HAS ACCEPTED DATA FROM THE PENTIUM CPU IN RESPONSE TO A WRITE.
BREQ#	O	THE INTERNAL CYCLE PENDING OUTPUT INDICATES THAT THE PENTIUM MICROPROCESSOR HAS A BUS CYCLE REQUEST PENDING.
BT3:BT0	NA	BRANCH TRACE LINES ARE DRIVEN DURING A BRANCH TRACE SPECIAL CYCLE.
BUSCHK#	I	THE BUS CHECK ALLOWS SYSTEM DESIGNERS TO NOTIFY THE CPU. IF A BUS CYCLE HAS NOT COMPLETED SUCCESSFULLY.
CACHE#	I/O	CACHE# SIGNAL IS ACTIVE WHEN INFORMATION IS BEGIN TRANSFREED BETWEEN EXTERNAL MEMORY AND AN INTERNAL CACHE.
CLK	I	CLOCK PROVIDES THE FUNDAMNTAL TIMING AND THE INTERNAL OPERATING FREQUENCY FOR THEE PENTIUM MICROPROCESSOR
CPUTYP	I	CPU TYPE PIN SAMPLED BY THE PROCESSOR AT THE TRAILING-EDGE OF RESET TO DETERMINE WHETHER IT IS PRIMARY OR THE DUAL PROCESSPR.

5.1 PENTIUM MICROPROCESSOR (P54LM)-2

SYMBOL	TYPE	DESCRIPTION
D7:D0	I/O	DATA PATH ZERO.
D51:D8	I/O	DATA PATH ONE.
D23:D16	I/O	DATA PATH TWO.
D31:D24	I/O	DATA PATH THREE.
D39:D32	I/O	DATA PATH FOUR.
D47:D40	I/O	DATA PATH FIVE.
D55:D48	I/O	DATA PATH SIX.
D63:D56	I/O	DATA PATH SEVEN.
D/C#	I/O	DATA OR CONTROL. AT THE START OF BUS CYCLE, THE PENTIUM PROCESSOR SETS THIS LINE HIGH IF DATA WILL BE TRANSFERED DURING THE CURRENT BUS CYCLE,OTHERWISE SETS IT TO LOW.
D/P#	O	DUAL/PRIMARY.THIS IS AN OUTPUT OF PRIMARY PROCESSOR AND IS NOT USED BY THE DUAL PROCESSOR.IT ASSERTED(LOW) BY THE PRIMARY PROCESSOR WHEN IT HAS ACQUIRED PRIVATE BUS OWNERSHIP AND HAS INITIATED A BUS CYCLE
DPO	I/O	PARITY BIT FOR DATA PATH 0,D7:D0.
DP1	I/O	PARITY BIT FOR DATA PATH 1,D15:D8.
DP2	I/O	PARITY BIT FOR DATA PATH 2,D23:D16.
DP3	I/O	PARITY BIT FOR DATA PATH 3,D31:D24.
DP4	I/O	PARITY BIT FOR DATA PATH 4,D39:D32.
DP5	I/O	PARITY BIT FOR DATA PATH 5,D47:D40.
DP6	I/O	PARITY BIT FOR DATA PATH 6,D55:D48.
DP7	I/O	PARITY BIT FOR DATA PATH 7,D63:D56.
DPEN#	I/O	DUAL PROCESSOR ENABLE.
EADS#	I	THE EXTERNAL ADDRESS STROBE SIGNAL INDICATES THAT A VALID EXTERNAL ADDRESS HAS BEEN DRIVEN ONTO THE PENTIUM'S A4:A31 ADDRESS LINES BY ANOTHER MASTER.
EWBE#	I	THE EXTERNAL WRITE BUFFER EMPTY IS USED TO ENSURE THAT MEMORY OPERATIONS OCCUR IN ORDER OF EXECUTION.
FLUSH#	I	THE CACHE FLUSH INPUT FORCES FORCES THE PENTIUM ROCESSOR TO FLUSH THE CONTENTS IN OF ITS INTERNAL CACHE.
FERR#	O	FLOATING0POINT ERROR OUTPUT PIN IS DRIVEN ACTIVE WHEN A FLOATING-POINT ERROR OCCURS.

SYMBOL	TYPE	DESCRIPTION
FRCMC#	I	THE FUNCTOIN REDUNDANCY CHECKING MASTER/CHECKER# PIN IS SAMPLED BY THE PENTIUM MICROPROCESSOR DURING RESET TO DETERMINE WHETHER THE MICROPROCESSOR SHOULD BE CONFIGED AS A FUNCTIONAL REDUNDANCY MASTER OR CHECKER.
HIT#	I/O	THE HIT# SIGNAL ACTIVE TO INDICATE A SNOOP HIT IN EITHER THE INTERNAL CODE OR DATA CACHE.
HITM#	I/O	THE PENTIUM MICOPROCESSOR DRIVES THE HIT MODIFIED SIGNAL ACTIVE TO INDICATE A SNOOP HIT TO A MODIFIED LINE IN THE DATA CACHE.
HLDA	I/O	BUS HOLD ACKNOWLEDGE.
HOLD	I	THE BUS HOLD REQUEST INPUT ALLOWS ANOTHER BUS MASTER TO GAIN COMPLETE CONTROL OF THE PENTIUM'S LOCAL BUSES.
IBT	NA	THE INSTRUCTION BRANCH TAKEN SIGNAL IS DRIVEN ACTIVE FOR ONE CLOCK CYCLE WHEN PENTIUM MICROPROCESSOE EXECUTES AN INSTRUCTION RESULTING IN AN EXECUTION BRANCH.
IERR#	O	INTERNAL ERROR IS ASSERTED WHEN A PARITY ERROR IS ENCOUNTERED INSIDE THE PENTIUM MICROPROCESSOR.
IGNNE#	I	IGNORE NUMERIC ERROR INPUT IS ASSERTED BY EXTERNAL LOGIC THE PENTIUM MICROPROCESSOR WILL IGNORE A NUMERIC ERROR. AND CONTINUE EXECUTING NON-CONTROL FLOATING-POINT INSTRUCTIONS.
INIT	I	PENTIUM MICROCESSOR INIT INPUT HASTHE SAME EFFECT AS THE RESET SIGNAL EXCEPT THAT THE FOLLOWING RETAIN THE VALUES.
INTR	I	THIS IS MASKABLE INTERRUPT REQUEST INPUT.
INV	I	THE INVALIDATE INPUT TELLS THE PENTIUM MICROPROCESSOR WHETHER THE CACHE LINE STATE SHOULD BE MARKED INVALIDATED OR SHARED AS A RESULT OF SNOOP HIT.
IU	NA	THE IU SIGNAL IDICATED THAT AN INSTRUCTION IN THE "u" PIPLINE HAS COMPLETED EXECUTION.
IV	NA	THE IU SIGNAL IDICATED THAT AN INSTRUCTION IN THE "v" PIPLINE HAS COMPLETED EXECUTION.

5.1 PENTIUM MICROPROCESSOR (P54LM)-3

SYMBOL	TYPE	DESCRIPTION
KEN#	I	THE CACHE ENABLE PIN IS SAMPLED TO DETERMINE IF THE CURRENT BUS CYCLE IS CACHEABLE.
LINT0 OR INTR	I	IF THE PROCESSOR'S LOCAL APIC IS ENABLE, THIS IS THE LINT0 INPUT TO THE APIC.
LOCK#	I/O	THE LOCK# SIGNAL IS ASSERTED WHEN THE PENTIUM MICROPROCESSOR WANTS TO RUN MULTIP BUS CYCLES WITHOUT HAVING THE BUSES TAKEN AWAY BY ANOTHER BUS MASTER.
M/IO#	I/O	MEMORY OR I/O. AT THE START OF BUS CYCLE, THE PENTIUM PROCESSOR SETS THIS LINE HIGH IF ADDRESSING A MEMORY LOC-ATION AND LOW IF ADDRESSING AN I/O LOCATION.
NA#	I	THE NEXT ADDRESS INPUT INDICATES THAT THE MEMORY SUBSYSTEM IS CAPABLE FO TAKING ADVANTAGE OF THE PENTIUM MICROPROCESSOR'S ADDRESS PIPELINING.
NMI	I	NON-MASKABLE INTERRUPT REQUEST.
PBREQ#	I/O	PRIVATE BUS REQUEST.ONLY USED IN DUAL PROCESSOR SYSTEM.
PBGNT#	I/O	PRIVATE BUS GRANT.ONLY USED IN DUAL PROCESSOR SYSTEM.
PCHK#	O	SEE DP0.
PCD	O	PAGE CACHE DISABLE.
PEN#	I	PARITY ENABLE.
PHIT#	I/O	PARIVATE BUS HIT.PHIT# IS AN OUTPUT FROM THE LRM AND AN INPUT TO THE MRM.TI IS USED IN A DUAL PROCESSOR SYTEM.
PHITM#	I/O	PRIVATE BUS HIT ON MODIFIED LINE.
PICCLK	I	PROGRAMMABLE INTERRUPT CONTROLLER CLOCK.
PICDO OR DEPN#	I/O	PROGRAMMABLE INTERRUPT CONTROLLER DATA LINE0.
PICD1 OR APICEN	I/O	PROGRAMMABLE INTERRUPT CONTROLLER DATA LINE1.
PRDY	O	PROBE READY.ASSERTED BY THE PROCESSOR WHEN IT HAS STOP-PED EXECUTION IN RESPONSE TO THE R/S# SIGNAL BEING ASSERTED LOW.
PWT	O	THE PAGE WRITE-THROUGHT PIN REFLECTS THE STATE OF THE PAGE ATTRIBUTE BIT.

SYMBOL	TYPE	DESCRIPTION
RESET	I	1.KEEPS THE MICROPROCESSOR FROM OPERATING UNTIL THE POWER SUPPLY VOLTAGES HAVE COME UP AND STSBILIZED. 2.FORCES KNOWN DEFAULT VALUES INTO THE PENTIUM PROCESSOR REGISTER.
R/S#	I	RUN/STOP. WHEN SET HIGH, THE PROCESSOR IS PERMITTED TO RUN NORMALLY.WHEN SET LOW, THE PROCESSOR CEASES TO EXECUTE INSTRUCTIONS AND ENTERS PROBE MODE.
SCYC	I/O	SPLIT CYCLE IS VALID FOR LOCKED BUS CYCLES OLY.SCYC IS ASSERTED WHEN A LOCKED TRANSFER RESULTS IN A MISALIGNED MWMORY ACCESS.
SMI#	I	SYSTEM MANAGEMENT INTERRUPT INFORMS THE PROCESSOR THAT A SYSTEM MANAGEMENT INTERRUPT ROUTINE.RESIDING IN SYSTEM MANAGEMENT ADDRESS SPACE NEEDS TO BE PERFORMED.
SMICAT#	O	SYSTEM MANAGEMENT INTERRUPT ACKNOWEDGW INFORMS EXTE-RNAL LOGIC THAT THE PROCESSOR IS IN SYSTEM MANAGEMENT MODE.
TCK	I	TEST CLOCK.USED TO CLOCK STATE INFORMATION AND DATA INTO AND OUT OF DEVICE DURING BOUNDARY SCAN.
TDI	I	TEST INPUT.USED TO SHIFT DATA AND INSTRUCTIONS INTO THE TEST ACCESS PORT IN A SERIAL BIT STREAM.
TDO	O	TEST OUTPUT.USED TO SHIFT DATA OUT OF THE TEST ACCESS PORT IN A SERIAL BIT STREAM.
TMS	I	TEST MODE SELECT.USED TO CONTROL THE STATE OF THE TEST ACCESS PORT CONTROLLER.
TRST#	I	TEST RESET.USED TO FORCE THE TEST ACCESS PORT CONTROLLER INTO AN INITIALIZED STATE.
WB/WT#	I	THE WRITE-BACK OR WRITE THROUGH INPUT ALLOWS EXTERNAL LOGIC TO DETERMINE WHETHER A IS PLACED IN THE WRITE BACK OR WRITE THROUGH STATE.
W/R#	I/O	WRITE OR READ.AT THE START OF A BUS CYCLE,THE PENTIUM PROCESSOR SETS THIS LINE HIGH IF THE CURRENT BUS CYCLE IS A WRITE BUS CYCLE.W/R# IS SET LOW IF THE CURRENT BUS CYCLE IS A READ BUS CYCLE.

5.2 PENTIUM MICROPROCESSOR (P55C)-1

Symbol	Type	Name and Function
A20M#	I	When the **address bit 20 mask** pin is asserted, the Pentium ?processor with MMX™ technology emulates the address wraparound at 1 Mbyte which occurs on the 8086 by masking physical address bit 20 (A20) before performing a lookup to the internal caches or driving a memory cycle on the bus. The effect of A20M# is undefined in protected mode. A20M# must be asserted only when the processor is in real mode. A20M# is internally masked by the Pentium processor with MMX technology when configured as a Dual processor.
A31-A3	I/O	As outputs, the **address** lines of the processor along with the byte enables define the physical area of memory or I/O accessed. The external system drives the inquire address to the processor on A31-A5.
ADS#	O	The **address strobe** indicates that a new valid bus cycle is currently being driven by the Pentium processor with MMX technology.
ADSC#	O	The **address strobe (copy)** is functionally identical to ADS#.
AHOLD	I	In response to the assertion of **address hold**, the Pentium processor with MMX technology will stop driving the address lines (A31-A3) and AP in the next clock. The rest of the bus will remain active so data can be returned or driven for previously issued bus cycles.
AP	I/O	**Address parity** is driven by the Pentium processor with MMX technology with even parity information on all Pentium processor with MMX technology generated cycles in the same clock that the address is driven. Even parity must be driven back to the Pentium processor with MMX technology during inquire cycles on this pin in the same clock as EADS# to ensure that correct parity check status is indicated by the Pentium processor with MMX technology.
APCHK#	O	The **address parity check** status pin is asserted two clocks after EADS# is sampled active if the Pentium processor with MMX technology has detected a parity error on the address bus during inquire cycles. APCHK# will remain active for one clock each time a parity error is detected (including during dual processing private snooping).
[APICEN] PICD1	I	**Advanced Programmable Interrupt Controller Enable** enables or disables the on-chip APIC interrupt controller. If sampled high at the falling edge of RESET, the APIC is enabled. APICEN shares a pin with the PICD1 signal.

Symbol	Type	Name and Function
BE7#-E4# BE3#-E0#	O I/O	The **byte enable** pins are used to determine which bytes must be written to external memory or which bytes were requested by the CPU for the current cycle. The byte enables are driven in the same clock as the address lines (A31-3). Additionally, the lower 4-byte enables (BE3#-BE0#) are used on the Pentium processor with MMX technology as APIC ID inputs and are sampled at RESET. In dual processing mode, BE4# is used as an input during Flush cycles.
BF[1:0]	I	The **bus frequency** pins determine the bus-to-core frequency ratio. BF[1:0] are sampled at RESET, and cannot be changed until another non-warm (1 ms) assertion of RESET. Additionally, BF[1:0] must not change values while RESET is active. See Table 3 for Bus Frequency Selections.
BOFF#	I	The **backoff** input is used to abort all outstanding bus cycles that have not yet completed. In response to BOFF#, the Pentium processor with MMX technology will float all pins normally floated during bus hold in the next clock. The processor remains in bus hold until BOFF# is negated, at which time the Pentium processor with MMX technology restarts the aborted bus cycle(s) in their entirety.
BP[3:2] PM/BP[1:0]	O	The **breakpoint** pins (BP3-0) correspond to the debug registers, DR3-DR0 These pins externally indicate a breakpoint match when the debug registers are programmed to test for breakpoint matches.
		BP1 and BP0 are multiplexed with the **performance monitoring** pins (PM1 and PM0). The PB1 and PB0 bits in the Debug Mode Control Register determine if the pins are configured as breakpoint or performance monitoring pins. The pins come out of RESET configured for performance monitoring.
BRDY#	I	The **burst ready** input indicates that the external system has presented valid data on the data pins in response to a read or that the external system has accepted the Pentium processor with MMX technology data in response to a write request. This signal is sampled in the T2, T12 and T2P bus states.
BRDYC#	I	The **burst ready (copy)** is functionally identical to BRDY#.
BREQ	O	The **bus request** output indicates to the external system that the Pentium processor with MMX technology has internally generated a bus request. This signal is always driven whether or not the Pentium processor with MMX technology is driving its bus.

5.2 PENTIUM MICROPROCESSOR (P55C)-2

Symbol	Type	Name and Function
BUSCHK#	I	The **bus check** input allows the system to signal an unsuccessful completion of a bus cycle. If this pin is sampled active, the Pentium processor with MMX technology will latch the address and control signals in the machine check registers. If, in addition, the MCE bit in CR4 is set, the Pentium processor with MMX technology will vector to the machine check exception. **NOTE:** To assure that BUSCHK# will always be recognized, STPCLK# must be deasserted any time BUSCHK# is asserted by the system, before the system allows another external bus cycle. If BUSCHK# is asserted by the system for a snoop cycle while STPCLK# remains asserted, usually (if MCE=1) the processor will vector to the exception after STPCLK# is deasserted. But if another snoop to the same line occurs during STPCLK# assertion, the processor can lose the BUSCHK# request.
CACHE#	O	For Pentium processor with MMX technology-initiated cycles the **cache** pin indicates internal cacheability of the cycle (if a read), and indicates a burst write back cycle (if a write). If this pin is driven inactive during a read cycle, the Pentium processor with MMX technology will not cache the returned data, regardless of the state of the KEN# pin. This pin is also used to determine the cycle length (number of transfers in the cycle).
CLK	I	The **clock** input provides the fundamental timing for the Pentium processor with MMX technology. Its frequency is the operating frequency of the Pentium processor with MMX technology external bus, and requires TTL levels. All external timing parameters except TDI, TDO, TMS, TRST#, and PICD0-1 are specified with respect to the rising edge of CLK. This pin is 3.3V-tolerant-only on the Pentium processor with MMX technology. Please refer to the Pentium ?Processor Family Developer• Manual (Order Number 241428) for the CLK and PICCLK signal quality specification. **NOTE:** It is recommended that CLK begin toggling within 150 ms after VCC reaches its proper operating level. This recommendation is to ensure long-term reliability of the device.
CPUTYP	I	**CPU type** distinguishes the Primary processor from the Dual processor. In a single processor environment, or when the Pentium processor with MMX technology is acting as the Primary processor in a dual processing system, CPUTYP should be strapped to VSS. The Dual processor should have CPUTYP strapped to VCC3.
D/C#	O	The **data/code** output is one of the primary bus cycle definition pins. It is driven valid in the same clock as the ADS# signal is asserted. D/C# distinguishes between data and code or special cycles.

Symbol	Type	Name and Function
D/P#	O	The **dual/primary** processor indication. The Primary processor drives this pin low when it is driving the bus, otherwise it drives this pin high. D/P# is always driven. D/P# can be sampled for the current cycle with ADS# (like a status pin). This pin is defined only on the Primary processor. Dual processing is supported in a system only if both processors are operating at identical core and bus frequencies. Within these restrictions, two processors of different steppings may operate together in a system.
D63-D0	I/O	These are the 64 **data lines** for the processor. Lines D7-D0 define the least significant byte of the data bus; lines D63-D56 define the most significant byte of the data bus. When the CPU is driving the data lines, they are driven during the T2, T12, or T2P clocks for that cycle. During reads, the CPU samples the data bus when BRDY# is returned.
DP7-DP0	I/O	These are the **data parity** pins for the processor. There is one for each byte of the data bus. They are driven by the Pentium processor with MMX technology with even parity information on writes in the same clock as write data. Even parity information must be driven back to the Pentium processor with MMX technology on these pins in the same clock as the data to ensure that the correct parity check status is indicated by the Pentium processor with MMX technology. DP7 applies to D63-56, DP0 applies to D7-0.
[DPEN#] PICD0	I/O	**Dual processing enable** is an output of the Dual processor and an input of the Primary processor. The Dual processor drives DPEN# low to the Primary processor at RESET to indicate that the Primary processor should enable dual processor mode. DPEN# may be sampled by the system at the falling edge of RESET to determine if the dual-processor socket is occupied. DPEN# is multiplexed with PICD0.
EADS#	I	This signal indicates that a valid **external address** has been driven onto the Pentium processor with MMX technology address pins to be used for an inquire cycle.
EWBE#	I	The **external write buffer empty** input, when inactive (high), indicates that a write cycle is pending in the external system. When the Pentium processor with MMX technology generates a write, and EWBE# is sampled inactive, the Pentium processor with MMX technology will hold off all subsequent writes to all E- or M-state lines in the data cache until all write cycles have completed, as indicated by EWBE# being active.
FERR#	O	The **floating-point error** pin is driven active when an unmasked **floating-point** error occurs. FERR# is similar to the ERROR# pin on the Intel387?math coprocessor. FERR# is included for compatibility with systems using DOS type **floating-point** error reporting. FERR# is never driven active by the Dual processor.

5.2 PENTIUM MICROPROCESSOR (P55C)-3

Symbol	Type	Name and Function
FLUSH#	I	When asserted, the **cache flush** input forces the Pentium processor with MMX technology to write back all modified lines in the data cache and invalidate its internal caches. A Flush Acknowledge special cycle will be generated by the Pentium processor with MMX technology indicating completion of the write back and invalidation. If FLUSH# is sampled low when RESET transitions from high to low, tristate test mode is entered. If two Pentium processors with MMX technology are operating in dual processing mode and FLUSH# is asserted, the Dual processor will perform a flush first (without a flush acknowledge cycle), then the Primary processor will perform a flush followed by a flush acknowledge cycle. **NOTE:** If the FLUSH# signal is asserted in dual processing mode, it must be deasserted at least one clock prior to BRDY# of the FLUSH Acknowledge cycle to avoid DP arbitration problems.
FRCMC#	I	Functional Redundancy Checking is not supported on the Pentium processor with MMX technology. The FRCMC# pin is not defined for the Pentium processor with MMX technology. This pin should be left as a • C?or tied to VCC3 via an external pull-up resistor.
HIT#	O	The **hit** indication is driven to reflect the outcome of an inquire cycle. If an inquire cycle hits a valid line in either the Pentium processor with MMX technology data or instruction cache, this pin is asserted two clocks after EADS# is sampled asserted. If the inquire cycle misses the Pentium processor with MMX technology cache, this pin is negated two clocks after EADS#. This pin changes its value only as a result of an inquire cycle and retains its value between the cycles.
HITM#	O	The **hit to a modified line** output is driven to reflect the outcome of an inquire cycle. It is asserted after inquire cycles which resulted in a hit to a modified line in the data cache. It is used to inhibit another bus master from accessing the data until the line is completely written back.
HLDA	O	The **bus hold acknowledge** pin goes active in response to a hold request driven to the processor on the HOLD pin. It indicates that the Pentium processor with MMX technology has floated most of the output pins and relinquished the bus to another local bus master. When leaving bus hold, HLDA will be driven inactive and the Pentium processor with MMX technology will resume driving the bus. If the Pentium processor with MMX technology has a bus cycle pending, it will be driven one clock cycle after HLDA is de-asserted.

Symbol	Type	Name and Function
HOLD	I	In response to the **bus hold request**, the Pentium processor with MMX technology will float most of its output and input/output pins and assert HLDA after completing all outstanding bus cycles. The Pentium processor with MMX technology will maintain its bus in this state until HOLD is de-asserted. HOLD is not recognized during LOCK cycles. The Pentium processor with MMX technology will recognize HOLD during reset.
IERR#	O	The **internal error** pin is used to indicate internal parity errors. If a parity error occurs on a read from an internal array, the Pentium processor with MMX technology will assert the IERR# pin for one clock and then shutdown.
IGNNE#	I	This is the **ignore numeric error** input. This pin has no effect when the NE bit in CR0 is set to 1. When the CR0.NE bit is 0, and the IGNNE# pin is asserted, the Pentium processor with MMX technology will ignore any pending unmasked numeric exception and continue executing floating-point instructions for the entire duration that this pin is asserted. When the CR0.NE bit is 0, IGNNE# is not asserted, a pending unmasked numeric exception exists (SW.ES = 1), and the floating-point instruction is one of FINIT, FCLEX, FSTENV, FSAVE, FSTSW, FSTCW, FENI, FDISI, or FSETPM, the Pentium processor with MMX technology will execute the instruction in spite of the pending exception. When the CR0.NE bit is 0, IGNNE# is not asserted, a pending unmasked numeric exception exists (SW.ES = 1), and the floating-point instruction is one other than FINIT, FCLEX, FSTENV, FSAVE, FSTSW, FSTCW, FENI, FDISI, or FSETPM,the Pentium processor with MMX technology will stop execution and wait for an external interrupt. IGNNE# is internally masked when the Pentium processor with MMX technology is configured as a Dual processor.
INIT	I	The Pentium processor with MMX technology **initialization** input pin forces the Pentium processor with MMX technology to begin execution in a known state. The processor state after INIT is the same as the state after RESET except that the internal caches, write buffers, and floating-point registers retain the values they had prior to INIT. INIT may NOT be used in lieu of RESET after power-up. If INIT is sampled high when RESET transitions from high to low, the Pentium processor with MMX technology will perform built-in self test prior to the start of program execution.
INTR/LINT0	I	An active **maskable interrupt** input indicates that an external interrupt has been generated. If the IF bit in the EFLAGS register is set, the Pentium processor with MMX technology will generate two locked interrupt acknowledge bus cycles and vector to an interrupt handler after the current instruction execution is completed. INTR must remain active until the first interrupt acknowledge cycle is generated to assure that the interrupt is recognized. If the local APIC is enabled, this pin becomes LINT0.

5.2 PENTIUM MICROPROCESSOR (P55C)-4

Symbol	Type	Name and Function
INV	I	The **invalidation** input determines the final cache line state (S or I) in case of an inquire cycle hit. It is sampled together with the address for the inquire cycle in the clock EADS# is sampled active.
KEN#	I	The **cache enable** pin is used to determine whether the current cycle is cacheable or not and is consequently used to determine cycle length. When the Pentium processor with MMX technology generates a cycle that can be cached (CACHE# asserted) and KEN# is active, the cycle will be transformed into a burst line fill cycle.
LINT0/INTR	I	If the APIC is enabled, this pin is **local interrupt 0**. If the APIC is disabled, this pin is INTR.
LINT1/NMI	I	If the APIC is enabled, this pin is **local interrupt 1**. If the APIC is disabled, this pin is NMI.
LOCK#	O	The **bus lock** pin indicates that the current bus cycle is locked. The Pentium processor with MMX technology will not allow a bus hold when LOCK# is asserted (but AHOLD and BOFF# are allowed). LOCK# goes active in the first clock of the first locked bus cycle and goes inactive after the BRDY# is returned for the last locked bus cycle. LOCK# is guaranteed to be de-asserted for at least one clock between back-to-back locked cycles.
M/IO#	O	The **memory/input-output** is one of the primary bus cycle definition pins. It is driven valid in the same clock as the ADS# signal is asserted. M/IO# distinguishes between memory and I/O cycles.
NA#	I	An active **next address** input indicates that the external memory system is ready to accept a new bus cycle although all data transfers for the current cycle have not yet completed. The Pentium processor with MMX technology will issue ADS# for a pending cycle two clocks after NA# is asserted. The Pentium processor with MMX technology supports up to 2 outstanding bus cycles.
NMI/LINT1	I	The **non-maskable interrupt** request signal indicates that an external non-maskable interrupt has been generated. If the local APIC is enabled, this pin becomes LINT1.
PBGNT#	I/O	**Private bus grant** is the grant line that is used when two Pentium processors with MMX technology are configured in dual processing mode, in order to perform private bus arbitration. PBGNT# should be left unconnected if only one Pentium processor with MMX technology exists in a system.

Symbol	Type	Name and Function
PBREQ#	I/O	**Private bus request** is the request line that is used when two Pentium processor with MMX technology are configured in dual processing mode, in order to perform private bus arbitration. PBREQ# should be left unconnected if only one Pentium processor with MMX technology exists in a system.
PCD	O	The **page cache disable** pin reflects the state of the PCD bit in CR3, the Page Directory Entry, or the Page Table Entry. The purpose of PCD is to provide an external cacheability indication on a page by page basis.
PCHK#	O	The **parity check** output indicates the result of a parity check on a data read. It is driven with parity status two clocks after BRDY# is returned. PCHK# remains low one clock for each clock in which a parity error was detected. Parity is checked only for the bytes on which valid data is returned. When two Pentium processors with MMX technology are operating in dual processing mode, PCHK# may be driven two or three clocks after BRDY# is returned.
PEN#	I	The **parity enable** input (along with CR4.MCE) determines whether a machine check exception will be taken as a result of a data parity error on a read cycle. If this pin is sampled active in the clock a data parity error is detected, the Pentium processor with MMX technology will latch the address and control signals of the cycle with the parity error in the machine check registers. If, in addition, the machine check enable bit in CR4 is set to ?? the Pentium processor with MMX technology will vector to the machine check exception before the beginning of the next instruction.
PHIT#	I/O	**Private hit** is a hit indication used when two Pentium processors with MMX technology are configured in dual processing mode, in order to maintain local cache coherency. PHIT# should be left unconnected if only one Pentium processor with MMX technology exists in a system.
PHITM#	I/O	**Private modified hit** is a hit on a modified cache line indication used when two Pentium processors with MMX technology are configured in dual processing mode, in order to maintain local cache coherency. PHITM# should be left unconnected if only one Pentium processor with MMX technology exists in a system.
PICCLK	I	The APIC interrupt controller serial data bus clock is driven into the **programmable interrupt controller clock** input of the Pentium processor with MMX technology. This pin is 3.3V-tolerant-only on the Pentium processor with MMX technology. Please refer to the Pentium ?Processor Family Developer• Manual (Order Number 241428) for the CLK and PICCLK signal quality specification.

5.2 PENTIUM MICROPROCESSOR (P55C)-5

Symbol	Type	Name and Function
PICD0-1 [DPEN#] [APICEN]	I/O	**Programmable interrupt controller data lines 0-1** of the Pentium processor with MMX technology comprise the data portion of the APIC 3-wire bus. They are open-drain outputs that require external pull-up resistors. These signals are multiplexed with DPEN# and APICEN respectively.
PM/BP[1:0]	O	These pins function as part of the performance monitoring feature. The breakpoint 1-0 pins are multiplexed with the **performance monitoring 1-0** pins. The PB1 and PB0 bits in the Debug Mode Control Register determine if the pins are configured as breakpoint or performance monitoring pins. The pins come out of RESET configured for performance monitoring.
PRDY	O	The **probe ready** output pin is provided for use with the Intel debug port. Please refer to the Pentium?Processor Family Developer• Manual (Order Number 241428) for more details.
PWT	O	The **page write through** pin reflects the state of the PWT bit in CR3, the page directory entry, or the page table entry. The PWT pin is used to provide an external write back indication on a page-by-page basis.
R/S#	I	The **run/stop** input is provided for use with the Intel debug port. Please refer to the Pentium?Processor Family Developer• Manual (Order Number 241428) for more details.
RESET	I	**RESET** forces the Pentium processor with MMX technology to begin execution at a known state. All the Pentium processor with MMX technology internal caches will be invalidated upon the RESET. Modified lines in the data cache are not written back. FLUSH# and INIT are sampled when RESET transitions from high to low to determine if tristate test mode or checker mode will be entered, or if Built-In Self-Test (BIST) will be run.
SCYC	O	The **split cycle** output is asserted during misaligned LOCKed transfers to indicate that more than two cycles will be locked together. This signal is defined for locked cycles only. It is undefined for cycles which are not locked.
SMI#	I	The **system management interrupt** causes a system management interrupt request to be latched internally. When the latched SMI# is recognized on an instruction boundary, the processor enters System Management Mode.
SMIACT#	O	An active **system management interrupt active** output indicates that the processor is operating in System Management Mode.

Symbol	Type	Name and Function
STPCLK#	I	Assertion of the **stop clock** input signifies a request to stop the internal clock of the Pentium processor with MMX technology, thereby causing the core to consume less power. When the CPU recognizes STPCLK#, the processor will stop execution on the next instruction boundary, unless superseded by a higher priority interrupt, and generate a stop grant acknowledge cycle. When STPCLK# is asserted, the Pentium processor with MMX technology will still respond to interprocessor and external snoop requests.
TCK	I	The **testability clock** input provides the clocking function for the Pentium processor with MMX technology boundary scan in accordance with the IEEE Boundary Scan interface (Standard 1149.1). It is used to clock state information and data into and out of the Pentium processor with MMX technology during boundary scan.
TDI	I	The **test data input** is a serial input for the test logic. TAP instructions and data are shifted into the Pentium processor with MMX technology on the TDI pin on the rising edge of TCK when the TAP controller is in an appropriate state.
TDO	O	The **test data output** is a serial output of the test logic. TAP instructions and data are shifted out of the Pentium processor with MMX technology on the TDO pin on TCK′s falling edge when the TAP controller is in an appropriate state.
TMS	I	The value of the **test mode select** input signal sampled at the rising edge of TCK controls the sequence of TAP controller state changes.
TRST#	I	When asserted, the **test reset** input allows the TAP controller to be asynchronously initialized.
VCC2 VCC3	I I	The Pentium processor with MMX technology has 25 2.8V **power** inputs. The Pentium processor with MMX technology has 28 3.3V **power** inputs.
VCC2DET#	O	**VCC2 detect** is used in flexible motherboard implementations to configure the voltage output set-point appropriately for the VCC2 inputs of the processor.
VSS	I	The Pentium processor with MMX technology has 53 **ground** inputs.
W/R#	O	**Write/read** is one of the primary bus cycle definition pins. It is driven valid in the same clock as the ADS# signal is asserted. W/R# distinguishes between write and read cycles.
WB/WT#	I	The **write back/write through** input allows a data cache line to be defined as write back or write through on a line-by-line basis. As a result, it determines whether a cache line is initially in the S or E state in the data cache.

5.3 INTEL FW82439TX MEMORY/PCI/CACHE CONTROLLER (MTXC)-1

2.1. MTXC Signals 2.1.1.HOST INTERFACE

Name	Type	Description
A[31:3]	I/O 3.3V/2.5V	**Address Bus.** A[31:3] connects to the address bus of the CPU. During CPU cycles A[31:3] are inputs. The MTXC drives A[31:3] during inquire cycles on behalf of PCI initiators. Bits A[31:26] act as inputs when RST# is active
BE[7:0]#	I 3.3V/2.5V	**Byte Enables.** The CPU byte enables indicate which byte lane the current CPU cycle is accessing. All eight byte lanes must be provided to the CPU if the cycle is a cacheable read regardless of the state of BE[7:0]#.
ADS#	I 3.3V/2.5V	**Address Status.** CPU asserts ADS# in T1 of the CPU bus cycle.
BRDY#	O 3.3V/2.5V	**Bus Ready.** The MTXC asserts BRDY# to indicate to the CPU that data is available on reads or has been received on writes
NA#	O 3.3V/2.5V	**Next Address.** This signal is asserted by the MTXC to indicate to the Processor that it is ready to process a second cycle.
AHOLD	O 3.3V/2.5V	**Address Hold.** The MTXC asserts AHOLD when a PCI initiator is performing a cycle to DRAM. AHOLD is held for the duration of the PCI burst transfer. The MTXC will negate AHOLD when the completion of the PCI to DRAM read or write cycles complete and during PCI peer transfers. AHOLD is kept asserted while PHLDA# is asserted (i.e., duration of PIIX4 granting).
EADS#	O 3.3V/2.5V	**External Address Strobe.** Asserted by the MTXC to inquire the first level cache when servicing PCI master references of DRAM.
BOFF#	O 3.3V/2.5V	**Back Off.** Asserted by the MTXC when required to terminate a CPU cycle that was in progress.
HITM#	I 3.3V/2.5V	**Hit Modified.** Asserted by the CPU to indicate that the address presented with the last assertion of EADS# is modified in the first level cache and needs to be written back.
M/IO#, D/C#, W/R#	I 3.3V/2.5V	**Memory/IO; Data/Control; Write/Read.** Asserted by the CPU with ADS# to indicate the type of cycle that the system needs to perform.
HLOCK#	I 3.3V/2.5V	**Host Lock.** All CPU cycles sampled with the assertion of HLOCK# and ADS#, until the negation of HLOCK# must be atomic, i.e. no PCI activity to DRAM is allowed.
CACHE#	I 3.3V/2.5	**Cache.** Asserted by the CPU during a read cycle to indicate the CPU will Vperform a burst line fill. Asserted by the CPU during a write cycle to indicate the CPU will perform a burst writeback cycle. If CACHE# is asserted to indicate cacheability, the MTXC will assert KEN# either with the first BRDY#, or with NA# if NA# is asserted before the first BRDY#.
KEN#/INV	O 3.3V/2.5V	**Ken/Invalidate.** KEN#/INV functions as both the KEN# signal during CPU read cycles, and the INV signal during L1 snoop cycles. During CPU cycles, KEN#/INV is normally low. KEN#/INV is driven high during the 1st BRDY# or NA# assertion of a non-L1-cacheable CPU read cycle. KEN#/INV is driven high(low) during the EADS# assertion of a PCI master DRAM write(read) snoop cycle. Note that KEN#/INV operation during snoop cycles is independent of the FLCE bit programming.
SMIACT#	I 3.3V/2.5V	**System Management Interrupt Active.** This is asserted by the CPU when it is in system management mode as a result of an SMI. This signal must be sampled active with ADS# for the processor to access the SMM space of DRAM, located at A0000h, after SMM space has been loaded and locked by BIOS at system boot.
HD[63:0]	I/O 3.3V/2.5V	**Host Data.** These signals are connected to the CPU data bus. These signals have internal pull-down resistors.

NOTES:
All of the signals in the host interface are described in the Pentium Processor data sheet. The preceding table highlights MTXC specific uses of these signals.

2.1.2. DRAM INTERFACE

Name	Type	Description
RAS[3:0]# Or CS[3:0]#, RAS4#/CS4#/ BA1, RAS5#/CS5#/ MA13	O 3.3V	**Row Address Strobe• ASx# (EDO/FPM).** These pins select the DRAM row. **Chip Select-CSx# (SDRAM).** These pins activate the SDRAMs. SDRAM accepts any command when its CS# pin is active low. Note: For 64Mbit SDRAM support, BA1/MA12 and MA13 are muxed with the RAS4# and RAS5# signals, respectively. When SDRAMC[bit 1]=1, BA1 and MA13 are driven out on these lines.
CAS[7:0]# or DQM[7:0]	O 3.3V	**Column Address Strobe (EDO/FPM).** These pins select the DRAM column. **Input/Output Data Mask SDRAM).** These pins act as synchronized output enables during a read cycle and a byte mask during a write cycle. The read cycles require Tdqz clock latency before the functions are actually performed. In case of a write cycle, word mask functions are performed in the same cycle (0 cycle latency).
MA[11:0]	O 3.3 V	**Memory Address (EDO/FPM/SDRAM).** This is the row and column address for DRAM. These buffers now include programmable size selection, as controlled by the DRAMEC[MAD] bit. For 64-Mbit SDRAM support BA1/MA12 and MA13 are muxed with the RAS4# and RAS5# signals, respectively.

5.3 INTEL FW82439TX MEMORY/PCI/CACHE CONTROLLER (MTXC)-2

Name	Type	Description
MWEB#	O 3.3 V	**Memory Write Enable (second copy) (EDO/FPM/SDRAM).** MWE# should be used as the write enable for the memory data bus. This signal has programmable buffer size selection.
MWE#	O 3.3 V	**Memory Write Enable (EDO/FPM/SDRAM).** MWE# should be used as the write enable for the memory data bus. This signal has programmable buffer size selection.
SRAS[A,B]#	O 3.3 V	**SDRAM Row Address Strobe (SDRAM).** When asserted, this signal latches Row Address on the positive edge of the clock. This signal also allows Row access and precharge. Two copies are provided for loading purpose. These signals have programmable buffer size selection.
SCAS[A,B]#	O 3.3 V	**SDRAM Column Address Strobe (SDRAM).** When asserted, this signal latches Column Address on the positive edge of the clock. This signal also allows Column access. Two copies provided for loading purpose. These signals have programmable buffer size selection.
CKE/MAA0	O 3.3 V	**SDRAM Clock Enable (SDRAM).** SDRAM clock enable pin. When this signal is negated, SDRAM enters power down mode. This signal is also muxed to provide a second copy of memory address MA0 (MAA0). The MA function is selected via DRT[bit2] (offset 67h). MTXC negates CKE (and CKEB) when SUSSTAT1# is asserted. Note that MTXC asserts CKE (and CKEB) for all rows (i.e., CKE and CKEB cannot be selectively asserted for certain rows and negated for other rows).
CKEB/MAA1	O 3.3 V	**SDRAM Clock Enable (SDRAM) (second copy).** SDRAM clock enable pin. When this signal is negated, SDRAM enters into power down mode. Note that this signal is not implemented in the • uspend Well?and should not be used if suspend to RAM (STR) is implemented. This signal is also muxed to provide a second copy of memory address MA1 (MAA1). The MA function is selected via DRT[bit2] (offset 67h). MTXC negates CKE (and CKEB) when SUSSTAT1# is asserted. Note that MTXC asserts CKE (and CKEB) for all rows (i.e., CKE and CKEB cannot be selectively asserted for certain rows and negated for other rows).
MD[63:0] 3.3V/5V	I/O	**Memory Data.** These signals are connected to the DRAM data bus. These signals have internal pull-down resistors

2.1.3. SECONDARY CACHE INTERFACE

Name	Type	Description
CADV#	O 3.3V	**Cache Advance.** Assertion causes the PBSRAM in the secondary cache to advance to the next QWord in the cache line.
CADS#	O 3.3V	**Cache Address Strobe.** Assertion causes the PBSRAM in the secondary cache to load the PBSRAM address register from the PBSRAM address pins.
CCS#	O 3.3V	**Cache Chip Select (CCS#).** The second level cache will power up, if necessary, and perform an access if this signal is asserted when CADS# is asserted. The second level cache will power down if this signal is negated when CADS# is asserted. When CCS# is negated the second level cache will ignore ADS#. If CCS# is asserted when ADS# is asserted, the second level cache will power up, if necessary, and perform an access.
COE#	O 3.3V	**Cache Output Enable.** The secondary cache data RAMs drive the CPUs data bus when COE# is asserted.
GWE#	O 3.3V	**Global Write Enable.** GWE# assertion causes all the byte lanes to be written into the secondary cache data RAMs, if they are powered up.
BWE#	O 3.3V	**Byte Write Enable.** Asserted low with GWE#=HIGH to enable using host• BE[7:0]# to be used to control byte lanes to pipeline burst SRAM cache.
TIO[7:0]	I/O 3.3V/5V	**Tag Address.** These are inputs during CPU accesses and outputs during second level cache line fills and second level cache line invalidates due to inquire cycles. These signals have internal pull-down resistors.
TWE#	O 3.3V	**Tag Write Enable.** When asserted, new state and tag addresses are written into the external tag.
KRQAK/ CS4_64#	I/O 3.3V	**KRQAK/Chip Select 4 (for 64-Mb Technology).** This pin is a dual-function signal. KRQAK is used in a DRAM Cache L2 implementation and is a bi-directional refresh request/acknowledge. The CS4_64# function is used to generate the fifth chip select line in a SDRAM L2 Cache implementation that supports five rows of 64-Mbit SDRAM. During a hard reset, this signal is sampled to determine if DRAM cache is in the system (see MTXC Strapping options). This signal has a weak internal pull-down. If SDRAMC[bit 1]=1 and DRAM cache is not present in the system (indicated by CEC[bit 5]=0, offset 53h), the CS4_64# function is selected. If DRAM cache is in the system or SDRAMC[bit 1] (offset 54h)=0, then KRQAK is used to drive the KRQAK function.

5.3 INTEL FW82439TX MEMORY/PCI/CACHE CONTROLLER (MTXC)-3

2.1.4. PCI INTERFACE

Name	Type	Description
AD[31:0]	I/O 3.3/5V	**Address/Data.** The standard PCI address and data lines. Address is driven with FRAME# assertion, data is driven or received in following clocks.
C/BE[3:0]#	I/O 3.3/5V	**Command/Byte Enable.** The command is driven with FRAME# assertion, byte enables corresponding to supplied or requested data is driven on following clocks
FRAME#	I/O 3.3/5V	**Frame.** Assertion indicates the address phase of a PCI transfer. Negation indicates that one more data transfer is desired by the cycle initiator.
DEVSEL#	I/O 3.3/5V	**Device Select.** This signal is driven by the MTXC when a PCI initiator is attempting to access DRAM. DEVSEL# is asserted at medium decode time.
IRDY#	I/O 3.3/5V	**Initiator Ready.** Asserted when the initiator is ready for a data transfer.
TRDY#	I/O 3.3/5V	**Target Ready.** Asserted when the target is ready for a data transfer.
STOP#	I/O 3.3/5V	**Stop.** Asserted by the target to request the master to stop the current transaction.
LOCK#	I/O 3.3/5V	**Lock.** Used to establish, maintain, and release resource locks on PCI.
REQ[3:0]#	I 3.3/5V	**PCI Request.** PCI master requests for PCI bus.
GNT[3:0]#	O 3.3V	**PCI Grant.** Permission is given to the master to use PCI.
PHLD#	I 3.3/5V	**PCI Hold.** This signal comes from the expansion bridge. It is the bridge request for PCI. The MTXC will drain the DRAM write buffers, drain the CPU-to-PCI posting buffers, and acquire the host bus before granting via PHLDA#.
PHLDA#	O 3.3V	**PCI Hold Acknowledge.** This signal is driven by the MTXC to grant PCI to the expansion bridge. PHLDA# protocol has been modified to include support for passive release.
PAR	I/O 3.3/5V	**Parity.** A single parity bit is provided over AD[31:0] and C/BE[3:0]. This signal should be pulled high through a weak external pull-up resistor.
CLKRUN#	I/O 3.3/5V	**CLOCK RUN.** An open drain output and also an input. MTXC requests the central resource (PIIX4) to start, or maintain the PCI clock by the assertion of CLKRUN#. MTXC will tri-state CLKRUN# upon negation of reset (since CLK is running upon negation of reset). External pull-up is required. Note: This signal should be connected to the PIIX4 CLKRUN# pin. However, if it is left as a no connect on the MTXC, it must be pulled low through a 100**W** (pull-down resistor.
RST#	I 3.3/5V	**Reset.** When asserted this signal asynchronously resets the MTXC. The PCI signals also tri-state compliant to PCI Rev 2.0 and 2.1 specifications.

2.1.5. TEST AND CLOCK

Name	Type	Description
TEST#	I 3.3/5V	**Test In.** NAND tree mode is activated by driving this pin low. The test mode selected depends on the state of REQ[3:0]#. This pin should be pulled high with an external pull-up during normal operation.
HCLKIN	I 3.3/2.5V	**Host Clock In.** This pin receives a buffered host clock. This clock is used by all of the MTXC logic that is in the Host clock domain.
PCLKIN	I 3.3/5V	**PCI Clock In.** This pin receives a buffered divide-by-2 host clock. This clock is used by all of the MTXC logic that is in the PCI clock domain.

2.1.6. POWER MANAGEMENT

Name	Type	Description
SUSCLK	I 3.3V	**Suspend Clock.** The signal is a 32 KHz input for DRAM refresh circuitry and clocking events in suspend state. The DRAM refresh during suspend and non-suspend states is performed based on this clock. This signal has an internal pull-down resistor.
SUSSTAT1#	I 3.3V	**Suspend Status.** SUSSTAT1# indicates MTXC• power plane status during suspend mode. SUSSTAT1#, along with SUSCLK and RST#, define the suspend protocol between MTXC and PIIX4. This signal has an internal pull-up resistor.

2.1.7. POWER AND GROUND PINS

Name	Type	Description
VCC	3.3V	**Main voltage supply.** These pins are the primary voltage supply for the MTXC core and I/O periphery and must be connected to 3.3V.
VCC (CPU)	3.3V or 2.5V	**CPU Interface Voltage Supply.** These pins are the primary voltage supply for the MTXC Host periphery and must be connected to either 2.5V or 3.3V, depending on the oltage level of the CPU interface. Refer to the Power sequencing requirements section for additional details.
VCC (SUS)	3.3V	**Suspend Well Voltage Supply.** These pins are the primary voltage supply for the MTXC suspend logic and I/O. If suspend to RAM is supported, these pins should be on an isolated power plane; otherwise, they can be connected to the same 3.3V source used for the VCC pins.
VCC5REF	3.3V or 5V	**Voltage Reference.** This pin is tied to 5V through a small external power sequencing circuit, if MTXC signals are required to be 5V Tolerant. In a non 5V tolerant system (i.e. 3.3V only system), this signal can be tied directly to VCC. Refer to the Power sequencing requirements section for additional details.
VSS	0V	**Ground.** These pins are the ground for the MTXC.

5.3 INTEL FW82439TX MEMORY/PCI/CACHE CONTROLLER (MTXC)-4

2.2. MTXC Strapping Options

Name	Type	Description
SCS	A[31:30]	**Secondary Cache Size.** Described in the Cache Control Register bits 7:6.
L2RAMT	A[29:28]	**Initial L2 RAM Type.** Described in the Cache Control Register bits 5:4.
DRAM Cache	KRQAK	**DRAM Cache L2 Present Upon Reset Negation.** This bit is sampled to detect DRAM L2 cache. If sampled high, a DRAM Cache is present. A weak pulldown is provided internally. A DRAM cache module should implement a pull-up on this pin that overrides the weak pulldown. BIOS does not have to be aware of this, this information is used by the MTXC to maintain optimal Pburst timings.
25VD	A26	**2.5V Voltage Detection.** This bit is used to determine the voltage level (3.3V or 2.5V)of the host clock connected to the host clock pin and the voltage on the VCC(CPU)pins. An external pull-down or pull-up resistor is required on this pin (pulled down for 2.5V and pulled up for 3.3V).
HFD	A27	**Frequency Detection.** BIOS can use this bit to determine if the system is 60 MHz (external pull-up) or 66 MHz (no strapping is present) as described in the DRTH Register, bit 7. DRTH[bit 7] register is initialized with the inverted value of pin A27 upon reset negation. The A27 input buffer includes a weak pulldown resistor which will force DRTH[bit 7] to default to 1 if no strapping is present.

5.4 INTEL FW82371AB PCI/ISA BRIDGE (PIIX4)-1

PIIX4 Signals PCI BUS INTERFACE

Name	Type	Description
AD[31:0]	I/O	**PCI ADDRESS/DATA.** AD[31:0] is a multiplexed address and data bus. During the first clock of a transaction, AD[31:0] contain a physical byte address (32 bits). During subsequent clocks, AD[31:0] contain data. A PIIX4 Bus transaction consists of an address phase followed by one or more data phases. Little-endian byte ordering is used. AD[7:0] define the least significant byte (LSB) and AD[31:24] the most significant byte (MSB). When PIIX4 is a Target, AD[31:0] are inputs during the address phase of a transaction. During the following data phase(s), PIIX4 may be asked to supply data on AD[31:0] for a PCI read, or accept data for a PCI write. As an Initiator, PIIX4 drives a valid address on AD[31:2] and 0 on AD[1:0] during the address phase, and drives write or latches read data on AD[31:0] during the data phase. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
C/BE#[3:0]	I/O	**BUS COMMAND AND BYTE ENABLES.** The command and byte enable signals are multiplexed on the same PCI pins. During the address phase of a transaction, C/BE[3:0]# define the bus command. During the data phase C/BE[3:0]# are used as Byte Enables. The Byte Enables determine which byte lanes carry meaningful data. C/BE0# applies to byte 0, C/BE1# to byte 1, etc. PIIX4 drives C/BE[3:0]# as an Initiator and monitors C/BE[3:0]# as a Target. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
CLKRUN#	I/O	**CLOCK RUN#.** This signal is used to communicate to PCI peripherals that the PCI clock will be stopped. Peripherals can assert CLKRUN# to request that the PCI clock be restarted or to keep it from stopping. This function follows the protocol described in the PCI Mobile Design Guide, Revision 1.0. **During Reset:** Low **After Reset:** Low **During POS:** High
DEVSEL#	I/O	**DEVICE SELECT.** PIIX4 asserts DEVSEL# to claim a PCI transaction through positive decoding or subtractive decoding (if enabled). As an output, PIIX4 asserts DEVSEL# when it samples IDSEL active in configuration cycles to PIIX4 configuration registers. PIIX4 also asserts DEVSEL# when an internal PIIX4 address is decoded or when PIIX4 subtractively or positively decodes a cycle for the ISA/EIO bus or IDE device. As an input, DEVSEL# indicates the response to a PIIX4 initiated transaction and is also sampled when deciding whether to subtractively decode the cycle. DEVSEL# is tri-stated from the leading edge of PCIRST#. DEVSEL# remains tri-stated until driven by PIIX4 as a target. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
FRAME#	I/O	**CYCLE FRAME.** FRAME# is driven by the current Initiator to indicate the beginning and duration of an access. While FRAME# is asserted data transfers continue. When FRAME# is negated the transaction is in the final data phase. FRAME# is an input to PIIX4 when it is the Target. FRAME# is an output when PIIX4 is the initiator. FRAME# remains tri-stated until driven by PIIX4 as an Initiator. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z

Name	Type	Description
IDSEL	I	**INITIALIZATION DEVICE SELECT.** IDSEL is used as a chip select during PCI configuration read and write cycles. PIIX4 samples IDSEL during the address phase of a transaction. If IDSEL is sampled active, and the bus command is a configuration read or write, PIIX4 responds by asserting DEVSEL# on the next cycle.
IRDY#	I/O	**INITIATOR READY.** IRDY# indicates PIIX4• ability, as an Initiator, to complete the current data phase of the transaction. It is used in conjunction with TRDY#. A data phase is completed on any clock both IRDY# and TRDY# are sampled asserted. During a write, IRDY# indicates PIIX4 has valid data present on AD[31:0]. During a read, it indicates PIIX4 is prepared to latch data. IRDY# is an input to PIIX4 when PIIX4 is the Target and an output when PIIX4 is an Initiator. IRDY# remains tri-stated until driven by PIIX4 as a master. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
PAR	O	**CALCULATED PARITY SIGNAL.** PAR is • ven?parity and is calculated on 36 bits; AD[31:0] plus C/BE[3:0]#. • ven?parity means that the number of ?• within the 36 bits plus PAR are counted and the sum is always even. PAR is always calculated on 36 bits regardless of the valid byte enables. PAR is generated for address and data phases and is only guaranteed to be valid one PCI clock after the corresponding address or data phase. PAR is driven and tri-stated identically to the AD[31:0] lines except that PAR is delayed by exactly one PCI clock. PAR is an output during the address phase (delayed one clock) for all PIIX4 initiated transactions. It is also an output during the data phase (delayed one clock) when PIIX4 is the Initiator of a PCI write transaction, and when it is the Target of a read transaction. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
PCIRST#	O	**PCI RESET.** PIIX4 asserts PCIRST# to reset devices that reside on the PCI bus. PIIX4 asserts PCIRST# during power-up and when a hard reset sequence is initiated through the RC register. PCIRST# is driven inactive a minimum of 1 ms after PWROK is driven active. PCIRST# is driven for a minimum of 1 ms when initiated through the RC register. PCIRST# is driven asynchronously relative to PCICLK. **During Reset:** Low **After Reset:** High **During POS:** High
PHOLD#	O	**PCI HOLD.** An active low assertion indicates that PIIX4 desires use of the PCI Bus. Once the PCI arbiter has asserted PHLDA# to PIIX4, it may not negate it until PHOLD# is negated by PIIX4. PIIX4 implements the passive release mechanism by toggling PHOLD# inactive for one PCICLK. **During Reset:** High-Z **After Reset:** High **During POS:** High
PHLDA#	I	**PCI HOLD ACKNOWLEDGE.** An active low assertion indicates that PIIX4 has been granted use of the PCI Bus. Once PHLDA# is asserted, it cannot be negated unless PHOLD# is negated first.
SERR#	I/O	**SYSTEM ERROR.** SERR# can be pulsed active by any PCI device that detects a system error condition. Upon sampling SERR# active, PIIX4 can be programmed to generate a non-maskable interrupt (NMI) to the CPU. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z

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Name	Type	Description
STOP#	I/O	**STOP.** STOP# indicates that PIIX4, as a Target, is requesting an initiator to stop the current transaction. As an Initiator, STOP# causes PIIX4 to stop the current transaction. STOP# is an output when PIIX4 is a Target and an input when PIIX4 is an Initiator. STOP# is tri-stated from the leading edge of PCIRST#. STOP# remains tri-stated until driven by PIIX4 as a slave. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
TRDY#	I/O	**TARGET READY.** TRDY# indicates PIIX4• ability to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#. A data phase is completed when both TRDY# and IRDY# are sampled asserted. During a read, TRDY# indicates that PIIX4, as a Target, has place valid data on AD[31:0]. During a write, it indicates PIIX4, as a Target is prepared to latch data. TRDY# is an input to PIIX4 when PIIX4 is the Initiator and an output when PIIX4 is a Target. TRDY# is tri-stated from the leading edge of PCIRST#. TRDY# remains tri-stated until driven by PIIX4 as a slave. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z

NOTES:
All of the signals in the host interface are described in the Pentium Processor data sheet. The preceding table highlights PIIX4 specific uses of these signals.

2.1.2. ISA BUS INTERFACE

Name	Type	Description
AEN	O	**ADDRESS ENABLE.** AEN is asserted during DMA cycles to prevent I/O slaves from misinterpreting DMA cycles as valid I/O cycles. When negated, AEN indicates that an I/O slave may respond to address and I/O commands. When asserted, AEN informs I/O resources on the ISA bus that a DMA transfer is occurring. This signal is also driven high during PIIX4 initiated refresh cycles. **During Reset:** High-Z **After Reset:** Low **During POS:** Low
BALE	O	**BUS ADDRESS LATCH ENABLE.** BALE is asserted by PIIX4 to indicate that the address (SA[19:0], LA[23:17]) and SBHE# signal lines are valid. The LA[23:17] address lines are latched on the trailing edge of BALE. BALE remains asserted throughout DMA and ISA master cycles. **During Reset:** High-Z **After Reset:** Low **During POS:** Low
IOCHK#/I GPI0	**I/O**	**CHANNEL CHECK.** IOCHK# can be driven by any resource on the ISA bus. When asserted, it indicates that a parity or an uncorrectable error has occurred for a device or memory on the ISA bus. A NMI will be generated to the CPU if the NMI generation is enabled. If the EIO bus is used, this signal becomes a general purpose input.

Name	Type	Description
IOCHRDY	I/O	**I/O CHANNEL READY.** Resources on the ISA Bus negate IOCHRDY to indicate that wait states are required to complete the cycle. This signal is normally high. IOCHRDY is an input when PIIX4 owns the ISA Bus and the CPU or a PCI agent is accessing an ISA slave, or during DMA transfers. IOCHRDY is output when an external ISA Bus Master owns the ISA Bus and is accessing DRAM or a PIIX4 register. As a PIIX4 output, IOCHRDY is driven inactive (low) from the falling edge of the ISA commands. After data is available for an ISA master read or PIIX4 latches the data for a write cycle, IOCHRDY is asserted for 70 ns. After 70 ns, PIIX4 floats IOCHRDY. The 70 ns includes both the drive time and the time it takes PIIX4 to float IOCHRDY. PIIX4 does not drive this signal when an ISA Bus master is accessing an ISA Bus slave. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
IOCS16#	I	**16-BIT I/O CHIP SELECT.** This signal is driven by I/O devices on the ISA Bus to indicate support for 16-bit I/O bus cycles.
IOR#	I/O	**I/O READ.** IOR# is the command to an ISA I/O slave device that the slave may drive data on to the ISA data bus (SD[15:0]). The I/O slave device must hold the data valid until after IOR# is negated. IOR# is an output when PIIX4 owns the ISA Bus. IOR# is an input when an external ISA master owns the ISA Bus. **During Reset:** High-Z **After Reset:** High **During POS:** High
IOW#	I/O	**I/O WRITE.** IOW# is the command to an ISA I/O slave device that the slave may latch data from the ISA data bus (SD[15:0]). IOW# is an output when PIIX4 owns the ISA Bus. IOW# is an input when an external ISA master owns the ISA Bus. **During Reset:** High-Z **After Reset:** High **During POS:** High
LA[23:17]/ GPO[7:1]	I/O	**ISA LA[23:17].** LA[23:17] address lines allow accesses to physical memory on the ISA Bus up to 16 Mbytes. LA[23:17] are outputs when PIIX4 owns the ISA Bus. The LA[23:17] lines become inputs whenever an ISA master owns the ISA Bus. If the EIO bus is used, these signals become a general purpose output. **During Reset:** High-Z **After Reset:** Undefined **During POS:** Last LA/GPO
MEMCS16#	I/O	**MEMORY CHIP SELECT 16.** MEMCS16# is a decode of LA[23:17] without any qualification of the command signal lines. ISA slaves that are 16-bit memory devices drive this signal low. PIIX4 ignores MEMCS16# during I/O access cycles and refresh cycles. MEMCS16# is an input when PIIX4 owns the ISA Bus. PIIX4 drives this signal low during ISA master to PCI memory cycles. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
MEMR#	I/O	**MEMORY READ.** MEMR# is the command to a memory slave that it may drive data onto the ISA data bus. MEMR# is an output when PIIX4 is a master on the ISA Bus. MEMR# is an input when an ISA master, other than PIIX4, owns the ISA Bus. This signal is also driven by PIIX4 during refresh cycles. For DMA cycles, PIIX4, as a master, asserts MEMR#. **During Reset:** High-Z **After Reset:** High **During POS:** High

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Name	Type	Description
MEMW#	I/O	**MEMORY WRITE.** MEMW# is the command to a memory slave that it may latch data from the ISA data bus. MEMW# is an output when PIIX4 owns the ISA Bus. MEMW# is an input when an ISA master, other than PIIX4, owns the ISA Bus. For DMA cycles, PIIX4, as a master, asserts MEMW#. **During Reset:** High-Z **After Reset:** High **During POS:** High
REFRESH#	I/O	**REFRESH.** As an output, REFRESH# is used by PIIX4 to indicate when a refresh cycle is in progress. It should be used to enable the SA[7:0] address to the row address inputs of all banks of dynamic memory on the ISA Bus. Thus, when MEMR# is asserted, the entire expansion bus dynamic memory is refreshed. Memory slaves must not drive any data onto the bus during refresh. As an output, this signal is driven directly onto the ISA Bus. This signal is an output only when PIIX4 DMA refresh controller is a master on the bus responding to an internally generated request for refresh. As an input, REFRESH# is driven by 16-bit ISA Bus masters to initiate refresh cycles. **During Reset:** High-Z **After Reset:** High **During POS:** High
RSTDRV	O	**RESET DRIVE.** PIIX4 asserts RSTDRV to reset devices that reside on the ISA/EIO Bus. PIIX4 asserts this signal during a hard reset and during power-up. RSTDRV is asserted during power-up and negated after PWROK is driven active. RSTDRV is also driven active for a minimum of 1 ms if a hard reset has been programmed in the RC register. **During Reset:** High **After Reset:** Low **During POS:** Low
SA[19:0]	I/O	**SYSTEM ADDRESS[19:0].** These bi-directional address lines define the selection with the granularity of 1 byte within the 1-Megabyte section of memory defined by the LA[23:17] address lines. The address lines SA[19:17] that are coincident with LA[19:17] are defined to have the same values as LA[19:17] for all memory cycles. For I/O accesses, only SA[15:0] are used, and SA[19:16] are undefined. SA[19:0] are outputs when PIIX4 owns the ISA Bus. SA[19:0] are inputs when an external ISA Master owns the ISA Bus. **During Reset:** High-Z **After Reset:** Undefined **During POS:** Last SA
SBHE#	I/O	**SYSTEM BYTE HIGH ENABLE.** SBHE# indicates, when asserted, that a byte is being transferred on the upper byte (SD[15:8]) of the data bus. SBHE# is negated during refresh cycles. SBHE# is an output when PIIX4 owns the ISA Bus. SBHE# is an input when an external ISA master owns the ISA Bus. **During Reset:** High-Z **After Reset:** Undefined **During POS:** High
SD[15:0]	I/O	**SYSTEM DATA.** SD[15:0] provide the 16-bit data path for devices residing on the ISA Bus. SD[15:8] correspond to the high order byte and SD[7:0] correspond to the low order byte. SD[15:0] are undefined during refresh. **During Reset:** High-Z **After Reset:** Undefined **During POS:** High-Z
SMEMR#	O	**STANDARD MEMORY READ.** PIIX4 asserts SMEMR# to request an ISA memory slave to drive data onto the data lines. If the access is below the 1-Mbyte range (00000000h?00FFFFFh) during DMA compatible, PIIX4 master, or ISA master cycles, PIIX4 asserts SMEMR#. SMEMR# is a delayed version of MEMR#. **During Reset:** High-Z **After Reset:** High **During POS:** High

Name	Type	Description
SMEMW#	O	**STANDARD MEMORY WRITE.** PIIX4 asserts SMEMW# to request an ISA memory slave to accept data from the data lines. If the access is below the 1-Mbyte range (00000000h?00FFFFFh) during DMA compatible, PIIX4 master, or ISA master cycles, PIIX4 asserts SMEMW#. SMEMW# is a delayed version of MEMW#. **During Reset:** High-Z **After Reset:** High **During POS:** High
ZEROWS#	I	**ZERO WAIT STATES.** An ISA slave asserts ZEROWS# after its address and command signals have been decoded to indicate that the current cycle can be shortened. A 16-bit ISA memory cycle can be reduced to two SYSCLKs. An 8-bit memory or I/O cycle can be reduced to three SYSCLKs. ZEROWS# has no effect during 16-bit I/O cycles. If IOCHRDY is negated and ZEROWS# is asserted during the same clock, then ZEROWS# is ignored and wait states are added as a function of IOCHRDY.

2.1.3. X-BUS INTERFACE

Name	Type	Description
A20GATE	I	**ADDRESS 20 GATE.** This input from the keyboard controller is logically combined with bit 1 (FAST_A20) of the Port 92 Register, which is then output via the A20M# signal.
BIOSCS#	O	**BIOS CHIP SELECT.** This chip select is driven active during read or write accesses to enabled BIOS memory ranges. BIOSCS# is driven combinatorially from the ISA addresses SA[16:0] and LA[23:17], except during DMA cycles. During DMA cycles, BIOSCS# is not generated. **During Reset:** High **After Reset:** High **During POS:** High
KBCCS#/ GPO26	O	**KEYBOARD CONTROLLER CHIP SELECT.** KBCCS# is asserted during I/O read or write accesses to KBC locations 60h and 64h. It is driven combinatorially from the ISA addresses SA[19:0] and LA[23:17]. If the keyboard controller does not require a separate chip select, this signal can be programmed to a general purpose output. **During Reset:** High **After Reset:** High **During POS:** High/GPO
MCCS#	O	**MICROCONTROLLER CHIP SELECT.** MCCS# is asserted during I/O read or write accesses to IO locations 62h and 66h. It is driven combinatorially from the ISA addresses SA[19:0] and LA[23:17]. **During Reset:** High **After Reset:** High **During POS:** High
PCS0# **PCS1#**	O	**PROGRAMMABLE CHIP SELECTS.** These active low chip selects are asserted for ISA I/O cycles which are generated by PCI masters and which hit the programmable I/O ranges defined in the Power Management section. The X-Bus buffer signals (XOE# and XDIR#) are enabled while the chip select is active. (i.e., it is assumed that the peripheral which is selected via this pin resides on the X-Bus.) **During Reset:** High **After Reset:** High **During POS:** High
RCIN#	I	**RESET CPU.** This signal from the keyboard controller is used to generate an INIT signal to the CPU.

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Name	Type	Description
RTCALE/	O	**REAL TIME CLOCK ADDRESS LATCH ENABLE.** RTCALE is used to latch the GPO25appropriate memory address into the RTC. A write to port 70h with the appropriate RTC memory address that will be written to or read from causes RTCALE to be asserted. RTCALE is asserted on falling IOW# and remains asserted for two SYSCLKs. If the internal Real Time Clock is used, this signal can be programmed as a general purpose output. **During Reset:** Low **After Reset:** Low **During POS:** Low/GPO
RTCCS#/ GPO24	O	**REAL TIME CLOCK CHIP SELECT.** RTCCS# is asserted during read or write I/O accesses to RTC location 71h. RTCCS# can be tied to a pair of external OR gates to generate the real time clock read and write command signals. If the internal Real Time Clock is used, this signal can be programmed as a general purpose output. **During Reset:** High **After Reset:** High **During POS:** High/GPO
XDIR#/ GPO22	O	**X-BUS TRANSCEIVER DIRECTION.** XDIR# is tied directly to the direction control of a 74?45 that buffers the X-Bus data, XD[7:0]. XDIR# is asserted (driven low) for all I/O read cycles regardless if the accesses is to a PIIX4 supported device. XDIR# is asserted for memory cycles only if BIOS or APIC space has been decoded. For PCI master initiated read cycles, XDIR# is asserted from the falling edge of either IOR# or MEMR# (from MEMR# only if BIOS or APIC space has been decoded), depending on the cycle type. For ISA master-initiated read cycles, XDIR# is asserted from the falling edge of either IOR# or MEMR# (from MEMR# only if BIOS space has been decoded), depending on the cycle type. When the rising edge of IOR# or MEMR# occurs, PIIX4 negates XDIR#. For DMA read cycles from the X-Bus, XDIR# is driven low from DACKx# falling and negated from DACKx# rising. At all other times, XDIR# is negated high. If the X-Bus not used, then this signal can be programmed to be a general purpose output. **During Reset:** High **After Reset:** High **During POS:** High/GPO
XOE#/ GPO23	O	**X-BUS TRANSCEIVER OUTPUT ENABLE.** XOE# is tied directly to the output enable of a 74?45 that buffers the X-Bus data, XD[7:0], from the system data bus, SD[7:0]. XOE# is asserted anytime a PIIX4 supported X-Bus device is decoded, and the devices decode is enabled in the X-Bus Chip Select Enable Register (BIOSCS#, KBCCS#, RTCCS#, MCCS#) or the Device Resource B (PCCS0#) and Device Resource C (PCCS1#). XOE# is asserted from the falling edge of the ISA commands (IOR#, IOW#, MEMR#, or MEMW#) for PCI Master and ISA master-initiated cycles. XOE# is negated from the rising edge of the ISA command signals for PCI Master initiated cycles and the SA[16:0] and LA[23:17] address for ISA master-initiated cycles. XOE# is not generated during any access to an X-Bus peripheral in which its decode space has been disabled. If an X-Bus not used, then this signal can be programmed to be a general purpose output. **During Reset:** High **After Reset:** High **During POS:** High/GPO

2.1.4. DMA SIGNALS

Name	Type	Description
DACK[0,1,2,3]# DACK[5,6,7]#	O	**DMA ACKNOWLEDGE.** The DACK# output lines indicate that a request for DMA service has been granted by PIIX4 or that a 16-bit master has been granted the bus. The active level (high or low) is programmed via the DMA Command Register. These lines should be used to decode the DMA slave device with the IOR# or IOW# line to indicate selection. If used to signal acceptance of a bus master request, this signal indicates when it is legal to assert MASTER#. If the DREQ goes inactive prior to DACK# being asserted, the DACK# signal will not be asserted. **During Reset:** High **After Reset:** High **During POS:** High
DREQ[0,1,2,3] DREQ[5,6,7]	I	**DMA REQUEST.** The DREQ lines are used to request DMA service from PIIX4 DMA controller or for a 16-bit master to gain control of the ISA expansion bus. The active level (high or low) is programmed via the DMA Command Register. All inactive to active edges of DREQ are assumed to be asynchronous. The request must remain active until the appropriate DACKx# signal is asserted.
REQ[A:C]#/ GPI[2:4]	I	**PC/PCI DMA REQUEST.** These signals are the DMA requests for PC/PCI protocol. They are used by a PCI agent to request DMA services and follow the PCI Expansion Channel Passing protocol as defined in the *PCI DMA* section. If the PC/PCI request is not needed, these pins can be used as general-purpose inputs.
GNT[A:C]#/ GPO[9:11]	O	**PC/PCI DMA ACKNOWLEDGE.** These signals are the DMA grants for PC/PCI protocol. They are used by a PIIX4 to acknowledge DMA services and follow the PCI Expansion Channel Passing protocol as defined in the *PCI DMA* section. If the PC/PCI request is not needed, these pins can be used as general-purpose outputs. **During Reset:** High **After Reset:** High **During POS:** High/GPO
TC	O	**TERMINAL COUNT.** PIIX4 asserts TC to DMA slaves as a terminal count indicator. PIIX4 asserts TC after a new address has been output, if the byte count expires with that transfer. TC remains asserted until AEN is negated, unless AEN is negated during an autoinitialization. TC is negated before AEN is negated during an autoinitialization. **During Reset:** Low **After Reset:** Low **During POS:** Low

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2.1.5. INTERRUPT CONTROLLER/APIC SIGNALS

Name	Type	Description
APICACK#/ GPO12	O	**APIC ACKNOWLEDGE.** This active low output signal is asserted by PIIX4 after its internal buffers are flushed in response to the APICREQ# signal. When the I/O APIC samples this signal asserted it knows that PIIX4• buffers are flushed and that it can proceed to send the APIC interrupt. The APICACK# output is synchronous to PCICLK. If the external APIC is not used, then this is a general-purpose output. **During Reset:** High **After Reset:** High **During POS:** High/GPO
APICCS#/ GPO13	O	**APIC CHIP SELECT.** This active low output signal is asserted when the APIC Chip Select is enabled and a PCI originated cycle is positively decoded within the programmed I/O APIC address space. If the external APIC is not used, this pin is a general-purpose output. **During Reset:** High **After Reset:** High **During POS:** High/GPO
APICREQ#/ GPI5	I	**APIC REQUEST.** This active low input signal is asserted by an external APIC device prior to sending an interrupt over the APIC serial bus. When PIIX4 samples this pin active it will flush its F-type DMA buffers pointing towards PCI. Once the buffers are flushed, PIIX4 asserts APICACK# which indicates to the external APIC that it can proceed to send the APIC interrupt. The APICREQ# input must be synchronous to PCICLK. If the external APIC is not used, this pin is a general-purpose input. **INTR** OD **INTERRUPT.** See CPU Interface Signals.
IRQ0/	O	**INTERRUPT REQUEST 0.** This output reflects the state of the internal IRQ0 signal GPO14 from the system timer. If the external APIC is not used, this pin is a general-purpose output. **During Reset:** Low **After Reset:** Low **During POS:** IRQ0/GPO
IRQ1	I	**INTERRUPT REQUEST 1.** IRQ1 is always edge triggered and can not be modified by software to level sensitive. A low to high transition on IRQ1 is latched by PIIX4. IRQ1 must remain asserted until after the interrupt is acknowledged. If the input goes inactive before this time, a default IRQ7 is reported in response to the interrupt acknowledge cycle.
IRQ 3:7, 9:11, 14:15	I	**INTERRUPT REQUESTS 3:7, 9:11, 14:15.** The IRQ signals provide both system board components and ISA Bus I/O devices with a mechanism for asynchronously interrupting the CPU. These interrupts may be programmed for either an edge sensitive or a high level sensitive assertion mode. Edge sensitive is the default configuration. An active IRQ input must remain asserted until after the interrupt is acknowledged. If the input goes inactive before this time, a default IRQ7 is reported in response to the interrupt acknowledge cycle.

Name	Type	Description
IRQ8#/ GPI6	I/O	**IRQ 8#.** IRQ8# is always an active low edge triggered interrupt and can not be modified by software. IRQ8# must remain asserted until after the interrupt is acknowledged. If the input goes inactive before this time, a default IRQ7 is reported in response to the interrupt acknowledge cycle. If using the internal RTC, then this can be programmed as a general-purpose input. If enabling an APIC, this signal becomes an output and must not be programmed as a general purpose input.
IRQ9OUT#/ GPO29	O	**IRQ9OUT#.** IRQ9OUT# is used to route the internally generated SCI and SMBus interrupts out of the PIIX4 for connection to an external IO APIC. If APIC is disabled, this signal pin is a General Purpose Output. **During Reset:** High **After Reset:** High **During POS:** IRQ9OUT#/GPO
IRQ 12/M	I	**INTERRUPT REQUEST 12.** In addition to providing the standard interrupt function as described in the pin description for IRQ[3:7,9:11,14:15], this pin can also be programmed to provide the mouse interrupt function. When the mouse interrupt function is selected, a low to high transition on this signal is latched by PIIX4 and an INTR is generated to the CPU as IRQ12. An internal IRQ12 interrupt continues to be generated until a Reset or an I/O read access to address 60h (falling edge of IOR#) is detected.
PIRQ[A:D]#	I/OD PCI	**PROGRAMMABLE INTERRUPT REQUEST.** The PIRQx# signals are active low, level sensitive, shareable interrupt inputs. They can be individually steered to ISA interrupts IRQ [3:7,9:12,14:15]. The USB controller uses PIRQD# as its output signal.
SERIRQ/ GPI7	I/O	**SERIAL INTERRUPT REQUEST.** Serial interrupt input decoder, typically used in conjunction with the Distributed DMA protocol. If not using serial interrupts, this pin can be used as a general-purpose input.

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E

2.1.6. CPU INTERFACE SIGNALS

Name	Type	Description
A20M#	OD	**ADDRESS 20 MASK.** PIIX4 asserts A20M# to the CPU based on combination of Port 92 Register, bit 1 (FAST_A20), and A20GATE input signal. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
CPURST	OD	**CPU RESET.** PIIX4 asserts CPURST to reset the CPU. PIIX4 asserts CPURST during power-up and when a hard reset sequence is initiated through the RC register. CPURST is driven inactive a minimum of 2 ms after PWROK is driven active. CPURST is driven active for a minimum of 2 ms when initiated through the RC register. The inactive edge of CPURST is driven synchronously to the rising edge of PCICLK. If a hard reset is initiated through the RC register, PIIX4 resets its internal registers (in both core and suspend wells) to their default state. This signal is active high for Pentium processor and active-low for Pentium II processor as determined by CONFIG1 signal. For values **During Reset**, **After Reset**, and **During POS**, see the *Suspend/Resume and Resume Control Signaling* section.
FERR#	I	**NUMERIC COPROCESSOR ERROR.** This pin functions as a FERR# signal supporting coprocessor errors. This signal is tied to the coprocessor error signal on the CPU. If FERR# is asserted, PIIX4 generates an internal IRQ13 to its interrupt controller unit. PIIX4 then asserts the INT output to the CPU. FERR# is also used to gate the IGNNE# signal to ensure that IGNNE# is not asserted to the CPU unless FERR# is active.
IGNNE#	OD	**IGNORE NUMERIC EXCEPTION.** This signal is connected to the ignore numeric exception pin on the CPU. IGNNE# is only used if the PIIX4 coprocessor error reporting function is enabled. If FERR# is active, indicating a coprocessor error, a write to the Coprocessor Error Register (F0h) causes the IGNNE# to be asserted. IGNNE# remains asserted until FERR# is negated. If FERR# is not asserted when the Coprocessor Error Register is written, the IGNNE# signal is not asserted. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
INIT	OD	**INITIALIZATION.** INIT is asserted in response to any one of the following conditions. When the System Reset bit in the Reset Control Register is reset to 0 and the Reset CPU bit toggles from 0 to 1, PIIX4 initiates a soft reset by asserting INIT. PIIX4 also asserts INIT if a Shut Down Special cycle is decoded on the PCI Bus, if the RCIN# signal is asserted, or if a write occurs to Port 92h, bit 0. When asserted, INIT remains asserted for approximately 64 PCI clocks before being negated. This signal is active high for Pentium processor and active-low for Pentium II processor as determined by CONFIG1 signal. **Pentium Processor:** **During Reset:** Low **After Reset:** Low **During POS:** Low **Pentium II Processor:** **During Reset:** High **After Reset:** High **During POS:** High
INTR	OD	**CPU INTERRUPT.** INTR is driven by PIIX4 to signal the CPU that an interrupt request is pending and needs to be serviced. It is asynchronous with respect to SYSCLK or PCICLK and is always an output. The interrupt controller must be programmed following PCIRST# to ensure that INTR is at a known state. **During Reset:** Low **After Reset:** Low **During POS:** Low

Name	Type	Description
NMI	OD	**NON-MASKABLE INTERRUPT.** NMI is used to force a nonmaskable interrupt to the CPU. PIIX4 generates an NMI when either SERR# or IOCHK# is asserted, depending on how the NMI Status and Control Register is programmed. The CPU detects an NMI when it detects a rising edge on NMI. After the NMI interrupt routine processes the interrupt, the NMI status bits in the NMI Status and Control Register are cleared by software. The NMI interrupt routine must read this register to determine the source of the interrupt. The NMI is reset by setting the corresponding NMI source enable/disable bit in the NMI Status and Control Register. To enable NMI interrupts, the two NMI enable/disable bits in the register must be set to 0, and the NMI mask bit in the NMI Enable/Disable and Real Time Clock Address Register must be set to 0. Upon PCIRST#, this signal is driven low. **During Reset:** Low **After Reset:** Low **During POS:** Low
SLP#	OD	**SLEEP.** This signal is output to the Pentium II processor in order to put it into Sleep state. For Pentium processor it is a No Connect. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
SMI#	OD	**SYSTEM MANAGEMENT INTERRUPT.** SMI# is an active low synchronous output that is asserted by PIIX4 in response to one of many enabled hardware or software events. The CPU recognizes the falling edge of SMI# as the highest priority interrupt in the system, with the exception of INIT, CPURST, and FLUSH. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
STPCLK#	OD	**STOP CLOCK.** STPCLK# is an active low synchronous output that is asserted by PIIX4 in response to one of many hardware or software events. STPCLK# connects directly to the CPU and is synchronous to PCICLK. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z

5.4 INTEL FW82371AB PCI/ISA BRIDGE (PIIX4)-7

2.1.7. CLOCKING SIGNALS

Name	Type	Description
CLK48	I	**48-MHZ CLOCK.** 48-MHz clock used by the internal USB host controller. This signal may be stopped during suspend modes.
PCICLK	I	**FREE-RUNNING PCI CLOCK.** A clock signal running at 30 or 33 MHz, PCICLK provides timing for all transactions on the PCI Bus. All other PCI signals are sampled on the rising edge of PCICLK, and all timing parameters are defined with respect to this edge. Because many of the circuits in PIIX4 run off the PCI clock, this signal MUST be kept active, even if the PCI bus clock is not active.
OSC	I	**14.31818-MHZ CLOCK.** Clock signal used by the internal 8254 timer. This clock signal may be stopped during suspend modes.
RTCX1, RTCX2	I/O	**RTC CRYSTAL INPUTS:** These connected directly to a 32.768-kHz crystal. External capacitors are required. These clock inputs are required even if the internal RTC is not being used.
SUSCLK	O	**SUSPEND CLOCK.** 32.768-kHz output clock provided to the Host-to-PCI bridge used for maintenance of DRAM refresh. This signal is stopped during Suspend-to-Disk and Soft Off modes. For values During Reset, After Reset, and During POS, see the *Suspend/Resume and Resume Control Signaling* section.
SYSCLK	O	**ISA SYSTEM CLOCK.** SYSCLK is the reference clock for the ISA bus. It drives the ISA bus directly. The SYSCLK is generated by dividing PCICLK by 4. The SYSCLK frequencies supported are 7.5 MHz and 8.33 MHz. For PCI accesses to the ISA bus, SYSCLK may be stretched low to synchronize BALE falling to the rising edge of SYSCLK. **During Reset:** Running **After Reset:** Running **During POS:** Low

2.1.8. IDE SIGNALS

Name	Type	Description
PDA[2:0]	O	**PRIMARY DISK ADDRESS[2:0].** These signals indicate which byte in either the ATA command block or control block is being addressed. If the IDE signals are configured for Primary and Secondary, these signals are connected to the corresponding signals on the Primary IDE connector. If the IDE signals are configured for Primary 0 and Primary 1, these signals are used for the Primary 0 connector. **During Reset:** High-Z **After Reset:** Undefined **During POS:** PDA
PDCS1#	O	**PRIMARY DISK CHIP SELECT FOR 1F0H- -1F7H RANGE.** For ATA command register block. If the IDE signals are configured for Primary and Secondary, this output signal is connected to the corresponding signal on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector. **During Reset:** High **After Reset:** High **During POS:** High
PDCS3#	O	**PRIMARY DISK CHIP SELECT FOR 3F0- -3F7 RANGE.** For ATA control register block. If the IDE signals are configured for Primary and Secondary, this output signal is connected to the corresponding signal on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector. **During Reset:** High **After Reset:** High **During POS:** High
PDD[15:0]	I/O	**PRIMARY DISK DATA[15:0].** These signals are used to transfer data to or from the IDE device. If the IDE signals are configured for Primary and Secondary, these signals are connected to the corresponding signals on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector. **During Reset:** High-Z **After Reset:** Undefined**During POS:** PDD
PDDACK#	O	**PRIMARY DMA ACKNOWLEDGE.** This signal directly drives the IDE device DMACK# signal. It is asserted by PIIX4 to indicate to IDE DMA slave devices that a given data transfer cycle (assertion of PDIOR# or PDIOW#) is a DMA data transfer cycle. This signal is used in conjunction with the PCI bus master IDE function. It is not associated with any AT compatible DMA channel. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector. **During Reset:** High **After Reset:** High **During POS:** High
PDDREQ	I	**PRIMARY DISK DMA REQUEST.** This input signal is directly driven from the IDE device DMARQ signal. It is asserted by the IDE device to request a data transfer, and used in conjunction with the PCI bus master IDE function. It is not associated with any AT compatible DMA channel. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector.

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Name	Type	Description
PDIOR#	O	**PRIMARY DISK IO READ.** In normal IDE this is the command to the IDE device that it may drive data onto the PDD[15:0] lines. Data is latched by PIIX4 on the negation edge of PDIOR#. The IDE device is selected either by the ATA register file chip selects (PDCS1#, PDCS3#) and the PDA[2:0] lines, or the IDE DMA slave arbitration signals (PDDACK#). In an Ultra DMA/33 read cycle, this signal is used as DMARDY# which is negated by the PIIX4 to pause Ultra DMA/33 transfers. In an Ultra DMA/33 write cycle, this signal is used as the STROBE signal, with the drive latching data on rising and falling edges of STROBE. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector. **During Reset:** High **After Reset:** High **During POS:** High
PDIOW#	O	**PRIMARY DISK IO WRITE.** In normal IDE mode, this is the command to the IDE device that it may latch data from the PDD[15:0] lines. Data is latched by the IDE device on the negation edge of PDIOW#. The IDE device is selected either by the ATA register file chip selects (PDCS1#, PDCS3#) and the PDA[2:0] lines, or the IDE DMA slave arbitration signals (PDDACK#). For Ultra DMA/33 mode, this signal is used as the STOP signal, which is used to terminate an Ultra DMA/33 transaction. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector. **During Reset:** High **After Reset:** High **During POS:** High-Z
PIORDY	I	**PRIMARY IO CHANNEL READY.** In normal IDE mode, this input signal is directly driven by the corresponding IDE device IORDY signal. In an Ultra DMA/33 read cycle, this signal is used as STROBE, with the PIIX4 latching data on rising and falling edges of STROBE. In an Ultra DMA/33 write cycle, this signal is used as the DMARDY# signal which is negated by the drive to pause Ultra DMA/33 transfers. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Primary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, this signal is used for the Primary Master connector. This is a Schmitt triggered input.

Name	Type	Description
SDA[2:0]	O	**SECONDARY DISK ADDRESS[2:0].** These signals indicate which byte in either the ATA command block or control block is being addressed. If the IDE signals are configured for Primary and Secondary, these signals are connected to the corresponding signals on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector. **During Reset:** High-Z **After Reset:** Undefined **During POS:** SDA
SDCS1#	O	**SECONDARY CHIP SELECT FOR 170H- -177H RANGE.** For ATA command register block. If the IDE signals are configured for Primary and Secondary, this output signal is connected to the corresponding signal on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector. **During Reset:** High **After Reset:** High **During POS:** High
SDCS3#	O	**SECONDARY CHIP SELECT FOR 370H- -377H RANGE.** For ATA control register block. If the IDE signals are configured for Primary and Secondary, this output signal is connected to the corresponding signal on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector. **During Reset:** High **After Reset:** High **During POS:** High-Z
SDD[15:0]	I/O	**SECONDARY DISK DATA[15:0].** These signals are used to transfer data to or from the IDE device. If the IDE signals are configured for Primary and Secondary, these signals are connected to the corresponding signals on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector. **During Reset:** High-Z **After Reset:** Undefined **During POS:** SDD
SDDACK#	O	**SECONDARY DMA ACKNOWLEDGE.** This signal directly drives the IDE device DMACK# signal. It is asserted by PIIX4 to indicate to IDE DMA slave devices that a given data transfer cycle (assertion of SDIOR# or SDIOW#) is a DMA data transfer cycle. This signal is used in conjunction with the PCI bus master IDE function. It is not associated with any AT compatible DMA channel. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector. **During Reset:** High **After Reset:** High **During POS:** High

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Name	Type	Description
SDDREQ	I	**SECONDARY DISK DMA REQUEST.** This input signal is directly driven from the IDE device DMARQ signal. It is asserted by the IDE device to request a data transfer, and used in conjunction with the PCI bus master IDE function. It is not associated with any AT compatible DMA channel. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector.
SDIOR#	O	**SECONDARY DISK IO READ.** In normal IDE mode, this is the command to the IDE device that it may drive data onto the SDD[15:0] lines. Data is latched by the PIIX4 on the negation edge of SDIOR#. The IDE device is selected either by the ATA register file chip selects (SDCS1#, SDCS3#) and the SDA[2:0] lines, or the IDE DMA slave arbitration signals (SDDACK#). In an Ultra DMA/33 read cycle, this signal is used as DMARDY# which is negated by the PIIX4 to pause Ultra DMA/33 transfers. In an Ultra DMA/33 write cycle, this signal is used as the STROBE signal, with the drive latching data on rising and falling edges of STROBE. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector. **During Reset:** High **After Reset:** High **During POS:** High
SDIOW#	O	**SECONDARY DISK IO WRITE.** In normal IDE mode, this is the command to the IDE device that it may latch data from the SDD[15:0] lines. Data is latched by the IDE device on the negation edge of SDIOW#. The IDE device is selected either by the ATA register file chip selects (SDCS1#, SDCS3#) and the SDA[2:0] lines, or the IDE DMA slave arbitration signals (SDDACK#). In read and write cycles this signal is used as the STOP signal, which is used to terminate an Ultra DMA/33 transaction. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector. **During Reset:** High **After Reset:** High **During POS:** High
SIORDY	I	**SECONDARY IO CHANNEL READY.** In normal IDE mode, this input signal is directly driven by the corresponding IDE device IORDY signal. In an Ultra DMA/33 read cycle, this signal is used as STROBE, with the PIIX4 latching data on rising and falling edges of STROBE. In an Ultra DMA write cycle, this signal is used as the DMARDY# signal which is negated by the drive to pause Ultra DMA/33 transfers. If the IDE signals are configured for Primary and Secondary, this signal is connected to the corresponding signal on the Secondary IDE connector. If the IDE signals are configured for Primary Master and Primary Slave, these signals are used for the Primary Slave connector. This is a Schmitt triggered input.

2.1.9. UNIVERSAL SERIAL BUS SIGNALS

Name	Type	Description
OC[1:0]#	I	**OVER CURRENT DETECT.** These signals are used to monitor the status of the USB power supply lines. The corresponding USB port is disabled when its over current signal is asserted.
USBP0+, USBP0-	I/O	**SERIAL BUS PORT 0.** This signal pair comprises the differential data signal for USB port 0. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
USBP1+, USBP1	I/O	**SERIAL BUS PORT 1.** This signal pair comprises the differential data signal for USB port 1. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z

2.1.10. POWER MANAGEMENT SIGNALS

Name	Type	Description
BATLOW#/ GPI9	I	**BATTERY LOW.** Indicates that battery power is low. PIIX4 can be programmed to prevent a resume operation when the BATLOW# signal is asserted. If the Battery Low function is not needed, this pin can be used as a general-purpose input.
CPU_STP#/ GPO17	O	**CPU CLOCK STOP.** Active low control signal to the clock generator used to disable the CPU clock outputs. If this function is not needed, then this signal can be used as a general-purpose output. For values **During Reset**, **After Reset**, and **During POS**, see the *Suspend/Resume and Resume Control Signaling* section.
EXTSMI#	I/OD	**EXTERNAL SYSTEM MANAGEMENT INTERRUPT.** EXTSMI# is a falling edge triggered input to PIIX4 indicating that an external device is requesting the system to enter SMM mode. When enabled, a falling edge on EXTSMI# results in the assertion of the SMI# signal to the CPU. EXTSMI# is an asynchronous input to PIIX4. However, when the setup and hold times are met, it is only required to be asserted for one PCICLK. Once negated EXTSMI# must remain negated for at least four PCICLKs to allow the edge detect logic to reset. EXTSMI# is asserted by PIIX4 in response to SMI# being activated within the Serial IRQ function. An external pull-up should be placed on this signal.
LID/ GPI10	I	**LID INPUT.** This signal can be used to monitor the opening and closing of the display lid of a notebook computer. It can be used to detect both low to high transition or a high to low transition and these transitions will generate an SMI# if enabled. This input contains logic to perform a 16-ms debounce of the input signal. If the LID function is not needed, this pin can be used as a general-purpose input.

5.4 INTEL FW82371AB PCI/ISA BRIDGE (PIIX4)-10

Name	Type	Description
PCIREQ[A:D]#	I	**PCI REQUEST.** Power Management input signals used to monitor PCI Master Requests for use of the PCI bus. They are connected to the corresponding REQ[0:3]# signals on the Host Bridge.
PCI_STP#/	O	**PCI CLOCK STOP.** Active low control signal to the clock generator used to disable GPO18the PCI clock outputs. The PIIX4 free running PCICLK input must remain on. If this function is not needed, this pin can be used as a general-purpose output. For values **During Reset**, **After Reset**, and **During POS**, see the *Suspend/Resume and Resume Control Signaling* section.
PWRBTN#	I	**POWER BUTTON.** Input used by power management logic to monitor external system events, most typically a system on/off button or switch. This input contains logic to perform a 16-ms debounce of the input signal.
RI# GPI12	I	**RING INDICATE.** Input used by power management logic to monitor external system events, most typically used for wake up from a modem. If this function is not needed, then this signal can be individually used as a general-purpose input.
RSMRST#	I	**RESUME RESET.** This signal resets the internal Suspend Well power plane logic and portions of the RTC well logic.
SMBALERT#/	I	**SM BUS ALERT.** Input used by System Management Bus logic to generate an GPI11interrupt (IRQ or SMI) or power management resume event when enabled. If this function is not needed, this pin can be used as a general-purpose input.
SMBCLK	I/O	**SM BUS CLOCK.** System Management Bus Clock used to synchronize transfer of data on SMBus. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
SMBDATA	I/O	**SM BUS DATA.** Serial data line used to transfer data on SMBus. **During Reset:** High-Z **After Reset:** High-Z **During POS:** High-Z
SUSA#	O	**SUSPEND PLANE A CONTROL.** Control signal asserted during power management suspend states. SUSA# is primarily used to control the primary power plane. This signal is asserted during POS, STR, and STD suspend states. **During Reset:** Low **After Reset:** High **During POS:** Low
SUSB#/ GPO15	O	**SUSPEND PLANE B CONTROL.** Control signal asserted during power management suspend states. SUSB# is primarily used to control the secondary power plane. This signal is asserted during STR and STD suspend states. If the power plane control is not needed, this pin can be used as a general-purpose output. **During Reset:** Low **After Reset:** High **During POS:** High/GPO

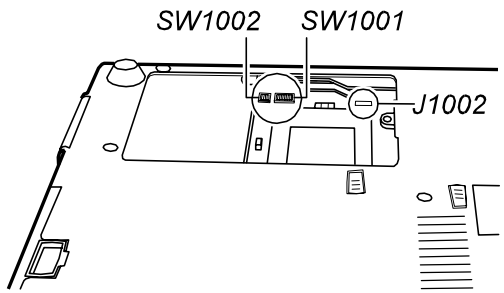
Name	Type	Description
SUSC#/	O	**SUSPEND PLANE C CONTROL.** Control signal asserted during power GPO16management suspend states, primarily used to control the tertiary power plane. It is asserted only during STD suspend state. If the power plane control is not needed, this pin can be used as a general-purpose output. **During Reset:** Low **After Reset:** High **During POS:** High/GPO
SUS_STAT1#/	O	**SUSPEND STATUS 1.** This signal is typically connected to the Host-to-PCI bridge GPO20and is used to provide information on host clock status. SUS_STAST1# is asserted when the system may stop the host clock, such as Stop Clock or during POS, STR,and STD suspend states. If this function is not needed, this pin can be used as a general-purpose output. **During Reset:** Low **After Reset:** High **During POS:** Low/GPO
SUS_STAT2#/	O	**SUSPEND STATUS 2.** This signal will typically connect to other system peripherals GPO21and is used to provide information on system suspend state. It is asserted during POS, STR, and STD suspend states. If this function is not needed, this pin can be used as a general-purpose output. **During Reset:** Low **After Reset:** High **During POS:** Low/GPO
THRM#/	I	**THERMAL DETECT.** Active low signal generated by external hardware to start the GPI8Hardware Clock Throttling mode. If enabled, the external hardware can force the system to enter into Hardware Clock Throttle mode by asserting THRM#. This causes PIIX4 to cycle STPCLK# at a preset programmable rate. If this function is not needed, this pin can be used as a general-purpose input.
ZZ/	O	**LOW-POWER MODE FOR L2 CACHE SRAM.** This signal is used to power down a GPO19cache• data SRAMs when the clock logic places the CPU into the Stop Clock. If this function is not needed, this pin can be used as a general-purpose output. **During Reset:** Low **After Reset:** Low **During POS:** Low

2.1.11. GENERAL PURPOSE INPUT AND OUTPUT SIGNALS

Some of the General Purpose Input and Output signals are multiplexed with other PIIX4 signals. The usage is determined by the system configuration.
The default pin usage is shown in Table 1 and Table 2. The configuration can be selected via the General Configuration register and X-Bus Chip Select register.

Name	Type	Description
GPI[21:0]	I	**GENERAL PURPOSE INPUTS.** These input signals can be monitored via the GPIREG register located in Function 3 (Power Management) System IO Space at address PMBase+30h. See Table 1 for details.

6.SWITCH & JUMPERS SETTING



Note: To access the switches, you need to remove the CPU cooling fan.

Voltage	SW1002			
	Pin 1	Pin 2	Pin 3	Pin 4
1.8	OFF	OFF	OFF	OFF
1.9	OFF	OFF	OFF	ON
2.0	OFF	OFF	ON	OFF
2.1	OFF	OFF	ON	ON
2.2	OFF	ON	OFF	OFF
2.3	OFF	ON	OFF	ON
2.4	OFF	ON	ON	OFF
2.5	OFF	ON	ON	ON
2.6	ON	OFF	OFF	OFF
2.7	ON	OFF	OFF	ON
2.8	ON	OFF	ON	OFF
2.9	ON	OFF	ON	ON
3.0	ON	ON	OFF	OFF
3.1	ON	ON	OFF	ON
3.2	ON	ON	ON	OFF
3.3	ON	ON	ON	ON

CPU	SW1001						J1002
	Pin 1	Pin 2	Pin 3	Pin 4	Pin 6	Pin 7	
P55CLM-166	OFF	ON	ON	ON	OFF	ON	1-2
P55CLM-200	OFF	OFF	ON	ON	OFF	ON	1-2
Tillamook-200	OFF	OFF	ON	ON	ON	OFF	2-3
Tillamook-233	OFF	OFF	OFF	ON	ON	OFF	2-3

	SW1001
	Pin 5
Normal	ON
Clear RTC*	OFF

* **Note:** Make sure the AC adapter is not connected when you clear RTC.

5031 M/B MAINTENANCE

7.ASSEMBLY & DISASSEMBLY

7.1 SYSTEM VIEW

7.1.1 RIGHT-SIDE VIEW
7.1.2 LEFT-SIDE VIEW
7.1.3 REAR VIEW
7.1.4 FRONT VIEW
7.1.5 BOTTOM VIEW

7.2 SYSTEM DISASSEMBLY

MODULAR COMPONENTS

7.2.1 RIGHT/LEFT BAY DEVICE
7.2.2 HARD DISK DRIVE
7.2.3 CPU
7.2.4 FAX/ MODEM/ VOICE CARD
7.2.5 KEYBOARD
7.2.6 MEMORY MODULE

LCD ASSEMBLY COMPONENTS

7.2.7 LCD ASSEMBLY
7.2.8 LCD PANEL
7.2.9 INVERTER BOARD

BASE UNIT COMPONENTS

7.2.10 BOTTOM CHASSIS
7.2.11 D/D BOARD
7.2.12 VIDEO CAPTURE BOARD
7.2.13 SYSTEM BOARD
7.2.14 TOUCH-PAD BOARD

7.ASSEMBLY & DISASSEMBLY

7.1 SYSTEM VIEW

7.1.1 RIGHT-SIDE VIEW

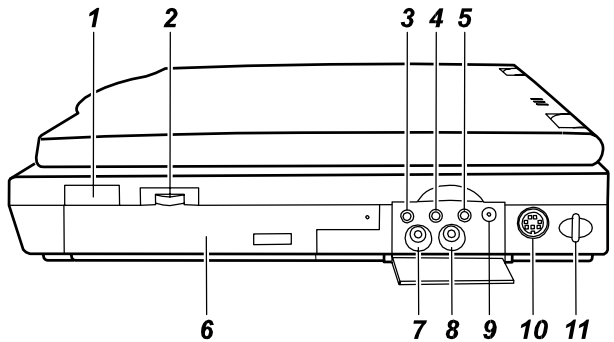


Figure 7-1. Right-Side View

1. **IR Port**
2. **Volume Control**
3. **Audio Input Connector**
4. **Audio Output Connector**
5. **Microphone Connector**
6. **CD-ROM Drive**
7. **Video Out Connector**
8. **Video In Connector**
9. **5V Power Connector**
10. **PS/2 Mouse/Keyboard Port**
11. **Power Button**

7.1.2 LEFT-SIDE VIEW

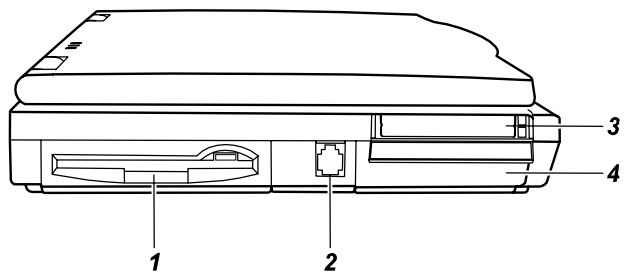


Figure 7-2. Left-Side View

1. **Floppy Disk Drive**
2. **Phone Line Connector**
3. **PC Card Slots**
4. **Hard Disk Drive**

7.ASSEMBLY & DISASSEMBLY

7.1.3 REAR VIEW

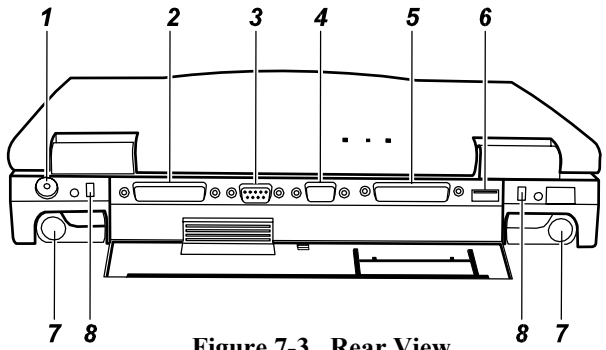


Figure 7-3. Rear View

1. **Power Connector**
2. **Parallel Port**
3. **Serial Port**
4. **VGA Port**
5. **Expansion Connector**
6. **USB Port**
7. **Legs**
8. **Kensington Lock Anchor**

7.1.4 FRONT VIEW

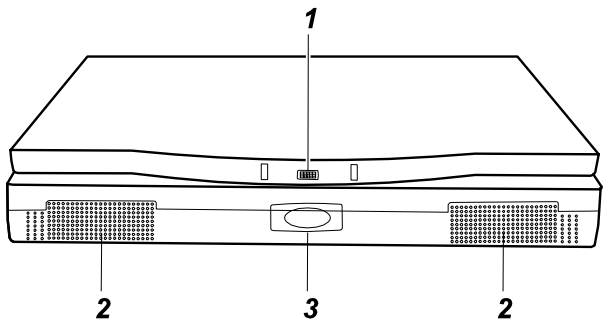
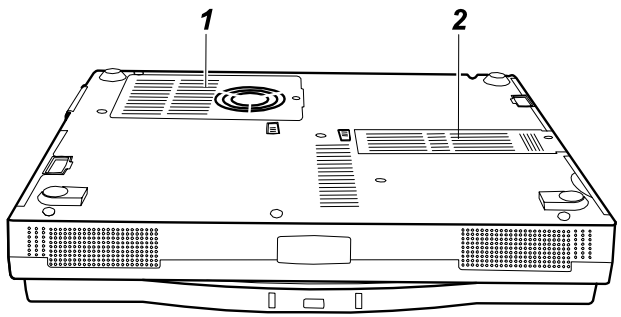


Figure 7-4. Front View

1. **CCD Camera Connector**
2. **Stereo Speaker Set**
3. **Top Cover Latch**

7.ASSEMBLY & DISASSEMBLY

7.1.5 BOTTOM VIEW

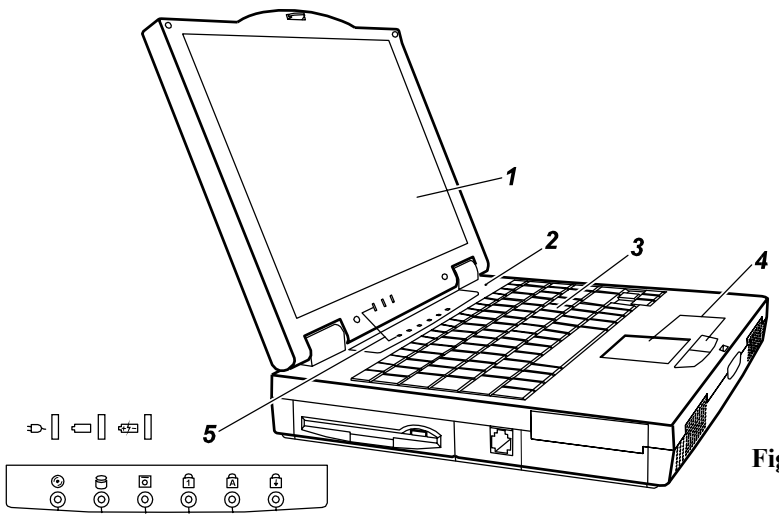


1. **CPU Compartment Cover**
2. **Fax/Modem/Voice Card Compartment**

Figure 7-5. Bottom View

7.1.6 TOP-OPEN VIEW

To open the cover, press the cover latch and lift the cover.



1. **LCD Display**
2. **Microphone**
3. **Keyboard**
4. **Touchpad**
5. **Microphone**
6. **Indicators Panel**

Figure 7-6. Top-Open View

7.ASSEMBLY & DISASSEMBLY

7.2 SYSTEM DISASSEMBLY

The section discusses at length each major component for disassembly/reassembly and show corresponding illustrations. Use the chart below to determine the disassembly sequence for removing components from the notebook.

7.2.1 RIGHT/LEFT BAY DEVICE

The left bay of the notebook can accommodate one of the following devices:

- Floppy disk drive
- AC adapter
- Battery pack
- MO drive
- Secondary hard disk drive
- Cartridge-removable hard disk drive

The right bay of the notebook can accommodate one of the following devices:

- Floppy disk drive
- CD-ROM drive
- Battery pack
- MO drive
- Secondary hard disk drive
- Cartridge-removable hard disk drive

7.ASSEMBLY & DISASSEMBLY

7.2.1 RIGHT/LEFT BAY DEVICE

DISASSEMBLY

1. Place the notebook upside down.
2. Press the locking latch toward the unlocked position and pull out the device.

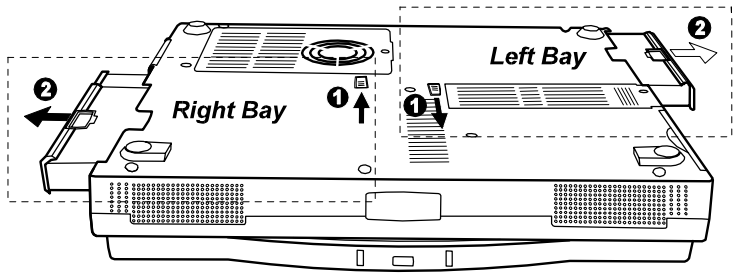


Figure 7-7. Removing the Right/Left Bay Device

REASSEMBLY

1. Slide the device module into the right bay until the location latch clicks into the locked position.(Refer to Figure 7-7)

7.ASSEMBLY & DISASSEMBLY

7.2.2 HARD DISK DRIVE

DISASSEMBLY

1. Place the notebook upside down.
2. Remove one bottom screw and pull out the hard disk drive module.
3. Remove the top cover.Remove four side screw and two rear screws and detach the hard disk drive from the bracket.
4. Unplug the connector card.

REASSEMBLY

1. Align the connector card with the hard disk drive connector and firmly plug the connector.
2. Attach the hard disk drive to the bracket.Secure with four screws on both sides and two screws on the rear of the bracket.Then fit the top cover into place.
3. Slide the hard disk module into the compartment and secure with one screw.

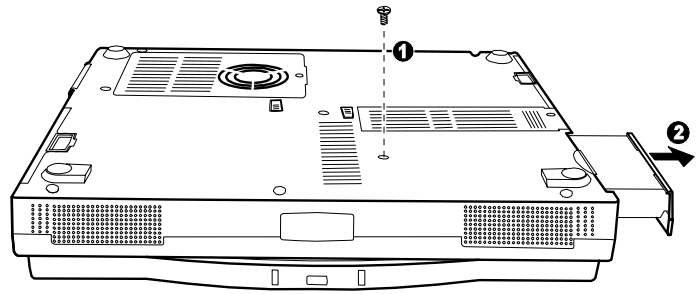


Figure 7-8. Removing the Hard Disk Drive Module

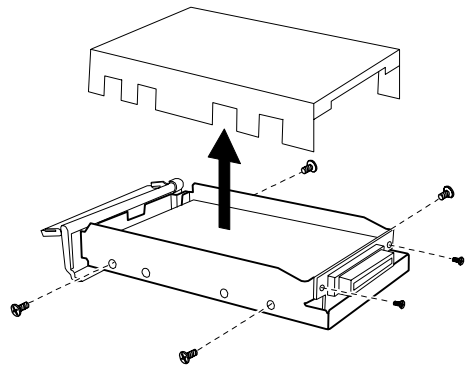


Figure. 7-9. Removing the Hard Disk Drive Bracket Screws

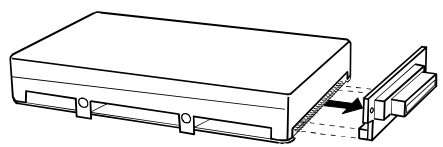


Figure. 7-10. Removing the Connector Card

7.ASSEMBLY & DISASSEMBLY

7.2.3 CPU

DISASSEMBLY

1. Place the notebook upside down.
2. To remove the compartment cover, remove one screw and lift up the cover.
3. To remove the CPU cooling fan, follow these steps:
   a. Remove the four screws.
   b. Unplug the fan power cord from the system board.
4. To remove the CPU, insert a flat screwdriver to the OPEN side of the socket and push the screwdriver toward the CPU to loosen the CPU.

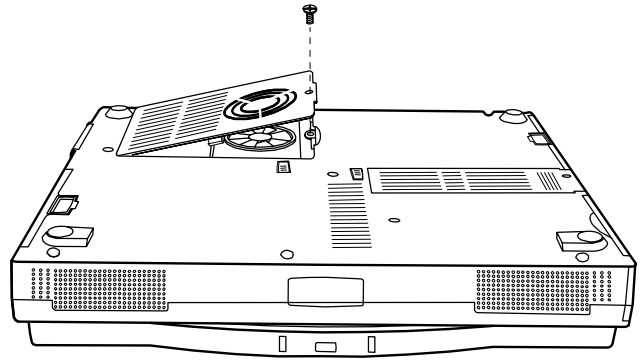


Figure 7-11. Removing the CPU Compartment Cover Screw

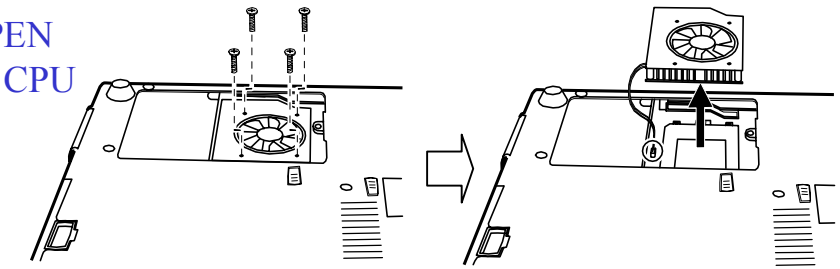


Figure 7-12. Removing the CPU Cooling Fan

REASSEMBLY

1. To install the CPU, align the beveled corner on the CPU with the beveled corner of the socket and insert the CPU pins into the holes. Insert a flat screwdriver to the CLOSE side of the socket and push the screwdriver toward the CPU to the CPU in place.
2. Make sure SW1001,SW1002,and J1002 are set according to the CPU install.
3. Reconnect the fan power cord. Then,attach the CPU cooling fan to the CPU and secure with four screws.
4. Replace the compartment cover and secure with one screw.

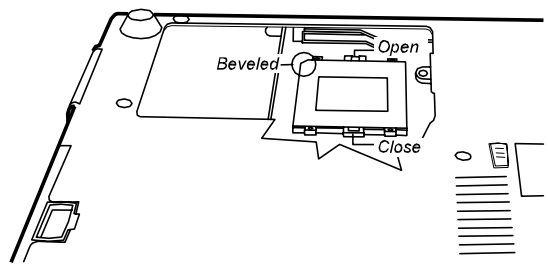


Figure 7-13. Removing the CPU

7.ASSEMBLY & DISASSEMBLY

7.2.4 FAX/ MODEM/ VOICE CARD

DISASSEMBLY

1. Place the notebook upside down.
2. To remove the comportment cover, remove one screw, then slide the cover outwards and lift up.
3. Lift up the inner edge of the card and remove the card.

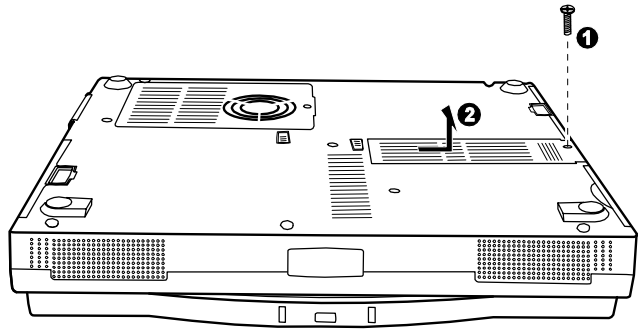


Figure 7-14. Removing the Fax/Modem/Voice Card Compartment Cover

REASSEMBLY

1. Hold the Fax/ Modem/ Voice Card at an angle so that the phone line connector is pointed towards the opening on the notebook. Insert the phone line connector into the opening and press the other end to plug the other connector into the socket on the system board.
2. Replace the compartment cover and secure with one screw.

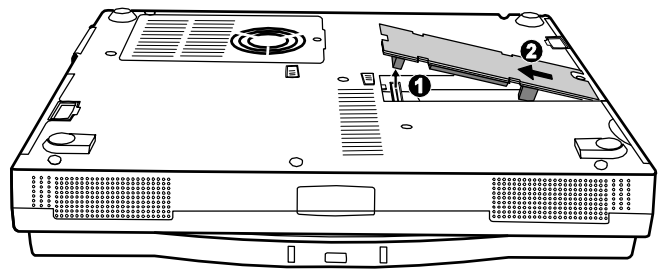


Figure 7-15. Removing the Fax/Modem/Voice Card

7.ASSEMBLY & DISASSEMBLY

7.2.5 KEYBOARD

DISASSEMBLY

1. Open the top cover. Remove the Indicators Panel cover by sliding it downwards and lifting the lower edge.
2. Lift the keyboard and unplug the keyboard cable.

REASSEMBLY

1. Reconnect the keyboard cable and fit the keyboard back into place.
2. Replace the Indicator Panel.

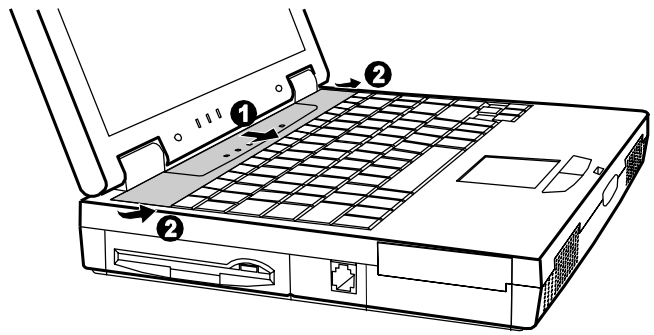


Figure 7-16. Removing the Indicator Panel

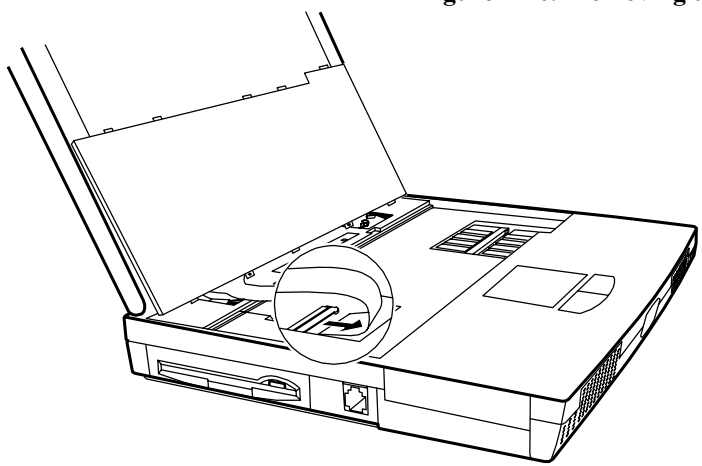


Figure 7-17. Unplugging the Keyboard Cable

7.ASSEMBLY & DISASSEMBLY

7.2.6 MEMORY MODULE

DISASSEMBLY

1. Open the keyboard without unplugging the keyboard cable.
2. Pull the retaining clips outwards and remove the SO-DIMM.

REASSEMBLY

1. To install the SO-DIMM, align the SO-DIMM notched part with the socket corresponding part and firmly insert the SO-DIMM into the socket at an angle. Then push down until the retaining clips lock the SO-DIMM into position.
2. Replace the keyboard.

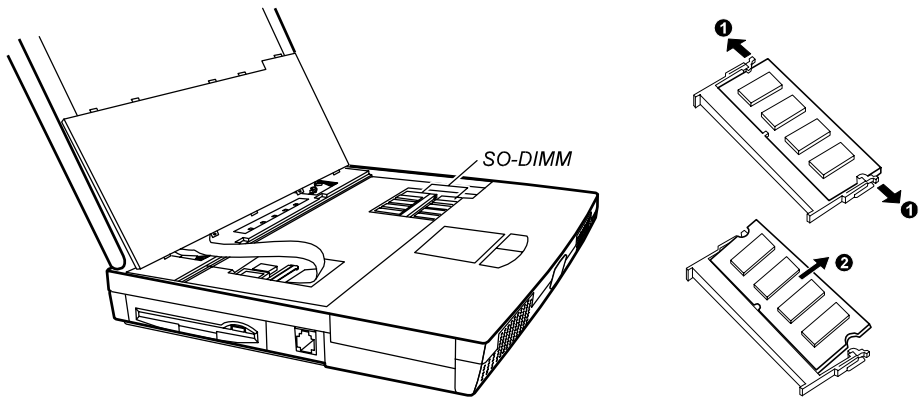


Figure 7-18. Removing the SO-DIMM

7.ASSEMBLY & DISASSEMBLY

7.2.7 LCD ASSEMBLY

DISASSEMBLY

1. Open the top cover. Remove the Indicators Panel cover by sliding it downwards and lifting the lower edge.
2. Remove the two hinge covers.
3. Unplug the LCD cable connector from the system board
4. Remove the four screws from the hinges. Now the LCD assembly is free.

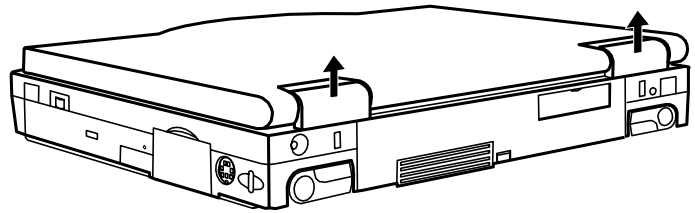


Figure 7-19. Removing the Hinge Covers

REASSEMBLY

1. Attach the LCD assembly to the base unit and secure with four screws on the hinges.
2. Reconnect the LCD cable connectors to the system board
3. Replace the two hinge covers.
4. Replace the Indicator Panel cover.

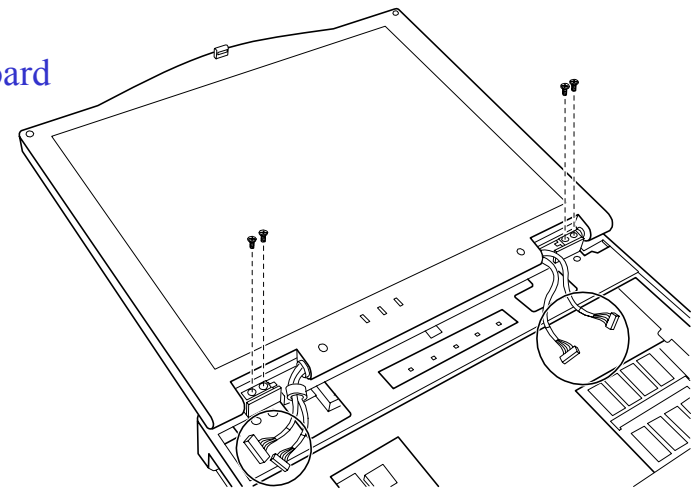


Figure 7-20. Unplugging the LCD Connectors and Removing the Hinge Screws

7.ASSEMBLY & DISASSEMBLY

7.2.8 LCD PANEL

DISASSEMBLY

1. Open the top cover. Remove the Indicators Panel cover by sliding it downwards and lifting the lower edge.
2. Unplug the LCD cable connectors from the system board.
3. Remove the four rubber pads and the four screws underneath. Now you can separate the LCD frame from the housing.
4. To remove the LCD, remove four screws and unplug the cables.

REASSEMBLY

1. Reconnect the cables to the LCD. Fit the LCD back into place and secure with four screws.
2. Fit the LCD frame back to the housing and replace the four screws and rubber pads.
3. Reconnect the LCD cable connectors to the system board.
4. Replace the two hinge covers.
5. Replace the Indicators Panel cover.

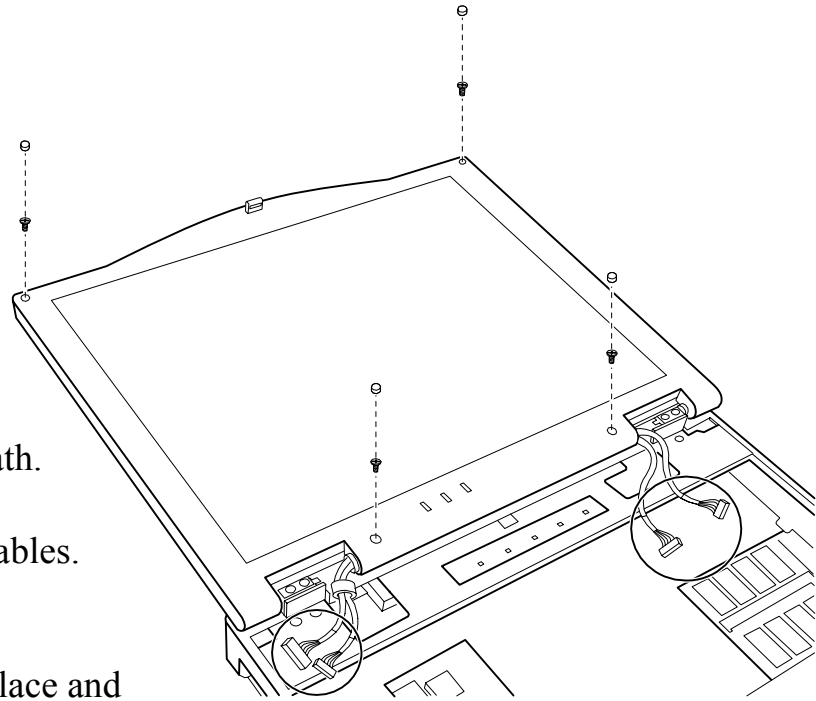


Figure 7-21. Removing the LCD Frame

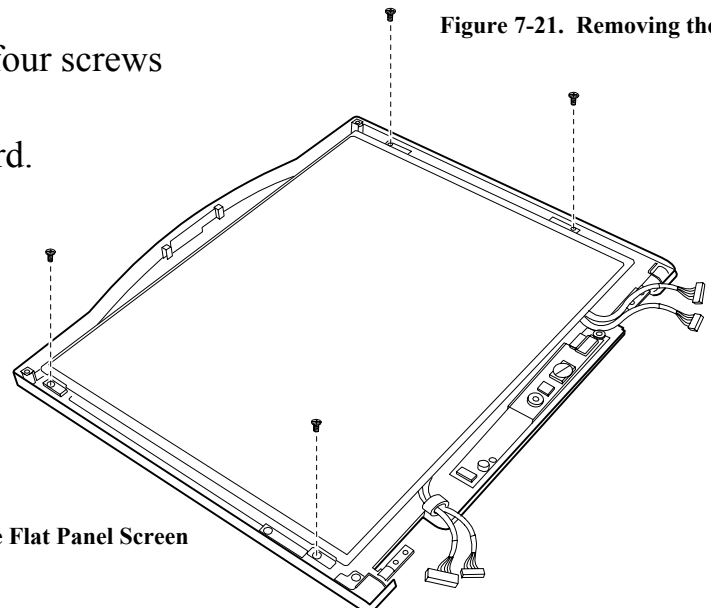


Figure 7-22. Removing the Flat Panel Screen

7.ASSEMBLY & DISASSEMBLY

7.2.9 INVERTER BOARD

DISASSEMBLY

1. Detach the LCD frame.
2. To remove the inverter board, one screw and unplug the connectors from the board.

REASSEMBLY

1. Reconnect the connectors. Fit the inverter board place and secure with one screw.
2. Fit the LCD frame back to the housing and replace the four screws and rubber pads.

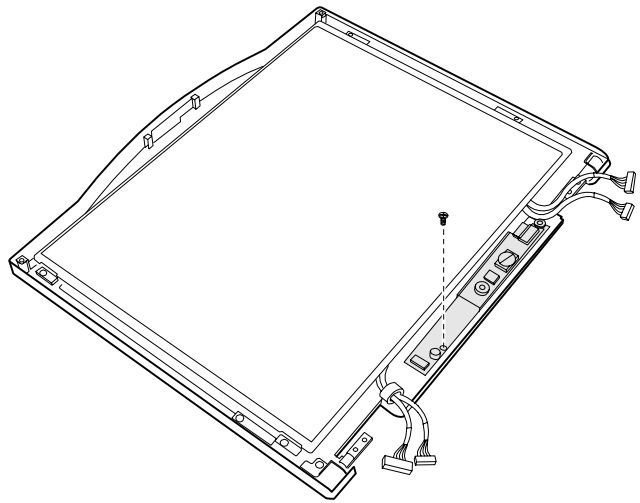


Figure 7-23. Removing the Inverter Board

7.2.10 BOTTOM CHASSIS

DISASSEMBLY

1. Remove the right and left bay devices.
2. Remove the hard disk drive module.
3. Remove the Fax/ Modem/ Voice Card.
4. Remove nine bottom screws to separate the bottom chassis from the base unit.

REASSEMBLY

1. Replace the bottom chassis and secure with nine bottom screw.
2. Replace the Fax/ Modem/ Voice Card.
3. Replace the hard disk drive module.
4. Replace the right and left bay devices.

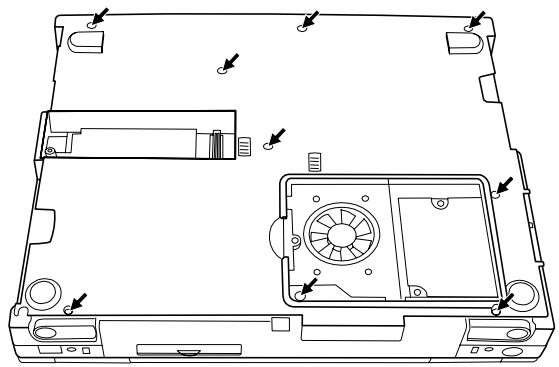


Figure 7-24. Removing the Bottom Chassis

7.ASSEMBLY & DISASSEMBLY

7.2.11 D/D BOARD

DISASSEMBLY

1. Remove the bottom chassis.
2. Remove the D/D board by removing one screw and lifting it up.

REASSEMBLY

1. Reconnect the D/D board connector to the system board and secure with one screw.
2. Replace the bottom chassis.

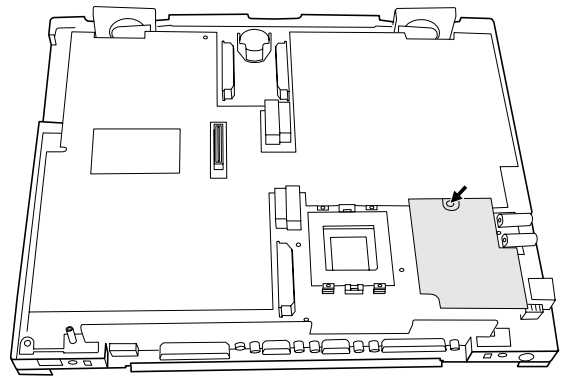


Figure 7-25. Removing the D/D Board

7.2.12 VIDEO CAPTURE BOARD

DISASSEMBLY

1. Remove the bottom chassis.
2. Remove the Video Capture board by removing one screw and lifting it up.

REASSEMBLY

1. Reconnect the Video Capture Board connector to the system board and secure with one screw.
2. Replace the bottom chassis.

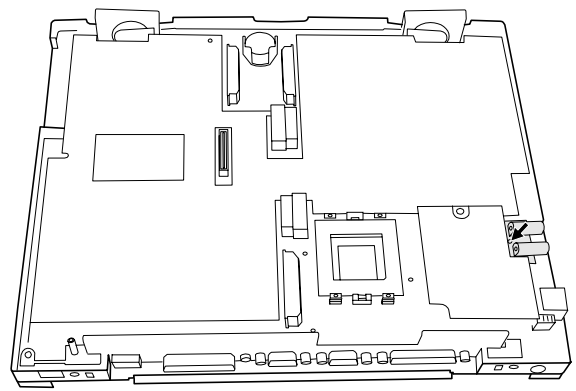


Figure 7-26. Removing the Video Capture Board

7.ASSEMBLY & DISASSEMBLY

7.2.13 SYSTEM BOARD

DISASSEMBLY

1. Remove two rear panel screws.
2. Remove the LCD assembly.
3. Remove the keyboard .
4. Unplug the touchpad connector and speaker connectors from the system board.
5. Remove the four screws from near the hinges.
6. Remove the bottom chassis.
7. Remove the D/D board.
8. Remove the CPU cooling fan.
9. Unplug any connectors that are still connected to the system board.
10. Remove the remaining three screws that secure the system board to the base unit.
11. Lift the system board free.

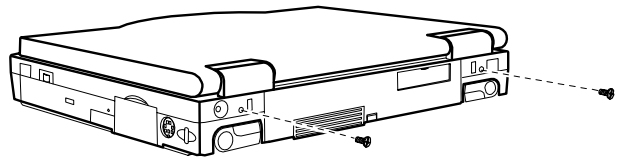


Figure 7-27. Removing Two Rear Panel Screws

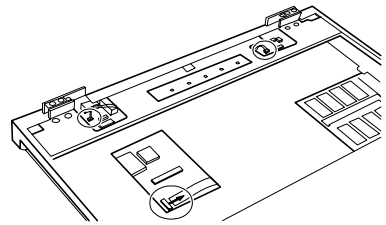


Figure 7-28. Unpluging the Connectors from the System Board

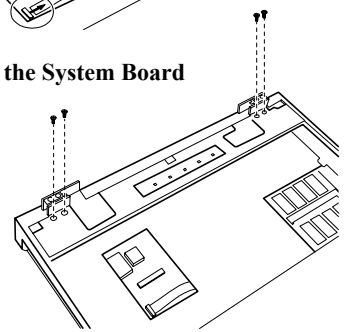


Figure 7-29. Removing Four Screws

REASSEMBLY

1. Fit the system board into place and replace the three screws to the system board.
2. Replace the CPU cooling fan.
3. Replace the D/D board.
4. Replaced the bottom chassis.
5. Connect the speaker connectors and touchpad connector to the system board.
6. Replace the four screws near the hinges.
7. Replace the keyboard.
8. Replace the two rear panel screws.
9. Replace the LCD assembly.

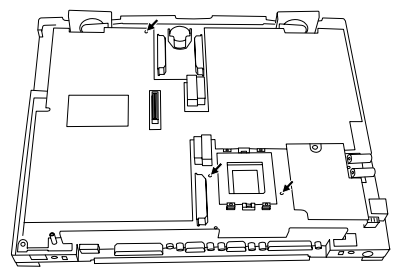


Figure 7-30. Removing the System Board Screws

7.ASSEMBLY & DISASSEMBLY

7.2.14 TOUCHPAD BOARD

DISASSEMBLY

1. Remove the system board
2. Remove the touchpad holder by removing three screws.
3. Slide the touchpad board out.

REASSEMBLY

1. Fit the touchpad board back into place.
2. Fit the touchpad holder back into place and secure with three screws.
3. Replace the system board.

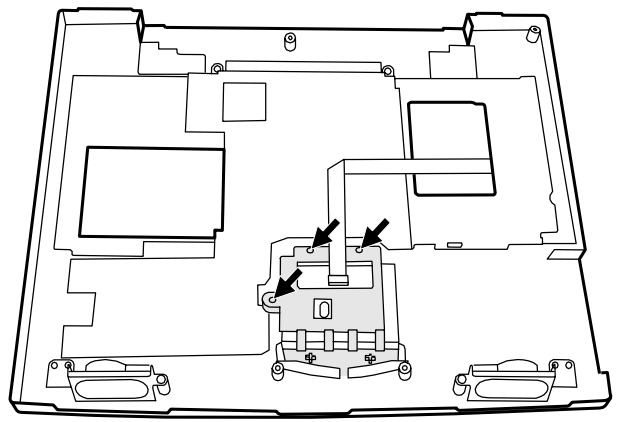


Figure 7-31. Removing the Touchpad Holder

8. MAINTENANCE DIAGNOSTICS

8.1 INTRODUCTION

EACH TIME THE COMPUTER IS TURNED ON ,THE SYSTEM BIOS RUNS A SERIES OF INTERNAL CHECKS ON THE HARDWARE. THIS POWER-ON SELF TEST (POST) ALLOWS THE COMPUTER TO DETECT PROBLEMS AS EARLY AS THE POWER-ON STAGE. ERROR MESSAGES OF POST CAN ALERT YOU TO THE PROBLEMS OF YOUR COMPUTER.

IF AN ERROR IS DETECTED DURING THESE TESTS, YOU WILL SEE AN ERROR MESSAGE DISPLAYED ON THE SCREEN. IF THE ERROR OCCURS BEFORE THE DISPLAY IS INITIALIZED , THEN THE SCREEN CANNOT DISPLAY THE ERROR MESSAGE. ERROR CODES OR SYSTEM BEEPS ARE USED TO IDENTIFY A POST ERROR THAT OCCURS WHEN THE SCREEN IS NOT AVAILABLE.

THE VALUE FOR THE DIAGNOSTIC POST(378H) IS WRITTEN AT THE BEGINNING OF THE TEST. THEREFORE , IF THE TEST FAILED, THE USER CAN DETERMINE WHERE THE PROBLEM OCCURRED BY READING THE LAST VALUE WRITTEN TO POST 378H BY THE PIO DEBUG BOARD PLUG AT PIO PORT.

8. MAINTENANCE DIAGNOSTICS

8.2 ERROR CODES : FOLLOWING IS A LIST OF ERROR CODES IN SEQUENCE DISPLAY ON THE PIO DEBUG BOARD.

Code	Description
00H	Start of BootLoader sequence.
01H	Disable A20 through A20, not send.
02H	Initialize ChipSet.
03H	Perform conventional RAM(1st 640K) test with crossed-pattern R/W.
04H	Move BootLoader to the RAM.
05H	Start point of execution of BootLoader in RAM.
06H	Perform PnP initialization for Crystal audio chip.
06H	Check OVERRIDE option, not send.
07H	Shadow System BIOS.
08H	Checksum System BIOS ROM, not send.
09H	Proceed with Normal Boot
0AH	Proceed with Crisis Boot
0FH	DRAM Sizing
10H	Initial L1,L2 cache, make stack and diagnose CMOS.
11H	Turn off FASTA20 for POST. Reset GDTs, 8259s guickly.
12H	Signal Power On Reset at COMS.
13H	Initialize the Chipset, (SDRAM).
14H	Search For ISA Bus VGA Adapter
15H	Reset Counter/Timer 1, exite the RAM.
16H	User register config through CMOS
18H	Dispatch to 1st 64K RAM Test
19H	Checksum the ROM
1AH	Reset PIC's(8259s)
1BH	Initialize Video Adapter(s)
1CH	Initialize Video (6845 Regs)
1DH	Initialize Color Adapter
1EH	Initialize Monochrome Adapter
1FH	Test 8237A Page Registers
20H	Perform Keyboard self test
21H	Test & Initialize Keyboard Controller

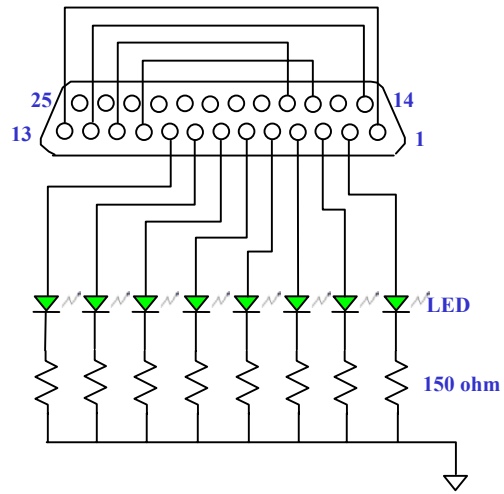
Code	Description
22H	Check If CMOS Ram Valid
23H	Test Battery Fail & CMOS X-SUM
24H	Test the DMA controllers
25H	Initialize 8237A Controller
26H	Initialize Interrupt Vectors Table.
27H	RAM Quick Sizing
28H	Protected mode entered safely
29H	RAM test completed
2AH	Protected mode exit successful
2BH	Setup Shadow
2CH	Prepare To Initialize Video
2DH	Search For Monochrome Adapter
2EH	Search For Color Adapter, VGA Initialize.
2FH	Signon messages displayed
30H	Special init of keyboard ctlr
31H	Test If Keyboard Present
32H	Test Keyboard Interrupt
33H	Test Keyboard Command Byte
34H	TEST, Blank and count all RAM
35H	Protected mode entered safely (2).
36H	RAM test complete
37H	Protected mode exit successful
38H	Update Keyboard output port to disable gate of A20
39H	Setup Cache Controller
3AH	Test If 18.2Hz Periodic Working
3BH	Initialize BIOS Data Area at 40:0.
3CH	Initialize the hardware interrupt vector table
3DH	Search and Init the Mouse
3EH	Update NumLock status
3FH	OEM initialization of COMM and LPT ports

8. MAINTENANCE DIAGNOSTICS

Code	Description
40H	Configure the COMM and LPT ports
41H	Initialize the floppies
42H	Initialize the hard disk
43H	Initialize additional ROMs
44H	OEM's init of Power Management, (check SMI)
45H	Update NUMLOCK status
46H	Test For Coprocessor Installed
47H	OEM functions before boot (PCMCIA, CardBus)
48H	Dispatch To Operation System Boot
49H	Jump Into Bootstrap Code
4AH	OEM's init of PM with USB

Code	Beeps	Description
0F0h	....	No RAM
0F1h	..._	RAM test failed
002h	.._.	BIOS is not shadowed
004h	._..	BIOS Checksum BAD
00Ah	_._.	No CR code/CR bad

PIO PORT (378H) DIAGNOSTIC TOOLS



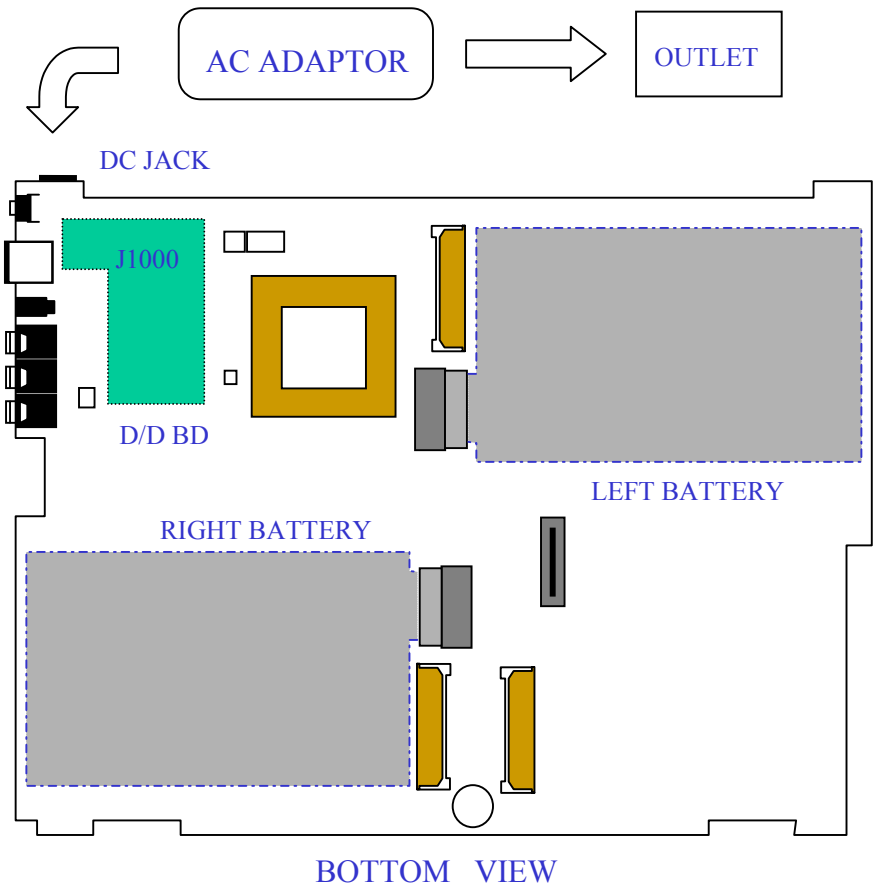
PIN1 : STROBE ⟷ PIN13: SLCT
PIN10: ACK# ⟷ PIN16: INT#
PIN11: BUSY ⟷ PIN17: SELIN#
PIN12:PTERR ⟷ PIN14: AUTOFD#
PIN[9:2]:PD[7:0]

9. TROUBLE SHOOTING

5031 M/B MAINTENANCE

9.1 NO POWER:

WHEN THE POWER BUTTON IS PRESSED, NOTHING HAPPENS ,POWER INDICATOR IS NOT LIGHT UP.



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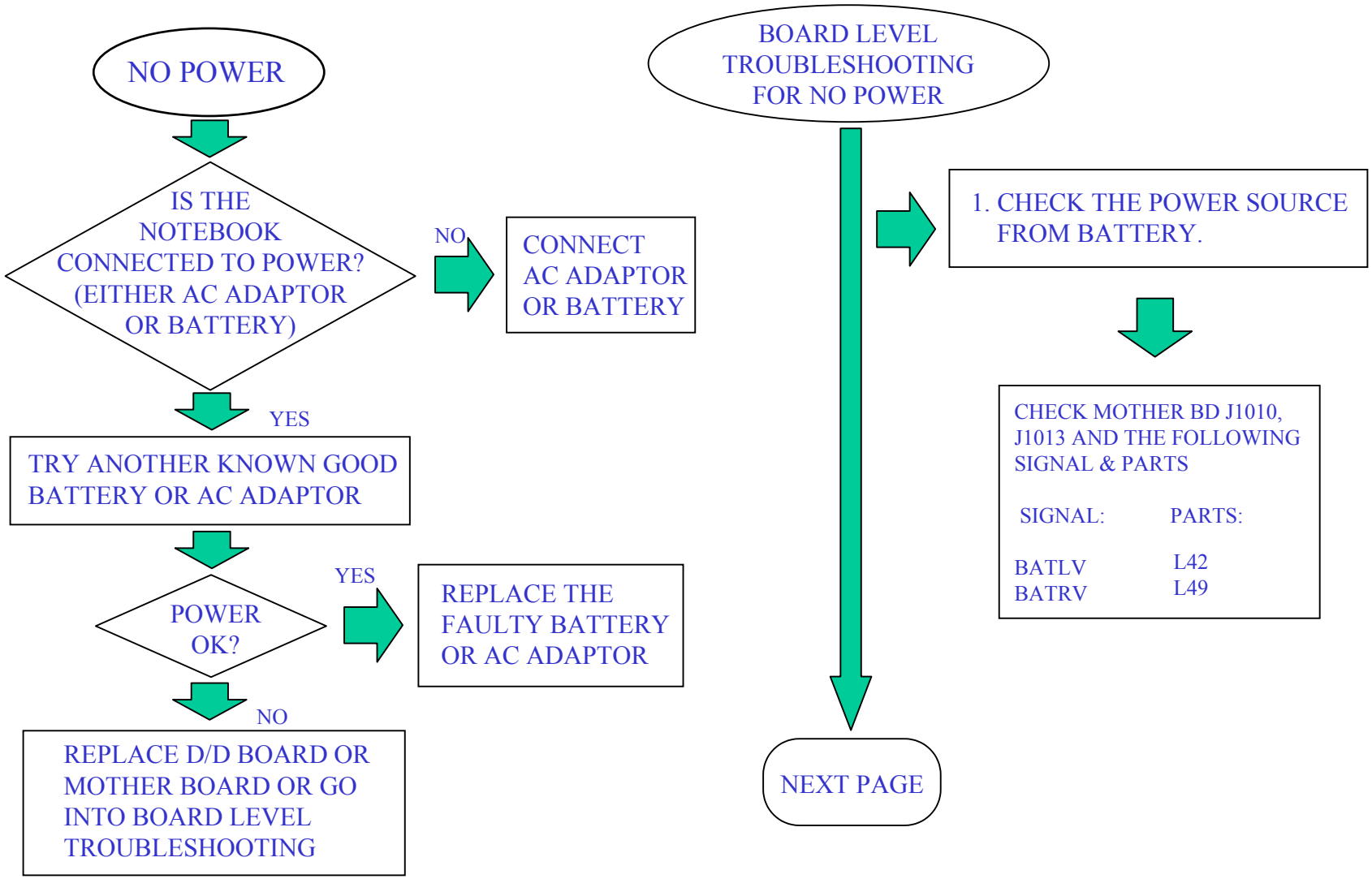

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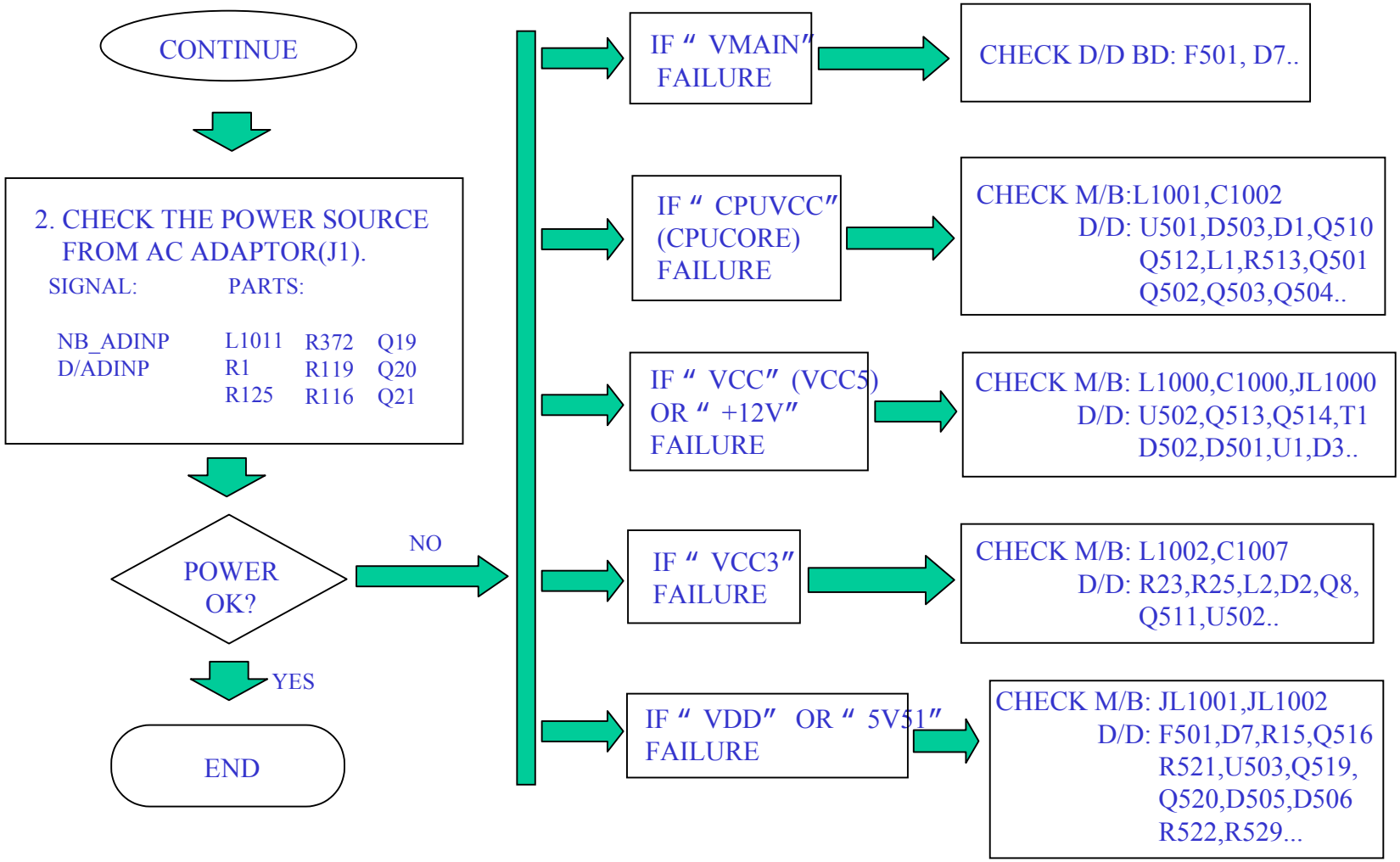
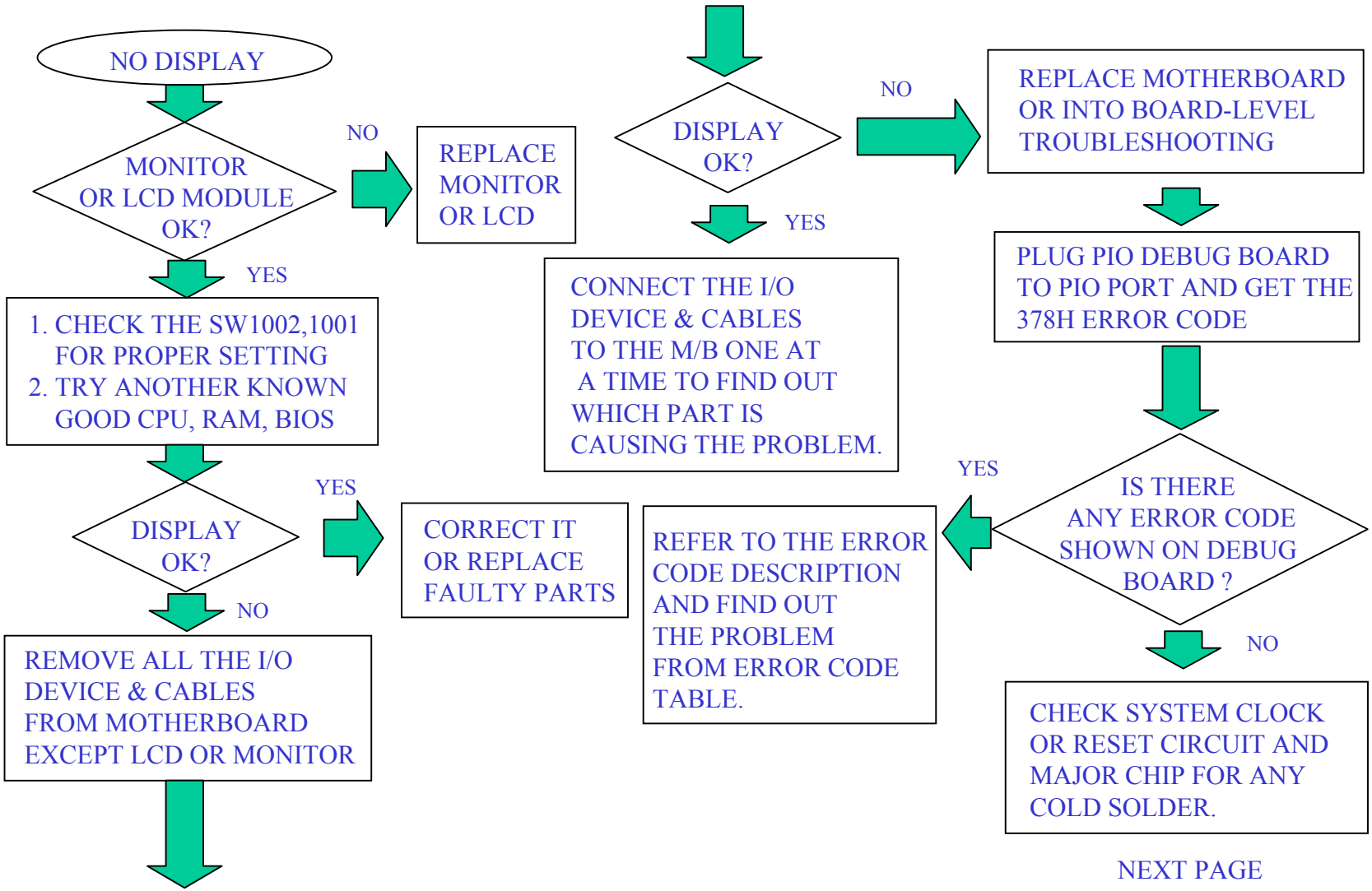


9.2 NO DISPLAY

THERE IS NO DISPLAY ON BOTH LCD AND MONITOR

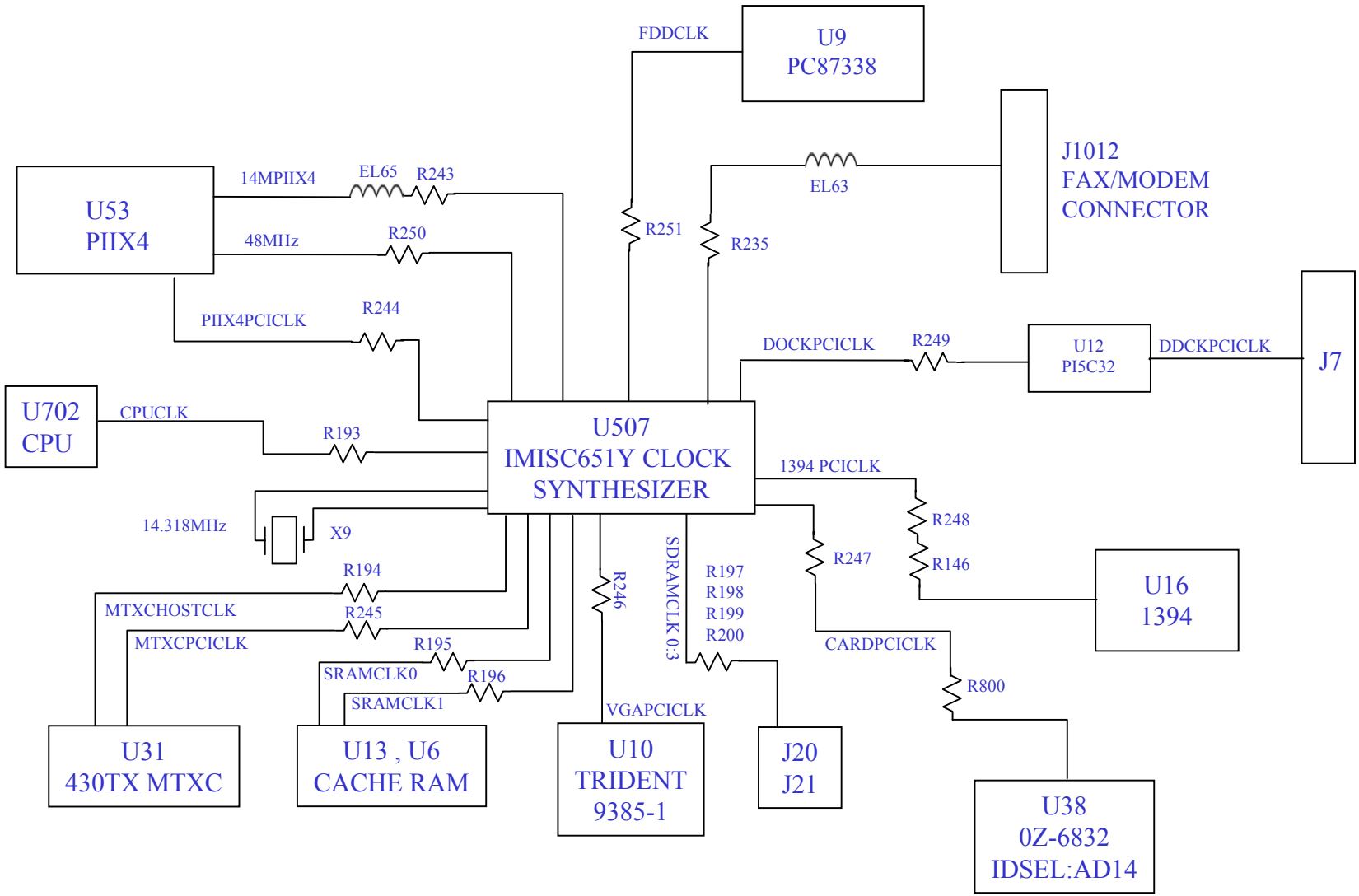


NEXT PAGE

5031 M/B MAINTENANCE

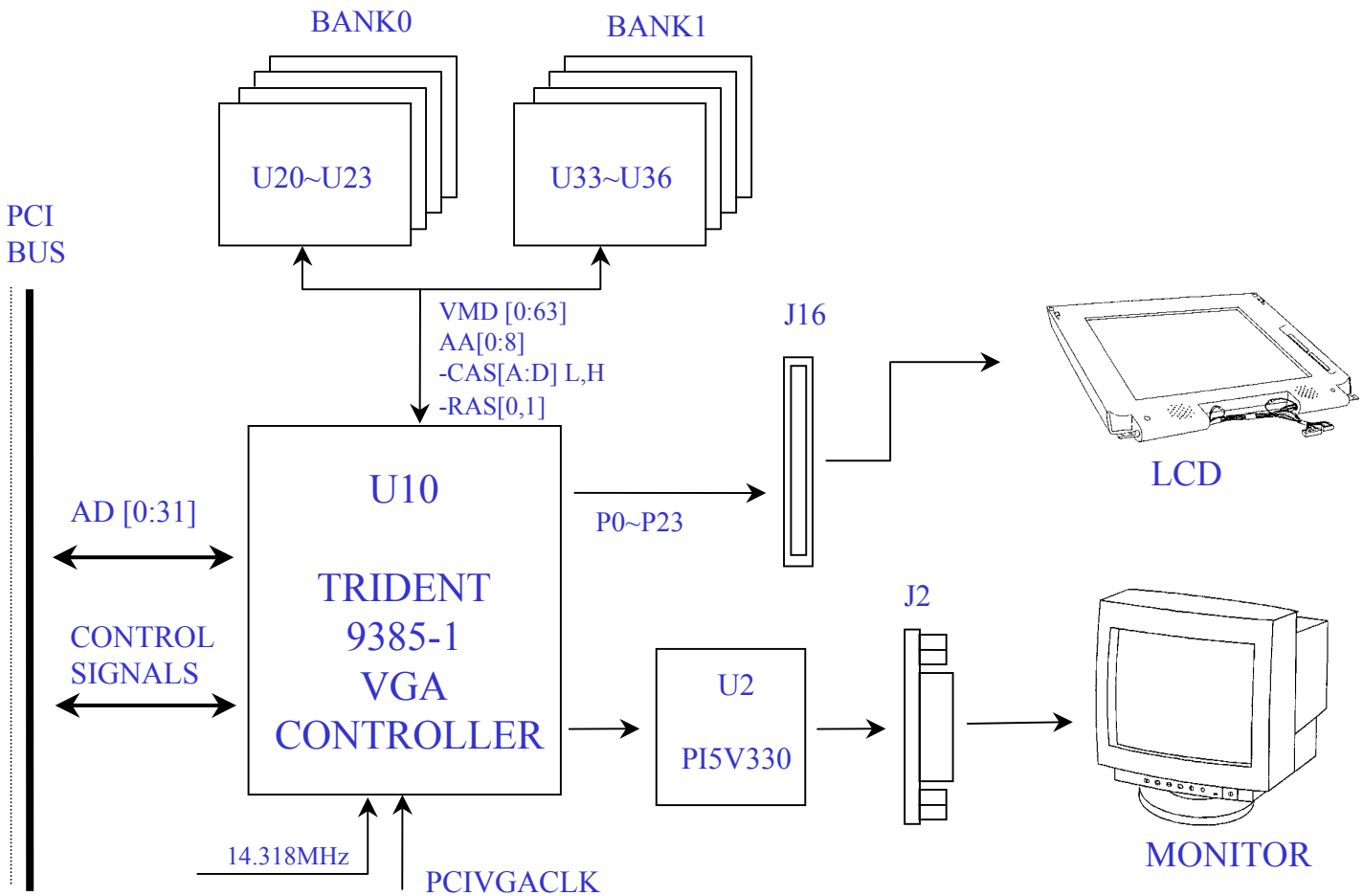
9.2 NO DISPLAY

******SYSTEM CLOCK CHECK ******



9.3 VGA CONTROLLERFAILURE

THERE IS NO DISPLAY ON BOTH LCD AND MONITOR ALYHOUGH POWER-ON-SELF-TEST IS PASSED.



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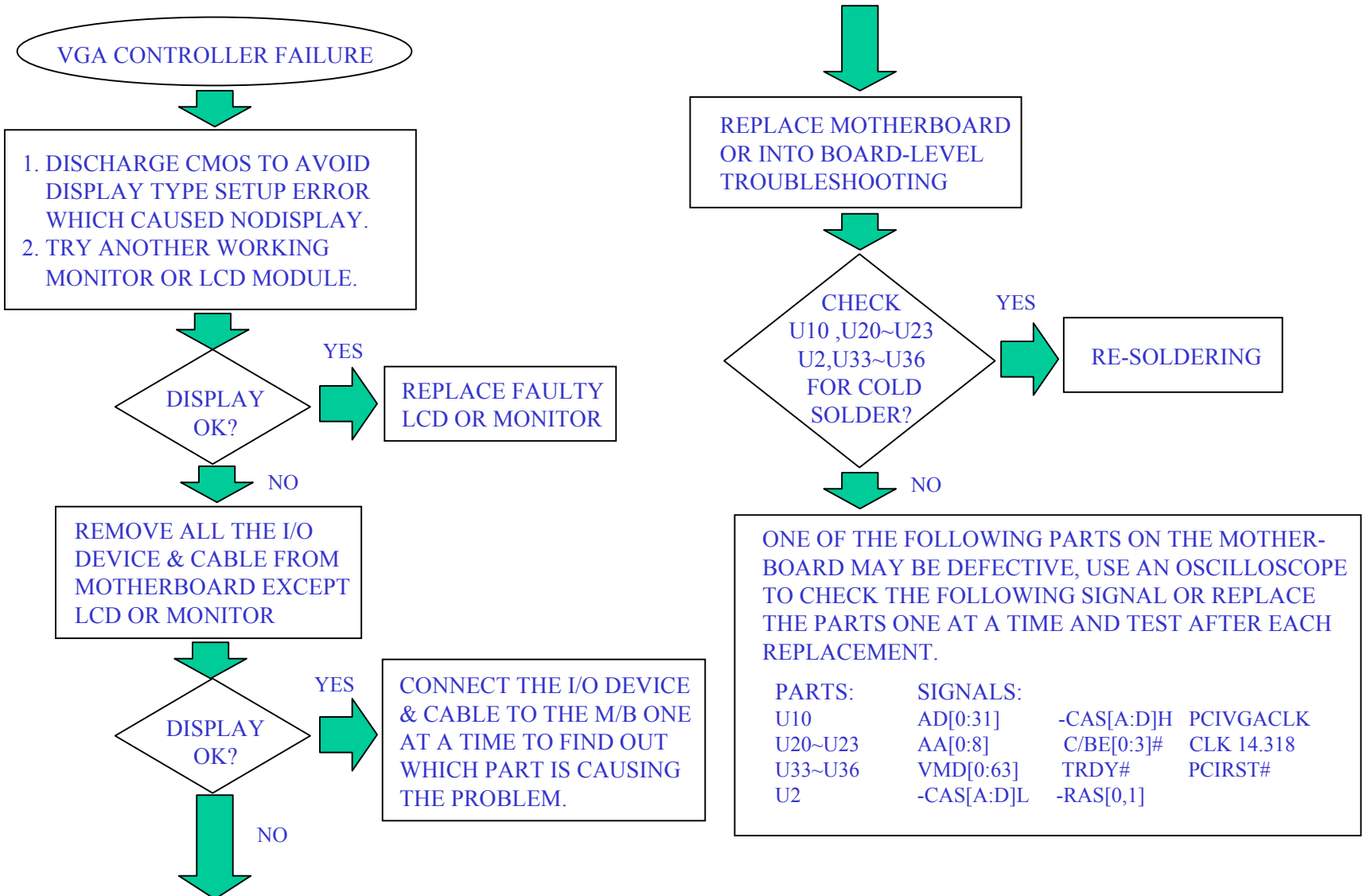
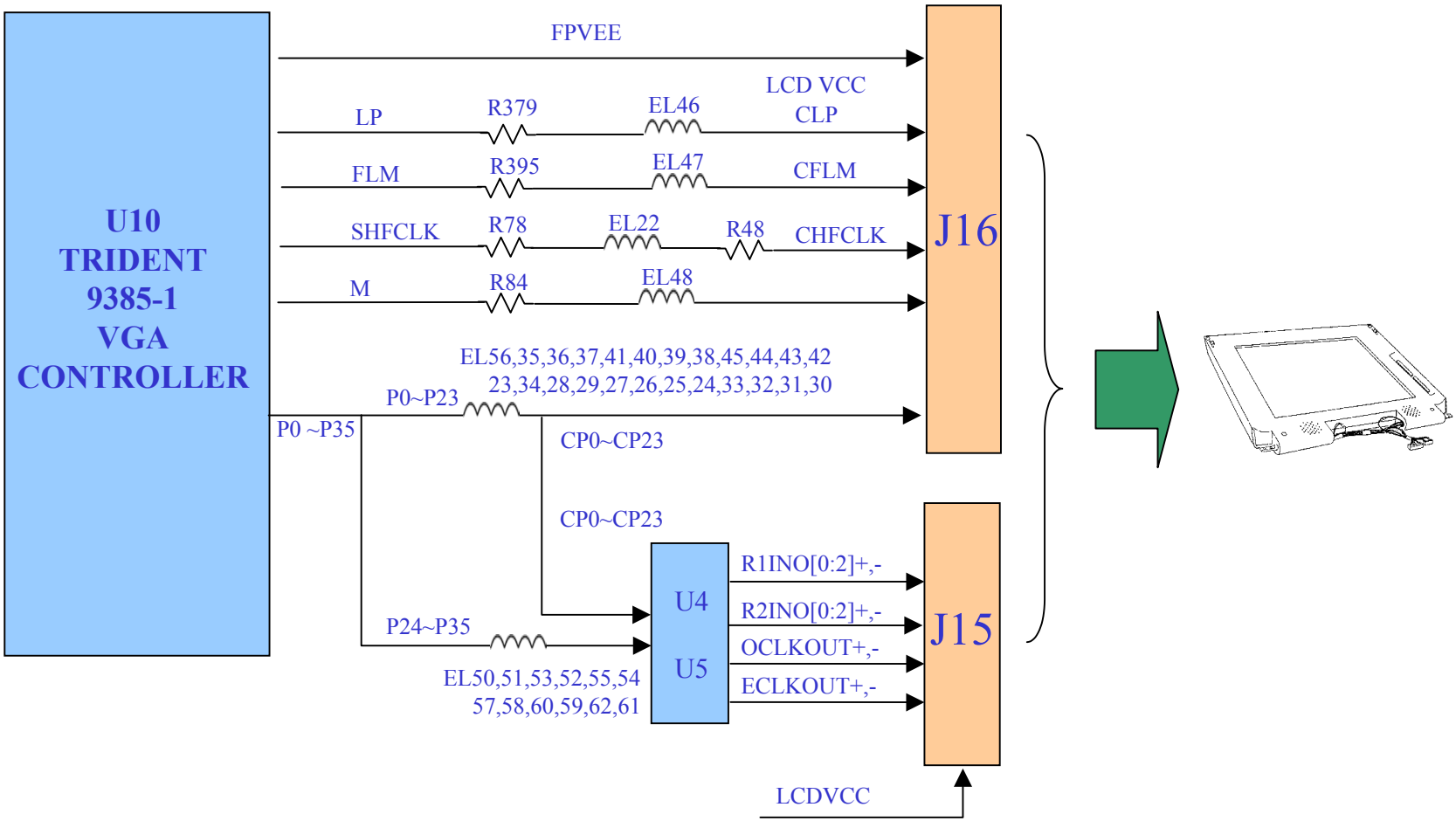
THERE IS NO DISPLAY ON BOTH LCD AND MONITOR ALTHOUGH POWER-ON-SELF-TEST IS PASSED.



9.4 LCD NO DISPLAY

THE LCD SHOWS NOTHING OR ABNORMAL PICTURE , BUT IT IS OK FOR EXTERNAL MONITOR.



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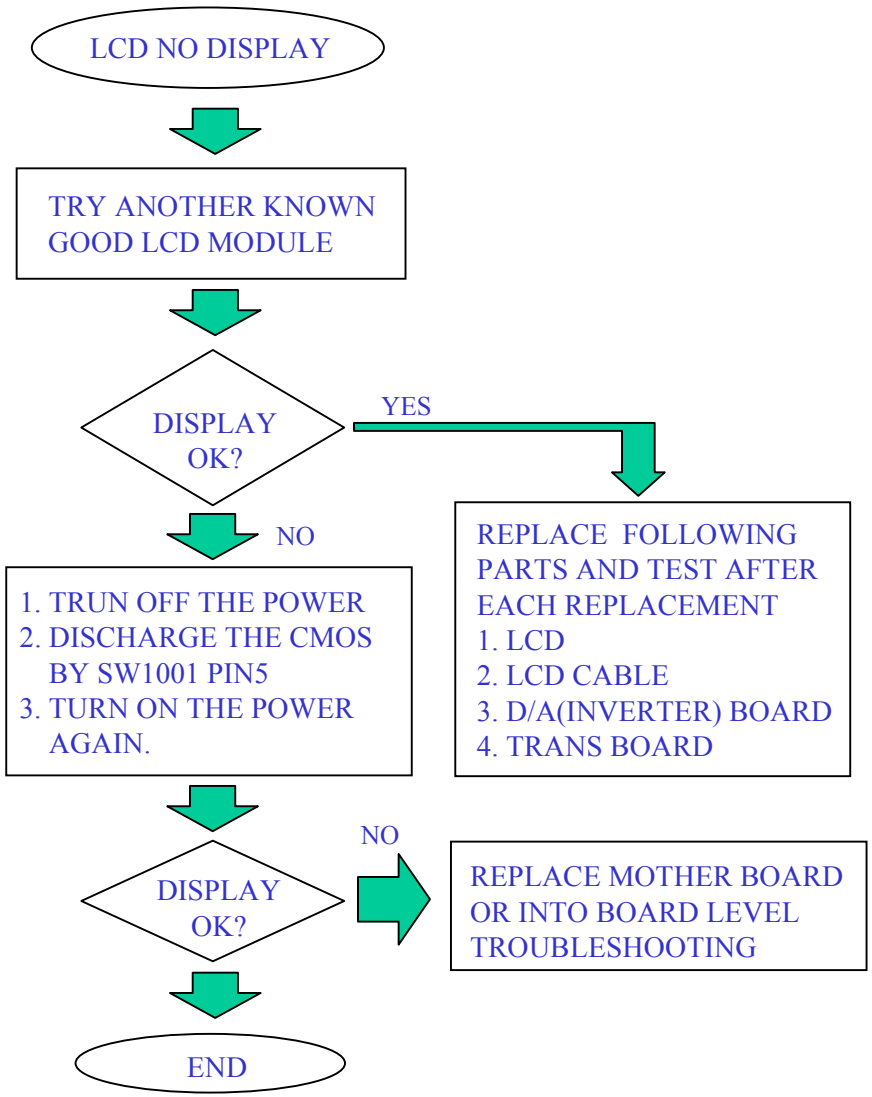
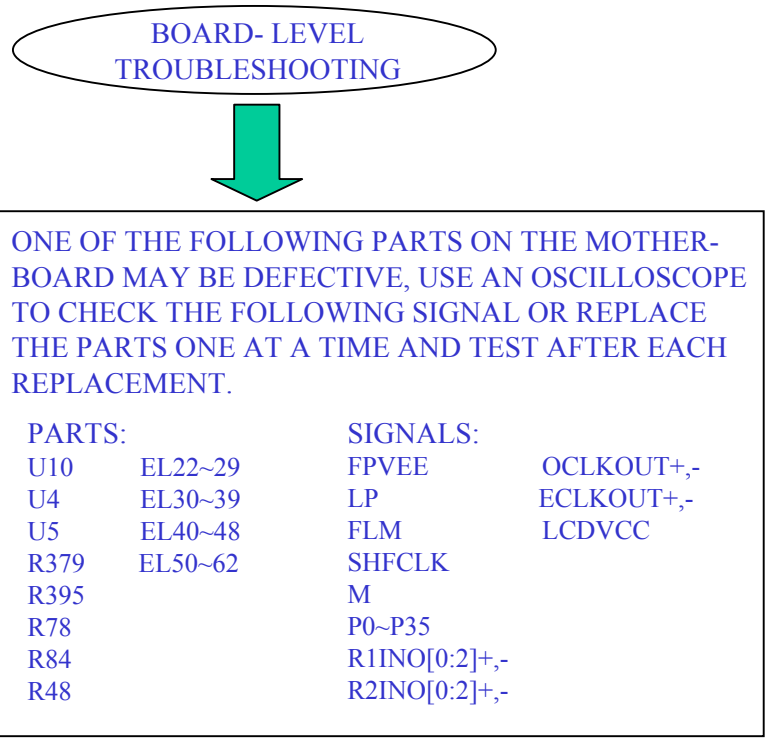
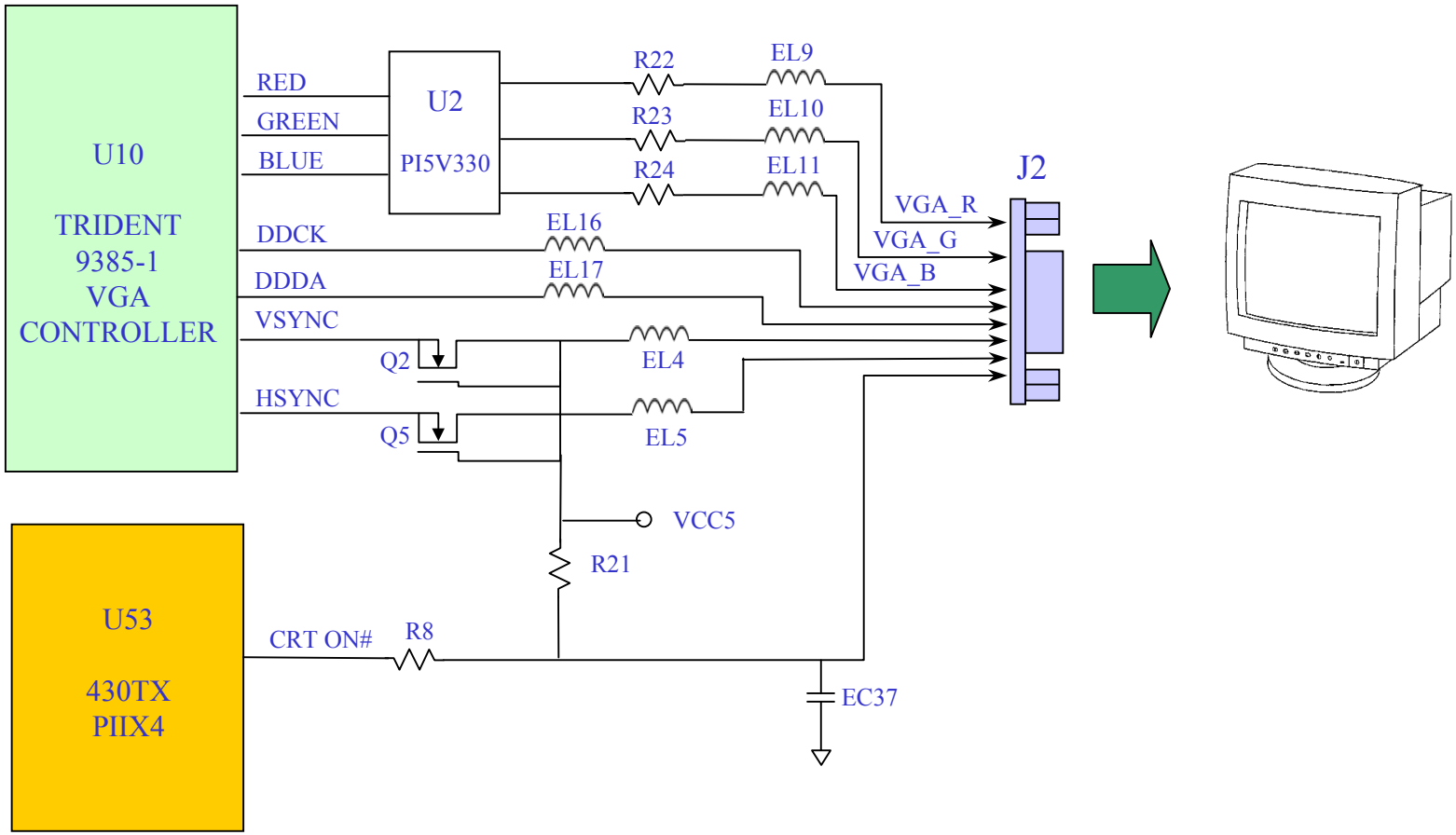




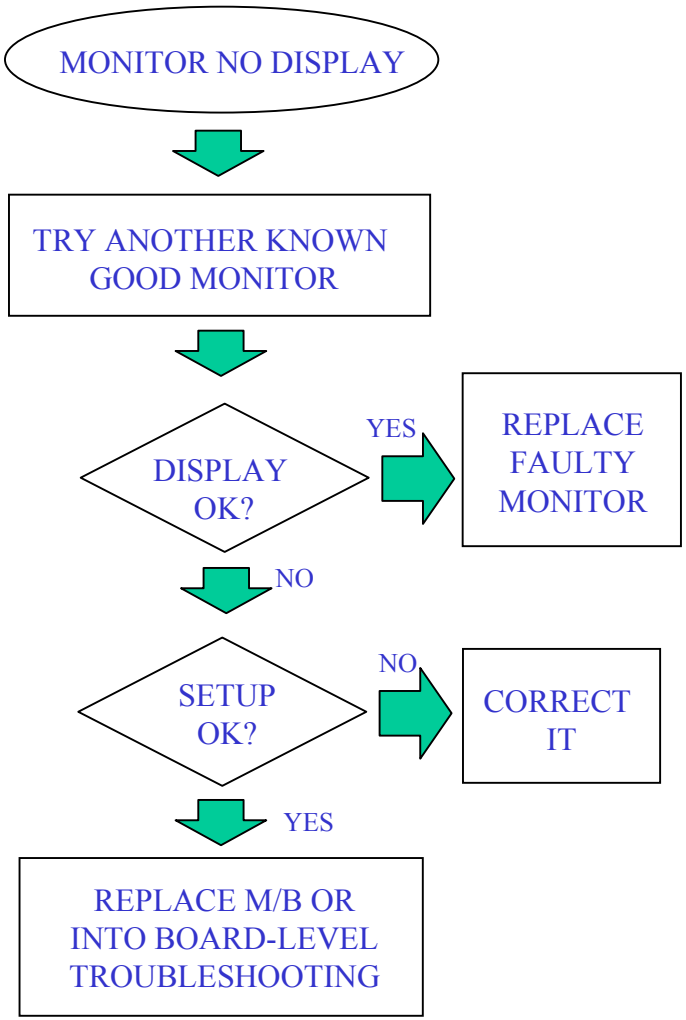
9.5 EXTERNAL MONITOR NO DISPLAY

THE CRT MONITOR SHOWS NOTHING OR ABNORMAL COLOR, BUT IT IS OK FOR LCD.



9.5 EXTERNAL MONITOR NO DISPLAY

THE CRT MONITOR SHOWS NOTHING OR ABNORMAL COLOR, BUT IT IS OK FOR LCD.



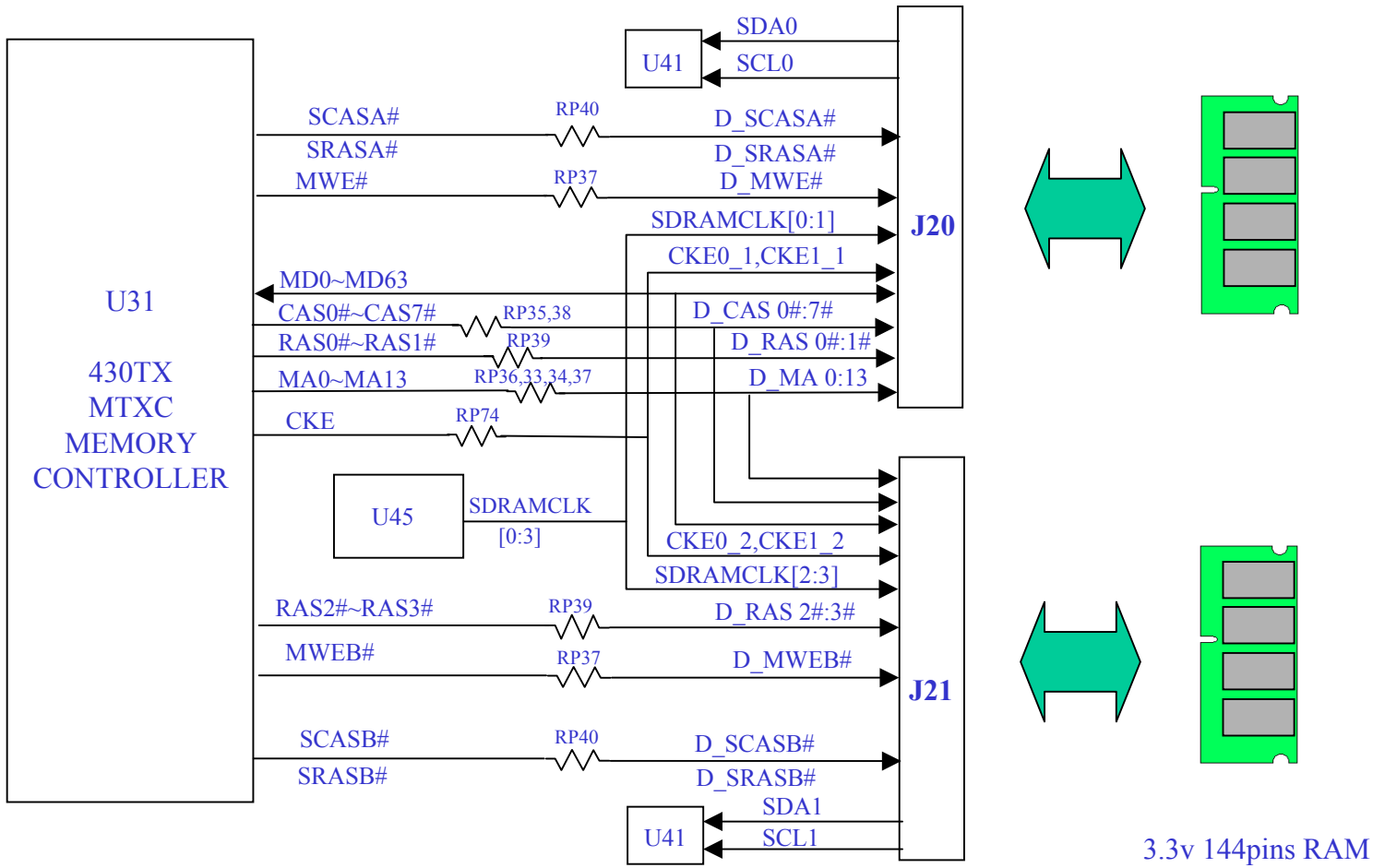
BOARD-LEVEL TROUBLESHOOTING FOR MONITOR NO DISPLAY

CHECK THE FOLLOWING PARTS FOR COLD SOLDER OR ONE OF THE FOLLOWING PARTS ON THE MOTHER-BOARD MAY BE DEFECTIVE, USE AN OSCILLOSCOPE TO CHECK THE FOLLOWING SIGNAL OR REPLACE THE PARTS ONE AT A TIME AND TEST AFTER EACH REPLACEMENT.

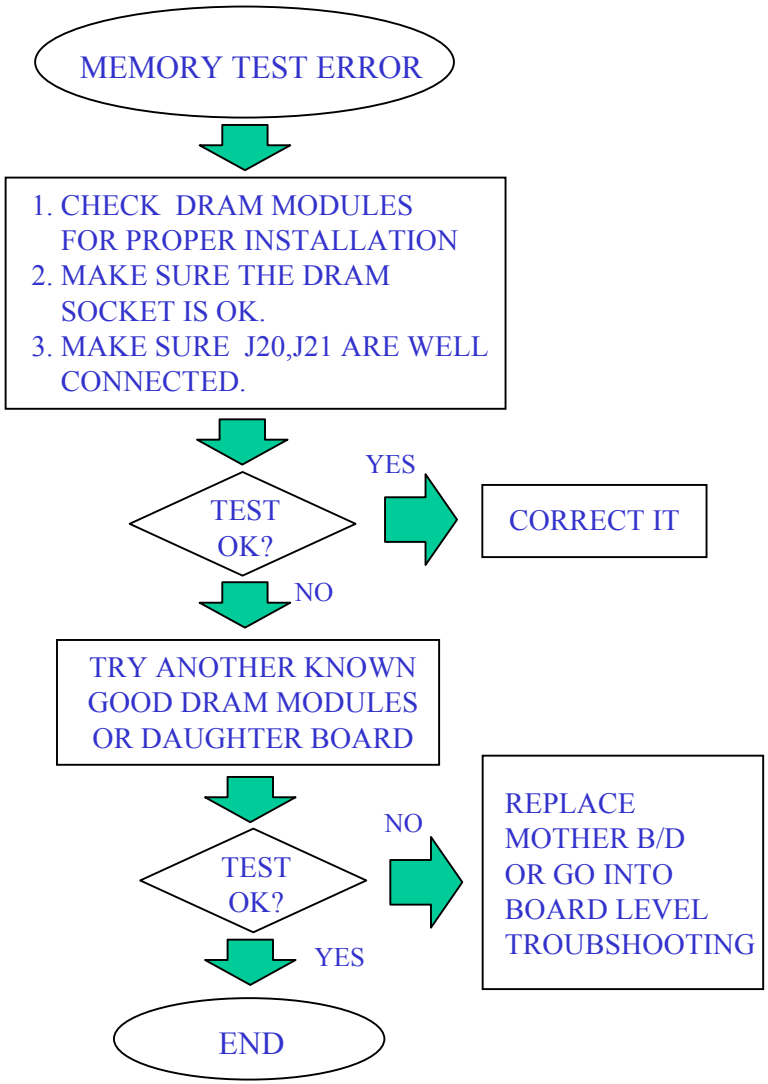
PARTS:	SIGNALS:	
U10,U53,U2	RED	VGA_R
Q2,Q5,R22	GREEN	VGA_G
R23,R24,R21	BLUE	VGA_B
R8,EC37,EL9	VSYNC	CRT ON#
EL10,EL11,	HSYNC	
EL16,EL17	DDCK	
EL4,EL5	DDDA	

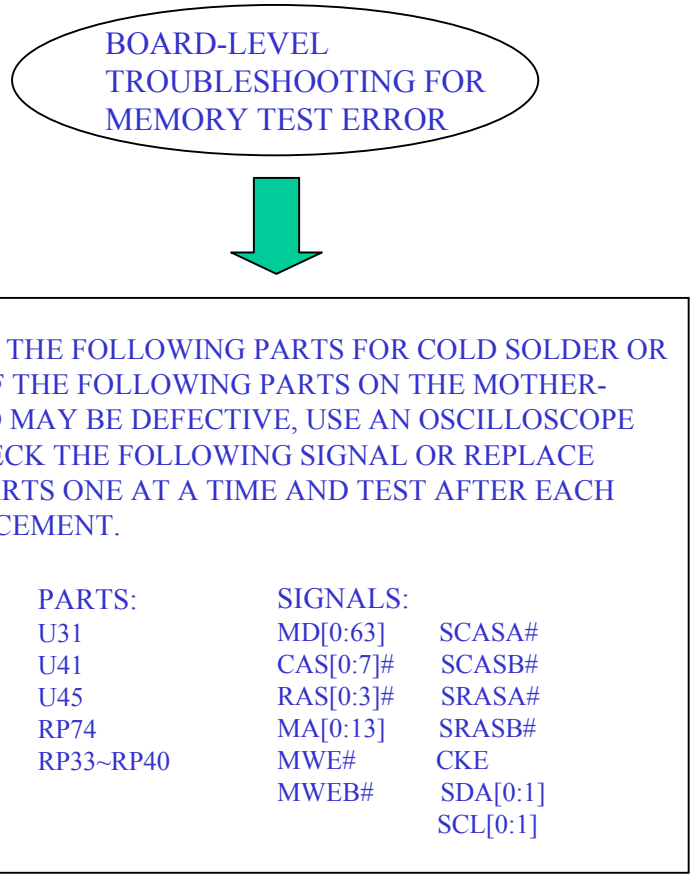
9.6 MEMORY TEST ERROR

THE ERROR CODE SHOWN ON THE PIO DEBUG BOARD IS 0FH, 13H,18H OR 27H AND SYSTEM HANGS UP.



9.6 MEMORY TEST ERROR

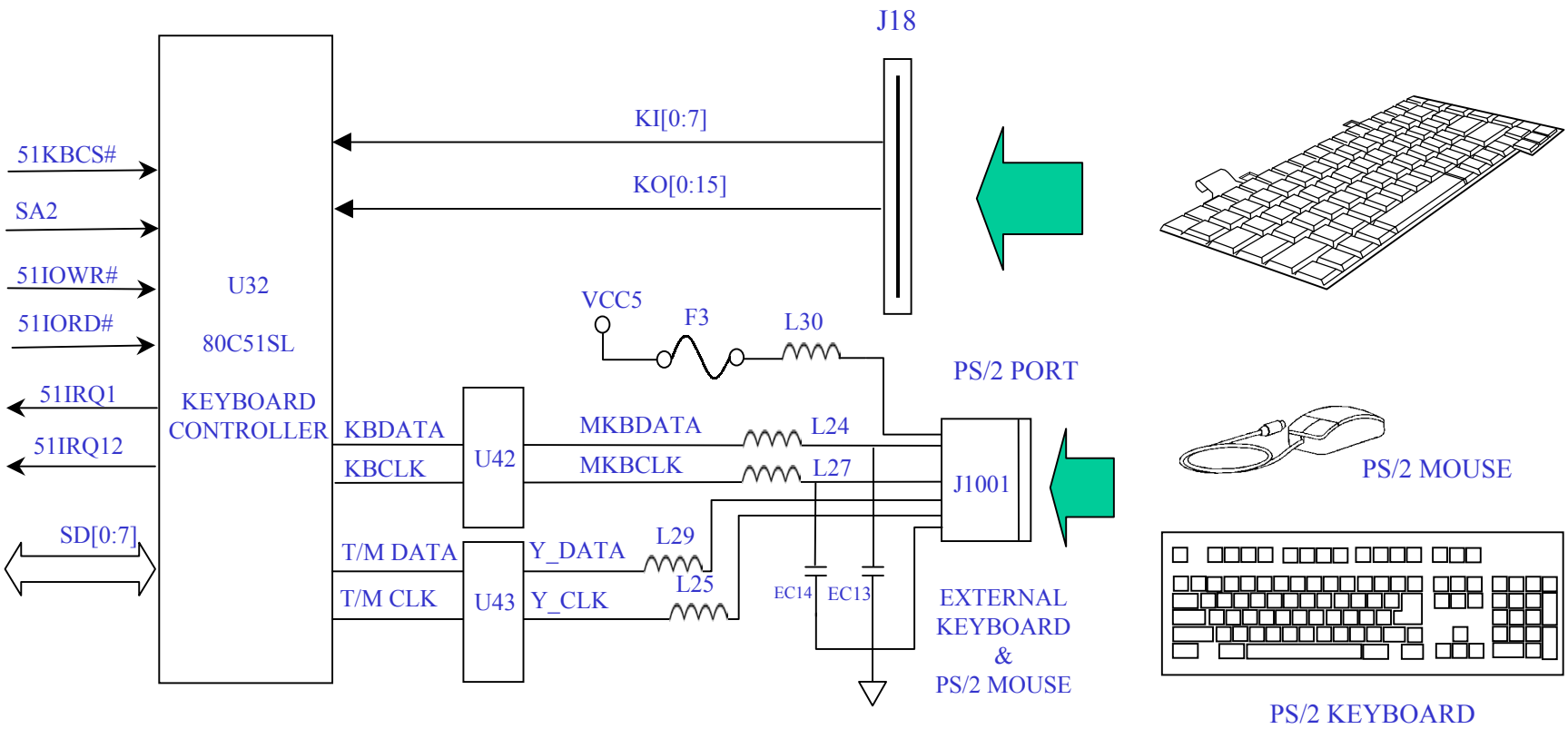




5031 M/B MAINTENANCE

9.7 KEYBOARD TEST ERROR

1. ERROR MESSAGE OF KEYBOARD FAILURE IS SHOWN OR ANY KEY DOESN′ T WORK.
2. PIO DEBUG BOARD SHOWS THE PORT 378H ERROR CODE IS STOPPED AT 30H,31H,32H OR 33H



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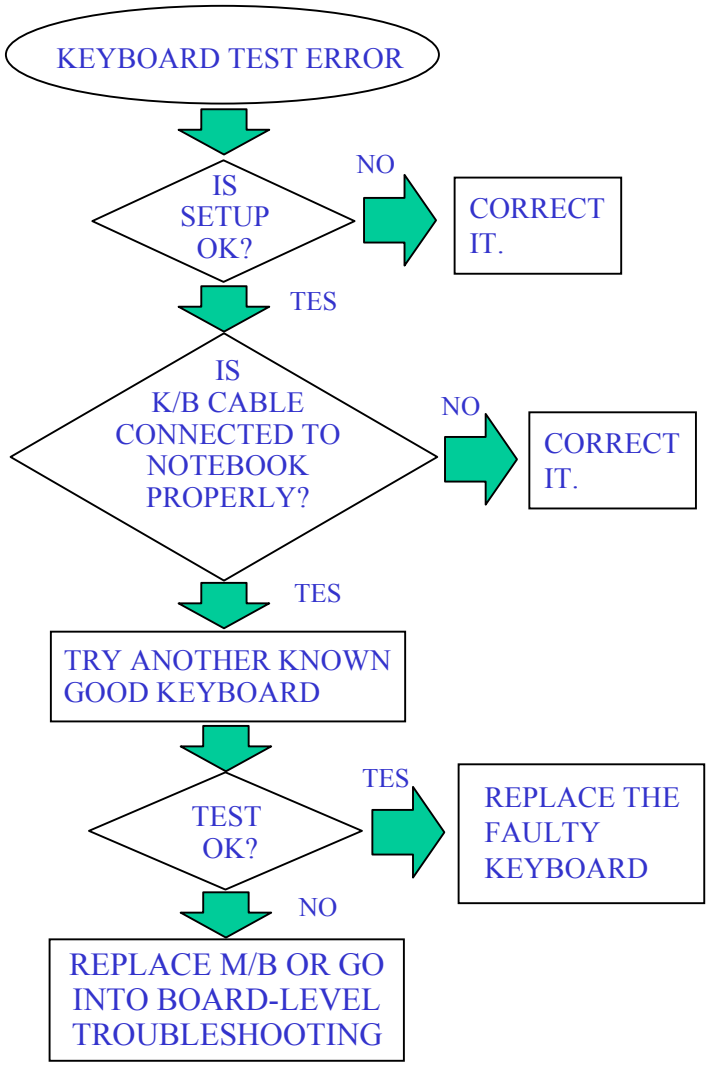


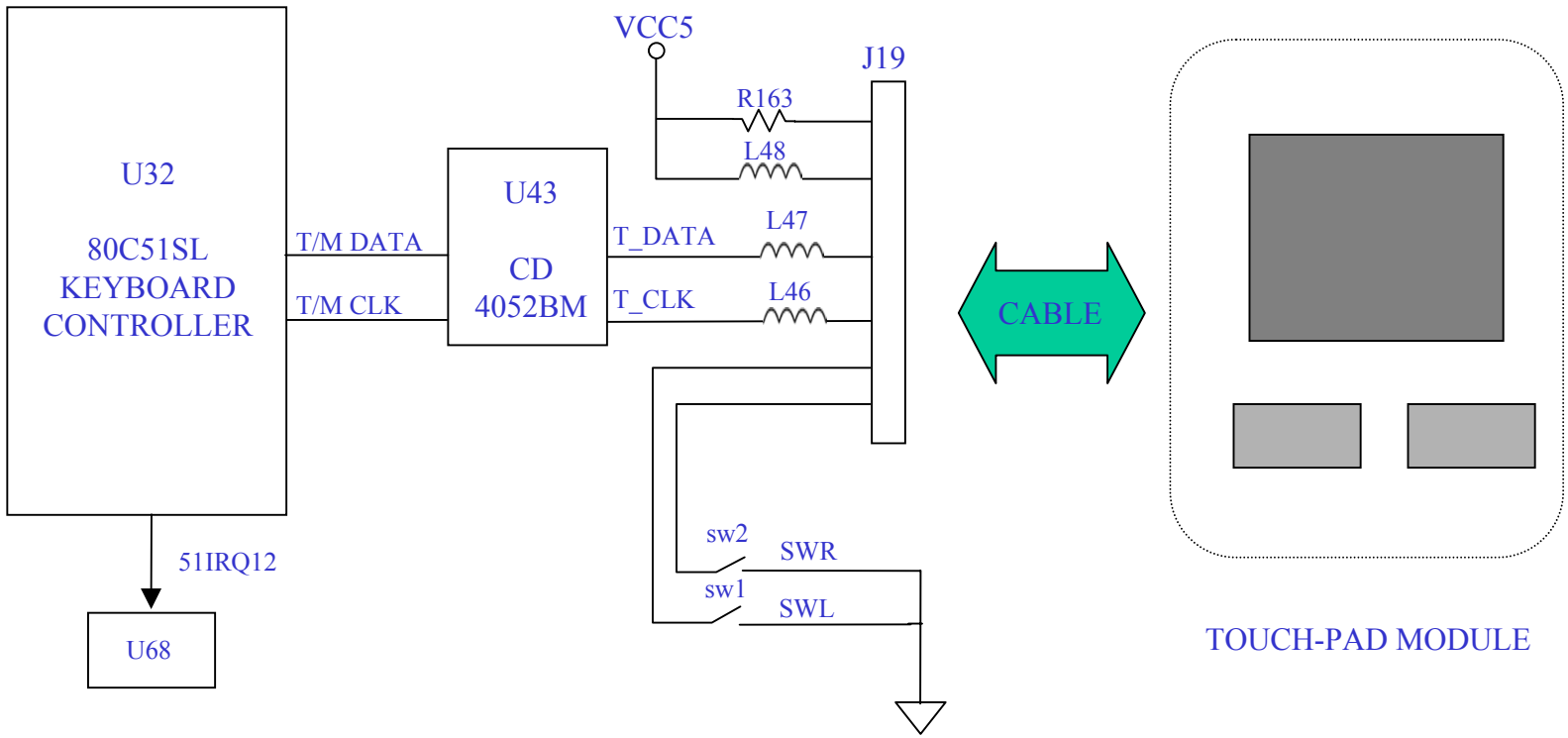
BOARD-LEVEL TROUBLESHOOTING FOR KEYBOARD TEST ERROR

CHECK THE FOLLOWING PARTS FOR COLD SOLDER OR ONE OF THE FOLLOWING PARTS ON THE MOTHER-BOARD MAY BE DEFECTIVE, USE AN OSCILLOSCOPE TO CHECK THE FOLLOWING SIGNAL OR REPLACE THE PARTS ONE AT A TIME AND TEST AFTER EACH REPLACEMENT.

PARTS:		SIGNALS:		
U32	L30	KI[0:7]	Y_DATA	SD[0:7]
U42	L24	KO[0:15]	Y_CLK	
U43	L27	KBDATA	51KBCS#	
J18	L29	MKBDATA	SA2	
J1001	L25	KBCLK	51IOWR#	
F3	EC13	MKBCLK	51IORD#	
	EC14	T/M DATA	51IRQ1	
		T/M CLK	51IRQ12	

9.8 TRACK PAD TEST ERROR

AN ERROR MESSAGE IS SHOWN WHEN TOUCH-PAD IS ENABLED.



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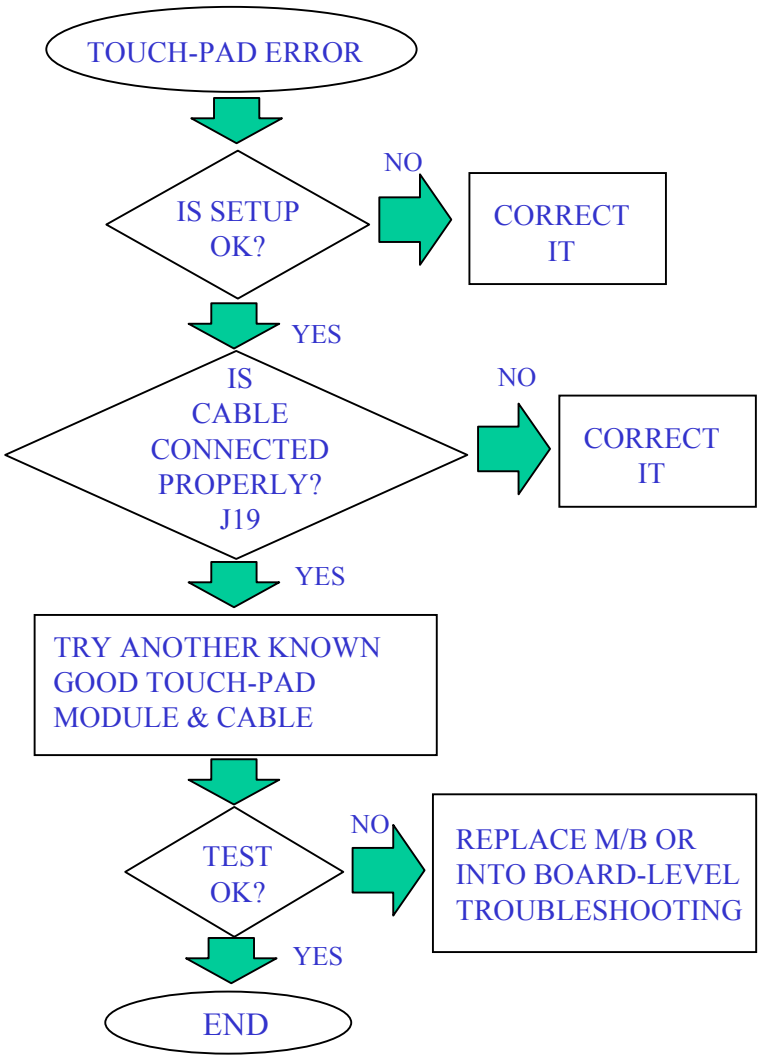


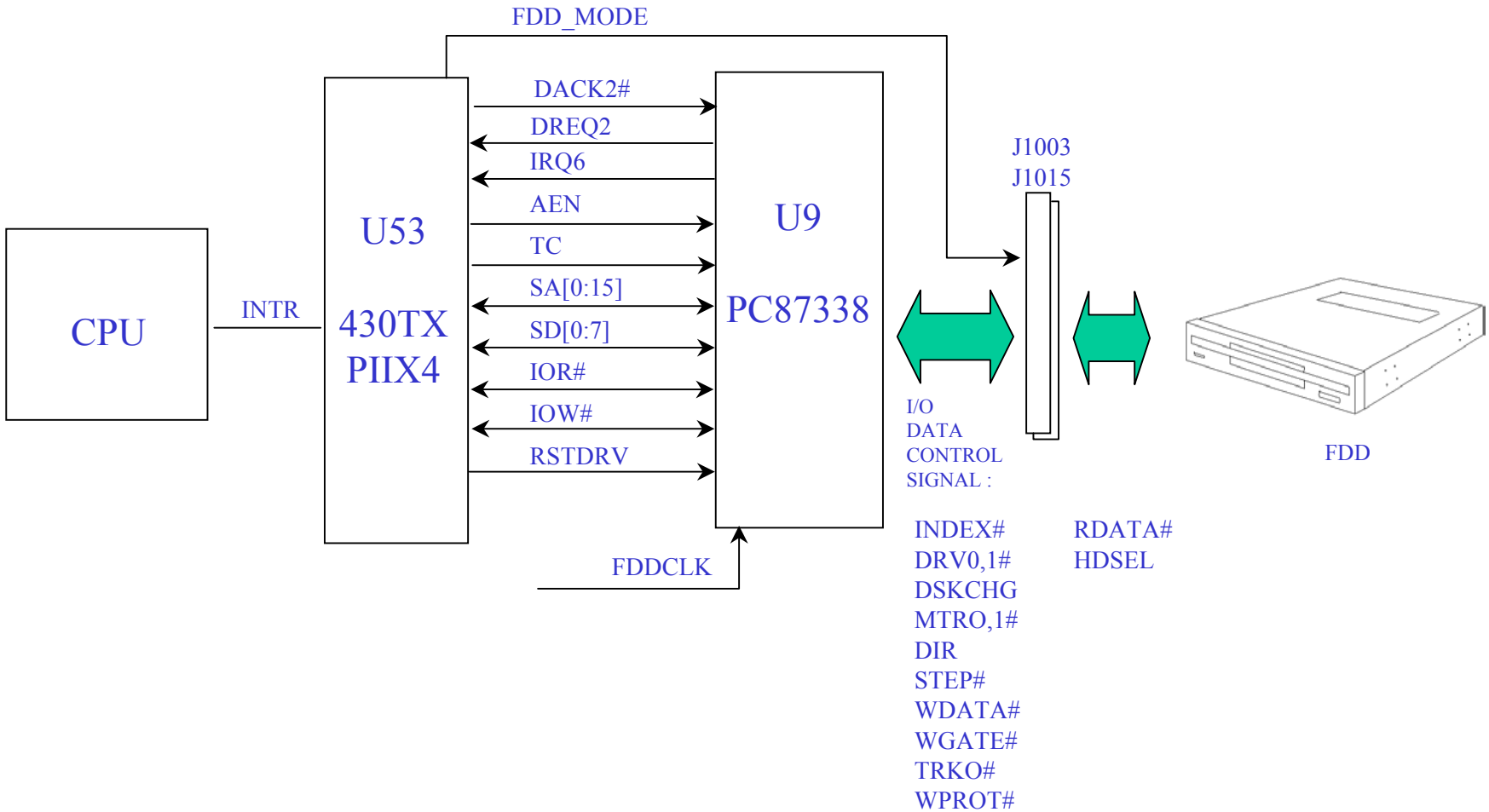
BOARD-LEVEL TROUBLESHOOTING FOR TOUCH-PAD TEST ERROR

CHECK THE FOLLOWING PARTS FOR COLD SOLDER OR ONE OF THE FOLLOWING PARTS ON THE MOTHER-BOARD MAY BE DEFECTIVE, USE AN OSCILLOSCOPE TO CHECK THE FOLLOWING SIGNAL OR REPLACE THE PARTS ONE AT A TIME AND TEST AFTER EACH REPLACEMENT.

PARTS:		SIGNALS:	
U32	SW1	T/M DATA	51IRQ12
U43	SW2	T/M CLK	VCC5
U68		T_DATA	
R163		T_CLK	
L48		SWR	
L47		SWL	
L46			

9.9 DISKETTE DRIVE TEST ERROR

AN ERROR MESSAGE IS SHOWN WHEN READING/ WRITING DATA FROM/TO DISKETTE DRIVE.



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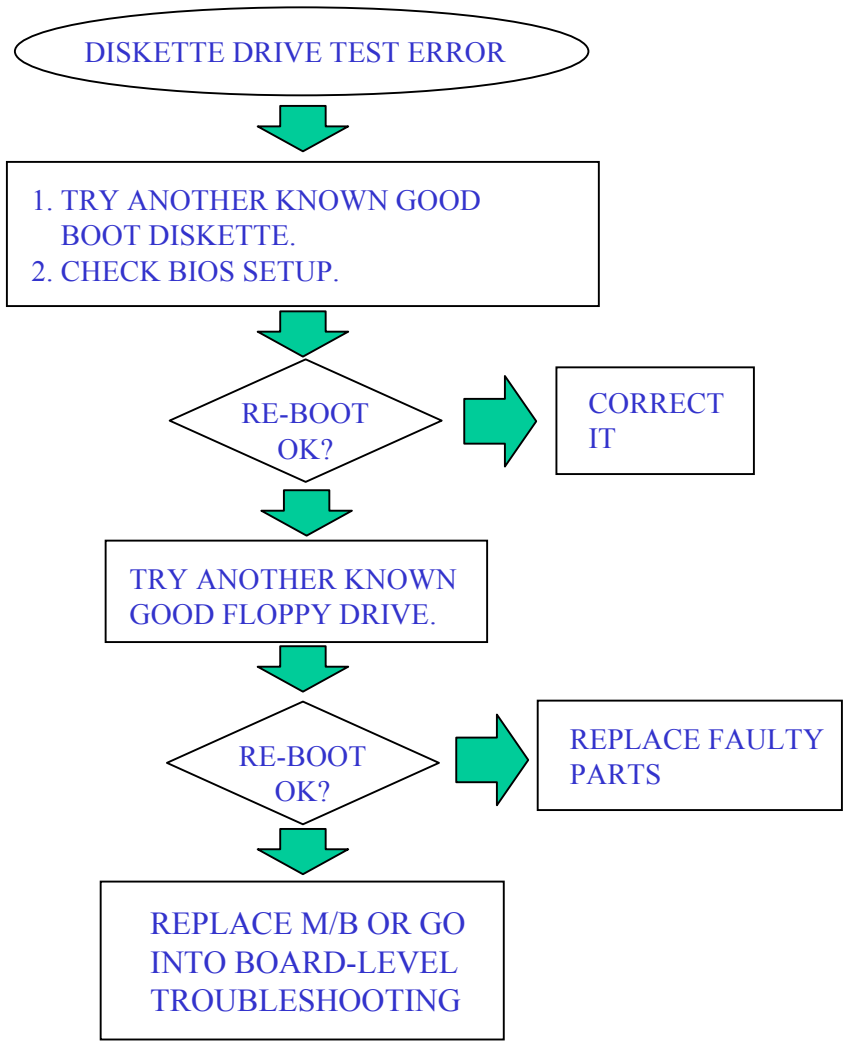


BOARD-LEVEL TROUBLESHOOTING FOR TOUCH-PAD TEST ERROR

CHECK THE FOLLOWING PARTS FOR COLD SOLDER OR ONE OF THE FOLLOWING PARTS ON THE MOTHER-BOARD MAY BE DEFECTIVE, USE AN OSCILLOSCOPE TO CHECK THE FOLLOWING SIGNAL OR REPLACE THE PARTS ONE AT A TIME AND TEST AFTER EACH REPLACEMENT.

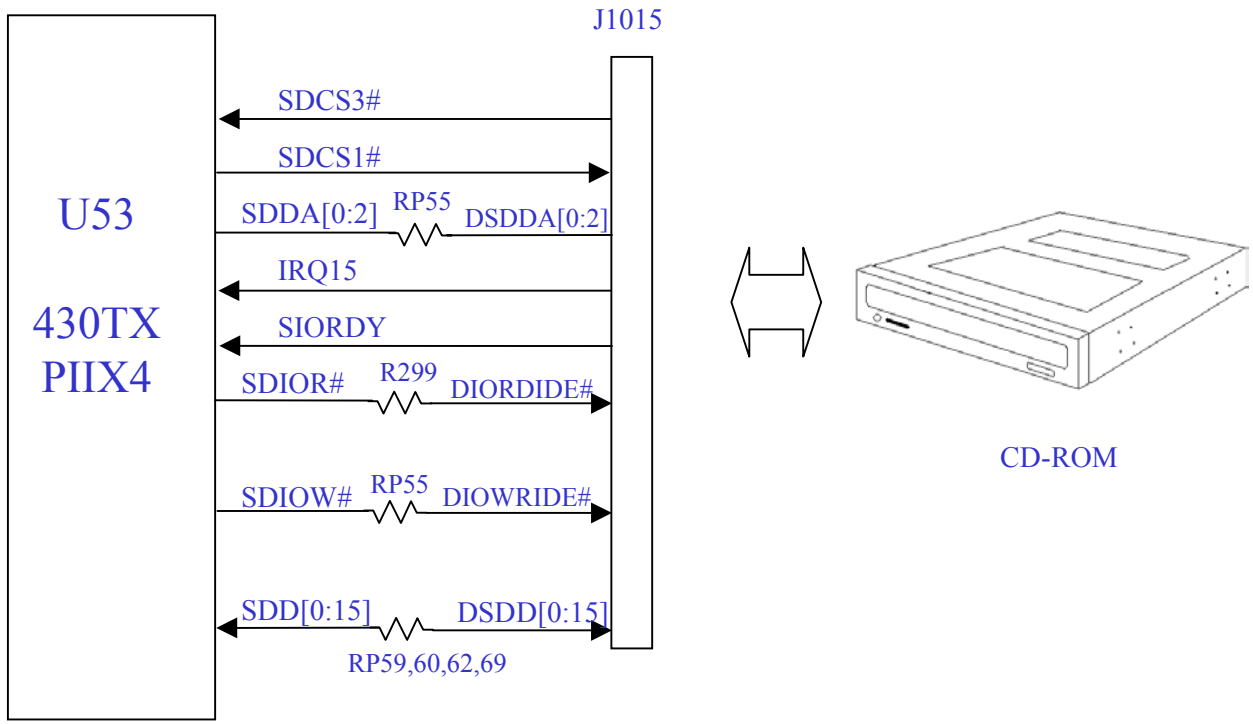
PARTS:
U53
U9
J1003
J1015

SIGNALS:

DACK2#	SD[0:7]
DREQ2	IOR#
IRQ6	IOW#
AEN	RSTDRV
TC	FDDCLK
SA[0:15]	

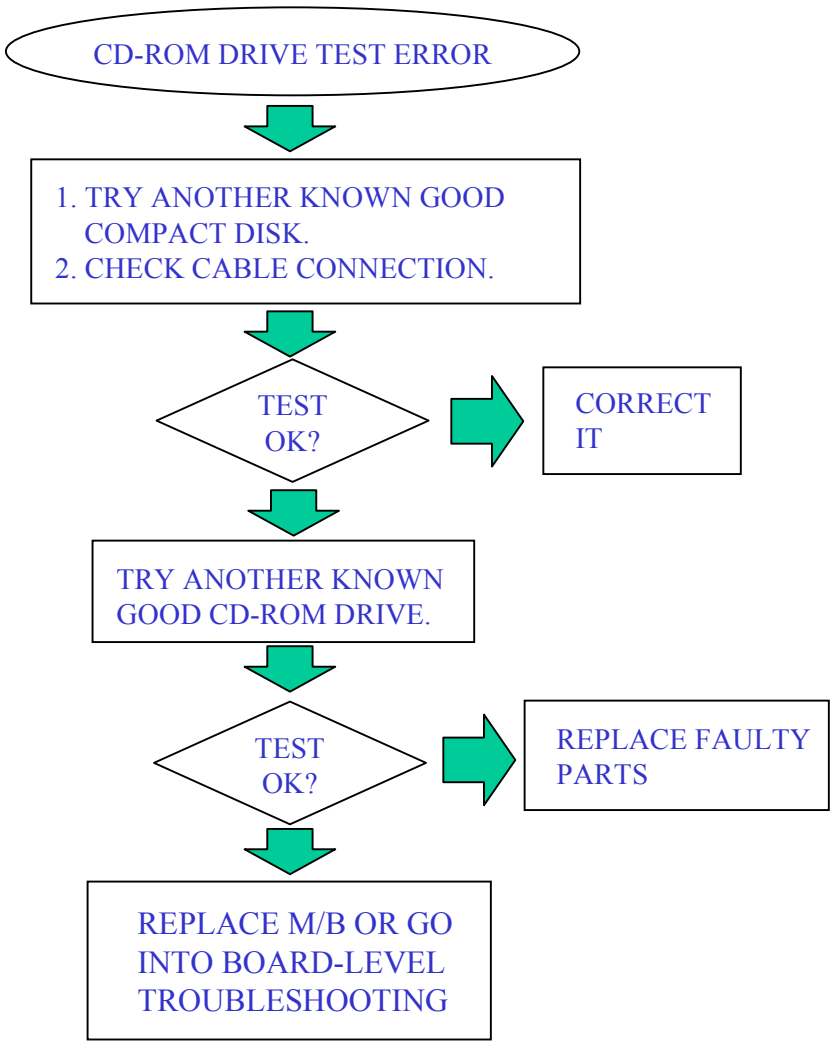
9.10 CD-ROM DRIVE TEST ERROR

AN ERROR MESSAGE IS SHOWN WHEN READING DATA FROM CD-ROM DRIVE.



9.10 CD-ROM DRIVE TEST ERROR

AN ERROR MESSAGE IS SHOWN WHEN READING GATA FROM CD-ROM DRIVE.



BOARD-LEVEL TROUBLESHOOTING FOR CD-ROM DRIVE TEST ERROR

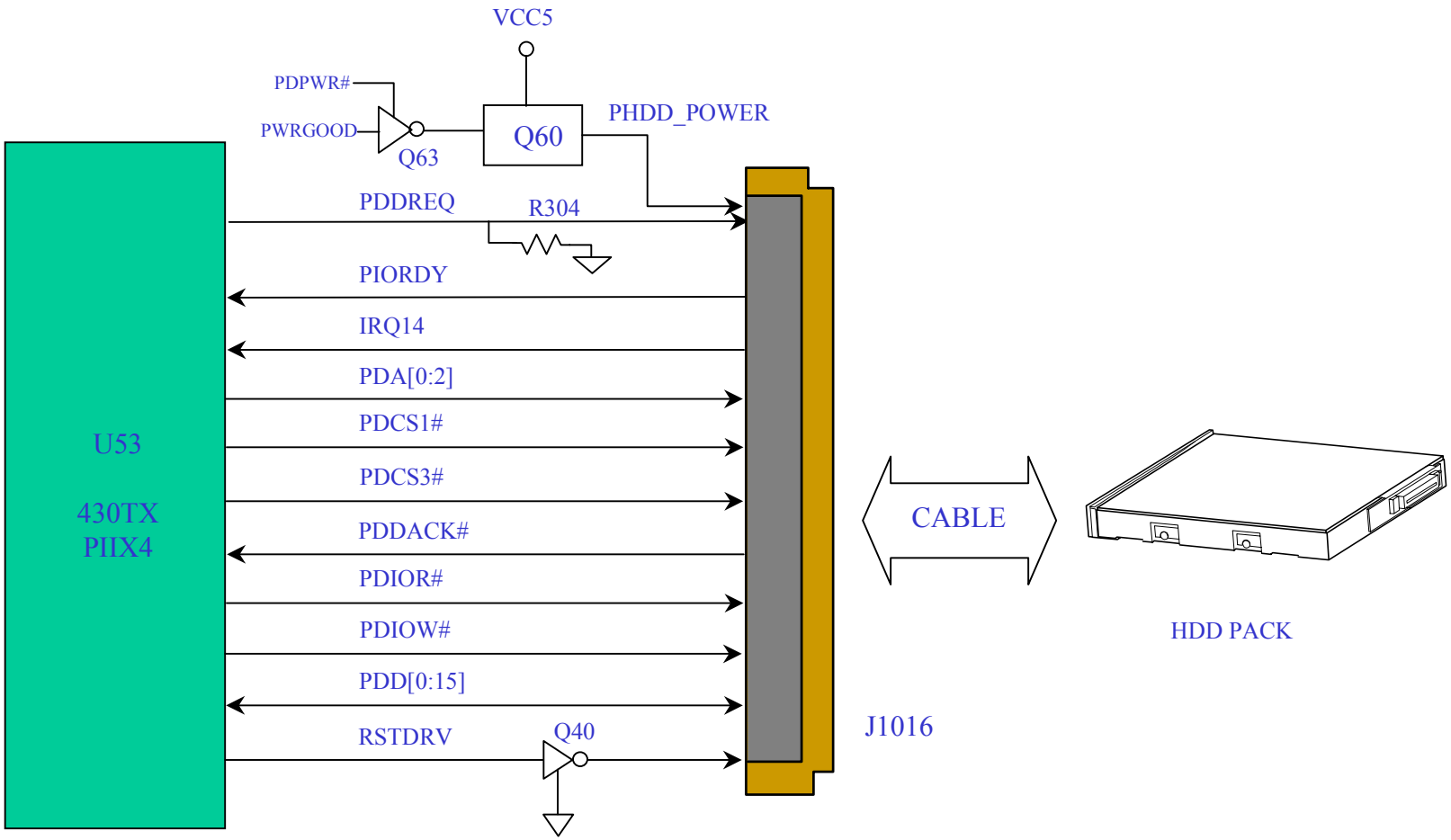
CHECK THE FOLLOWING PARTS FOR COLD SOLDER OR ONE OF THE FOLLOWING PARTS ON THE MOTHER-BOARD MAY BE DEFECTIVE, USE AN OSCILLOSCOPE TO CHECK THE FOLLOWING SIGNAL OR REPLACE THE PARTS ONE AT A TIME AND TEST AFTER EACH REPLACEMENT.

PARTS:
U53
J1015

SIGNALS:
SDCS3#
SDCS1#
SDDA2
SDDA1
SDDA0
IRQ15
SIORDY
SDIOR#
SDIOW#
SDD[0:15]

9.11 HARD DRIVE TEST ERROR

EITHER AN ERROR MESSAGE IS SHOWN , OR THE DRIVER MOTOR SPINS NON-STOP , WHILE READING DATA FROM OR WRITING DATA TO HARD-DISK.



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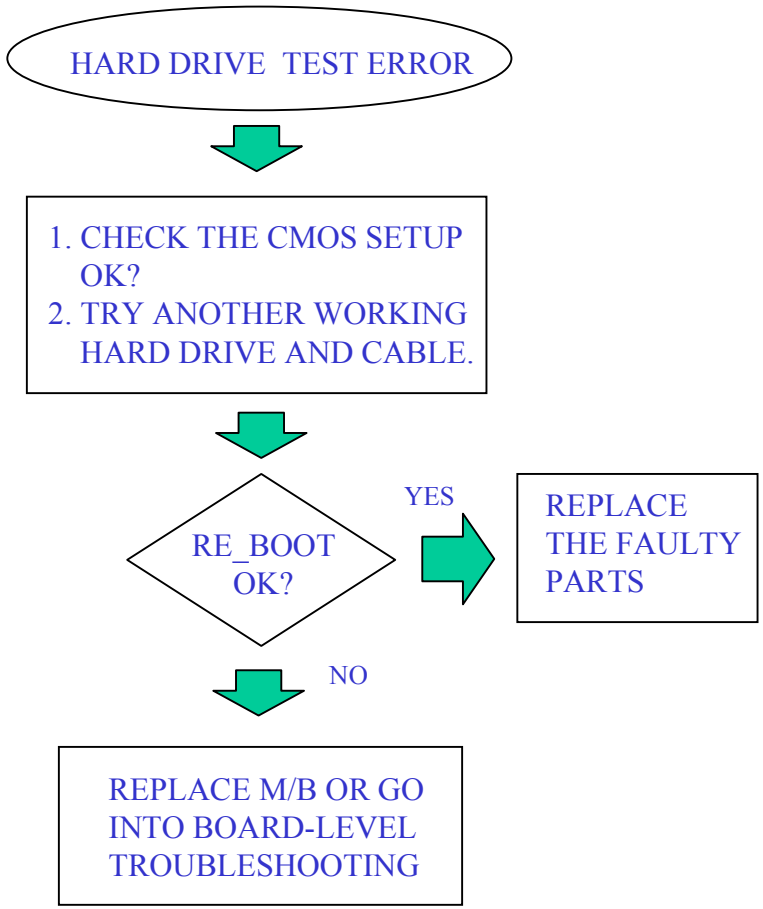


BOARD-LEVEL TROUBLESHOOTING FOR HARD DRIVE TEST ERROR

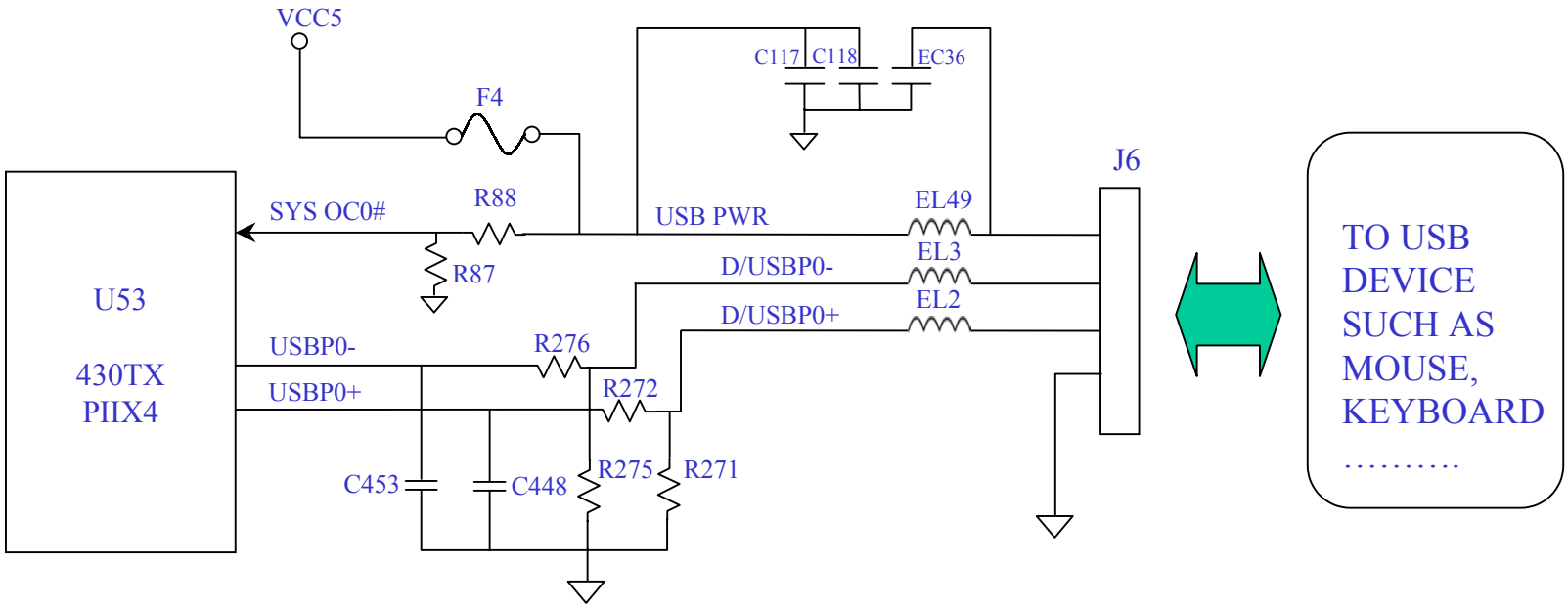
CHECK THE FOLLOWING PARTS FOR COLD SOLDER OR ONE OF THE FOLLOWING PARTS ON THE MOTHER-BOARD MAY BE DEFECTIVE, USE AN OSCILLOSCOPE TO CHECK THE FOLLOWING SIGNAL OR REPLACE THE PARTS ONE AT A TIME AND TEST AFTER EACH REPLACEMENT.

PARTS:
U53
Q63
Q60
Q40
R304
J1016

SIGNALS:
PDDREQ
PIORDY
IRQ14
PDA[0:2]
PDCS1#
PDCS3#
PDDACK#
PDIOR#
PDIOW#
PDD[0:15]
RSTDRV
VCC5
PHDD_POWER

9.12 USB PORT TEST ERROR

AN ERROR OCCURS WHEN A USB I/O DEVICE IS INSTALLED.



9.12 USB PORT TEST ERROR

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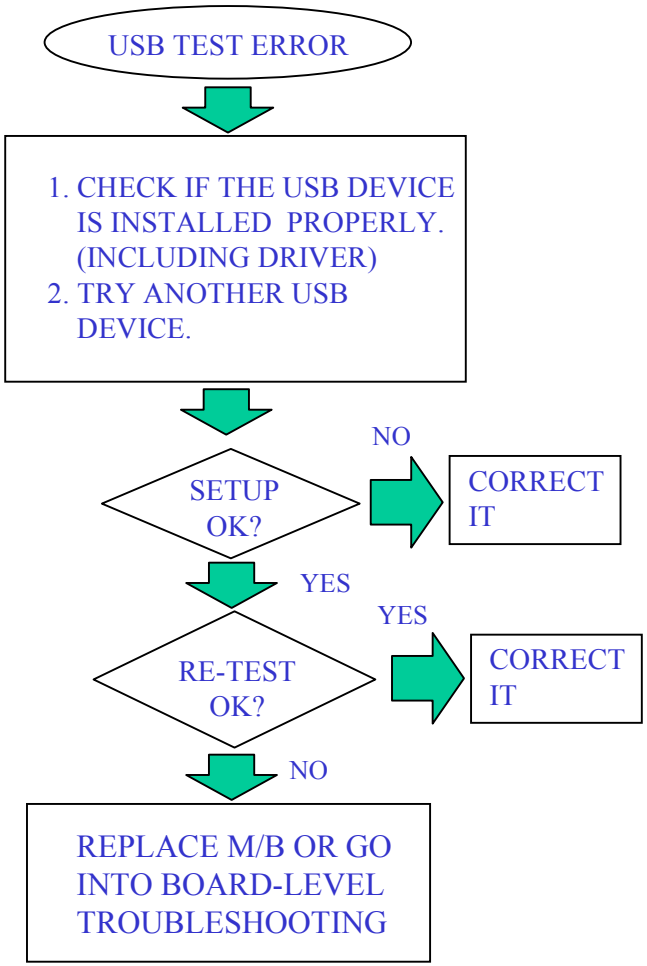

BOARD-LEVEL TROUBLESHOOTING FOR USB TEST ERROR

CHECK THE FOLLOWING PARTS FOR COLD SOLDER OR ONE OF THE FOLLOWING PARTS ON THE MOTHER-BOARD MAY BE DEFECTIVE, USE AN OSCILLOSCOPE TO CHECK THE FOLLOWING SIGNAL OR REPLACE THE PARTS ONE AT A TIME AND TEST AFTER EACH REPLACEMENT.

PARTS:

U53	R272
F4	R275
EL49	R271
EL3	C453
EL2	C448
R88	C117
R87	C118
R276	EC36

SIGNALS:
SYSOCO#
USBPO-
USBPO+
USB PWR

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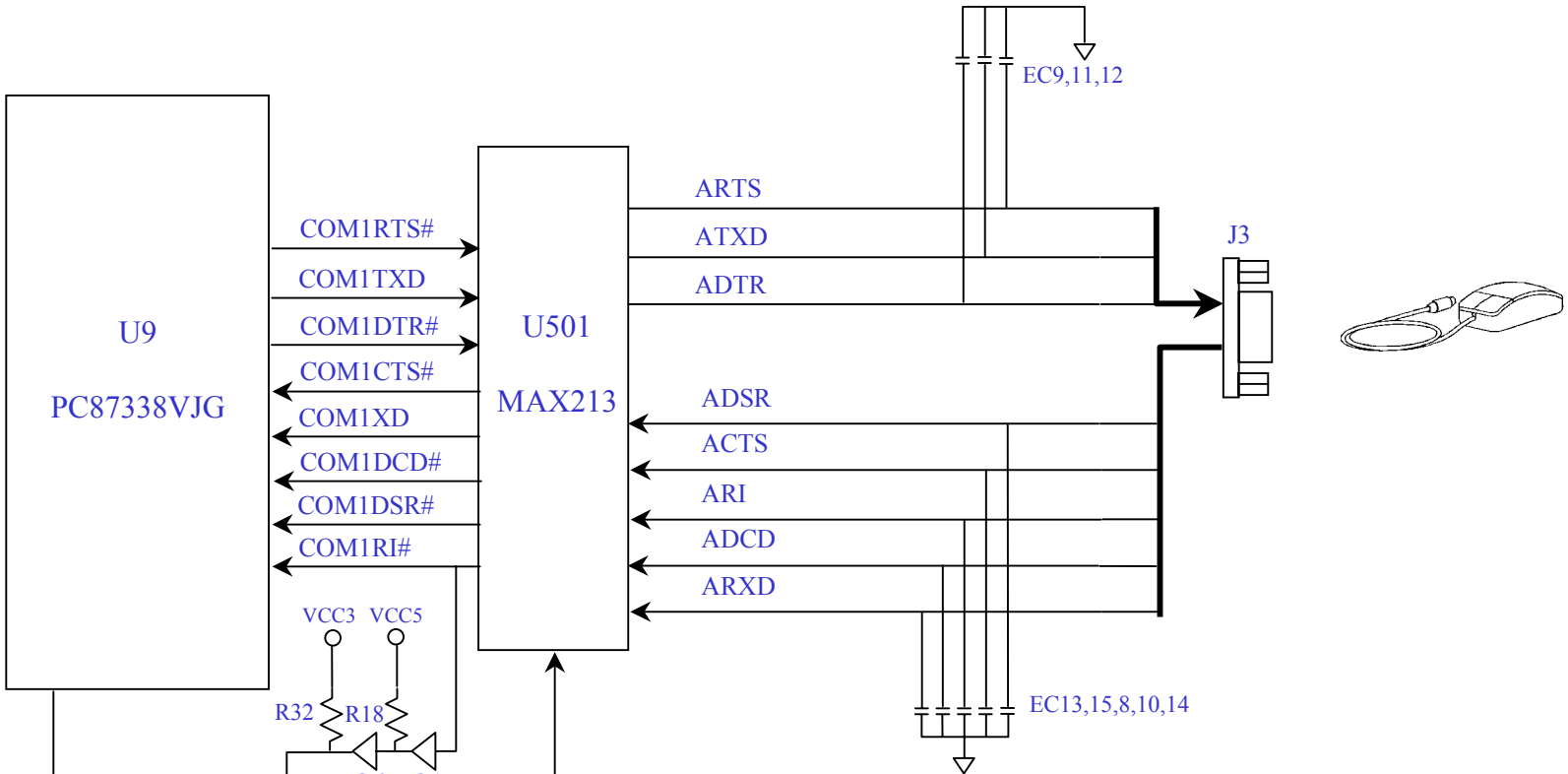
9.13 SIO PORT TEST ERROR

AN ERROR OCCURS WHEN A MOUSE OR OTHER I/O DEVICE IS INSTALLED.



PIN DEFINITION OF SIO PORT:

PIN 1 :	DCD-----	DATA CARRIER DETECT	PIN 6 :	DSR------	DATA SET READY
PIN 2 :	RD-------	RECEIVE DATA	PIN 7 :	RTS------	REQUEST TO SEND
PIN 3 :	TD-------	TRANSMIT DATA	PIN 8 :	CTS------	CLEAR TO SEND
PIN 4 :	DTR-----	DATA TERMINAL READY	PIN 9 :	RI--------	RING INDICATOR
PIN 5 :	SG--------	SIGNAL GROUND			

LOOPBACK CONNECTOR FOR SIO TEST:

PIN 1, 4, 6	SHORT
PIN 2, 3	SHORT
PIN 7, 8, 9	SHORT

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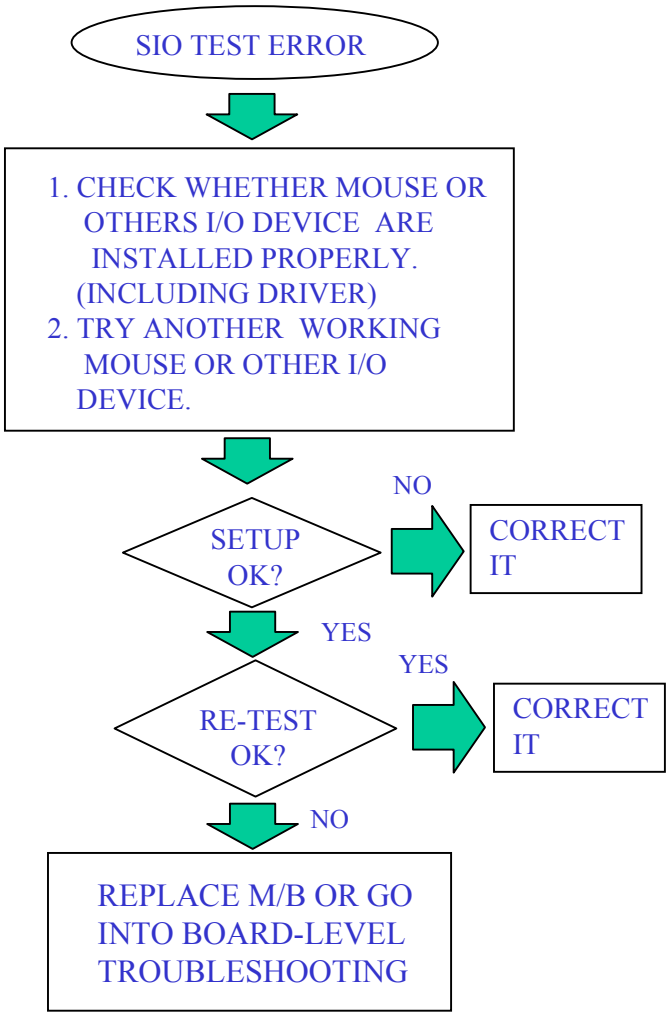
9.13 SIO PORT TEST ERROR

AN ERROR OCCURS WHEN A MOUSE OR OTHER I/O DEVICE IS INSTALLED.



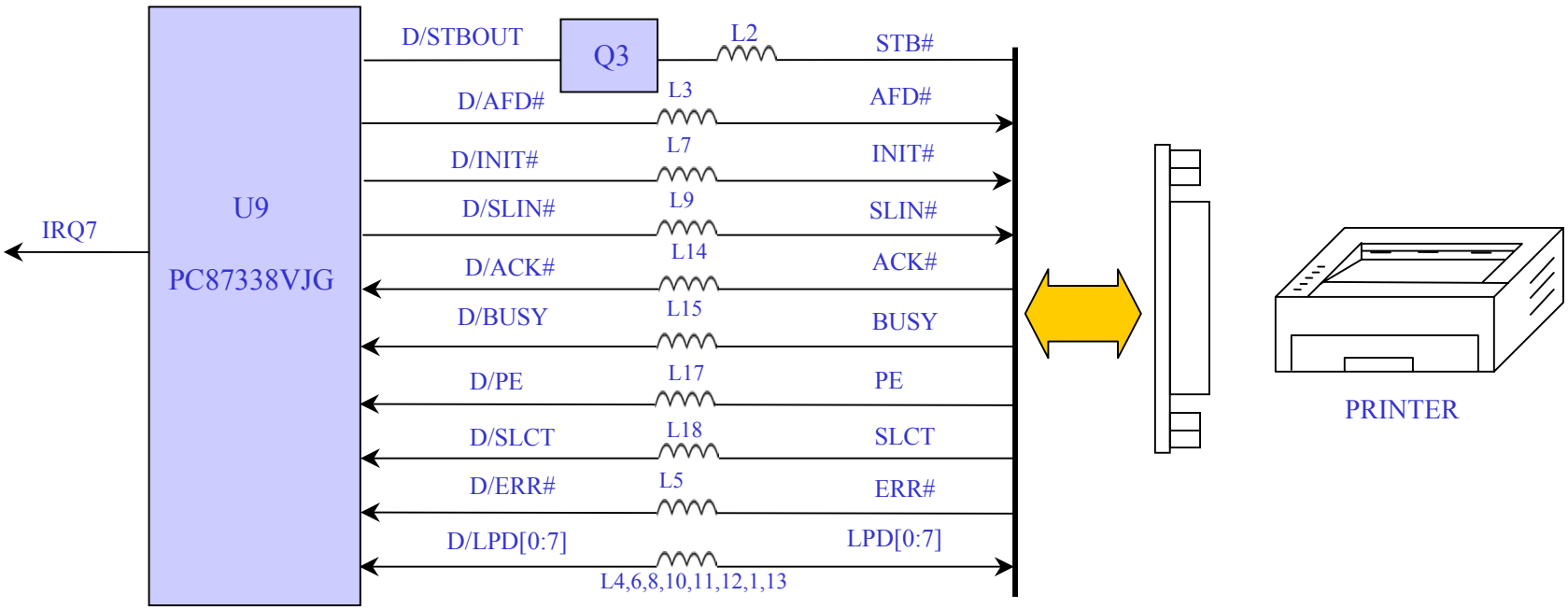
BOARD-LEVEL TROUBLESHOOTING FOR SIO TEST ERROR

CHECK THE FOLLOWING PARTS FOR COLD SOLDER OR ONE OF THE FOLLOWING PARTS ON THE MOTHER-BOARD MAY BE DEFECTIVE, USE AN OSCILLOSCOPE TO CHECK THE FOLLOWING SIGNAL OR REPLACE THE PARTS ONE AT A TIME AND TEST AFTER EACH REPLACEMENT.

PARTS:	SIGNALS:		
U9	IRQ4	COM1DSR#	TRXD
U501	IO OFF#	COM1RI#	COM1RIWAKE#
U53	COM1RTS#	ARTS	
Q6	COMETXD	ADTR	
Q1	COM1DTR#	ADSR	
R32	COM1CTS#	ACTS	
R18	COM1XD	ARI	
EC8~EC15	COM1DCD#	ADCD	

9.14 PIO PORT TEST ERROR

WHEN A PRINT COMMAND IS ISSUED, PRINTER PRINTS NOTHING OR GARBAGE.



PIN DEFINITION OF PIO PORT

PIN 1	STB	STROBE SIGNAL	PIN 14	AFD	AUTO LINE FEED
PIN 2-9	D0 -D7	PARALLEL PORT DATA BUS D0 TO D7	PIN 15	ERR	ERROR AT PRINTER
PIN 10	ACK	ACKNOW LEDGE HANDSHANK	PIN 16	INIT	INITIATE OUTPUT
PIN 11	BUSY	BUSY SIGNAL	PIN 17	SLIN	PRINTER SELECT
PIN 12	PE	PAPER END	PIN 18-25:		SIGNAL GROUND
PIN 13	SLCT	PRINTER SELECTED			

LOOPBACK CONNECTOR FOR PIO TEST:

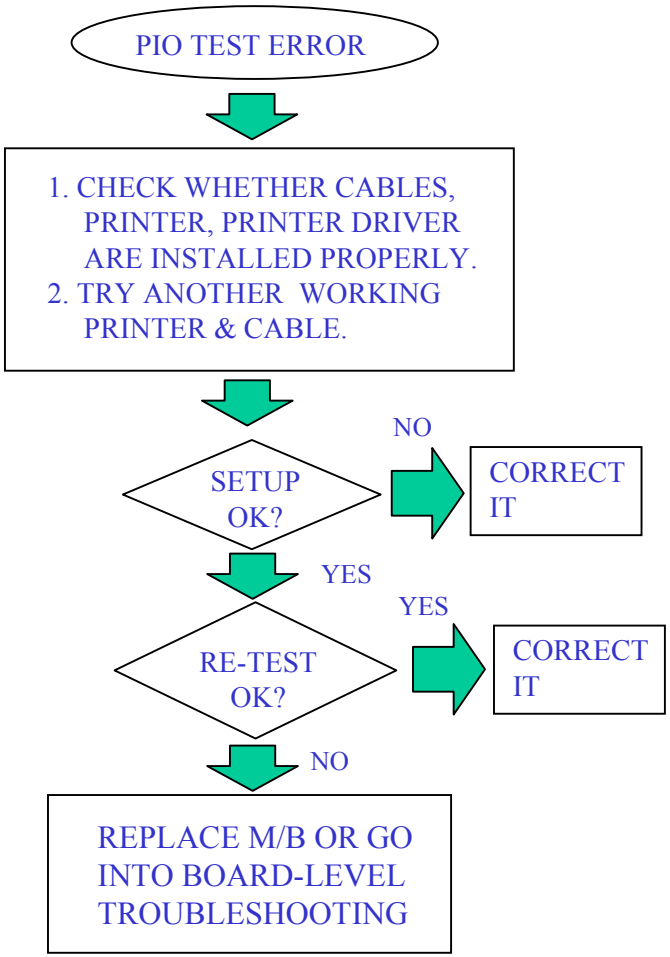
PIN 1,13	SHORT	PIN 10,16	SHORT
PIN 2,15	SHORT	PIN 11,17	SHORT
PIN 12,14	SHORT		

LOOPBACK CONNECTOR FOR EPP TEST:

PIN 1,2,4,6,8	SHORT
PIN 3,5,7,9,16	SHORT
PIN 18,19,20,21,22,23,24,25	SHORT

9.14 PIO PORT TEST ERROR

WHEN A PRINT COMMAND IS ISSUED, PRINTER PRINTS NOTHING OR GARBAGE.



BOARD-LEVEL TROUBLESHOOTING FOR PIO TEST ERROR

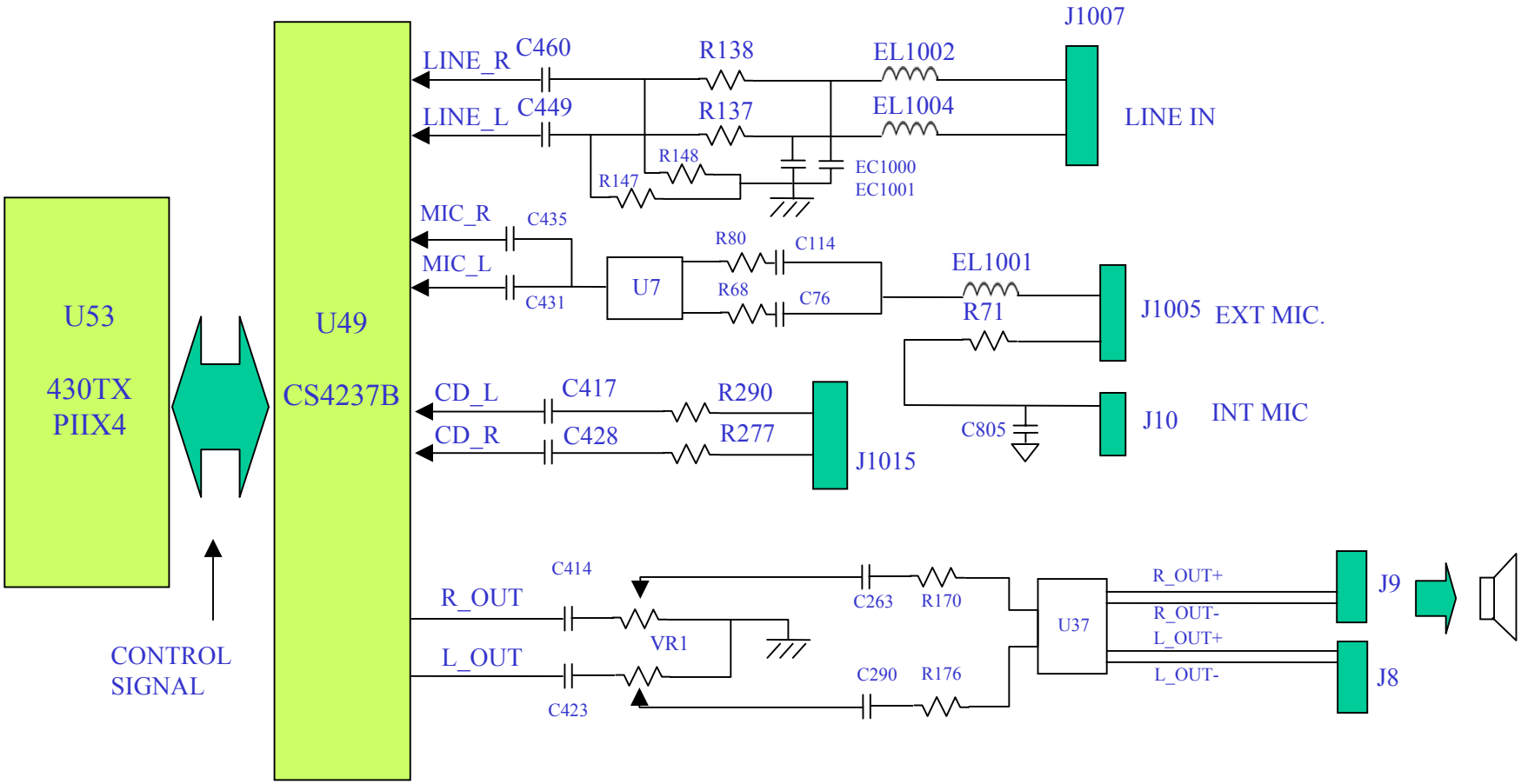
CHECK THE FOLLOWING PARTS FOR COLD SOLDER OR ONE OF THE FOLLOWING PARTS ON THE MOTHER-BOARD MAY BE DEFECTIVE, USE AN OSCILLOSCOPE TO CHECK THE FOLLOWING SIGNAL OR REPLACE THE PARTS ONE AT A TIME AND TEST AFTER EACH REPLACEMENT.

PARTS:
U9
Q3
L1~L15
L17,L18

SIGNALS:
STB#
AFD#
INIT#
SLIN#
ACK#
BUSY
PE
SLCT
ERR#
LP[0:7]
IRQ7
STB#_PH

9.15 AUDIO FAILURE

NO SOUND FROM SPEAKER AFTER AUDIO DRIVER IS INSTALLED.



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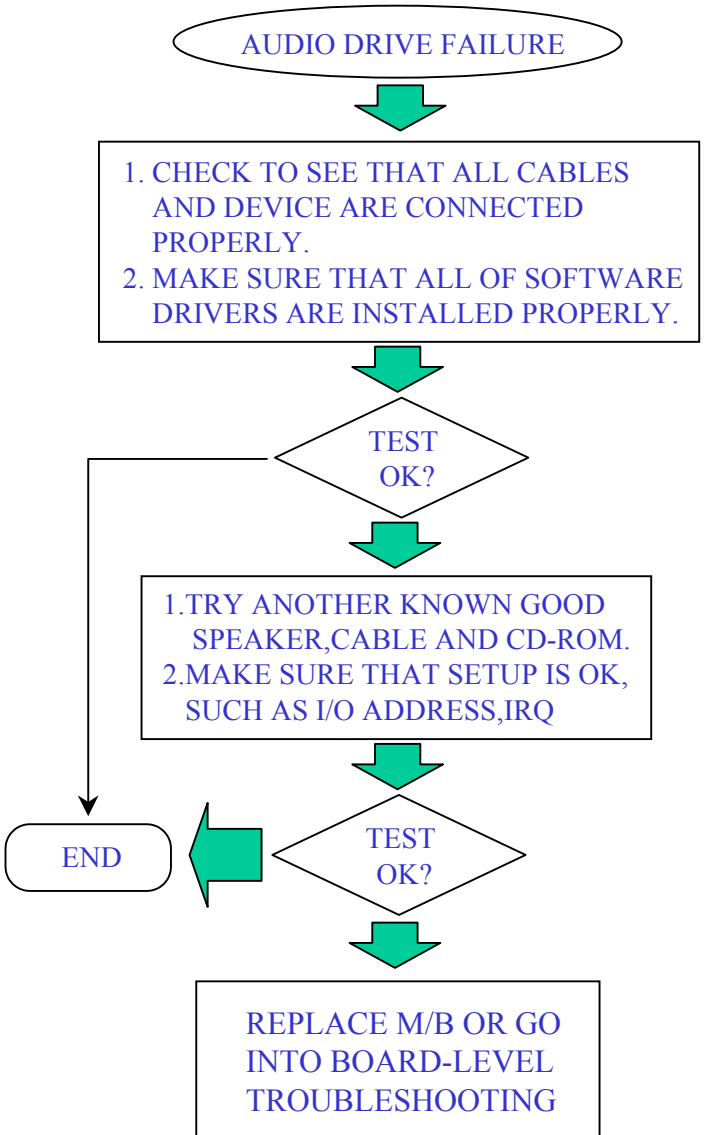

BOARD-LEVEL TROUBLESHOOTING FOR AUDIO TEST ERROR

CHECK THE FOLLOWING PARTS FOR COLD SOLDER OR ONE OF THE FOLLOWING PARTS ON THE MOTHERBOARD MAY BE DEFECTIVE, USE AN OSCILLOSCOPE TO CHECK THE FOLLOWING SIGNAL OR REPLACE THE PARTS ONE AT A TIME AND TEST AFTER EACH REPLACEMENT.

1.IF NO SOUND CAUSE OF LINE IN CHECK THE FOLLOWING PARTS & SIGNALS:

PARTS:		SIGNALS:
J1007	EC1000	LINE_R
EL1002	EC1001	LINE_L
EL1004		
R138		
R137		
C460		
C449		
R147		
R148		

2.IF NO SOUND CAUSE OF MIC CHECK THE FOLLOWING PARTS & SIGNALS:

PARTS:		SIGNALS:
J1005	C435	MIC_R
J10	C431	MIC_L
EL1001		
R71		
R80		
R68		
C114		
C76		
U7		

3.IF NO SOUND CAUSE OF CD-ROM CHECK THE FOLLOWING PARTS & SIGNALS:

PARTS:	SIGNALS:
J1015	CD_L
R290	CD_R
R277	
C417	
C428	

IF STILL GET PROBLEM ,PLEASE CHECK THE OUTPUT CIRCUIT PARTS & SIGNALS AS ABOVE PAGE SHOWN.

10. SPARE PARTS LIST-1

***** PC;5031N/TD-001-SC/EN-1 N/1 Spare Parts List *****

PART_NO	DESCRIPTION	LOCATION
526266510002	PC;5031N/TD-001-SC/EN-1 N/1	
340665100007	COVER ASSY A;LED,5031	
344665100022	LENS;LED LENS,5031	
344665100026	COVER;LED COVER,5031	
345665100007	PAD;MICROPHONE PAD,5031	
431665100021	CASE KIT;5031	
340665100020	HOUSING ASSY;BOTTOM CASE,5031	
341664700006	SPRING PLATE;FOOT,BTM CASE,5026	
341664700007	SPRING;SLIDE,BTM CASE,5026	
341664700010	SPRING;CHANGE,BTM CASE,5026	
341664700021	SPRING-WASHER;BTM CASE,5026	
341664700023	SPRING PLATE;BASE,BTM,5026	
341665100004	SPRING;LCD HOOK SPRING,5031	
342664700024	SCREW;M3,FOOT,BTM CASE,5026	
343665100003	BRKT;FAN SUPPORT,5031	
344664700047	FOOT;R,BTM CASE,5026	
344664700048	FOOT;L,BTM CASE,5026	
344664710068	DOOR;CHANGE,B-CASE,1,5026	
344664800021	HOOK;SLIDE,HOUSING,PITCHING	
344665100002	HOUSING;BOTTOM CASE,5031	
344665100005	BUTTON;MODULE LOCK BUTTON,5031	
344665100010	BUTTON;POWER BUTTON,5031	
344665100016	BUTTUN;LCD HOOK BUTTUN,5031	
345665100012	CONDTIVE SPONGE;I/O SLOT(L),5031	
345665100013	CONDTIVE SPONGE;I/O SLOT(R),5031	
345665100014	CONDTIVE SPONGE;I/O BRKT,5031	
345665200004	FOOT;PAD,PITCHING3	
345665100018	CONDTIVE SPONGE;VEDIO,5031	
346665100008	INSULATOR;FAN BRKT,5031	
345665100016	PAD;FOOT PAD(REAR),5031	
340665100013	COVER ASSY;REAR,5031	
344665100023	COVER;DOCKING COVER,5031	

PART_NO	DESCRIPTION	LOCATION
344665100027	COVER;REAR COVER,5031	
431665100001	TOP CABINET ASSY;5031	
340665100021	COVER ASSY;TOP CASE,#1,5031	
342665200031	FINGER;H/S,COVER,PITCHING3	
343665100001	SUPPORT;K/B SUPPORT,5031	
344665100001	COVER;TOP CASE,5031	
344665100017	LENS;IR LENS,5031	
345665100010	CONDTIVE SPONGE;I/O SLOT,5031	
345665100011	CONDTIVE SPONGE;KEYBOARD,5031	
345665200017	CONDTIVE SPONG;AUDIO,PITCHING3	
345665200019	CONDTIVE SPONG;HINGE,PITCHING3	
371102610303	SCREW;M2.6L3,K-HEAD(+),NIW	TOP CASE TO K/B
343665100002	HEATSINK;VGA,M/B,5031	
344665100014	HOLDER;T/P HOLDER,5031	
370102610602	SPC-SCREW;M2.6 L6,NIB,K-HD,727	T/P HOLDER TO TOP
421664700071	FFC ASSY;TOUCH PAD,UPPER CASE,50	
421665100031	MICROPHONE ASSY;5031	
421664900001	WIRE ASSY;COVER SWITCH,5027	
421665100051	SPEAKER ASSY;LEFT,5031	
339111100004	SPEAKER ASSY;LEFT,5031	
342665100001	BRKT;SPEAKER BRACKET(L),5031	
370102610602	SPC-SCREW;M2.6 L6,NIB,K-HD,727	SPK/BKT
421665100052	SPEAKER ASSY;RIGHT,5031	
339111100003	SPEAKER ASSY;RIGHT,5031	
342665100002	BRKT;SPEAKER BRACKET(R),5031	
370102610602	SPC-SCREW;M2.6 L6,NIB,K-HD,727	SPK/BKT
442110500005	TOUCH PAD MODULE;904236-0000,502	
345665100004	PAD;SPK WIRE PAD,5031	
421664900062	CABLE ASSY;ESD TOUCH PAD,5027	
345665100015	PAD;T/P BUTTON SUPPORT PAD,5031	
442664700002	AC ADPT ASSY;5026 RFC	
451665100001	ME KIT;SYSTEM,5031	

10. SPARE PARTS LIST-2

PART_NO	DESCRIPTION	LOCATION
342665100006	HEATSINK;W/FAN,5031	
344665100008	COVER;HINGE COVER(L),5031	
344665100009	COVER;HINGE COVER(R),5031	
340665100017	COVER ASSY;CPU,5031	
344665100018	COVER;CPU COVER,5031	
346665100007	MESH;FAN MESH,5031	
344665100019	COVER;MODEM COVER,5031	
344665100024	COVER;AUDIO COVER,5031	
346665200004	THERMAL PAD;UP,CPU,PITCHING3	
370102610401	SPC-SCREW;M2.6L4,NIB,727,NLK	COVER TO I/Ox2
370102610602	SPC-SCREW;M2.6 L6,NIB,K-HD,727	
371102031500	SCREW;M2L15,PAN(+),NIW	
370102610801	SPC-SCREW;M2.6L8,NIB,K-HD,NYLOCK	
342665200029	COVER;DRAM,PITCHING3	
344665100032	COVER;MODEM CON. COVER,5031	
346665100005	WASHER;MODEM COVER WASHER,5031	
342665100007	BRKT;LCD CABLE(R),5031	
342665100008	BRKT;LCD CABLE(L),5031	
371102612201	SCREW;M2.6L22,K HEAD	
222600020023	PE BAG;120*170MM,W/SEAL,COMMON	
222600020049	PE BAG;50*70MM,W/SEAL,COMMON	
451665100002	ME KIT;MAIN BD,5031	
340665200008	PAD ASSY;MB,PITCHING3	
341664700013	SHIELDING;PS/2,M/B,5026	
341665100003	BRKT;PORT BRACKET,5031	
342664800009	STANDOFF;DOCKING,PITCHING	
346665100002	INSULATOR;PCMCIA,5031	
346665200002	INSULATOR;D/D,PITCHING3	
346665200003	INSULATOR;M/B,UP,PITCHING3	
346665200010	INSULATOR;LED M/B,PITCHING3	
343665100004	PLATE;D/D T-WIN,5031	
346665200013	INSULATOR;DOCKING,PITCHING3	

PART_NO	DESCRIPTION	LOCATION
370102610401	SPC-SCREW;M2.6L4,NIB,727,NLK	LED/B TO /MBx1
375120262008	NUT-HEX;M2.6,NIW	
377102610001	STANDOFF;M2,6DP3.5H5L5,NYLOK	
377244010002	STANDOFF;#4-40DP3.5H5L5.5,NIW	
377102610004	STANDOFF;M2.6DP12.4H14.9L5,NYLOK	
411665100001	PWA;PWA-5031 MOTHER BD	
242600000001	LABEL;PAL,20*5MM,COMMON	
242600000145	LABEL;10*10,BLANK,COMMON	
242600000170	LABEL;PCMCIA CARD WORKS/95 EN	
242600000195	LABEL;PENTIUM-BP,SYSTEMSOFT BIOS	
338530010009	BATTERY;LI,3V/195mAH,BR2032	
344600000215	IC CARD CON PART;160P,55150-1605	
370102010502	SPC-SCREW;M2 L5,NIB,K-HD,727	
371102011201	SCREW;M2 L12,FLT(+),NIW	
371102510402	SCREW;M2.5L4,FLT(+),NIW	
411665100002	PWA;PWA-5031 M/B T/U BD	
313000510003	FILTER;4LINE,360OHM/100MHZ,8P	L1011
331040010002	CON;HDR,MA,10P,2MM,R/A,SUYIN	J1010,1013
331030003004	CON;HDR,MA,3P*1,2.54MM,ST	J14
331190002001	JUMPER;2P*1,2MM,MINI,GOLD FLUSH	
331210020401	CON;EDGE,204P,1.0MM,R/A,AMP	J7
331650029606	IC SOCKET;296P,ZIF,ZIFPGAFC	U702
331720009004	CON;D,MA,9P,2.775,R/A	J3
331720015006	CON;D,FM,15P,2.29,R/A,3ROW	J2
331720025005	CON;D,FM,25P,2.775,R/A	J4
331840005002	CON;STEREO JACK,5P,R/A,D3.6,2 SW	J1005,1007,1009
331872706019	CON;DIN,SKT,6P,MINI,R/A,PCB MT	J1001
331910003003	CON;POWER JACK,3P,16VDC/3A	J1
331910003006	CON;POWER JACK,3P,6.3VDC/2A	J1004
337120124001	SW;DIP,SPST,2P,25VDC,24MA,HDK632	SW1000
338000000008	BATTERY HOLDER;BH32T,5031	BT1000
411665100005	PWA;PWA-5031 V1 SMT MOTHER BD	

10. SPARE PARTS LIST-3

PART_NO	DESCRIPTION	LOCATION
271002000301	RES;0 ,1/10W,5% ,0805,SMT	R150,115,
271012000301	RES;0 ,1/8W,5% ,1206,SMT	R118,1016,1019,
271012202301	RES;2K ,1/8W,5% ,1206,SMT	R340
271012561301	RES;560 ,1/8W,5% ,1206,SMT	R334
271013100301	RES;10 ,1/4W,5% ,1206,SMT	R309,310,353
271071100302	RES;10 ,1/16W,5% ,0603,SMT	R28,175,235,194
271071000002	RES;0 ,1/16W,0603,SMT	R25,71,82,123,130
271071101301	RES;100 ,1/16W,5% ,0603,SMT	R27,159,206
271071102302	RES;1K ,1/16W,5% ,0603,SMT	R14,36,103,129,273
271071103302	RES;10K ,1/16W,5% ,0603,SMT	R1,79,94,96,110
271071102311	RES;102K ,1/16W,1% ,0603,SMT	R16
271071104101	RES;100K ,1/16W,1% ,0603,SMT	R345,108,157,207,17
271071104302	RES;100K ,1/16W,5% ,0603,SMT	R7,13,42,31
271071105101	RES;1M ,1/16W,1% ,0603,SMT	R49,162,220
271071111101	RES;110 ,1/16W,1% ,0603,SMT	R60
271071153301	RES;15K ,1/16W,5% ,0603,SMT	R264,267,271,275,
271071202301	RES;2K ,1/16W,5% ,0603,SMT	R261
271071203101	RES;20K ,1/16W,1% ,0603,SMT	R95,100,101,131,224,
271071221301	RES;220 ,1/16W,5% ,0603,SMT	R119
271071221302	RES;22 ,1/16W,5% ,0603,SMT	R120,186,202,243
271071222302	RES;2.2K ,1/16W,5% ,0603,SMT	R29,30,1003
271071223302	RES;22K ,1/16W,5% ,0603,SMT	R68,109,85,1002
271071224301	RES;220K ,1/16W,5% ,0603,SMT	R116,232,1057
271071242301	RES;2.4K ,1/16W,5% ,0603,SMT	R295,279
271071249311	RES;249K ,1/16W,1% ,0603,SMT	R114
271071270301	RES;27 ,1/16W,5% ,0603,SMT	R272,276
271071273301	RES;27K ,1/16W,5% ,0603,SMT	R348
271071301311	RES;301K ,1/16W,1% ,0603,SMT	R208,158
271071303301	RES;30K ,1/16W,5% ,0603,SMT	R258,253
271071330302	RES;33 ,1/16W,5% ,0603,SMT	R61,84,89,121,
271071332302	RES;3.3K ,1/16W,5% ,0603,SMT	R237
271071333301	RES;33K ,1/16W,5% ,0603,SMT	R226,227,306,1004,

PART_NO	DESCRIPTION	LOCATION
271071470301	RES;47 ,1/16W,5% ,0603,SMT	R244,245
271071471302	RES;470 ,1/16W,5% ,0603,SMT	R307
271071472302	RES;4.7K ,1/16W,5% ,0603,SMT	R8,51,107,259,328
271071473301	RES;47K ,1/16W,5% ,0603,SMT	R91-93,372,325
271071474301	RES;470K ,1/16W,5% ,0603,SMT	R371,1058
271071499111	RES;4.99K,1/16W,1% ,0603,SMT	R189,204
271071562301	RES;5.6K ,1/16W,5% ,0603,SMT	R167,219,147,148
271071563302	RES;56K ,1/16W,5% ,0603,SMT	R278,294
271071564301	RES;560K ,1/16W,5% ,0603,SMT	R87,300
271071680301	RES;68 ,1/16W,5% ,0603,SMT	R104-106
271071682101	RES;6.8K ,1/16W,1% ,0603,SMT	R252,256,
271071683301	RES;68K ,1/16W,5% ,0603,SMT	R288
271071750101	RES;75 ,1/16W,1% ,0603,SMT	R3-5,266,1011
271611000301	RP;0*4 ,8P ,1/16W,5% ,0612,SMT	RP54
271611100301	RP;10*4 ,8P ,1/16W,5% ,0612,SMT	RP33,34,36,37,39,40
271611102301	RP;1K*4 ,8P ,1/16W,5% ,0612,SMT	RP73
271611103301	RP;10K*4 ,8P ,1/16W,5% ,0612,SMT	RP5,43,46,50,57,65,
271611104301	RP;100K*4,8P ,1/16W,5% ,0612,SMT	RP31,42,44
271611203301	RP;20K*4 ,8P ,1/16W,5% ,0612,SMT	RP702,703
271611220301	RP;22*4 ,8P ,1/16W,5% ,0612,SMT	RP28,30
271611222301	RP;2.2K*4,8P ,1/16W,5% ,0612,SMT	RP12
271611330301	RP;33*4 ,8P ,1/16W,5% ,0612,SMT	RP2-4,6-8,14-16,21,
271611472301	RP;4.7K*4,8P ,1/16W,5% ,0612,SMT	RP11
271621102303	RP;1K*8 ,10P,1/16W,5% ,1206,SMT	RP9,70
271621103303	RP;10K*8 ,10P,1/16W,5% ,1206,SMT	RP1,24-26,29,32,45,
271621472303	RP;4.7K*8,10P,1/16W,5% ,1206,SMT	RP17,23,61,63,64,66,
271911103901	VR;10K ,.05W,20%,XV0102GPH1N-93	VR1
272002105701	CAP;1U ,CR,16V ,-20+80%,0805,SM	C169,281,282,344,
272003224701	CAP;.22U ,CR,25V ,+80-20%,0805,Y	C286,289,413,804
272005473401	CAP;.047U,CR,50V,10%,0805,X7R	C263,290
272012225702	CAP;2.2U ,CR,16V ,+80-20%,1206,Y	C191,268,309,311,
272012335701	CAP;3.3U ,CR,16V ,-20+80%,1206,S	C331

10. SPARE PARTS LIST-4

PART_NO	DESCRIPTION	LOCATION
272012475701	CAP;4.7U ,CR,16V ,+80-20%,1206,Y	C418,475,516
272015474501	CAP;.47U ,CR,50V,20%,1206,Z5U	C527,538
272022106701	CAP;10U ,16V,+80-20%,1210,Y5V,S	C23,28,29,33,43
272072104702	CAP;.1U ,16V,+80-20%,0603,SMT	C15,16,18,20,26,27
272072221301	CAP;220P ,16V,5% ,-30+85'C,0603,	C380,393,513,EC48
272073180401	CAP;18P ,CR,25V ,10%,0603,NPO,S	C6,270,271,442,451
272075100401	CAP;10P ,50V ,10%,0603,COG,SMT	C70,71,406,420
272075101701	CAP;100P ,50V ,+80-20%,0603,SMT	C3,4,7,21,22,464
272075102501	CAP;1000P,CR,50V ,20%,0603,SMT	C333,432,438,510
272075103702	CAP;.01U ,50V,+80-20%,0603,SMT	C17,61,63,79,80,84,
272075121401	CAP;120P ,CR,50V ,10%,0603,NPO,S	EC4,7
272075181301	CAP;180P ,50V ,5% ,0603,SMT	EC31-33,39-41,43,46
272075220301	CAP;22P ,50V ,5% ,0603,COG,SMT	C396,404
272075222401	CAP;2200P,50V ,10%,0603,SMT	C500
272075331501	CAP;330P ,50V ,20%,0603,COG,SMT	C445
272075470401	CAP;47P ,50V ,10%,0603,COG,SMT	C323,324,329,362,
272075471401	CAP;470P ,50V,10%,0603,SMT	C97,265,291,
272075472701	CAP;4700P,50V ,+80-20%,0603,SMT	C824
272075561701	CAP;560P ,CR,50V ,+80-20%,0603,S	C95,103,266,292
272075681401	CAP;680P ,50V ,10%,0603,NPO,SMT	C473,459
272601336501	EC;33U ,10V,D5L5.4,20%,-40+85,S	C1004
272602107501	EC;100U,16V,M,6.3*5.5,-55+85'C,S	C492,1005,1008
272602226502	EC;22U ,16V,D5L5.4,20%,-40+85,S	C1001,1003
272602227502	EC;220U ,16V,M,6.3*7.7,-15+105',	C456,478,457,
273000010003	FERRITE CHIP;36OHM/100MHZ,4332	L23,41,42,44,49,
273000053228	INDUCTOR;2.2UH,5%,3225,SMT	L26,33
273000130001	FERRITE CHIP;120OHM/100MHZ,1608,	L24,25,27
273000130006	FERRITE CHIP;600OHM/100MHZ,.2A,1	EL1001,1002,1004
273000130012	FERRITE CHIP;70OHM/100MHZ,1608,S	EL23-48,50-63,65
273000130013	FERRITE CHIP;30OHM/100MHZ,1608	R301,EL1000,L66
273000150002	FERRIET CHIP;120OHM/100MHZ,2012,	EL4,5,21,
273000500005	CHOKE COIL;7UH,T6*3*3,D.3,SMT	T1

PART_NO	DESCRIPTION	LOCATION
274011431404	XTAL;14.318MHZ,30PPM,32PF,SMT	X1,9
274011431405	XTAL;14.318MHZ,20PPM,18PF,SMT	X11
274011600405	XTAL;16MHZ,30PPM,16PF,SMT	X5
274011693401	XTAL;16.9344MHZ,50PPM,20PF,SMT	X6
274012863401	XTAL;28.63636M,30PPM,30PF,SMT,FU	X7
274013276103	XTAL;32.768KHZ,30PPM,12.5PF,CM20	X10
274013546401	XTAL;35.46895MHZ,30PPM,30PF,SMT,	X8
282104052001	IC;CD4052BM,MULTIPLEXER,SO,16P	U42,43
286329152001	IC;MIC29152,VOL REG,TO-263-5	U1000
282153238401	IC;PI5C32X384C,BUS SWITCH,QVSOP,	U11,12,17
282574000005	IC;74AHC00,QUAD 2I/P NAND,TSSOP,	U62
282574014004	IC;74AHC14,HEX INVERTER,TSSOP,14	U52,64
282574032005	IC;74AHC32,QUAD 2-I/P OR,TSSOP,1	U72
282574074004	IC;74AHC74,DUAL D F/F,TSSOP,14P	U54
282574123003	IC;74VHC123,RETRI. M/RESET,SSOP,	U47
282574244005	IC;74AHC244,OCT,BUF/DRIVE,TSSOP,	U55,58,68,73,707,
282574373004	IC;74AHC373,OCT D-TRAN,TSSOP,20P	U24
282574374003	IC;74AHC374,OCT 3ST D F/F,TSSOP,	U25,26
283666510003	IC;SRAM,64K*32,LQFP100,3.3V,5031	U13,6
283666510004	IC;SRAM,64K*32,TQFP100,2.5-3.5,5	U6,U13
283666510002	IC;SRAM,32K*8-12,SOJ,28P,5031	U30
283766510001	IC;DRAM,256K*16,EDO,60NS,SOJ40,5	U20-23,33-36
284100430001	IC;FW82439TX,MTXC,CPU/PCI,BGA,32	U31
284100430002	IC;FW82371AB,PIIX4,PCI/ISA,BGA,3	U53
284500045001	IC;LM45B,TEMPERATURE SENSORS,SOT	U1001
284500724001	IC;AD724,RGB TO NTSC/PAL,SO,16P	U18
284500827001	IC;BT827,VIDEO DECODER,PQFP,100P	U50
284504237001	IC;CS4237B,AUDIO 3D SOUND,TQFP,1	U49
284504331001	IC;CS4331,STEREO D/A CONVERTER,S	U70
284504867001	IC;W48S67-02,SYSTEM CLOCK,SSOP,4	U45
284505330001	IC;PI5V330,WIDEBAND/VIDEO,QSOP,1	U2
284506701001	IC;CL-PD6701,PC CARD COMPANION,S	U713

10. SPARE PARTS LIST-5

PART_NO	DESCRIPTION	LOCATION
284506832004	IC;OZ6832TC2,PCI/CARDBUS,TQFP,20	U38
284509385002	IC;CYBER9385-1X,VGA,CTRL,BGA,256	U10
284580051001	IC;80C51SL-BG,KBD CTLR,PQFP,100P	U32
284587338002	IC;PC87338VJG,SUPER I/O,TQFP,100	U9
284590363001	IC;DS90C363,LVDS,18BIT,SSOP,48P	U4,5
286100102001	IC;TPA0102,AUDIO AMP,1.5W,TSSOP,	U37
286100358012	IC;LM358,DUAL OP/AMP,SO 8P	U27
286100372014	IC;TLC372CD,DUAL COMP,SO	U60
286133078001	IC;MC33078D,LOW NOISE OP AMP.,SO	U7,44,59
286200213001	IC;MAX213,RS-232,SSOP,28P	U1
286300809002	IC;MAX809,RESET CIRCUIT,2.9V,SOT	U56
286302206001	IC;TPS2206,CARDBUS PWR CTLR,SSOP	U40
286302951015	IC;LP2951ACM,VOLTAGE REGULATOR,S	U8
286305200001	IC;MIC5200-5BS,VOL REG,SOT-223	U67
286501410001	IC;MK1410,NTSC/PAL CLOCK,SO,8P,S	U74
288001100001	FIR;HSDL-1100,TRANSCEIVER,X07,SM	U63
288100056001	DIODE;RLZ5.6B,ZENER,5.6V,5%,LL34	D20
288100202001	DIODE;DAN202K,80V,SWITCH,SMT	D13
288100202002	DIODE;DAP202K,80V,SWITCH,DUAL,SO	D12,14
288100212001	DIODE;DAN212K,80V,SWITCH,SOT23	D2,4,6,7,9-11,15,16
288100701002	DIODE;BAV70LT1,70V,225MW,SOT-23	D8,18
288200144001	TRANS;DTC144WK,NPN,SMT	Q1,6,9,13-18,4,7
288200352001	TRANS;NDS352P,DMOS,TO-236AB	Q22,53,71
288203904010	TRANS;MMBT3904L,NPN,Tr35NS,TO236	Q74,80,81
288203906018	TRANS;MMBT3906L,PNP,Tr35NS,TO236	Q51
288209410001	TRANS;SI9410DY,N-MOSFET,.04OHM,S	Q8
288209430001	TR;NDS9430,P-FET,.06OHM,SO,8P	Q19,20,72
288227002001	TRANS;2N7002LT1,N-CHANNEL FET	Q2,5,21
291000010604	CON;HDR,FM,6P*1,1.25MM,ST,SMT	J11,13
291000010605	CON;HDR,FM,3P*2,2.0MM,ST,SMT	J1008
291000011601	CON;HDR,MA,80P*2,.635MM,ST,SMT	J22
291000011602	CON;HDR,FM,8P*2,2.0MM,ST,SMT	J14

PART_NO	DESCRIPTION	LOCATION
291000012001	CON;HDR,MA,10P*2,1.25MM,ST,SMT	J15
291000015004	CON;HDR,FM,25P*2,1.27,ST,PITCHIN	J1000
291000020402	CON;HDR,SHROUD,MA,4P*1,2.0,R/A,U	J6
291000025202	CON;HDR,MA,26P*2,.635MM,H11,R/A,	J1003,1015,1016
291000150804	CON;FPC/FFC,8P,1MM,R/A,2CONTAC,E	J19
291000152401	CON;FPC/FFC,24P,1MM,R/A,ELCO	J18
291000410201	CON;WFR,MA,2P,1.25,ST,SMT/MB	J8,9,12,1006,
291000410301	CON;WFR,MA,3P,1.25,ST,SMT/MB	J10
291000410401	CON;WFR,MA,4P,1.25MM,ST,SMT	J23
291000516005	CON;RBN,MA,30P*2,ST,H9.6,SMT,800	J1012
291000610032	IC SOCKET;32P,PLCC,TIN,W/O PEGS,	U14
291000621443	DIMM SOCKET;144P,.8MM,H=4MM,SMT	J20,J21
295000010014	FUSE;1.1A/6V,POLY SWITCH,PTC,SMD	F2-4
295000010102	FUSE;FAST,3A,32V,1206,SMT,CERAMI	F1000,1001
297040101003	SW;PUSH BUTTON,SPST,.1A,30V,2P,S	SW1,2
297120101005	SW;DIP,SPST,8P,50VDC,.1A,SMT,DHS	SW1002
288209958001	TRANS;NDS9958,DUAL N&P MOSFET,SO	Q3
297120101006	SW;DIP,SPST,16P,50VDC,.1A,SMT,DH	SW1001
316665200001	PCB;PWA-PITCHING3/M BD	R01
481665100001	F/W ASSY;SYS/VGA BIOS,5031	U15
242600000158	LABEL;10*10,BLANK,COMMON,HI-TEMP	
283420402003	IC;FLASH,256K*8-120,5V,PLCC32,BT	U15
273000110015	FERRITE CHIP;80OHM/100MHZ,3216,3	EL49,18,L30
272015104701	CAP;.1U(A5),CR,50V,+80-20%,1206,	C901
271002333301	RES;33K ,1/10W,5% ,0805,SMT	R397
342665200013	CONTACTOR;AUDIO,PITCHING3	
346665100002	INSULATOR;PCMCIA,5031	
481665100002	F/W ASSY;KBD CTRL,EN,5031/6031	
283305402001	IC;EPROM,32K*8,120NS,CMOS,PLCC,3	U14
242600000145	LABEL;10*10,BLANK,COMMON	
411665200027	PWA;PWA-PITCHING3 OVERSEA D/D BD	
312271006152	EC;100U ,10V,M,RA,D6.3*9.8,OS-CO	C2,C5,C7,C19

10. SPARE PARTS LIST-6

PART_NO	DESCRIPTION	LOCATION
312271006350	EC;100U ,25V,20%,RA,6.3*7,-40~10	C3,6,8
312273306151	EC;330U ,6.3V,20%,RA,D10,W/OS-CO	C4,C1
313000020078	CHOKE COIL;15UH,D.7*16T/.2*32,55	T1
313000020110	CHOKE COIL;8uH,12.5TS,D0.8,55130	L2
313000020114	CHOKE COIL;15uH,16.5TS,D0.8,5513	L1
328101002001	DIODE;HRW1002A,10A,20V,TO-220AB	D7
342665200002	SHIELDING;D/D BD,PITCHING3	
346665200027	INSULATOR;D/D,SHIELDING,PITCHING	
346665200036	INSULATOR;D/D CHOKE,PITCHING3	
411665200028	PWA;PWA-PITCHING3 OVERSEA SMT D/	
271002100301	RES;10 ,1/10W,5% ,0805,SMT	R514
271045107101	RES;.01 ,1W ,1% ,2512,SMT	R515,R513
271045257101	RES;.025 ,1W ,1% ,2512,SMT	R524
271071000002	RES;0 ,1/16W,0603,SMT	R534,6,543
271071100302	RES;10 ,1/16W,5% ,0603,SMT	R519,R15
271071103302	RES;10K ,1/16W,5% ,0603,SMT	R20,R23,R25,R41,R523
271071104101	RES;100K ,1/16W,1% ,0603,SMT	R17,R39,R40,R510
271071104302	RES;100K ,1/16W,5% ,0603,SMT	R7,24
271071105101	RES;1M ,1/16W,1% ,0603,SMT	R30,R525
271071105301	RES;1M ,1/16W,5% ,0603,SMT	R8,R34,R531
271071121211	RES;12.1K,1/16W,1% ,0603,SMT	R532,540
271071124311	RES;124K ,1/16W,1% ,0603,SMT	R38,R512
271071133311	RES;133K ,1/16W,1% ,0603,SMT	R33,R26
271071169311	RES;169K ,1/16W,1% ,0603,SMT	R27,R21
271071204101	RES;200K ,1/16W,1% ,0603,SMT	R1,R32,R506
271071221301	RES;220 ,1/16W,5% ,0603,SMT	R5,R516
271071224301	RES;220K ,1/16W,5% ,0603,SMT	R4,R12,R501,R502
271071226311	RES;226K ,1/16W,1% ,0603,SMT	R530
271071237311	RES;237K ,1/16W,1% ,0603,SMT	R37
271071301311	RES;301K ,1/16W,1% ,0603,SMT	R31
271071332311	RES;332K ,1/16W,1% ,0603,SMT	R505
271071392311	RES;392K ,1/16W,1% ,0603,SMT	R509

PART_NO	DESCRIPTION	LOCATION
271071432211	RES;43.2K,1/16W,1% ,0603,SMT	R22,R28
271071473301	RES;47K ,1/16W,5% ,0603,SMT	R10,R3
271071474301	RES;470K ,1/16W,5% ,0603,SMT	R9,R11,R13,R14,R16
271071499211	RES;49.9K,1/16W,1% ,0603,SMT	R508
271071562311	RES;562K ,1/16W,1% ,0603,SMT	R539,541
271071681111	RES;6.81K,1/16W,1% ,0603,SMT	R18,R29
271071787311	RES;787K ,1/16W,1% ,0603,SMT	R507
271071976211	RES;97.6K,1/16W,1% ,0603,SMT	R538,542
272002105701	CAP;1U ,CR,16V ,-20+80%,0805,SM	C516,C9
272013105501	CAP;1U ,CR,25V ,+80-20%,1206,S	C505
272022106701	CAP;10U ,16V,+80-20%,1210,Y5V,S	C12,C508
272073104501	CAP;.1U ,25V,20%,0603,SMT	C14,C18,C20,C502
272075101701	CAP;100P ,50V ,+80-20%,0603,SMT	C13,17
272075102501	CAP;1000P,CR,50V ,20%,0603,SMT	C517
272075103501	CAP;.01U ,50V ,20%,0603,SMT	C21,501
272075104701	CAP;.1U ,50V,+80-20%,0603,SMT	C11,C15,C16,C503
272075470701	CAP;47P ,50V ,+80-20%,0603,SMT	C10
273000250005	FERRITE CHIP;160OHM/100MHZ,6A,45	L501,L502
286100339002	IC;LP339,ULTRA-LOW PWR COMP.,SO,	U503,U2
286300431004	IC;AIC431,.5%,ADJ SHUNT REG,SOT-	Q521
286300786001	IC;MAX786CAI,PWM CTLR,DUAL,SSOP,	U502
286300798001	IC;MAX798ESE,PWM CTLR,SO,16P	U501
286317812001	IC;HA178L12UA,VOLT REGULATOR,SC-	U1
288100024002	DIODE;RLZ24D,ZENER,23.63V,5%,SMT	D507
288100032013	DIODE;BAS32L,VRRM75V,MELF,SOD-80	D4,D503,D504,D506
288100056001	DIODE;RLZ5.6B,ZENER,5.6V,5%,LL34	D501
288100202001	DIODE;DAN202K,80V,SWITCH,SMT	D5,D6,D505
288101004024	DIODE;EC10QS04,RECT,40V,1A,CHIP,	D1,D2,D3,D502
288200144001	TRANS;DTC144WK,NPN,SMT	Q522
288202222001	TRANS;MMBT2222AL,NPN,TO236AB	Q5,Q9,Q515,Q517
288204410001	TRANS;SI4410DY,N-MOSFET,.02OHM,S	Q8,Q510,Q511,Q512
288204435001	TRANS;SI4435DY,P-MOSFET,.035OHM,	Q1,2,506,507

10. SPARE PARTS LIST-7

PART_NO	DESCRIPTION	LOCATION
288227002001	TRANS;2N7002LT1,N-CHANNEL FET	Q3,Q4,Q6,Q7,Q10,Q501
291000015005	CON;HDR,SHROUD,MA,25P*2,1.27MM,S	J1
295000010009	FUSE;NORMAL,5A/32VDC,3216,SMT	F501,F502,F503
316665200002	PCB;PWA-PITCHING3/DD BD	R01B
411665200006	PWA;PWA-PITCHING3 VIDEO JACK BD	
411665200007	PWA;PWA-PITCHING3 SMT VIDEO JACK	
316665200004	PCB;PWA-PITCHING3/VIDEO JACK BD	R00C
272075101701	CAP;100P ,50V ,+80-20%,0603,SMT	C501,502
273000130006	FERRITE CHIP;600OHM/100MHZ,.2A,1	L501
273000130001	FERRITE CHIP;120OHM/100MHZ,1608,	L502
273000130013	FERRITE CHIP;30OHM/100MHZ,1608	L503,504
331030006011	CON;HDR,MA,3P*2,2.0MM,ST,GLD	J1
331850002006	CON;RCA PIN JACK,2PYEL,JPJ254501	J502
331850002007	CON;RCA PIN JACK,2PBLK,RJ1091011	J501
411665200009	PWA;PWA-PITCHING3 BOTTOM LED BD	
316665200006	PCB;PWA-PITCHING3/LED BD	R0A
331030016005	CON;HDR,MA,8P*2,2.0MM,ST,GLD,SUY	J501
272075101701	CAP;100P ,50V ,+80-20%,0603,SMT	C501-509
294011200001	LED;GRN,H1.5,0805,PG1102W,SMT	D1-3,6-8
288100202002	DIODE;DAP202K,80V,SWITCH,DUAL,SO	D501,503
288100212001	DIODE;DAN212K,80V,SWITCH,SOT23	D502
288203904010	TRANS;MMBT3904L,NPN,Tr35NS,TO236	Q501-505,508
288200144001	TRANS;DTC144WK,NPN,SMT	Q506,507
288203906018	TRANS;MMBT3906L,PNP,Tr35NS,TO236	Q509,510
271611104301	RP;100K*4,8P ,1/16W,5% ,0612,SMT	PR501,503
271611103301	RP;10K*4 ,8P ,1/16W,5% ,0612,SMT	RP502
271071681301	RES;680 ,1/16W,5% ,0603,SMT	R501,502,504,508,
271071223302	RES;22K ,1/16W,5% ,0603,SMT	R503
271071104302	RES;100K ,1/16W,5% ,0603,SMT	R505-507
282574032005	IC;74AHC32,QUAD 2-I/P OR,TSSOP,1	U501
346665200024	INSULATOR;DIMM,PITCHING3	
346665200032	INSULATOR;CPU SCREW HOLE,PITCHIN	

PART_NO	DESCRIPTION	LOCATION
345665200017	CONDTIVE SPONG;AUDIO,PITCHING3	
345665100017	PAD;T/P BUTTON CUSHION PAD,5031	
451665100003	ME KIT;HDD,5031	
340665100016	HDD HOLDER ASSY;5031	
342665100003	HOLDER;HDD HOLDER,5031	
344665100006	COVER;HDD COVER,5031	
344665100007	COVER;PCMCIA COVER,5031	
346664700002	INSULATOR;REM,HDD,5026	
342665100005	BRKT;HDD,5031	
346664700007	INSULATOR;HDD TOP,5026	
370103010603	SPC-SCREW;M3L4,K-HEAD(+),NIW	HDD TO HOLDERx4
370102010402	SPC-SCREW;M2L4,NIW,K-HD(+),731	
412665200004	PCB ASSY;HDD CONN. BD,PITCHING3	
523466470002	FDD ASSY;1.44M,3.5",D-5026	
242664710020	LABEL;FDD,PC T=0.2,1,5026	
340664710008	HOUSING COMP;FDD,1,5026	
344664710036	COVER;FDD,1,5026	
421664700053	FPC ASSY;REM. FDD CON.,FPC,5026	
242664710019	LABEL;CAUTION,FDD,1,5026	
342664800006	HEATSINK;FDD,PITCHING	
523410290015	FD DRIVE;1.44M,3 MODE,FD-05HG-56	
421664710003	CABLE ASSY;EXT FDD,1,5026	
344664710065	COVER;FDD CON.,1,5026	
421664700002	CABLE ASSY;FDD,5026	
342664700021	GROUND;FDD CON.,5026	
411664700032	PWA;PWA-5026 FDD TRANS BD	
316664700029	PCB;PWA-5026/FDD TRAN BD	R01
331120020001	CON;HDR,SHROUD,MA,10P*2,2MM,ST	J2
331030052002	CON;HDR,MA,26P*2,1.27,ST,GOLD	J1
373203010601	T-SCREW;P,M3,L6,PAN(+),0,ZNC	
222600020009	PE BUBBLE BAG;10"*8",COMMON	
441664700063	BATT ASSY;12V/4AH,NIMH,SANYO,502	

10. SPARE PARTS LIST-8

PART_NO	DESCRIPTION	LOCATION
242664700021	LABEL;BATT ASSY,12V/4.0AH,SNY,50	
310131103002	CFM-BAT;NTCR,10K,ISUZU,103AT-2	
316664700011	PCB;PWA-5026/BATT CONN BD	R00
331030010006	CON;HDR,FM,10P*1,2.0MM,ST,GLD	
335152000020	CFM-BAT;THERMAL BREAKER,ISUZU,IP	
335152000021	CFM-BAT;FUSE,THERMAL,ELMWOOD,D09	
335512000001	POLYSWITCH;3.5A,SRP350	
338712010011	BATTERY;NIMH,1.2V/4AH,D18,SANYO	
340664710044	HOUSING ASSY;BATT 4000mA,1,5026	
344664710058	PANEL;BATTERY,1,5026	
344664710100	COVER;BATT,10*18D,1,5026	
272003104701	CAP;.1U ,CR,25V ,+80-20%,0805,Y	C1,2,3,4
288100062001	DIODE;RLZ6.2B,ZENER,SMT,LL34	D1
294011200004	LED;YE/GR,H1.1,L2,W1.25,CL170YG,	D2,3,4,5,6
288100032013	DIODE;BAS32L,VRRM75V,MELF,SOD-80	D501,502
288202222001	TRANS;MMBT2222AL,NPN,TO236AB	Q1
271002104101	RES;100K ,1/10W,1% ,0805,SMT	R2
271002104301	RES;100K ,1/10W,5% ,0805,SMT	R1,3,501
271002909311	RES;909K ,1/10W,1% ,0805,SMT	R4
271002204301	RES;200K ,1/10W,5% ,0805,SMT	R7,8,11,511
271045507101	RES;.05 ,1W ,1% ,2512,SMT	R9,10
271002471301	RES;470 ,1/10W,5% ,0805,SMT	R504,505,506,507,508
271002101301	RES;100 ,1/10W,5% ,0805,SMT	R509
297040105002	SW;PUSH BUTTON,SPST,12V/50MA,4P,	SW1
286002014001	IC;BQ2014,GAS GAUGE,SO,16P	U1
316664700052	PCB;PWA-5026/BATT VIEW 4AH BD	R00B
461665100001	PACKING KIT;5031	
523466470002	FDD ASSY;1.44M,3.5",D-5026	
242664710020	LABEL;FDD,PC T=0.2,1,5026	
340664710008	HOUSING COMP;FDD,1,5026	
344664710036	COVER;FDD,1,5026	
421664700053	FPC ASSY;REM. FDD CON.,FPC,5026	

PART_NO	DESCRIPTION	LOCATION
242664710019	LABEL;CAUTION,FDD,1,5026	
342664800006	HEATSINK;FDD,PITCHING	
523410290015	FD DRIVE;1.44M,3 MODE,FD-05HG-56	
541566470014	FRU;CD ROM MODULE,20X,5026	
523466470013	CD ROM DRIVE ASSY;20X,SR200S,502	
222663920001	PE BAG;150*50,FRU,LP486	
222664820007	PE BAG;90*130,PITCHING	
340664710002	BEZEL ASSY;CD ROM(MITSU),5026	
342665100009	BRKT;CD ROM (MIT),5031	
340664710018	FRAME COMP;CD-ROM(MAT),1,5026	
370102010302	SPC-SCREW;M2L3,NIW,K-HD,736	
370102010701	SPC-SCREW;M2L7,K-HD,NIB	
377102010001	STANDOFF;M2 DP5 H4*13*L1.5	
421665200041	FPC ASSY;CD-ROM,PITCHING3	
523411442506	CD ROM DRIVE;8-20X,SR200S	
227664700004	END CAP-1;CD ROM,5026	
227664700005	END CAP-2;CD ROM,5026	
227664800008	END CAP-1;CD ROM,PITCHING	
221664740002	BOX;CD ROM,5026	
222664820003	PE BAG;CD ROM,PITCHING	
242600000088	LABEL;BAR CODE,125*65,COMMON	
565166470001	S/W;1.44M,UTILITY DRIVE,5026	
222600050108	ENVELOPE;3.5" FD,PVC,COMMON	
242661900008	LABEL;3.5",EN,ALL COMMON	
551103200013	FLOPPY DISKETTE;3.5",1.44MB,2HD	
561566470019	MANUAL;EN/GR,14X/20X CD ROM,5026	
531004870031	KBD;87,US,NK1K002-US,6031	
451665100031	LABEL KIT;5031	
541666510001	ACCESSORY KIT;AK-5031-EN	
332810000033	PWR CORD;125V/7A,2P,BLACK,AMERIC	
422664700001	CABLE ASSY;A/D - CHASSIS,120CM,5	
561566530001	MANUAL;USER'S,EN,6031/5031	

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PART_NO	DESCRIPTION	LOCATION
561566530002	MANUAL;QUICK REF,EN,6031/5031	
222600020009	PE BUBBLE BAG;10"*8",COMMON	
421664710003	CABLE ASSY;EXT FDD,1,5026	
344664710065	COVER;FDD CON.,1,5026	
421664700002	CABLE ASSY;FDD,5026	
342664700021	GROUND;FDD CON.,5026	
411664700032	PWA;PWA-5026 FDD TRANS BD	
316664700029	PCB;PWA-5026/FDD TRAN BD	R01
331120020001	CON;HDR,SHROUD,MA,10P*2,2MM,ST	J2
331030052002	CON;HDR,MA,26P*2,1.27,ST,GOLD	J1
373203010601	T-SCREW;P,M3,L6,PAN(+),0,ZNC	
565166510005	S/W;1.44M,CD ROM DRIVER,5031	
222600050108	ENVELOPE;3.5" FD,PVC,COMMON	
242661900008	LABEL;3.5",EN,ALL COMMON	
551103200013	FLOPPY DISKETTE;3.5",1.44MB,2HD	
565166510011	S/W;CD ROM,SYSTEM DRIVER,5031	
324180586033	IC;CPU,P55C,200MHZ,2.8V,PPGA,296	
323766490021	SDRAM MODULE;16M,ATP,5027	
441665100001	LCD ASSY;13.3(S),TFT,5031	
340665100005	HOUSING ASSY;13.3(S) LCD,5031	
344665100003	LENS;POWER LENS(B),5031	
344665100011	HOUSING;13.3 LCD HOUSING,5031	
345665100001	PAD;LCD HOUSING(S),5031	
345665100003	PAD;LCD HOUSING SIDE PAD(S),5031	
344665100029	COVER;CCD CON COVER,5031	
345665100005	PAD;LCD HOUSING TOP PAD(S),5031	
345665100006	PAD;LCD HOUSING TOP PAD(H),5031	
340665100006	COVER ASSY;13.3(S) LCD,5031	
344665100004	LENS;POWER LENS(T),5031	
344665100012	COVER;13.3S LCD COVER,5031	
344665100030	PLUG;LCD HOOK,5031	
345665100009	CUSHION;TOP,LCD COVER,5031	

PART_NO	DESCRIPTION	LOCATION
345665200006	CUSHION;DOWN,LCD,PITCHING3	
346665100003	INSULATOR;INVERTER,5031	
370102010301	SPC-SCREW;M2L3,NNIB,K-HD,727	
370102010601	SPC-SCREW;M2L6,K-HEAD(+),NIW	
370102610602	SPC-SCREW;M2.6 L6,NIB,K-HD,727	
411665300006	PWA;PWA-6031 CCD TRANS BOTTOM BD	
272072104702	CAP;.1U ,16V,+80-20%,0603,SMT	C1
291000012004	CON;HDR,FM,10P*2,1.27MM,ST,SMT	J1
291000020803	CON;HDR,MA,8P*1,1.25,R/A,SMT,HIR	J2
316665300003	PCB;PWA-6031/CCD-TRAN BOTTON BD	R03
273000130010	FERRITE CHIP;130OHM/100MHZ,1608,	R1,R2
273000130013	FERRITE CHIP;30OHM/100MHZ,1608	R3
412665200001	PCB ASSY;INVERTER BD,PITCHING3	
413000020093	LCD;LT133X1-104,TFT,13.3,XGA	
421665100001	WIRE ASSY;LCD(CCD)-M/B,5031	
421665100004	WIRE ASSY;D/A,5031	
421665200002	WIRE ASSY;LCD TO M/B,PITCHING3	
340665100001	TILT UNIT;13.3S(L),5031	
340665100003	TILT UNIT;13.3(R),5031	
341665100001	BRKT;13.3S(L) LCD BRACKET,5031	
341665100002	BRKT;13.3(R) LCD BRACKET,5031	