

# 5027 N/B MAINTENANCE

TROUBLE SHOOTING GUIDE FOR NOTEBOOK

5027

BY:

CALVIN CHUANG



**MiTAC**

# 5027 N/B MAINTENANCE

<b>1. DEFINITION OF CONNECTORS &amp; SWITCHES.....</b>	<b>3</b>
<b>2. LOCATION OF SWITCHES &amp; CONNECTORS.....</b>	<b>4</b>
<b>3. MAJOR COMPONENTS.....</b>	<b>6</b>
<b>4. LOCATION OF MAJOR COMPONENTS.....</b>	<b>7</b>
<b>5. PIN DESCRIPTIONS OF MAJOR CHIPS.....</b>	<b>9</b>
<b>6. SWITCH &amp; JUMPERS SETTING.....</b>	<b>20</b>
<b>7. ASSEMBLY &amp; DISASSEMBLY.....</b>	<b>21</b>
<b>8. MAINTENANCE DIAGNOSTICS.....</b>	<b>45</b>
<b>9. TROUBLE SHOOTING.....</b>	<b>48</b>
<b>10. SPARE PARTS LIST.....</b>	<b>81</b>
<b>11. EXPLODED VIEWS AND CIRCUIT DIAGRAM</b>	

# 5027 N/B MAINTENANCE

## 1. DEFINITION OF CONNECTORS & SWITCHS

Connector	Definition
J1	Audio input connector
J2	LVDS board connector
J3	Internal microphone connector
J4	External speaker connector
J5	Internal speaker connector
J6	Voltage selection for LED panel: 1-2: 5V panel 2-3: 3.3V panel
J7	Internal keyboard connector
J8	LCD indicator connector
J9	Backlight connector
J10	Cover switch
J12	Touchpad connector
J13	Touchpad button connector
J14	Voltage selection for CPU I/O: 1-2: 3.3V CPU I/O voltage 2-3: 2.5V CPU I/O voltage
J500	PS/2 keyboard/mouse connector
J501	TV out connector
J502	Power jack
J503	CRT video connector
J504	Parallel port (PIO)
J505	Serial port (SIO)
J507	USB Port
J508	Expansion Bus Connector
J509	Secondary battery connector
J510	DIMM daughter board connector
J511	External microphone board connector
J513	Fax/Modem/Voice Card connector
J514	PCMCIA IC card connector
J515	Cooling fan connector
J516	FDD/CD-ROM connector
J517	Hard disk drive connector
J518	CMOS battery
J519	DC/DC board connector

# 5027 N/B MAINTENANCE

## 2. LOCATION OF CONNECTORS & SWITCHES (A)

J1: AUDIO INPUT CONNECTOR

J2: LVDS BOARD CONNECTOR

J3: INTERNAL MICROPHONE CONNECTOR

J4: EXTERNAL SPEAKER CONNECTOR

J5: INTERNAL SPEAKER CONNECTOR

J6: VOLTAGE SELECTION FOR LED PANEL

1-2: 5V PANEL

2-3: 3.3V PANEL

J7: INTERNAL KEYBOARD CONNECTOR

J8: LCD INDICATOR CONNECTOR

J9: BACKLIGHT CONNECTOR

J10: COVER CWITCH

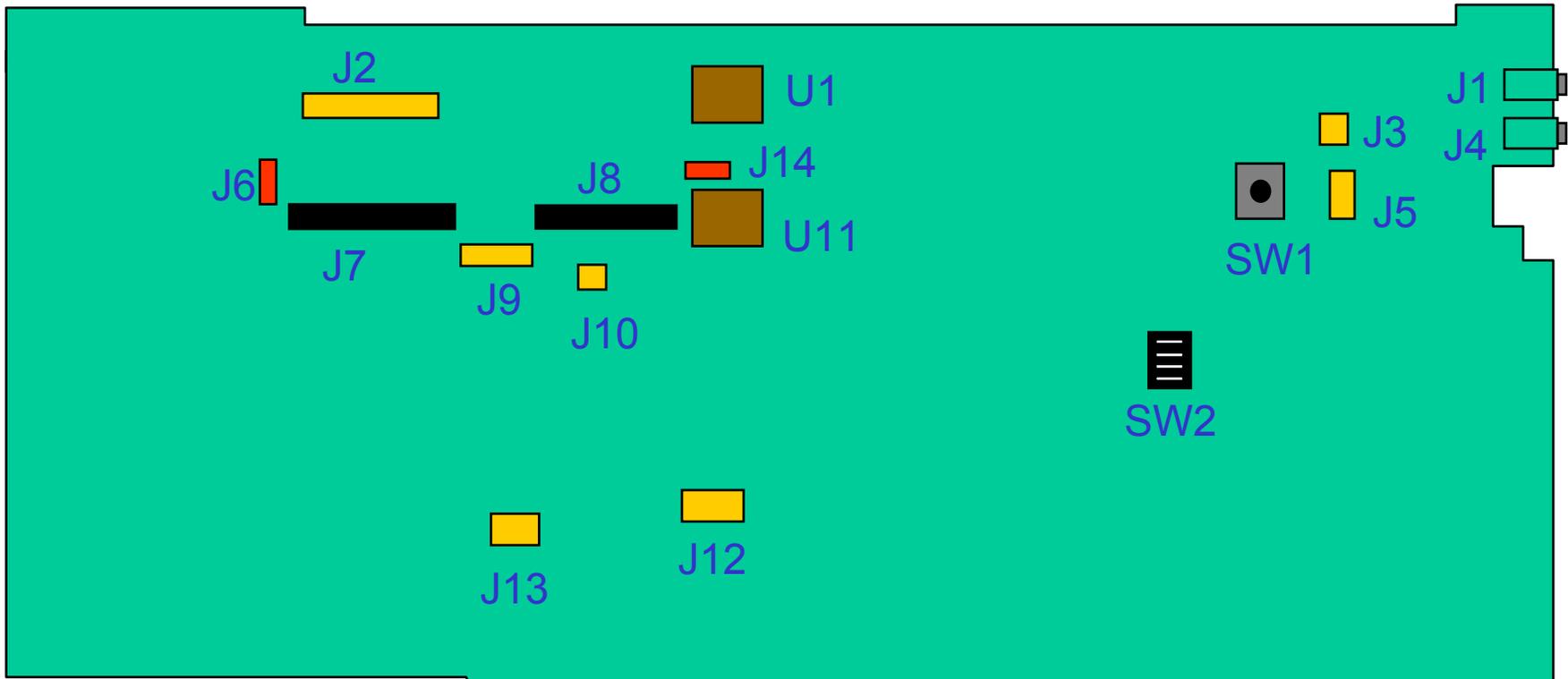
J12: TOUCHPAD CONNECTOR

J13: TOUCHPAD BUTTON CONNECTOR

J14: VOLTAGE SELECTION FOR CPU I/O

1-2: 3.3V CPU I/O VOLTAGE

2-3: 2.5V CPU I/O VOLTAGE



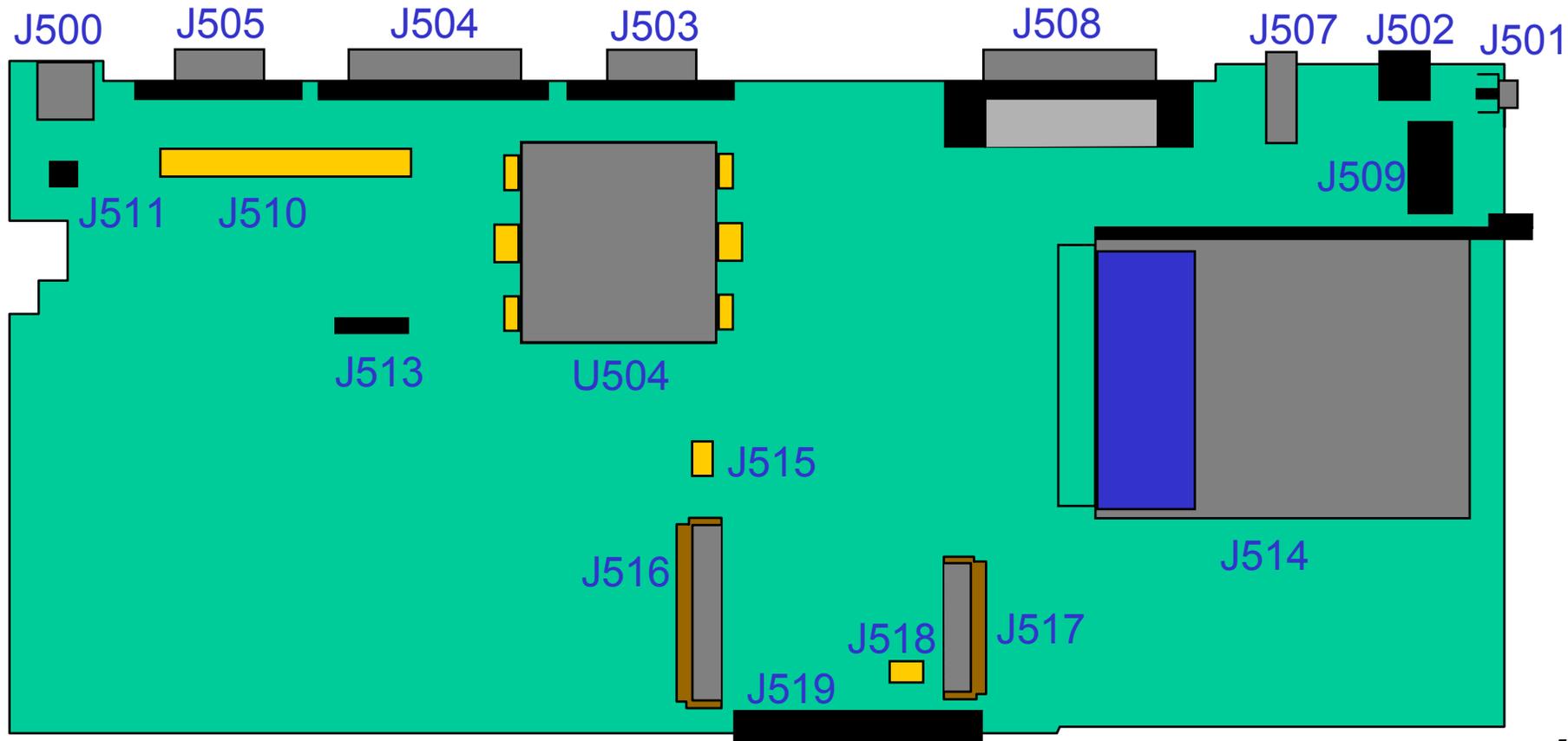
# 5027 N/B MAINTENANCE

## 2. LOCATION OF CONNECTORS & SWITCHES (B)

J500: PS/2 KEYBOARD/MOUSE CONNECTOR  
J501: TV OUT CONNECTOR  
J502: POWER JACK  
J503: MONITOR CONNECTOR  
J504: PARALLEL PORT (PIO)  
J505: SERIAL PORT (SIO)  
J507: USB PORT

J508: EXPANSION BUS CONNECTOR  
J509: SECONDARY BATTERY CONNECTOR  
J510: DIMM DAUGHTER BOARD CONNECTOR  
J511: EXTERNAL MICROPHONE BOARD CONNECTOR  
J513: FAX/MODEM/VOICE CARD CONNECTOR  
U504

J514: PCMCIA IC CARD CONNECTOR  
J515: COOLING FAN CONNECTOR  
J516: FDD/CD-ROM CONNECTOR  
J517: HARD DRIVE CONNECTOR  
J518: CMOS BATTERY  
J519: DC/DC BOARD CONNECTOR



# 5027 N/B MAINTENANCE

## 3. MAJOR COMPONENTS

1. U504 PENTIUM PROCESSOR
2. U27 INTEL 430TX (MTXC) SYSTEM CONTROLLER, HOST TO PCI BRIDGE.
3. U26 430TX (PIIX4) ,PCI TO ISA ,IDE BRIDGE.
4. U28 TRIDENT 9385F, VGA CONTROLLER.
5. U31 OZ-6382 PCI-PCMCIA CONTROLLER.
6. U40 PC87338VJG, SUPER I/O CONTROLLER.
7. U524 80C51SL , KB CONTROLLER.
8. U1 PLCC256KBFLASH ROM
9. U5,U12 512K L2 CACHE
10. U11 KEYBOARD BIOS
11. U29 AUDIO CONTROLLER
12. U507 THE CLOCK SYNTHESIZER PROVIDES.

# 5027 N/B MAINTENANCE

## 4. LOCATION OF MAJOR COMPONENTS (A)

U1: SYSTEM BIOS

U11: KB BIOS

U31: MICRO OZ6832T

U28: TRIDENT 9385

U26: FW82371AB(PIIX4)

U27: FW82439TX(MTXC)

U5,U12: 512K CACHE

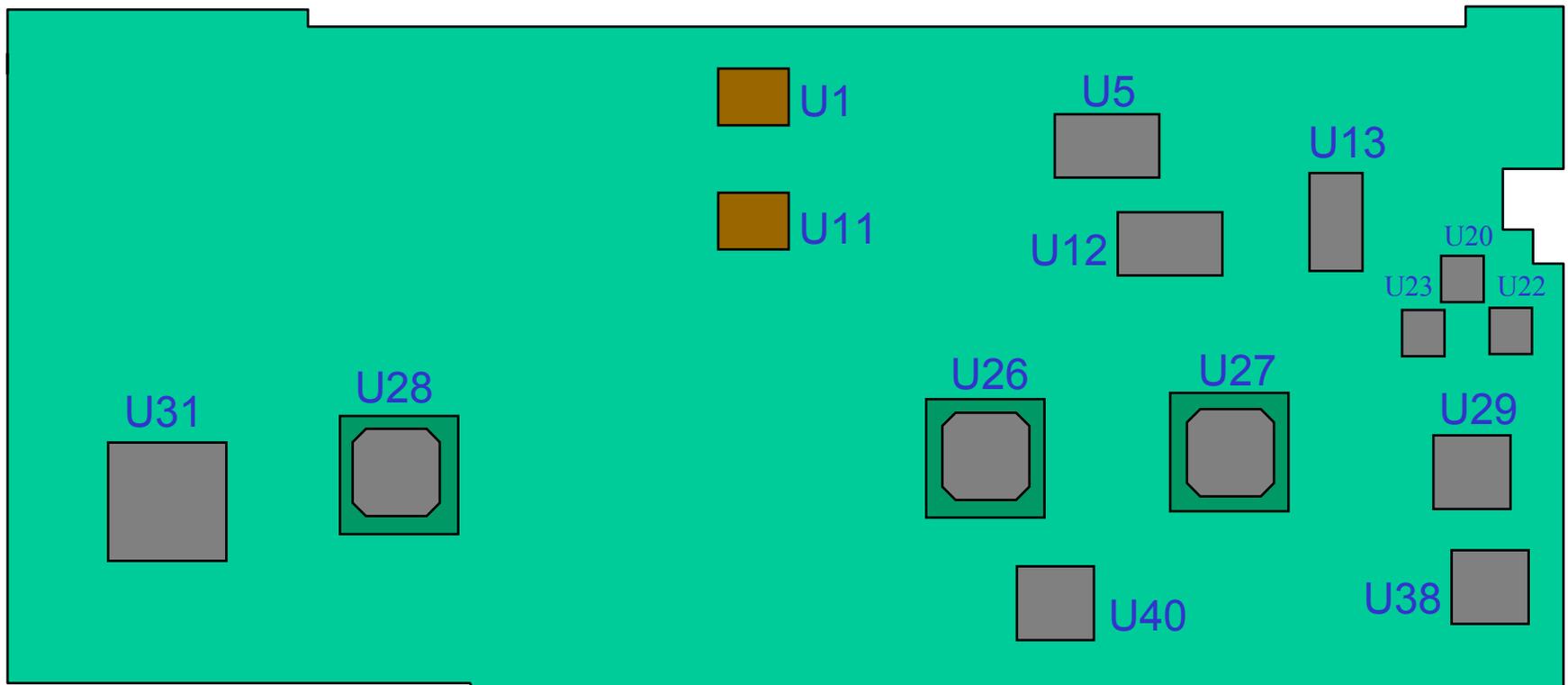
U13: IS61C256AH-12J

U29: YAMAHA YMF7158

U38: YAMAHA YMF704C-S

U40: PC87338VJG

U20,22,23: 2MB VIDEO MEMORY



# 5027 N/B MAINTENANCE

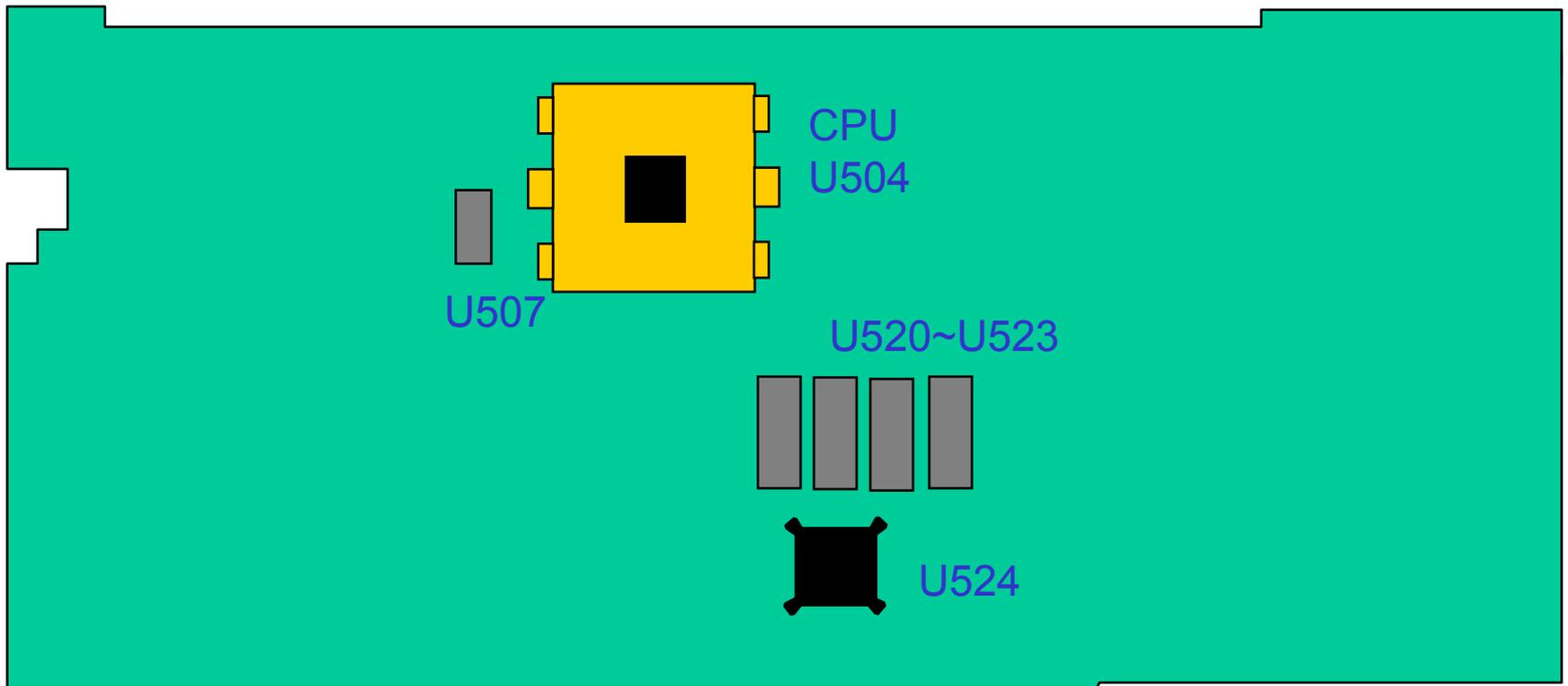
## 4. LOCATION OF MAJOR COMPONENTS (B)

U504: CPU

U507: PLL52C62

U520~523: VIDEO RAM

U524: KU80C51SL



# 5027 N/B MAINTENANCE

## 5. PIN DESCRIPTIONS OF MAJOR COMPONENTS

### 5.1 PENTIUM MICROPROCESSOR (P54LM)-1

SYMBOL	TYPE	DESCRIPTION
A20M#	I	WHEN THE ADDRESS BIT 20 MASK PIN IS ACTIVE, THE 20 (A20) PENTIUM MICROPROCESSOR MASKS PHYSICAL ADDRESS BIT BEFORE PERFORMING A LOOKUP TO THE INTERNAL CACHE OR EMULATES THE ADDRESS WRAPAROUND AT THE ADDRESS DRIVING A MEMORY BUS CYCLE ONTO THE BUSES. A20M# BOUNDARY THAT OCCURS ON THE 8086/8088.
A31A5 A4A3	IO O	A31A3 COMPRESSES THE PENTIUM MICROPROCESSOR'S ADDRESS BUS.
ADS#	IO	WHEN ACTIVE, THE ADDRESS STATUS OUTPUT INDICATES THAT A VALID BUS CYCLE DEFINITION AND ADDRESS ARE AVAILABLE ON THE BUS CYCLE DEFINITION AND BUS LINES.
AHOLD	I	THE ADDRESS HOLD REQUEST INPUT ALLOWS ANOTHER BUS MASTER ACCESS TO PENTIUM MICROPROCESSOR'S ADDRESS BUS FOR A CACHE INVALIDATION, BACK INVALIDATION, OR INQUIRE CYCLE.
AP	IO	THE PENTIUM PROCESS GENERATES ADDRESS PARITY DURING MEMORY WRITE OPERATIONS AND CHECK ADDRESS PARITY DURING CACHE INVALIDATION CYCLES (ADDRESS BUS SNOOPING).
APCHK#	O	THE PENTIUM PROCESS ASSERTS THE ADDRESS PARITY CHECK OUTPUT WHEN AN ADDRESS BUS PARITY ERROR IS DETECTED. APCHK# IS ASSERTED 2 CLOCK CYCLES AFTER ADS# IS SAMPLE ACTIVE. APCHK# REMAINS ACTIVE FOR ONE CLOCK CYCLE.
[APCHEN] OR PCD1	IO	APIC ENABLE.
BE0#	O	BYTE ENABLE, PATH 0 (D7-D0).
BE1#	O	BYTE ENABLE, PATH 1 (D15-D8).
BE2#	O	BYTE ENABLE, PATH 2 (D23-D16).
BE3#	O	BYTE ENABLE, PATH 3 (D31-D24).
BE4#	O	BYTE ENABLE, PATH 4 (D39-D32).
BE5#	O	BYTE ENABLE, PATH 5 (D47-D40).
BE6#	O	BYTE ENABLE, PATH 6 (D55-D48).
BE7#	O	BYTE ENABLE, PATH 7 (D63-D56).

SYMBOL	TYPE	DESCRIPTION
BF	I	THE BUS FREQUENCY SIGNAL (BF) DETERMINES THE IO BUS TO PROCESSOR CORE FREQUENCY RATIO.
BOFF#	I	ENSURE THAT THE PROCESSOR DOESN'T FETCH STALE DATA FROM MAIN MEMORY.
BP3-2	O	THE BREAK POINT OUTPUTS INDICATE THAT A BREAKPOINT MATCH HAS BEEN DETECTED THROUGH THE BREAKPOINT REGISTER.
BP/PM1-0	O	BREAKPOINT AND PERFORMANCE MONITORING PINS.
BRDY#	I	THE BURS READY INPUT INDICATES THAT THE CURRENTLY ADDRESSED DEVICE HAS PRESENTED VALID DATA ON THE DATA BUS PINS IN RESPONSE TO A READ OR THAT CURRENTLY ADDRESSED DEVICE HAS ACCEPTED DATA FROM THE PENTIUM CPU IN RESPONSE TO A WRITE.
BRDCY#	I	THE BURS READY INPUT INDICATES THAT THE LEVEL 2 CACHE HAS PRESENTED VALID DATA ON THE DATA BUS PINS IN RESPONSE TO A READ OR THAT THE LEVEL 2 CACHE HAS ACCEPTED DATA FROM THE PENTIUM CPU IN RESPONSE TO A WRITE.
BREQ#	O	THE INTERNAL CYCLE PENDING OUTPUT INDICATES THAT THE PENTIUM MICROPROCESSOR HAS A BUS CYCLE REQUEST PENDING.
BT3-BT0	NA	BRANCH TRACE LINES ARE DRIVEN DURING A BRANCH TRACE SPECIAL CYCLE.
BUSCHK#	I	THE BUS CHECK ALLOW SYSTEM DESIGNERS TO NOTIFY THE CPU, IF A BUS CYCLE HAS NOT COMPLETED SUCCESSFULLY.
CACHE#	IO	CACHE# SIGNAL IS ACTIVE WHEN INFORMATION IS BEING TRANSFERRED BETWEEN EXTERNAL MEMORY AND AN INTERNAL CACHE.
CLK	I	CLOCK PROVIDES THE FUNDAMENTAL TIMING AND THE INTERNAL OPERATING FREQUENCY FOR THE PENTIUM MICROPROCESSOR.
CPUTYP	I	CPU TYPE PIN SAMPLED BY THE PROCESSOR AT THE TRAILING-EDGE OF RESET TO DETERMINE WHETHER IT IS PRIMARY OR THE DUAL PROCESSOR.

# 5027 N/B MAINTENANCE

## 5.1 PENTIUM MICROPROCESSOR (P54LM)-2

SYMBOL	TYPE	DESCRIPTION
D7D0	IO	DATA PATH ZERO.
D51D8	IO	DATA PATH ONE.
D23D16	IO	DATA PATH TWO.
D31D24	IO	DATA PATH THREE.
D39D32	IO	DATA PATH FOUR.
D47D40	IO	DATA PATH FIVE.
D55D48	IO	DATA PATH SIX.
D63D56	IO	DATA PATH SEVEN.
D/C#	IO	DATA OR CONTROL. AT THE START OF BUS CYCLE, THE PENTIUM PROCESSOR SETS THIS LINE HIGH IF DATA WILL BE TRANSFERRED DURING THE CURRENT BUS CYCLE, OTHERWISE SETS IT TO LOW.
D/#	O	DUAL/PRIMARY. THIS IS AN OUTPUT OF PRIMARY PROCESSOR AND IS NOT USED BY THE DUAL PROCESSOR. IT ASSERTED (LOW) BY THE PRIMARY PROCESSOR WHEN IT HAS ACQUIRED PRIMARY BUS OWNERSHIP AND HAS INITIATED A BUS CYCLE.
DP0	IO	PARITY BIT FOR DATA PATH 0D7D0.
DP1	IO	PARITY BIT FOR DATA PATH 1D15D8.
DP2	IO	PARITY BIT FOR DATA PATH 2D23D16.
DP3	IO	PARITY BIT FOR DATA PATH 3D31D24.
DP4	IO	PARITY BIT FOR DATA PATH 4D39D32.
DP5	IO	PARITY BIT FOR DATA PATH 5D47D40.
DP6	IO	PARITY BIT FOR DATA PATH 6D55D48.
DP7	IO	PARITY BIT FOR DATA PATH 7D63D56.
DPEN#	IO	DUAL PROCESSOR ENABLE.
EADS#	I	THE EXTERNAL ADDRESS STROBE SIGNAL INDICATES THAT A VALID EXTERNAL ADDRESS HAS BEEN DRIVEN ONTO THE PENTIUM S A4A31 ADDRESS LINES BY ANOTHER MASTER.
EWBE#	I	THE EXTERNAL WRITE BUFFER EMPTY IS USED TO ENSURE THAT MEMORY OPERATIONS OCCUR IN ORDER OF EXECUTION.
FLUSH#	I	THE CACHE FLUSH INPUT FORCES THE PENTIUM PROCESSOR TO FLUSH THE CONTENTS OF ITS INTERNAL CACHE.
FERR#	O	FLOATING-POINT ERROR OUTPUT PIN IS DRIVEN ACTIVE WHEN A FLOATING-POINT ERROR OCCURS.

SYMBOL	TYPE	DESCRIPTION
FRMC#	I	THE FUNCTION REDUNDANCY CHECKING MASTER/CHECKER# PIN IS SAMPLED BY THE PENTIUM MICROPROCESSOR DURING RESET TO DETERMINE WHETHER THE MICROPROCESSOR SHOULD BE CONFIGURED AS A FUNCTIONAL REDUNDANCY MASTER OR CHECKER.
HIT#	IO	THE HIT# SIGNAL ACTIVE TO INDICATE A SNOOP HIT IN EITHER THE INTERNAL CODE OR DATA CACHE.
HITM#	IO	THE PENTIUM MICROPROCESSOR DRIVES THE HIT MODIFIED SIGNAL ACTIVE TO INDICATE A SNOOP HIT TO A MODIFIED LINE IN THE DATA CACHE.
HLDA	IO	BUS HOLD ACKNOWLEDGE.
HOLD	I	THE BUS HOLD REQUEST INPUT ALLOWS ANOTHER BUS MASTER TO GAIN COMPLETE CONTROL OF THE PENTIUM S LOCAL BUSES.
IBT	NA	THE INSTRUCTION BRANCH TAKEN SIGNAL IS DRIVEN ACTIVE FOR ONE CLOCK CYCLE WHEN PENTIUM MICROPROCESSOR EXECUTES AN INSTRUCTION RESULTING IN AN EXECUTION BRANCH.
ERR#	O	INTERNAL ERROR IS ASSERTED WHEN A PARITY ERROR IS ENCOUNTERED INSIDE THE PENTIUM MICROPROCESSOR.
IGNNE#	I	IGNORE NUMERIC ERROR INPUT IS ASSERTED BY EXTERNAL LOGIC. THE PENTIUM MICROPROCESSOR WILL IGNORE A NUMERIC ERROR. AND CONTINUE EXECUTING NON-CONTROL FLOATING-POINT INSTRUCTIONS.
INT	I	PENTIUM MICROPROCESSOR INT INPUT HAS THE SAME EFFECT AS THE RESET SIGNAL EXCEPT THAT THE FOLLOWING RETAIN THE VALUES.
NTR	I	THIS IS MASKABLE INTERRUPT REQUEST INPUT.
INV	I	THE INVALIDATE INPUT TELLS THE PENTIUM MICROPROCESSOR WHETHER THE CACHE LINE STATE SHOULD BE MARKED INVALIDATED OR SHARED AS A RESULT OF SNOOP HIT.
IJ	NA	THE IJ SIGNAL INDICATES THAT AN INSTRUCTION IN THE "u" PIPELINE HAS COMPLETED EXECUTION.
IV	NA	THE IV SIGNAL INDICATES THAT AN INSTRUCTION IN THE "v" PIPELINE HAS COMPLETED EXECUTION.

# 5027 N/B MAINTENANCE

## 5.1 PENTIUM MICROPROCESSOR (P54LM)-3

SYMBOL	TYPE	DESCRIPTION
KEN#	I	THE CACHE ENABLE PIN IS SAMPLED TO DETERMINE IF THE CURRENT BUS CYCLE IS CACHEABLE.
LINT0 OR INTR	I	IF THE PROCESSOR'S LOCAL APIC IS ENABLE, THIS IS THE LINT0 INPUT TO THE APIC.
LOCK#	I/O	THE LOCK# SIGNAL IS ASSERTED WHEN THE PENTIUM MICROPROCESSOR WANTS TO RUN MULTIP BUS CYCLES WITHOUT HAVING THE BUSES TAKEN AWAY BY ANOTHER BUS MASTER.
M/IO#	I/O	MEMORY OR I/O. AT THE START OF BUS CYCLE, THE PENTIUM PROCESSOR SETS THIS LINE HIGH IF ADDRESSING A MEMORY LOCATION AND LOW IF ADDRESSING AN I/O LOCATION.
NA#	I	THE NEXT ADDRESS INPUT INDICATES THAT THE MEMORY SUBSYSTEM IS CAPABLE FO TAKING ADVANTAGE OF THE PENTIUM MICROPROCESSOR'S ADDRESS PIPELINING.
NMI	I	NON-MASKABLE INTERRUPT REQUEST.
PBREQ#	I/O	PRIVATE BUS REQUEST.ONLY USED IN DUAL PROCESSOR SYSTEM.
PBGNT#	I/O	PRIVATE BUS GRANT.ONLY USED IN DUAL PROCESSOR SYSTEM.
PCHK#	O	SEE DP0.
PCD	O	PAGE CACHE DISABLE.
PEN#	I	PARITY ENABLE.
PHIT#	I/O	PARIVATE BUS HIT.PHIT# IS AN OUTPUT FROM THE LRM AND AN INPUT TO THE MRM.TI IS USED IN A DUAL PROCESSOR SYTEM.
PHITM#	I/O	PRIVATE BUS HIT ON MODIFIED LINE.
PICCLK	I	PROGRAMMABLE INTERRUPT CONTROLLER CLOCK.
PICDO OR DEPN#	I/O	PROGRAMMABLE INTERRUPT CONTROLLER DATA LINE0.
PICD1 OR APICEN	I/O	PROGRAMMABLE INTERRUPT CONTROLLER DATA LINE1.
PRDY	O	PROBE READY.ASSERTED BY THE PROCESSOR WHEN IT HAS STOPPED EXECUTION IN RESPONSE TO THE R/S# SIGNAL BEING ASSERTED LOW.
PWT	O	THE PAGE WRITE-THROUGHT PIN REFLECTS THE STATE OF THE PAGE ATTRIBUTE BIT.

SYMBOL	TYPE	DESCRIPTION
RESET	I	1.KEEPS THE MICROPROCESSOR FROM OPERATING UNTIL THE POWER SUPPLY VOLTAGES HAVE COME UP AND STSBILIZED. 2.FORCES KNOWN DEFAULT VALUES INTO THE PENTIUM PROCESSOR REGISTER.
R/S#	I	RUN/STOP. WHEN SET HIGH, THE PROCESSOR IS PERMITTED TO RUN NORMALLY.WHEN SET LOW, THE PROCESSOR CEASES TO EXECUTE INSTRUCTIONS AND ENTERS PROBE MODE.
SCYC	I/O	SPLIT CYCLE IS VALID FOR LOCKED BUS CYCLES OLY.SCYC IS ASSERTED WHEN A LOCKED TRANSFER RESULTS IN A MISALIGNED MWMORY ACCESS.
SMI#	I	SYSTEM MANAGEMENT INTERRUPT INFORMS THE PROCESSOR THAT A SYSTEM MANAGEMENT INTERRUPT ROUTINE.RESIDING IN SYSTEM MANAGEMENT ADDRESS SPACE NEEDS TO BE PERFORMED.
SMICAT#	O	SYSTEM MANAGEMENT INTERRUPT ACKNOWLEDGW INFORMS EXTERNAL LOGIC THAT THE PROCESSOR IS IN SYSTEM MANAGEMENT MODE.
TCK	I	TEST CLOCK.USED TO CLOCK STATE INFORMATION AND DATA INTO AND OUT OF DEVICE DURING BOUNDARY SCAN.
TDI	I	TEST INPUT.USED TO SHIFT DATA AND INSTRUCTIONS INTO THE TEST ACCESS PORT IN A SERIAL BIT STREAM.
TDO	O	TEST OUTPUT.USED TO SHIFT DATA OUT OF THE TEST ACCESS PORT IN A SERIAL BIT STREAM.
TMS	I	TEST MODE SELECT.USED TO CONTROL THE STATE OF THE TEST ACCESS PORT CONTROLLER.
TRST#	I	TEST RESET.USED TO FORCE THE TEST ACCESS PORT CONTROLLER INTO AN INITIALIZED STATE.
WB/WT#	I	THE WRITE-BACK OR WRITE THROUGH INPUT ALLOWS EXTERNAL LOGIC TO DETERMINE WHETHER A IS PLACED IN THE WRITE BACK OR WRITE THROUGH STATE.
W/R#	I/O	WRITE OR READ.AT THE START OF A BUS CYCLE,THE PENTIUM PROCESSOR SETS THIS LINE HIGH IF THE CURRENT BUS CYCLE IS A WRITE BUS CYCLE.W/R# IS SET LOW IF THE CURRENT BUS CYCLE IS A READ BUS CYCLE.

# 5027 N/B MAINTENANCE

## 5.2 INTEL FW82439TX MEMORY/PCI/CACHE CONTROLLER (MTXC).

SYMBOL	TYPE	FUNCTION
A(31:1)	I/O	ADDRESS BUS. CONNECT TO THE ADDRESS BUS OF CPU.
BE(7:0)#	I	BYTE ENABLE.THE CPU BYTE ENABLES INDICATE WHICH BYTE LANE THE CURRENT CPU CYCLE IS ACCESSING.
ADS#	I	ADDRESS STATUS.THE CPU ASSERTS ADS# TO INDICATE THAT A NEW BUS CYCLE IS BEING DRIVEN.
BRDY#	O	BUS READY.THE TVX ASSERTS BRDY# TO INDICATES TO THE CPU THAT DATA IS AVAILABLE ON READS OR HAS BEEN RECEIVED ON WRITES.
NA#	O	NEXT ADDRESS.WHEN BURST SRAMS ARE USED IN THE SECOND LEVEL CACHE OR THE SECOND LEVEL CACHE IS DISABLE,THE TVX ASSERTS NA# IN T2 DURING CPU WRITE CYCLES AND WITH THE FIRST ASSERTION OF BRDY# DURING CPU LINE FILLS.
AHOLD	O	ADDRESS HOLD.THE TVX ASSERTS AHOLD WHEN A PCI INITIATOR IS PERFORMING A CYCLE TO DRAM.
EADS#	O	EXTERNAL ADDRESS STROBED.ASSERTS BY THE TVX TO REQUIRE THE FIRST LEVEL CACHE WHEN SERVICING PCI MASTER REFERENCES TO MAIN MEMORY.
BOFF#	O	BACK OFF.ASSERTS BY THE TVX WHEN REQUIRED TO TERMINATE A CPU CYCLE THAT WAS IN PROGRESS.
HITM#	I	HIT MODIFIED.ASSERTED BY THE CPU TO INDICATE THAT THE ADDRESS PRESENTED WITH THE LAST ASSERTION OF EADS# IS MODIFIED IN THE FIRST LEVEL CACHE AND NEED TO BE WRITTEN BACK.
M/ IO# D/ C# W/ R#	I	MEMORY/ IO;DATA/CONTROL;WRITE/READ.ASSERTS BY THE CPU TO INDICATE THE TYPE OF CYCLE THAT THE SYSTEM NEEDS TO PERFORM.
HLOCK#	I	HOST LOCK.ALL CPU CYCLES SAMPLED WITH THE ASSERTION OF HLOCK# AND ADS#,UNTIL THE NEGATION OF HLOCK# MUST BE ATOMIC.
CACHE#	I	CACHEABLE.ASSERTED BY THE CPU DURING A READ CYCLE TO INDICATE THE CPU WILL PERFORM A BURST LINE FILL.ASSERTED BY THE CPU DURING WRITE CYCLE TO INDICATE THE CPU WILL PERFORM A BURST WRITE-BACK CYCLE.

SYMBOL	TYPE	FUNCTION
KEN# / INV	I	CACHE ENABLE.KEN#/INV FUNCTIONS AS BOTH THE KEN# SIGNAL DURING CPU READ CYCLES,AND THE INV SIGNAL DURING L1 SNOOP CYCLES.
SMIACT#	I	SYSTEM MANAGEMENT INTERRUPT ACTIVE.SMIACT# IS ASSERTED BY THE CPU WHEN IT IS IN SYSTEM MANAGEMENT MODE AS A RESULT OF AN SMI.
RAS(5:0)#/ CS(5:0)#	O	ROW ADDRESS STROBE(EDO/SPM).THESE PINS SELECT THE DRAM ROW.CHIP SELECT(SDRAM).THESE PINS ACTIVATE THE SDRAM AND ACCEPT COMMAND WHEN IT IS LOW.
CAS(7:0)/ DQM(7:0)	O	COLUMN ADDRESS STROBE(EDO/SPM).THESE PINS SELECT WHICH BYTES ARE AFFECTED BY A DRAM CYCLE. INPUT/OUTPUT DATA MASK(SDRAM).THESE PINS ACT AS SYNCHRONIZED OUTPUT ENABLEDURING A READ CYCLE AND BYTE MASK DURING A WRITE CYCLE.
SRAS(B:A)#	O	SDRAM ROW ADDRESS STROBE(SDRAM). WHEN ACTIVE LOW THIS SIGNAL LATCHES ROW ADDRESS ON THE POSITIVE EDGE OF THE CLOCK. THIS SIGNAL ALSO ALLOWS ROW ACCESS AND PRE-CHARGE.
HD(63:0)	I/O	HOST DATA. THESE SIGNAL ARE CONNECTED TO HOST DATA BUS.
SCAS(B:A)#	O	SDRAM COLUMN ADDRESS STROBE.SCAS(B:A)# LATCH COLUMN ADDRESS ON THE POSITIVE EDGE OF THE CLOCK WITH SCRAS(B:A)# LOW.THESE SIGNALS ENABLE COLUMN ACCESS.
MA(11:0)	O	MEMORY ADDRESS.
MWEB#	O	MEMORY WRITE ENABLE.MWE# SHOULD BE USED AS THE WRITE ENABLE PIN FOR THE MEMORY DATA BUS.
MWE#	O	MEMORY WRITE ENABLE.MWE# SHOULD BE USED AS THE WRITE ENABLE PIN FOR THE MEMORY DATA BUS.
CADV#	O	CACHE ADVANCE. ASSERTION CAUSES THE PBSRAM IN THE SECONDARY CACHE TO ADVANCE TO THE NEXT QWARD IN THE CACHE LINE.
CKE	O	SDRAM CLOCK ENABLE. WHEN THIS SIGNAL IS DIS-ASSERTED SDRAM ENTERS INTO POWER-DOWN MODE.

# 5027 N/B MAINTENANCE

## 5.2 INTEL FW82439TX MEMORY/PCI/CACHE CONTROLLER (MTXC).

SYMBOL	TYPE	FUNCTION
CADS#	O	CACHE ADDRESS STROBE. ASSERTION CAUSES THE PBSRAM IN THE SECONDARY CACHE TO LOAD THE PBSRAM ADDRESS REGISTER FROM THE PBSRAM ADDRESS PINS.
CKEB	O	SDRAM CLOCK ENABLE. WHEN THIS SIGNAL IS DE-ASSERTED SDRAM ENTERS POWER-DOWN MODE.
CCS#	O	CACHE CHIP SELECT. THE SECONDARY LEVEL CACHE WILL POWER UP, AND PERFORM AN ACCESS IF THIS SIGNAL IS ASSERTED WHEN CADS# IS ASSERTED.
COE#	O	CACHE OUTPUT ENABLE.THE SECONDARY CACHE DATA RAMS DRIVE THE CPUS DATA BUS WHEN COE# IS ASSERTED
GWE#	O	GLOBAL WRITE ENABLE.WHEN THE L2 RAM TYPE IS PIPELINED BURST,GWE# ASSERTED CAUSES A QWORD TO BE WRITTEN INTO THE SECONDARY CACHE DATA RAMS IF THEY ARE POWERED UP.IT IS USED FOR L2 LINE FILLS.
BWE#	O	BYTE WRITE ENABLE/CACHE GLOBAL CHIP SELECT.WHEN THE L2 RAM TYPE IS PIPELINED BURST,THIS PIN FUNCTIONS AS A BYTE WRITE ENABLE.WHEN THE L2 RAM TYPE IS STANDARD ASYNCHRONOUS RAMS,THIS PIN ACTS AS A GLOBAL CHIP SELECT.
TIO(7:0)	I/O	TAG ADDRESS.THESE ARE INTPUTS DURING CPU ACCESS AND OUTPUTS DURING SECOND LEVEL CACHE LINE FILLS AND THE SECOND LEVEL CACHE LINE INVALIDATES DUE TO INQUIRE CYCLES.
TWE#	O	TAG WRITE ENABLE.WHEN ASSERTED.NEW STATE AND TAG ADDRESSES ARE WRITTEN INTO THE EXTERNAL TAG.
AD(31:0)	I/O	ADDRESS DATA.THE STANDARD PCI ADDRESS AND DATA LINES.
C/BE(3:0)#	I/O	COMMAND/BYTE ENABLE.THE COMMAND IS DRIVEN WITH FRAME# ASSERTION,BYTE ENABLES CORRESPONDING TO SUPPLIED OR REQUESTED DATA IS DRIVEN ON FOLLOWING CLOCKS.
FRAME#	I/O	FRAME ASSERTION INDICATES THE ADDRESS PHASE OF PCI TRANSFER.
HCLKIN	I	HOST CLOCK IN.
PCLKIN	I	PCI CLOCK IN.
GNT3#	O	PCI GRANT.PERMISSION IS GIVEN TO THE MASTER TO UED
DEVSEL#	I/O	DEVICE SELECT.THIS SIGNAL IS DRIVEN BY THE TVX WHEN A PCI INITIATOR IS ATTEMPTING TO ACCESS DRAM.
REQ(3:0)#	I	REQUEST.PCI MASTER REQUESTS FOR PCI.

SYMBOL	TYPE	FUNCTION
IRDY#	I/O	INITIATOR READY ASSERTED WHEN THE INITIATOR IS READY FOR DATA TRANSFER.
TRDY#	I/O	TARGET READY ASSERTED WHEN THE TARGET IS READY FOR A DATA TRANSFER.
STOP#	I/O	STOP ASSERTED BY THE TARGET TO REQUEST THE MASTER TO STOP CURRENT TRANSACTION.
LOCK#	I/O	LOCK.UESD TO ESTABLISH, MAINTAIN,AND RELEASE RESOURCE LOCKS ON PCI.
KRQAK	I/O	KRQAK: THIS PIN IS USED WHEN A DRAM BASED CACHE TECHNOLOGY IS USED TO IMPLEMENT AN L2 CACHE. KRQAK IS A BI-DIRECTIONAL REFRESH REQUEST/ACKNOWLEDGE.
GNT(2:0)#	O	PCI GRANT.PERMISSION IS GIVEN TO THE MASTER TO UED PCI.
RST#	I	RESET: WHEN ASSERTED THIS SIGNAL WILL ASYNCHRONOUSLY RESET THE MTXC. THE PCI SIGNALS WILL ALSO TRI-STATE COMPLIANT TO PCI REV 2.0 AND 2.1 SPECIFICATION.
PHOLD#	I	PCI HOLD.THIS SIGNAL COMES FROM PIIX3.IT IS THE PIIX3 REQUEST FOR PCI.
PHLDA#	O	PCI HOLD ACKNOWLEDGE.THIS SIGNAL IS DRIVEN BY THE TVX TO GRANT PCI TO PIIX3.
PAR	I/O	PARITY.A SIGNAL PARITY BIT IS PROVIDED OVER AD(31:0) AND C/BE(3:0).
CLKRUN#	I/O	CLOCK RUN: AN OPEN DRAIN OUTPUT AND ALSO AN INPUT. MTXC REQUESTS THE ECNTRAL RESOURCE TO START, OR MAINTAIN THE PCI CLOCK BY THE ASSERTION OF CLKRUN#. MTXC WILL TRI-STATE CLKRUN# UPON DEASSERTION OF RESET.
TESTIN#	I	TEST IN: NAND-TREE MODE IS ACTIVATED BY DRIVING THIS PIN WHEN REQ# PINS ARE 0.
SUSCLK	I	SUSPEND CLOCK: 32KHZ INPUT FOR DRAM REFRESH CIRCUITY AND HIGH CLOCKING EVENTS IN SUSPEND STATE.
SUSTAT1#	I	SUSPEND STATE: SUS_STAT1 INDICATES MTXC'S POWER PLANE STATUS DURING SUSPEND MODE STATE.
VREF	3.3V OR 5V	VOLTAGE REFERENCE.
VCC	3.3V	MAIN VOLTAGE SUPPLY.
VCC(CPU)	3.3V OR 2.5V	CPU INTERFACE VOLTAGE SUPPLY.
VCC(SUS)	3.3V	SUSPEND WELL VOLTAGE SUPPLY: THESE PINS ARE THE PRIMARY VOLTAGE SUPPLY FOR THE MTXC SUSPEND LOGIC AND I/O.

# 5027 N/B MAINTENANCE

## 5.3 INTEL FW82371AB PCI/ISA BRIDGE (PIIX4).

SYMBOL	TYPE	FUNCTION
PCICLK	I	PCI CLOCK. PROVIDES TIMING FOR ALL TRANSACTIONS ON THE PCI BUS.
AD{31:0}	I/O	PCI ADDRESS/DATA. THE STANDARD PCI ADDRESS AND DATA LINE.
C/BE{3:0}#	I/O	BUS COMMAND AND BYTE ENABLES. THE COMMAND IS DRIVEN WITH FRAME# ASSERTION.
FRAME#	I/O	FRAME: ASSERTION INDICATES THE ADDRESS PHASE OF A PCI TRANSFER. NEGATION INDICATES THAT ONE MORE DATA TRANSFER IS DESIRED BY THE CYCLE INITIATOR.
TRDY#	I/O	TARGET READY. ASSERTED WHEN THE TARGET IS READY FOR A DATA TRANSFER.
IRDY#	I/O	INITIATOR READY. ASSERTED WHEN THE INITIATOR IS READY FOR A DATA TRANSFER.
STOP#	I/O	STOP: ASSERTED BY THE TARGET TO REQUEST THE MASTER TO STOP THE CURRENT TRANSACTION.
IDSEL	I	INITIALIZATION DEVICE SELECT: IDSEL IS USED AS A CHIP SELECT DURING CONFIGURATION THROUGH POSITIVE OR SUBTRACTIVE DECODING.
PAR	O	CALCULATED PARITY SIGNAL: PAR IS EVEN PARITY AND IS CALCULATED ON 36 BIT ---AD{31:0} PLUS C/BE{3:0}#.
SERR#	I	SYSTEM ERROR: SERR# CAN BE PULSED ACTIVE BY ANY PCI DEVICE THAT DETECTS A SYSTEM ERROR CONDITION.
PHOLD#	O	PCI HOLD: THE 82371 ASSERTS THIS TO REQUEST THE PCI BUS.
PHLDA#	I	PCI HOLD ACKNOWLEDGE: THIS SIGNAL IS ASSERTED TO GRANT THE PCI BUS.
CLKRUN#	I/O	CLOCK RUN: AN OPEN DRAIN OUTPUT AND ALSO AN INPUT. MTXC REQUESTS THE CENTRAL RESOURCE TO START, OR MAINTAIN THE PCI CLOCK BY THE ASSERTION OF CLKRUN#. MTXC WILL TRI-STATE CLKRUN# UPON DEASSERTION OF RESET.
DEVSEL#	I/O	DEVICE SELECT: THE PIIX4 ASSERTS DEVSEL# TO CLAIM A PCI TRANSACTION THROUGH POSITIVE DECODING OR SUBTRACTIVE DECODING.
PCIRST#	O	PCI RESET: THE PIIX4 ASSERTS PCIRST# TO RESET DEVICE THAT RESIDE ON THE PCI BUS.

SYMBOL	TYPE	FUNCTION
MEMCSI6#	I/O	MEMORY CHIP SELECT 16: MEMCSI6# IS A DECODE OF LA{23:17} WITHOUT ANY QUALIFICATION OF THE COMMAND SIGNAL LINE. ISA SLAVES THAT ARE 16-BIT MEMORY DEVICES DRIVE THIS SIGNAL LOW. THE PIIX4 IGNORES MEMCSI6# DURING I/O ACCESS CYCLES AND REFRESH CYCLES.
MEMR#	I/O	MEMORY READ: MEMR# IS THE COMMAND TO A MEMORY SLAVE THAT IT MAY DRIVE DATA ONTO THE ISA DATA BUS.
MEMW#	I/O	MEMORY WRITE: MEMW# IS THE COMMAND TO A MEMORY SLAVE THAT IT MAY LATCH DATA FROM THE ISA DATA BUS.
REFRESH#	I/O	REFRESH: AS AN OUTPUT, REFRESH# IS USED BY THE PIIX4 TO INDICATE WHEN A REFRESH CYCLE IS IN PROGRESS.
RSTDRV	O	RESET DRIVE: THE PIIX4 ASSERTS RSTDRV TO RESET DEVICES THAT RESIDE ON THE ISA/EIO BUS. THE PIIX4 ASSERTS THIS SIGNAL DURING A HARD RESET AND DURING POWER-UP.
SA{19:0}	I/O	SYSTEM ADDRESS{19:0}: THESE BI-DIRECTIONAL ADDRESS LINE DEFINE THE SELECTION WITH THE GRANULARITY OF ONE BYTE WITHIN THE ONE MEGABYTE SECTION OF MEMORY DEFINED BY THE LA{23:17} ADDRESS LINES.
SBHE#	I/O	SYSTEM BYTE HIGH ENABLE: SBHE# INDICATES, WHEN ASSERTED, THAT A BYTE IS BEING TRANSFERRED ON THE UPPER BYTE OF THE DATA BUS.
SD{15:0}	I/O	SYSTEM DATA BUS.
SMEMR#	O	STANDARD MEMORY READ: THE PIIX4 ASSERTS SMEMR# TO REQUEST AN ISA MEMORY SLAVE TO DRIVE DATA ONTO THE DATA LINES.
SMEMW#	O	STANDARD MEMORY WRITE: THE PIIX4 ASSERTS SMEMW# TO REQUEST AN ISA MEMORY SLAVE TO ACCEPT DATA FROM THE DATA LINES.
ZEROW#	I	ZERO WAIT STATES: AN ISA SLAVE ASSERTS ZEROW# AFTER ITS ADDRESS AND COMMAND SIGNALS HAVE BEEN DECODED TO INDICATE THAT THE CURRENT CYCLE CAN BE SHORTENED.

# 5027 N/B MAINTENANCE

## 5.3 INTEL FW82371AB PCI/ISA BRIDGE (PIIX4) .

SYMBOL	TYPE	FUNCTION
A20GATE	I	ADDRESS 20 GATE: THIS INPUT FROM THE KEYBOARD CONTROLLER IS INTERNALLY "ORED" WITH BIT 1 OF THE PORT 92 REGISTER, WHICH IS THEN OUTPUT VIA THE A20M# SIGNAL.
BIOSCS#	O	BIOS CHIP SELECT: THIS ACTIVE LOW CHIP SELECT IS DRIVEN ACTIVE DURING READ OR WRITE ACCESSES TO ENABLED BIOS MEMORY RANGES.
BALE	O	BUS ADDRESS LATCH ENABLE: INDICATE THE SBHE# AND ADDRESS SA(19:0), LA(23:17) SIGNAL LINES ARE VALID.
AEN	O	ADDRESS ENABLE: AEN IS ASSERTED DURING DMA CYCLES TO PREVENT I/O SLAVES FROM MISINTERPRETING DMA CYCLES AS VALID I/O CYCLES.
YSCLK	O	ISA SYSTEM CLOCK.
IOCHRDY	I/O	I/O CHANNEL READY: RESOURCES ON THE ISA BUS NEGATE IOCHRDY TO INDICATE THAT ADDITIONAL TIME IS REQUIRED TO COMPLETE THE CYCLE.
IOCS16#	I	16-BIT I/O CHIP SELECT: THIS SIGNAL IS DRIVEN BY I/O DEVICES ON THE ISA BUS TO INDICATE THAT THEY SUPPORT 16-BIT I/O BUS CYCLES.
IOCHK#	I	I/O CHANNEL CHECK: IOCHK# CAN BE DRIVEN BY ANY RESOURCE ON THE ISA BUS. IT INDICATES THAT A PARITY OR AN UNCORRECTABLE ERROR HAS OCCURRED FOR A DEVICE OR MEMORY ON THE ISA BUS. IF ENABLED, A NMI IS GENERATED TO THE CPU.
IOR#	I/O	I/O READ: IOR# IS THE COMMAND TO AN ISA I/O SLAVE DEVICE THAT THE SLAVE MAY DRIVE DATA ON TO THE ISA DATA BUS SD(15:0).
IOW#	I/O	I/O READ: IOR# IS THE COMMAND TO AN ISA I/O SLAVE DEVICE THAT THE SLAVE MAY LATCH DATA FROM THE ISA DATA BUS SD(15:0).
LA(23:17)/GPO{7:1}	I/O	UNLATCHED ADDRESS: THE LA(23:17) ADDRESS LINES ARE BIDI-DIRECTIONAL. THESE ADDRESS LINES ALLOW ACCESSES TO PHYSICAL MEMORY ON THE ISA BUS UP TO 16 MBYTES. IF THE EIO BUS IS USED, THESE SIGNALS BECOMES A GENERAL PURPOSE OUTPUTS.

SYMBOL	TYPE	FUNCTION
KBCCS#	O	KEYBOARD CONTROLLER CHIP SELECT: KBCCS# IS ASSERTED DURING I/O READ OR WRITE ACCESSES TO KBC LOCATIONS 60H AND 64H.
MCCS#	O	MICROCONTROLLER CHIP SELECT: MCCS# IS ASSERTED DURING I/O READ OR WRITE ACCESSES TO IO LOCATIONS 62H AND 66H. IT IS DRIVEN COMBINATORIALLY FROM THE ISA ADDRESSES SA{19:0} AND LA{23:17}
MEMCS16#	OD	MEMORY CHIP SELECT 16: MEMCS16# IS A DECODE OF LA(23:17) WITHOUT ANY QUALIFICATION OF THE COMMAND SIGNAL LINES.
MEMR#	I/O	MEMORY READ: MEMR# IS THE COMMAND TO THE MEMORY SLAVE THAT IT MAY DRIVE DATA ON TO THE ISA DATA BUS.
MEMW#	I/O	MEMORY READ: MEMR# IS THE COMMAND TO THE MEMORY SLAVE THAT IT MAY LATCH DATA ON TO THE ISA DATA BUS.
SMEMR#	O	STANDARD MEMORY READ: THE 82371 ASSERTS SMEMR# TO REQUEST AN ISA MEMORY SLAVE TO DRIVEN DATA ON TO THE DATA LINES.
SMEMW#	O	STANDARD MEMORY WRITE: THE 82371 ASSERTS SMEMW# TO REQUEST AN ISA MEMORY SLAVE TO ACCEPT DATA FROM THE DATA LINES.
ZEROWS#	I	ZERO WAIT-STATES: AN ISA SLAVE ASSERTS ZEROWS# AFTER ITS ADDRESS AND COMMAND SIGNALS HAVE BEEN DECODED TO INDICATE THAT THE CURRENT CYCLE CAN BE SHORTENED.
SD(15:0)	I/O	SYSTEM DATA: SD(15:0) PROVIDE THE 16-BIT DATA PATH FOR DEVICES RESIDING ON THE ISA BUS.
DREQ(7:3,3:0)	I	DMA REQUEST: THE DREQ LINES ARE USED TO REQUEST DMA SERVICE FROM THE 82371 DMA CONTROLLER OR FOR A 16-BIT MASTER TO GAIN CONTROL OF THE ISA BUS.
DACK(7:3,3:0)#	O	DMA ACKNOWLEDGE: THE DACK OUTPUT LINES INDICATE THAT A REQUEST FOR DMA SERVICE HAS BEEN GRANTED BY THE 82371 OR THAT A 16-BIT MASTER HAS BEEN GRANTED THE BUS.

# 5027 N/B MAINTENANCE

## 5.3 INTEL FW82371AB PCI/ISA BRIDGE (PIIX4) .

SYMBOL	TYPE	DESCRIPTION
PCSO#	O	PROGRAMMABLE CHIP SELECTS: THESE ACTIVE
PCSl#		LOW CHIP SELECTS ARE ASSERTED FOR ISA IO CYCLES WHICH ARE GENERATED BY PCIMASTERS AND WHICH HIT THE PROGRAMMABLE IO RANGES DEFINED IN THE POWER MANAGEMENT SECTION .
RCIN#	I	RESET CPU: THIS SIGNAL FROM THE KEYBOARD CONTROLLER IS USED TO GENERATE AN INT SIGNAL TO THE CPU .
RTCALE	O	REAL TIME CLOCK ADDRESS LATCH ENABLE: RTCALE IS USED TO LATCH THE APPROPRIATE MEMORY ADDRESS INTO THE RTC. A WRITE TO PORT 70H WITH THE APPROPRIATE RTC MEMORY ADDRESS THAT WILL BE WRITTEN TO OR READ FROM CAUSES RTCALE TO BE ASSERTED .
RTCCS#	O	REAL TIME CLOCK CHIP SELECT: RTCCS# IS ASSERTED DURING READ OR WRITE IO ACCESSES TO RTC LOCATION 71H .
XDIR#	O	X-BUS TRANSCEIVER DIRECTION: XDIR# IS TIED DIRECTLY TO THE DIRECTION CONTROL OF A 74X245 THAT BUFFERS THE X-BUS DATA .
XOE#	IO	X-BUS TRANSCEIVER DIRECTION: XDIR# IS TIED DIRECTLY TO THE OUTPUT ENABLE OF A 74X245 THAT BUFFERS THE X-BUS DATA .
DACK {3:0} DACK {7:5}	O	DMA ACKNOWLEDGE: THE DACK OUTPUT LINES INDICATE THAT A REQUEST FOR DMA SERVICE HAS BEEN GRANTED BY THE PIIX4 OR THAT A 16 BIT MASTER HAS BEEN GRANTED THE BUS .
DREQ {3:0} DREQ {7:5}	I	DMA REQUEST: THE DREQ LINES ARE USED TO REQUEST DMA SERVICE FROM THE PIIX4S DMA CONTROLLER OR FOR A 16-BIT MASTER TO GAIN CONTROL OF THE ISA EXPANSION BUS .
REQ {A C}#	I	PC/PCIDMA REQUEST .
GNT {A C}#	O	PC/PCIDMA ACKNOWLEDGE .
TC	O	TERMINAL COUNT: THE PIIX4 ASSERTS TC TO DMA SLAVES AS A TERMINAL COUNT INDICATOR THE PIIX4 ASSERTS TC AFTER A NEW ADDRESS HAS BEEN OUTPUT. IF THE BYTE COUNT EXPIRES WITH THAT TRANSFER. TC REMAINS ASSERTED UNTIL AEN IS NEGATED .

SYMBOL	TYPE	DESCRIPTION
APICACK#	O	THIS ACTIVE LOW OUTPUT SIGNAL IS ASSERTED BY THE PIIX4 AFTER ITS INTERNAL BUFFERS ARE FLUSHED IN RESPONSE TO THE APICREQ# SIGNAL . WHEN THE IO APIC SAMPLES THIS SIGNAL ASSERTED IT KNOWS THAT THE PIIX4S BUFFERS ARE FLUSHED AND THAT IT CAN PROCEED TO SEND THE APIC INTERRUPT .
APICCS#	O	APIC CHIP SELECT: THIS ACTIVE LOW OUTPUT SIGNAL IS ASSERTED WHEN THE APIC CHIP SELECT IS ENABLED AND A PCIORIGINATED CYCLE IS POSITIVELY DECODED WITHIN THE PROGRAMMED IO APIC ADDRESS SPACE .
APICREQ#	I	APIC REQUEST: THIS ACTIVE LOW INPUT SIGNAL IS ASSERTED BY AN EXTERNAL APIC DEVICE PRIOR TO SENDING AN INTERRUPT OVER THE APIC SERIAL BUS .
INTR	O	INTERRUPT .
IRQ0	O	INTERRUPT REQUEST 0: THIS OUTPUT REFLECTS THE STATE OF THE INTERNAL IRQ0 SIGNAL FROM THE SYSTEM TIMER. IF THE EXTERNAL APIC IS NOT USED, THEN THIS GENERAL-PURPOSE OUTPUT .
IRQ1	IO	INTERRUPT REQUEST 1: IRQ1 IS ALWAYS EDGE TRIGGERED AND CAN NOT BE MODIFIED BY SOFTWARE TO LEVEL SENSITIVE. A LOW TO HIGH TRANSITION ON IRQ1 IS LATCHED BY THE PIIX4 .
IRQ 3:7 9:11 14:15	IO	INTERRUPT REQUESTS 3:7,9:11,14:15. THE IRQ SIGNALS PROVIDE BOTH SYSTEM BOARD COMPONENTS AND ISA BUS IO DEVICES WITH A MECHANISM FOR ASYNCHRONOUSLY INTERRUPTING THE CPU .
IRQ8#	IO	IRQ8#: IRQ8# IS ALWAYS AN ACTIVE LOW EDGE TRIGGERED INTERRUPT AND CAN NOT BE MODIFIED BY SOFTWARE .
IRQ12M	IO	INTERRUPT REQUEST 12: IN ADDITION TO PROVIDING THE STANDARD INTERRUPT FUNCTION AS DESCRIBED IN THE PIN DESCRIPTION FOR IRQ 3:7, 9:11, 14:15, THIS PIN CAN ALSO BE PROGRAMMED TO PROVIDE THE MOUSE INTERRUPT FUNCTION .

# 5027 N/B MAINTENANCE

## 5.3 INTEL FW82371AB PCI/ISA BRIDGE (PIIX4) .

SYMBOL	TYPE	DESCRIPTION
PIRQ {A-D}#	I/O	PROGRAMMABLE INTERRUPT REQUEST:THE PIRQ# SIGNAL ARE ACTIVE LOW ,LEVEL SENSITIVE ,SHAREABLE INTERRUPT INPUTS. THEY CAN BE INDIVIDUALLY STEERED TO ISA INTERRUPTS IRQ {3:7,9:12,14:15}.THE USB CONTROLLER USES PIRQ {D} AS ITS OUTPUT SIGNAL.
SERIRQ	I/O	SERIAL INTERRUPT REQUEST:SERIAL INTERRUPT INPUT DECODER ,TYPICALLY USED IN CONJUNCTION WITH THE DISTRIBUTED DMA PROTOCOL.
RTCX {2:1}	O	CRYSTAL INPUTS:THESE CONNECTED DIRECTLY TO THE 32.768KHZ CRYSTAL.
A20M#	OD	ADDRESS 20 MASK:THE PIIX4 ASSERTS A20M# TO THE CPU BASED ON AN INTERNAL "OR" OF PORT 92 REGISTER.
CPURST	OD	CPU RESET.THE PIIX4 ASSERTS CPURST TO RESET THE CPU.
FEER#	I	NUMERIC COPROCESSOR ERROR .THIS PIN FUNCTIONS AS A FEER# SIGNAL SUPPORTING COPROCESSOR ERRORS.THIS SIGNAL IS TIED TO THE COPROCESSOR ERROR SIGNAL ON THE CPU. THE PIIX4 THEN ASSERTS THE INT OUTPUT TO THE CPU.
IGNNE#	OD	IGNORE ERROR:THIS SIGNAL IS CONNECTED TO THE IGNORE ERROR PIN ON THE CPU.IGNNE# IS ONLY USED IF THE PIIX4 COPROCESSOR ERROR REPORTING FUNCTION IS ENABLED.
INIT	OD	INITIALIZATION:INIT IS ASSERTED IN RESPONSE TO ANY ONE OF THE FOLLOWING CONDITION. WHEN THE SYSTEM HARD RESET BIT IN THE TURBO-RESET CONTROL REGISTER IS RESET TO 0 AND THE RESET CPU BIT TOGGLES FROM 0 TO 1, THE PIIX4 INITIATES A SOFT RESET BY ASSERTING INIT.THE PIIX4 ALSO ASSERTS INIT IF A SHUT DOWN SPECIAL CYCLE IS DECODED ON THE PCI BUS.IF THE RCIN# SIGNAL IS ASSERTED .OR IF A WRITE OCCURS TO PORT 92H.

SYMBOL	TYPE	DESCRIPTION
INTR	OD	CPU INTERRUPT:INTR IS DRIVEN BY THE PIIX4 TO SIGNAL THE CPU THAT A INTERRUPT REQUEST IS PENDING AND NEEDS TO BE SERVICED.
NMI	OD	NON-MASKABLE INTERRUPT:NMI IS USED TO FORCE A NON-MASKABLE INTERRUPT TO THE CPU.
SLP#	OD	SLEEP:THIS SIGNAL IS OUTPUT TO THE PENTIUM PRO PROCESSOR IN ORDER TO PUT IT INTO SLEEP STATE.
SMI#	OD	SYSTEM MANAGEMENT INTERRUPT:SMI# IS AN ACTIVE LOW SYNCHRONOUS OUTPUT THAT IS ASSERTED BY THE PIIX4 IN RESPONSE TO ONE OF MANY ENABLED HARDWARE OR SOFTWARE EVENTS.
STPCLK#	OD	STOP CLOCK: STPCLK# IS AN ACTIVE LOW SYNCHRONOUS OUTPUT THAT IS ASSERTED BY THE PIIX4 IN RESPONSE TO ONE OF MANY HARDWARE OR SOFTWARE EVENTS.
CLK48	I	48 MHZ CLOCK.IT IS USED BY INTERNAL USB HOST CONTROLLER.
OSC	I	14.318 MHZ CLOCK .ITS USED BY THE INTRENAL 8254 TIMER.
SUSCLK	O	SUSPEND CLOCK :32.768KHZ OUTPUT CLOCK PROVIDED TO THE HOST-TO-PCIBRIDGE USED FOR MAINTENANCE OF DRAM REFRESH.
PDA {2:0}	O	PRIMARY DISK ADDRESS 2:0:THESE SIGNALS INDICATE WHICH BYTE IN EITHER THE ATA COMMAND BLOCK OR CONTROL BLOCK IS BEING ADDRESSING.
PDCS1#	O	PRIMARY DISK CHIP SELECT FOR 100 RANGE:FOR ATA COMMAND REGISTER BLOCK .IF THE IDE SIGNALS ARE CONFIGURED FOR PRIMARY AND SECONDARY ,THIS OUTPUT SIGNAL IS CONNECTED TO THE CORRESPONDING SIGNAL ON THE PRIMARY IDE CONNECTOR .IF THE IDE SIGNALS ARE CONFIGURED FOR PRIMARY 0 AND 1,THIS SIGNAL IS USED FOR THE PRIMARY 0 CONNECTOR.

# 5027 N/B MAINTENANCE

## 5.3 INTEL FW82371AB PCI/ISA BRIDGE (PIIX4) .

SYMBOL	TYPE	DESCRIPTION
PDCS3#	O	PRIMARY DISK CHIP SELECT FOR 300 RANGE:FOR ATA CONTROL REGISTER BLOCK .IF THE IDE SIGNALS ARE CONFIGURED FOR PRIMARY AND SECONDARY ,THIS OUTPUT SIGNAL IS CONNECTED TO THE CORRESPONDING SIGNAL ON THE PRIMARY IDE CONNECTOR .IF THE IDE SIGNALS ARE CONFIGURED FOR PRIMARY 0 AND 1,THIS SIGNAL IS USED FOR THE PRIMARY 0 CONNECTOR .
PDD {15:0}	IO	PRIMARY DISK DATA {15:0}:THESE SIGNALS ARE USED TO TRANSFER DATA TO OR FROM THE IDE DEVICE .
PDDACK#	O	PRIMARY DMA ACKNOWLEDGE:THIS SIGNAL DIRECTLY DRIVES THE DAK# SIGNAL .IT IS ASSERTED BY THE PIIX4 TO INDICATE TO IDE DMA SLAVE DEVICES THAT A GIVEN DATA TRANSFER CYCLE IS A DMA DATA TRANSFER CYCLE .
PDDREQ	I	PRIMARY DISK DMA REQUEST:THIS INPUT SIGNAL IS DIRECTLY DRIVEN FROM THE DRQ SIGNAL .IT IS ASSERTED BY THE IDE DEVICE TO REQUEST A DATA TRANSFER .AND USED IN CONJUNCTION WITH THE PCIBUS MASTER IDE FUNCTION .
PDIOR#	O	PRIMARY DISK IO READ:THIS IS THE COMMAND TO THE IDE DEVICE THAT IT MAY DRIVE DATA ONTO THE DD {15:0} LINE .
PDIOW#	O	PRIMARY DISK IO READ:THIS IS THE COMMAND TO THE IDE DEVICE THAT IT MAY LATCH DATA FROM THE DD {15:0} LINE .
PIORDY	I	PRIMARY IO CHANNEL READY:THIS IS INPUT SIGNAL IS DIRECTLY DRIVEN BY THE CORRESPONDING IO READY SIGNAL .
SDA {2:0}	O	SECONDARY DISK ADDRESS 2:0:THESE SIGNALS INDICATE WHICH BYTE IN EITHER THE ATA COMMAND BLOCK OR CONTROL BLOCK IS BEING ADDRESSED .
SDDREQ	I	SECONDARY DISK DMA REQUEST:THIS INPUT SIGNAL IS DIRECTLY DRIVEN FROM THE DRQ SIGNAL .IT IS ASSERTED BY THE IDE DEVICE TO REQUEST A DATA TRANSFER .

SYMBOL	TYPE	DESCRIPTION
SDCS3#	O	SECONDARY CHIP SELECT FOR 300 RANGE:FOR ATA COMMAND REGISTER BLOCK .IF THE IDE SIGNALS ARE CONFIGURED FOR PRIMARY AND SEDONARY ,THIS OUTPUT SIGNAL IS CONNECTED TO THE CORRESPONDING SIGNAL ON THE SECONDARY IDE CONNECTOR .IF THE IDE SIGNALS ARE CONFIGURED FOR PRIMARY 0 AND PRIMARY 1 ,THIS SIGNAL IS USED FOR THE PRIMARY 1 CONNECTOR .
SDD {15:0}	IO	SECONDARY DISK DATA {15:0}:THIS SIGNALS ARE USED TO TRANSFER DATA TO OR FROM THE IDE DEVICE .
SDDACK#	O	SECONDARY DMA ACKNOWLEDGE:THIS SIGNAL DIRECTLY DRIVES THE DAK# SIGNAL .IT IS ASSERTED BY THE PIIX4 TO INDICATE TO IDE DMA SLAVE DEVICES THAT A GIVEN DATA TRANSFER CYCLE IS A DMA DATA TRANSFER CYCLE .
SDIOR#	O	SECONDARY DISK IO READ:THIS IS THE COMMAND TO THE IDE DEVICE THAT IT MAY DRIVE DATA ONTO THE DD {15:0} LINES .
SDIOW#	O	SECONDARY DISK IO WRITE:THIS IS THE COMMAND TO THE IDE DEVICE THAT IT MAY LATCH DATA FROM THE DD {15:0} LINES .
SIORDY	I	SECONDARY IO CHANNEL READY:THIS INPUT SIGNAL IS DIRECTLY DRIVEN BY THE CORRESPONDING IO READY SIGNAL .
OC {1:0}#	I	OVER CURRENT DETECT:THIS SIGNALS ARE USED TO MONITOR THE STATUS OF THE USB POWER SUPPLY LINES .
USBP0+ , USBP0-	IO	SERIAL BUS PORT0:THIS SIGNAL PAIR COMPRISES THE DIFFERENTIAL DATA SIGNAL FOR USB PORT 0 .
USBP1+ , USBP1-	IO	SERIAL BUS PORT1:THIS SIGNAL PAIR COMPRISES THE DIFFERENTIAL DATA SIGNAL FOR USB PORT10 .
BATLOW#	I	BATTERY LOW :INDICATES THAT BATTERY POWER IS LOW .
CPU_STP#	O	CPU CLOCK STOP:ACTIVE LOW CONTROL SIGNAL TO THE CLOCK GENERATOR .USED TO DISABLE THE CPU CLOCK OUTPUTS .

# 5027 N/B MAINTENANCE

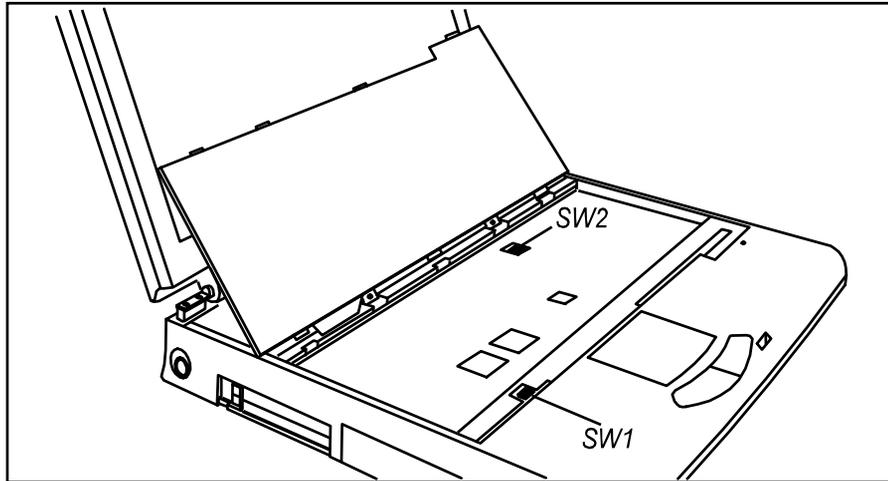
## 5.3 INTEL FW82371AB PCI/ISA BRIDGE (PIIX4) .

SYMBOL	TYPE	DESCRIPTION
SDCS1#	O	SECONDARY CHIP SELECT FOR 100 RANGE:FOR ATA COMMAND REGISTER BLOCK .IF THE IDE SIGNALS ARE CONFIGURED FOR PRIMARY AND SEDONDARY ,THIS OUTPUT SIGNAL IS CONNECTED TO THE CORRESPONDING SIGNAL ON THE SECONDARY IDE CONNECTOR .IF THE IDE SIGNALS ARE CONFIGURED FOR PRIMARY 0 AND PRIMARY 1 ,THIS SIGNAL IS USED FOR THE PRIMARY 1 CONNECTOR .
EXTSM #	I	EXTERNAL SYSTEM MANAGEMENT INTERRUPT: EXTSM # IS A FALLING EDGE TRIGGERED INPUT TO THE PIIX4 INDICATING THAT AN EXTERNAL DEVICE IS REQUESTING THE SYSTEM TO ENTER SMM MODE .
LID	I	LID INPUT:THIS SIGNAL CAN BE USED TO MONITOR THE OPENING AND CLOSING OF THE DISPLAY LID OF A NOTEBOOK COMPUTER .IT CAN BE USED TO DETECT BOTH LOW TO HIGH TRANSITION OR A HIGH TO LOW TRANSITION AND GENERATE AN SM # IF ENABLED .
PCIREQ {3:0}#	I	PCIREQUEST:PCIMASTER REQUESTS USED TO REQUEST ACCESS TO PCIBUS IN SYSTEM PCI ARBITER .MONITORED BY PIIX4 AS POWER MANAGEMENT EVENTS .
PCI_STP#	O	PCICLOCK STOP:ACTIVE LOW CONTROL SIGNAL TO THE CLOCK GENERATOR USED TO DISABLE THE PCICLOCK OUTPUTS .
PWRBTN	I	POWER BUTTON:INPUT USED TO MONITOR SYSTEM ON/OFF BUTTON OR SWITCH .
R#	I	RING INDICATE:RESUME EVENT INPUT WHICH CAN BE USED FOR WAKEUP FROM MODEM .
SM_BCLK	IO	SM BUS CLOCK:SYSTEM MANAGEMENT BUS CLOCK USED TO SYNCHRONIZE TRANSFER OF DATA ON SM BUS .

SYMBOL	TYPE	DESCRIPTION
RSMRST#	I	RESUME RESET:RESETS THE INTERNAL RESUME WELL POWER PLANE LOGIC .
SM_BALERT#	I	SM BUS ALERT:RESUME EVENT INPUT WHICH CAN BE USED FOR WAKEUP FROM SM BUS .
SM_BDATA	IO	SM BUS DATA:SERIAL DATA LINE USED TO TRANSFER DATA ON SM BUS .
SUSA#	O	SUSPEND PLANE A CONTROL:USED TO CONTROL THE PRIMARY POWER PLANE .
SUSB#	O	SUSPEND PLANE B CONTROL:USED TO CONTROL THE SECONDARY POWER PLANE .
SUSC#	O	SUSPEND PLANE C CONTROL:USED TO CONTROL THE TERTIARY POWER PLANE .
SUS_STAT1#	O	SUSPEND STATUS 1:THIS SIGNAL WILL TYPICALLY CONNECT TO THE HOST-TO-PCIBRIDGE AND IS USED TO PROVIDE INFORMATION ON SYSTEM SUSPEND STATE .
SUS_STAT2#	O	SUSPEND STATUS 1:THIS SIGNAL WILL TYPICALLY CONNECT TO THE PERIPHERALS AND IS USED TO PROVIDE INFORMATION ON SYSTEM SUSPEND STATE .
THRM #	I	THERMAL DETECT:ACTIVE LOW SIGNAL GENERATED BY EXTERNAL HARDWARE TO START THE HARDWARE CLOCK THROTTLING MODE .
ZZ	O	LOW -POWER MODE FOR L2CACHE SRAM :THIS SIGNAL IS USED TO POWER DOWN THE L2CACHES DATA SRAMS WHEN THE CLOCK LOGIC PLACES THE CPU INTO EITHER THE STOP CLOCK OR STOP GRANT STATES .
GPI{X Y}	I	GENERAL PURPOSE INPUTS:THESE SIGNALS CAN BE CONTROLLED VIA REGISTERS LOCATED IN FUNCTION 3 SYSTEM IO SPACE .
GPO {A B}	O	GENERAL PURPOSE OUTPUTS:THESE SIGNALS CAN BE MONITORED VIA REGISTERS LOCATED IN FUNCTION 3 SYSTEM IO SPACE .

# 5027 N/B MAINTENANCE

## 6.SWITCH & JUMPERS SETTING



SW1 Selecting CPU Voltage

Voltage	SW 1			
	Pin1	Pin2	Pin3	Pin4
1.8	OFF	OFF	OFF	OFF
1.9	OFF	OFF	OFF	ON
2.0	OFF	OFF	ON	OFF
2.1	OFF	OFF	ON	ON
2.2	OFF	ON	OFF	OFF
2.3	OFF	ON	OFF	ON
2.4	OFF	ON	ON	OFF
2.5	OFF	ON	ON	ON
2.6	ON	OFF	OFF	OFF
2.7	ON	OFF	OFF	ON
2.8	ON	OFF	ON	OFF
2.9	ON	OFF	ON	ON
3.0	ON	ON	OFF	OFF
3.1	ON	ON	OFF	ON
3.2	ON	ON	ON	OFF
3.3	ON	ON	ON	ON

SW2 CPU Local Bus Frequency CPU Bus/Core Ratio

	Pin1
60MHz	ON
66MHz	OFF

Bus/Core Ratio	Pin2	Pin3
2/3(P54C only)	OFF	OFF
1/3	OFF	ON
1/2	ON	OFF
3/5	ON	ON

Discharging CMOS

	Pin4
Normal	ON
Rest RTC	OFF

	Pin1	Pin2	Pin3
133MHz	OFF	ON	OFF
150MHz	ON	ON	ON
166MHz	OFF	ON	ON
200MHz	OFF	OFF	ON
233MHz	OFF	OFF	OFF

# 5027 N/B MAINTENANCE

## **7.ASSEMBLY & DISASSEMBLY**

### 7.1 SYSTEM VIEW

### **MODULAR COMPONENTS**

7.2 RIGHT BAY DEVICE

7.3 HARD DISK DRIVE

7.4 BATTERY PACK

7.5 CPU

7.6 MEMORY CARD

7.7 FAX/ MODEM/ VOICE CARD

7.8 KEYBOARD

### **LCD ASSEMBLY COMPONENTS**

7.9 LCD

7.10 INVERTER BOARD

### **BASE UNIT COMPONENTS**

7.11 BOTTOM CHASSIS

7.12 D/D BOARD

7.13 SYSTEM BOARD

7.14 TOUCH-PAD

## 7.ASSEMBLY & DISASSEMBLY

### 7.1 SYSTEM VIEW

#### 7.1.1 RIGHT-SIDE VIEW (FIG 7-1)

1. FLOPPY DISK DRIVE
2. PHONE LINE CONNECTOR (  )
3. AUDIO OUTPUT CONNECTOR (  )
4. MICROPHONE CONNECTOR (  )
5. AUDIO INPUT CONNECTOR (  )
6. IR PORT

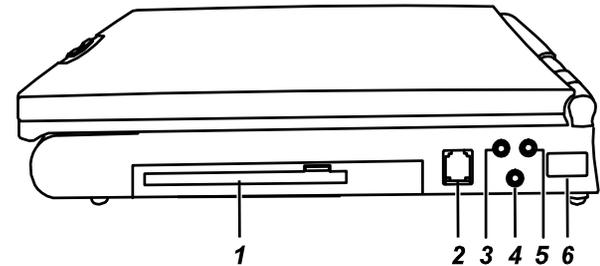


Figure 7-1. Right-Side View

#### 7.1.2 LEFT-SIDE VIEW (FIG 7-2)

1. VIDEO OUT CONNECTOR (  )
2. PC CARD SLOTS
3. HARD DISK DRIVE

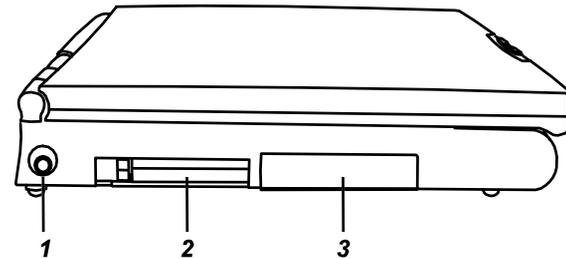


Figure 7-2. Left-Side View

# 5027 N/B MAINTENANCE

## 7.ASSEMBLY & DISASSEMBLY

### 7.1.3 REAL-SIDE VIEW (FIG 7-3)

1. PS/2 MOUSE/KEYBOARD PORT (  )
2. SERIAL PORT (  )
3. PARALLEL PORT (  )
4. VGA PORT (  )
5. EXPANSION CONNECTOR (  )
6. USB PORT (  )
7. POWER CONNECTOR (  )

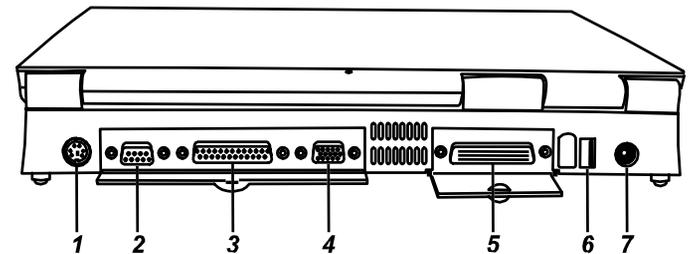


Figure 7-3. Rear View

### 7.1.4 BOTTOM VIEW (FIG 7-4)

1. BATTERY PACK

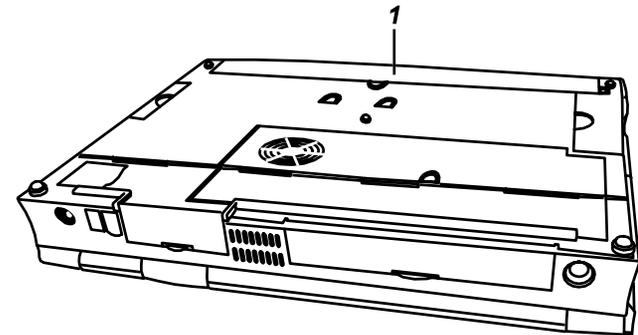


Figure 7-4. Bottom View

# 5027 N/B MAINTENANCE

## 7.ASSEMBLY & DISASSEMBLY

### 7.1.5 TOP-OPEN VIEW (FIG 7-5,FIG 7-6)

1. LCD DISPLAY
2. STEREO SPEAKER SET
3. KEYBOARD
4. TOUCHPAD
5. MICROPHONE
6. POWER BUTTON (  )
7. INDICATOR PANEL
8. POWER ON INDICATOR

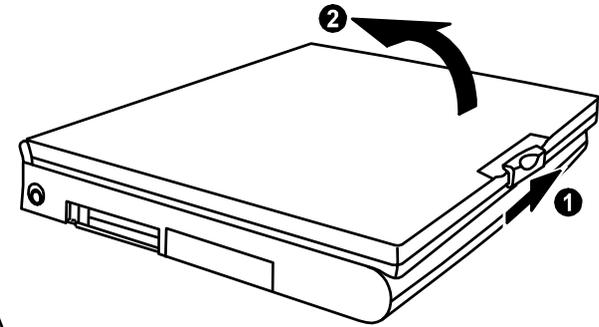


Figure 7-5. Opening the Cover

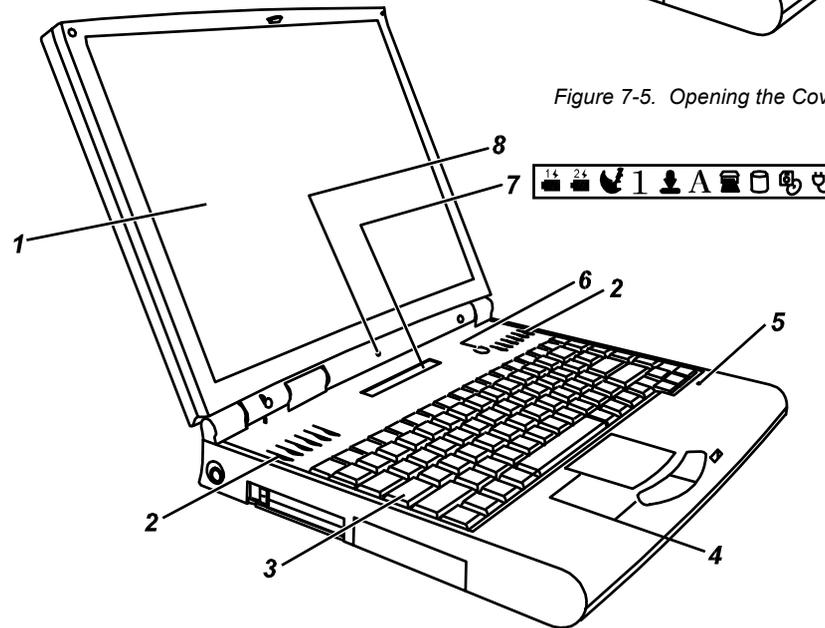


Figure 7-6. Top-Open View

# 5027 N/B MAINTENANCE

## 7.ASSEMBLY & DISASSEMBLY

### 7.2 SYSTEM DISASSEMBLY

#### 7.2.1 RIGHT BAY DEVICE

THE RIGHT BAY OF THE NOTEBOOK CAN ACCOMMODATE THE FOLLOWING DEVICES:

- \* FLOPPY DISK DRIVE
- \* CD-ROM DRIVE

#### DISASSEMBLY

1. PLACE THE NOTEBOOK UPSIDE DOWN.
2. TO REMOVE THE RIGHT BAY DEVICE, PRESS THE LOCKING LATCH TOWARD THE UNLOCKED POSITION AND PULL OUT THE DEVICE MODULE.

#### RE-ASSEMBLY

SLIDE THE DEVICE MODULE INTO THE RIGHT BAY UNTIL THE LOCKING LATCH CLICKS INTO THE LOCKED POSITION. (FIG 7-7)

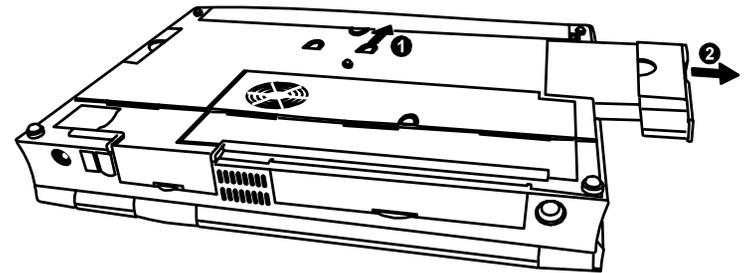


Figure 7-7. Removing the Right Bay Device

## 7.ASSEMBLY & DISASSEMBLY

### 7.2.2 HARD DISK DRIVE

#### DISASSEMBLY

1. PLACE THE NOTEBOOK UPSIDE DOWN
2. PRESS THE LOCKING LATCH TOWARD THE UNLOCKED POSITION AND PULL OUT THE HARD DISK DRIVE MODULE.(Fig 7-8)
3. REMOVE THE REAR COVER PLATE BY REMOVING TWO CONNECTORS. (Fig 7-9)
4. REMOVE THREE SCREWS ON BOTH SIDES OF THE HARD DISK DRIVE BRACKET. (Fig 7-10)
5. REMOVE THE TOP COVER FROM THE BRACKET BY LIFTING THE REAR END AND THEN DETACHING THE FRONT TAP.(Fig 7-11)

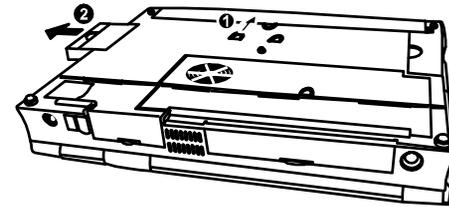


Figure 7-8. Removing the Hard Disk Drive Module

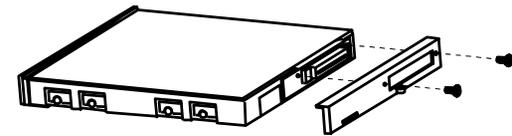


Figure 7-9. Removing the Rear Cover Plate

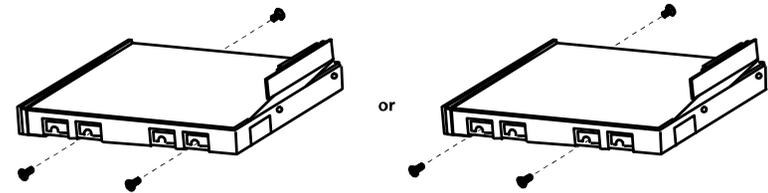


Figure 7-10. Removing the Hard Disk Drive Bracket Screws

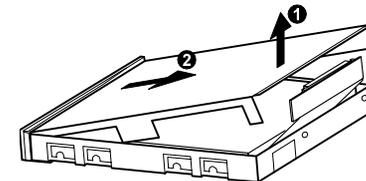


Figure 7-11. Removing the Bracket Top Cover

## 7.ASSEMBLY & DISASSEMBLY

### 7.2.2 HARD DISK DRIVE

6. LIFT UP THE HARD DISK DRIVE AND UNPLUG THE CONNECTOR CARD.

### RE-ASSEMBLY

1. ALIGN THE CONNECTOR CARD WITH THE HARD DISK DRIVE CONNECTOR AND FIRMLY PLUG THE CONNECTOR. THEN ATTACH THE HARD DISK DRIVE TO THE BRACKET.(ref fig 7-12)
2. ATTACH THE TOP COVER TO THE BRACKET BY INSERTING THE FRONT TAB AT AN ANGLE AND THEN LOWERING THE REAR END.(ref fig 7-11)
3. SECURE WITH THREE SCREWS ON BOTH SIDE.(ref fig 7-10)
4. FOLD THE CONNECTOR CARD AS SHOWN BELOW. THEN ATTACH THE REAR COVER PLATE TO THE HARD DISK DRIVE AND SECURE WITH TWO SCREWS.(ref fig 7-9)

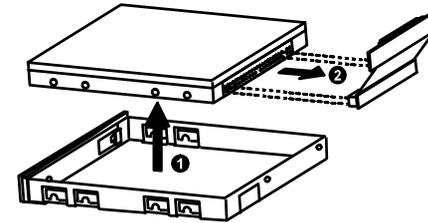


Figure 7-12. Removing the Hard Disk Drive and Connector Card

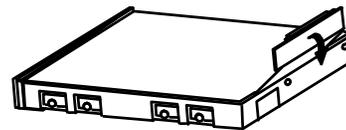


Figure 7-13. Folding the Connector Card

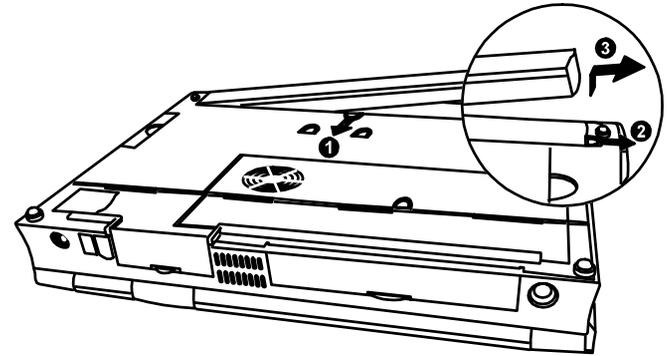
5. SLIDE THE HARD DISK DRIVE MODULE INTO THE LEFT BAY UNTIL THE LOCKING LATCH CLICKS INTO THE LOCKED POSITION.(ref fig 7-8)

## 7.ASSEMBLY & DISASSEMBLY

### 7.2.3 BATTERY PACK

#### DISASSEMBLY

1. PLACE THE NOTEBOOK UPSIDE DOWN
2. SLIDE THE SIDE LOCKING LATCH TO THE UNLOCKED POSITION. PRESS THE END LOCKING LATCH OUTWARDS TO THE UNLOCKED POSITION AND, WHILE KEEPING THE LATCH IN THE UNLOCKED POSITION, LIFT UP THE END OF THE BATTERY PACK AND PULL IT OUT OF THE COMPARTMENT.



*Figure 7-14. Removing the Battery Pack*

#### RE-ASSEMBLY

1. INSERT THE CONNECTOR END FIRST AND THEN PUT DOWN THE OTHER END. SLIDE THE SIDE LOCKING LATCH TO THE LOCKED POSITION. (ref fig 7-14)

## 7.ASSEMBLY & DISASSEMBLY

### 7.2.4 CPU

#### DISASSEMBLY

1. PLACE THE NOTEBOOK UPSIDE DOWN
2. REMOVE THE COMPARTMENT COVER SCREW.
3. SLIDE THE COMPARTMENT COVER TOWARD THE LEFT AND LIFT THE COVER INNER EDGE (FACING THE FRONT OF THE NOTEBOOK) TO REMOVE THE COVER.
4. TO REMOVE THE HEAT SINK, FOLLOW THESE STEPS:
  - a. UNPLUG THE FAN POWER CORD FROM THE SYSTEM BOARD.
  - b. REMOVE THE FOUR SCREWS FROM THE HEAT SINK.

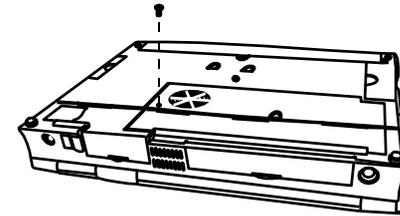


Figure 7-15. Removing the Compartment Cover Screw

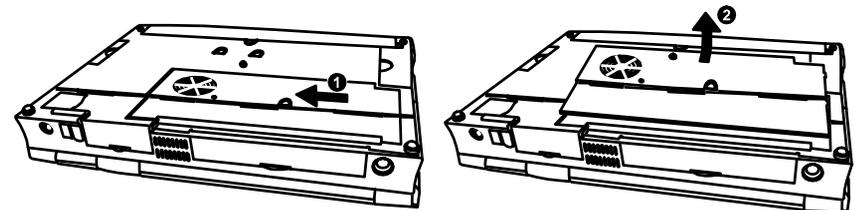


Figure 7-16. Removing the Compartment Cover

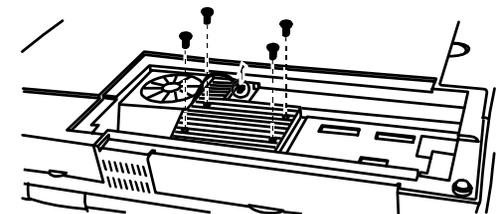


Figure 7-17. Removing the Heat Sink

# 5027 N/B MAINTENANCE

## 7.ASSEMBLY & DISASSEMBLY

### 7.2.4 CPU

5. TO REMOVE THE CPU, INSERT A FLAT SCREWDRIVER TO THE OPEN SIDE OF THE SOCKET AND PUSH THE SCREWDRIVER TOWARD THE CPU TO LOOSEN THE CPU.

### RE-ASSEMBLY

1. TO INSTALL THE CPU , ALIGN THE BEVELED CORNER ON THE CPU WITH THE BEVELED CORNER OF THE SOCKET AND INSERT THE CPU PINS INTO THE HOLES. INSERT A FLAT SCREWDRIVER TO THE CLOSE SIDE OF THE SOCKET AND PUSH THE SCREWDRIVER TOWARD THE CPU TO SECURE THE CPU IN PLACE. (ref fig 7-18)
2. ATTACH THE HEAT SINK TO CPU AND SECURE WITH FOUR SCREWS. RECONNECT THE FAN POWER CORD. (ref fig 7-17)
3. MAKE SURE SW1 AND SW2 ARE ACCORDING TO THE CPU INSTALLED.
4. TO REPLACE THE COMPARTMENT COVER, FIRST INSERT THE COVER OUTER EDGE (NEAR THE REAR OF THE NOTEBOOK) AT AN ANGLE, PUT DOWN THE COVER, AND THEN SLIDE IT TOWARD THE RIGHT. SECURE WITH ONE SCREW. (ref fig 7-15,7-16)

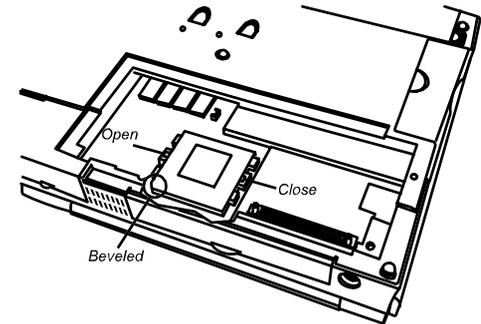


Figure 7-18. Removing the CPU

## 7.ASSEMBLY & DISASSEMBLY

### 7.2.5 MEMORY CARD

#### DISASSEMBLY

1. REMOVE THE BOTTOM COMPARTMENT COVER.( REF STEPS 1 TO 3 IN SECTION 7.2.4 DISASSEMBLY.)
2. TEMPORARILY REMOVE THE HEAT SINK BY UNPLUGGING THE FAN POWER CORD AND UNFASTENING FOUR SCREWS. (FIG 7-17)
3. REMOVE TWO SCREWS AND LIFT THE MEMORY CARD UP UNPLUG THE CONNECTOR.

#### RE- ASSEMBLY

1. REPLACE THE MEMORY CARD BY PLUGGING THE CONNECTOR AND SECURING WITH TWO SCREW. (ref fig 7-19)
- 2.TO REPLACE THE COMPARTMENT COVER, FIRST INSERT THE COVER OUTER EDGE(NEAR THE REAR OF THE NOTEBOOK) AT AN ANGLE, PUT DOWN THE COVER, AND THEN SLIDE IT TOWARD THE RIGHT. SECURE WITH ONE SCREW. (ref fig 7-15,7-16)

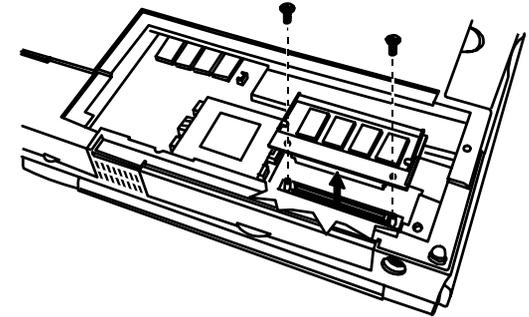


Figure 7-19. Removing the Memory Card Screws

## 7.ASSEMBLY & DISASSEMBLY

### 7.2.6 FAX/ MODEM/VOICE CARD

#### DISASSEMBLY

1. REMOVE THE BOTTOM COMPARTMENT COVER.  
(REF STEPS 1 TO 3 IN SEC 7.2.4 DISASSEMBLY.)
2. REMOVE ONE SCREW AND PULL UP ONE END OF THE CARD TO UNPLUG THE CONNECTOR FROM THE SYSTEM BOARD AND THEN LIFT IT FREE.

#### RE-ASSEMBLY

1. HOLD THE FAX/MODEM/VOICE CARD AT AN ANGLE SO THAT THE PHONE LINE CONNECTOR IS POINTED TOWARDS THE OPENING ON THE NOTEBOOK. INSERT THE PHONE LINE CONNECTOR INTO THE OPENING AND PRESS THE OTHER END TO PLUG THE OTHER CONNECTOR INTO THE SOCKET ON THE SYSTEM BOARD. FASTEN ONE SCREW TO SECURE THE CARD IN PLACE.( ref fig 7-20)
2. TO REPLACE THE COMPARTMENT COVER, FIRST INSERT THE COVER OUTER EDGE(NEAR THE REAR OF THE NOTEBOOK)AT AN ANGLE, PUT DOWN THE COVER, AND THEN SLIDE IT TOWARD THE RIGHT. SECURE WITH ONE SCREW. (ref fig 7-16,7-16)

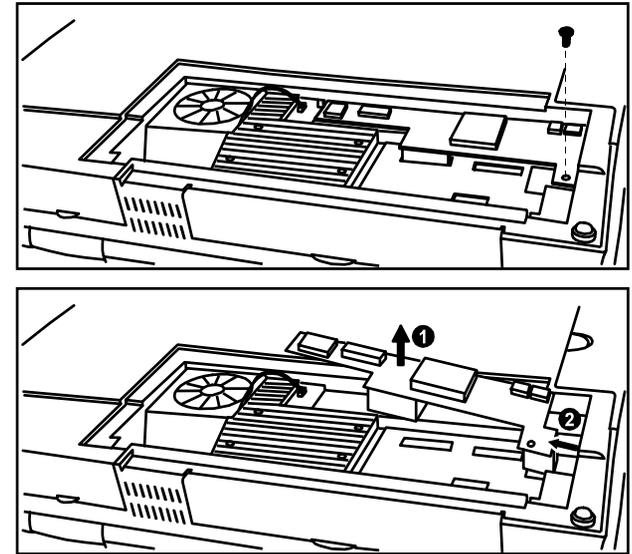


Figure 7-20. Removing the Fax/Modem/Voice Card

# 5027 N/B MAINTENANCE

## 7.ASSEMBLY & DISASSEMBLY

### 7.2.7 KEYBOARD

#### DISASSEMBLY

1. OPEN THE TOP COVER. REMOVE THE HINGE COVER BY INSERTING A FLAG SCREWDRIVER TO PRY THE COVER OUTWARDS.
2. REMOVE THE INDICATORS PANEL COVER BY SLIDING IT DOWNWARDS AND LIFTING THE UPPER EDGE.

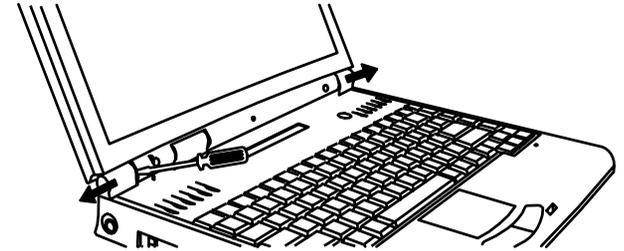


Figure 7-21. Removing the Hinge Covers

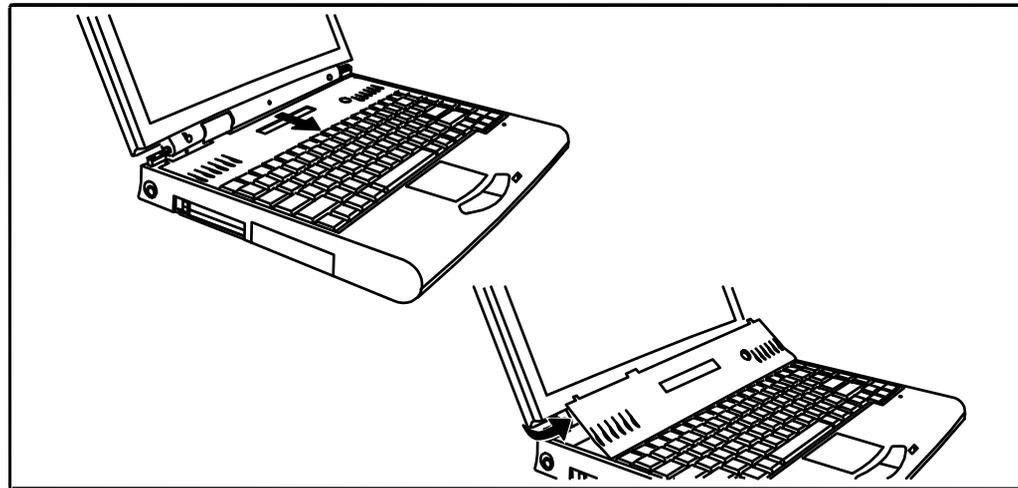
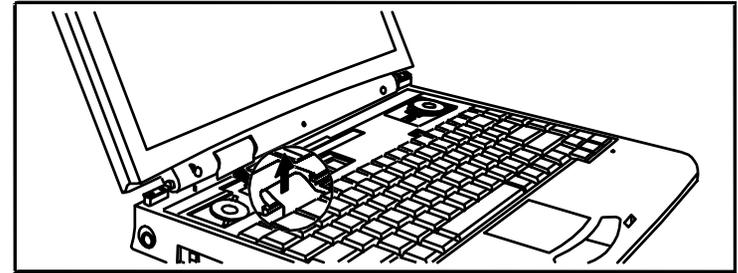


Figure 7-22. Removing the Indicator Panel

## 7.ASSEMBLY & DISASSEMBLY

### 7.2.7 KEYBOARD

3. UNPLUG THE KEYBOARD CABLE.
4. REMOVE THE KEYBOARD BY UNFASTENING TWO SCREWS AND LIFTING THE UPPER EDGE.



*Figure 7-23. Unplugging the Keyboard Cable*

### RE-ASSEMBLY

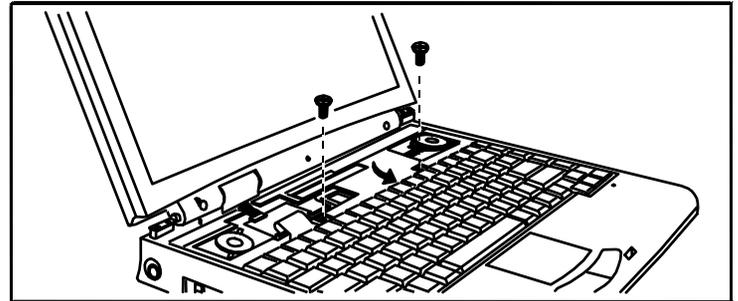
1. REPLACE THE KEYBOARD BY INSERTING THE LOWER EDGE FIRST AND THEN LAY DOWN THE UPPER EDGE. SECURE WITH TWO SCREWS.

(ref fig 7-24)

2. RECONNECT THE KEYBOARD CABLE.(ref fig 7-23)

3. REPLACE THE INDICATORS PANEL BY INSERTING THE LOWER EDGE FIRST AND THEN LAY DOWN THE UPPER EDGE. (ref fig 7-22)

4. REPLACE THE TWO HINGE COVERS. (ref fig 7-21)



*Figure 7-24. Removing the Keyboard*

## 7.ASSEMBLY & DISASSEMBLY

### 7.3 LCD ASSEMBLY COMPONENTS

#### 7.3.1 LCD

##### DISASSEMBLY

1. Open the top cover. Remove the four rubber pads and the four screws underneath. Now you can separate the LCD frame from the housing.

*NOTE :*The upper two screws are different from the lower two. Put the screws removed in different containers and label them.

2. To remove the LCD, remove four screws and unplug the connectors from the LCD.

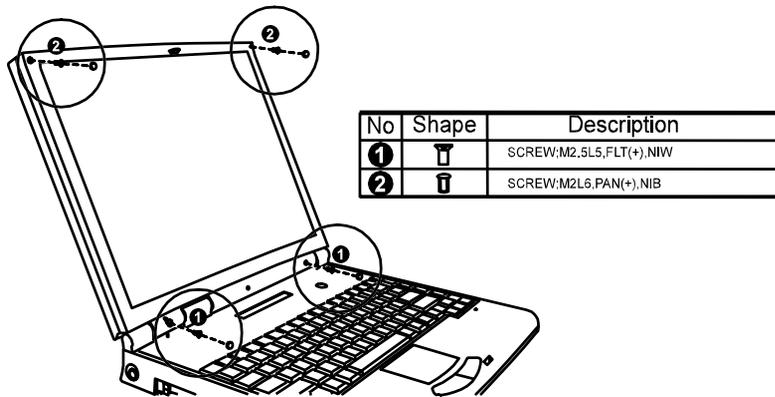


Figure 7-25. Removing the LCD Frame

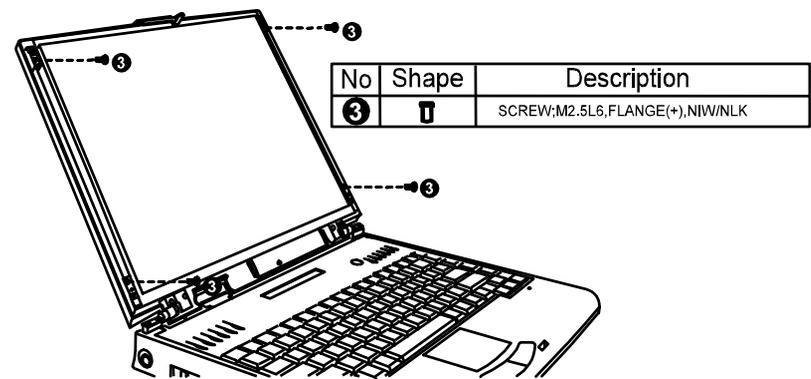


Figure 7-26. Removing the Flat Panel Screen

##### RE-ASSEMBLY

1. Reconnect the connectors and replace four screws. (ref fig 7-26)
2. Fit the LCD frame back to the housing and replace the four screws and rubber pads (ref fig 7-25.)

## 7.ASSEMBLY & DISASSEMBLY

### 7.3.2 INVERTER BOARD

#### DISASSEMBLY

1. Detach the LCD frame .(ref step 1 in section 7.3.1 Disassembly)
2. To remove the inverter board, remove one screw and unplug the connectors from both sides of the board.

#### RE-ASSEMBLY

1. Reconnect the two connectors. Fit the inverter board back into place and secure with one screw. (fig 7-27)
2. Fit the LCD frame back to the housing and replace the screws and rubber pads (ref fig 7-25)



*Figure 7-27. Removing the Inverter Board*

# 5027 N/B MAINTENANCE

## 7.ASSEMBLY & DISASSEMBLY

### 7.4 BASE UNIT COMPONENTS

#### 7.4.1 BOTTOM CHASSIS

##### DISASSEMBLY

1. Remove the right bay device .(ref section 7.2.1 Disassembly.)
2. Remove the hard disk drive module .(ref section 7.2.2 Disassembly.)
3. Remove the battery pack. (ref section 7.2.3 Disassembly.)
4. Remove the memory card .(ref section 7.2.5 Disassembly.)  
*NOTE:* Put the screws removed in different containers and label them.
5. Remove the Fax/Modem/Voice card .(ref section 7.2.6 Disassembly.)  
*NOTE:* Put the screws removed in a container and label them.
6. Open the secondary battery connector compartment.
7. Remove 13 screws (see the arrows in the figure 7-29) from the bottom chassis. Lift the rear end of the bottom chassis to detect it.  
*NOTE:* Put the different kinds of screws in different containers. It is important to use the correct screws when you re-assemble the bottom chassis.

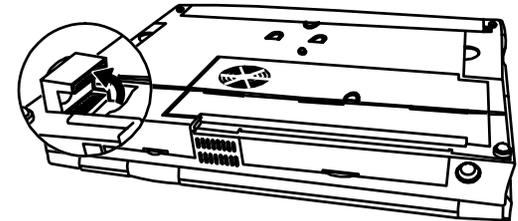
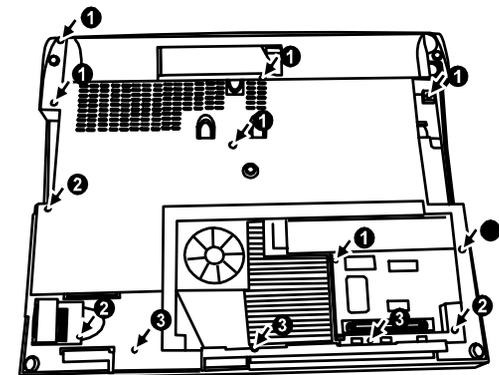


Figure 7-28. Opening the Battery Connector Compartment



No	Shape	Description
①		SCREW;M2L6,PAN(+),NIB
②		SPC-SCREW;M2L10,PAN(+),NIW,NLK
③		SPC-SCREW;M2L3,K-HEAD(+),NIB

Figure 7-29. Removing the Bottom Chassis

## **7.ASSEMBLY & DISASSEMBLY**

### 7.4.1 BOTTOM CHASSIS

#### **RE-ASSEMBLY**

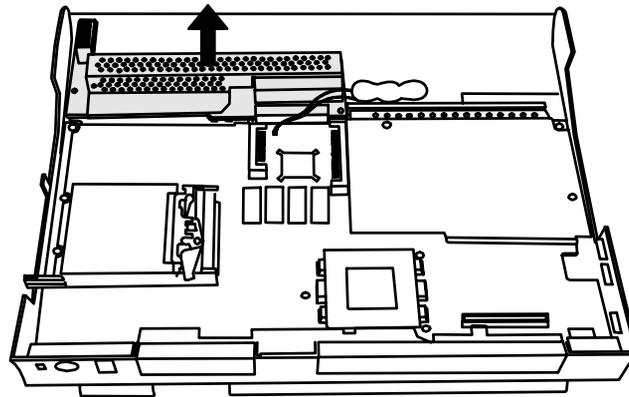
1. Replace the bottom cover by inserting the front end first and then lay down the rear end. Replace the 13 screws. Be careful to use the correct screws for the screw holes. (ref fig 7-29)
2. Close the secondary battery connector compartment. (ref fig 7-28)
3. Replace the Fax/Modem/Voice card .( ref section 7.2.6 Re-assembly.)
4. Replace the memory card .(ref section 7.2.5 Re-assembly.)
5. Replace the battery pack. (ref section 7.2.3 Re-assembly.)
6. Replace the hard disk drive module. (ref section 7.2.2 Re-assembly.)
7. Replace the right bay device. (ref section 7.2.1 Re-assemble.)

## 7.ASSEMBLY & DISASSEMBLY

### 7.4.2 D/D BOARD

#### DISASSEMBLY

1. Remove the bottom chassis. (ref section 7.4.1 Disassembly.)
2. Remove the D/D board by unplugging the connector.



*Figure 7-30. Removing the D/D Board*

#### RE-ASSEMBLY

1. Reconnect the D/D board connector to the system board.(ref fig 7-30)
2. Replace the bottom chassis. (ref section 7.4.1 Re-assembly.)

## 7.ASSEMBLY & DISASSEMBLY

### 7.4.3 SYSTEM BOARD

#### DISASSEMBLY

1. To disconnect all connectors from the top side of the system:

- a. Remove the keyboard.
- b. Disconnect the cables from J5 (for speaker), J3 (for microphone), J12 and J13 (for touch-pad).
- c. Disconnect the LCD cable by first unfastening three screws to remove the shield plate and then unfasten two screws.

*NOTE* : Put the screws removed in different containers and label them.

2. Remove the bottom chassis

3. Remove the D/D board

4. Remove the heat sink

*NOTE* : Put the screws removed in a container and label them.

5. Disconnect one connector from J518 on the system board.

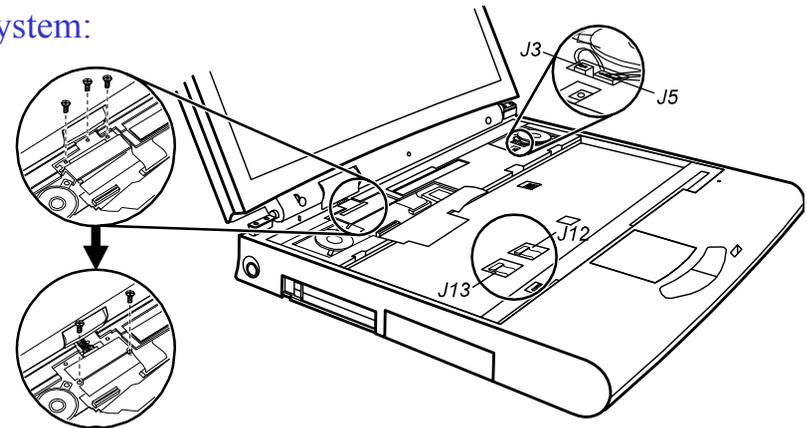


Figure 2-30. Disconnecting the Connectors from the System Board

## 7.ASSEMBLY & DISASSEMBLY

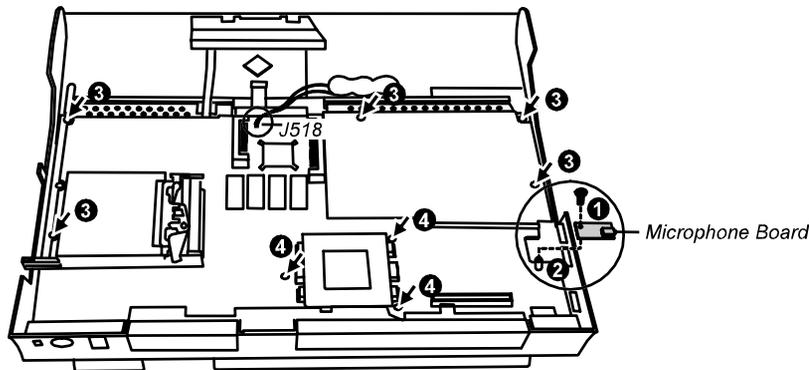
### 7.4.3 SYSTEM BOARD

6. Remove the small microphone board by unfastening one screw (fig 7-32- ❶). Then , remove the stand-off (fig 7-32- ❷) where the screw was removed from .

*NOTE* : Put the screws removed in a container and label them.

7. Remove the remaining eight screws (fig 7-32- ❸ and ❹) that secure the system board to the base unit.

*NOTE* : Put the different kinds of screws in different containers. It is important to use the correct screws when you re-assemble the bottom chassis.



No	Shape	Description
❶		SPC-SCREW;M2L3,K-HEAD(+),NIB
❷		STAND-OFF;M2DP4H11.3L8.5,NIW;FAX/MODEM
❸		SPC-SCREW;M2L5,NIB,K-HD,727
❹		SPC-SCREW,M2L4,NIW,FLT(+),NL,731

Figure 2-31. Removing the System Board Screws

8. Lift the system board free

## 7.ASSEMBLY & DISASSEMBLY

### 7.4.3 SYSTEM BOARD

#### RE-ASSEMBLY

1. Fit the system board into place and replace the eight screws to the system board. Be careful to use the correct screws for the screw holes. (ref fig 7-32).
2. Replace the stand-off and secure the microphone board with one screw. (ref fig 7-32).
3. Reconnect the connector to J518 on the system board (ref fig 7-32).
4. Replace the heat sink .(ref steps 2 in section 7.2.4 re-assembly).
5. Replace the D/D board .(ref section 7.4.2 re-assembly).
6. Replace the bottom chassis. (ref section 7.4.1 re-assembly).
7. Reconnect the connectors to J3,J5,J12 and J15 (ref fig 7-31).
8. Reconnect the LCD cable by tightening two screws. Then replace the shield plate by tightening three screws. (ref fig 7-31).

## 7.ASSEMBLY & DISASSEMBLY

### 7.4.4 TOUCH-PAD

#### DISASSEMBLY

1. Remove the bottom chassis. (ref section 7.4.1 Disassembly).
2. Remove the D/D board
3. Detach the touch-pad button board by removing two screws and put it aside.
4. Remove the button part.
5. Remove the screw of the grounding wire and unplug the touch-pad cable. Then, lift the touch-pad board free.

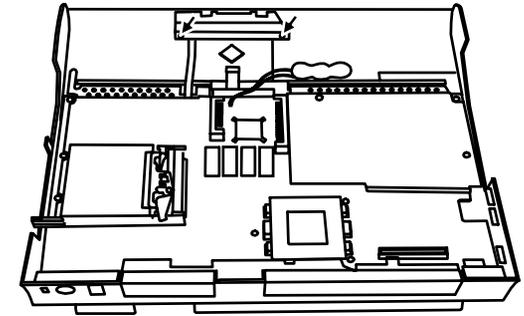


Figure 7-33. Removing Two Screws from the Touch-pad Button Board

#### RE-ASSEMBLY

1. Fit the touch-pad cable back into place. Reconnect the grounding wire by tightening one screw and reconnect the cable .
2. Fit the button part back into place.
3. Fit the touch-pad button board back into place and secure with two screws.
4. Replace the D/D board.
5. Replace the bottom chassis.

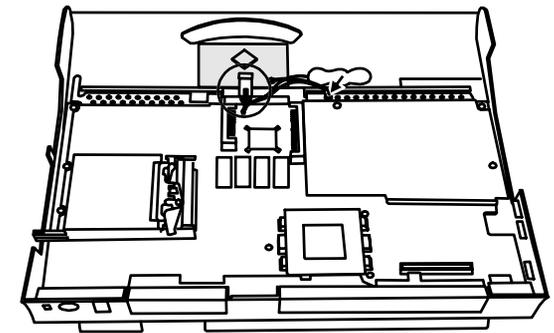
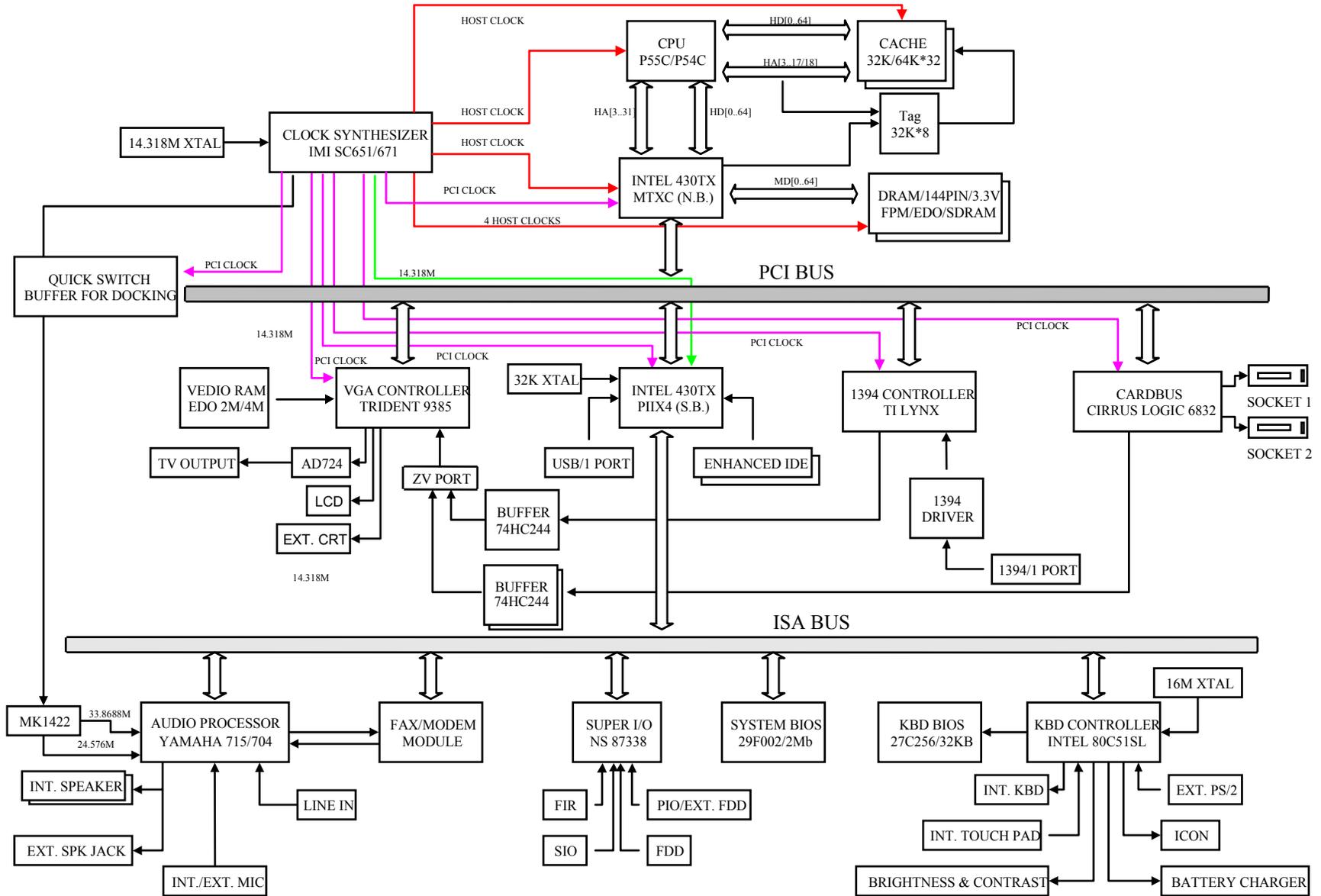


Figure 7-34. Removing the Touch-pad Board

# 5027 N/B MAINTENANCE

## 8. 5027 SYSTEM BLOCK DIAGRAM



# 5027 N/B MAINTENANCE

## 8. MAINTENANCE DIAGNOSTICS

### 8.1 INTRODUCTION

EACH TIME THE COMPUTER IS TURNED ON ,THE SYSTEM BIOS RUNS A SERIES OF INTERNAL CHECKS ON THE HARDWARE. THIS POWER-ON SELF TEST (POST) ALLOWS THE COMPUTER TO DETECT PROBLEMS AS EARLY AS THE POWER-ON STAGE. ERROR MESSAGES OF POST CAN ALERT YOU TO THE PROBLEMS OF YOUR COMPUTER.

IF AN ERROR IS DETECTED DURING THESE TESTS, YOU WILL SEE AN ERROR MESSAGE DISPLAYED ON THE SCREEN. IF THE ERROR OCCURS BEFORE THE DISPLAY IS INITIALIZED , THEN THE SCREEN CANNOT DISPLAY THE ERROR MESSAGE. ERROR CODES OR SYSTEM BEEPS ARE USED TO IDENTIFY A POST ERROR THAT OCCURS WHEN THE SCREEN IS NOT AVAILABLE.

THE VALUE FOR THE DIAGNOSTIC POST(378H) IS WRITTEN AT THE BEGINNING OF THE TEST. THEREFORE , IF THE TEST FAILED, THE USER CAN DETERMINE WHERE THE PROBLEM OCCURRED BY READING THE LAST VALUE WRITTEN TO POST 378H BY THE PIO DEBUG BOARD PLUG AT PIO PORT.

# 5027 N/B MAINTENANCE

## 8. MAINTENANCE DIAGNOSTICS

8.2 ERROR CODES : FOLLOWING IS A LIST OF ERROR CODES IN SEQUENCE DISPLAY ON THE PIO DEBUG BOARD.

Code	Description
00H	Start of BootLoader sequence.
01H	Disable A20 through A20, not send.
02H	Initialize ChipSet.
03H	Perform conventional RAM(1st 640K) test with crossed-pattern R/W.
04H	Move BootLoader to the RAM.
05H	Start point of execution of BootLoader in RAM.
06H	Perform PnP initialization for Crystal audio chip.
06H	Check OVERRIDE option, not send.
07H	Shadow System BIOS.
08H	Checksum System BIOS ROM, not send.
09H	Proceed with Normal Boot
0AH	Proceed with Crisis Boot
0FH	DRAM Sizing
10H	Initial L1,L2 cache, make stack and diagnose CMOS.
11H	Turn off FASTA20 for POST. Reset GDTs, 8259s quickly.
12H	Signal Power On Reset at COMS.
13H	Initialize the Chipset, (SDRAM).
14H	Search For ISA Bus VGA Adapter
15H	Reset Counter/Timer 1, exite the RAM.
16H	User register config through CMOS
18H	Dispatch to 1st 64K RAM Test
19H	Checksum the ROM
1AH	Reset PIC's(8259s)
1BH	Initialize Video Adapter(s)
1CH	Initialize Video (6845 Regs)
1DH	Initialize Color Adapter
1EH	Initialize Monochrome Adapter
1FH	Test 8237A Page Registers
20H	Perform Keyboard self test
21H	Test & Initialize Keyboard Controller

(To be continued)

(Continued)

Code	Description
22H	Check If CMOS Ram Valid
23H	Test Battery Fail & CMOS X-SUM
24H	Test the DMA controllers
25H	Initialize 8237A Controller
26H	Initialize Interrupt Vectors Table.
27H	RAM Quick Sizing
28H	Protected mode entered safely
29H	RAM test completed
2AH	Protected mode exit successful
2BH	Setup Shadow
2CH	Prepare To Initialize Video
2DH	Search For Monochrome Adapter
2EH	Search For Color Adapter, VGA Initialize.
2FH	Signon messages displayed
30H	Special init of keyboard ctrl
31H	Test If Keyboard Present
32H	Test Keyboard Interrupt
33H	Test Keyboard Command Byte
34H	TEST, Blank and count all RAM
35H	Protected mode entered safely (2).
36H	RAM test complete
37H	Protected mode exit successful
38H	Update Keyboard output port to disable gate of A20
39H	Setup Cache Controller
3AH	Test If 18.2Hz Periodic Working
3BH	Initialize BIOS Data Area at 40:0.
3CH	Initialize the hardware interrupt vector table
3DH	Search and Init the Mouse
3EH	Update NumLock status
3FH	OEM initialization of COMM and LPT ports

(To be continued)

# 5027 N/B MAINTENANCE

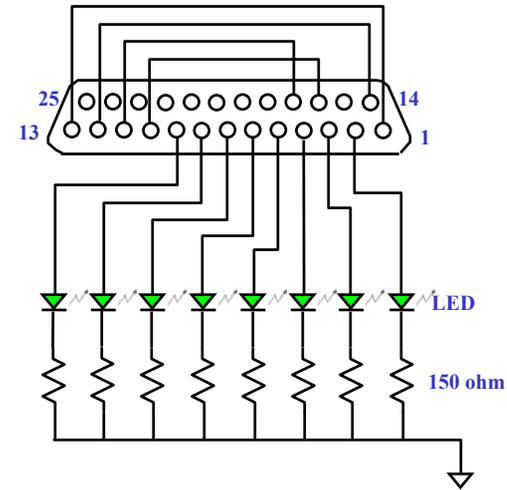
## 8. MAINTENANCE DIAGNOSTICS

(Continued)

Code	Description
40H	Configure the COMM and LPT ports
41H	Initialize the floppies
42H	Initialize the hard disk
43H	Initialize additional ROMs
44H	OEM's init of Power Management, (check SMI)
45H	Update NUMLOCK status
46H	Test For Coprocessor Installed
47H	OEM functions before boot (PCMCIA, CardBus)
48H	Dispatch To Operation System Boot
49H	Jump Into Bootstrap Code
4AH	OEM's init of PM with USB

Code	Beeps	Description
0F0h	....	No RAM
0F1h	..._	RAM test failed
002h	.._.	BIOS is not shadowed
004h	._..	BIOS Checksum BAD
00Ah	._.	No CR code/CR bad

### PIO PORT (378H) DIAGNOSTIC TOOLS



PIN1 : STROBE ↔ PIN13: SLCT  
 PIN10: ACK# ↔ PIN16: INT#  
 PIN11: BUSY ↔ PIN17: SELIN#  
 PIN12:PTERR ↔ PIN14: AUTOFD#  
 PIN[9:2]:PD[7:0]

# 5027 N/B MAINTENANCE

## 9. TROUBLE SHOOTING

9.1 NO POWER

9.2 NO DISPLAY

9.3 VGA CONTROLLER FAILURE

9.4 LCD NO DISPLAY

9.5 EXTERNAL MONITOR  
NO DISPLAY

9.6 MEMORY TEST ERROR

9.7 KEYBOARD TEST ERROR

9.8 TRACK PAD/BALL TEST ERROR

9.9 DISKETTE DRIVE TEST ERROR

9.10 CD-ROM DRIVE TEST ERROR

9.11 HARD DRIVE TEST ERROR

9.12 USB PORT TEST ERROR

9.13 SIO PORT TEST ERROR

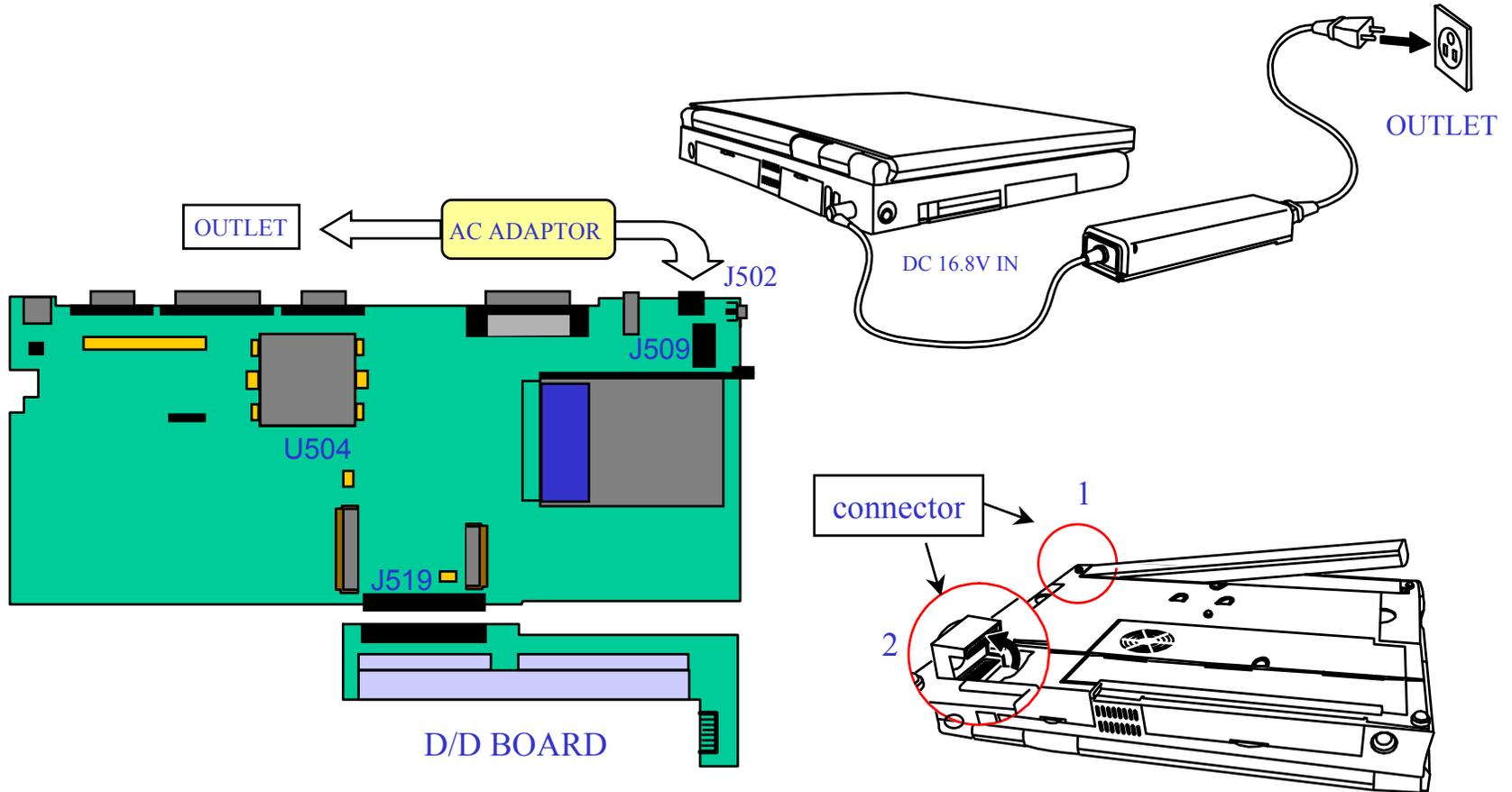
9.14 PIO PORT TEST ERROR

9.15 AUDIO FAILURE

# 5027 N/B MAINTENANCE

## 9.1 NO POWER:

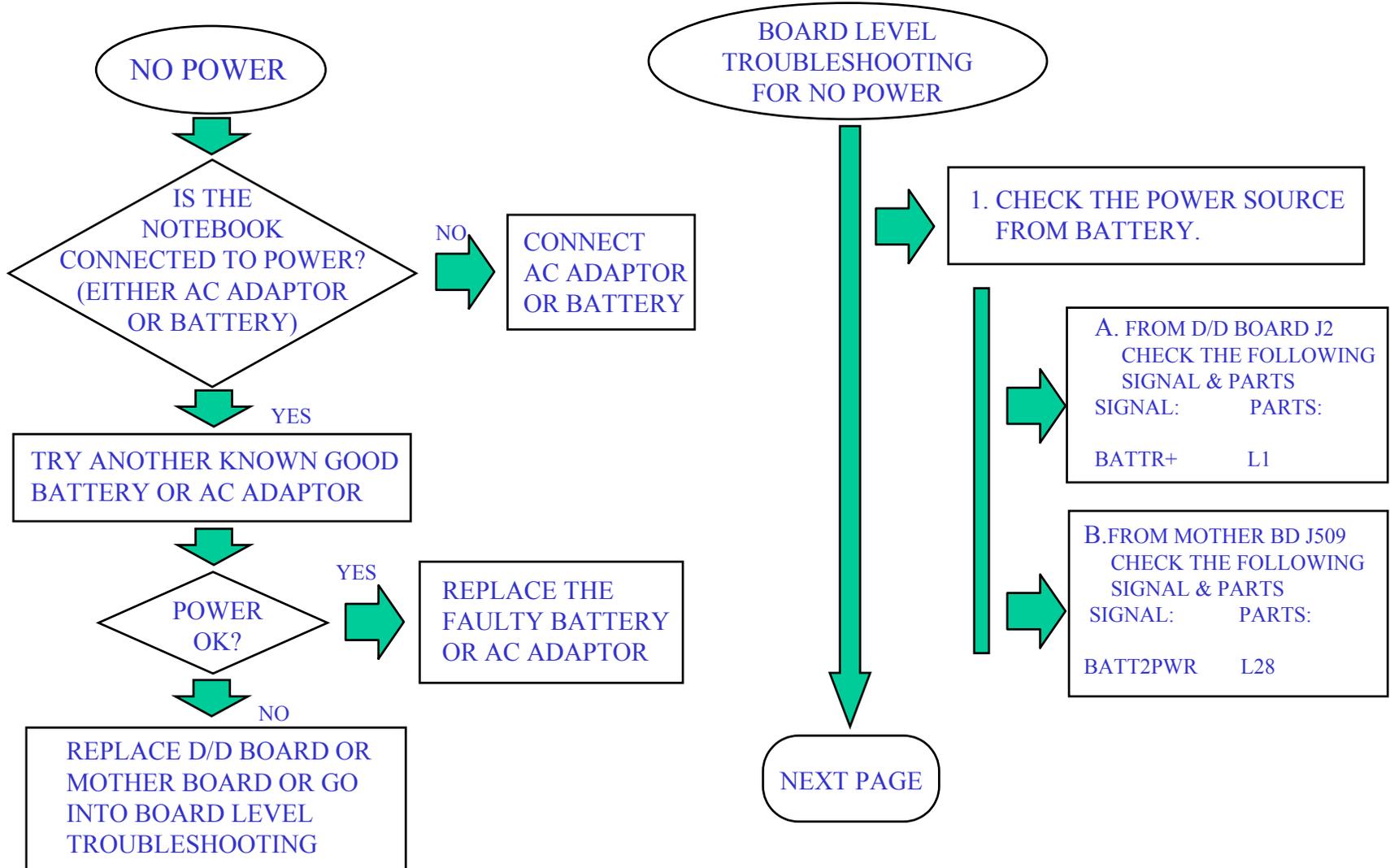
WHEN THE POWER BUTTON IS PRESSED, NOTHING HAPPENS ,POWER INDICATOR IS NOT LIGHT UP.



# 5027 N/B MAINTENANCE

## 9.1 NO POWER:

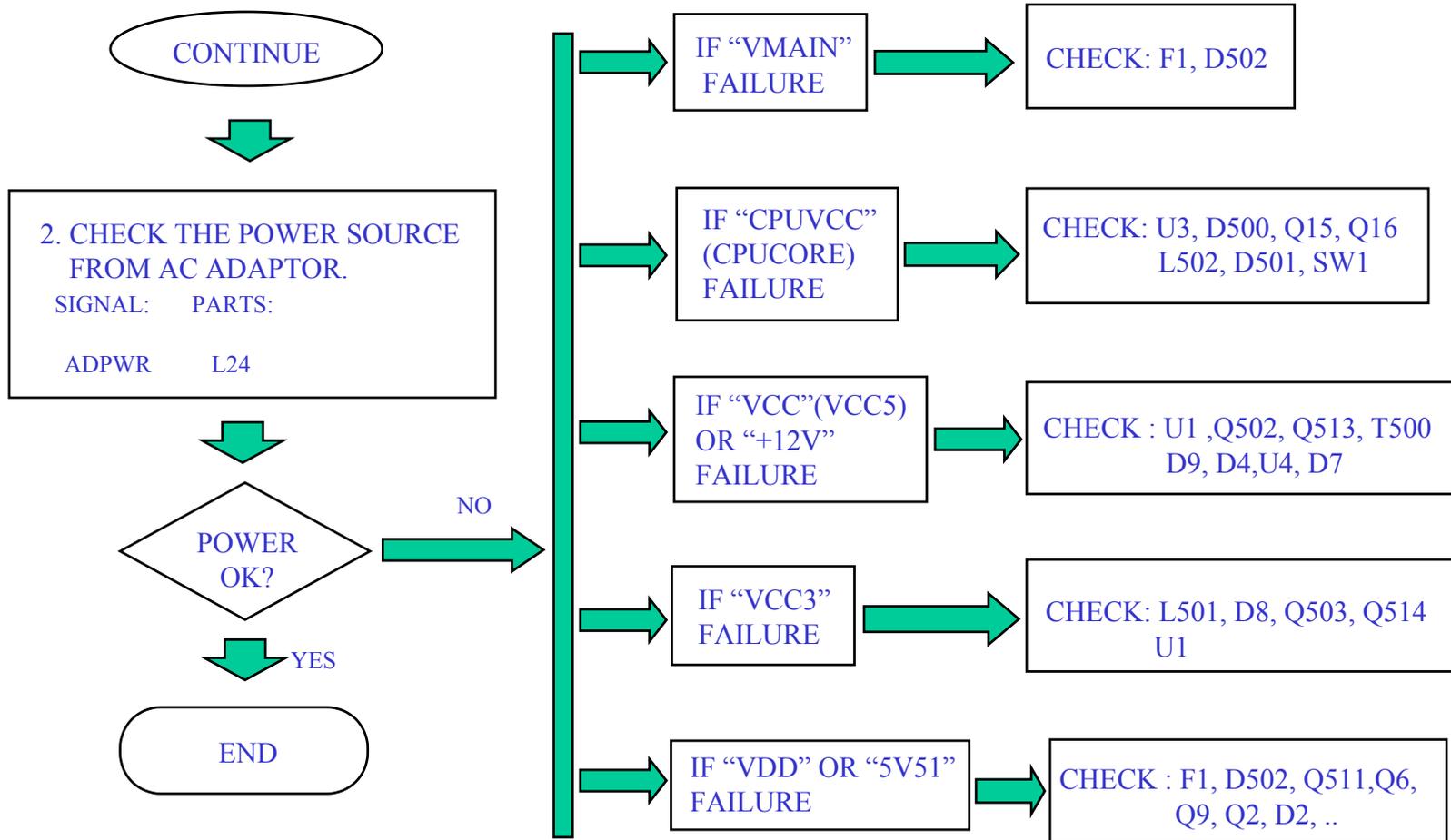
WHEN THE POWER BUTTON IS PRESSED, NOTHING HAPPENS ,POWER INDICATOR IS NOT LIGHT UP.



# 5027 N/B MAINTENANCE

## 9.1 NO POWER:

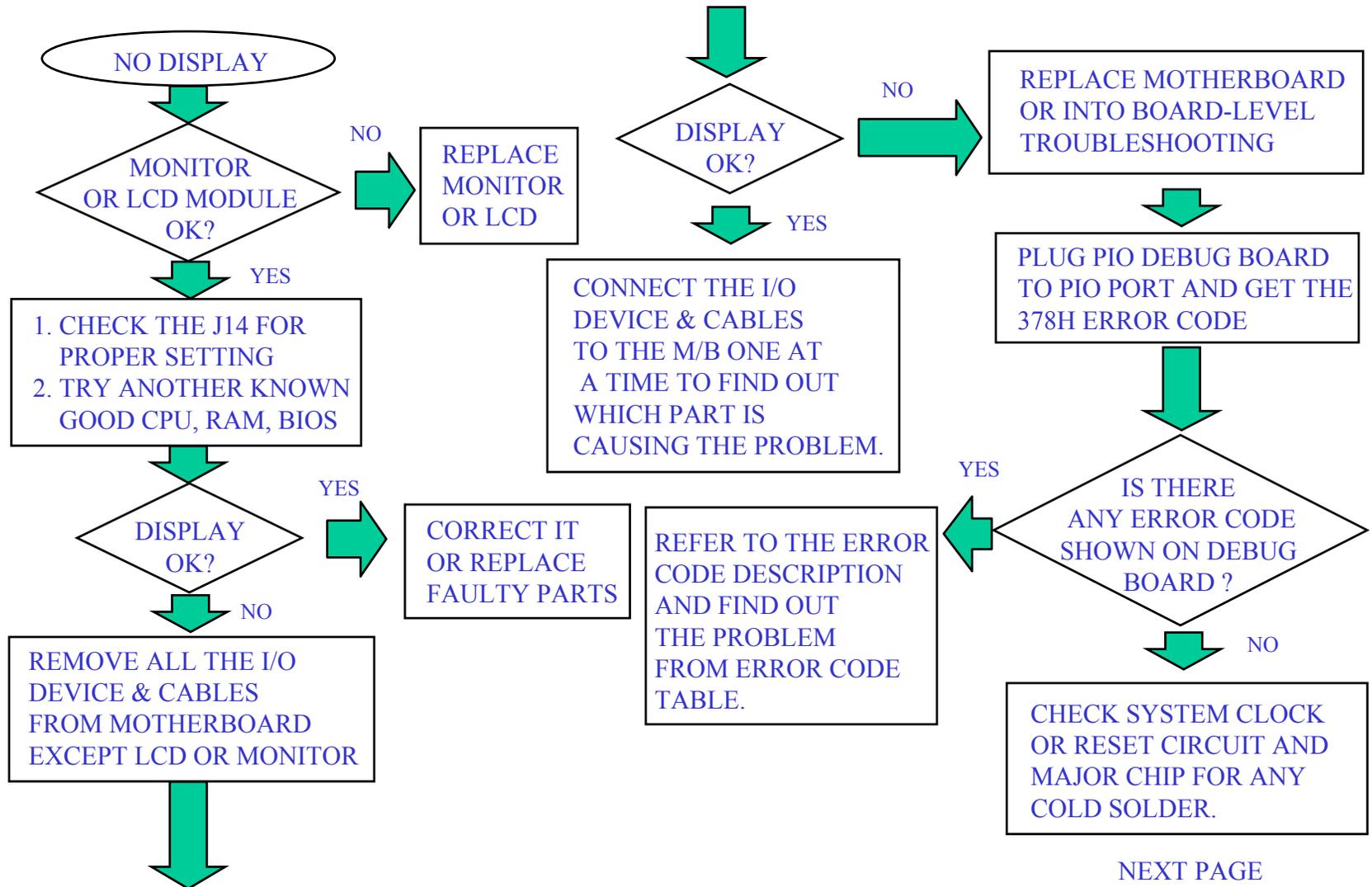
WHEN THE POWER BUTTON IS PRESSED, NOTHING HAPPENS ,POWER INDICATOR IS NOT LIGHT UP.



# 5027 N/B MAINTENANCE

## 9.2 NO DISPLAY

THERE IS NO DISPLAY ON BOTH LCD AND MONITOR

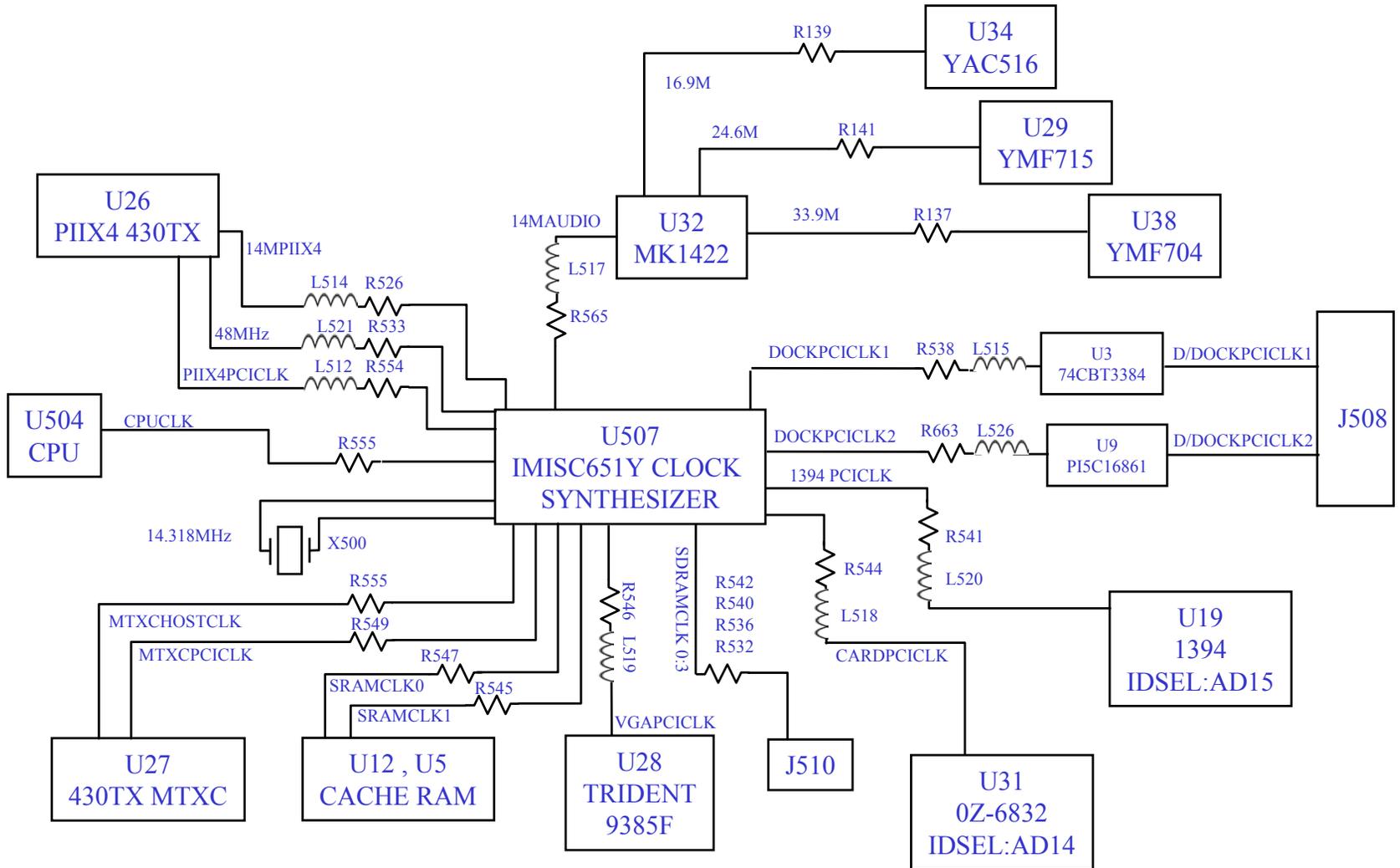


NEXT PAGE

# 5027 N/B MAINTENANCE

## 9.2 NO DISPLAY

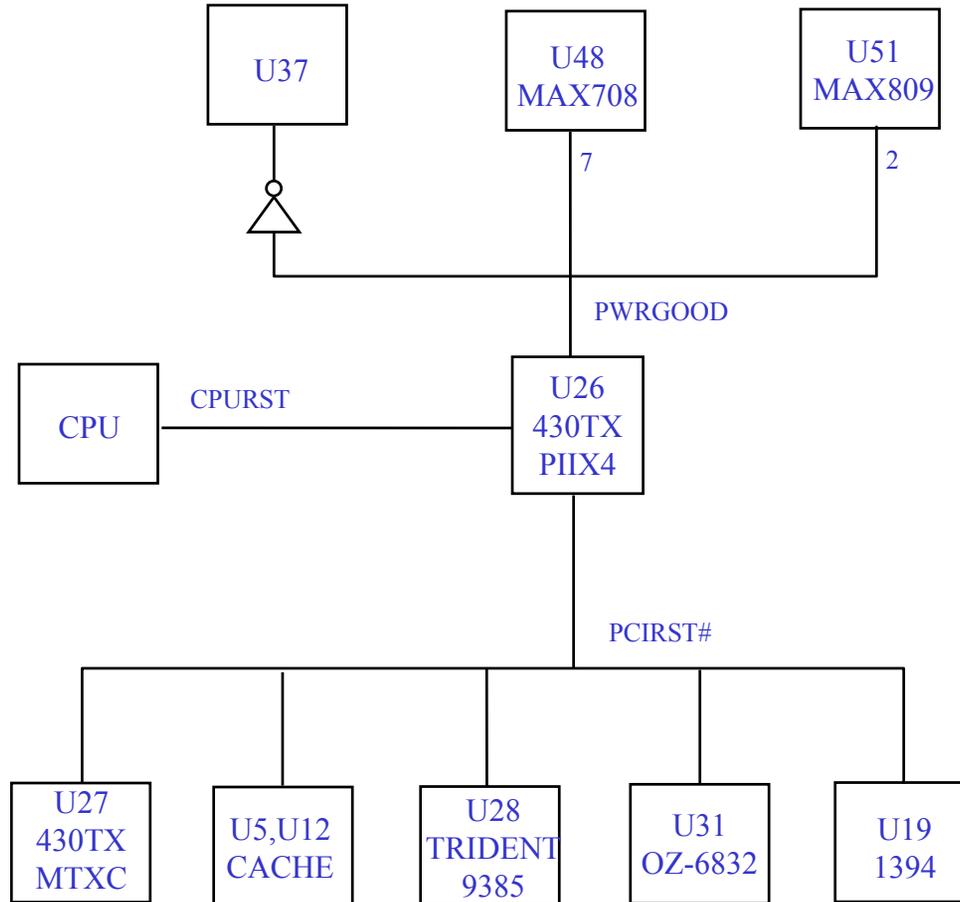
\*\*\*\*\*SYSTEM CLOCK CHECK\*\*\*\*\*



# 5027 N/B MAINTENANCE

## 9.2 NO DISPLAY

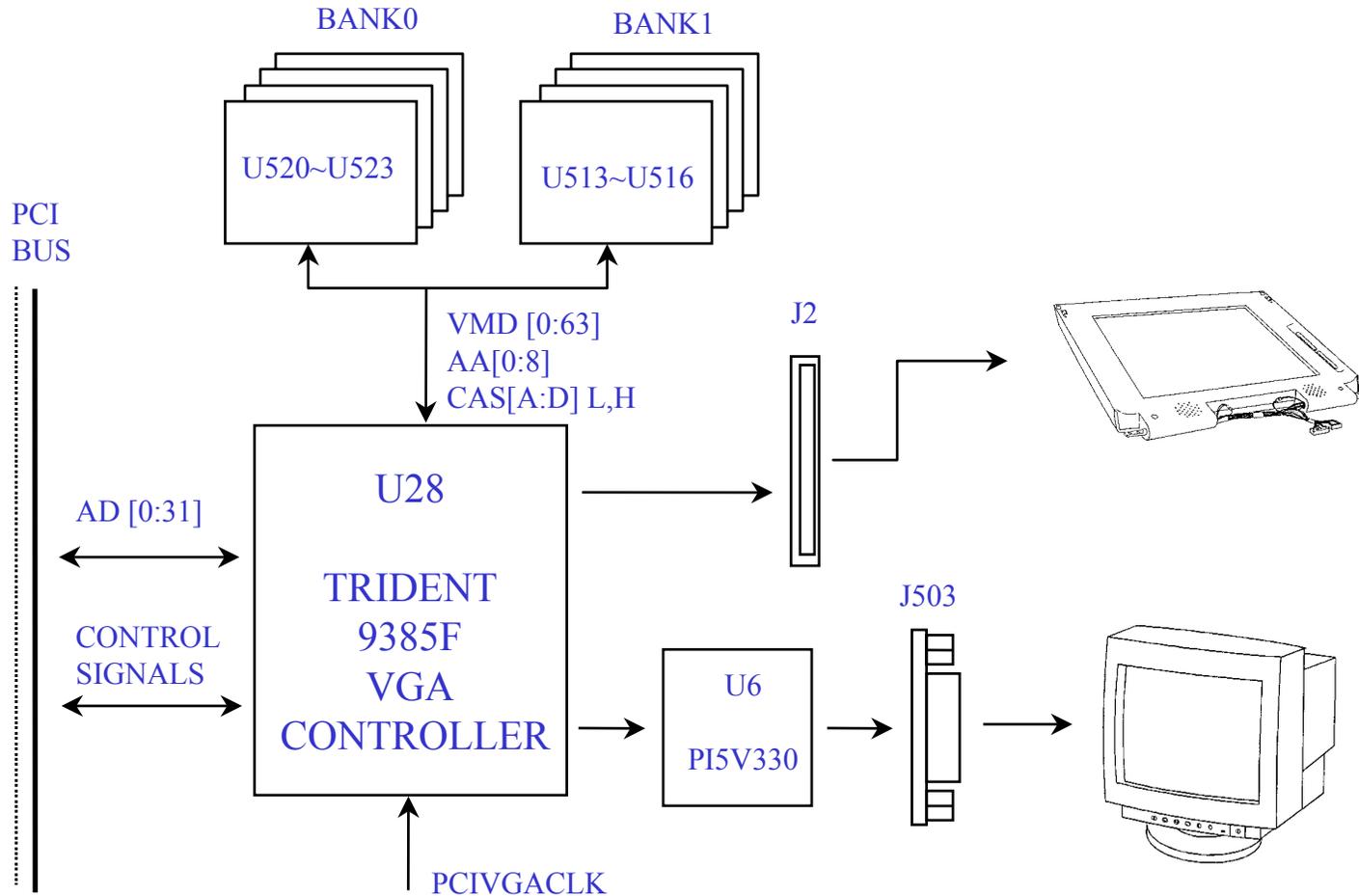
\*\*\*\*\*SYSTEM RESET SIGNAL CHECK \*\*\*\*\*



# 5027 N/B MAINTENANCE

## 9.3 VGA CONTROLLER FAILURE

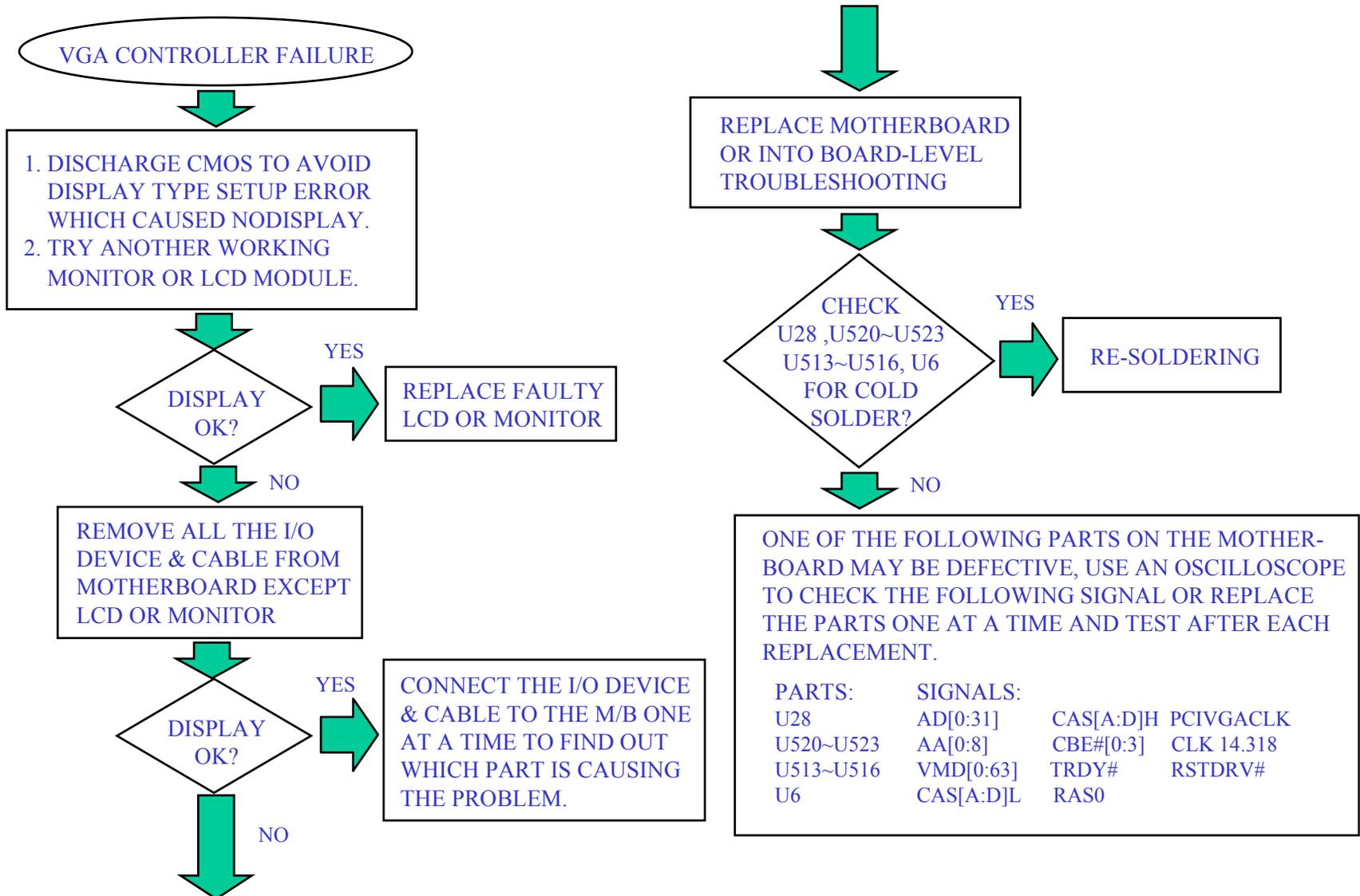
THERE IS NO DISPLAY ON BOTH LCD AND MONITOR ALYHOUGH POWER-ON-SELF-TEST IS PASSED.



# 5027 N/B MAINTENANCE

## 9.3 VGA CONTROLLER FAILURE

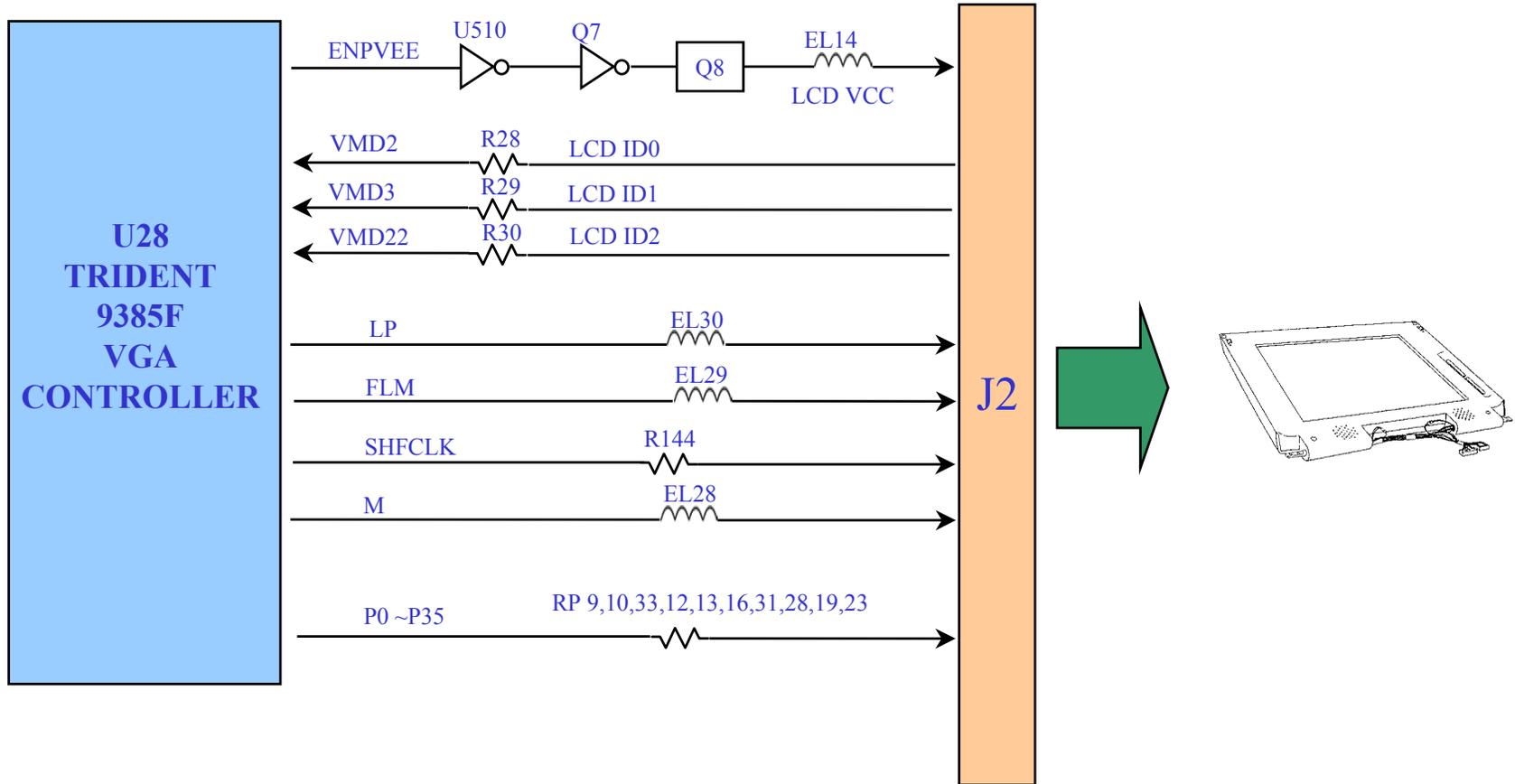
THERE IS NO DISPLAY ON BOTH LCD AND MONITOR ALTHOUGH POWER-ON-SELF-TEST IS PASSED.



# 5027 N/B MAINTENANCE

## 9.4 LCD NO DISPLAY

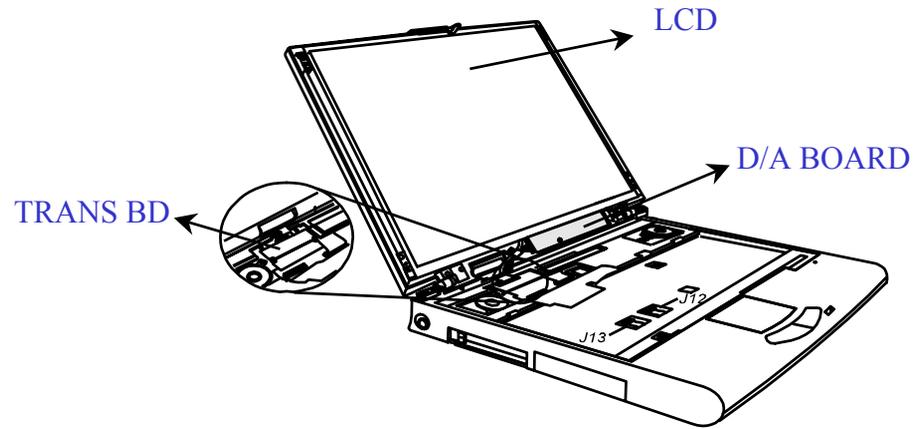
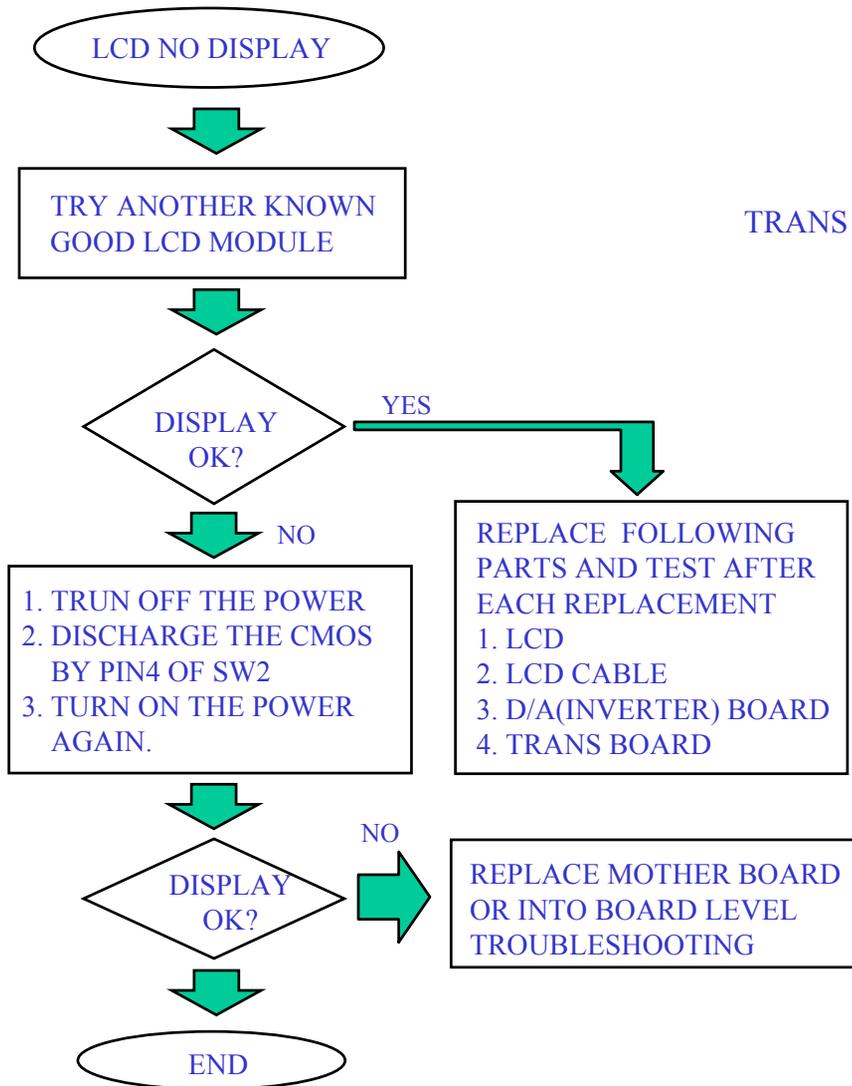
THE LCD SHOWS NOTHING OR ABNORMAL PICTURE , BUT IT IS OK FOR EXTERNAL MONITOR.



# 5027 N/B MAINTENANCE

## 9.4 LCD NO DISPLAY

THE LCD SHOWS NOTHING OR ABNORMAL PICTURE , BUT IT IS OK FOR EXTERNAL MONITOR.



BOARD-LEVEL TROUBLESHOOTING

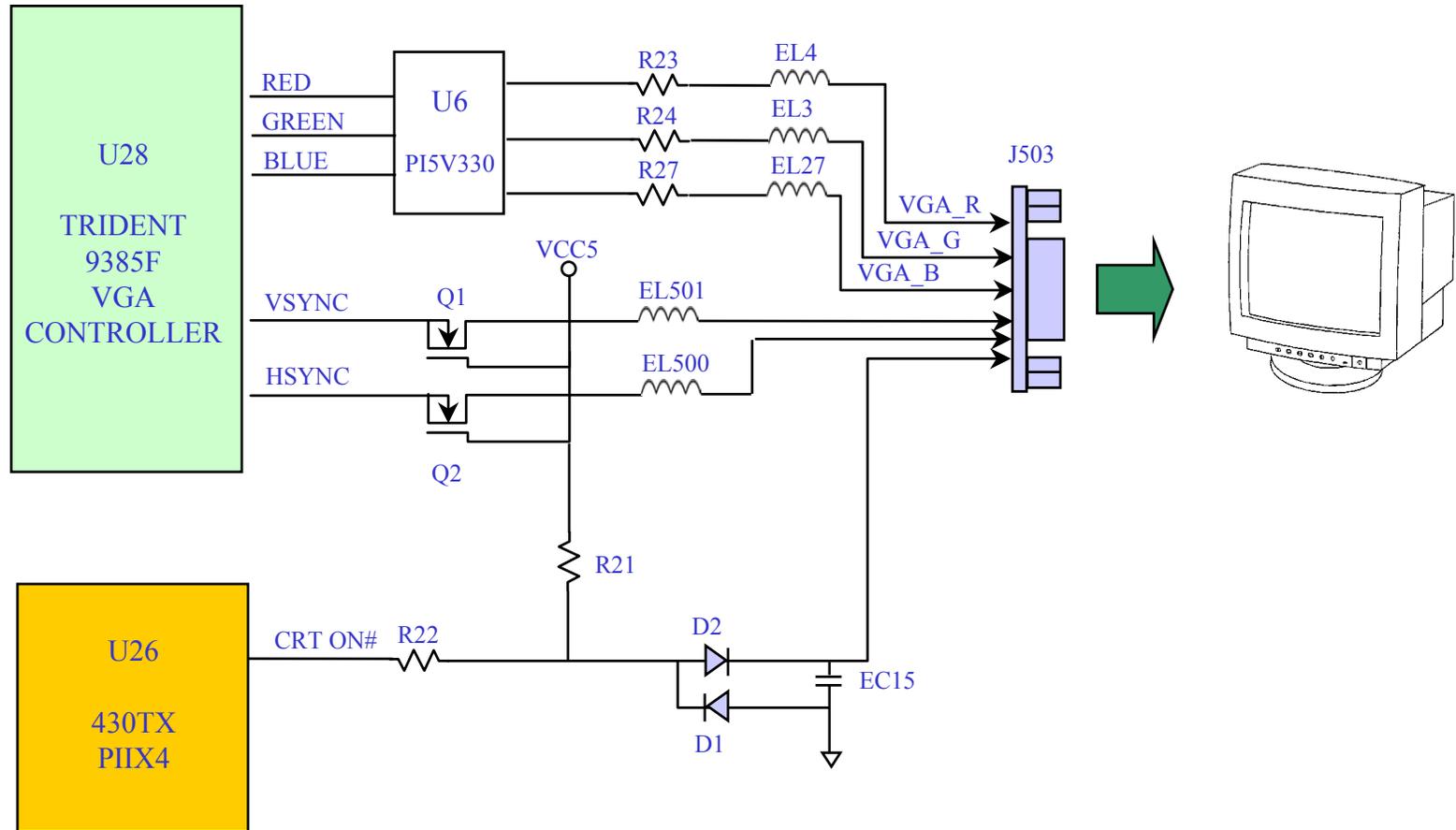
ONE OF THE FOLLOWING PARTS ON THE MOTHER-BOARD MAY BE DEFECTIVE, USE AN OSCILLOSCOPE TO CHECK THE FOLLOWING SIGNAL OR REPLACE THE PARTS ONE AT A TIME AND TEST AFTER EACH REPLACEMENT.

PARTS:		SIGNALS:	
U28,U510	RP 9,10,12,13	ENPEVV	M
Q7,Q8,EL14	16,19, 23,28	VMD 2,3,22	P0~P35
R28,R29,R30	31,33	LP	
EL28,29,30		FLM	
R144		SHFCLK	

# 5027 N/B MAINTENANCE

## 9.5 EXTERNAL MONITOR NO DISPLAY

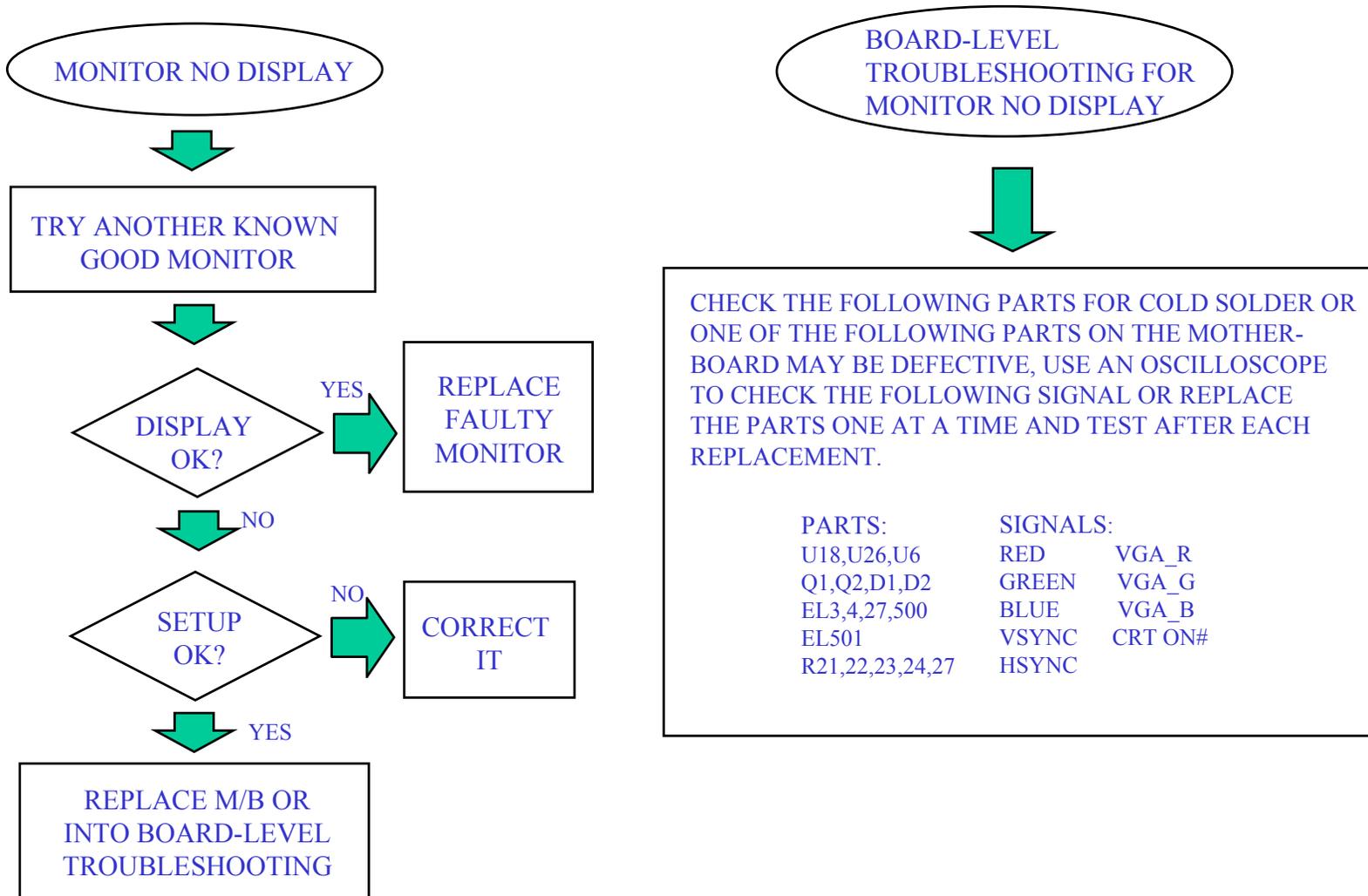
THE CRT MONITOR SHOWS NOTHING OR ABNORMAL COLOR, BUT IT IS OK FOR LCD.



# 5027 N/B MAINTENANCE

## 9.5 EXTERNAL MONITOR NO DISPLAY

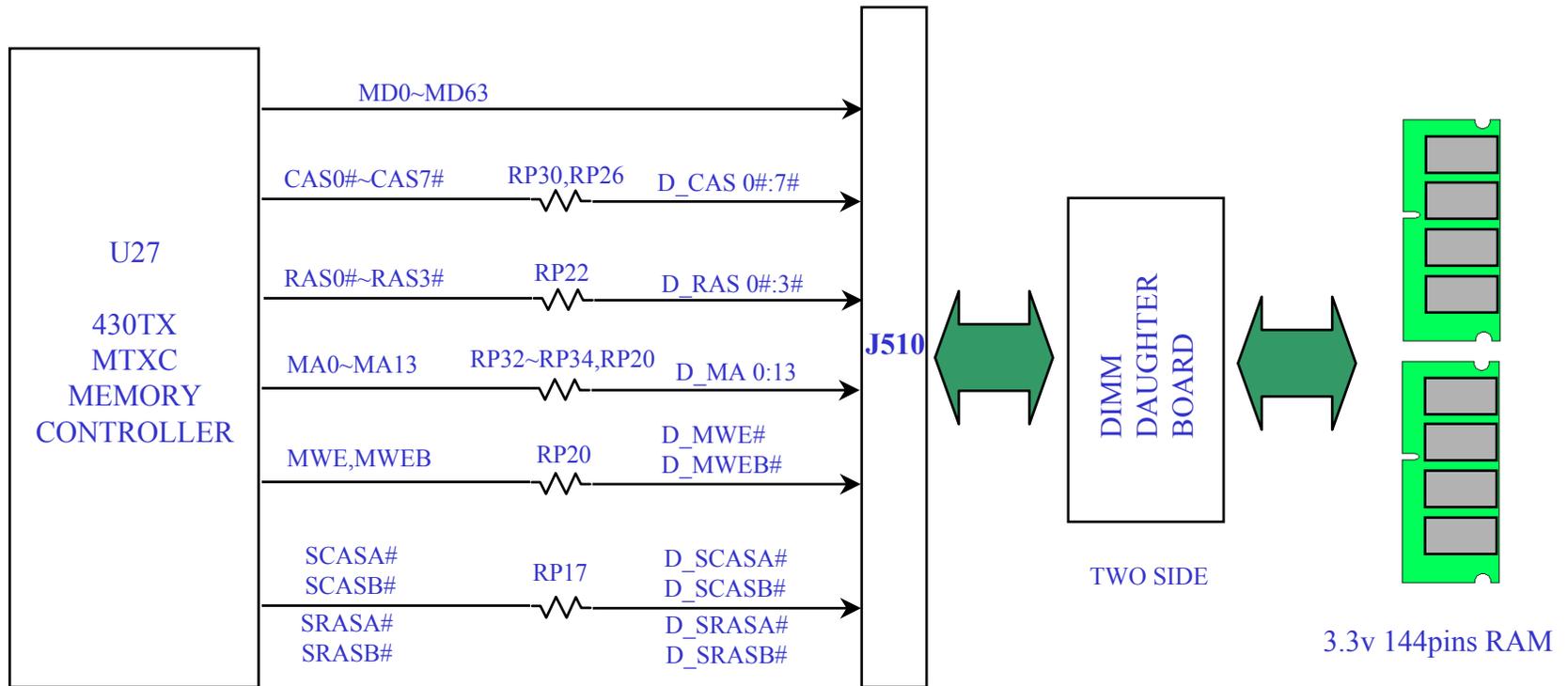
THE CRT MONITOR SHOWS NOTHING OR ABNORMAL COLOR, BUT IT IS OK FOR LCD.



# 5027 N/B MAINTENANCE

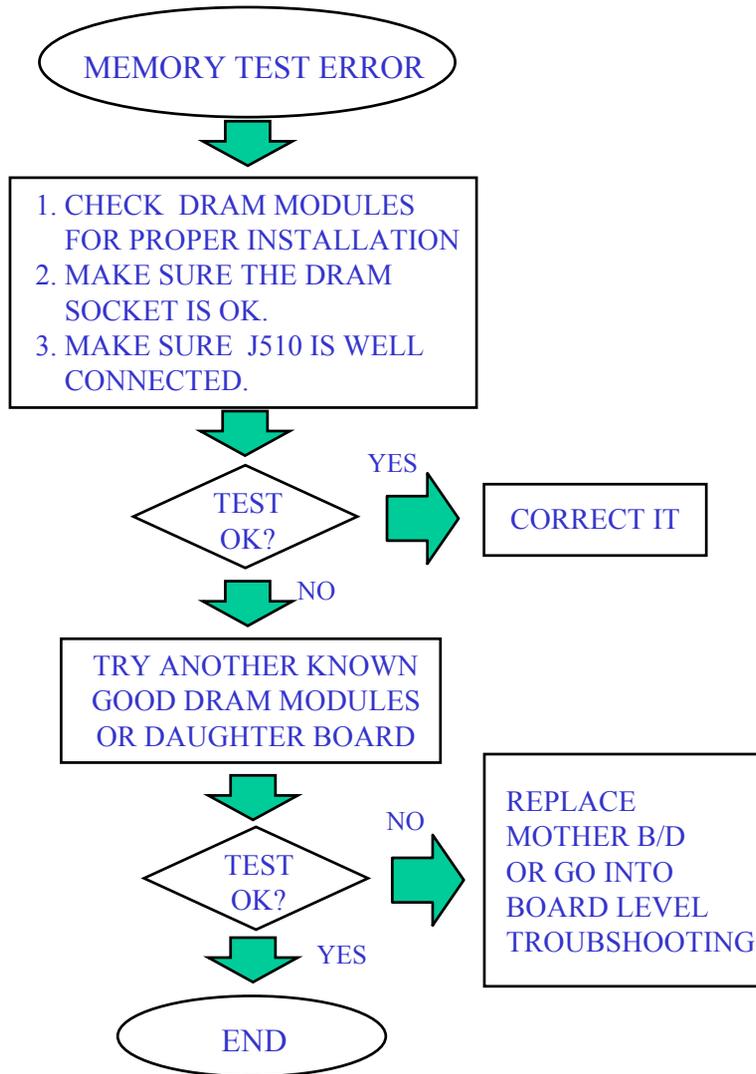
## 9.6 MEMORY TEST ERROR

THE ERROR CODE SHOWN ON THE PIO DEBUG BOARD IS 0FH, 13H,18H OR 27H AND SYSTEM HANGS UP.



# 5027 N/B MAINTENANCE

## 9.6 MEMORY TEST ERROR



### BOARD-LEVEL TROUBLESHOOTING FOR MEMORY TEST ERROR

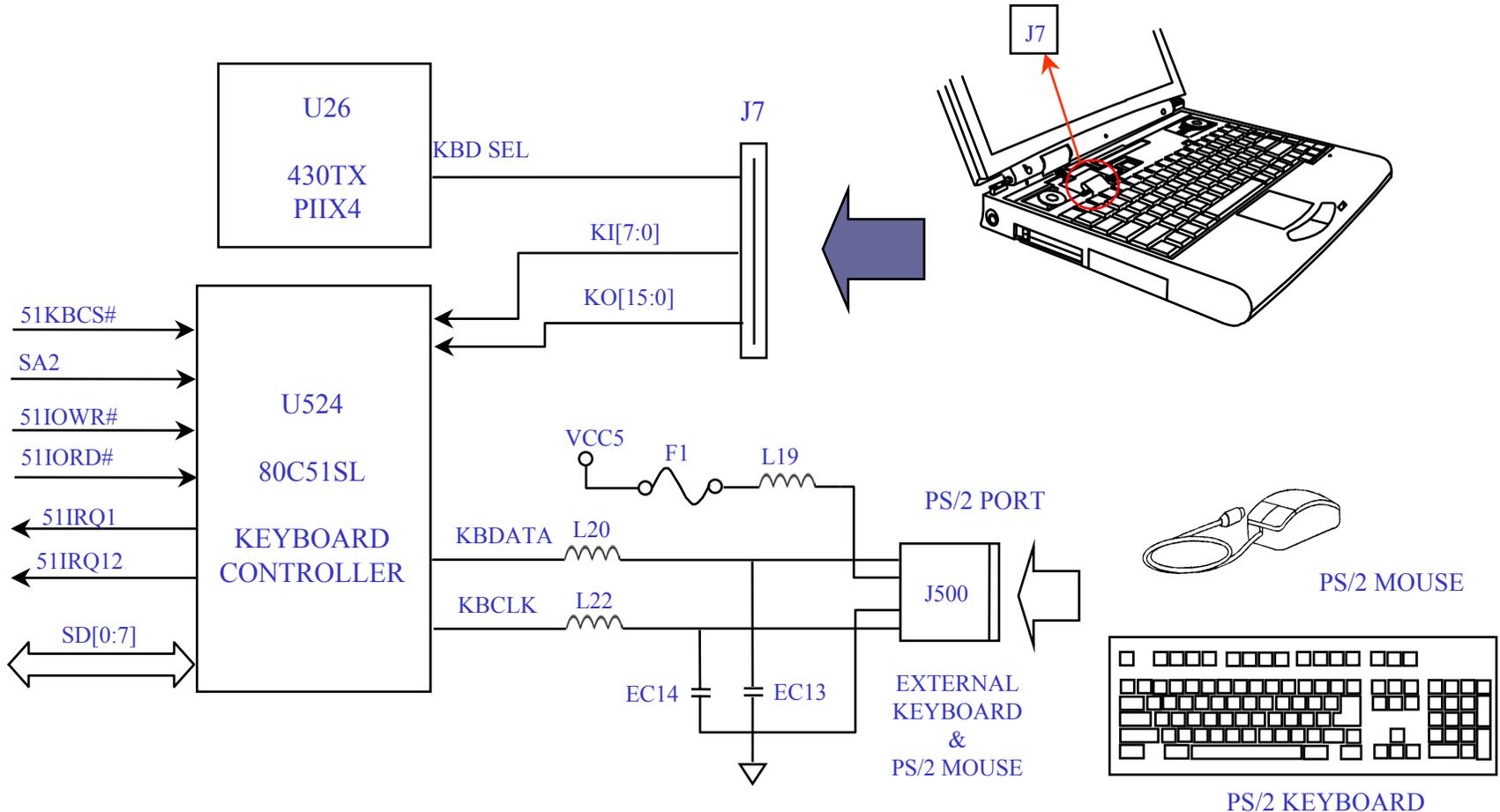
CHECK THE FOLLOWING PARTS FOR COLD SOLDER OR ONE OF THE FOLLOWING PARTS ON THE MOTHERBOARD MAY BE DEFECTIVE, USE AN OSCILLOSCOPE TO CHECK THE FOLLOWING SIGNAL OR REPLACE THE PARTS ONE AT A TIME AND TEST AFTER EACH REPLACEMENT.

PARTS:	SIGNALS:	
U27	MD[0:63]	SCASA#
RP26,30,22,32,	CAS[0:7]#	SCASB#
33,34,20,17	RAS[0:3]#	SRASA#
J510	MA[0:13]	SRASB#
DAUGHTER-BOARD	MWE	
	MWEB	

# 5027 N/B MAINTENANCE

## 9.7 KEYBOARD TEST ERROR

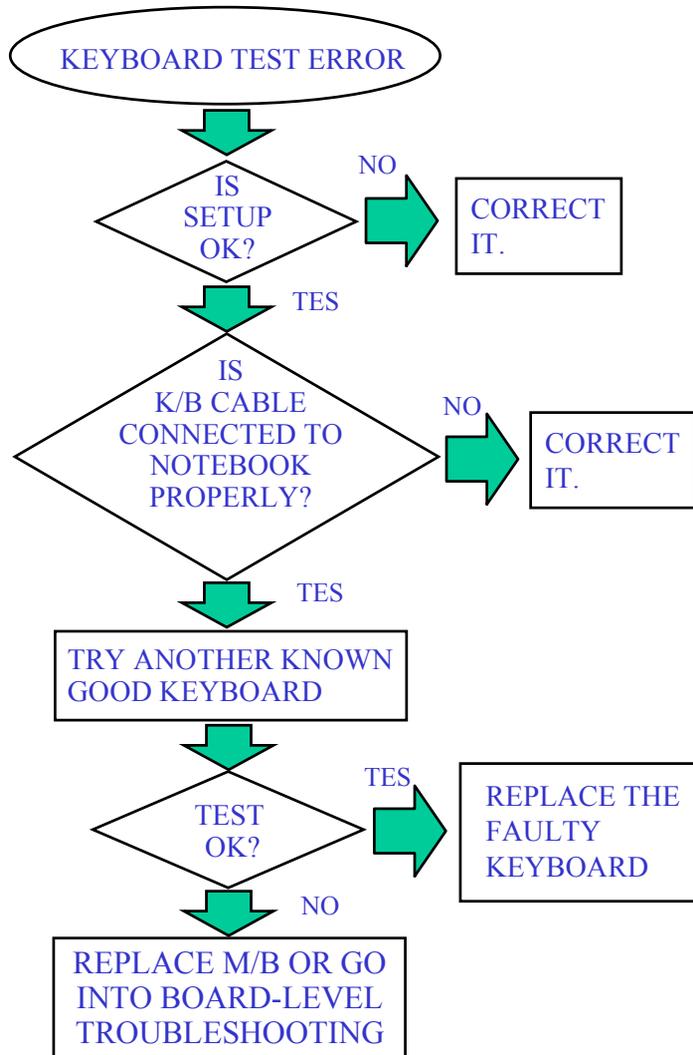
1. ERROR MESSAGE OF KEYBOARD FAILURE IS SHOWN OR ANY KEY DOESN'T WORK.
2. PIO DEBUG BOARD SHOWS THE PORT 378H ERROR CODE IS STOPPED AT 30H,31H,32H OR 33H



# 5027 N/B MAINTENANCE

## 9.7 KEYBOARD TEST ERROR

1. ERROR MESSAGE OF KEYBOARD FAILURE IS SHOWN OR ANY KEY DOESN'T WORK.
2. PIO DEBUG BOARD SHOWS THE PORT 378H ERROR CODE IS STOPPED AT 30H,31H,32H,33H



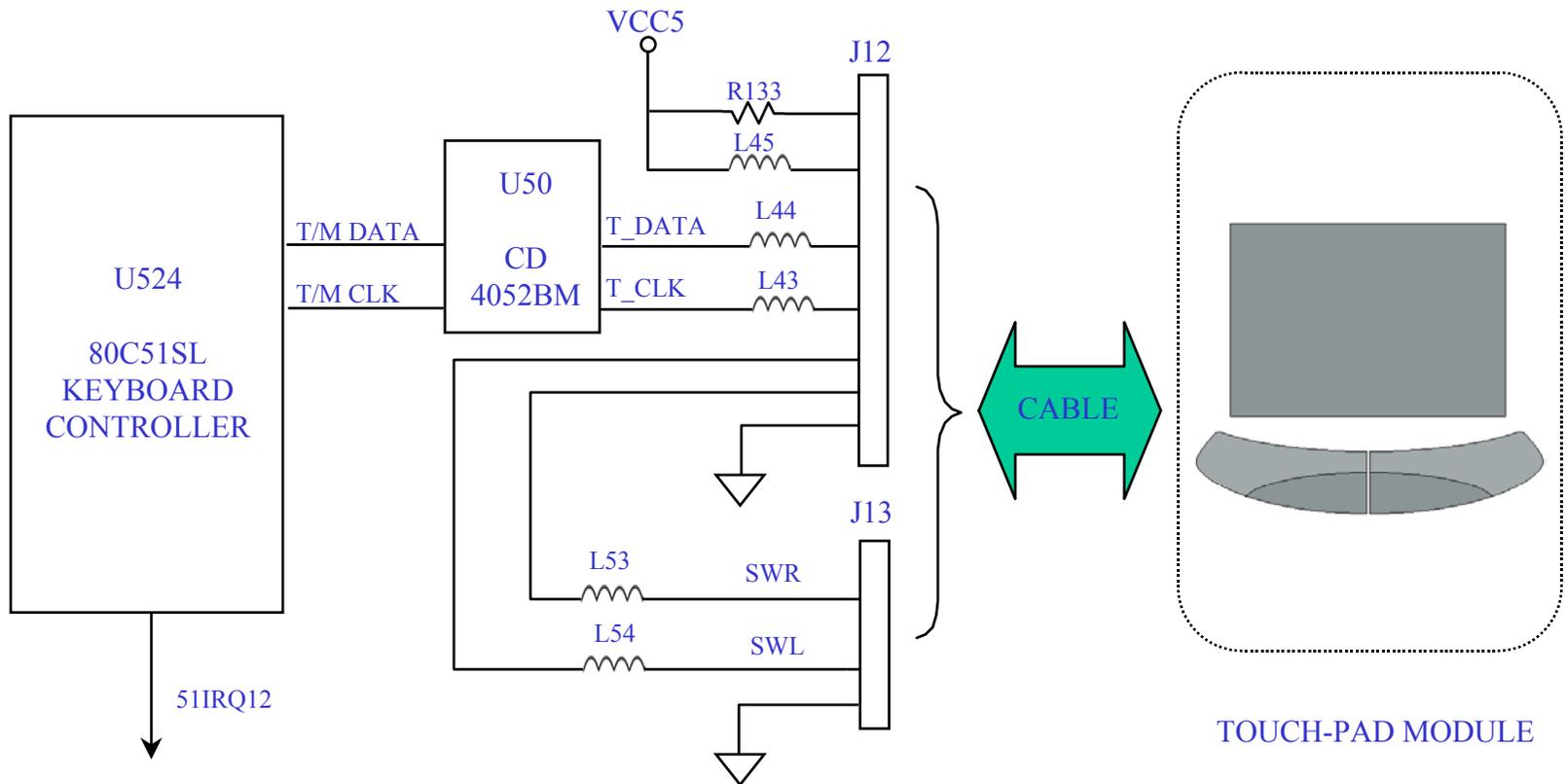
CHECK THE FOLLOWING PARTS FOR COLD SOLDER OR ONE OF THE FOLLOWING PARTS ON THE MOTHERBOARD MAY BE DEFECTIVE, USE AN OSCILLOSCOPE TO CHECK THE FOLLOWING SIGNAL OR REPLACE THE PARTS ONE AT A TIME AND TEST AFTER EACH REPLACEMENT.

PARTS:	SIGNALS:
U26, U524	KBD SEL SA2
J7, J500	KI[0:7] 51IOWR#
F1, L19, L20	KO[0:15] 51IORD#
L22, EC13	KBDATA 51IRQ1
EC14	KBCLK 51IRQ12
	SIKBCS# SD[0:7]

# 5027 N/B MAINTENANCE

## 9.8 TRACK PAD TEST ERROR

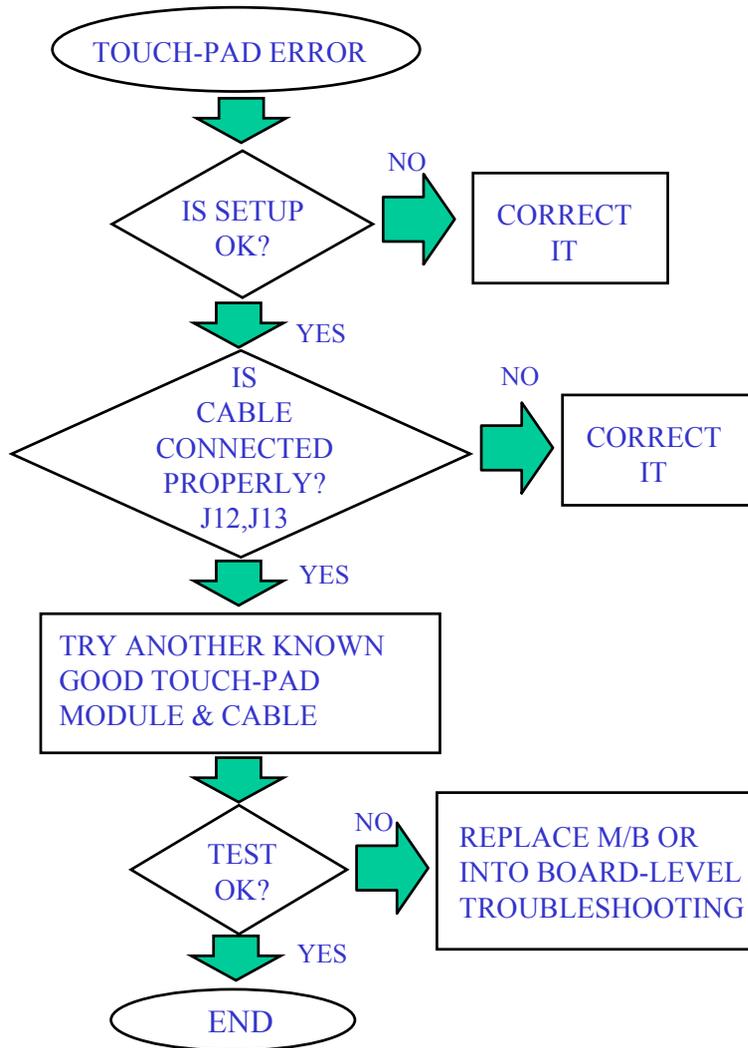
AN ERROR MESSAGE IS SHOWN WHEN TOUCH-PAD IS ENABLED.



# 5027 N/B MAINTENANCE

## 9.8 TRACK PAD TEST ERROR

AN ERROR MESSAGE IS SHOWN WHEN TOUCH-PAD IS ENABLED.



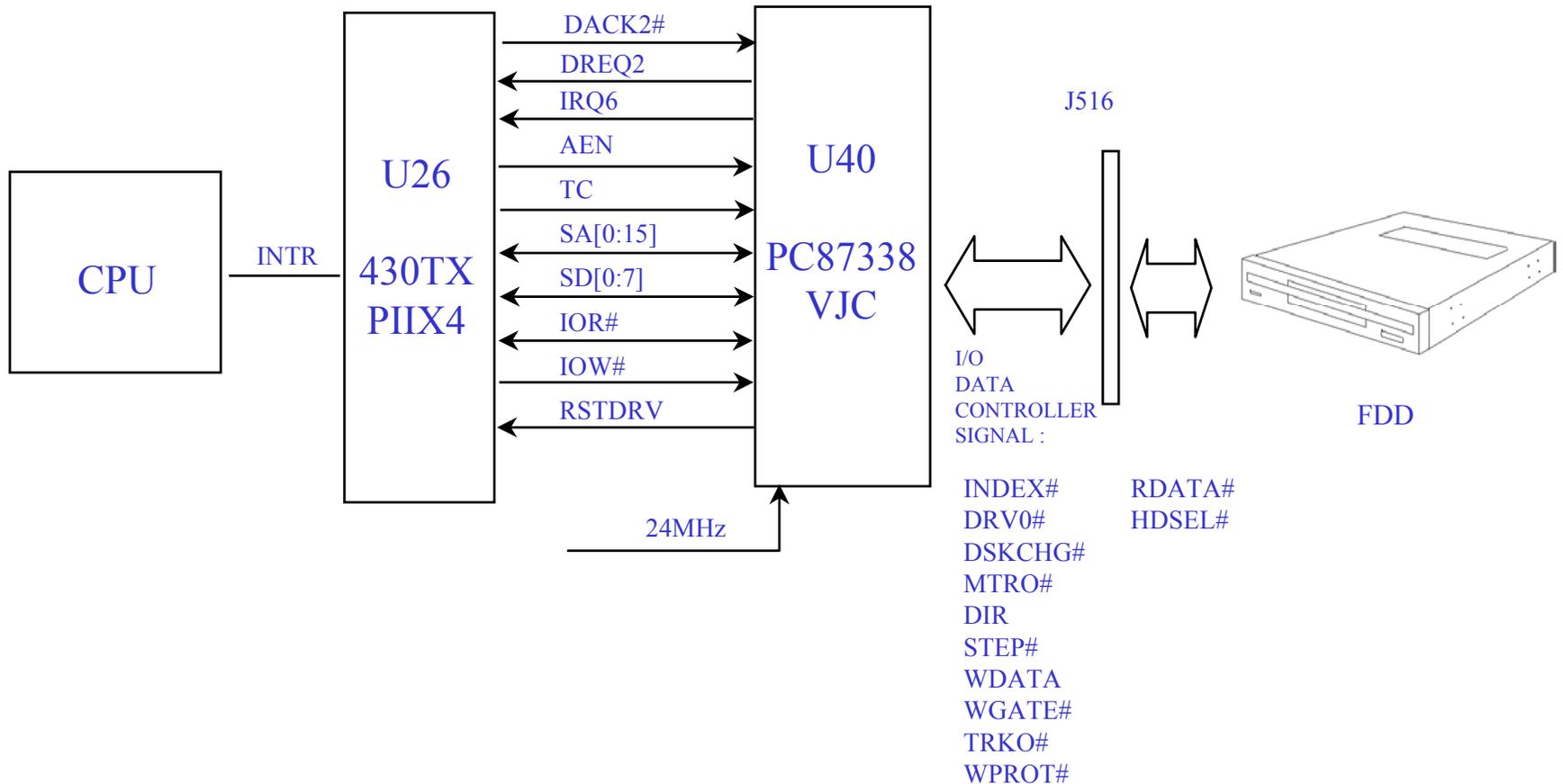
CHECK THE FOLLOWING PARTS FOR COLD SOLDER OR ONE OF THE FOLLOWING PARTS ON THE MOTHERBOARD MAY BE DEFECTIVE, USE AN OSCILLOSCOPE TO CHECK THE FOLLOWING SIGNAL OR REPLACE THE PARTS ONE AT A TIME AND TEST AFTER EACH REPLACEMENT.

PARTS:	SIGNALS:	
U524	T/M DATA	51HQ12
U50	T/M CLK	VCC5
R133	T_DATA	
L43 L53	T_CLK	
L44 L54	SWR	
L45	SWL	

# 5027 N/B MAINTENANCE

## 9.9 DISKETTE DRIVE TEST ERROR

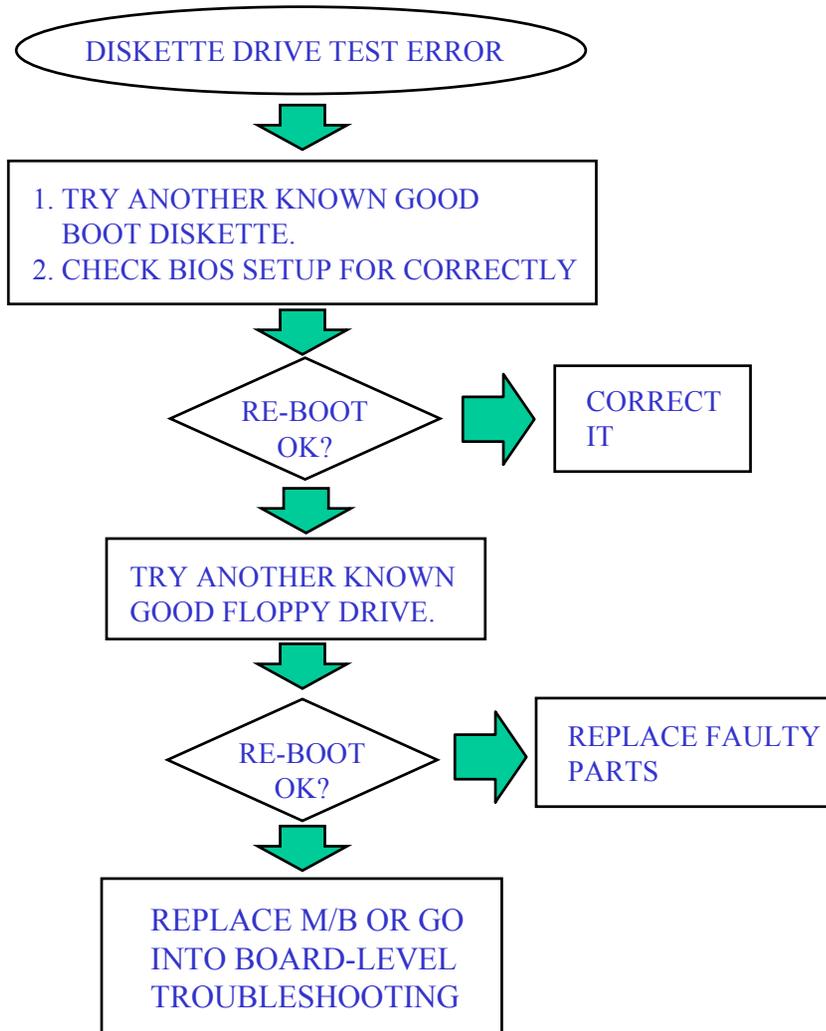
AN ERROR MESSAGE IS SHOWN WHEN READING/ WRITING DATA FROM/TO DISKETTE DRIVE.



# 5027 N/B MAINTENANCE

## 9.9 DISKETTE DRIVE TEST ERROR

AN ERROR MESSAGE IS SHOWN WHEN READING/ WRITING DATA FROM/TO DISKETTE DRIVE.



## BOARD-LEVEL TROUBLESHOOTING FOR TOUCH-PAD TEST ERROR

CHECK THE FOLLOWING PARTS FOR COLD SOLDER OR ONE OF THE FOLLOWING PARTS ON THE MOTHERBOARD MAY BE DEFECTIVE, USE AN OSCILLOSCOPE TO CHECK THE FOLLOWING SIGNAL OR REPLACE THE PARTS ONE AT A TIME AND TEST AFTER EACH REPLACEMENT.

### PARTS:

U26  
U40

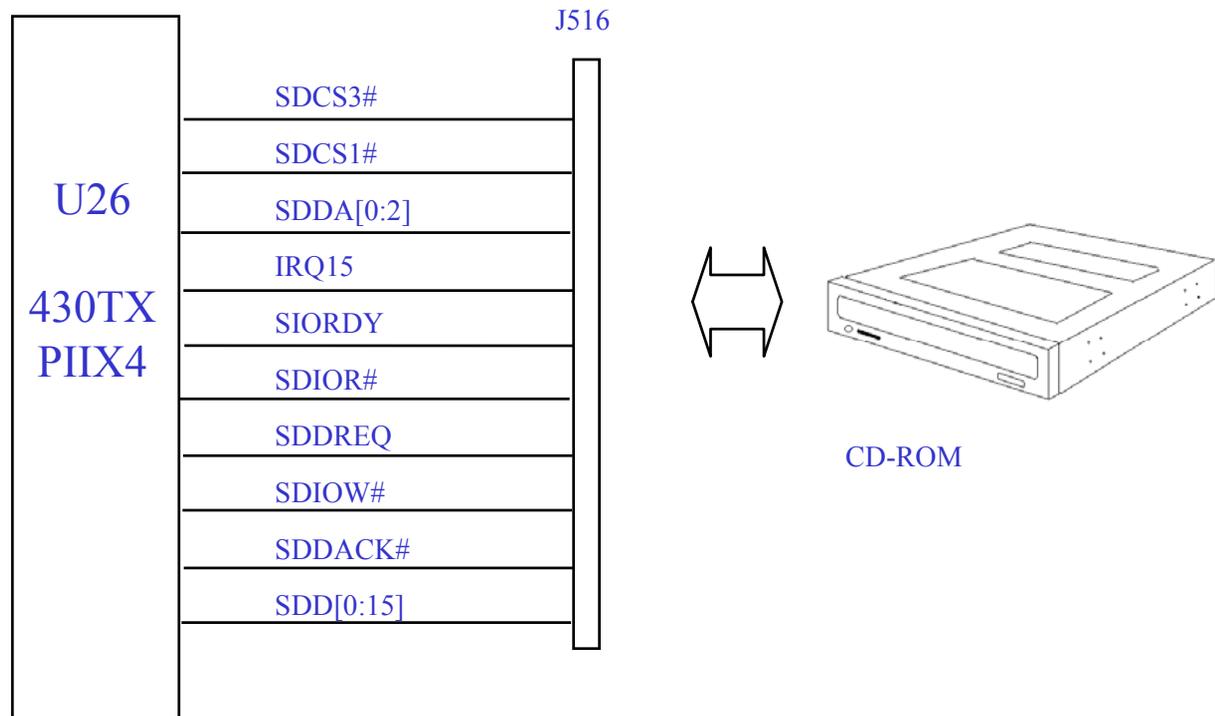
### SIGNALS:

DACK2# SD[0:7]  
DREQ2 IOR#  
IRQ6 IOW#  
AEN RSTDRV  
TC 24MHz  
SA[0:15]

# 5027 N/B MAINTENANCE

## 9.10 CD-ROM DRIVE TEST ERROR

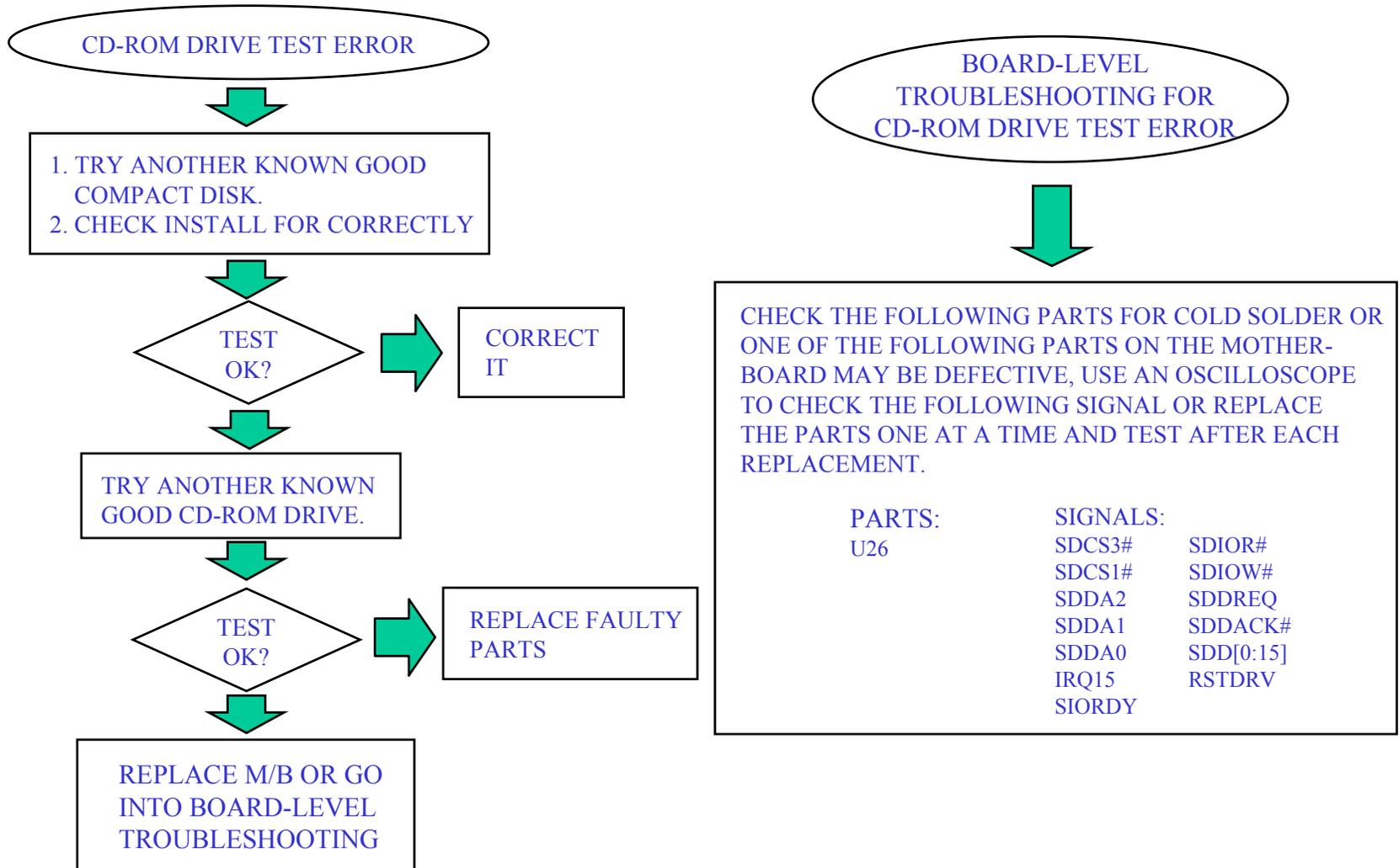
AN ERROR MESSAGE IS SHOWN WHEN READING DATA FROM CD-ROM DRIVE.



# 5027 N/B MAINTENANCE

## 9.10 CD-ROM DRIVE TEST ERROR

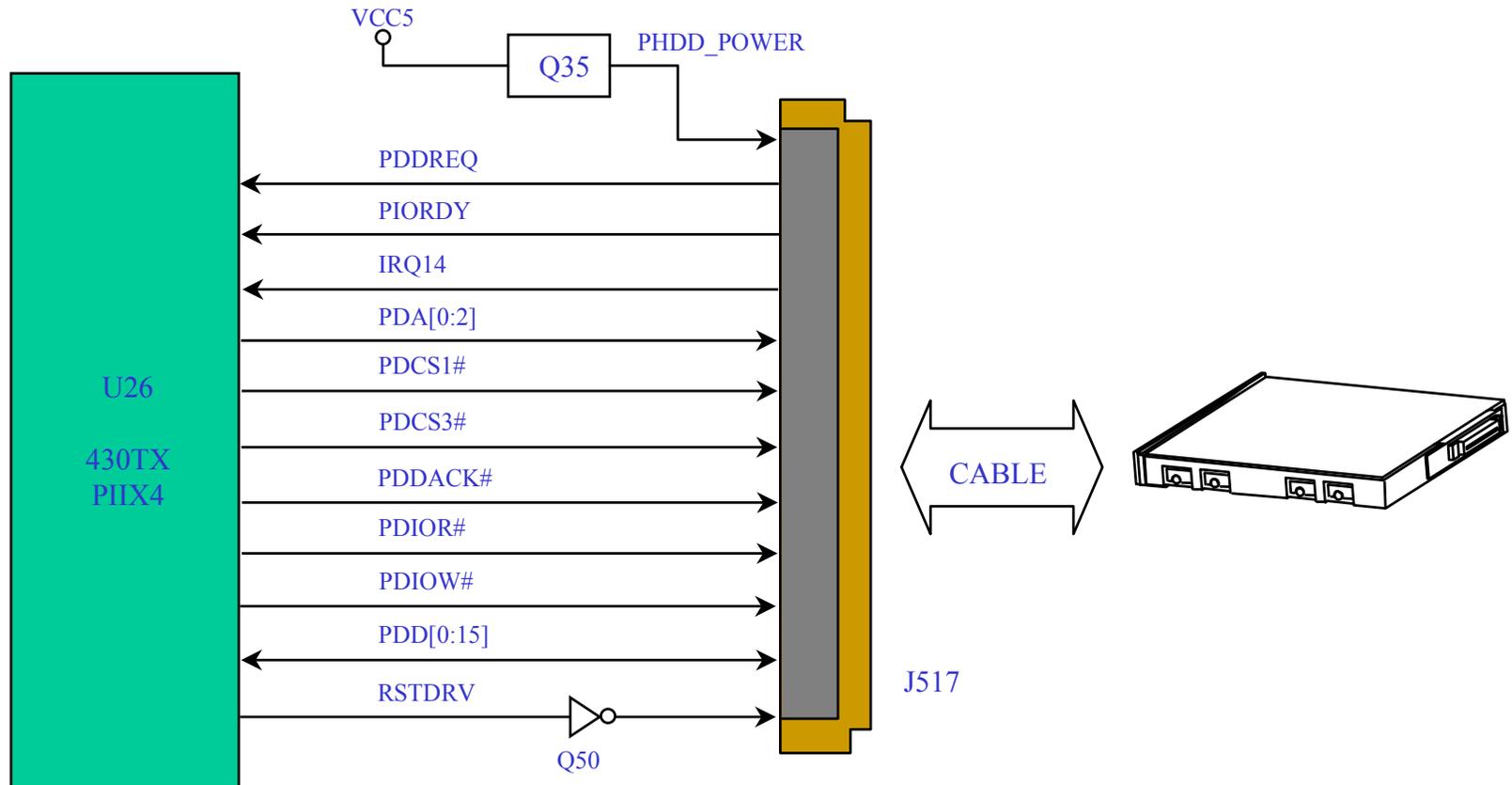
AN ERROR MESSAGE IS SHOWN WHEN READING GATA FROM CD-ROM DRIVE.



# 5027 N/B MAINTENANCE

## 9.11 HARD DRIVE TEST ERROR

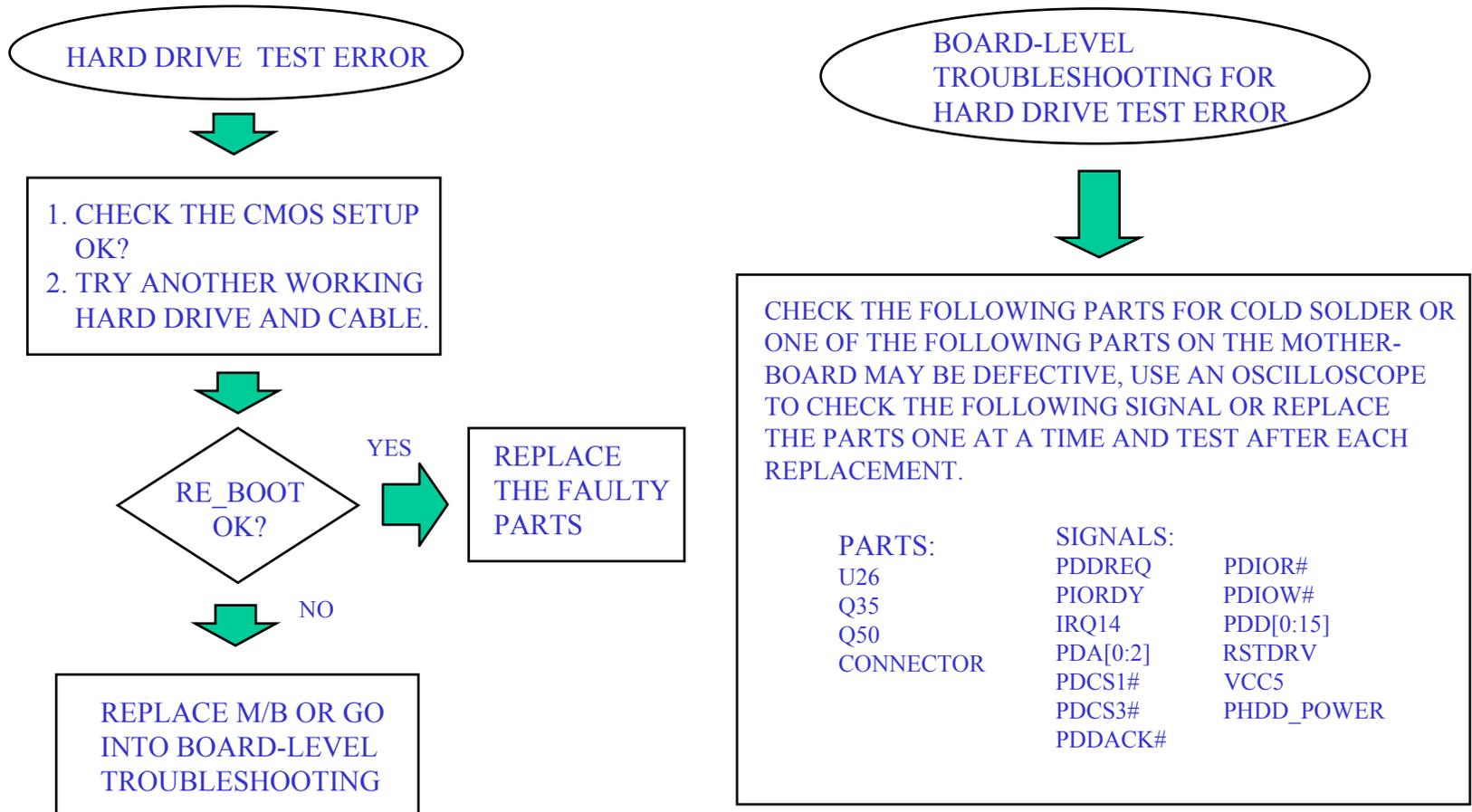
EITHER AN ERROR MESSAGE IS SHOWN , OR THE DRIVER MOTOR SPINS NON-STOP , WHILE READING DATA FROM OR WRITING DATA TO HARD-DISK.



# 5027 N/B MAINTENANCE

## 9.11 HARD DRIVE TEST ERROR

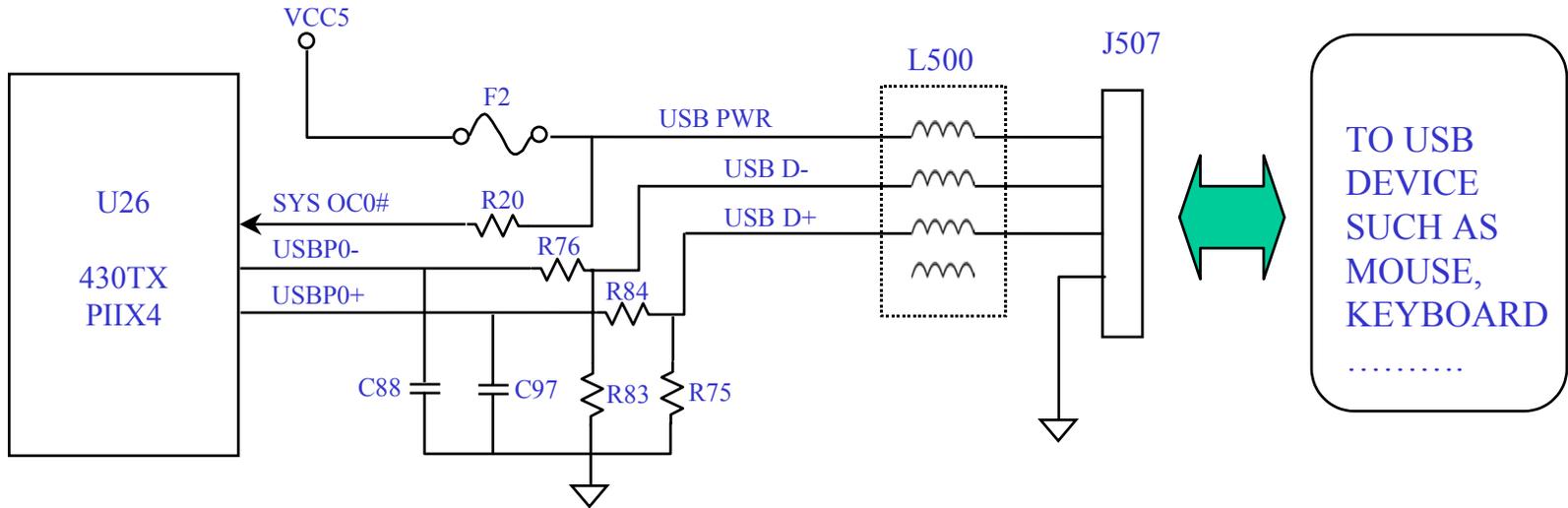
EITHER AN ERROR MESSAGE IS SHOWN , OR THE DRIVER MOTOR SPINS NON-STOP , WHILE READING DATA FROM OR WRITING DATA TO HARD-DISK.



# 5027 N/B MAINTENANCE

## 9.12 USB PORT TEST ERROR

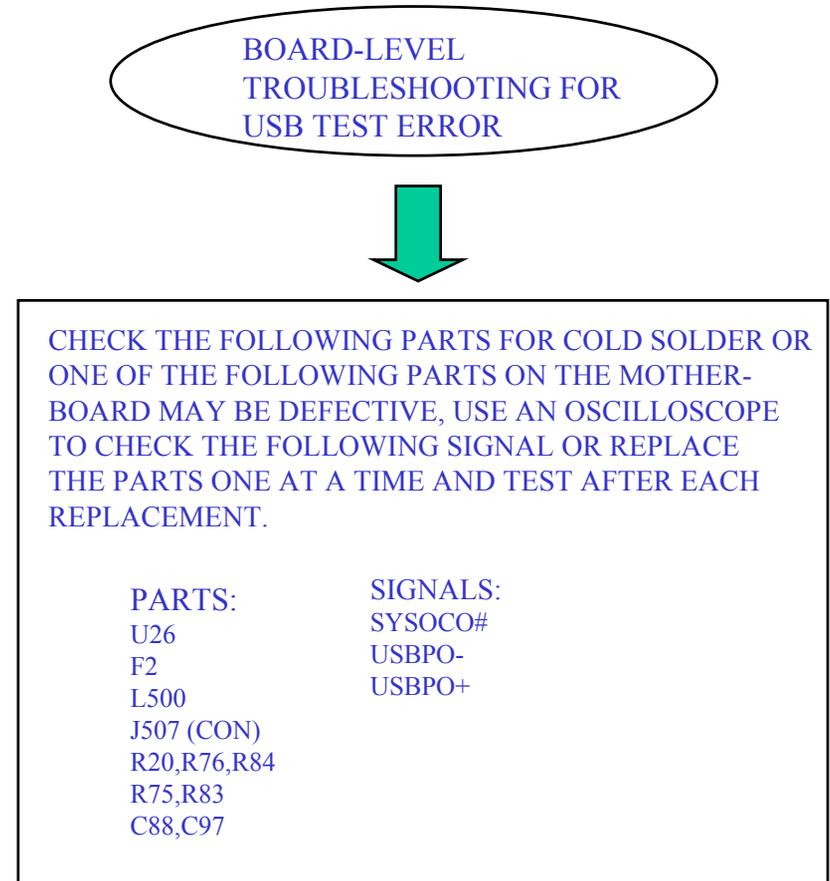
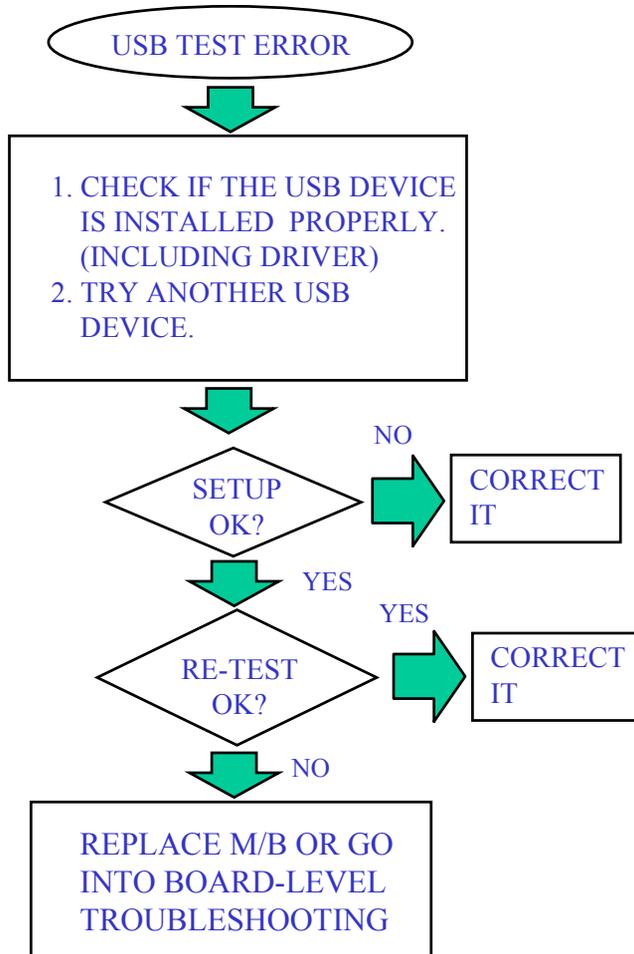
AN ERROR OCCURS WHEN A USB I/O DEVICE IS INSTALLED.



# 5027 N/B MAINTENANCE

## 9.12 USB PORT TEST ERROR

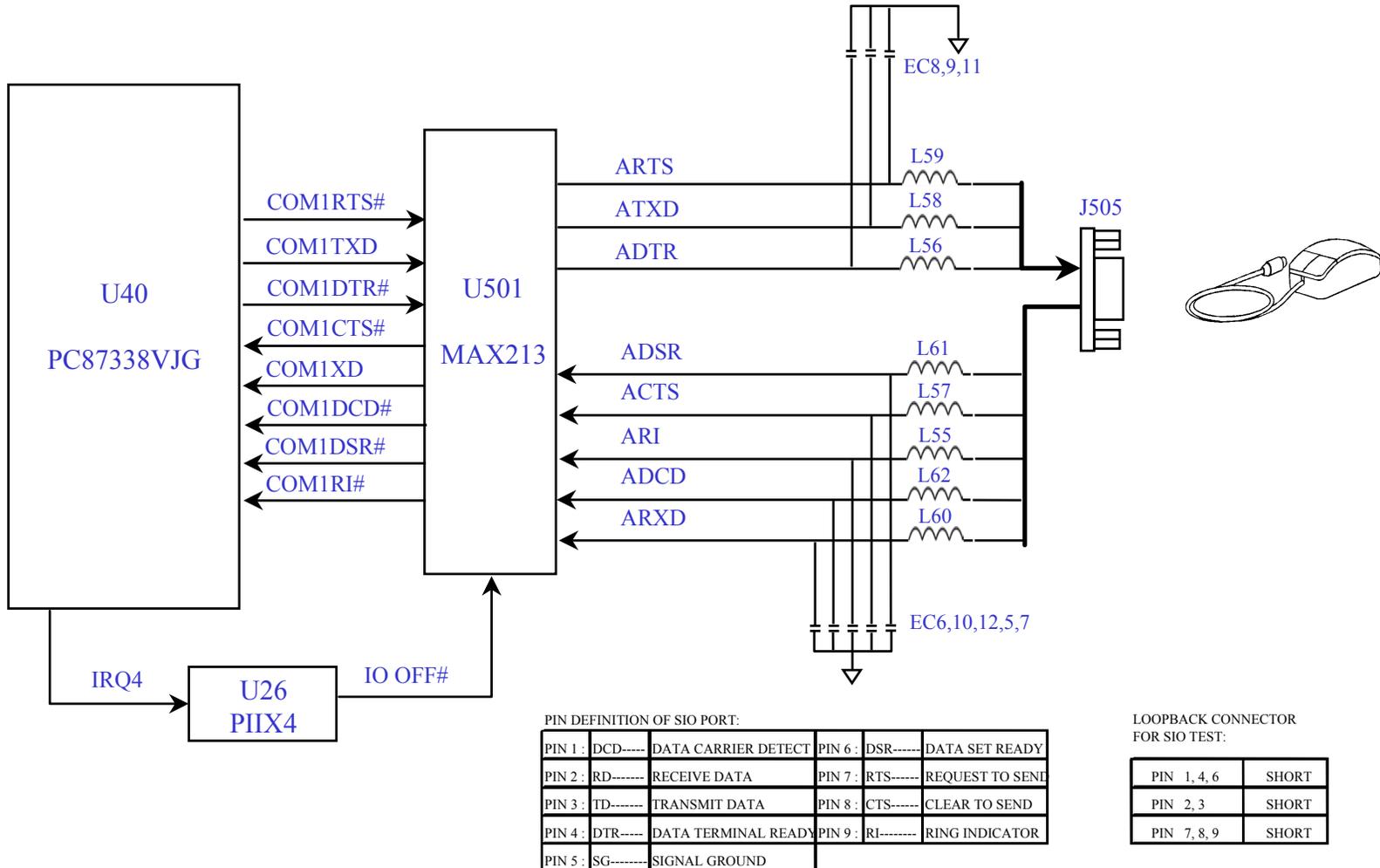
AN ERROR OCCURS WHEN A USB I/O DEVICE IS INSTALLED.



# 5027 N/B MAINTENANCE

## 9.13 SIO PORT TEST ERROR

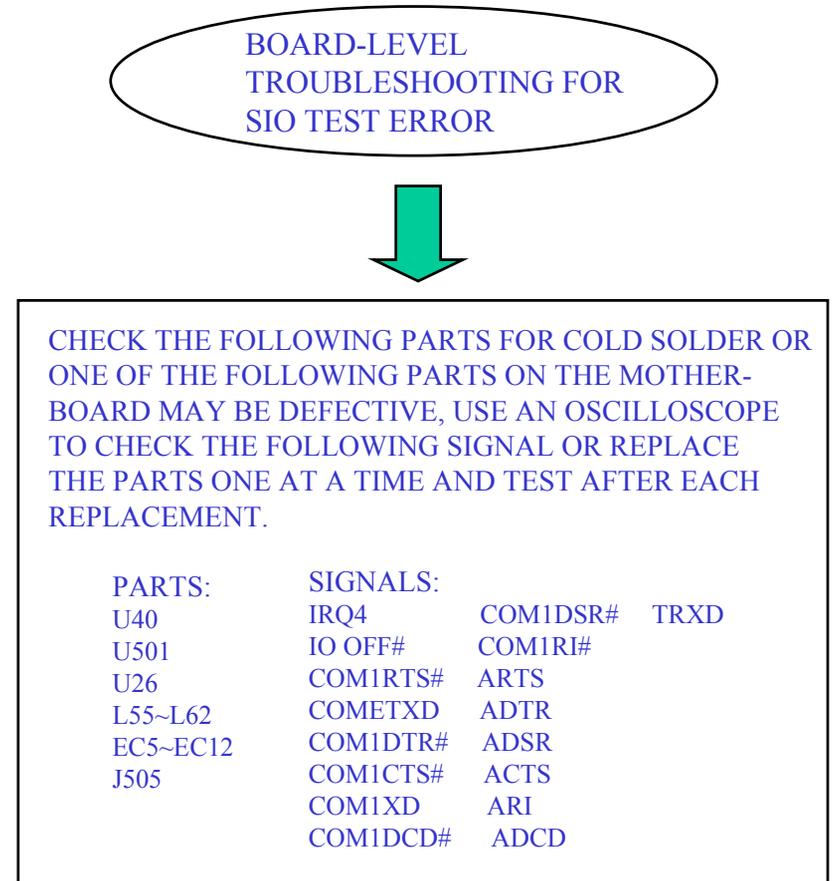
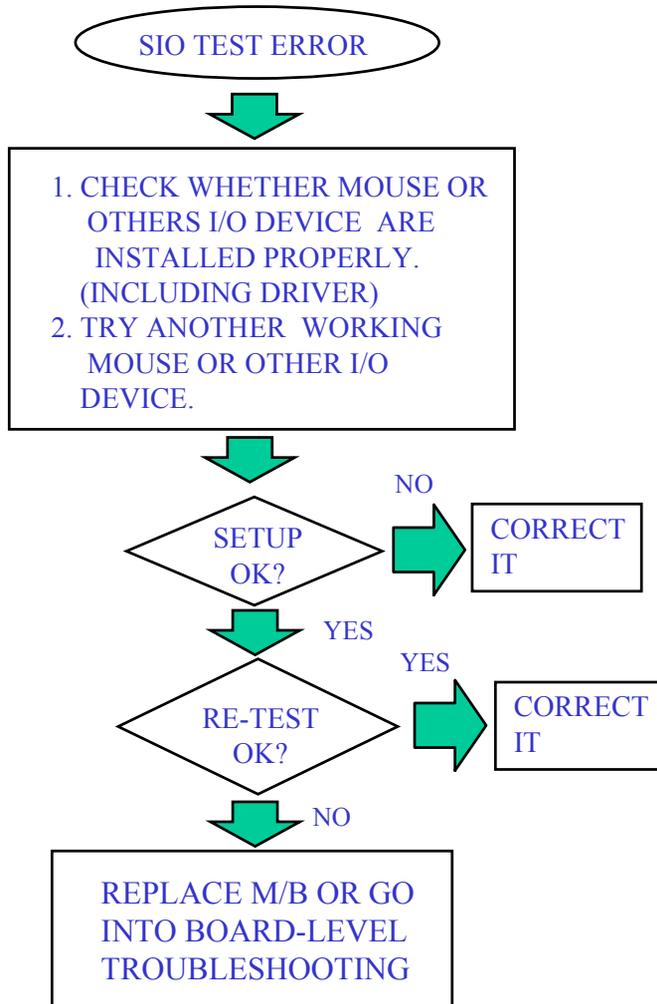
AN ERROR OCCURS WHEN A MOUSE OR OTHER I/O DEVICE IS INSTALLED.



# 5027 N/B MAINTENANCE

## 9.13 SIO PORT TEST ERROR

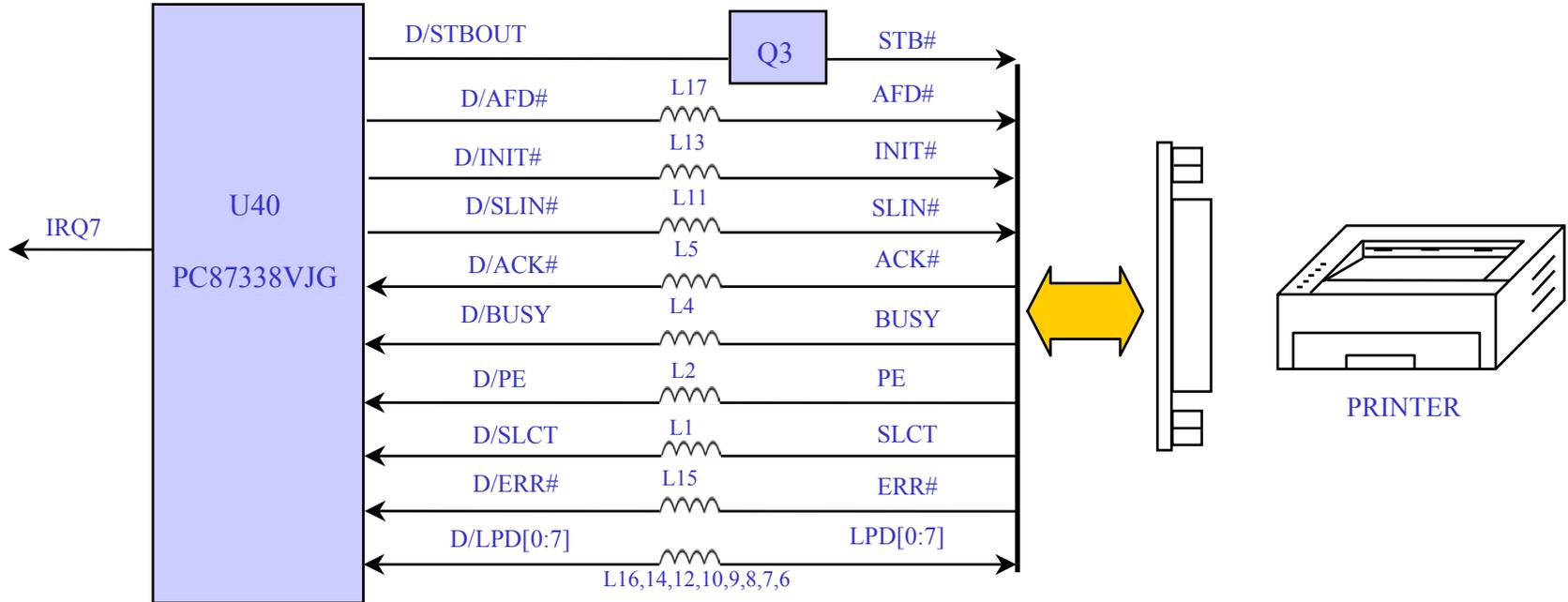
AN ERROR OCCURS WHEN A MOUSE OR OTHER I/O DEVICE IS INSTALLED.



# 5027 N/B MAINTENANCE

## 9.14 PIO PORT TEST ERROR

WHEN A PRINT COMMAND IS ISSUED, PRINTER PRINTS NOTHING OR GARBAGE.



PIN DEFINITION OF PIO PORT

PIN 1	STB	STROBE SIGNAL	PIN 14	AFD	AUTO LINE FEED
PIN 2-9	D0 -D7	PARALLEL PORT DATA BUS D0 TO D7	PIN 15	ERR	ERROR AT PRINTER
PIN 10	ACK	ACKNOWLEDGE HANDSHAK	PIN 16	INIT	INITIATE OUTPUT
PIN 11	BUSY	BUSY SIGNAL	PIN 17	SLIN	PRINTER SELECT
PIN 12	PE	PAPER END	PIN 18-25:		SIGNAL GROUND
PIN 13	SLCT	PRINTER SELECTED			

LOOPBACK CONNECTOR FOR PIO TEST:

PIN 1,13	SHORT	PIN 10,16	SHORT
PIN 2,15	SHORT	PIN 11,17	SHORT
PIN 12,14	SHORT		

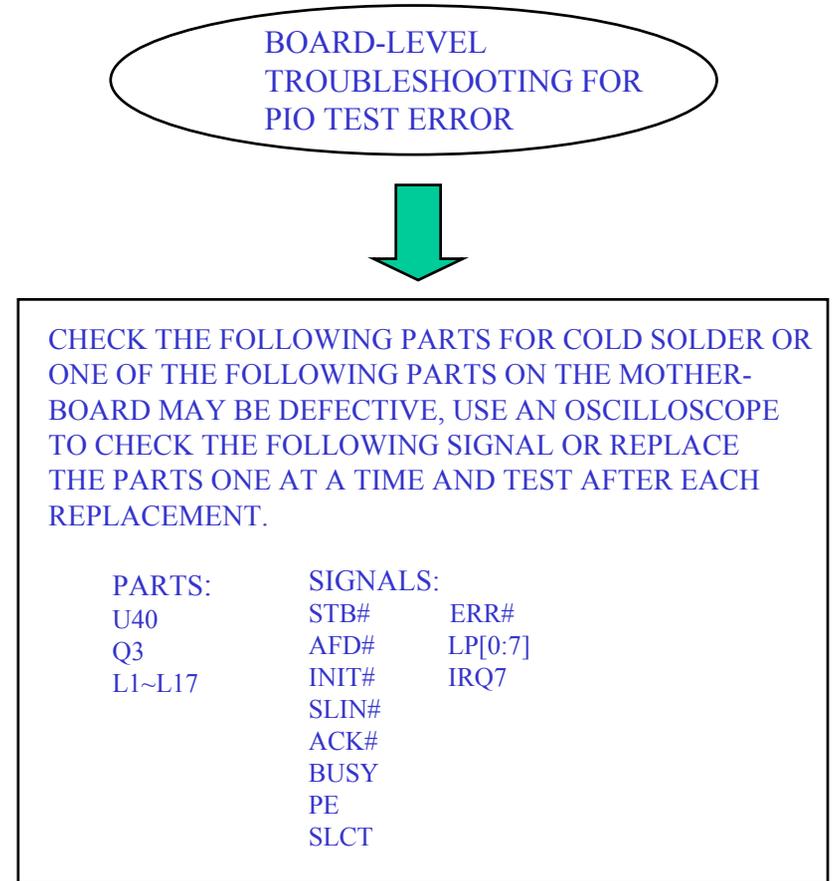
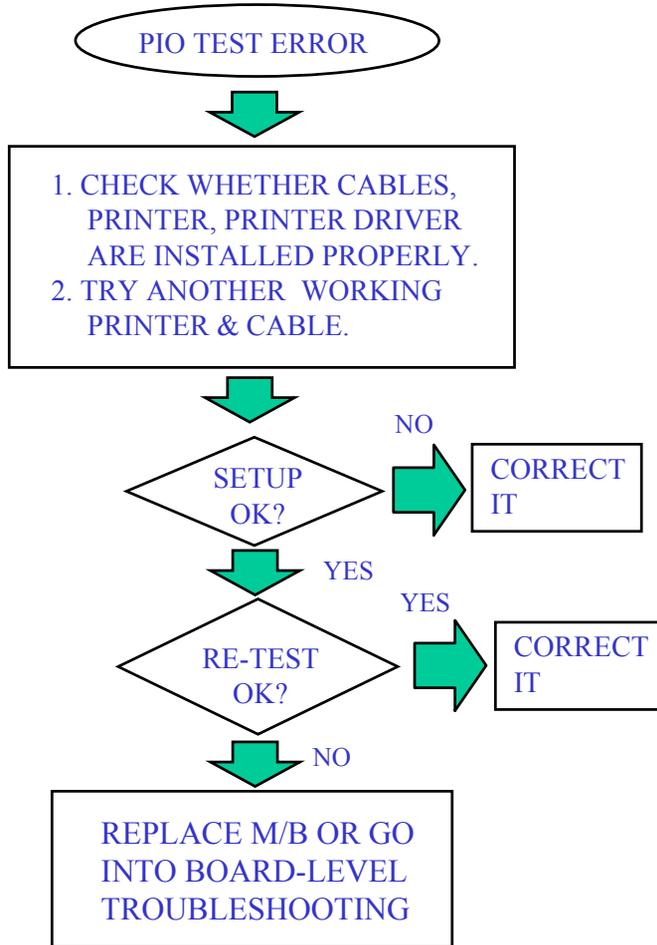
LOOPBACK CONNECTOR FOR EPP TEST:

PIN 1,2,4,6,8	SHORT
PIN 3,5,7,9,16	SHORT
PIN 18,19,20,21,22,23,24,25	SHORT

# 5027 N/B MAINTENANCE

## 9.14 PIO PORT TEST ERROR

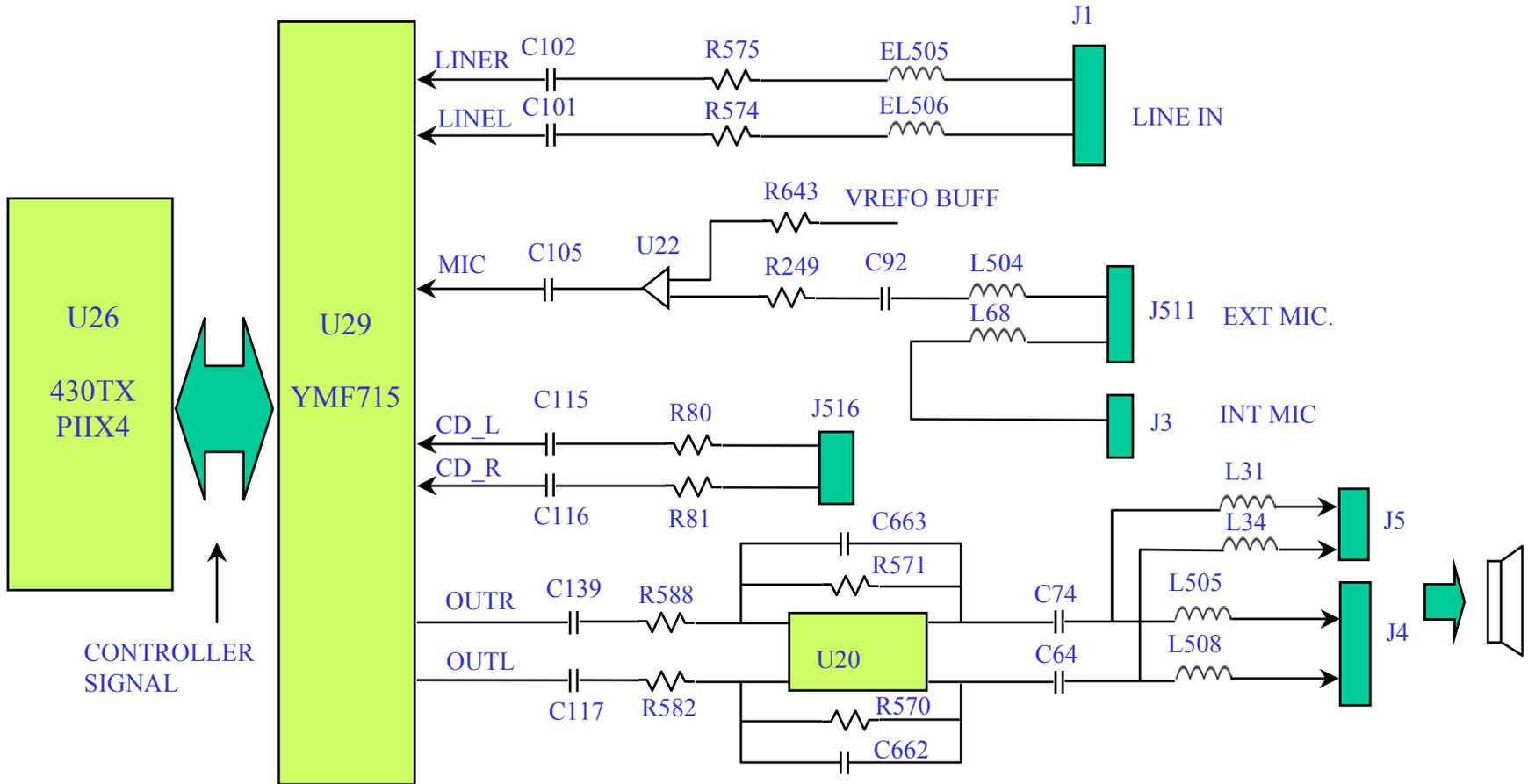
WHEN A PRINT COMMAND IS ISSUED, PRINTER PRINTS NOTHING OR GARBAGE.



# 5027 N/B MAINTENANCE

## 9.15 AUDIO FAILURE

NO SOUND FROM SPEAKER AFTER AUDIO DRIVER IS INSTALLED.



# 5027 N/B MAINTENANCE

## 9.15 AUDIO FAILURE

NO SOUND FROM SPEAKER AFTER AUDIO DRIVER IS INSTALLED.

AUDIO DRIVE FAILURE

1. CHECK TO SEE THAT ALL CABLES AND DEVICE ARE CONNECTED PROPERLY.
2. MAKE SURE THAT ALL OF SOFTWARE DRIVERS ARE INSTALLED PROPERLY.

TEST  
OK?

1. TRY ANOTHER KNOWN GOOD SPEAKER, CABLE AND CD-ROM.
2. MAKE SURE THAT SETUP IS OK, SUCH AS I/O ADDRESS, IRQ

TEST  
OK?

END

REPLACE M/B OR GO INTO BOARD-LEVEL TROUBLESHOOTING

BOARD-LEVEL  
TROUBLESHOOTING FOR  
AUDIO TEST ERROR

CHECK THE FOLLOWING PARTS FOR COLD SOLDER OR ONE OF THE FOLLOWING PARTS ON THE MOTHERBOARD MAY BE DEFECTIVE, USE AN OSCILLOSCOPE TO CHECK THE FOLLOWING SIGNAL OR REPLACE THE PARTS ONE AT A TIME AND TEST AFTER EACH REPLACEMENT.

1. IF NO SOUND  
CAUSE OF  
LINE IN CHECK  
THE FOLLOWING  
PARTS & SIGNALS:

PARTS:	SIGNALS:
J1	LINER
EL505	LINEL
EL506	
R575	
5574	
C101	
C102	
U29	

2. IF NO SOUND  
CAUSE OF  
MIC CHECK  
THE FOLLOWING  
PARTS & SIGNALS:

PARTS:	SIGNALS:
J3	MIC
J511	
L504	
L68	
C92	
R249	
U22	
C105	
U29	

3. IF NO SOUND  
CAUSE OF  
CD-ROM CHECK  
THE FOLLOWING  
PARTS & SIGNALS:

PARTS:	SIGNALS:
J516	CD_L
R80	CD_R
R81	
C115	
C116	

IF STILL GET PROBLEM ,PLEASE CHECK THE OUTPUT CIRCUIT PARTS & SIGNALS AS ABOVE PAGE SHOWN.

# 5027 N/B MAINTENANCE

## 11. SPARE PARTS LIST (1)

PART_NO	DESCRIPTION	LOCATION
526266490003	PC;5027X/TG-001-00/XX-0M/1X	
431664900001	CASE KIT;5027	
332300000112	CABLE FFC,4P,T/P SW-M/B,130MM,50	
411664900001	PWA;PWA-5027 MOTHER BD	
242600000001	LABEL;PAL,20*5MM,COMMON	
242600000158	LABEL;10*10,BLANK,COMMON,HI-TEMP	
242600000172	LABEL;PCMCIA CARD WORKS/95 EN	
242600000174	LABEL;PENTIUM,PWR SUITE 1 NOTEBI	
242901300011	LABEL;BAR CODE,IB,BBU	
377102010300	S-STANDOFF;M2DP2H3L4,NIW	
377102010580	S-STANDOFF;M2DP4H5.8L4,NIW	
377102010800	S-STANDOFF;M2DP4H8.0L4,NIW	
411664900045	PWA;PWA-5027 V2 T/U MOTHER BD	
313000510003	FILTER;4LINE,360OHM/100MHZ,8P	L500,EL504
314149357402	XTAL;3.57MHZ,30PPM,AT-49,FUND	X1
314149443402	XTAL;4.43MHZ,30PPM,AT-49,FUND	X3
331030003004	CON;HDR,MA,3P*1,2.54MM,ST	J6,14
331030004010	CON;HDR,FM,2P*2,2MM,ST,SUYIN	J511
331030010010	CON;HDR,FM,5P*2,2.0MM,ST,DIP	J509
331040040004	CON;HDR,MA,20P*2,1.27MM,R/A	J517
331040046001	CON;HDR,FM,23P*2,2MM,R/A	J519
331040060001	CON;HDR,MA,30P*2,1.27MM,R/A	J516
331130004007	CON;HDR,SHR,MA,4P*1,H=13.83,R/A,	J507
331650029606	IC SOCKET;296P,ZIF,ZIFPGAFC	U504
331720009004	CON;D,MA,9P,2.775,R/A	J505
331720015011	CON;D,FM,15P,R/A,2.29,3 ROW,BLUE	J503
331720017601	CON;D,MA,176P,.8MM,R/A,4 ROW	J508
331720025005	CON;D,FM,25P,2.775,R/A	J504
331840005006	CON;STEREO JACK,5P,R/A,W9.1,MOJB	J1,4
331850002008	CON;RCA PIN JACK,2P,BLK,RJ-1003-	J501

PART_NO	DESCRIPTION	LOCATION
331870006008	CON;DIN,SKT,6P,MINI,R/A,W/SHIELD	J500
331910003003	CON;POWER JACK,3P,16VDC/3A	J502
411664900046	PWA;PWA-5027 V2 SMT MOTHER BD	
271002472301	RES;4.7K ,1/10W,5% ,0805,SMT	R5
271012000301	RES;0 ,1/8W,5% ,1206,SMT	R31,63,120,123,142,
271023918301	RES;9.1 ,1/4W,5% ,1210,SMT	R1,2
271071000002	RES;0 ,1/16W,0603,SMT	R35,43,46
271071100302	RES;10 ,1/16W,5% ,0603,SMT	R109,130
271071101301	RES;100 ,1/16W,5% ,0603,SMT	R80,81,127,185,188
271071102302	RES;1K ,1/16W,5% ,0603,SMT	R64,98,115,187,212
271071103302	RES;10K ,1/16W,5% ,0603,SMT	R10,16,19,34
271071104101	RES;100K ,1/16W,1% ,0603,SMT	R184,557,4,20,21,32,
271071105301	RES;1M ,1/16W,5% ,0603,SMT	R118,122,114,168,563
271071111101	RES;110 ,1/16W,1% ,0603,SMT	R152
271071153301	RES;15K ,1/16W,5% ,0603,SMT	R75,83,579,590
271071169311	RES;169K ,1/16W,1% ,0603,SMT	R148
271071203101	RES;20K ,1/16W,1% ,0603,SMT	R181,582,588
271071204101	RES;200K ,1/16W,1% ,0603,SMT	R131,580,581
271071221302	RES;22 ,1/16W,5% ,0603,SMT	R3,6,7,23,24,27,37,
271071223302	RES;22K ,1/16W,5% ,0603,SMT	R99
271071224301	RES;220K ,1/16W,5% ,0603,SMT	R566,567
271071270301	RES;27 ,1/16W,5% ,0603,SMT	R84,76
271071301311	RES;301K ,1/16W,1% ,0603,SMT	R203
271071303301	RES;30K ,1/16W,5% ,0603,SMT	R196,171
271071309311	RES;309K ,1/16W,1% ,0603,SMT	R556
271071330302	RES;33 ,1/16W,5% ,0603,SMT	R108,116,121,125
271071331301	RES;330 ,1/16W,5% ,0603,SMT	R155,531,548,179,90
271071333301	RES;33K ,1/16W,5% ,0603,SMT	R570-575
271071470301	RES;47 ,1/16W,5% ,0603,SMT	R159,100
271071471302	RES;470 ,1/16W,5% ,0603,SMT	R62,147,598

# 5027 N/B MAINTENANCE

## 11. SPARE PARTS LIST (2)

PART_NO	DESCRIPTION	LOCATION
271071472302	RES;4.7K ,1/16W,5% ,0603,SMT	R22,28-30,56,82
271071499111	RES;4.99K,1/16W,1% ,0603,SMT	R175
271071750302	RES;75 ,1/16W,5% ,0603,SMT	R9,594-596,513,514
271611100301	RP;10*4 ,8P ,1/16W,5% ,0612,SMT	RP17,20,22,32-34,500
271611103301	RP;10K*4 ,8P ,1/16W,5% ,0612,SMT	RP15,27,40,45,57,505
271611104301	RP;100K*4,8P ,1/16W,5% ,0612,SMT	RP21,29,35,46-48,52,
271611220301	RP;22*4 ,8P ,1/16W,5% ,0612,SMT	RP26,30,36
271611222301	RP;2.2K*4,8P ,1/16W,5% ,0612,SMT	RP506
271611272301	RP;2.7K*4,8P ,1/16W,5% ,0612,SMT	RP24
271611330301	RP;33*4 ,8P ,1/16W,5% ,0612,SMT	RP7,9,10,12-14,16,
271611472301	RP;4.7K*4,8P ,1/16W,5% ,0612,SMT	RP3
271621102303	RP;1K*8 ,10P,1/16W,5% ,1206,SMT	RP2,39
271621103303	RP;10K*8 ,10P,1/16W,5% ,1206,SMT	RP6,25,37,43,51,502
271621272301	RP;2.7K*8,10P,1/16W,5% ,1206,SMT	RP44
271621472303	RP;4.7K*8,10P,1/16W,5% ,1206,SMT	RP38,41,42,49,50,
272002105701	CAP;1U ,CR,16V , -20+80%,0805,SM	C72,75,76,92
272003224701	CAP;.22U ,CR,25V ,+80-20%,0805,Y	C77,78,83,85,584,
272012105702	CAP;1U ,CR,16V ,+80-20%,1206,Y	C2,7,22,24,84,114,
272012225702	CAP;2.2U ,CR,16V ,+80-20%,1206,Y	C170,169
272012335701	CAP;3.3U ,CR,16V , -20+80%,1206,S	C1,583
272072104702	CAP;.1U ,16V,+80-20%,0603,SMT	EC40,78-80,82-84,
272073180401	CAP;18P ,CR,25V ,10%,0603,NPO,S	EC81,85,559,C526,
272075100701	CAP;10P ,50V ,+80-20%,0603,SMT	C3,94,110,EC67,72,
272075101701	CAP;100P ,50V ,+80-20%,0603,SMT	RP17,20,22,32-34,500
272075102402	CAP;1000P,CR,50V,10%,0603,X7R,IN	C124,125,135,136,
272075103702	CAP;.01U ,50V,+80-20%,0603,SMT	EC34,C126
272075120301	CAP;12P ,CR,50V ,5% ,0603,NPO,S	C600,601
272075121401	CAP;120P ,CR,50V ,10%,0603,NPO,S	EC521,522
272075181301	CAP;180P ,50V ,5% ,0603,SMT	C41,EC16-33,41,43,
272073152401	CAP;1500P,CR,25V ,10%,0603,X7R,S	C222

PART_NO	DESCRIPTION	LOCATION
272075271401	CAP;270P ,50V,+ -10%,0603,SMT	C238,239
272075470701	CAP;47P ,50V ,+80-20%,0603,SMT	C88,93,97,209,215,
272075509801	CAP;5P ,CR,50V,+ -.5PF,0603,NP	C560
272075561701	CAP;560P ,CR,50V ,+80-20%,0603,S	C99,100
272401226502	CAP;22U ,TT,10V ,20%,6032,SMT	C63,112,130,175
272401476501	CAP;47U ,TT,10V ,20%,6032,SMT	C64,74
272402106501	CAP;10U ,TT,16V,20%,6032	C23,29,30,81,178,
272403106502	CAP;10U ,TT,25V ,20%,6032,SMT	C227
272421226501	CAP;22U ,TT,6.3V,20%,3528,SMT	C52,515
272422106501	CAP;10U ,TT,16V ,20%,3528,SMT	C162,163,180,192
272423475501	CAP;4.7U ,TT,20V ,20%,3528,SMT	C190,234,232
272431107502	CAP;100U ,TT,10V ,20%,7343,SMT	C657-659,546,545
272431151401	CAP;150U ,TT,10V ,10%,7343H,LOW	C532
272431227501	CAP;220U ,TT,6.3V,20%,7343,SMT	C14
273000053228	INDUCTOR;2.2UH,5%,3225,SMT	L40,47
273000130001	FERRITE CHIP;120OHM/100MHZ,1608,	L20,22,36-38,43-45
273000130003	FERRITE CHIP;40OHM/100MHZ,1608,S	L19,511
273000130006	FERRITE CHIP;600OHM/100MHZ.,2A,1	L1-18,30,31,33,34,
273000150002	FERRITE CHIP;120OHM/100MHZ,2012,	EL1-4,6,7,8,10,
273000150009	FERRITE CHIP;30OHM/100MHZ,2012,S	L39,503
273000250005	FERRITE CHIP;160OHM/100MHZ,6A,45	L24,49,51,52,27,28
274011431402	XTAL;14.318MHZ,16PF,50PPM,H=1.4M	X4,500
274011600404	XTAL;16MHZ,16PF,50PPM,H=1.4MM,SM	X5
274013276101	XTAL;32.768KHZ,FUND,50PPM,SMT	X501
282074338401	IC;74CBT3384DBQ,Q SWITCH,QSOP,24	U2,3
282104052001	IC;CD4052BM,MULTIPLEXER,SO,16P	U36,50
282151686101	IC;PI5C16861,BUS SW,150MIL,BQSOP	U8,9
282574014004	IC;74AHC14,HEX INVERTER,TSSOP,14	U15,510
282574032005	IC;74AHC32,QUAD 2-I/P OR,TSSOP,1	U23
282574074004	IC;74AHC74,DUAL D F/F,TSSOP,14P	U47

# 5027 N/B MAINTENANCE

## 11. SPARE PARTS LIST (3)

PART_NO	DESCRIPTION	LOCATION
282574086002	IC;74VHC86,QUAD 2I/P XOR,SSOP,14	U511,512,517-519
282574244004	IC;74VHC244MSC,OCTAL BUF,SSOP,20	U44-46,55-57
282574245003	IC;74VHC245,OCT TRANS,SSOP,20P	U37
282574373003	IC;74VHC373,OCT D-TRAN,SSOP,20P	U505
282574374003	IC;74AHC374,OCT 3ST D F/F,TSSOP,	U42,54
284100430001	IC;FW82439TX,MTXC,CPU/PCI,BGA,32	U27
284100430002	IC;FW82371AB,PIIX4,PCI/ISA,BGA,3	U26
284500045001	IC;LM45B,TEMPERATURE SENSORS,SOT	U506
284500516001	IC;YAC516-E,DAC,SSOP,24P	U34
286505262001	IC;PLL52C62-01,CLOCK GEN.,SSOP,4	U507
284500704002	IC;YMF704C,FM+WAVE TABLE,SQFP,10	U38
284500715001	IC;YMF715,AUDIO CHIP,SQFP,100P	U29
284500724001	IC;AD724,RGB TO NTSC/PAL,SO,16P	U10
284502563001	IC;MIC2563,CARDBUS PWR CTRL,SSOP	U17
284505330001	IC;PI5V330,WIDEBAND/VIDEO,QSOP,1	U6
284506832003	IC;OZ6832,PCI/CARDBUS,TQFP,208P	U31
284508228001	IC;82C28,INTERRUPT/PWR CTRL,SOL,	U24
284509385001	IC;CYBER9385F,VGA,CTRL,BGA,256P	U28
284580051001	IC;80C51SL-BG,KBD CTRL,PQFP,100P	U524
284587338002	IC;PC87338VJG,SUPER I/O,TQFP,100	U40
286100358012	IC;LM358,DUAL OP/AMP,SO 8P	U22,30,49,52,58
286100372014	IC;TLC372CD,DUAL COMP,SO	U39
286104863001	IC;LM4863,1W,AUDIO AMP,SO,16P	U20
286200213002	IC;ADM213E,RS-232,+/-15KVESD,SSOP	U501
286301267001	IC;DS1267,POTENTIOMETER,SOL,16P	U33
286302951015	IC;LP2951ACM,VOLTAGE REGULATOR,S	U35
286305200001	IC;MIC5200-5BS,VOL REG,SOT-223	U41
286329152001	IC;MIC29152,VOL REG,TO-263-5	U14,U7
286500351001	IC;CDC351,CLOCK DRIVER,SSOP,24P	U503
286501422001	IC;MK1422,CLOCK GENERATOR,SO,8P	U32

PART_NO	DESCRIPTION	LOCATION
288031110001	FIR;IBM31T1100A,TRANSCE. MODULE,	U500
288100202002	DIODE;DAP202K,80V,SWITCH,DUAL,SO	D23
288100212001	DIODE;DAN212K,80V,SWITCH,SOT23	D1-4,6-15,17-22,500
288100701002	DIODE;BAV70LTI,70V,225MW,SOT-23	D5,16,502
288200144001	TRANS;DTC144WK,NPN,SMT	Q4,11,7,18,49-53
288200352001	TRANS;NDS352P,DMOS,TO-236AB	Q12,19,20,27,31
288203906018	TRANS;MMBT3906L,PNP,Tr35NS,TO236	Q37
288209410001	TRANS;SI9410DY,N-MOSFET,.04OHM,S	Q8,
288209430001	TR;NDS9430,P-FET,.06OHM,SO,8P	Q35,41
288209958001	TRANS;NDS9958,DUAL N&P MOSFET,SO	Q3
288227002001	TRANS;2N7002LTI,N-CHANNEL FET	Q1,2,26,33
291000010802	CON;HDR,MA,8P*1,1.25,ST,SMT,HIRO	J9
291000016010	CON;HDR,MA,30P*2,.6MM,ST,SMT,H=4	J2
291000022401	CON;HDR,FM,12P*2,1.27MM,R/A,SMT	J513
291000142004	CON;FPC/FFC,20P,1MM,ST,ZIF,SMT	J8
291000142602	CON;FPC/FFC,26P,1MM,ST,ZIF,SMT	J7
291000150401	CON;FPC/FFC,4P,1MM,R/A,SMT	J13
291000150804	CON;FPC/FFC,8P,1MM,R/A,2CONTAC,E	J12
291000251563	CON;IC CARD,78P*2,MA,.6MM,SMT	J514
291000410201	CON;WFR,MA,2P,1.25,ST,SMT/MB	J3,10,518
291000410301	CON;WFR,MA,3P,1.25,ST,SMT/MB	J515
291000410401	CON;WFR,MA,4P,1.25MM,ST,SMT	J5
291000610032	IC SOCKET;32P,PLCC,TIN,W/O PEGS,	U1,11
295000010014	FUSE;1.1A/6V,POLY SWITCH,PTC,SMD	F1,2
297030105001	SW;PUSH BUTTON,SPSD,48V/.05A,SMT	SW1
297120101005	SW;DIP,SPST,8P,50VDC,1A,SMT,DHS	SW2
316664900001	PCB;PWA-5027/MOTHER BD	R02
291000011408	CON;HDR,MA,70P*2,.6MM,ST,SMT,AMP	J510
271071222302	RES;2.2K,1/16W,5%,0603,SMT	R220
271071753301	RES;75K,1/16W,5%,0603,SMT	R79,603

# 5027 N/B MAINTENANCE

## 11. SPARE PARTS LIST (4)

PART_NO	DESCRIPTION	LOCATION
286300809002	IC;MAX809,RESET CIRCUIT,2.9V,SOT	U51
271071683301	RES;68K ,1/16W,5% ,0603,SMT	R160
283766490003	IC;DRAM,256K*16,60NS,EDO,SOJ,502	U520-523
283666490001	IC;SRAM,32K*8,12NS,SOJ,28P,5027	U13
283666490002	IC;SRAM,64K*32,7NS,PQFP,100P,502	U5,12
273000130010	FERRITE CHIP;130OHM/100MHZ,1608,	EL28,29,30
271071102311	RES;102K ,1/16W,1% ,0603,SMT	R511
271071392301	RES;3.9K ,1/16W,5% ,0603,SMT	R551
271071562301	RES;5.6K ,1/16W,5% ,0603,SMT	R522
481664900001	F/W ASSY;SYS/VGA BIOS,5027	
283420402003	IC;FLASH,256K*8-120,5V,PLCC32,BT	U1
242600000158	LABEL;10*10,BLANK,COMMON,HI-TEMP	
481664900002	F/W ASSY;KBD CTRL,5027	
283305402001	IC;EPROM,32K*8,120NS,CMOS,PLCC,3	U11
242600000145	LABEL;10*10,BLANK,COMMON	
338736010002	BATTERY;NIMH,3.6V/70MAH,VARTA	J518
375102030010	NUT-HEX;M2,2,NIW	
370102011501	SPC-SCREW;M2L15,NIW,FLT(+),NL,73	
371102011502	SCREW;M2L15,FLT(+),NIW/NLK	
331170013602	CON;IC CARD,136P,CARDBUS,HIROSE	
331190602047	MINI JUMP;2P, 1,H6.5mm,OPEN	J6,14
411664900043	PWA;PWA-5027 V1 D/D BD	
312271006358	EC;100U,25V,RA,M,D6.3*7,SGX,SANY	C500,528
312271006152	EC;100U ,10V,M,RA,D6.3*9.8,OS-CO	C501,C502,C503,C506
312273306151	EC;330U ,6.3V,20%,RA,D10,W/OS-CO	C504,C521
312271006354	CAP;100U ,EL,20V ,20%,RA,W/OS-CO	C509
312273305354	EC;33U ,25V ,M,RA,D6.3*7,SGX,SA	C523
331030010011	CON;HDR,MA,10P*1,2MM,ST,GLD,H=13	J2
331130046001	CON;HDR,SHROUD,MA,23P*2,2.0MM,SU	J3
313000020078	CHOKE COIL;15UH,D.7*16T/2*32,55	T500

PART_NO	DESCRIPTION	LOCATION
411664900044	PWA;PWA-5027 V1 SMT D/D BD	
272073104501	CAP;1U ,25V,20%,0603,SMT	C1,2,13,22
272022106701	CAP;10U ,16V,+80-20%,1210,Y5V,S	C3,C524
272075103501	CAP;01U ,50V ,20%,0603,SMT	C8
272002105701	CAP;1U ,CR,16V ,-20+80%,0805,SM	C6,C522
272075104701	CAP;1U ,50V,+80-20%,0603,SMT	C7,C512,C515
272013105501	CAP;1U ,CR,25V ,+80-20%,1206,S	C11
272075102501	CAP;1000P,CR,50V ,20%,0603,SMT	C505
272075470701	CAP;47P ,50V ,+80-20%,0603,SMT	C24
288100202001	DIODE;DAN202K,80V,SWITCH,SMT	D1,D2,D5
288100032013	DIODE;BAS32L,VRRM75V,MELF,SOD-80	D3,D10,D11,D500
288100056001	DIODE;RLZ5.6B,ZENER,5.6V,5%,LL34	D4
288101004024	DIODE;EC10QS04,RECT,40V,1A,CHIP,	D7,8,9,501
295000010009	FUSE;NORMAL,5A/32VDC,3216,SMT	F1,F2,F500
273000010003	FERRITE CHIP;36OHM/100MHZ,4332	L500,L1
288227002001	TRANS;2N7002LT1,N-CHANNEL FET	Q1,Q2,Q4,Q5,Q7
288204435001	TRANS;SI4435DY,P-MOSFET,035OHM,	Q3,Q14
288200144001	TRANS;DTC144WK,NPN,SMT	Q6
288202222001	TRANS;MMBT2222AL,NPN,TO236AB	Q10,Q11,Q12,Q509
286300431004	IC;AIC431 ,5%,ADJ SHUNT REG,SOT-	Q501
288204410001	TRANS;SI4410DY,N-MOSFET,020OHM,S	Q502,503,15
271071103302	RES;10K ,1/16W,5% ,0603,SMT	R1,R9,R14
271071267211	RES;26.7K,1/16W,1% ,0603,SMT	R2,R16
271071000002	RES;0 ,1/16W,0603,SMT	R3,R54,R59,R61,R57
271071474301	RES;470K ,1/16W,5% ,0603,SMT	R4,R12,R17,R18,R32
271071301311	RES;301K ,1/16W,1% ,0603,SMT	R41,R517
271071104101	RES;100K ,1/16W,1% ,0603,SMT	R11
271071114101	RES;110K ,1/16W,1% ,0603,SMT	R28,R30
271071221301	RES;220 ,1/16W,5% ,0603,SMT	R7,R508
271071224301	RES;220K ,1/16W,5% ,0603,SMT	R8,505,R43

# 5027 N/B MAINTENANCE

## 11. SPARE PARTS LIST (5)

PART_NO	DESCRIPTION	LOCATION
271071226311	RES;226K ,1/16W,1% ,0603,SMT	R10
271071104302	RES;100K ,1/16W,5% ,0603,SMT	R44,R511
271071787311	RES;787K ,1/16W,1% ,0603,SMT	R15
271071105101	RES;1M ,1/16W,1% ,0603,SMT	R19,R24
271045107101	RES;.01 ,1W ,1% ,2512,SMT	R20,R27
271071392311	RES;392K ,1/16W,1% ,0603,SMT	R21,R39
271045257101	RES;.025 ,1W ,1% ,2512,SMT	R25
271071412211	RES;41.2K,1/16W,1% ,0603,SMT	R26,R34
271071204101	RES;200K ,1/16W,1% ,0603,SMT	R29,R48,R527
271071169311	RES;169K ,1/16W,1% ,0603,SMT	R31,R35,R507
271071499211	RES;49.9K,1/16W,1% ,0603,SMT	R37,R506,R518
271071473301	RES;47K ,1/16W,5% ,0603,SMT	R516,R38
271071124311	RES;124K ,1/16W,1% ,0603,SMT	R40,R50
271071499111	RES;4.99K,1/16W,1% ,0603,SMT	R51
271071203101	RES;20K ,1/16W,1% ,0603,SMT	R52
271071105301	RES;1M ,1/16W,5% ,0603,SMT	R502,R500
271071105301	RES;1M ,1/16W,5% ,0603,SMT	R502,500,58
271071123301	RES;12K ,1/16W,5% ,0603,SMT	R520,R503
271071287311	RES;287K ,1/16W,1% ,0603,SMT	R519,R514
271071100302	RES;10 ,1/16W,5% ,0603,SMT	R522,R526
271002100301	RES;10 ,1/10W,5% ,0805,SMT	R55
297120101005	SW;DIP,SPST,8P,50VDC, .1A,SMT,DHS	SW1
286300786001	IC;MAX786CAL,PWM CTRL,DUAL,SSOP,	U1
286100339002	IC;LP339,ULTRA-LOW PWR COMP.,SO,	U500,U2
286300798001	IC;MAX798ESE,PWM CTRL,SO,16P	U3
286317812001	IC;HA178L12UA,VOLT REGULATOR,SC-	U4
316664900012	PCB;PWA-5027/DD BD	R01C
272075101701	CAP;100P ,50V ,+80-20%,0603,SMT	C9,10
271071205301	RES;2M ,1/16W,5% ,0603,SMT	R528,R60
328101002001	DIODE;HRW1002A,10A,20V,TO-220AB	D502

PART_NO	DESCRIPTION	LOCATION
411664900008	PWA;PWA-5027 EXT U-PHONE BD	
316664900014	PCB;PWA-5027/EXT. PHONE BD	R00
331030004005	CON;HDR,MA,2P*2,2MM,ST	J1
331840005006	CON;STEREO JACK,5P,R/A,W9.1,MOJB	J501
411664900022	PWA;PWA-5027 DIMM DAUGHTER	
316664900010	PCB;PWA-5027/DIMM DAUGHTER BD	R02
272072104702	CAP;.1U ,16V,+80-20%,0603,SMT	C500-505,507-509
291000621443	DIMM SOCKET;144P, 8MM,H=4MM,SMT	J2,J501
291000011408	CON;HDR,MA,70P*2, 6MM,ST,SMT,AMP	
421664900001	WIRE ASSY;COVER SWITCH,5027	
421664900011	MICROPHONE ASSY;5027	
442664900001	AC ADPT ASSY;5027	
441664900021	EXT BOX ASSY;5027	
411664900047	PWA;PWA-5027 EXT BOX BD	
316664900032	PCB;PWA-5027/AD-TRANS BD	R00
344664900059	STANDOFF;ADAPTER CONNECTOR,5027	
331910003003	CON;POWER JACK,3P,16VDC/3A	J1
331030010006	CON;HDR,FM,10P*1,2.0MM,ST,GLD	J2
344664900053	TOP COVER;EXT BOX,5027	
344664900054	HOUSING;EXT BOX,5027	
344664900052	HOOK;EXT BOX,ADA,5027	
341664700007	SPRING;SLIDE,BTM CASE,5026	
344664900081	BUTTON;EXT BOX,5027	
370102010502	SPC-SCREW;M2 L5,NIB,K-HD,727	
441664900031	TOUCH PAD ASSY;5027	
411664900013	PWA;PWA-5027 TOUCH PAD BD	
316664900019	PCB;PWA-5027/TOUCH PAD BD	R02
291000150401	CON;FPC/FFC,4P,1MM,R/A,SMT	J1
297040101003	SW;PUSH BUTTON,SPST, .1A,30V,2P,S	SW1,2
442110500005	TOUCH PAD MODULE;904236-0000,502	

# 5027 N/B MAINTENANCE

## 11. SPARE PARTS LIST (6)

PART_NO	DESCRIPTION	LOCATION
33230000111	CABLE;FFC,8P,T/P TO M/B,80MM,502	
441664900041	2ND BATT BD ASSY;5027	
344664900029	HOUSING;EXT,BATT,5027	
411664900048	PWA;PWA-5027 2ND BATTERY BD	
316664900015	PCB;PWA-5027/2ND BATTERY BD	R02
331030010014	CON;HDR,MA,10P*1,2MM,ST,BATT PLA	
451664900031	HOUSING KIT;5027	
344664900001	TOP CASE;5027	
341664900002	PLATE SHIELDING;TOP,5027	
344664900009	KNOB;TOUCH-PAD,5027	
344664900064	BRACKET;T/P SW,5027	
343664900001	BRACKET;I/O,5027	
340664900009	SHIELD ASSY;CD ROM-MB,5027	
340664900012	BOTTOM CASE ASSY;5027	
344664900031	LOCK;BATTERY,5027	
341664900012	SPRING;LOCK BATT,5027	
344664900032	LATCH;BATTERY,5027	
344664900015	KNOB;HDD/FDD/CD-ROM,5027	
344664900016	LOCK;HDD/FDD/CD-ROM,5027	
341664900009	SPRING;HDD/FDD/CD-ROM,5027	
345664900006	FOOT-PAD;5027	
340664900021	KEYBOARD COVER ASSY;5027	
344664900030	LOCK;BATTERY,EXT,5027	
344664900033	KNOB;BATTERY,EXT,5027	
344664900005	DOOR;COVER I/O,5027	
344664900006	DOOR COVER;DOCKING,5027	
344664900008	LENS;I/R,5027	
344664900038	COVER HINGE (R);5027	
344664900039	COVER HINGE (L);5027	
344664900040	CABLE COVER,5027	

PART_NO	DESCRIPTION	LOCATION
344664900060	COVER;PCMCIA,5027	
341664900013	SPRING;PCMCIA,5027	
343664900007	AIR FIN;5027	
451664900041	HEATSINK ASSY;CPU,5027	
343664900005	HEATSINK;TCP,5027	
345664900010	GAP PAD;PPGA UP SIDE,5027	
371102011002	SCREW;M2L10,PAN(+),NIW/NLK	
377102011130	S-STANDOFF;M2DP4H1.3L8.5,NIW	
421664900021	SPEAKER ASSY;5027	
371102510601	SCREW;M2.5L6,PAN(+),NIW/NLK	
370102010602	SPC-SCREW;M2L6,NIW,K-HD,NL,731	
371102010503	SCREW;M2.5L5,FLT(+),NIW	
370102011002	SPC-SCREW;M2L10,NIW,K-HD,731	
370102010401	SPC-SCREW;M2L4,NIW,FLT(+),NL,731	
344664900073	PLUG;FAX/MODEM,5027	
343664900015	SHIELDING;HINGE/HEATSINK,5027	
343664900014	SHIELDING;FAX/AUDIO,5027	
343664900012	SHIELDING;DC-IN,5027	
343664900013	SHIELDING;K/B-LVDS,5027	
343664900010	SHIELDING;AUDIO,5027	
343664900009	SHIELDING;AUDIO*2,5027	
341664900026	CLIP;LCD CABLE,HEATSINK,5027	
340664900023	SHIELDING ASSY;DC-DC/UP,5027	
345664900012	GASKET;UC-3E0433,FDD/HEATSINK,50	
340664900013	CPU COVER ASSY;5027	
344664900080	INSULATOR;TV-OUT,5027	
371102010603	SCREW;M2L6,PAN(+),NIW/NLK	
371102010401	SCREW;M2L4,PAN(+),NIW/NLK	
370102010402	SPC-SCREW;M2L4,NIW,K-HD(+),731	
451664900071	HDD ME KIT;5027	

# 5027 N/B MAINTENANCE

## 11. SPARE PARTS LIST (7)

PART_NO	DESCRIPTION	LOCATION
344664900017	BEZEL;HDD,5027	
341664900004	BRACKET;HDD,5027	
342664900003	SHIELDING;HDD,5027	
344664900057	COVER;HDD,5027	
370103010603	SPC-SCREW;M3L4,K-HEAD(+),NIW	
370102010502	SPC-SCREW;M2 L5,NIB,K-HD,727	
346664900002	INSULATOR;HDD,5027	
421664900034	FPC ASSY;HDD,5027	
371102010402	SCREW;M2L4,PAN(+),NIW	
523466490001	FDD ASSY;1.44M,3.5",5027	
523410290015	FD DRIVE;1.44M,3 MODE,FD-05HG-56	
344664900018	FRAME;FDD,TEAC,5027	
341664900007	BRACKET;FDD,5027	
341664900005	SHIELDING;FDD,5027	
344664900058	COVER;FDD,5027	
370102510302	SPC-SCREW;M2.5L3,NIB,K-HD,727	
371102010402	SCREW;M2L4,PAN(+),NIW	
346664900001	INSULATOR;FDD,5027	
421664900032	FPC ASSY;FDD,5027	
441664900051	LCD ASSY;X/T,MIT,14.2",5027	
413000020084	LCD;AA142XB01,TFT,14.2",XGA	
412664900002	PCB ASSY;5027,INVERTER BD	
451664900001	LCD ME KIT;X/T 14.2 MIT,5027	
340664900016	HOUSING ASSY;LCD142,5027	
340664900017	BEZEL ASSY;LCD142,5027	
344664900046	LATCH;LCD 14.2",5027	
344664900056	HOOK;LCD14.2",5027	
341664900021	SPRING;LCD,5027	
340664900004	HINGE (R);LCD 14.2",5027	
340664900005	HINGE (L);LCD 14.2",5027	

PART_NO	DESCRIPTION	LOCATION
345664900005	RUBBER PAD;UPSIDE,LCD142,5027	
345664900002	RUBBER PAD;DOWNSIDE,LCD,5027	
371102010603	SCREW;M2L6,PAN(+),NIW/NLK	
371102510602	SCREW;M2.5L6,FLNG(+),NIW/NLK	
421664900056	CABLE ASSY;INVERTER/MB,LCD142,50	
421664900059	CABLE ASSY;LCD/INVERTER,MIT142,5	
421664900051	CABLE ASSY;LCD/MB,MITS14.2,5027	
345664900013	CUSHION-1;LCD,MITS142,5027	
345664900014	CUSHION-2;LCD,MITS142,5027	
346664900006	INSULATOR;INVERTER,MITS142,5027	
341664900025	CLIP;LCD CABLE,PANEL,5027	
371102010503	SCREW;M2.5L5,FLT(+),NIW	
371102510601	SCREW;M2.5L6,PAN(+),NIW/NLK	
371102010401	SCREW;M2L4,PAN(+),NIW/NLK	
411664900017	PWA;PWA-5027 LVDS 14.2" TRANS BD	
316664900009	PCB;PWA-5027/LVDS TRANS/MITSUBIS	R04
272075103702	CAP;.01U ,50V,+80-20%,0603,SMT	EC515,516,518,520
272072104702	CAP;.1U ,16V,+80-20%,0603,SMT	EC2
272401226502	CAP;22U ,TT,10V ,20%,6032,SMT	C1
291000012101	CON;HDR,MA,21P,0.625MM,ST,SMT	J1
291000016005	CON;HDR,MA,30P*2 ,6MM,ST,SMT	J501
272075101701	CAP;100P ,50V ,+80-20%,0603,SMT	EC3,8-29,519,525
271071000002	RES;0 ,1/16W,0603,SMT	R4,5,6,8,502
271012000301	RES;0 ,1/8W,5% ,1206,SMT	R2
284590561001	IC;DS90CF561,LVDS/LCD,18BIT,SSOP	U501,502
272073180401	CAP;18P ,CR,25V ,10%,0603,NPO,S	EC501
272075102402	CAP;1000P,CR,50V,10%,0603,X7R,IN	EC510,511
273000150002	FERRIET CHIP;120OHM/100MHZ,2012,	EL1,2
273000130010	FERRITE CHIP;130OHM/100MHZ,1608,	EL501,R7,R501
271002000301	RES;0 ,1/10W,5% ,0805,SMT	R3

# 5027 N/B MAINTENANCE

## 11. SPARE PARTS LIST (8)

PART_NO	DESCRIPTION	LOCATION
271611221301	RP;220*4 ,8P ,1/16W,5% ,0612,SMT	RP1,2,501,502
341664900019	SHIELDING;LVDS,5027	
461664900001	PACKING KIT;5027	
227664900001	END CAP;5027	
222664920001	PE BAG;340*475,T0.08,5027	
221664920003	CARTON;INNER AK,5027	
221664920001	CARTON;PC,5027	
222664920002	PE BUBBLE BAG;200*350,BATTERY,50	
222600020009	PE BUBBLE BAG;10"*8",COMMON	
221664950001	PARTITION;AK,5027	
451664900051	LABEL KIT;MITAC,5027	
343664900006	NAMEPLATE;5027	
242664900004	LABEL;AGENCY-GLOBAL,5027	
441999900006	BATT ASSY OPTION;NIMH,5027	
441664900001	BATT ASSY;9.6V/4AH,NIMH,SANYO,50	
242664900002	LABEL;BATTASSY,9.6V/4AH,SYO,5027	
310131103002	CFM-BAT;NTCR,10K,ISUZU,103AT-2	
316664900024	PCB;PWA-5027/BATT CONN. BD	
331030010006	CON;HDR,FM,10P*1,2.0MM,ST,GLD	
335152000020	CFM-BAT;THERMAL BREAKER,ISUZU,IP	
335152000021	CFM-BAT;FUSE,THERMAL,ELMWOOD,D09	
335512000001	POLYSWITCH;3.5A,SRP350	
338712010011	BATTERY;NIMH,1.2V/4AH,D18,SANYO	
344664900024	TOP CASE;BATT,NI-MH,5027	
340664900011	BOTTOM CASE BATT ASSY;5027	
411664900029	PWA;PWA-5027 NIMH BATT VIEW BD	
272003104701	CAP;.1U ,CR,25V ,+80-20%,0805,Y	C1,C2,C3,C4
294011200004	LED;YE/GR,H1.1,L2,W1.25,CL170YG,	D1,D2,D3,D4
288100032013	DIODE;BAS32L,VRRM75V,MELF,SOD-80	D5,D6,D8,D9
288100056001	DIODE;RLZ5.6B,ZENER,5.6V,5%,LL34	D7

PART_NO	DESCRIPTION	LOCATION
331040010003	CON;HDR,MA,10P*1,2MM,R/A,20010A1	J501
288202222001	TRANS;MMBT2222AL,NPN,TO236AB	Q1
271002204301	RES;200K ,1/10W,5% ,0805,SMT	R1,R15
271002101301	RES;100 ,1/10W,5% ,0805,SMT	R8,R2
271002471301	RES;470 ,1/10W,5% ,0805,SMT	R4,R5,R6,R7
271002104101	RES;100K ,1/10W,1% ,0805,SMT	R10
271002104301	RES;100K ,1/10W,5% ,0805,SMT	R3
271002698311	RES;698K ,1/10W,1% ,0805,SMT	R9
271002102301	RES;1K ,1/10W,5% ,0805,SMT	R11
271002103301	RES;10K ,1/10W,5% ,0805,SMT	R16,R12
271045507101	RES;.05 ,1W ,1% ,2512,SMT	R14,R13
297040105002	SW;PUSH BUTTON,SPST,12V/50MA,4P,	SW1
481664900003	F/W ASSY;24C02,SMART BATTERY,502	U1
283400900003	IC;EEPROM,256*8,S24C02A,SO,8P,SM	
286002092001	IC;BQ2092SN,GAS GAUGE,SMBUS,SO,1	U2
316664900023	PCB;PWA-5027/BATT VIEW BD	R00C
242664900005	LABEL;BATTERY,CAUTION,5027	
343664900006	NAMEPLATE;5027	