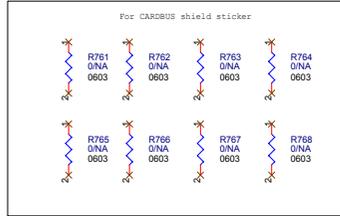


7068T Schematic R01

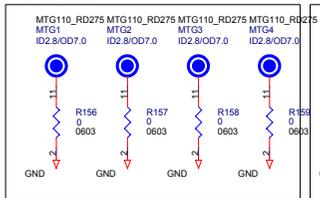
PAGE01 TITLE
 PAGE02 FC-PGA CPU (1/2)
 PAGE03 FC-PGA CPU (2/2)
 PAGE04 NB(1)-VGA AND HOST IF
 PAGE05 NB(2)-MEMORY AND PCI IF
 PAGE06 CLOCK - ICS950602
 PAGE07 SODIMM
 PAGE08 LCD CONNECTOR/CRT
 PAGE09 SB_VT8231(1)-PCI/USB/PIO/SIO IF
 PAGE10 SB_VT8231(2)-AC97/IDE/CPU/POWER MANAGEMENT
 PAGE11 SB_VT8231(3)-ISA/LAN IF
 PAGE12 HDD/CDROM CONNECTOR
 PAGE13 MINI-PCI/MDC
 PAGE14 PCMCIA CONTROLLER AND SLOT
 PAGE15 IEEE1394-UPD72872
 PAGE16 AUDIO CODEC
 PAGE17 AUDIO AMPLIFIER
 PAGE18 H8
 PAGE19 LED/TOUCH_PAD
 PAGE20 LAN PHY/TRANSFORMER AND IR MODULE/BIOS
 PAGE21 PULL UP
 PAGE22 PERIPHERAL CIRCUIT
 PAGE23 CPU CORE/VTT/2.5V
 PAGE24 +1.5V/+3V/+5V/+12V
 PAGE25 GEYSERVILLE CONTROLLER
 PAGE26 FOR 7X68 80 PIN

PCI DEVICE	INTERRUPT	REQ/GNT	IDSEL
MINI-PCI	PCINTB#	REQ2#/GNT2#	AD21
IEEE1394	PCINTC#	REQ3#/GNT3#	AD22
TI1410	PCINTB#	REQ0#/GNT0#	AD19

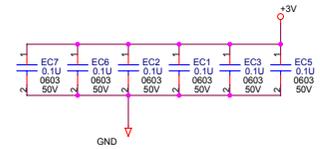
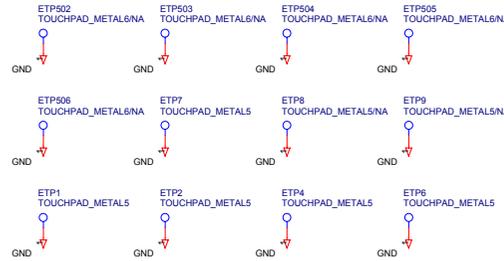
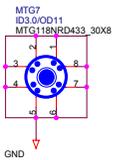
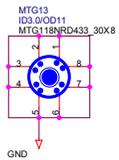
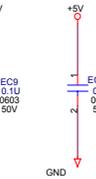
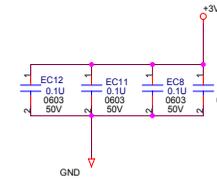
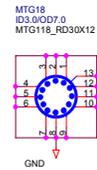
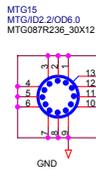
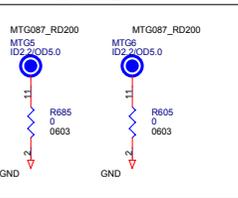
REVISION	TAPEOUT DAY	HISTORY
R0A	91/1/23	DESIGN FOR DVT
R0B		1. Add CPU Vcore Switch(P.3) 2. CPU Clock Change Auto select(P.6) 3. Add Black Light Enable Control(P.5)
R01	91/07/02	1. FOLLOW INTEL RES SPEC(P2,P25) 2.V-CORE ADD CAP(P3) 3.ADD C81 FOR NB SKEW(P4) 4.VTT ADD CAP FOR NB(P4) 5.PICCLK CHANGE TO 2V (P2,P6) 6.CPU POWER GOOD CHANGE TO 1.8V(P22) 7. ADD PR514,DEL PD501,PQ501 FOR V-CORE NOISE(P23)



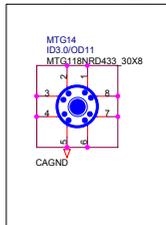
FOR CPU



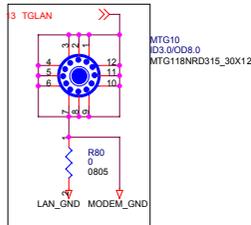
FOR MDC



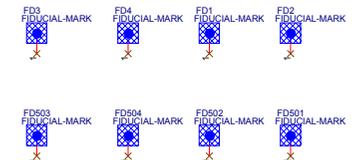
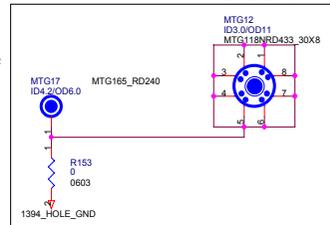
FOR AUDIO



FOR LAN



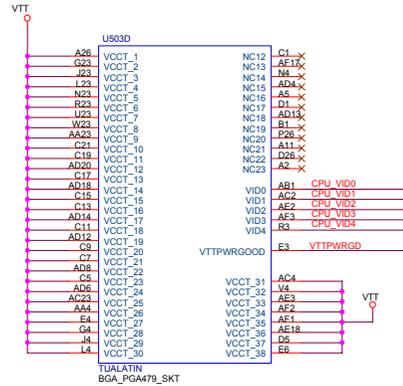
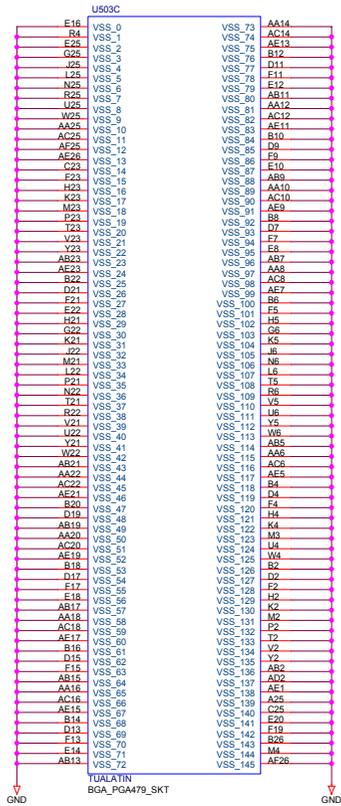
FOR 1394



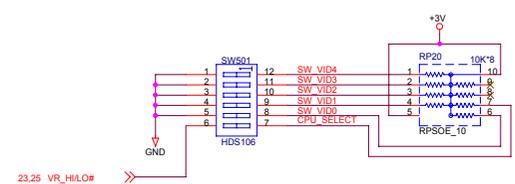
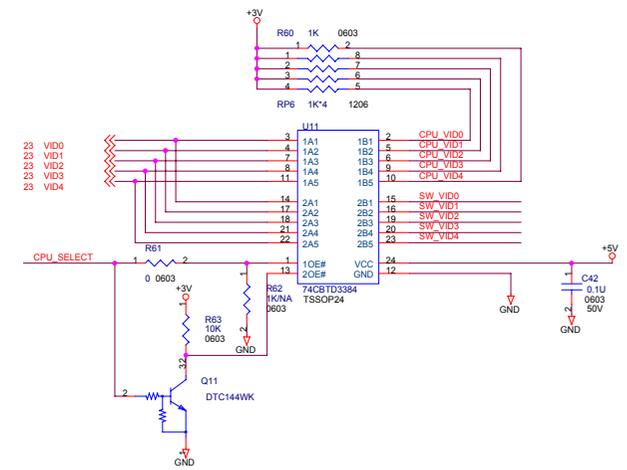
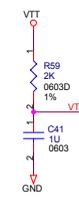
DRAWN	DESIGN	CHECK	ISSUES

MITAC	
Title: 7068T M/D B/D	
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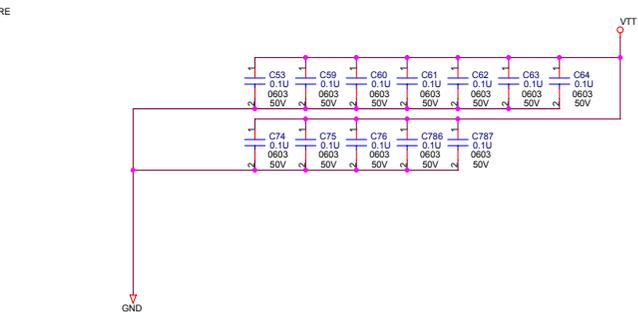
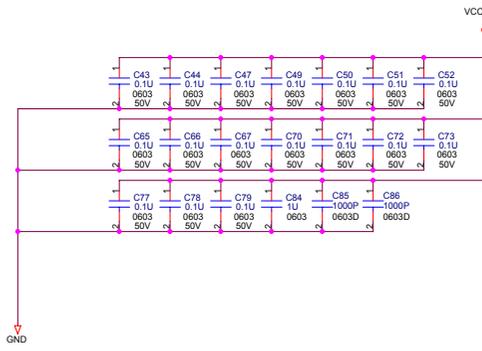
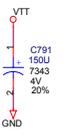
CPU(2)



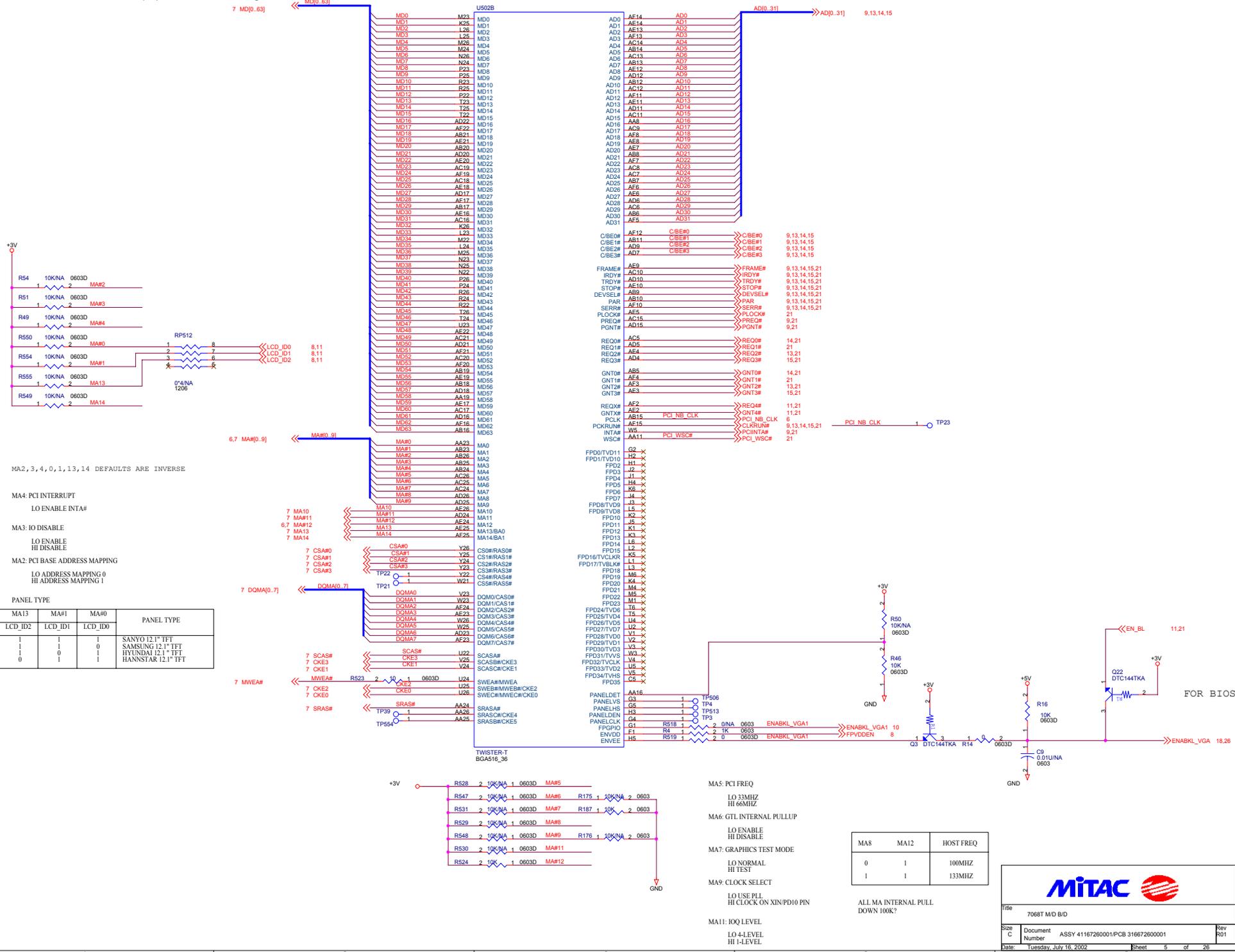
VID4	VID3	VID2	VID1	VID0	VOLT.
0	0	0	0	0	1.75
0	0	0	0	1	1.70
0	0	0	0	1	1.65
0	0	0	1	1	1.60
0	0	1	0	0	1.55
0	0	1	0	1	1.50
0	0	1	1	0	1.45
0	0	1	1	1	1.40
0	1	0	0	0	1.35
0	1	0	0	1	1.30
0	1	0	1	0	1.25
0	1	0	1	1	1.200
0	1	1	0	0	1.15
0	1	1	0	1	1.100
0	1	1	1	0	1.050
0	1	1	1	1	1.000
1	0	0	0	0	0.975
1	0	0	0	1	0.950
1	0	0	1	0	0.925
1	0	0	1	1	0.9
1	0	1	0	0	0.875
1	0	1	0	1	0.85
1	0	1	1	0	0.825
1	0	1	1	1	0.8
1	1	0	0	0	0.775
1	1	0	0	1	0.75
1	1	0	1	0	0.725
1	1	0	1	1	0.7
1	1	1	0	0	0.675
1	1	1	0	1	0.65
1	1	1	1	0	0.625
1	1	1	1	1	0.6



VID : SWITCH
 1 : Pull High(OFF)
 0 : Pull Low(ON)
 CPU_SELECT(ON : Intel; OFF : C3)



TWISTER (2)- Memory and PCI Interface



MA2, 3, 4, 0, 1, 13, 14 DEFAULTS ARE INVERSE

MA4: PCI INTERRUPT
LO ENABLE INTA#

MA3: IO DISABLE
LO ENABLE HI DISABLE

MA2: PCI BASE ADDRESS MAPPING
LO ADDRESS MAPPING 0 HI ADDRESS MAPPING 1

PANEL TYPE

LCD_ID2	LCD_ID1	LCD_ID0	PANEL TYPE
1	1	1	SANYO 12.1" TFT
1	1	0	SAMSUNG 12.1" TFT
1	0	1	HYUNDAI 12.1" TFT
0	1	1	HANNSTAR 12.1" TFT

MA5: PCI FREQ
LO 33MHZ
HI 66MHZ

MA6: GTL INTERNAL PULLUP
LO ENABLE HI DISABLE

MA7: GRAPHICS TEST MODE
LO NORMAL HI TEST

MA9: CLOCK SELECT
LO USE PLL HI CLOCK ON XIN/PD10 PIN

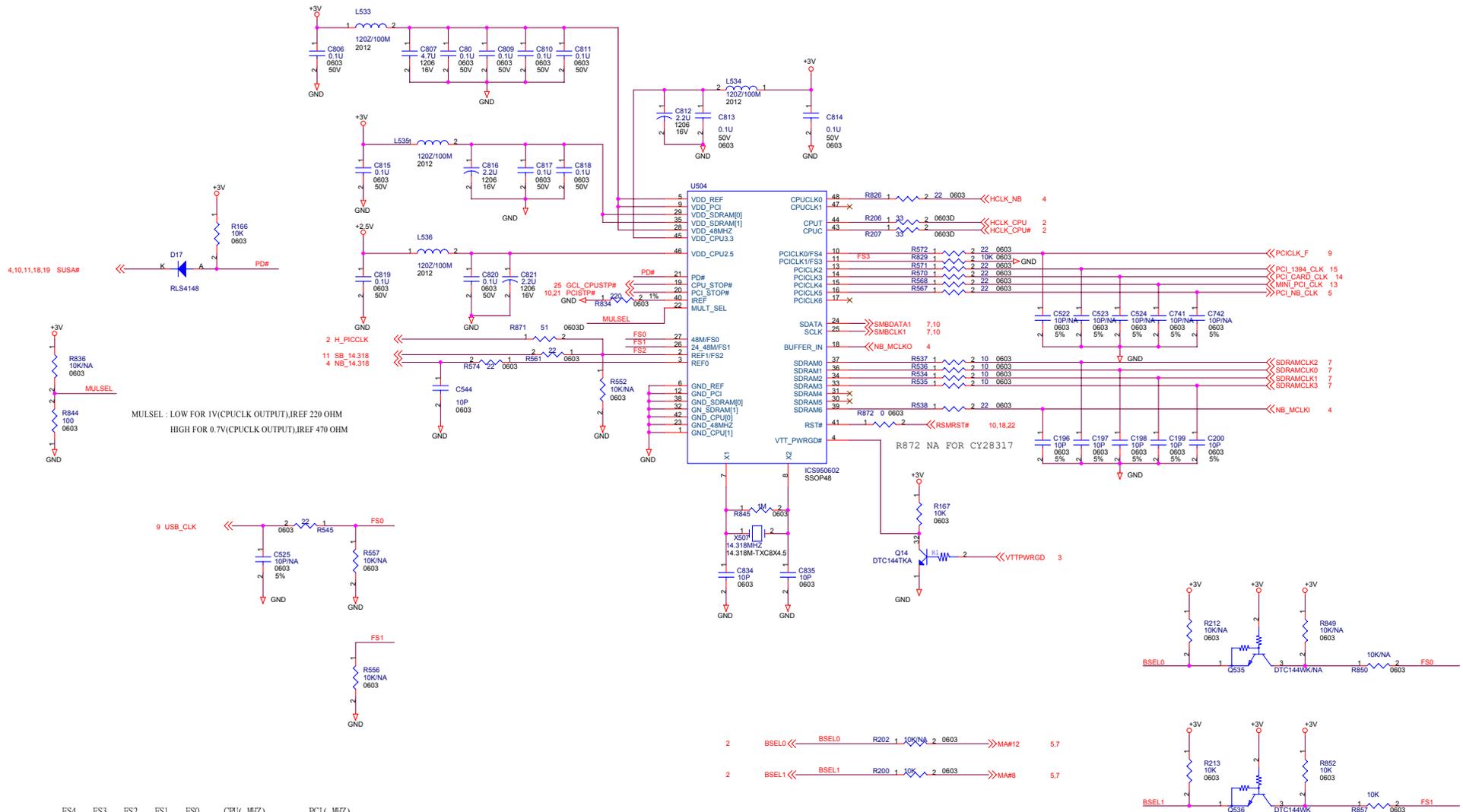
MA11: IOQ LEVEL
LO 4-LEVEL HI 1-LEVEL

MA8	MA12	HOST FREQ
0	1	100MHZ
1	1	133MHZ

ALL MA INTERNAL PULL DOWN 100K?

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CLOCK SYNTHESISER- ICS950602/CY28317



MULSEL : LOW FOR 1V(CPUCLK OUTPUT), IREF 220 OHM
HIGH FOR 0.7V(CPUCLK OUTPUT), IREF 470 OHM

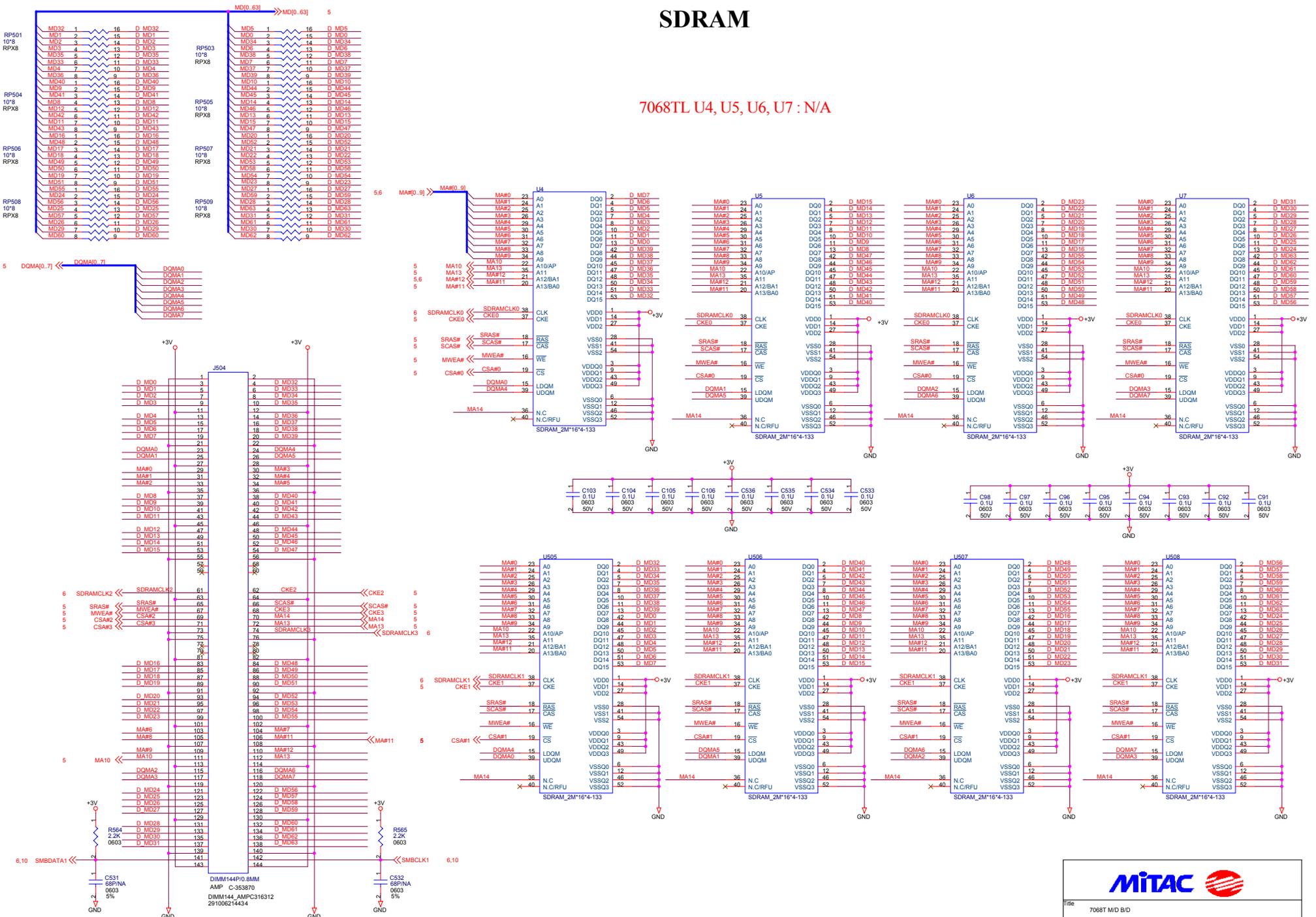
FS4	FS3	FS2	FS1	FS0	CPU(MHz)	PCI(MHz)
1	0	1	0	1	100.00	33.33
1	0	1	1	1	133.33	33.33

FS0, FS1, FS2, FS3, FS4 INTERNAL PULL UP

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 Date: Tuesday, July 16, 2002
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SDRAM

7068TL U4, U5, U6, U7 : N/A



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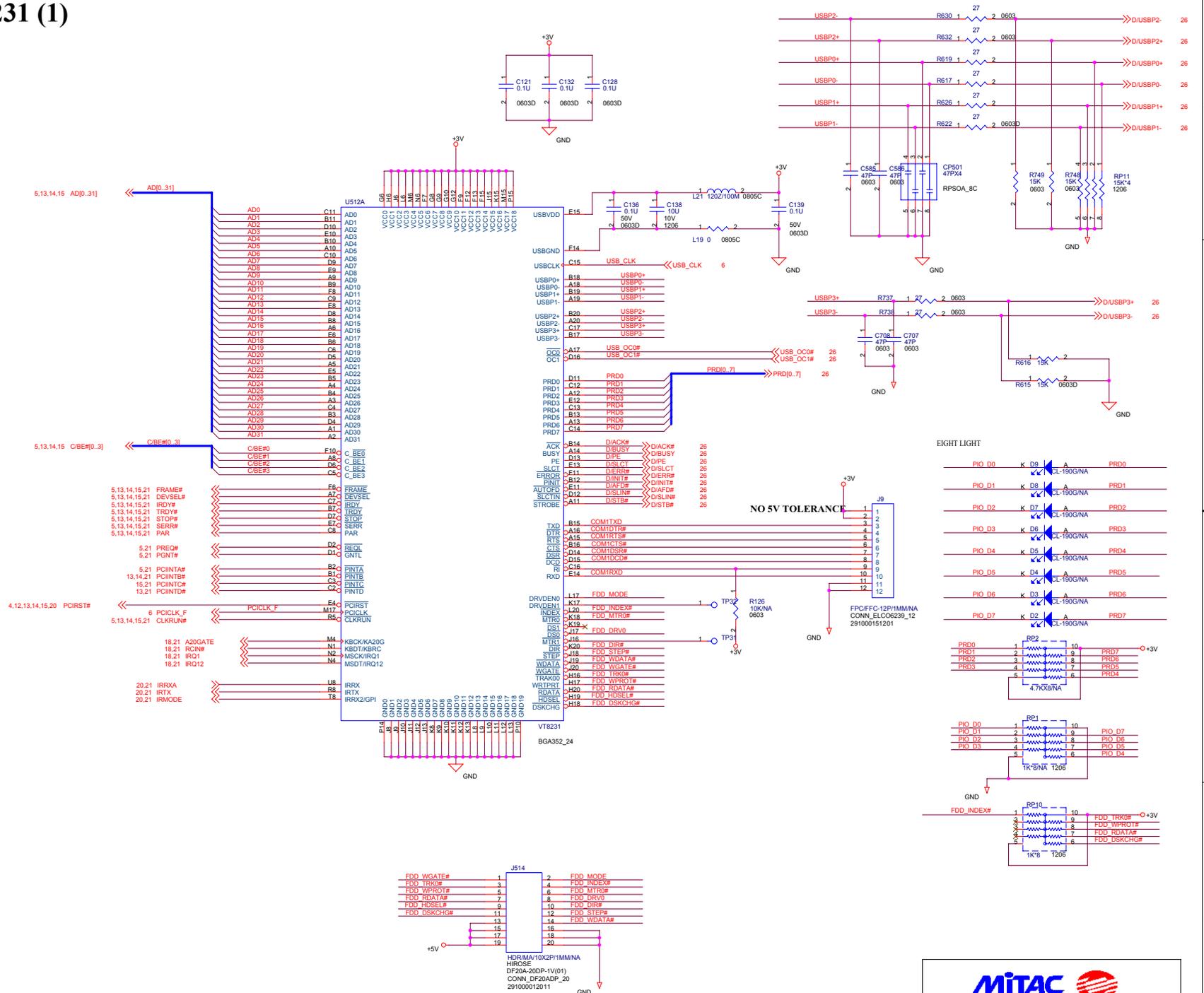
File: 7068T M/D B/D

Size C Document ASSY 41167260001/PCB 31667260001 Rev R01

Number

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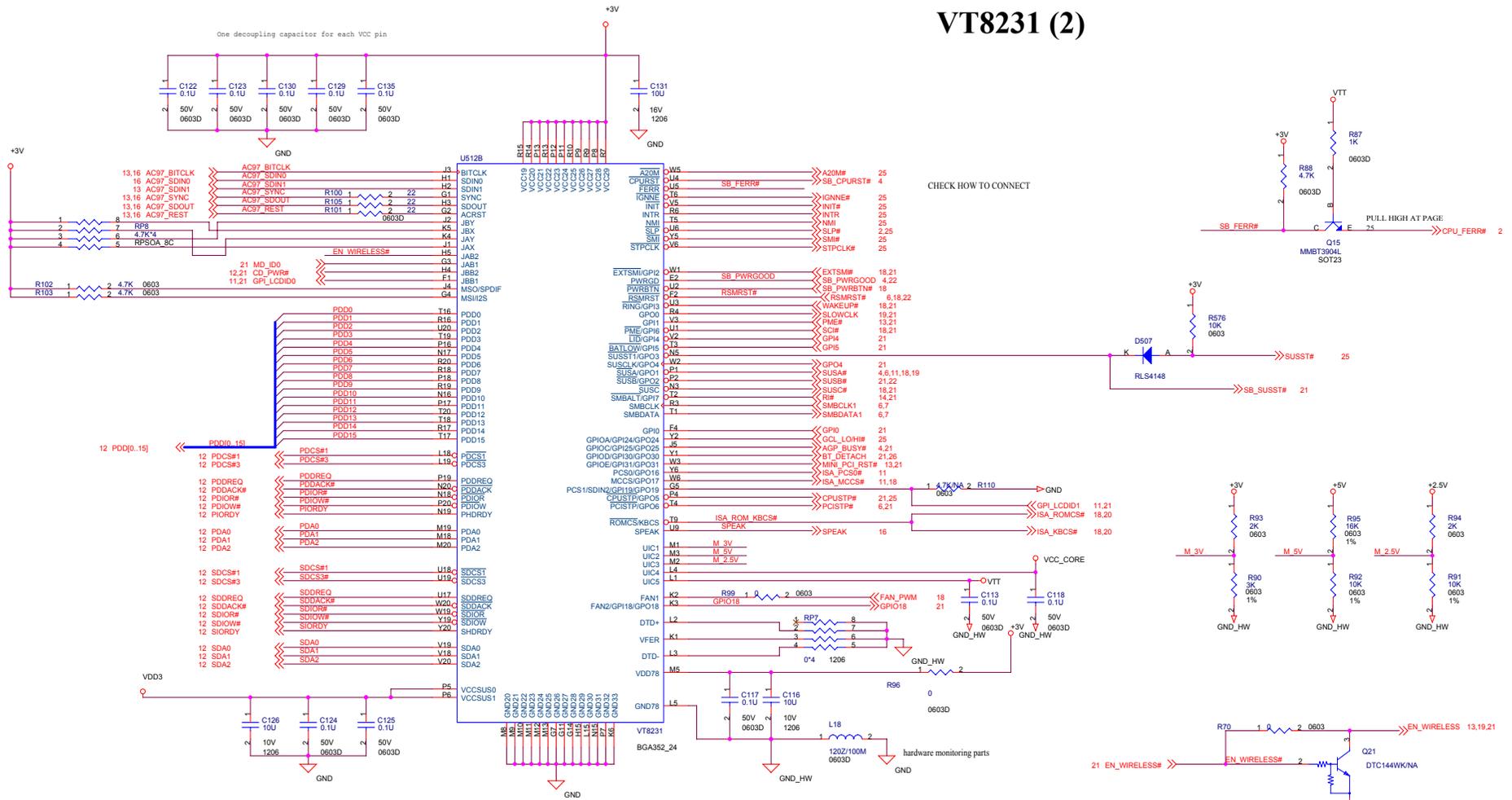
VT8231 (1)



MITAC

Title 7068T M/D B/D		
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VT8231 (2)



DVT GPIO DEFINITION

PIN#	FUNCTION	POWER	PIN#	FUNCTION	POWER	PIN#	FUNCTION	POWER
F4	GPIO0:	RESERVE#	R4	GP00:	SLOWCLK	K3	GPIO18	RESERVE#
V3	GPIO1:	RESERVE#	P1	GP01:	SUS4#	G5	GPIO19	MAIN
W1	GPIO2:	EXTSMI#	P2	GP02:	SUSB#	W13	GPIO20	MAIN
U3	GPIO3:	WAKEUP#	N5	GP03:	SUSIF#	Y13	GPIO21	MAIN
V2	GPIO4:	RESERVE#	W2	GP04:	RESERVE/SUSCLK	U7	GPIO22	MAIN
T3	GPIO5:	RESERVE#	P4	GP05:	CPUSTP#	T7	GPIO23	MAIN
U1	GPIO6:	SCIF	T4	GP06:	PCISTP#	Y2	GPIO24	(GPIOA)
T2	GPIO7:	RESERVE#	U6	GP07:	SLP#	J5	GPIO25	(GPIOC)
F3	GPIO8:	RESERVE#	W11	GP08:	HDD_RST	R2	GPIO26	MAIN
Y3	GPIO9:	MPCIACT#	T10	GP09:	CDROM_RST	R1	GPIO27	MAIN
Y11	GPIO10:	CANNOT USE	Y10	GP10:	CARD_SUS#	Y1	GPIO30	MAIN
V11	GPIO11:	CANNOT USE	V10	GP11:	IR_MODE#	W3	GPIO31	(GPIOE)
U10	GPIO12:	CANNOT USE	H5	GP12:	EN_WIRELESS			
W10	GPIO13:	CANNOT USE	H4	GP13:	CD_PWR#			
V4	GPIO14:	MD_IDI	R8	GP14:	IRTX			
Y8	GPIO15:	BT_WAKEUP	U8	GP15:	IRRXA			
V1	GPIO16:	CARD_IN	V6	GP16:	ISA_PCS0#			
P3	GPIO17:	THRM#	W6	GP17:	ISA_MCCS#			
G3	GPIO28:	MD_ID0	V4	GP28:	EN_BL			
F1	GPIO29:	GPIO_LCIDID0	Y4	GP29:	HDD_PWR#			

5 ENABKL_VGA1 << R199 1 0NA 2 0603 GPIO18

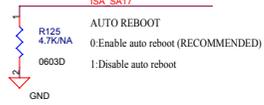
File: 7068T M/D B/D

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VT8231 (3)

POWER-UP STRAPPING

IT HAS PULL HIGH



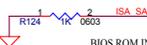
CPURST/INIT POLARITY

H: SLOT-1/SOCKET-370/SLOT-A/SOCKET-462
L: SOCKET-7



CPU FREQ STRAPPING

H: DISABLE
L: ENABLE

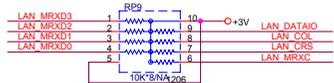


BIOS ROM INTERFACE

H: LPC
L: CONVENTIONAL



ISA DATA BUS RANGE
HI 16BITS
LO 8BITS



12,18,20,21 SDD[0..15] >> SDD[0..15]

SDD0	ISA SA0
SDD1	ISA SA1
SDD2	ISA SA2
SDD3	ISA SA3
SDD4	ISA SA4
SDD5	ISA SA5
SDD6	ISA SA6
SDD7	ISA SA7
SDD8	ISA SA8
SDD9	ISA SA9
SDD10	ISA SA10
SDD11	ISA SA11
SDD12	ISA SA12
SDD13	ISA SA13
SDD14	ISA SA14
SDD15	ISA SA15

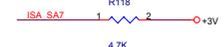
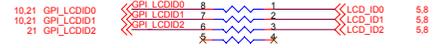
12,18,20,21 ISA_SA[0..17] << ISA SA[0..17]

ISA SA0	Y18	SA0/SDD0
ISA SA1	Y17	SA1/SDD1
ISA SA2	Y16	SA2/SDD2
ISA SA3	Y15	SA3/SDD3
ISA SA4	Y14	SA4/SDD4
ISA SA5	Y13	SA5/SDD5
ISA SA6	Y12	SA6/SDD6
ISA SA7	Y11	SA7/SDD7
ISA SA8	Y10	SA8/SDD8
ISA SA9	Y9	SA9/SDD9
ISA SA10	Y8	SA10/SDD10
ISA SA11	Y7	SA11/SDD11
ISA SA12	Y6	SA12/SDD12
ISA SA13	Y5	SA13/SDD13
ISA SA14	Y4	SA14/SDD14
ISA SA15	Y3	SA15/SDD15
ISA SA16	Y2	SA16
ISA SA17	Y1	SA17
ISA SA18	U13	SA18
ISA SA19	U13	SA19
ISA SA20	U13	SA20
ISA SA21	U13	SA21
ISA SA22	U13	SA22
ISA SA23	U13	SA23
ISA SA24	U13	SA24
ISA SA25	U13	SA25
ISA SA26	U13	SA26
ISA SA27	U13	SA27
ISA SA28	U13	SA28
ISA SA29	U13	SA29
ISA SA30	U13	SA30
ISA SA31	U13	SA31
ISA SA32	U13	SA32
ISA SA33	U13	SA33
ISA SA34	U13	SA34
ISA SA35	U13	SA35
ISA SA36	U13	SA36
ISA SA37	U13	SA37
ISA SA38	U13	SA38
ISA SA39	U13	SA39
ISA SA40	U13	SA40
ISA SA41	U13	SA41
ISA SA42	U13	SA42
ISA SA43	U13	SA43
ISA SA44	U13	SA44
ISA SA45	U13	SA45
ISA SA46	U13	SA46
ISA SA47	U13	SA47
ISA SA48	U13	SA48
ISA SA49	U13	SA49
ISA SA50	U13	SA50
ISA SA51	U13	SA51
ISA SA52	U13	SA52
ISA SA53	U13	SA53
ISA SA54	U13	SA54
ISA SA55	U13	SA55
ISA SA56	U13	SA56
ISA SA57	U13	SA57
ISA SA58	U13	SA58
ISA SA59	U13	SA59
ISA SA60	U13	SA60
ISA SA61	U13	SA61
ISA SA62	U13	SA62
ISA SA63	U13	SA63
ISA SA64	U13	SA64
ISA SA65	U13	SA65
ISA SA66	U13	SA66
ISA SA67	U13	SA67
ISA SA68	U13	SA68
ISA SA69	U13	SA69
ISA SA70	U13	SA70
ISA SA71	U13	SA71
ISA SA72	U13	SA72
ISA SA73	U13	SA73
ISA SA74	U13	SA74
ISA SA75	U13	SA75
ISA SA76	U13	SA76
ISA SA77	U13	SA77
ISA SA78	U13	SA78
ISA SA79	U13	SA79
ISA SA80	U13	SA80
ISA SA81	U13	SA81
ISA SA82	U13	SA82
ISA SA83	U13	SA83
ISA SA84	U13	SA84
ISA SA85	U13	SA85
ISA SA86	U13	SA86
ISA SA87	U13	SA87
ISA SA88	U13	SA88
ISA SA89	U13	SA89
ISA SA90	U13	SA90
ISA SA91	U13	SA91
ISA SA92	U13	SA92
ISA SA93	U13	SA93
ISA SA94	U13	SA94
ISA SA95	U13	SA95
ISA SA96	U13	SA96
ISA SA97	U13	SA97
ISA SA98	U13	SA98
ISA SA99	U13	SA99
ISA SA100	U13	SA100

ISA_SDD[0..7] >> ISA_SDD[0..7] 18,20,21

SDD0	ISA SDD0
SDD1	ISA SDD1
SDD2	ISA SDD2
SDD3	ISA SDD3
SDD4	ISA SDD4
SDD5	ISA SDD5
SDD6	ISA SDD6
SDD7	ISA SDD7
SDD8	ISA SDD8
SDD9	ISA SDD9
SDD10	ISA SDD10
SDD11	ISA SDD11
SDD12	ISA SDD12
SDD13	ISA SDD13
SDD14	ISA SDD14
SDD15	ISA SDD15

REQ#	REQ#	5,21
GNT#	GNT#	5,21
LAN CRS	LAN CRS	20
LAN COL	LAN COL	20
LAN MTXE	LAN MTXE	20
LAN MTXD0	LAN MTXD0	20
LAN MTXD1	LAN MTXD1	20
LAN MTXD2	LAN MTXD2	20
LAN MTXD3	LAN MTXD3	20
LAN MRXC	LAN MRXC	20
LAN MRXD0	LAN MRXD0	20
LAN MRXD1	LAN MRXD1	20
LAN MRXD2	LAN MRXD2	20
LAN MRXD3	LAN MRXD3	20



REQ#	REQ#	5,21
GNT#	GNT#	5,21
LAN CRS	LAN CRS	20
LAN COL	LAN COL	20
LAN MTXE	LAN MTXE	20
LAN MTXD0	LAN MTXD0	20
LAN MTXD1	LAN MTXD1	20
LAN MTXD2	LAN MTXD2	20
LAN MTXD3	LAN MTXD3	20
LAN MRXC	LAN MRXC	20
LAN MRXD0	LAN MRXD0	20
LAN MRXD1	LAN MRXD1	20
LAN MRXD2	LAN MRXD2	20
LAN MRXD3	LAN MRXD3	20

REQ#	REQ#	5,21
GNT#	GNT#	5,21
LAN CRS	LAN CRS	20
LAN COL	LAN COL	20
LAN MTXE	LAN MTXE	20
LAN MTXD0	LAN MTXD0	20
LAN MTXD1	LAN MTXD1	20
LAN MTXD2	LAN MTXD2	20
LAN MTXD3	LAN MTXD3	20
LAN MRXC	LAN MRXC	20
LAN MRXD0	LAN MRXD0	20
LAN MRXD1	LAN MRXD1	20
LAN MRXD2	LAN MRXD2	20
LAN MRXD3	LAN MRXD3	20

REQ#	REQ#	5,21
GNT#	GNT#	5,21
LAN CRS	LAN CRS	20
LAN COL	LAN COL	20
LAN MTXE	LAN MTXE	20
LAN MTXD0	LAN MTXD0	20
LAN MTXD1	LAN MTXD1	20
LAN MTXD2	LAN MTXD2	20
LAN MTXD3	LAN MTXD3	20
LAN MRXC	LAN MRXC	20
LAN MRXD0	LAN MRXD0	20
LAN MRXD1	LAN MRXD1	20
LAN MRXD2	LAN MRXD2	20
LAN MRXD3	LAN MRXD3	20

REQ#	REQ#	5,21
GNT#	GNT#	5,21
LAN CRS	LAN CRS	20
LAN COL	LAN COL	20
LAN MTXE	LAN MTXE	20
LAN MTXD0	LAN MTXD0	20
LAN MTXD1	LAN MTXD1	20
LAN MTXD2	LAN MTXD2	20
LAN MTXD3	LAN MTXD3	20
LAN MRXC	LAN MRXC	20
LAN MRXD0	LAN MRXD0	20
LAN MRXD1	LAN MRXD1	20
LAN MRXD2	LAN MRXD2	20
LAN MRXD3	LAN MRXD3	20

REQ#	REQ#	5,21
GNT#	GNT#	5,21
LAN CRS	LAN CRS	20
LAN COL	LAN COL	20
LAN MTXE	LAN MTXE	20
LAN MTXD0	LAN MTXD0	20
LAN MTXD1	LAN MTXD1	20
LAN MTXD2	LAN MTXD2	20
LAN MTXD3	LAN MTXD3	20
LAN MRXC	LAN MRXC	20
LAN MRXD0	LAN MRXD0	20
LAN MRXD1	LAN MRXD1	20
LAN MRXD2	LAN MRXD2	20
LAN MRXD3	LAN MRXD3	20

REQ#	REQ#	5,21
GNT#	GNT#	5,21
LAN CRS	LAN CRS	20
LAN COL	LAN COL	20
LAN MTXE	LAN MTXE	20
LAN MTXD0	LAN MTXD0	20
LAN MTXD1	LAN MTXD1	20
LAN MTXD2	LAN MTXD2	20
LAN MTXD3	LAN MTXD3	20
LAN MRXC	LAN MRXC	20
LAN MRXD0	LAN MRXD0	20
LAN MRXD1	LAN MRXD1	20
LAN MRXD2	LAN MRXD2	20
LAN MRXD3	LAN MRXD3	20

REQ#	REQ#	5,21
GNT#	GNT#	5,21
LAN CRS	LAN CRS	20
LAN COL	LAN COL	20
LAN MTXE	LAN MTXE	20
LAN MTXD0	LAN MTXD0	20
LAN MTXD1	LAN MTXD1	20
LAN MTXD2	LAN MTXD2	20
LAN MTXD3	LAN MTXD3	20
LAN MRXC	LAN MRXC	20
LAN MRXD0	LAN MRXD0	20
LAN MRXD1	LAN MRXD1	20
LAN MRXD2	LAN MRXD2	20
LAN MRXD3	LAN MRXD3	20

REQ#	REQ#	5,21
GNT#	GNT#	5,21
LAN CRS	LAN CRS	20
LAN COL	LAN COL	20
LAN MTXE	LAN MTXE	20
LAN MTXD0	LAN MTXD0	20
LAN MTXD1	LAN MTXD1	20
LAN MTXD2	LAN MTXD2	20
LAN MTXD3	LAN MTXD3	20
LAN MRXC	LAN MRXC	20
LAN MRXD0	LAN MRXD0	20
LAN MRXD1	LAN MRXD1	20
LAN MRXD2	LAN MRXD2	20
LAN MRXD3	LAN MRXD3	20

REQ#	REQ#	5,21
GNT#	GNT#	5,21
LAN CRS	LAN CRS	20
LAN COL	LAN COL	20
LAN MTXE	LAN MTXE	20
LAN MTXD0	LAN MTXD0	20
LAN MTXD1	LAN MTXD1	20
LAN MTXD2	LAN MTXD2	20
LAN MTXD3	LAN MTXD3	20
LAN MRXC	LAN MRXC	20
LAN MRXD0	LAN MRXD0	20
LAN MRXD1	LAN MRXD1	20
LAN MRXD2	LAN MRXD2	20
LAN MRXD3	LAN MRXD3	20

REQ#	REQ#	5,21
GNT#	GNT#	5,21
LAN CRS	LAN CRS	20
LAN COL	LAN COL	20
LAN MTXE	LAN MTXE	20
LAN MTXD0	LAN MTXD0	20
LAN MTXD1	LAN MTXD1	20
LAN MTXD2	LAN MTXD2	20
LAN MTXD3	LAN MTXD3	20
LAN MRXC	LAN MRXC	20
LAN MRXD0	LAN MRXD0	20
LAN MRXD1	LAN MRXD1	20
LAN MRXD2	LAN MRXD2	20
LAN MRXD3	LAN MRXD3	20

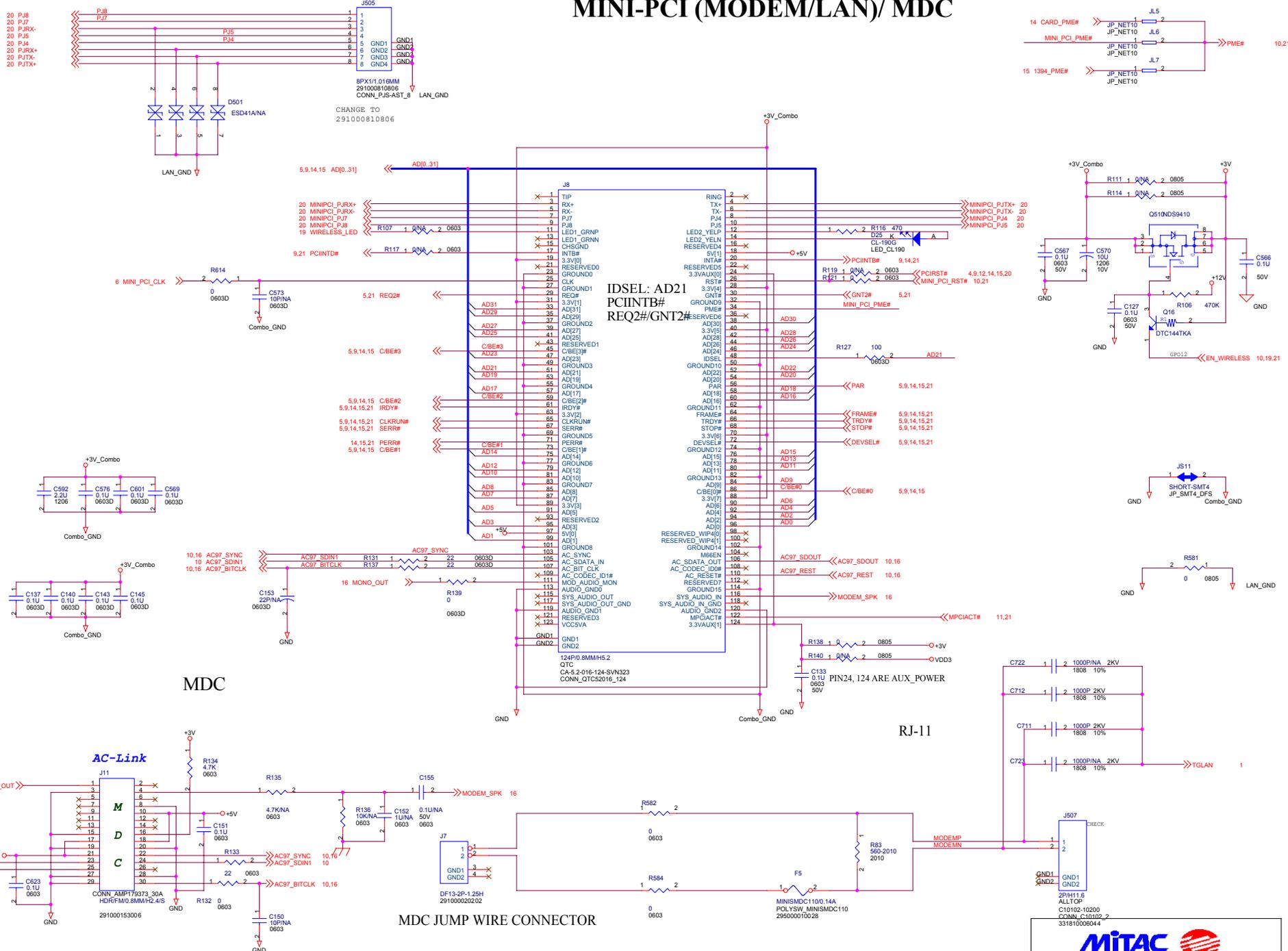
REQ#	REQ#	5,21
GNT#	GNT#	5,21
LAN CRS	LAN CRS	20
LAN COL	LAN COL	20
LAN MTXE	LAN MTXE	20
LAN MTXD0	LAN MTXD0	20
LAN MTXD1	LAN MTXD1	20
LAN MTXD2	LAN MTXD2	20
LAN MTXD3	LAN MTXD3	20
LAN MRXC	LAN MRXC	20
LAN MRXD0	LAN MRXD0	20
LAN MRXD1	LAN MRXD1	20
LAN MRXD2	LAN MRXD2	20
LAN MRXD3	LAN MRXD3	20

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MINI-PCI (MODEM/LAN)/ MDC



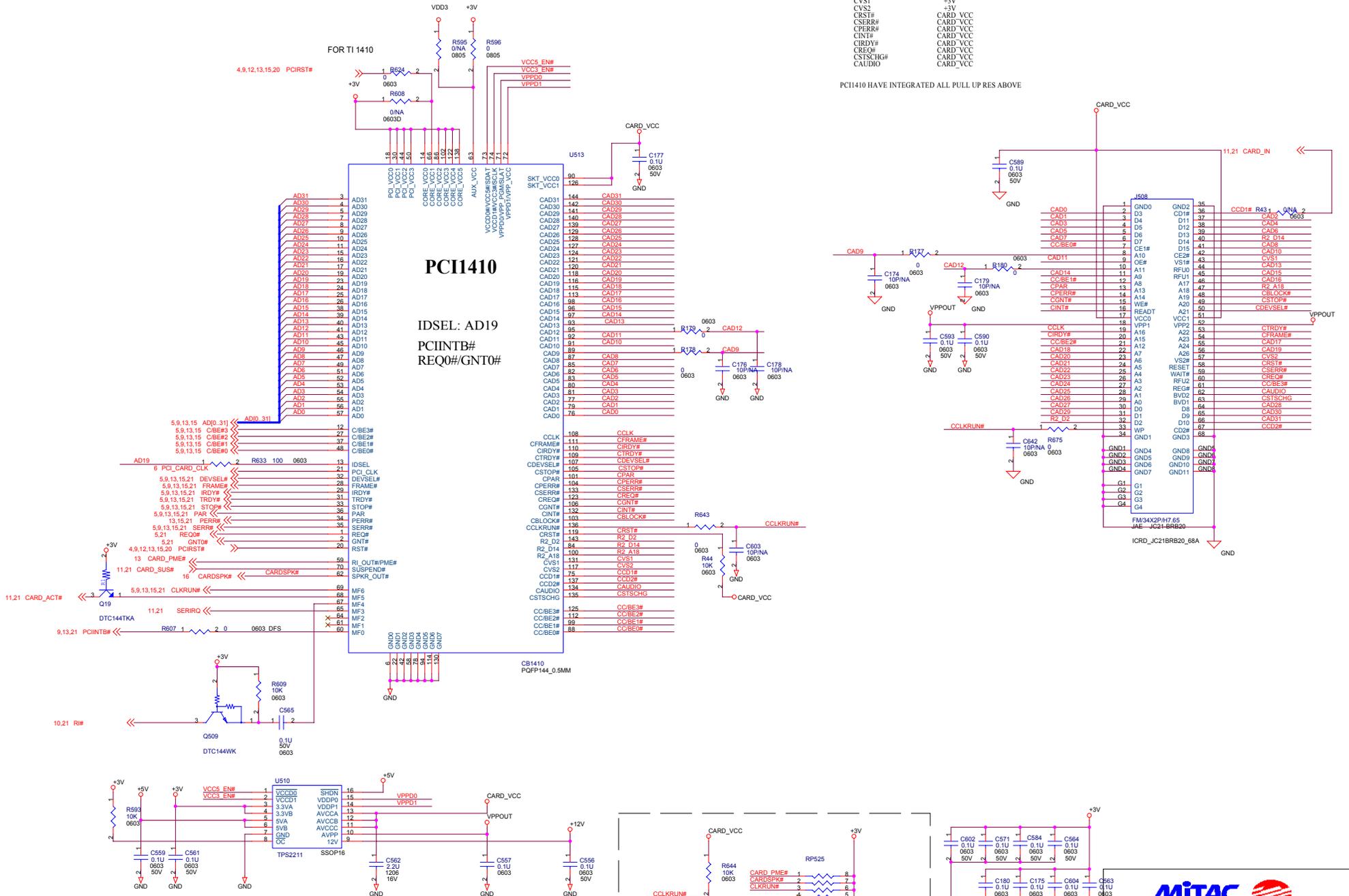
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CARDBUS CONTROLLER

SIGNAL	PC CARD PULL UP	VOLT	SEND THE SCHEMATIC TO TI FAE DOUBLE CHECK
CCD#1	+3V		
CCD#2	+3V		
CBLOCK#	CARD_VCC		
CSTOP#	CARD_VCC		
CDEVSEL#	CARD_VCC		
CVS1	+3V		
CVS2	+3V		
CRST#	CARD_VCC		
CSERR#	CARD_VCC		
CPERR#	CARD_VCC		
CINT#	CARD_VCC		
CIRDY#	CARD_VCC		
CREQ#	CARD_VCC		
CSCHG#	CARD_VCC		
CAUDIO	CARD_VCC		

PCI1410 HAVE INTEGRATED ALL PULL UP RES ABOVE



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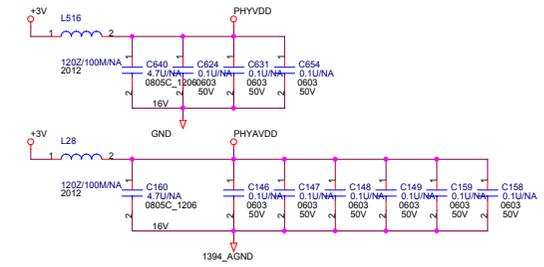
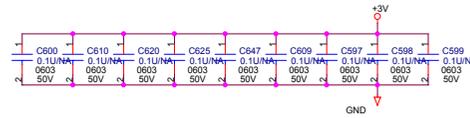
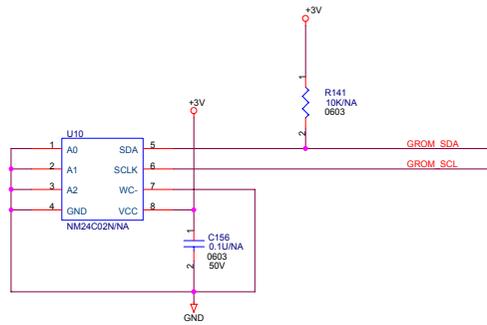
Document Number: ASSY 41167260001/PCB 31667260001

Date: Tuesday, July 16, 2002

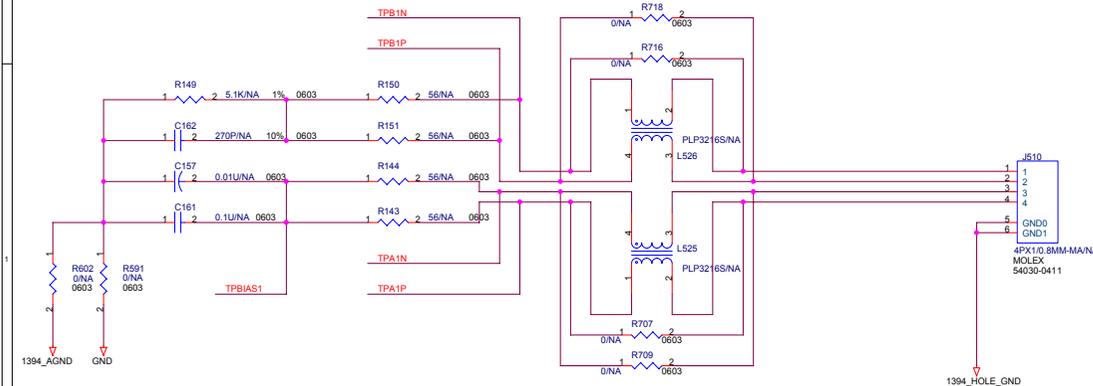
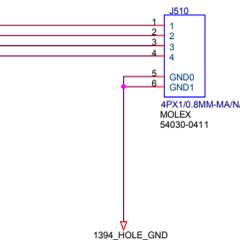
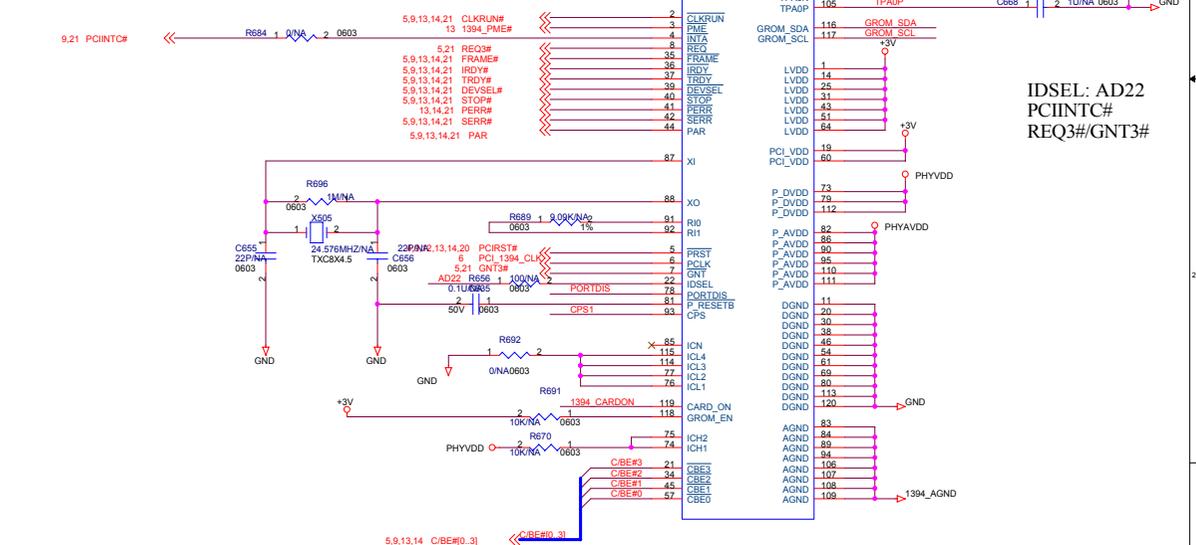
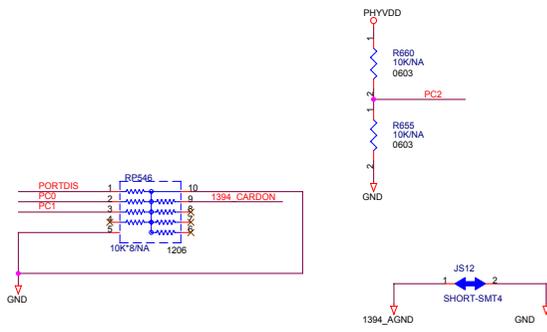
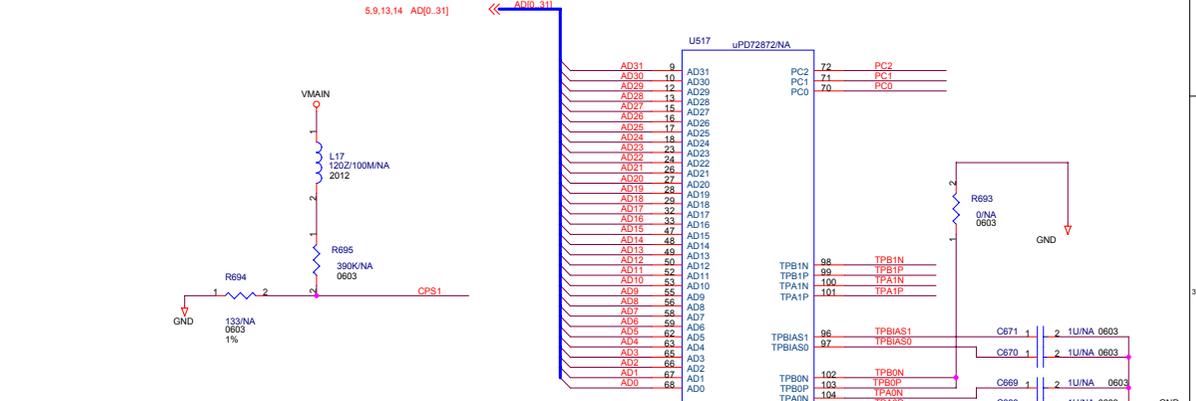
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IEEE1394- UPD72872

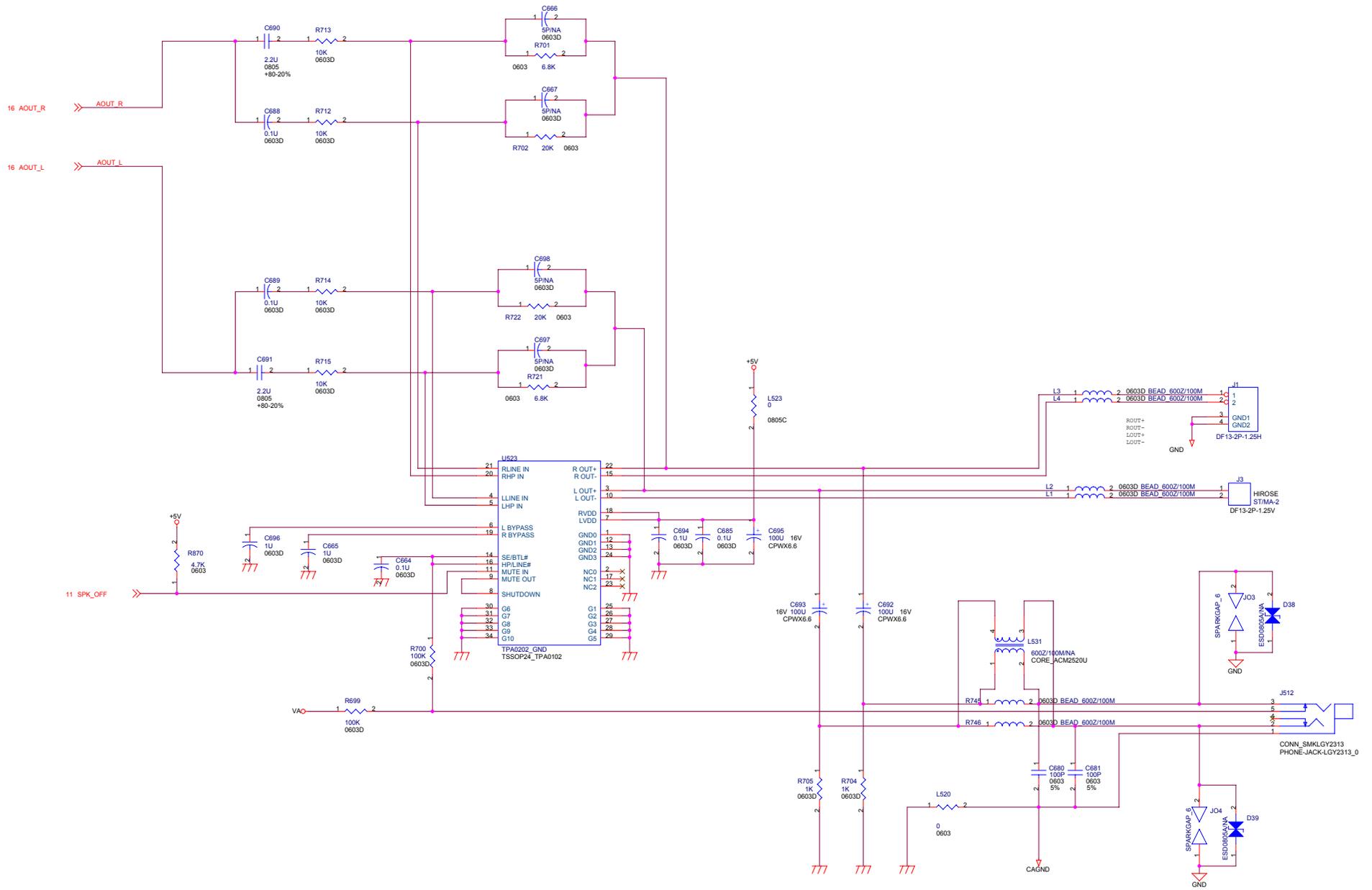


DEVICE:= C:\O1394DRV.SYS IN CONFIG.SYS

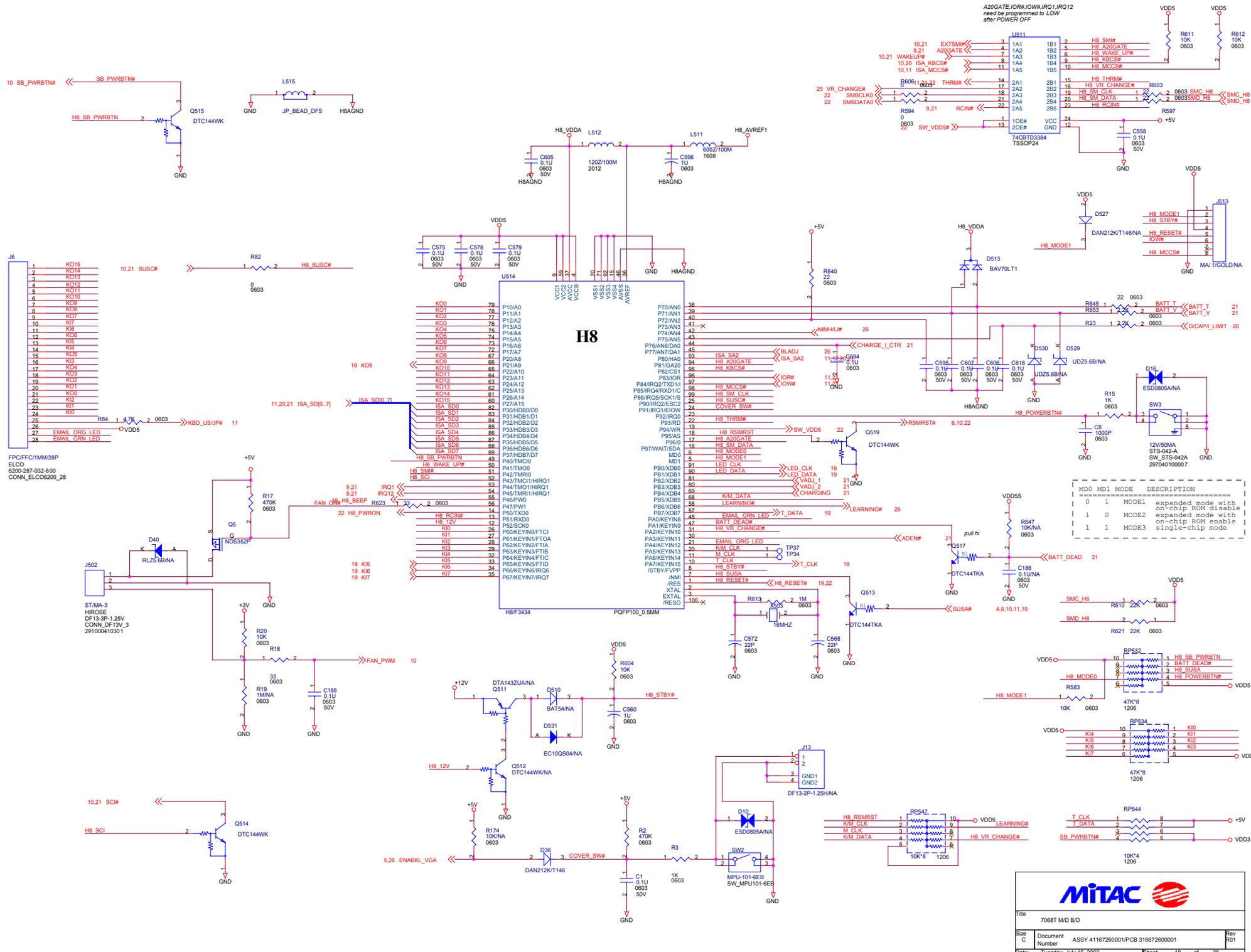


IDSEL: AD22
PCINTC#
REQ3#/GNT3#

AUDIO AMPLIFIER - TPA0202



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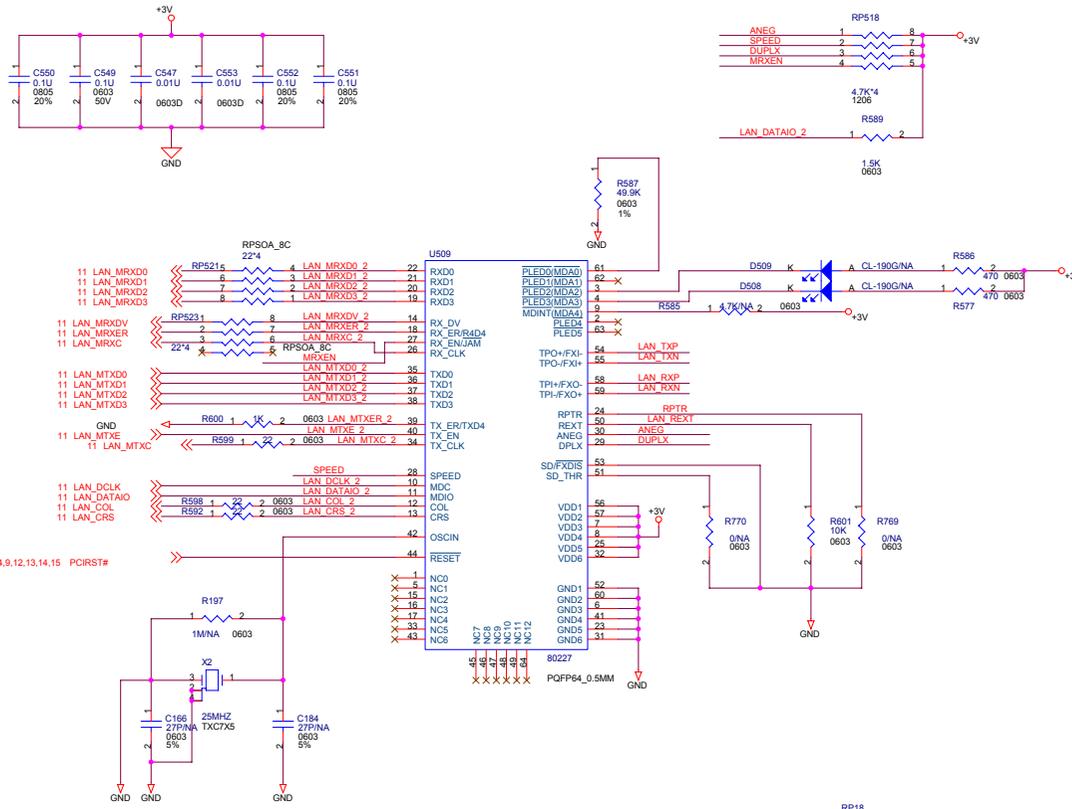
Size C Document Number: ASSY 41167260001/PCB 316672600001

Date: Tuesday, July 16, 2002

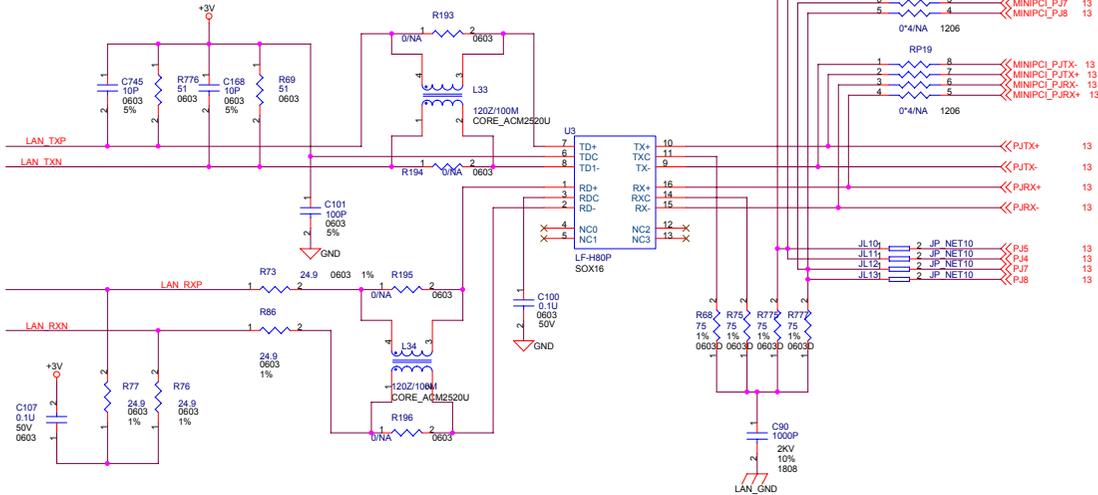
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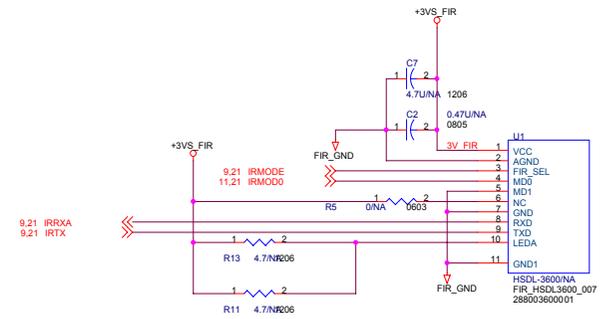
LAN PHY-LSI80227



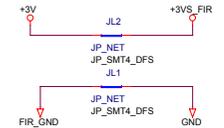
4,9,12,13,14,15 PCIRST#



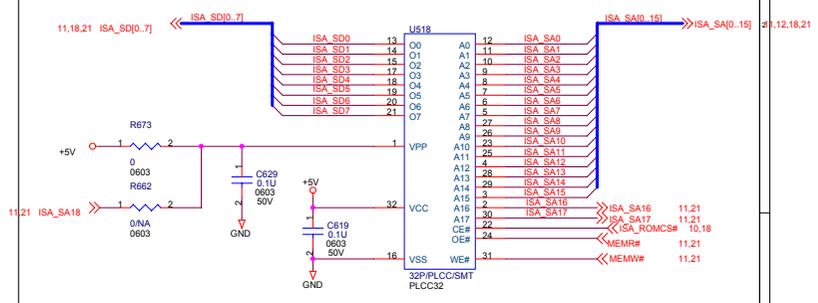
IR MODULE HP FIR MODULE HSDL-3600#007



CHECK VIA SUPPORT WHICH IR MODULE

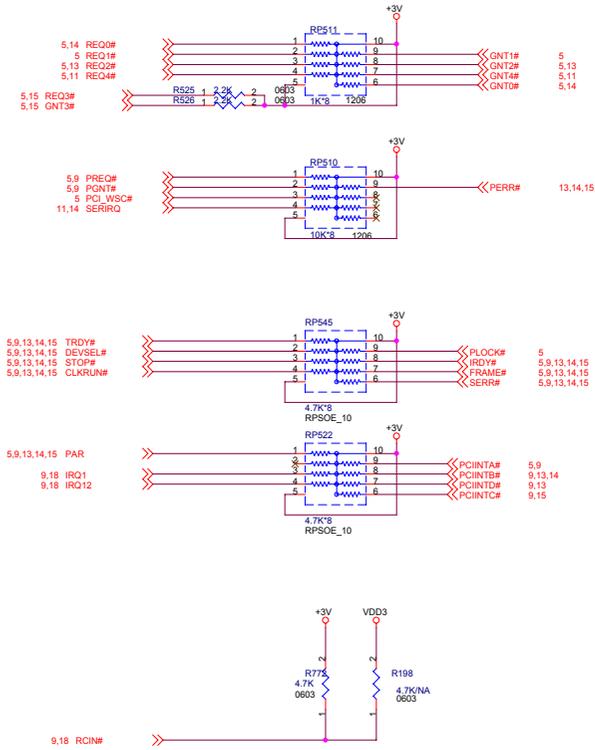


SYSTEM BIOS

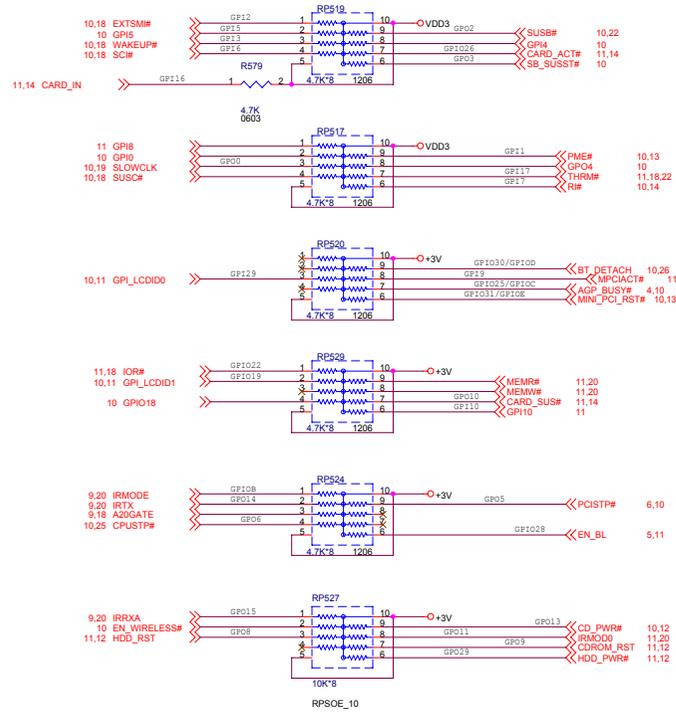


MITAC		
Title: 7068T M/D B/D		
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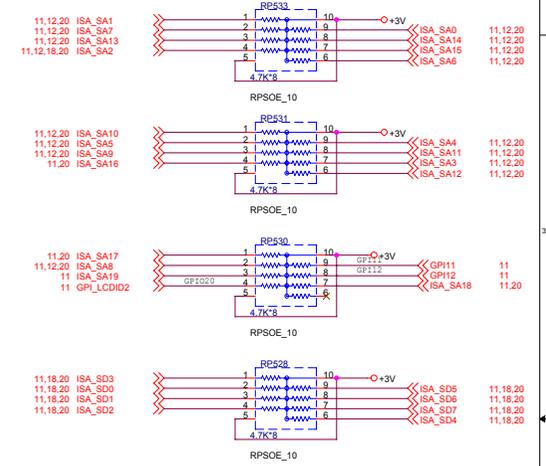
PCI PULL-HIGH



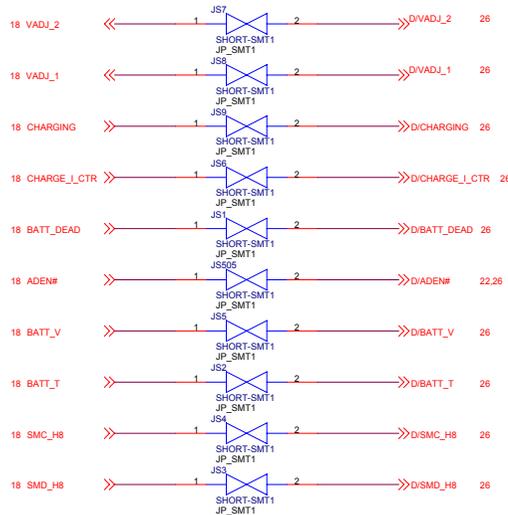
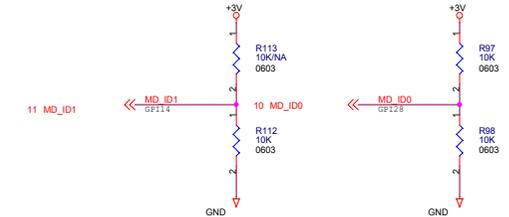
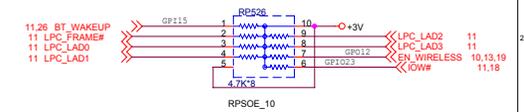
GPIO-PULL HIGH



ISA-PULL HIGH



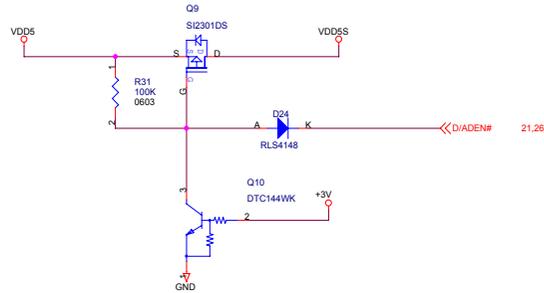
LPC-RESERVE-PULL HIGH



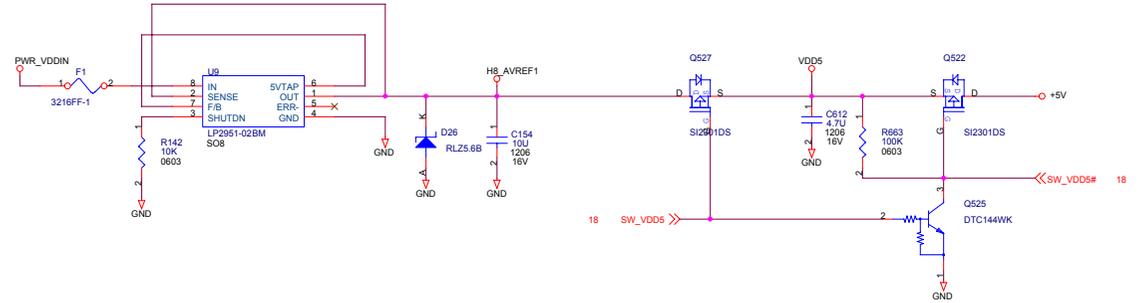
MITAC		
Title: 7068T M/D B/D		
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VDD5S

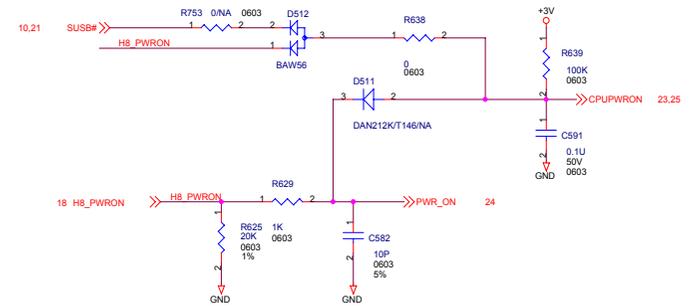
sent to d/d bd for charging comparator ckt when system is in powered off state



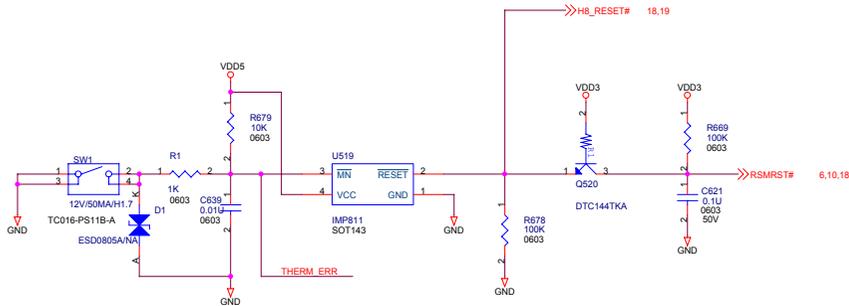
VDD5



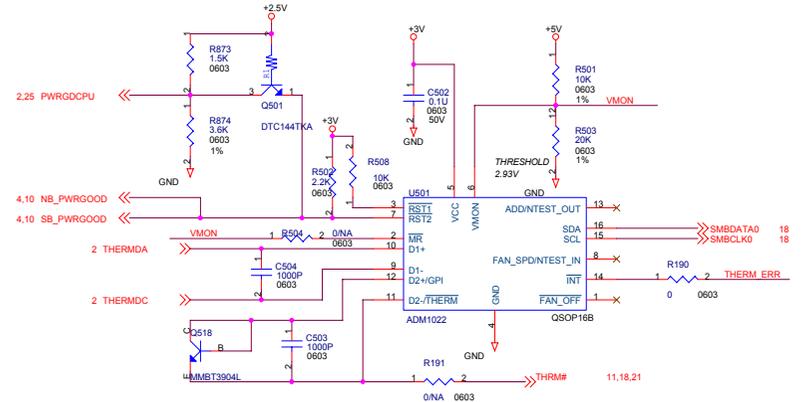
POWER ON



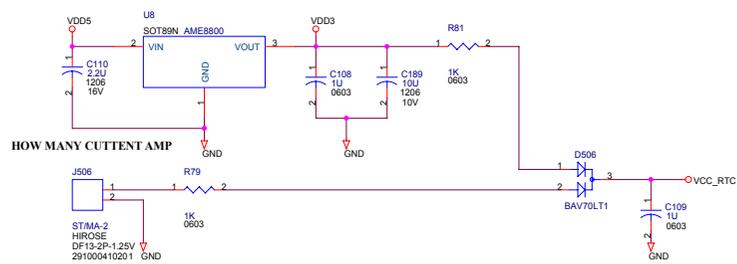
H8 RESET



POWER OK

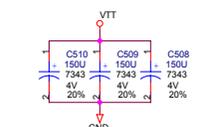
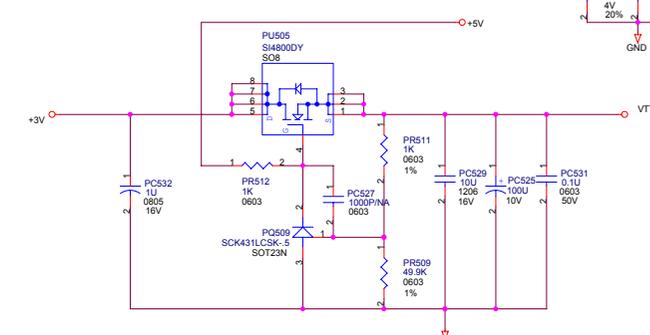
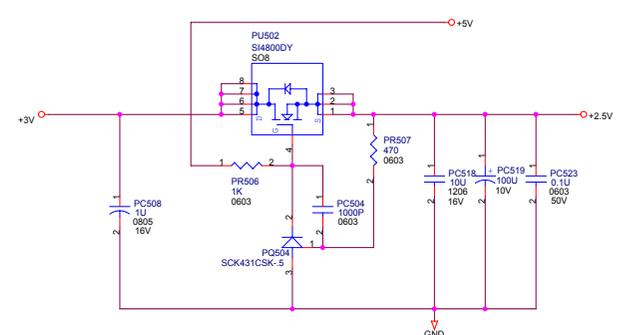
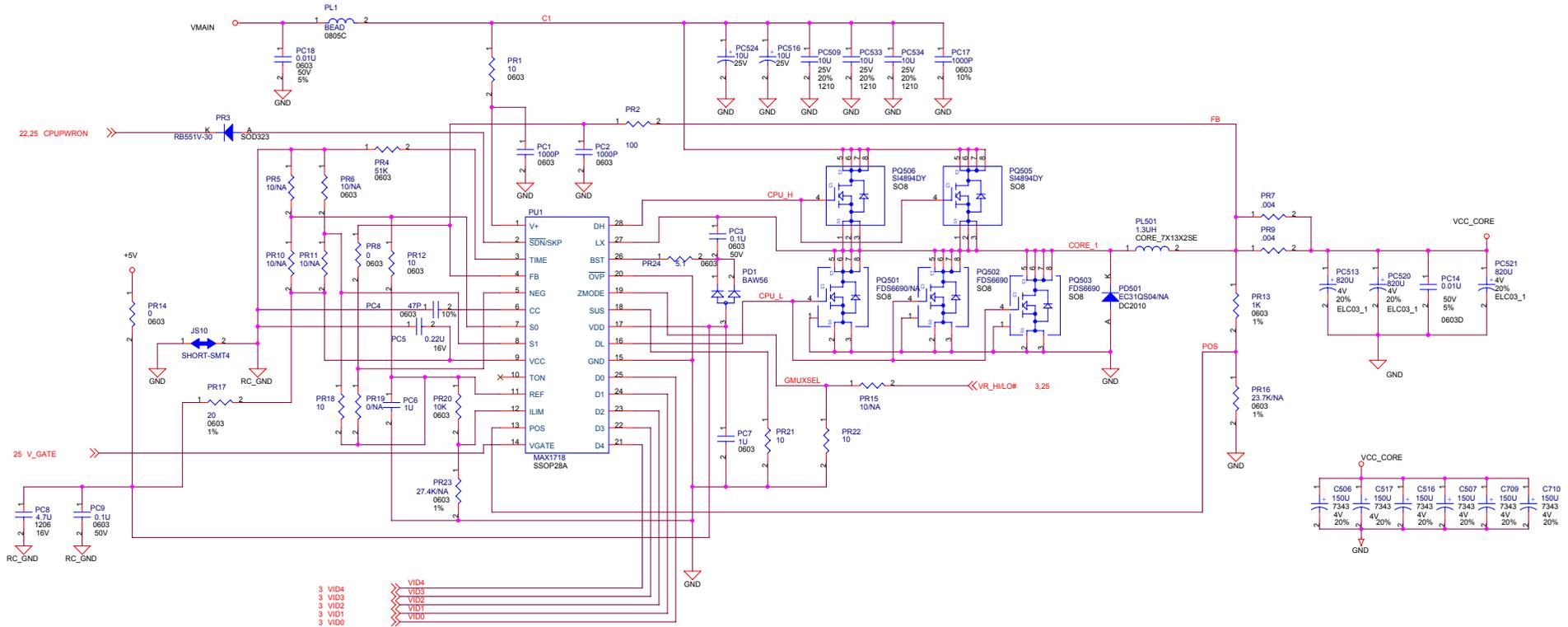


RTC BATTERY CONNECTOR



Title	7068T M/D B/D	
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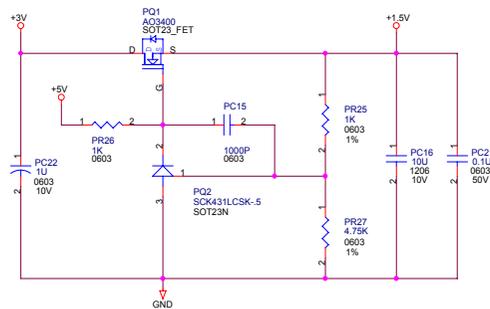
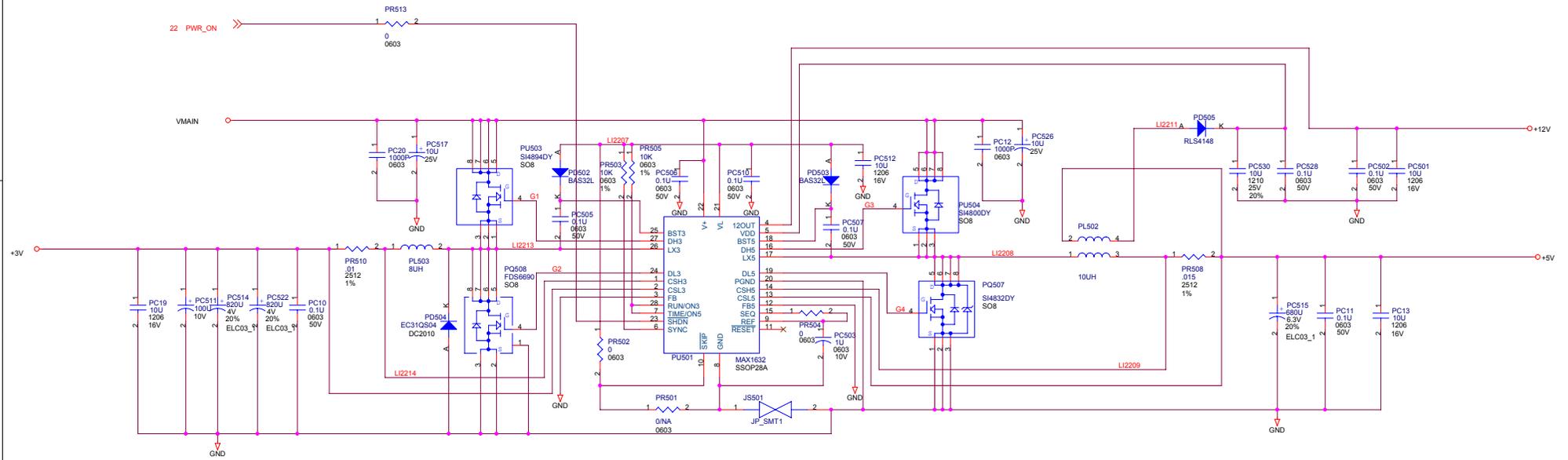
CPU_CORE/+2.5V/VTT



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+1.5V/+3V/+5V/+12V



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