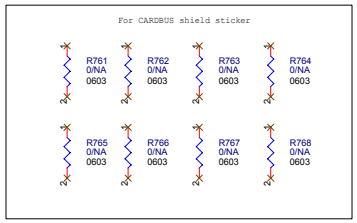
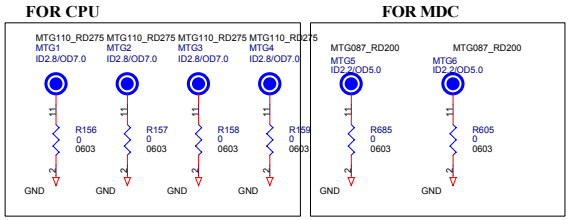
7068T Schematic R01

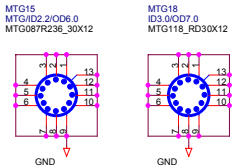
PRODUCT CODE : 6726 PROJECT CODE : G009

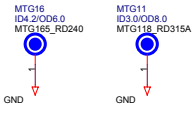
PCI DEVICE	INTERRUPT	REQ/GNT	IDSEL
MINI-PCI	PCIINTB#	REQ2#/GNT2#	AD21
IEEE1394	PCIINTC#	REQ3#/GNT3#	AD22
TI1410	PCIINTB#	REQ0#/GNT0#	AD19

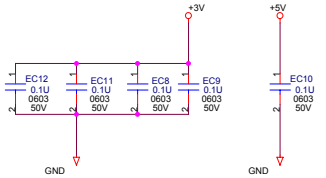
REVISION	TAPEOUT DAY	HISTORY
R0A	91/1/23	DESIGN FOR DVT
R0B		1. Add CPU Vcore Switch(P.3) 2. CPU Clock Change Auto select(P.6) 3. Add Black Light Enable Control(P.5)
R01	91/07/02	1. FOLLOW INTEL RES SPEC.(P2,P25) 2.V-CORE ADD CAP(P3) 3.ADD C81 FOR NB SKEW(P4) 4.VTT ADD CAP FOR NB(P4) 5.PICCLK CHANGE TO 2V (P2,P6) 6.CPU POWER GOOD CHANGE TO 1.8V(P22) 7. ADD PR514,DEL PD501,PQ501 FOR V-CORE NOISE(P23)

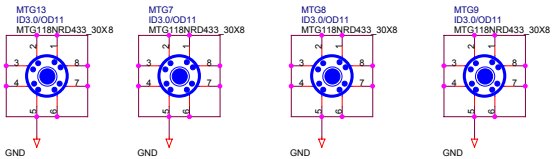


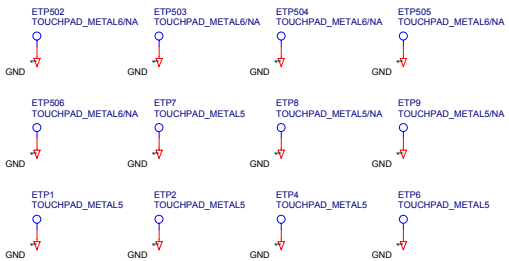


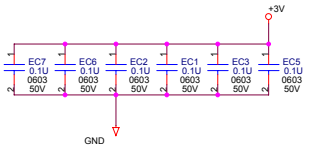


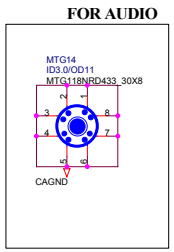


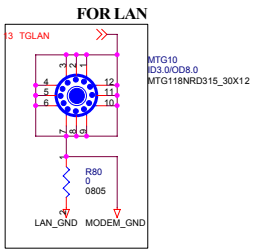


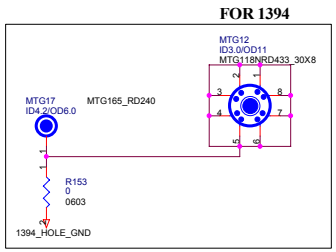


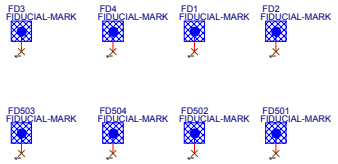












DRAWN	DESIGN	CHECK	ISSUES

MiTAC

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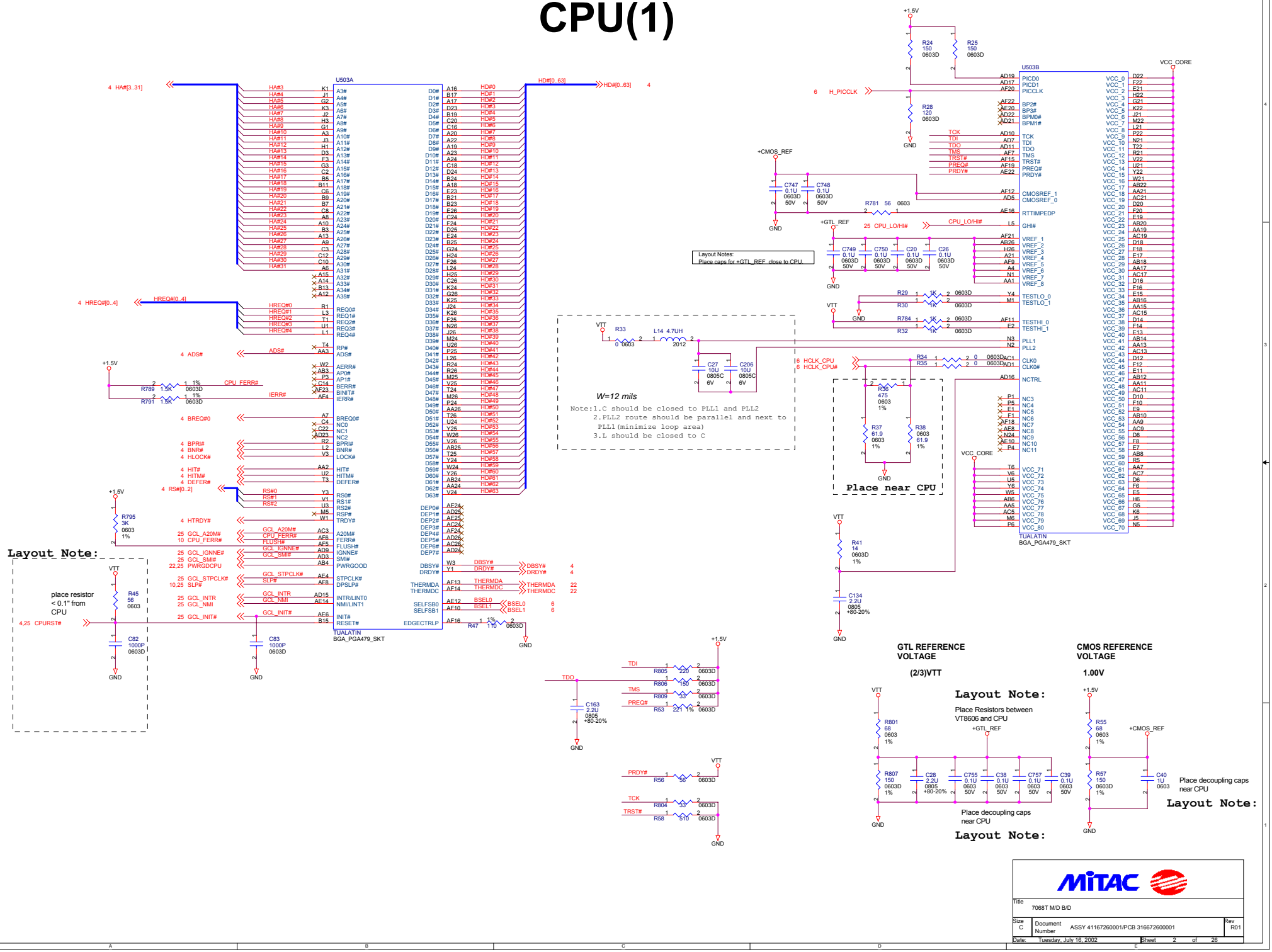
CPU(1)


U503A
TUALATIN
BGA_PGA479_SKT
U503B
TUALATIN
BGA_PGA479_SKT
VCC_CORE
Layout Notes:
Place caps for +GTL_REF close to CPU
W=12 mils
Note:1.C should be closed to PLL1 and PLL2
2.PLL2 route should be parallel and next to PLL1(minimize loop area)
3.L should be closed to C
Place near CPU
Layout Note:
place resistor < 0.1" from CPU
GTL REFERENCE VOLTAGE
(2/3)VTT
CMOS REFERENCE VOLTAGE
1.00V
Layout Note:
Place Resistors between VT8606 and CPU
Place decoupling caps near CPU
Layout Note:
Place decoupling caps near CPU
Layout Note:
MiTAC
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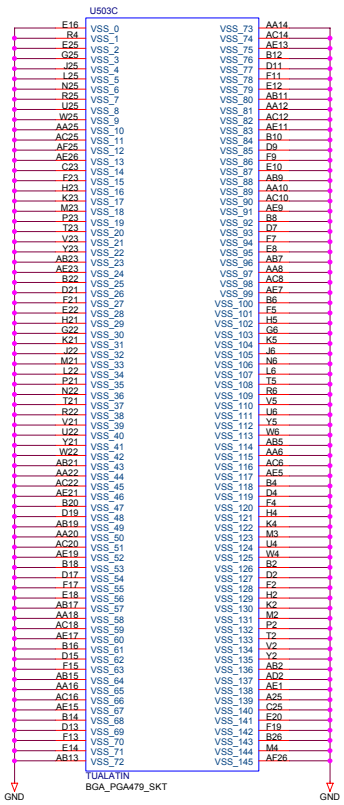
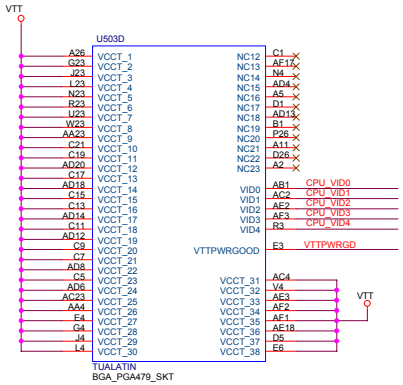
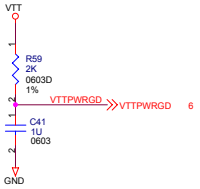
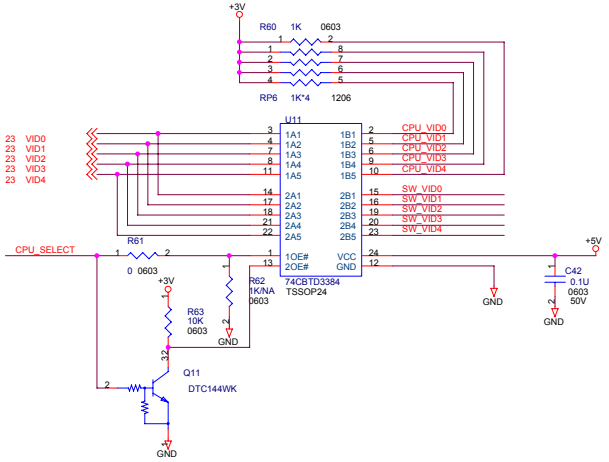
CPU(2)



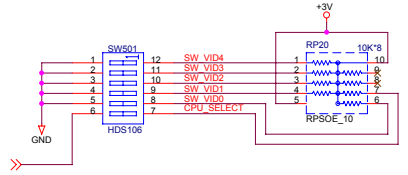




VID[0..4] pull up 10K to +3V in VRM side



VID4	VID3	VID2	VID1	VID0	VOLT.
0	0	0	0	0	1.75
0	0	0	0	1	1.70
0	0	0	1	0	1.65
0	0	0	1	1	1.60
0	0	1	0	0	1.55
0	0	1	0	1	1.50
0	0	1	1	0	1.45
0	0	1	1	1	1.40
0	1	0	0	0	1.35
0	1	0	0	1	1.30
0	1	0	1	0	1.25
0	1	0	1	1	1.200
0	1	1	0	0	1.15
0	1	1	0	1	1.100
0	1	1	1	0	1.050
0	1	1	1	1	1.000
1	0	0	0	0	0.975
1	0	0	0	1	0.950
1	0	0	1	0	0.925
1	0	0	1	1	0.9
1	0	1	0	0	0.875
1	0	1	0	1	0.85
1	0	1	1	0	0.825
1	0	1	1	1	0.8
1	1	0	0	0	0.775
1	1	0	0	1	0.75
1	1	0	1	0	0.725
1	1	0	1	1	0.7
1	1	1	0	0	0.675
1	1	1	0	1	0.65
1	1	1	1	0	0.625
1	1	1	1	1	0.6

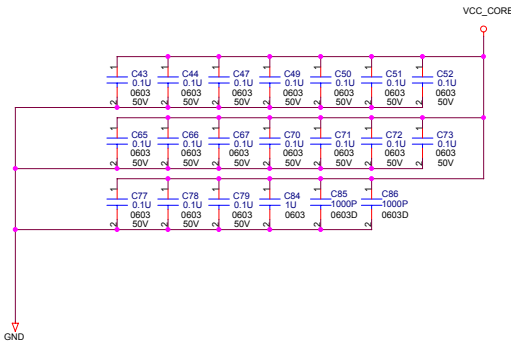


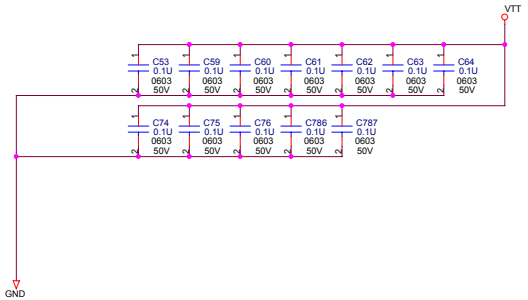
VID : SWITCH

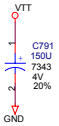
1 : Pull High(OFF)

0 : Pull Low(ON)

CPU_SELECT(ON : Intel; OFF : C3)







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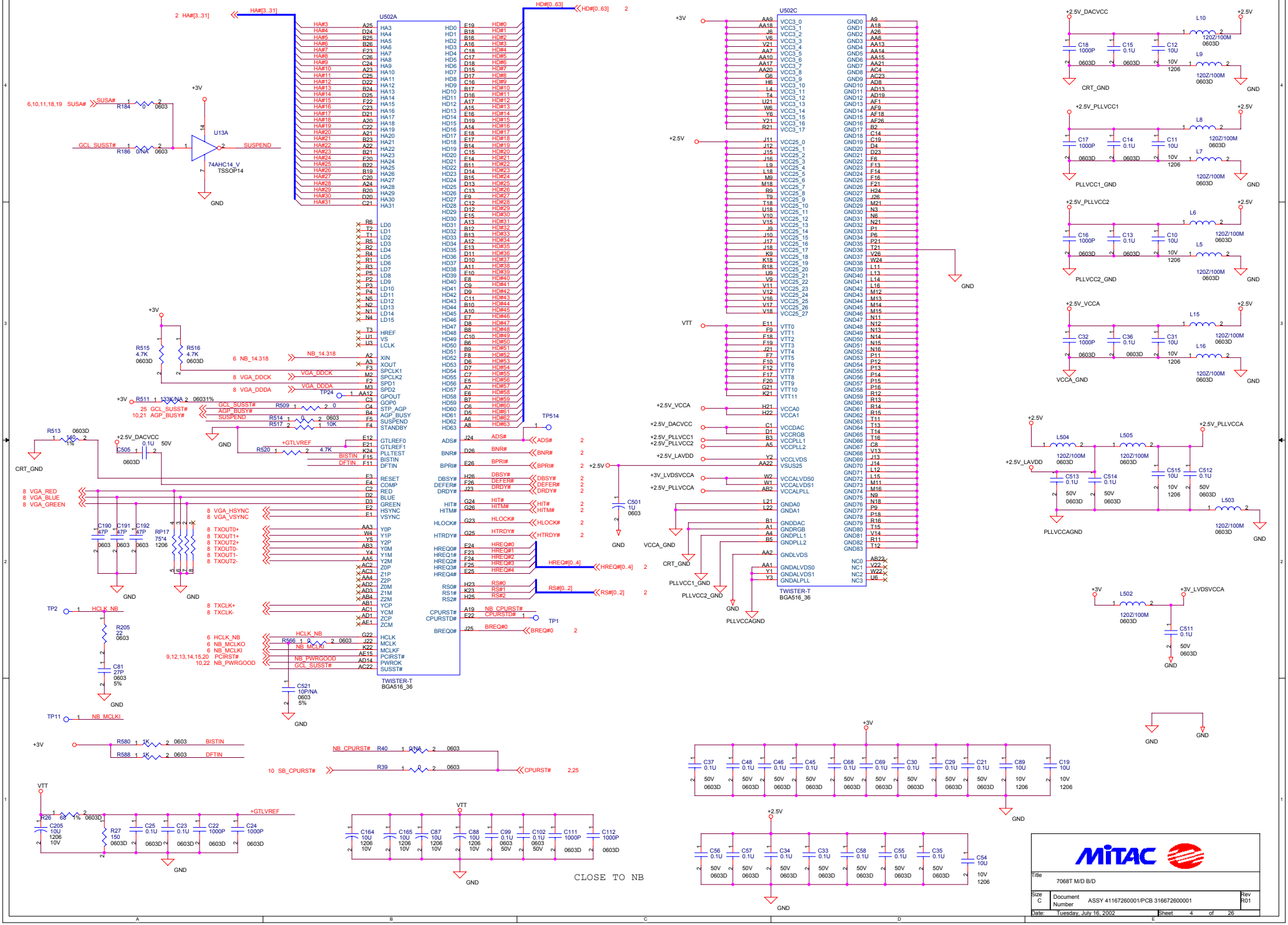
NORTH BRIDGE-TWISTER (1)- VGA and HOST INTERFACE



MiTAC

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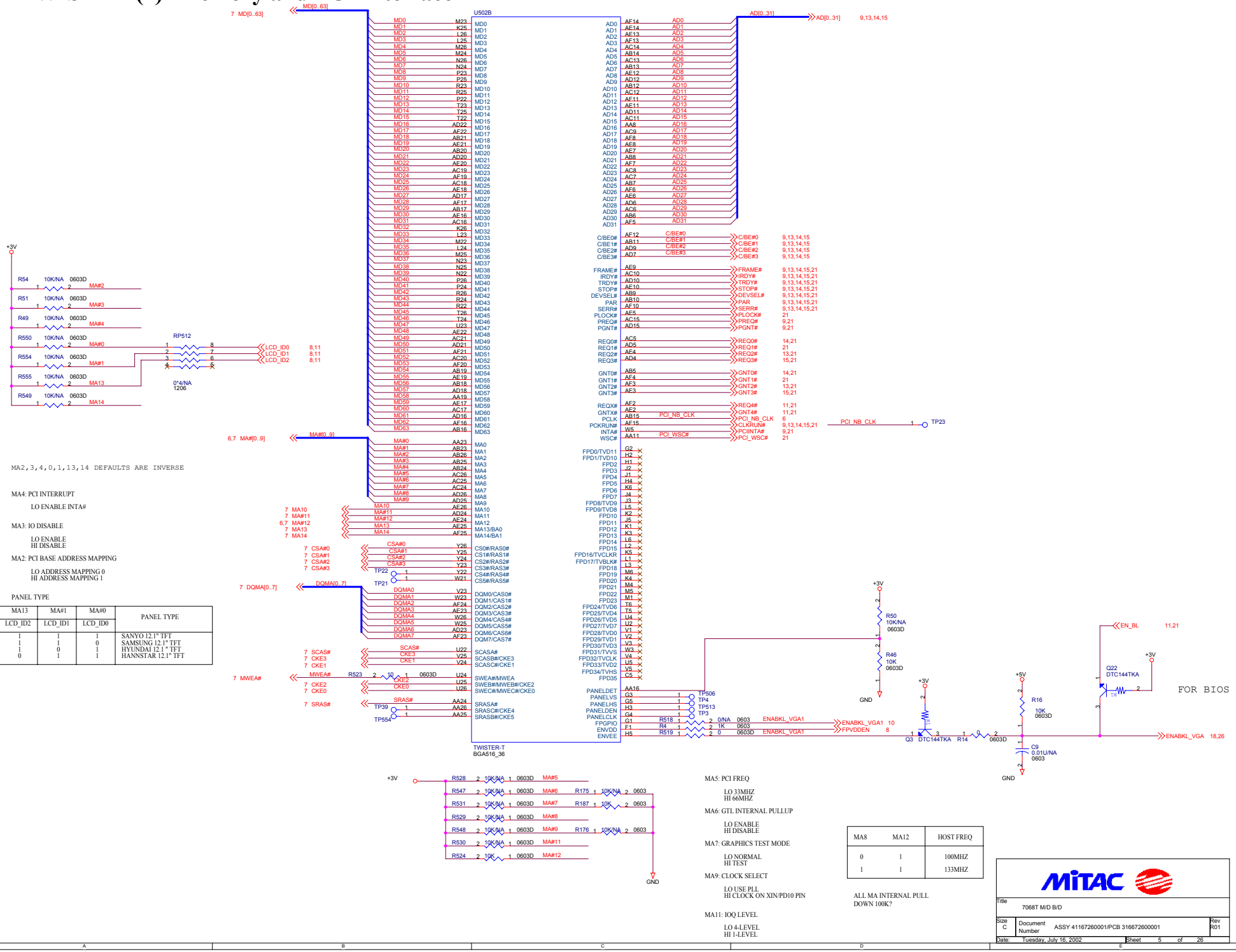
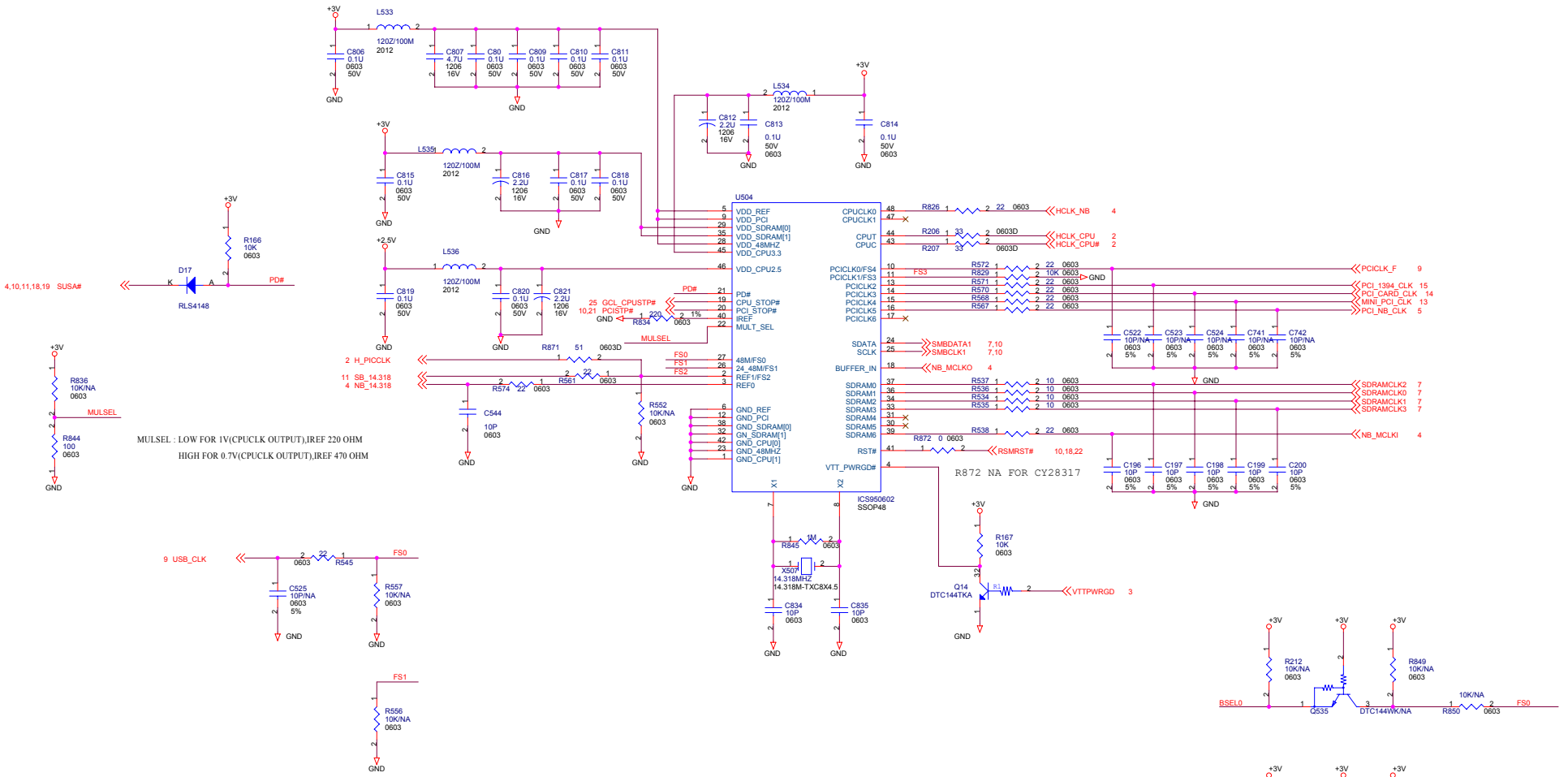
TWISTER (2)- Memory and PCI Interface



CLOCK SYNTHERISZER- ICS950602/CY28317



FS4	FS3	FS2	FS1	FS0	CPU(MHZ)	PCI(MHZ)
1	0	1	0	1	100.00	33.33
1	0	1	1	1	133.33	33.33

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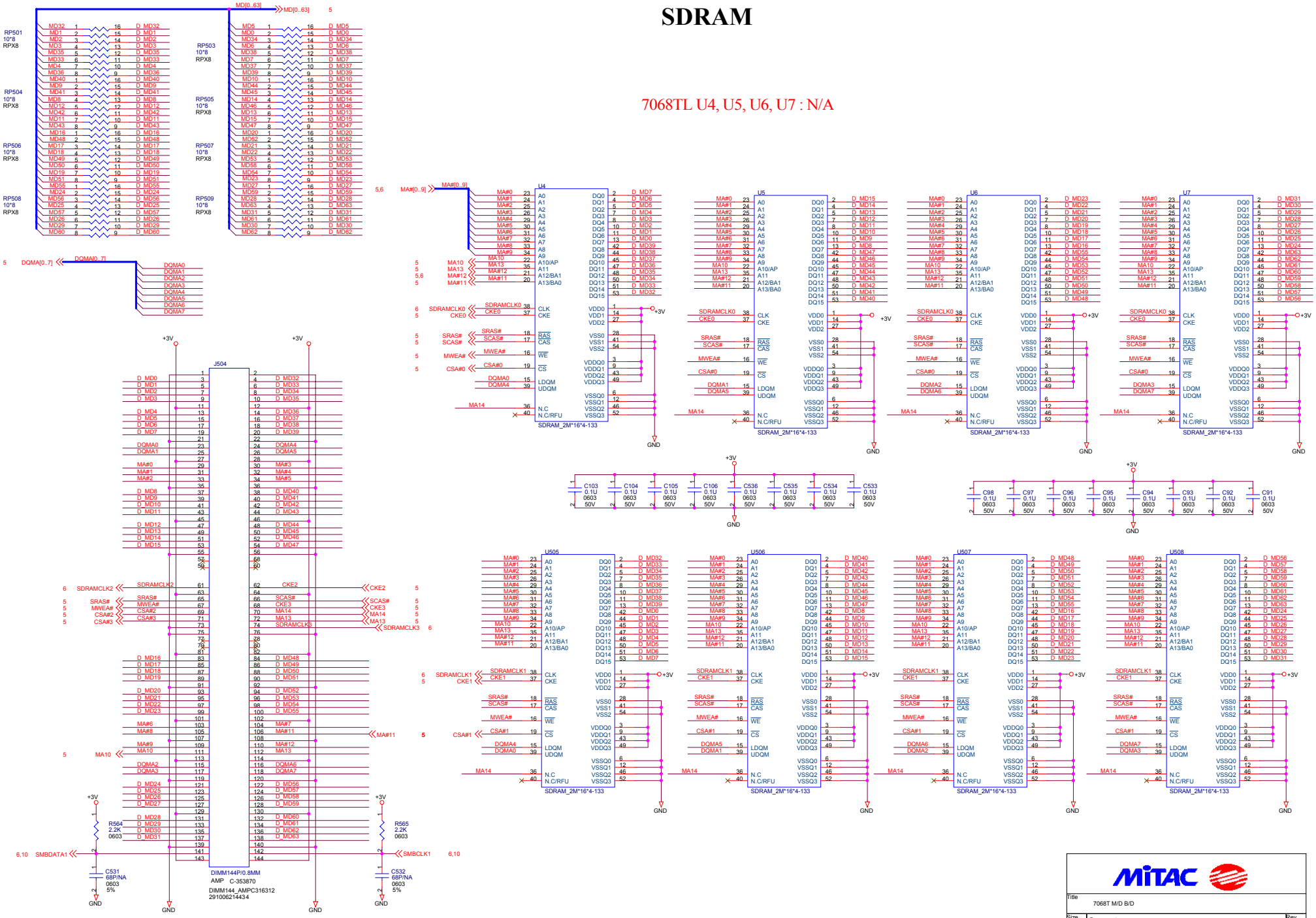
SDRAM

7068TL U4, U5, U6, U7 : N/A



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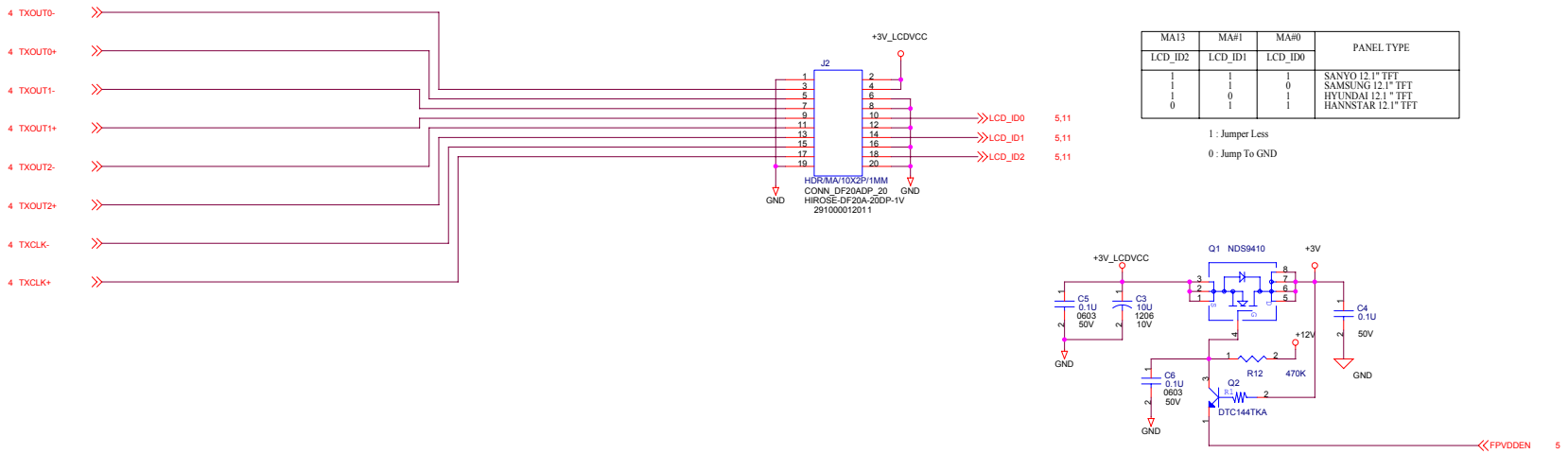
LCD CONNECTOR

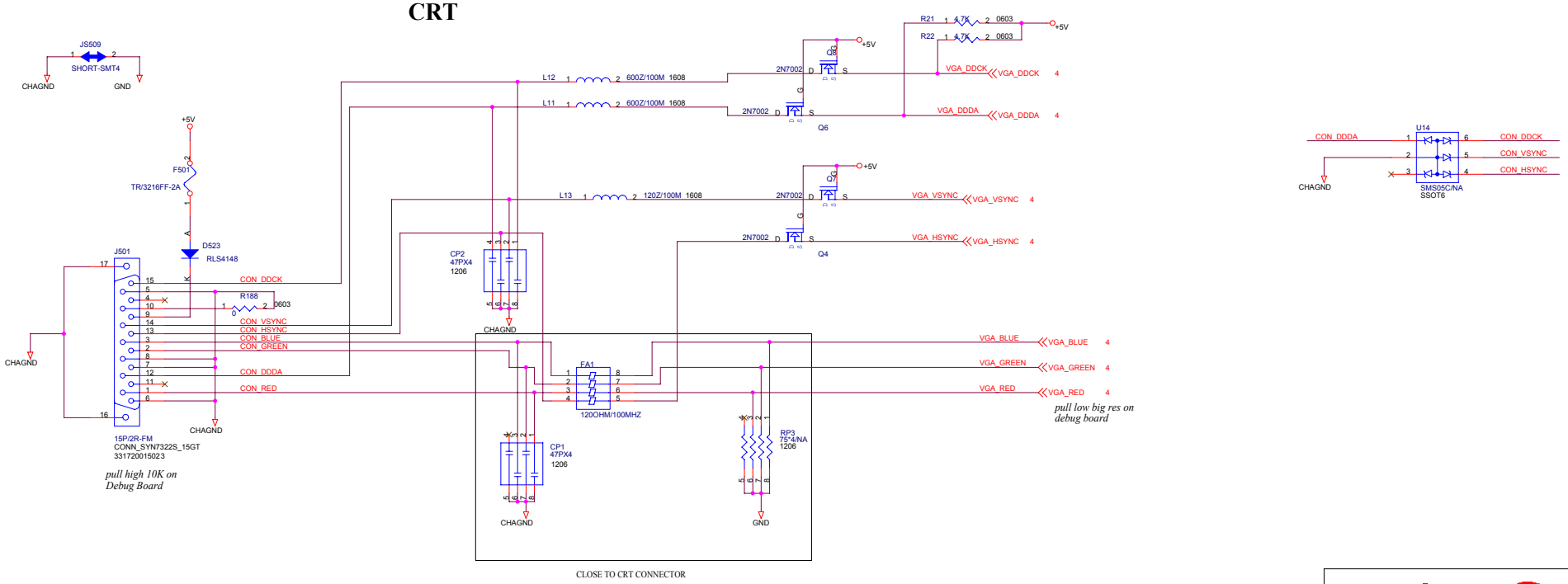


MA13	MA#1	MA#0	PANEL TYPE
LCD_ID2	LCD_ID1	LCD_ID0	
1	1	1	SANYO 12.1" TFT
1	1	0	SAMSUNG 12.1" TFT
1	0	1	HYUNDAI 12.1 " TFT
0	1	1	HANNSTAR 12.1" TFT

1 : Jumper Less

0 : Jump To GND

CRT



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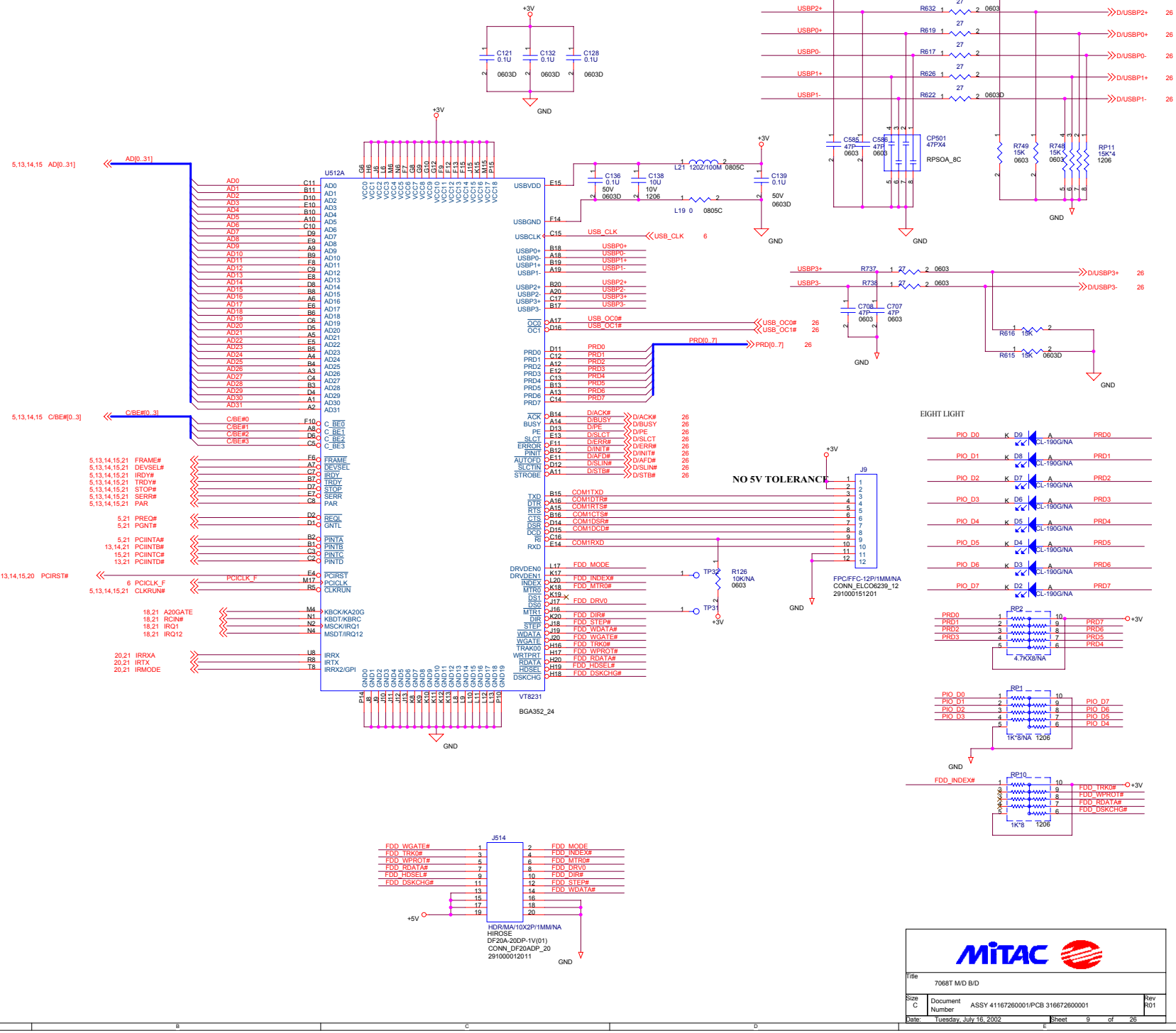
VT8231 (1)


U512A
VT8231
BGA352_24
AD[0..31]
C/BE#[0..3]
USB_CLK
PRD[0..7]
USBP0+
USBP0-
USBP1+
USBP1-
USBP2+
USBP2-
USBP3+
USBP3-
D/USBP0+
D/USBP0-
D/USBP1+
D/USBP1-
D/USBP2+
D/USBP2-
D/USBP3+
D/USBP3-
NO 5V TOLERANCE
J9
FPC/FFC-12P/1MM/NA
CONN_ELCO6239_12
291000151201
EIGHT LIGHT
J514
HDR/MA/10X2P/1MM/NA
HIROSE
DF20A-20DP-1V(01)
CONN_DF20ADP_20
291000012011
RPSOA_8C
4.7KX8/NA
1K*8/NA 1206
1K*8 1206
MiTAC
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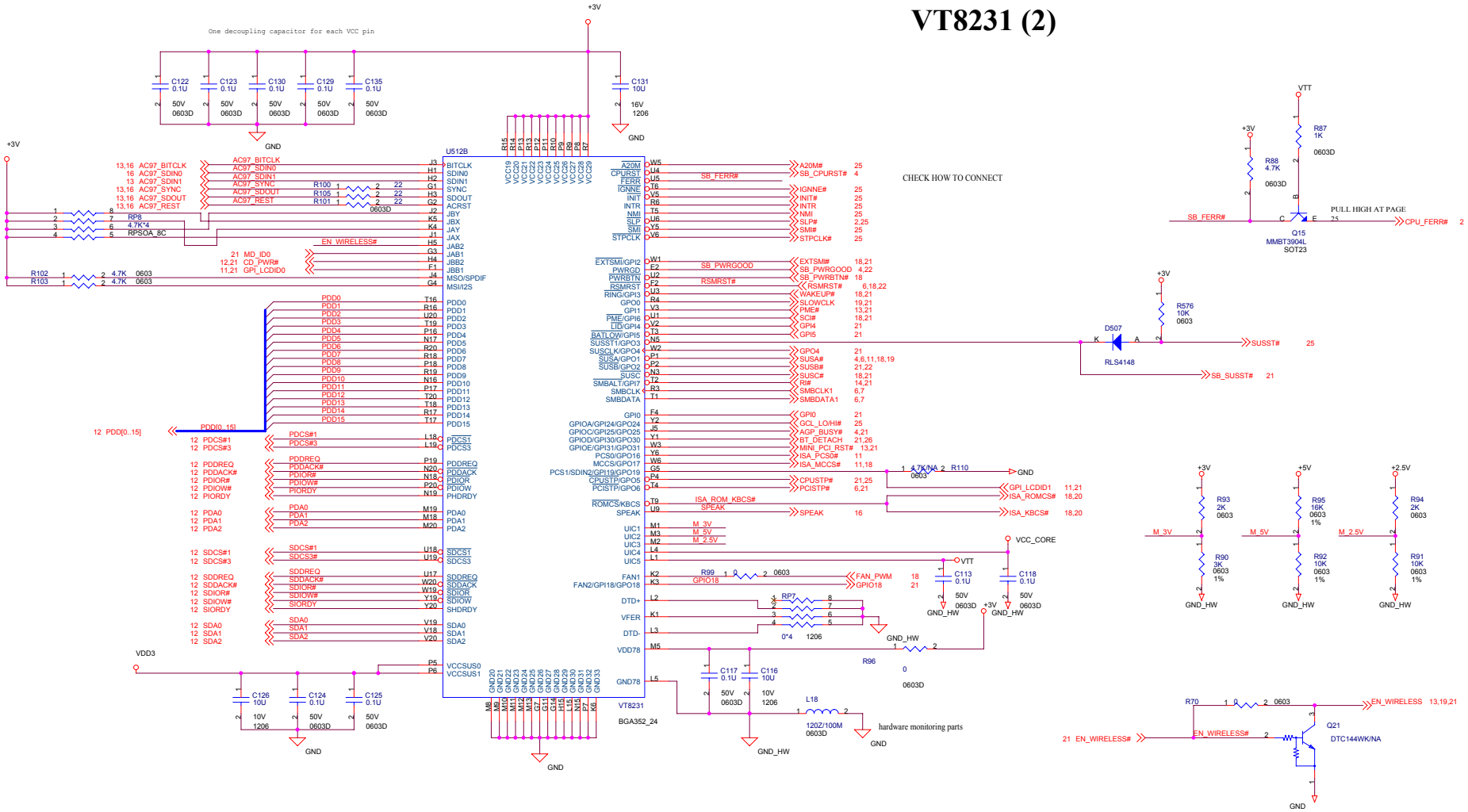
VT8231 (2)



DVT GPIO DEFINITION

PIN#		FUNCTION	POWER	PIN#		FUNCTION	POWER	PIN#		FUNCTION	POWER
F4	GPI0:	RESERVE	RESUME	R4	GPO0:	SLOWCLK	RESUME	K3	GPIO18	RESERVE	MAIN
V3	GPI1:	PME#	RESUME	P1	GPO1:	SUSA#	RESUME	G5	GPIO19	GPI_LCDID1	MAIN
W1	GPI2:	EXTSMI#	RESUME	P2	GPO2:	SUSB#	RESUME	W13	GPIO20	GPI_LCDID2	MAIN
U3	GPI3:	WAKEUP#	RESUME	N5	GPO3:	SUSST#	RESUME	Y13	GPIO21	SPK_OFF	MAIN
V2	GPI4:	RESERVE	RESUME	W2	GPO4:	RESERVE/SUSCLK	RESUME	U7	GPIO22	IOR#	MAIN
T3	GPI5:	RESERVE	RESUME	P4	GPO5:	CPUSTP#	MAIN	T7	GPIO23	IOW#	MAIN
U1	GPI6:	SCI#	RESUME	T4	GPO6:	PCISTP#	MAIN	Y2	GPIO24	(GPIOA) GCL_LO/HI#	MAIN
T2	GPI7:	RI#	RESUME	U6	GPO7:	SLP#	MAIN	J5	GPIO25	(GPIOC) AGP_BUSY#	MAIN
F3	GPI8:	RESERVE	RESUME	W11	GPO8:	HDD_RST	MAIN	R2	GPIO26	CARD_ACT#	RESUME
Y3	GPI9:	MPCIACT#	MAIN	T10	GPO9:	CDROM_RST	MAIN	R1	GPIO27	KBD_US/JP#	RESUME
Y11	GPI10:	CANNOT USE	MAIN	Y10	GPO10:	CARD_SUS#	MAIN	Y1	GPIO30	(GPIOD) BT_DETACH	MAIN
V11	GPI11:	CANNOT USE	MAIN	V10	GPO11:	IR_MODE0	MAIN	W3	GPIO31	(GPIOE) MINI_PCI_RST#	MAIN
U10	GPI12:	CANNOT USE	MAIN	H5	GPO12:	EN_WIRELESS	MAIN				
W10	GPI13:	CANNOT USE	MAIN	H4	GPO13:	CD_PWR#	MAIN	T8	GPIOB	IR_MODE	MAIN
V4	GPI14:	MD_ID1	MAIN	R8	GPO14:	IRTX	MAIN				
Y8	GPI15:	BT_WAKEUP	MAIN	U8	GPO15:	IRRXA	MAIN				
V1	GPI16:	CARD_IN	RESUME	Y6	GPO16:	ISA_PCS0#	MAIN				
P3	GPI17:	THRM#	RESUME	W6	GPO17:	ISA_MCCS#	MAIN				
G3	GPI28:	MD_ID0	MAIN	W4	GPO28:	EN_BL	MAIN				
F1	GPI29:	GPI_LCDID0	MAIN	Y4	GPO29:	HDD_PWR#					

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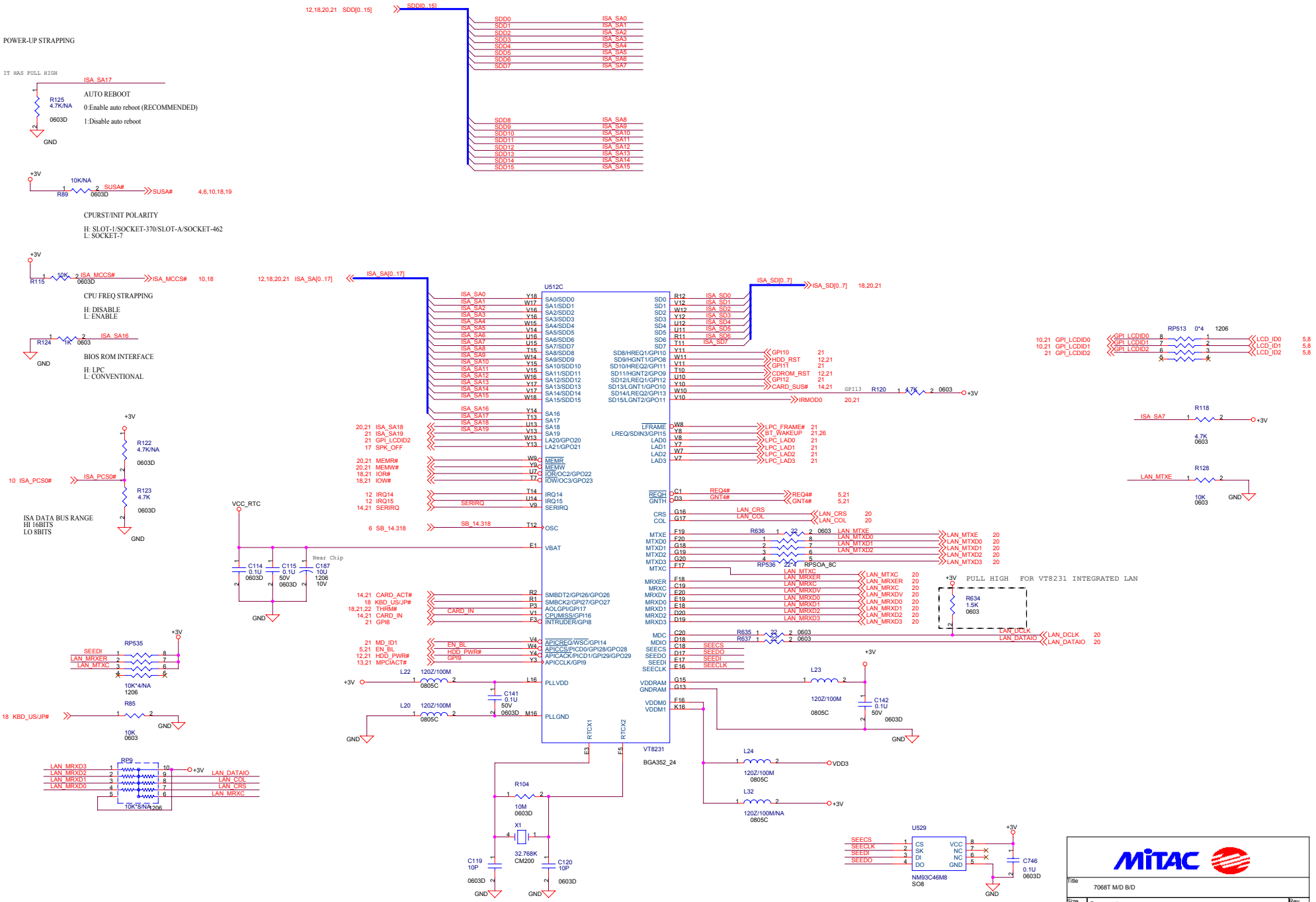
VT8231 (3)



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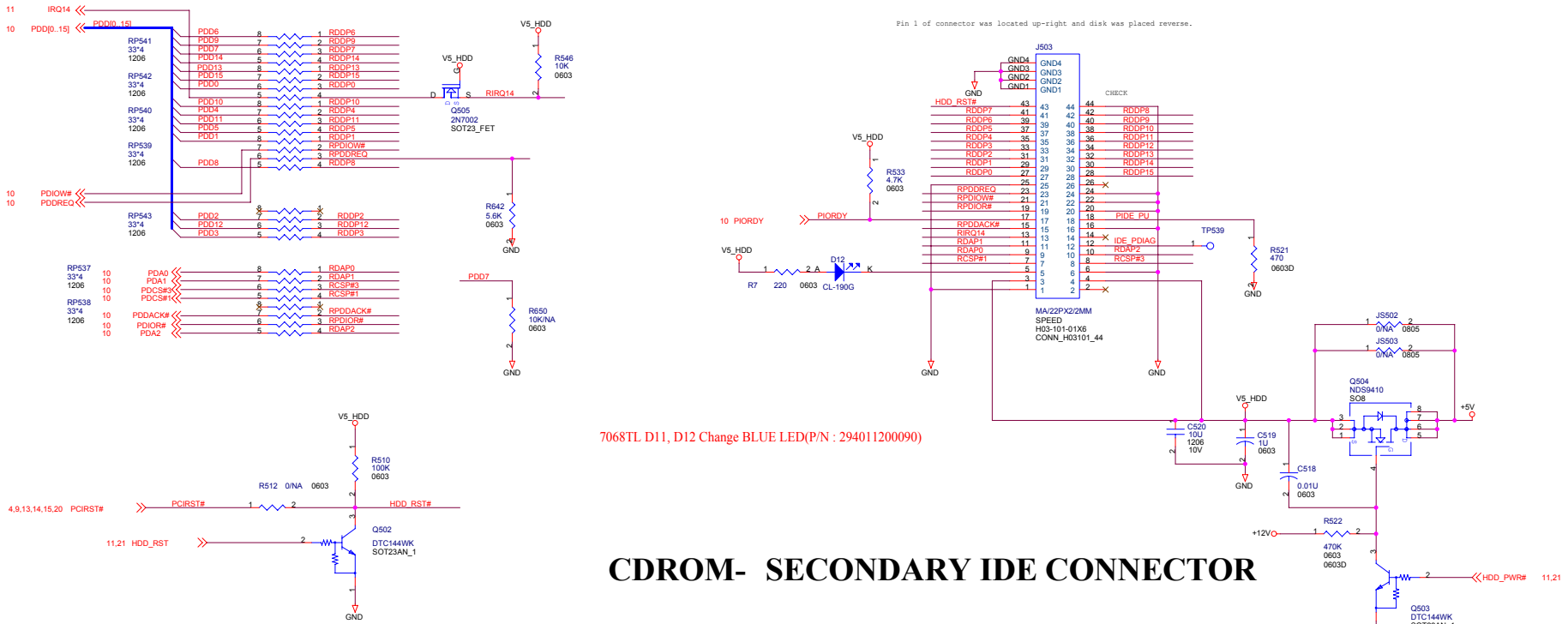
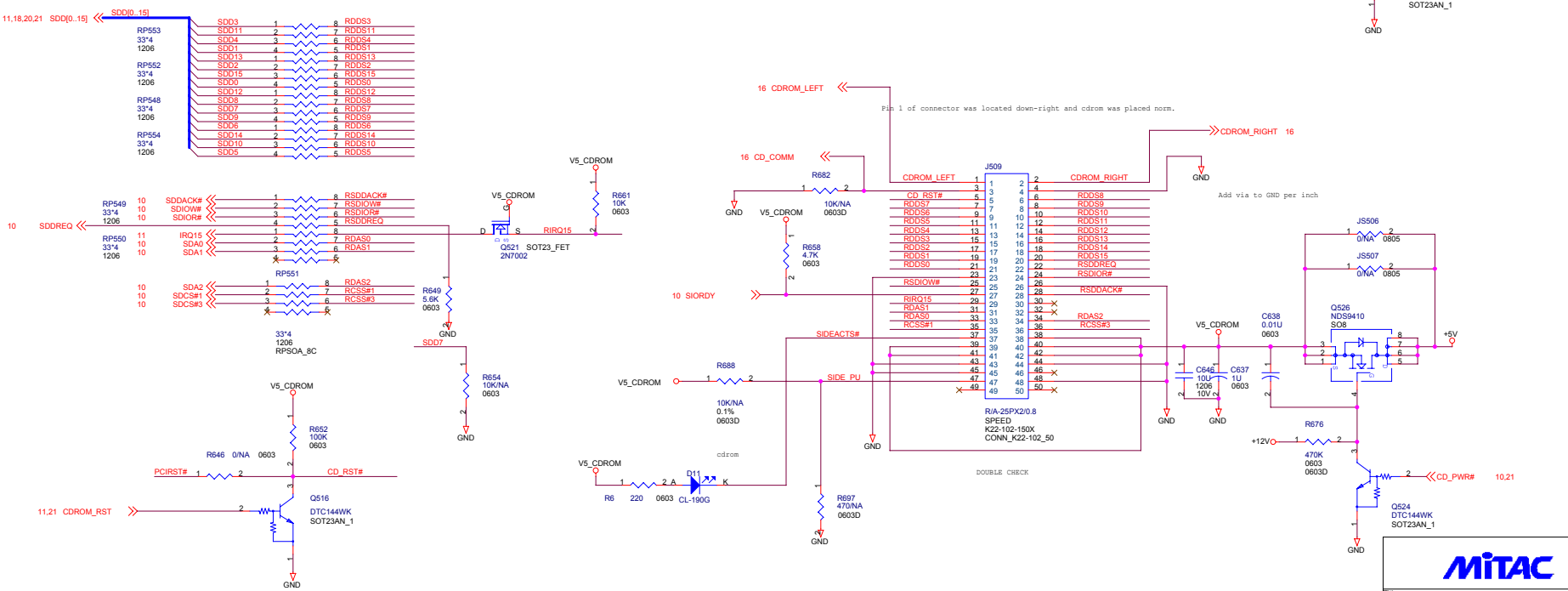
HDD- PRIMARY IDE CONNECTOR



CDROM- SECONDARY IDE CONNECTOR



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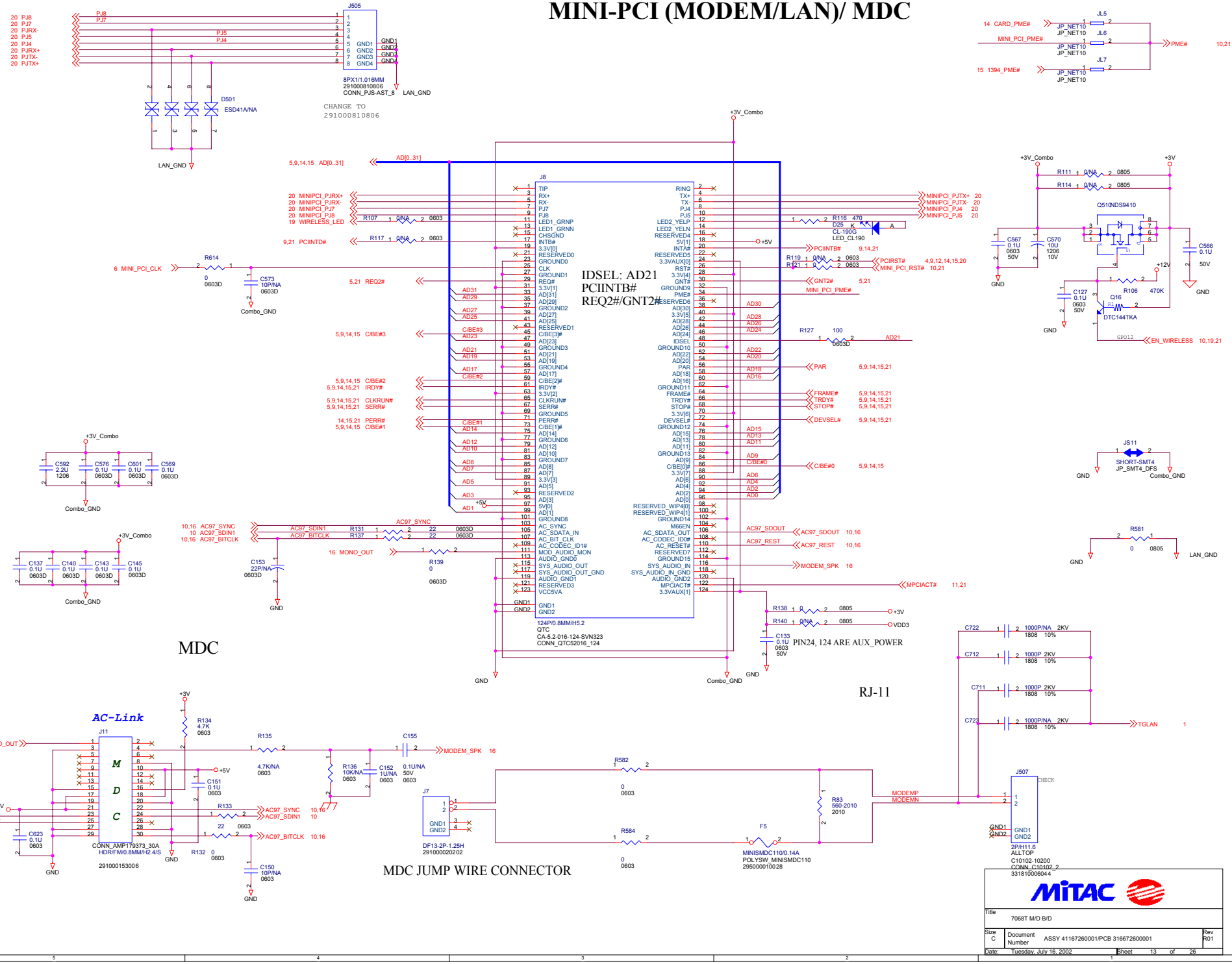
MINI-PCI (MODEM/LAN)/ MDC



CARDBUS CONTROLLER

SIGNAL	PC CARD PULL UP	VOLT
CCD#1	+3V	
CCD#2	+3V	
CBLOCK#	CARD_VCC	
CSTOP#	CARD_VCC	
CDEVSEL#	CARD_VCC	
CTRDY#	CARD_VCC	
CVS1	+3V	
CVS2	+3V	
CRST#	CARD_VCC	
CSERR#	CARD_VCC	
CPERR#	CARD_VCC	
CINT#	CARD_VCC	
CIRDY#	CARD_VCC	
CREQ#	CARD_VCC	
CSTSCHG#	CARD_VCC	
CAUDIO	CARD_VCC	

SEND THE SCHEMATIC TO TI FAE DOUBLE CHECK

PCI1410 HAVE INTEGRATED ALL PULL UP RES ABOVE

FOR TI 1410

PCI1410

IDSEL: AD19

PCIINTB#

REQ0#/GNT0#

U513

CB1410

PQFP144_0.5MM

U510

TPS2211

SSOP16

J508

FM/34X2P/H7.65

JAE JC21BRB20

ICRD_JC21BRB20_68A

ONLY FOR OZ6812

MiTAC

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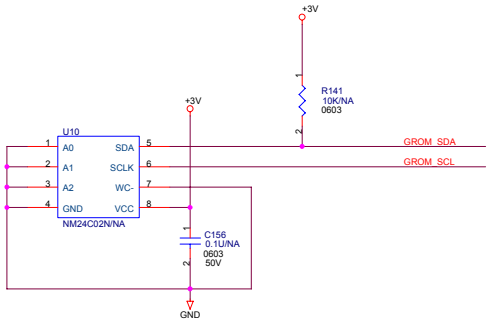
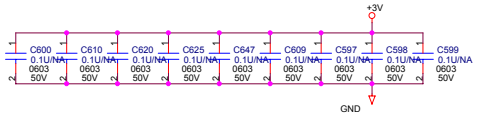
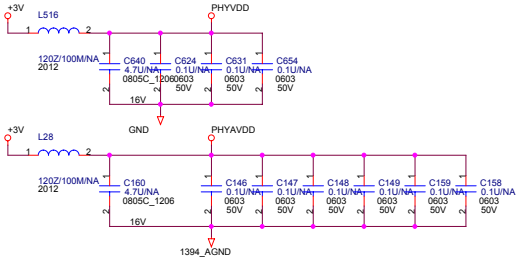
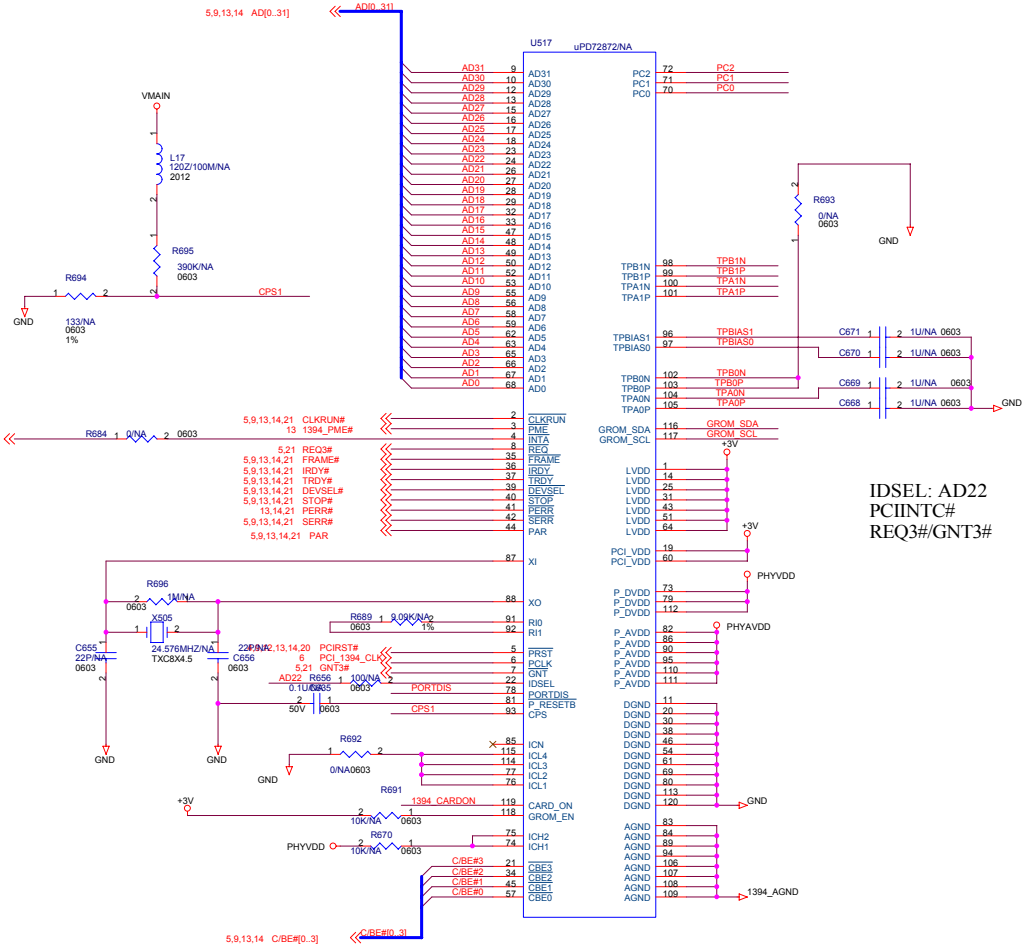
IEEE1394- UPD72872



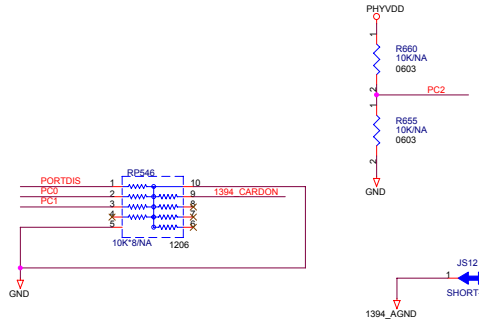


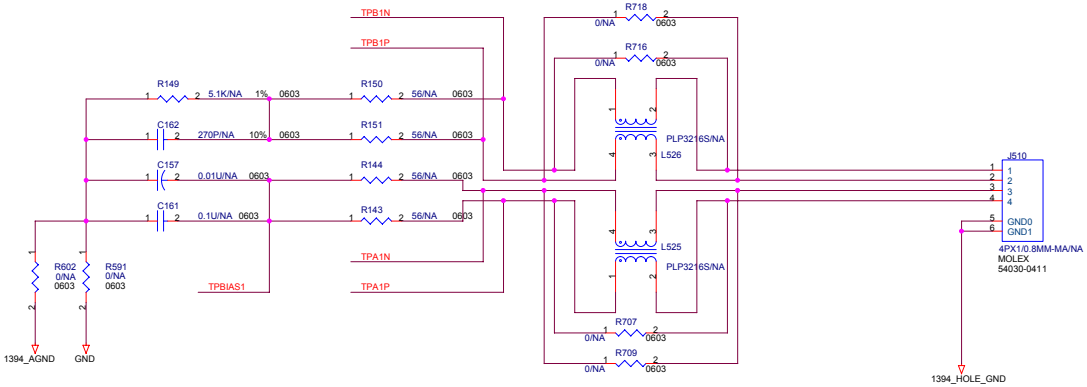


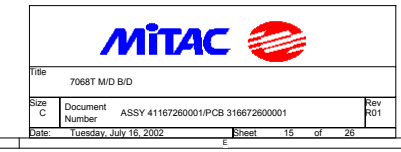
DEVICE:= C:\O1394DRV.SYS IN CONFIG.SYS



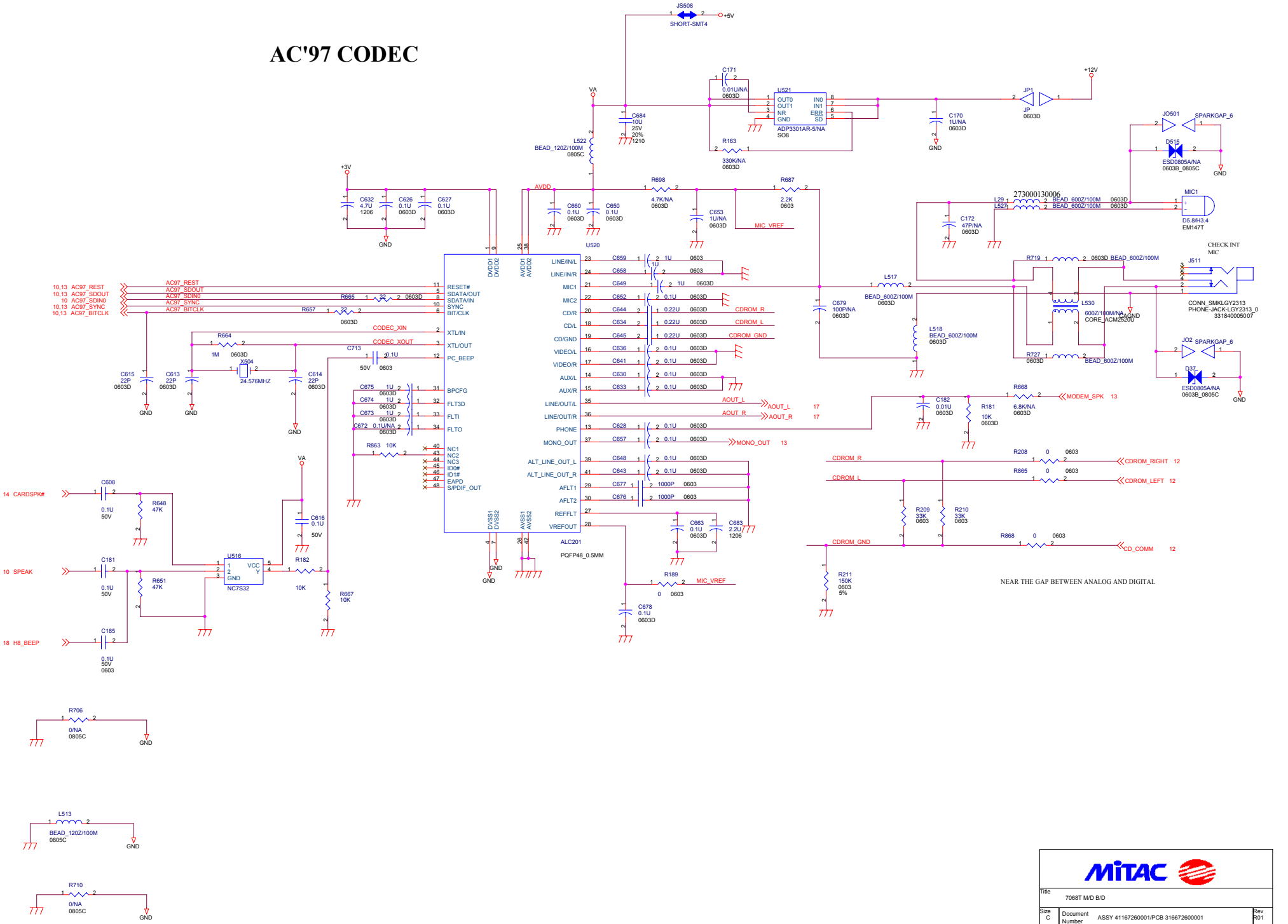
IDSEL: AD22
PCIINTC#
REQ3#/GNT3#







AC'97 CODEC



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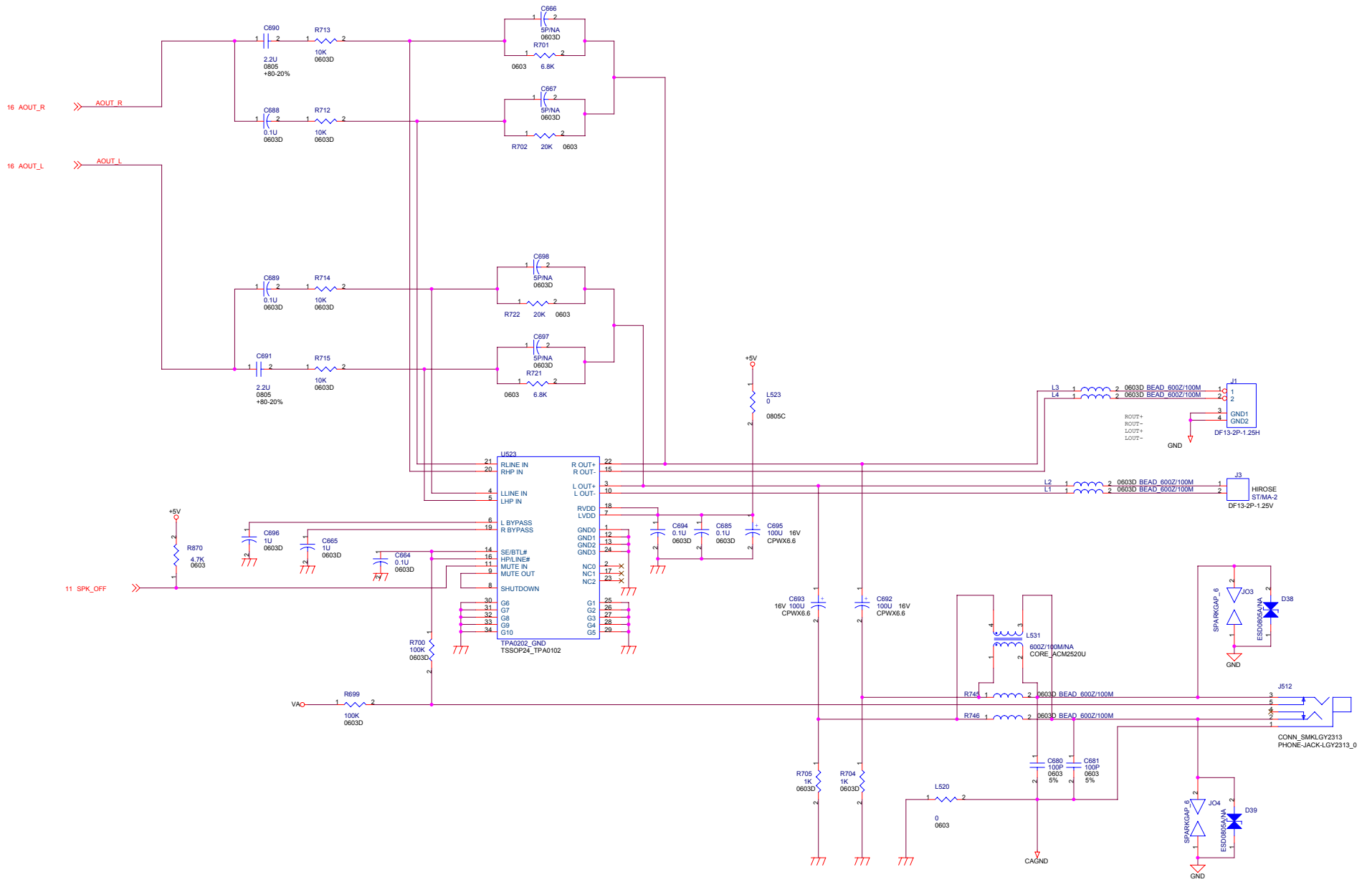
AUDIO AMPLIFIER - TPA0202



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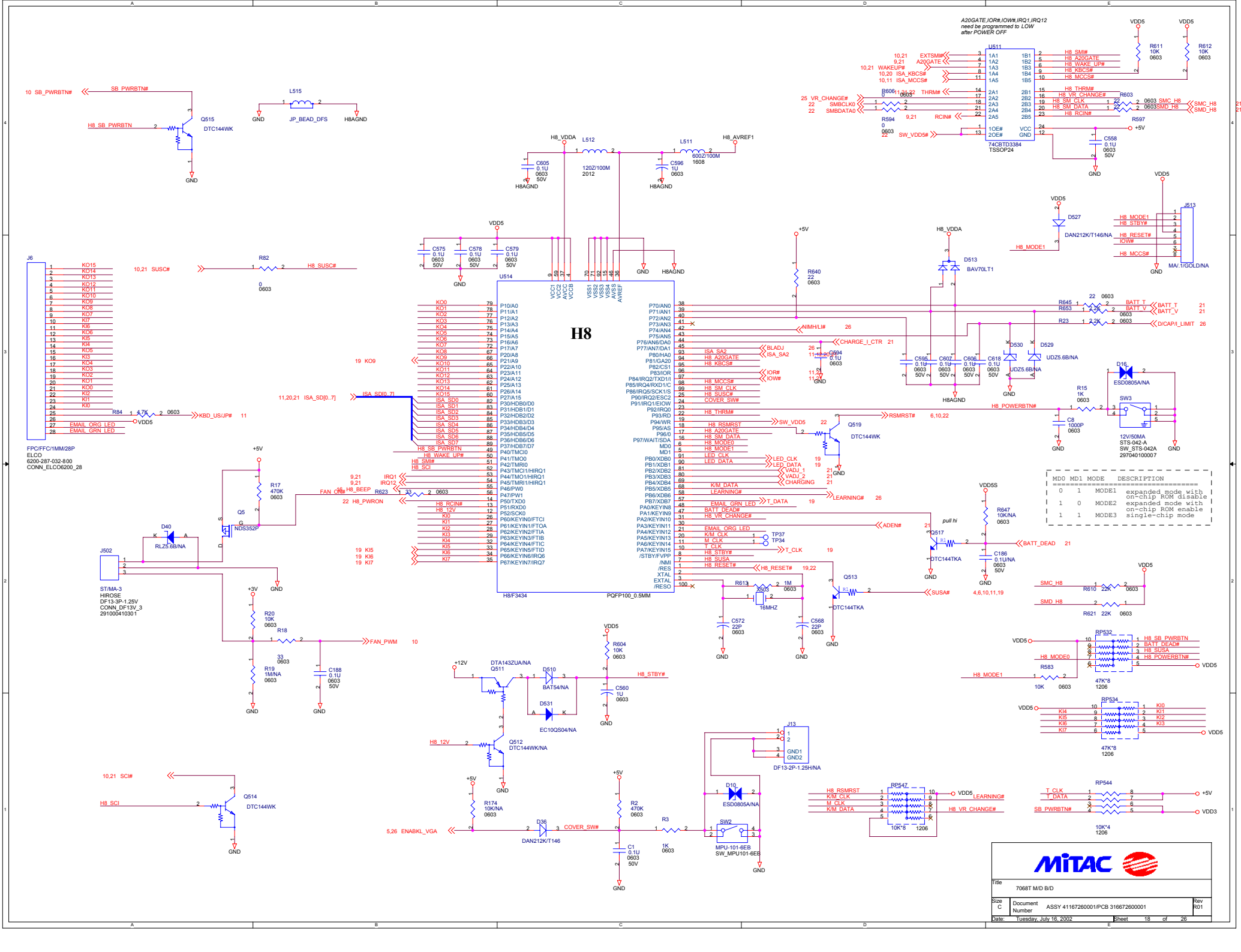
A20GATE,IOR#,IOW#,IRQ1,IRQ12
need be programmed to LOW
after POWER OFF
H8
H8/F3434
PQFP100_0.5MM
U511
74CBTD3384
TSSOP24
U514
J6
FPC/FFC/1MM/28P
ELCO
6200-287-032-800
CONN_ELCO6200_28
J502
ST/MA-3
HIROSE
DF13-3P-1.25V
CONN_DF13V_3
291000410301
J513
MA/.1/GOLD/NA
J13
DF13-2P-1.25H/NA
SW3
12V/50MA
STS-042-A
SW_STS-042A
297040100007
SW2
MPU-101-6EB
SW_MPU101-6EB
X503
16MHZ
MD0 MD1 MODE DESCRIPTION
0 1 MODE1 expanded mode with on-chip ROM disable
1 0 MODE2 expanded mode with on-chip ROM enable
1 1 MODE3 single-chip mode
MiTAC
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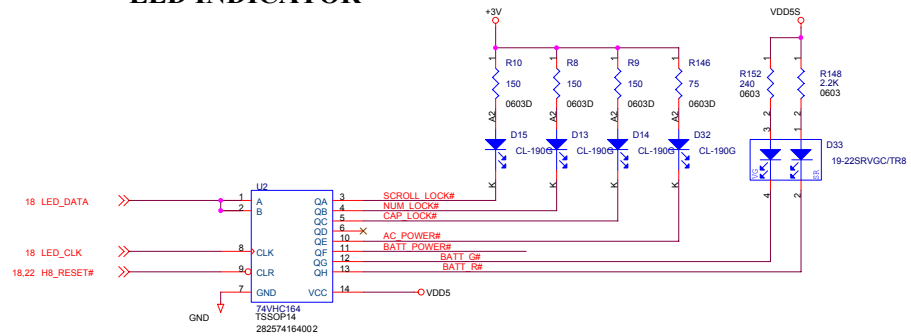
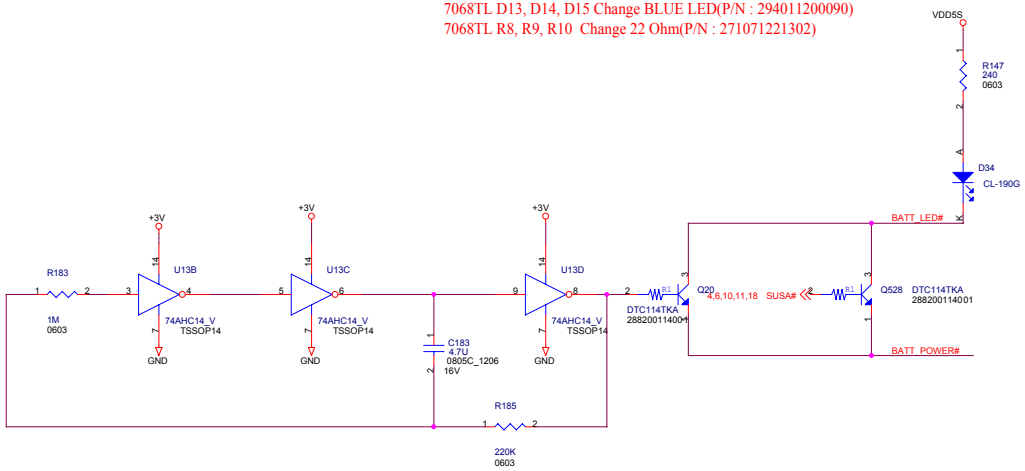
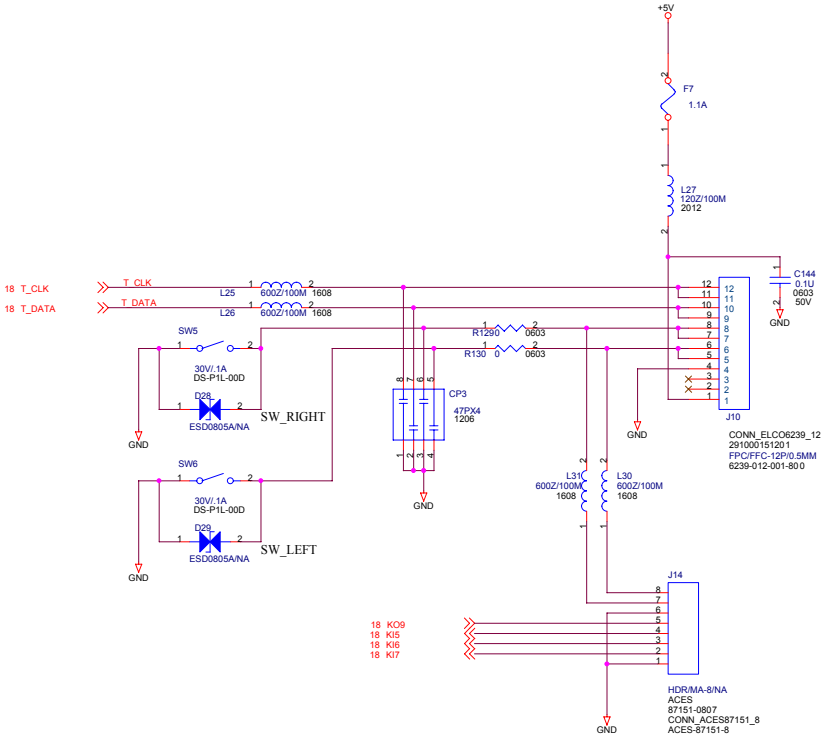
LED INDICATOR



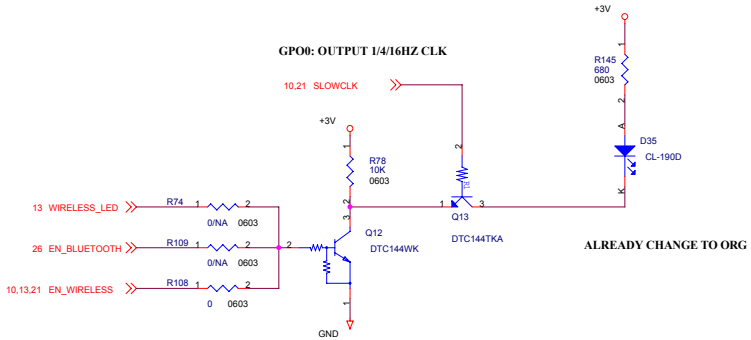
7068TL D13, D14, D15 Change BLUE LED(P/N : 294011200090)
7068TL R8, R9, R10 Change 22 Ohm(P/N : 271071221302)



TOUCH_PAD



WIRELESS LED



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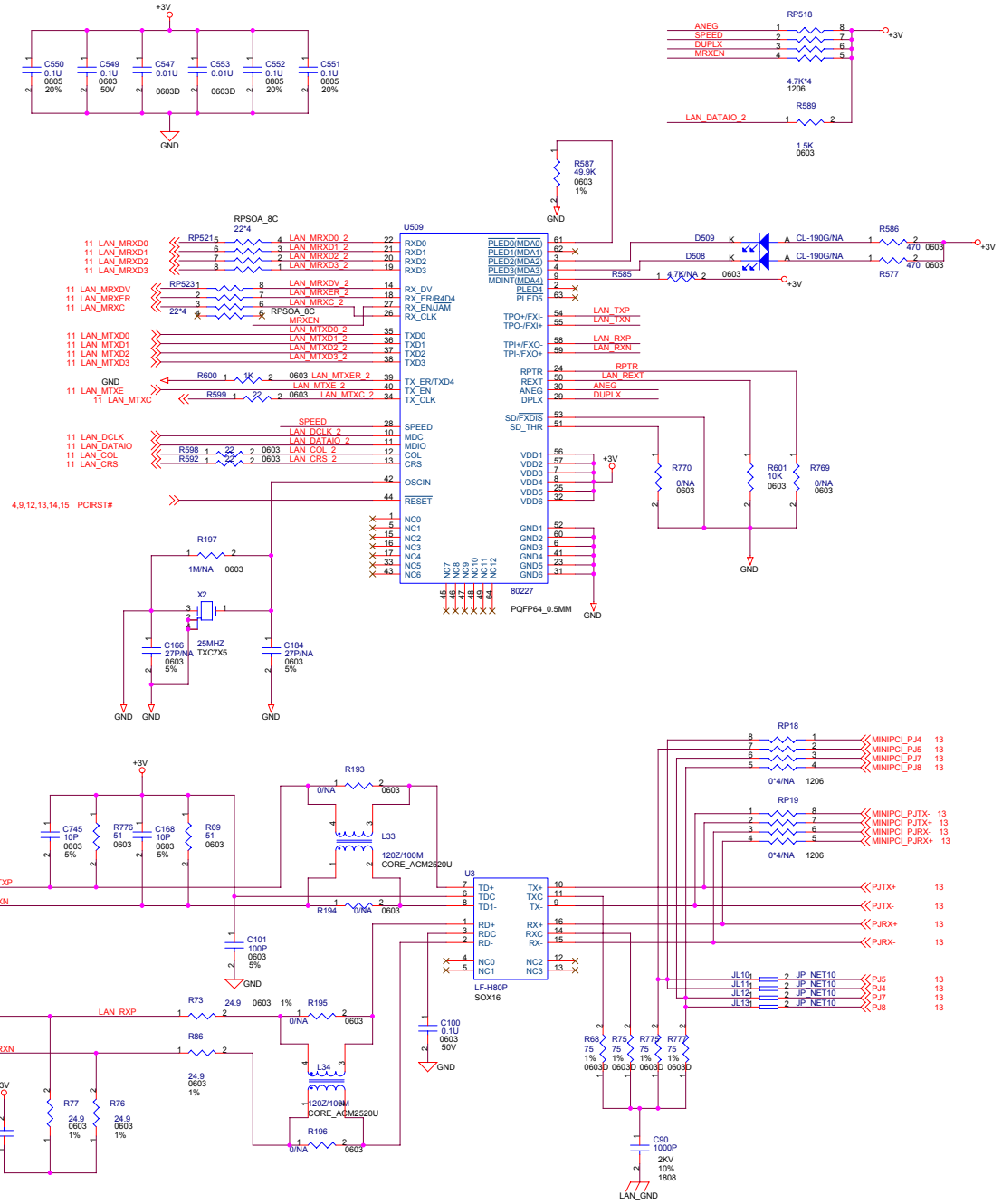
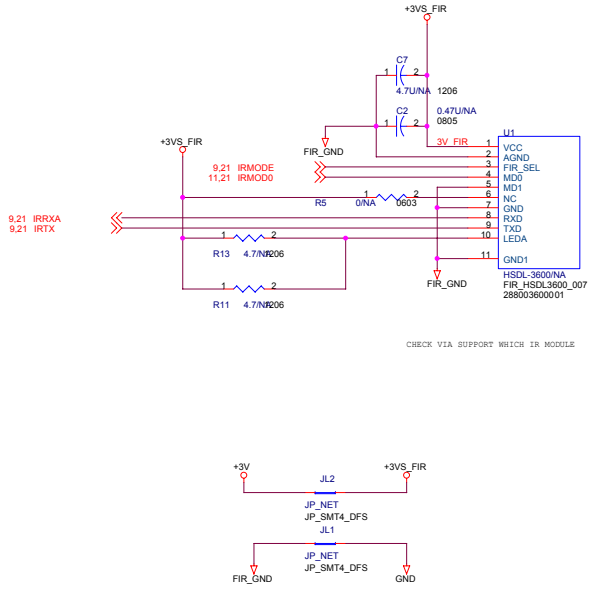
LAN PHY-LSI80227

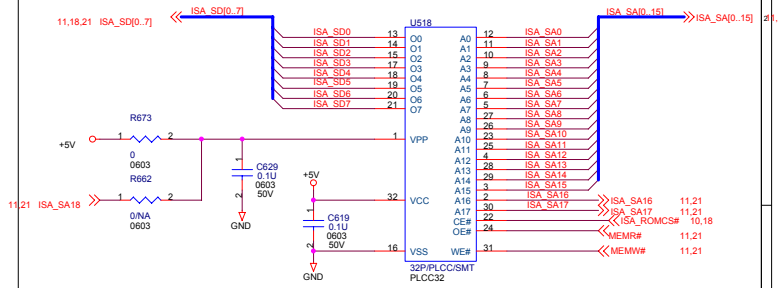


IR MODULE

HP FIR MODULE HSDL-3600#007



SYSTEM BIOS



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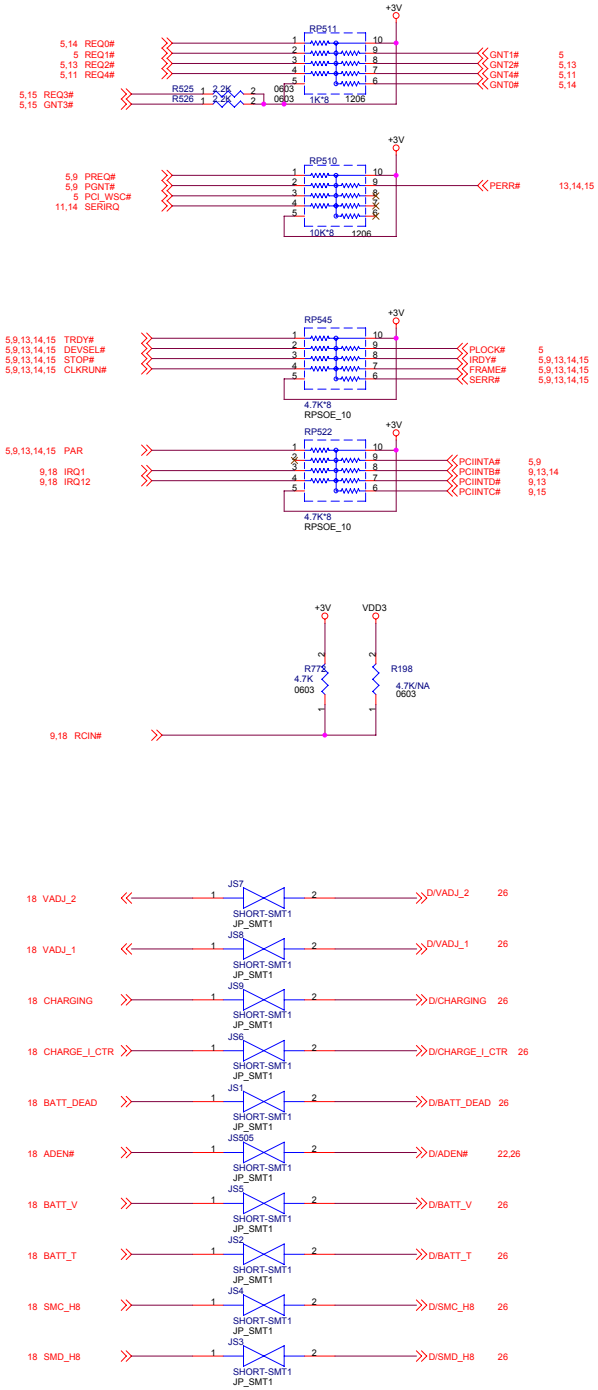
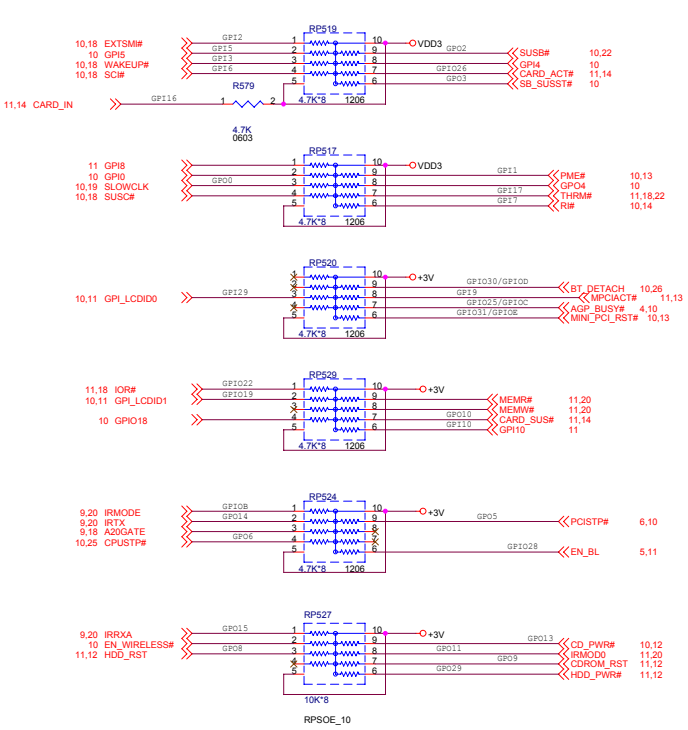
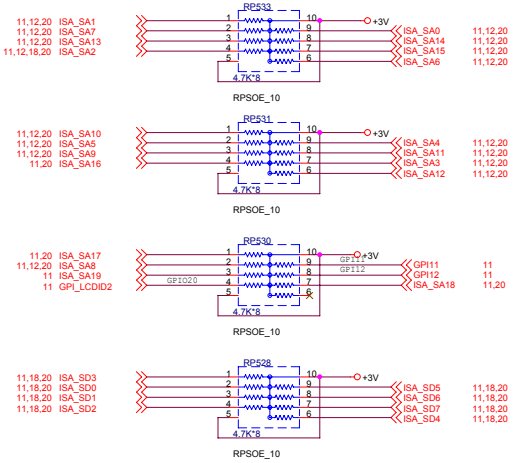
PCI PULL-HIGH



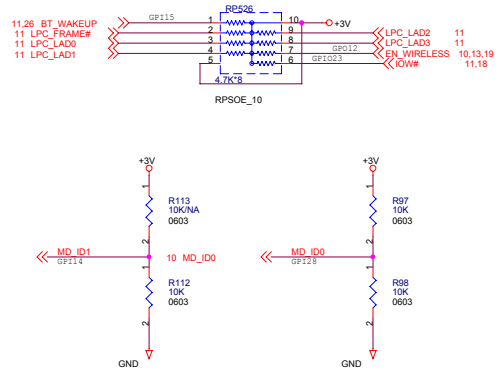
GPIO- PULL HIGH



ISA-PULL HIGH



LPC-RESERVE-PULL HIGH



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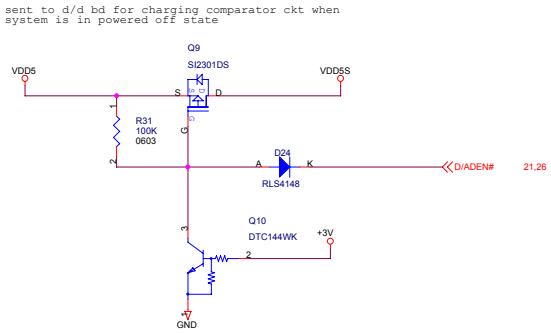
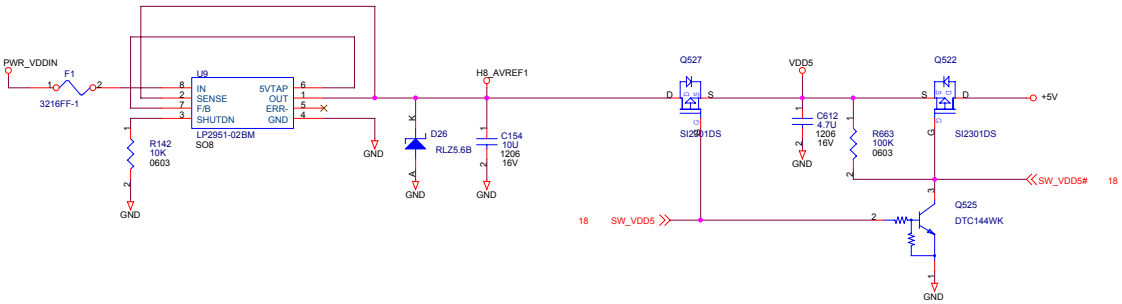
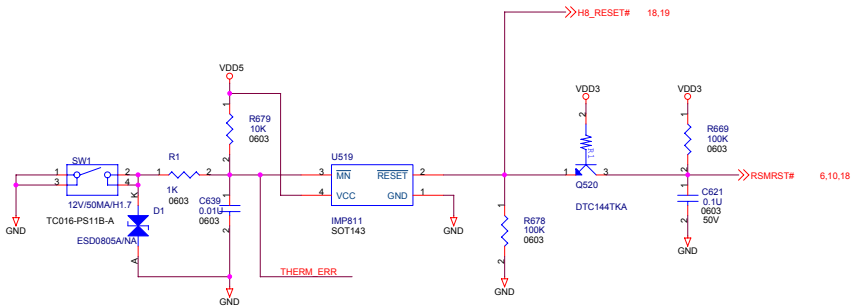
VDD5S



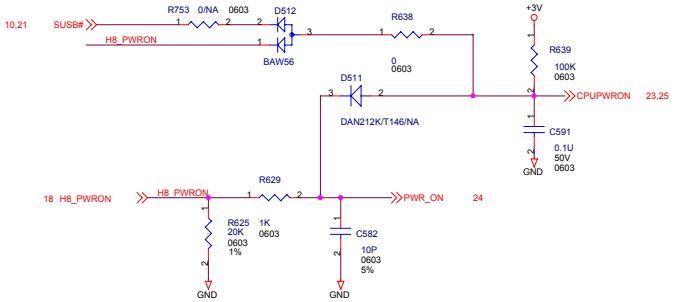
VDD5



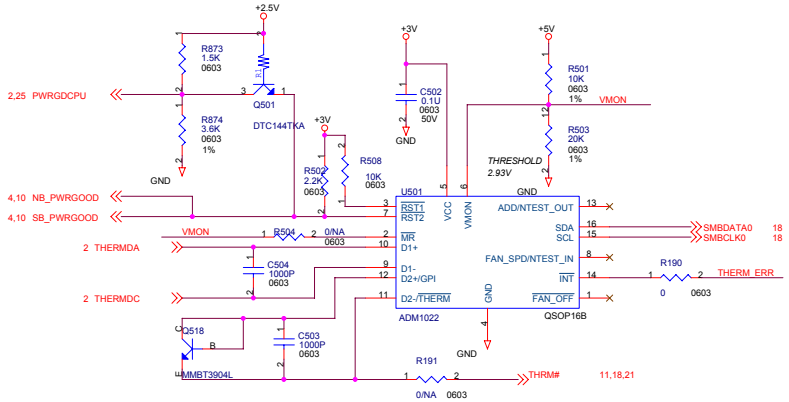
H8 RESERT



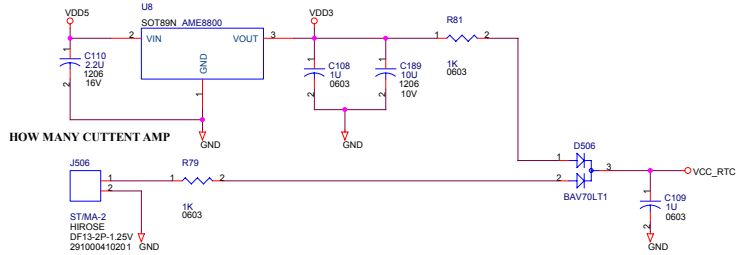
POWER ON



POWER OK



RTC BATTERY CONNECTOR



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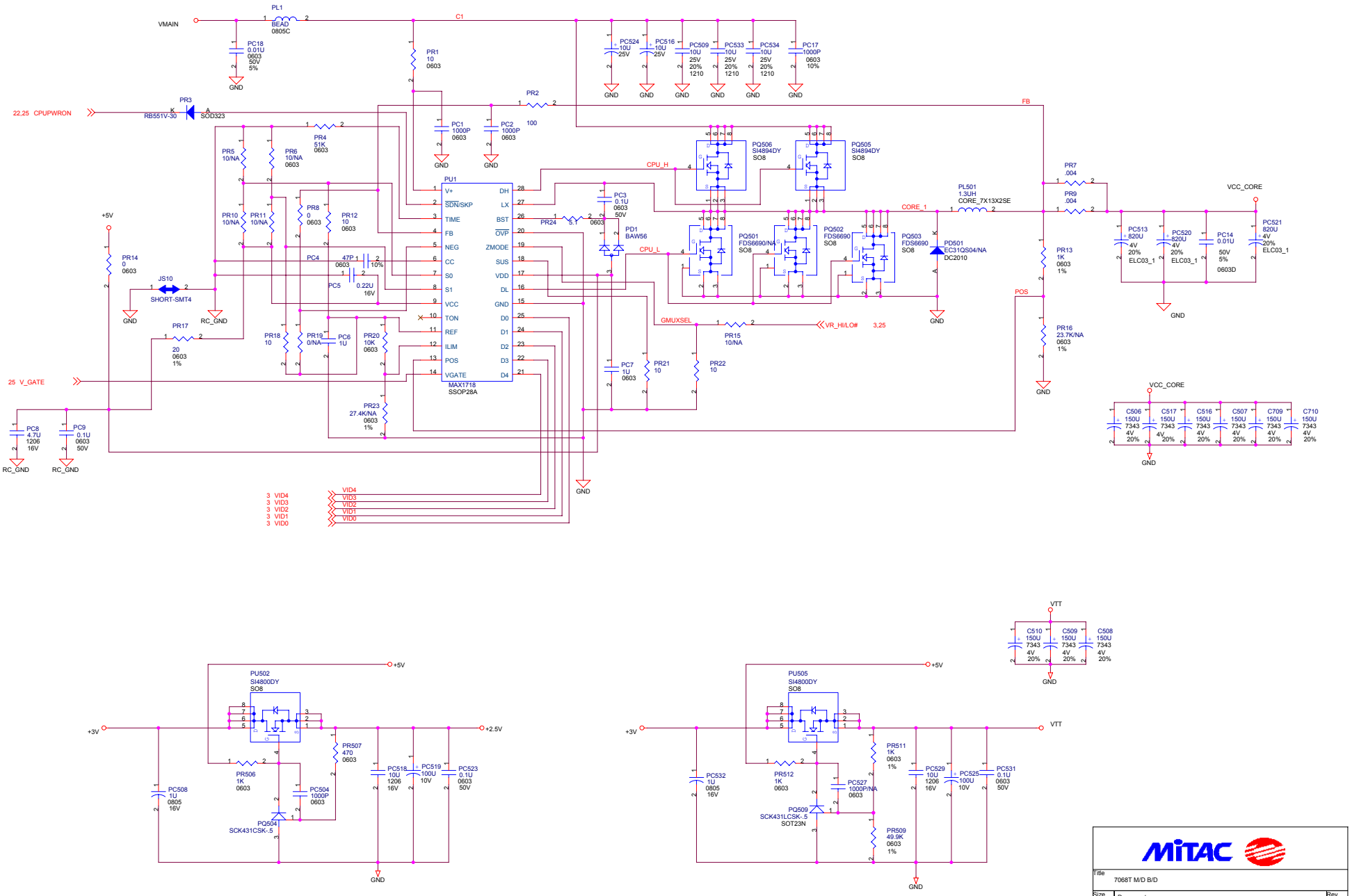
CPU_CORE/+2.5V/VTT



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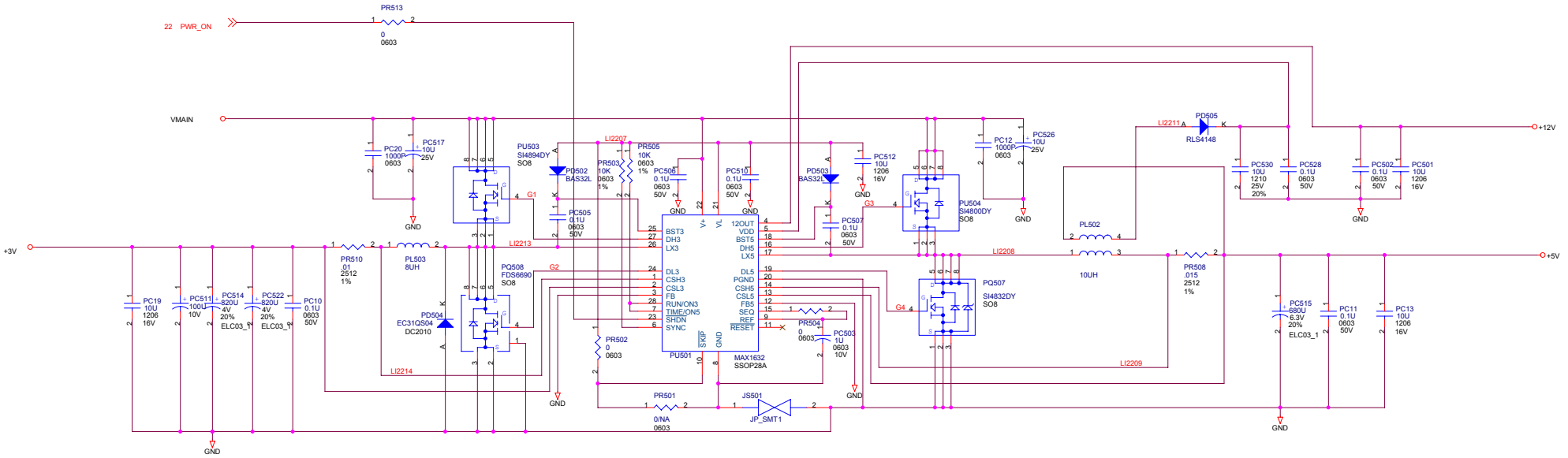
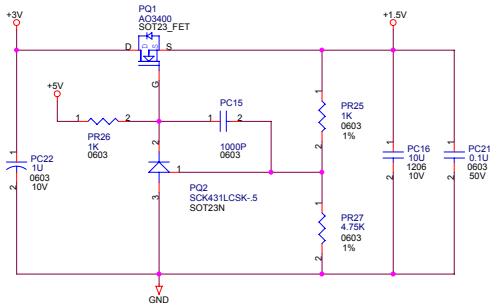
+1.5V/+3V/+5V/+12V





MiTAC

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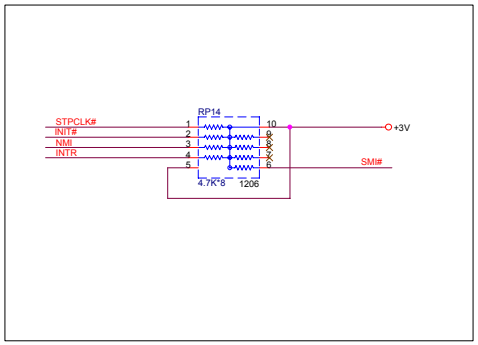
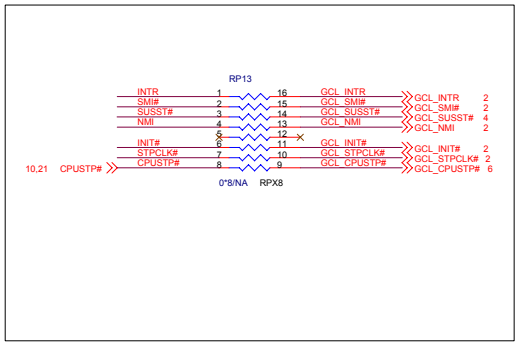
GEYSERVILLE CONTROL LOGIC

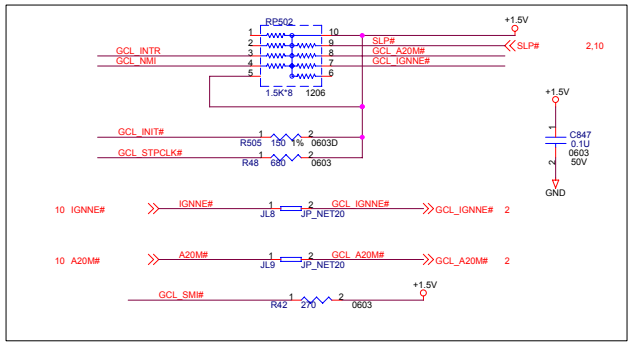
W/GEYSERVILLE MOUNTED THIS RES ARRAY

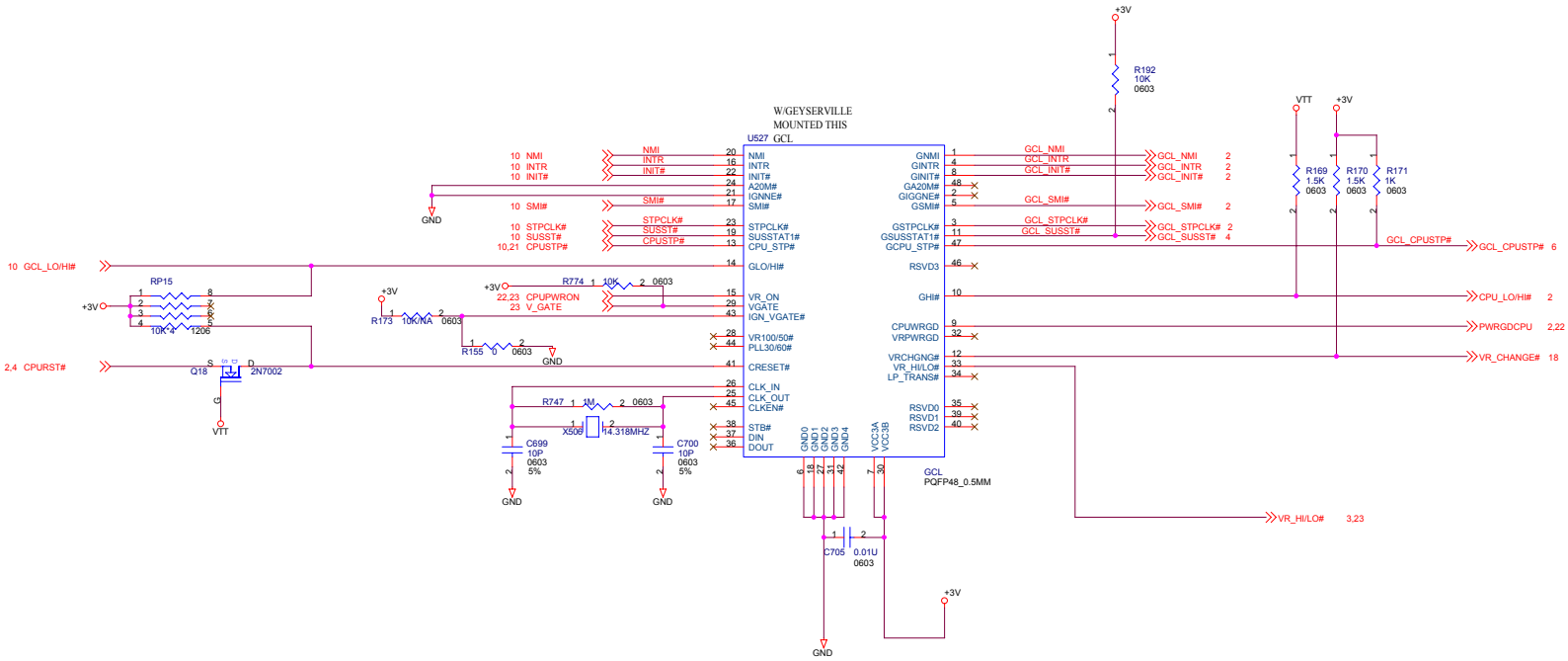


W/O GEYSERVILLE MOUNTED THIS RES ARRAY



UNCONDITIONAL MOUNTED THIS RES ARRAY





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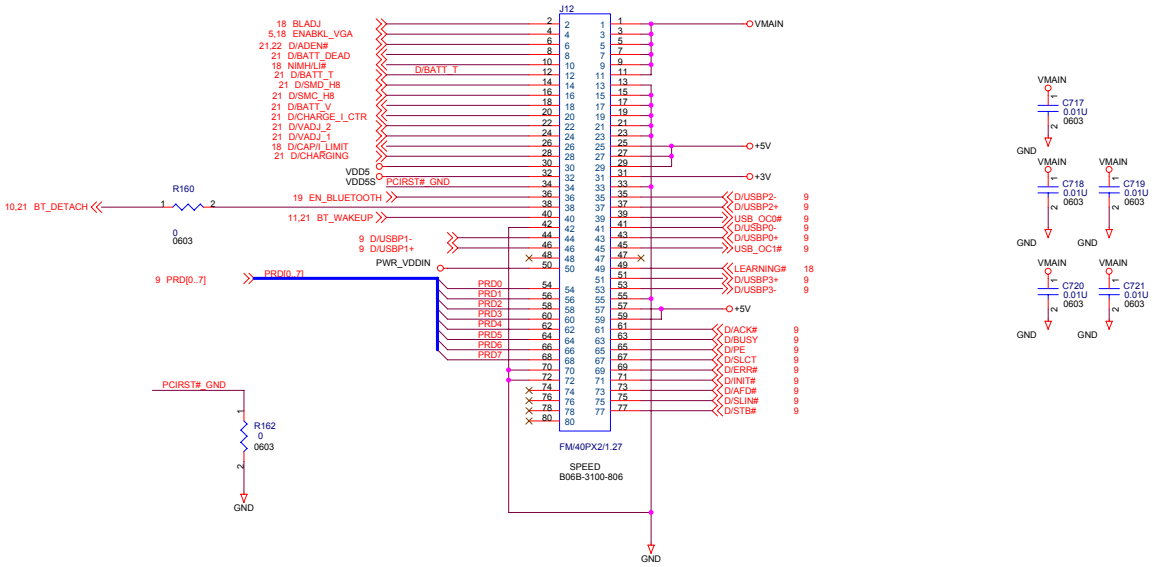

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