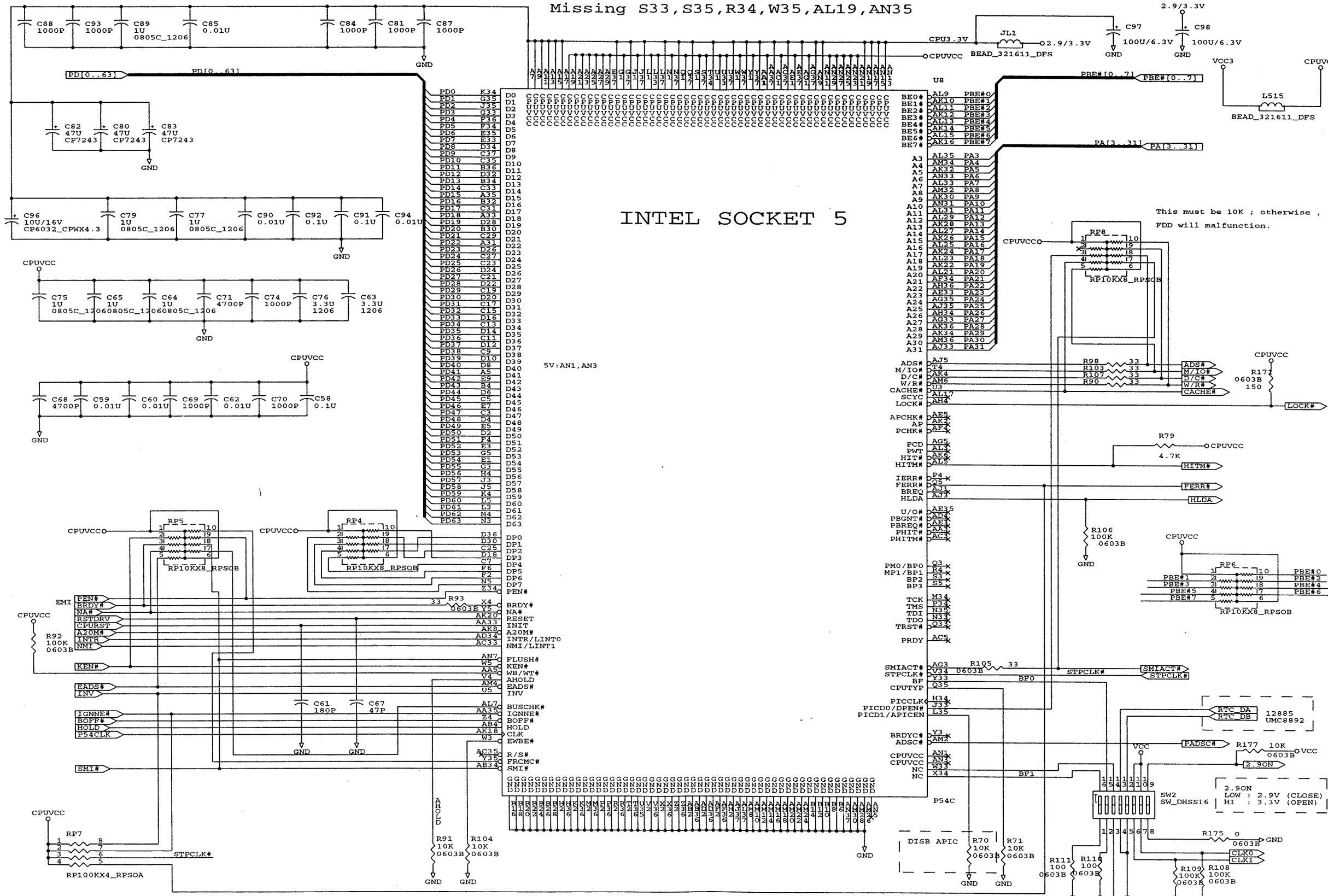


Missing S33, S35, R34, W35, AL19, AN35



INTEL SOCKET 5

5V: AN1, AN3

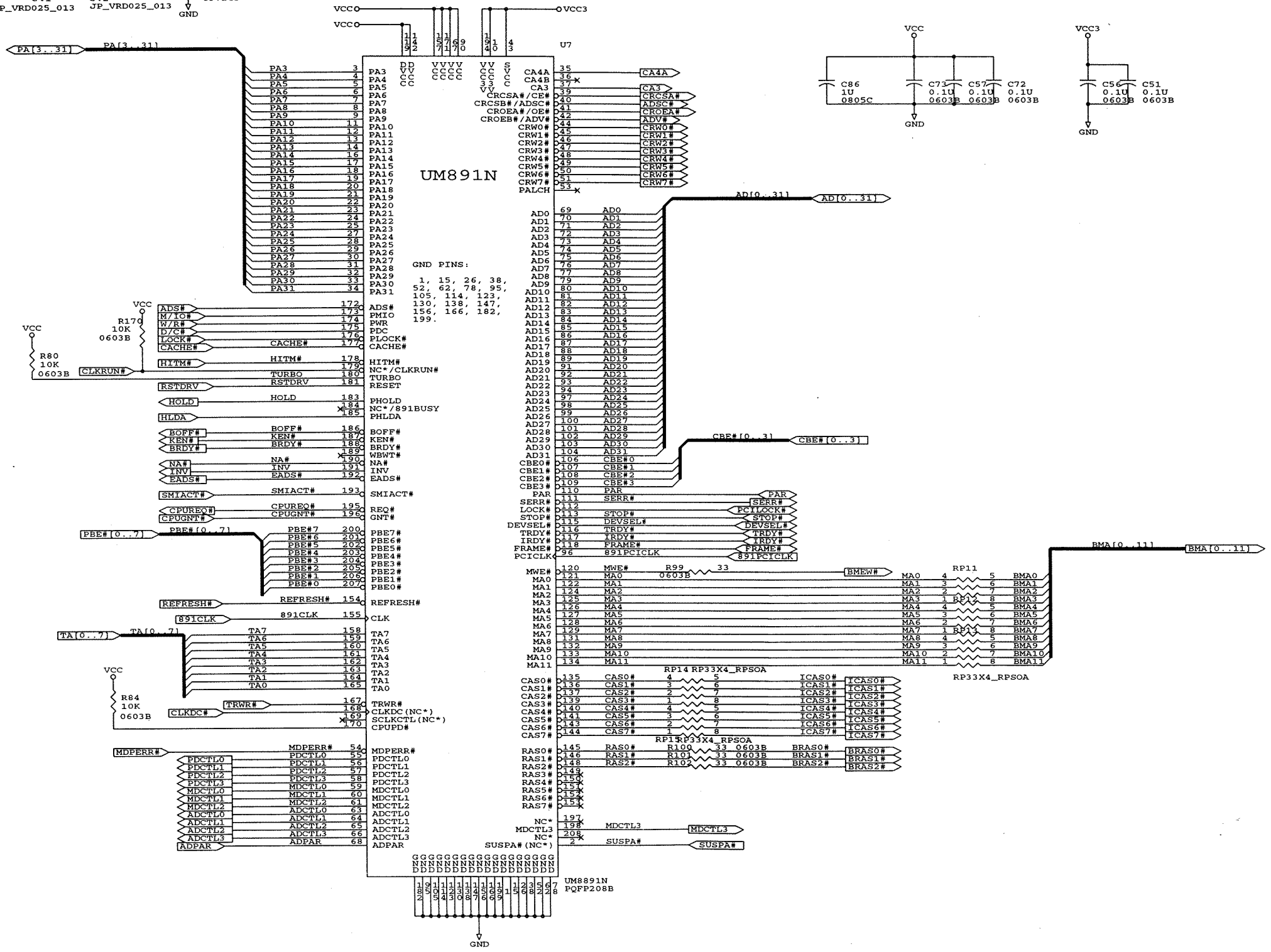
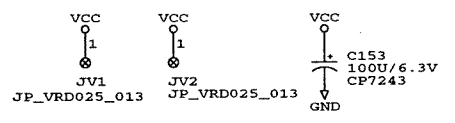
This must be 10K; otherwise, FDD will malfunction.

CPUVCC MAY NEED STRONG PULL

CLOCK RATIO SEL				FREQUENCY SELECTION			
BF1	BF0	P54CS	P55C	CLK1	CLK0	MHz	
0	0	275	275	OFF	OFF	50	
0	1	1/2	---	OFF	ON	20	
1	0	1/2	---	ON	OFF	66.66	
1	1	2/3	---	ON	ON	50	



FOR VCC PIN142/119

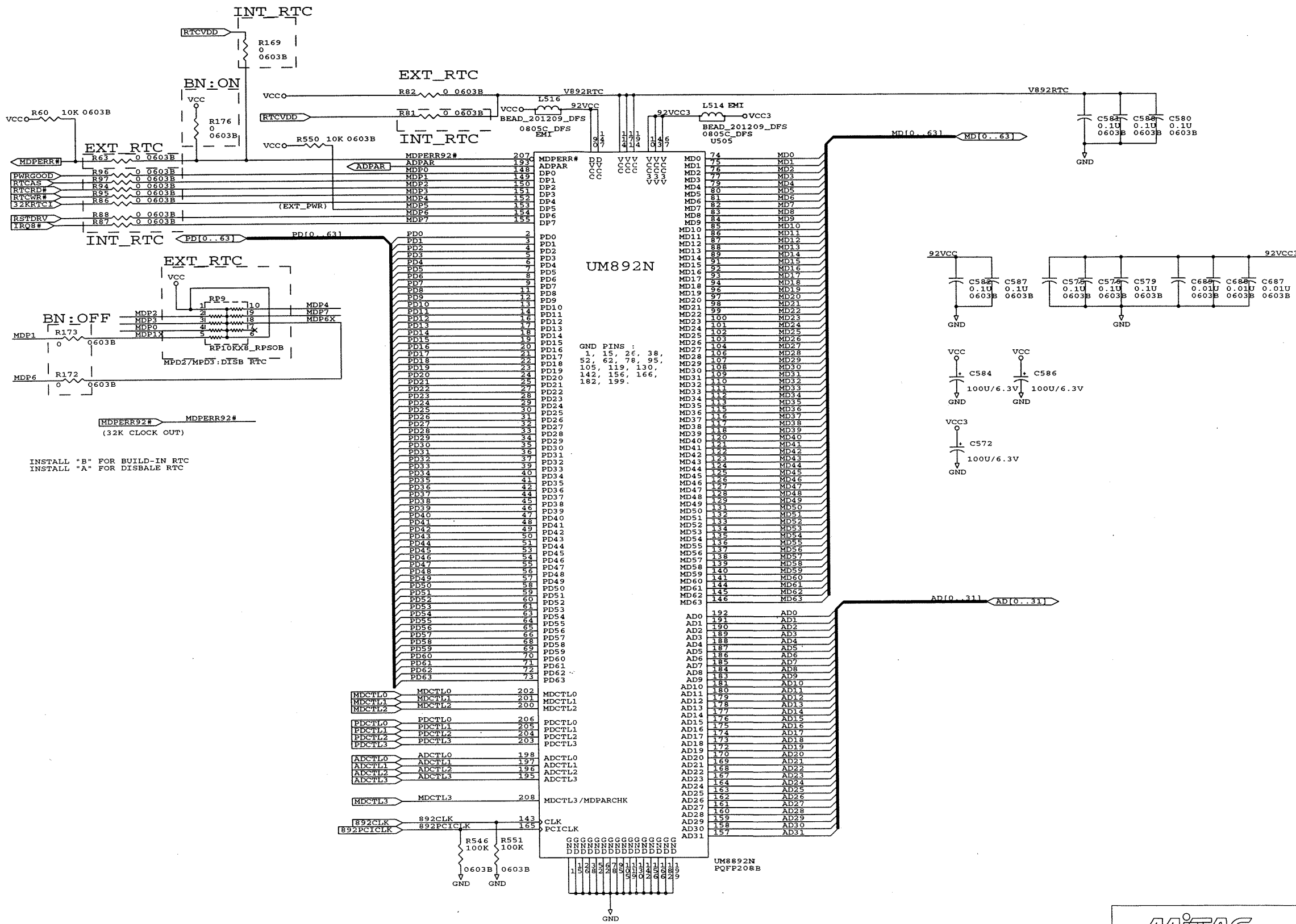


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Size: Document Number: SD41166440001

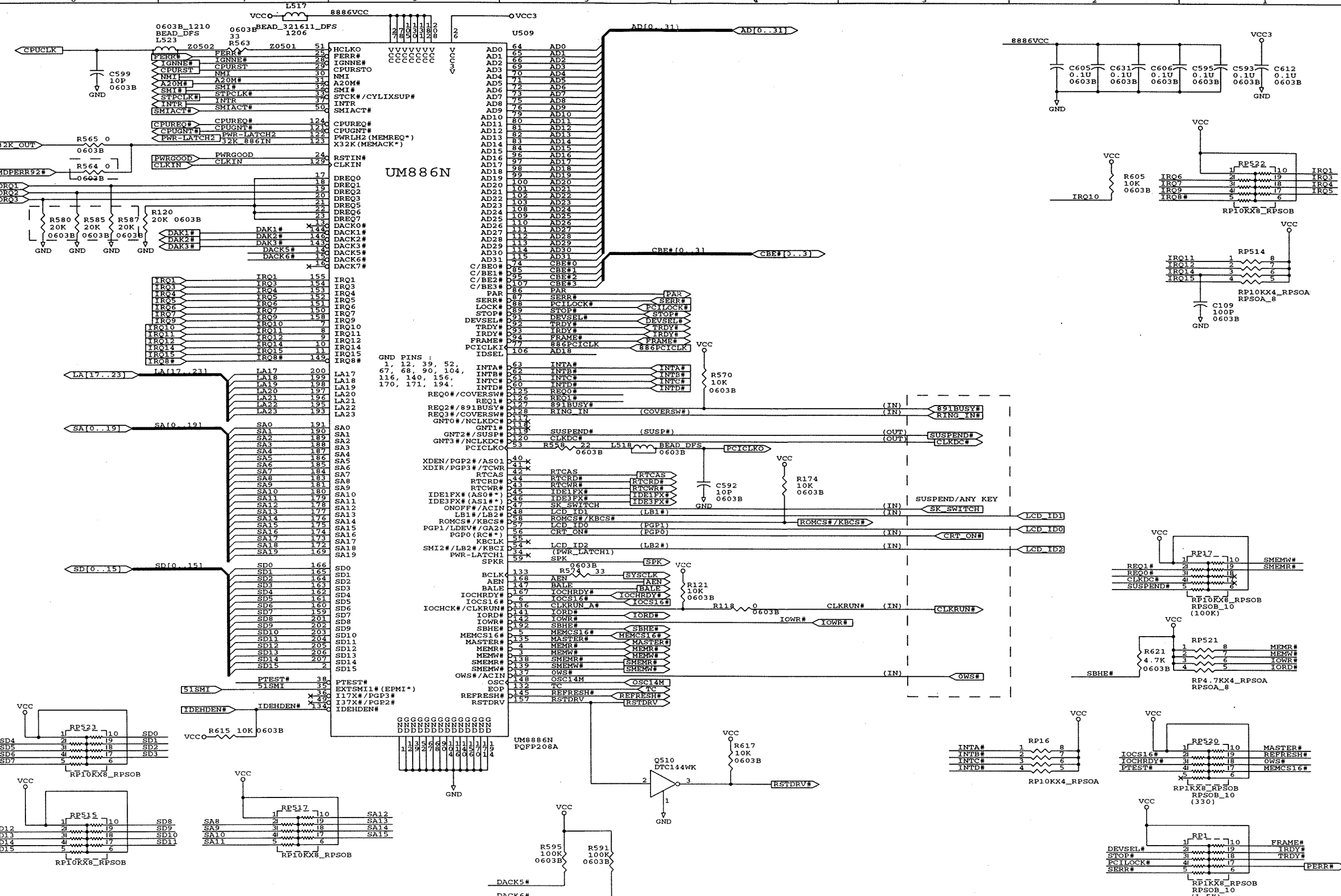
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UM892N

GND PINS :
 1, 15, 26, 38,
 52, 62, 78, 95,
 105, 119, 130,
 142, 156, 166,
 182, 199.

INSTALL "B" FOR BUILD-IN RTC
 INSTALL "A" FOR DISBALE RTC



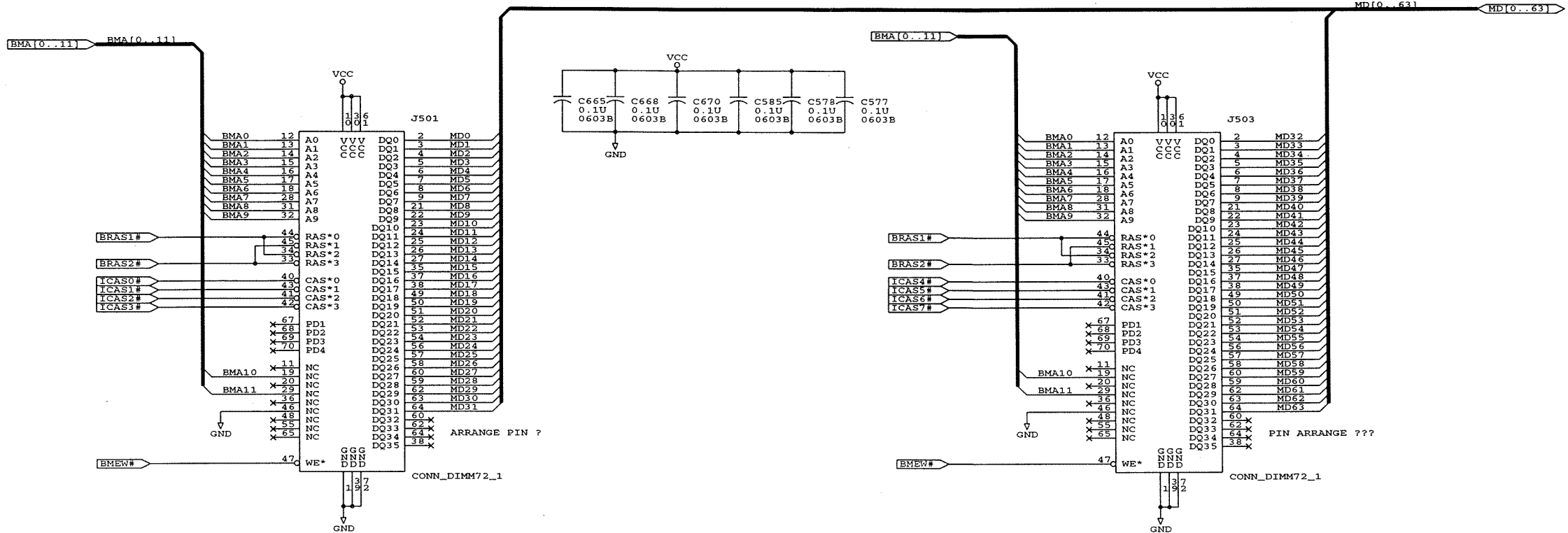
CONFIGURATION



DIMM 0

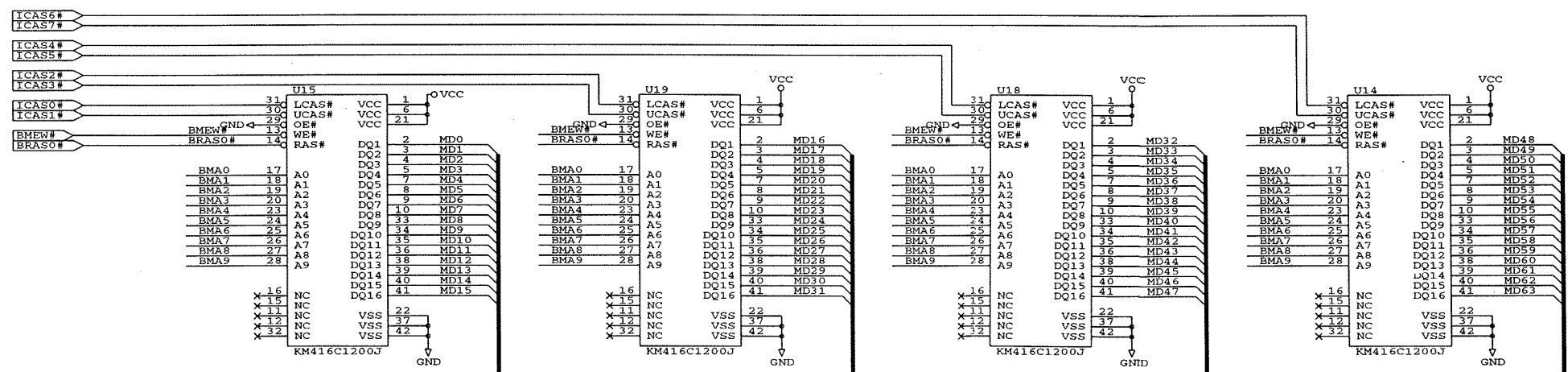
DIMM SOCKET

DIMM 1

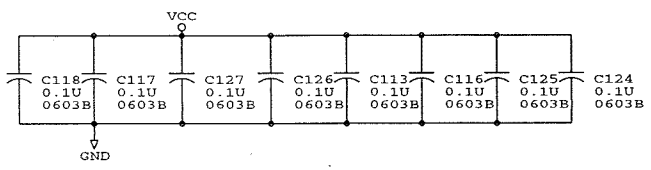


BANK 1 & 2 : LOW 32 BITS

BANK 1 & 2 : HIGH 32 BITS



BANK 0 (ON-BOARD)

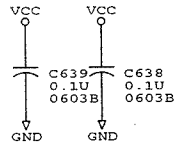
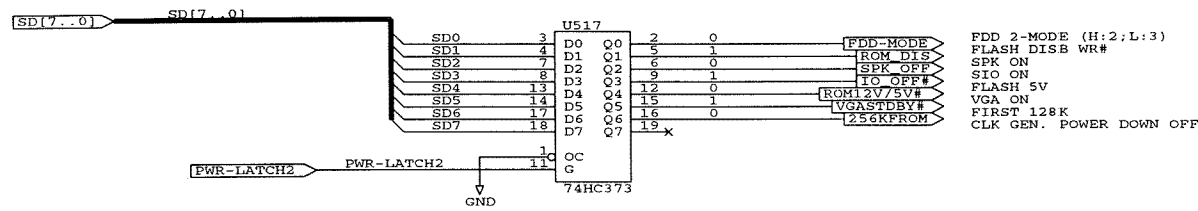


MD[0..63]

MD[0..63]

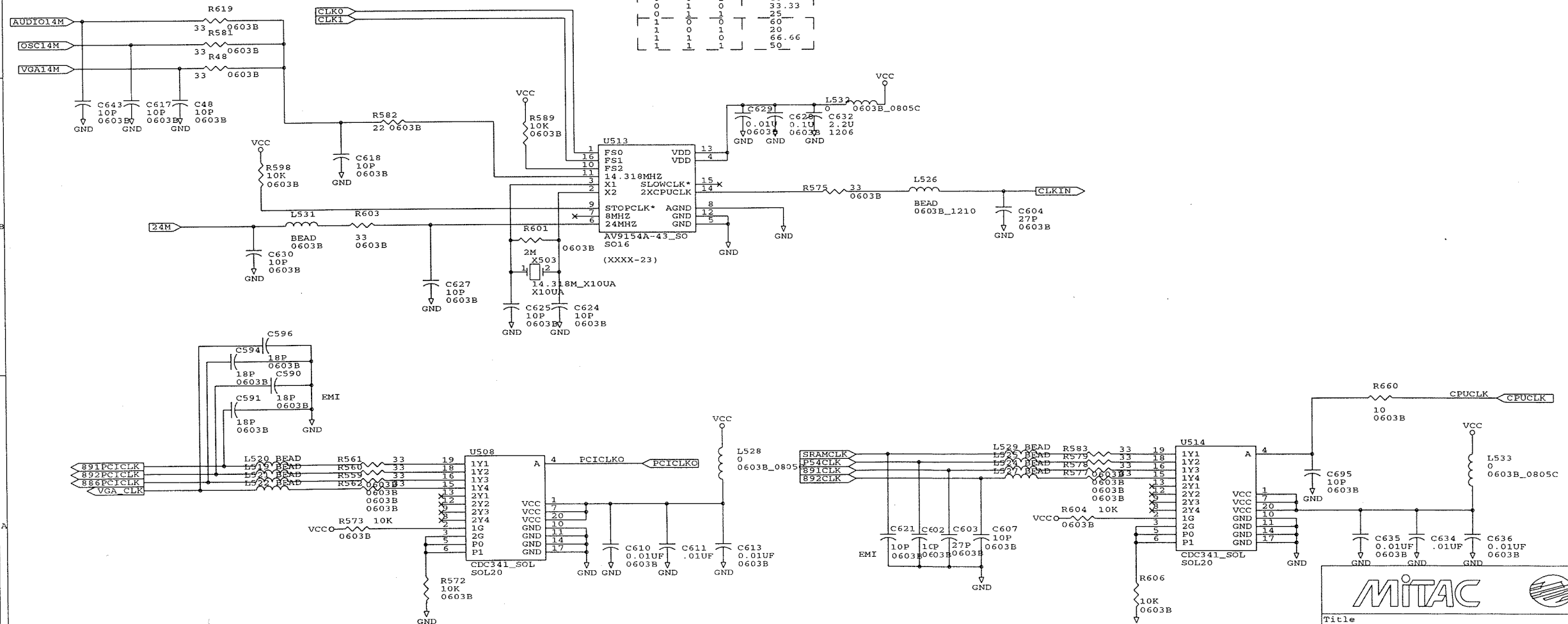


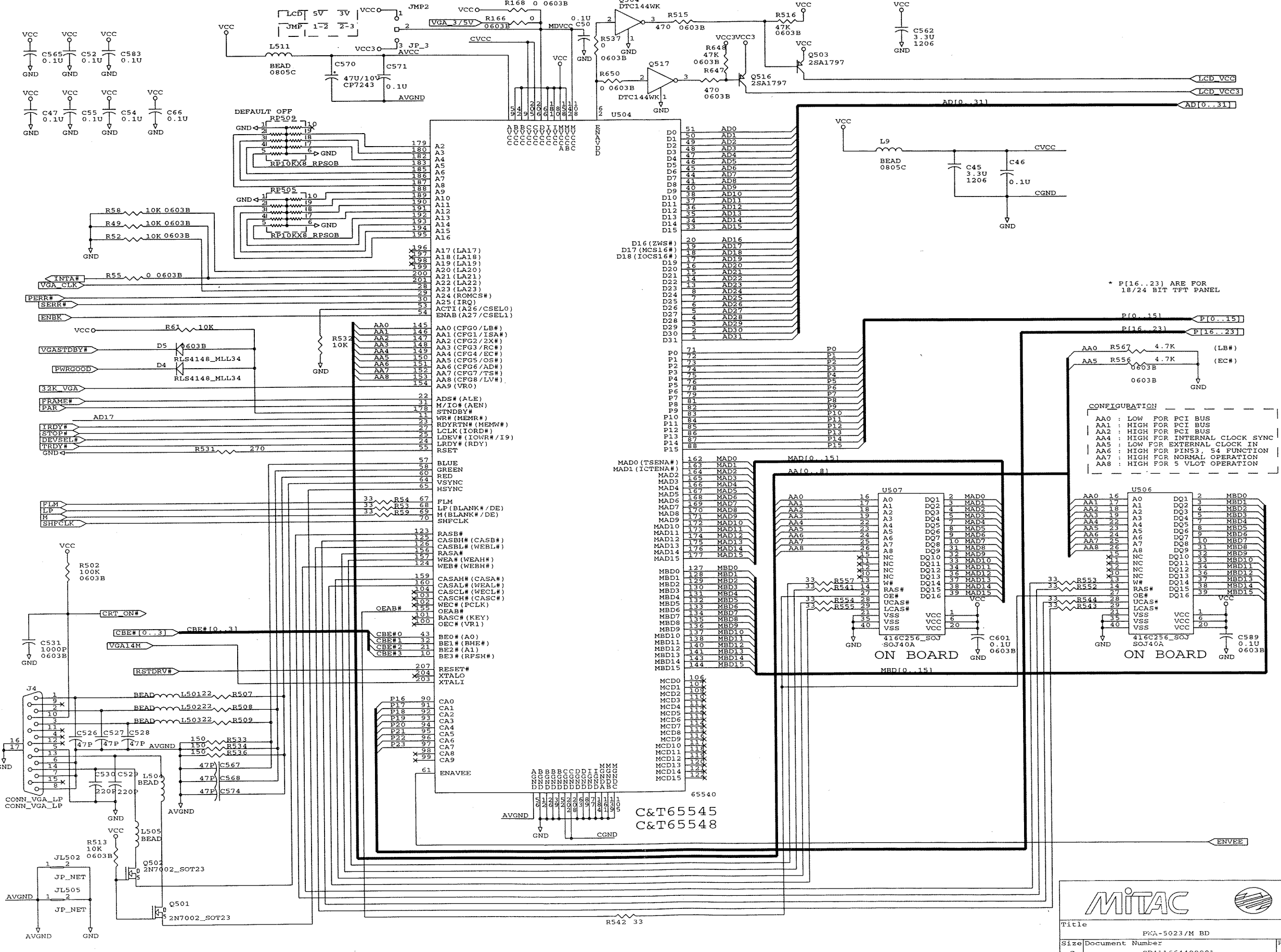
PMC LATCH 2



CLOCK SYNC.

Ps2	FS1	FS0	2XCPUCLK
0	0	0	16
0	0	1	40
0	1	0	33.33
0	1	1	25
1	0	0	60
1	0	1	20
1	1	0	66.66
1	1	1	50





* P[16..23] ARE FOR 18/24 BIT TFT PANEL

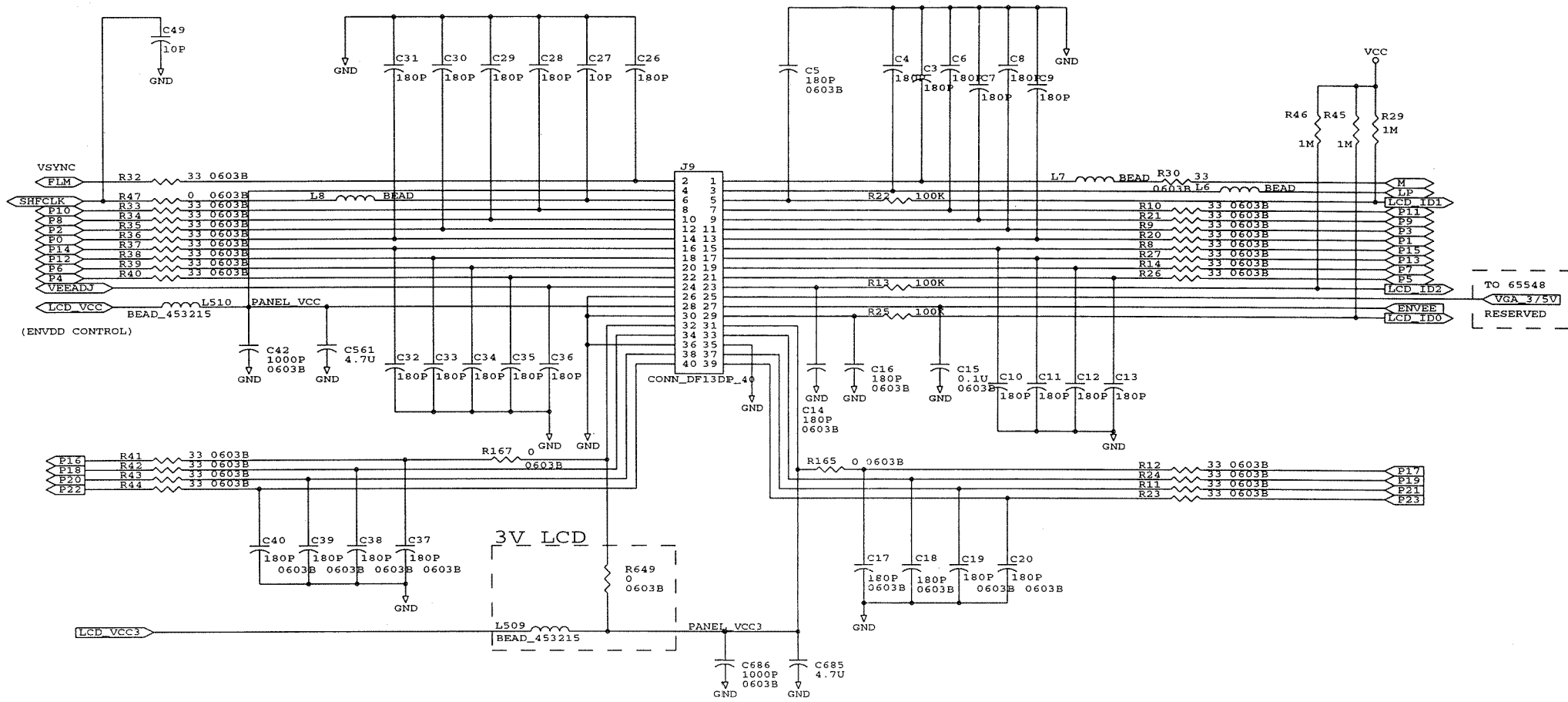
CONFIGURATION
 AA0 : LOW FOR PCI BUS
 AA1 : HIGH FOR PCI BUS
 AA2 : HIGH FOR PCI BUS
 AA4 : HIGH FOR INTERNAL CLOCK SYNC
 AA5 : LOW FOR EXTERNAL CLOCK IN
 AA6 : HIGH FOR PINS3, 54 FUNCTION
 AA7 : HIGH FOR NORMAL OPERATION
 AA8 : HIGH FOR 5 VLOT OPERATION

ON BOARD

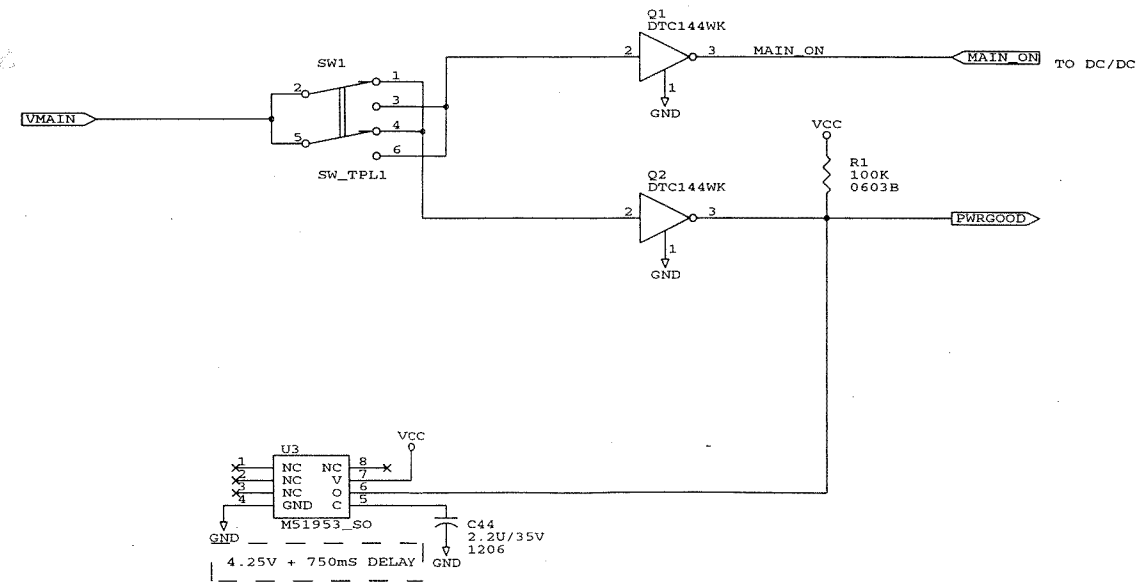
ON BOARD

C&T65545
 C&T65548

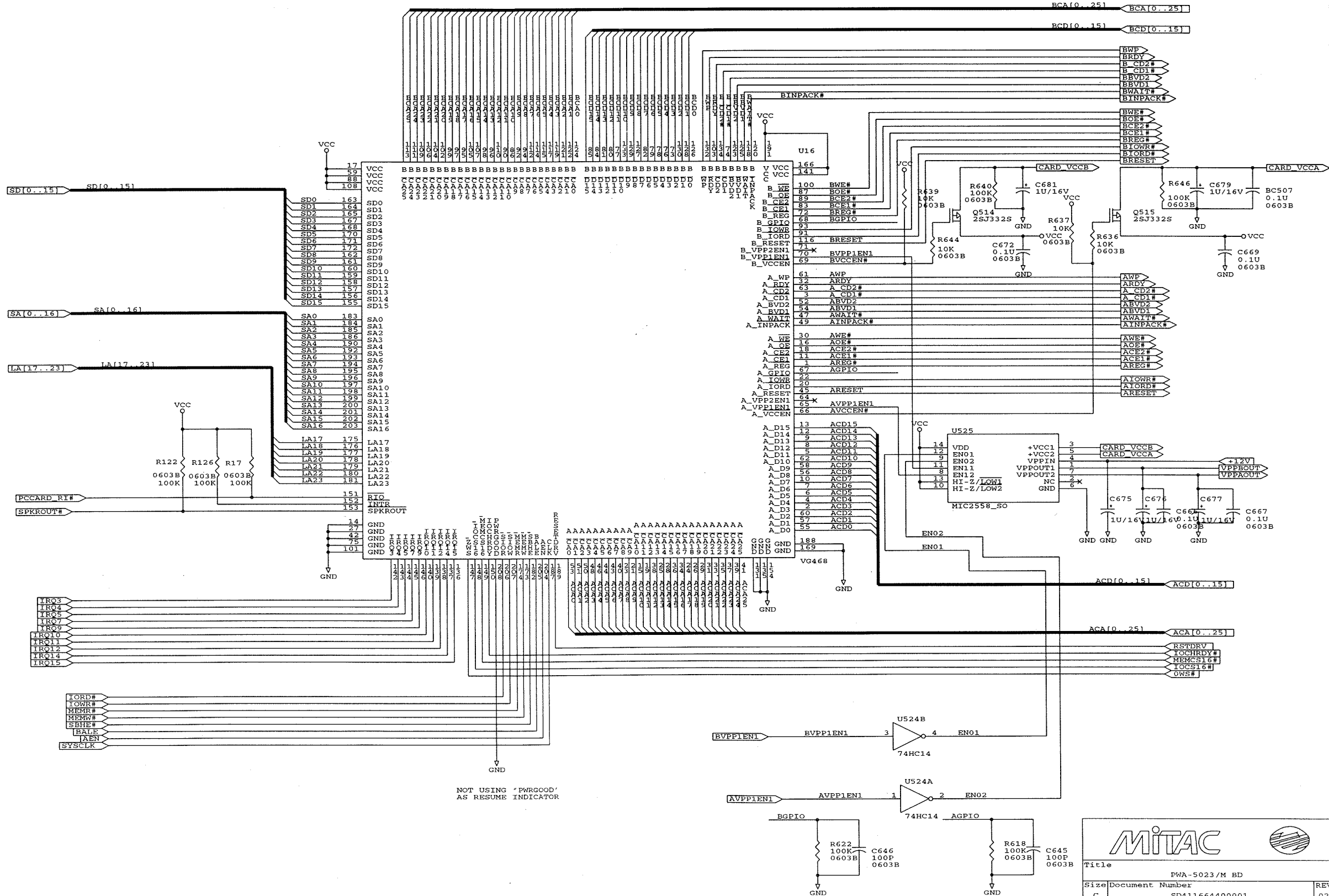
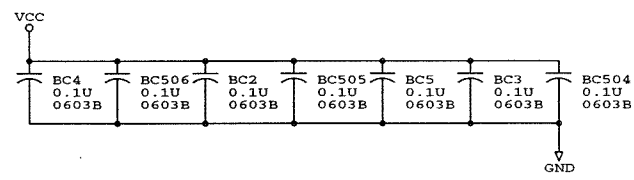




DSTN/TFT LCD PANEL CONN.



POWER-ON CIRCUITRY



NOT USING 'PWGOOD'
AS RESUME INDICATOR

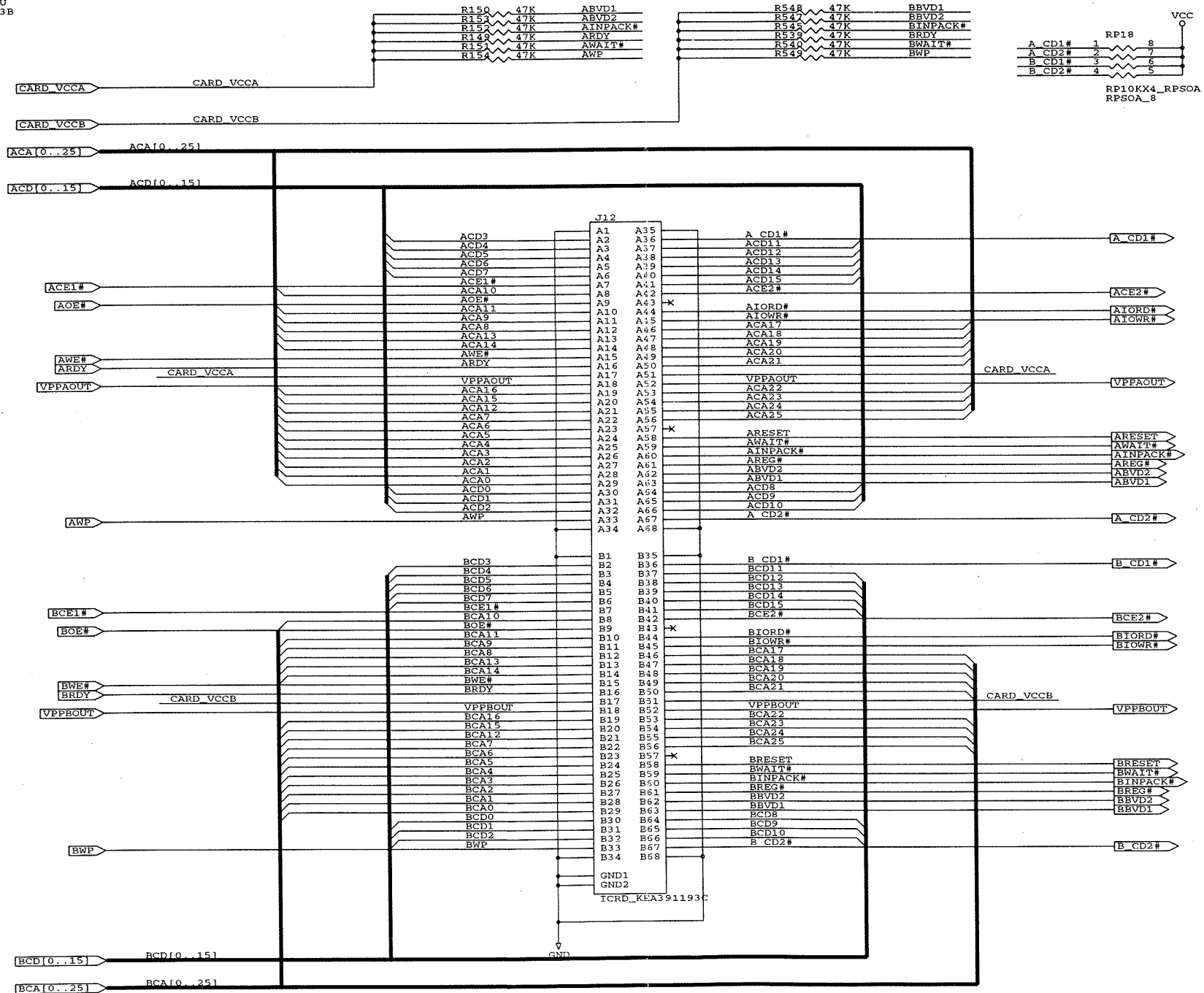
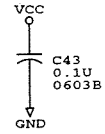
MITAC

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Size: Document Number: SD411664400001

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PCMCIA SOCKET



MITAC

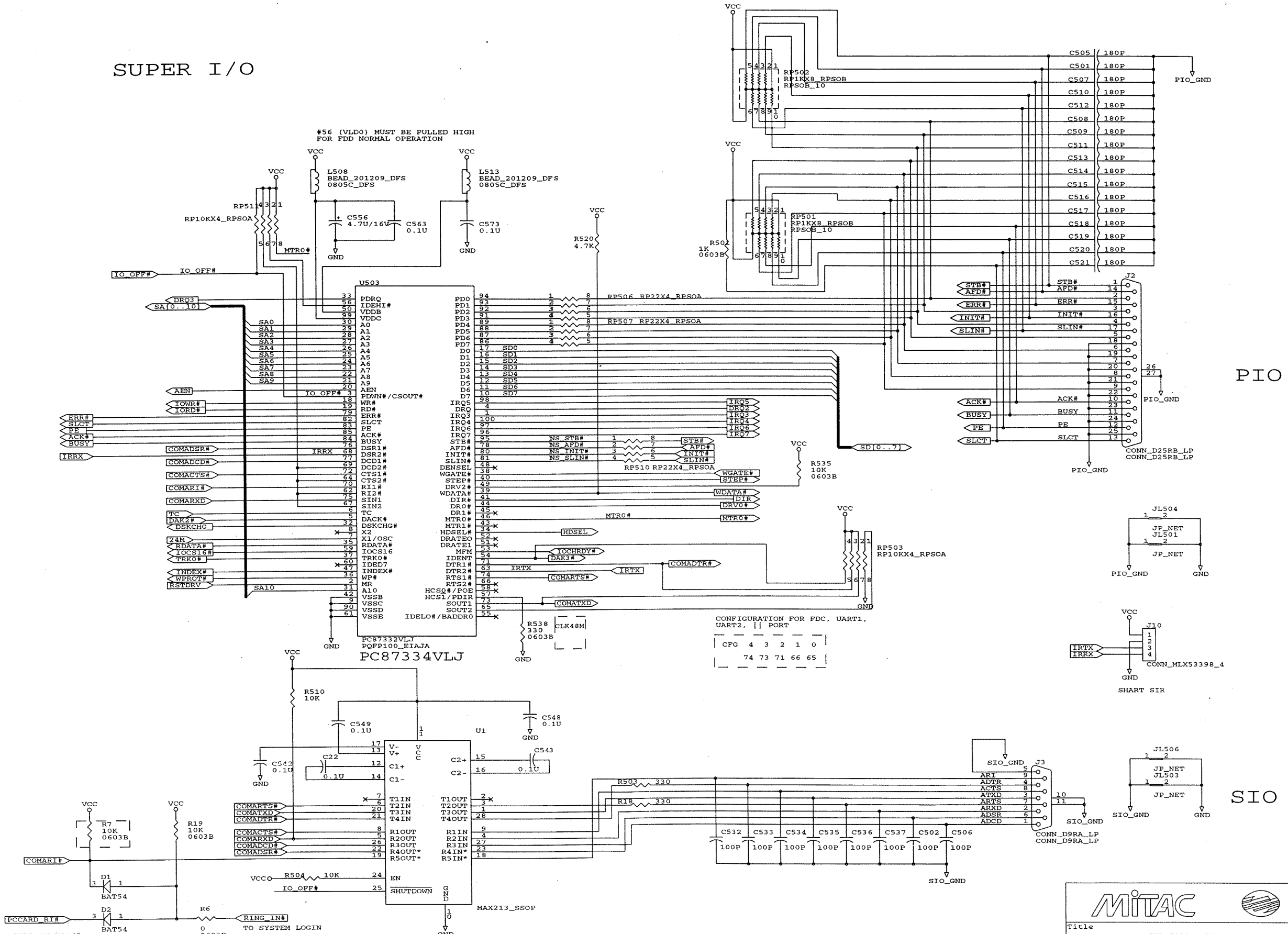
Title: PWA-5023/M BD

Size	Document Number	REV
C	SD411664400001	02

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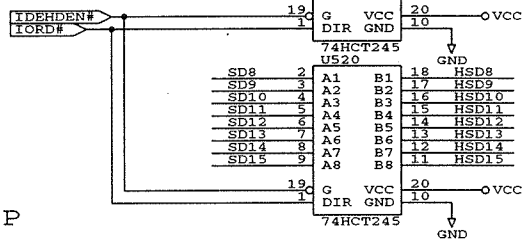
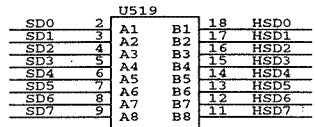
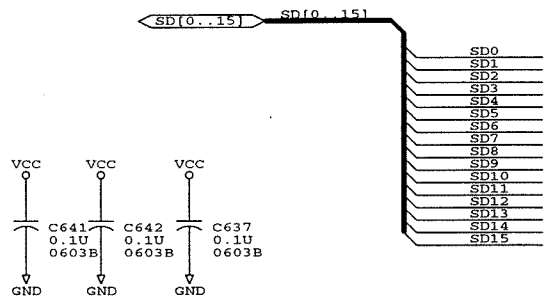
SUPER I/O

#56 (VLD0) MUST BE PULLED HIGH FOR FDD NORMAL OPERATION

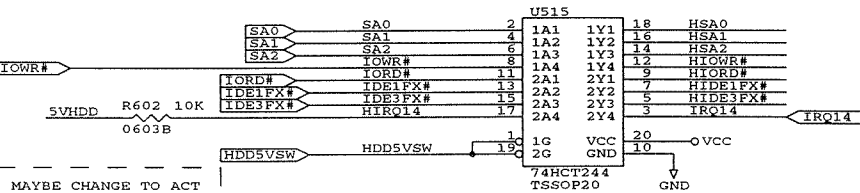


CONFIGURATION FOR FDC, UART1, UART2, || PORT

CFG	4	3	2	1	0
	74	73	71	66	65

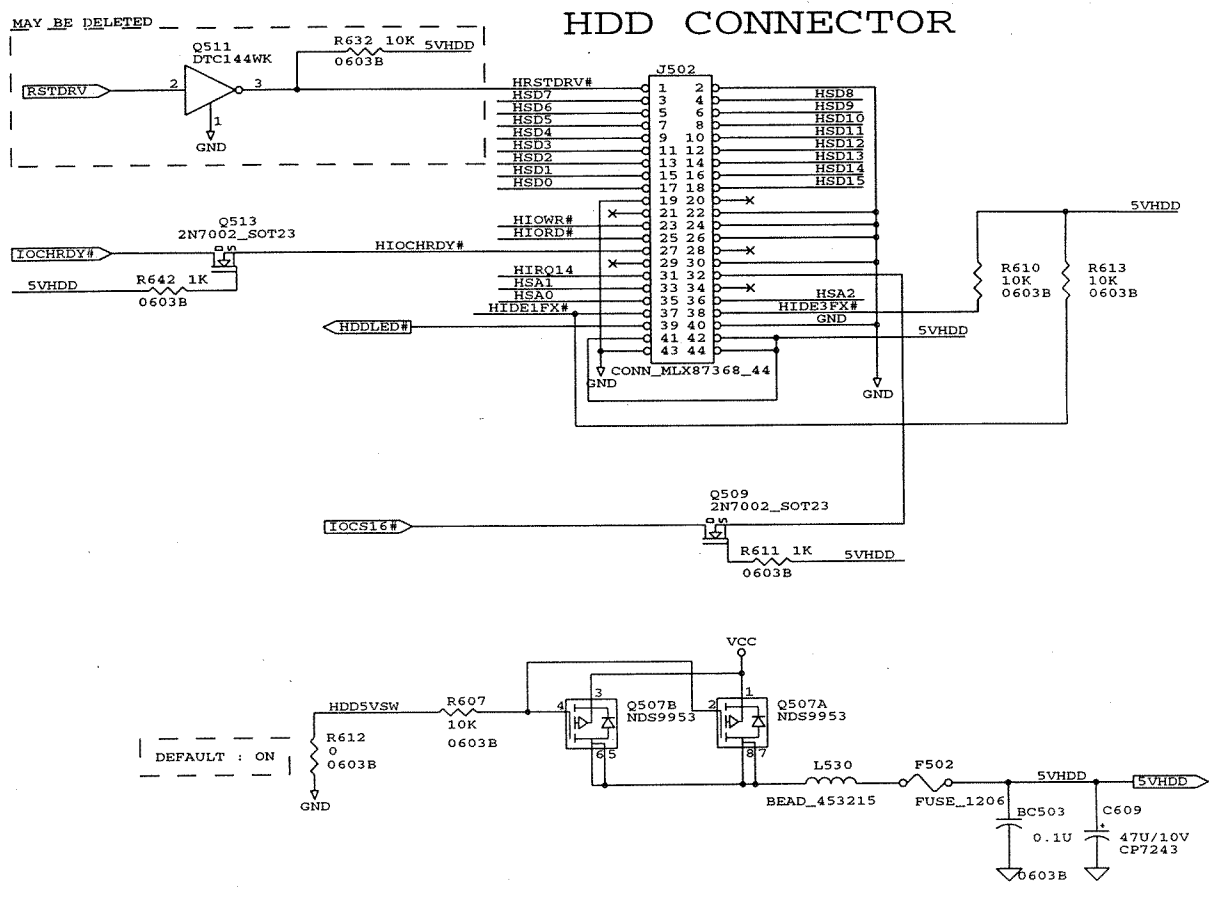
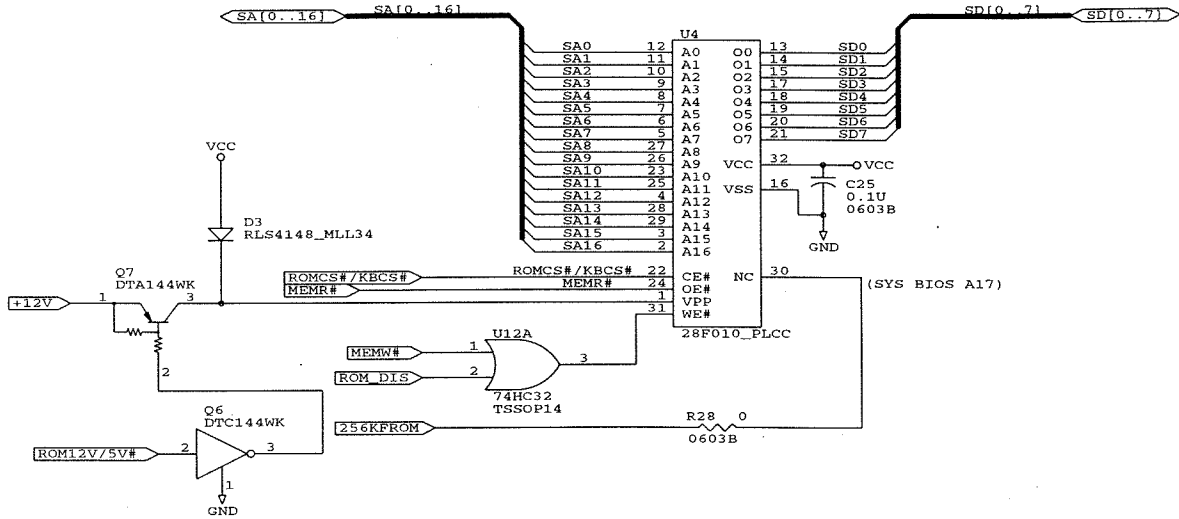


BUFFER CHIP

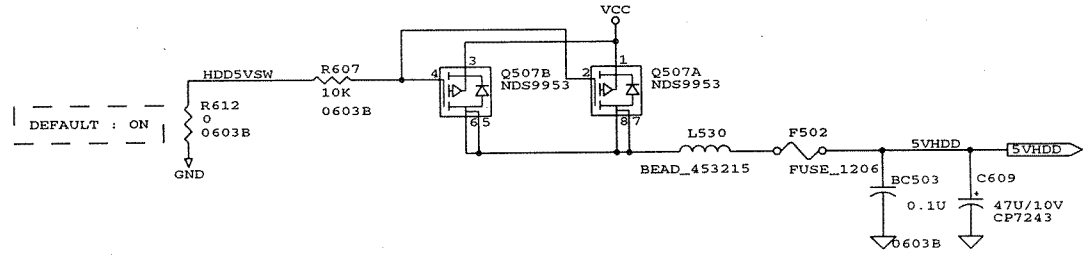


MAYBE CHANGE TO ACT TO SUPPORT 3MODE HDD

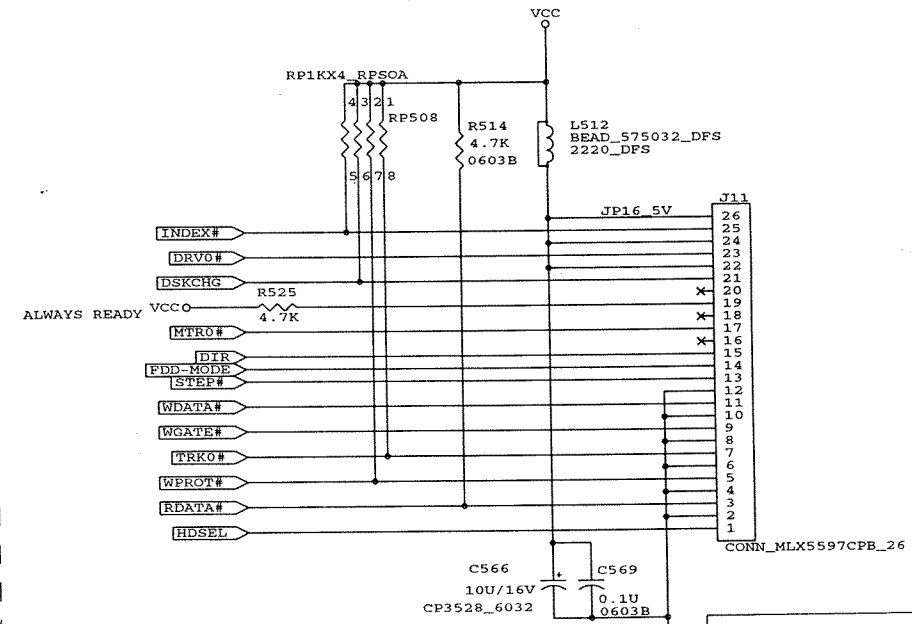
SYSTEM BIOS



HDD CONNECTOR



FDD CONNECTOR



MITAC

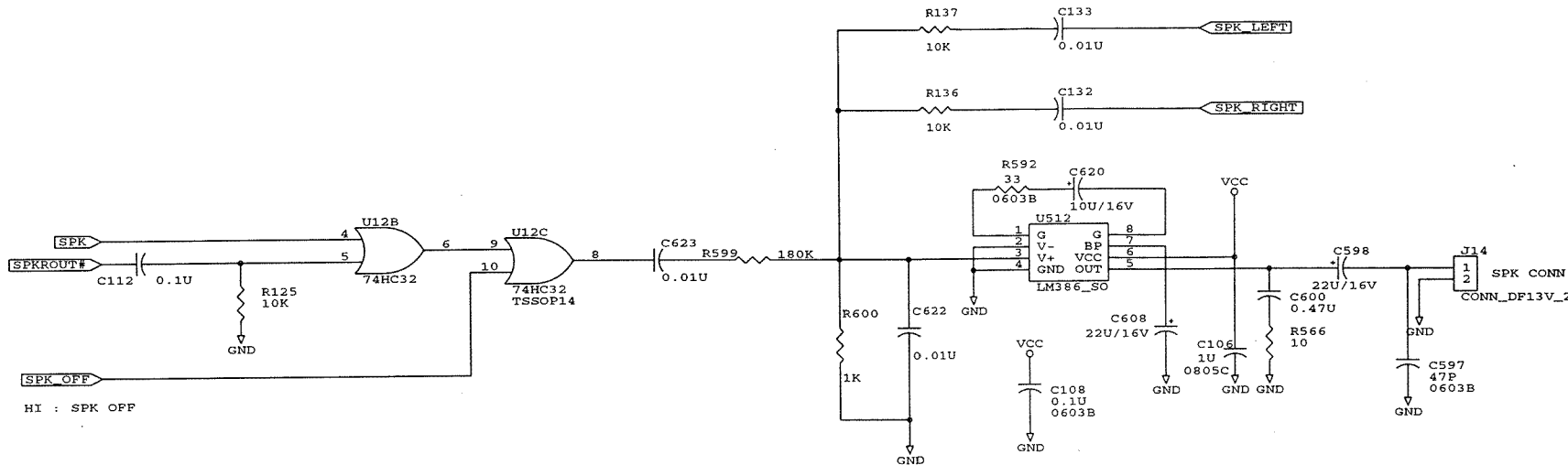
Title: PWA-5023/M BD

Size: Document Number: SD411664400001

Date: February 27, 1996

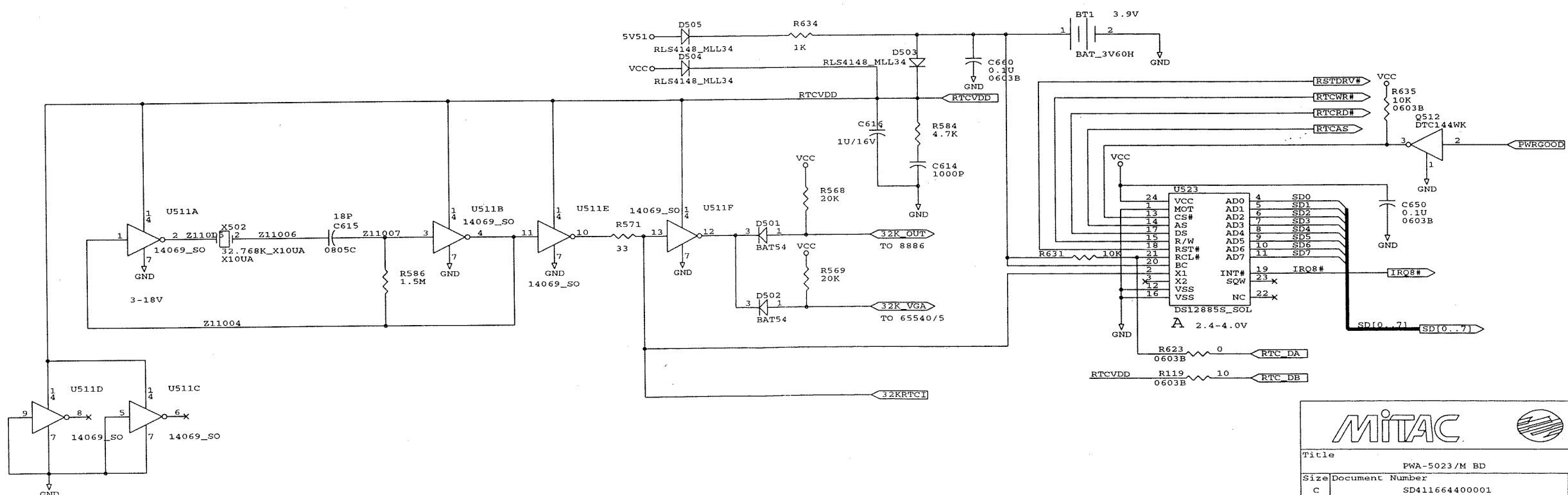
REV: 02

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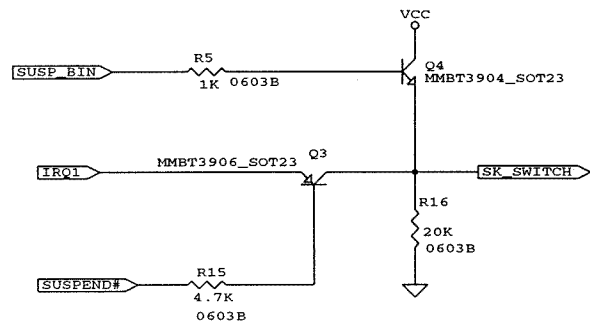


INTERNAL SPEAKER

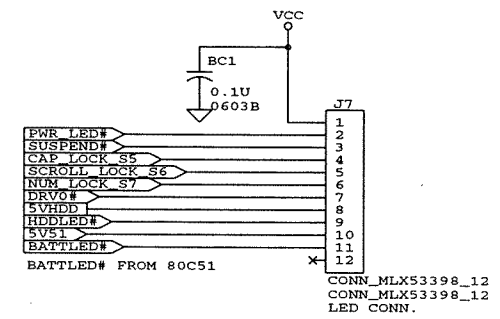
RTC



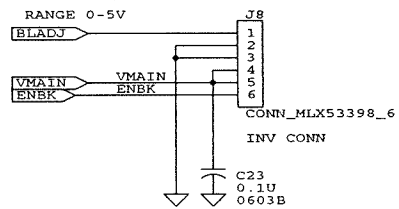
SUSPEND & ANY KEY RESUME CKT



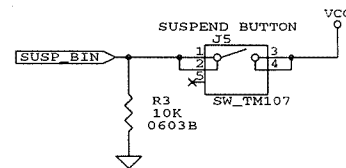
LED INDICATOR CONNECTOR



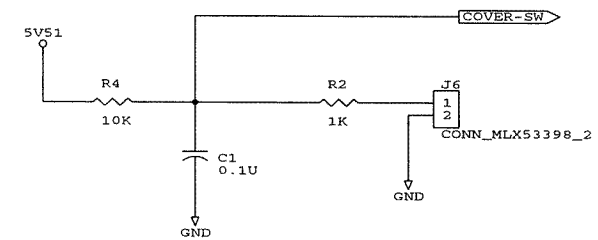
BACKLIGHT



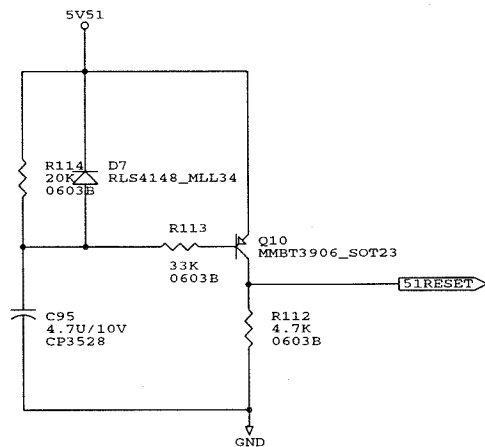
SUSPEND BUTTON

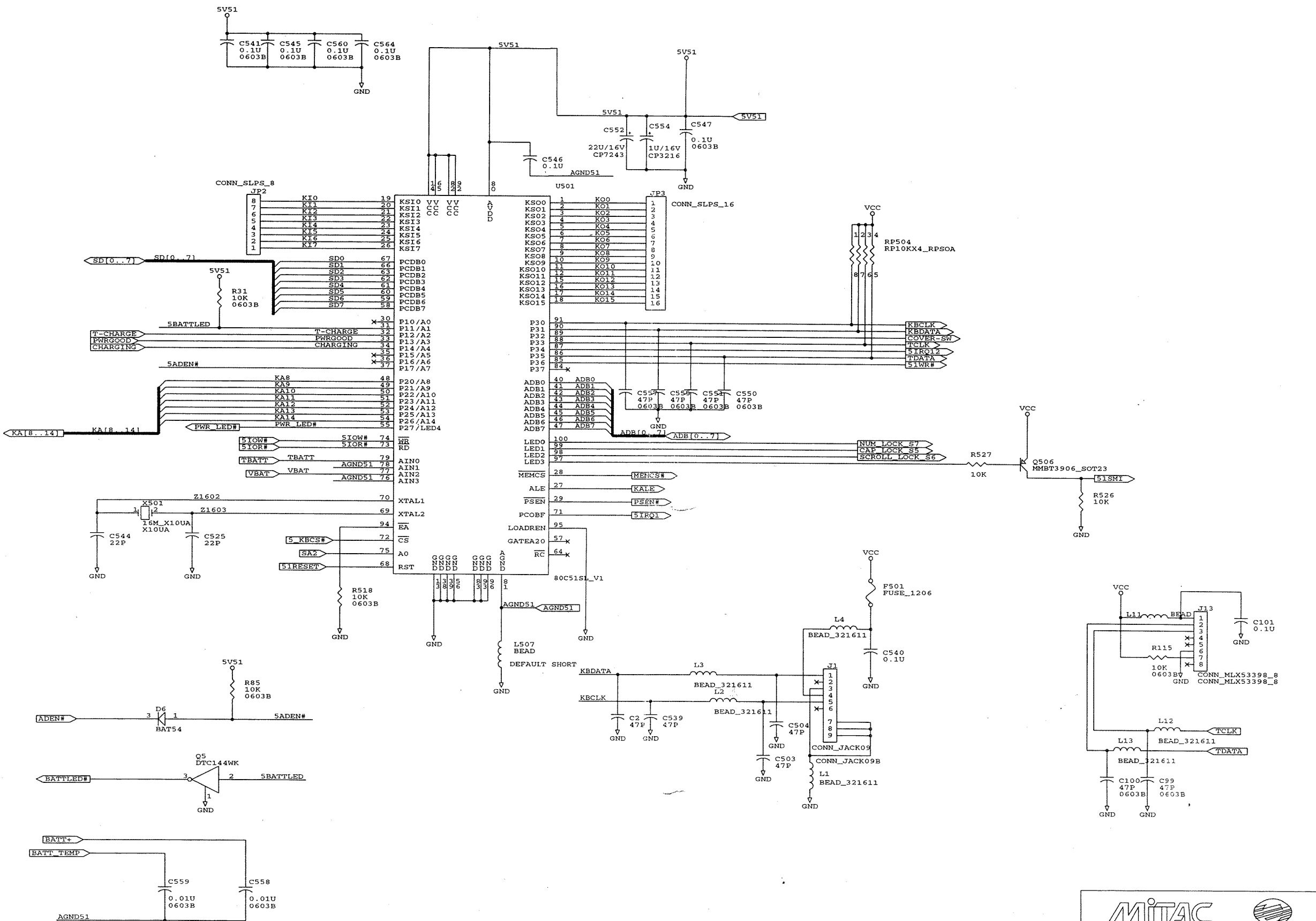


COVER SWITCH

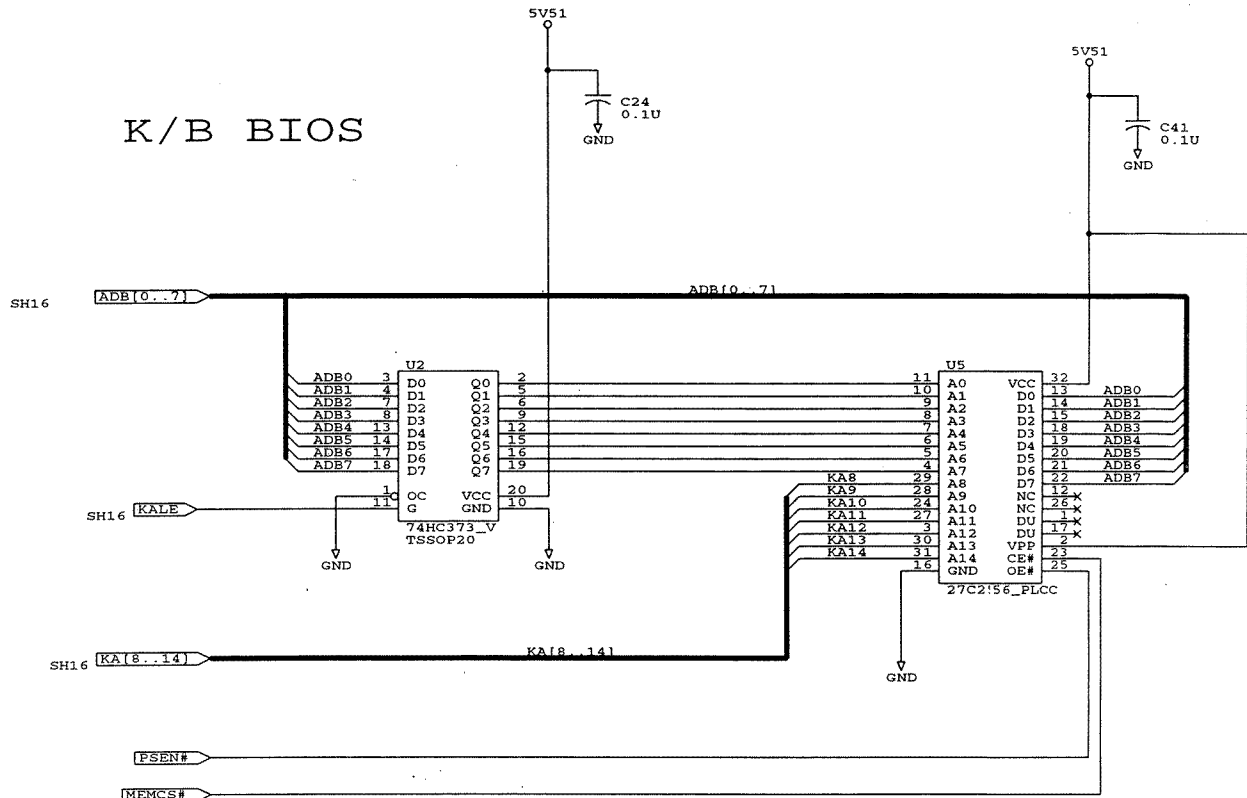


51 RESET CKT

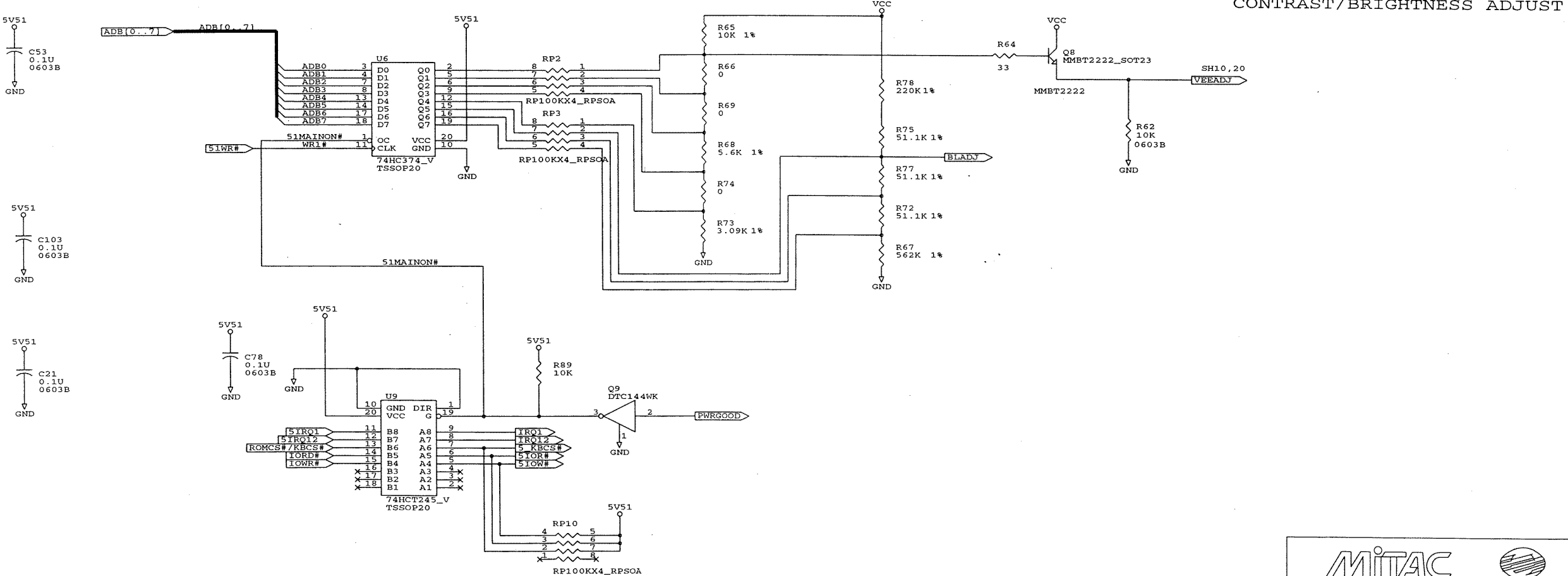


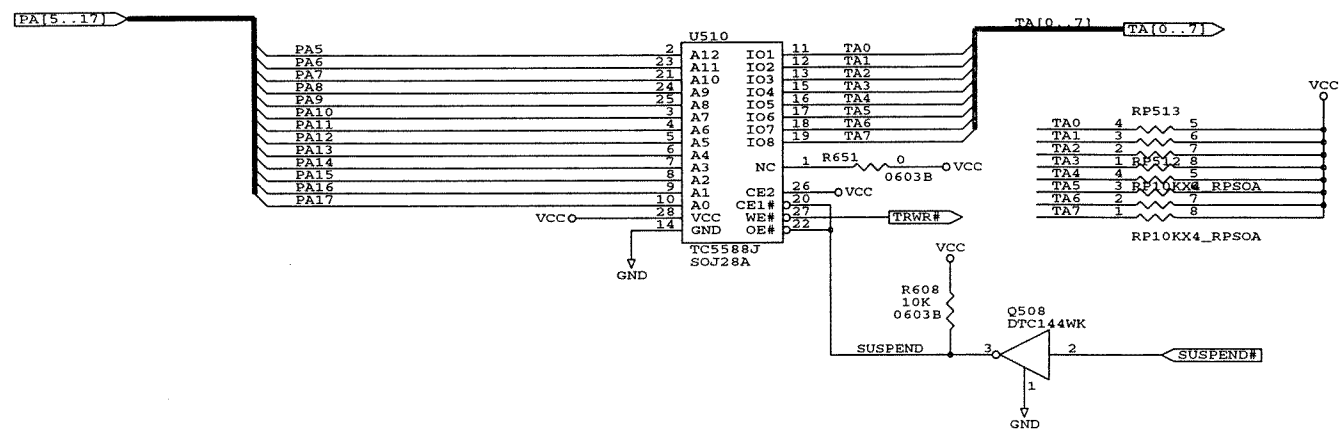


K/B BIOS

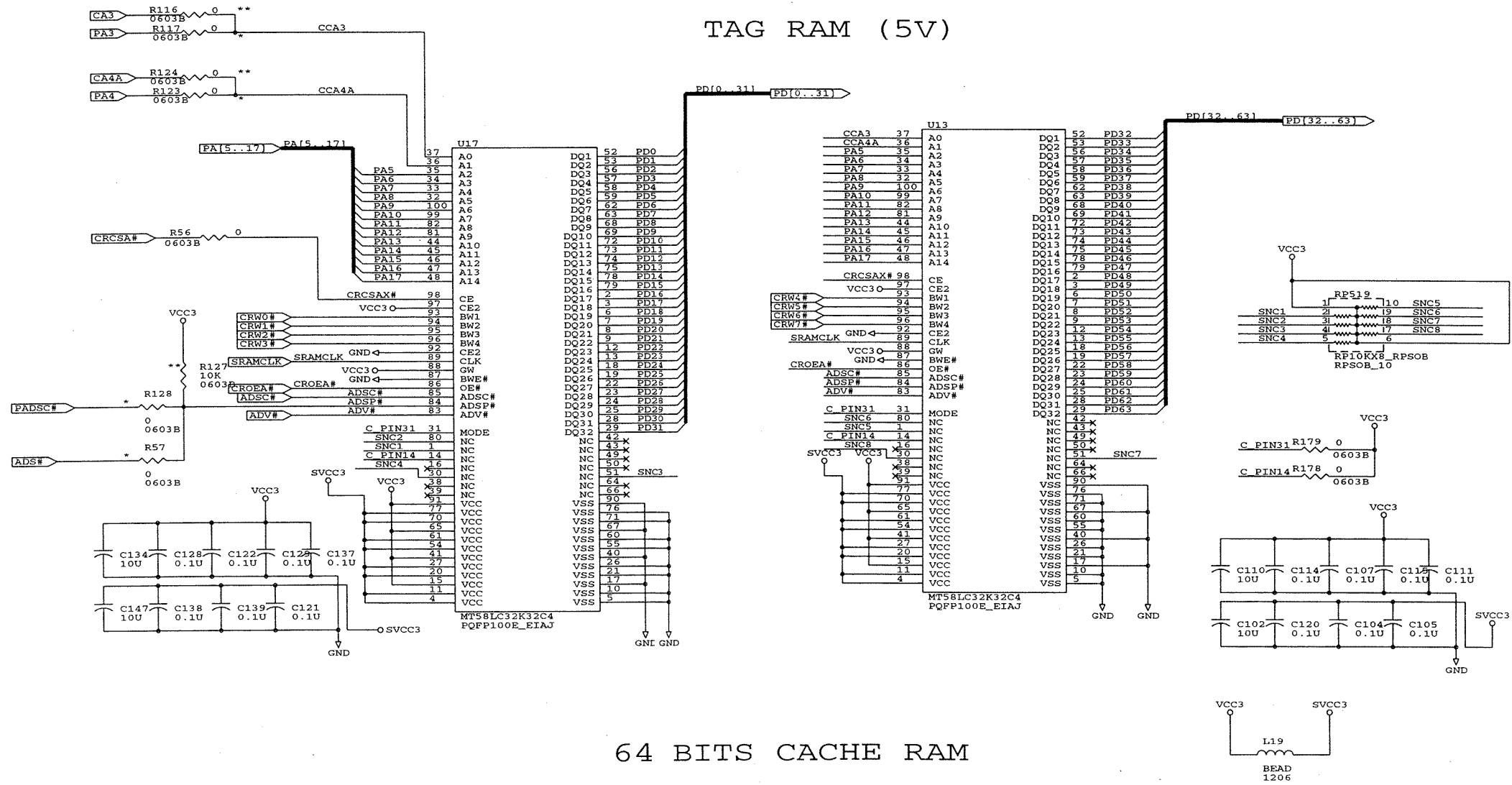


CONTRAST/BRIGHTNESS ADJUST



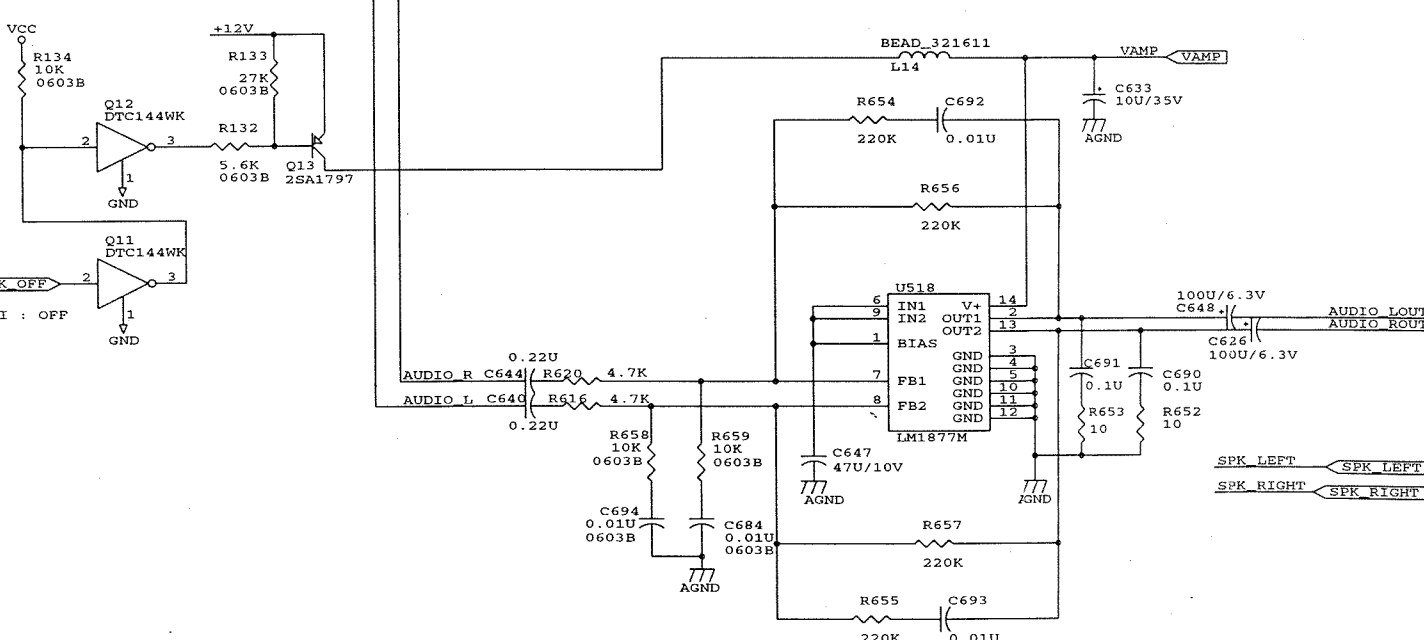
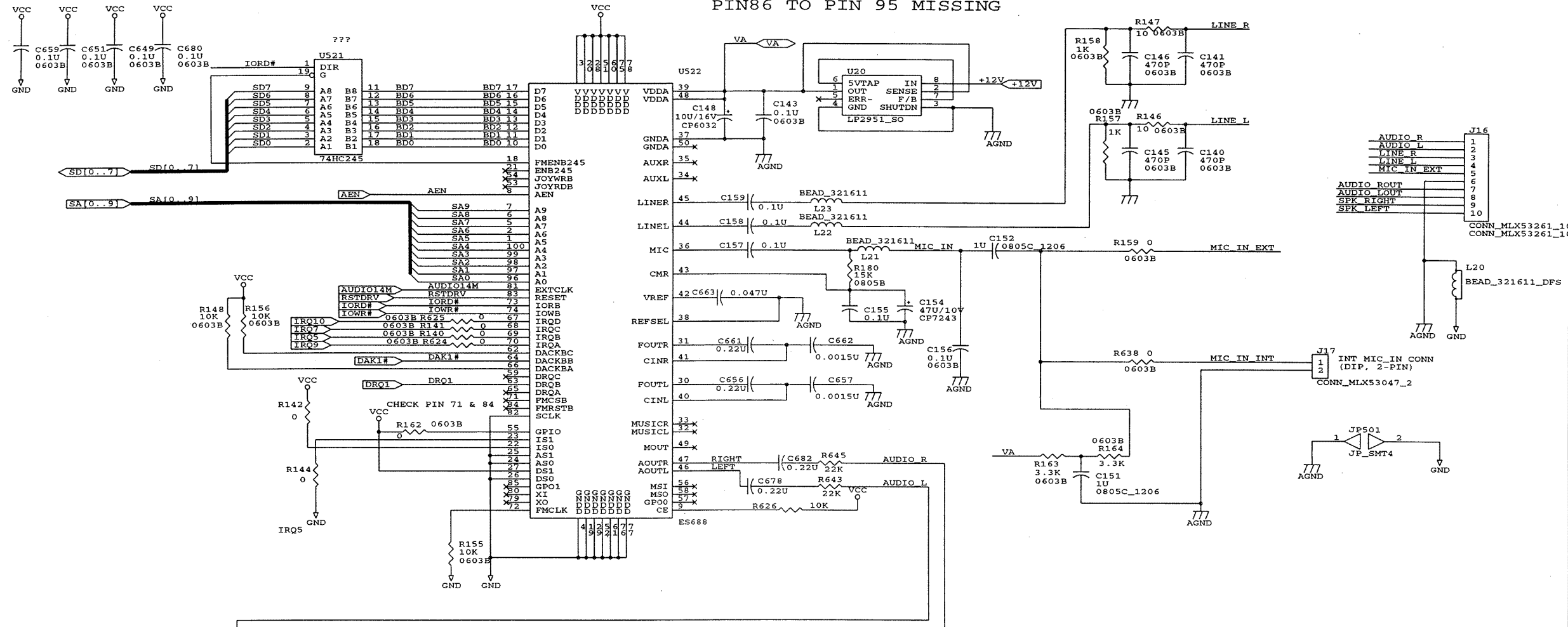


TAG RAM (5V)

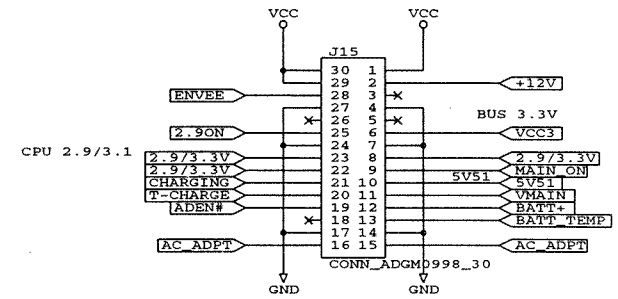
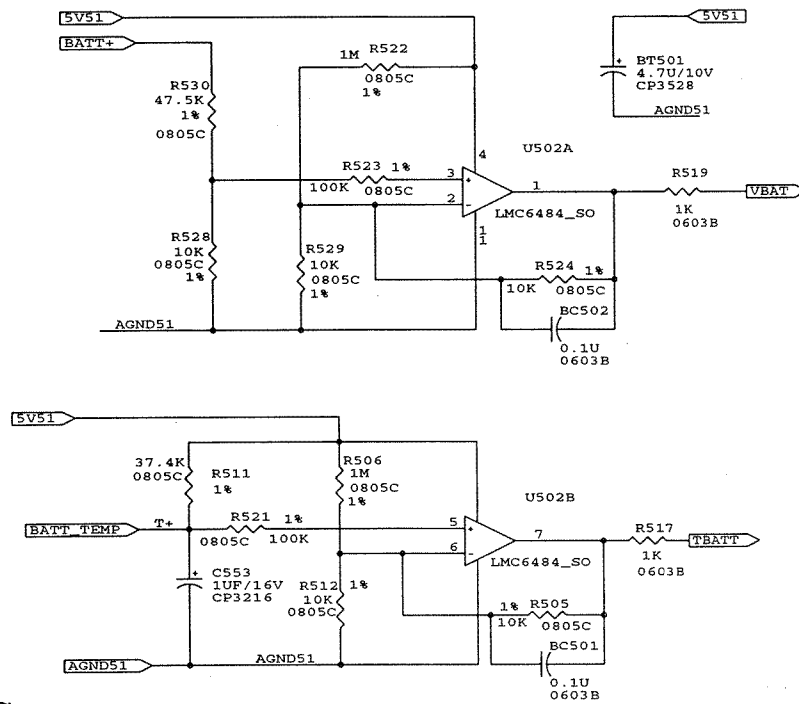


64 BITS CACHE RAM

PIN86 TO PIN 95 MISSING



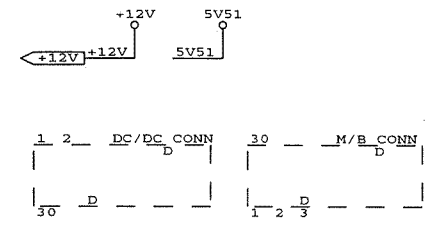
DC/DC CONNECTOR



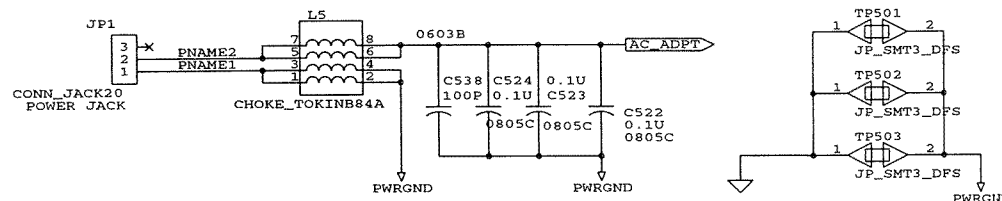
2.90N : HIGH IS 3.3V
 LOW IS 2.9V

MAIN_ON : LOW IS POWER ON
 FLOAT IS POWER OFF

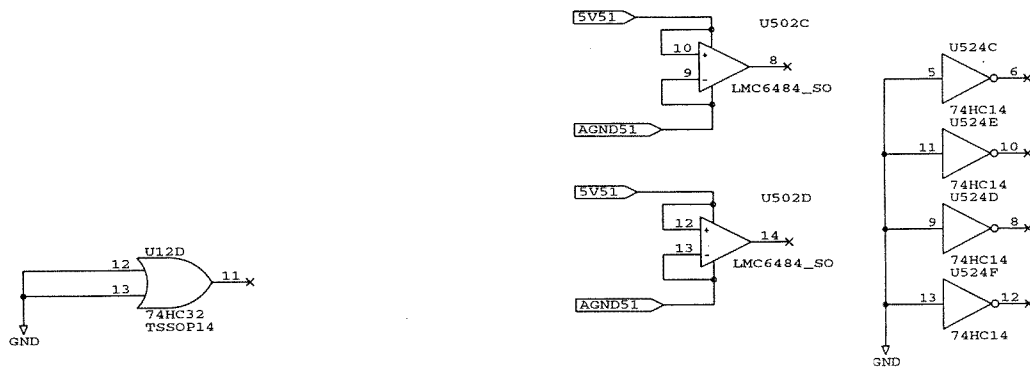
ADEN# : LOW IS ADAPTOR IN
 HIGH IS ADAPTOR OFF



80C51 ANALOG



POWER JACK



SPARE PART

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