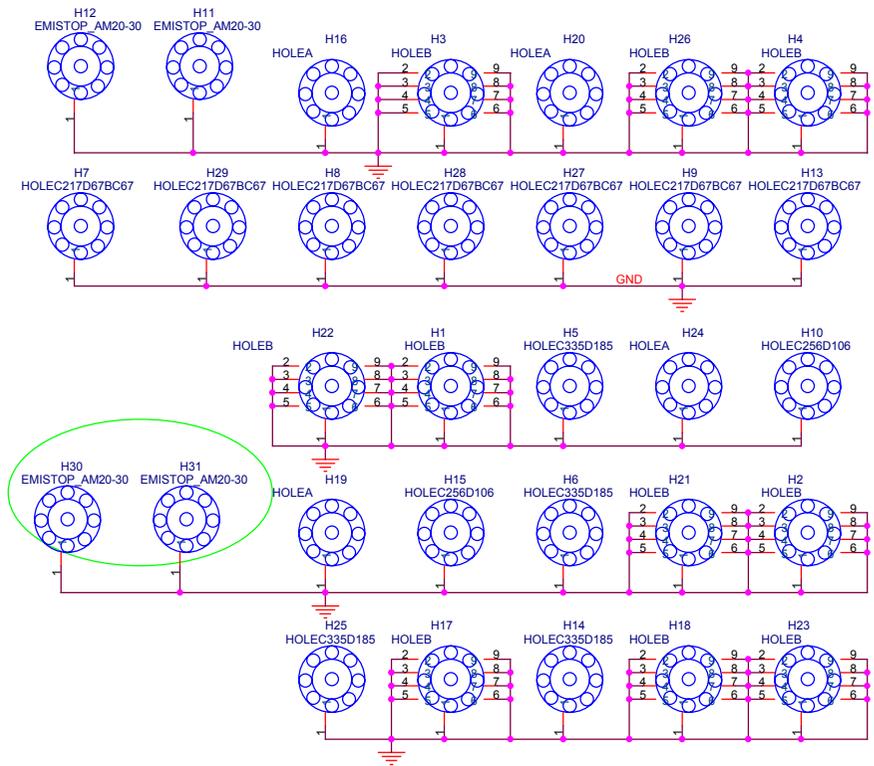


- 01:TITLE
- 02:Pentium 4-1
- 03:Pentium 4-2
- 04:Pentium 4-3
- 05:SIS648(HOST/AGP)
- 06:SIS648(RAM CONTROLLER)
- 07:SIS648(HYPER ZIP/AGP)
- 08:SIS648(POWER)
- 09:DDR_SODIMM
- 10:DDR_TERMINATION RESISTOR
- 11:M10_VGA_IO
- 12:M10_VGA_MEM
- 13:M10_VGA_POWER
- 14:DDR_SG8Mx32_BGA_A
- 15:DDR_SG8Mx32_BGA_B
- 16:963(PCI/IDE)
- 17:963(MISC)
- 18:963(USB CONTROLLER)
- 19:963(POWER)
- 20:KBC PC87591
- 21:W832517D LPC SUPER I/O
- 22:CRT & P.P.
- 23:AUDIO DJ
- 24:HDD & CD-ROM CONN.
- 25:AUDIO & AMP
- 26:LCD CRT &TV CONN
- 27:USB CONN &RJ11
- 28:TI 1410 CONTROLLER
- 29:MINIPCI & PCMCIA SLOT
- 30:RTL8201 LAN PHY
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- 32:CLOCK GENERATOR
- 33:CLOCK BUFFER
- 34:RTC&POWER GOOD
- 35:POWER SWITCH
- 36:SELECTOR
- 37:MAX1772 CHARGER
- 38:MAX1632 SYSTEM POWER
- 39:HIP6301 CPU POWER
- 40:RT9202_RT9173_LDO
- 41:MAX1858 VGA/RAM POWER
- 42:HISTORY

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REV	6.B	6.0	6.A	6.0	6.B	6.0	6.0	6.0	6.0	6.0	6.B	6.0	6.0	6.0	6.0	6.0	6.A	6.0	6.0
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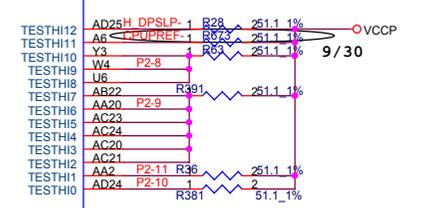
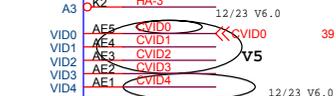
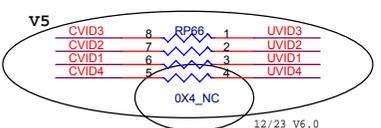
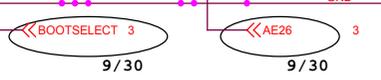
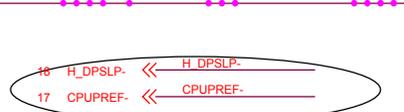
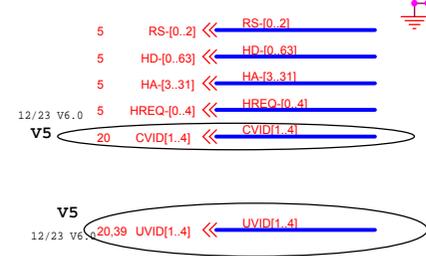
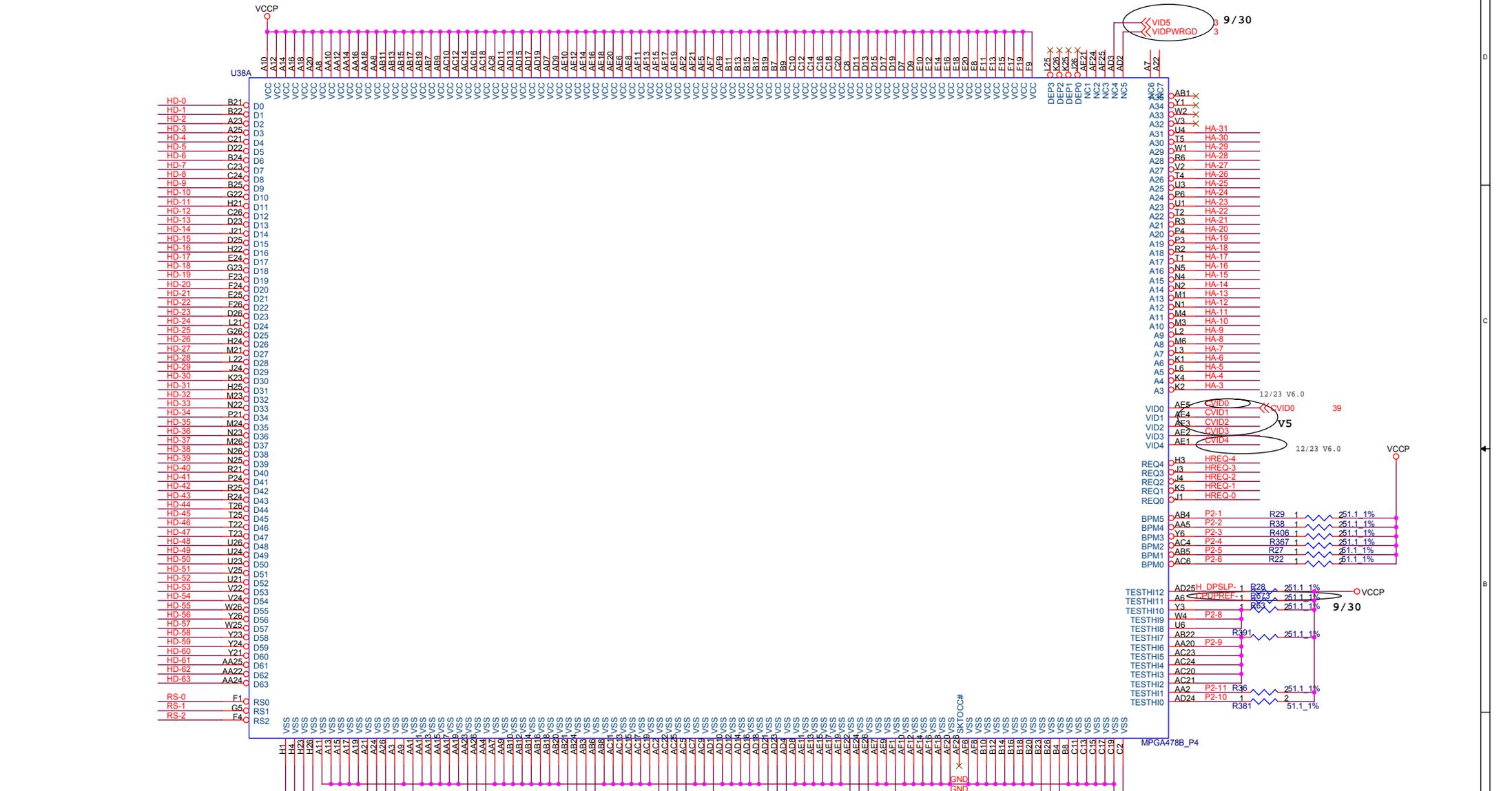
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DATE	12/23	12/23	02/18	02/18



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 Y = 1206 TYPE
 C3216 = A TYPE
 C3528 = B TYPE
 C6032 = C TYPE
 C7343 = D TYPE

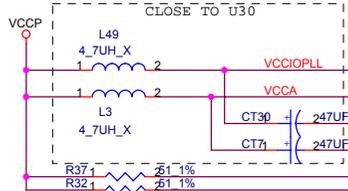
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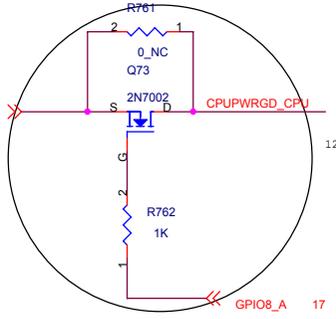
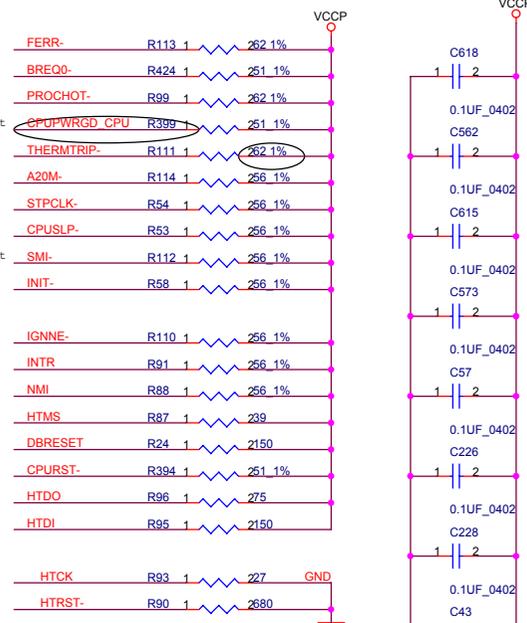
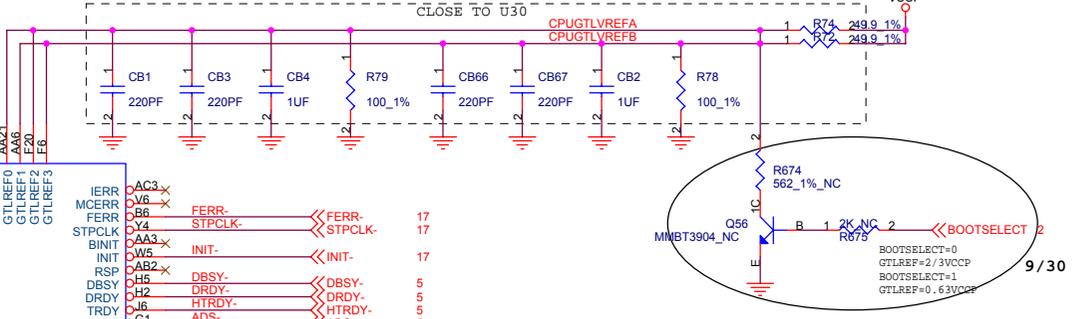
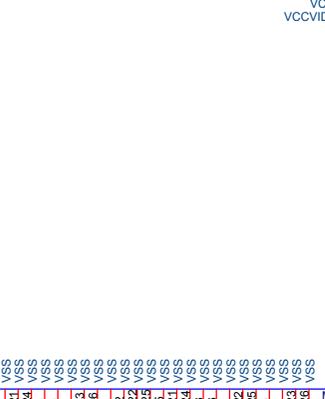
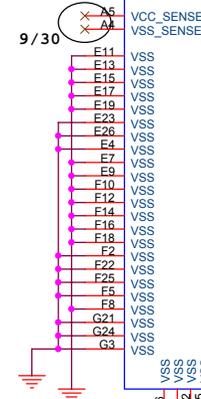
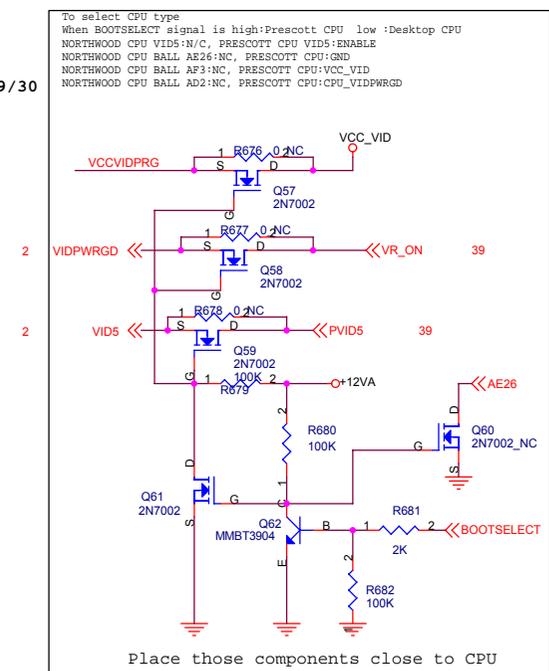


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Size	Document Number	Rev
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Date:	Thursday, February 19, 2004	Sheet 2 of 42

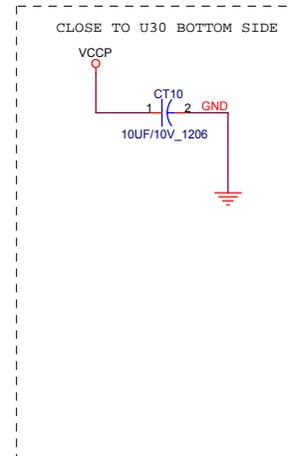
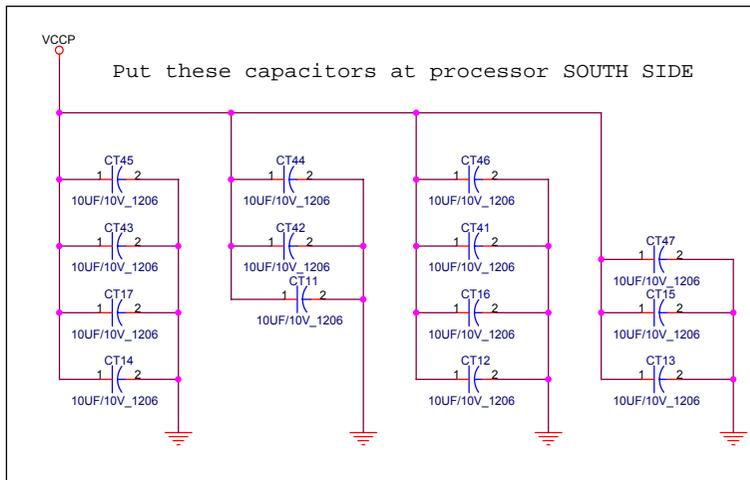
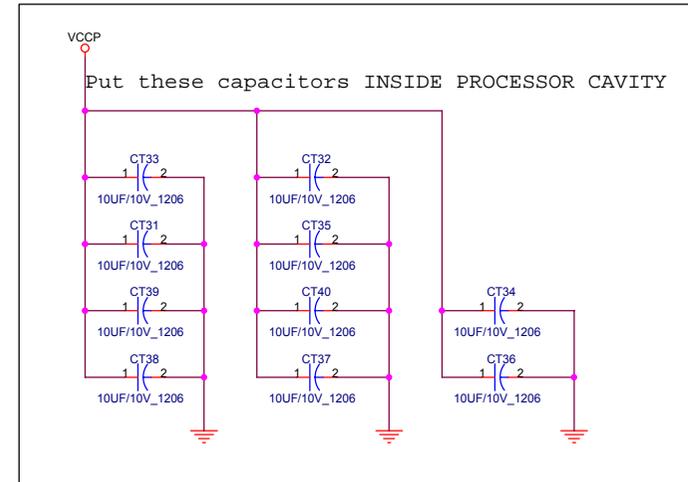
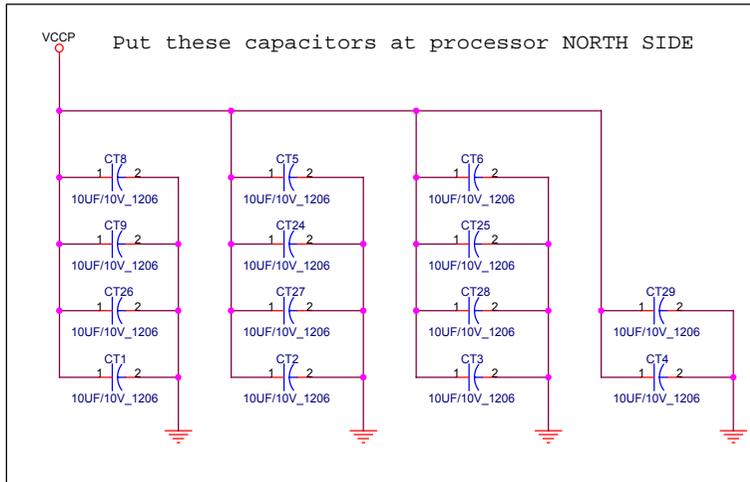
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- 5 HDSTBN[0..3] << HDSTBN[0..3]
- 5 DBI[0..3] << DBI[0..3]
- 5 HASTB[0..1] << HASTB[0..1]



- DBI-3 V21
- DBI-2 P26
- DBI-1 G25
- DBI-0 E24
- DB#0
- HASTB-1 R5
- HASTB-0 L5
- DBRESET AE25
- NMI << NMI E5
- INTR << INTR D1
- CPUCLK0 << CPUCLK0 AF23
- CPUCLK0 << CPUCLK0 AF22
- 51.1% COMP1 P1
- 51.1% COMP0 L24
- HDSTBP-3 W23
- HDSTBP-2 P23
- HDSTBP-1 J23
- HDSTBP-0 F21
- HDSTBN-3 W22
- HDSTBN-2 R22
- HDSTBN-1 K22
- HDSTBN-0 E22



ECS CORP. (G736 M/B)			
Title CPU_FSBI-2			
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Title	CPU_POWER-3	
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3 HDSTBP[0..3] << HDSTBP[0..3]
 3 HDSTBN[0..3] << HDSTBN[0..3]
 3 DBI[0..3] << DBI[0..3]
 2 HD[0..63] << HD[0..63]
 3 HASTB[0..1] << HASTB[0..1]
 2 HA[3..31] << HA[3..31]
 2 HREQ[0..4] << HREQ[0..4]
 2 RS[0..2] << RS[0..2]

G_AD[0..31] << G_AD[0..31] 11
 G_SBA[0..7] << G_SBA[0..7] 11
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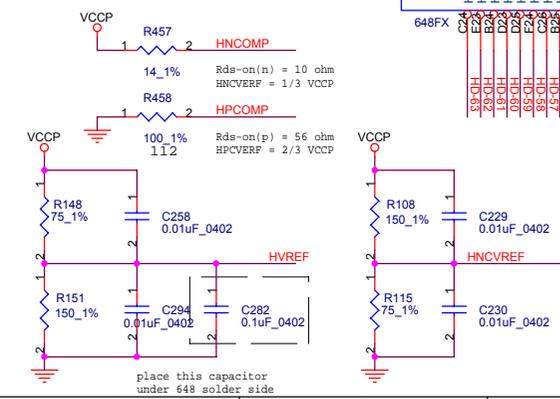
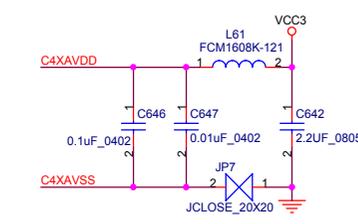
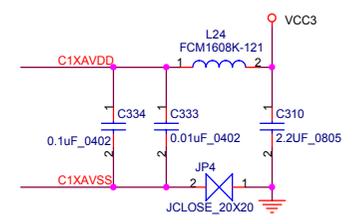
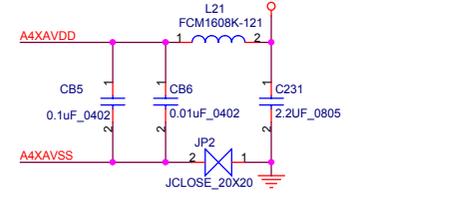
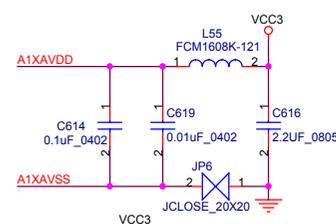
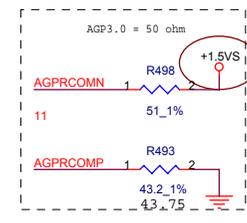
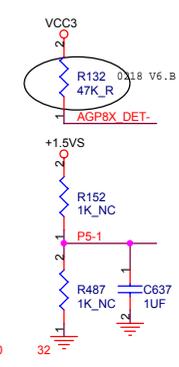
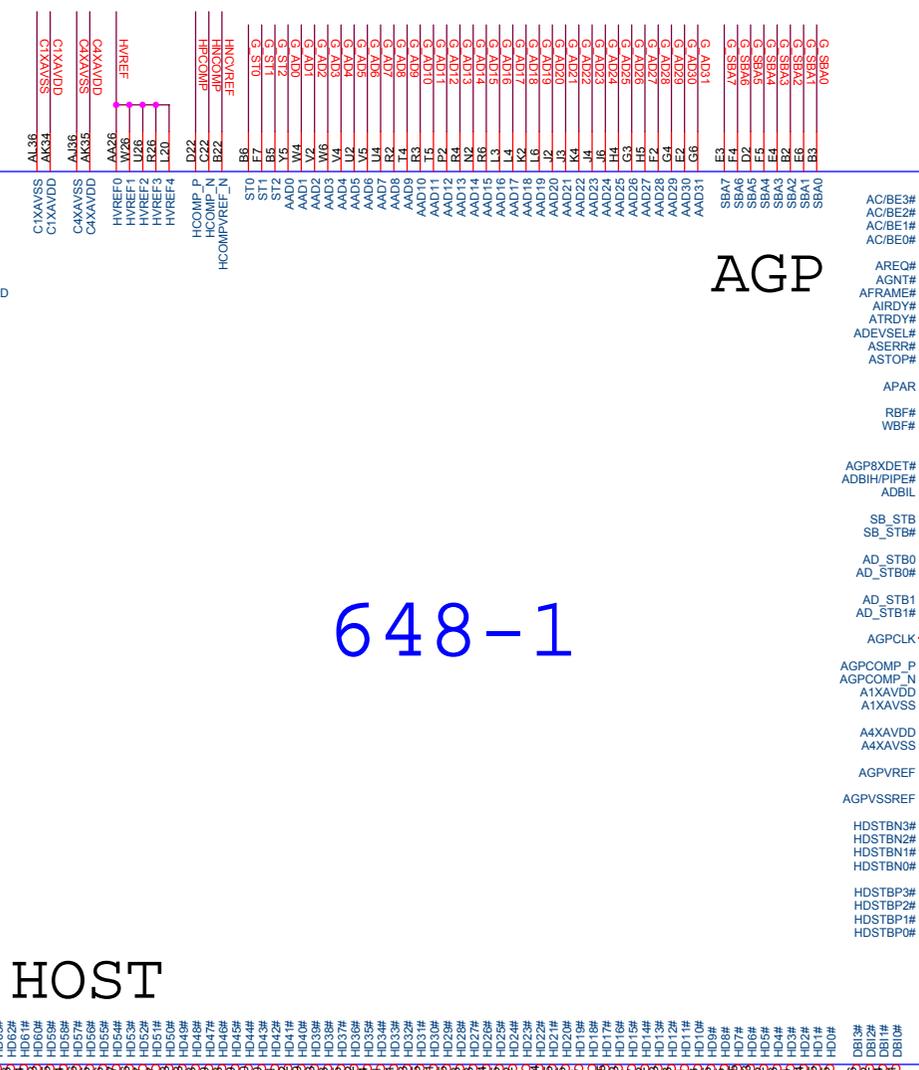
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 32 CPUCLK-1 << CPUCLK-1 A133 CPUCLK#
 3 HLOCK << HLOCK T33 HLOCK#
 3 DEFER << DEFER T35 DEFER#
 3 HTRDY << HTRDY V32 HTRDY#
 3 CPURST << CPURST B23 CPURST#
 3 CPUPWRGD << CPUPWRGD F22 CPUPWRGD#
 3 BPRI << BPRI R34 BPR#
 3 BREQ0 << BREQ0 U31 BREQ0#
 RS-2 << RS-2 R33 RS#2
 RS-1 << RS-1 T32 RS#1
 RS-0 << RS-0 U35 RS#0
 ADS << ADS V35 ADS#
 HITM << HITM R35 HITM#
 HIT << HIT U34 HIT#
 DRDY << DRDY W34 DRDY#
 DBSY << DBSY U33 DBSY#
 BNR << BNR V33 BNR#

HREQ-4 << HREQ-4 W35 HREQ4#
 HREQ-3 << HREQ-3 Y33 HREQ3#
 HREQ-2 << HREQ-2 W31 HREQ2#
 HREQ-1 << HREQ-1 W33 HREQ1#
 HREQ-0 << HREQ-0 Y35 HREQ0#
 HASTB-1 << HASTB-1 AG31 HASTB1#
 HASTB-0 << HASTB-0 AA33 HASTB0#
 HA-31 << HA-31 AH33 HA31#
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 HA-29 << HA-29 AJ35 HA29#
 HA-28 << HA-28 AE32 HA28#
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 HA-22 << HA-22 AF35 HA22#
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 HA-18 << HA-18 AF33 HA18#
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 HA-16 << HA-16 AC33 HA16#
 HA-15 << HA-15 AD32 HA15#
 HA-14 << HA-14 AD33 HA14#
 HA-13 << HA-13 AC35 HA13#
 HA-12 << HA-12 AC31 HA12#
 HA-11 << HA-11 AC34 HA11#
 HA-10 << HA-10 AC34 HA10#
 HA-9 << HA-9 AB35 HA9#
 HA-8 << HA-8 AB32 HA8#
 HA-7 << HA-7 AB33 HA7#
 HA-6 << HA-6 AC35 HA6#
 HA-5 << HA-5 AA31 HA5#
 HA-4 << HA-4 Y32 HA4#
 HA-3 << HA-3 AA34 HA3#

HOST

648-1

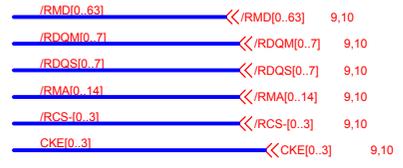
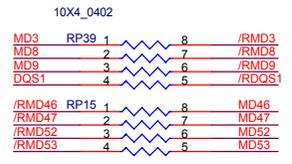
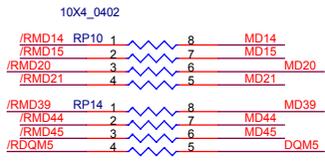
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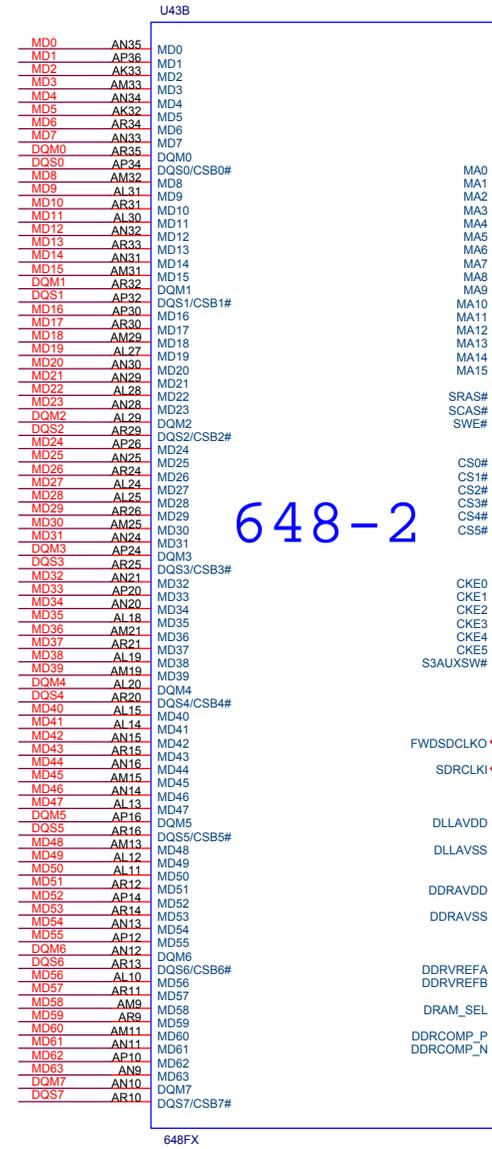
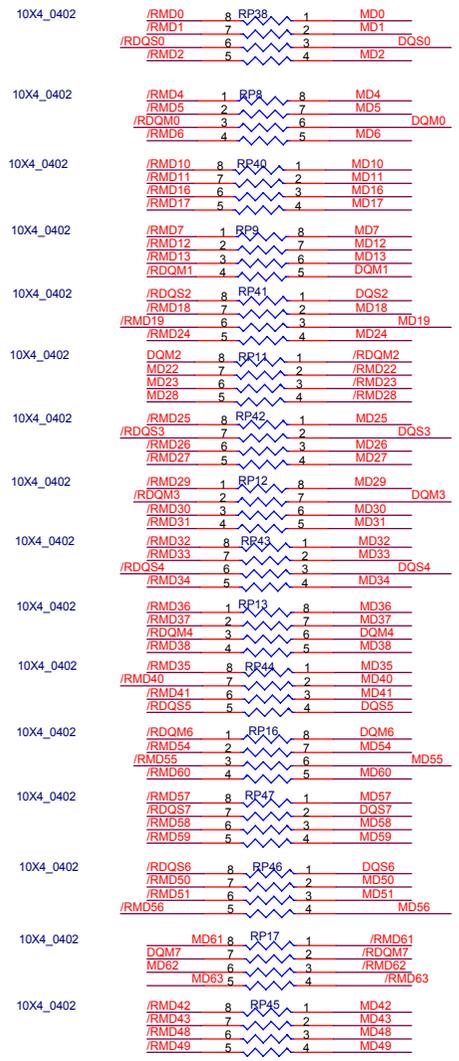
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Size	Document Number
Customer	G736-1-4-01
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P5-1

place this capacitor under 648 solder side



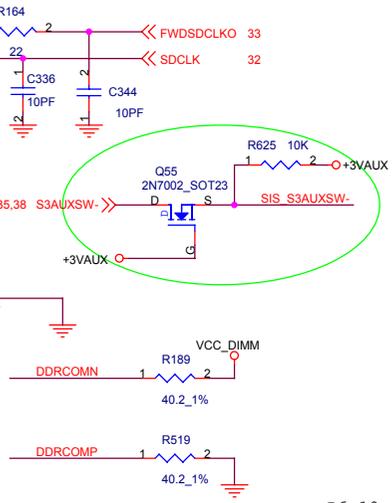
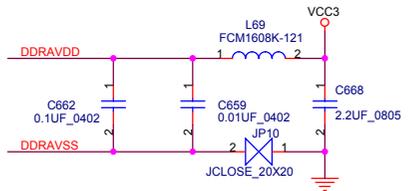
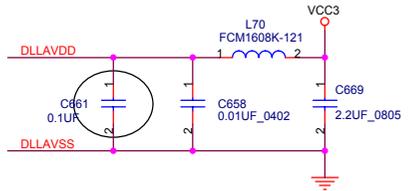
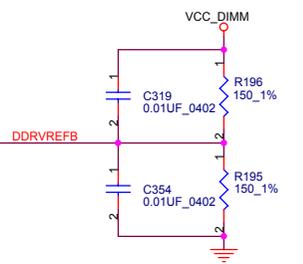
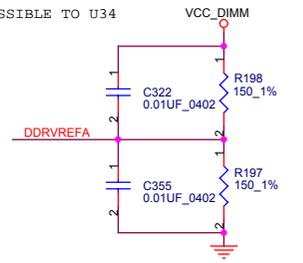
Resistors place close to DIMM1
Rs place close to DIMM1



648-2

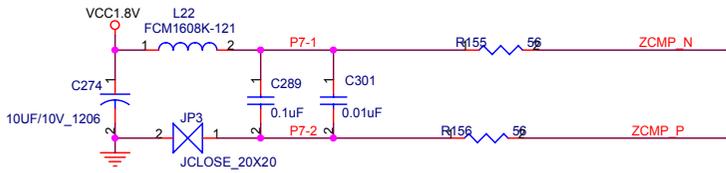
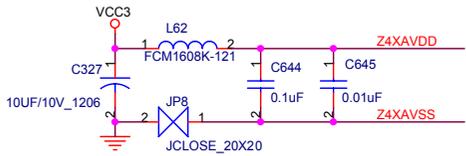
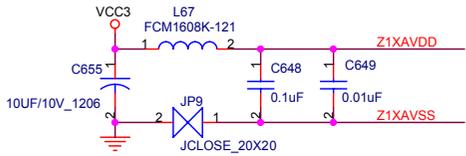
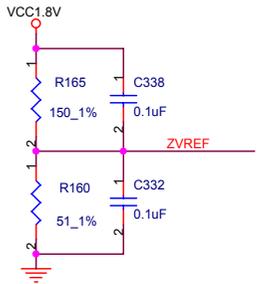
Rs place close to DIMM1

AS CLOSE AS POSSIBLE TO U34



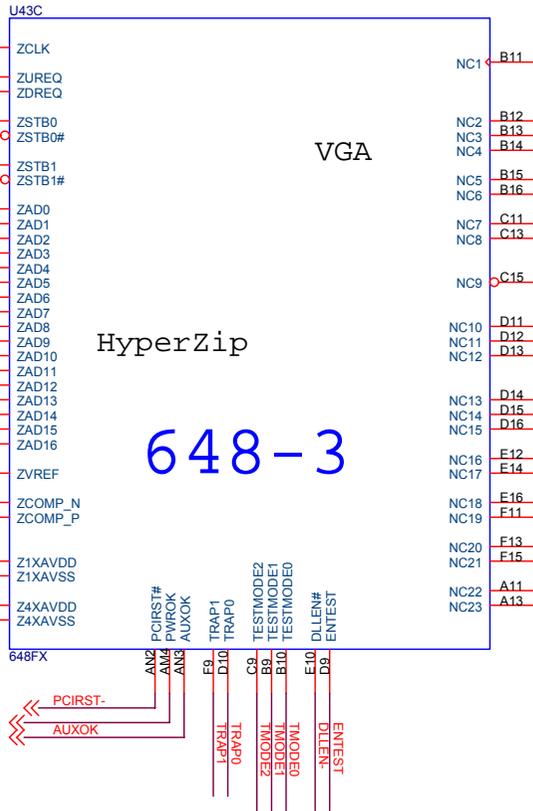
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Size CustomG736-1-4-01	Document Number	Rev 6.0
Date: Thursday, February 19, 2004	Sheet 6	of 42

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 16 ZSTB[0..1] << ZSTBI0..1I
 16 ZSTB[-0..1] << ZSTB-0I..1I

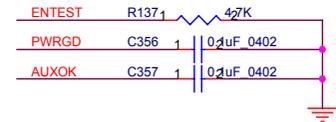
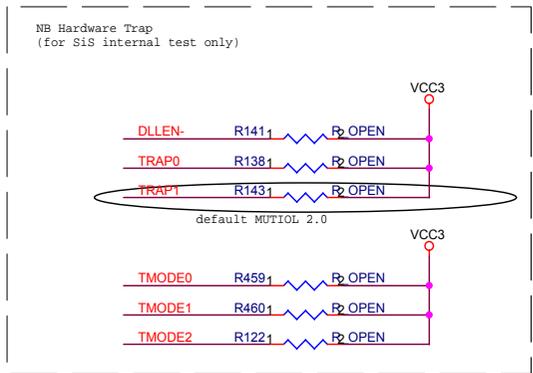


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 16 ZUREQ << ZUREQ AL4
 16 ZDREQ << ZDREQ AK5
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 ZSTB-0 AJ3
 ZSTB1 AE3
 ZSTB-1 AE2
 ZAD0 AH5
 ZAD1 AK2
 ZAD2 AJ4
 ZAD3 AJ6
 ZAD4 AH2
 ZAD5 AH4
 ZAD6 AG3
 ZAD7 AG6
 ZAD8 AF4
 ZAD9 AG2
 ZAD10 AF5
 ZAD11 AG4
 ZAD12 AD2
 ZAD13 AE6
 ZAD14 AE2
 ZAD15 AE4
 ZAD16 AL3
 ZVREF AK4
 ZCMP_N AD5
 ZCMP_P AD4
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 Z1XAVSS AM2
 Z4XAVDD AL2
 Z4XAVSS AL1

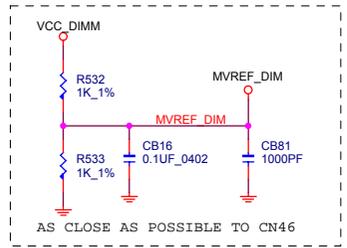
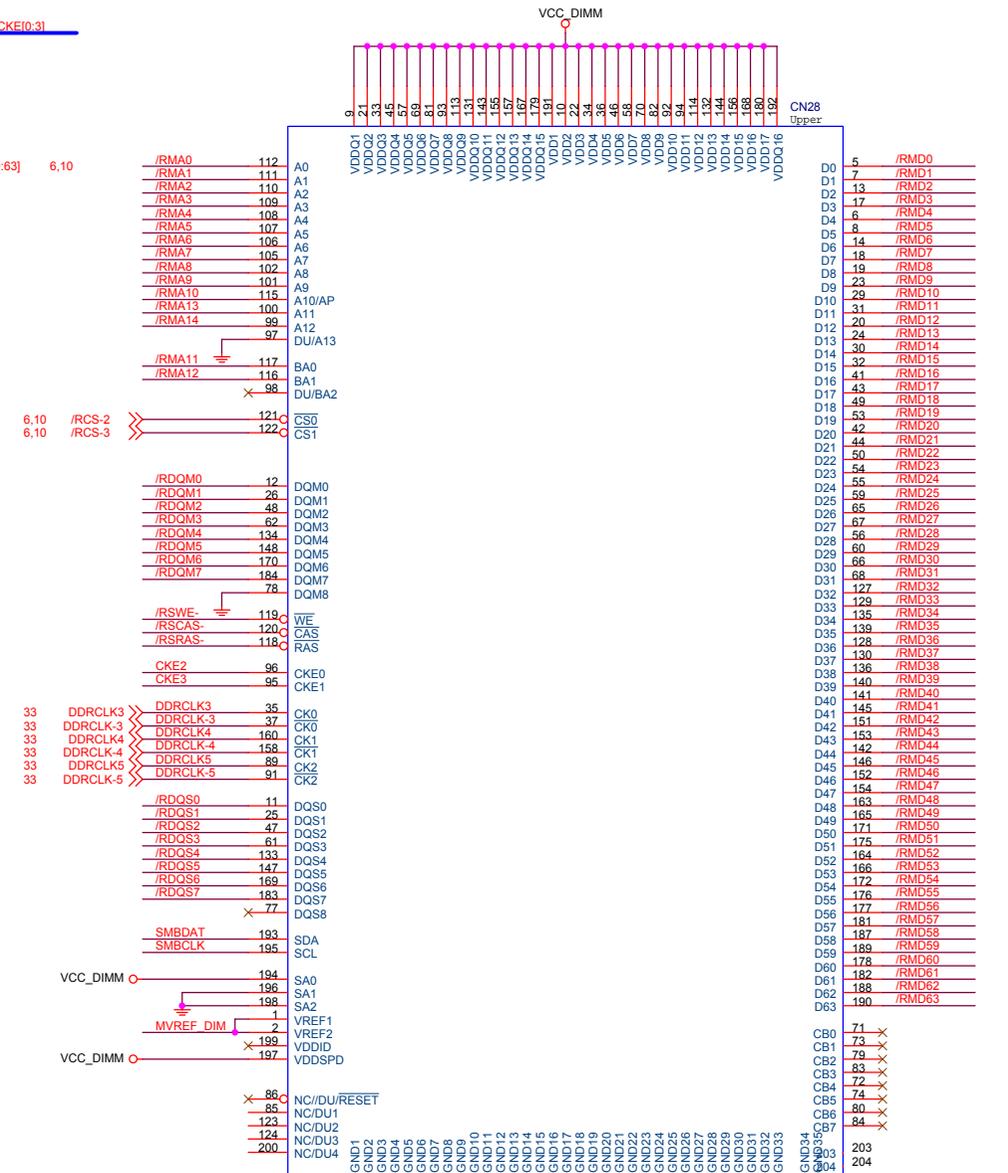
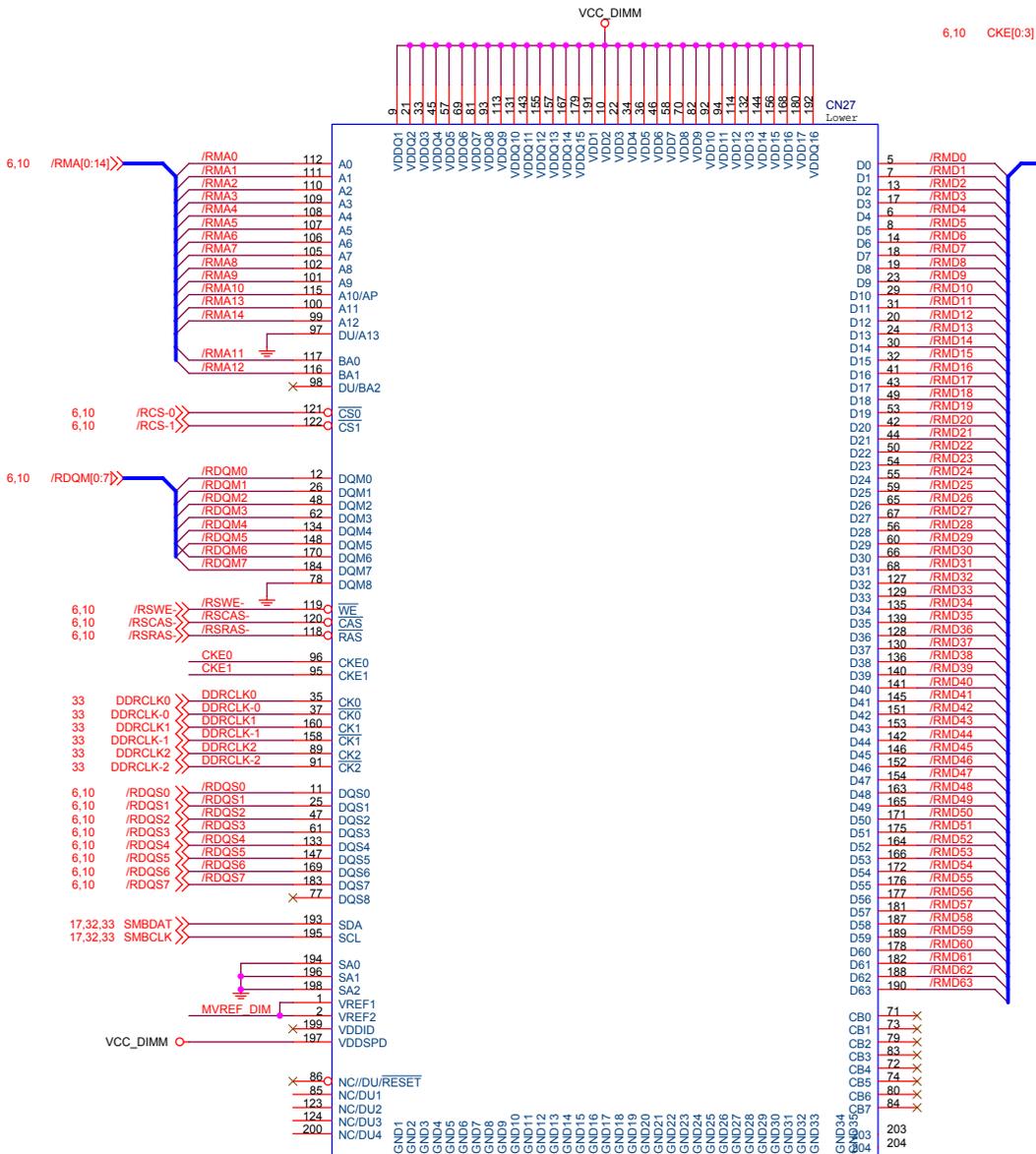
11,20,21,24,28,29,35 PCIRST-
 17,34 PWRGD
 17,30,34 AUXOK



PCIRST#
 PWRGD
 AUXOK
 TRAP1
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 TESTMODE2
 TESTMODE1
 TESTMODE0
 DLEN#
 ENTEST
 ENTEST
 DLEN#
 ENTEST

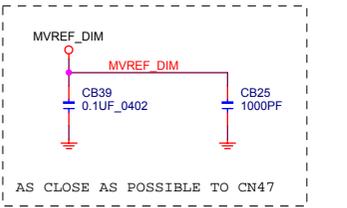


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Size B	Document Number G736-1-4-01	Rev 6.0
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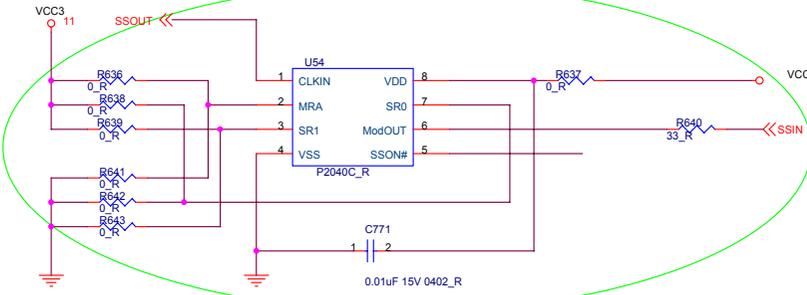
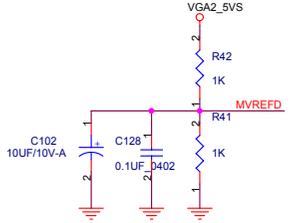
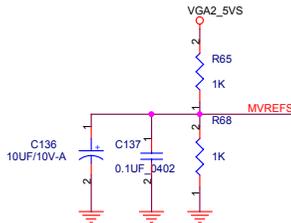
KEYLINK_5746-2-111_DDR92_S
Outsight

PC2100 - CL2 = 15 to Data 2-2-2/2.5-3-3
R = 0101 CL2.5 = 18.75 to Data
DDR266 256MB 4Bx8 Pmax = 8W
Ptyp = 7W
64MB/128MB/256MB = 500MB/s - 1.0W
- 1000MB/s - 1.65W
- 1500MB/s - 2.5W
- 2000MB/s - 3.2W



ECS CORP. (G736MB)			
Title DDR_SODIMM			
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14 M_DQMA[0..7] << M_DQMA[0..7] 15
 14 M_MAA[0..13] << M_MAA[0..13] 15
 14 M_MDA[0..63] << M_MDA[0..63] 15



14	M_QSA0	QSA0	J27	QSA0
14	M_QSA1	QSA1	F30	QSA1
14	M_QSA2	QSA2	F24	QSA2
14	M_QSA3	QSA3	B27	QSA3
14	M_QSA4	QSA4	E16	QSA4
14	M_QSA5	QSA5	B16	QSA5
14	M_QSA6	QSA6	F10	QSA6
14	M_QSA7	QSA7	B11	QSA7
14	M_RASA-	RASA#	A19	RASA#
14	M_CASA-	CASA#	E18	CASA#
14	M_WEA-	WEA#	E19	WEA#
14	M_CSA0-	CAS0#	F20	CAS0#
14	M_CSA1-	CSA1#	F20	CSA1#
14	M_CKEA	CKEA	B19	CKEA
14	M_CLKA0	CLKA0	B21	CLKA0
14	M_CLKA0-	CLKA0#	C20	CLKA0#
14	M_CLKA1	CLKA1	C18	CLKA1
14	M_CLKA1-	CLKA1#	A18	CLKA1#
14	TP115	D30	D30	D30
14	TP117	B13	B13	B13
14	MVREFD	MVREFD	B7	MVREFD
14	MVREFS	MVREFS	B8	MVREFS

M_DQMB[0..7] << M_DQMB[0..7] 15
 M_MAB[0..13] << M_MAB[0..13] 15
 M_MDB[0..63] << M_MDB[0..63] 15

MAB_0	N5	M_MAB0
MAB_1	M1	M_MAB1
MAB_2	L3	M_MAB2
MAB_3	L2	M_MAB3
MAB_4	M2	M_MAB4
MAB_5	M5	M_MAB5
MAB_6	P6	M_MAB6
MAB_7	N3	M_MAB7
MAB_8	K2	M_MAB8
MAB_9	K3	M_MAB9
MAB_10	J2	M_MAB10
MAB_11	P5	M_MAB11
MAB_12	P2	M_MAB12
MAB_13	P3	M_MAB13
MAB_14	P2	M_MAB14

DQMB#0	E6	M_DQMB-0
DQMB#1	B2	M_DQMB-1
DQMB#2	J5	M_DQMB-2
DQMB#3	C3	M_DQMB-3
DQMB#4	W6	M_DQMB-4
DQMB#5	W2	M_DQMB-5
DQMB#6	AC6	M_DQMB-6
DQMB#7	AD2	M_DQMB-7

QSB0	F6	QSB0	M_QSB0	15
QSB1	B3	QSB1	M_QSB1	15
QSB2	K6	QSB2	M_QSB2	15
QSB3	G1	QSB3	M_QSB3	15
QSB4	V5	QSB4	M_QSB4	15
QSB5	W1	QSB5	M_QSB5	15
QSB6	AC3	QSB6	M_QSB6	15
QSB7	AD1	QSB7	M_QSB7	15

RASB# R2 M_RASB- << M_RASB- 15
 CASB# T5 M_CASB- << M_CASB- 15

WEB# T6 M_WEB- << M_WEB- 15
 CSB0# R5 M_CSB0- << M_CSB0- 15

CSB1# R6 << M_CSB1- 15
 CKEB R3 << M_CKEB 15

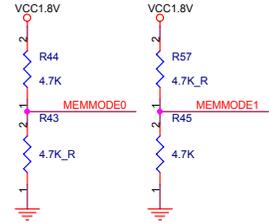
CLKB0 N2 << M_CLKB0 15
 CLKB0# T2 << M_CLKB0- 15

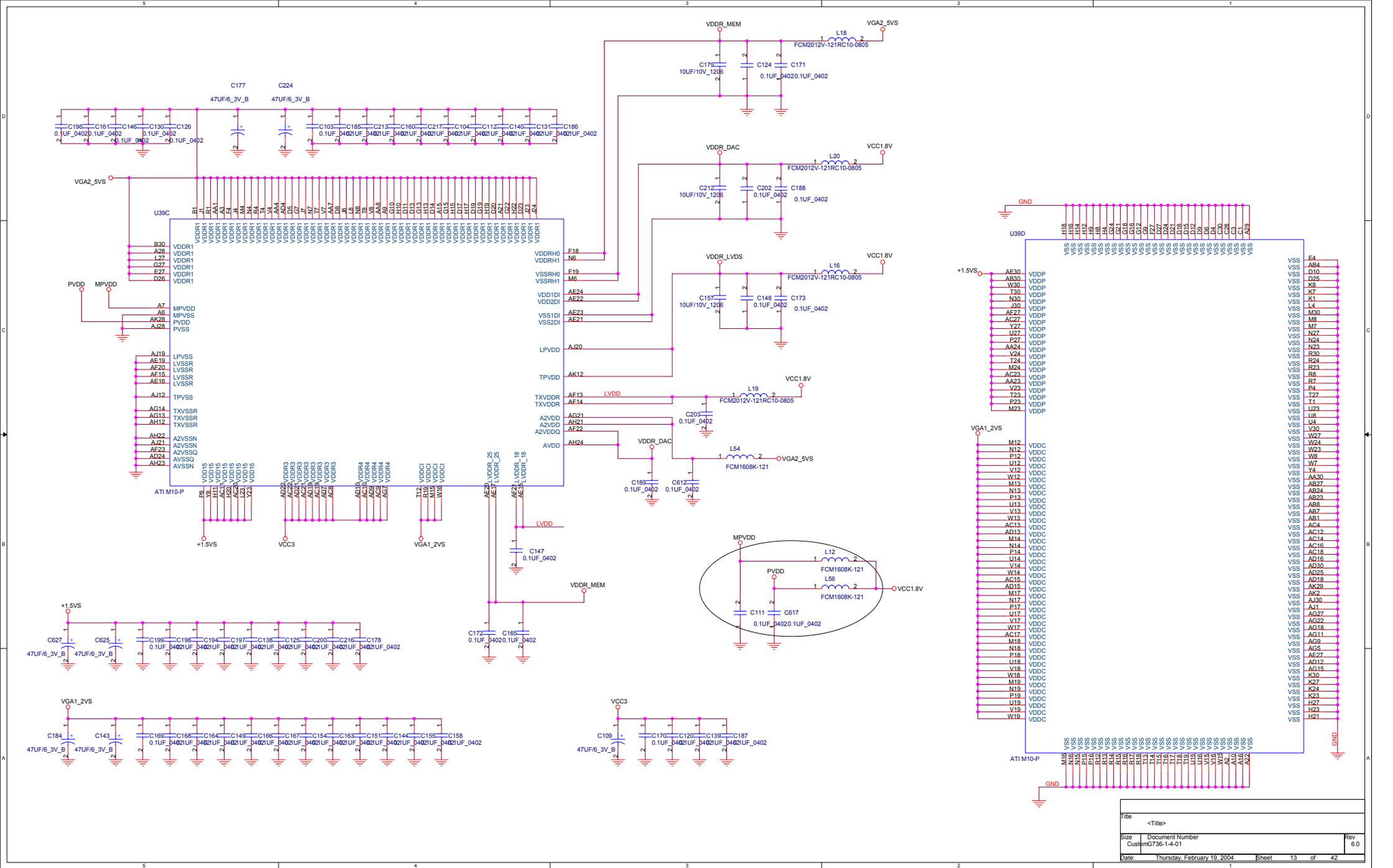
CLKB1 T3 << M_CLKB1 15
 CLKB1# T3 << M_CLKB1- 15

DIMB_0 E3 1 TP116
 DIMB_1 AA3 1 TP118

ROMCS# AF5 1 TP119

MEMMODE[1:0]	
01	:VDDR1 2.5V (SSTL-2/DDR)
10	:VDDR1 1.8V (SLP1DA/DDR)
11	:VDDR1 2.8V (SST-2/DDR)





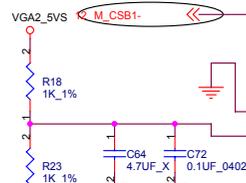
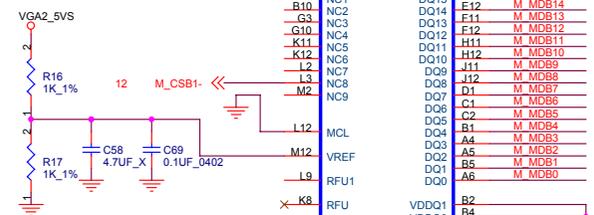
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Size	Document Number	Rev
	Custom6736-1-4-01	6.0
Date	Thursday, February 19, 2004	Sheet 13 of 42

All of signal trace 5mil spacing 10mil .

M MAB13	M3	BA0	DO31	A7	M MDB31
M MAB12	M4	BA1	DO30	B8	M MDB30
			DO29	A8	M MDB29
M MAB11	M6	A11	DO28	A9	M MDB28
M MAB10	M5	A10	DO27	B12	M MDB27
M MAB9	M7	A9	DO26	C11	M MDB26
M MAB8	M10	A8/AP	DO25	C12	M MDB25
M MAB7	M9	A7	DO24	D12	M MDB24
M MAB6	M8	A6	DO23	J2	M MDB23
M MAB5	M8	A6	DO22	J1	M MDB22
M MAB4	M7	A4	DO21	H1	M MDB21
M MAB3	M6	A3	DO20	H2	M MDB20
M MAB2	M5	A2	DO19	F1	M MDB19
M MAB1	M4	A1	DO18	F2	M MDB18
M MAB0	M4	A0	DO17	E1	M MDB17
			DO16	E2	M MDB16
			DO15	E11	M MDB15
			DO14	E12	M MDB14
			DO13	F11	M MDB13
			DO12	F12	M MDB12
			DO11	H12	M MDB11
			DO10	H11	M MDB10
			DO9	J11	M MDB9
			DO8	J12	M MDB8
			DO7	D1	M MDB7
			DO6	C2	M MDB6
			DO5	B1	M MDB5
			DO4	A4	M MDB4
			DO3	A5	M MDB3
			DO2	B5	M MDB2
			DO1	B6	M MDB1
			DO0	A6	M MDB0

12 M_DQMB[0..7] << M_DQMB[0..7]
 12 M_MAB[0..13] << M_MAB[0..13]
 12 M_MDB[0..63] << M_MDB[0..63]

M MAB13	M3	BA0	DO31	A7	M MDB63
M MAB12	M4	BA1	DO30	B8	M MDB62
			DO29	A8	M MDB61
M MAB11	M6	A11	DO28	B12	M MDB60
M MAB10	M5	A10	DO27	C11	M MDB59
M MAB9	M7	A9	DO26	C12	M MDB58
M MAB8	M10	A8/AP	DO25	D12	M MDB57
M MAB7	M9	A7	DO24	J2	M MDB56
M MAB6	M8	A6	DO23	J1	M MDB55
M MAB5	M8	A6	DO22	J1	M MDB54
M MAB4	M7	A4	DO21	H1	M MDB53
M MAB3	M6	A3	DO20	H2	M MDB52
M MAB2	M5	A2	DO19	F1	M MDB51
M MAB1	M4	A1	DO18	F2	M MDB50
M MAB0	M4	A0	DO17	E1	M MDB49
			DO16	E2	M MDB48
			DO15	E11	M MDB47
			DO14	E12	M MDB46
			DO13	F11	M MDB45
			DO12	F12	M MDB44
			DO11	H12	M MDB43
			DO10	H11	M MDB42
			DO9	J11	M MDB41
			DO8	J12	M MDB40
			DO7	D1	M MDB39
			DO6	C1	M MDB38
			DO5	B1	M MDB37
			DO4	A4	M MDB36
			DO3	A5	M MDB35
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			DO1	B6	M MDB33
			DO0	A6	M MDB32

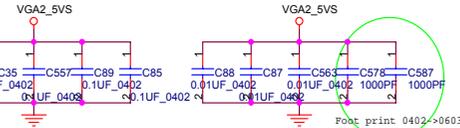
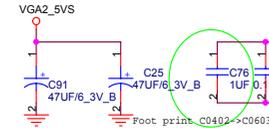
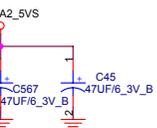
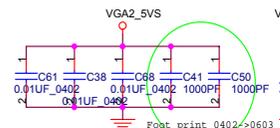
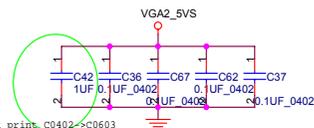
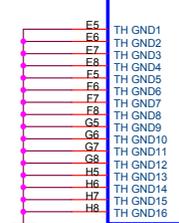
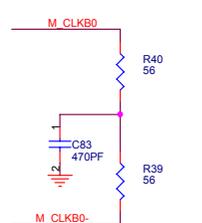
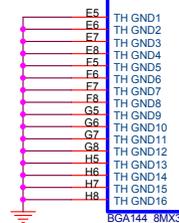


- 12 M_CLKB0- << M_CLKB0-
- 12 M_CSBO- << M_CSBO-
- 12 M_RASB- << M_RASB-
- 12 M_CASB- << M_CASB-
- 12 M_WEB- << M_WEB-
- M_DQMB-3 A11
- M_DQMB-2 G2
- M_DQMB-1 G11
- M_DQMB-0 A2
- 12 M_CLKB0 << M_CLKB0
- 12 M_CKEB << M_CKEB

- 12 M_CLKB1- << M_CLKB1-
- 12 M_CSBO- << M_CSBO-
- 12 M_RASB- << M_RASB-
- 12 M_CASB- << M_CASB-
- 12 M_WEB- << M_WEB-
- M_DQMB-7 A11
- M_DQMB-6 G2
- M_DQMB-5 G11
- M_DQMB-4 A2
- 12 M_CLKB1 << M_CLKB1
- 12 M_CKEB << M_CKEB

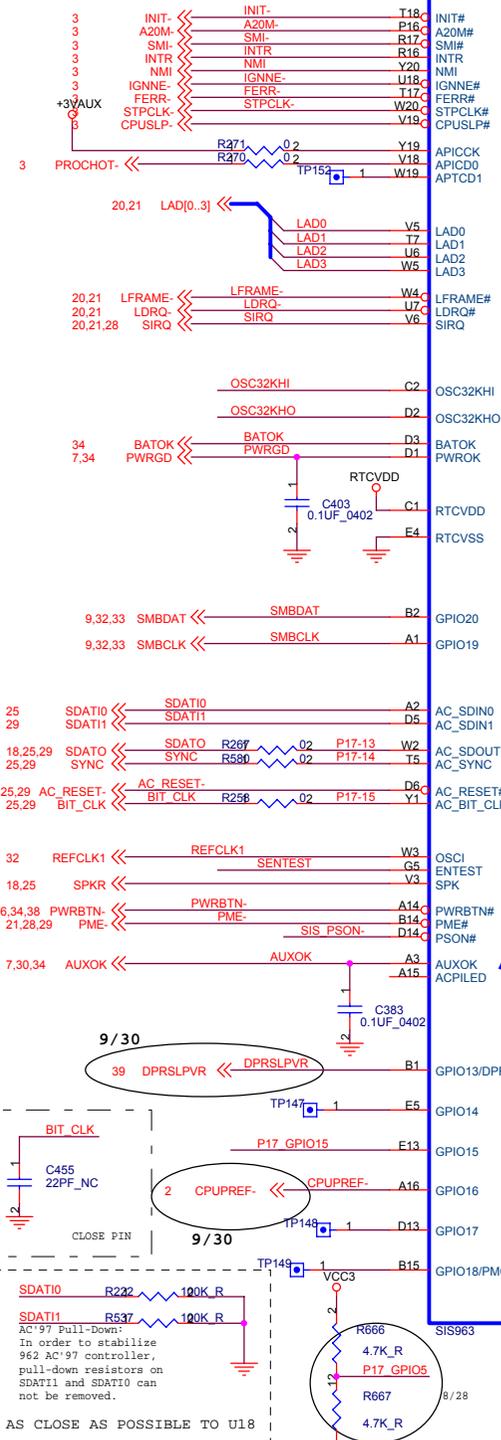
- 12 M_QSB3 << M_QSB3 M_QSB0-3 A12
- 12 M_QSB2 << M_QSB2 M_QSB0-2 G1
- 12 M_QSB1 << M_QSB1 M_QSB0-1 G12
- 12 M_QSB0 << M_QSB0 M_QSB0-0 A1

- 12 M_QSB7 << M_QSB7 M_QSB0-7 A12
- 12 M_QSB6 << M_QSB6 M_QSB0-6 G1
- 12 M_QSB5 << M_QSB5 M_QSB0-5 G12
- 12 M_QSB4 << M_QSB4 M_QSB0-4 A1



ECS CORP.	
Title	DDR_SG4Mx32_BGA_B
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Programmable on-die pull-high strength for CPU_S:
 (Infinite, 150, 110, 56 Ohm)



CPU_S

APIC

LPC

RTC

GPIO

AC97

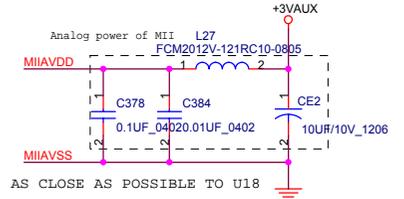
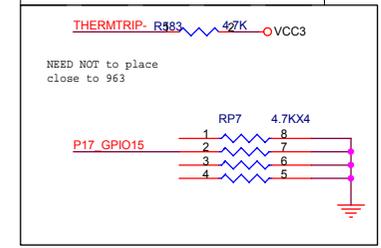
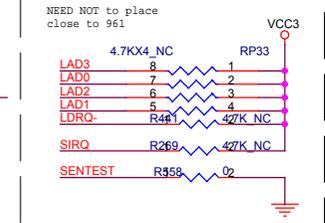
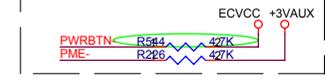
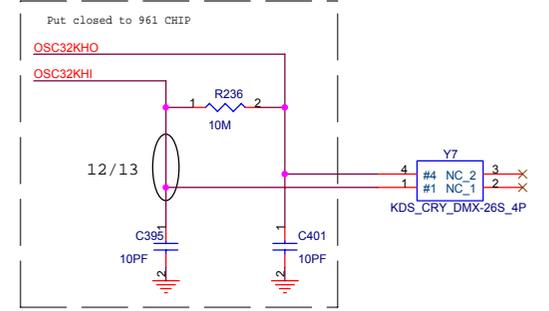
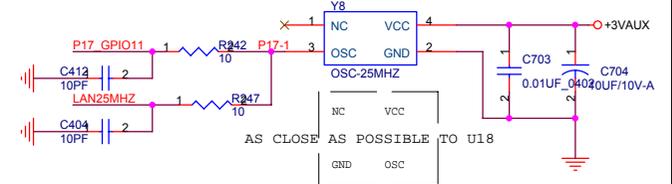
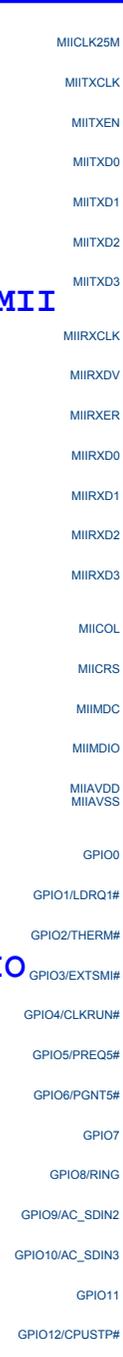
ACPI / OTHER

KBC /geyserville

U22B

MII

GPIO



ECS CORP. (G736 M/B)		
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Size	Document Number	Rev
Custom	G736-1-4-01	6.A
Date:	Thursday, February 19, 2004	Sheet 17 of 42

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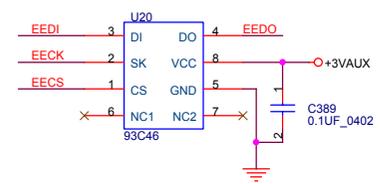
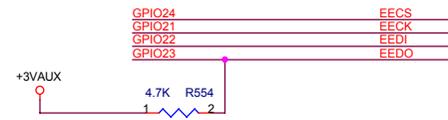
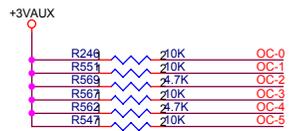
AS CLOSE AS POSSIBLE TO U18

9/30

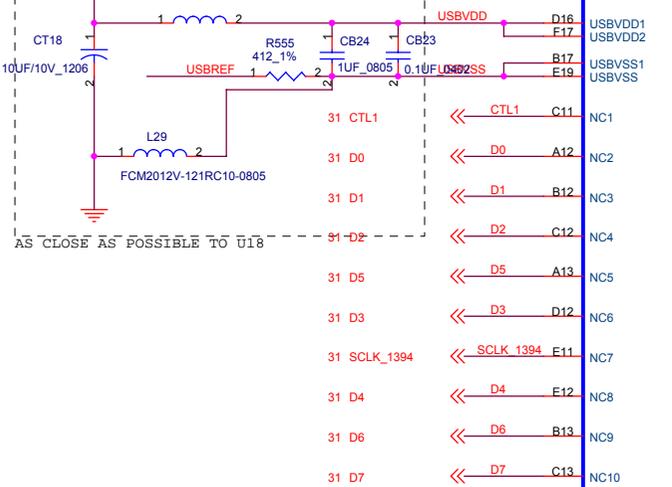
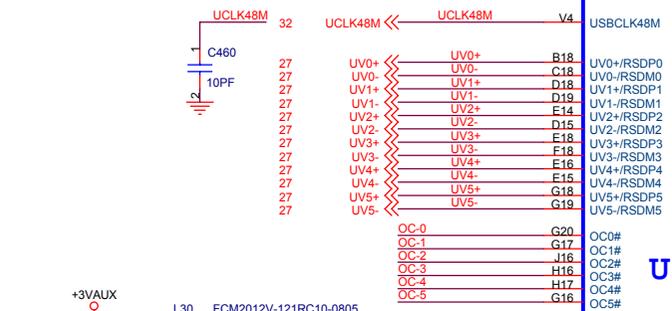
GPIO12 / CPU_STP-

18,30,39

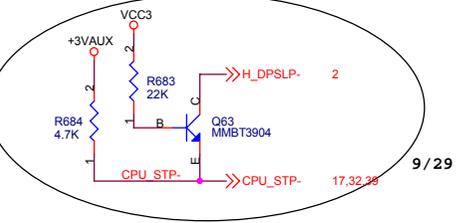
VCC3



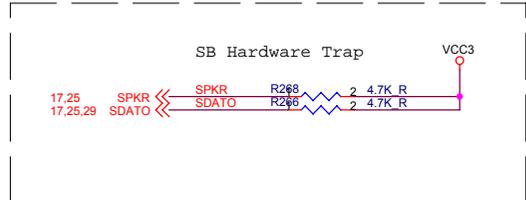
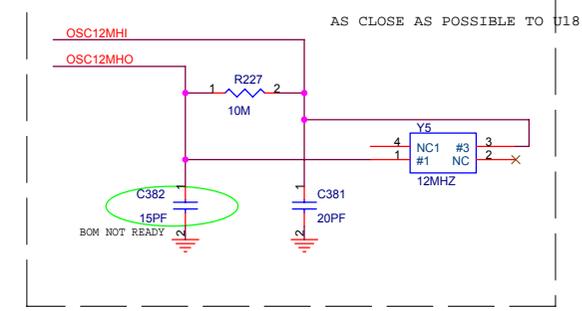
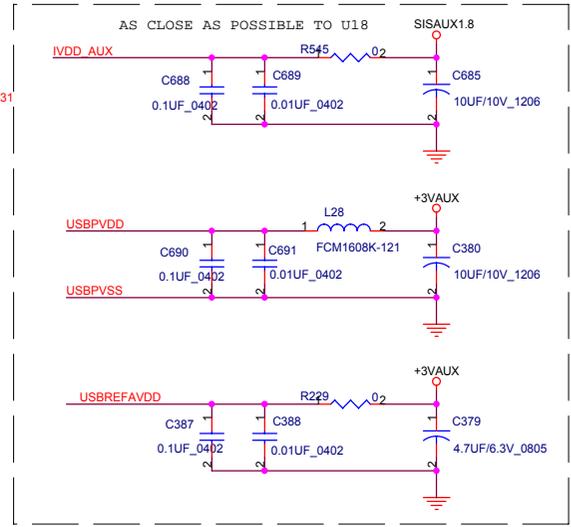
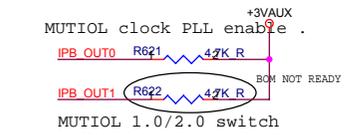
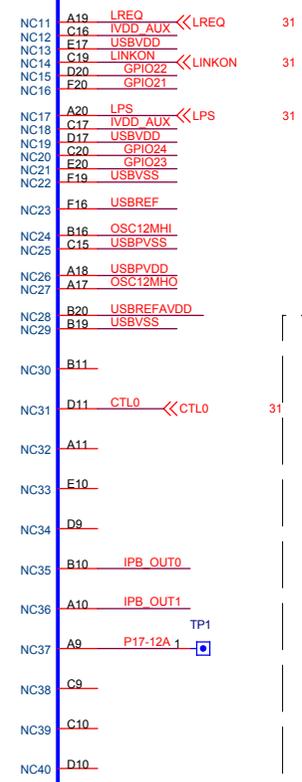
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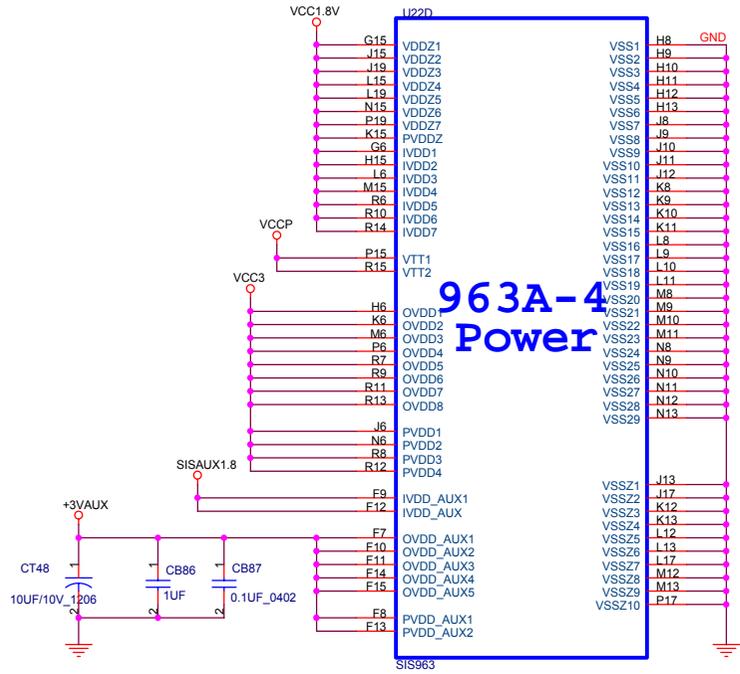
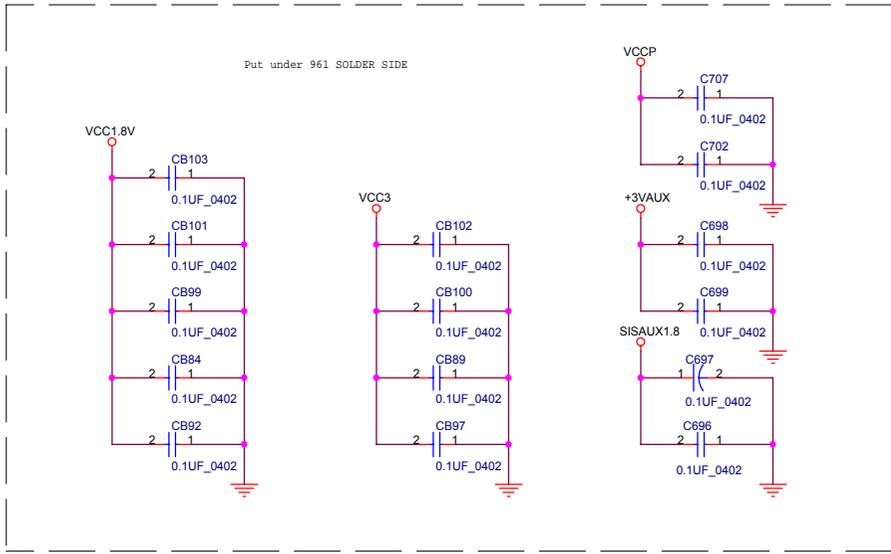
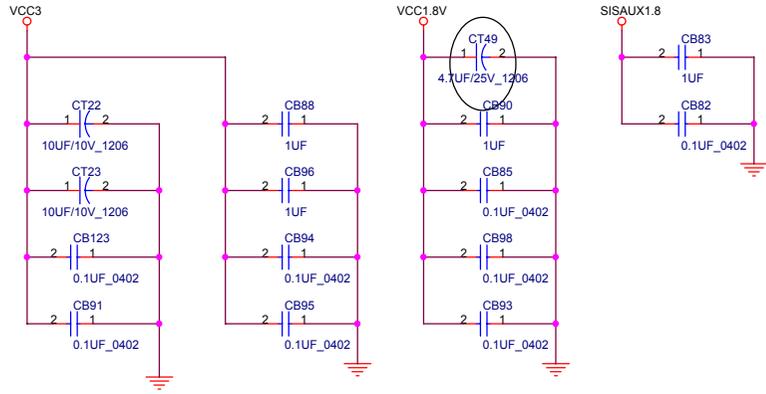


963A-3

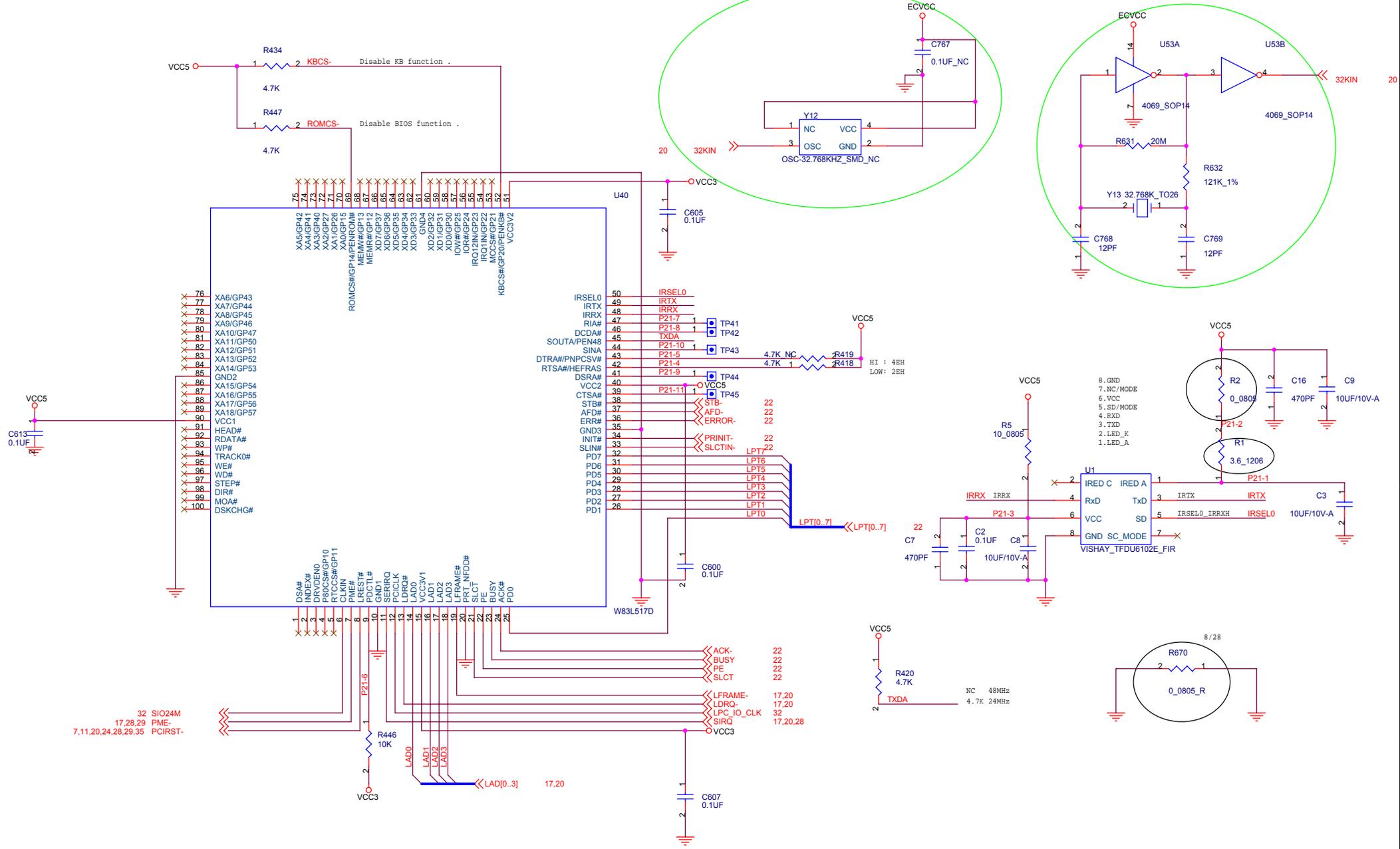


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SPKR(LPC addr mapping)	disable	enable	0
SDATO(PCICLK PLL)	enable	disable	0
OC2-(SB debug mode)	enable	disable	1
OC5-(Trap mode)	PCI AD	ROM	1

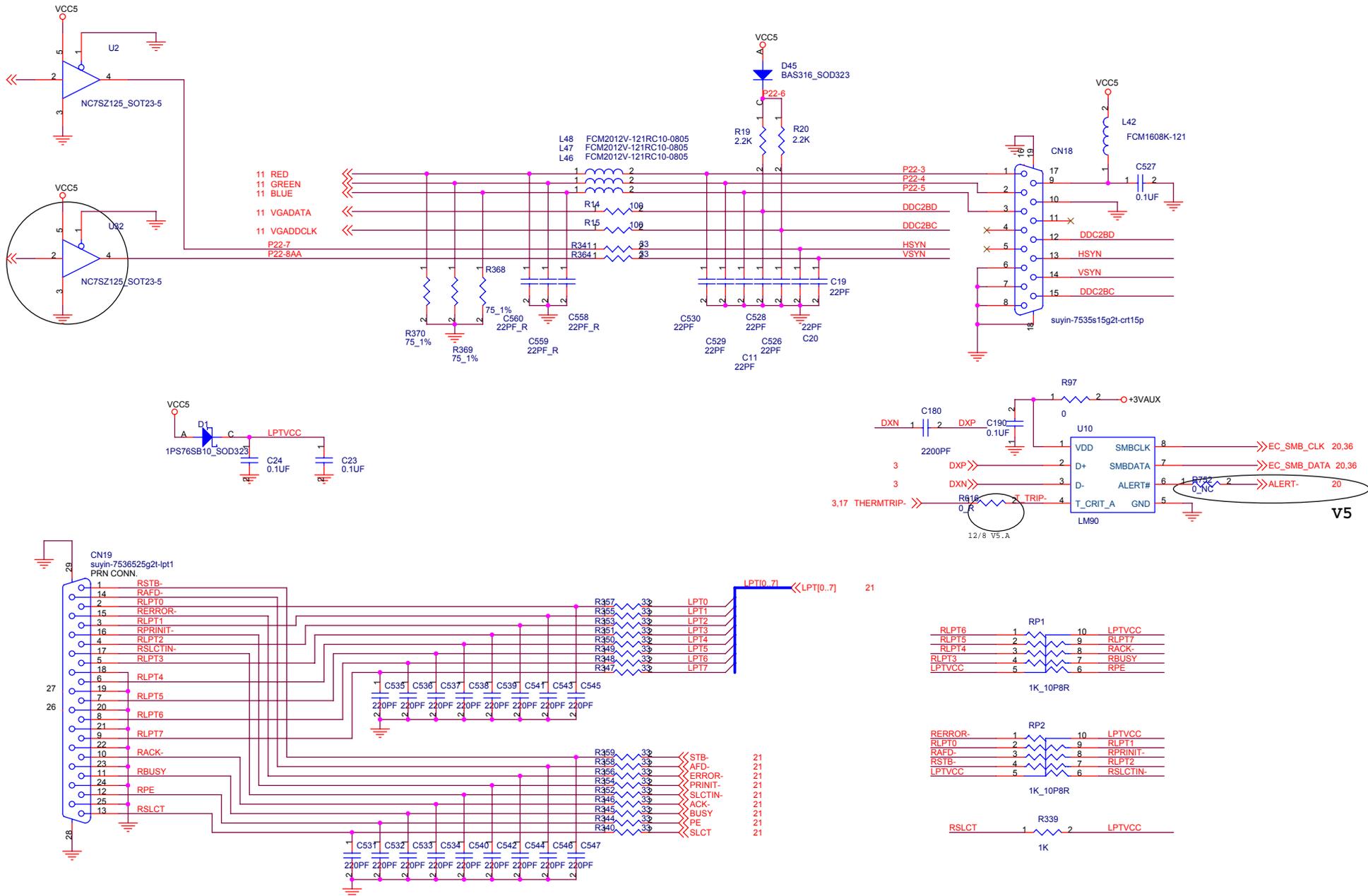




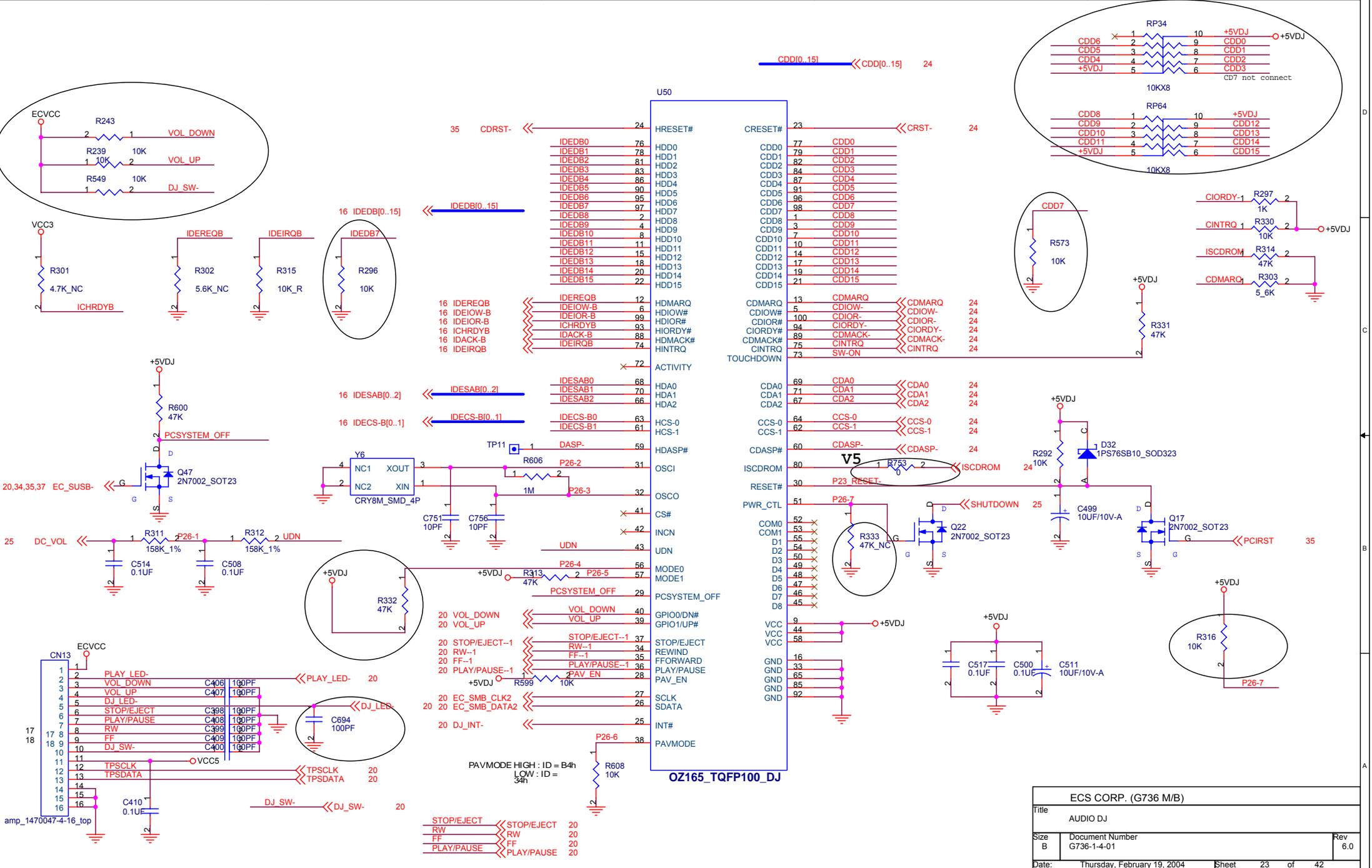
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Custom	G736-1-4-01	6.0
Date:	Thursday, February 19, 2004	Sheet 19 of 42



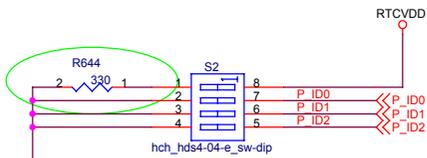
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Title SUPER I/O & IR			
Size Custom	Document Number G736-1-4-01	Rev 6.0	
Date: Thursday, February 19, 2004	Sheet 21	of 42	



ECS CORP. (G736M/B)		
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Size Custom	Document Number G736-1-4-01	Rev 6.0
Date: Thursday, February 19, 2004	Sheet 22	of 42

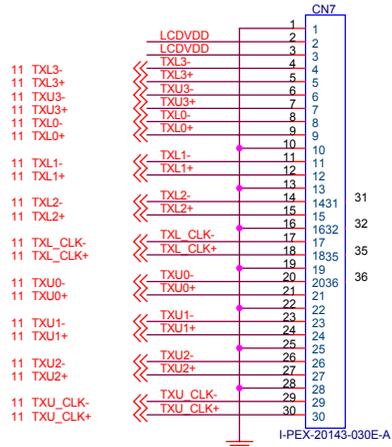
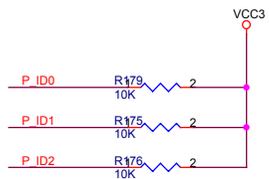


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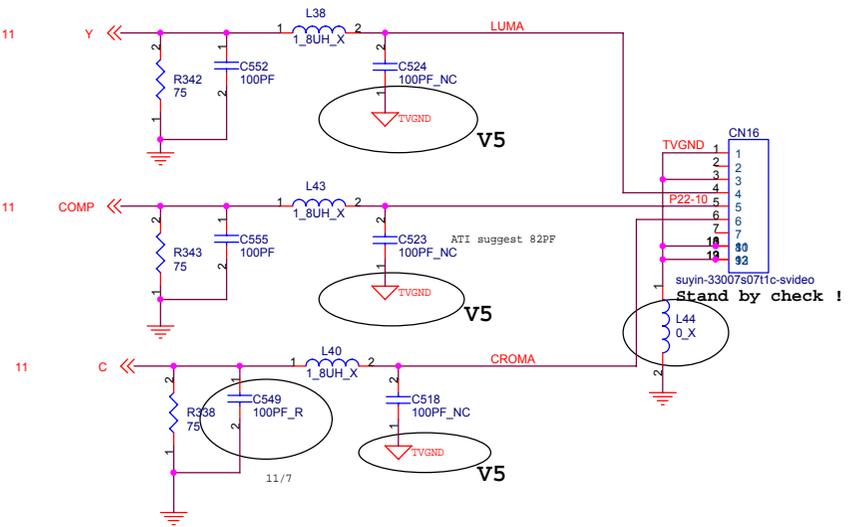
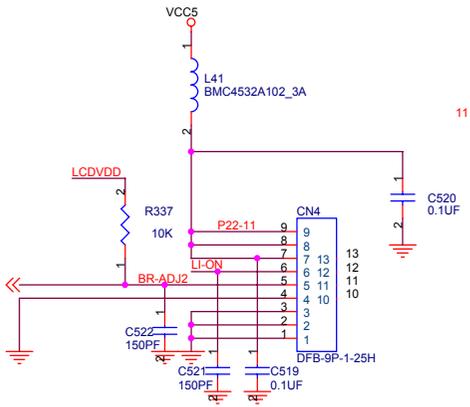
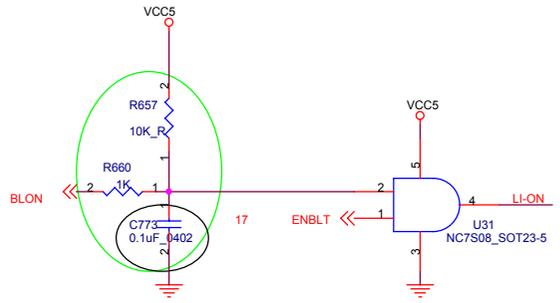
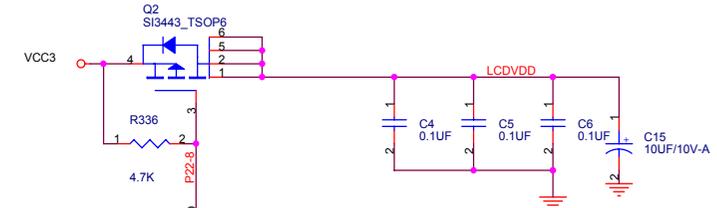
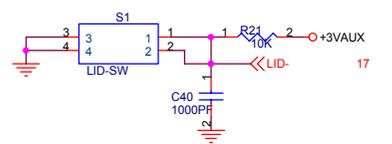
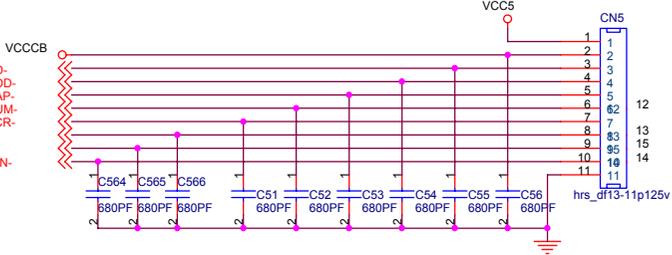


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OFF	OFF	ON	16 UXGA 1600*1200
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OFF	ON	OFF	15.4 WSXGA 1680*1050
ON	OFF	OFF	15.4 WUXGA 1920*1200

12/23

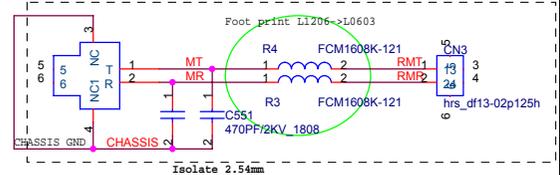
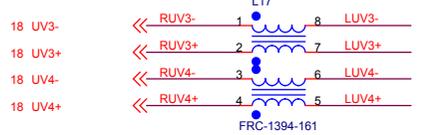
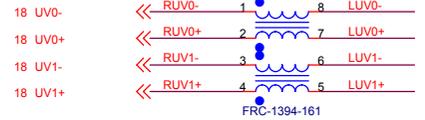
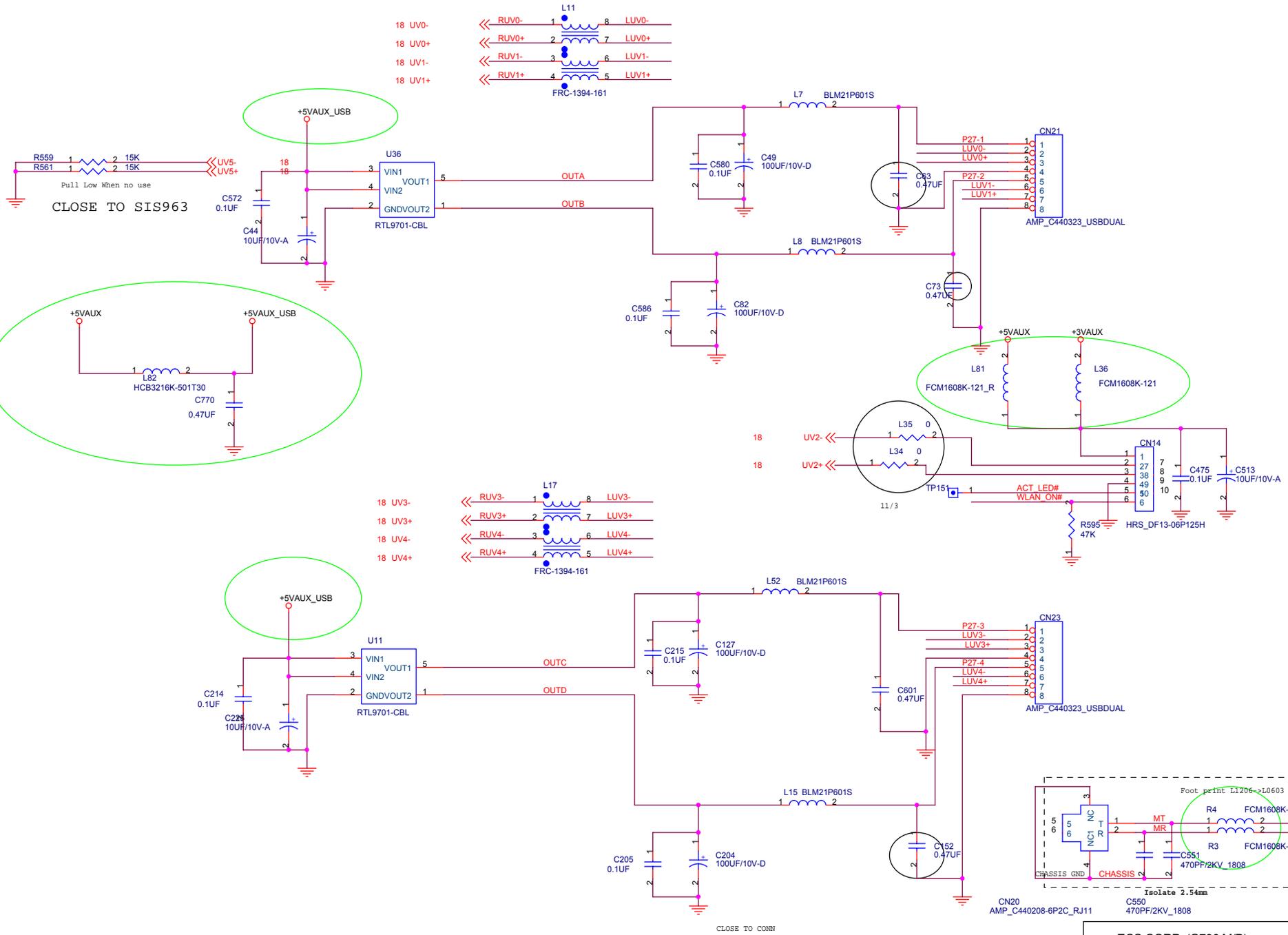


- 24 CD_LED-
- 24 LED_HDD-
- 20 LED_CAP-
- 20 LED_NUM-
- 20 LED_SCR-
- 20 MAIL-K-
- 20 IE-K-
- 17,20,34,38 PWRBTN-



ECS CORP. (M/B)		
Title LCD CRT & TV CONNECTOR		
Size	Document Number	Rev
Customer	G736-1-4-01	6.0
Date	Thursday, February 19, 2004	Sheet 26 of 42

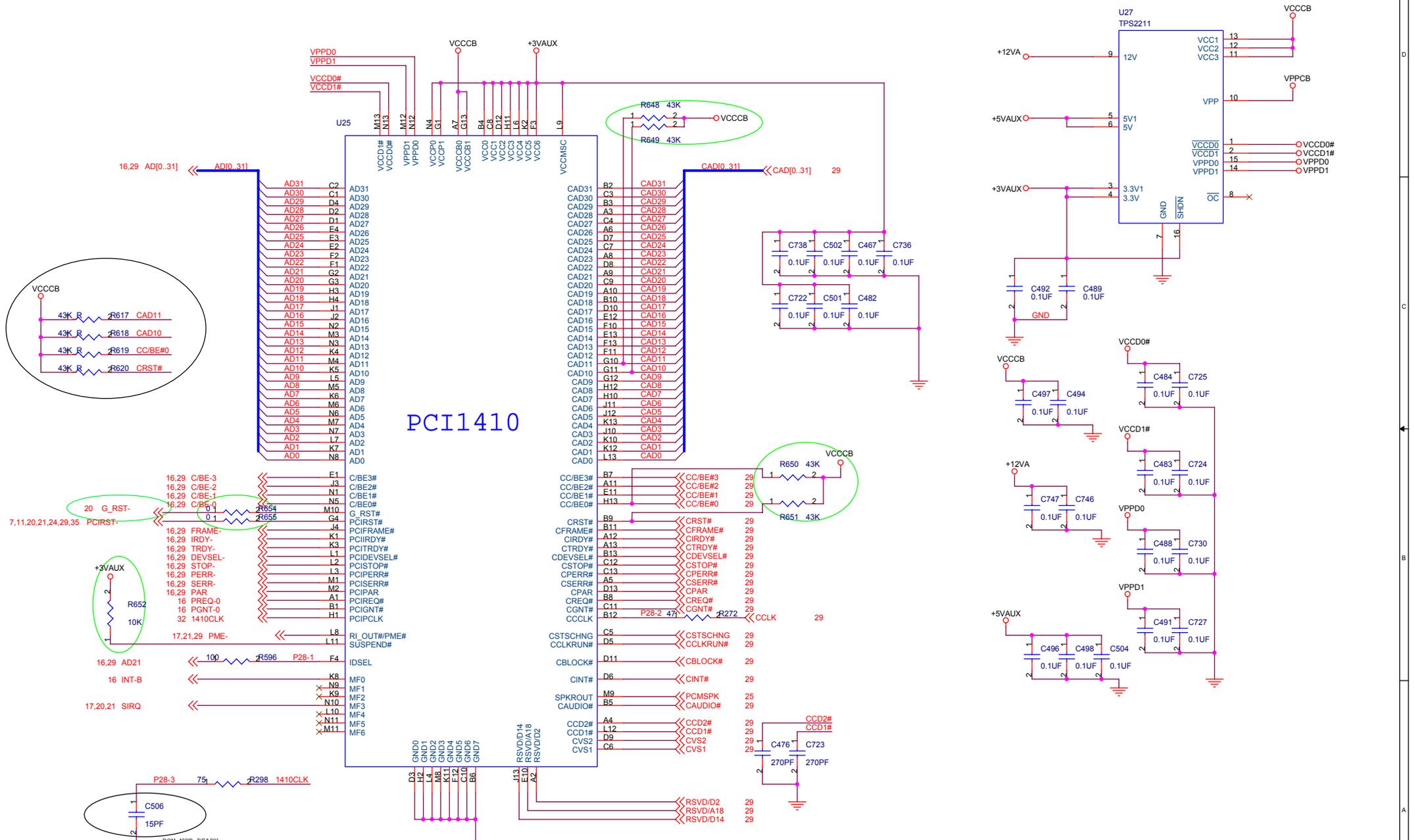
P22-11



ECS CORP. (G736 M/B)		
Title	USB CONN & RJ11	
Size	Document Number	Rev
Custom	G736-1-4-01	6.0
Date:	Thursday, February 19, 2004	Sheet 27 of 42

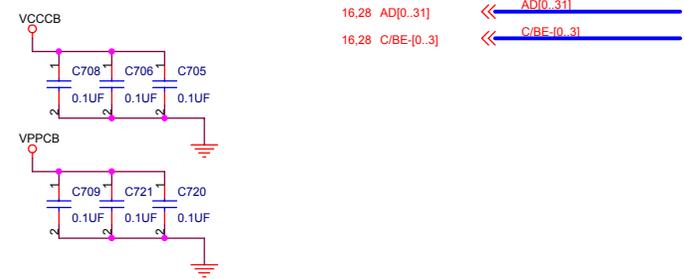
CLOSE TO CONN

PCI1410

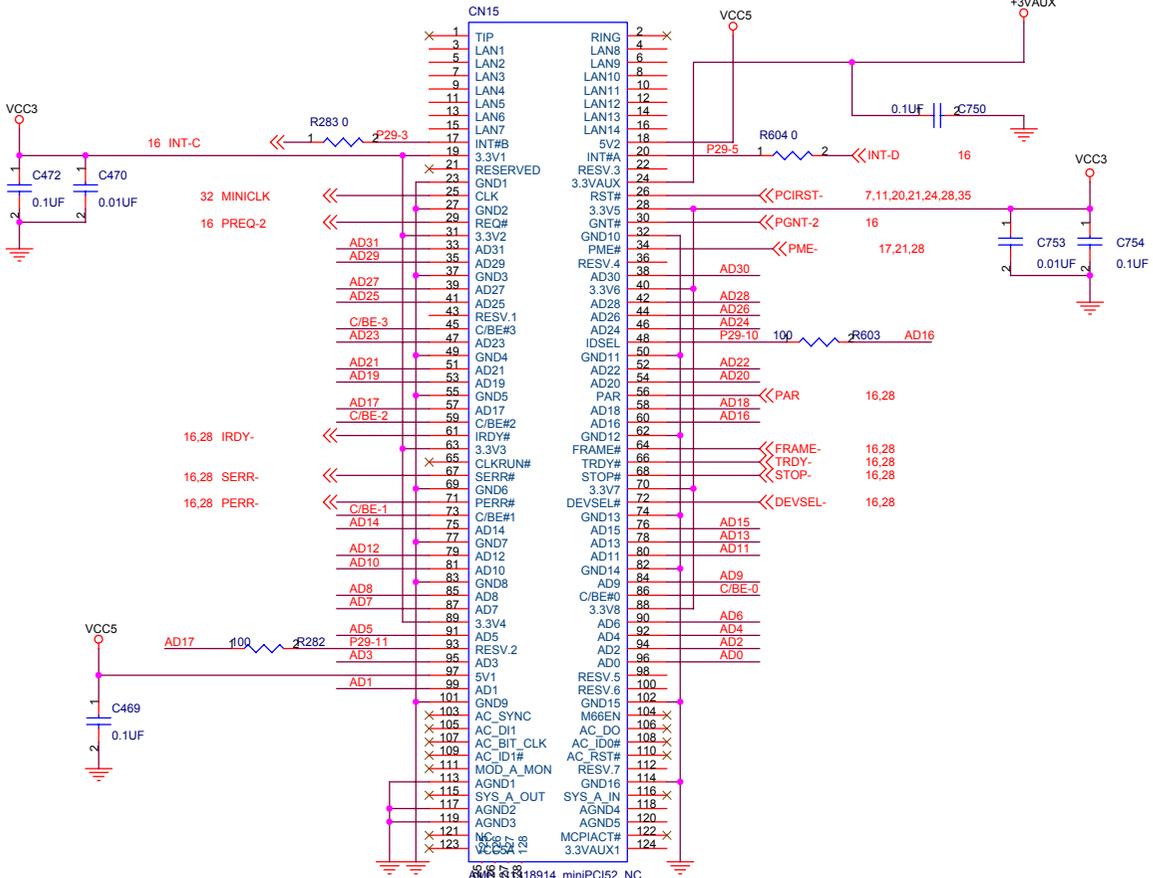
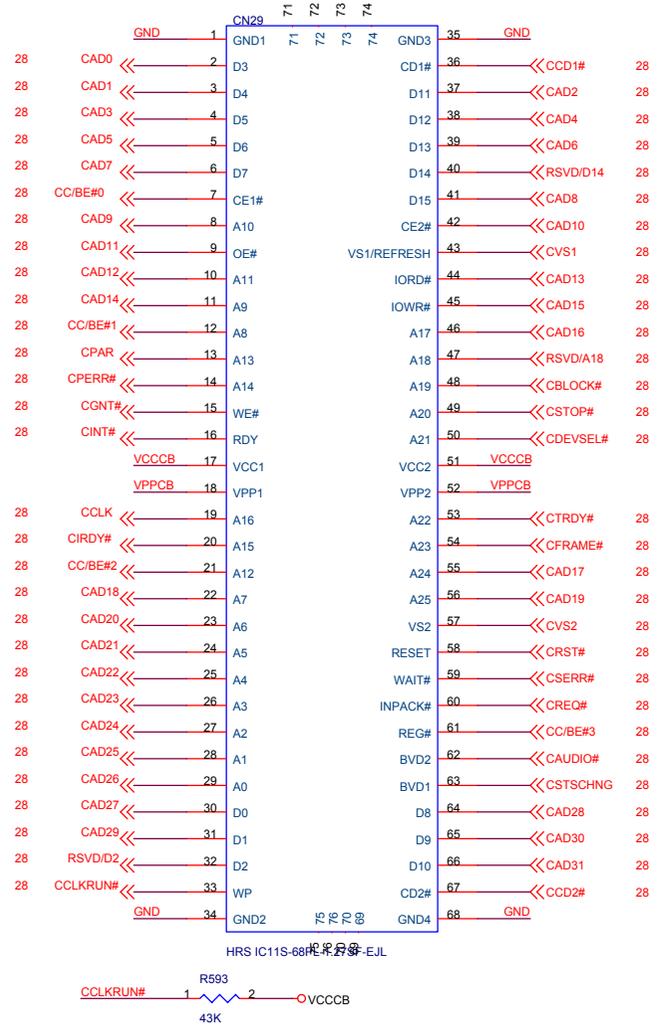


ECS CORP. (G736M/B)		
Title PCI 1410		
Size Custom	Document Number G736-1-4-01	Rev 6.0
Date: Thursday, February 19, 2004	Sheet 28	of 42

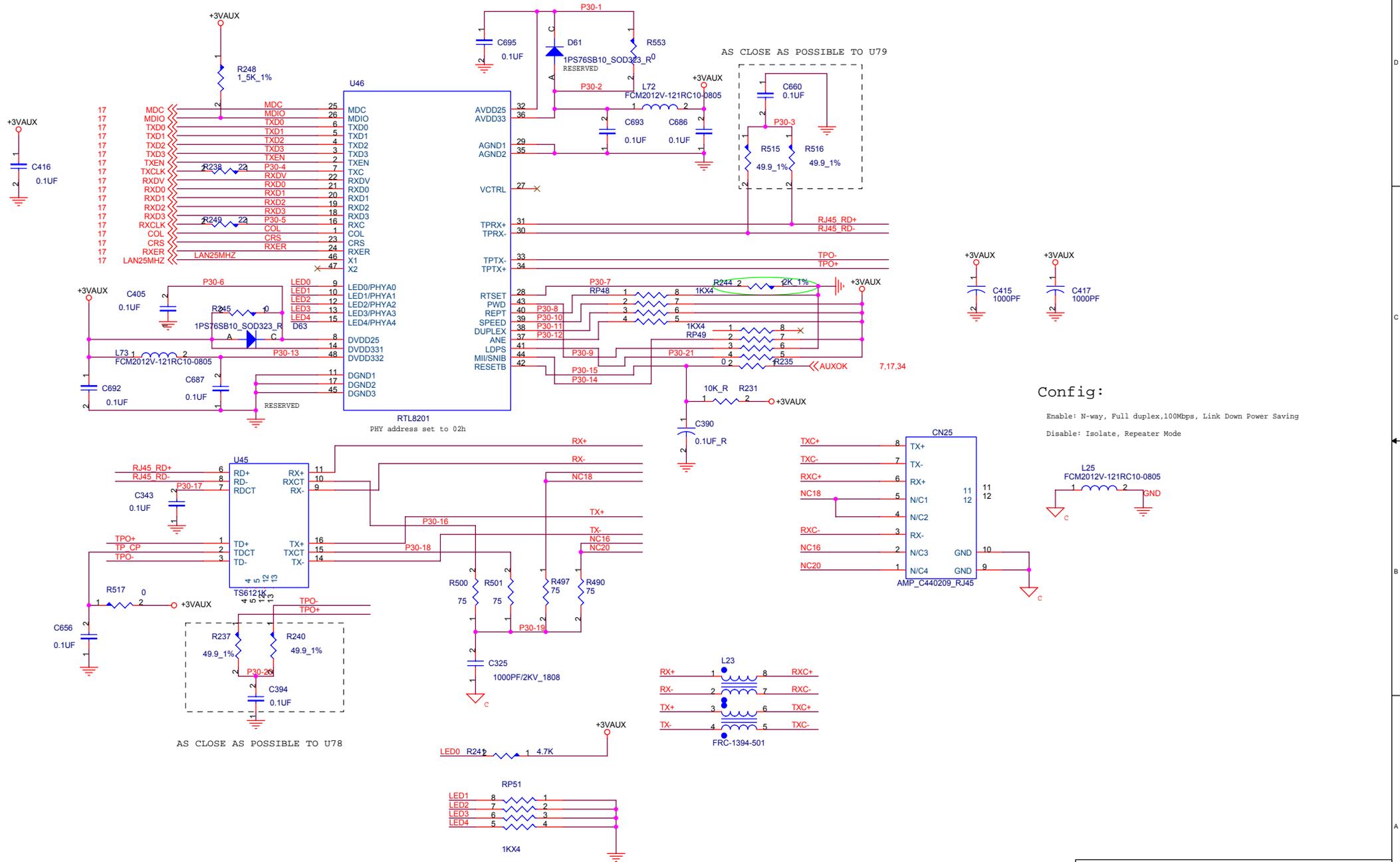
MINI PCI SOCKET



PCMCIA SLOT

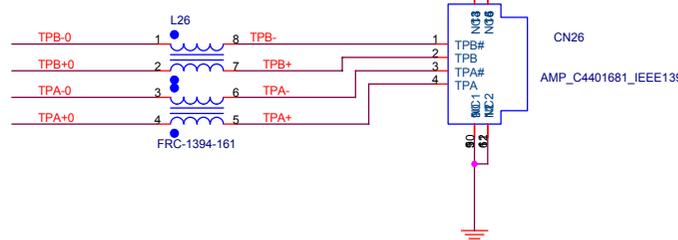
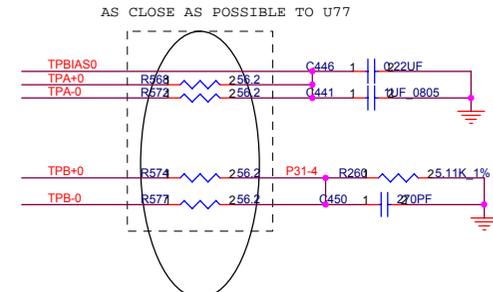
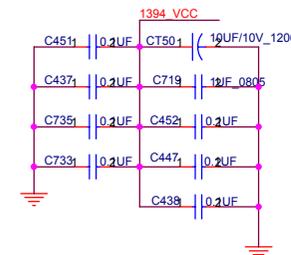
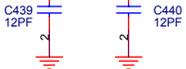
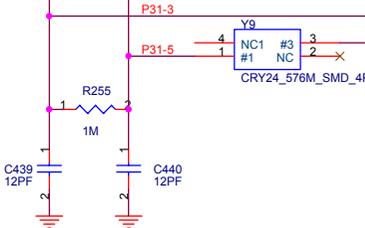
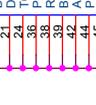
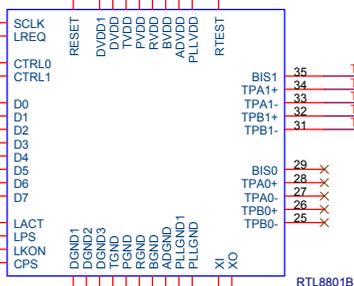
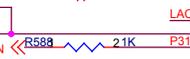
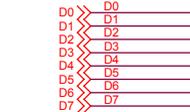
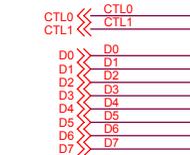
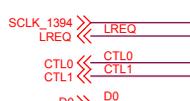
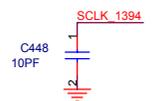
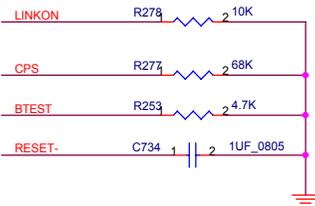
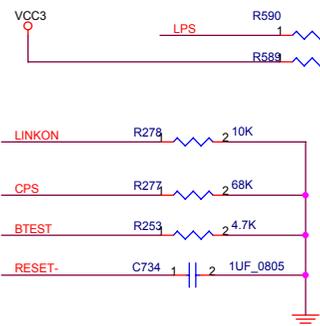


RTL8201



Enable: N-way, Full duplex, 100Mbps, Link Down Power Saving
 Disable: Isolate, Repeater Mode

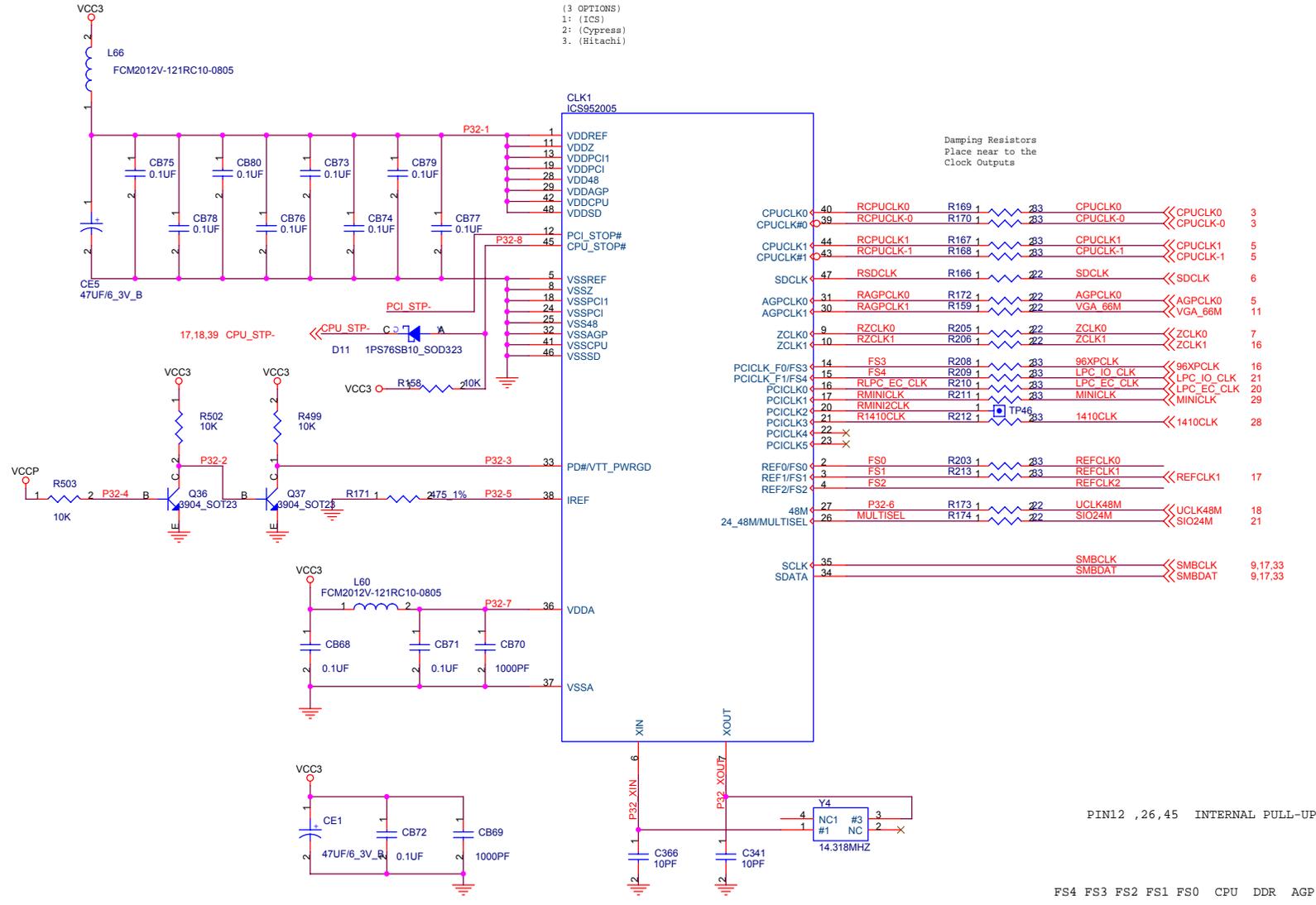
ECS CORP. (G736 M/B)		
Title	LAN & RJ45	
Size	Document Number	Rev
Custom	G736-1-4-01	6.0
Date:	Thursday, February 19, 2004	Sheet 30 of 42



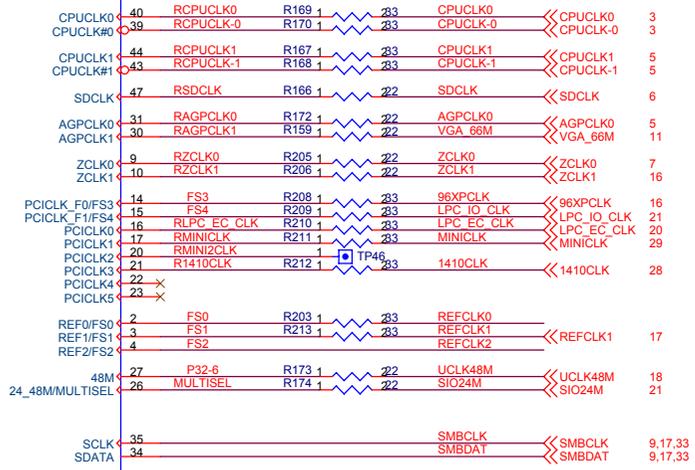
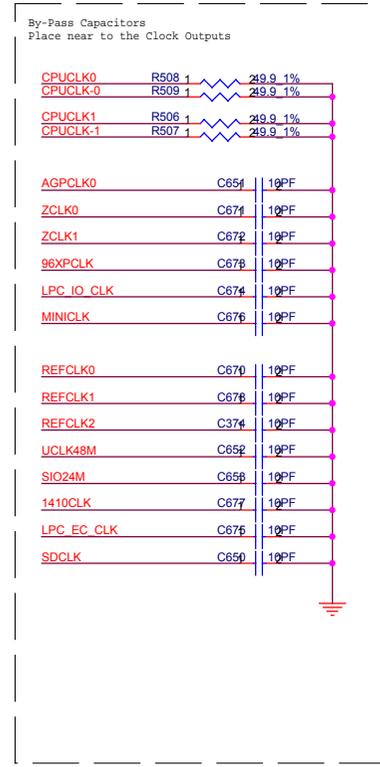
ECS CORP. (G736 M/B)		
Title IEEE 1394		
Size Custom	Document Number G736-1-4-01	Rev 6.0
Date: Thursday, February 19, 2004	Sheet 31	of 42

Main Clock Generator

(3 OPTIONS)
 1: (ICS)
 2: (Cypress)
 3: (Hitachi)

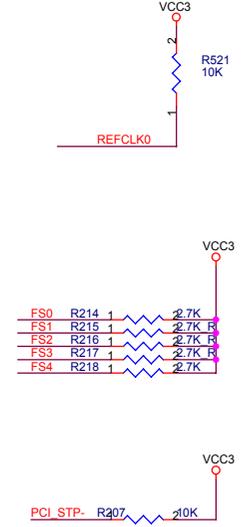
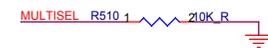


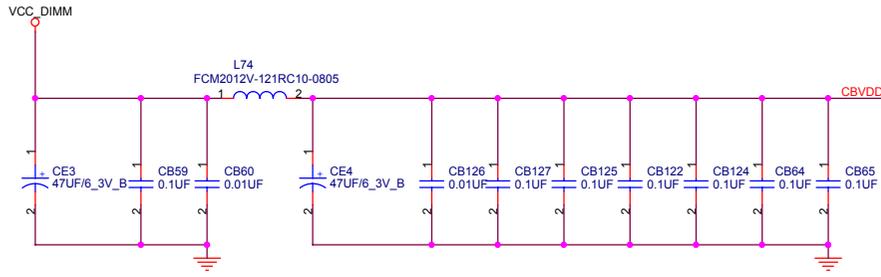
Damping Resistors
 Place near to the
 Clock Outputs



PIN12 ,26,45 INTERNAL PULL-UP

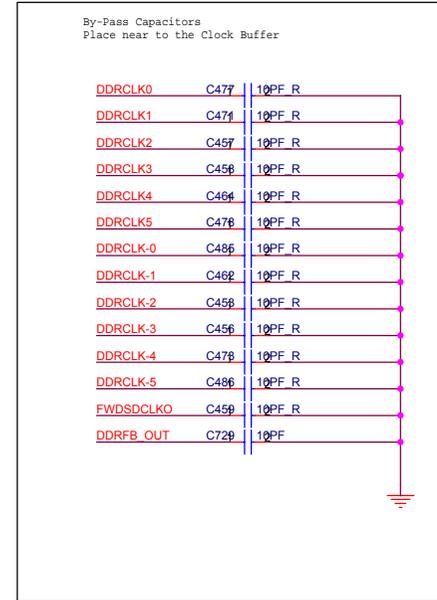
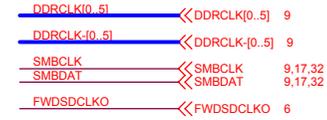
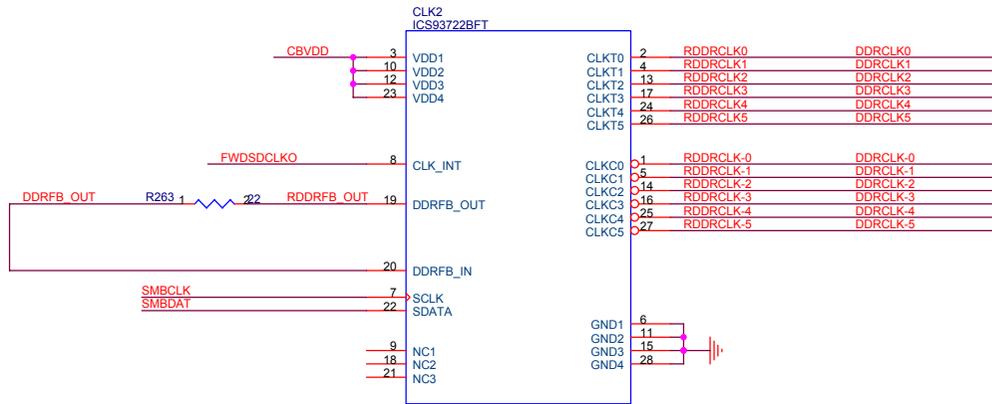
	FS4	FS3	FS2	FS1	FS0	CPU	DDR	AGP	PCI	ZCLK
1	0	0	0	0	1	100	133	66	33	133
1	0	1	0	0	1	133	133	66	33	133

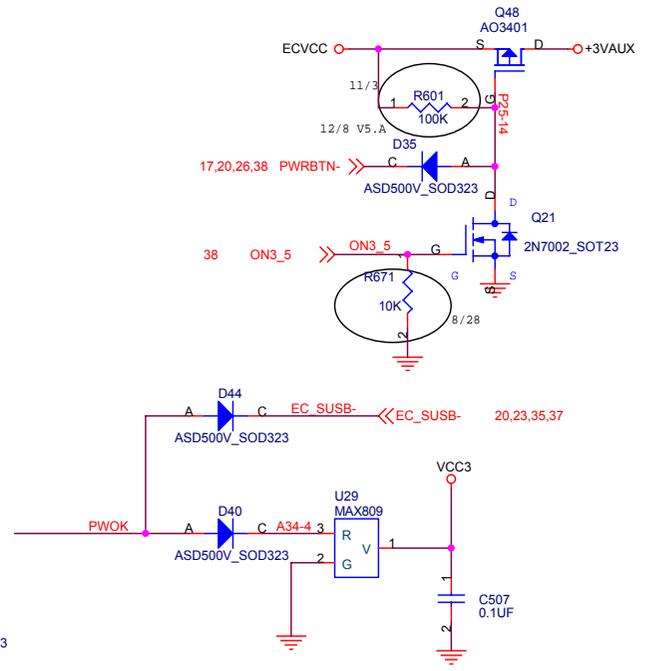
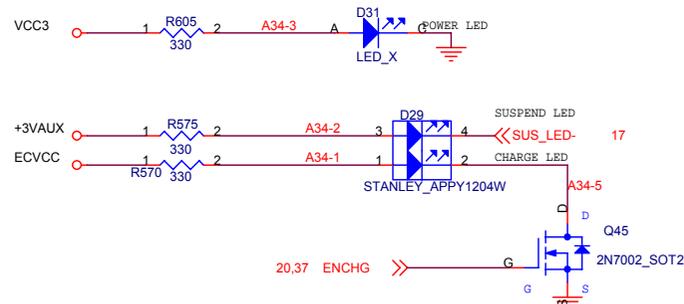
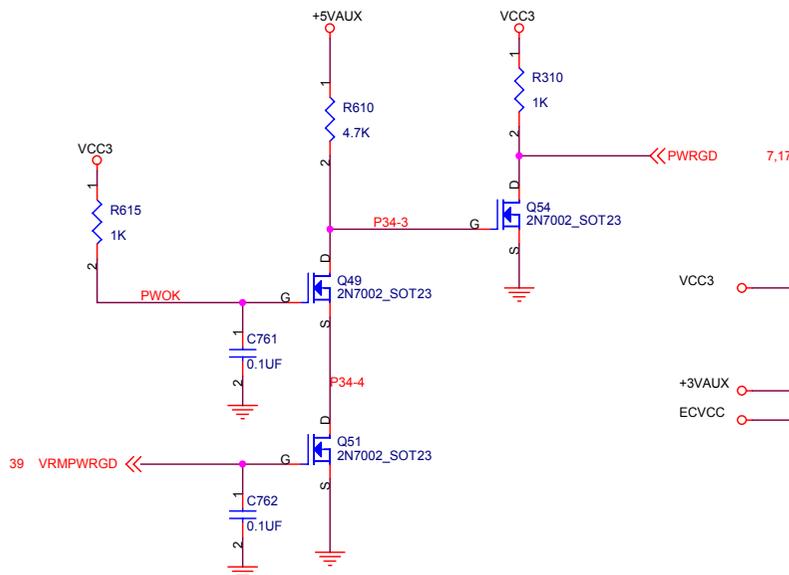
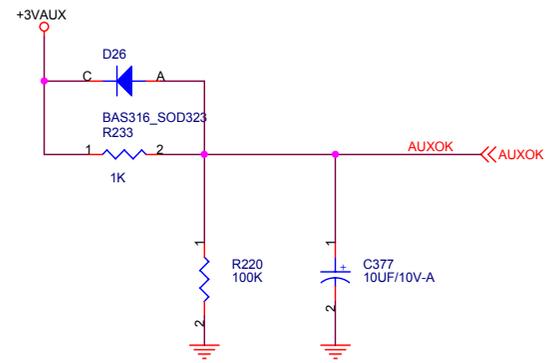
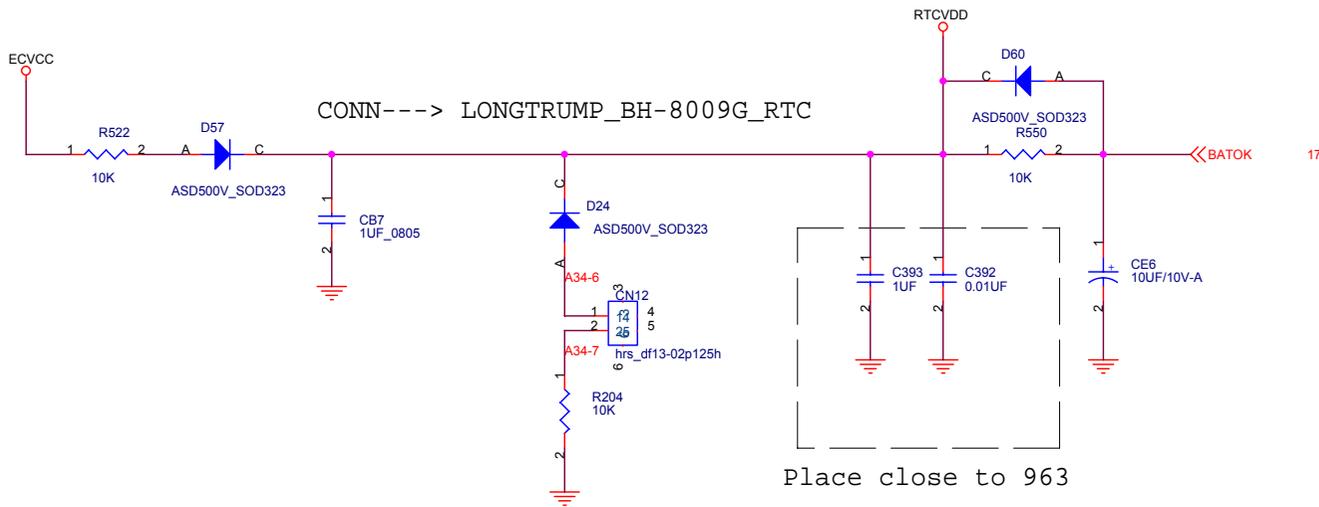




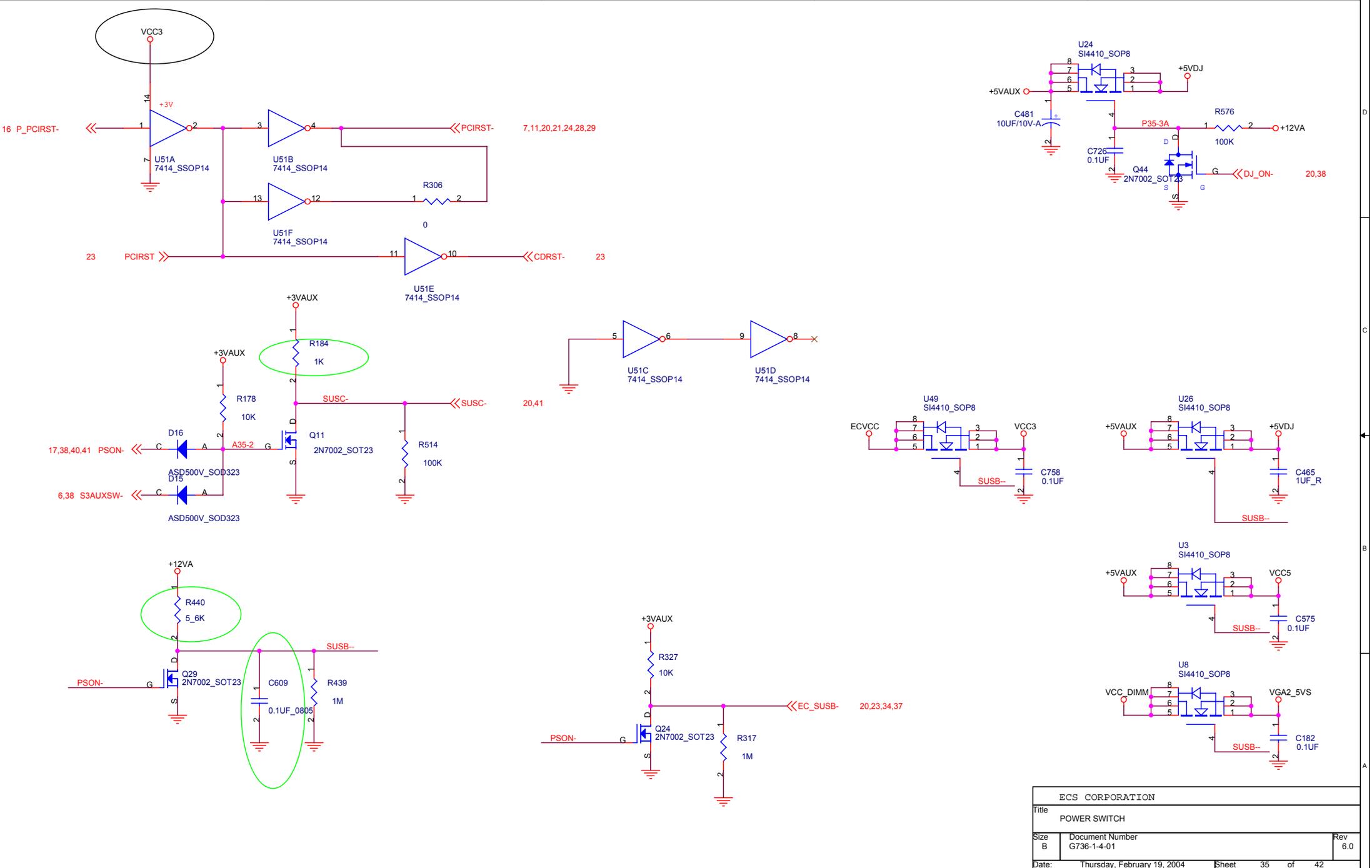
Clock Buffer (DDR)

(OPTIONS)
1: (ICS-93705)

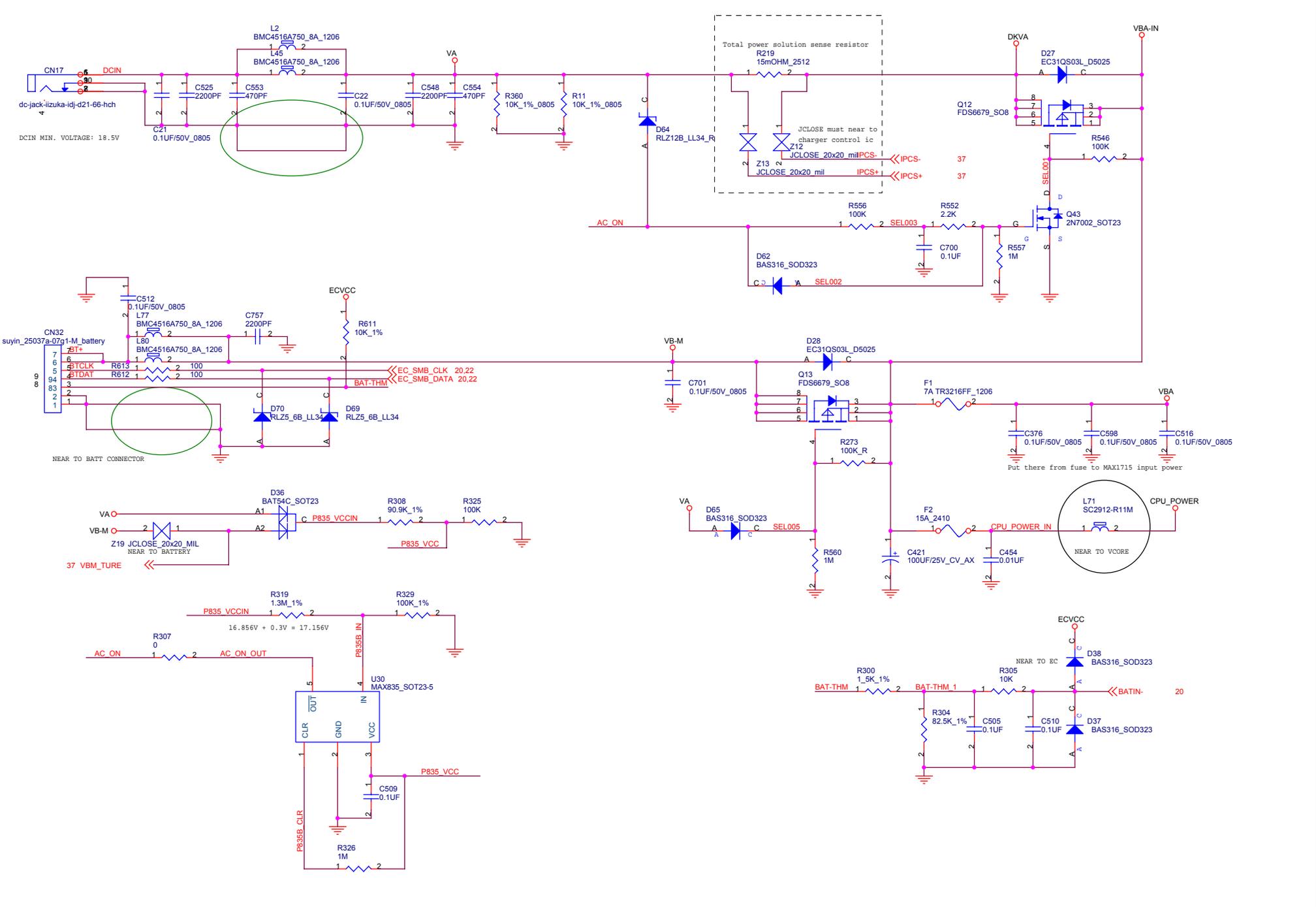




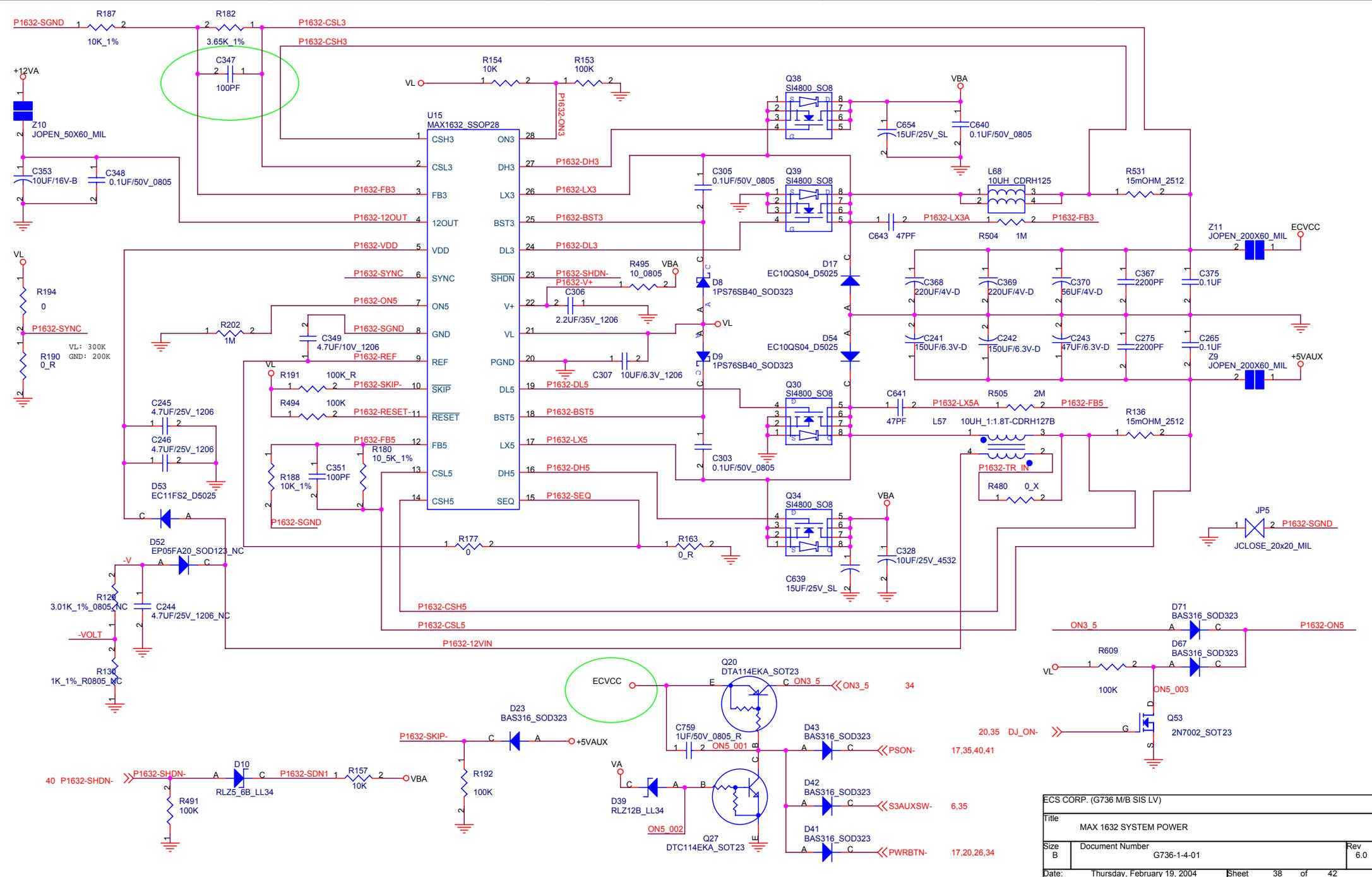
ECS CORP. (G736M/B)		
Title RTC & POWER SWITCH		
Size B	Document Number G736-1-4-01	Rev 6.0
Date: Thursday, February 19, 2004	Sheet 34	of 42



ECS CORPORATION		
Title POWER SWITCH		
Size B	Document Number G736-1-4-01	Rev 6.0
Date: Thursday, February 19, 2004	Sheet 35	of 42

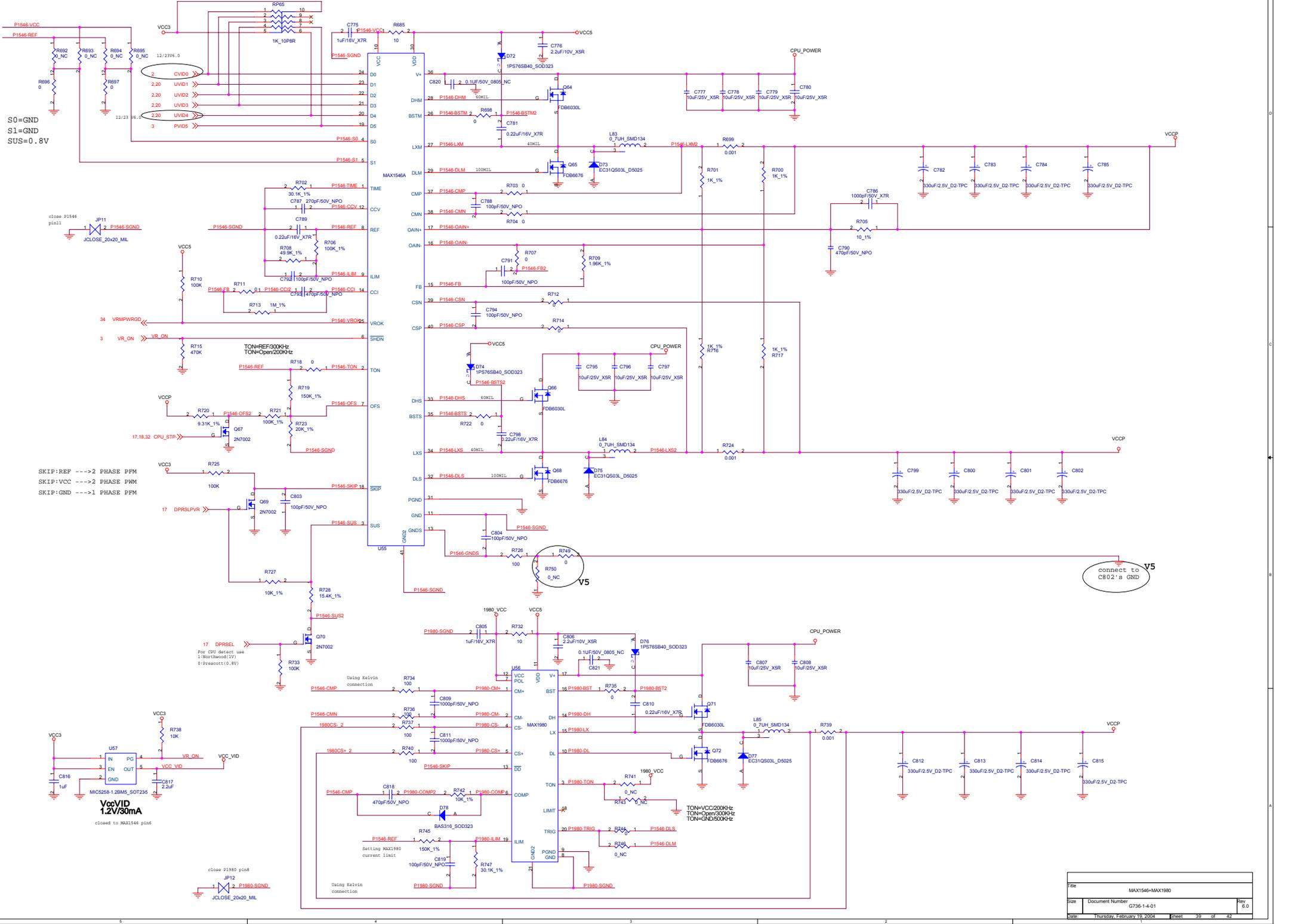


ECS CORP. (G736 M/B SIS LV)		
Title SELECTOR		
Size Custom	Document Number G736-1-4-01	Rev 6.0
Date Thursday, February 19, 2004	Sheet 36	of 42



ECS CORP. (G736 M/B SIS LV)		
Title MAX 1632 SYSTEM POWER		
Size B	Document Number G736-1-4-01	Rev 6.0
Date: Thursday, February 19, 2004	Sheet 38	of 42

MP5V/3VAUX/±12VA SUPPLY



S0=GND
S1=GND
SUS=0.8V

close P1546
pin11
JCLOSE_20x20_ML

SKIP: REF ---> 2 PHASE PFM
SKIP: VCC ---> 2 PHASE PFM
SKIP: GND ---> 1 PHASE PFM

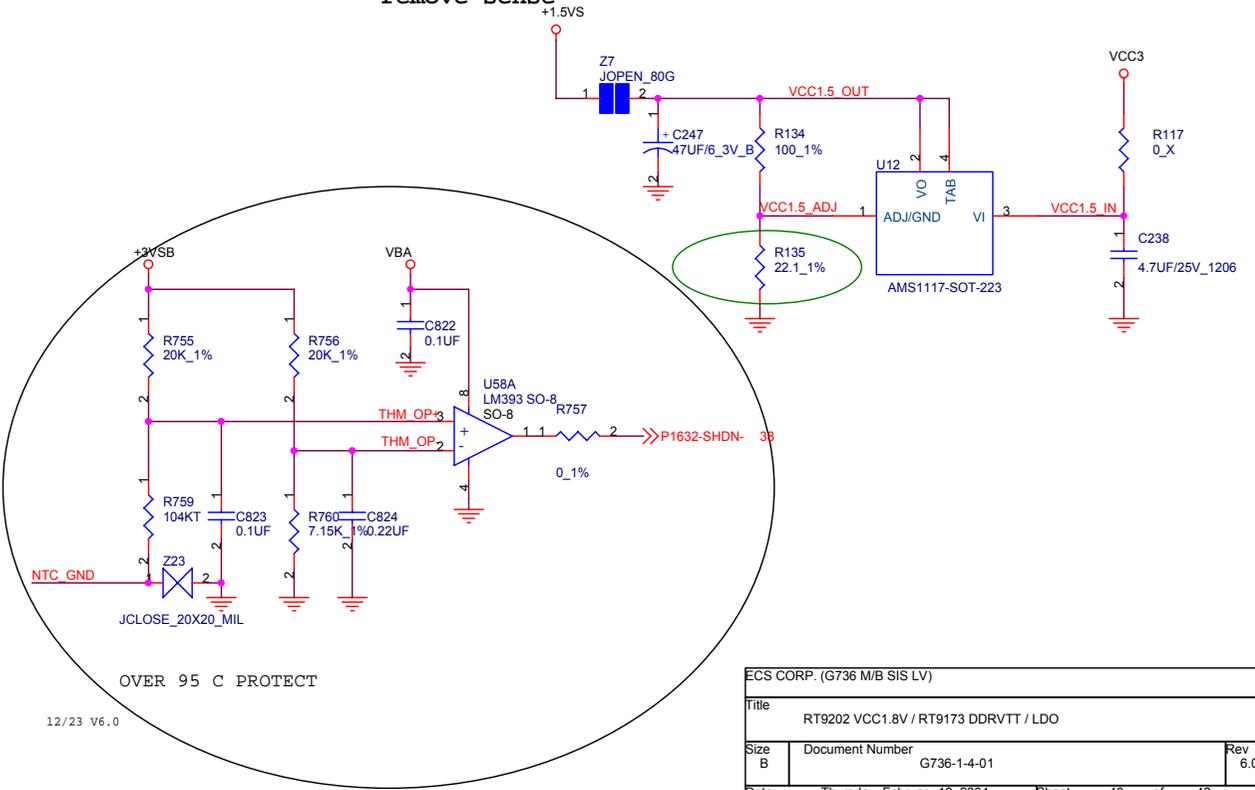
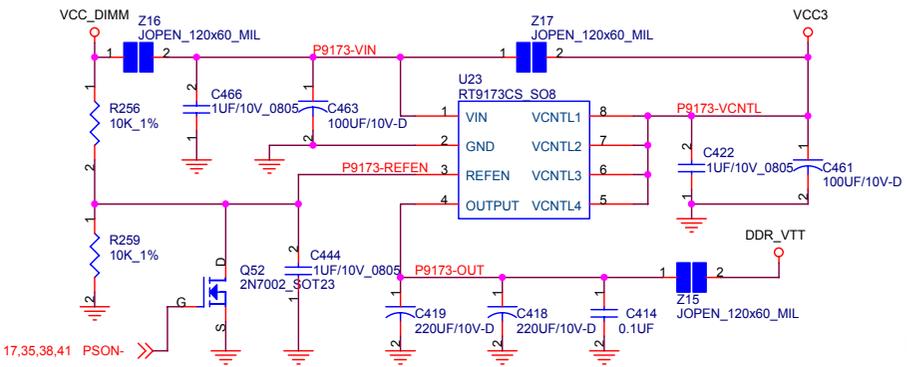
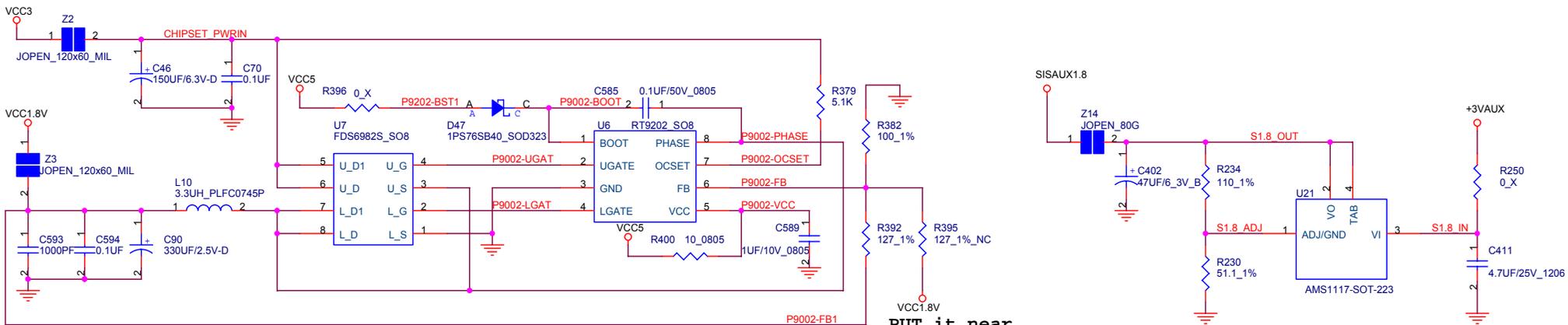
For CPU detect use
1: 3.3v detect (V)
0: Preassert (0.8V)

**VccVID
1.2V/30mA**

closed to MAX1546 pin6

close P1980 pin8
JP12
JCLOSE_20x20_ML

File	MAX1548-MAX1980		
Size	Document Number	G736-1-4-01	Rev 6.0
Date:	Thursday, February 19, 2004	Sheet	39 of 42



ECS CORP. (G736 M/B SIS LV)		
Title	RT9202 VCC1.8V / RT9173 DDRVTT / LDO	
Size	Document Number	Rev
B	G736-1-4-01	6.0
Date:	Thursday, February 19, 2004	Sheet 40 of 42

HISTORY:

- 1.0 : INITIAL
- 2.A : To avoid signal "ON3_5" float
- 2.B : FOR G736 DEBUG
- 2.C : AUDIO NOISE BUG FIXED
- 2.D : FOR AUDIO VOLUME TOO SMALL
- 3.0 : INITIAL
- 4.0 : INITIAL
- 4.A: WIRELESS LAN AND ADAPTER INSERT
- 4.B: FOR 1394/USB EMI SOLUTION
- 4.C: EMI SOLUTION
- 5.0: INITIAL(DYNAMIC VID OF DT CPU/DDR VOLTAGE TO 2.65V)
- 5.A:FOR G736 EMI,BUG MODIFY AND ADD SUBSTITUTE
- 5.B:FOR G736 M11 , PULL UP OCP AND VOLTAGE
- 6.0 :FOR G736 M11 , DYNAMIC VID MODIFY
- 6.A :supporting Intel Prescott C-step CPU
- 6.B :FOR G736 V6.0 3DMark2001 FAIL

ECS CORP. (G736M/B)			
Title		HISTORY	
Size	Document Number		Rev
B	G736-1-4-01		6.B
Date:	Thursday, February 19, 2004	Sheet	42 of 42