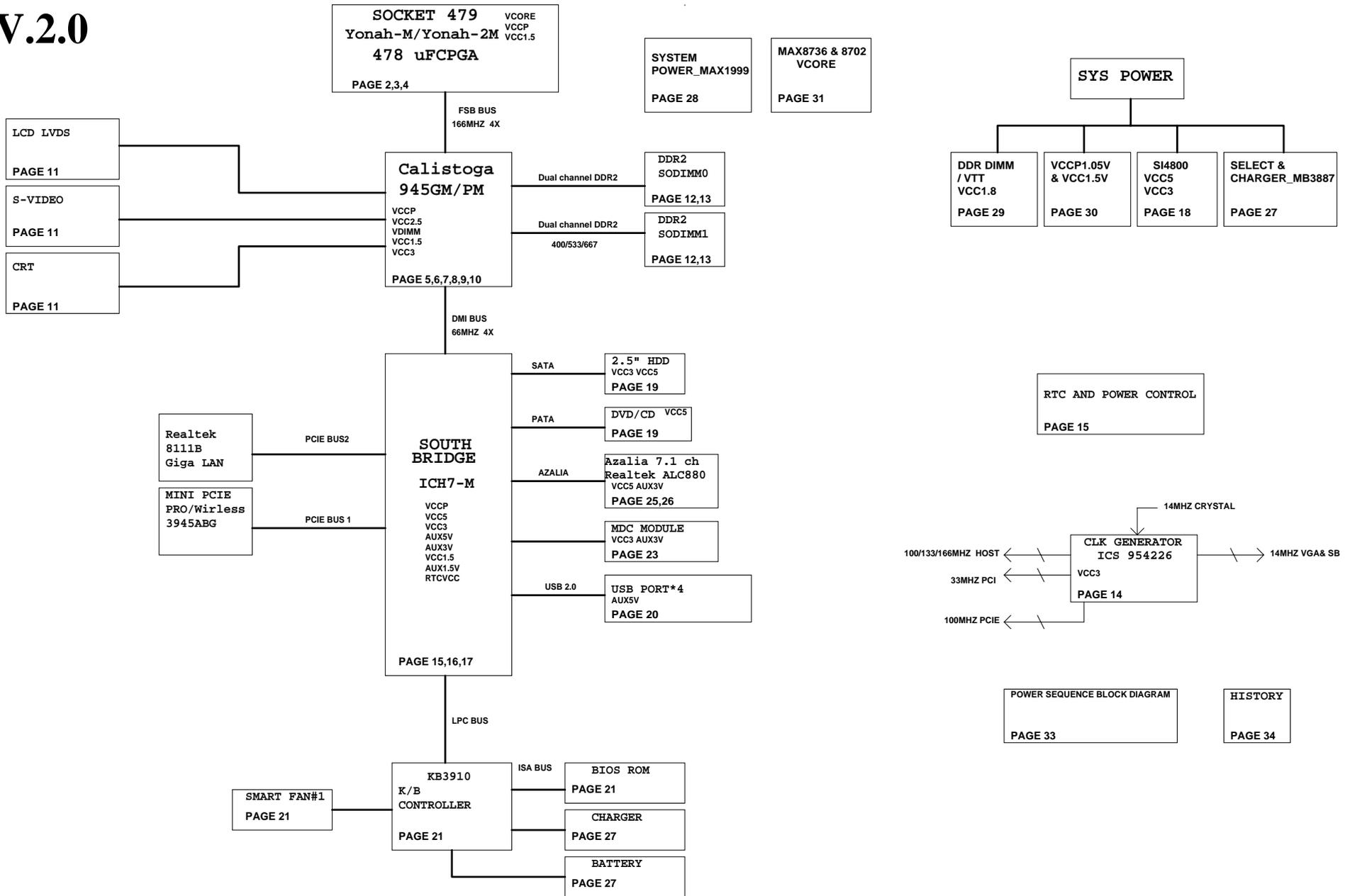


G335 V.2.0

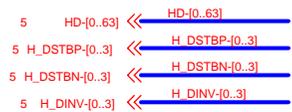
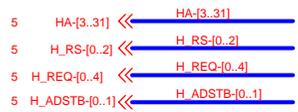


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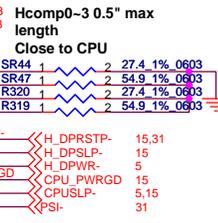
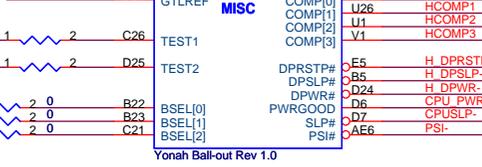
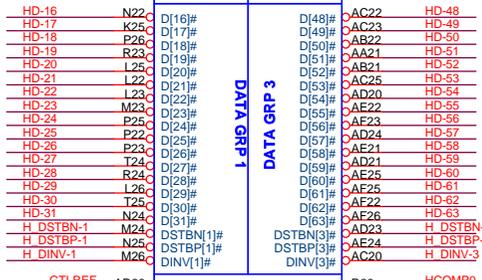
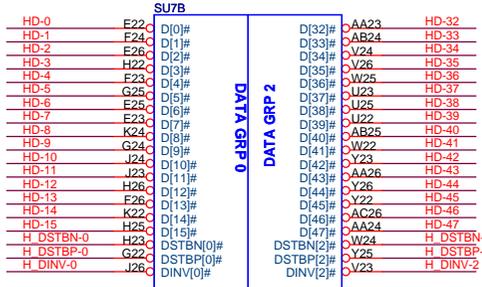
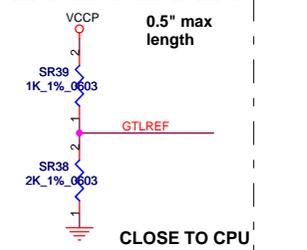
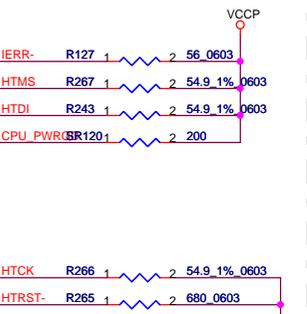
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DATE	2006/01/23	2006/01/23	2006/01/23	2006/01/23	2006/01/23	2006/01/23	2006/01/23	2006/01/23	2006/01/23	2006/01/23	2006/01/23	2006/01/23	2006/01/23	2006/01/23	2006/01/23	2006/01/23	2006/01/23	2006/01/23	2006/01/23	2006/01/23

PAGE	21	22	23	24	25	26	27	28	29	30	31	32	33	34
REV	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0	2.0
DATE	2006/01/23	2006/01/23	2006/01/23	2006/01/23	2006/01/23	2006/01/23	2006/01/23	2006/01/23	2006/01/23	2006/01/23	2006/01/23	2006/01/23	2006/01/23	2006/01/23

Approved by	Checked by	Designed by
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Size A2 G335-1-4-01	Document Number G335-1-4-01	Rev 2.0
Date: Monday, January 23, 2006 Sheet 1 of 34		

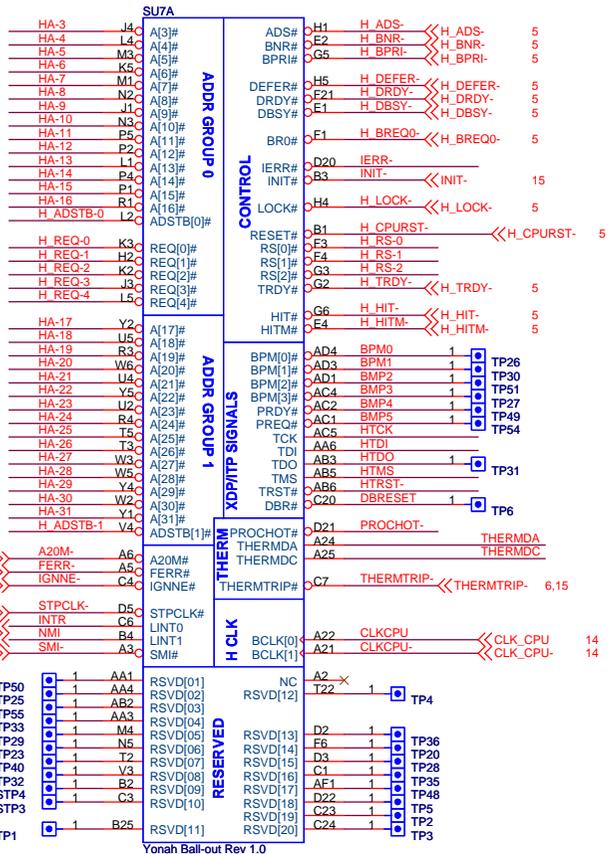


Place testpoint on IERR- with GND 0.1" away



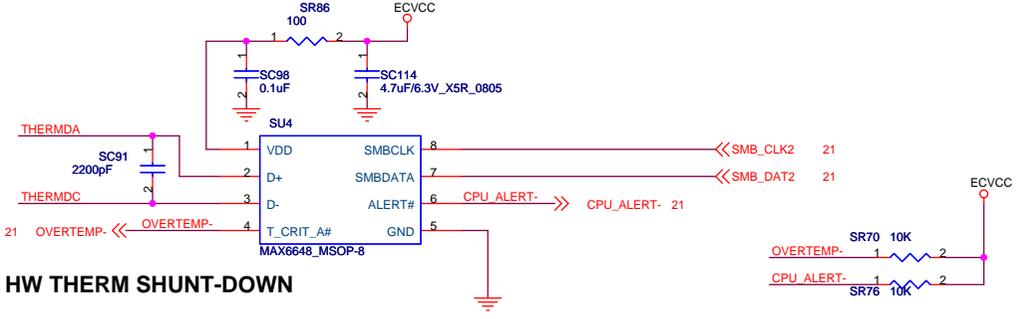
SR41 51 ohm: Intel has determined that Test2 pin needs to be populated with a 51 ohm +/-5% resistor in order for Yonah B-0 silicon to boot due to issue in the reset sequence needed for the processor.

CHECK

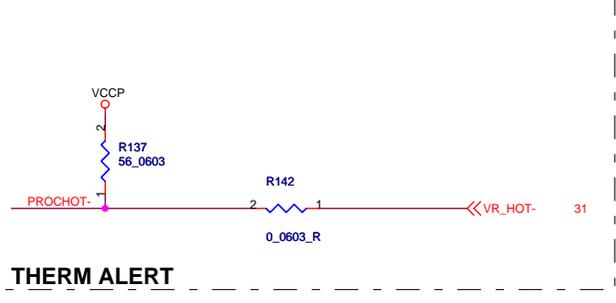


Yonah Ball-out Rev 1.0

Remote and Local Thermal Sensor



HW THERM SHUNT-DOWN



THERM ALERT

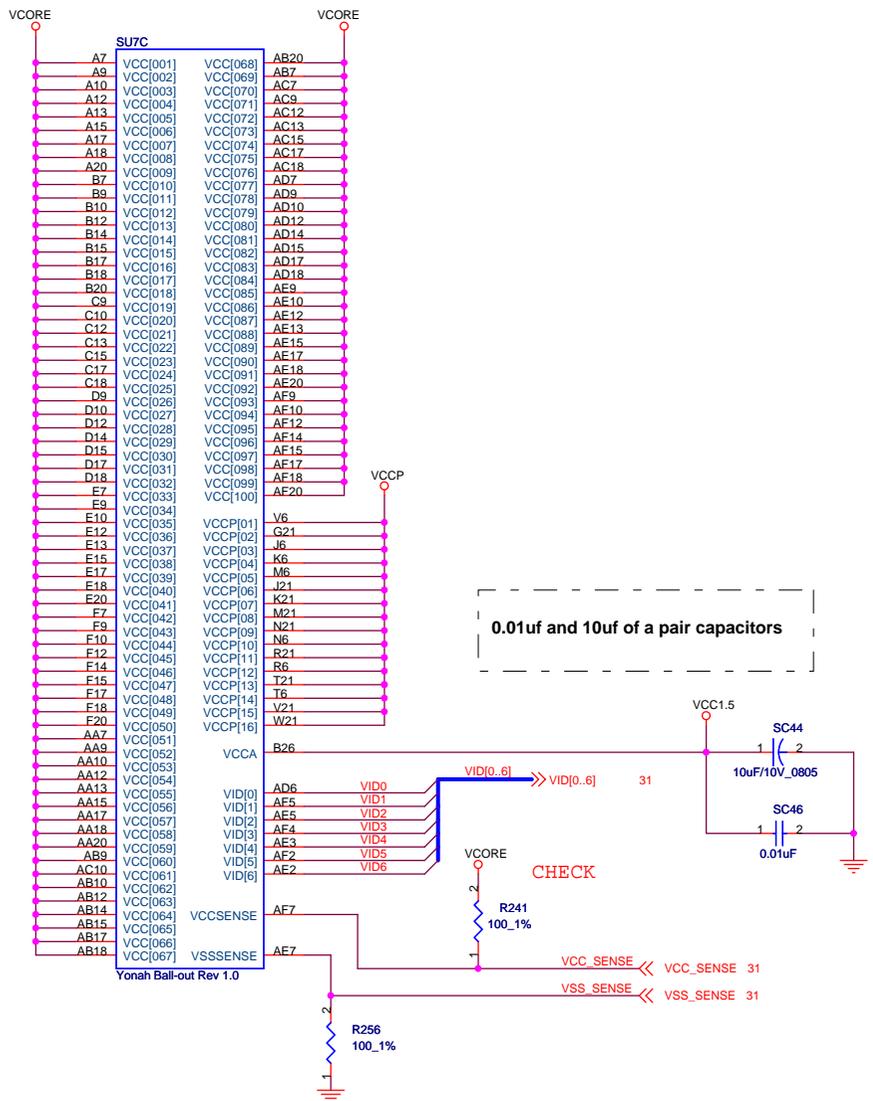
BSEL[0]	BSEL[1]	BSEL[2]	BCLK frequency
L	L	L	RESERVED
H	L	L	133MHZ
L	H	L	RESERVED
H	H	L	166MHZ

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Title: **Yonah-1**

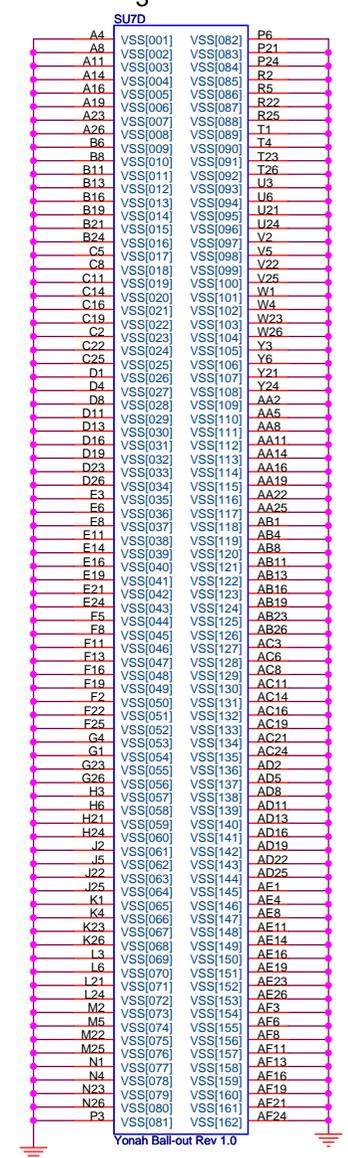
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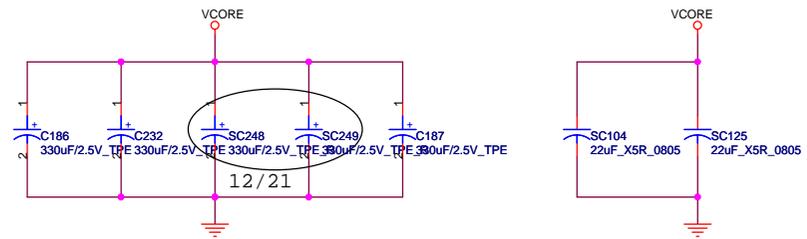
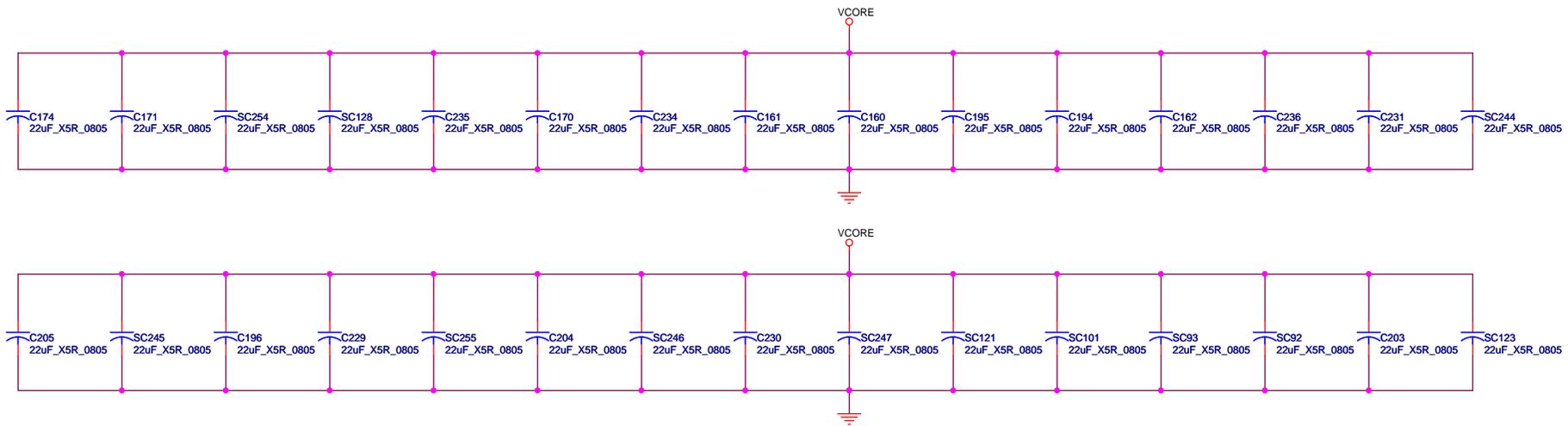
Date: Monday, January 23, 2006 Sheet 2 of 34



0.01uF and 10uF of a pair capacitors

Layout Note:
Route VCC_SENSE and VSS_SENSE trace at 27.4 ohm with 50 mil spacing.
Place PU and PD within 1 inch of CPU.



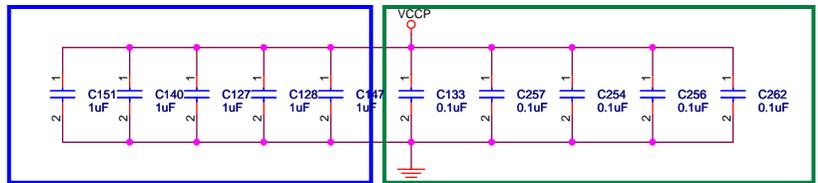


VCORE Bypass: Close to CPU Socket

22uF 32 PCs

ADD 330uF x 5 (Total * 8)

VCCP Bypass: Close to CPU Socket

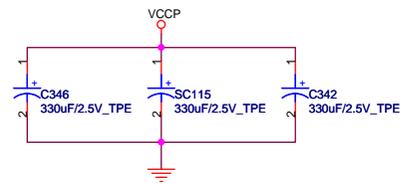


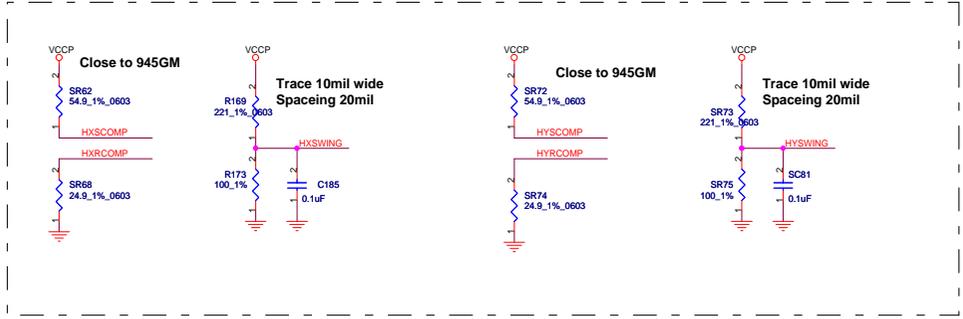
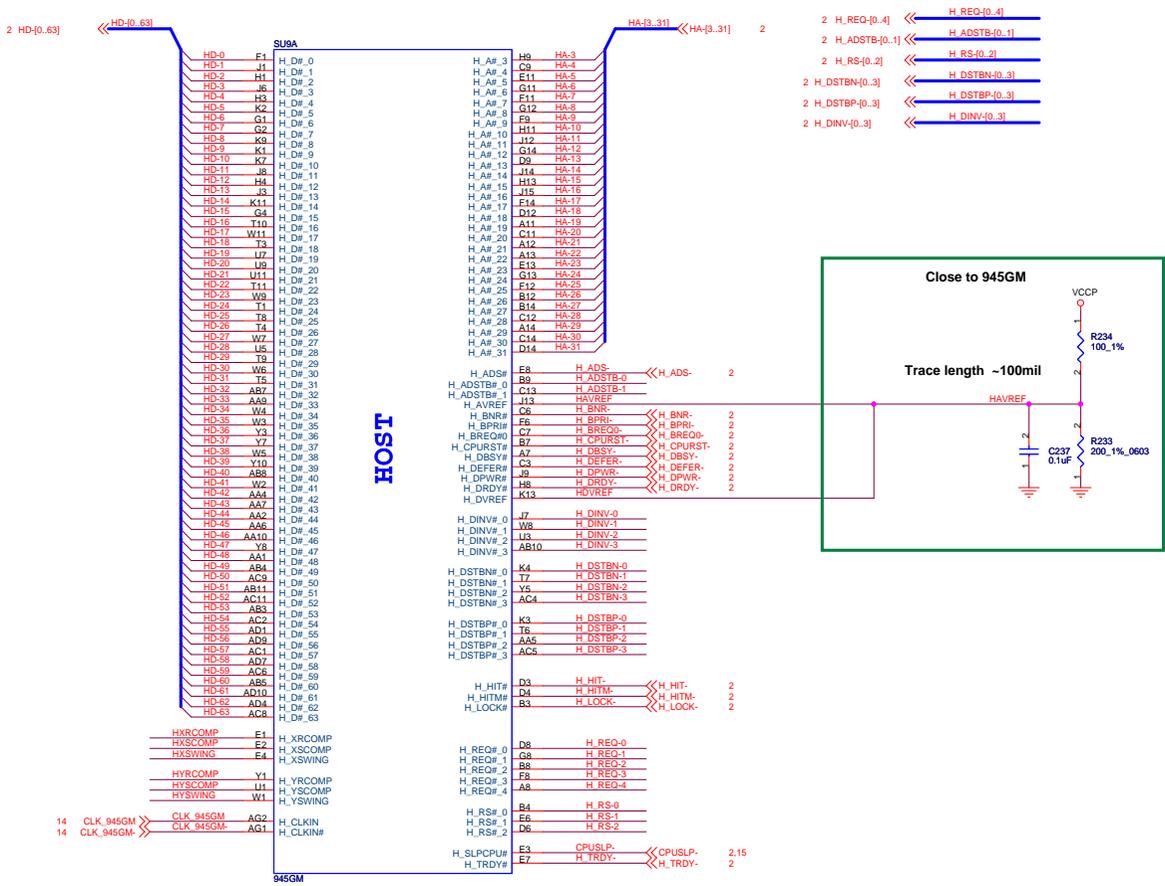
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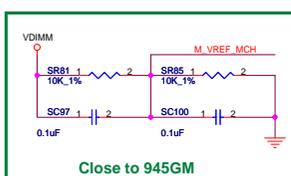
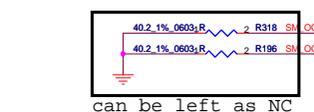
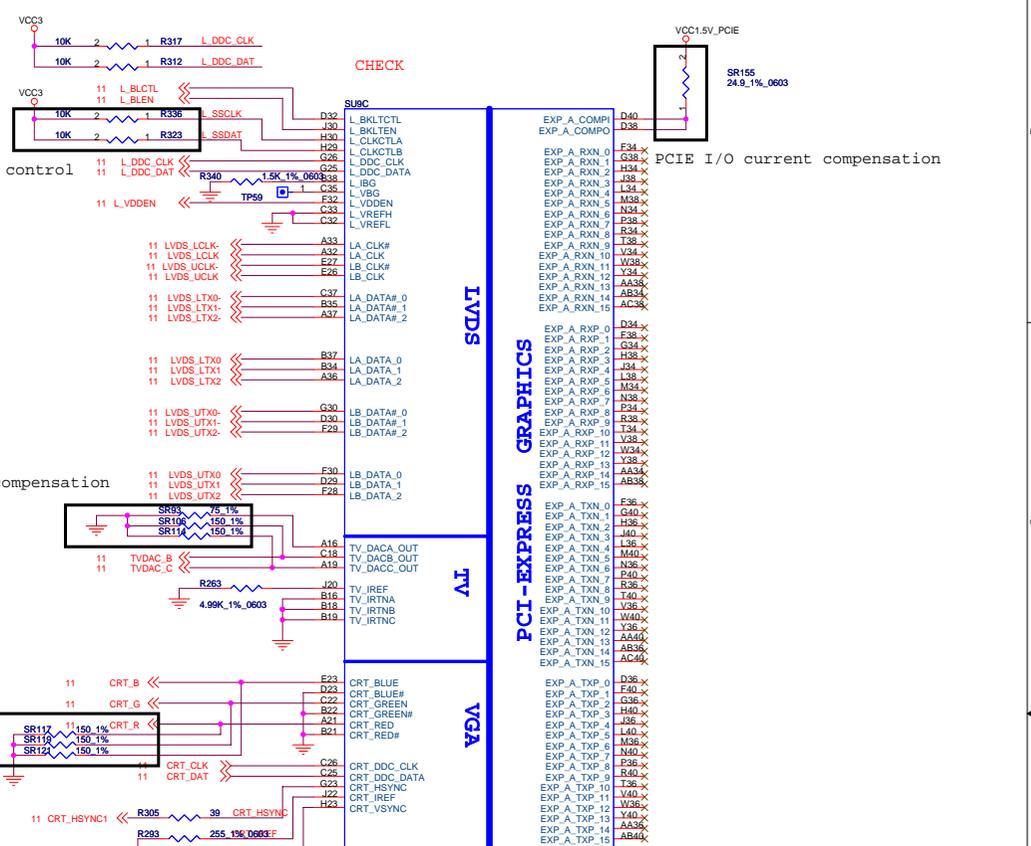
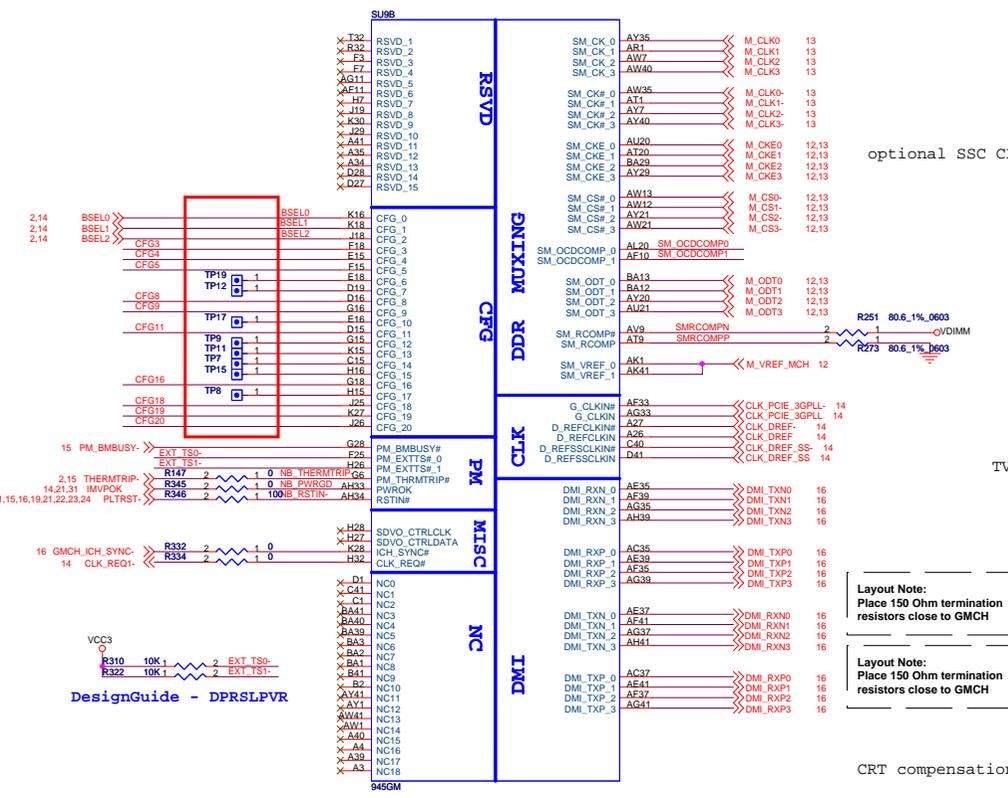
INTEL DEMO

ADD 330uF x 1 (CPU side)

0.1uF 5 PCs
1uF 5 PCs
270uF 1 PCs

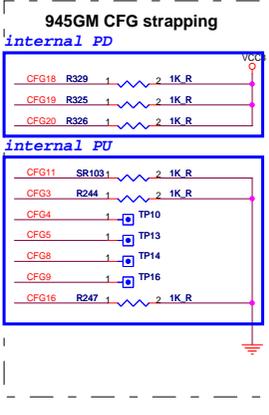




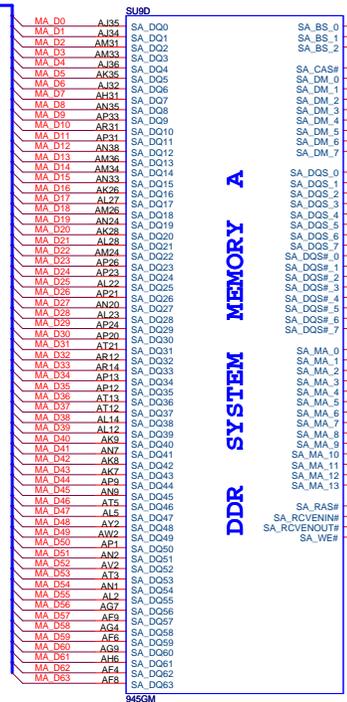


CFG[3:17] have internal pull-ups
CFG[18:20] have internal pull-downs

CFG[2:0] 001= FSB 533 MHZ 011= FSB 667 MHZ	CFG9(PCIE Graphics Lane) LOW=Reserved Lane HIGH=Normal Operation (default)	CFG17(Global Rcomp Disable) RESERVED
CFG[4:3] RESERVED	CFG10 (HOST PLL VCC SELET) RESERVED	CFG18 (VCC SELECT) LOW=1.05V (default) HIGH=1.5V
CFG5 LOW=DMIx2 HIGH=DMIx4 (default)	CFG11 (PSB 4X CLK ENABLE) LOW= 4X ENABLED HIGH=8X ENABLED	CFG19 (DMI LANE RESERVED) LOW=Normal (default) HIGH=LANES REVERSED (3->0, 2->1)
CFG6 RESERVED	CFG[13:12] 00 = Partial Clock Gating Disabled 01 = XOR Mode Enables 10 = All-Z Mode Enabled 11 = Normal Operation (default)	CFG20 (PCIe Backward Interoperability mode) 0 = only SDVO or PCIE x1 is operational (defaults) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port
CFG7 (CPU Strap) LOW=RSVD HIGH=Mobile CPU (default)	CFG[15:14] RESERVED	SDVO_CRTLDATA 0 = no SDVO Device Present (default) 1 = SDVO Device Present
CFG8 (LP PCIe) RESERVED	CFG16 (FSB Dynamic ODT) LOW=Dynamic ODT Enabled HIGH=Dynamic ODT Disabled (default)	

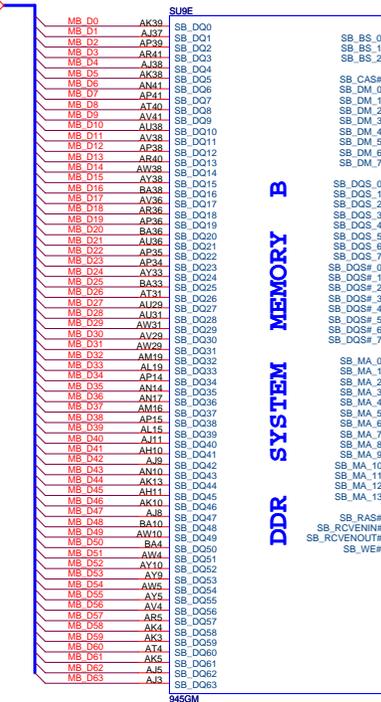


13 MA_D[0..63] >>



945GM

13 MB_D[0..63] >>



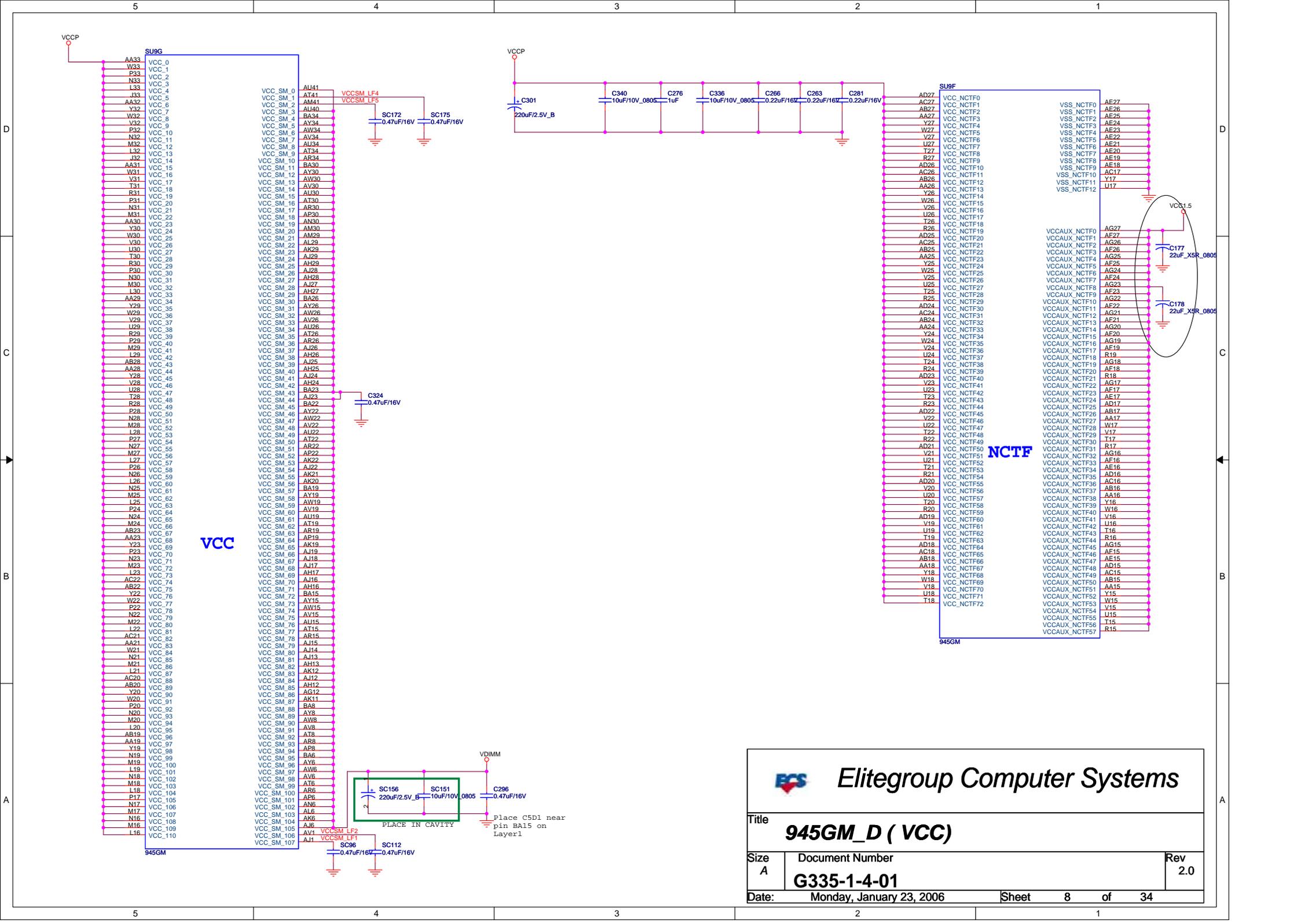
945GM

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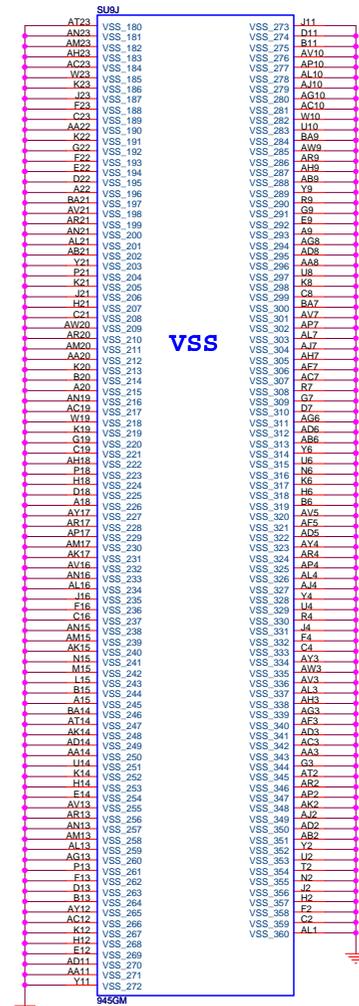
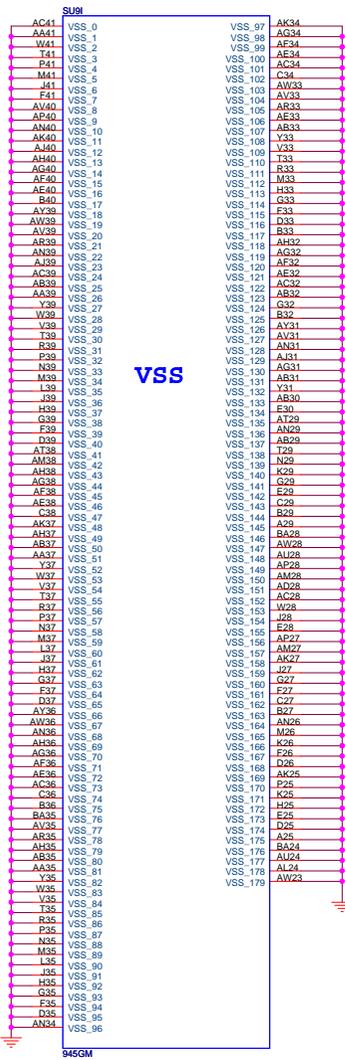
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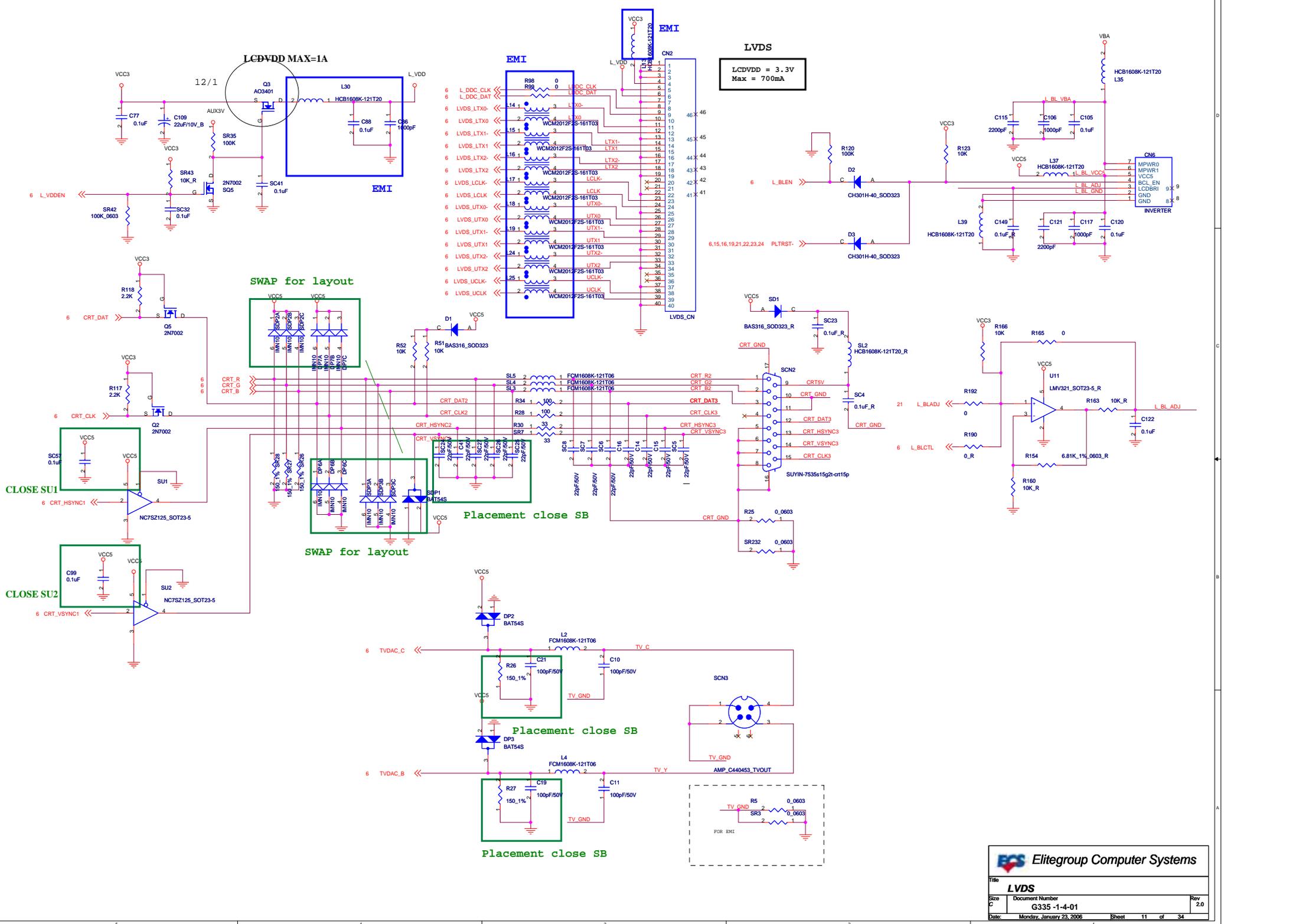
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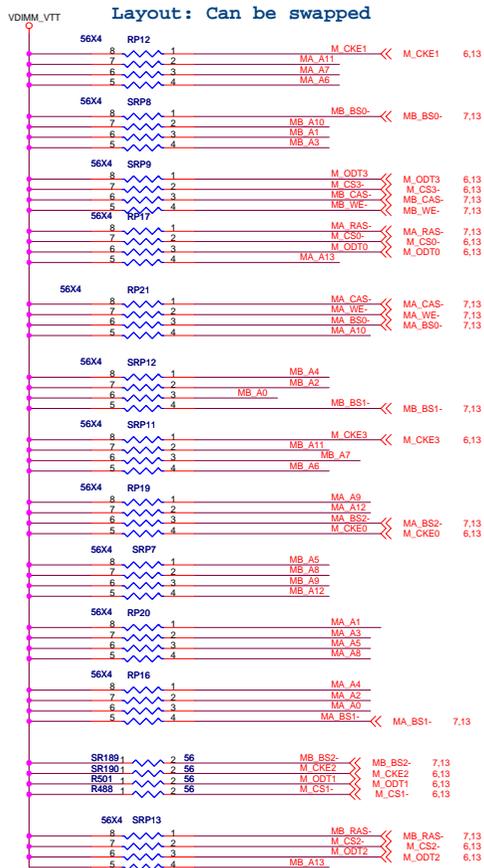
Date: Monday, January 23, 2006 Sheet: 7 of 34



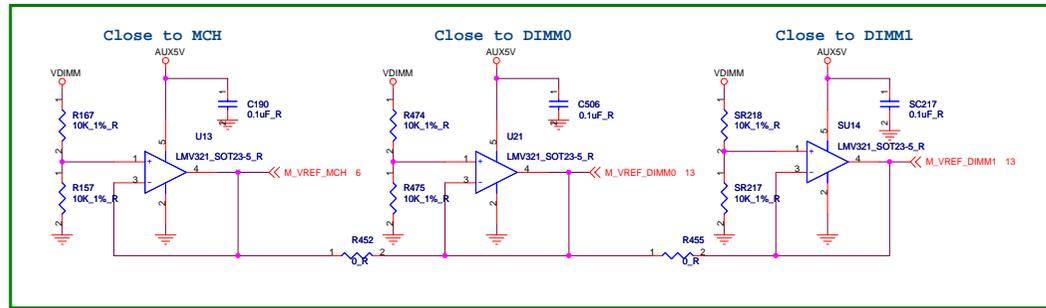
 Elitegroup Computer Systems		
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945GM_D (VCC)		
Size	Document Number	Rev
A	G335-1-4-01	2.0
Date:	Monday, January 23, 2006	Sheet 8 of 34



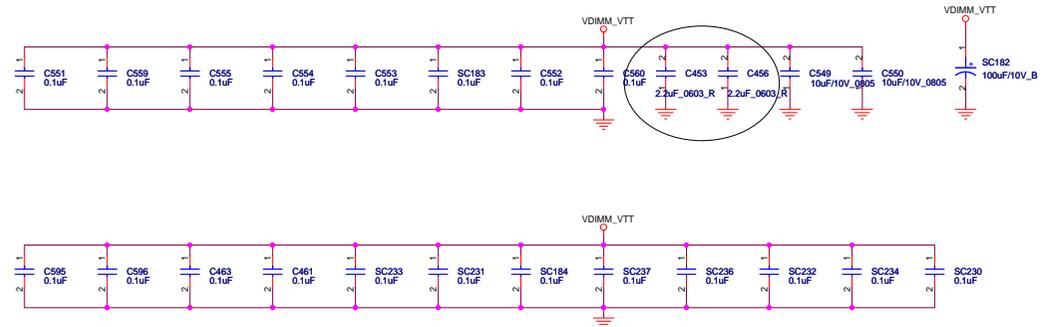


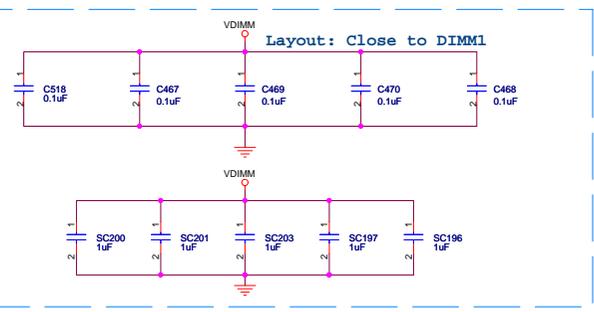
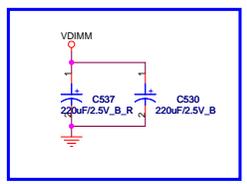
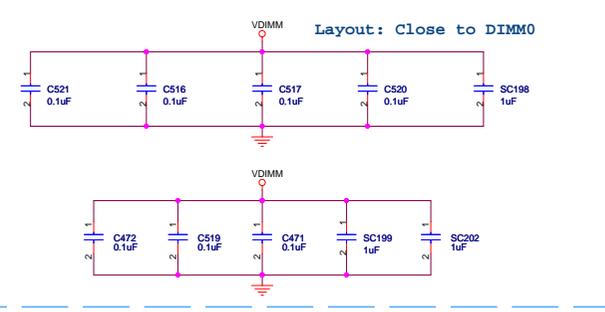
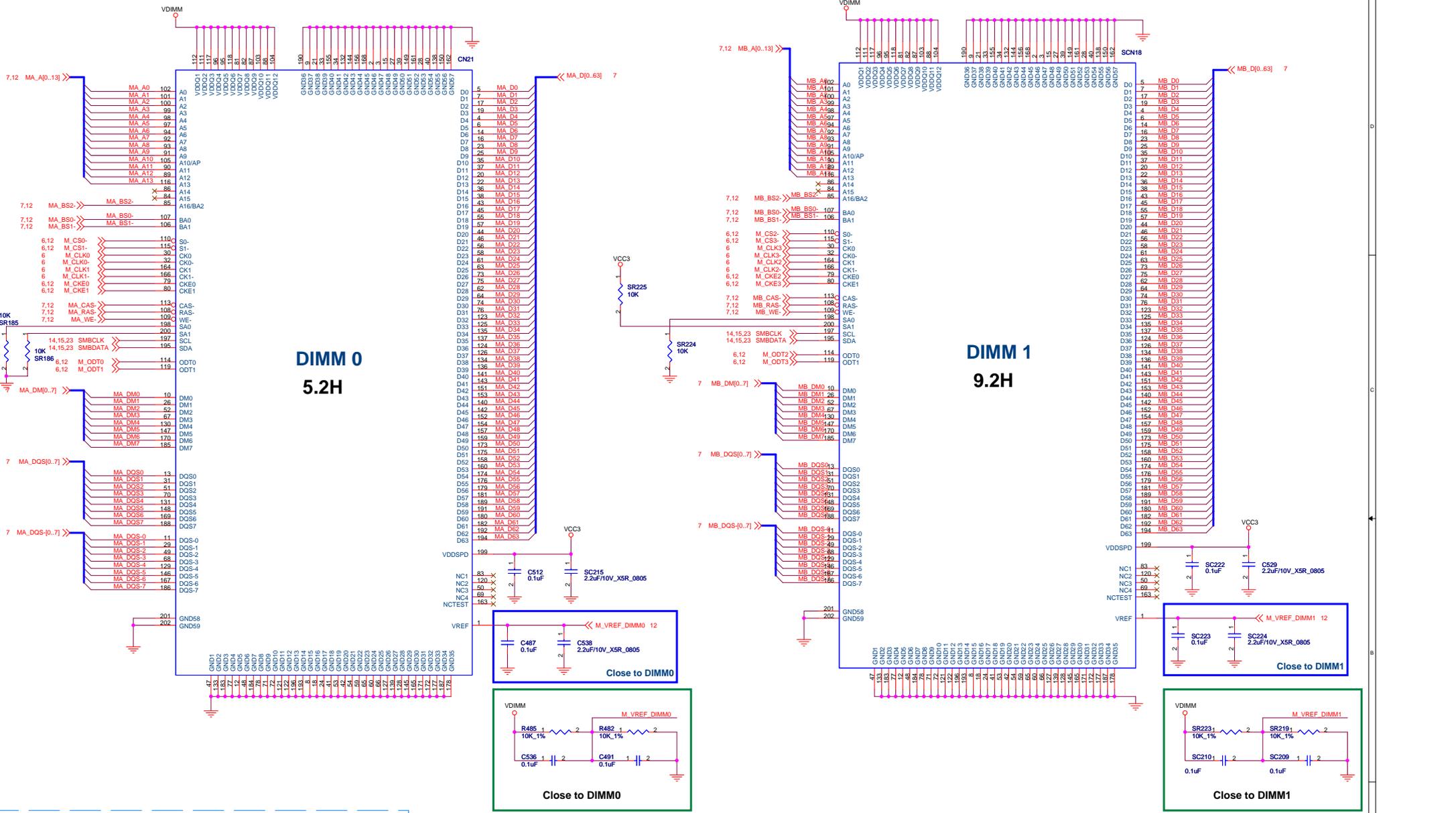


<<MA_A[0..13] 7.13
 <<MB_A[0..13] 7.13



Every 2 Resistors with 1 CAP



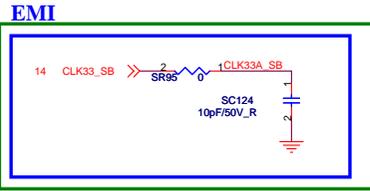
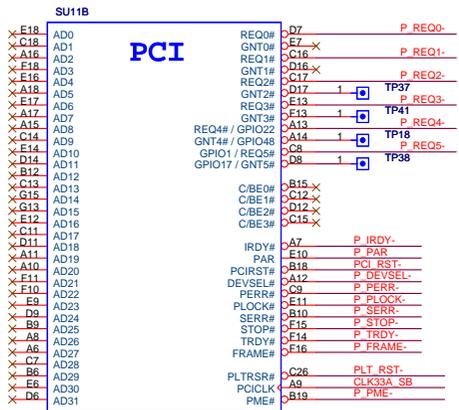


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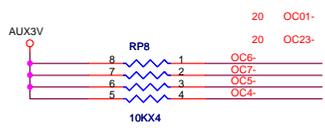
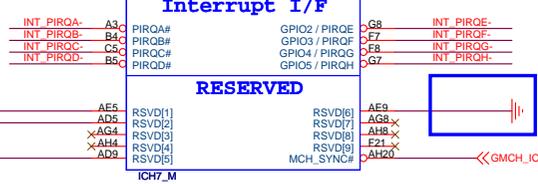
DDR2 SODIMM

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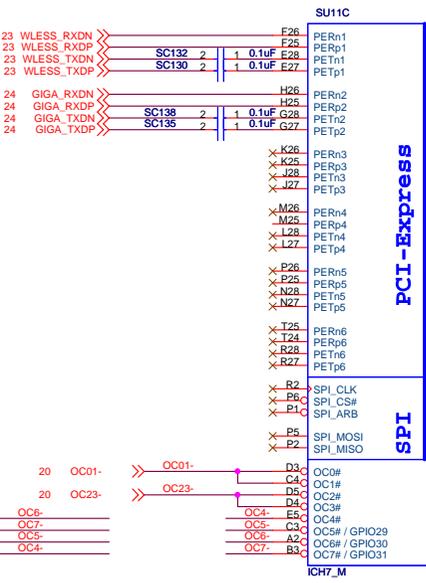
Date: Monday, January 23, 2006 Sheet 13 of 34



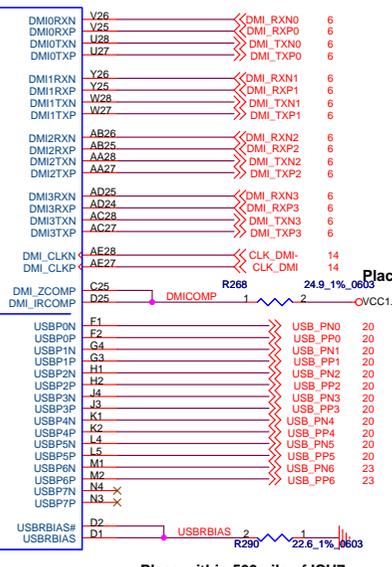
CLOSE SB



For SATA RSVD Pin



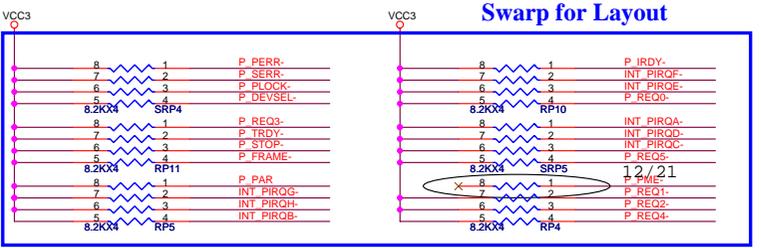
Direct Media Interface



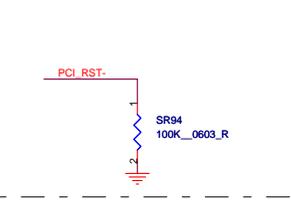
Place within 500mils of ICH7

Place within 500mils of ICH7

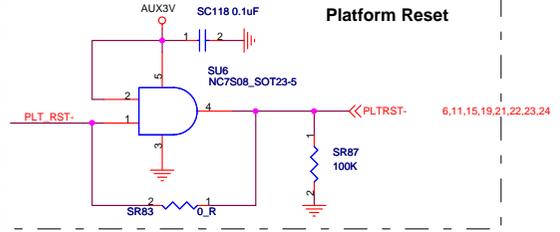
PCI INTERFACE PULL UP



PCI RESET



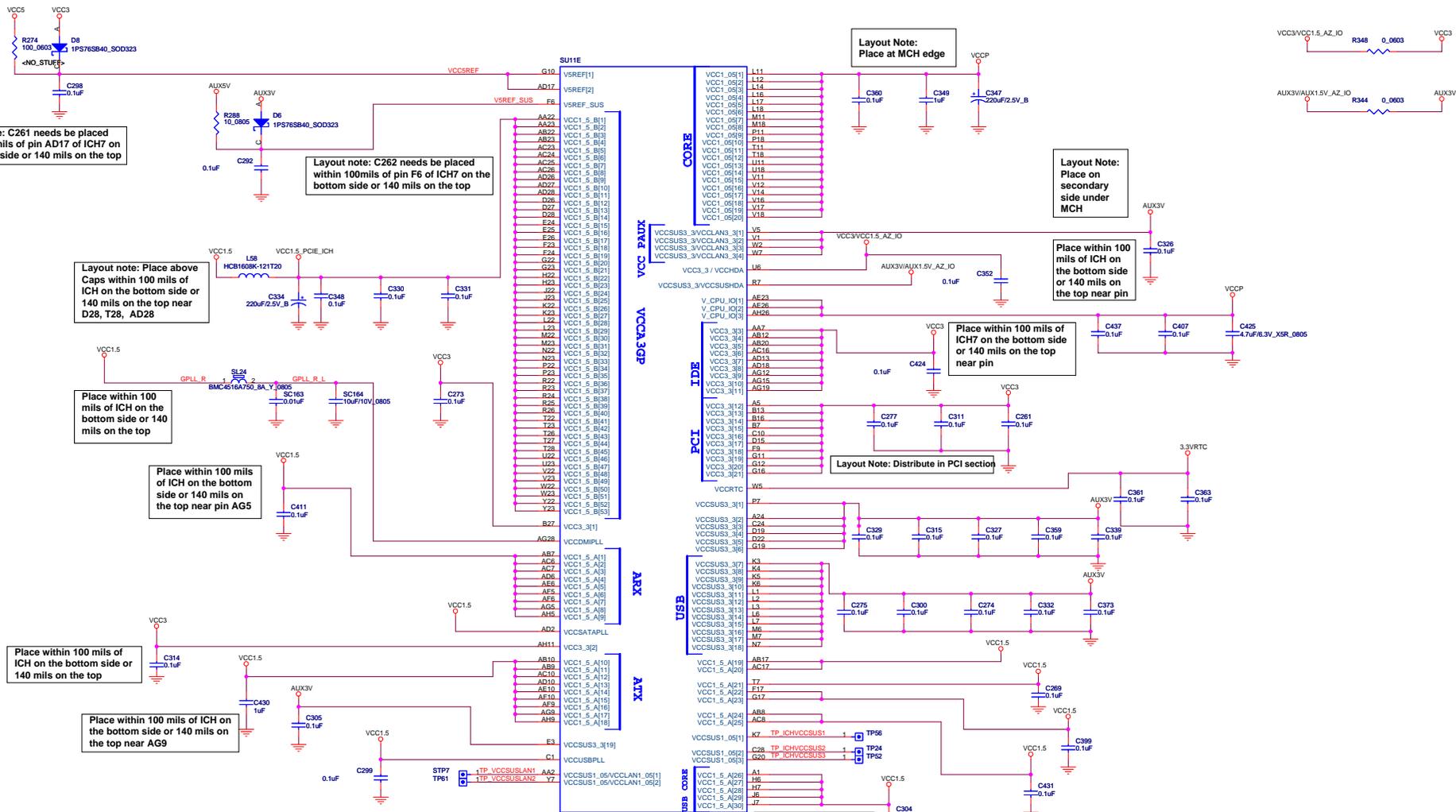
Platform Reset



Elitegroup Computer Systems

File: **ICH7-M(DMI/PCI/USB/PCIE)**

Size	Document Number	Rev
Custom	G335-1-4-01	2.0
Date:	Monday, January 23, 2006	Sheet 16 of 34



Layout note: C261 needs to be placed within 100mils of pin AD17 of ICH7 on the bottom side or 140 mils on the top

Layout note: C262 needs to be placed within 100mils of pin F6 of ICH7 on the bottom side or 140 mils on the top

Layout note: Place above Caps within 100 mils of ICH on the bottom side or 140 mils on the top near D28, T28, AD28

Place within 100 mils of ICH on the bottom side or 140 mils on the top

Place within 100 mils of ICH on the bottom side or 140 mils on the top near pin AG5

Place within 100 mils of ICH on the bottom side or 140 mils on the top

Place within 100 mils of ICH on the bottom side or 140 mils on the top near AG9

Layout Note: Place at MCH edge

Layout Note: Place on secondary side under MCH

Place within 100 mils of ICH on the bottom side or 140 mils on the top near pin

Place within 100 mils of ICH7 on the bottom side or 140 mils on the top near pin

Layout Note: Distribute in PCI section

Place within 100 mils of ICH on the bottom side or 140 mils on the top

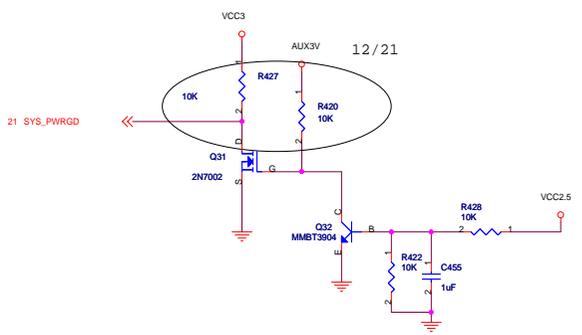
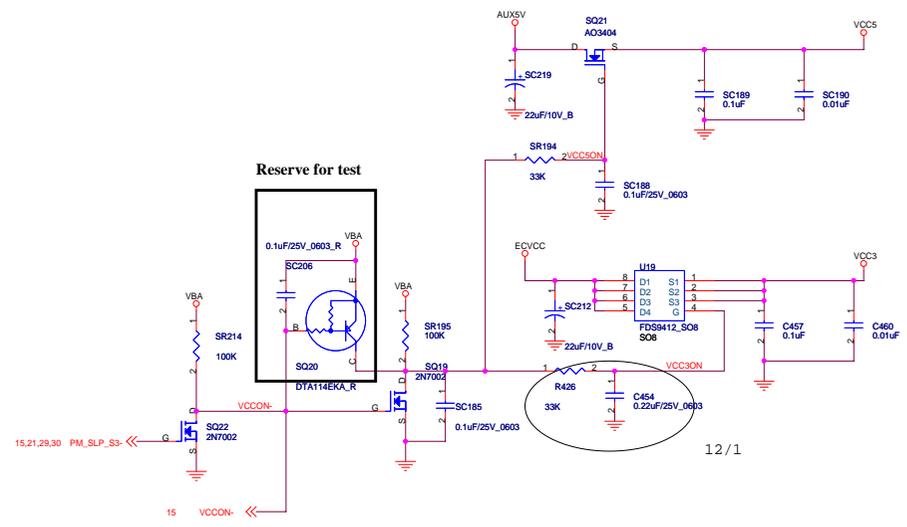
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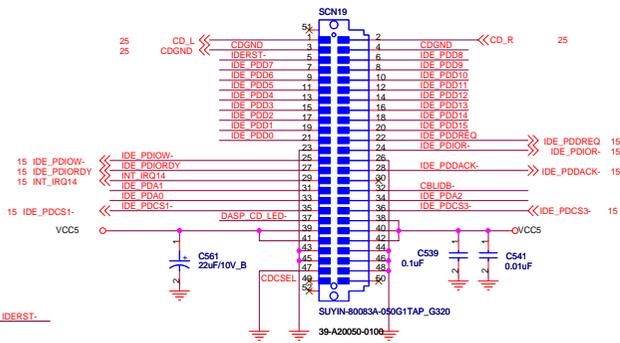
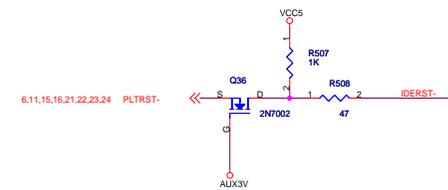
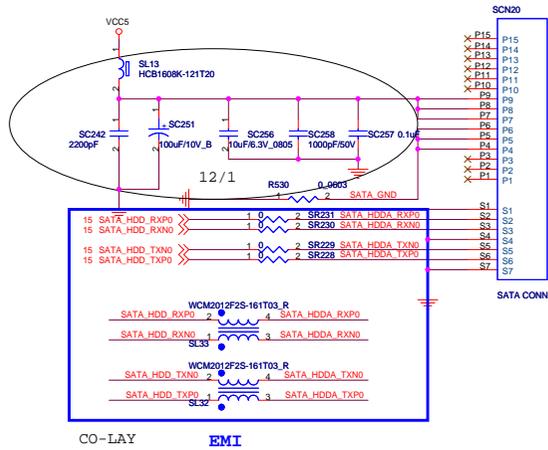
Elitegroup Computer Systems

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Size: Custom Document Number **G335-1-4-01** Rev: 2.0

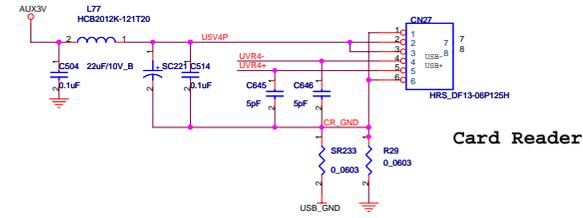
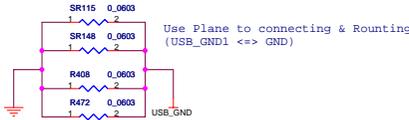
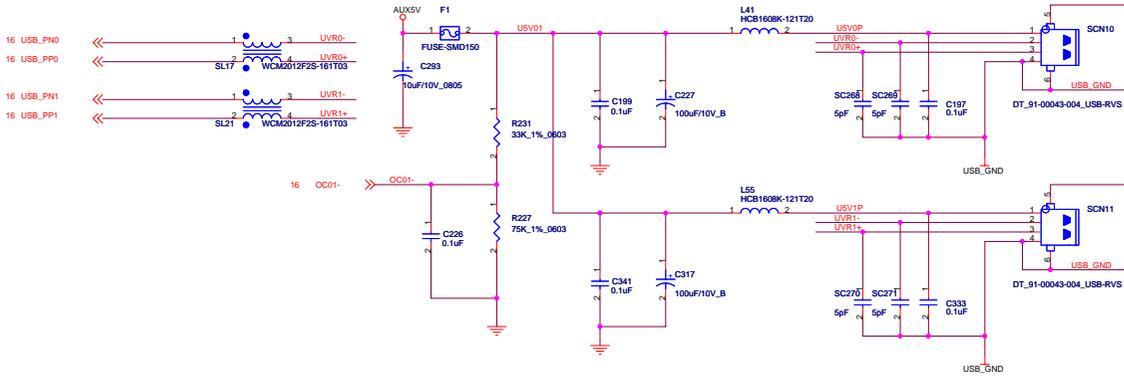
Date: Monday, January 23, 2006 Sheet 17 of 34



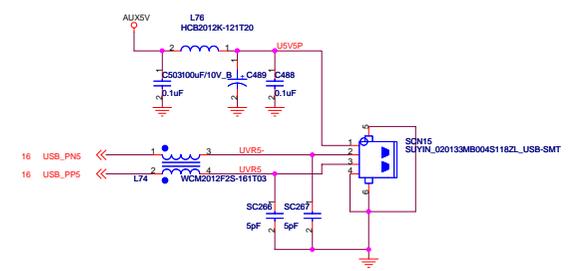
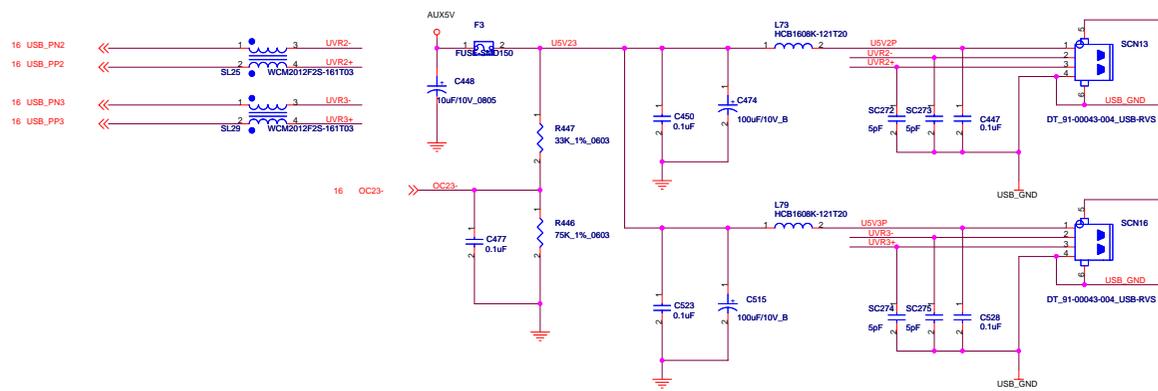


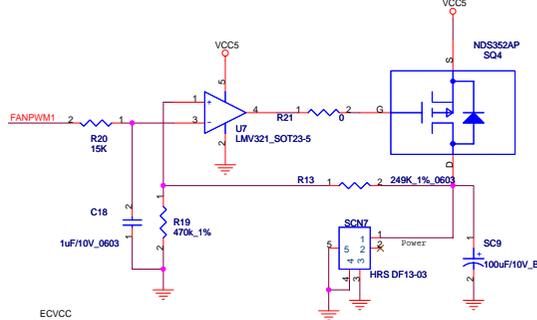
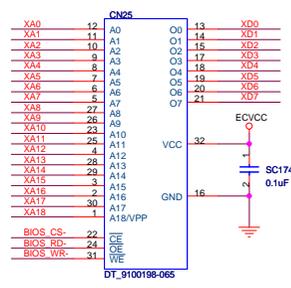
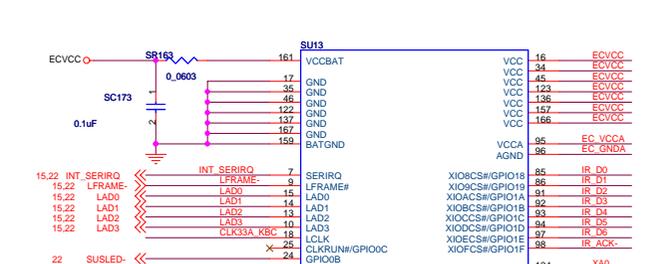
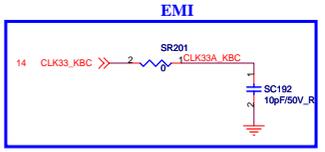
ALL THESE CLOSE TO CONNECTOR

Two ports .1.5A, at least 60 mils
 The dotted line is a moat for layout placement reference.
 Pls Place the components of block into USB moat
 Bead & resistor are bridge

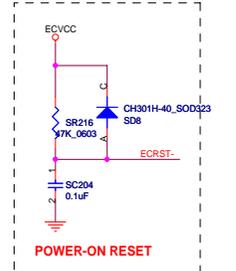


Card Reader

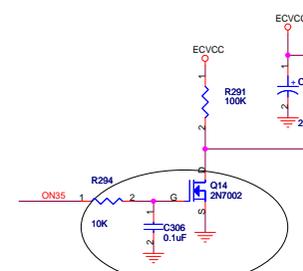
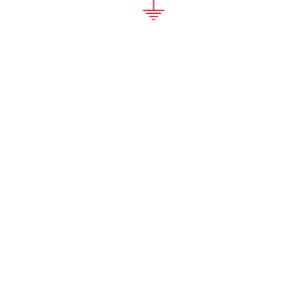
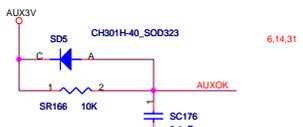
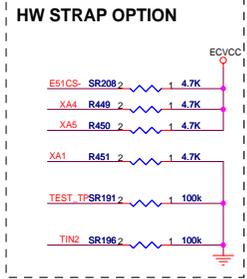
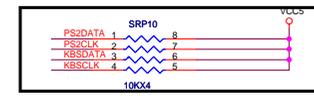
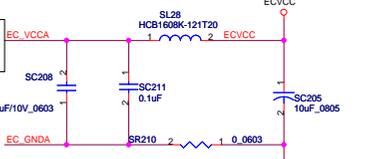




6,11,15,16,19,22,23,24 PLTRST $R364$ 10K_R
 Pull-Down resistor required to avoid leakage current



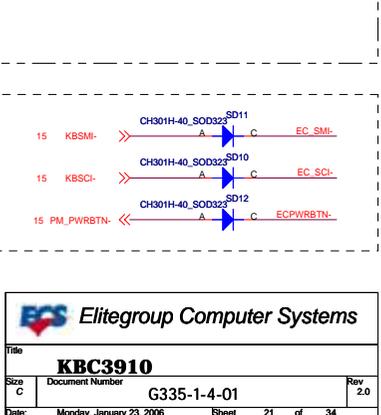
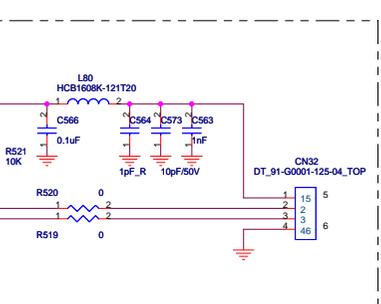
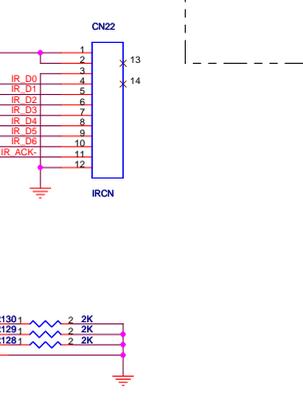
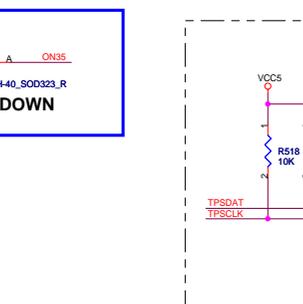
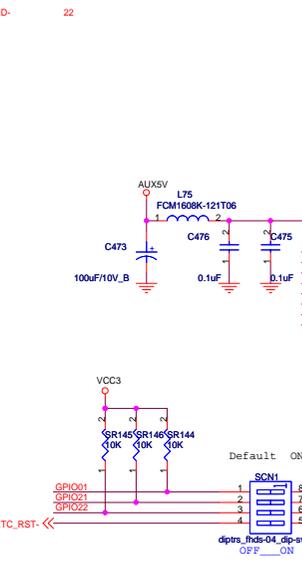
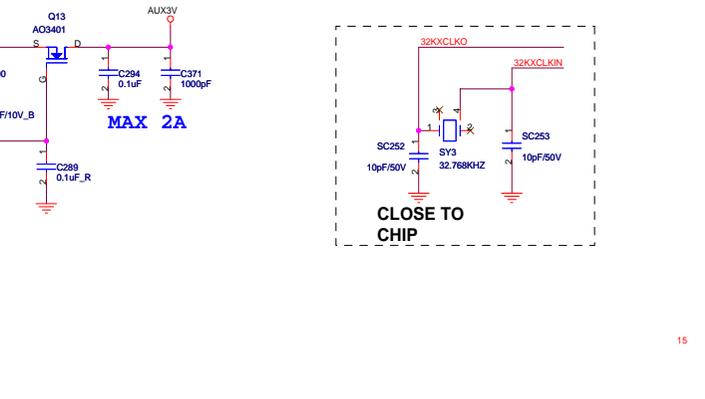
check--> LID SW output to turn-off backlight

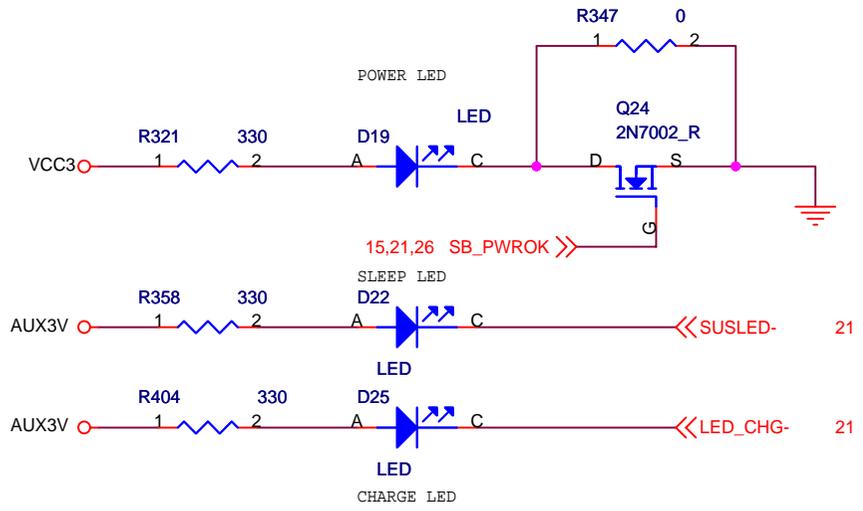


12/1

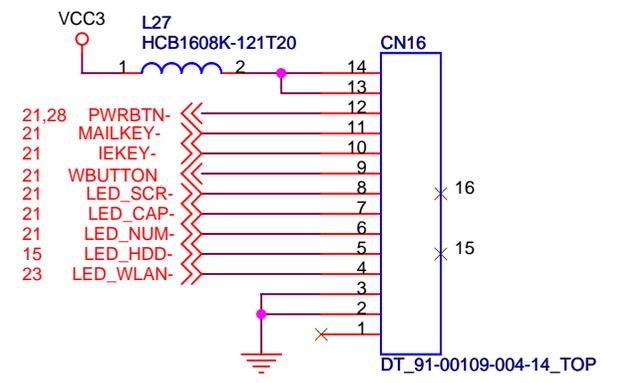
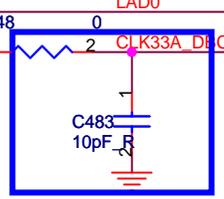
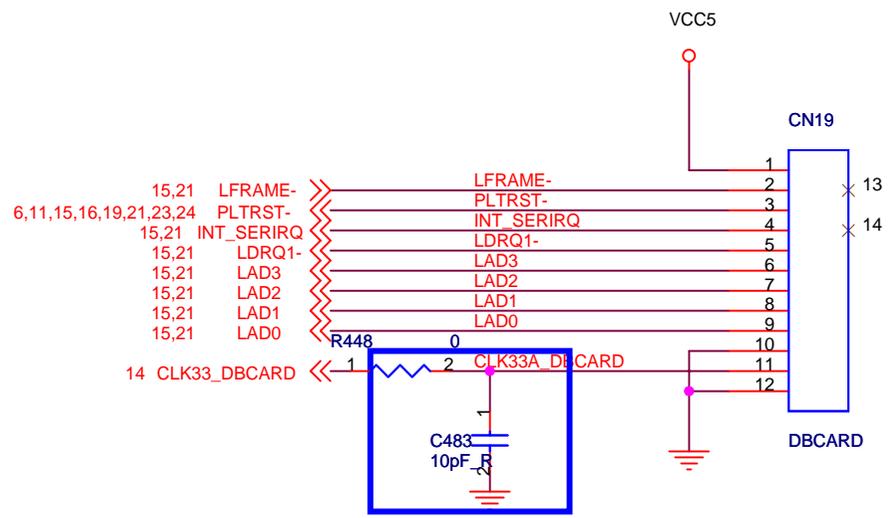
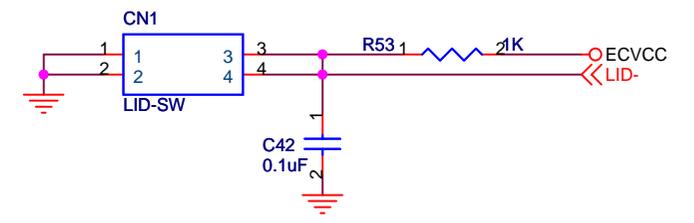


KB3910_176L0FP

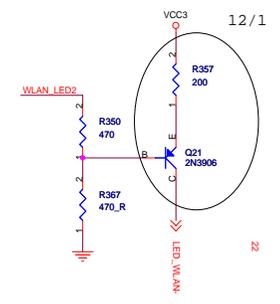
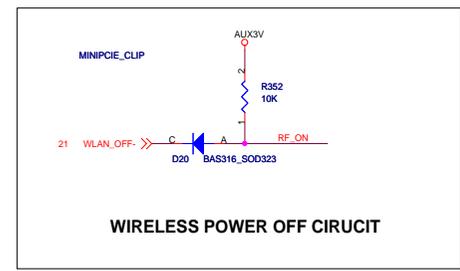
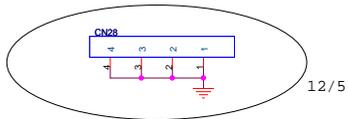
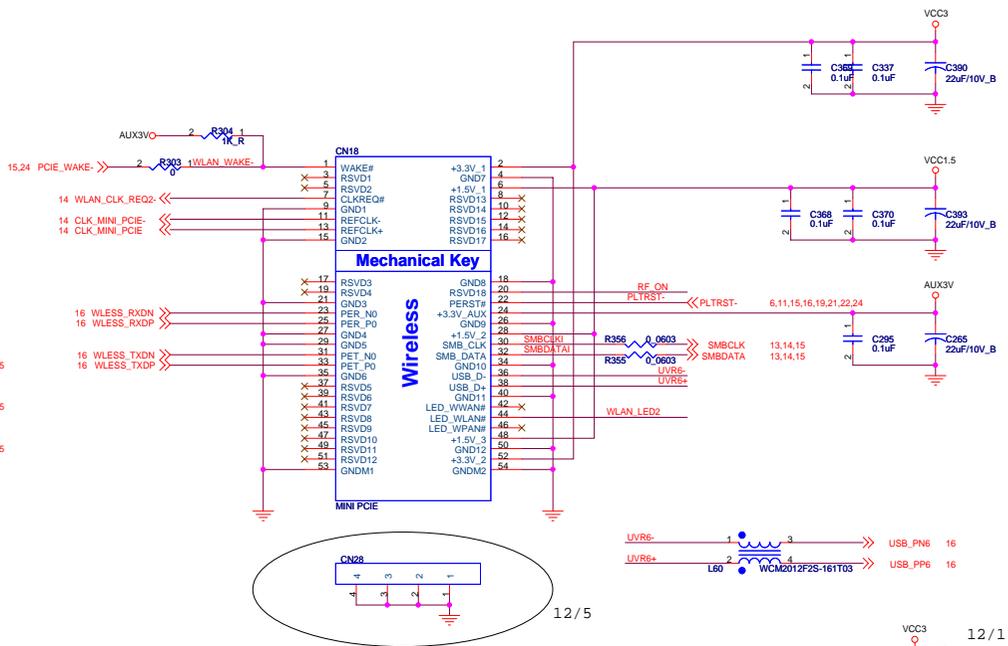
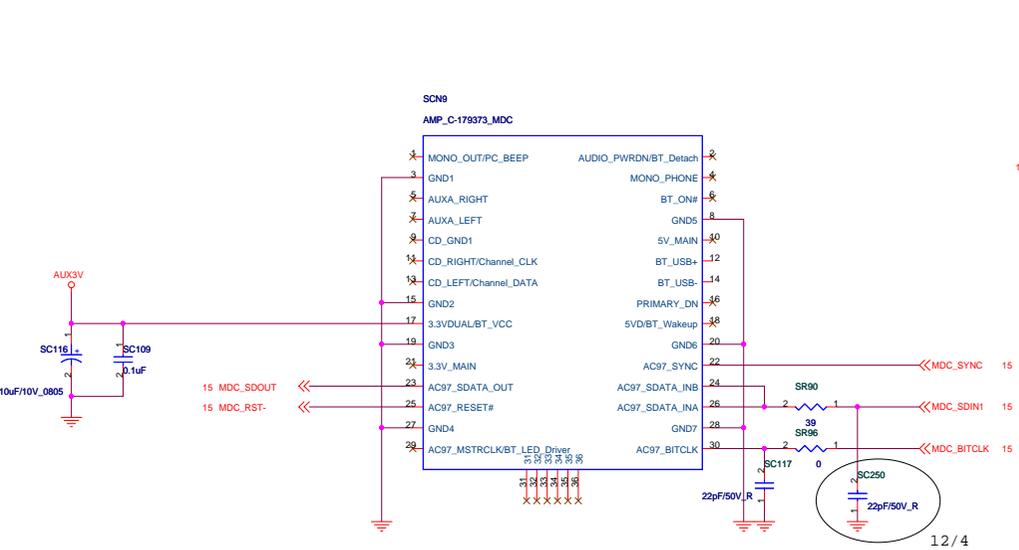


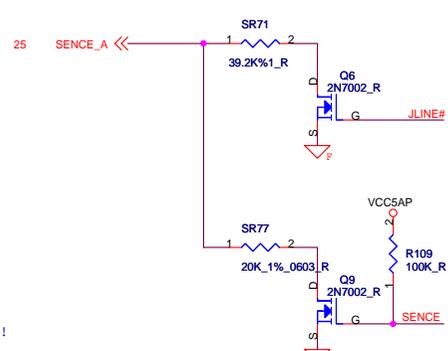
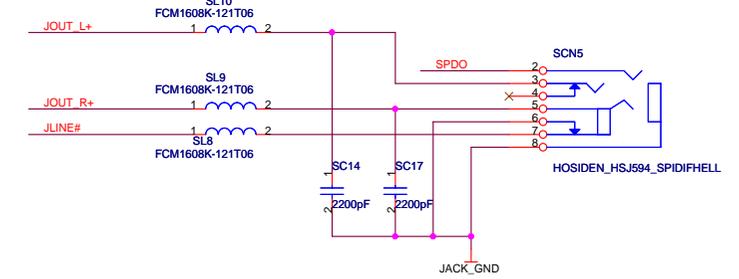
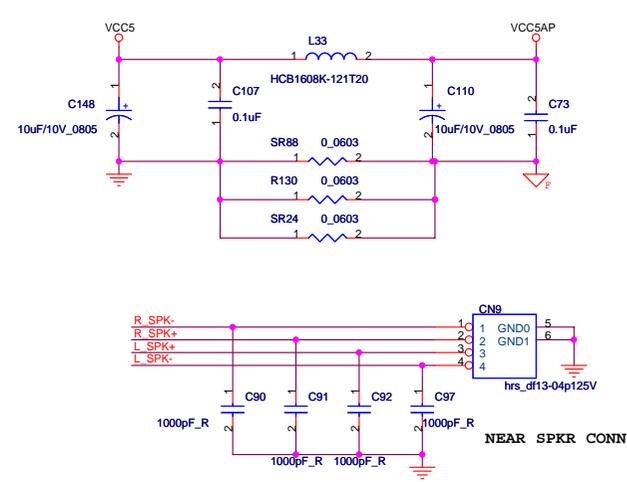
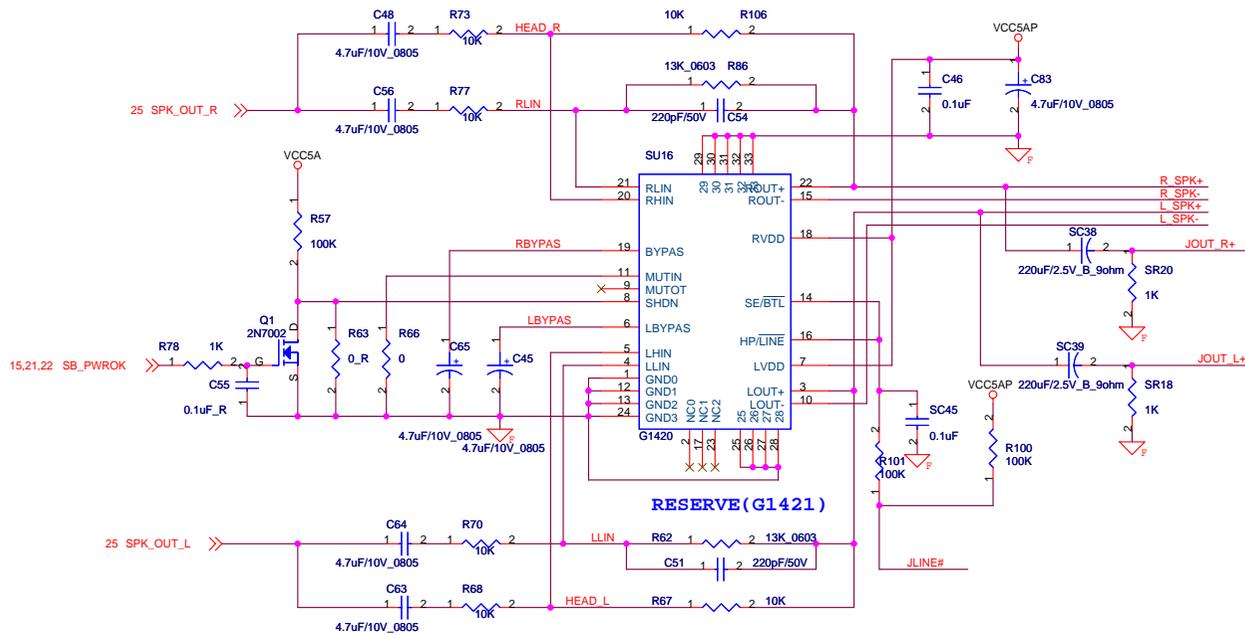


pin 1 & 4 to press

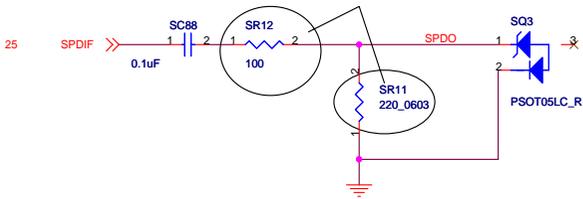


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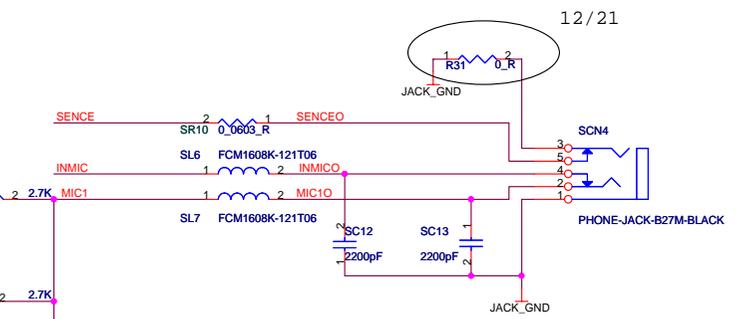
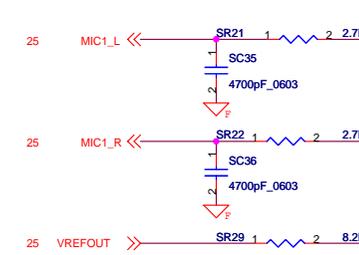
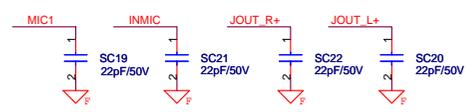




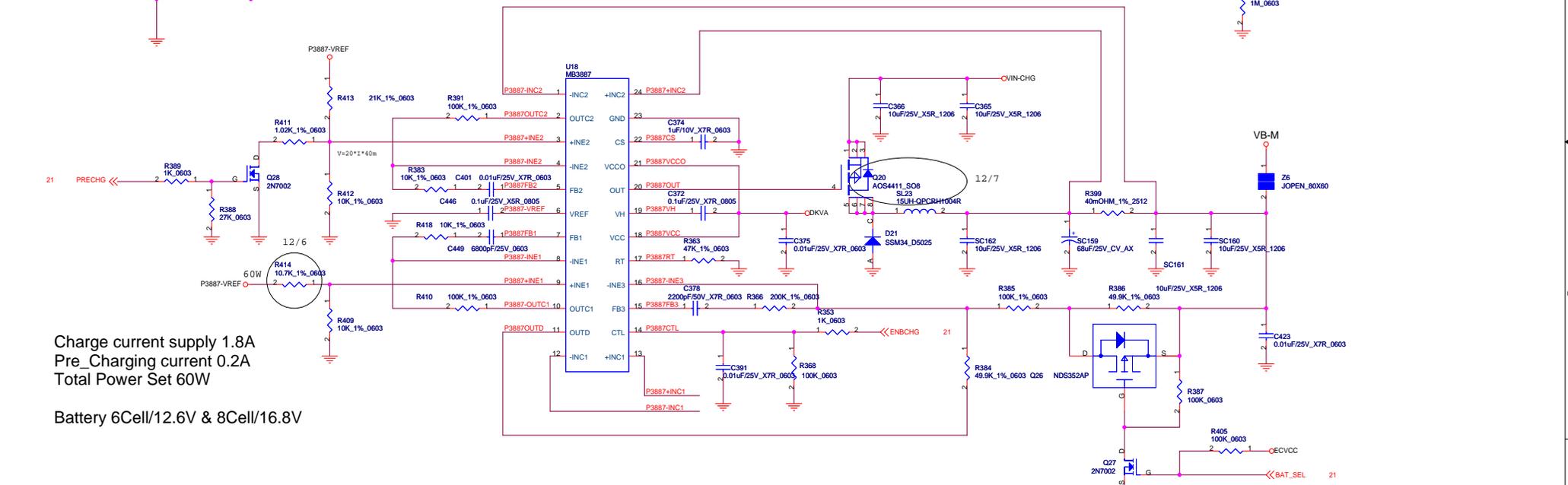
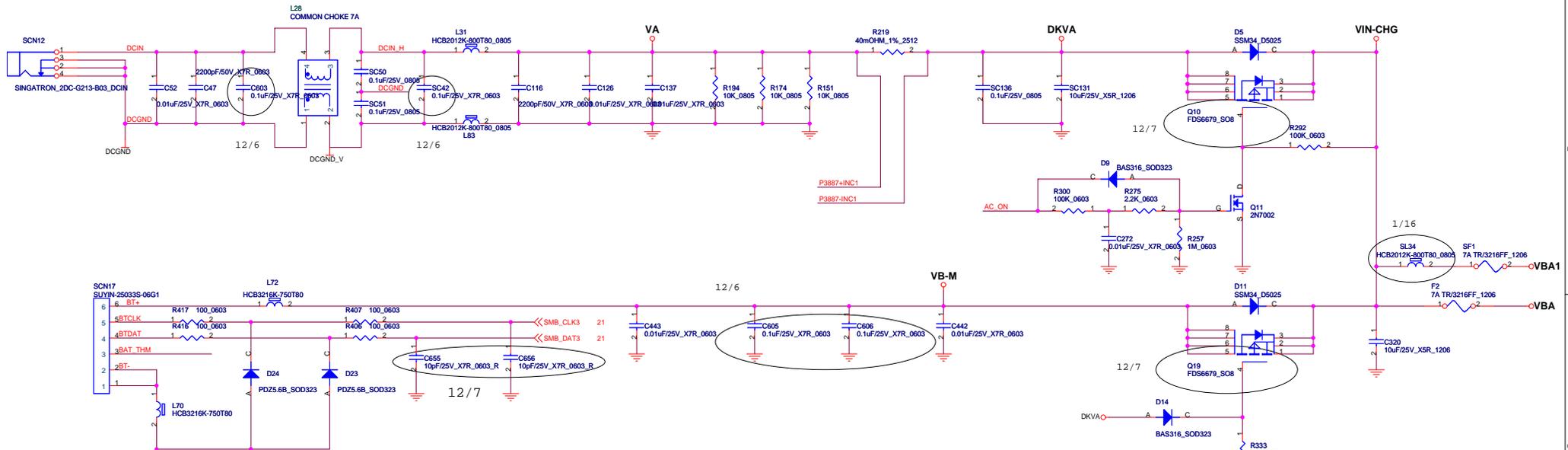
若訊號因為外部CABLE線衰減太大, 將此電阻互換!!



PC2001 SPEC. 12KHz--15KHz
 $F_c = 1 / [2 * 3.14 * R(2.7K) * C(4700PF)] = 12.548KHz$
VREFOUT CONTROL MIC & REAR_OUT_R/L FUNCTION



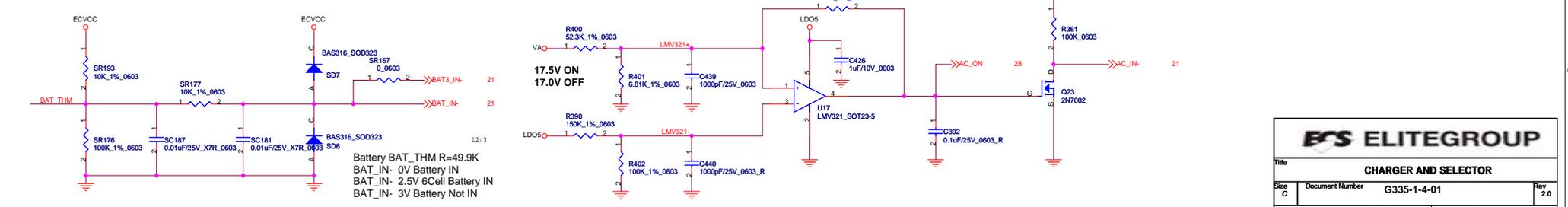
Elitegroup Computer Systems		
OPA & AUDIO JACK		
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Charge current supply 1.8A
 Pre_Charging current 0.2A
 Total Power Set 60W

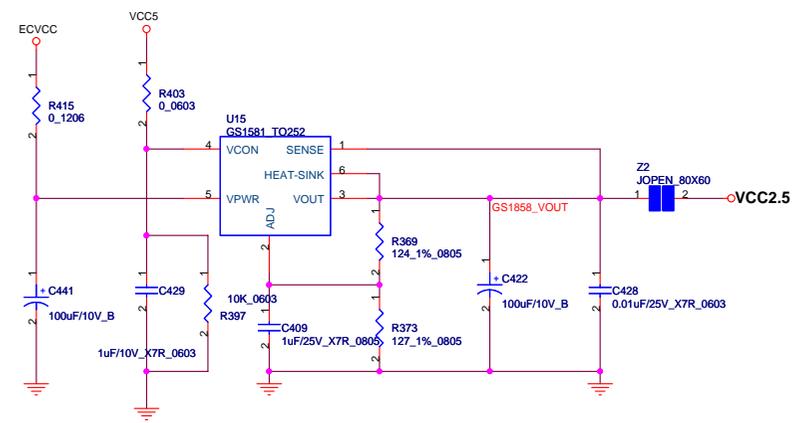
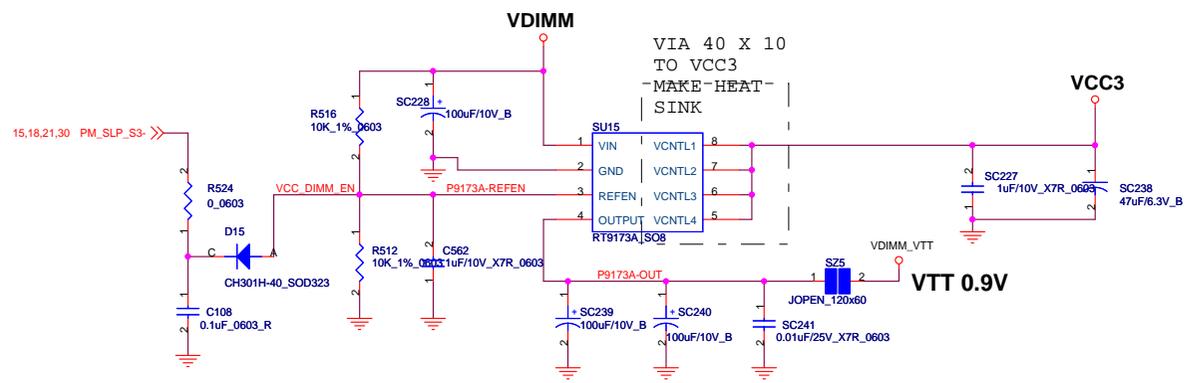
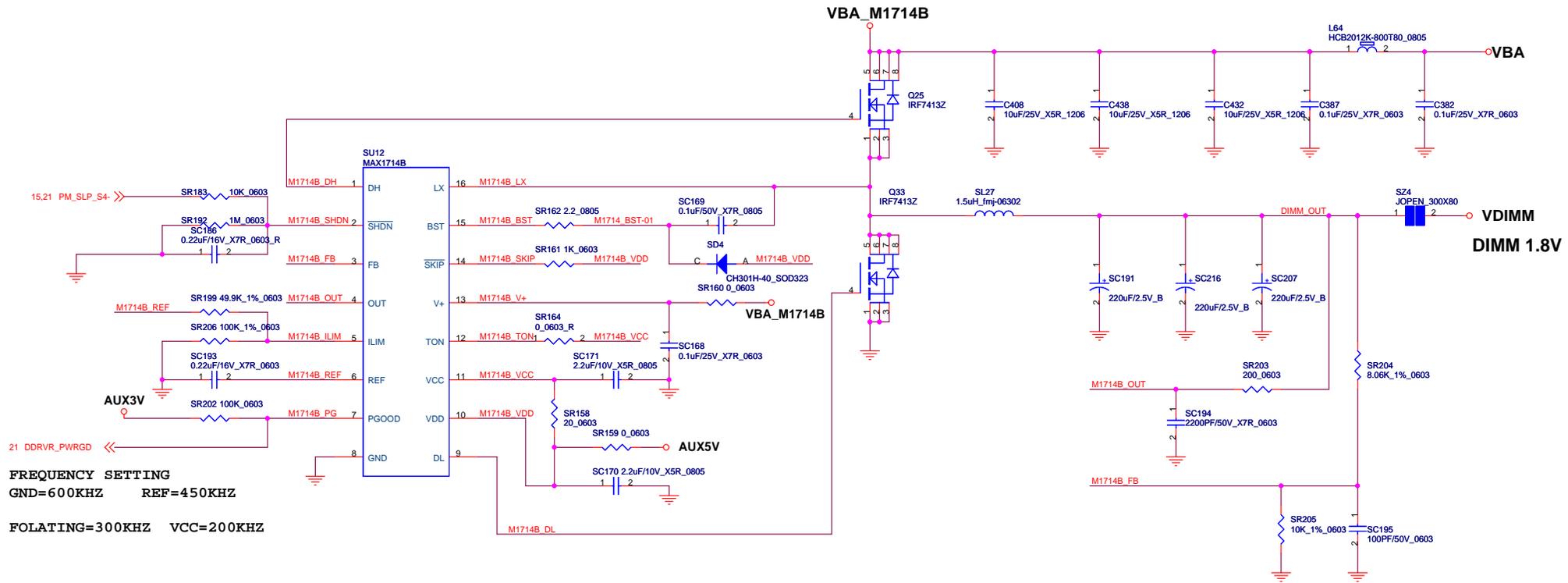
Battery 6Cell/12.6V & 8Cell/16.8V

BAT_SEL H->6Cell L->8Cell

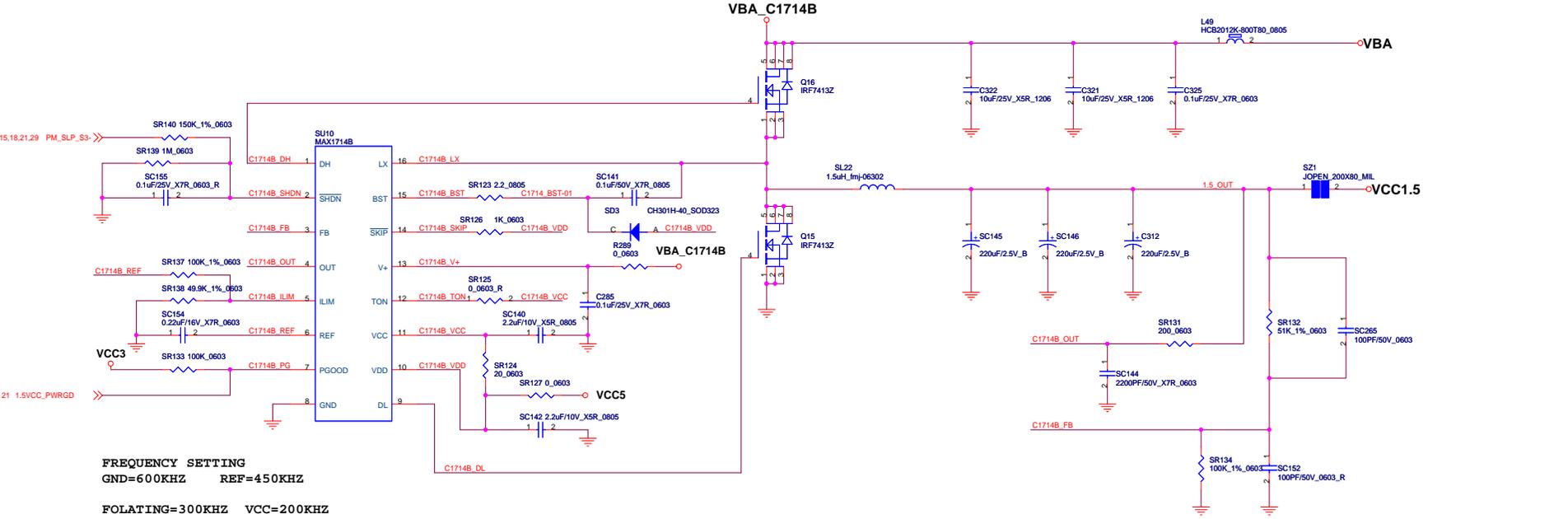
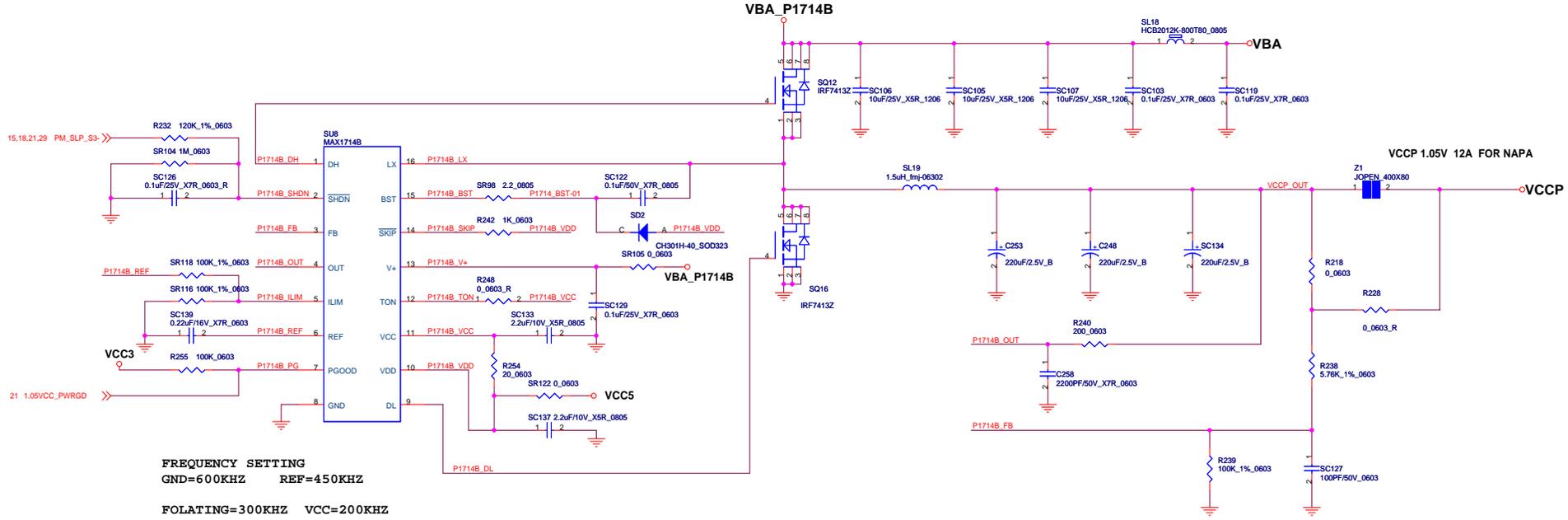


Battery BAT_THM R=49.9K
 BAT_IN- 0V Battery IN
 BAT_IN- 2.5V 6Cell Battery IN
 BAT_IN- 3V Battery Not IN

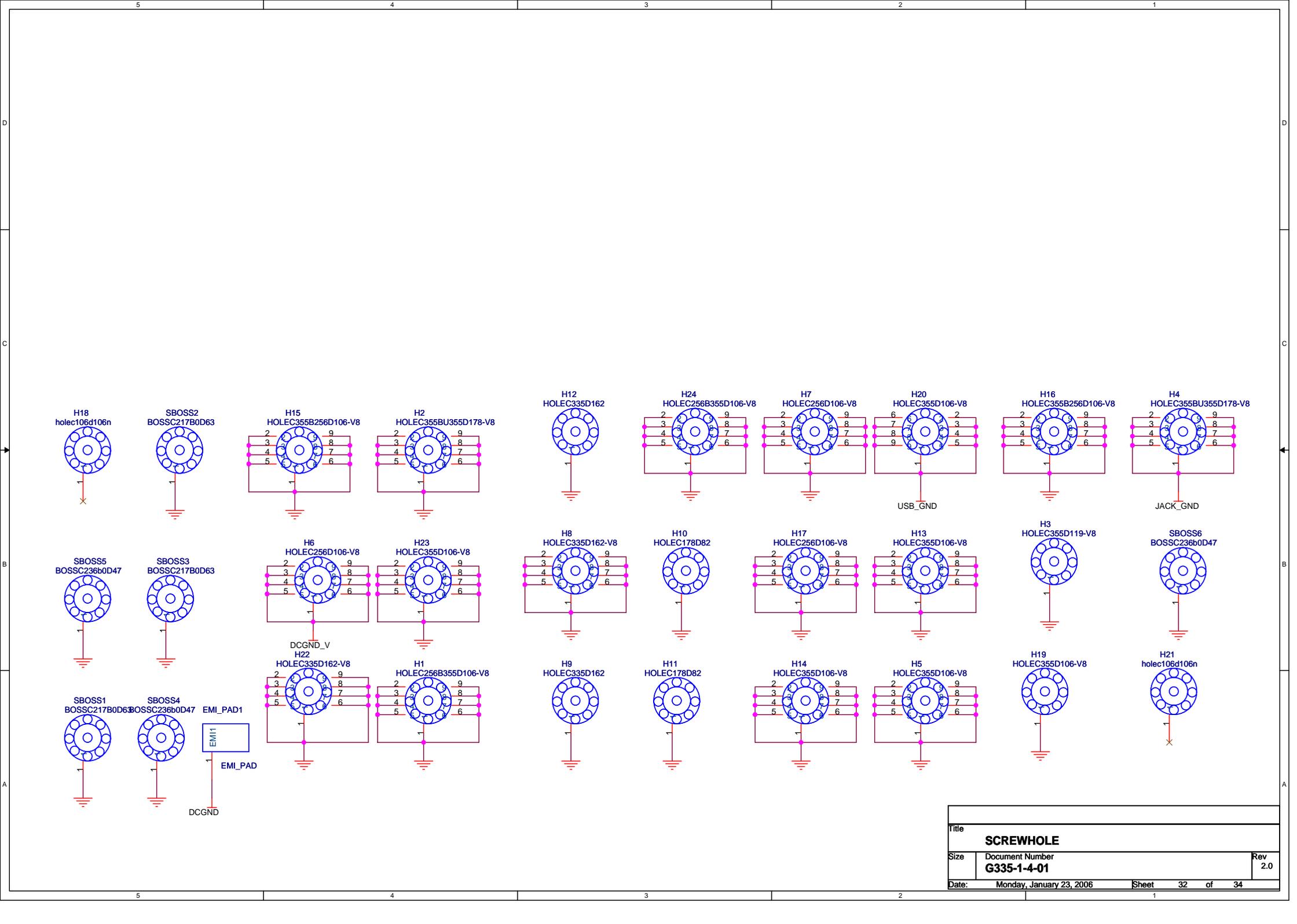
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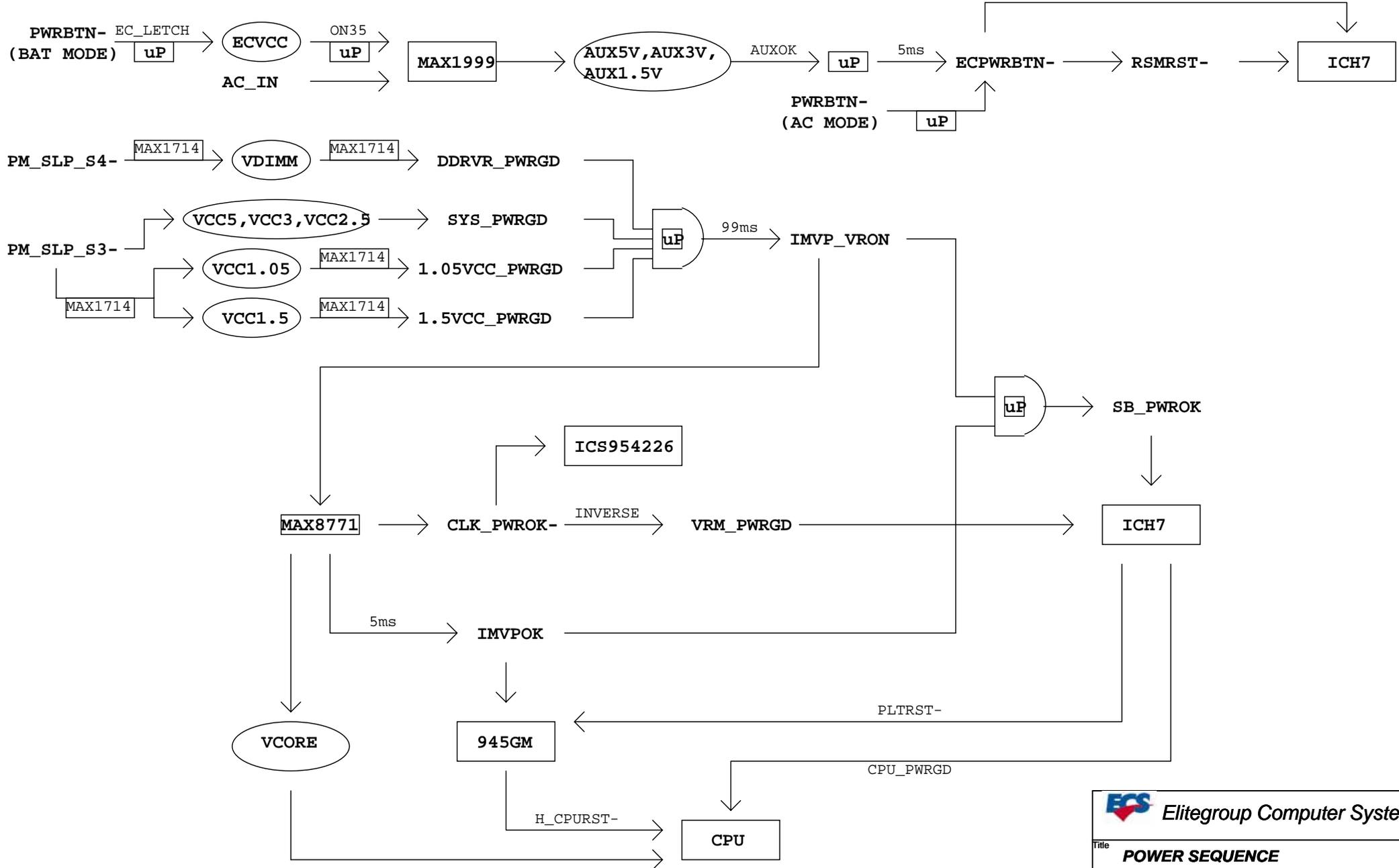
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Title MAX1714B DIMM/DDR		
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ELITEGROUP		
Title MAX1714B VCCP/VCC1.5		
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SCREW HOLE		
Size	Document Number	Rev
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A.0: 2005/11/11 Initial Release 15-F71-010010

B.0: 2005/12/10 Release 15-F71-010020

1.0: 2005/12/23 Release 15-F71-011001

Change R427,R420 10K

Del C453, C456 2.2uF

Del SC62 1uF

Change R550 100 ohm

2.0: 2006/01/23 Release 15-F71-012000

Del C537 220uF

Add SL34 HCB2012K-800T80

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