

A531 SCHEMATICS

- | | |
|---|---|
| <ul style="list-style-type: none"> 01.THIS PAGE 02.TM5800 DDR Interface 03.TM5800 PCI Interface 04.TM5800 SIDEBAND 05.TM5800 POWER&GND 06.CKE SW& TDM DEBUG PORT 07.DDR DIMM MOUDLE 08.PARALLEL&SERIAL ROM&DEBUG PORT 09.CLOCK GENERATOR 10.M1535+(PCI+IDE) 11.M1535+ MISC. 12.M1535+(AUDIO/IO) 13.M1535+(POWER+GPIO) 14.HDD & CDROM CONN. 15.M1535+(AUDIO/IO/KB/IR) 16.SIS315E-1 17.SIS315E-2 18.SIS315E-3 19.VIDEO MEMORY 20.LCD POWER & BL CONTROL 21.LVDS TRANSMITTER 22.CRT Connector 23.ALI M5273 24.USB PORT 25.KBC & T/P 26.AUDIO OP AMPLIFIER 27.RJ45 28.MINIPCI 29.RTC | <ul style="list-style-type: none"> 30.LPC ROM&LED&PWRGD 31.POWER-SW&PLLVDD&VCP33/25 32.AUDIO CODEC 33.OPA & AUDIO JACK 34.CHARGER AND SELECTOR 35.DC-DC MAX1817 36.VCORE FAN5250 37.BAT. LOW & OVER T.& LDO PWR 38.DDR POWER 39.HISTORY |
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PCB NO. : 15-F22-011001
REV. : V1.0

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P.Leader	Appr.by	Check by	Design by

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2.80k_1% FOR C_VREF SPEC=1.4V +/- 7% FOR TM5800 VER /1.X (UNDER 933MHz)

2.15K_1% FOR C_VREF SPEC=1.2V +/- 1.25% FOR TM5800 VER 2.X (ABOVE 1GHz)

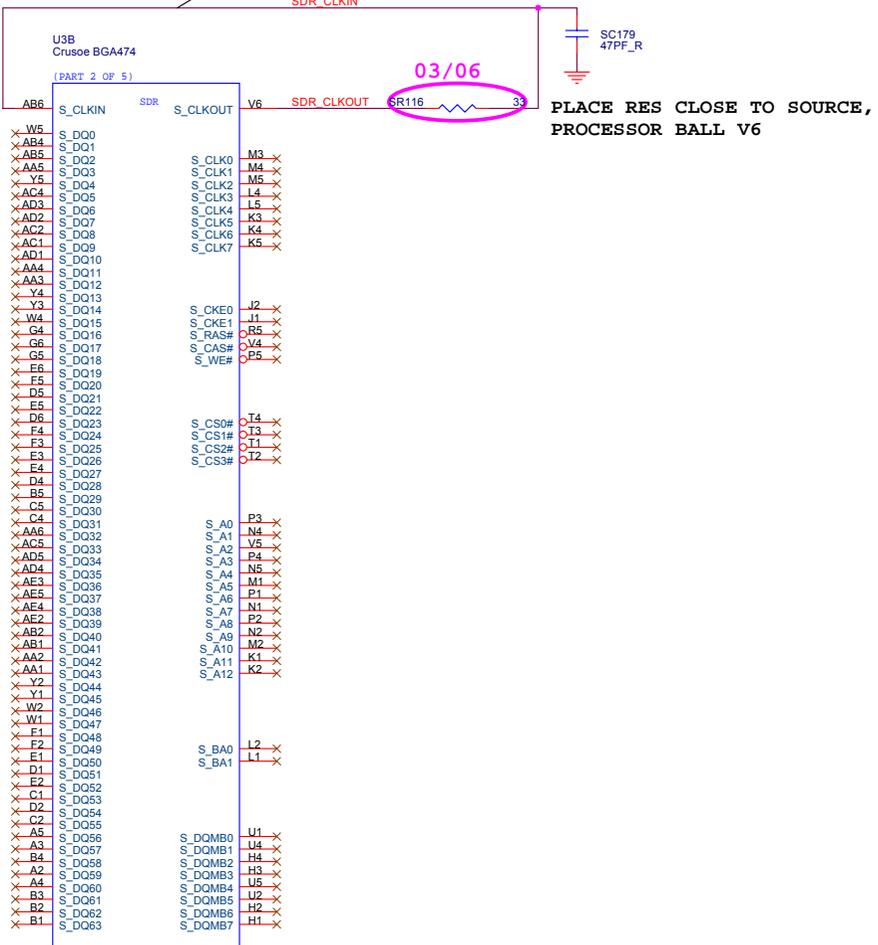
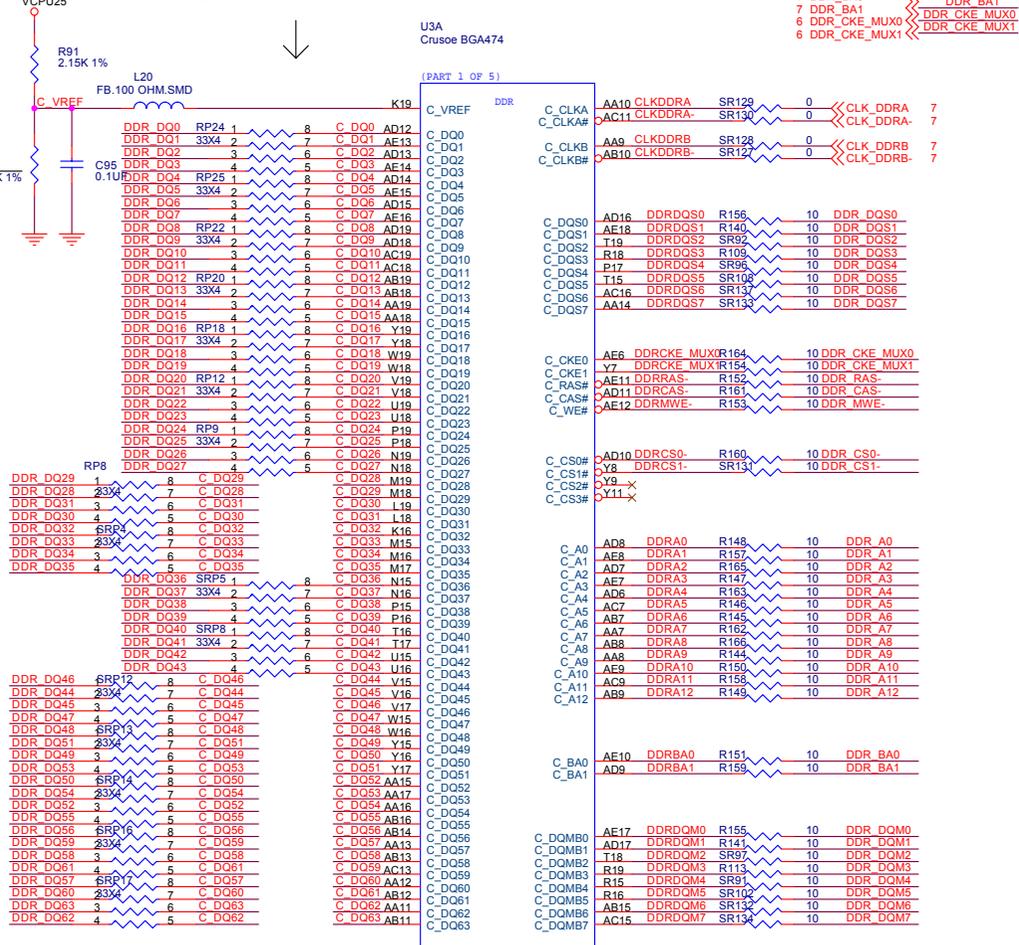
FB 100 OHM
PART NUMBER-->16-100-101160

U3A
Crusoe BGA474

- 7 DDR_A[12..0] << DDR_A[12..0]
- 7 DDR_DQM[7..0] << DDR_DQM[7..0]
- 7 DDR_DQ[0..63] << DDR_DQ[0..63]
- 7 DDR_DQS[7..0] << DDR_DQS[7..0]
- 7 DDR_CS0- << DDR_CS0-
- 7 DDR_CS1- << DDR_CS1-
- 7 DDR_RAS- << DDR_RAS-
- 7 DDR_CAS- << DDR_CAS-
- 7 DDR_MWE- << DDR_MWE-
- 7 DDR_BA0 << DDR_BA0
- 7 DDR_BA1 << DDR_BA1
- 6 DDR_CKE_MUX0 << DDR_CKE_MUX0
- 6 DDR_CKE_MUX1 << DDR_CKE_MUX1

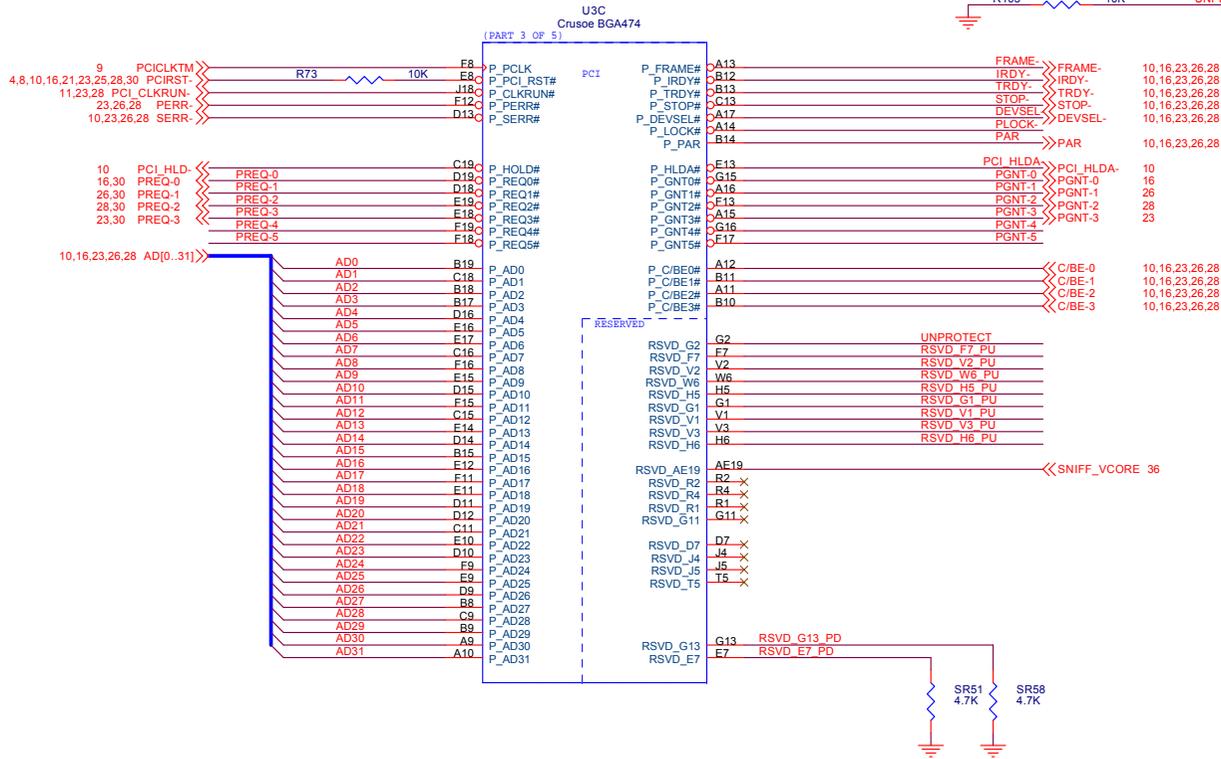
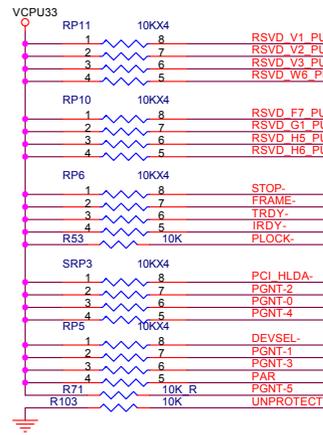
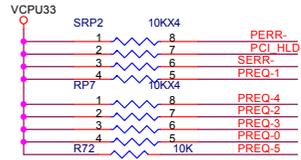
NOTE:
REFER TO SYSTEM DESIGN

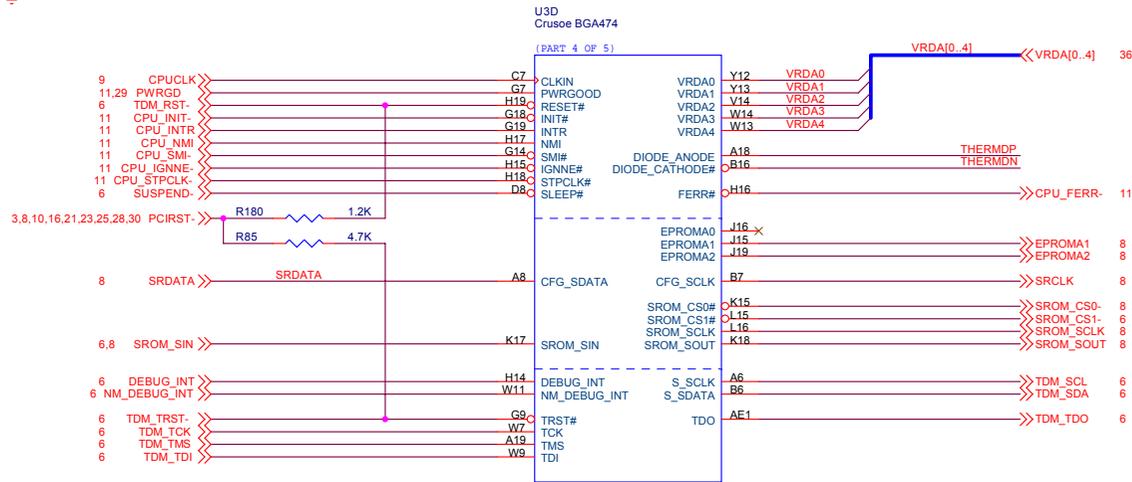
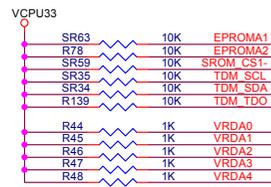
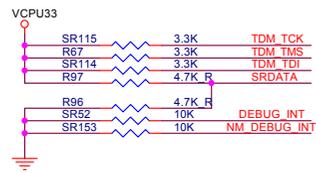
GUIDE FOR TRACE LENGTH



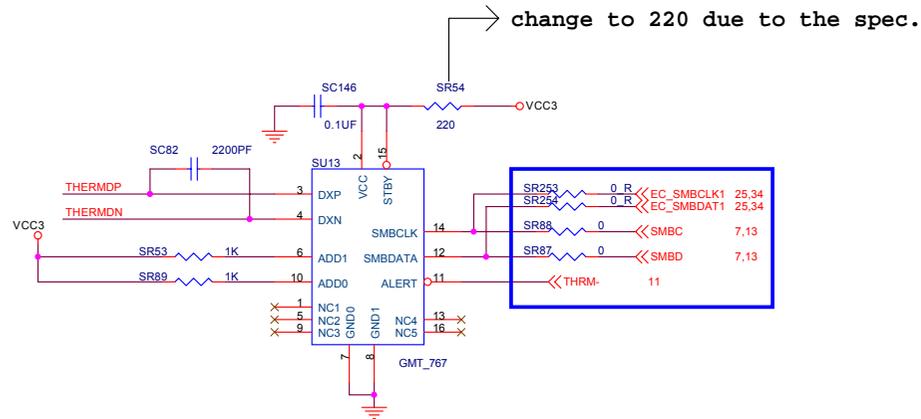
PLACE RES CLOSE TO SOURCE,
PROCESSOR BALL V6

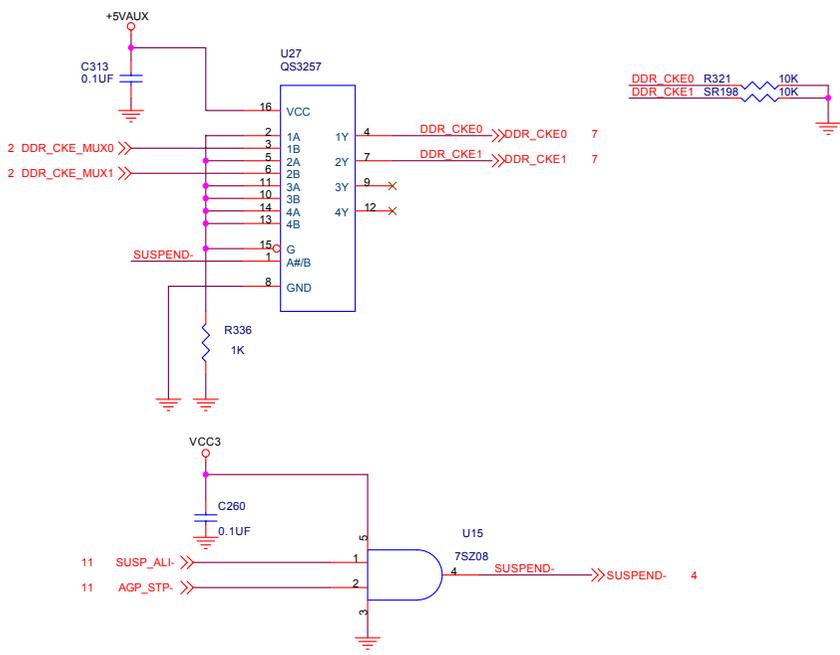






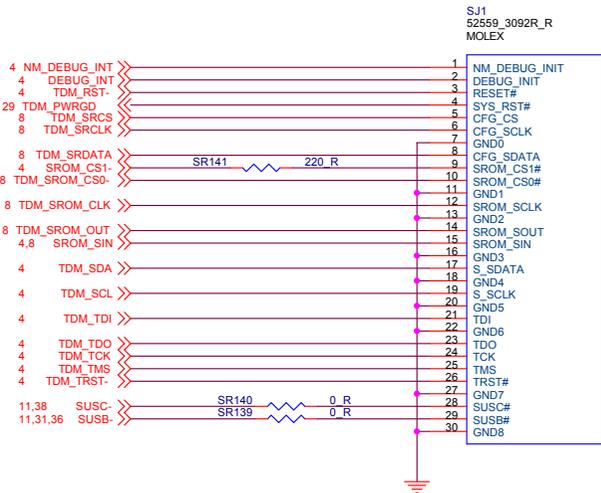
SYSTEMS THAT DO NOT INSTALL MODE BIT ROM:
 INSTALL PU R407 WHEN CMS IS IN THE SERIAL ROM
 INSTALL PD R409 WHEN CMS IS IN THE PARALLEL ROM





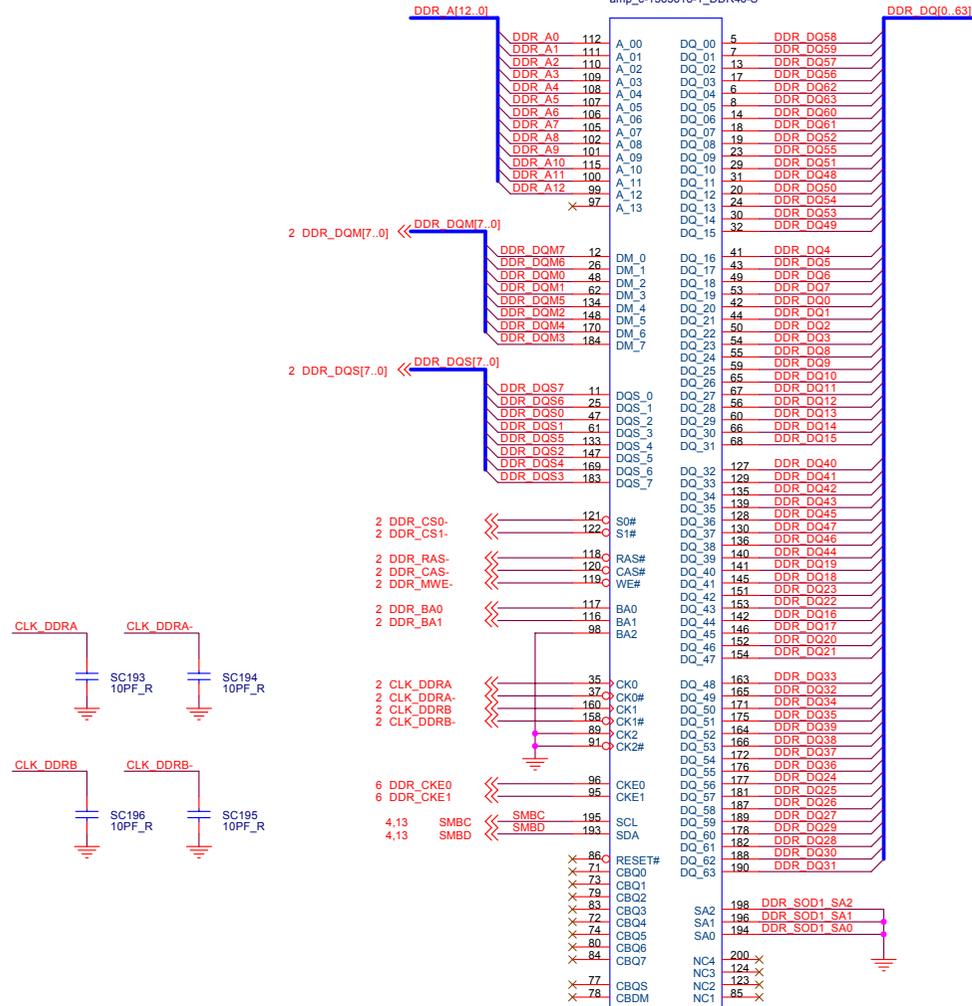
TRANSMETA DEBUG CONNECTOR

NOTE: Pinout depends on type of connector used. The pinout below is for the vertical TDC connector. See the Design Guide for the pinout of the right angle connector.

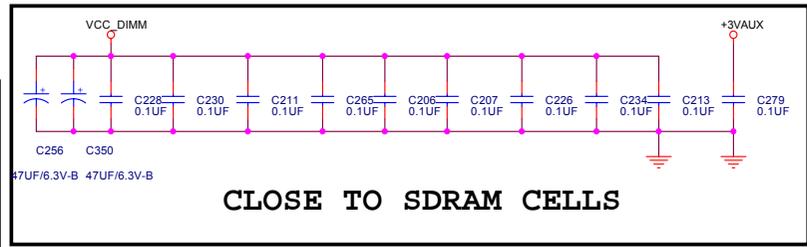
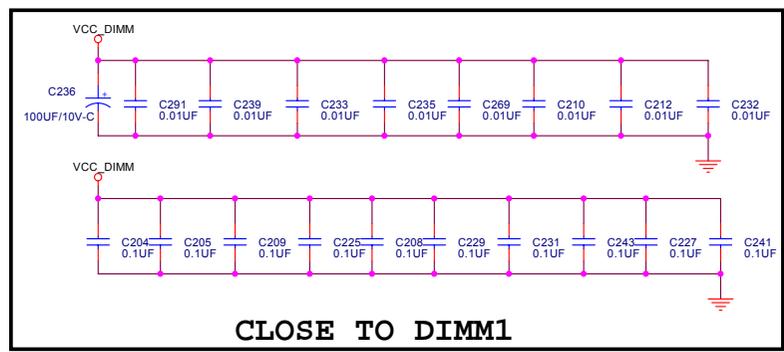
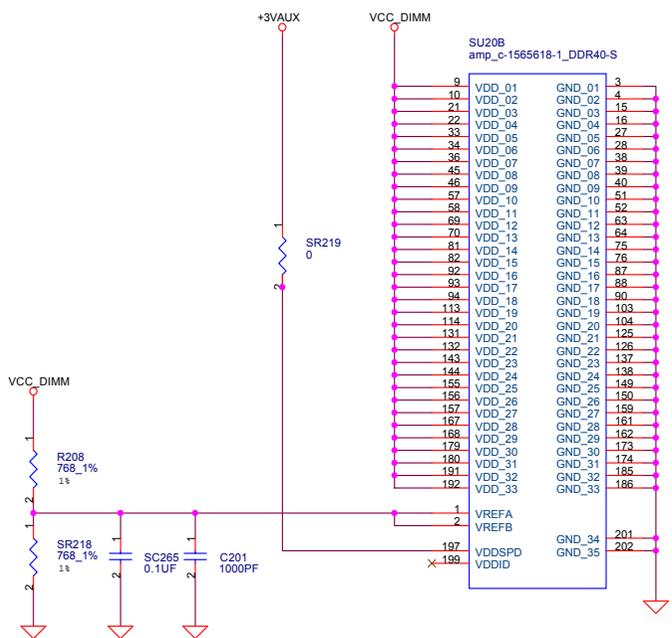


DIMM1

SU20A
amp_c-1565618-1_DDR40-S



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- 2 DDR_DQM[7..0] << DDR_DQM[7..0]
- 2 DDR_DQ[0..63] << DDR_DQ[0..63]
- 2 DDR_DQS[7..0] << DDR_DQS[7..0]

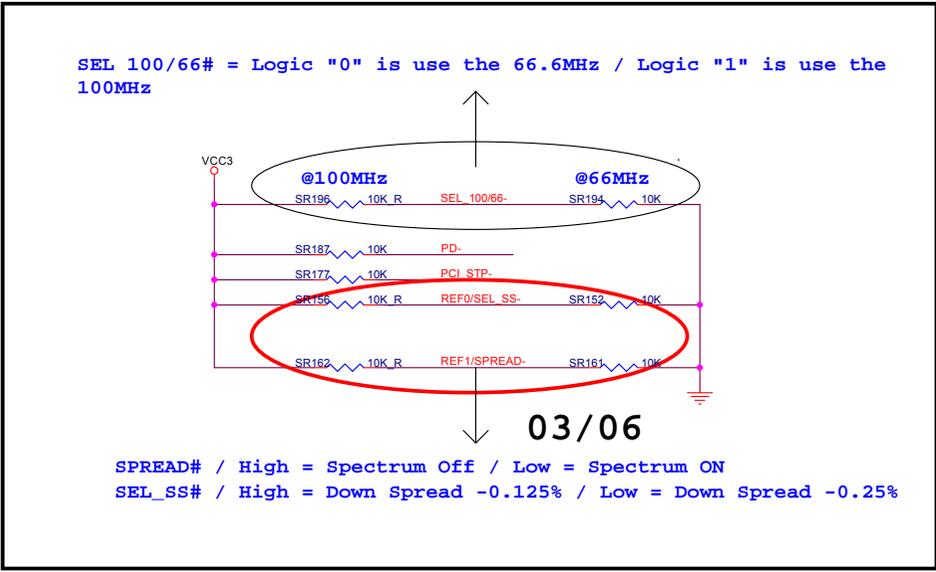
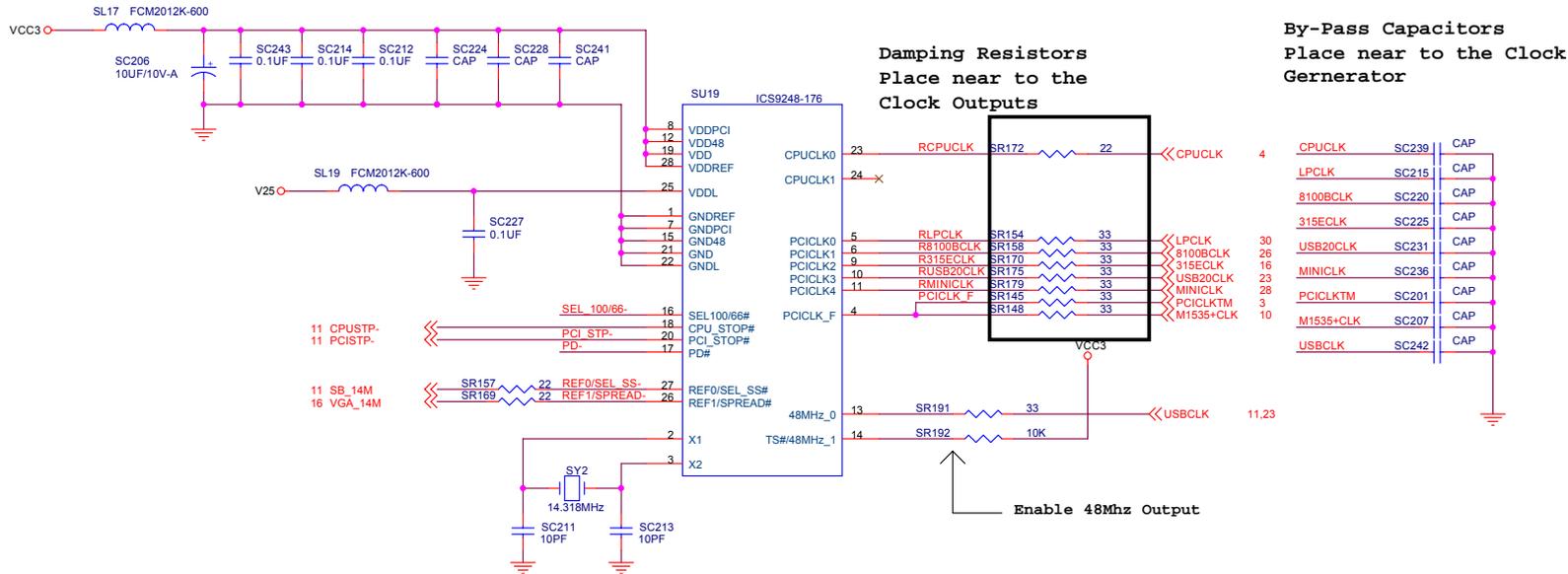


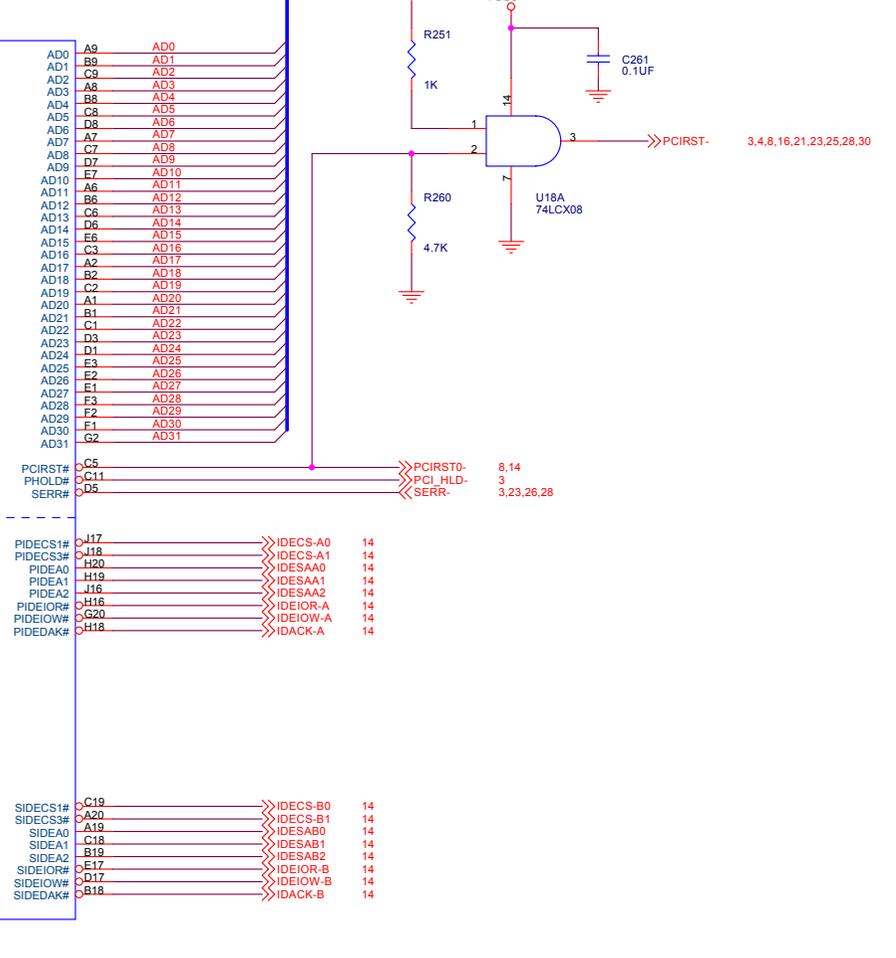
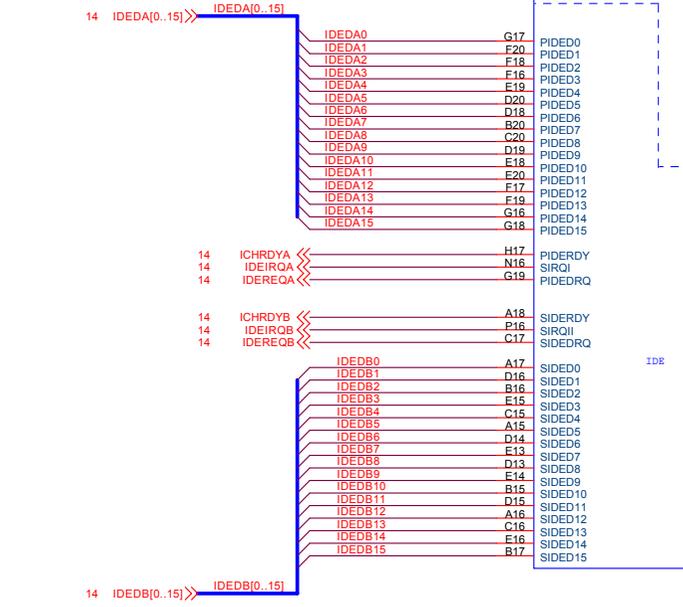
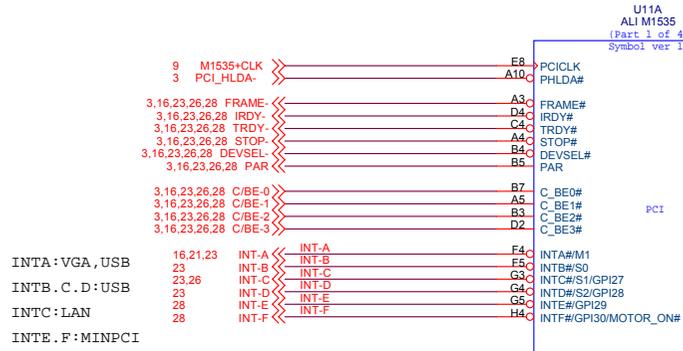
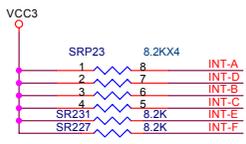
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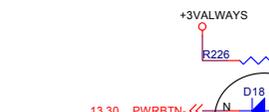
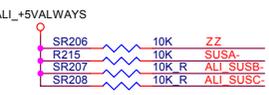
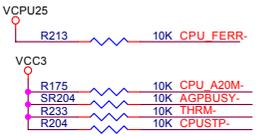
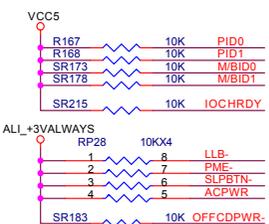
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Size: B Document Number: A531-1-4-01 Rev: V1.0

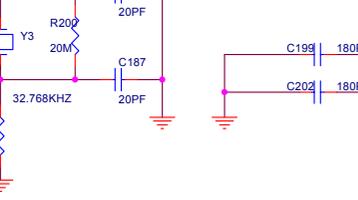
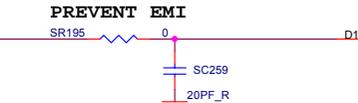
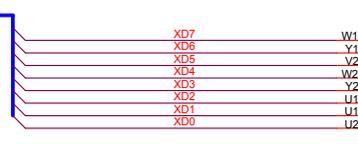
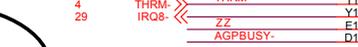
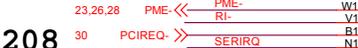
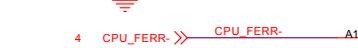
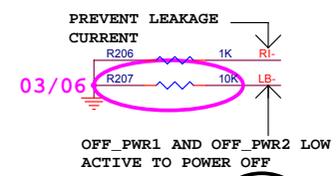
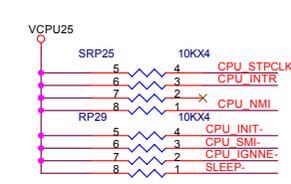
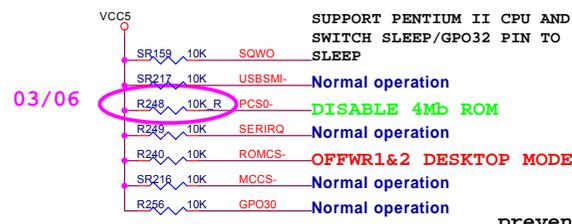
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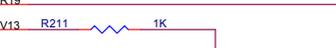
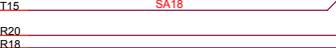
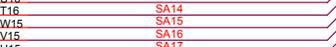
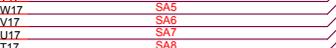
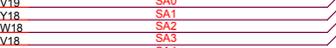
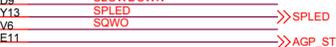
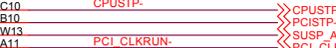
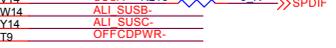
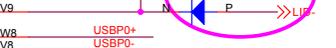




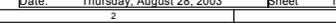
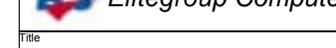
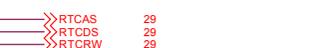
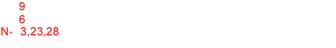
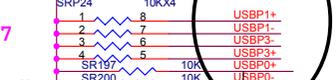
PUT SAME R208
DEL R208, C215 03/27



prevent resume power flow out



OFF_PWR1 AND OFF_PWR2 LOW ACTIVE TO POWER OFF

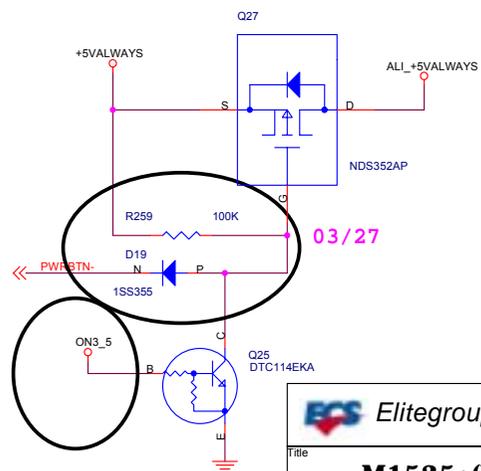
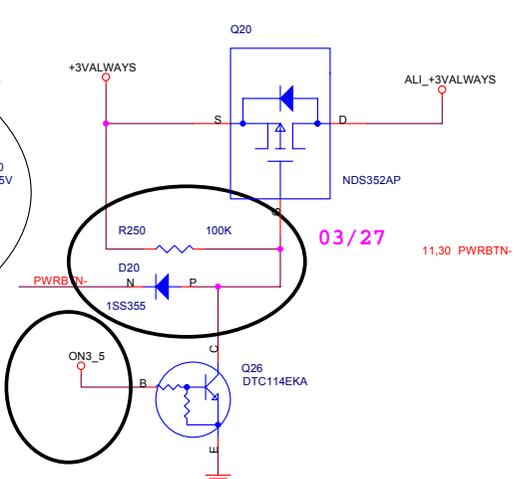
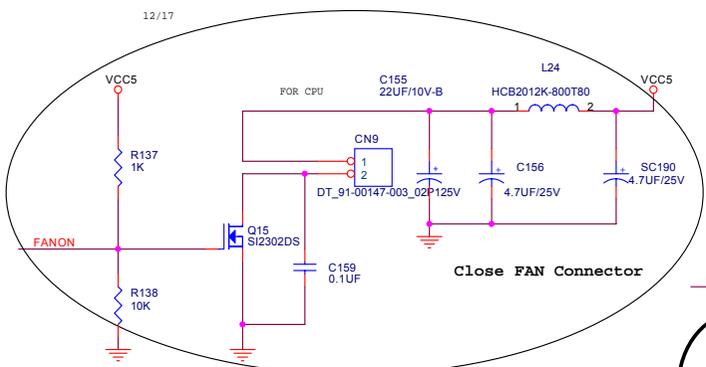
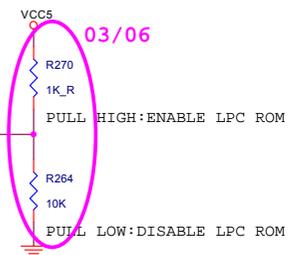
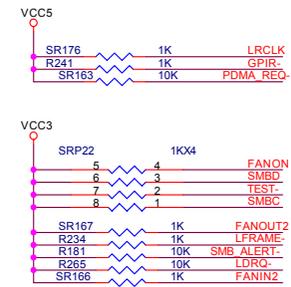
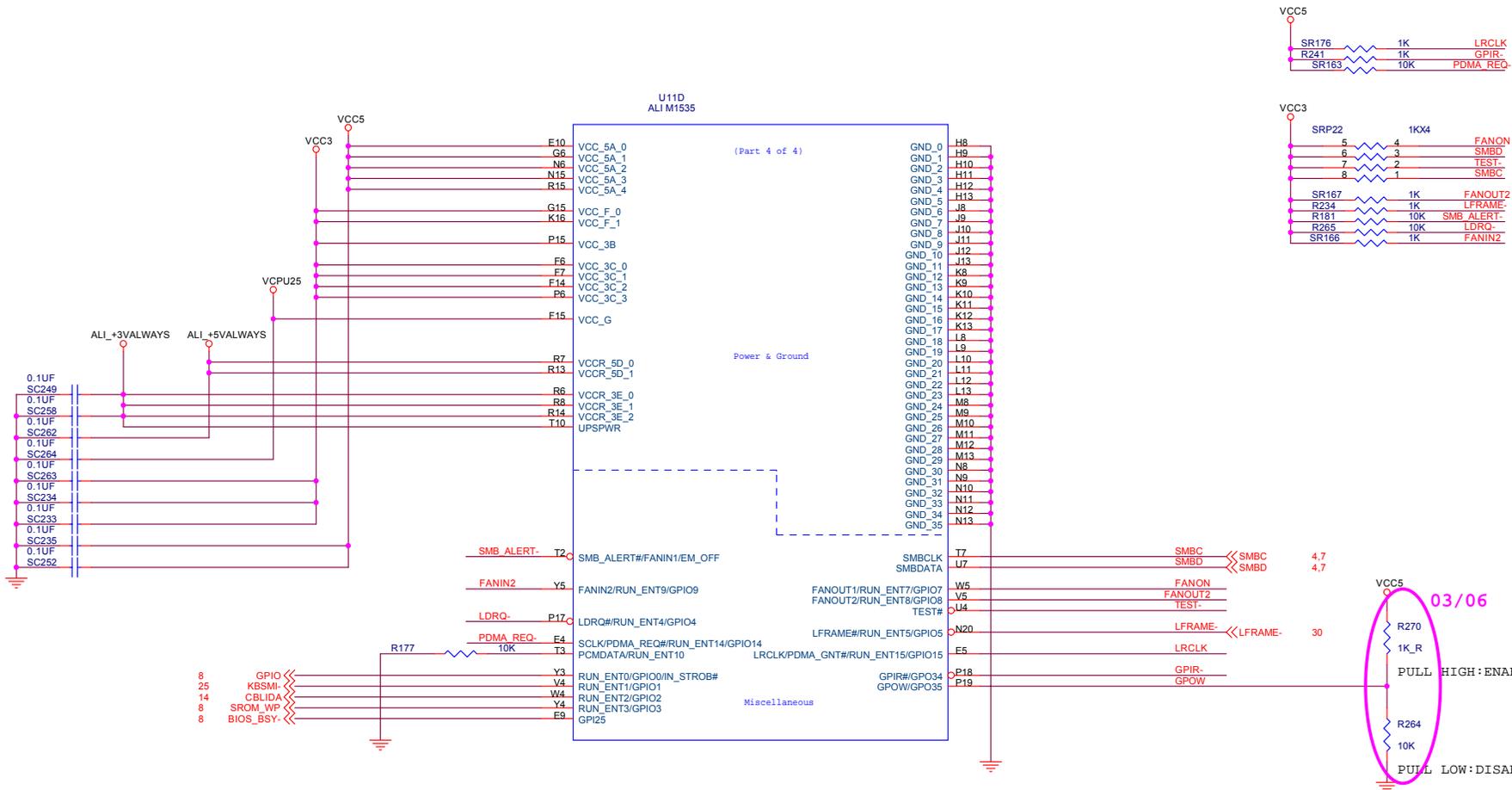


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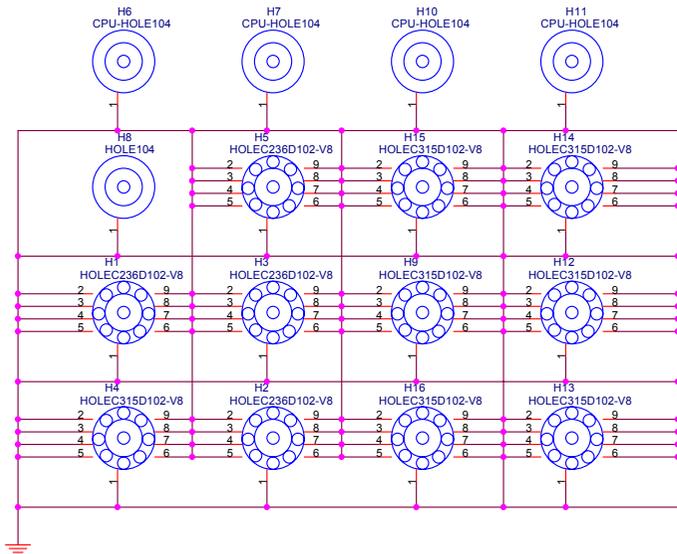
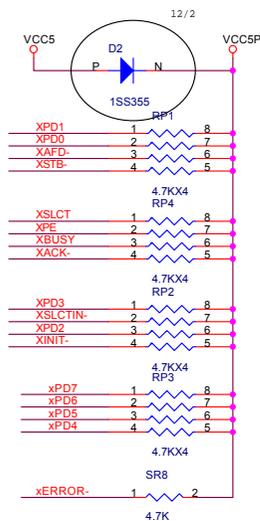
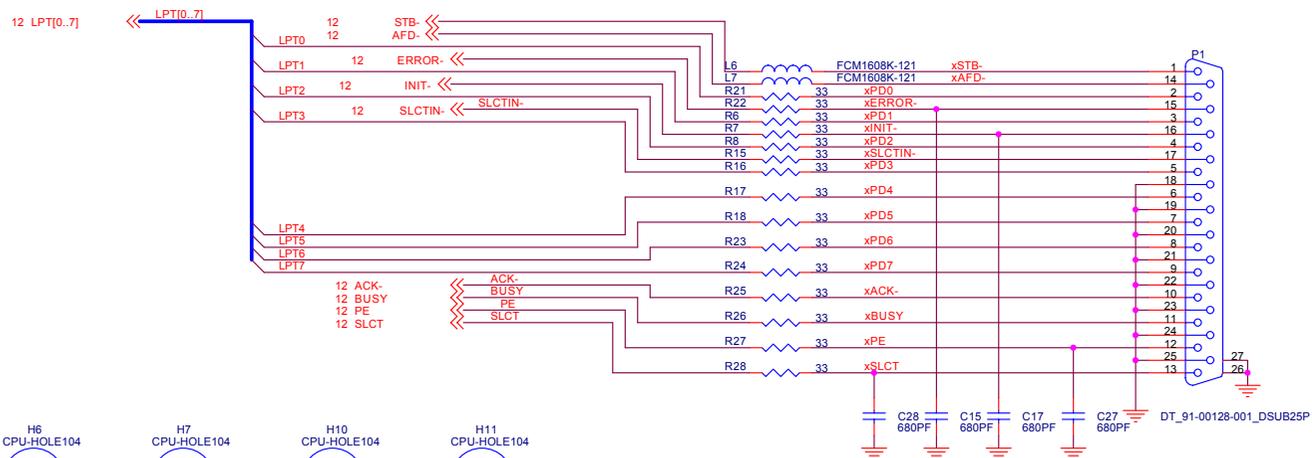
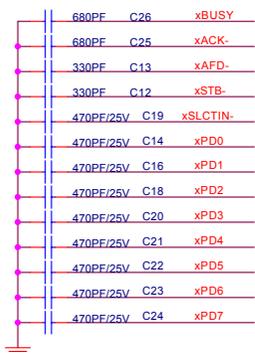
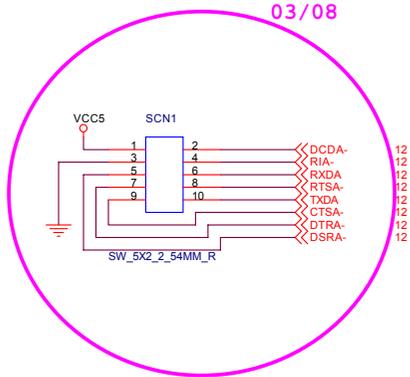
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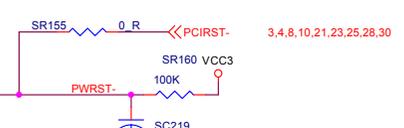
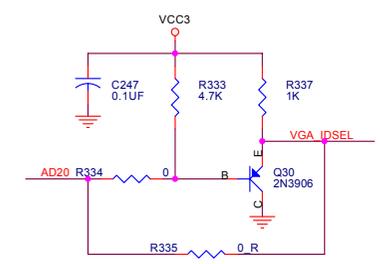
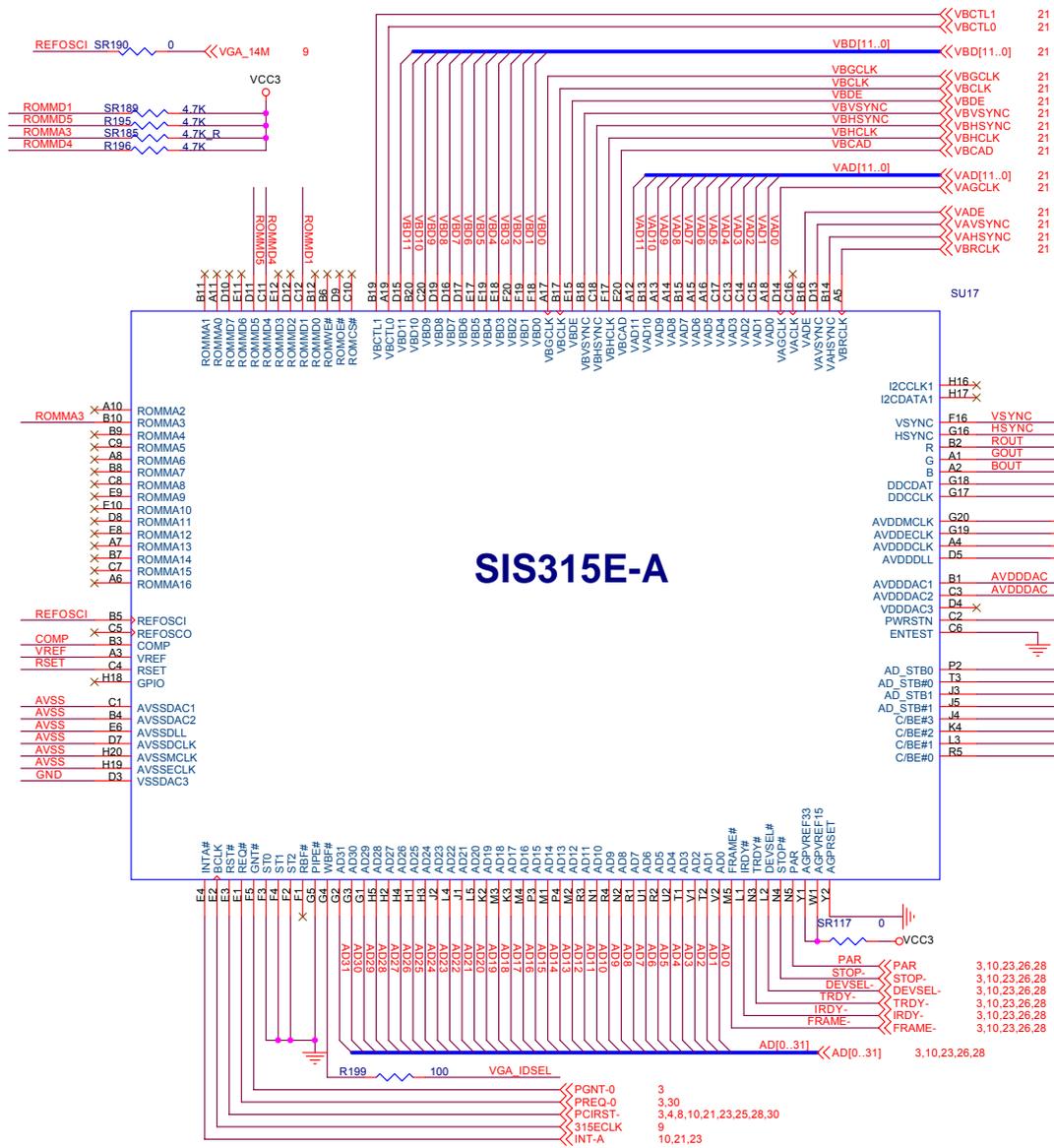


ECS Elitegroup Computer Systems

Title: **COM & LPT PORT**

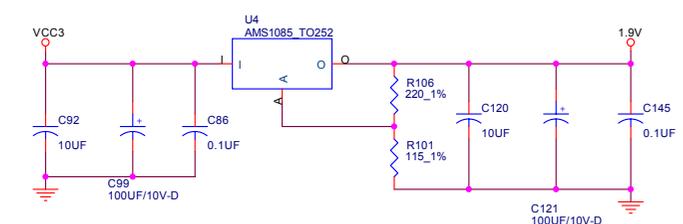
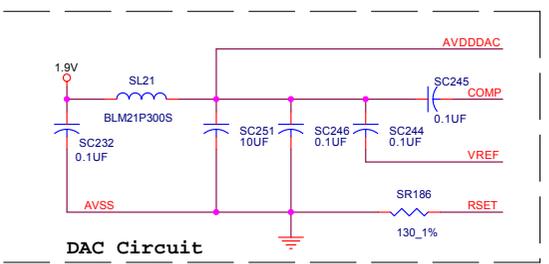
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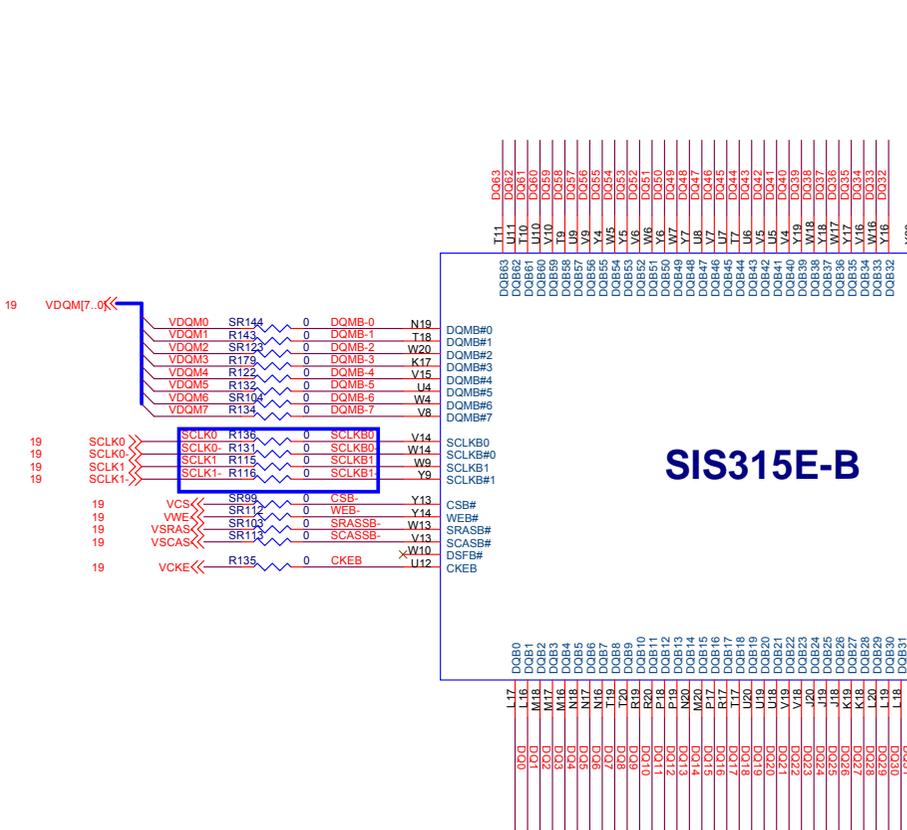
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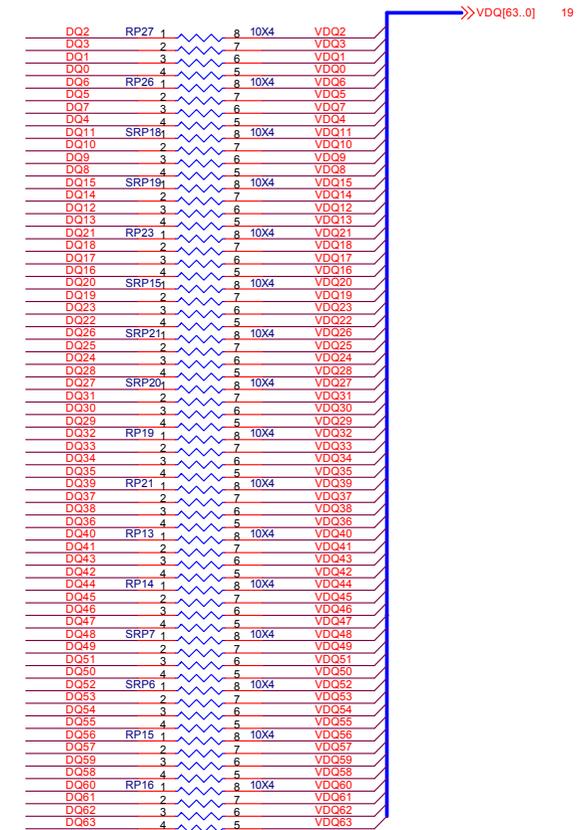
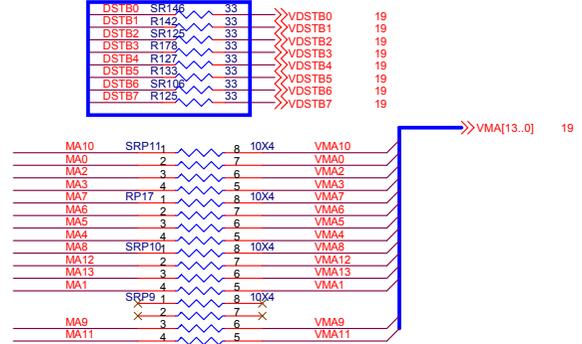
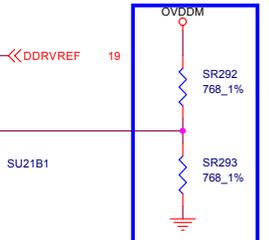
HW TRAPPING

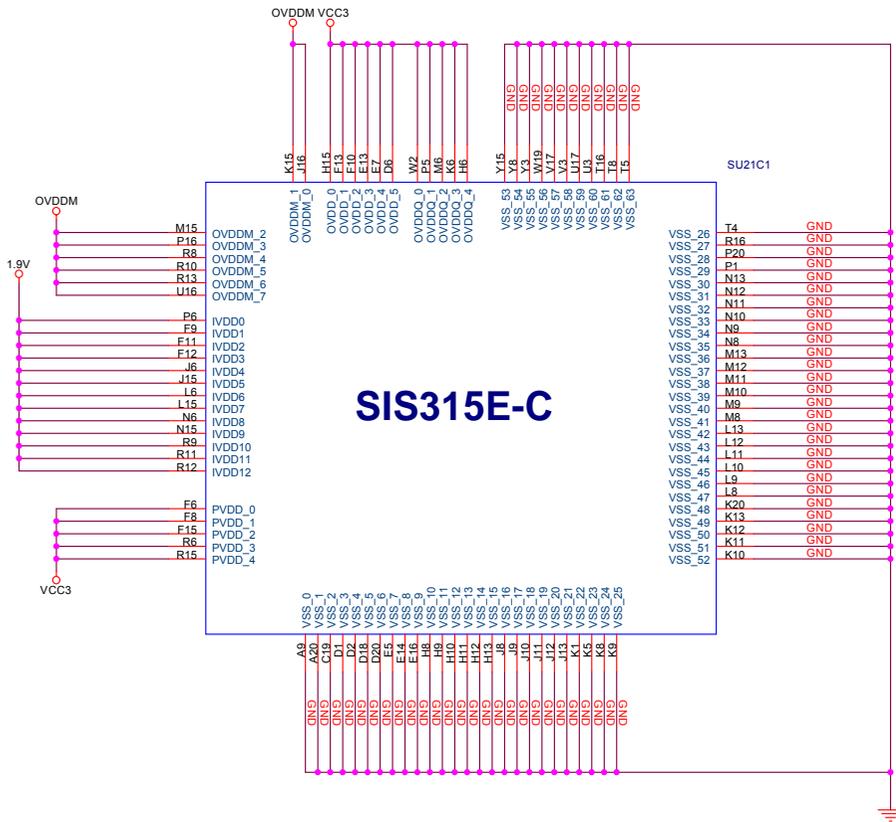
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		1	PAL TV OUT
ROMMA[2:1]	:	00	64KB ROM DECODING
		01	32KB ROM DECODING
		10	128KB ROM DECODING
		11	DISABLE ROM DECODING
ROMMA[3]	:	0	INTA DISABLE
		1	INTA ENABLE
ROMMA[4]	:	0	SUB-SYSTEM ID AUTO-FETCH
		1	SUB-SYSTEM ID PROGRAMMABLE
ROMMA[5]	:	0	VIDEO BRIDGE DISABLE
		1	VIDEO BRIDGE ENABLE
ROMMA[6]	:	0	AGP VOLTAGE AUTO-DETECTION ENABLE
		1	AGP VOLTAGE AUTO-DETECTION DISABLE
ROMMA[7]	:	0	PCI FAST BACK-TO-BACK DISABLE
		1	PCI FAST BACK-TO-BACK ENABLE
ROMMA[8]	:	0	PCI MULTIPLE FUNCTION DISABLE
		1	PCI MULTIPLE FUNCTION ENABLE
ROMMA[9]	:	0	PCI MULTIPLE FUNCTION 0
		1	PCI MULTIPLE FUNCTION 1
ROMMA[10]	:	0	PCI DEVICE MEDIUM DECODING SPEED
		1	PCI DEVICE SLOW DECODING SPEED
ROMMA[11]	:	0	AGP I/O INTERFACE LOW DRIVING
		1	AGP I/O INTERFACE HIGH DRIVING
ROMMA[13:12]	:	00	PCI CLOCK DLL PARAMETER SELECTION
		01	
		10	
		11	
ROMMA[14]	:	0	AGP I/O INTERFACE LOW SLEW RATE
		1	AGP I/O INTERFACE HIGH SLEW RATE
ROMMA[15]	:	0	AGP SIDE-BAND FUNCTION ENABLE
		1	AGP I/O PIPE-LINE FUNCTION ENABLE
ROMMA[16]	:	0	Down 64K address of ROM
		1	Up 64K address of ROM
ROMMD[1:0]	:	00	SDRAM
		01	SGRAM
		10	DDR SDRAM
		11	DDOR SGRAM
ROMMD[2]	:	0	AGP interface voltage 3.3V
		1	AGP interface voltage 1.5V
ROMMD[3]	:	0	ACPI D2 enable
		1	ACPI D2 disable
ROMMD[5:4]	:	00	AGP2X MODE
		01	AGP 1X MODE
		10	AGP 4X MODE
		11	PCI MODE
ROMMD[6]	:	0	SELECT INTERNAL CLOCK GENERATORS
		1	SELECT EXTERNAL CLOCK GENERATORS
ROMMD[7]	:	0	BCLK DLL ENABLE
		1	BCLK DLL DISABLE



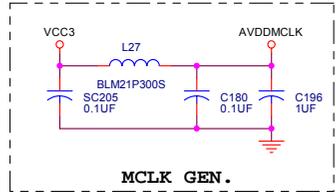


SIS315E-B

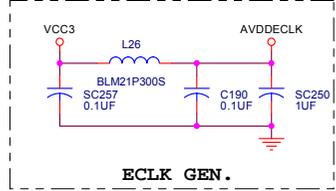




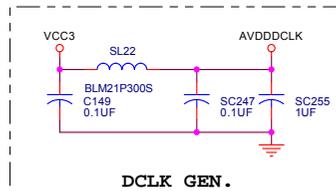
SIS315E-C



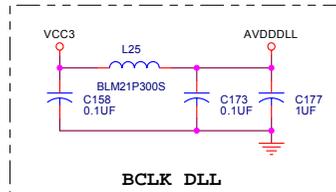
MCLK GEN.



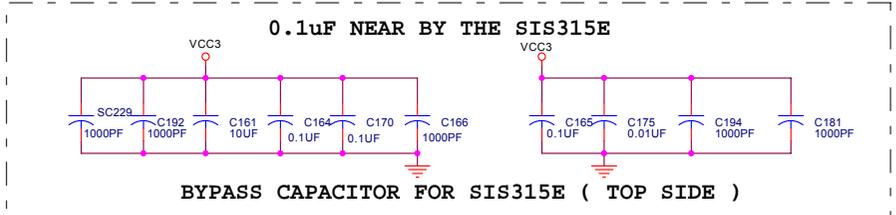
ECLK GEN.



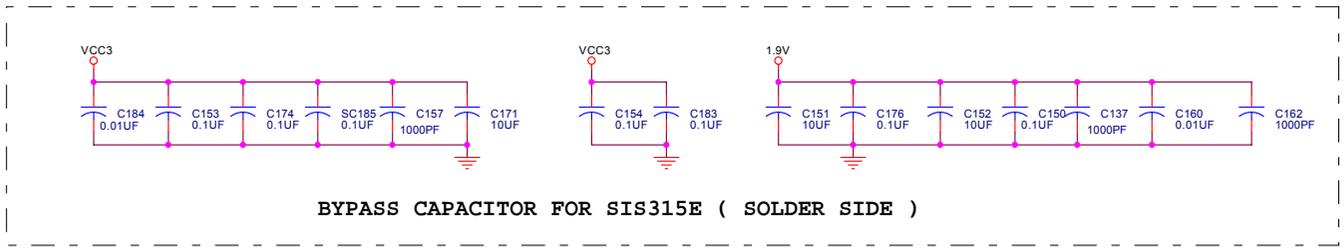
DCLK GEN.



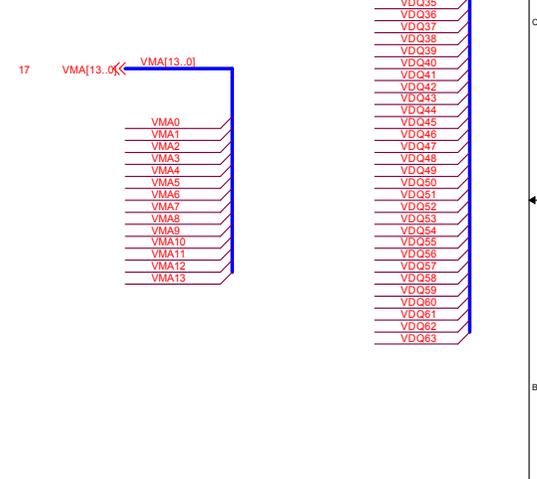
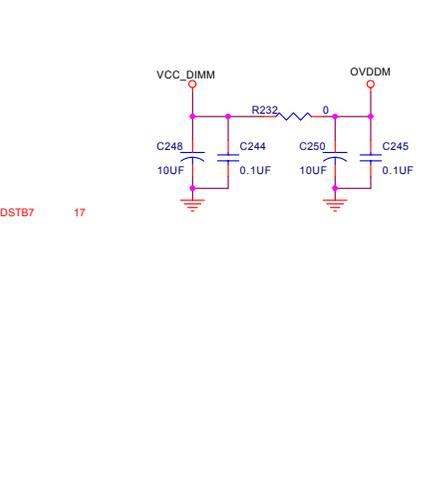
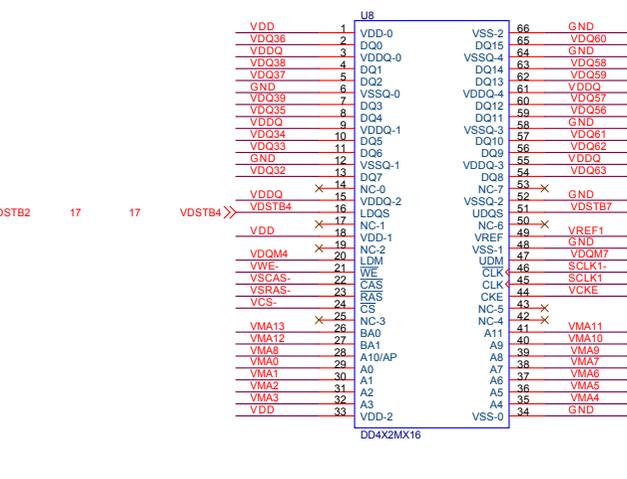
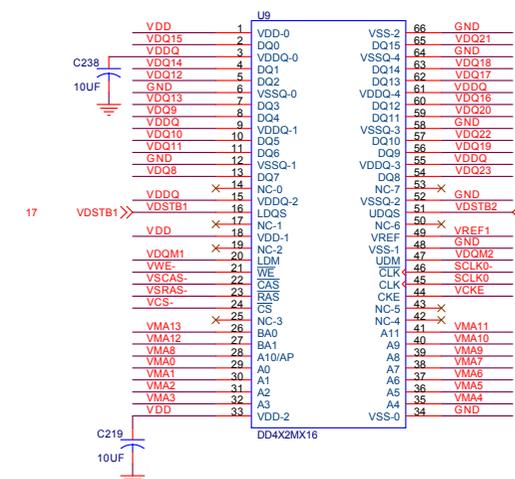
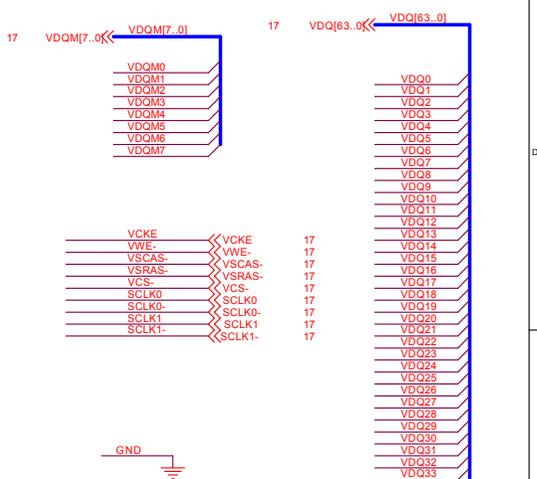
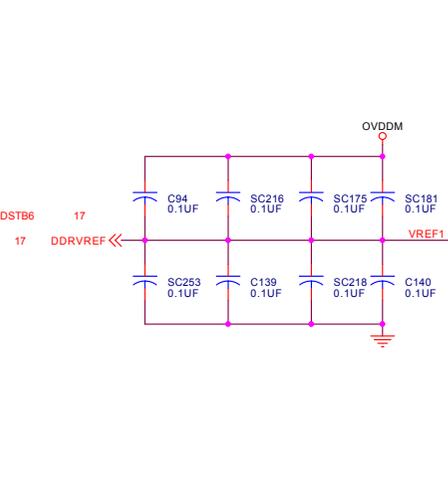
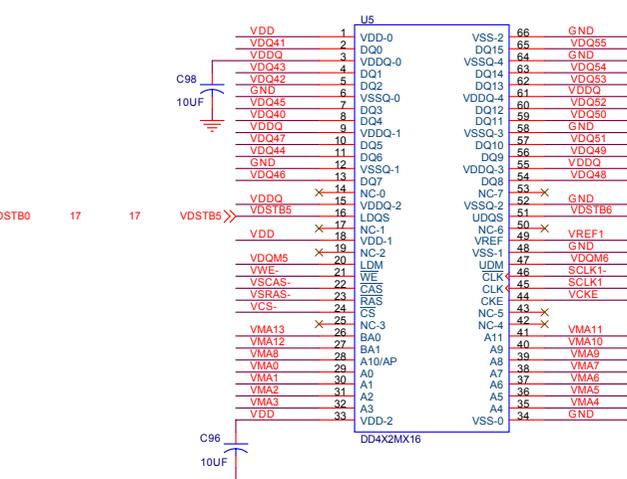
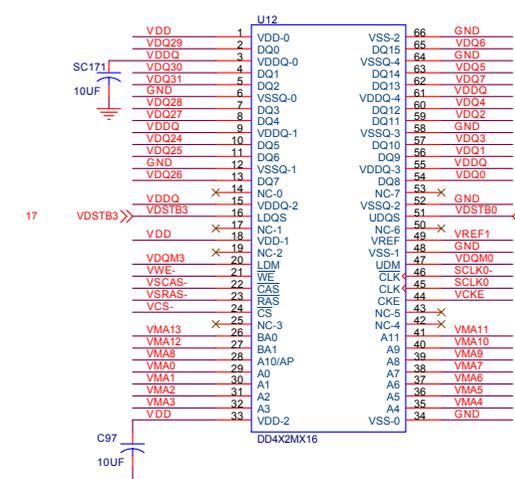
BCLK DLL



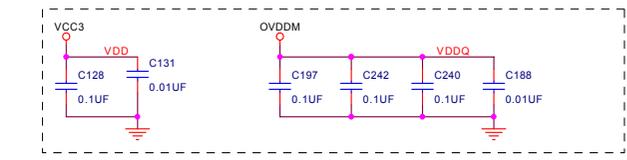
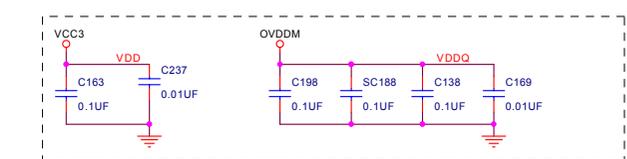
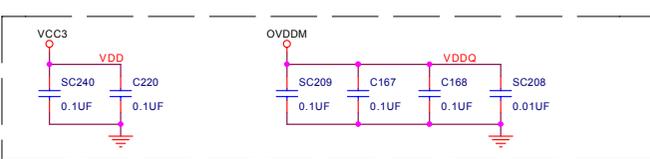
BYPASS CAPACITOR FOR SIS315E (TOP SIDE)



BYPASS CAPACITOR FOR SIS315E (SOLDER SIDE)



NEAR BY THE DDRSDRAM
Each Power pin of DDRSDRAM to add a bypass C



Elitegroup Computer Systems

Title: VIDEO MEMORY

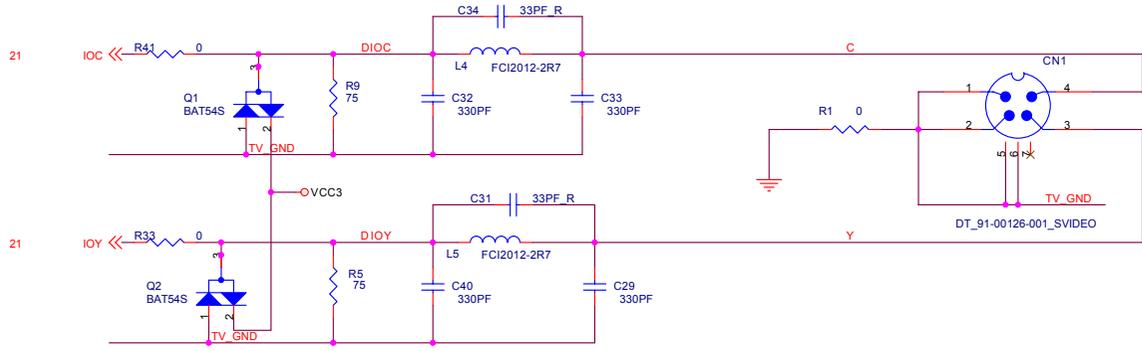
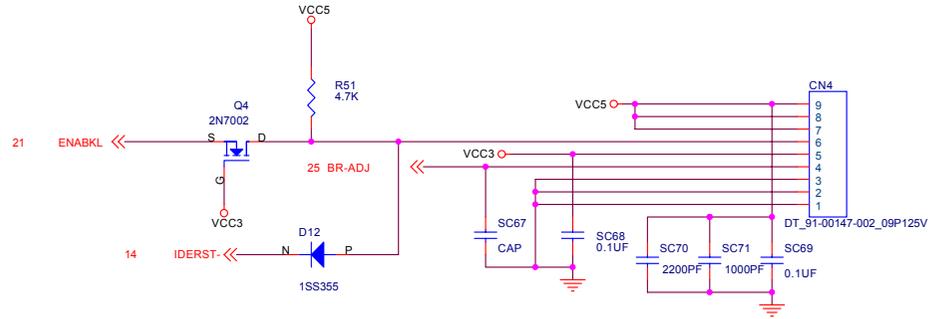
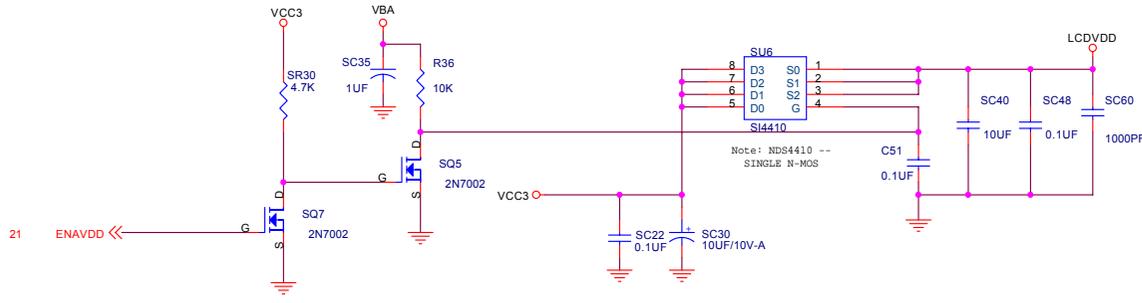
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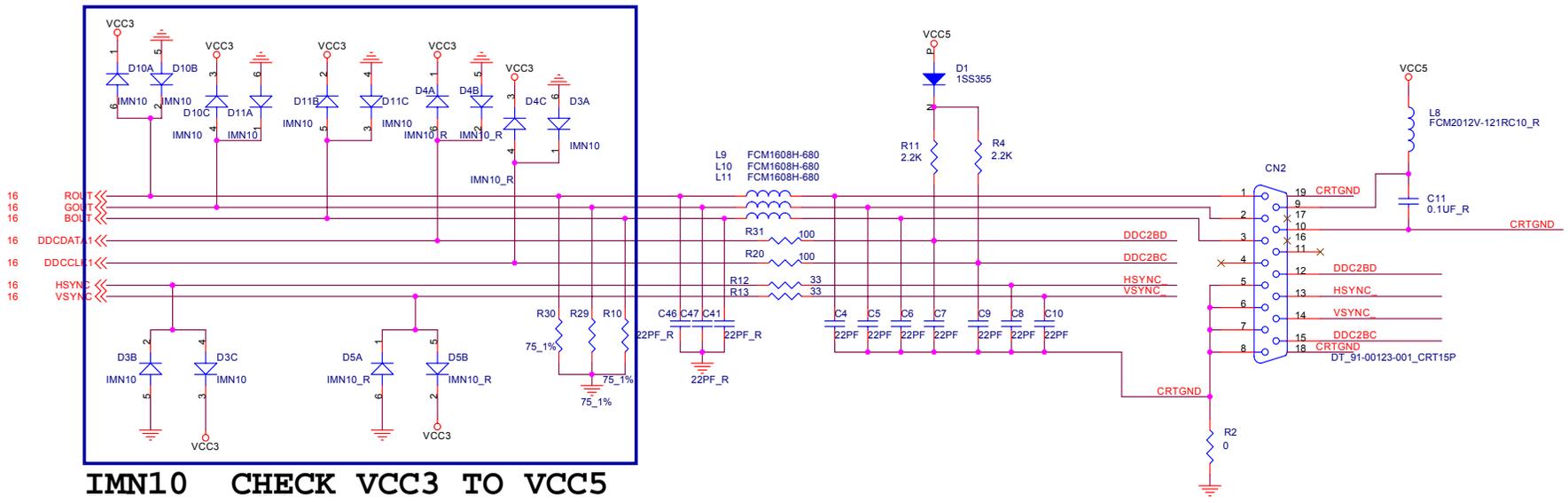
Document Number: A531-1-4-01

Date: Thursday, August 28, 2003

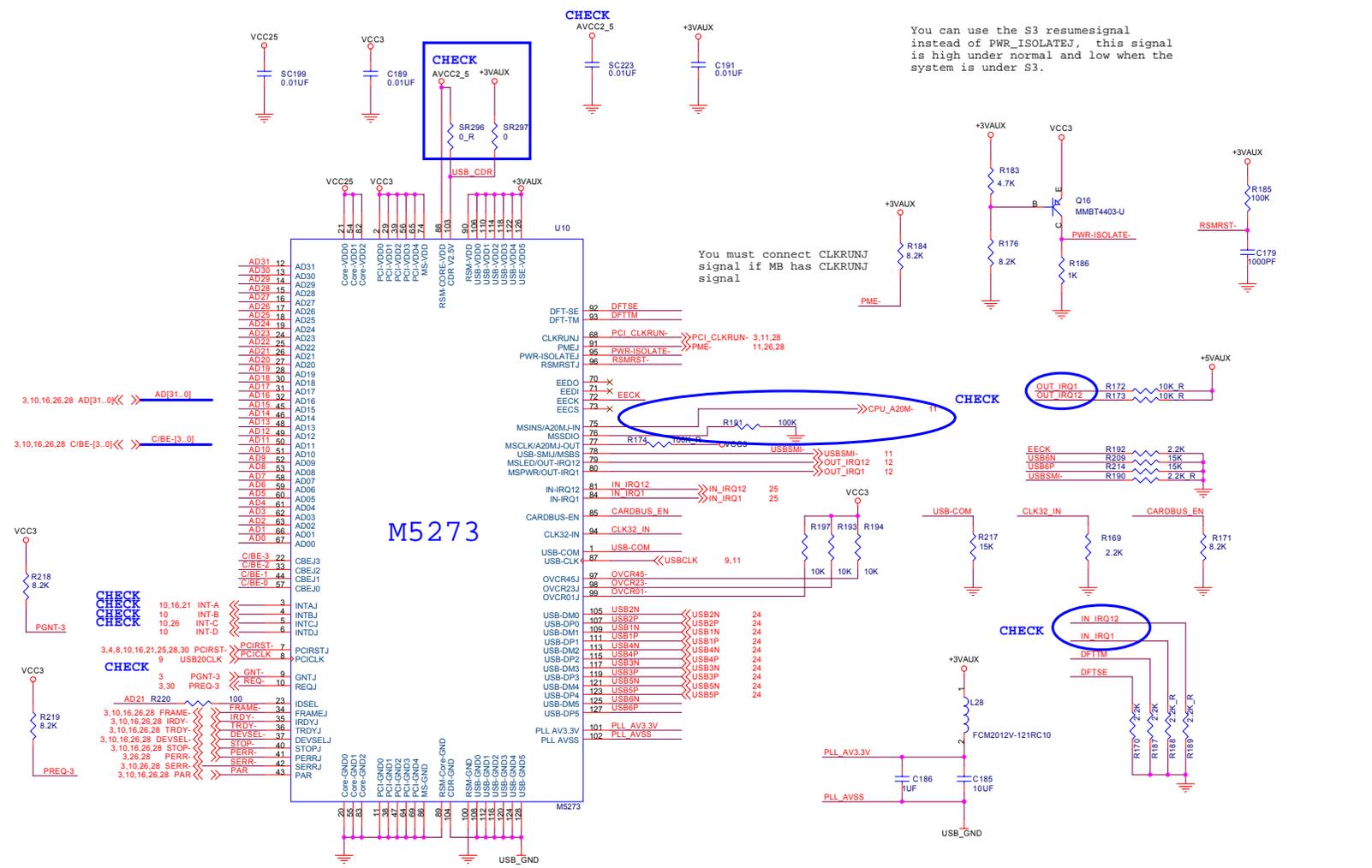
Sheet: 19 of 39

Rev: V1.0





IMN10 CHECK VCC3 TO VCC5



You can use the S3 resumesignal instead of PWR_ISOLATEJ, this signal is high under normal and low when the system is under S3.

You must connect CLKRUNJ signal if MB has CLKRUNJ signal

H/W Setting

OUT_IRQ1 (SW1.1)	OUT_IRQ12 (SW1.2)	Function
0	0	Disable OHCI 0.1.2
0	1	Enable OHCI 0
1	0	Enable OHCI 0.1
1	1	Enable OHCI 0.1.2

EECK (SW1.3)	Function
0	Disable eeprom
1	Enable eeprom

USB_SMIJ/MSBS (SW1.4)	Function
0	Enable MS
1	Enable Legacy

IDSEL	CARDBUS_EN	Function
IDSEL	0	Disable CARDBUS
1	1	Enable CARDBUS

M5273

3,10,16,26,28 ADJ[31..0] <<> ADJ[31..0]

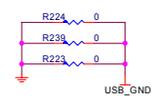
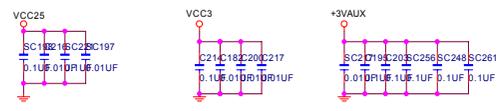
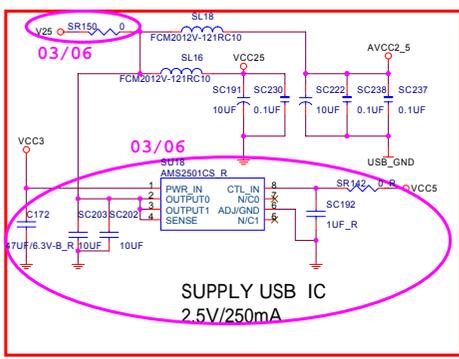
3,10,16,26,28 C/BE[13..0] <<> C/BE[13..0]

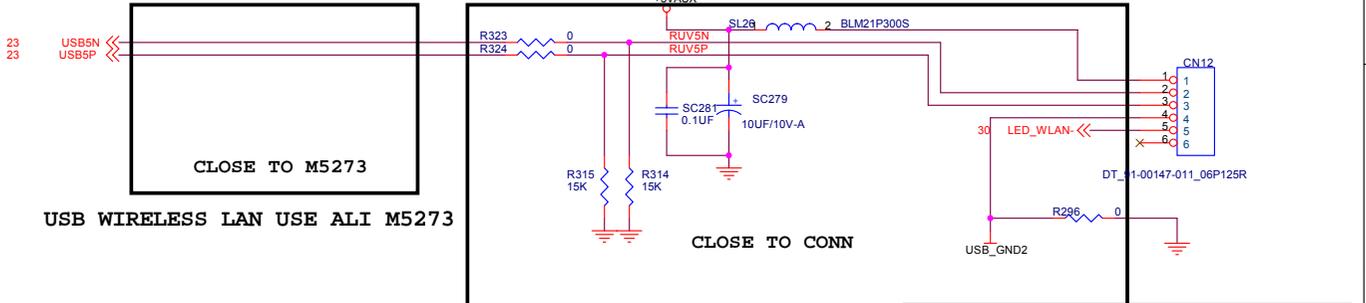
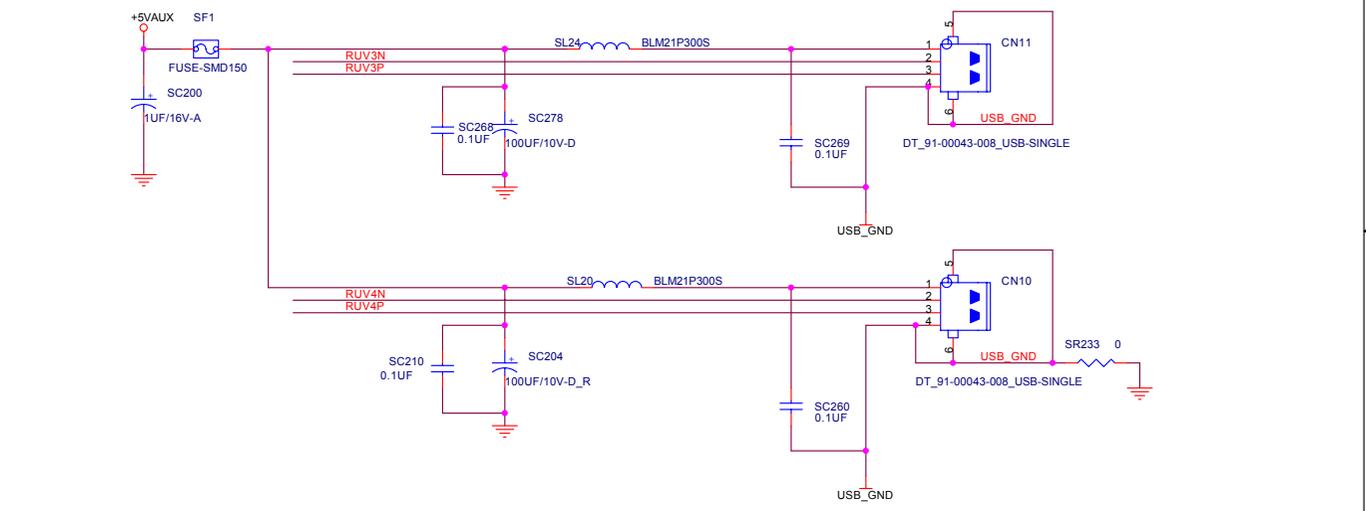
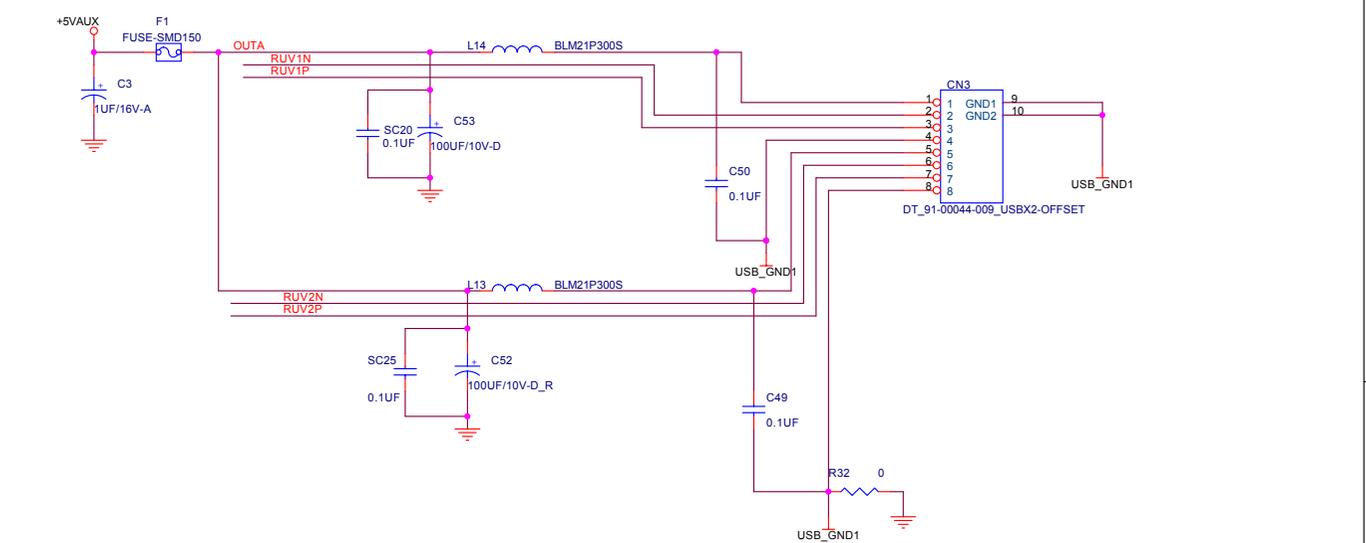
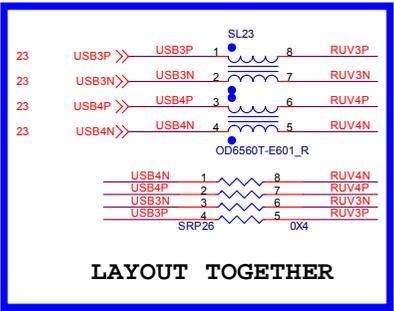
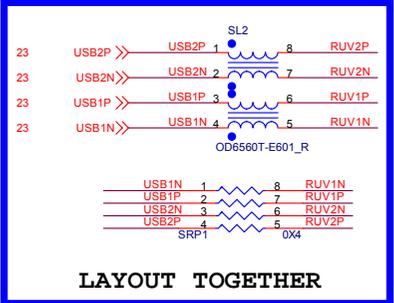
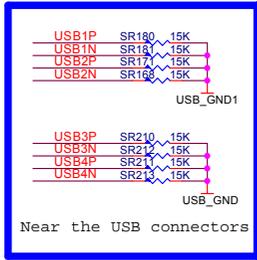
CHECK
CHECK
CHECK
CHECK

CHECK

CHECK

CHECK





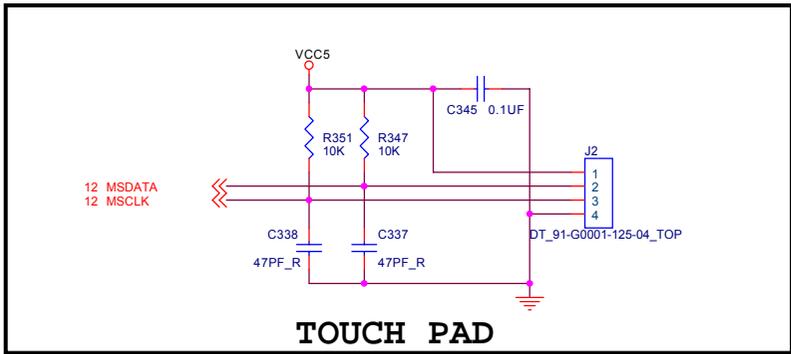
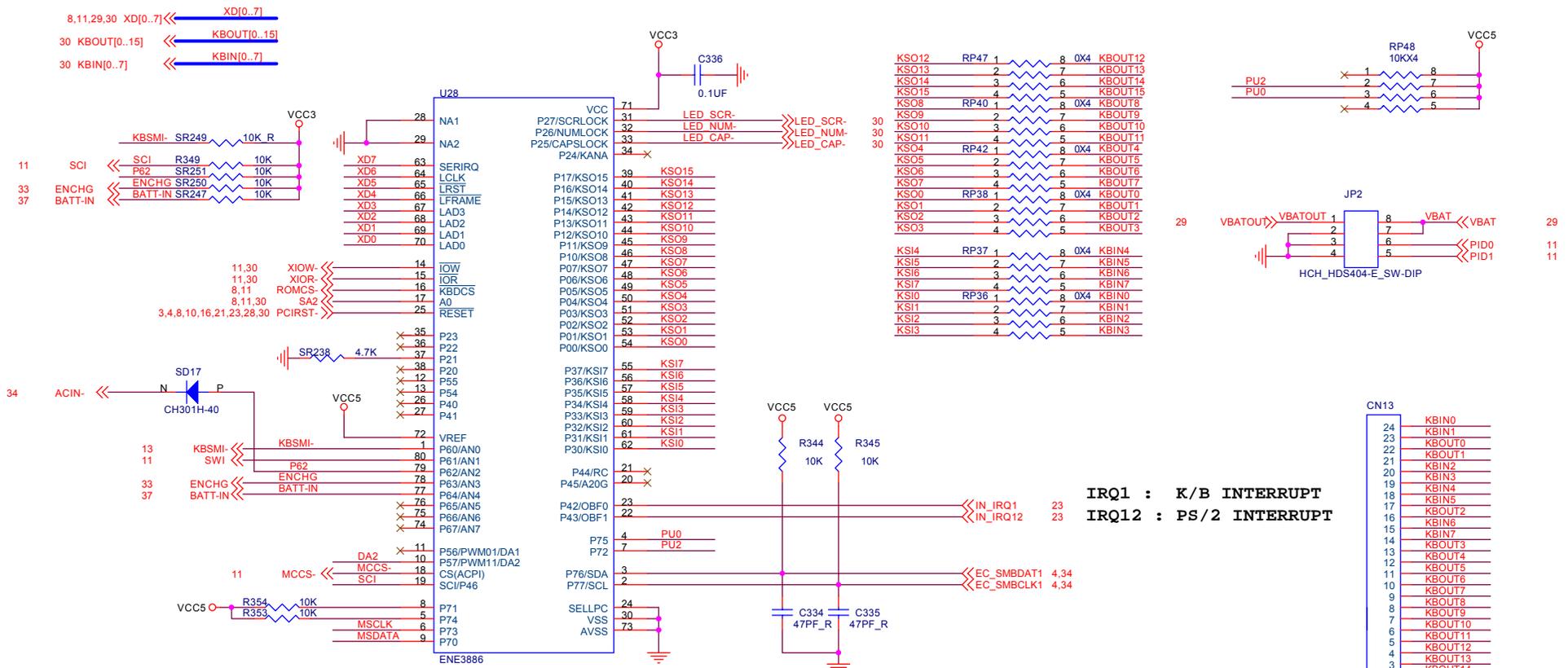
23 USB5N <<<

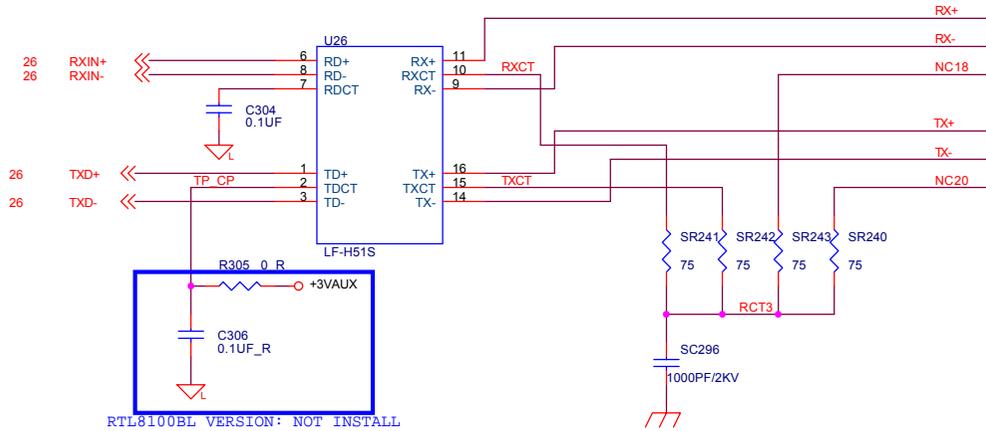
23 USB5P <<<

CLOSE TO M5273

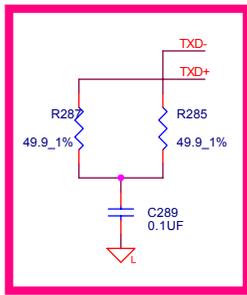
USB WIRELESS LAN USE ALI M5273

CLOSE TO CONN

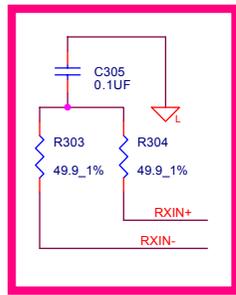




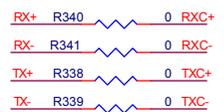
RTL8100BL VERSION: NOT INSTALL



PLACED CLOSELY TO THE RTL8100B(L)

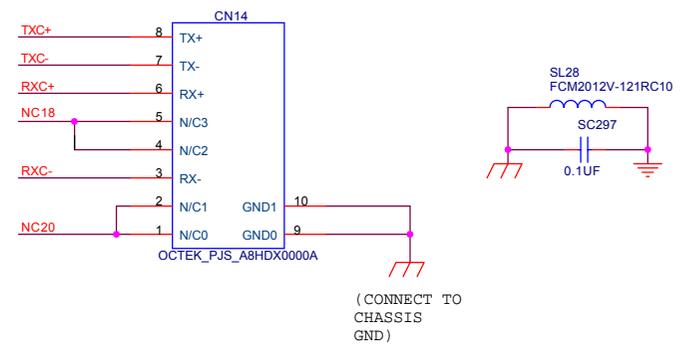


PLACED CLOSELY TO THE 10/100M MAGNETIC



Config:

Enable: N-way, Full duplex, 100Mbps, Link Down Power Saving
 Disable: Isolate, Repeater Mode

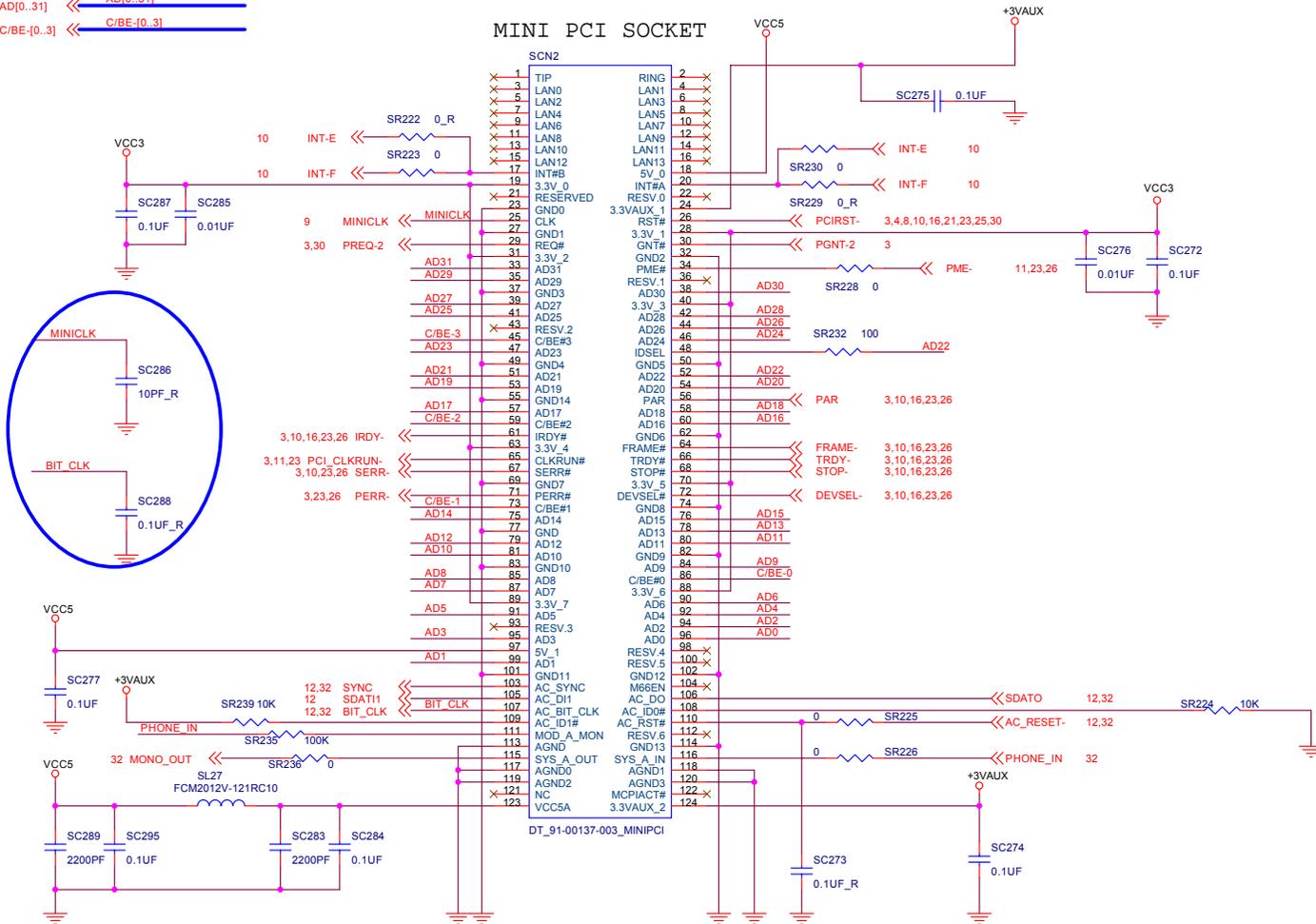


Elitegroup Computer Systems

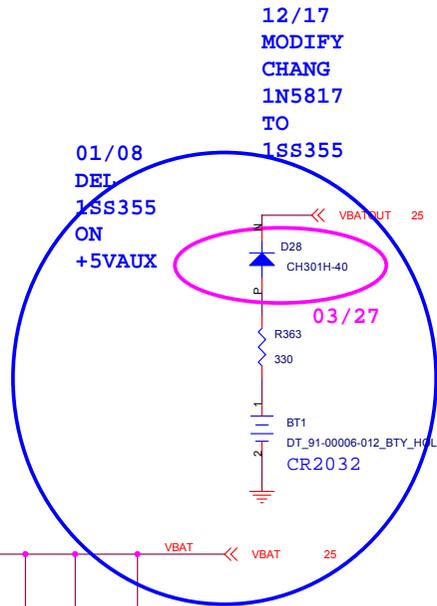
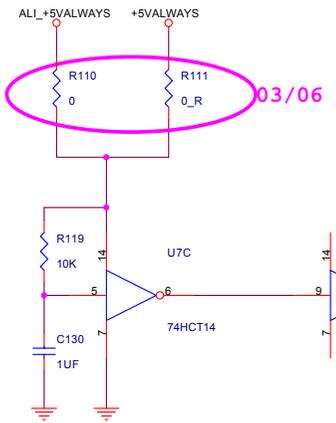
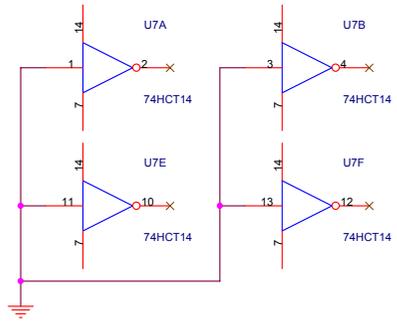
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RJ45		
Size	Document Number	Rev
Custom	A531-1-4-01	V1.0
Date:	Thursday, August 28, 2003	Sheet 27 of 39

3,10,16,23,26 AD[0..31] << AD[0..31]
 3,10,16,23,26 C/BE-[0..3] << C/BE-[0..3]

MINI PCI SOCKET



12/17
 MODIFY
 CHANGE
 CAP. TO
 RESERVE

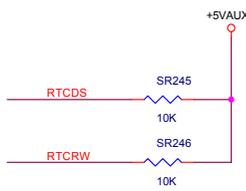
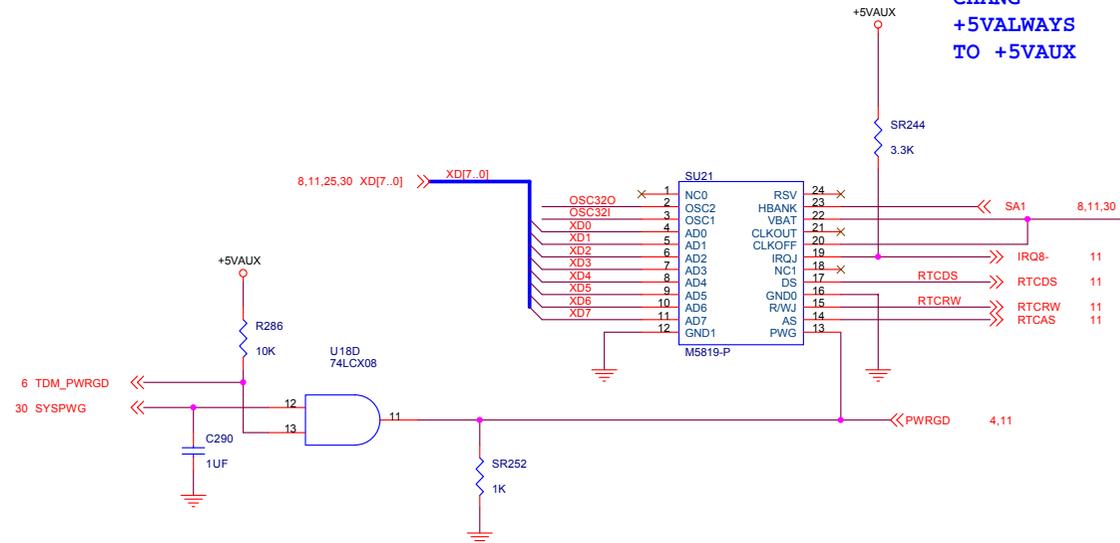


12/17
MODIFY
CHANG
1N5817
TO
1SS355

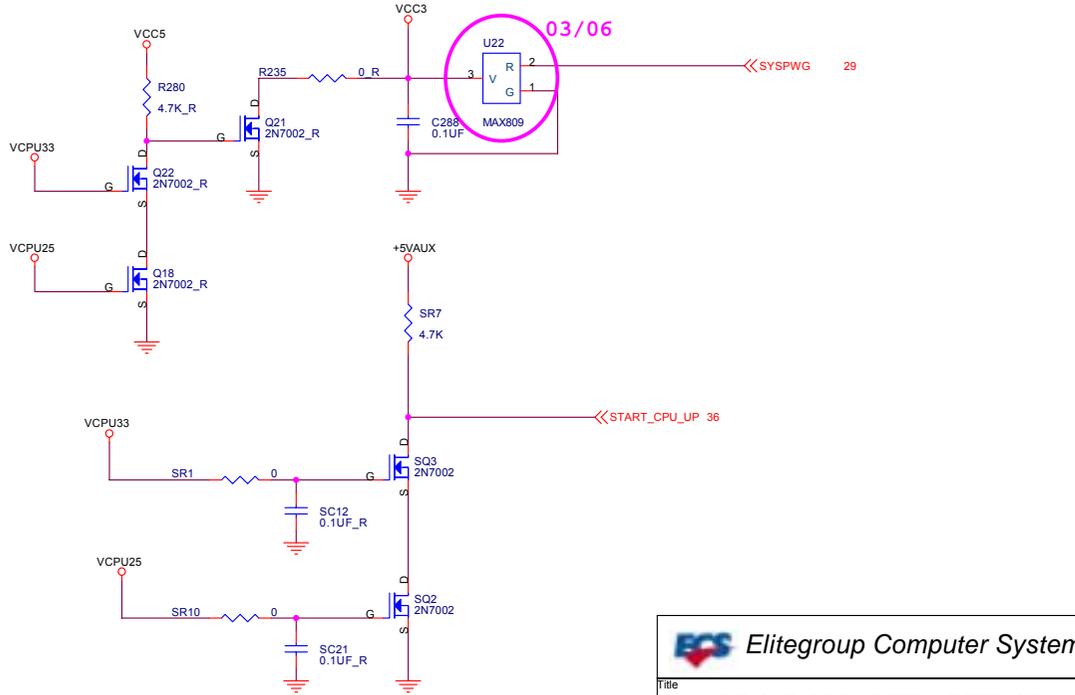
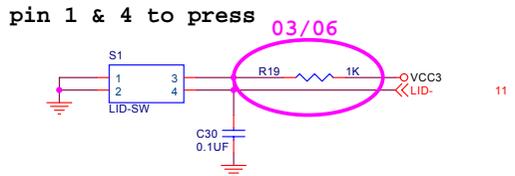
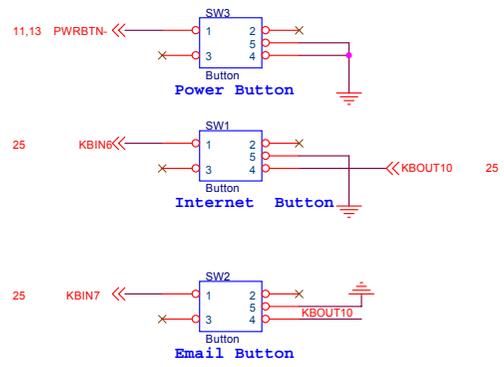
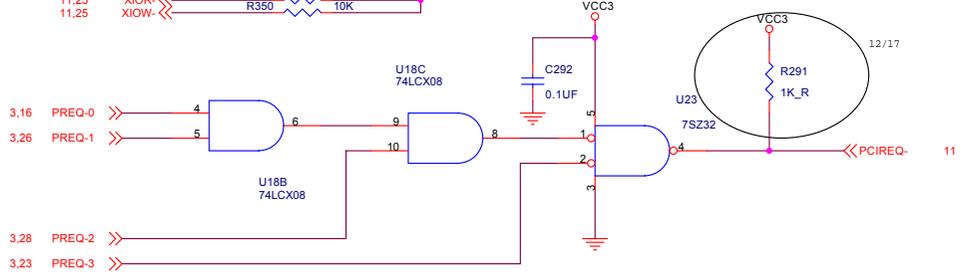
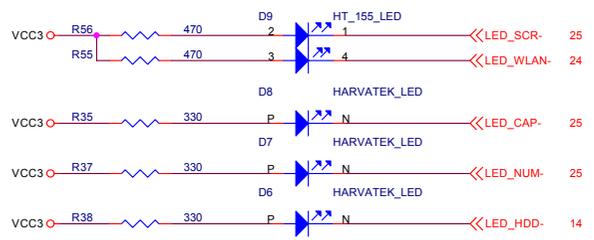
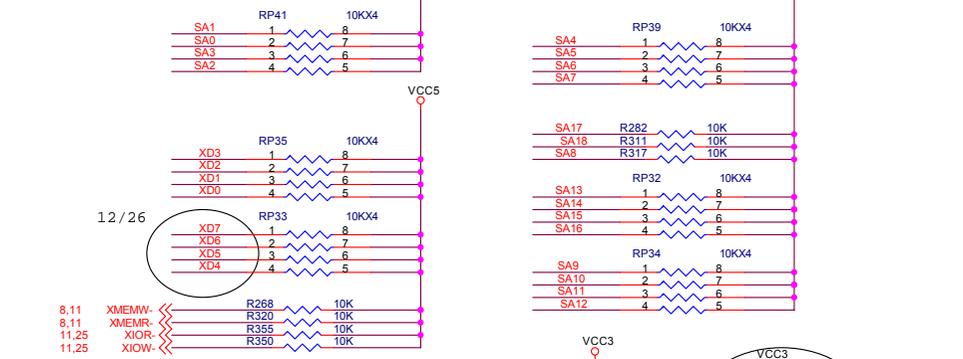
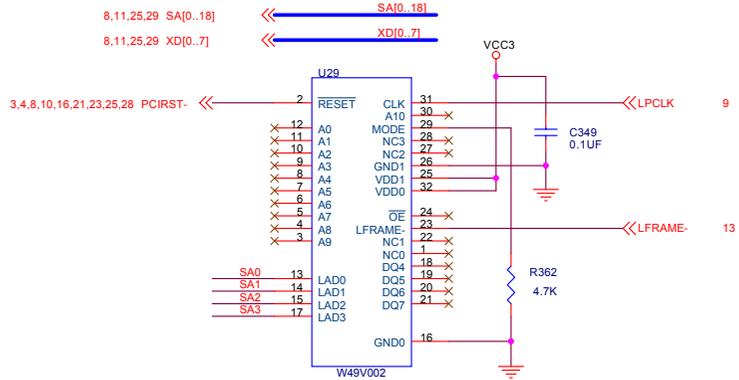
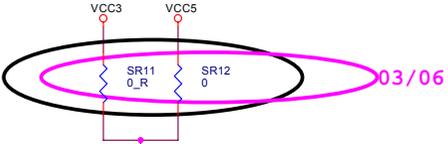
01/08
DEL
1SS355
ON
+5VAUX

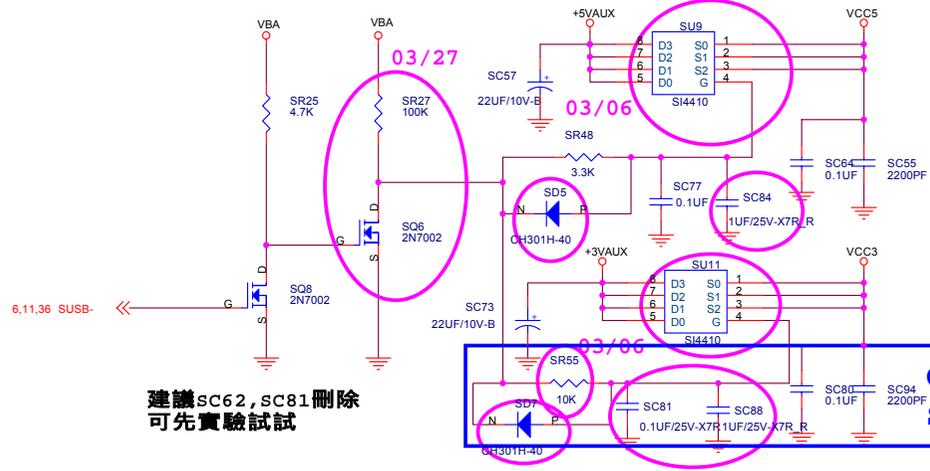
01/08
MODIFY
CHANG
+5VALWAYS
TO +5VAUX

VBATOUT-VBAT = NORMAL
VBAT-GND = CLEAR CMOS



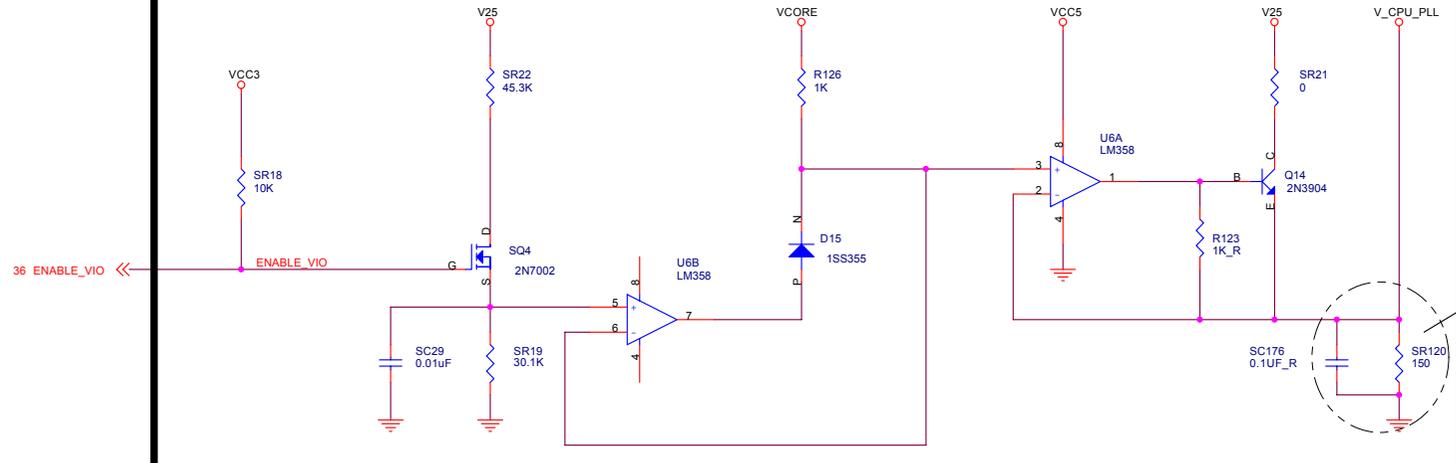
FOR LPC USED



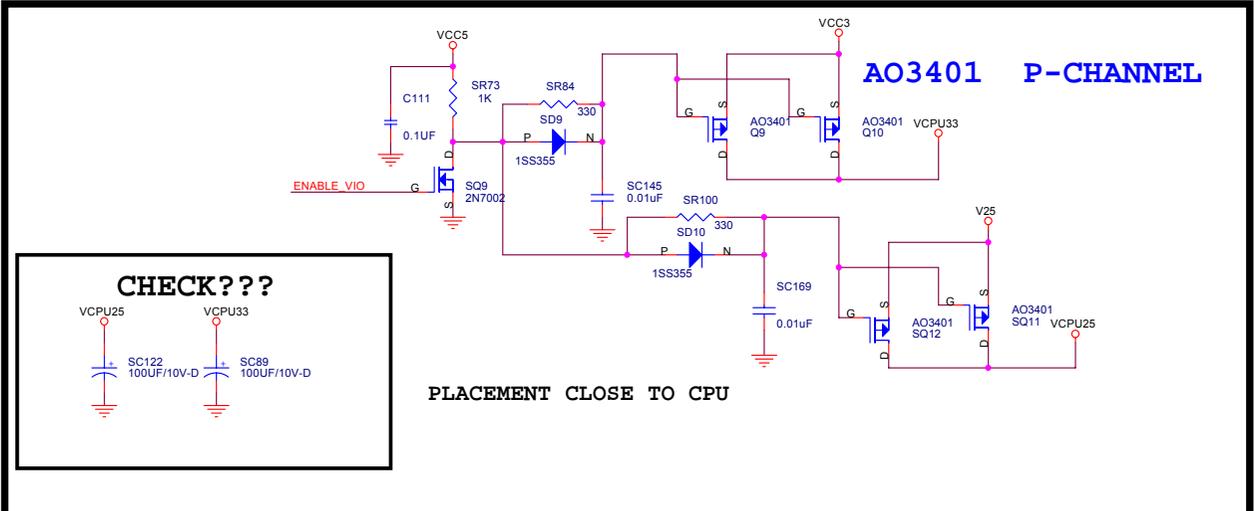


建議SC62, SC81刪除
可先實驗試試

**CHANGE
SC81, SC88, SR55**



CLOSE TO CPU SIDE



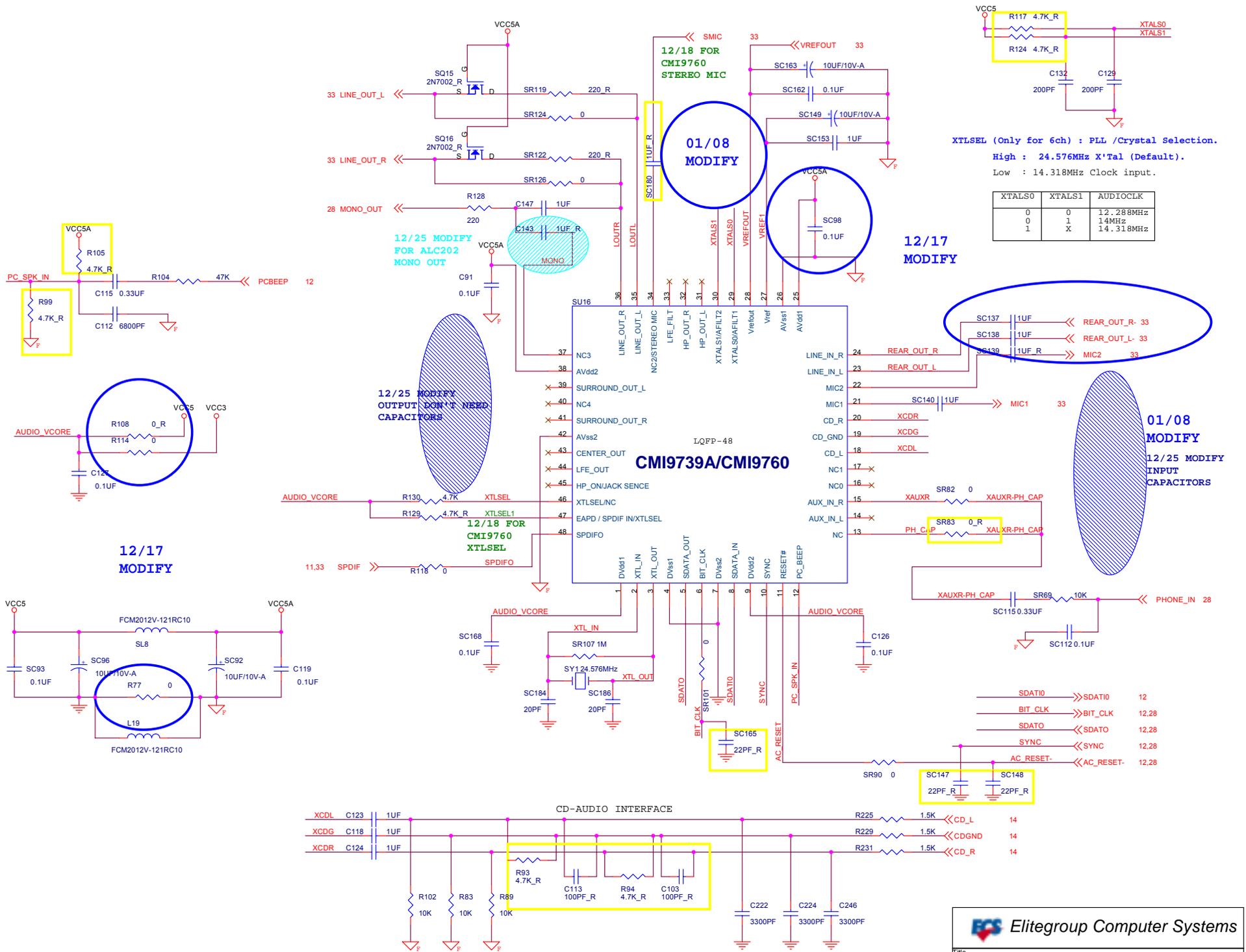
CHECK???

VCPU25 VCPU33

SC122 SC88

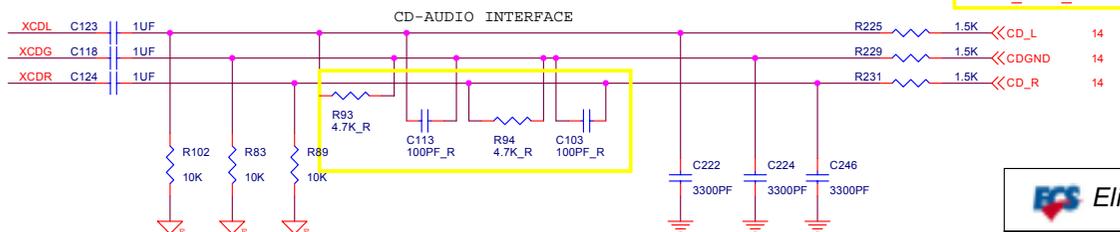
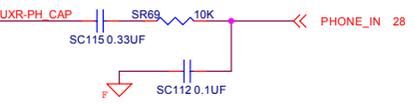
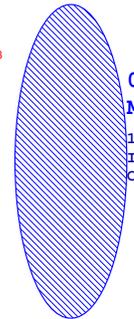
100UF/10V-D 100UF/10V-D

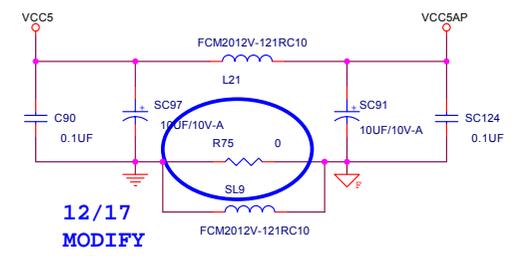
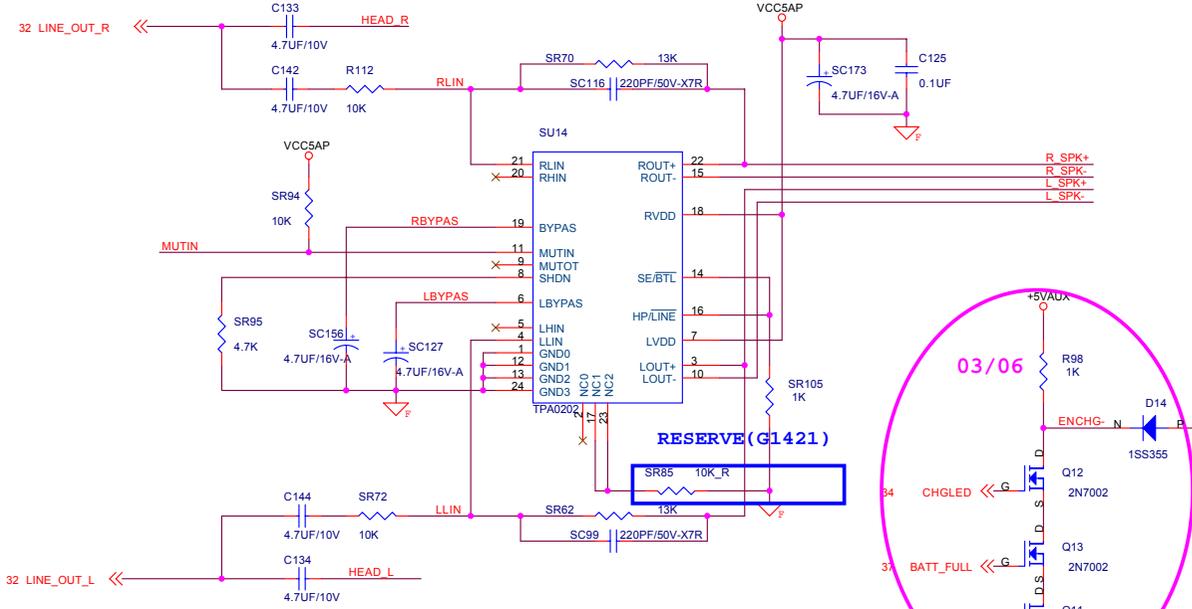
PLACEMENT CLOSE TO CPU



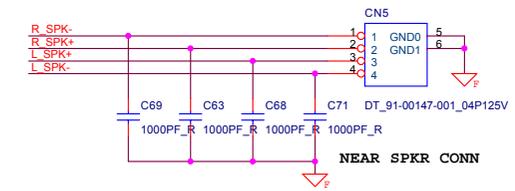
XTLSEL (Only for 6ch) : PLL /Crystal Selection.
 High : 24.576MHz X'Tal (Default).
 Low : 14.318MHz Clock input.

XTALS0	XTALS1	AUDIOCLK
0	0	12.288MHz
0	1	14MHz
1	X	14.318MHz

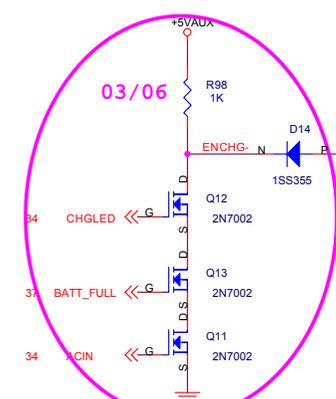




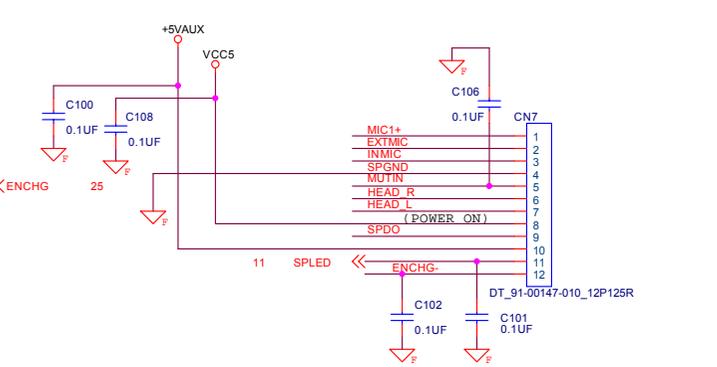
12/17
MODIFY



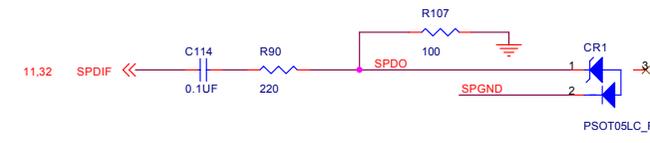
NEAR SPKR CONN



03/06



SPDO VOLTAGE ABOUT = 0.7V(RES. 390 OHM)
SPDO VOLTAGE ABOUT = 1V(RES. 220 OHM)

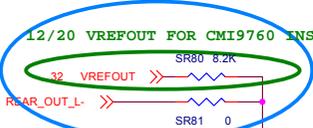


PC2001 SPEC. 12KHz--15KHz
 $F_c = 1 / [2 * 3.14 * R(2.7K) * C(4700PF)] = 12.548KHz$
VREFOUT CONTROL MIC & REAR_OUT_R/L FUNCTION

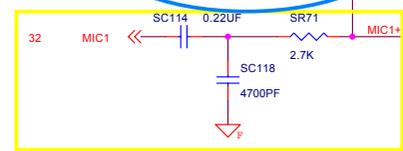
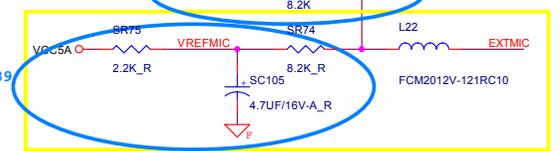
12/18 STEREO MIC FOR CMI9760



12/18 REAR_OUT_L- FOR 4CH

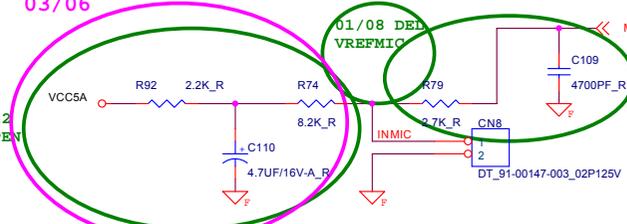


12/20 VREFOUT FOR 4CH



03/06

12/20 R963, R964, C1042 FOR CMI9760 OPEN



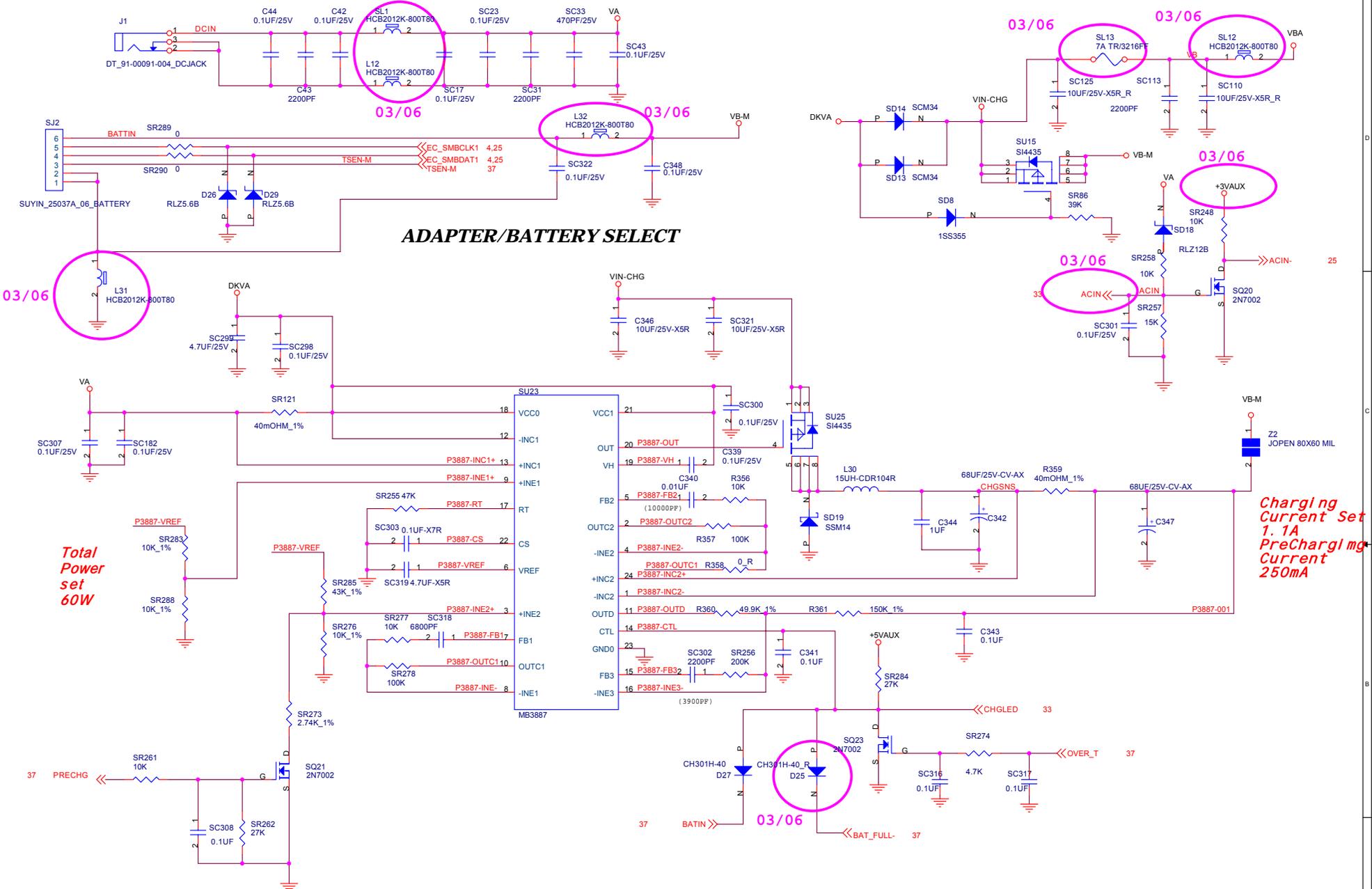
12/20 MIC2 FOR 2 FUNCTION

Elitegroup Computer Systems

Title: **OPA & AUDIO JACK**

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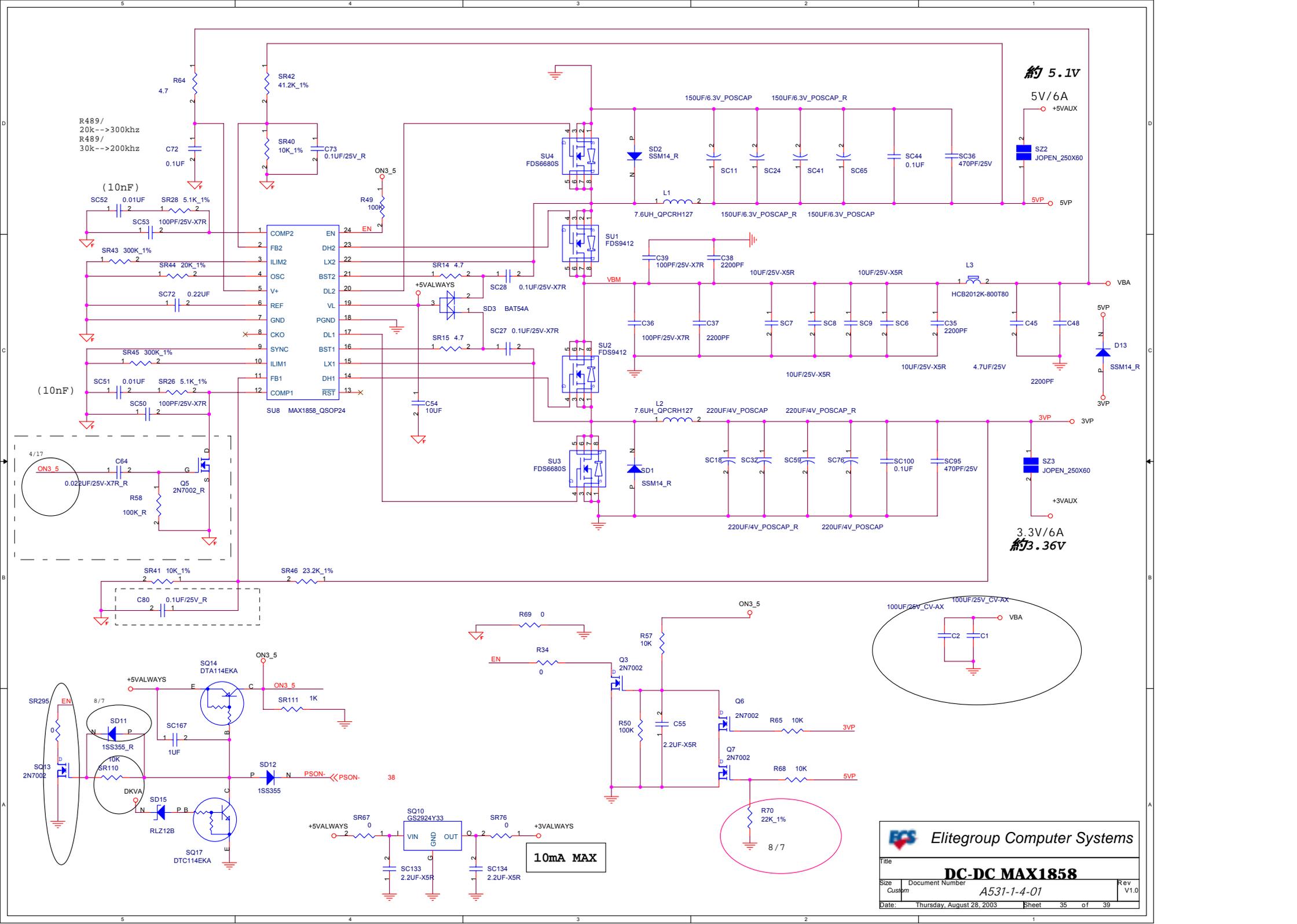


ADAPTER/BATTERY SELECT

CHARGE

Total Power set 60W

Charging Current Set 1.1A
PreCharging Current 250mA



約 5.1V

5V/6A

+5VAUX

SZ2 JOPEN_250X60

5VP 5VP

VBA

5VP

3VP

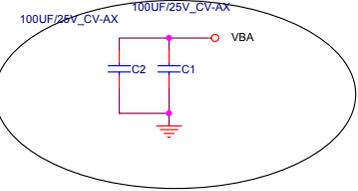
+3VAUX

SZ3 JOPEN_250X60

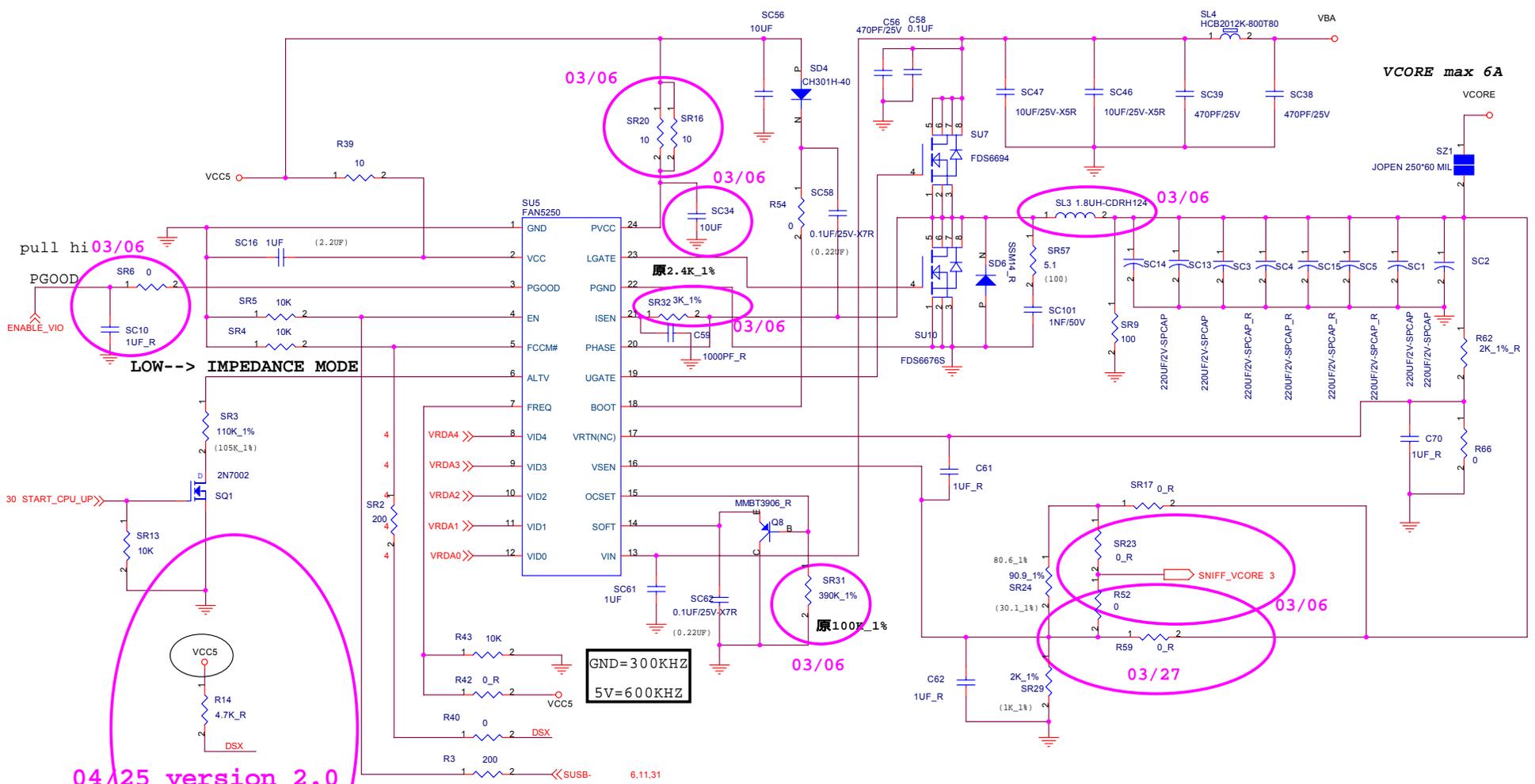
3.3V/6A

約 3.36V

10mA MAX



Title		
DC-DC MAX1858		
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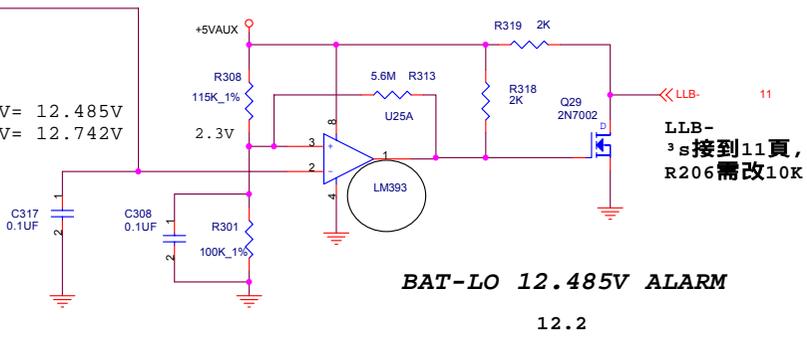
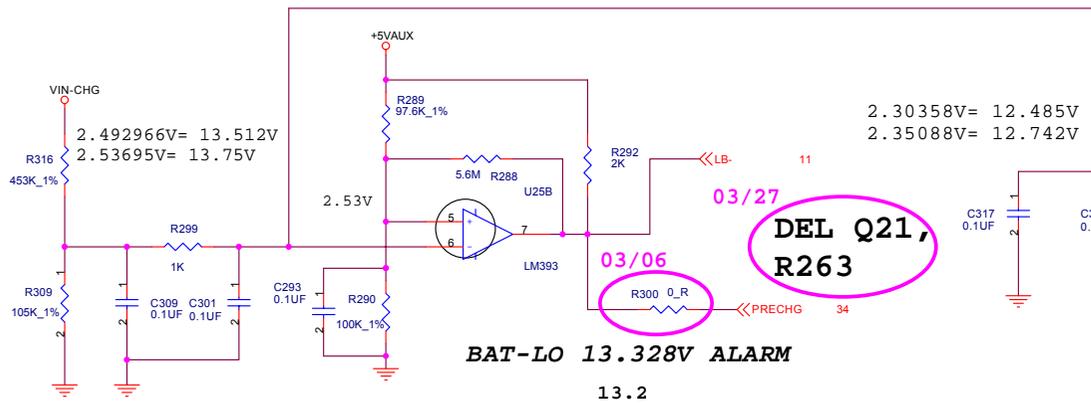
VCORE max 6A

pull hi 03/06
 PGOOD
 ENABLE_VIO
 LOW--> IMPEDANCE MODE

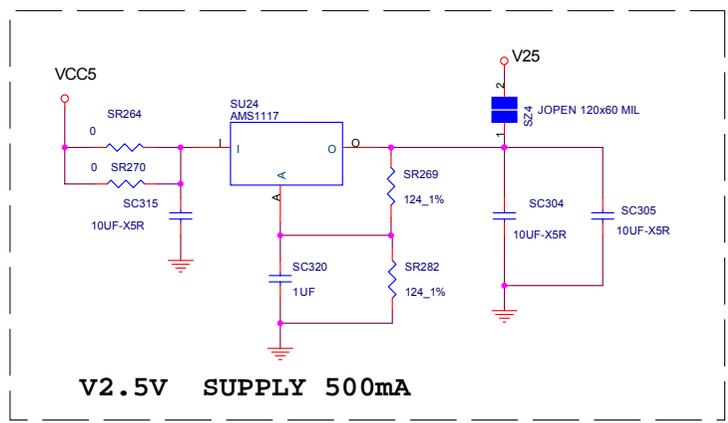
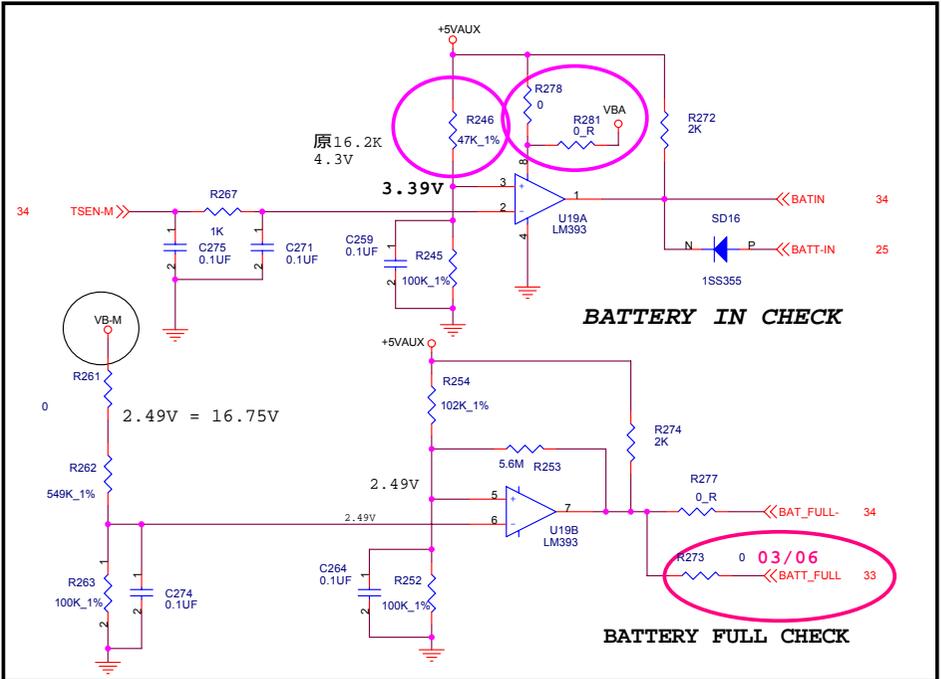
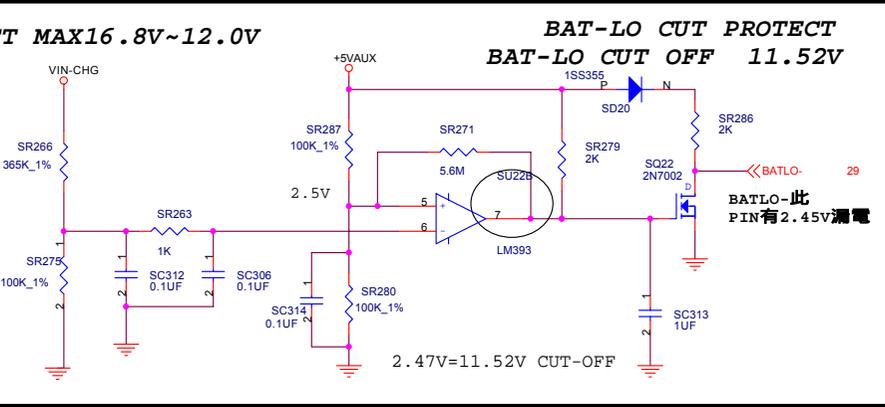
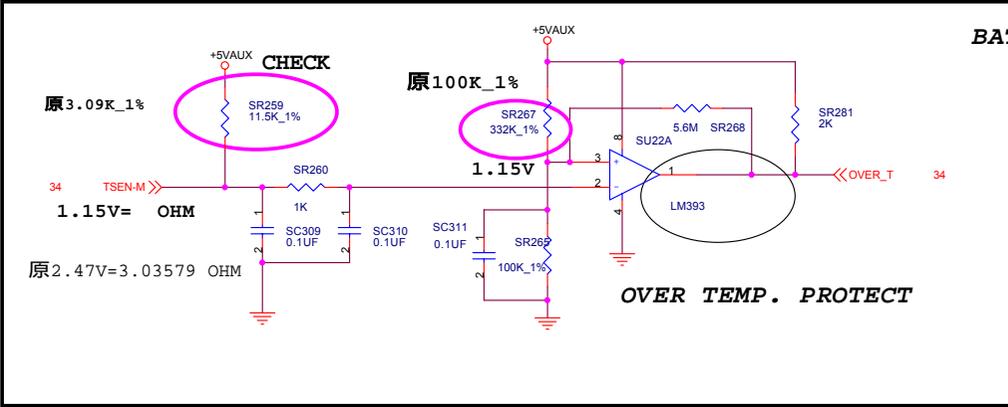
30 START_CPU_UP
 VCC5
 DSX
 04/25 version 2.0

STAR=ON VOUT=1.05V
 DSX=ON VOUT=0.9V

GND=300KHZ
 5V=600KHZ



LLB-
3s 接到11頁,
R206需改10K



T	MAX	TYP	MIN
0C-->	27.844K	27.303K	26.974K
5C -->	22.442K	22.075K	21.727K
25C-->	10.1k	10.0k	9.9k
55C-->	3.6k	3.54k	3.463k
60C-->	3.083k	3.0215k	2.9536k

A531 HISTORY

A531_VERSION B

- 01.PAGE 2 change SR129,SR130,SR128,SR127 RESISTER VALUE (10--->0 OHM)
- 02.PAGE 2 change R156,R140,SR92,R109,SR96,SR108,SR137,SR133,R164,
R154,R152,R161,R163,R155,R141,SR97,R113,SR91,SR102,SR132,SR134
RESISTER VALUE (33--->10 OHM)
- 03.PAGE 6 MODIFY U27 SCHEMATIC
- 04.PAGE 17 MODIFY SU21B1 SCHEMATIC (DDRVREF AND ADD RESISTER)
- 05.PAGE 25 MODIFY U14 SCHEMATIC (NET DA2)
- 06.PAGE 35 DELLETE D13,SD11 AND MODIFY SCHEMATIC SD11
- 07.PAGE 35 ADD R70 22K AND SR295 0

 Elitegroup Computer Systems		
Title		
HISTORY		
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