

Page	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20
Rev.	B.0																			
Data	2004/10/13	2004/10/13	2004/10/13	2004/10/13	2004/10/13	2004/10/13	2004/10/13	2004/10/13	2004/10/13	2004/10/13	2004/10/13	2004/10/13	2004/10/13	2004/10/13	2004/10/13	2004/10/13	2004/10/13	2004/10/13	2004/10/13	2004/10/13

Page	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37
Rev.	B.0																
Data	2004/10/13	2004/10/13	2004/10/13	2004/10/13	2004/10/13	2004/10/13	2004/10/13	2004/10/13	2004/10/13	2004/10/13	2004/10/13	2004/10/13	2004/10/13	2004/10/13	2004/10/13	2004/10/13	2004/10/13

**Elitegroup Computer Systems**

File: **BLOCK DIAGRAM**

Size: C Document Number: **558-1-4-01** Rev: B.0

Date: Thursday, October 14, 2004 Sheet 1 of 37

Voltage Rails	ON S0-S1	ON S3	ON S4	ON S5	Control signal
12VOUT	X	X	X	X	
3V_59T	X	X	X	X	
5VPCU	X	X	X	X	
+3V_S5	X	X	X	X	SS_ON
+1.5V_S5	X	X	X	X	SS_ON
+1.8V/SUS	X	X			SUSON
+3V/SUS	X	X			SUSON
+4V/SUS	X	X			SUSON
+0.8V/SUS	X	X			SUSON
GPU_CORE	X				VR_ON
+0.5V	X				MAINON
+1VSCP	X				MAINON
+1.5V	X				MAINON
+1.8V	X				MAINON
+2.5V	X				MAINON
+3V	X				MAINON
+5V	X				MAINON
+12V	X				MAINON

### External PCI Devices

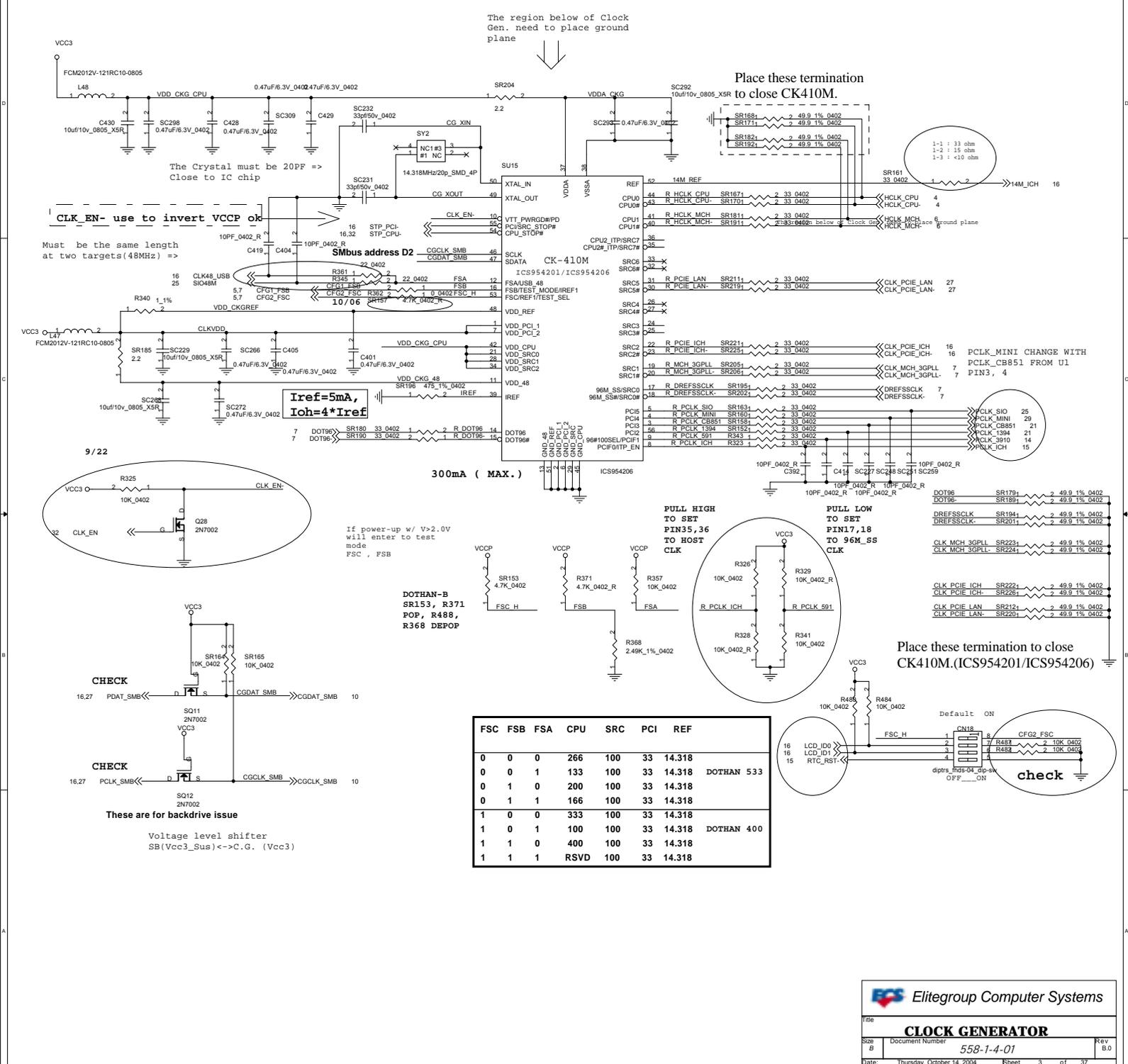
Device	IDSEL#	REQ#GNT#	Interrupts
CardBus+1394	AD17	1	PIRODC
Mini-PCI	AD19	2	PIROBD

### EC SM Bus1 address

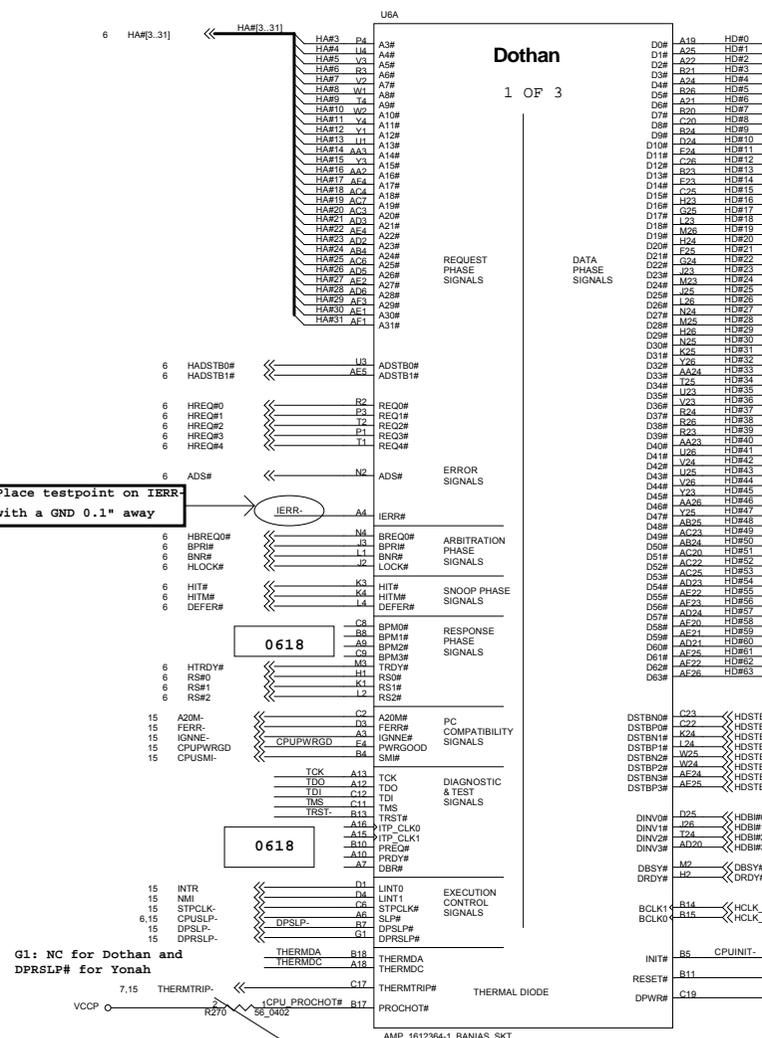
**Device**  
Smart Battery  
THERMAL SENSOR

### ICH4-M SM Bus address

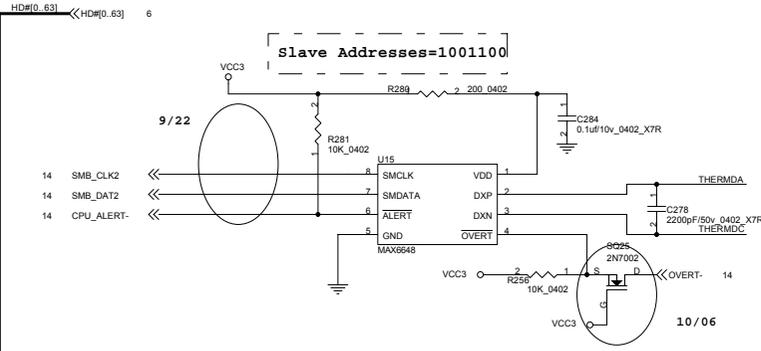
**Device**  
SDIMM           1010 000X b  
Clock Gen       1101 001x b



	FSC	FSB	FSA	CPU	SRC	PCI	REF
0	0	0	0	266	100	33	14.318
0	0	1	1	133	100	33	14.318
0	1	0	0	200	100	33	14.318
0	1	1	1	166	100	33	14.318
1	1	0	0	333	100	33	14.318
1	1	0	1	100	100	33	14.318
1	1	1	0	400	100	33	14.318
1	1	1	1	RSVD	100	33	14.318



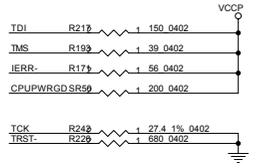
**Dothan**  
1 OF 3



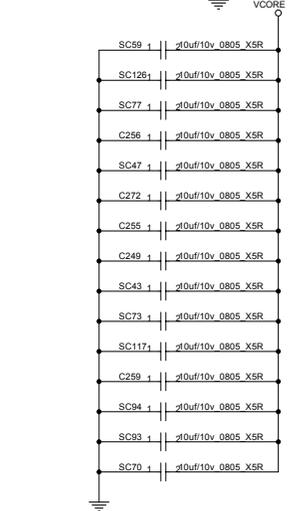
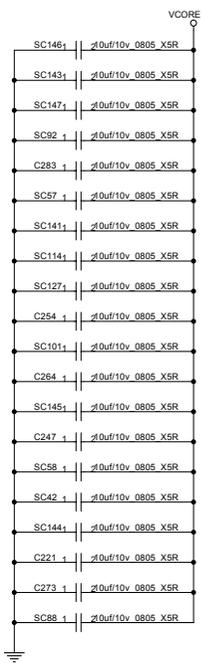
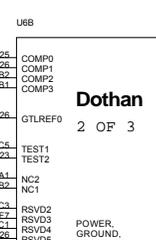
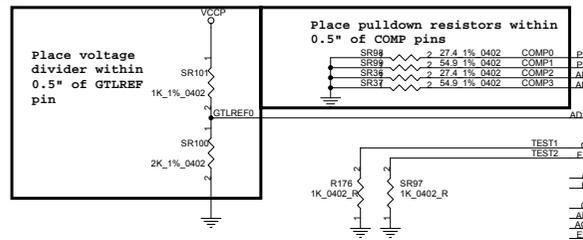
Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 ohm +/- 5%	VTT	Within 2.0" of the CPU
TMS	39 ohm +/- 5%	VTT	Within 2.0" of the CPU
TRST#	680 ohm +/- 5%	GND	Within 2.0" of the CPU
TCK	27 ohm +/- 5%	GND	Within 2.0" of the CPU
TDO	Open	NC	Within 2.0" of the CPU

Del R682 because no ITP  
Del R672 because no ITP

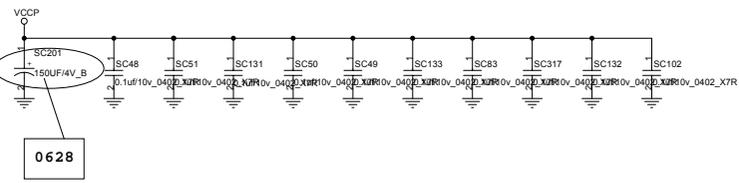
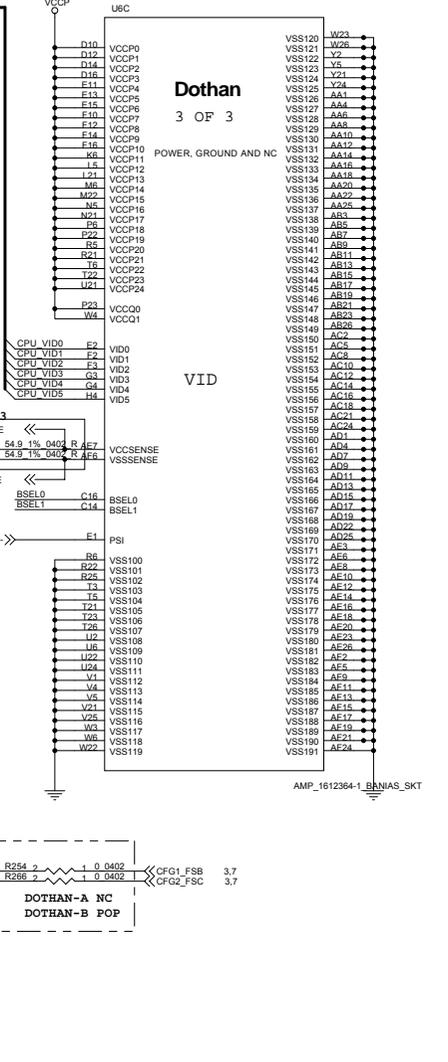
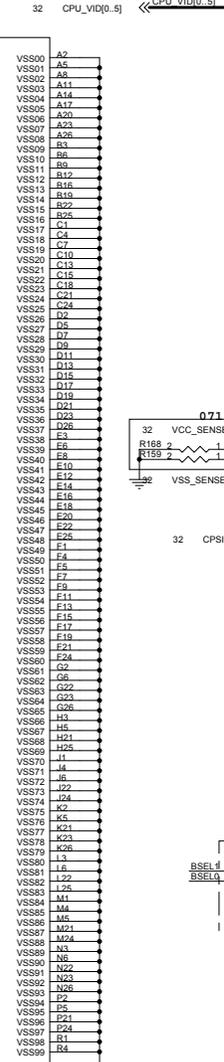
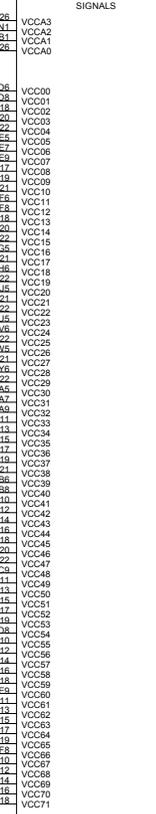
close to CPU



VCC\_CORE  
+VCCP  
+1.8V



Total caps = 2633 uF  
ESR = 15m ohm/5 // 5m ohm/25 // 5m ohm/15



0628

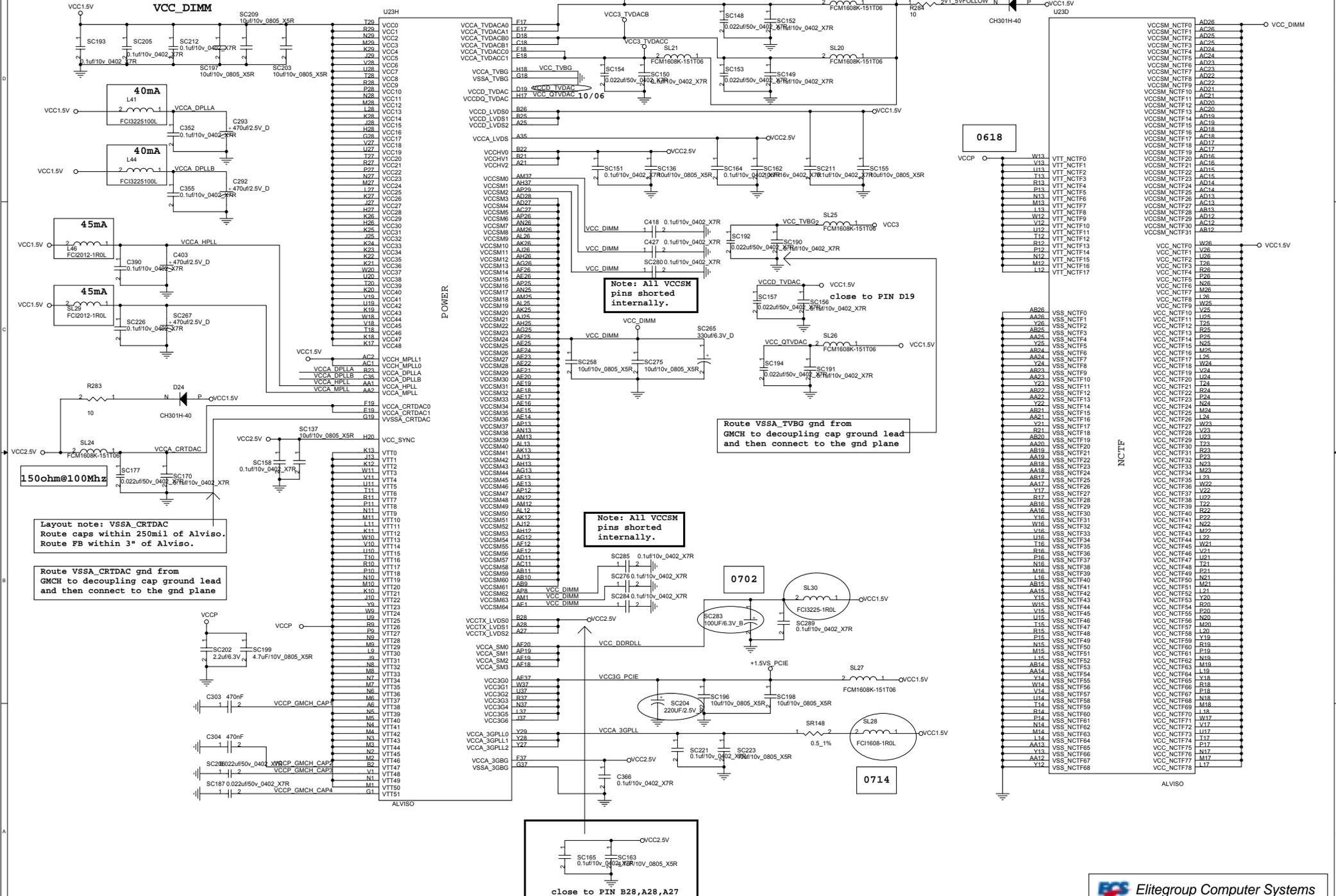








+VCC\_GMCH\_CORE --> 1.5V  
 +VCCP  
 +2.5V  
 VCC\_DIMM



Note: All VCCSM pins shorted internally.

Route VSSA\_TVDBG gnd from GMCH to decoupling cap ground lead and then connect to the gnd plane

Note: All VCCSM pins shorted internally.

Layout note: VSSA\_CRTDAC  
 Route caps within 250mil of Alviso.  
 Route FB within 3" of Alviso.

Route VSSA\_CRTDAC gnd from GMCH to decoupling cap ground lead and then connect to the gnd plane

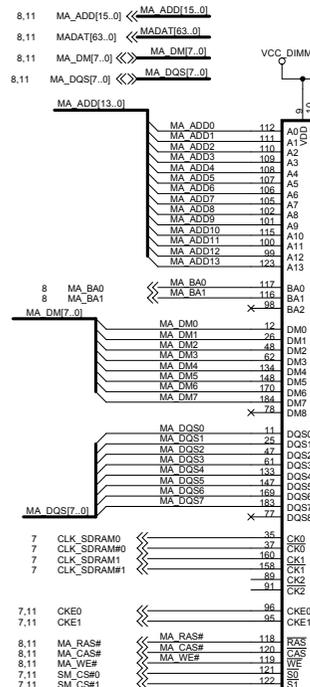
close to PIN B28,A28,A27

**Elitegroup Computer Systems**

ALVISO D (POWER)

558-1-4-01

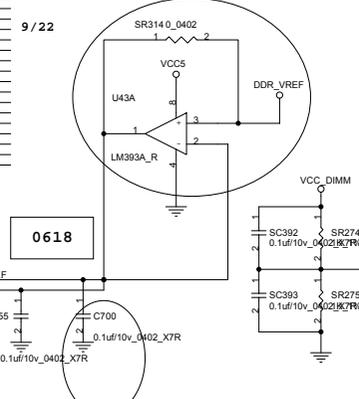
Thursday, October 14, 2004



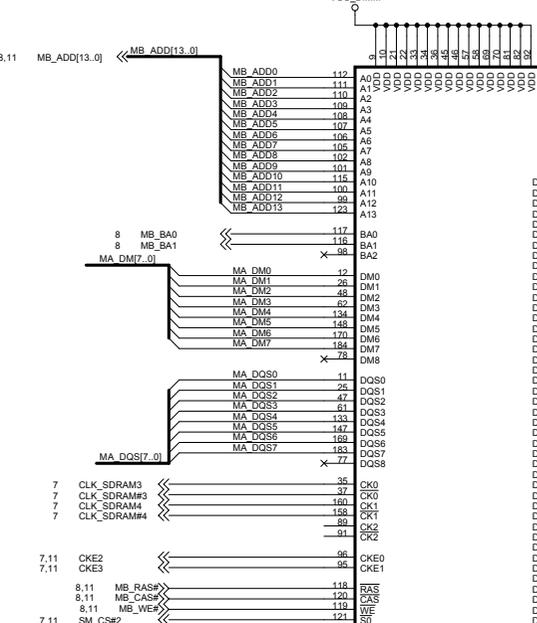
SO-DIMM (NORMAL)



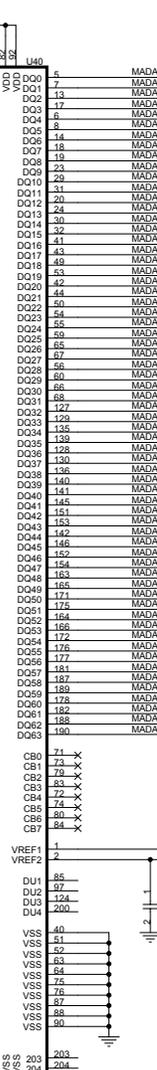
8/12 add intel recommend SMVREF to necessary current and reference voltage



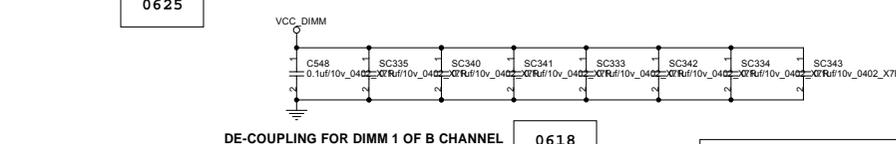
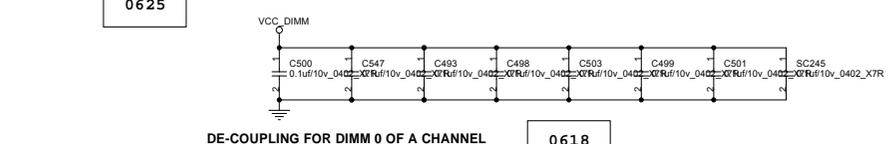
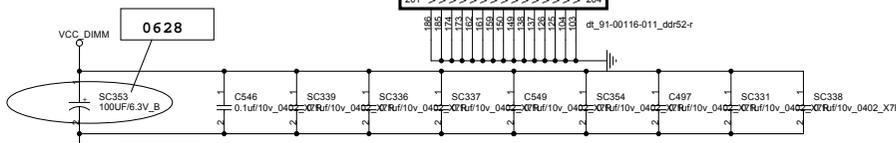
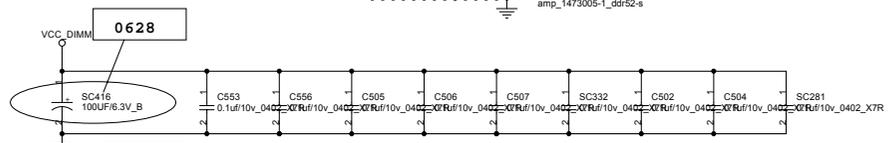
8/13 change location from SC357

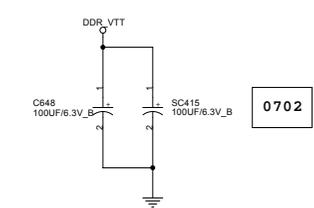
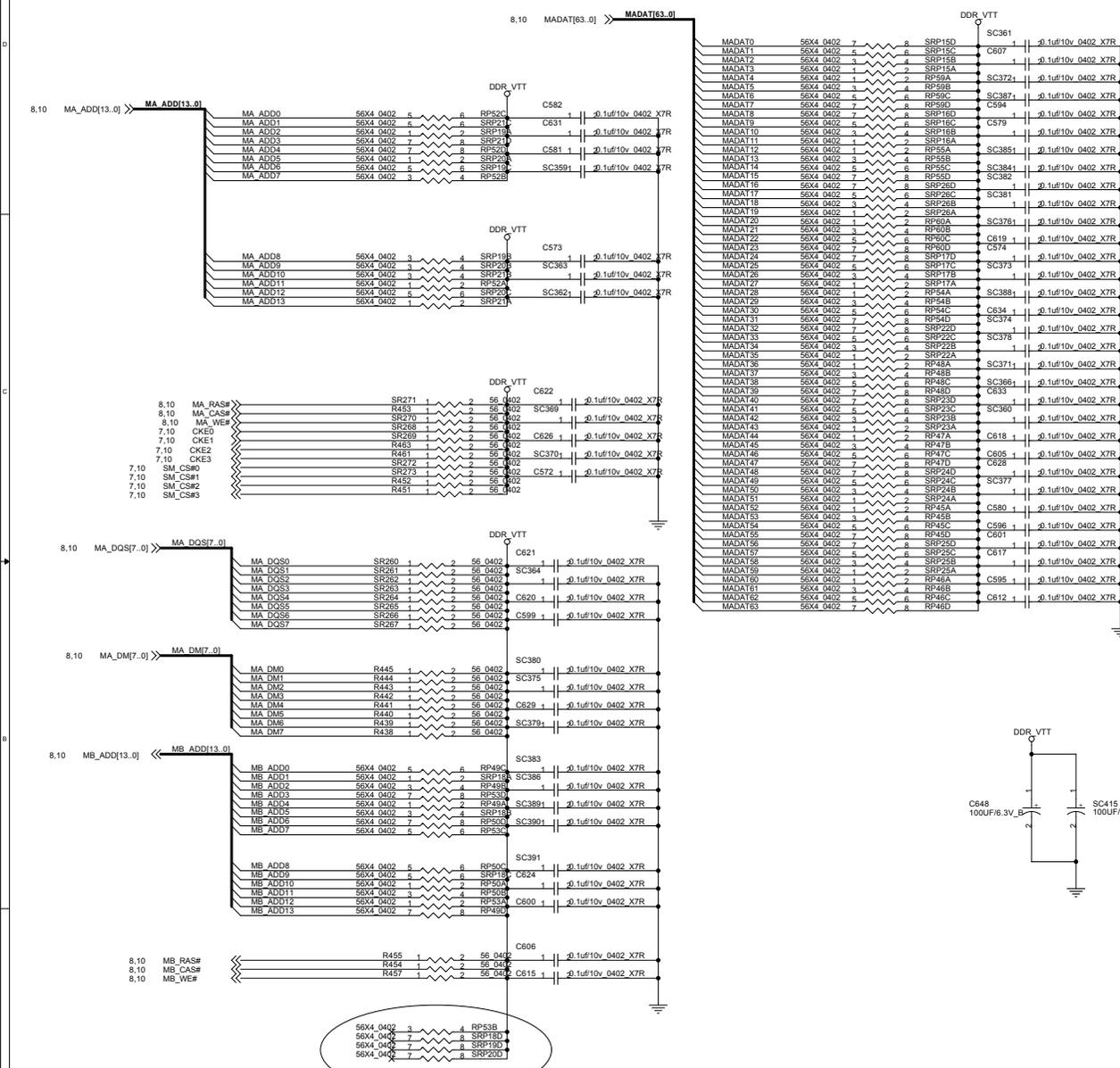


SO-DIMM (REVERSE)

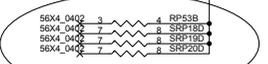


8/13 change location from SC365

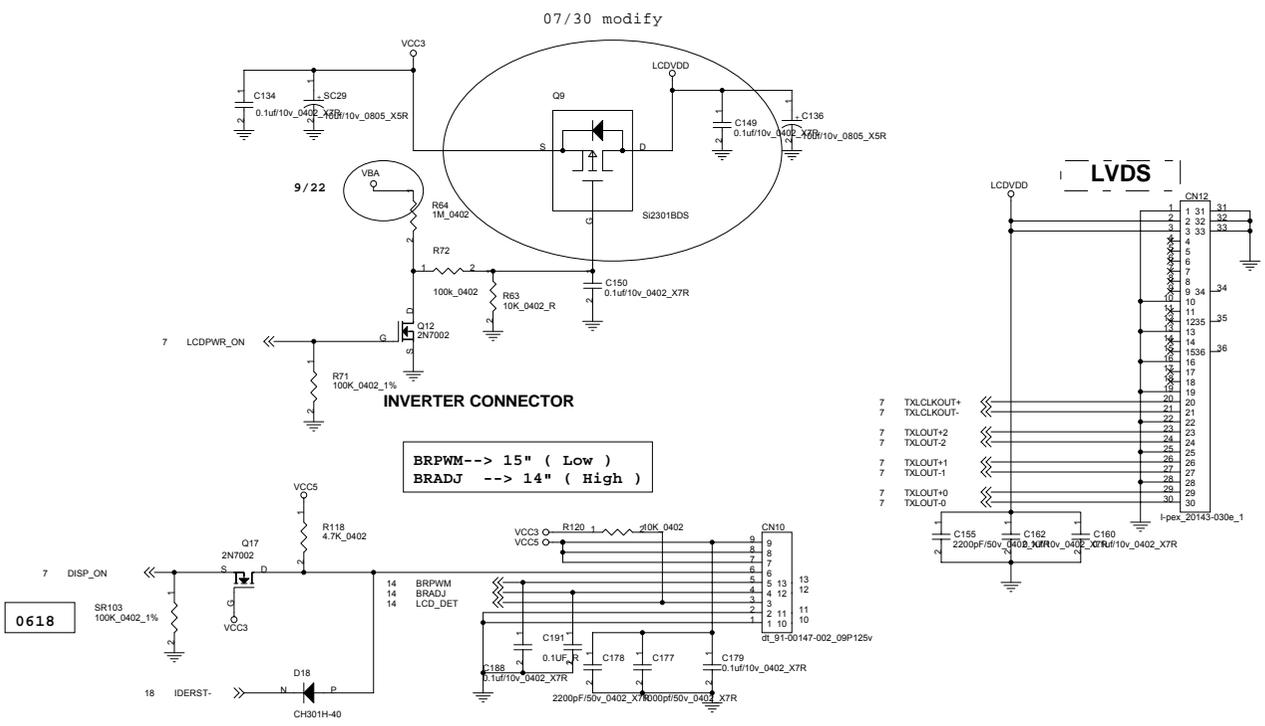


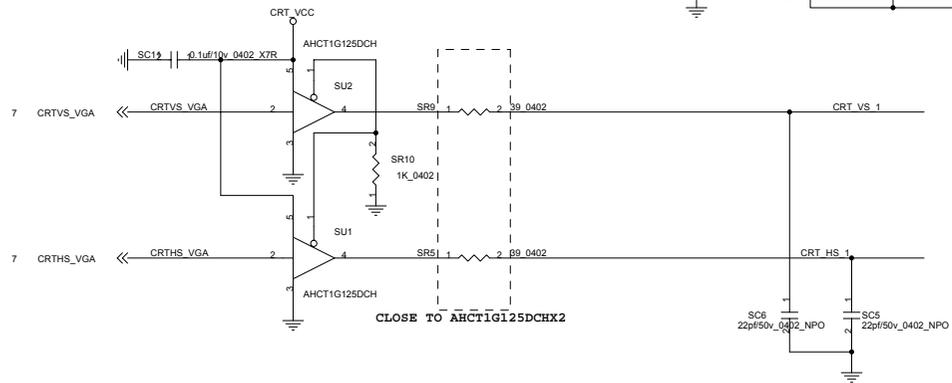
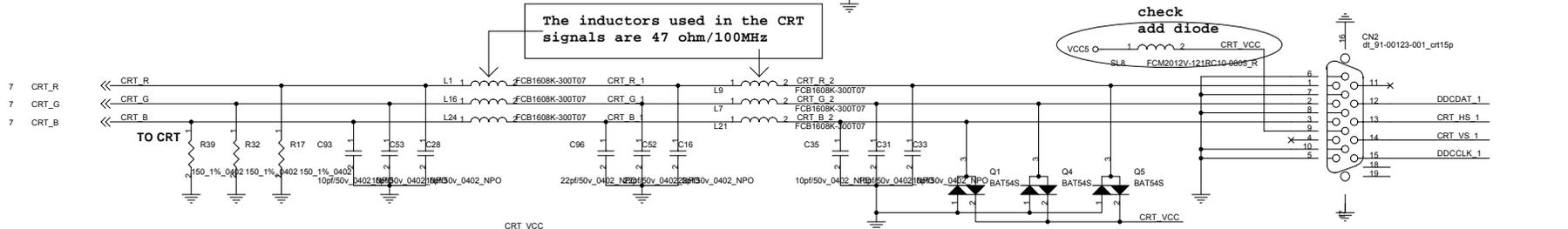
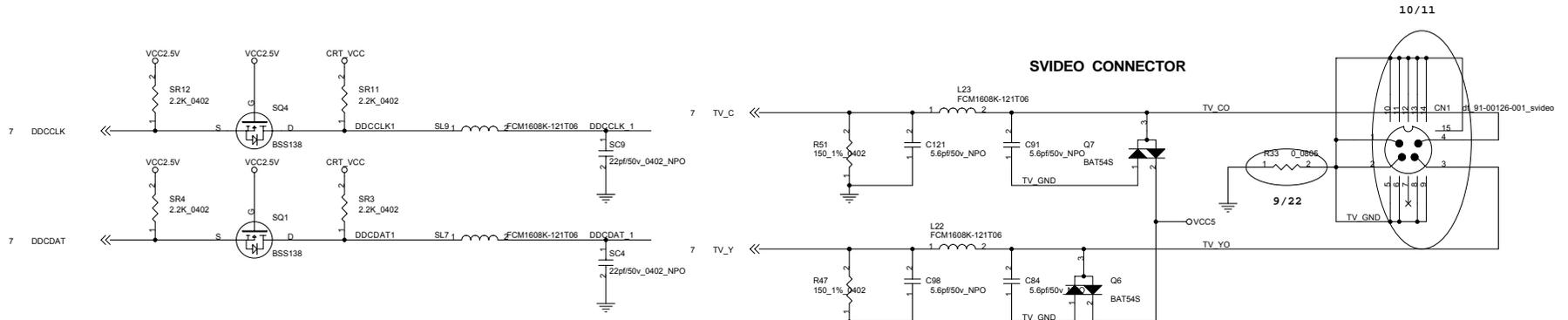


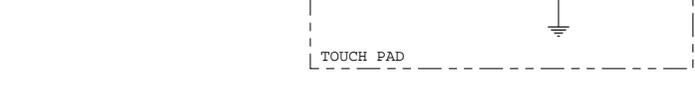
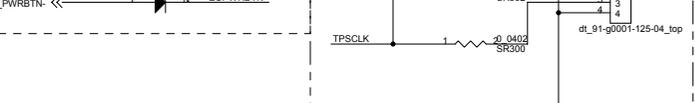
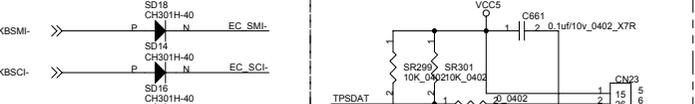
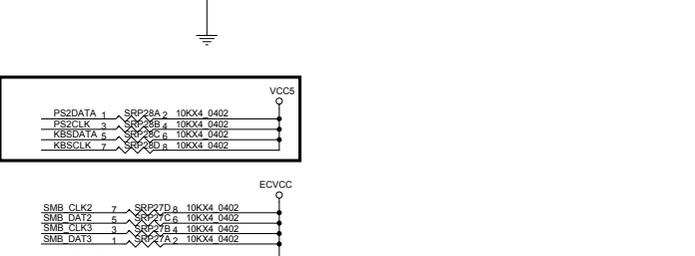
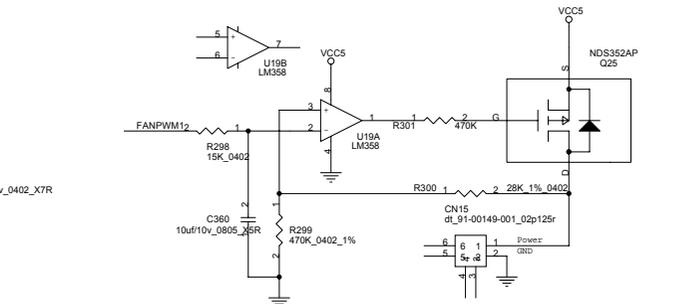
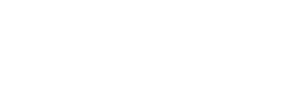
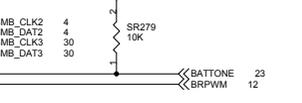
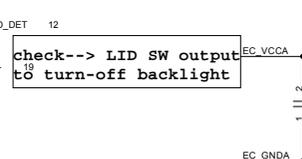
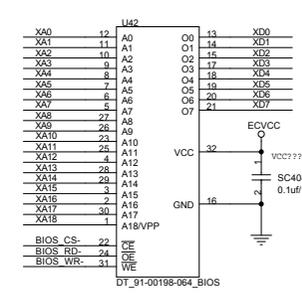
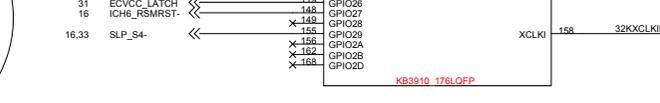
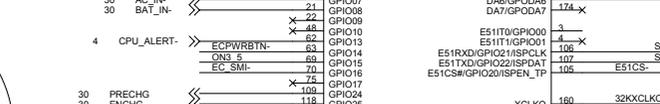
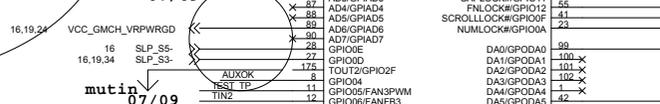
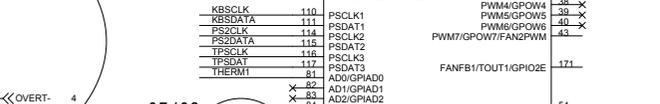
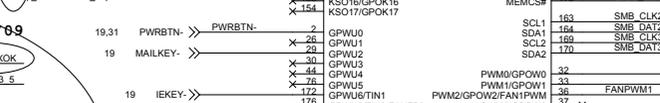
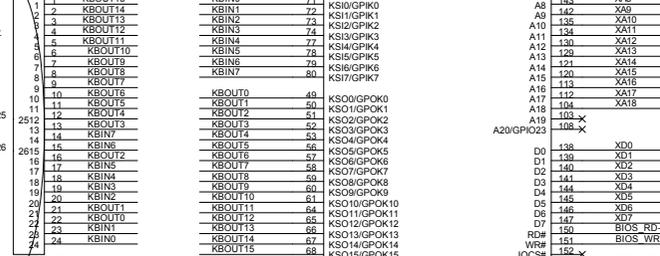
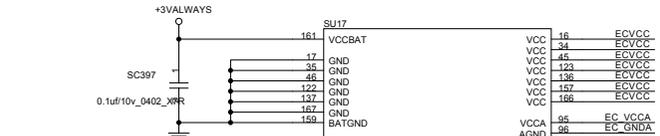
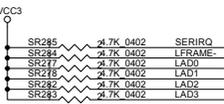
0702



08/04



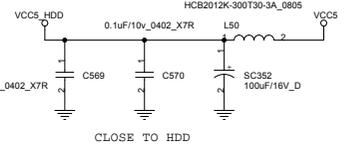
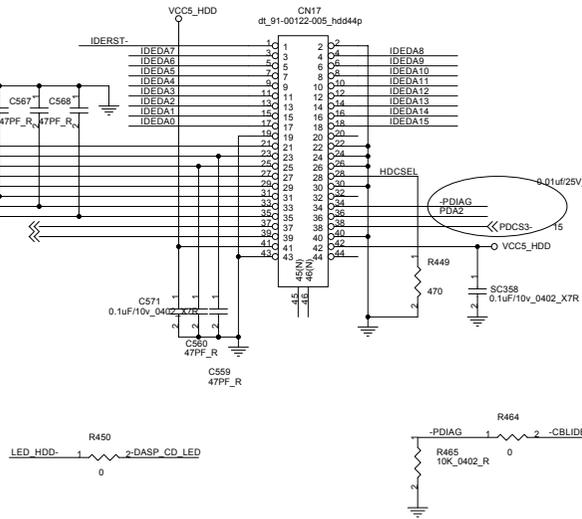
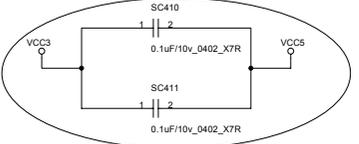
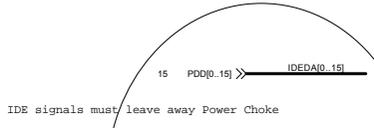




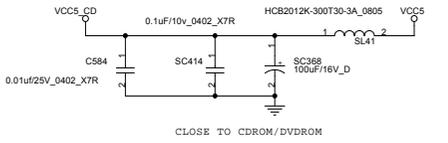
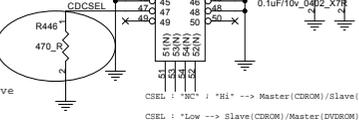
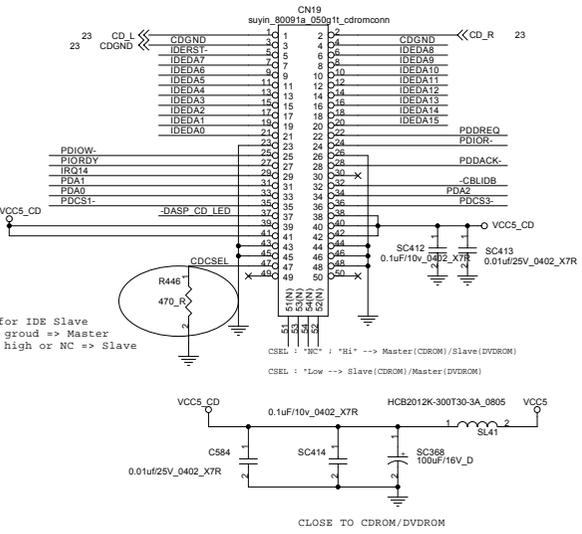
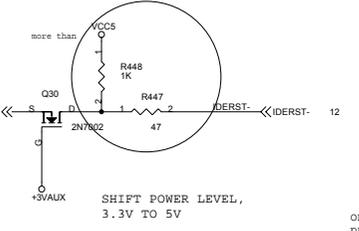








14,15,16,25,27 PLTRST-



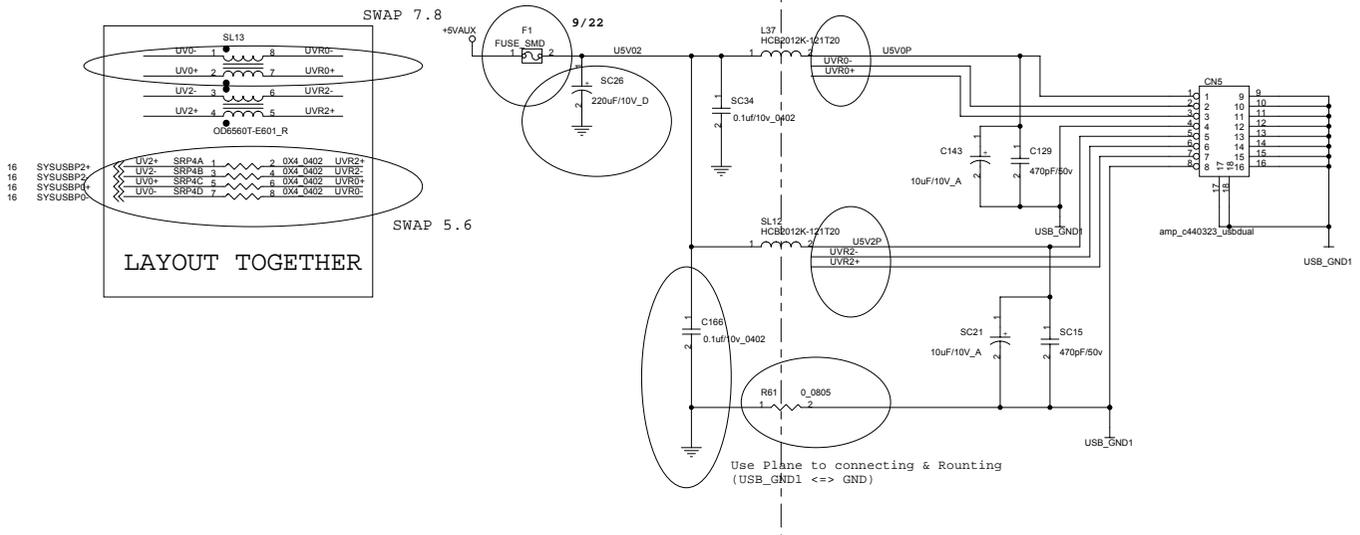


**ALL THESE CLOSE TO CONNECTOR**

8/26 change F1 P/N: from  
16-285-150370 to  
16-200-150010

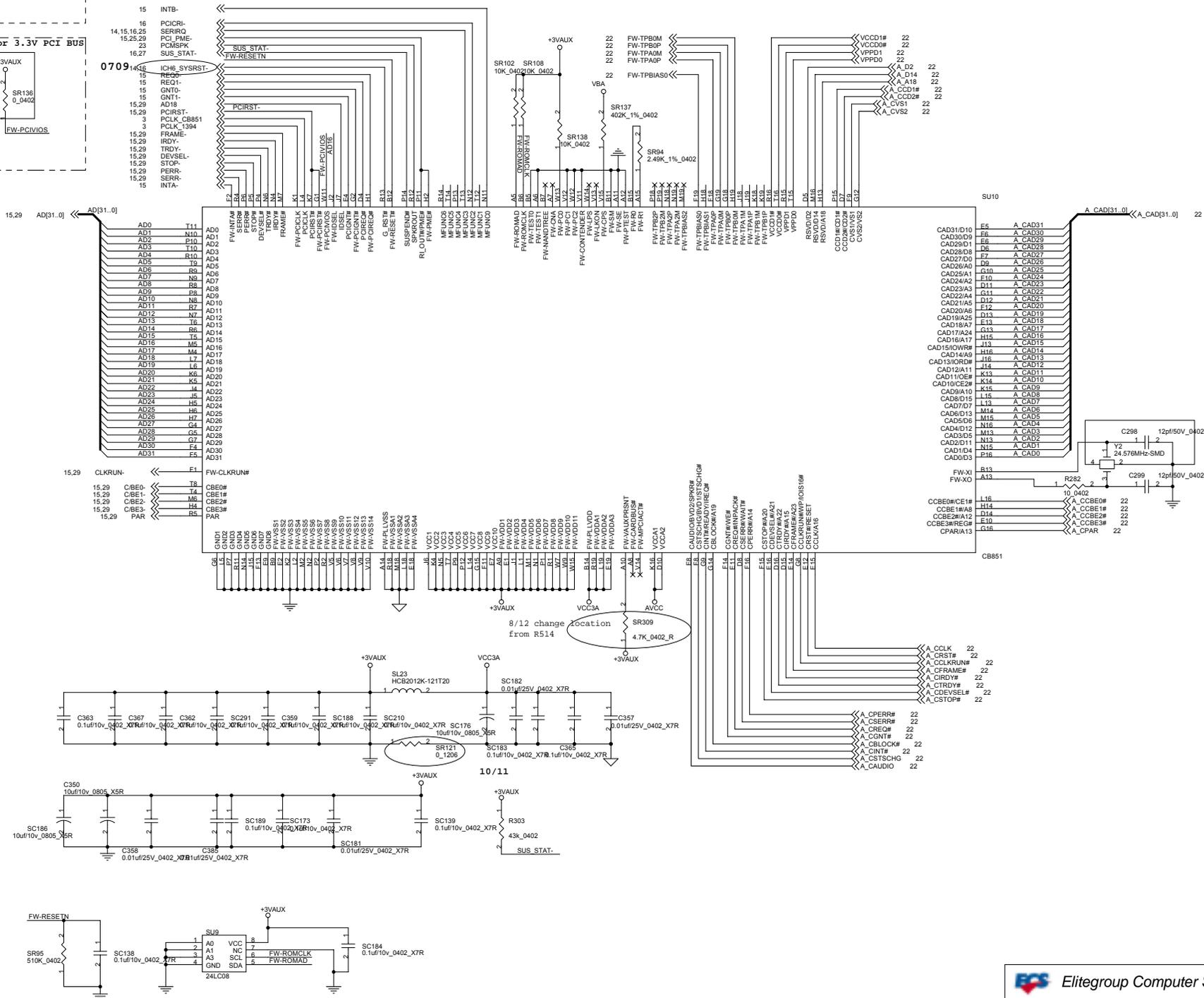
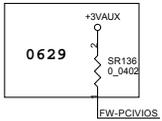
Two ports ,1.5A,at least 60 mils

The dotted line is a moat for layout placement reference.  
Pis Place the components of block into USB moat  
Bead & resistor are bridge



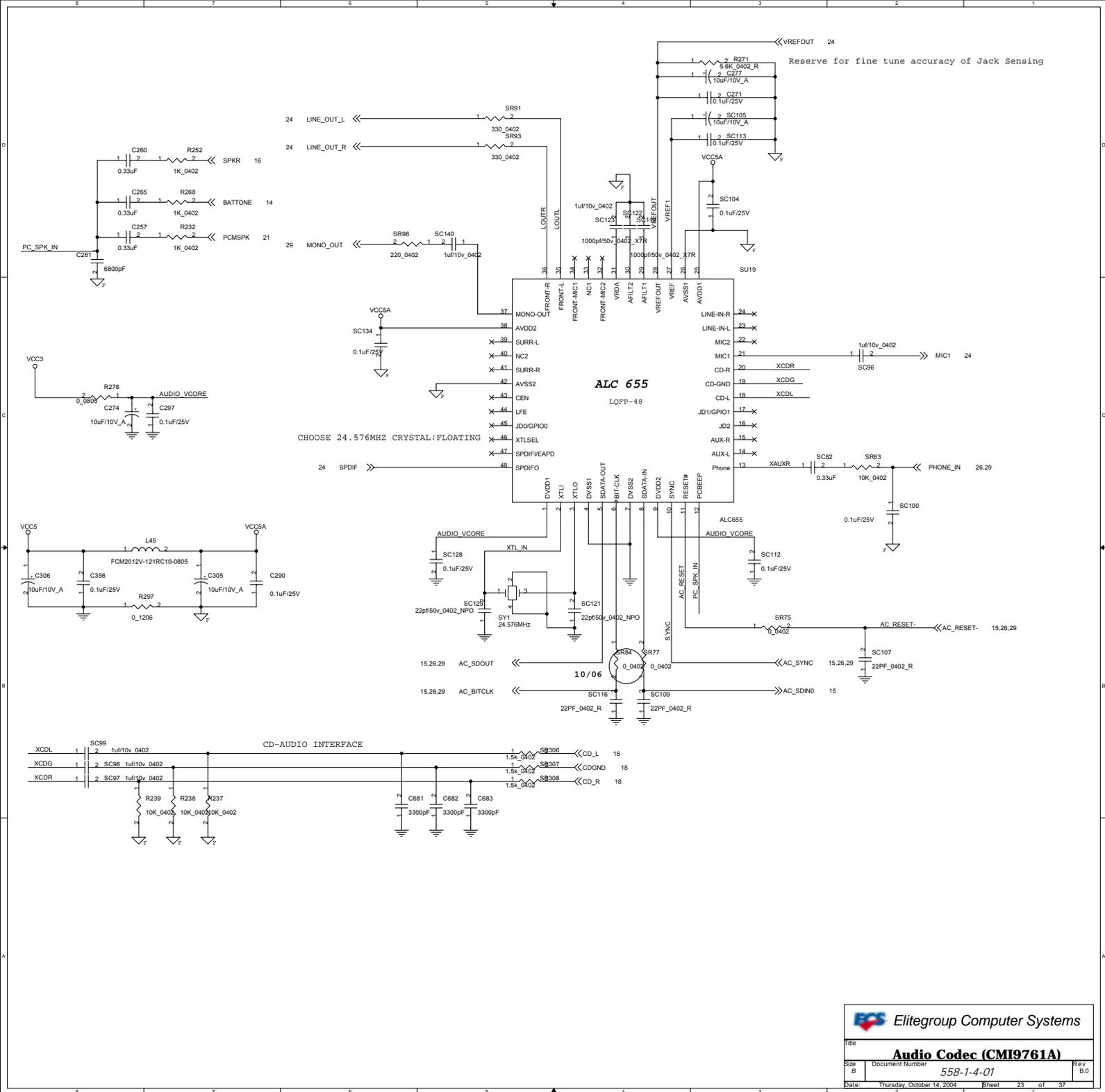
GRST# should connect to Power  
On reset if support S3

Pull High for 3.3V PCI BUS

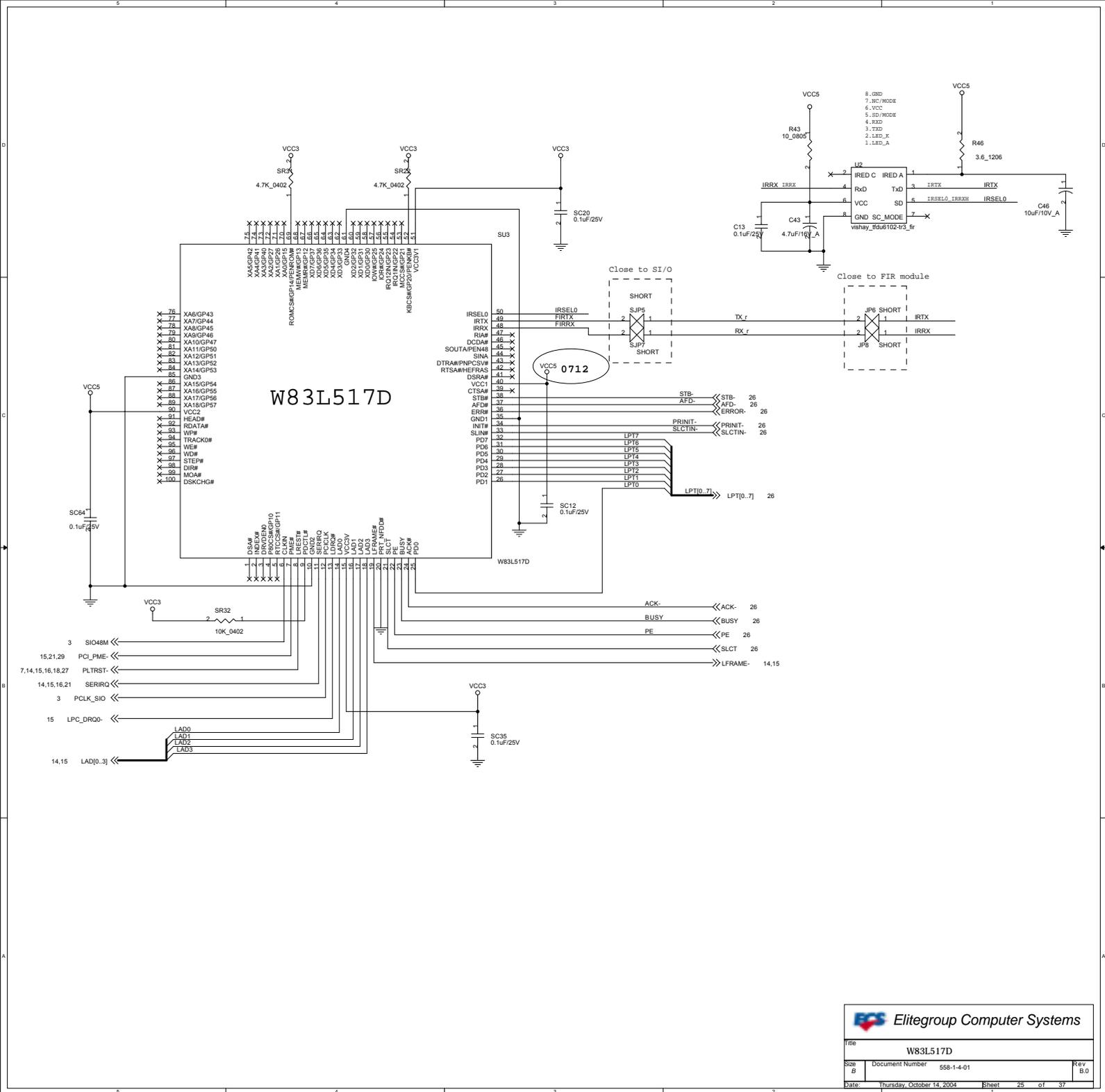


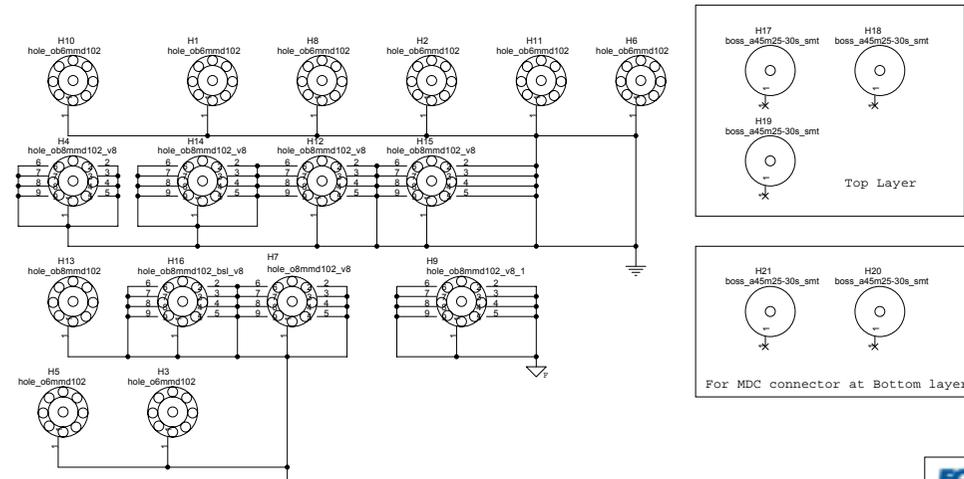
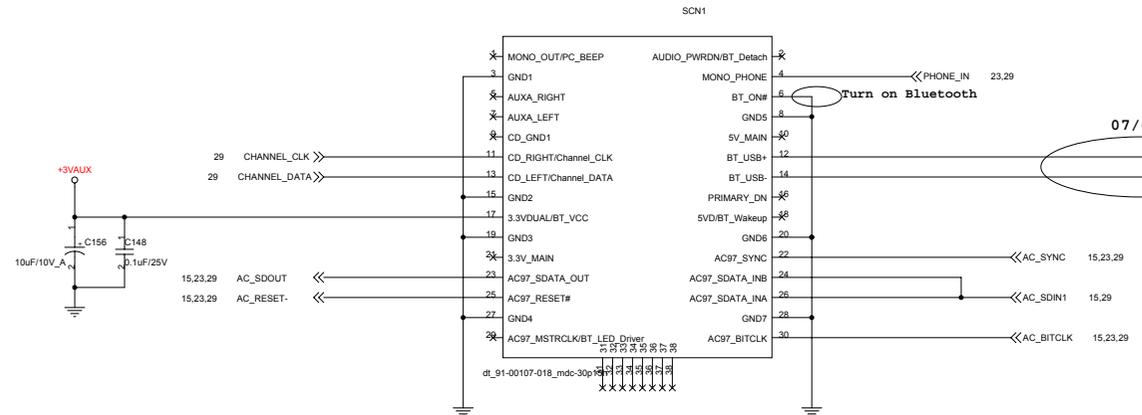
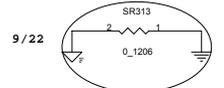
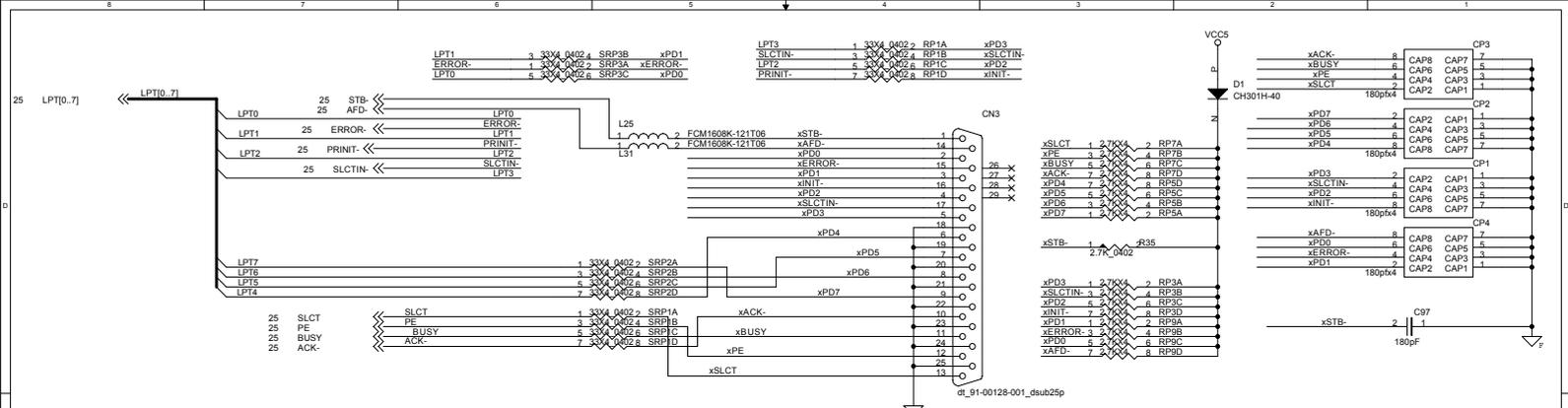
Title			CB851_CARDBUS
Size	Document Number	Rev	
C	558-1-4-01	B.0	
Date:	Thursday, October 14, 2004	Sheet	21 of 37











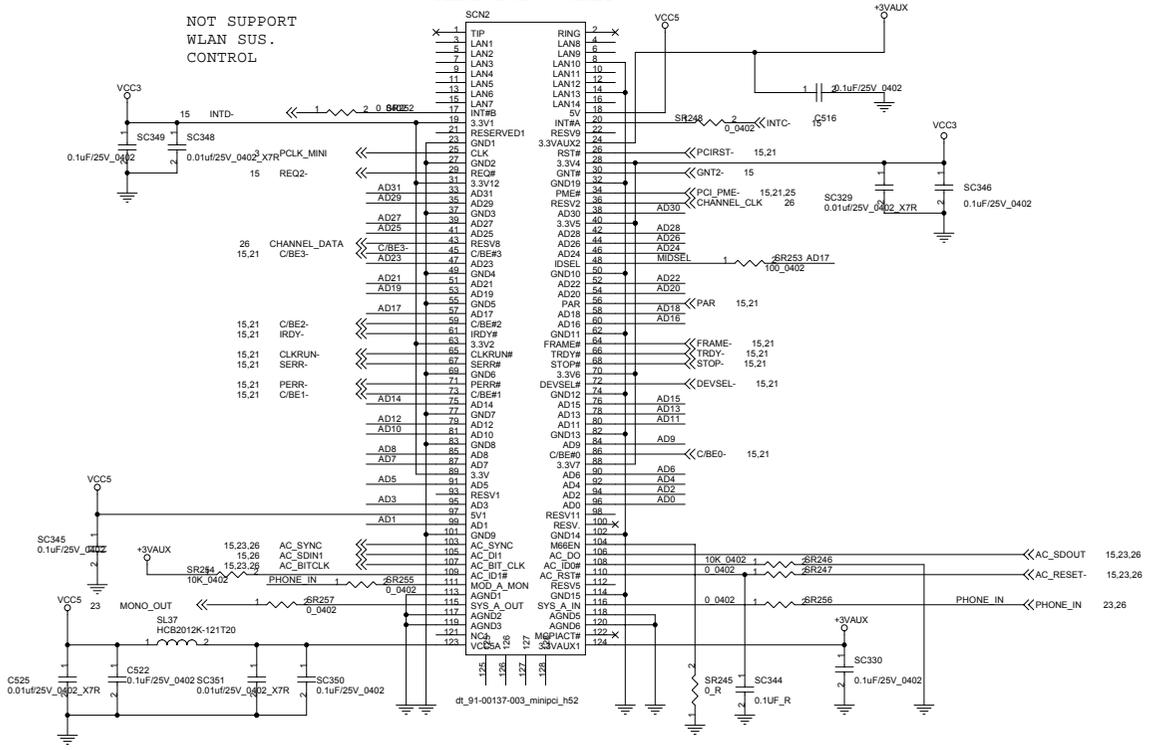


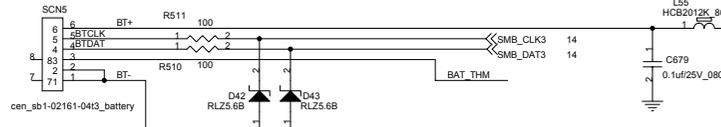
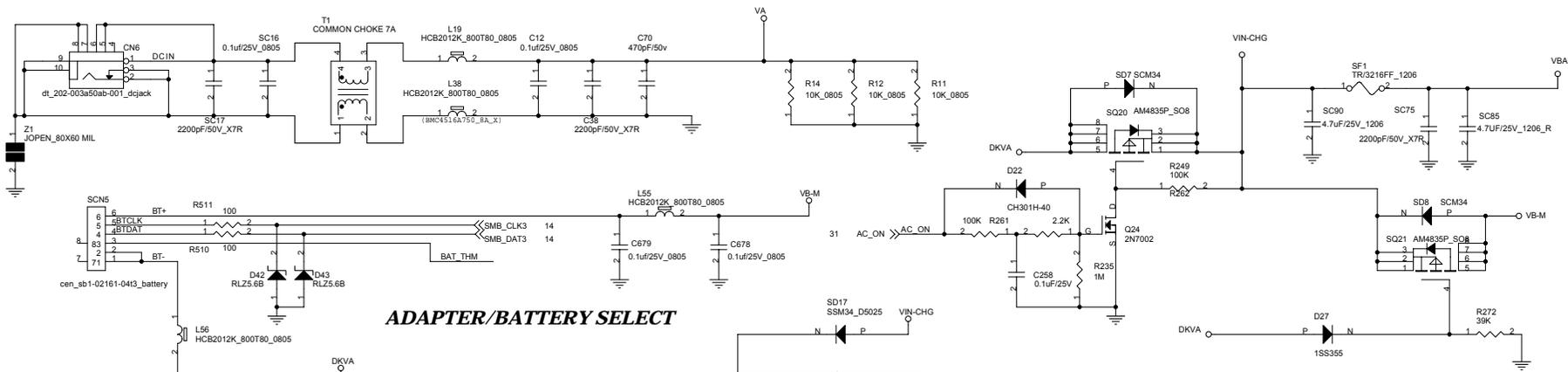


15.21 AD[0..31] ← AD[0..31]

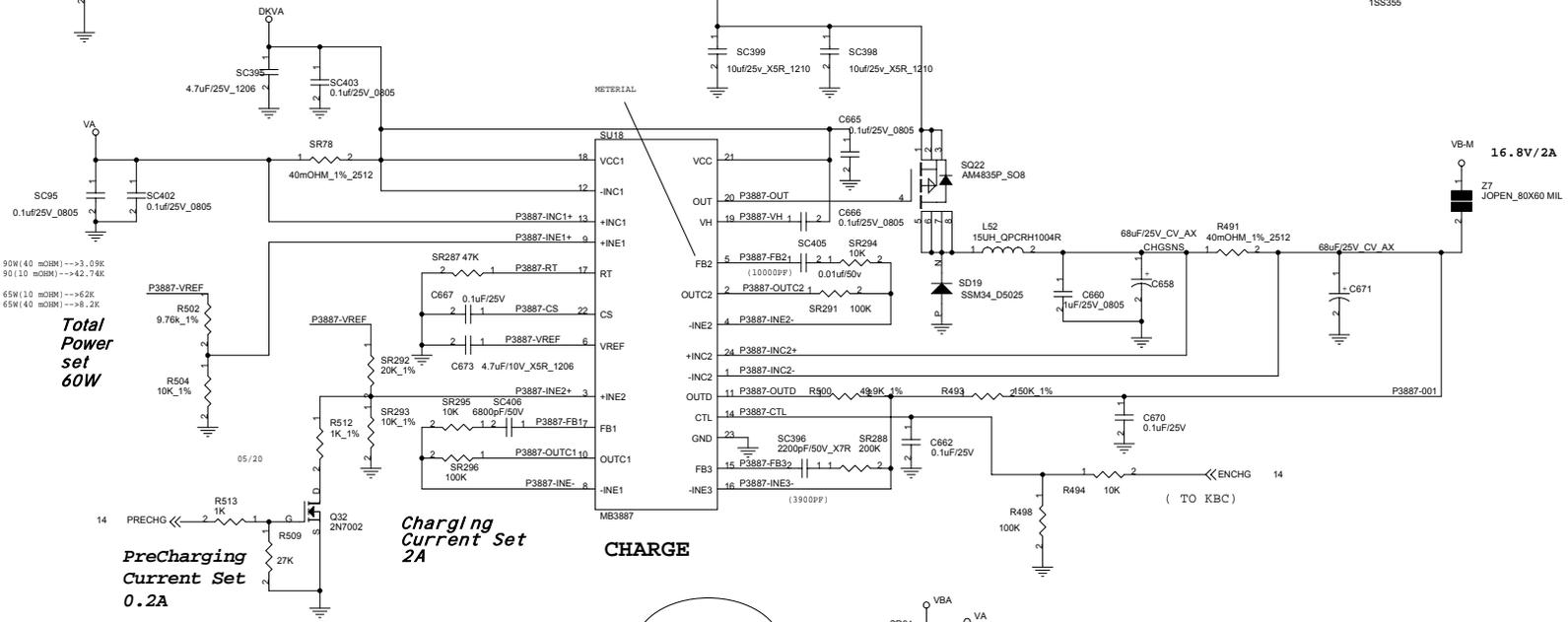
MINI PCI SOCKET

NOT SUPPORT  
WLAN SUS.  
CONTROL





**ADAPTER/BATTERY SELECT**



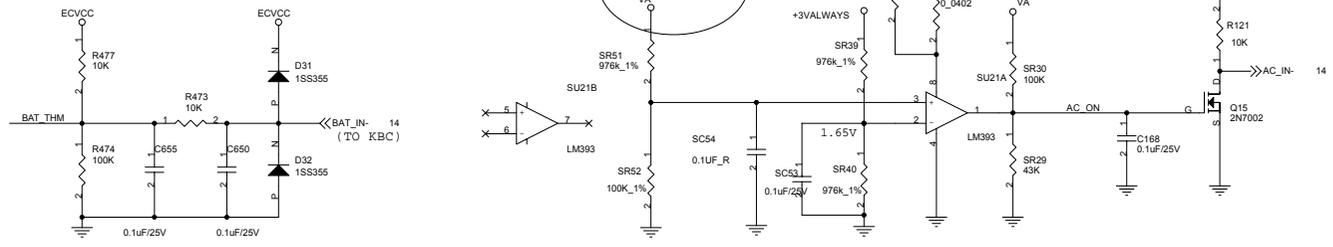
**CHARGE**

90W (40 mOhm) --> 3.09K  
 90 (10 mOhm) --> 42.74K  
 65W (10 mOhm) --> 6.2K  
 65W (40 mOhm) --> 8.2K

**Total Power set 60W**

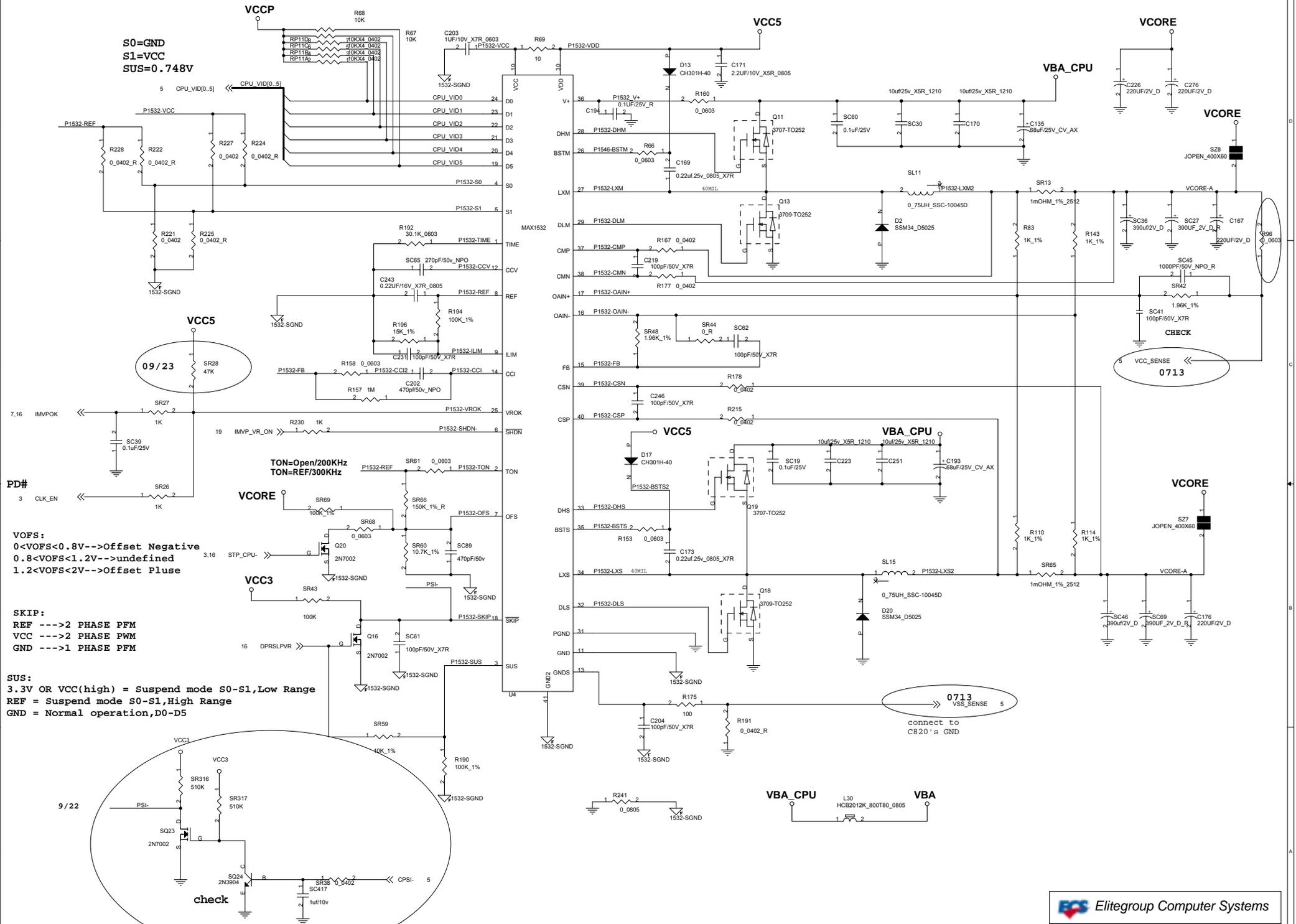
**PreCharging Current Set 0.2A**

**Charging Current Set 2A**





S0=GND  
S1=VCC  
SUS=0.748V

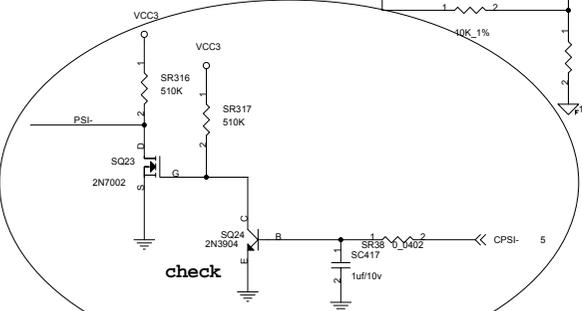


PD#  
3 CLK\_EN

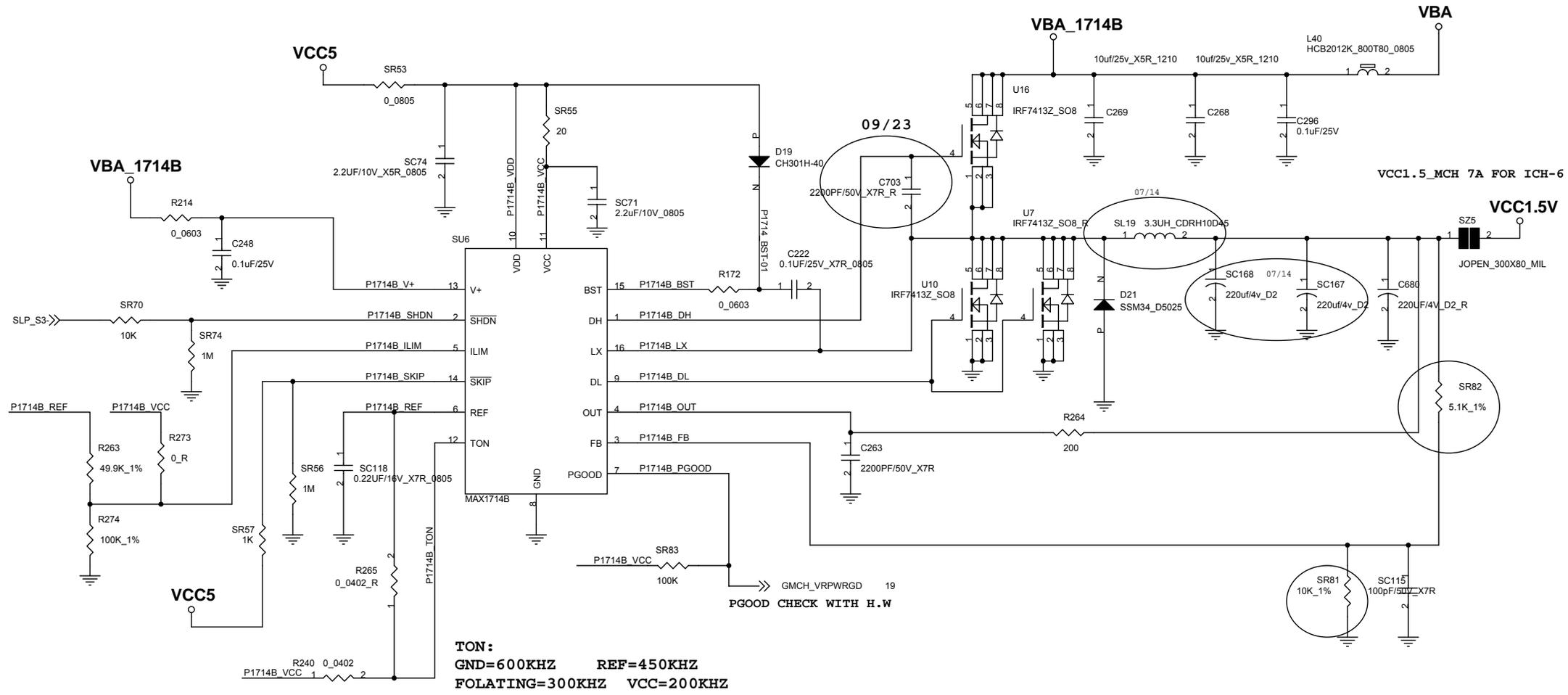
VOFS:  
0<VOFS<0.8V-->Offset Negative  
0.8<VOFS<1.2V-->undefined  
1.2<VOFS<2V-->Offset Plus

SKIP:  
REF --->2 PHASE PFM  
VCC --->2 PHASE PWM  
GND --->1 PHASE PFM

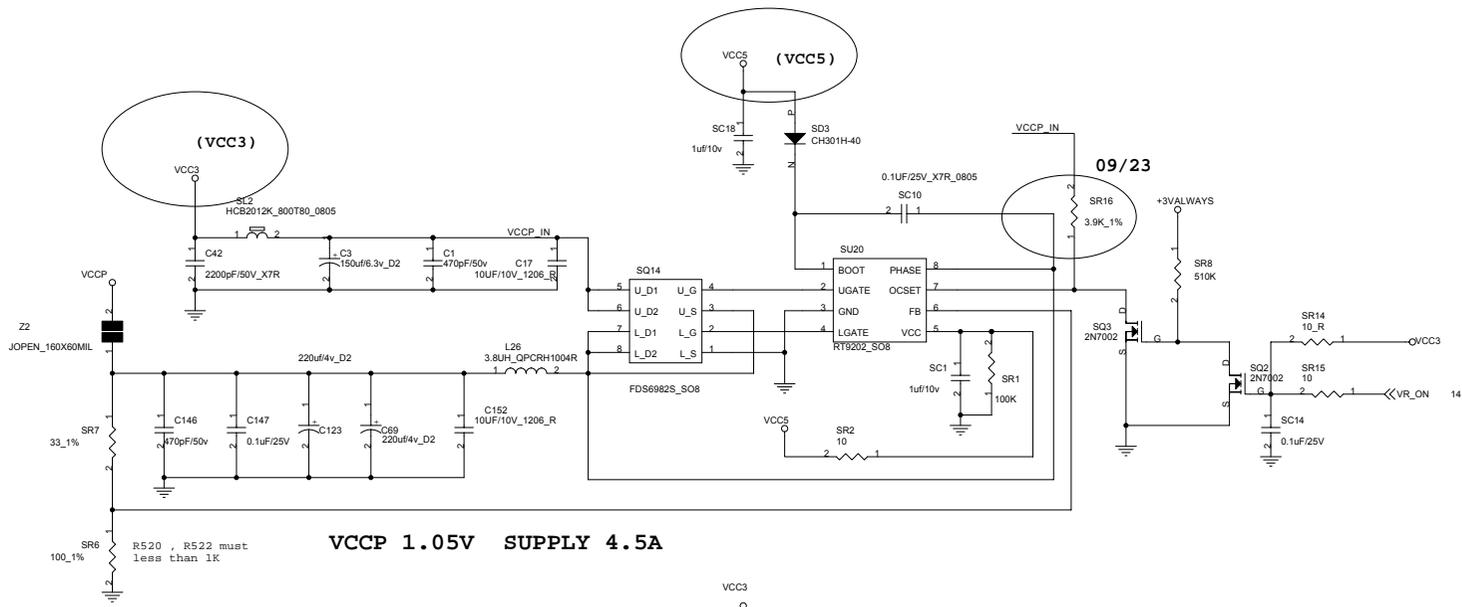
SUS:  
3.3V OR VCC(high) = Suspend mode S0-S1, Low Range  
REF = Suspend mode S0-S1, High Range  
GND = Normal operation, D0-D5



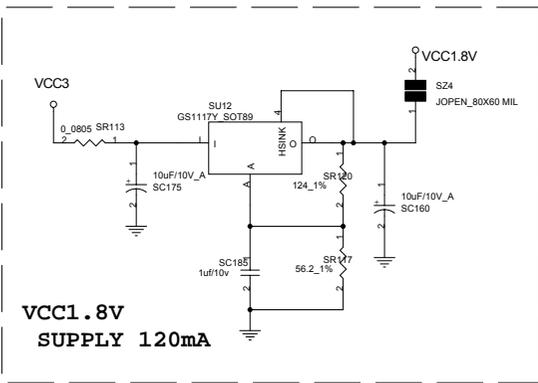
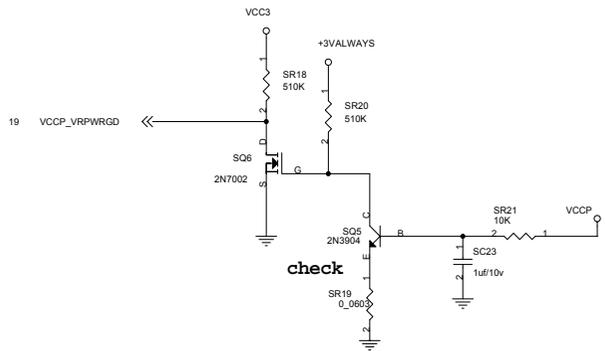




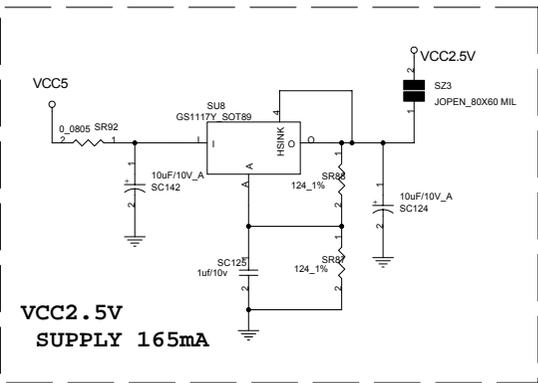
<b>Title</b> <b>VCC1.5V_MAX1714B</b>		
Size	Document Number	Rev
Custom	558-1-4-01	B.0
Date:	Thursday, October 14, 2004	Sheet 34 of 37



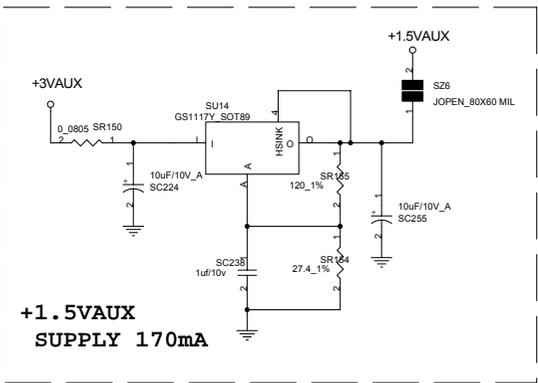
VCCP 1.05V SUPPLY 4.5A



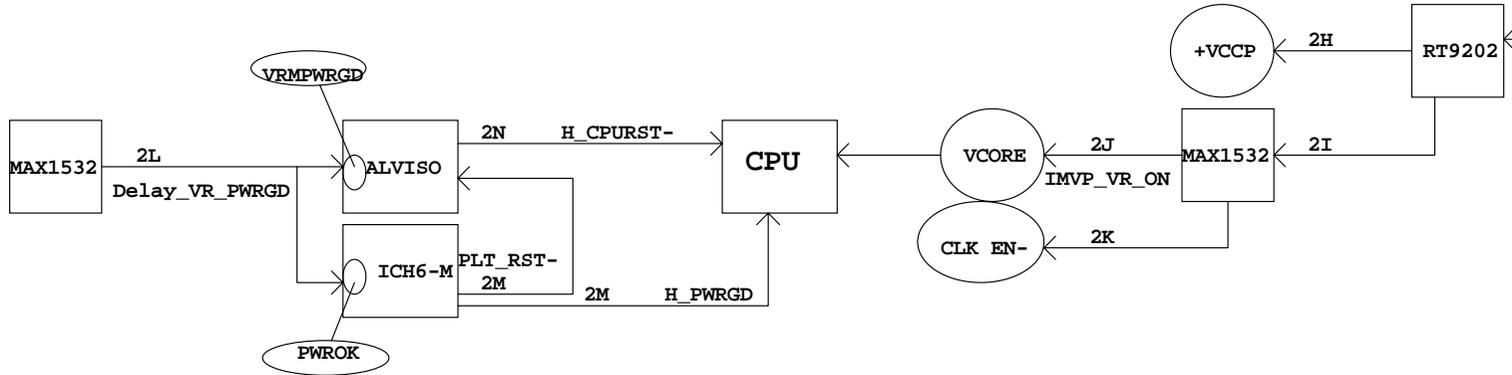
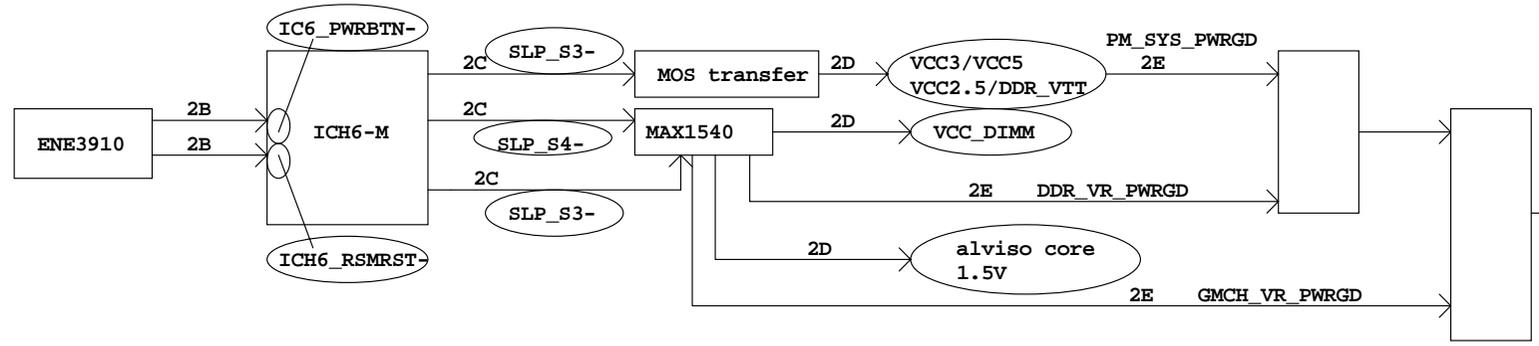
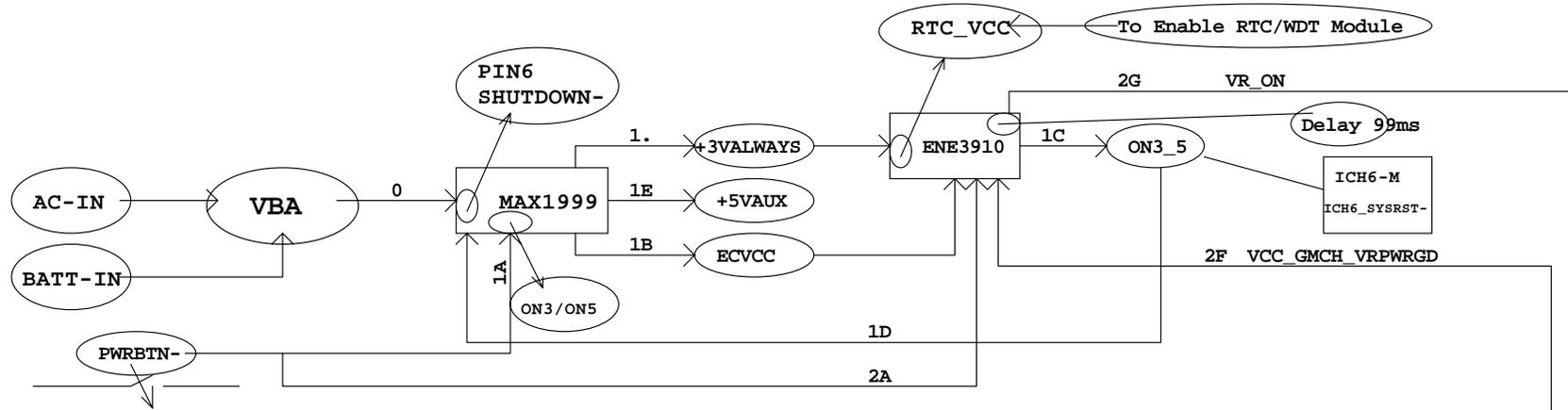
VCC1.8V  
SUPPLY 120mA



VCC2.5V  
SUPPLY 165mA



+1.5VAUX  
SUPPLY 170mA



V.A: Initial Release 2004/08/09 15-F55-010010

V.B: Initial Release 2004/10/13 15-F55-010020

 <b>Elitegroup Computer Systems</b>		
Title		
<b>History</b>		
Size C	Document Number 558-1-4-01	Rev B.0
Date	Thursday, October 14, 2004	Sheet 37 of 37