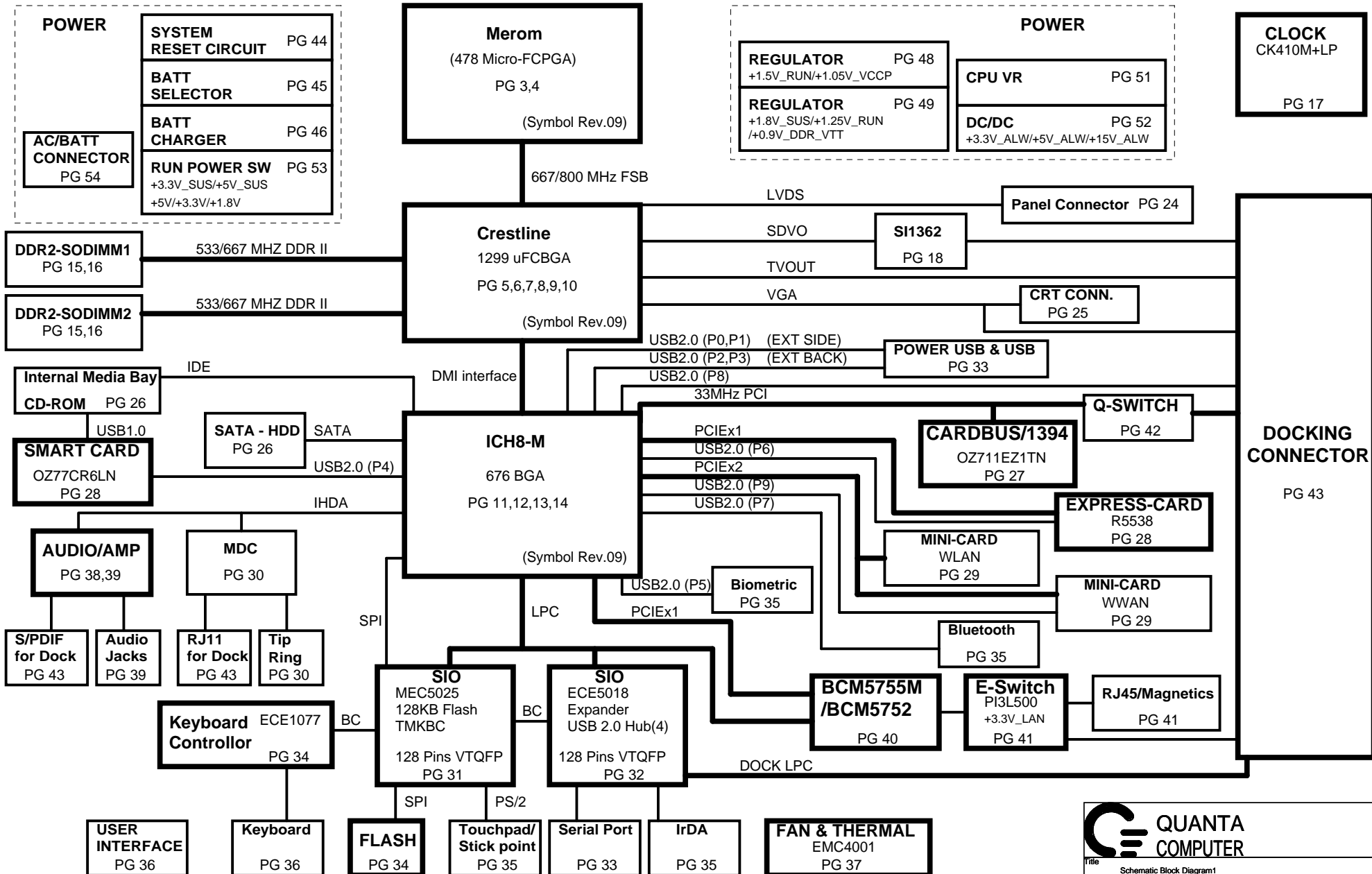


JM7-INTEGRATED

PWA FP381, PWB DY483,
SCHEM UW474.
VER : 1A

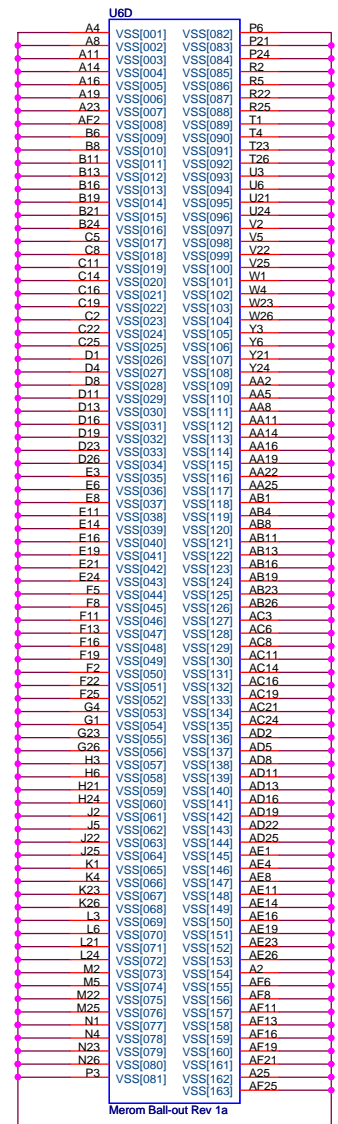
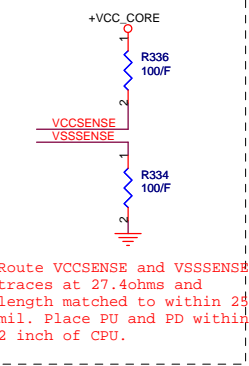
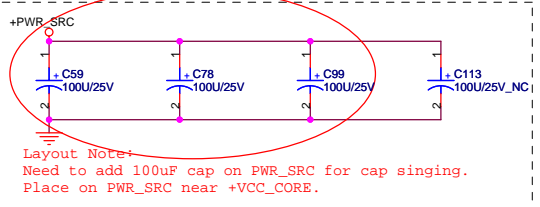
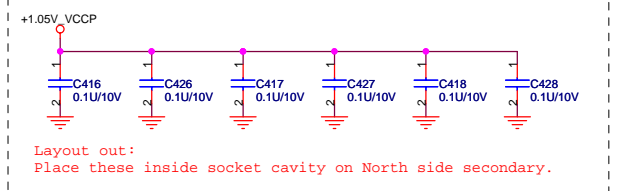
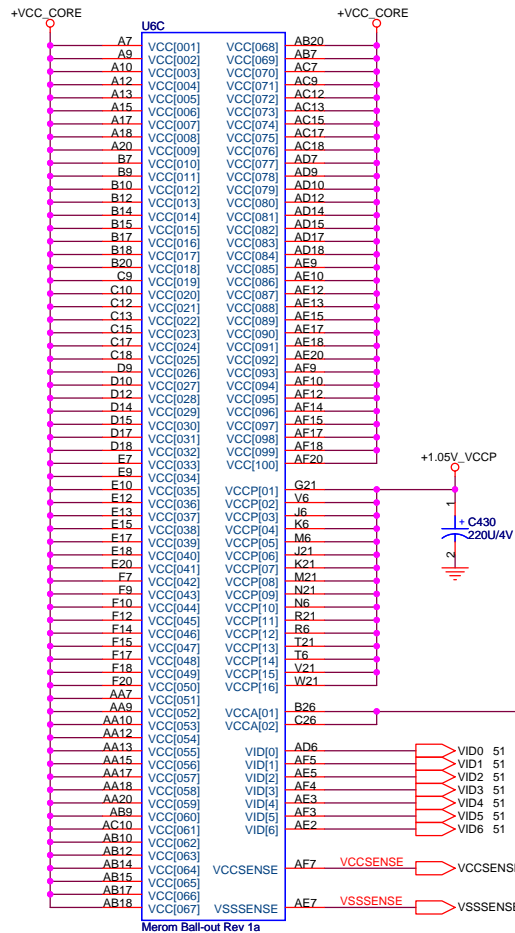
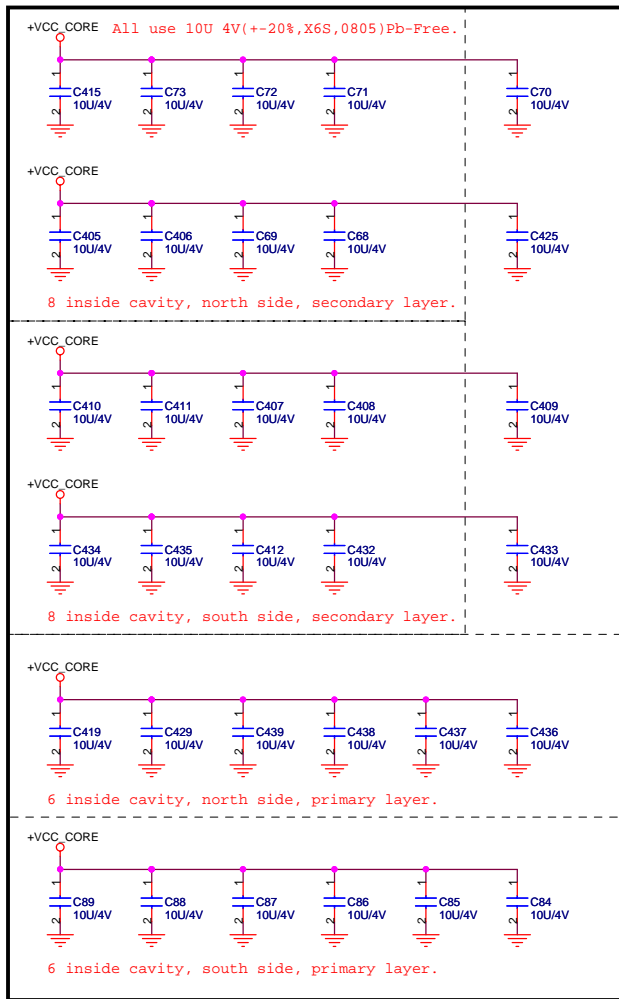


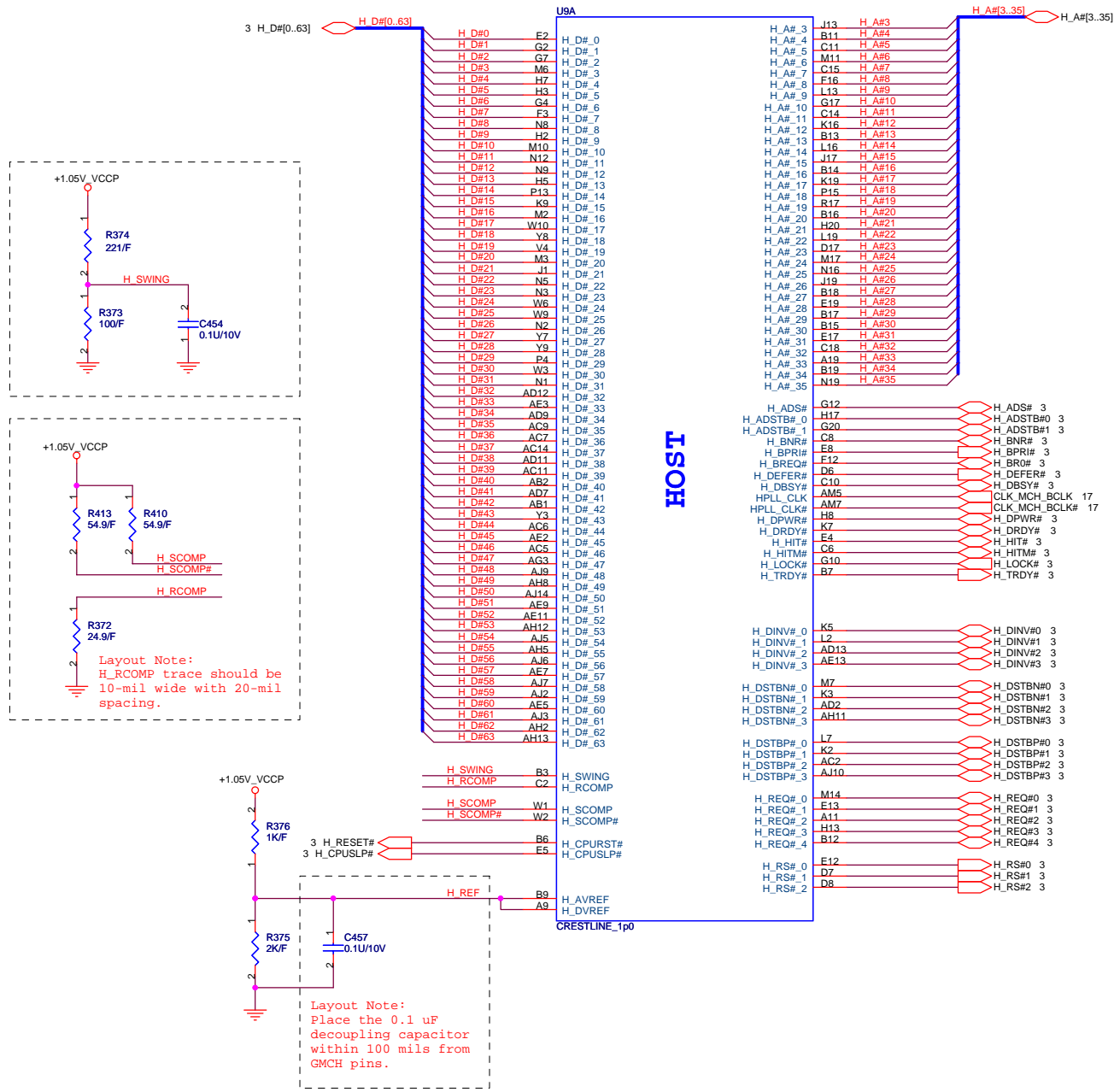
QUANTA COMPUTER

Title: Schematic Block Diagram1

Size: Document Number JM7 Rev 1A

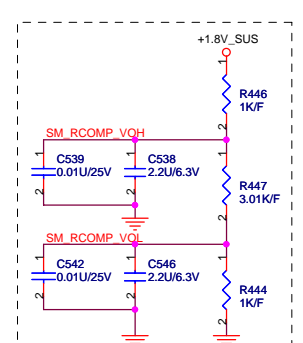
Date: Monday, June 26, 2006 Sheet 1 of 57



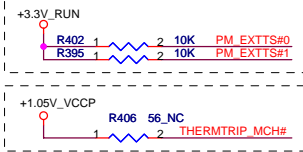


HOST

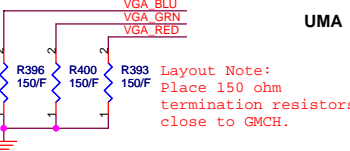
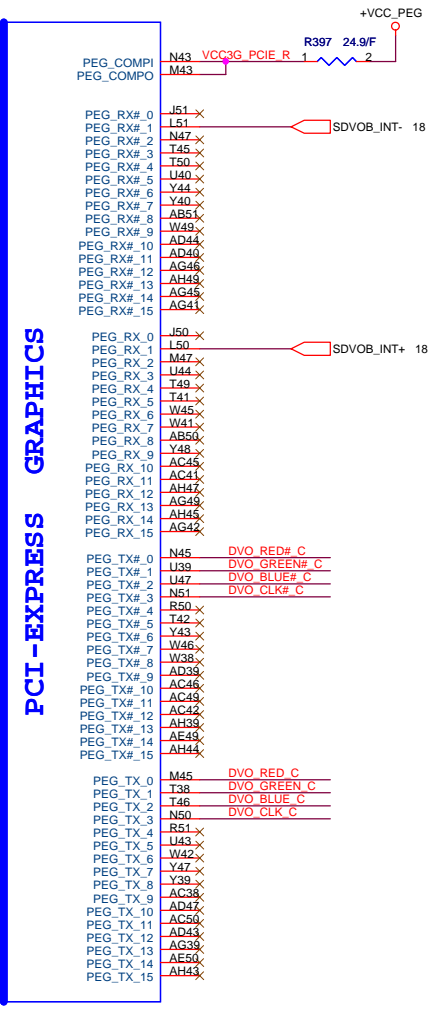
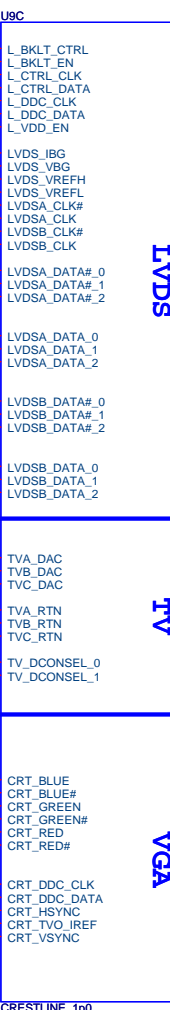
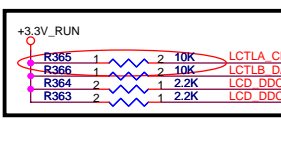
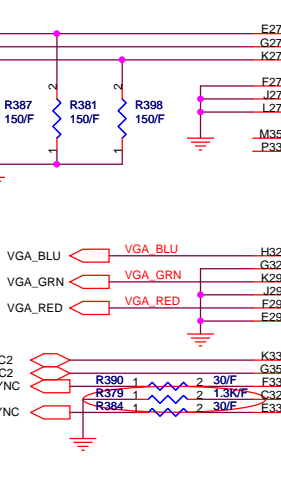
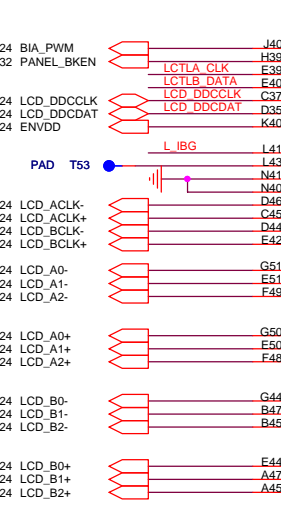
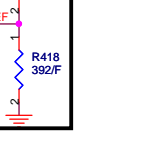
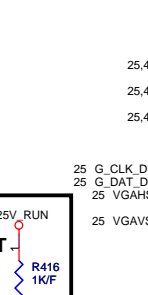
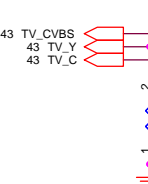
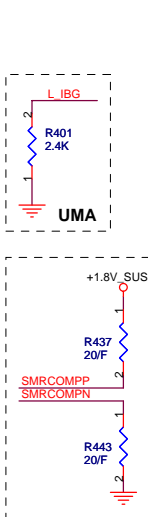
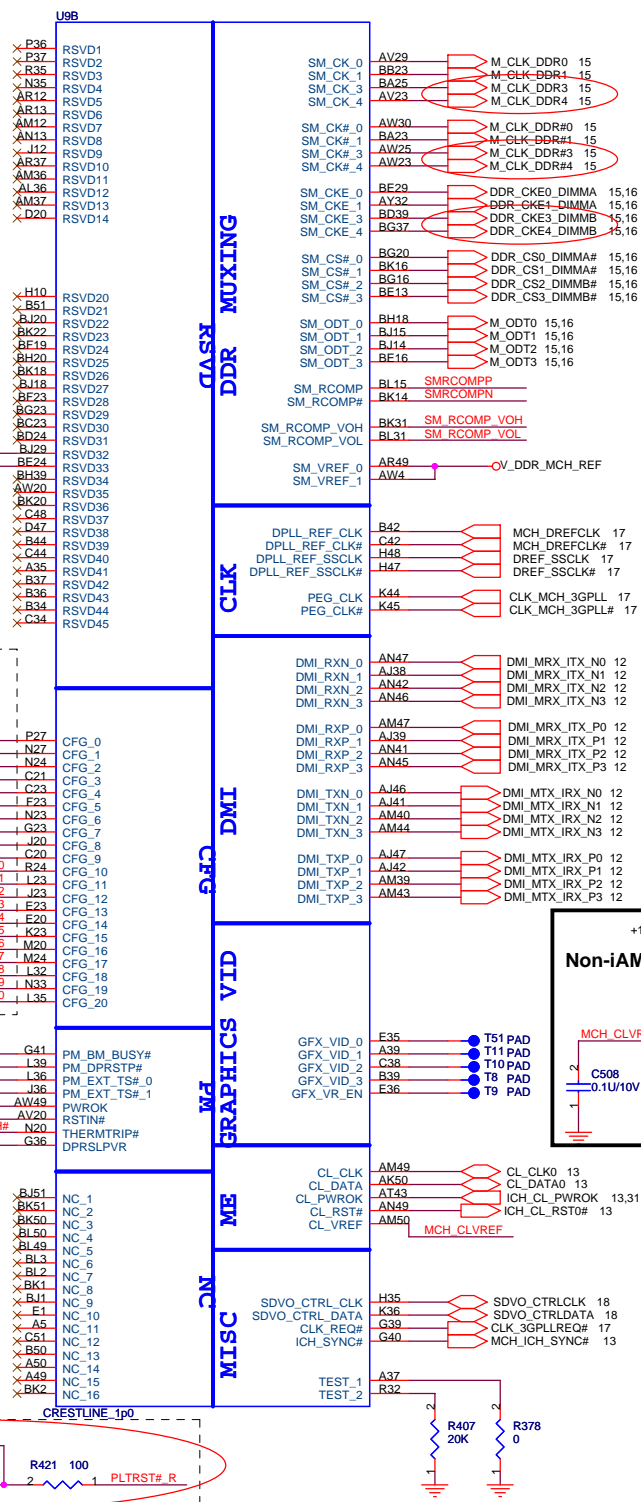
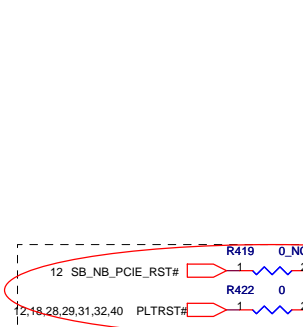
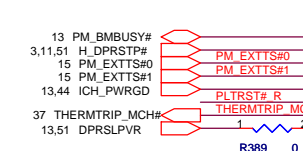
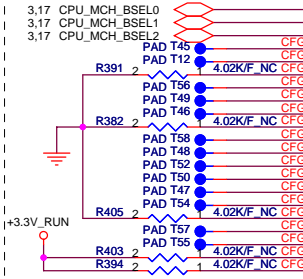




Santa Rosa Platform MOW W115
For 4Gb DRAM support,
change Pin-BJ29 to DDR_A_MA14,
change Pin-BE24 to DDR_B_MA14.



Layout Note:
Location of all MCH_CFG strap
resistors needs to be close to
minimize stub.



Signal	Value	Component	Location
DVO_RED#_C	0.1u/10V	R475	SDVOB_RED- 18
DVO_GREEN#_C	0.1u/10V	R489	SDVOB_GREEN- 18
DVO_BLUE#_C	0.1u/10V	R483	SDVOB_BLUE- 18
DVO_CLK#_C	0.1u/10V	R471	SDVOB_CLK- 18
DVO_RED_C	0.1u/10V	R473	SDVOB_RED+ 18
DVO_GREEN_C	0.1u/10V	R486	SDVOB_GREEN+ 18
DVO_BLUE_C	0.1u/10V	R480	SDVOB_BLUE+ 18
DVO_CLK_C	0.1u/10V	R481	SDVOB_CLK+ 18

CFG	Setting	Effect
CFG5	DMI X2 Select	Low=DMiX2, High=DMiX4(Default)
CFG9	PCI Express Graphic Lane	Low= Reverse Lane, High=Normal operation
CFG16	FSB Dynamic ODT	Low=Dynamic ODT Disable, High=Dynamic ODT Enable(default).
CFG19	DMI Lane Reversal	Low=Normal(default), High=Lane Reversed
CFG20	SDVO/PCIE Concurrent Operation	Low=Only SDVO or PCIEx1 is operational (defaults), High=SDVO and PCIEx1 are operating simultaneously via PEG port
SDVO_CTRL_DATA	SDVO Present	Low=No SDVO Device Present (default), High=SDVO Device Present

QUANTA COMPUTER

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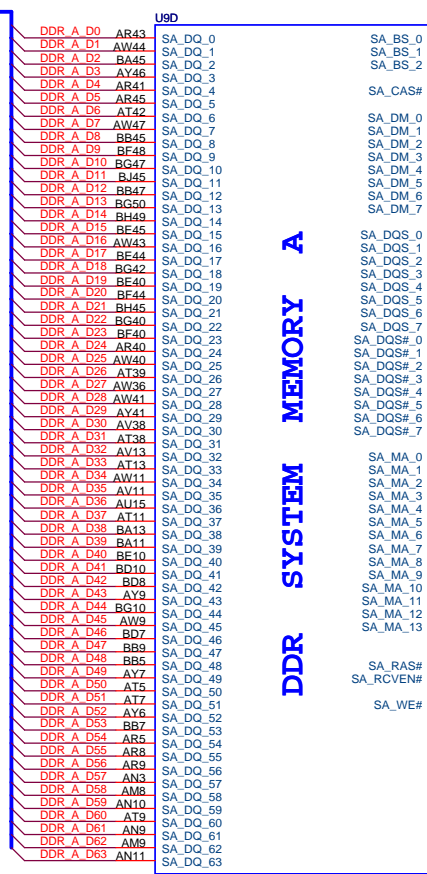
Size: Document Number JM7

Date: Wednesday, June 28, 2006

Sheet: 6 of 57

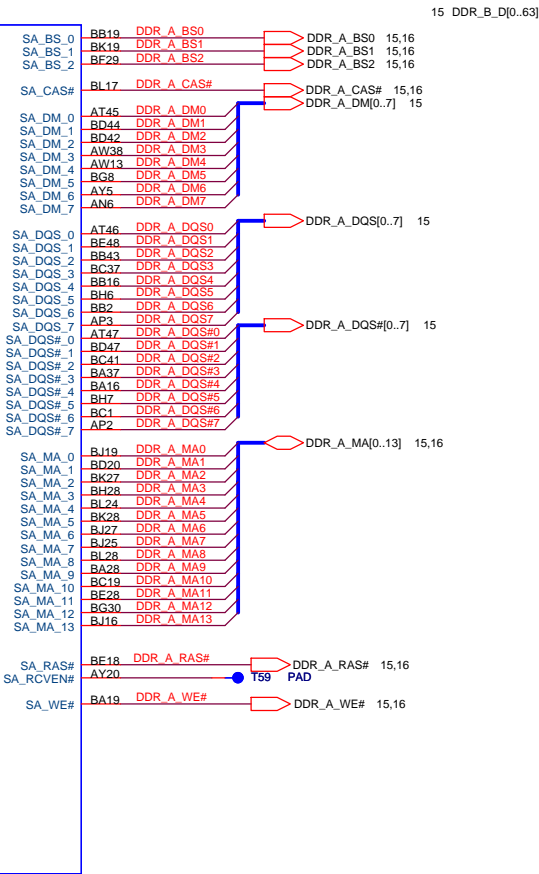
Rev: 1A

15 DDR_A_D[0..63]

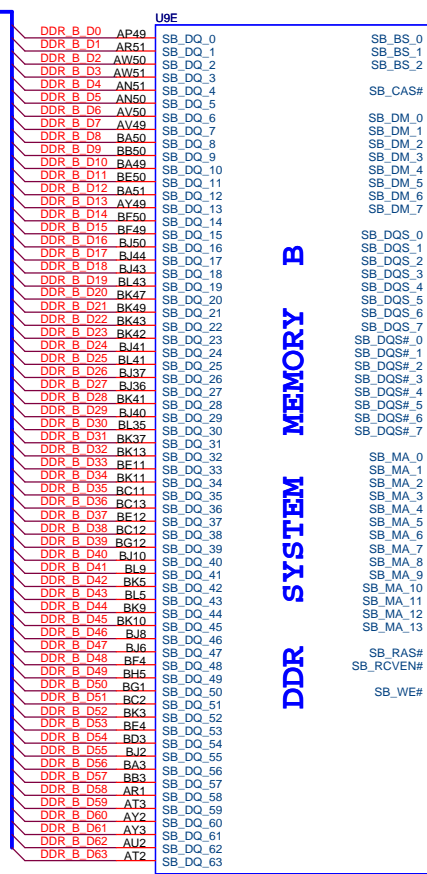


DDR SYSTEM MEMORY A

CRESTLINE_1p0

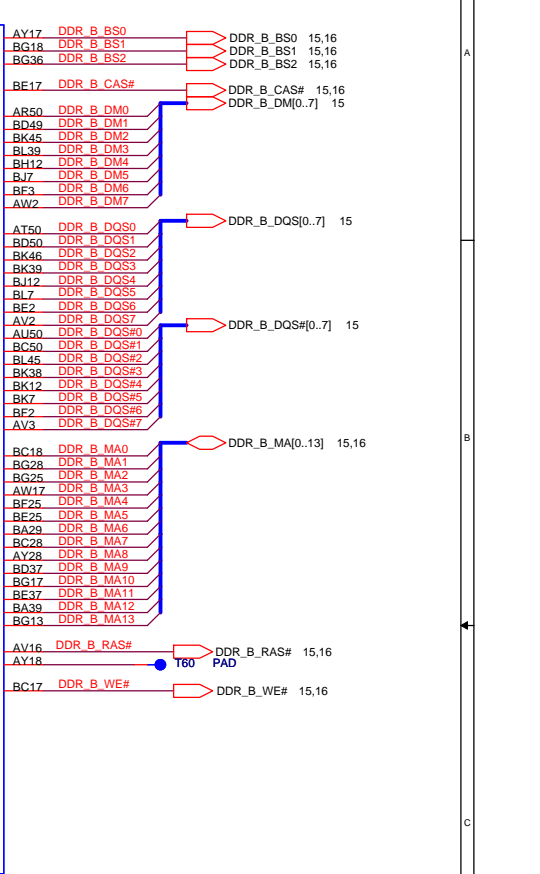


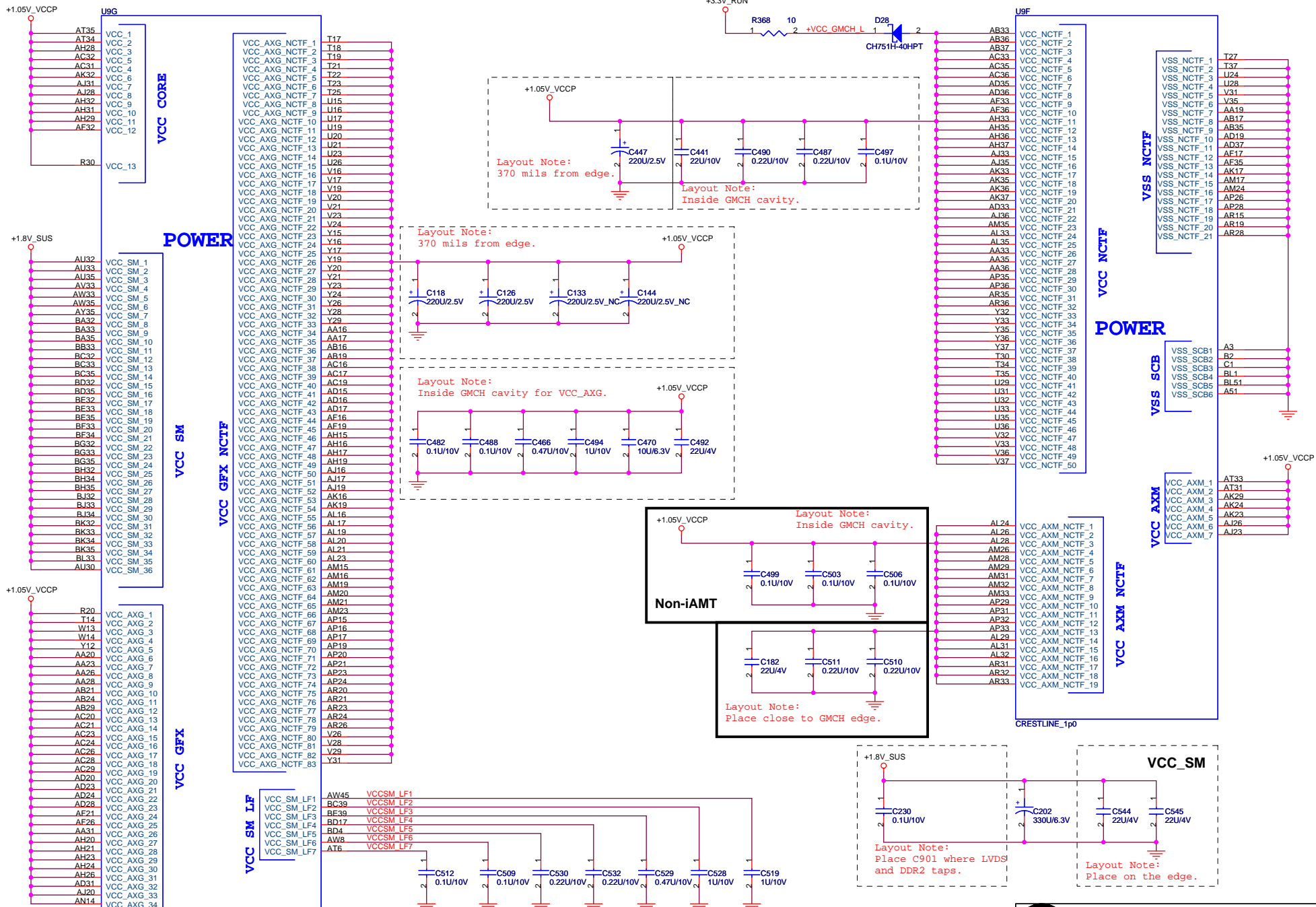
15 DDR_B_D[0..63]

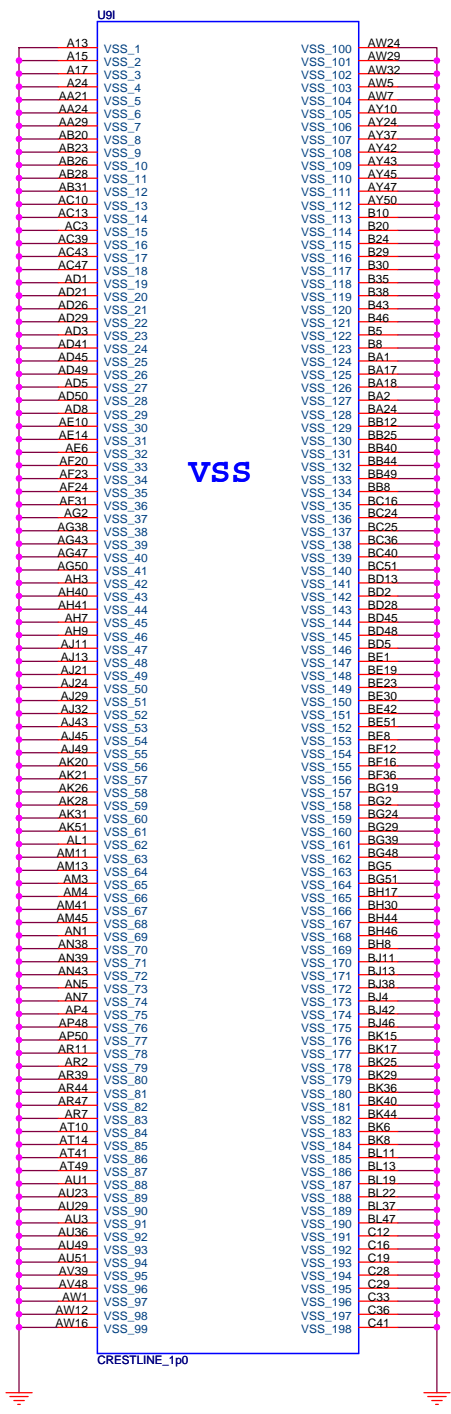


DDR SYSTEM MEMORY B

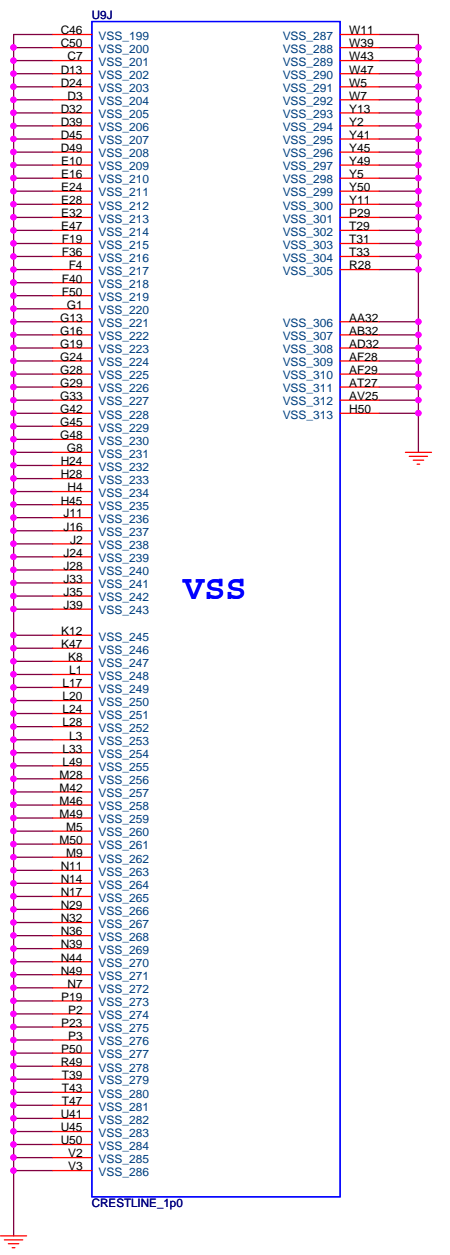
CRESTLINE_1p0







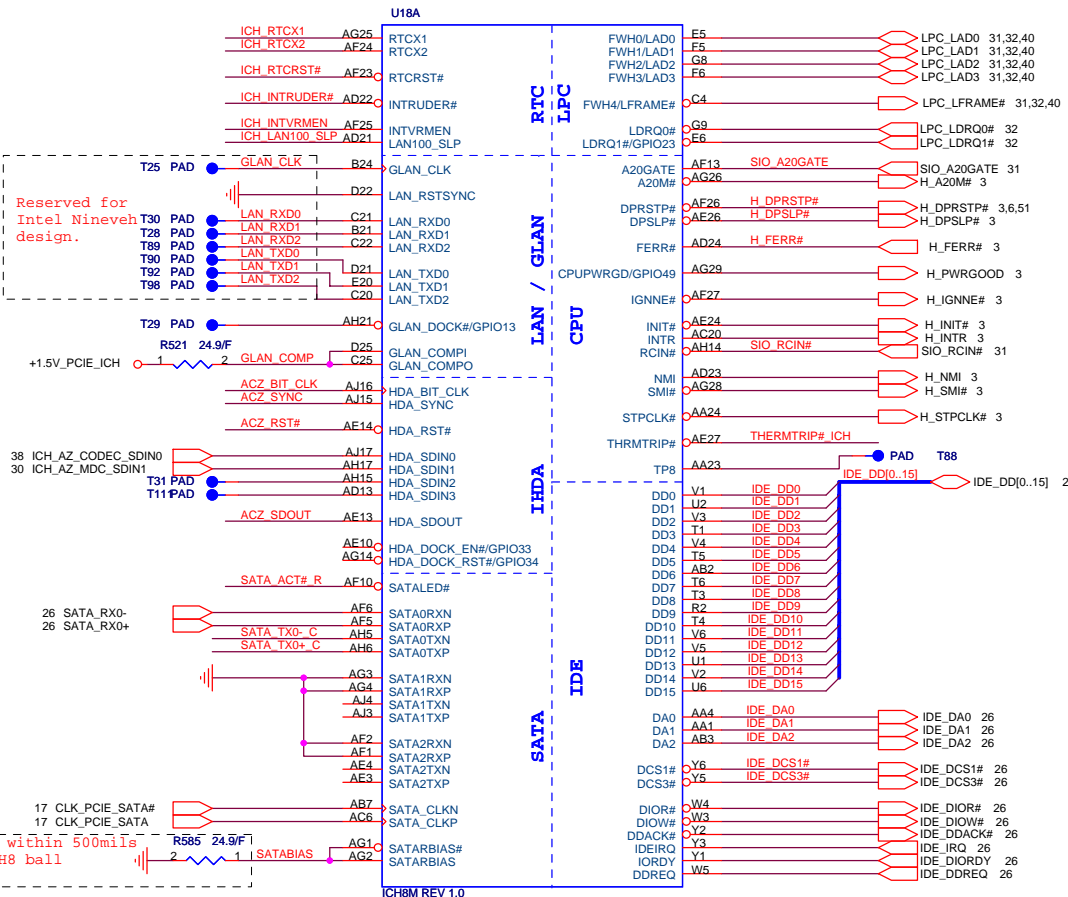
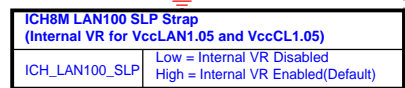
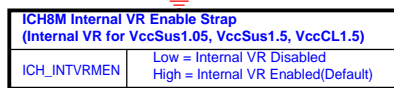
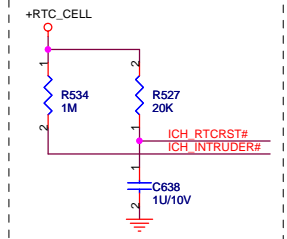
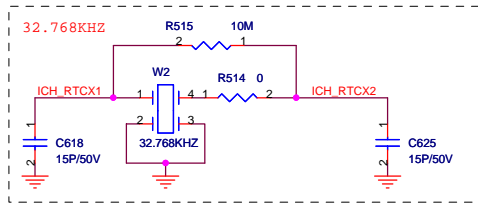
VSS



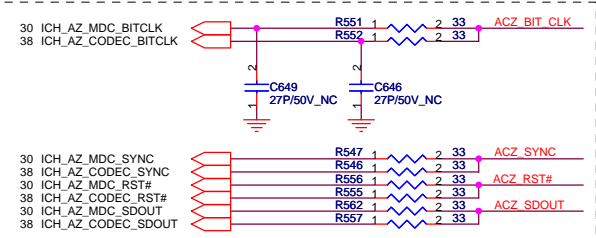
VSS



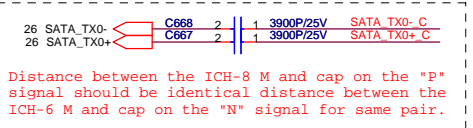
Title		
Crestline (VSS)		
Size	Document Number	Rev
	JM7	1A
Date:	Wednesday, June 28, 2006	Sheet 10 of 57



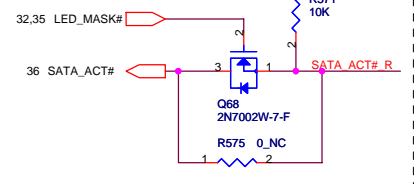
Reserved for Intel Nineveh design.



Place all series terms close to ICH8 except for SDIN input lines, which should be close to source. Placement of R292, R286, R283 & R289 should equal distance to the T split trace point as R291, R285, R284 & R290 respective. Basically, keep the same distance from T for all series termination resistors.

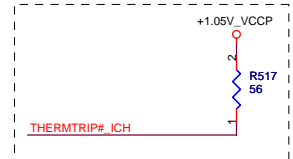
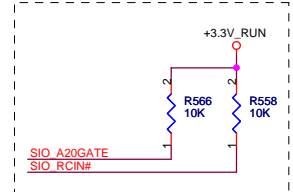
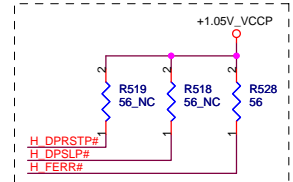
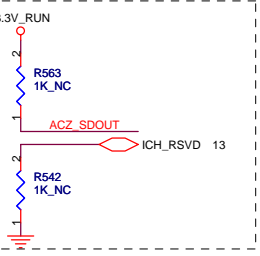


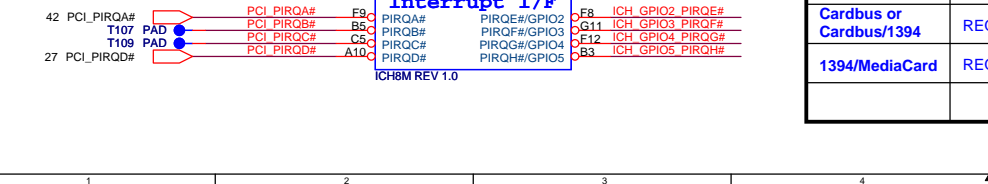
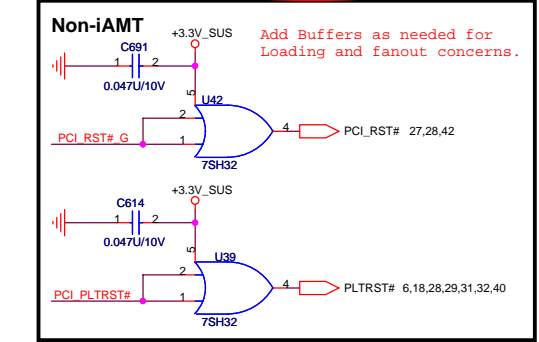
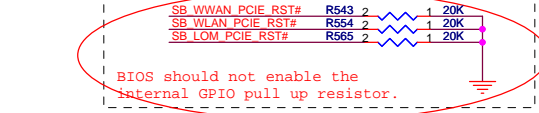
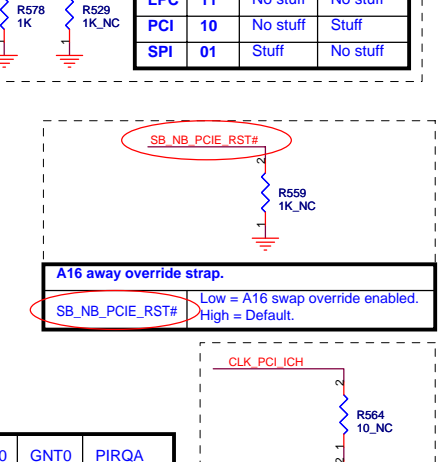
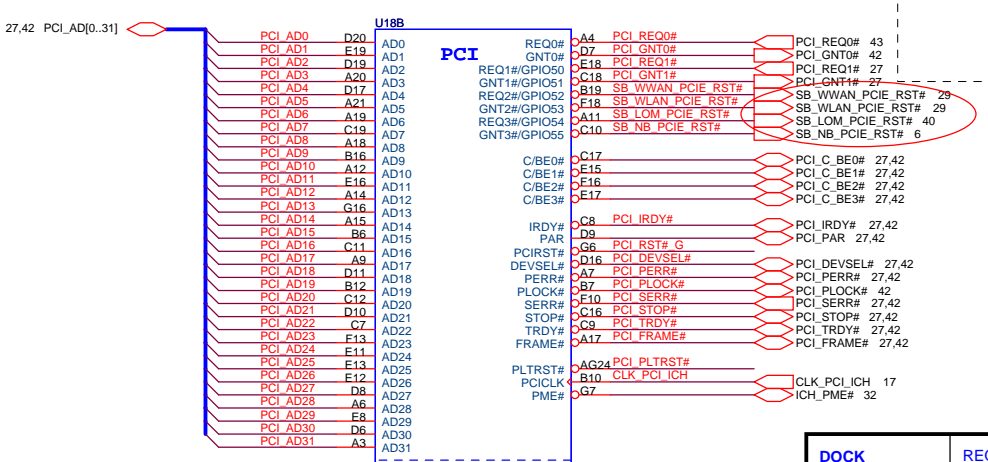
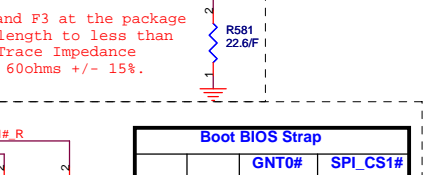
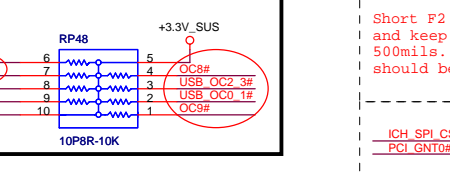
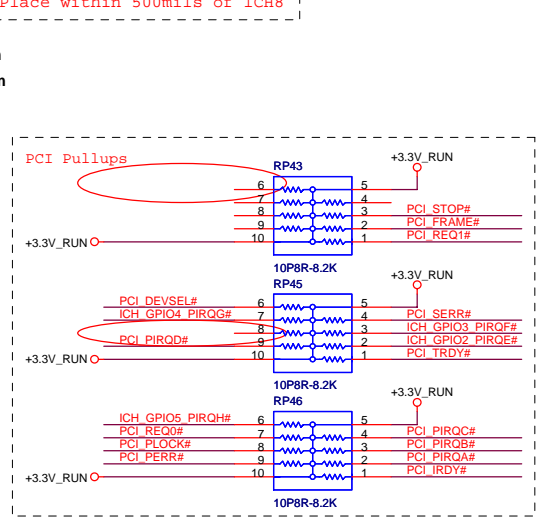
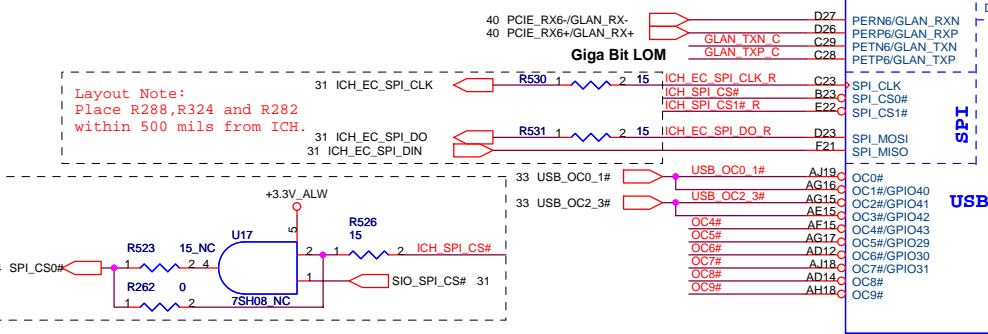
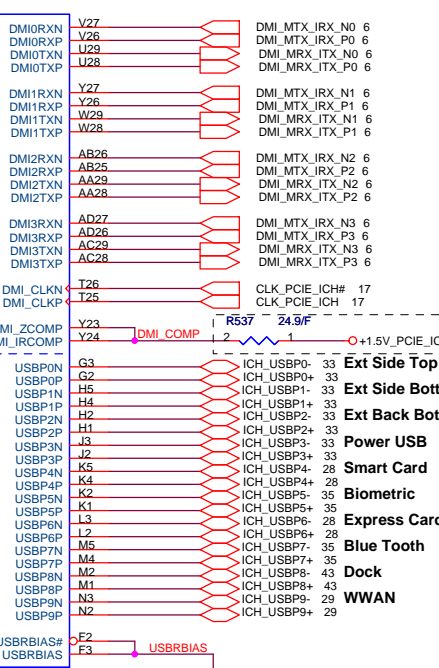
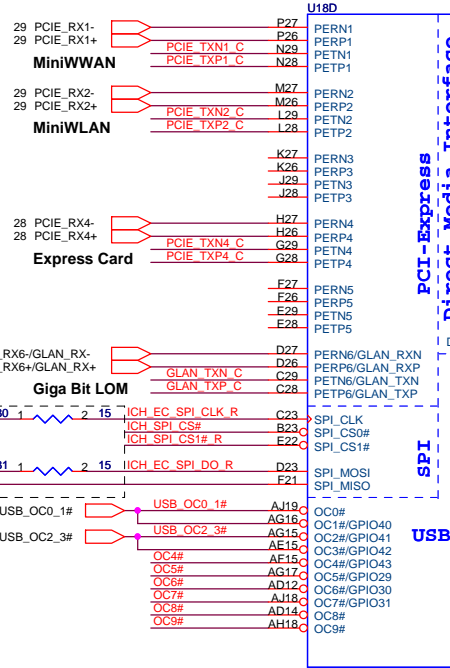
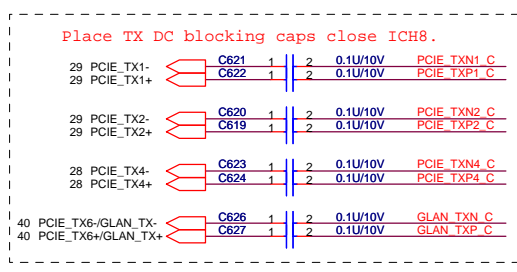
Distance between the ICH-8 M and cap on the "P" signal should be identical distance between the ICH-6 M and cap on the "N" signal for same pair.



XOR Chain Entrance Strap

ICH_RSVD	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (Default)
1	1	Set PCIE port config bit 1



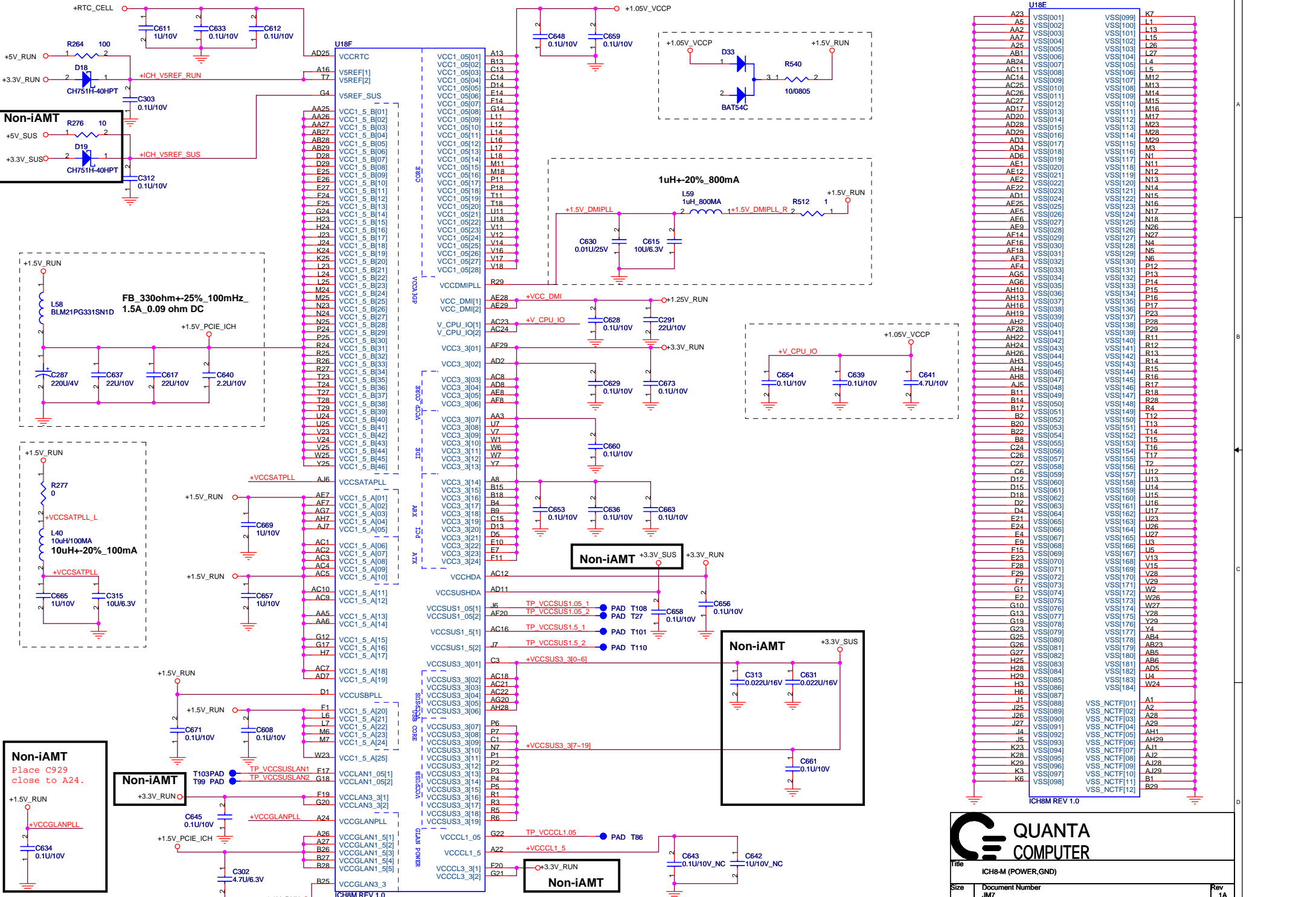


QUANTA COMPUTER

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Size: Document Number JM17 Rev 1A

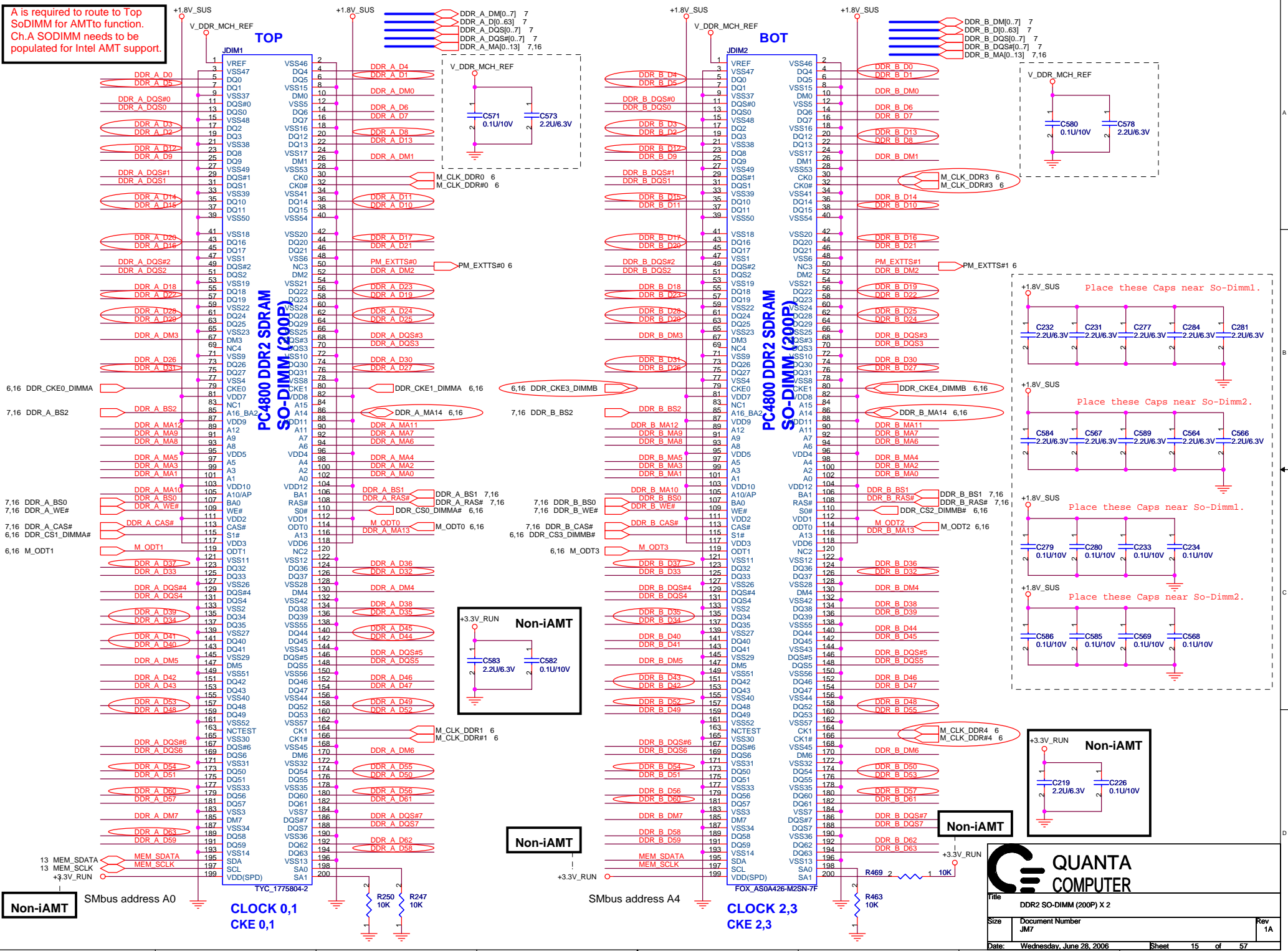
Date: Wednesday, June 28, 2006 Sheet 12 of 57



U18E	VSSJ[099]	K7
A23	VSSJ[001]	L1
A5	VSSJ[002]	L13
AA2	VSSJ[003]	L15
AA7	VSSJ[004]	L26
A25	VSSJ[005]	L27
AB1	VSSJ[006]	L4
AB24	VSSJ[007]	L5
AC11	VSSJ[008]	M12
AC14	VSSJ[009]	M13
AC25	VSSJ[010]	M14
AC26	VSSJ[011]	M15
AC27	VSSJ[012]	M16
AD17	VSSJ[013]	M17
AD20	VSSJ[014]	M23
AD28	VSSJ[015]	M28
AD29	VSSJ[016]	M29
AD3	VSSJ[017]	M3
AD4	VSSJ[018]	N1
AD6	VSSJ[019]	N11
AE1	VSSJ[020]	N18
AE12	VSSJ[021]	N19
AE2	VSSJ[022]	N14
AE22	VSSJ[023]	N15
AD1	VSSJ[024]	N16
AE25	VSSJ[025]	N17
AE5	VSSJ[026]	N8
AE6	VSSJ[027]	N25
AE9	VSSJ[028]	N26
AF14	VSSJ[029]	N27
AF16	VSSJ[030]	N4
AF18	VSSJ[031]	N5
AF3	VSSJ[032]	N6
AF4	VSSJ[033]	P12
AG5	VSSJ[034]	P13
AG6	VSSJ[035]	P14
AH10	VSSJ[036]	P15
AH13	VSSJ[037]	P16
AH16	VSSJ[038]	P17
AH19	VSSJ[039]	P28
AH2	VSSJ[040]	P29
AF28	VSSJ[041]	R11
AH22	VSSJ[042]	R12
AH24	VSSJ[043]	R14
AH26	VSSJ[044]	R15
AH3	VSSJ[045]	R16
AH4	VSSJ[046]	R17
AJ5	VSSJ[047]	R18
B11	VSSJ[048]	R28
B14	VSSJ[049]	R22
B17	VSSJ[050]	T12
B2	VSSJ[051]	T13
B20	VSSJ[052]	T14
VCC3_3[08]	VSSJ[053]	T15
VSSJ[054]	VSSJ[054]	T16
B8	VSSJ[055]	T17
C24	VSSJ[056]	T2
C27	VSSJ[057]	T12
C6	VSSJ[058]	T13
D12	VSSJ[059]	T14
D15	VSSJ[060]	T15
D18	VSSJ[061]	T16
D2	VSSJ[062]	T17
D4	VSSJ[063]	U23
E21	VSSJ[064]	U26
E24	VSSJ[065]	U27
E4	VSSJ[066]	U3
E9	VSSJ[067]	U33
F15	VSSJ[068]	U34
E23	VSSJ[069]	U35
F28	VSSJ[070]	U36
F29	VSSJ[071]	U37
F7	VSSJ[072]	W2
G1	VSSJ[073]	W26
F2	VSSJ[074]	W27
G10	VSSJ[075]	W28
G13	VSSJ[076]	W29
G19	VSSJ[077]	Y4
G23	VSSJ[078]	Y4
G25	VSSJ[079]	Y4
G26	VSSJ[080]	Y4
G27	VSSJ[081]	Y4
H25	VSSJ[082]	Y4
H28	VSSJ[083]	Y4
H29	VSSJ[084]	Y4
H3	VSSJ[085]	Y4
H6	VSSJ[086]	Y4
H9	VSSJ[087]	Y4
J1	VSSJ[088]	Y4
J25	VSSJ[089]	Y4
J26	VSSJ[090]	Y4
J27	VSSJ[091]	Y4
J4	VSSJ[092]	Y4
J5	VSSJ[093]	Y4
K23	VSSJ[094]	Y4
K28	VSSJ[095]	Y4
P2	VSSJ[096]	Y4
K29	VSSJ[097]	Y4
K3	VSSJ[098]	Y4
K6	VSSJ[099]	Y4
VSSJ[099]	VSS_NCTF[01]	A1
VSSJ[002]	VSS_NCTF[02]	A2
VSSJ[003]	VSS_NCTF[03]	A29
VSSJ[004]	VSS_NCTF[04]	AH1
VSSJ[005]	VSS_NCTF[05]	AH29
VSSJ[006]	VSS_NCTF[06]	AH11
VSSJ[007]	VSS_NCTF[07]	AH2
VSSJ[008]	VSS_NCTF[08]	AH29
VSSJ[009]	VSS_NCTF[09]	AH29
VSSJ[010]	VSS_NCTF[10]	B1
VSSJ[011]	VSS_NCTF[11]	B29
VSSJ[012]	VSS_NCTF[12]	B29

QUANTA COMPUTER	
Title: ICH8-M (POWER,GND)	
Size: JM7	Document Number: Rev 1A
Date: Wednesday, June 28, 2006	
Sheet: 14 of 57	

A is required to route to Top SoDIMM for AMTto function. Ch.A SODIMM needs to be populated for Intel AMT support.



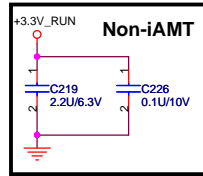
Non-iAMT

CLOCK 0,1
CKE 0,1

Non-iAMT

CLOCK 2,3
CKE 2,3

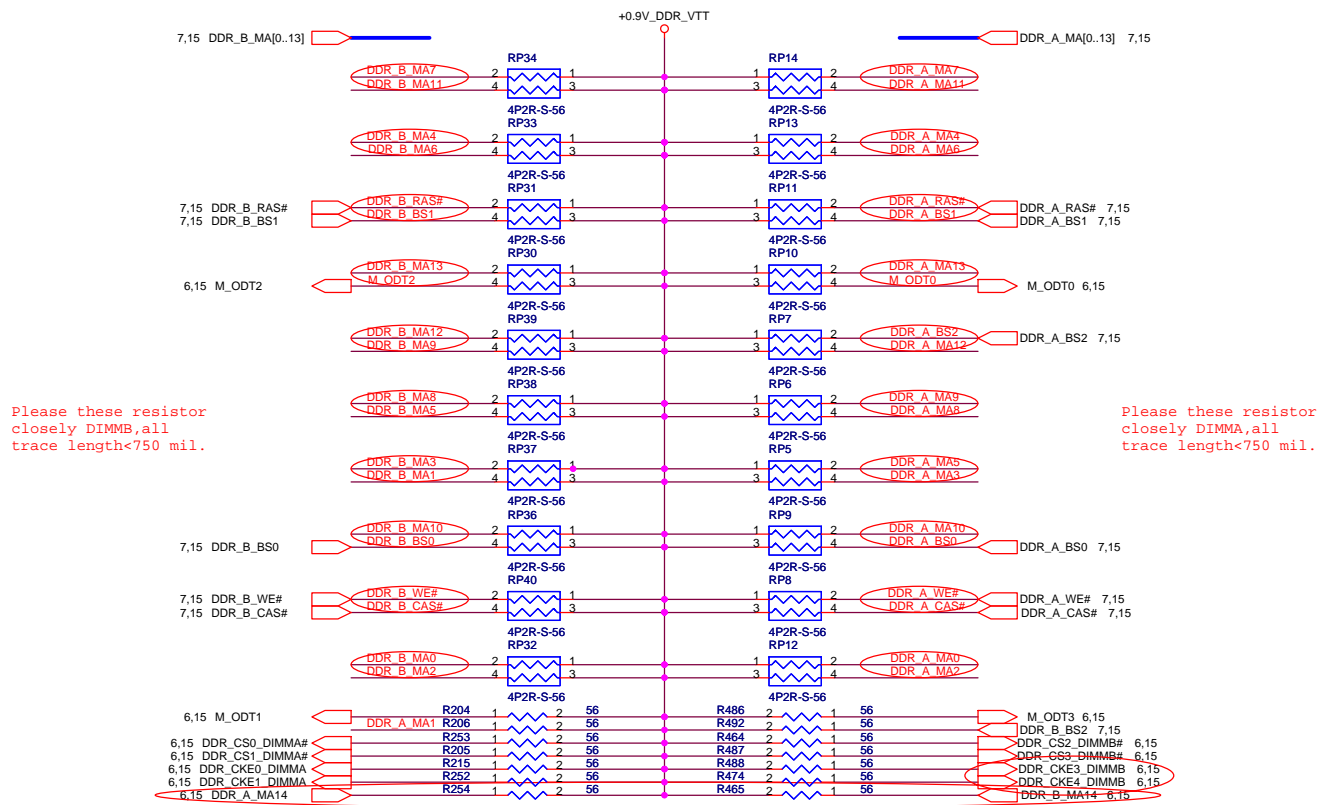
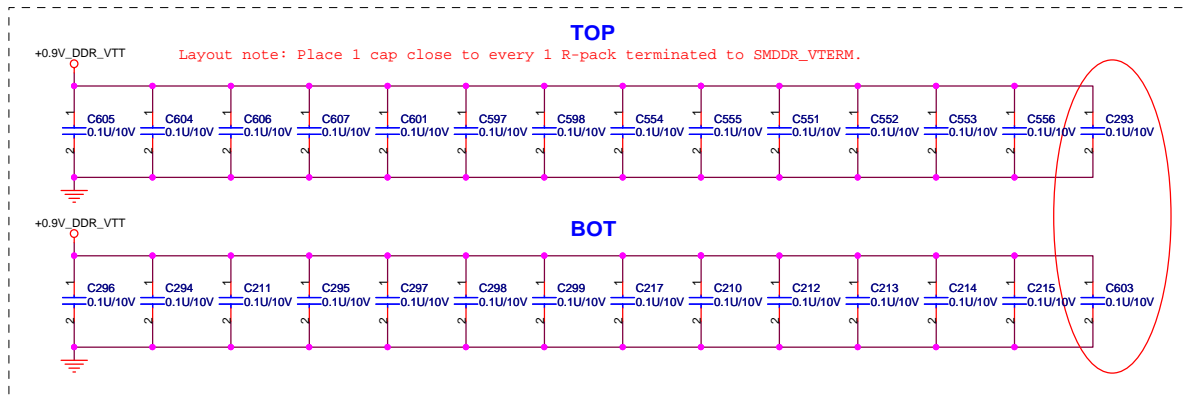
Non-iAMT



QUANTA COMPUTER

Title: DDR2 SO-DIMM (200P) X 2

Size	Document Number JM17	Rev 1A
Date:	Wednesday, June 28, 2006	Sheet 15 of 57

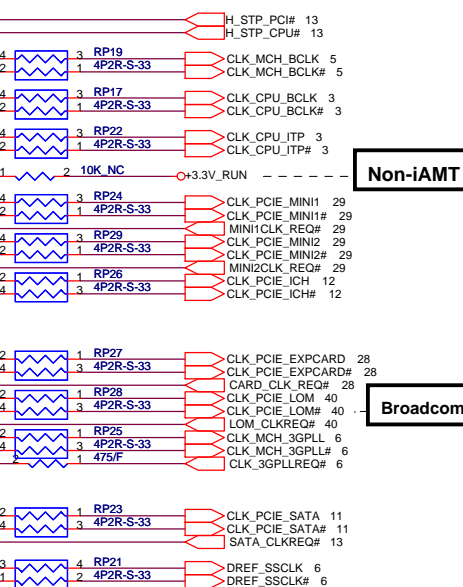
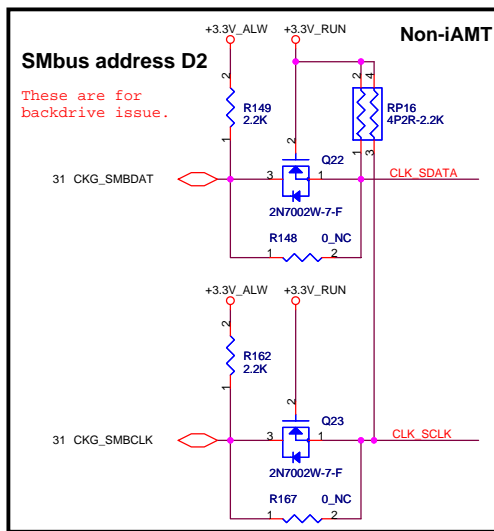
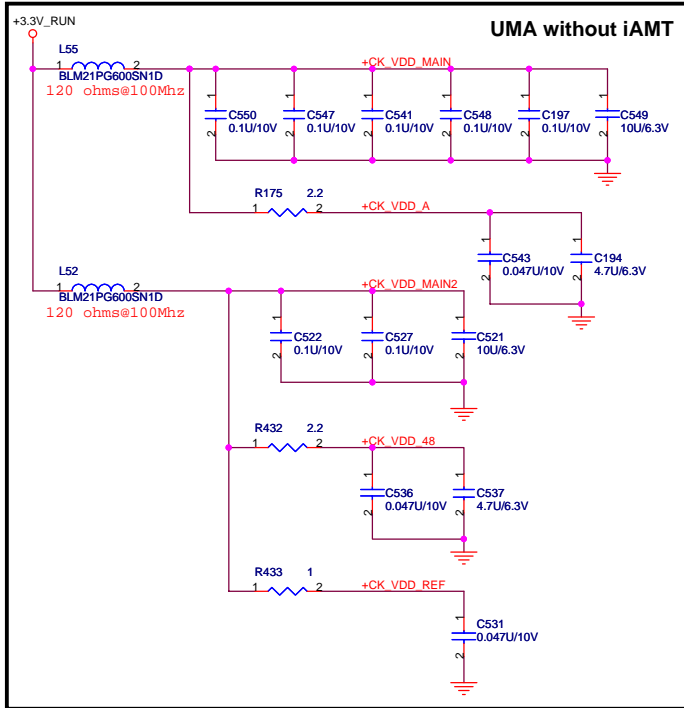
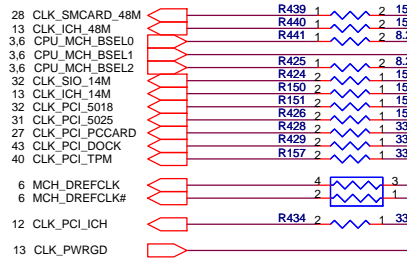
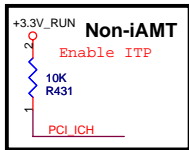
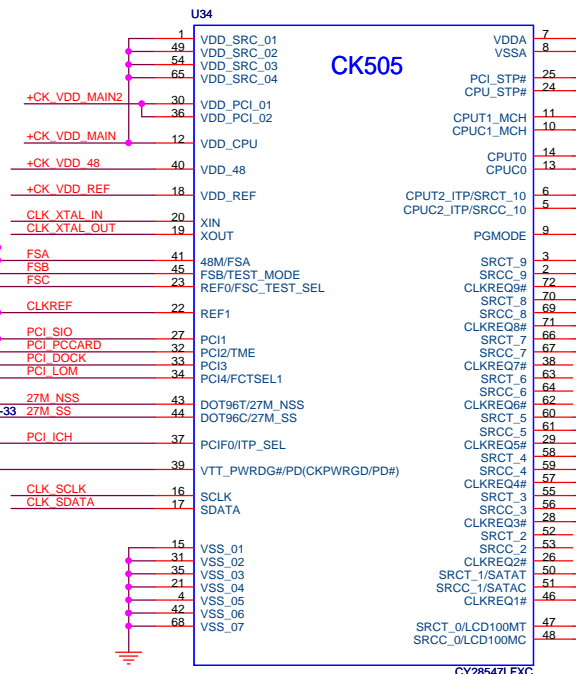
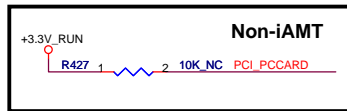
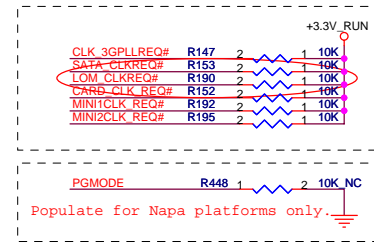
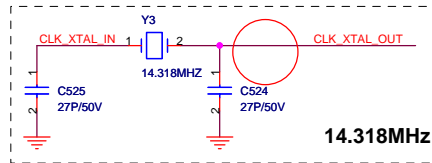
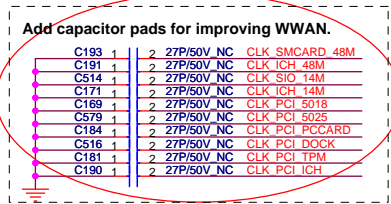
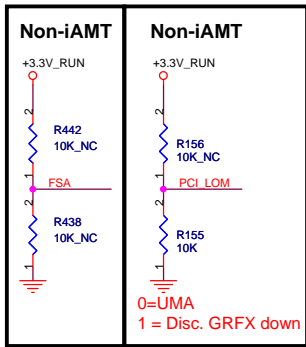


**QUANTA
COMPUTER**

Title: **DDR2 RES ARRAY**

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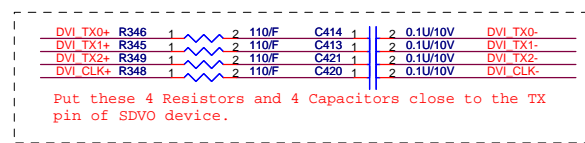
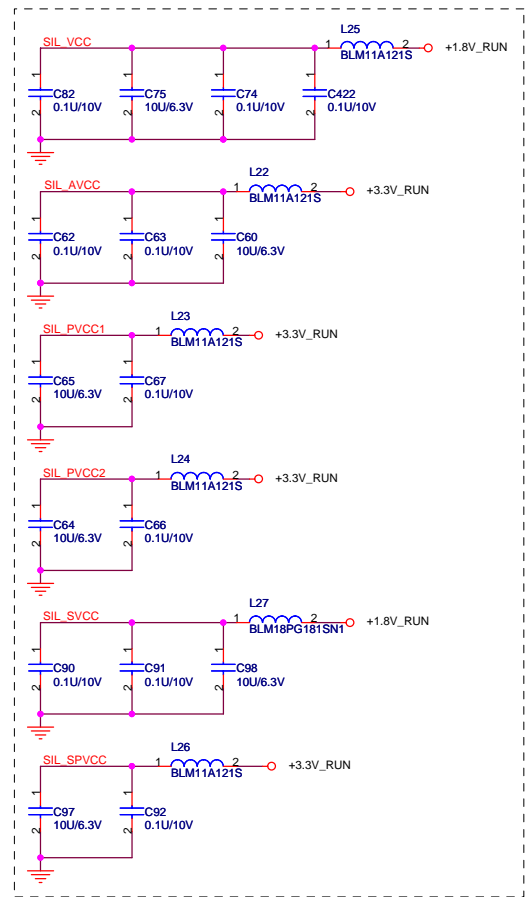
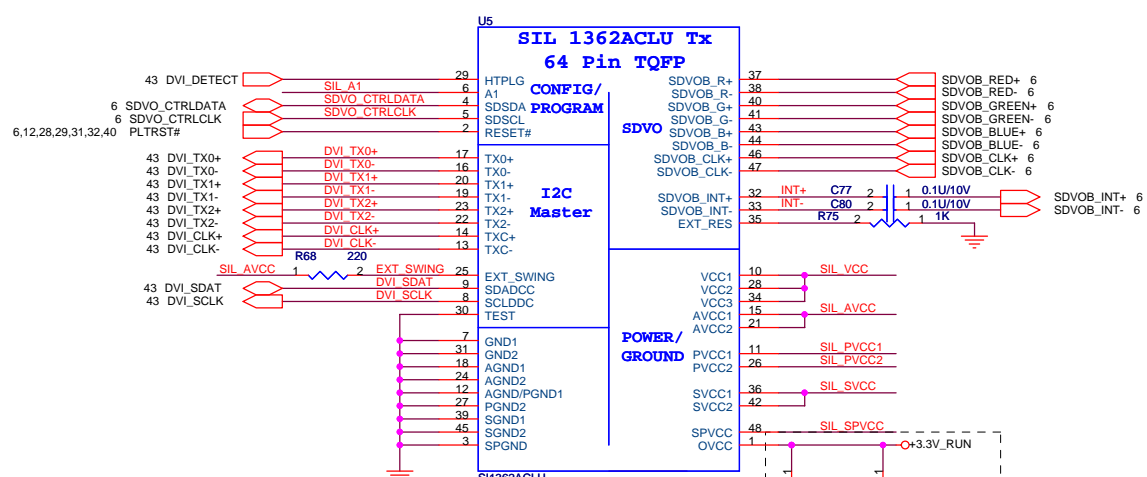
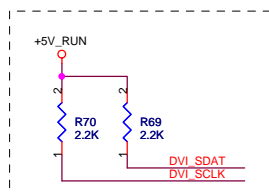
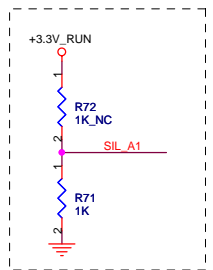
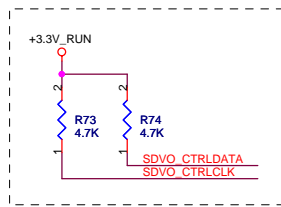


FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	0	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

PCI_LOM = FCTSEL1

FCTSEL1 (PIN34)	PIN43	PIN44	PIN47	PIN48
0=UMA	DOT96T	DOT96C	96/100M_T	96/100M_C
1 = Disc. GRFX down	27Mout	27MSSout	SRCT0	SRCC0







Placed this capacitor close to OVCC.




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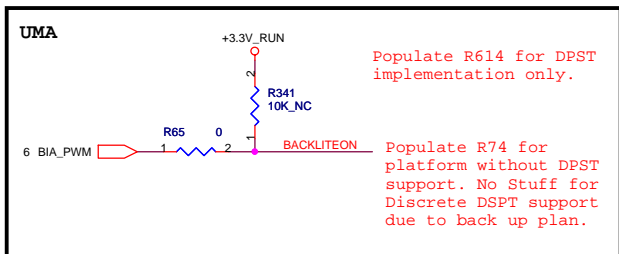
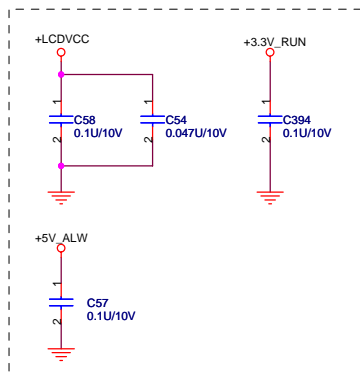
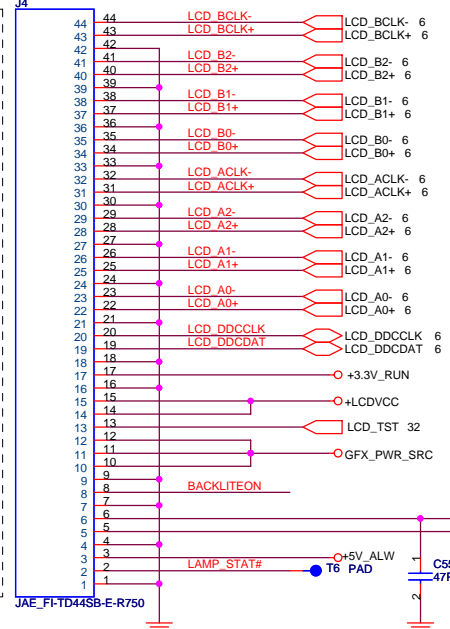
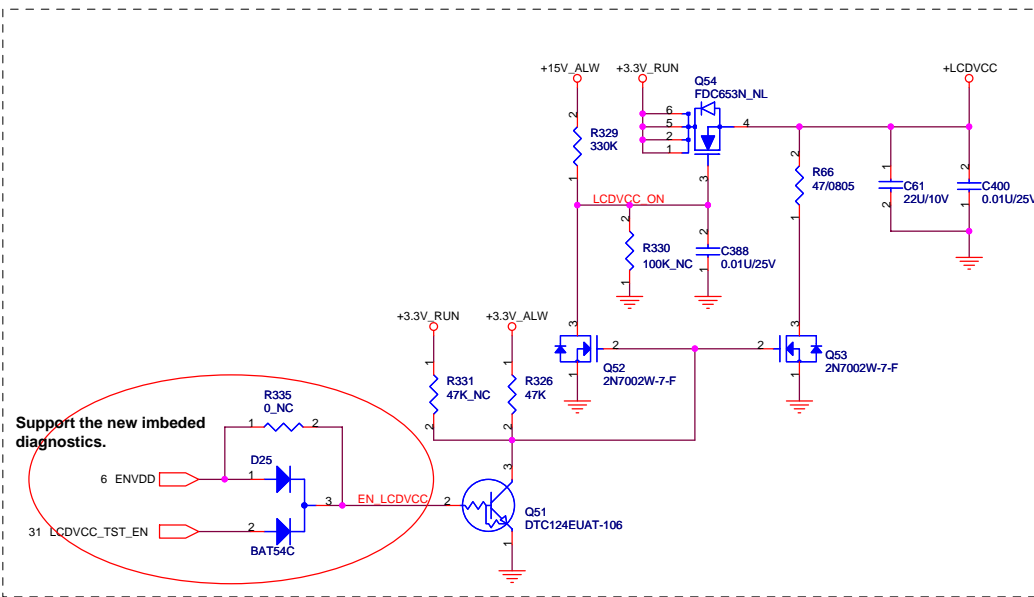
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Title		
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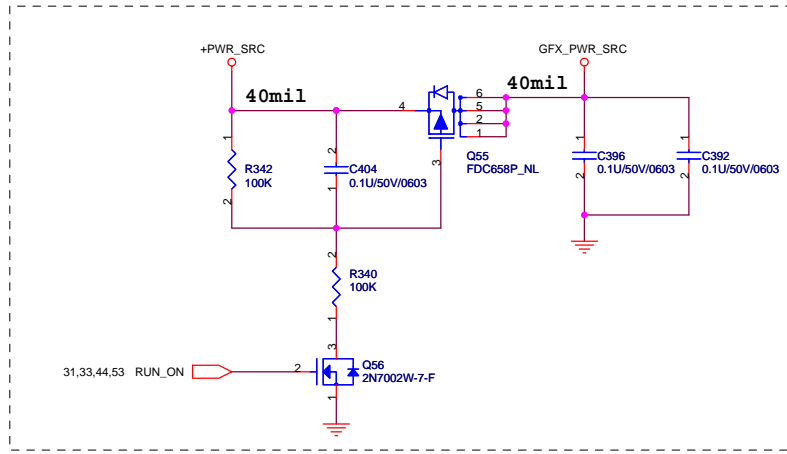
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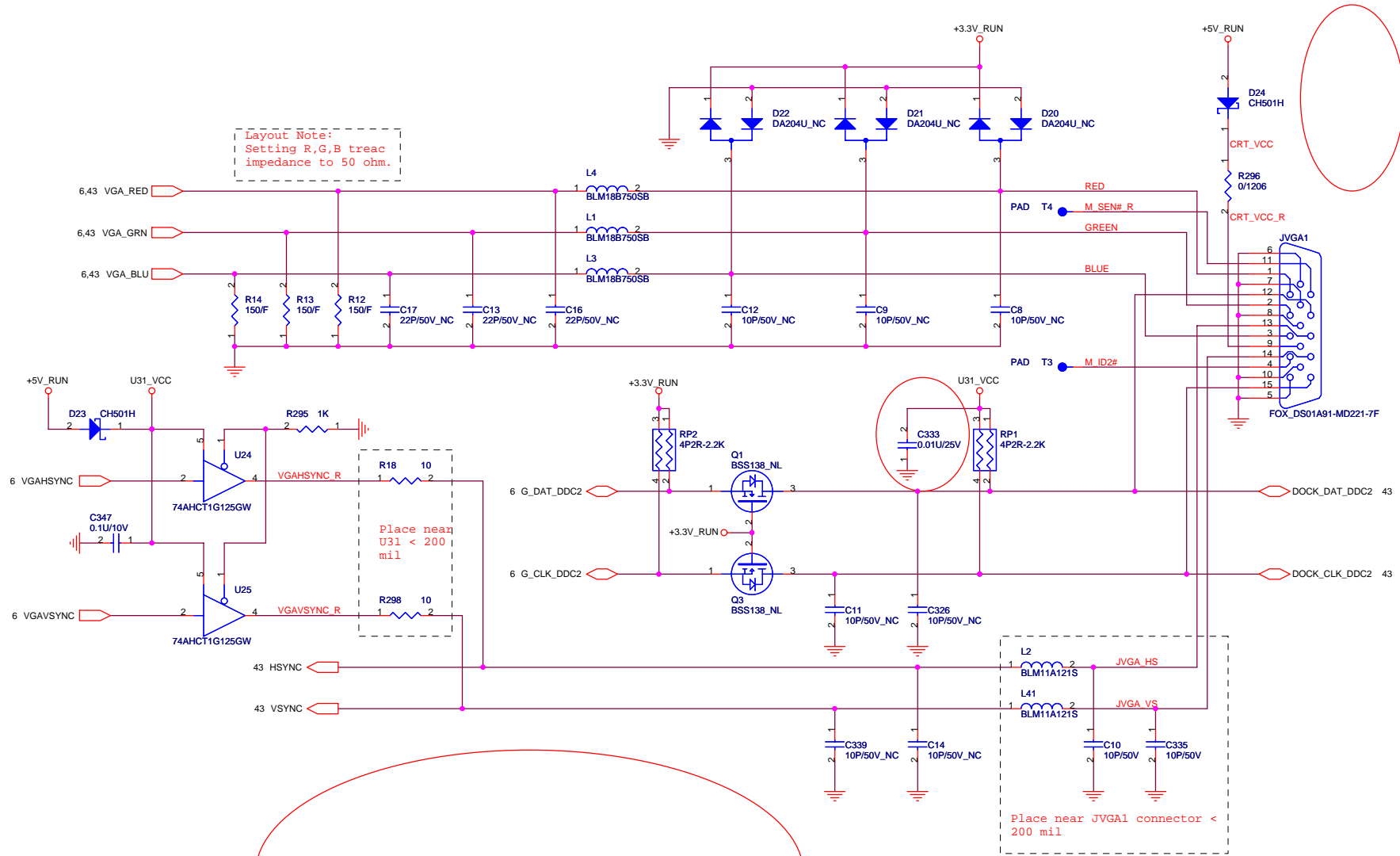
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Shunt capacitors on LVDS for improving WWAN.

LCD B0-	C399	1	2	3.3P/50V	NC	LCD B0+
LCD B1-	C398	1	2	3.3P/50V	NC	LCD B1+
LCD B2-	C384	1	2	3.3P/50V	NC	LCD B2+
LCD BCLK-	C386	1	2	3.3P/50V	NC	LCD BCLK+
LCD A0-	C403	1	2	3.3P/50V	NC	LCD A0+
LCD A1-	C402	1	2	3.3P/50V	NC	LCD A1+
LCD A2-	C397	1	2	3.3P/50V	NC	LCD A2+
LCD ACLK-	C393	1	2	3.3P/50V	NC	LCD ACLK+





Layout Note:
Setting R,G,B treac
impedance to 50 ohm.

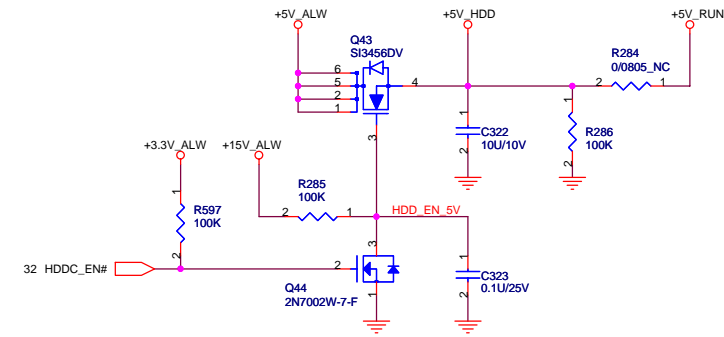
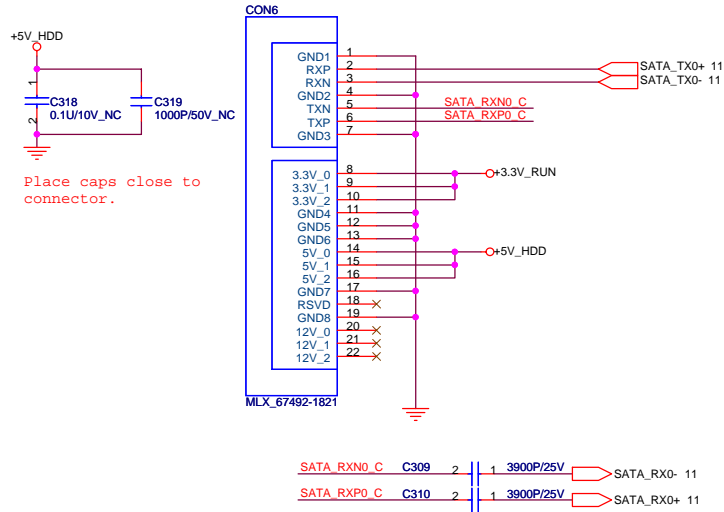
Place near
U31 < 200
mil

Place near JVGA1 connector <
200 mil

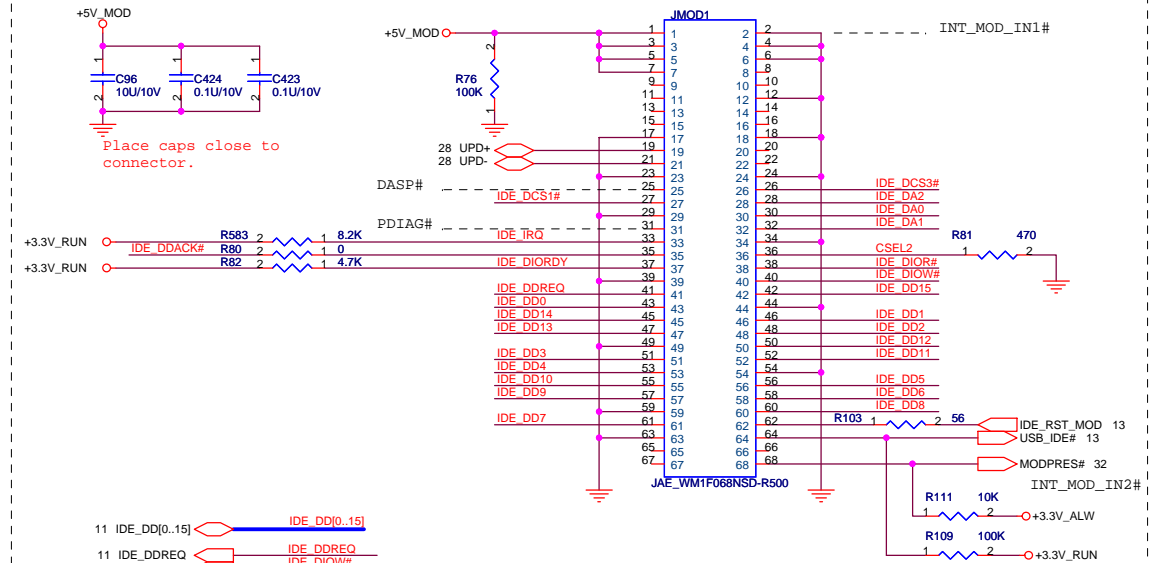


Title		CRT&TV CONN
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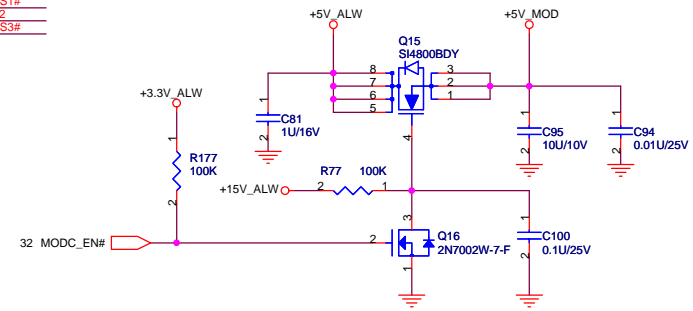
SATA Connector.

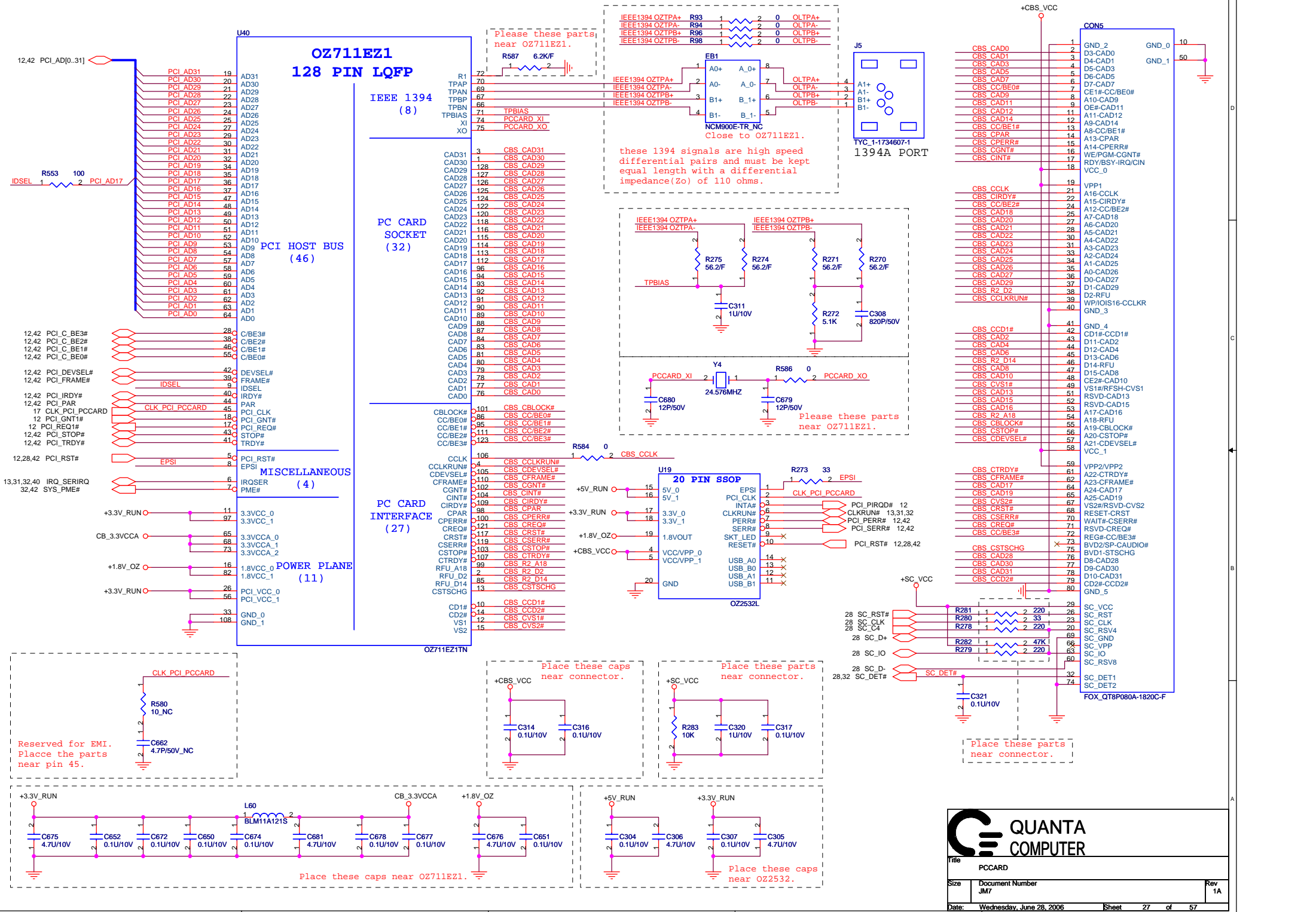


ODD Connector.



- 11 IDE_DD[0..15] IDE_DD[0..15]
- 11 IDE_DDREQ IDE_DDREQ
- 11 IDE_DDIOW# IDE_DDIOW#
- 11 IDE_DIOR# IDE_DIOR#
- 11 IDE_DIORDY IDE_DIORDY
- 11 IDE_DDACK# IDE_DDACK#
- 11 IDE_IRQ IDE_IRQ
- 11 IDE_DA1 IDE_DA1
- 11 IDE_DA0 IDE_DA0
- 11 IDE_DCS1# IDE_DCS1#
- 11 IDE_DA2 IDE_DA2
- 11 IDE_DCS3# IDE_DCS3#





QUANTA COMPUTER

Title: PCCARD

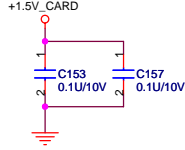
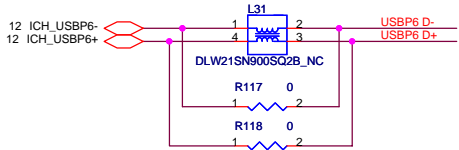
Size: Document Number JM7

Date: Wednesday, June 28, 2006

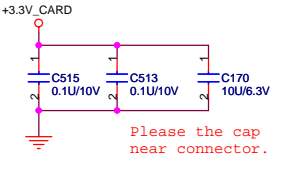
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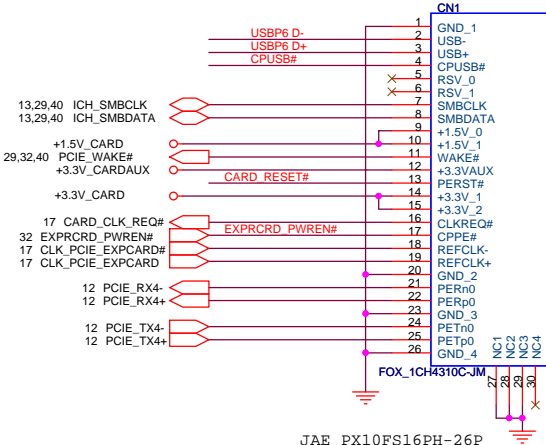
Express Card



Please the cap near connector.



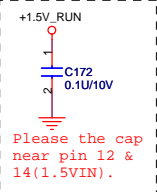
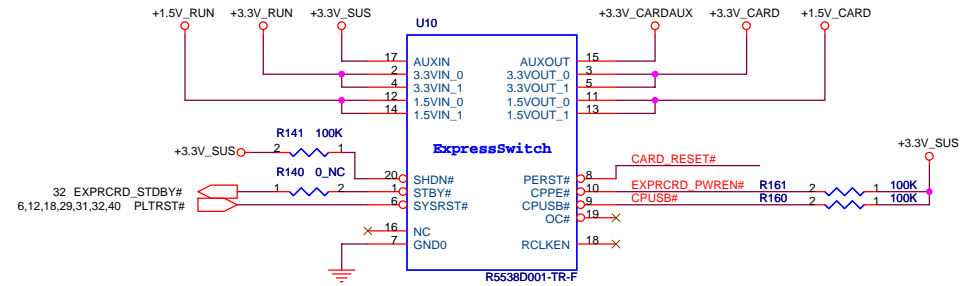
Please the cap near connector.



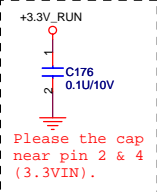
JAE PX10FS16PH-26P

PCI-Express TX and RX direct to connector.

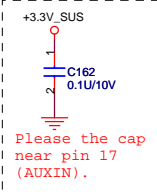
+1.5V_CARD Max. 650mA, Average 500mA.
+3V_CARD Max. 1300mA, Average 1000mA.



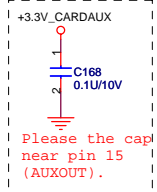
Please the cap near pin 12 & 14 (1.5VIN).



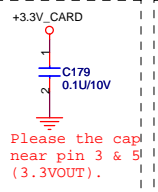
Please the cap near pin 2 & 4 (3.3VIN).



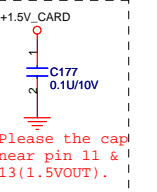
Please the cap near pin 17 (AUXIN).



Please the cap near pin 15 (AUXOUT).



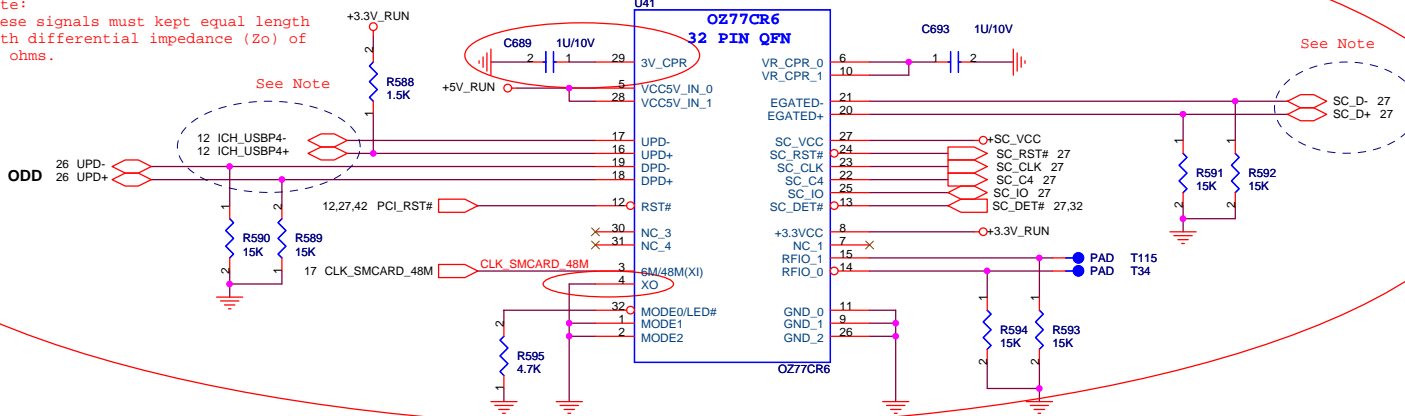
Please the cap near pin 3 & 5 (3.3VOUT).



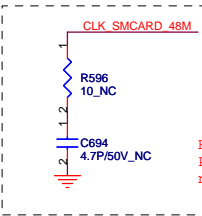
Please the cap near pin 11 & 13 (1.5VOUT).

Smart Card

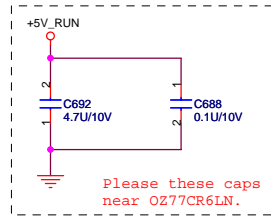
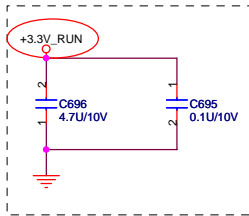
Note:
These signals must kept equal length with differential impedance (Z_0) of 90 ohms.



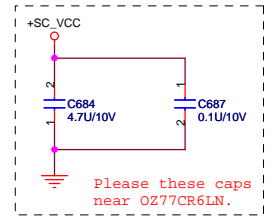
See Note



Reserved for EMI. Place the parts near pin 45.



Please these caps near OZ77CR6LN.

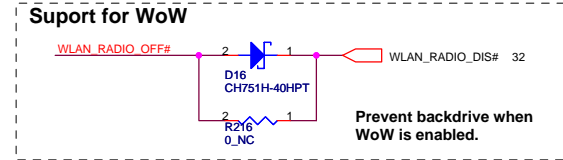
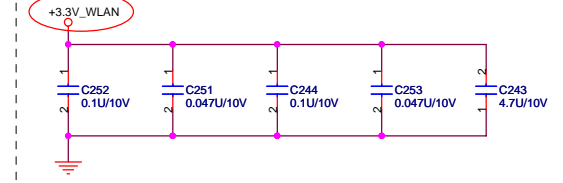
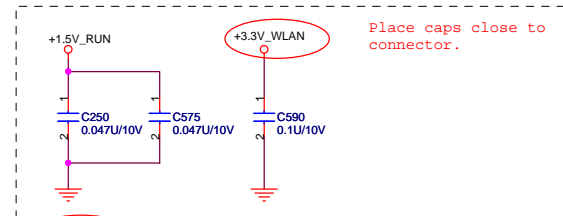
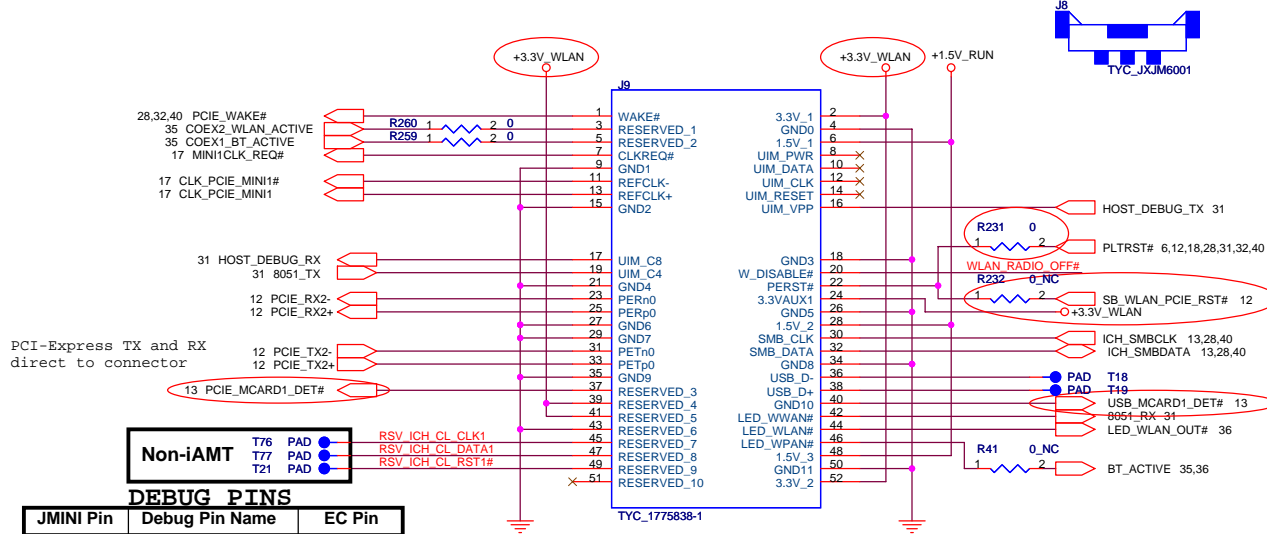


Please these caps near OZ77CR6LN.

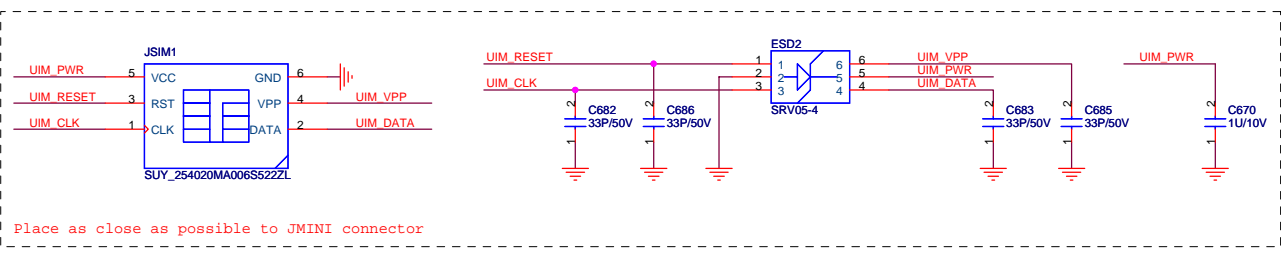
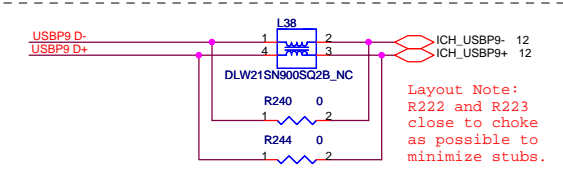
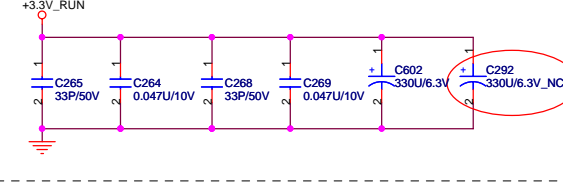
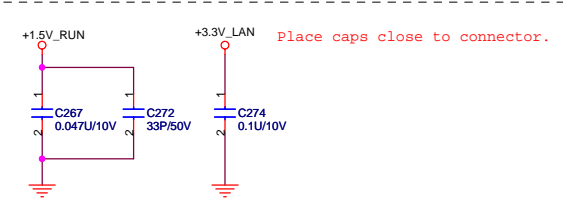
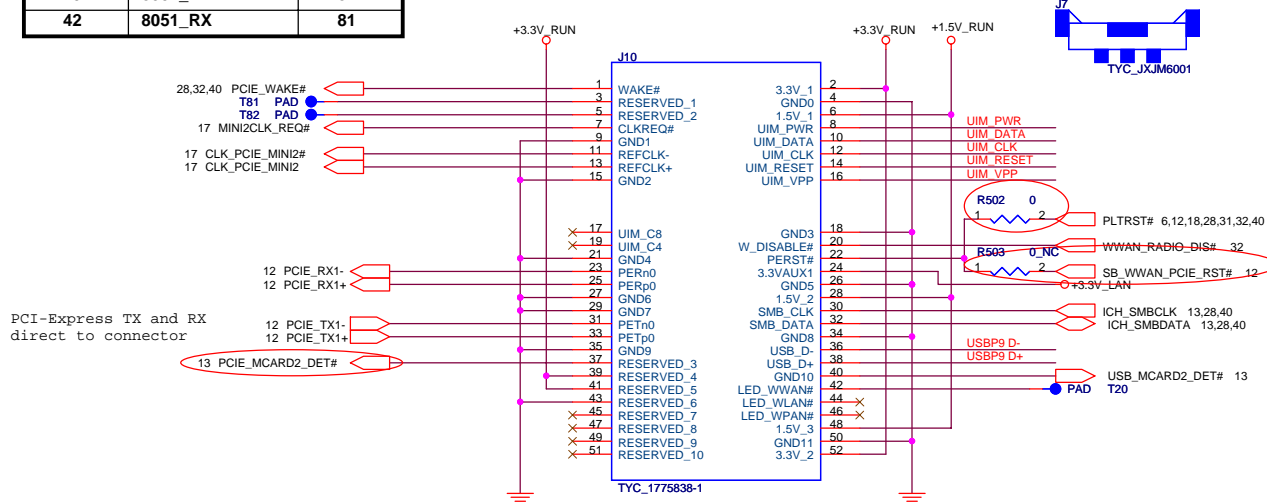


Title ExpressCard/SmartCard		
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MiniCard WLAN connector



MiniCard WWAN connector



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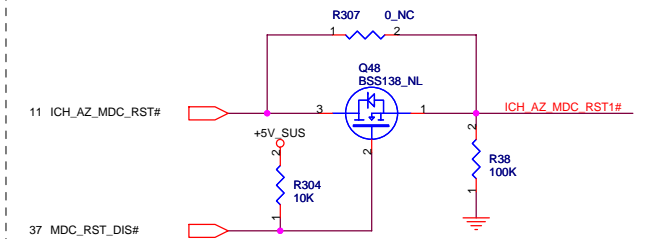
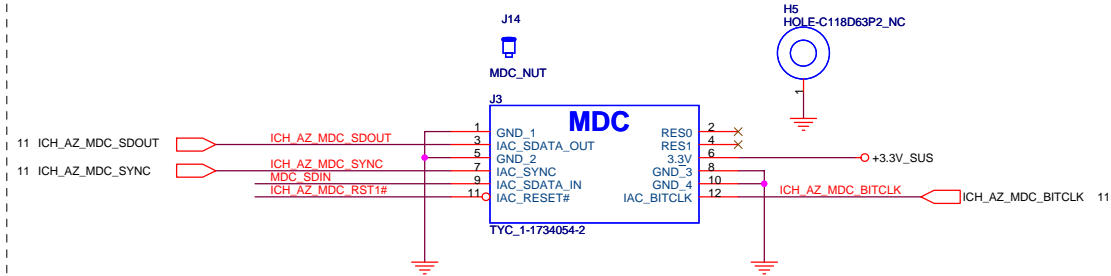
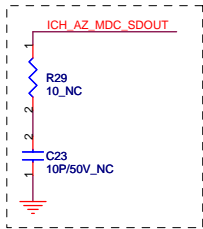
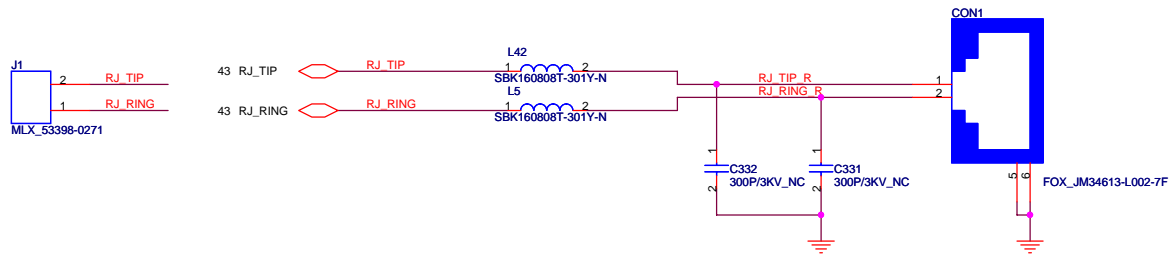
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Size: Document Number JM7

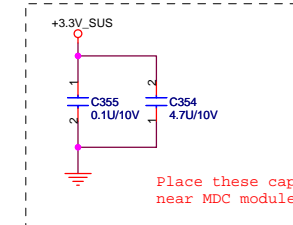
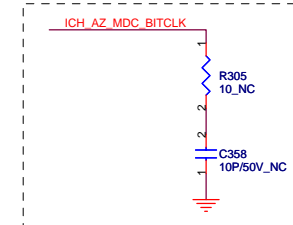
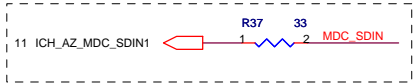
Date: Wednesday, June 28, 2006

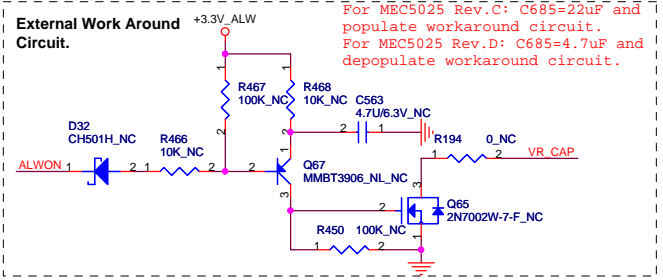
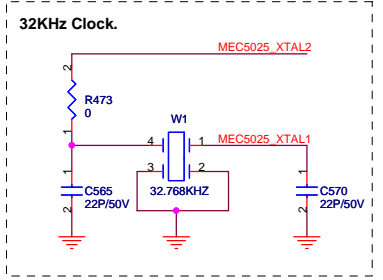
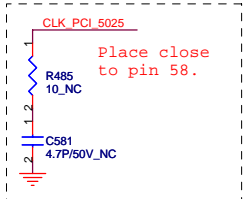
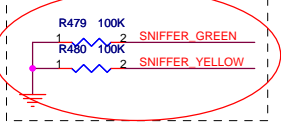
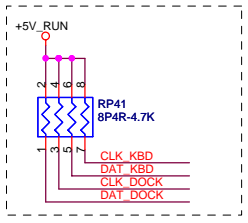
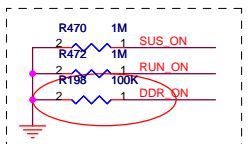
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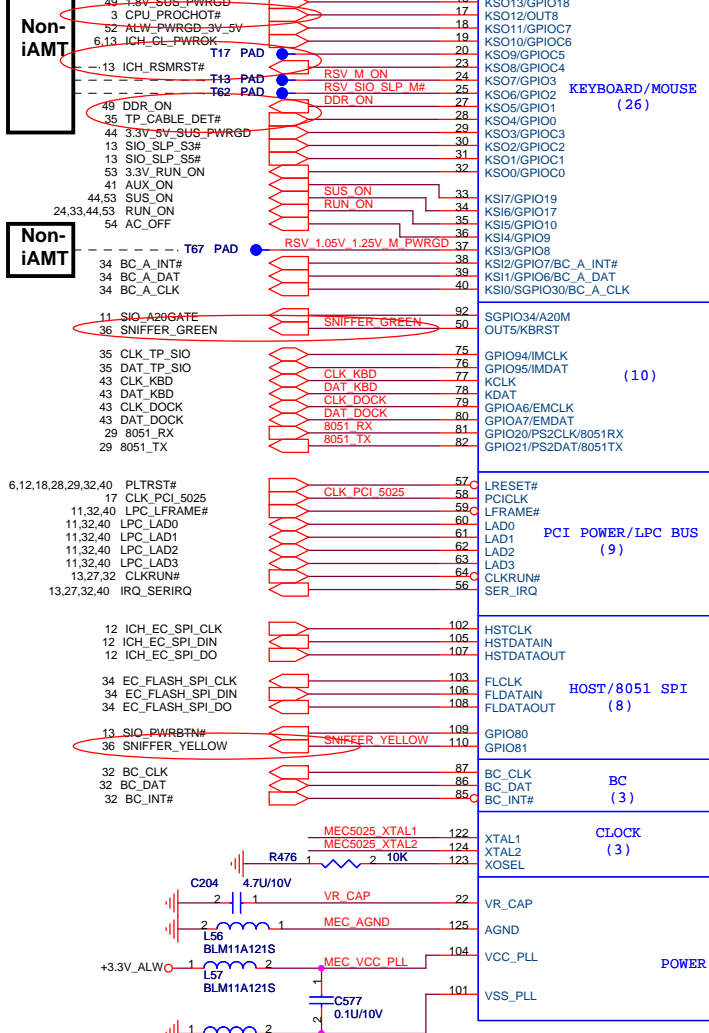


NOTE : MDC DISABLE
 If platform requires MDC disable, populate this circuit.
 If MDC disable isn't required, connect ICH_AZ_MDC_RST# directly to JMDC connector.

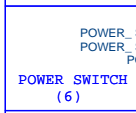




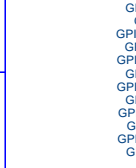
MEC5025 EC-08 128 PIN VTQFP



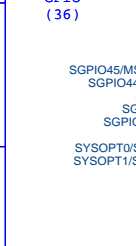
POWER PLANES (6)



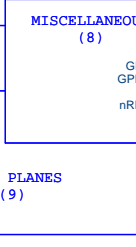
ACCESS BUS (4)



GPIO (36)



MISCELLANEOUS (8)



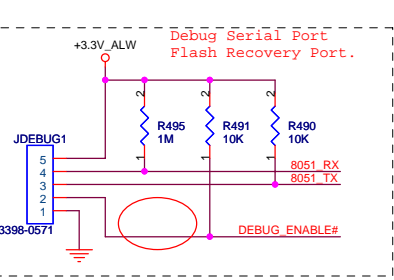
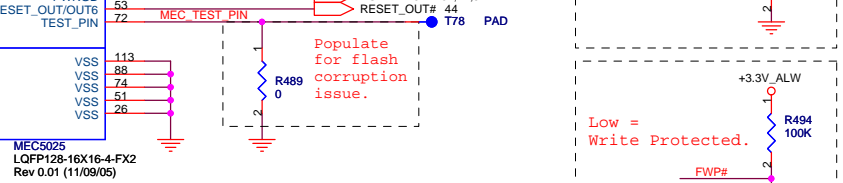
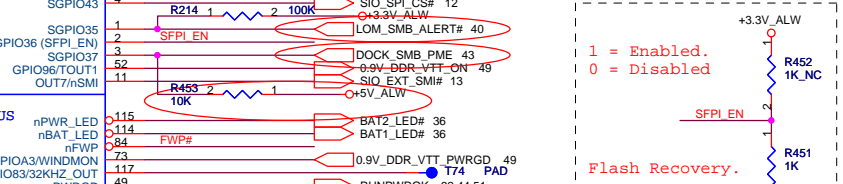
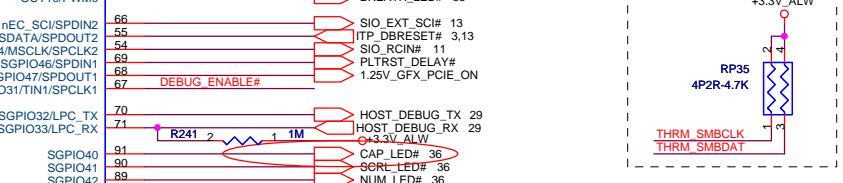
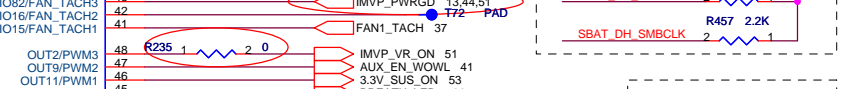
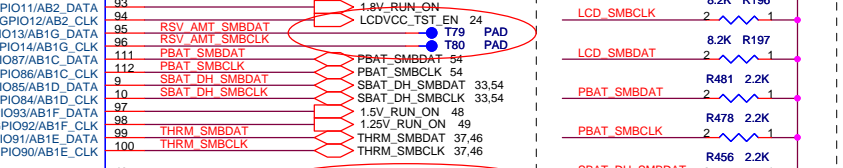
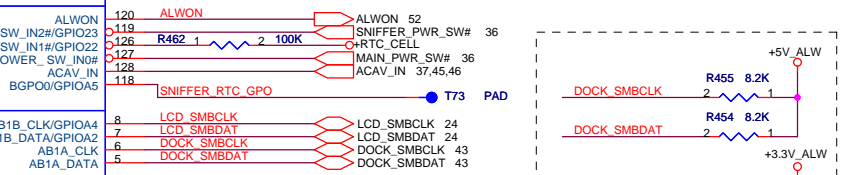
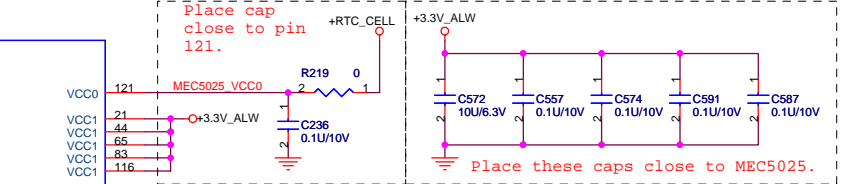
KEYBOARD/MOUSE (26)

PCI POWER/LPC BUS (9)

HOST/8051 SPI (8)

CLOCK (3)

POWER PLANES (9)



QUANTA COMPUTER

Title: Ultra I/O Controller MEC5025

Size	Document Number	Rev
	JM7	1A

Date: Wednesday, June 28, 2006 Sheet 31 of 57

1 = Enabled.
0 = Disabled

Flash Recovery.

Low = Write Protected.

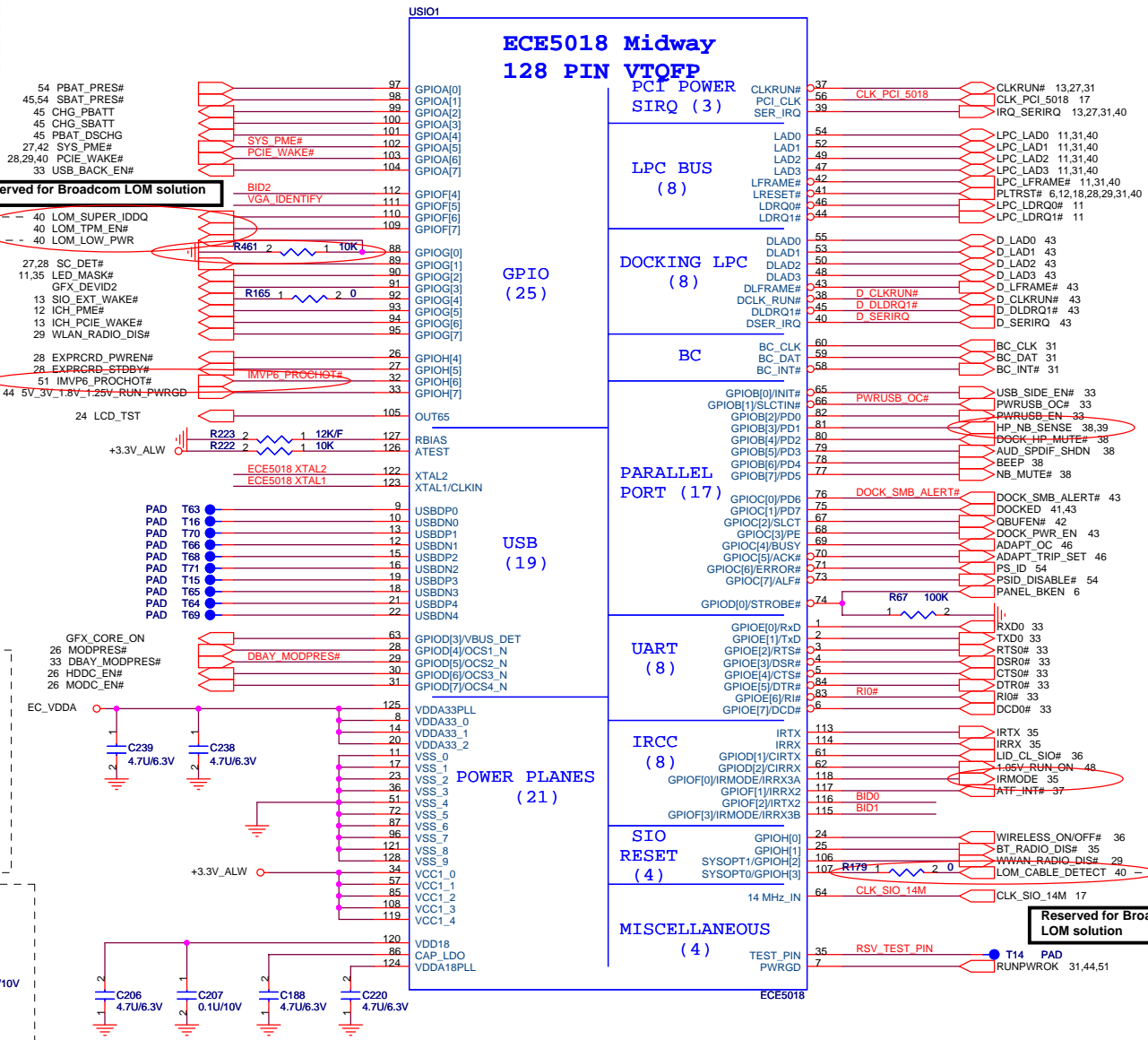
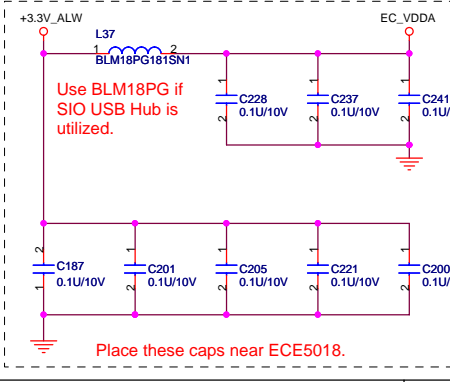
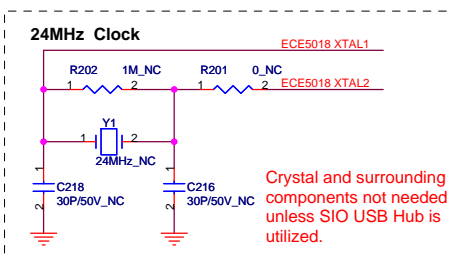
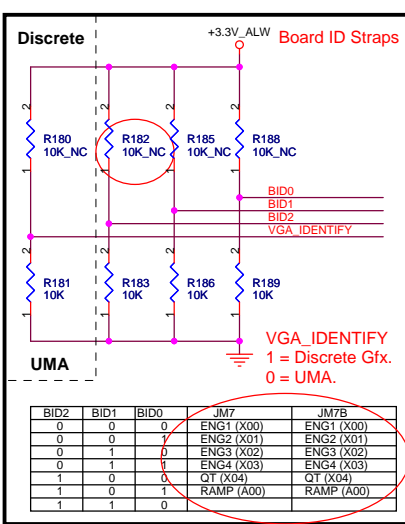
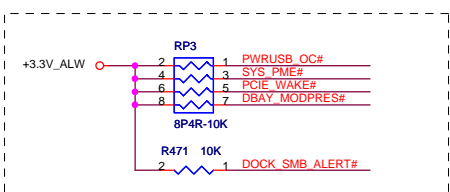
Flash Write Protect bottom 4K of internal bootblock flash.

Populate for flash corruption issue.

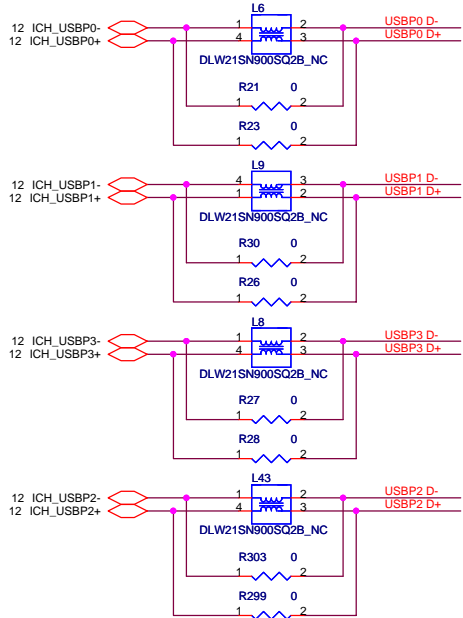
Place cap close to pin 121.

Place these caps close to MEC5025.

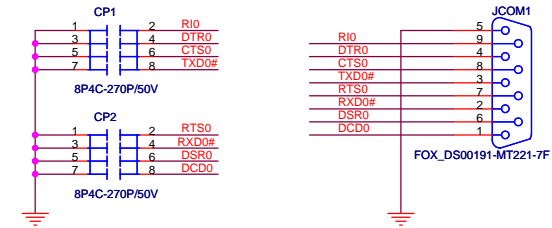
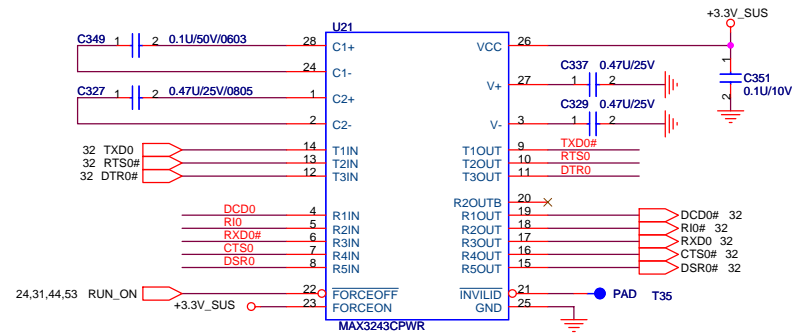
Place close to pin 58.



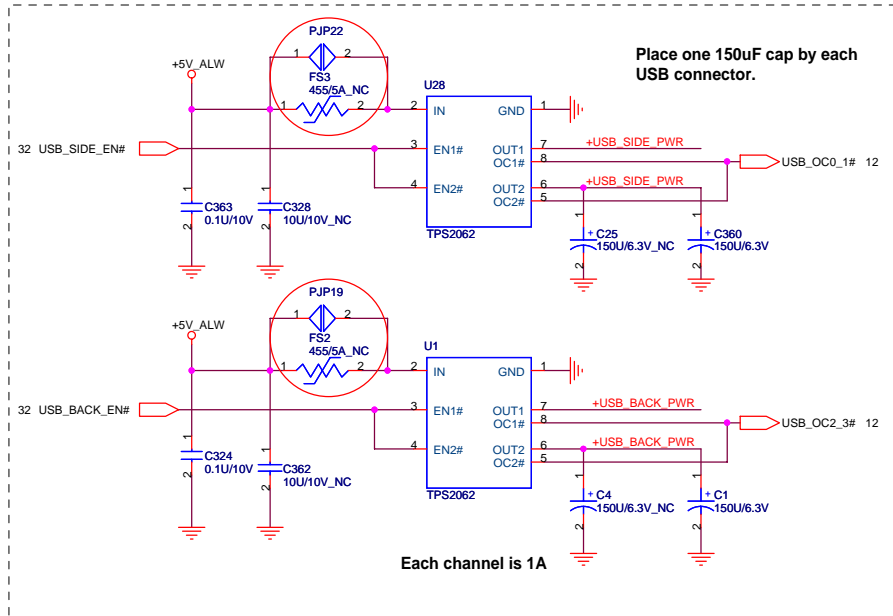
External USB PORT hookup reference. Your design may need more or less external ports and may be mapped differently



Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.

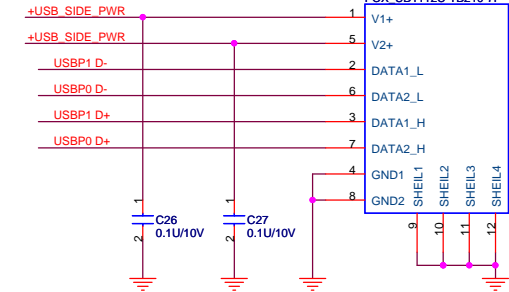


Place these beads close to JCOM1 as soon as possible
If MAX3243 pin 22 tied to RUN_ON, then it can not support Ring Out

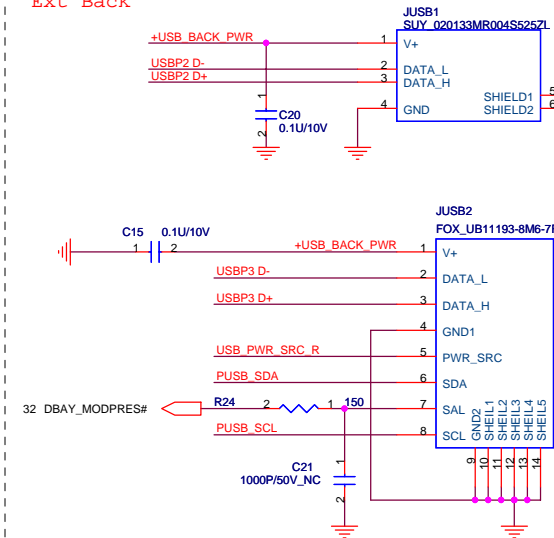


Each channel is 1A

Ext Side



Ext Back



QUANTA COMPUTER

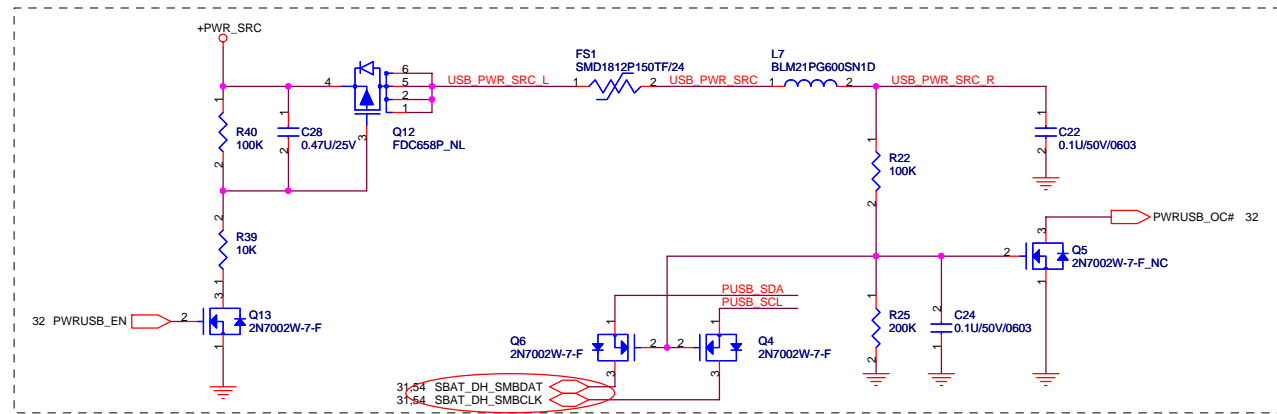
Title: SERIAL PORT & USB

Size: Document Number JM7

Date: Wednesday, June 28, 2006

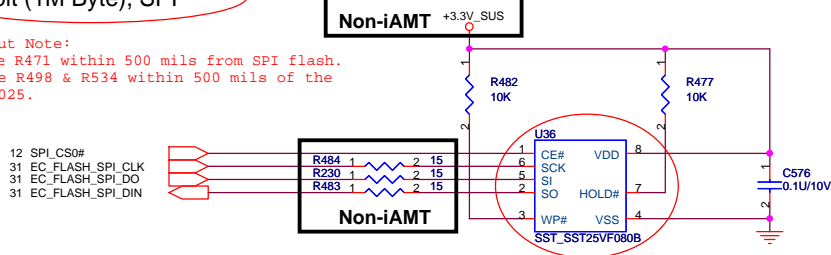
Sheet: 33 of 57

Rev: 1A



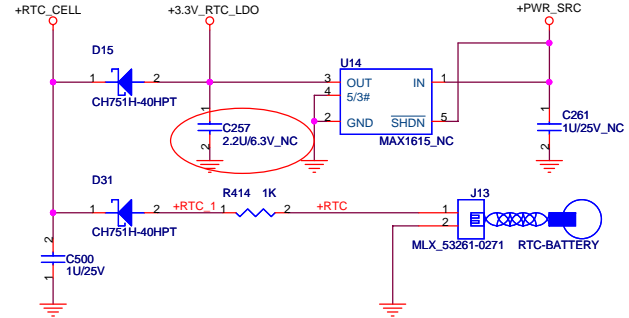
8Mbit (1M Byte), SPI

Layout Note:
Place R471 within 500 mils from SPI flash.
Place R498 & R534 within 500 mils of the MEC5025.

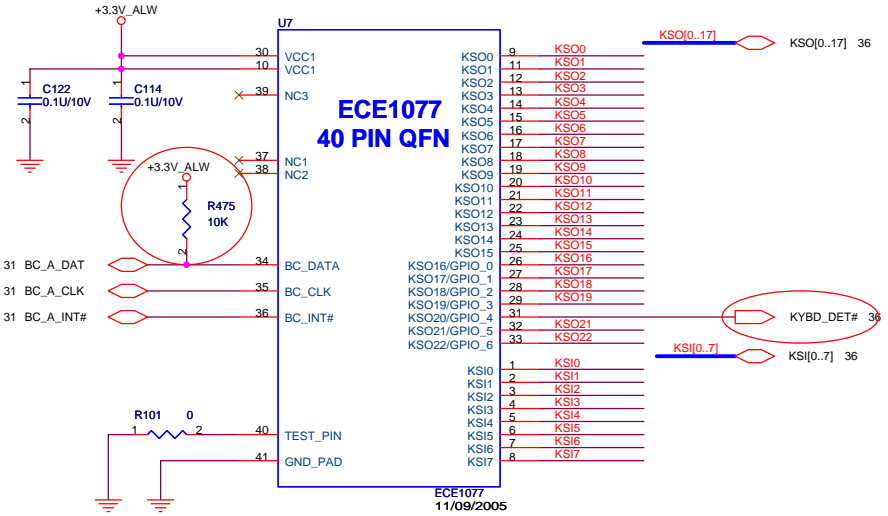


- 12 SPI_CS#
- 31 EC_FLASH_SPI_CLK
- 31 EC_FLASH_SPI_DO
- 31 EC_FLASH_SPI_DIN

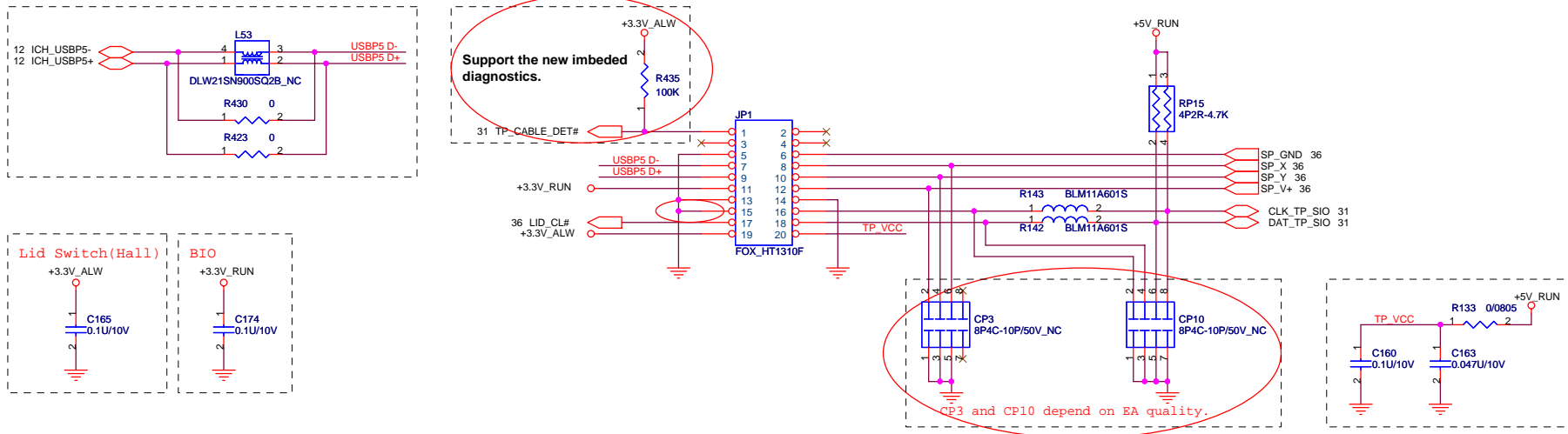
RTC BATTERY



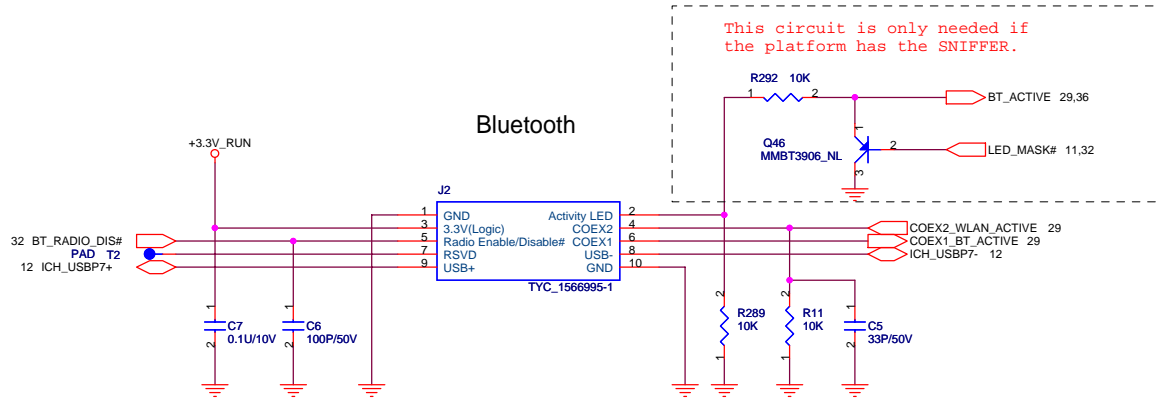
Keyboard Scan Extension



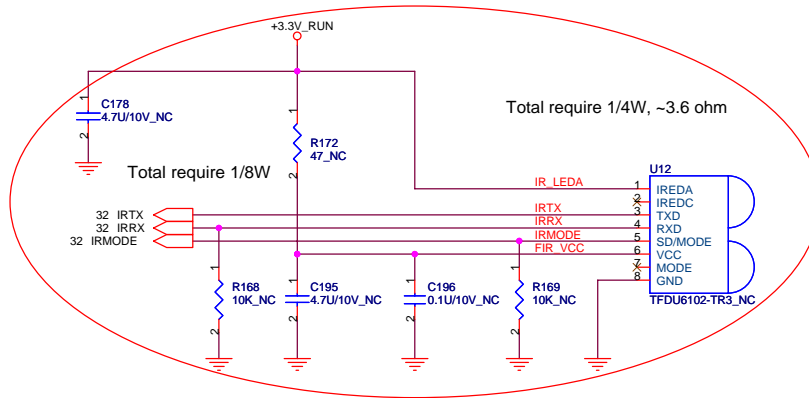
Touch Pad



Bluetooth



FIR



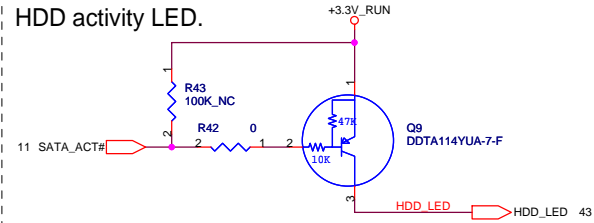
QUANTA COMPUTER

Title: TOUCH PAD, BULE TOOTH & FIR

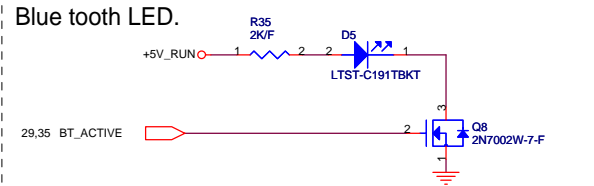
Size: Document Number JM7 Rev 1A

Date: Wednesday, June 28, 2006 Sheet 35 of 57

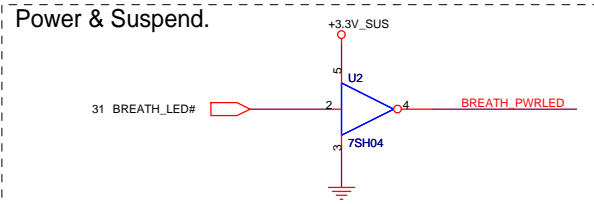
HDD activity LED.



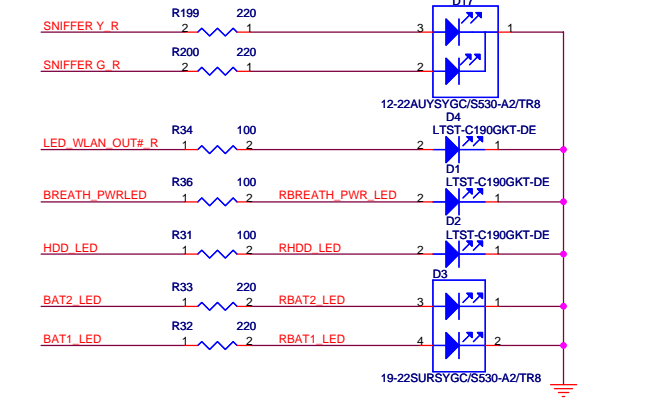
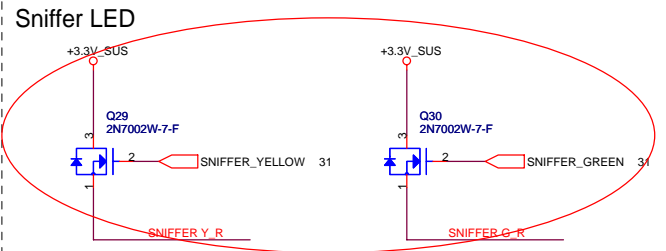
Blue tooth LED.



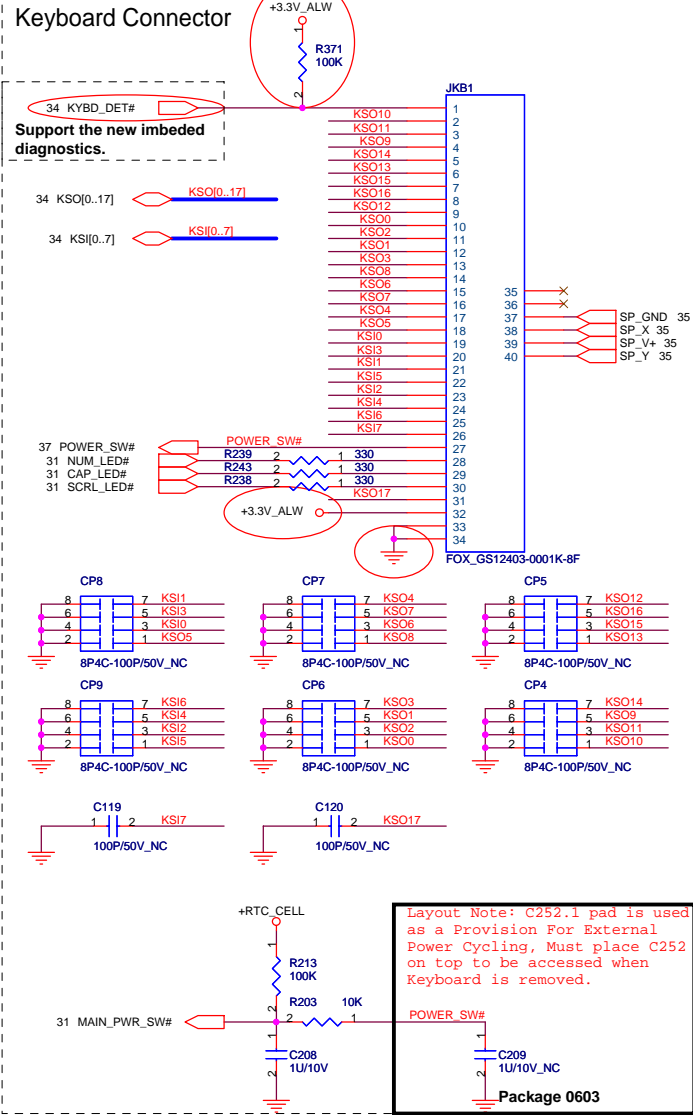
Power & Suspend.



Sniffer LED

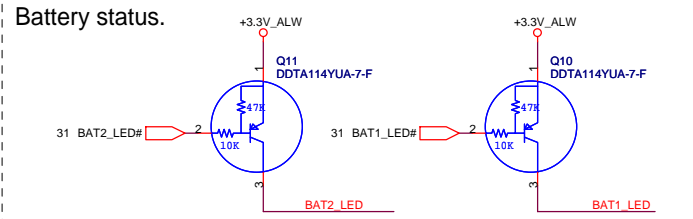


Keyboard Connector

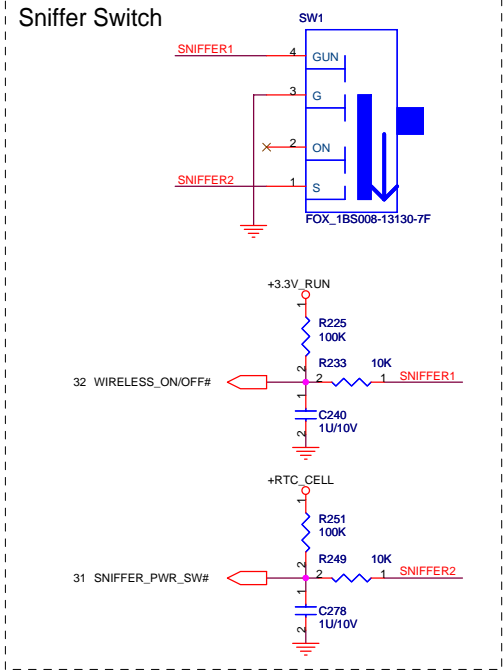


Layout Note: C252.1 pad is used as a Provision For External Power Cycling, Must place C252 on top to be accessed when Keyboard is removed.

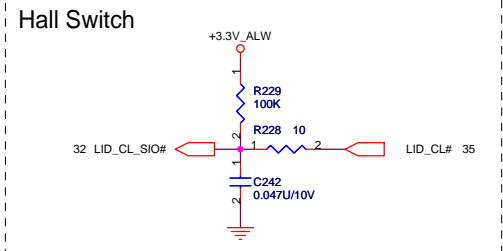
Battery status.



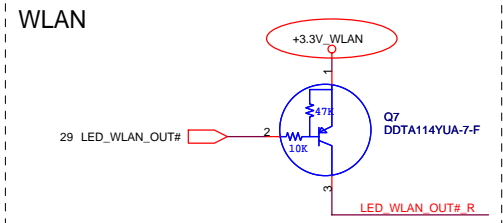
Sniffer Switch

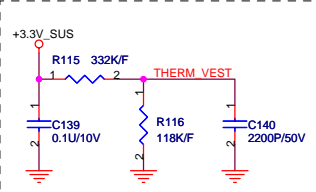
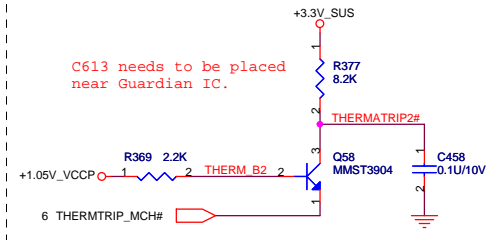
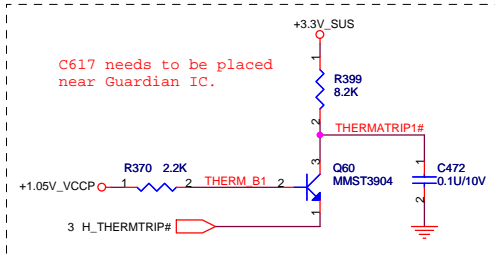
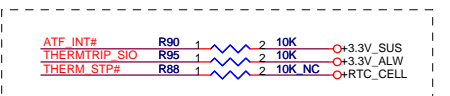
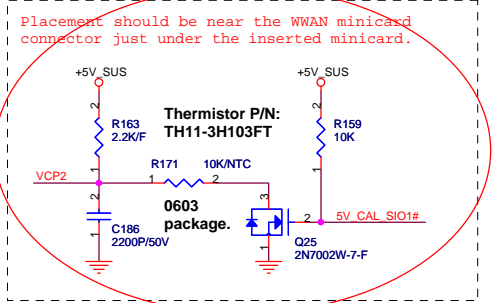
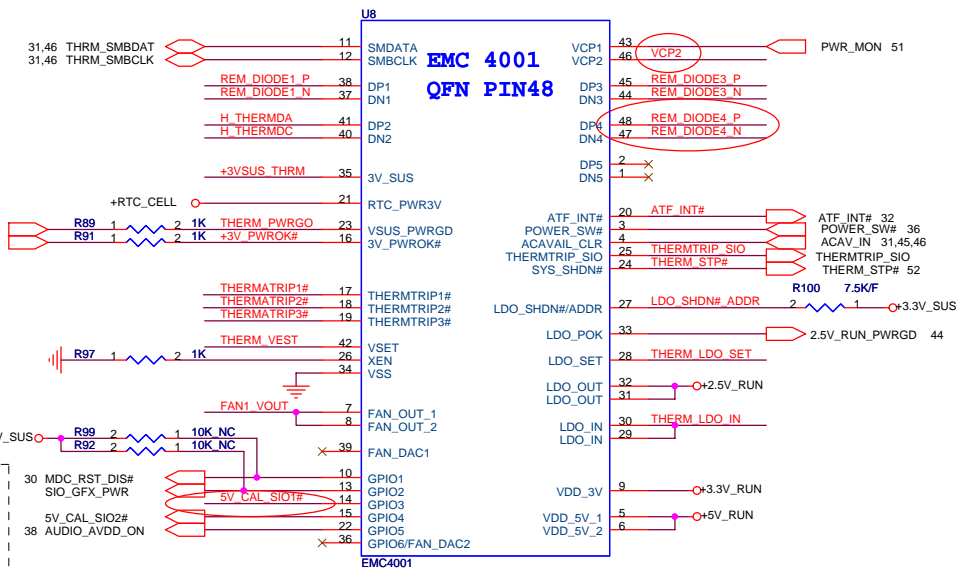
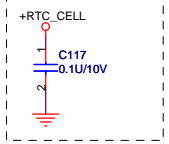
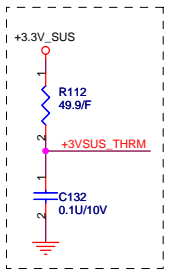
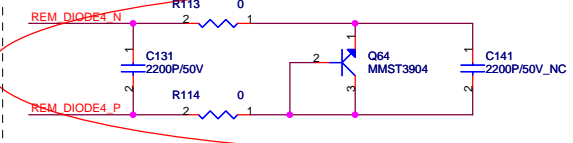
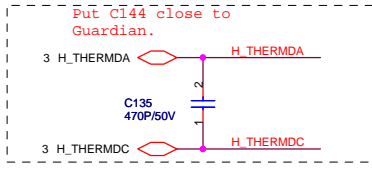
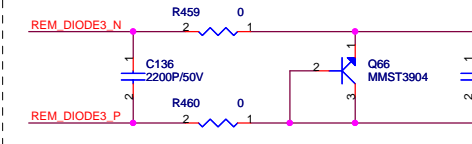
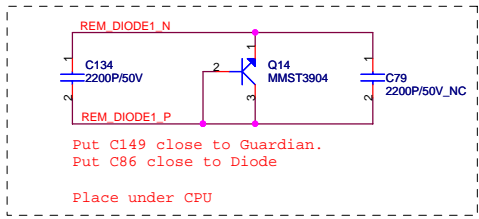
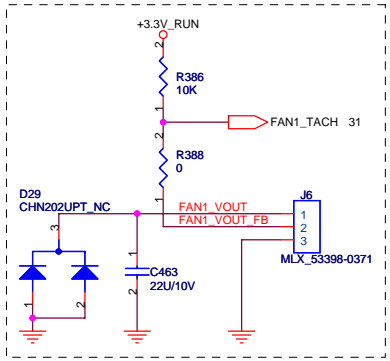


Hall Switch

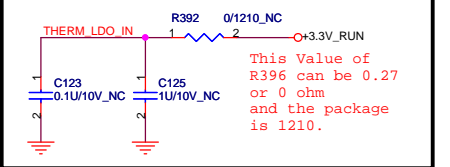
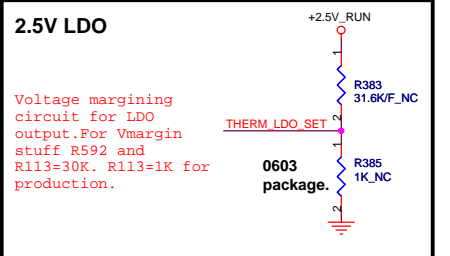
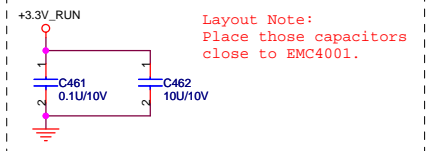


WLAN





Note:
VSET = (Tp-70)/21, where
Tp = 70 to 101 degrees C.
Tp set at 88 degrees C.
Guardian temp tolerance =
+-3 degrees C.



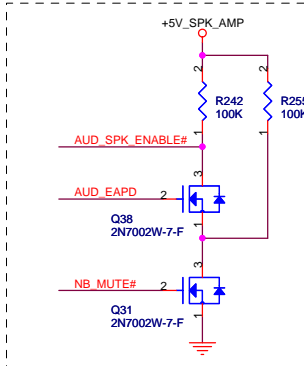
INTERNAL SPEAKER AMP

Package 1206 For THD+N performance and Vista Logo requirements.

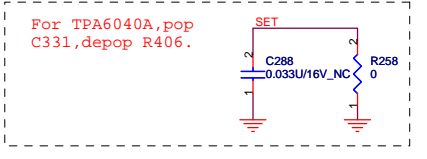
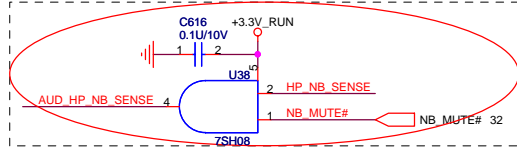
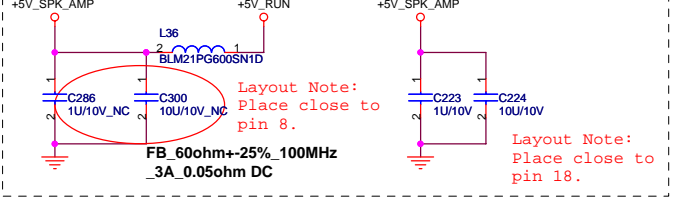
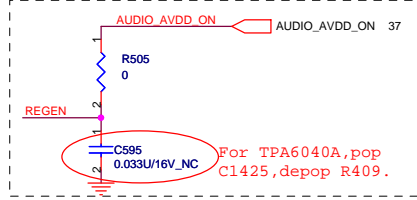
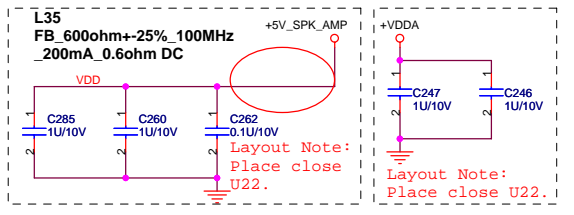
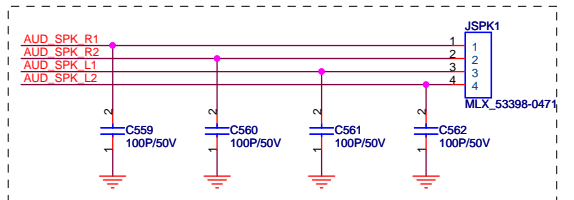
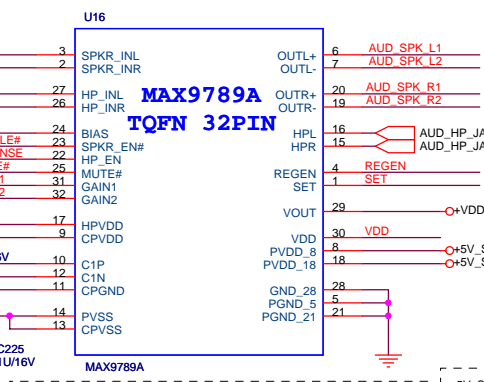
AUD_LINE_OUT_L C301 1 0.033U/200V
 AUD_LINE_OUT_R C259 1 0.033U/200V
 AUD_HP_OUT_L C613 2 1U/100V
 AUD_HP_OUT_R C594 2 1U/100V

For TPA6040A, pop C866, depop R865.

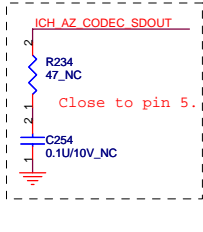
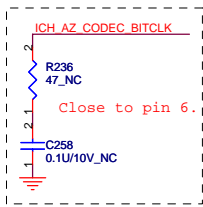
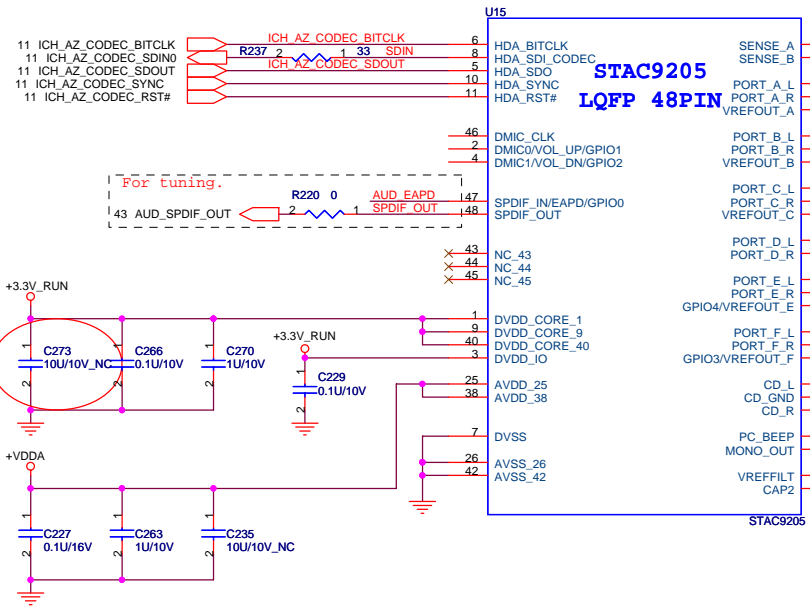
AUDIO_AVDD_ON 1
 AUD AMP MUTE#



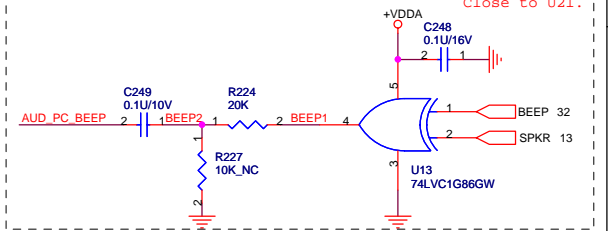
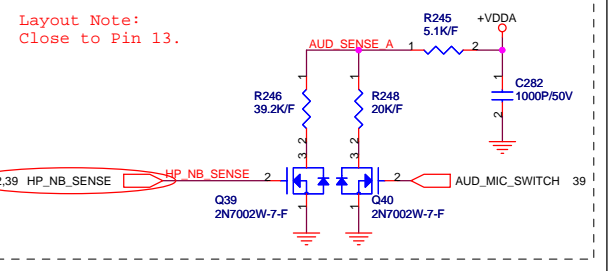
GAIN2	GAIN1	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

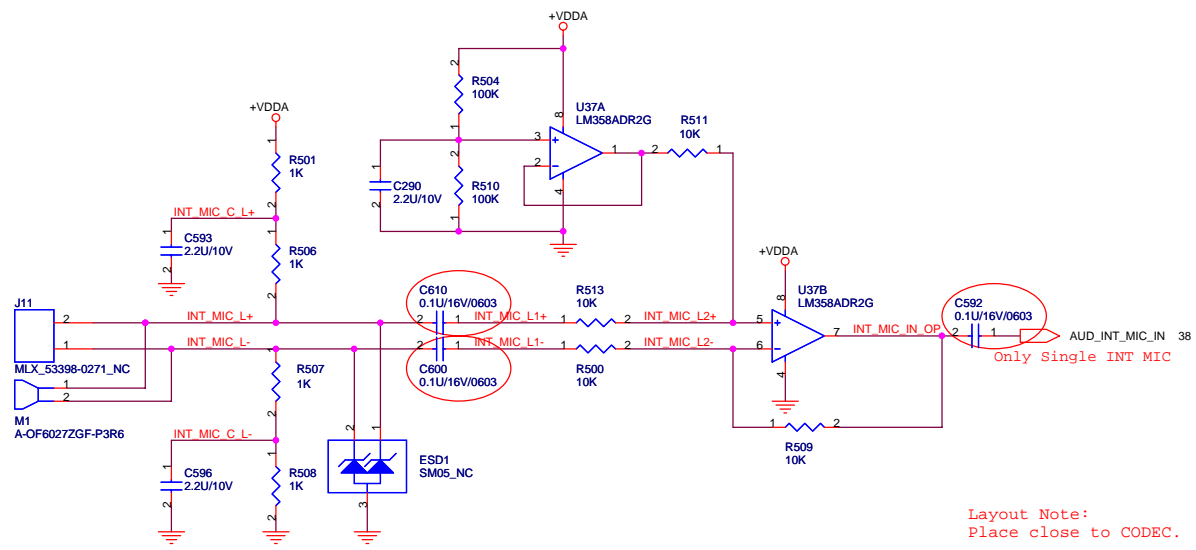
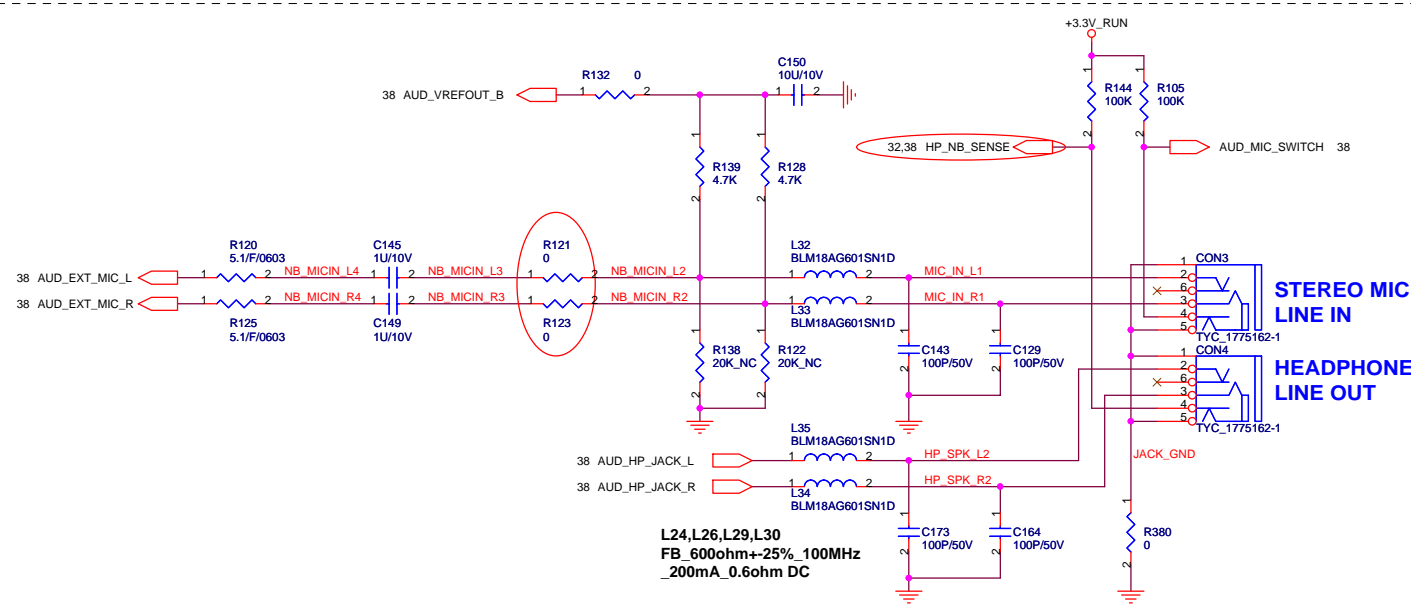


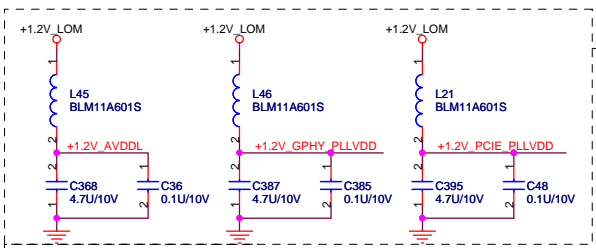
AZALIA (HD) CODEC



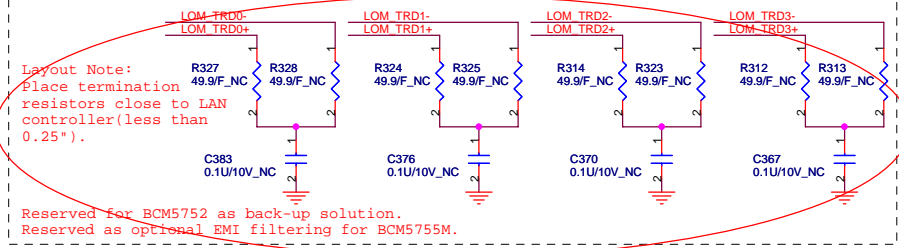
For tuning.
 R220 0 AUD_EAPD SPDIF_OUT





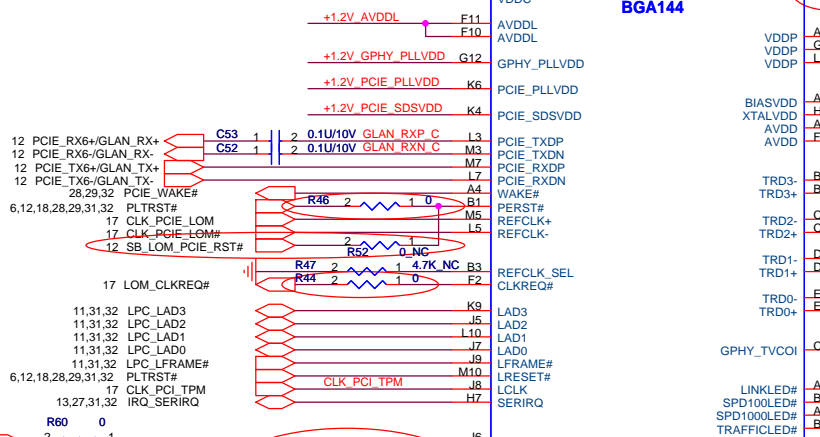
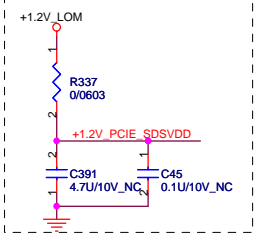


Place filters close to the power pins - 0.1uF should be closest to the power pin. Minimize the loop path from pin to cap to power feed via. The length of the path from the ground side of the cap to the ground via should also be minimized.



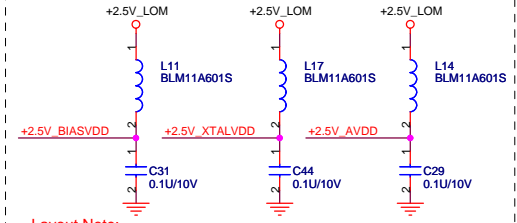
Layout Note:
Place termination resistors close to LAN controller (less than 0.25").

Reserved for BCM5752 as back-up solution.
Reserved as optional EMI filtering for BCM5755M.

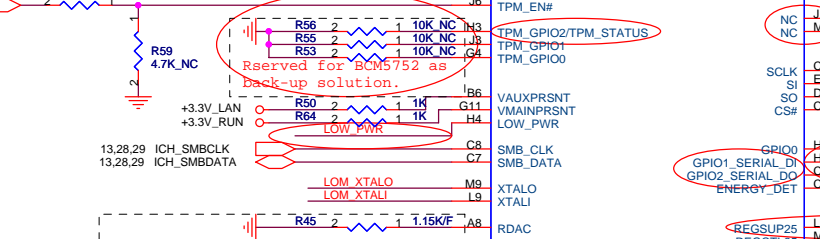
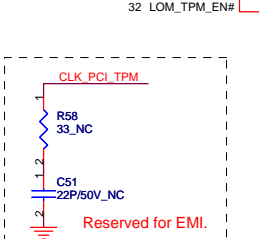


BCM5755M 10mm x 10mm BGA144

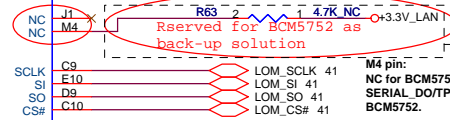
Place R676 as close as possible to the ASIC. Pad is needed to measure 125Mhz clock for debugging.



Layout Note:
Place filters close to the power pins - 0.1uF should be closest to the power pin. Minimize the loop path from pin to cap to power feed via. The length of the path from the ground side of the cap to the ground via should also be minimized.

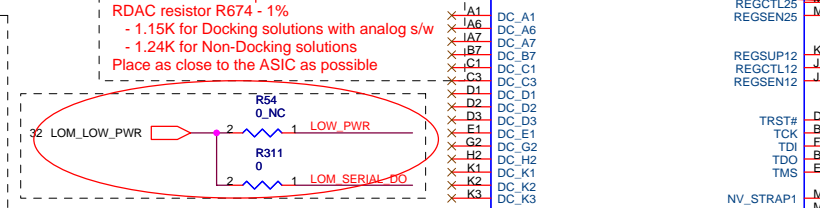
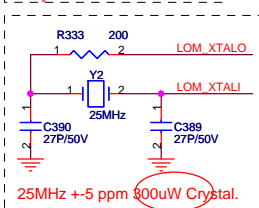


Reserved for BCM5752 as back-up solution.

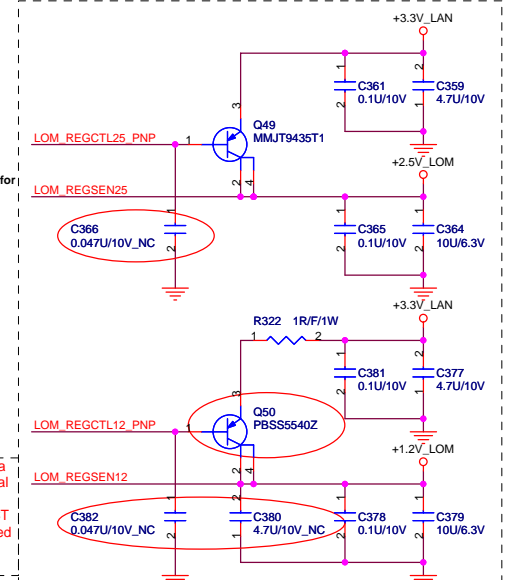
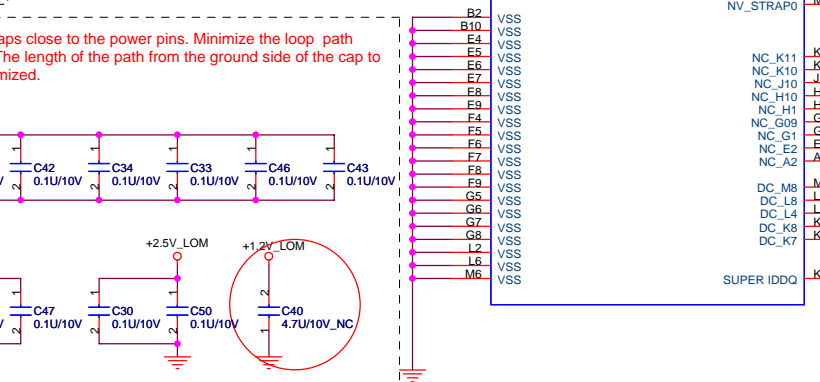
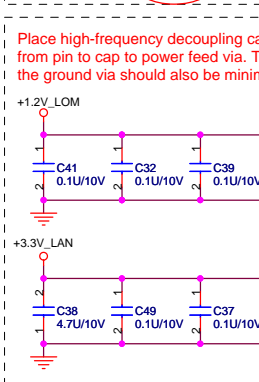


Reserved for BCM5752 as back-up solution.

Reserved for BCM5752 as back-up solution.

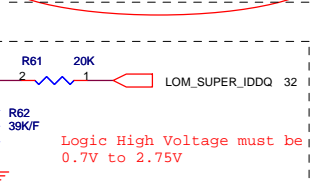


RDAC resistor R674 - 1%
- 1.15K for Docking solutions with analog s/w
- 1.24K for Non-Docking solutions
Place as close to the ASIC as possible



LOM_REGSEN12 and LOM_REGSEN25 should be routed using a trace from the load (PNP) back to the controller. Do not use a direct connection to the power plane. Use 8 mils trace width for these signals.

Reserved for BCM5752 as back-up solution.



Logic High Voltage must be 0.7V to 2.75V

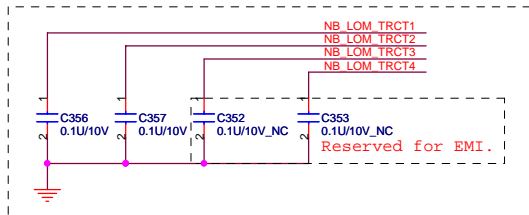
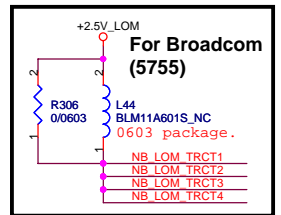
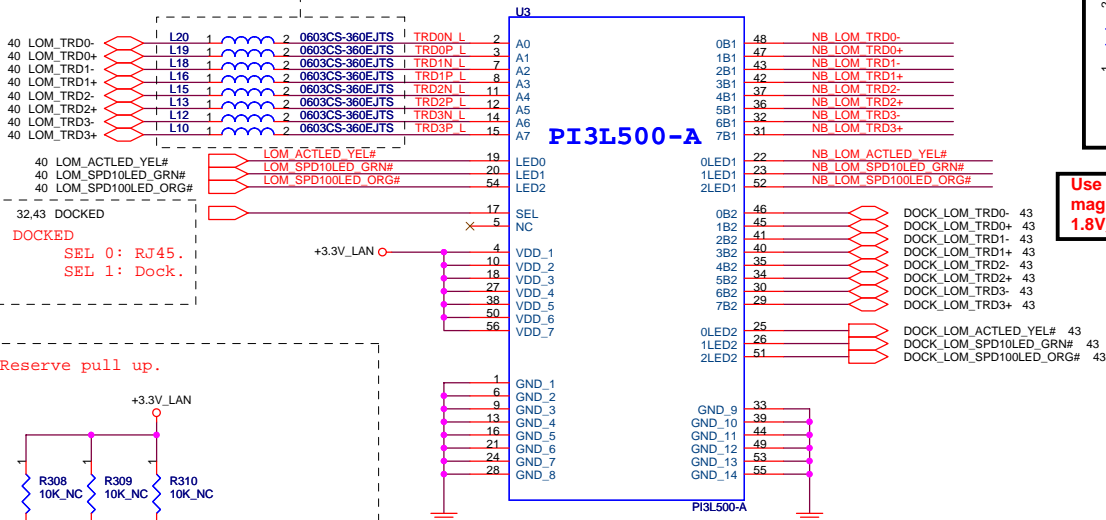
**QUANTA
COMPUTER**

Title: LAN Broadcom 5755

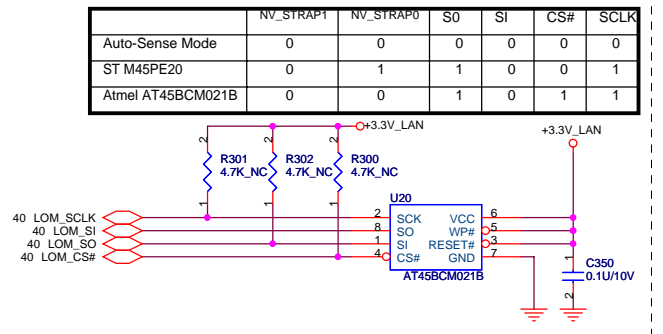
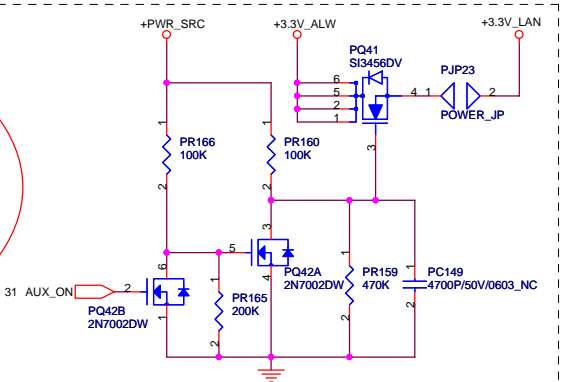
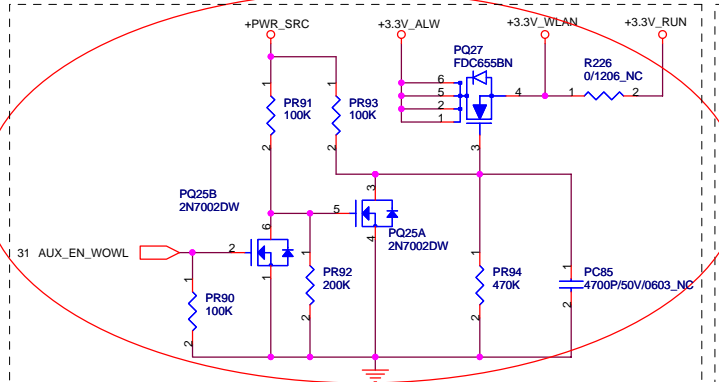
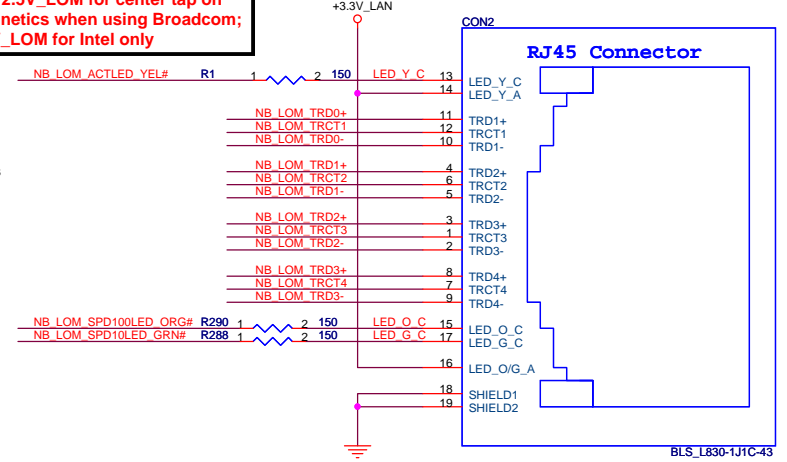
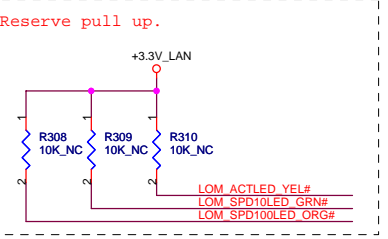
Size: JM7	Document Number	Rev: 1A
Date: Wednesday, June 28, 2006	Sheet: 40	of: 57

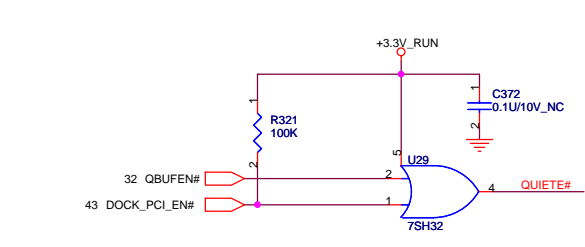
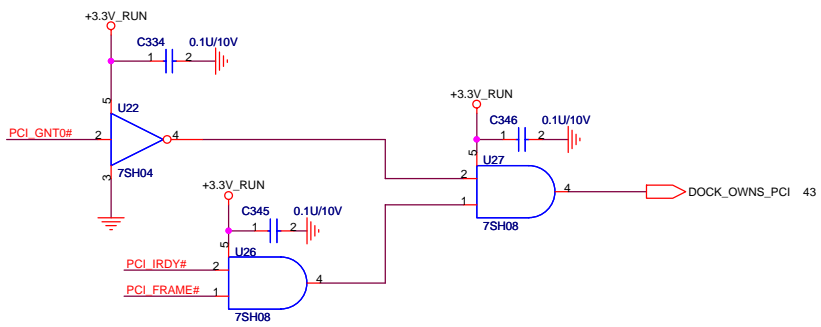
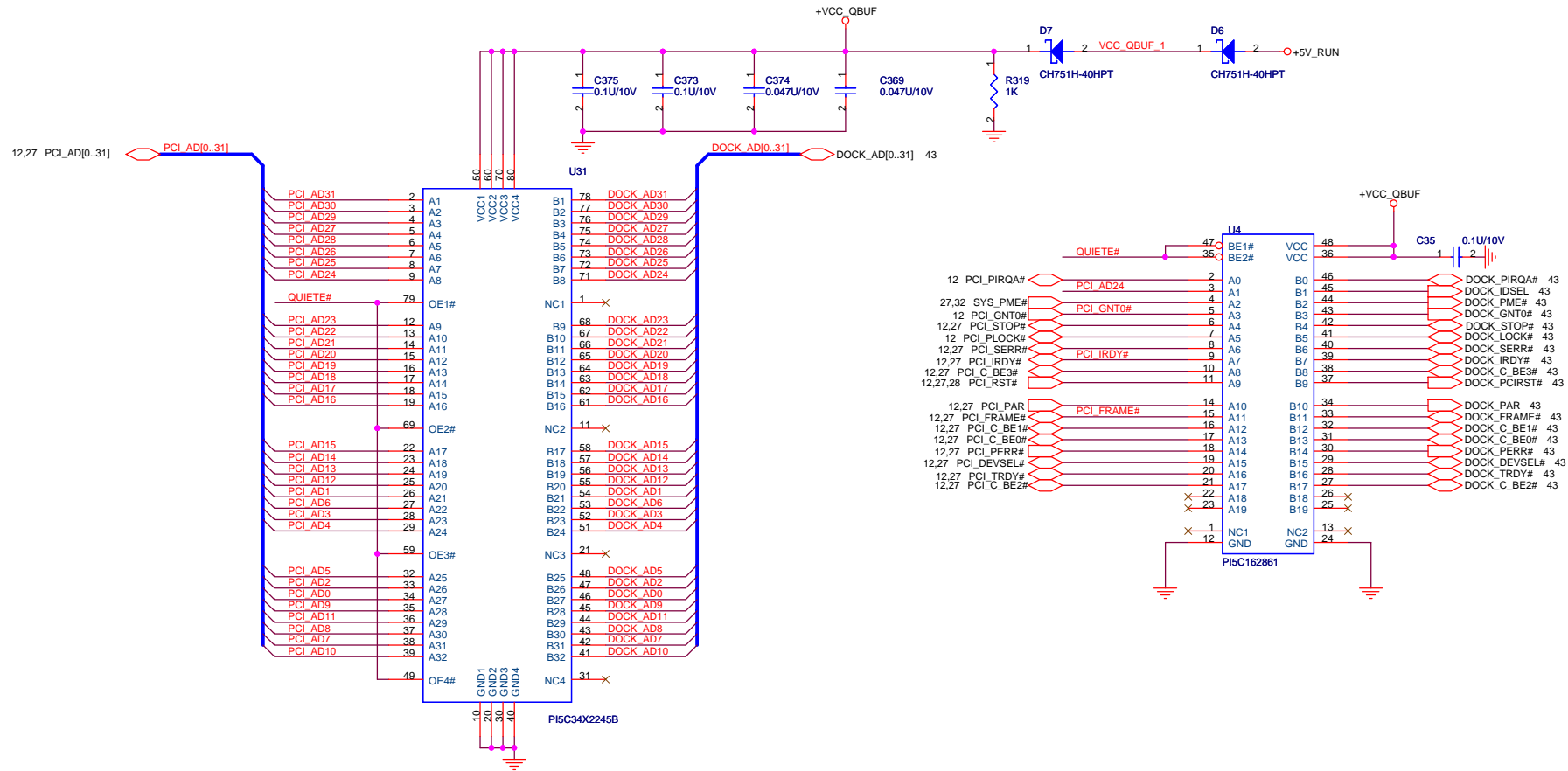
TRANSFORM+RJ45

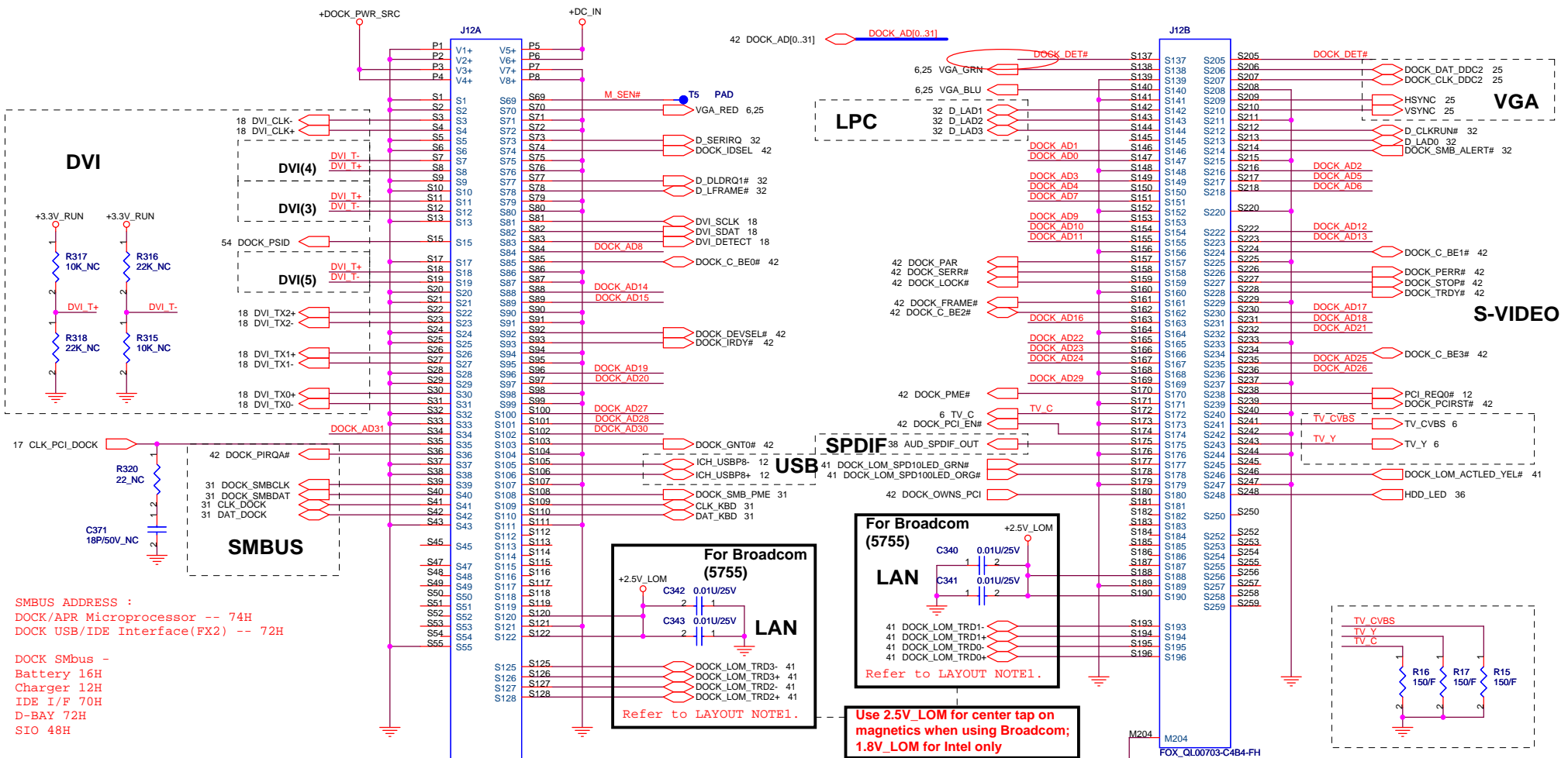
36nH is a suggested value.
Actual value will be system dependent.
Must use 0603 package for lower DC resistance.



Use 2.5V_LOM for center tap on magnetics when using Broadcom; 1.8V_LOM for Intel only

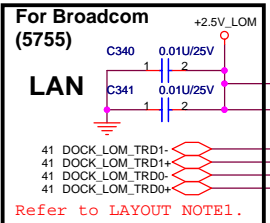
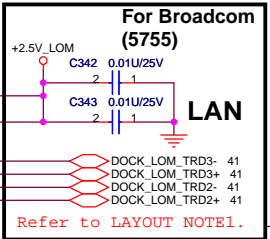






SMBUS ADDRESS :
 DOCK/APR Microprocessor -- 74H
 DOCK USB/IDE Interface(FX2) -- 72H

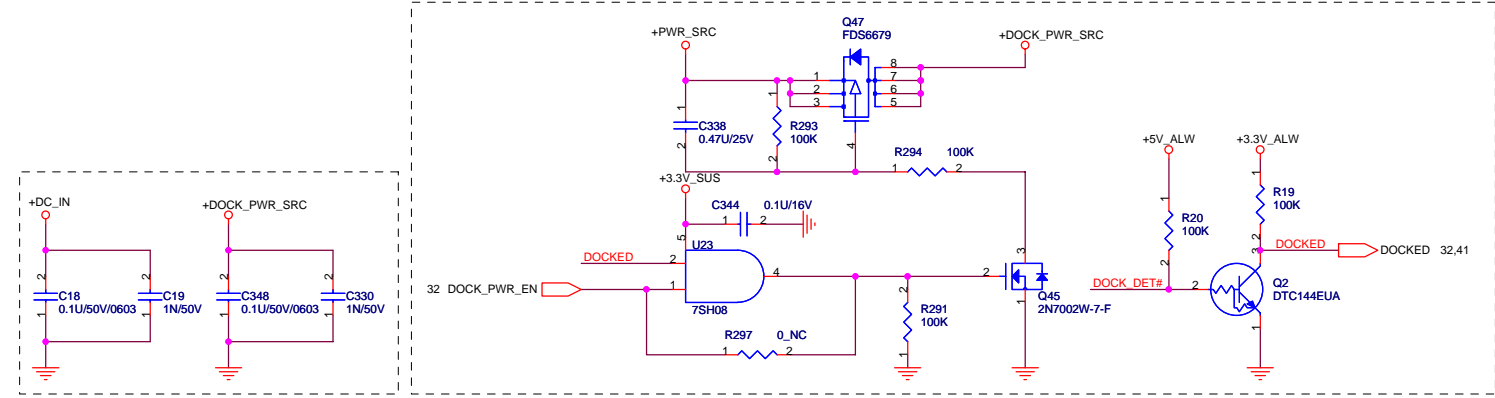
DOCK SMBus -
 Battery 16H
 Charger 12H
 IDE I/F 70H
 D-BAY 72H
 SIO 48H



Use 2.5V_LOM for center tap on magnetics when using Broadcom;
 1.8V_LOM for Intel only

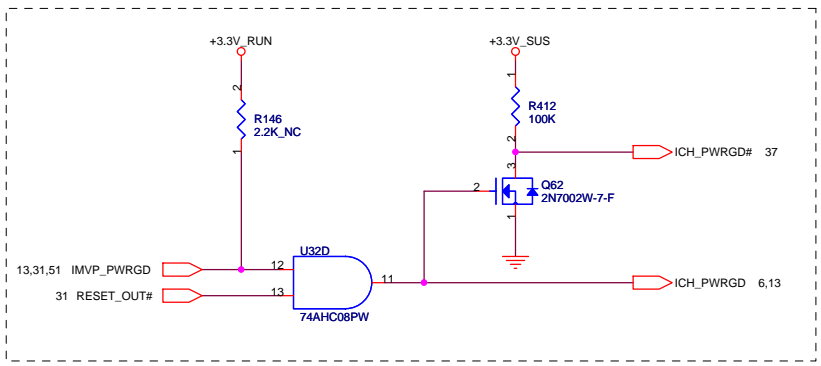
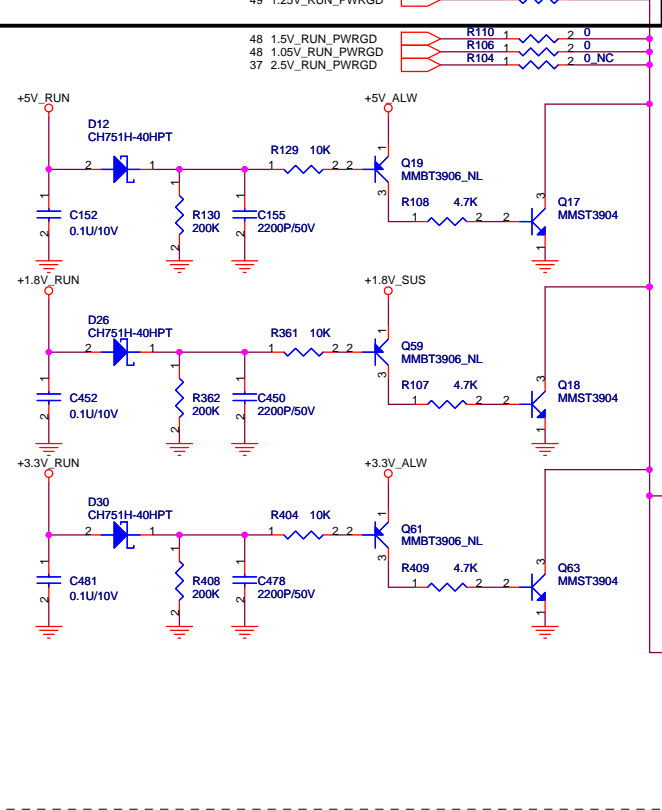
LAYOUT NOTES:
 Follow the Intel Platform Design
 Guideline routing recommendations
 for the following buses: PCI, DVI,
 LPC & USB.

LAYOUT NOTES1:
 Terminators should be as close as
 possible to dock connector pins.
 Keep traces as short as possible.

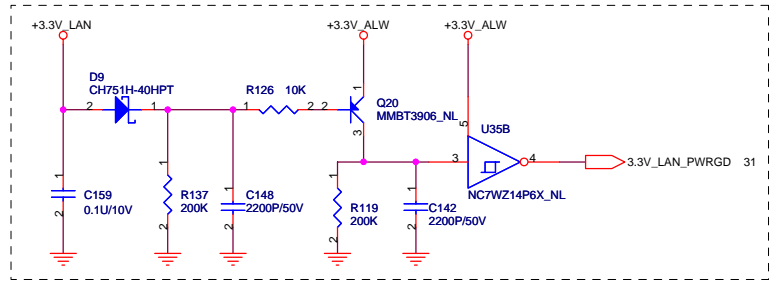
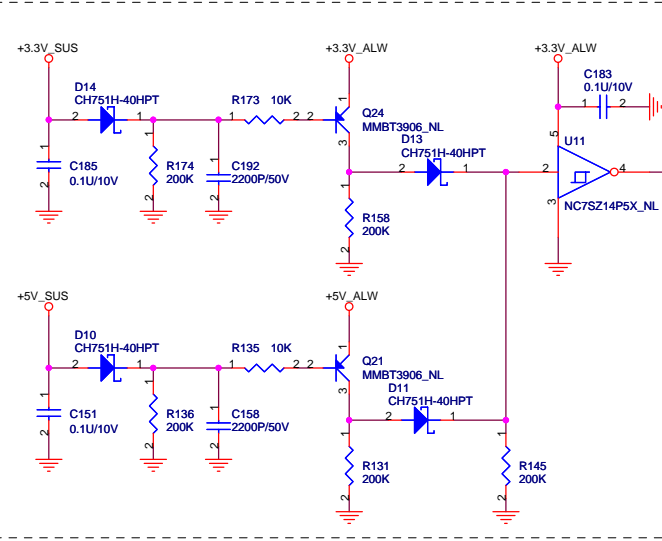
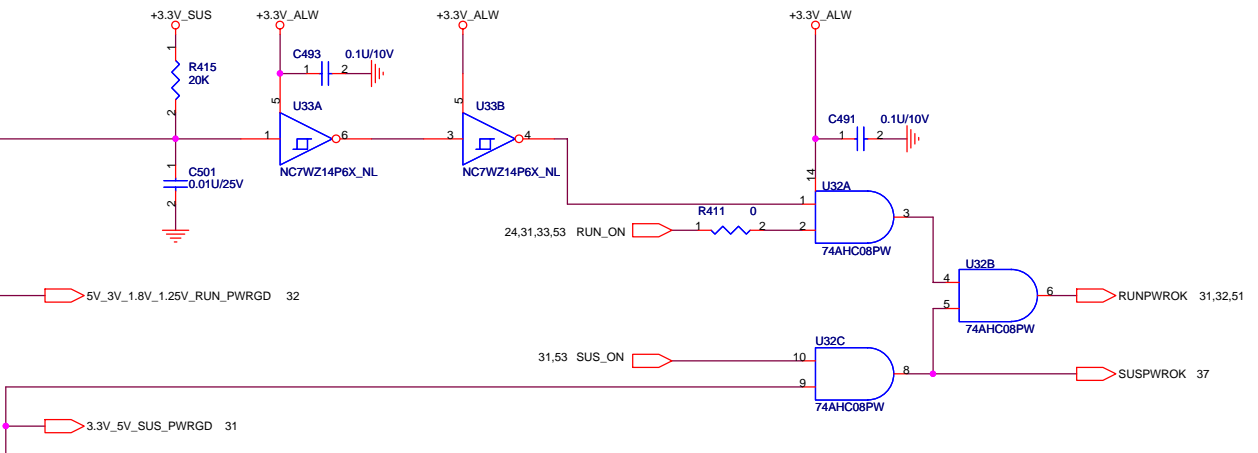


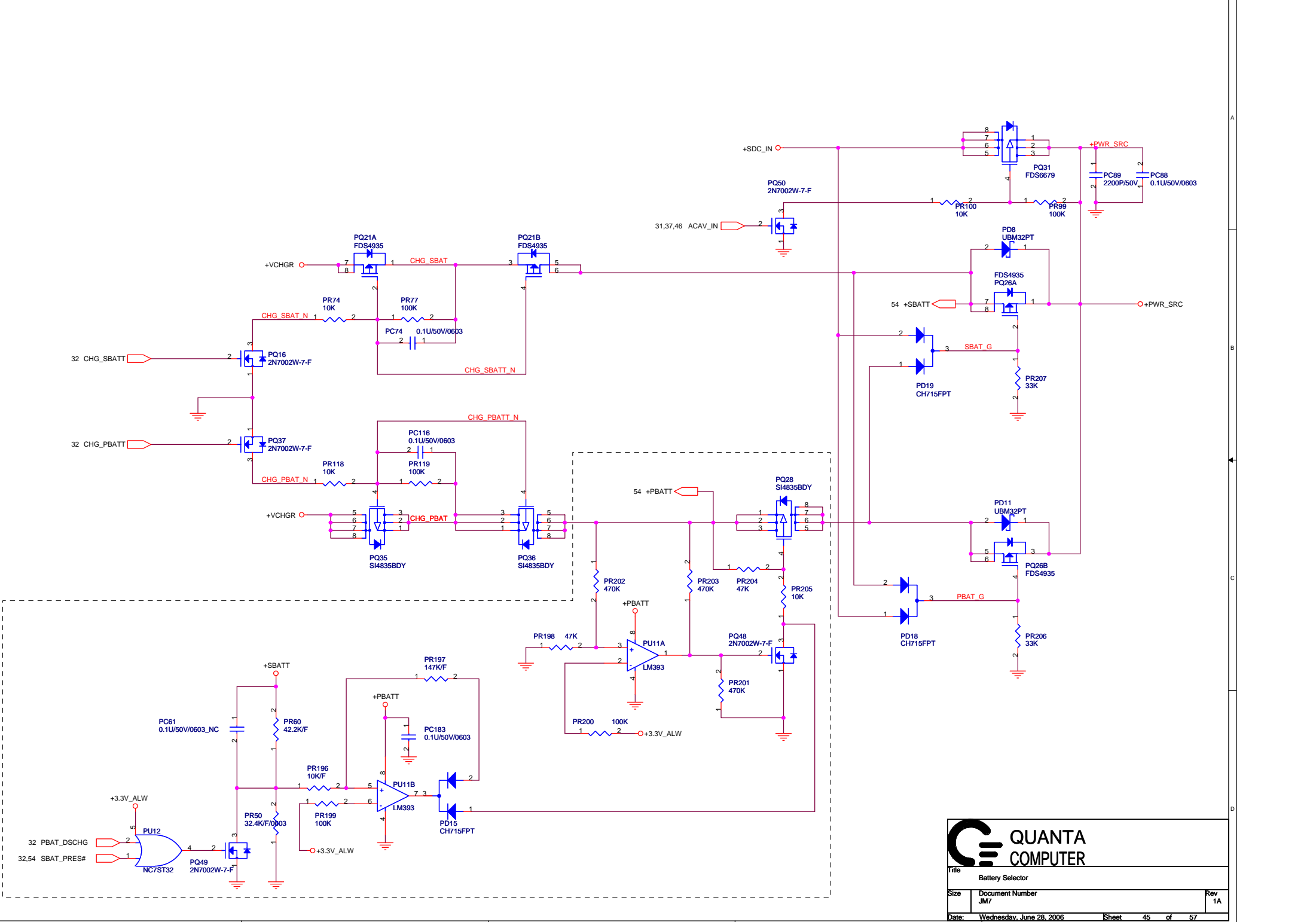
Title Docking Station CONN.		
Size	Document Number JM7	Rev 1A
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Non-iAMT



Keep Away from high speed buses



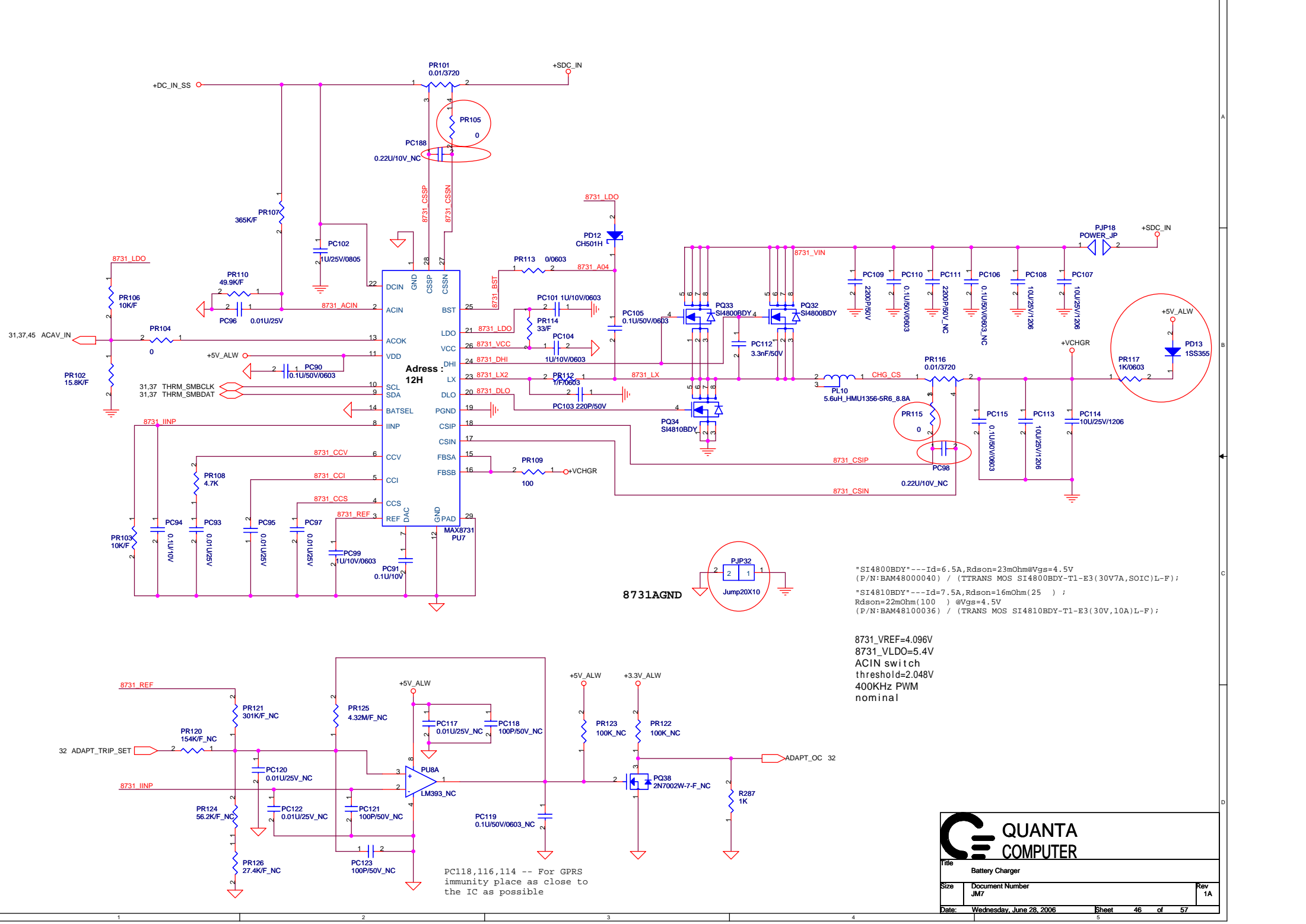


QUANTA COMPUTER

Title: Battery Selector

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Date: Wednesday, June 28, 2006 Sheet 45 of 57



8731AGND


"SI4800BDY"---Id=6.5A,Rdson=23mOhm@Vgs=4.5V
 (P/N:BAM48000040) / (TTRANS MOS SI4800BDY-T1-E3(30V7A,SOIC)L-F) ;
 "SI4810BDY"---Id=7.5A,Rdson=16mOhm(25) ;
 Rdson=22mOhm(100) @Vgs=4.5V
 (P/N:BAM48100036) / (TRANS MOS SI4810BDY-T1-E3(30V,10A)L-F) ;

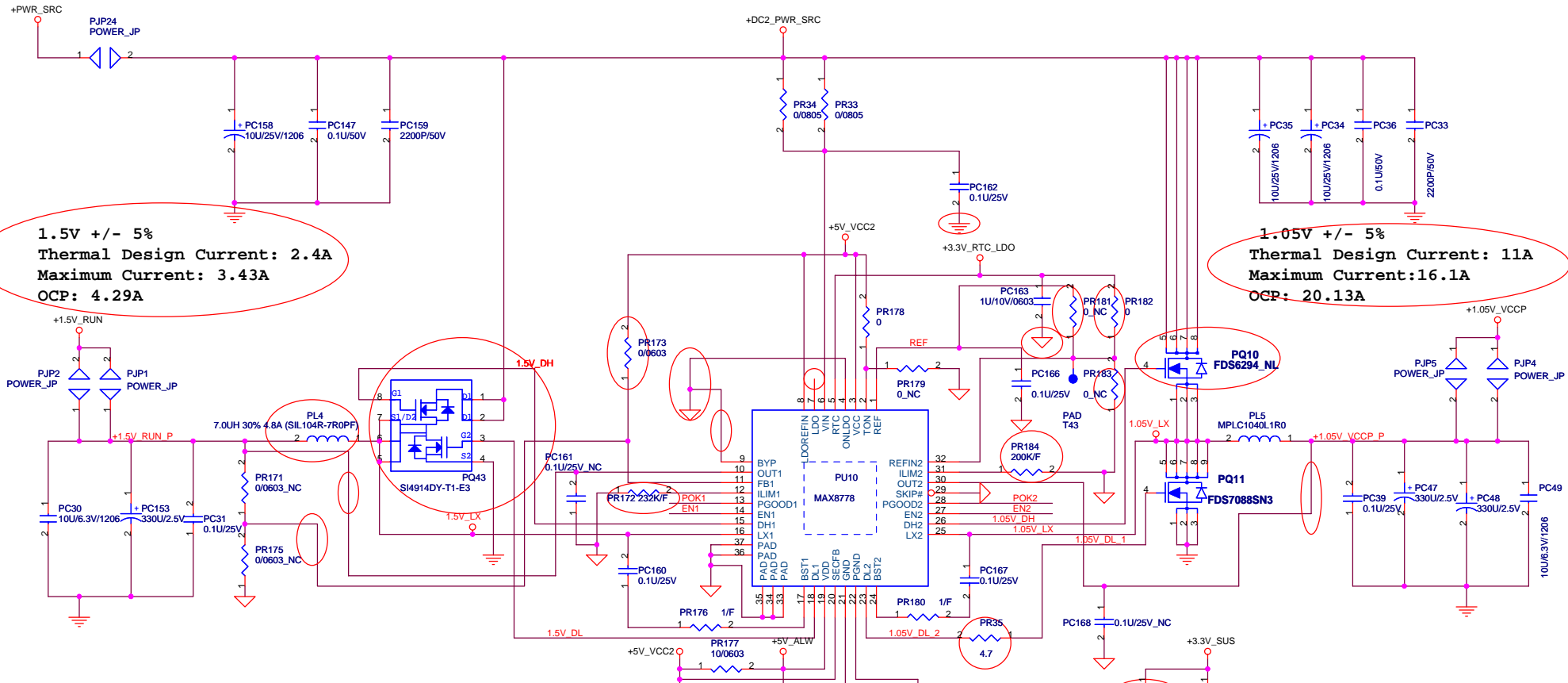
8731_VREF=4.096V
 8731_VLDO=5.4V
 ACIN switch
 threshold=2.048V
 400KHz PWM
 nominal

PC118,116,114 -- For GPRS immunity place as close to the IC as possible

		Title	
		Battery Charger	
Size	Document Number	Rev	
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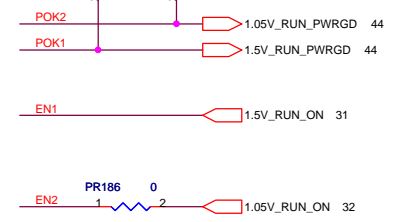
 QUANTA COMPUTER		
Title		
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1.5V +/- 5%
Thermal Design Current: 2.4A
Maximum Current: 3.43A
OCP: 4.29A

1.05V +/- 5%
Thermal Design Current: 11A
Maximum Current: 16.1A
OCP: 20.13A

Layout Notes:
 Place C7 very near U1-pin19 and PU1-pin20.
 Place C8 very near U1-pin3.
 Place R19 very near U1-pin21.
 Minimize loop including Q4, L2, C11, C12 and R19.
 Minimize loop including Q2, L3, C17, C18, C19 and R19.
 Route GNDA_DC2 using at least 25 mil trace width.
 Minimize GNDA_DC2 trace length.
 Place C15 near U1-pin7.
 Place C20 near U1-pin5.
 Place R7 near U1-pin11.
 Place R12 near U1-pin31.
 Place R3, C10 near U1-pins 24 and 25.
 Place R2, C9 near U1-pins 16 and 17.
 Route +1.05V_BOOT, +1.05V_BOOST, +1.5V_BOOT, +1.5V_BOOST using 25mil trace width and minimize lengths.
 Connect large copper fill areas to PQ1, PQ2, PQ3 and Q4 signals for thermal improvement.
 Minimize length of +1.5V_RUN_PL and +1.05V_VCCP_PL.
 Place C1, C2, C3, C22 very near Q3-pins 5, 6, 7, 8.
 Place C4, C5, C6, C23 very near Q1-pins 5, 6, 7, 8.
 Route +DC2_PWR_SRC using 50 mil trace width and minimize length.
 Route OUT1 and OUT2 away from inductor and switch-node.
 Sense Vout directly at output bulk cap.

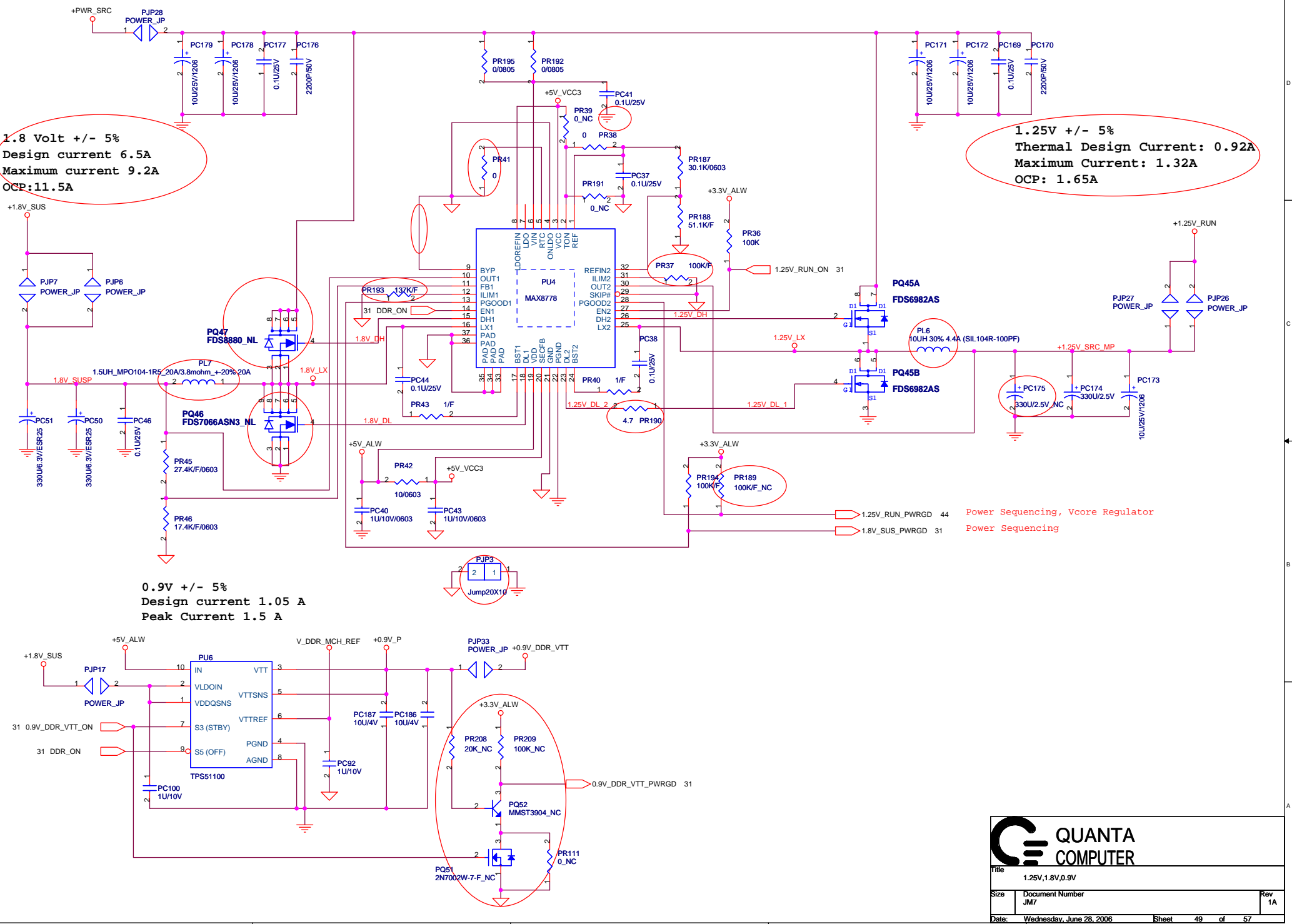


Title		1.5V,1.05V
Size	Document Number	Rev
	JM7	1A
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1.8 Volt +/- 5%
 Design current 6.5A
 Maximum current 9.2A
 OCP: 11.5A

1.25V +/- 5%
 Thermal Design Current: 0.92A
 Maximum Current: 1.32A
 OCP: 1.65A

0.9V +/- 5%
 Design current 1.05 A
 Peak Current 1.5 A




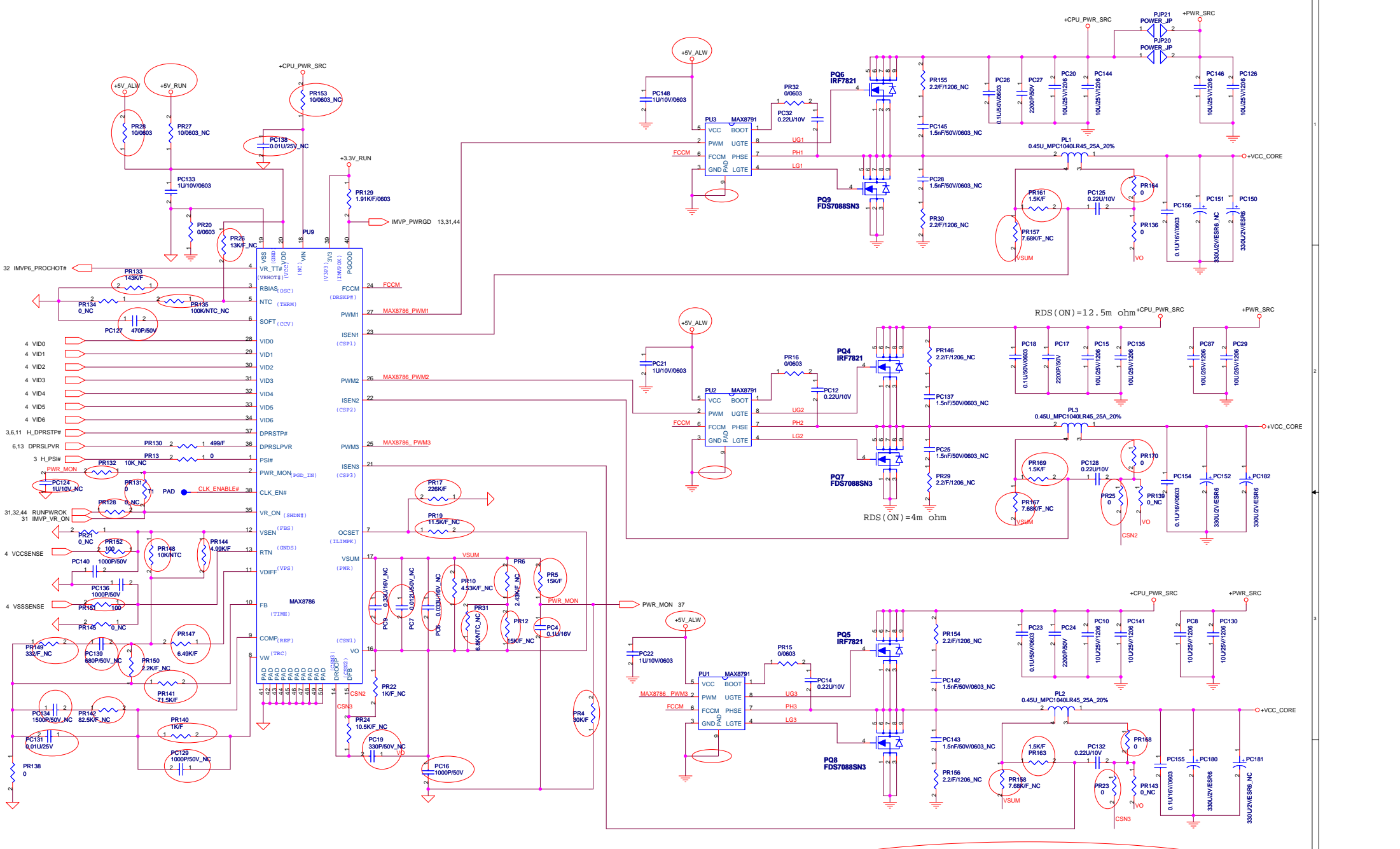
Power Sequencing, Voore Regulator
 Power Sequencing



Title		1.25V, 1.8V, 0.9V
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If use ISL6260C:PR34 and PR38 are 0 ohm , PR37 and PR41 no stuff.
 If use MAX8786:PR34,PR38,PR326 and PR327 no stuff , PR37 and PR41 are 0 ohm.

PHASE 3 populate

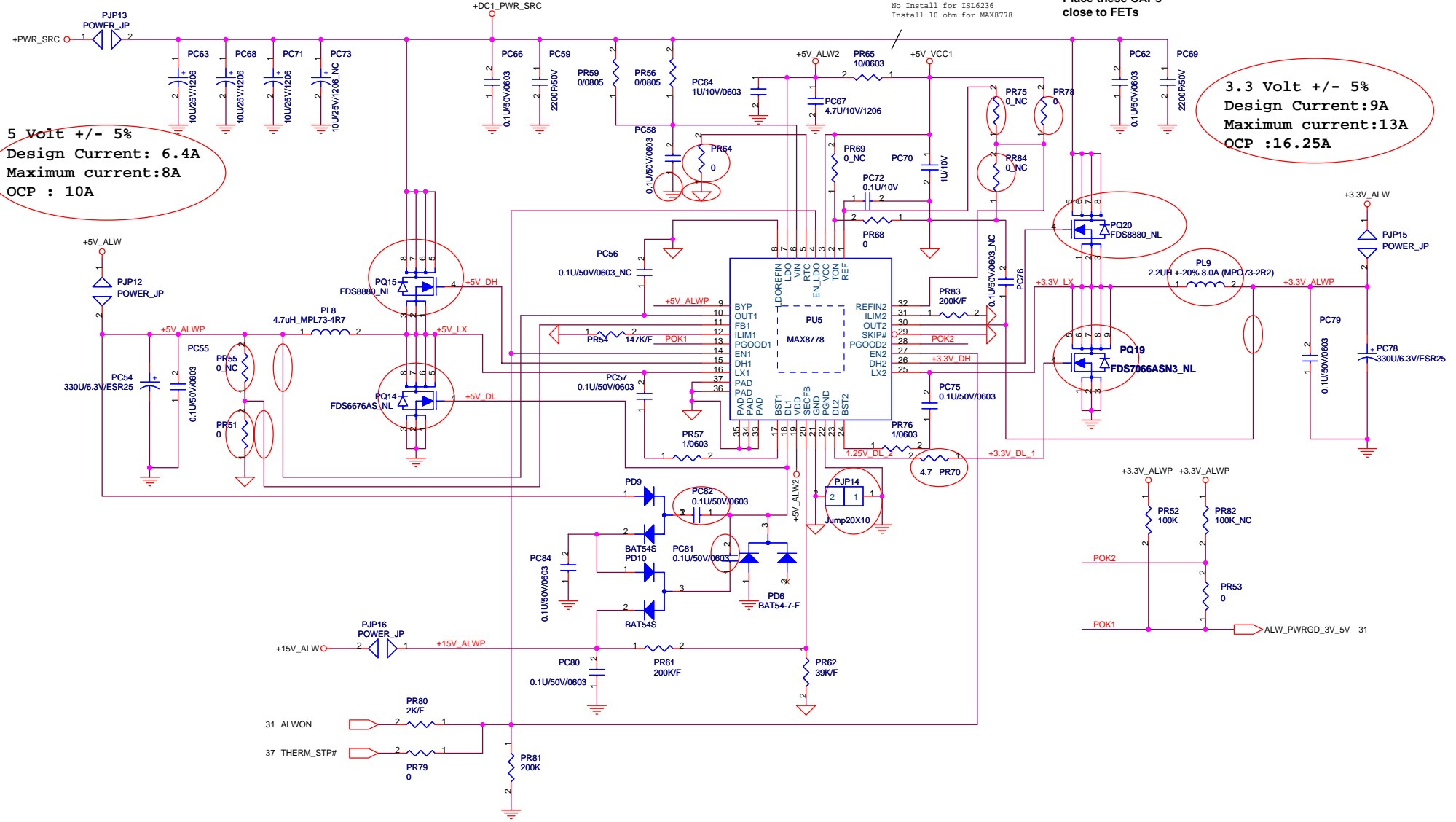


DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+15V_ALW

Place these CAPS close to FETs

No Install for ISL6236
Install 10 ohm for MAX8778

Place these CAPS close to FETs



5 Volt +/- 5%
Design Current: 6.4A
Maximum current: 8A
OCP : 10A

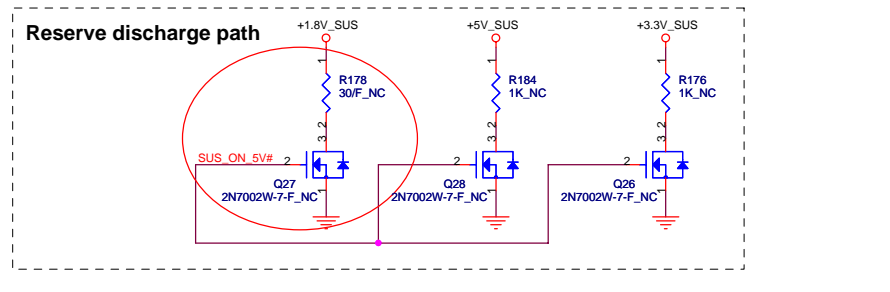
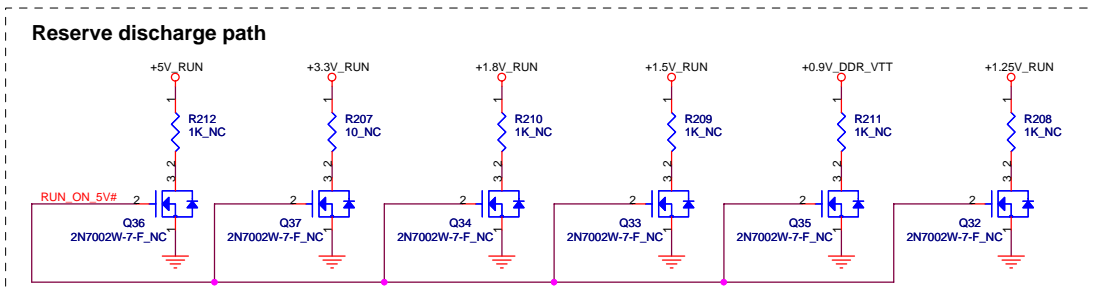
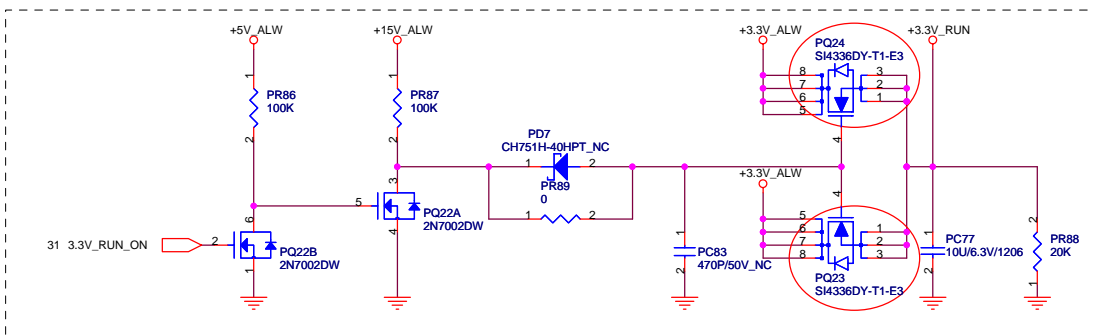
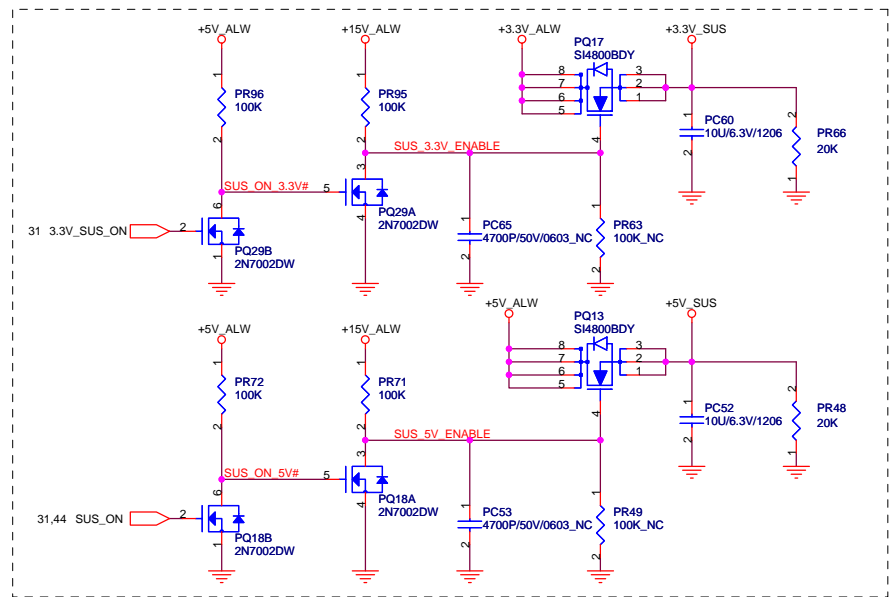
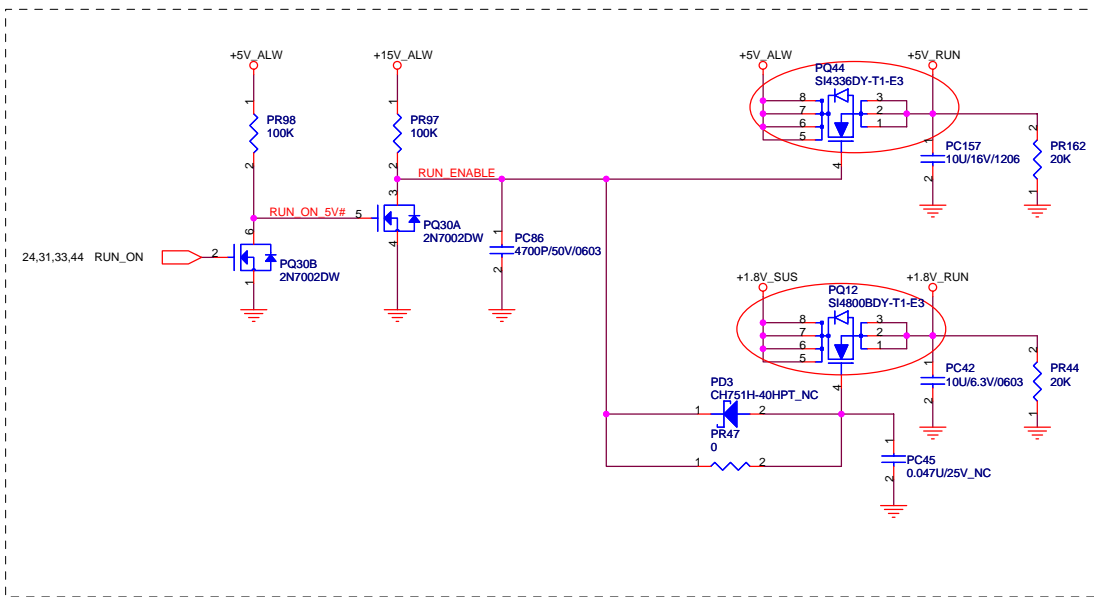
3.3 Volt +/- 5%
Design Current: 9A
Maximum current: 13A
OCP : 16.25A

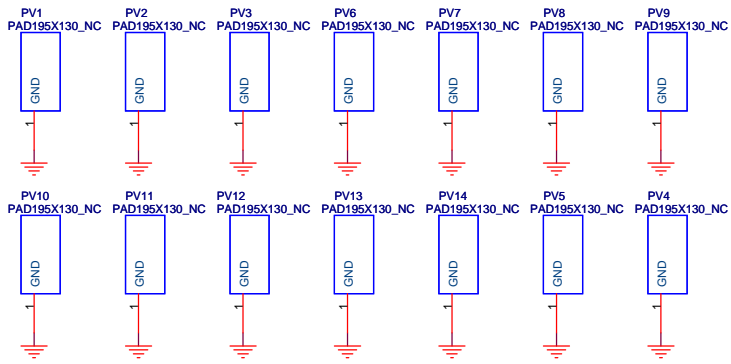
QUANTA COMPUTER

Title: 3VALW.5V.3V, Power On

Size: Document Number JM7 Rev 1A

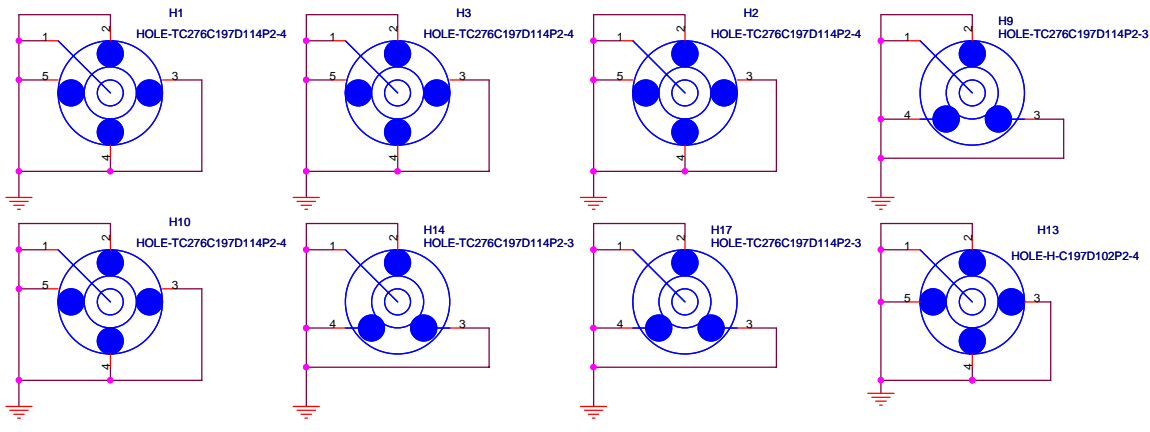
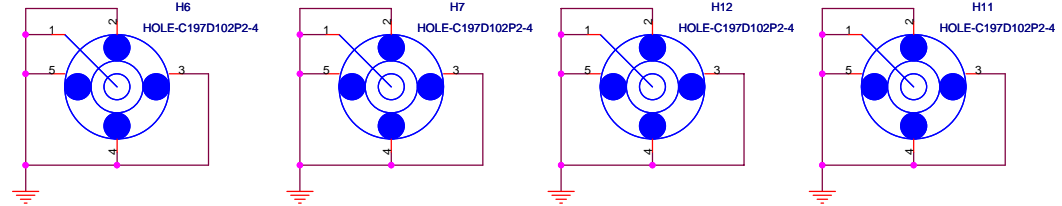
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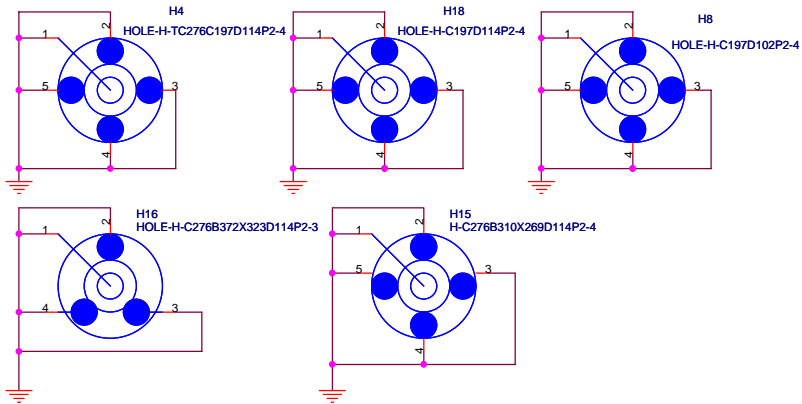



Reserved for EMI.

CPU



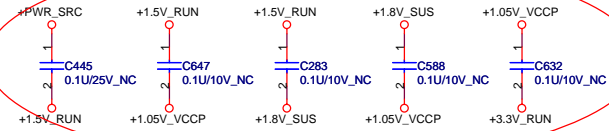
HDD



 QUANTA COMPUTER		
Title SCREW PAD		
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Reserved for EMI.

Stitching caps



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SATA (HDD&CD_ROM)

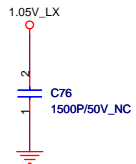
Page 27
PCCARD /CONN

Page 31
SIO(MEC5025)

Page 38
Azelia CODEC

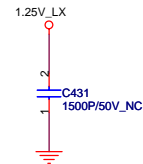
Page 40
LAN(BCM5755M)

Page 48
1.5VRUN,1.05V(VTT)

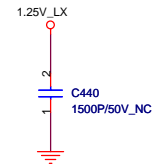


Place C860,C216,C1426 close to PQ33.
Place C862,C222,C1427 close to PQ73.

Page 49
1.25V,1.8V,0.9V



Place C867,C254,C1428 close to PQ91.
Place C863,C253,C1429 close to PQ92.



Page 51
CPU_MAX8786(3phase)

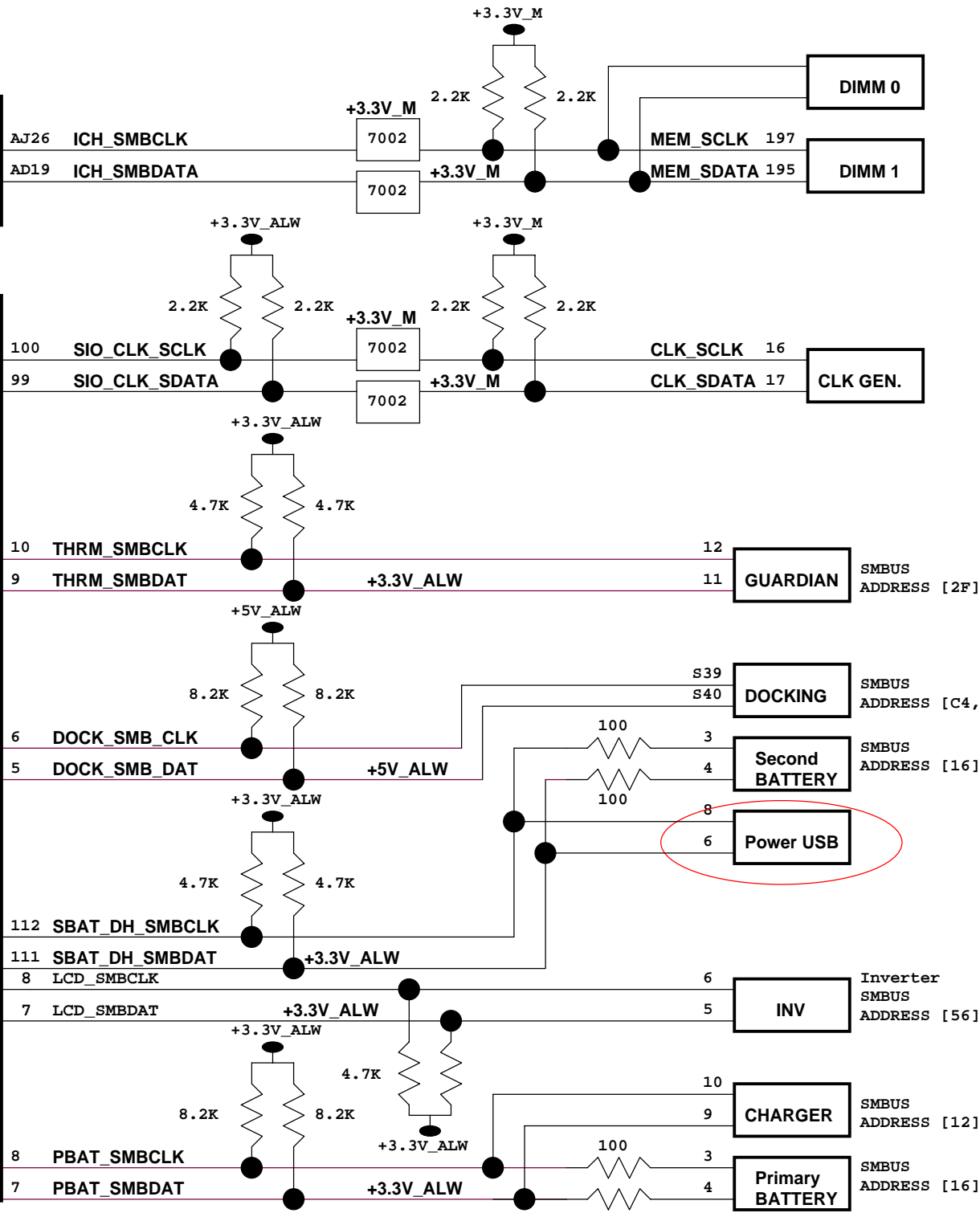
Page 52
D/D Power



Title EMI CAP		
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ICH8-M

SIO MEC5025



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