

# COMPAL CONFIDENTIAL

MODEL NAME : **IBQ00**

PCB NO : **LA-3301P (DA80000771L)**

BOM P/N : **45144631L01**

## M08 (UMA) Briscoe uFCPGA Mobile Merom Intel Crestline + ICH8M

2007-03-07

REV : 1.0 (A00)

**DAZ P/N: DAZZGX0010L**

MB PCB	
Part Number	Description
DA80000771L	PCB ZGX LA-3301P REV1 M/B UMA

PCB1	
IBQ00	LS-3301P REV1
IC08	LED/B
LS-3301P REV1 LED/B	

PCB1	
IBQ00	LS-3302P REV1
IC08	LS-3302P I/O Board

**BOM NO. 45144631L01**

**PCB P/N: DA80000771L**

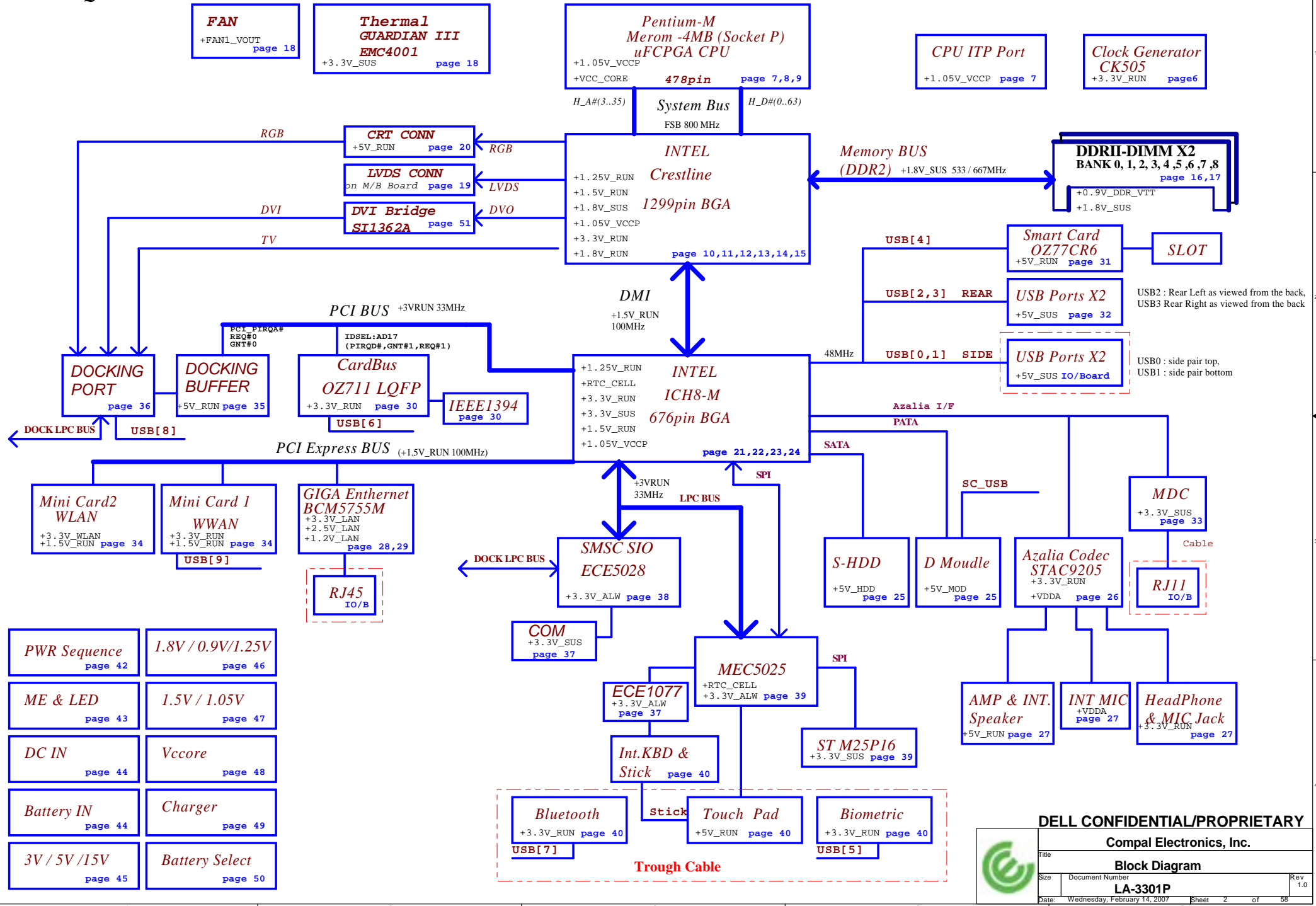
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Title		Cover Sheet	
Size	Document Number	Rev	1.0
Date: Wednesday, March 07, 2007		Sheet	1 of 58

**Block Diagram**  
 Compal confidential  
 Model : IBQ00



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Block Diagram

LA-3301P

**POWER STATES**

State \ Signal	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M1	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	OFF	ON
S4 (Suspend to DISK) / M1	LOW	HIGH	HIGH	LOW	HIGH	ON	ON	ON	OFF	ON
S5 (SOFT OFF) / M1	LOW	HIGH	LOW	LOW	HIGH	ON	ON	ON	OFF	ON
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

**PM TABLE**

State \ power plane	+15V_ALW +5V_ALW +3.3V_ALW +3.3V_RTC_LDO	+5V_SUS +3.3V_SUS +1.8V_SUS	+5V_RUN +3.3V_RUN +2.5V_RUN +1.8V_RUN +1.5V_RUN +0.9V_DDR_VTT +VCC_CORE +1.05V_VCCP +1.25V_RUN
S0	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC don't exist	OFF	OFF	OFF

**PCI TABLE**

PCI DEVICE	IDSEL	REQ#/GNT#	PIRQ
OZ711	AD17	REQ#1 / GNT#1	PIRQD
Docking	AD24	REQ#0 / GNT#0	PIRQA

	USB PORT#	DESTINATION
<b>ICH8-M</b>	0	Side Top
	1	Side Bottom
	2	Rear Left
	3	Rear Right
	4	Smart Card
	5	Biometric
	6	Card Bus
	7	Bluetooth
	8	Docking
	9	WWAN
<b>ECE 5028</b>	1	None
	2	None
	3	None
	4	None

PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-1 WWAN
Lane 2	MINI CARD-2 WLAN
Lane 3	None
Lane 4	None
Lane 5	None
Lane 6	GIGA LAN

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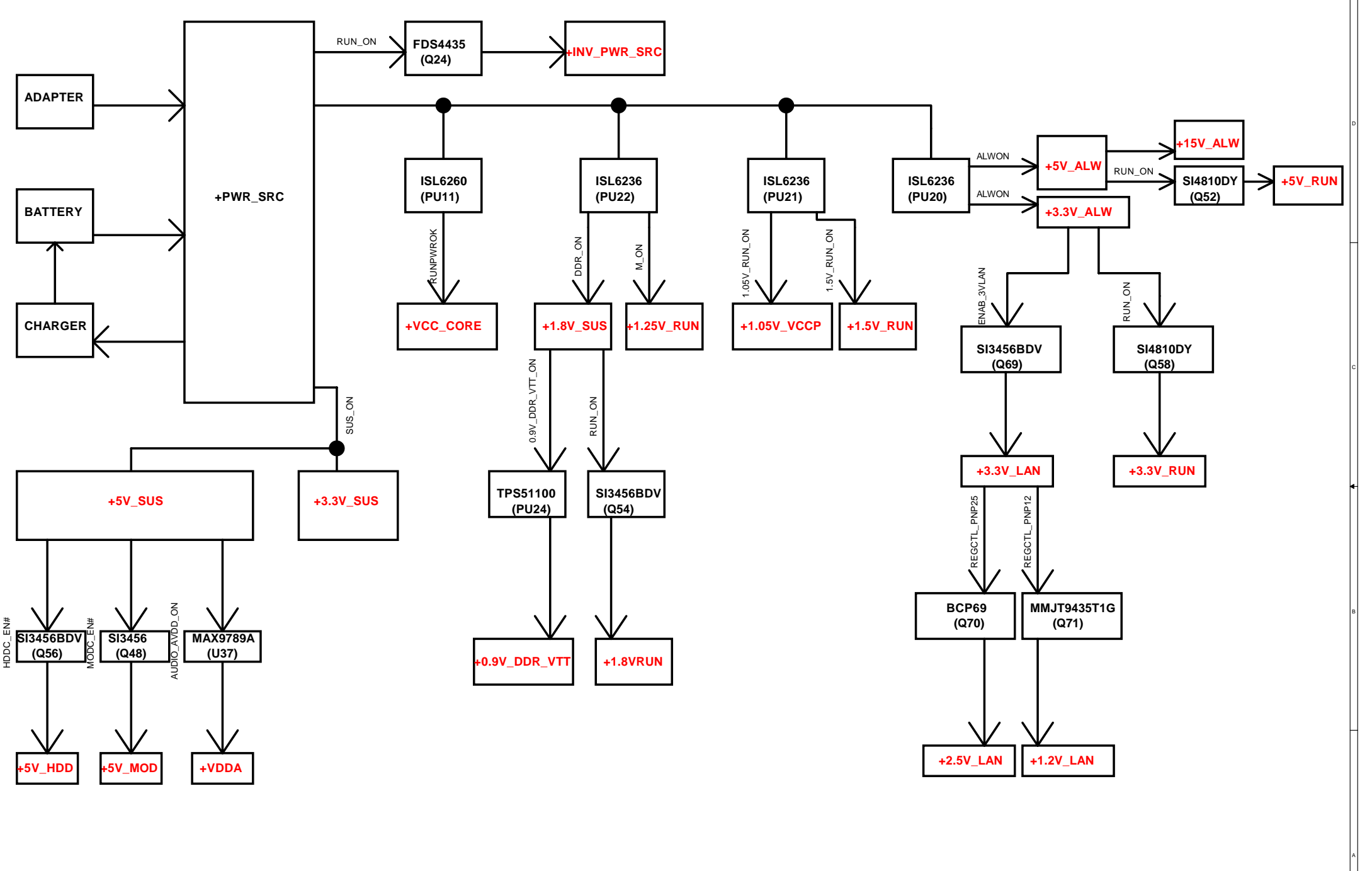
Index and Config.

LA-3301P

Title	Index and Config.		Rev
Size	Document Number	1.0	
Date:	Wednesday, February 14, 2007	Sheet	3 of 58

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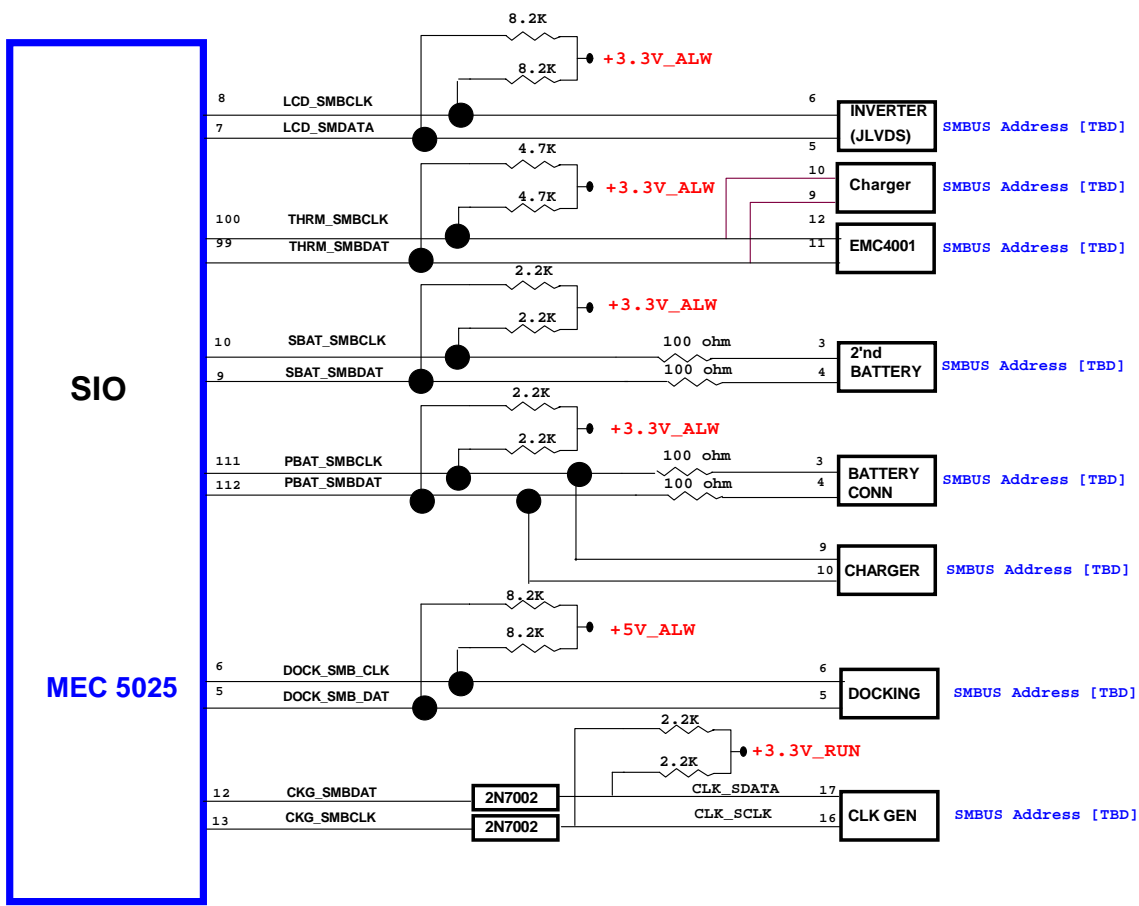
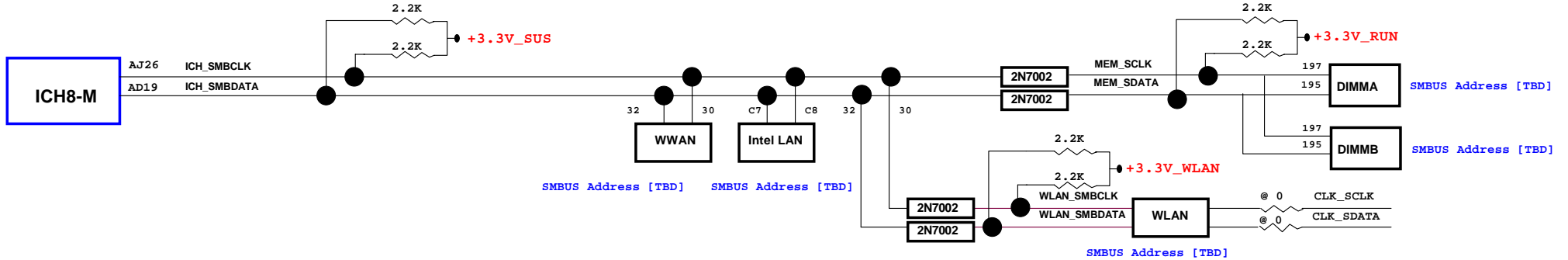


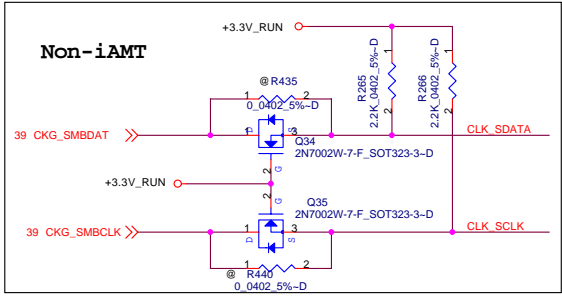
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Title <b>Power Rail</b>			
Size	Document Number	Rev 1.0	
Date: Wednesday, February 14, 2007		Sheet	4 of 58

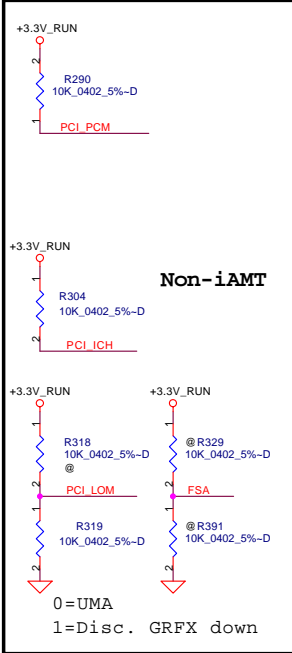




FSC	FSB	FSA	CPU	SRC	PCI
CLKSEL2	CLKSEL1	CLKSELO	MHz	MHz	MHz
0	0	0	266	100	33.3
0	0	1	133	100	33.3
0	1	0	200	100	33.3
0	1	1	166	100	33.3
1	0	0	333	100	33.3
1	0	1	100	100	33.3
1	1	0	400	100	33.3
1	1	1	200	100	33.3

Table : ICS954305AK

CPU_BSEL	CPU_BSEL2(FSC)	CPU_BSEL1(FSB)
133	0	0
166	0	1

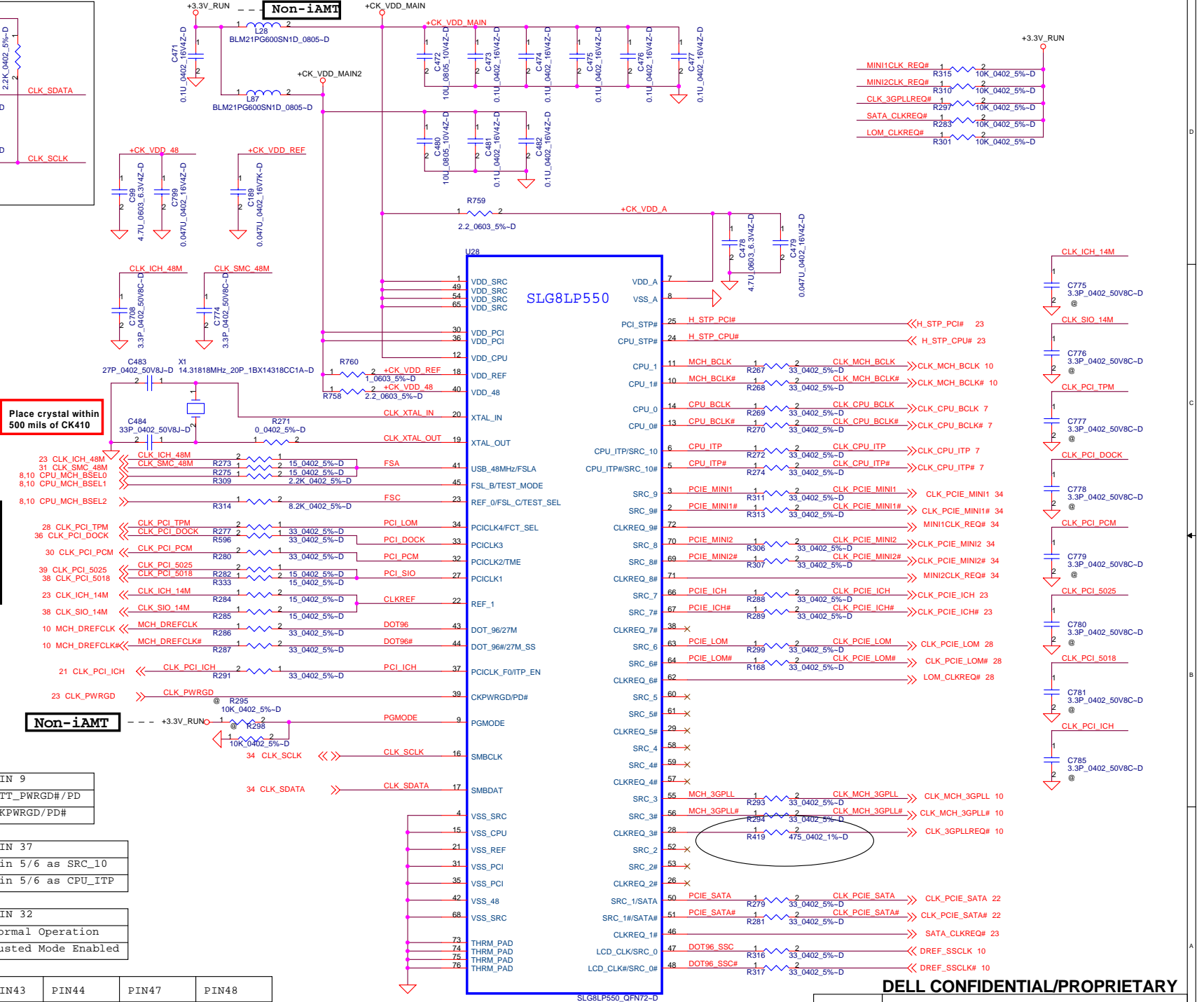


PGMODE	PIN 9
0	VTT_PWRGD#/PD
1	CKPWRGD/PD#

ITP_EN	PIN 37
0	Pin 5/6 as SRC_10
1	Pin 5/6 as CPU_ITP

TME	PIN 32
0	Normal Operation
1	Trusted Mode Enabled

FCTSEL1	PIN43	PIN44	PIN47	PIN48
0=UMA	DOT96T	DOT96C	96/100M_T	96/100M_C
1=DIS	27M_out	27M SSout	SRCT0	SRCC0



Place crystal within 500 mils of CK410

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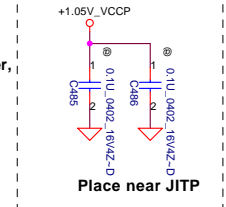
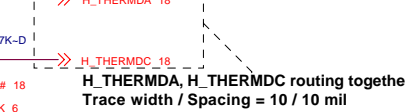
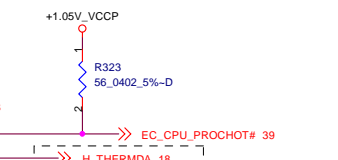
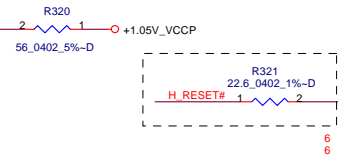
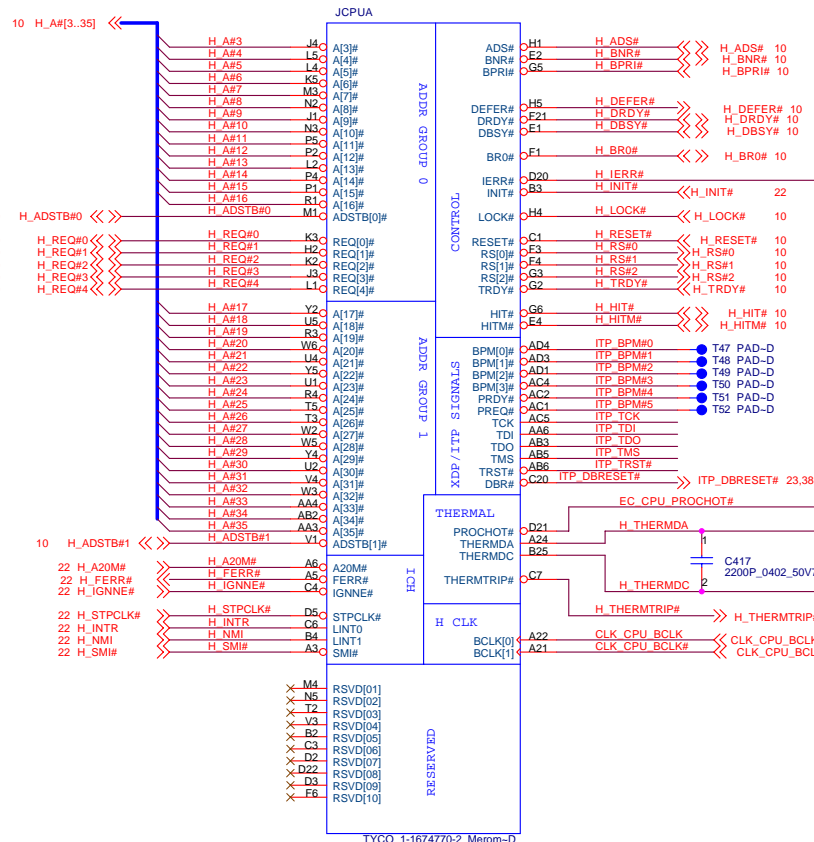
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**Clock Generator**

**LA-3301P**

Date: Monday, February 26, 2007 Sheet 6 of 58

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H\_THERMDA, H\_THERMDC routing together,  
Trace width / Spacing = 10 / 10 mil

Place near JITP

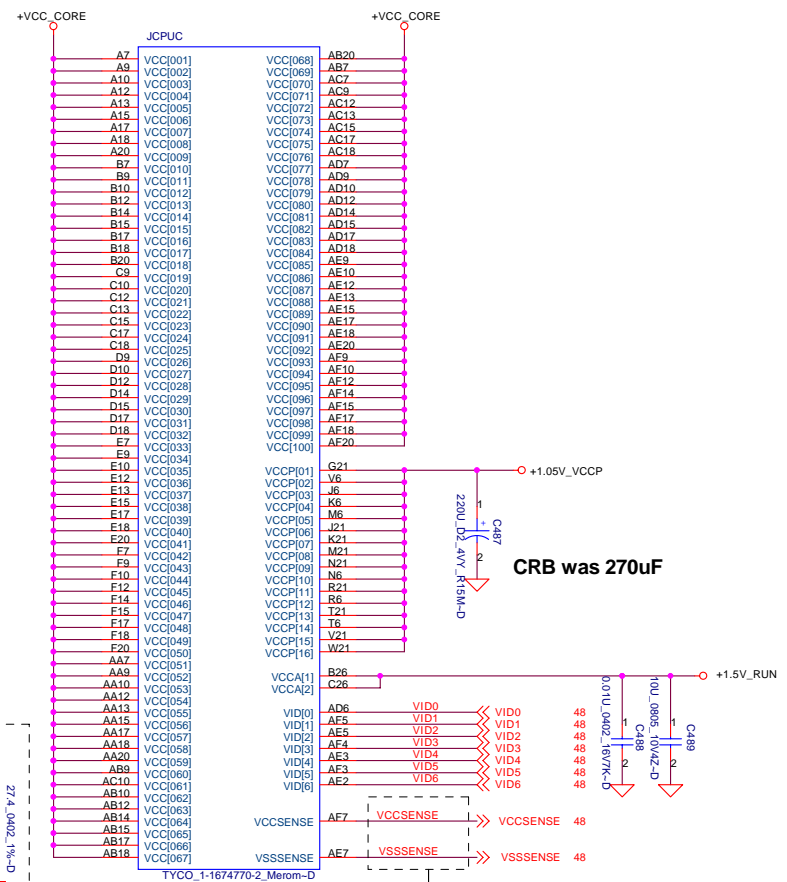
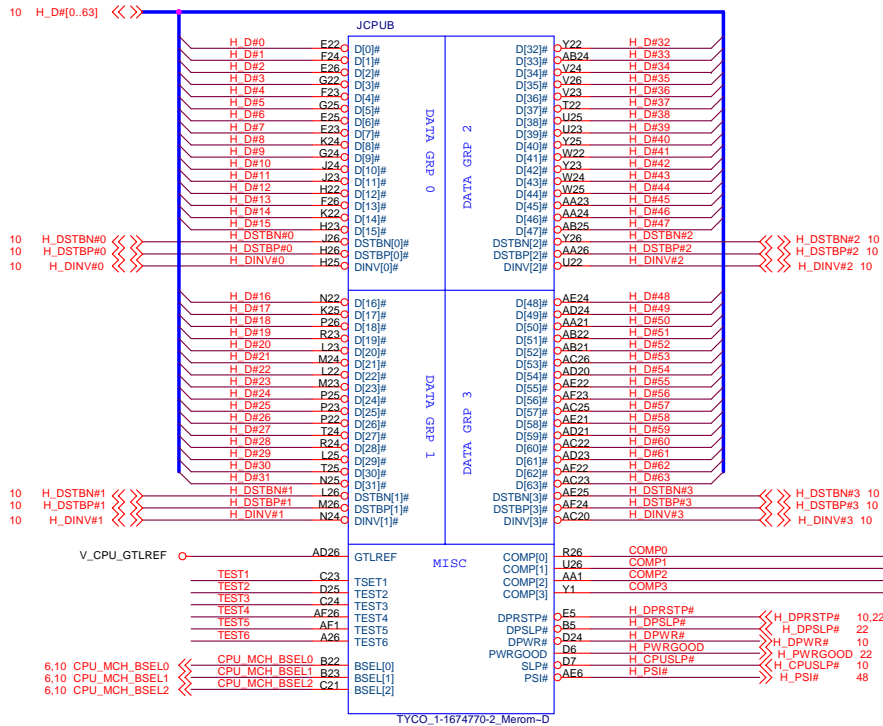
This shall place near CPU

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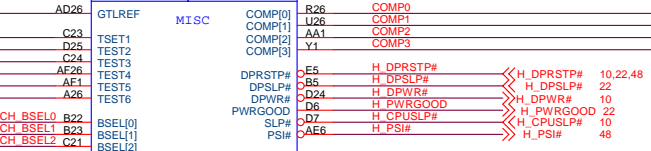
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Title			Merom Processor (1/2)		
Size	Document Number	Rev			1.0
LA-3301P					
Date:	Monday, February 26, 2007	Sheet	7	of	58

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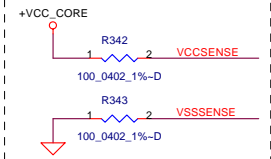
6,10 CPU\_MCH\_BSEL0  
6,10 CPU\_MCH\_BSEL1  
6,10 CPU\_MCH\_BSEL2



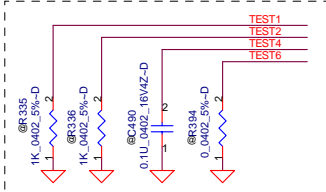
Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMPO, COMP2 trace should be 27.4 ohm. COMP1, COMP3 should be 55 ohm.

Length match within 25 mils Z0=27.4 ohm

Place R342 and R343 near CPU



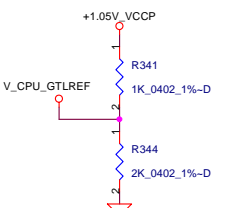
Route VCCSENSE and VSSSENSE trace at 27.4 ohms, 7 mils spacing and 1 inch (max)



For the purpose of testability, route these signals through a ground referenced Z0 = 55ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.

Place C close to the CPU\_TEST4 pin. Make sure CPU\_TEST4 routing is reference to GND and away from other noisy signal.

FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0

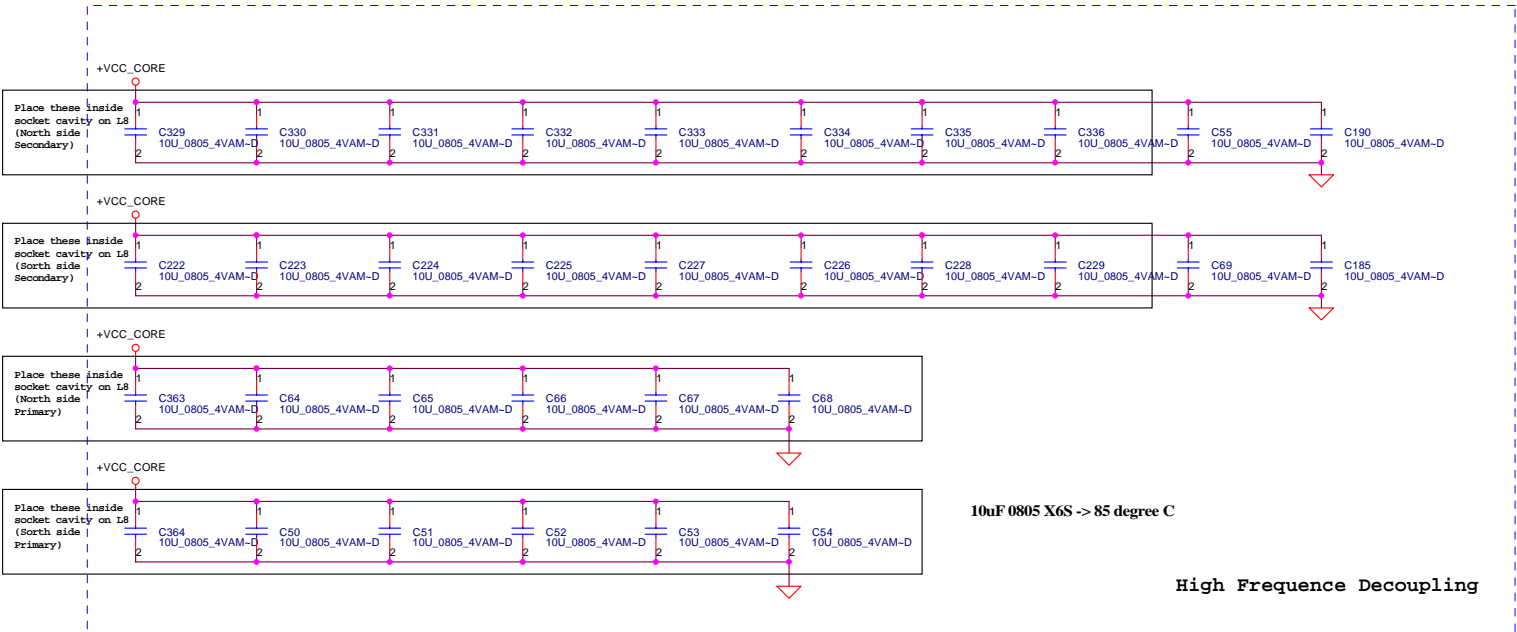


Layout close CPU PIN AD26  
55 ohm, 0.5 inch (max)

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 Title: Merom Processor(2/2)  
 Part Number: LA-3301P  
 Date: Monday, February 26, 2007  
 Sheet 8 of 58

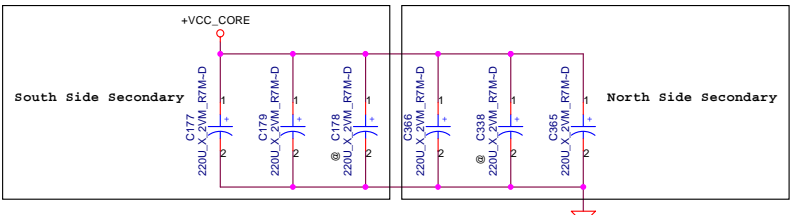




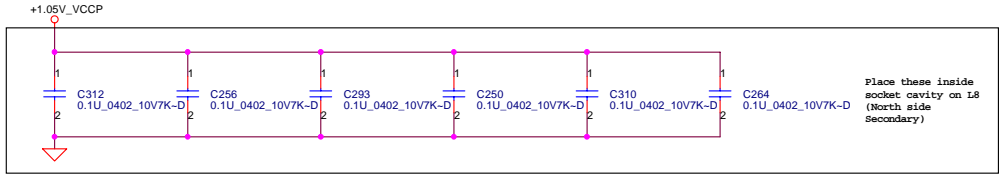
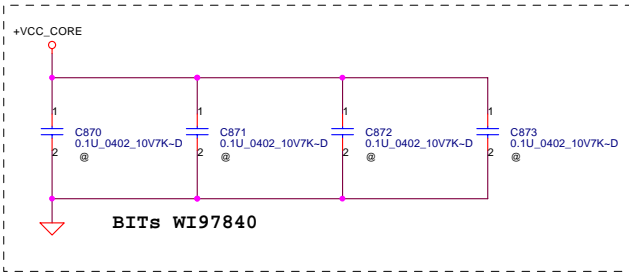
10uF 0805 X6S -> 85 degree C

High Frequency Decoupling

Near VCORE regulator.



ESR <= 1.5m ohm  
Capacitor > 1980uF



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CPU Bypass

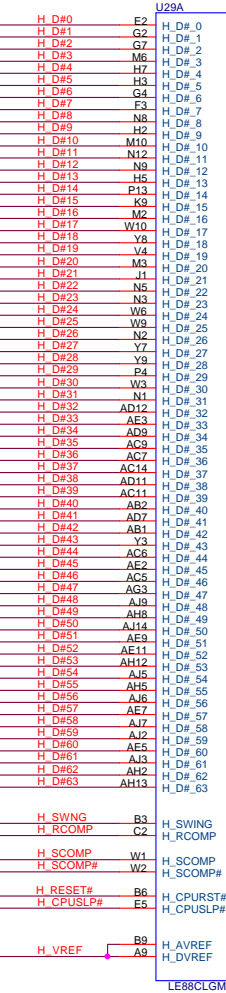
LA-3301P

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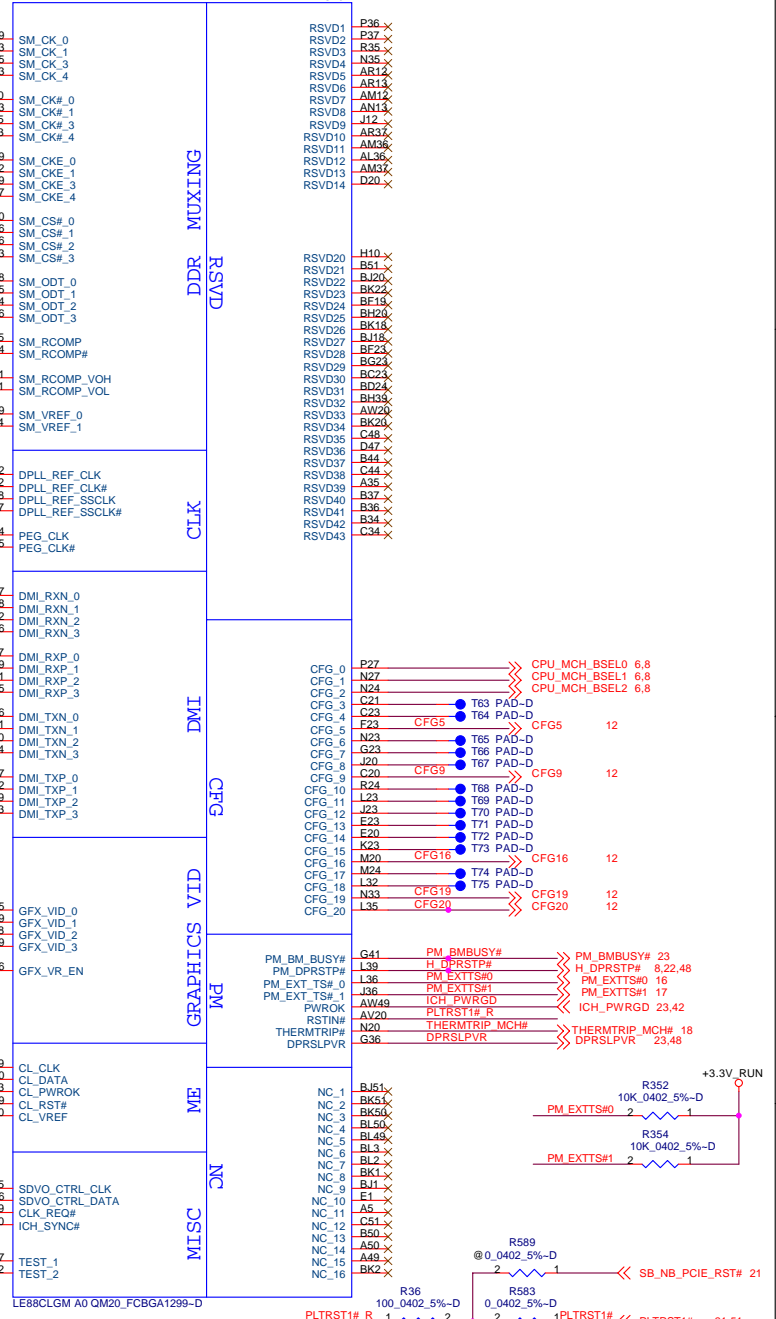
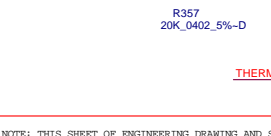
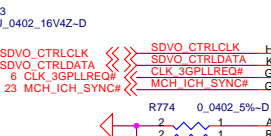
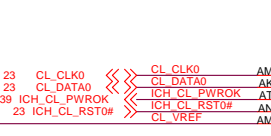
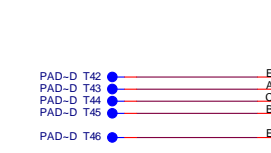
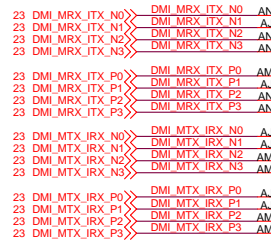
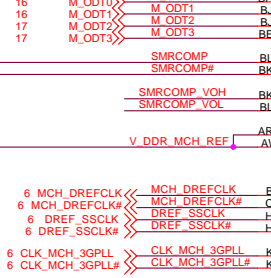
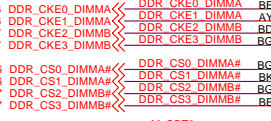
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Size	Document Number			
Date	Wednesday, February 14, 2007	Sheet	9	of 58

8 H\_D#0[0.63] <<>

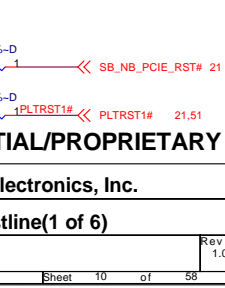
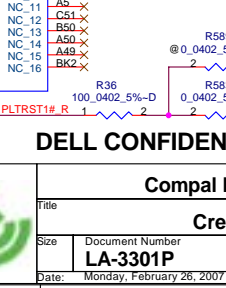
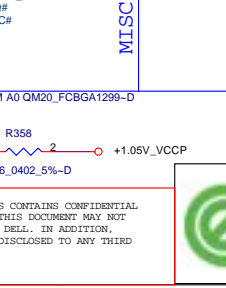
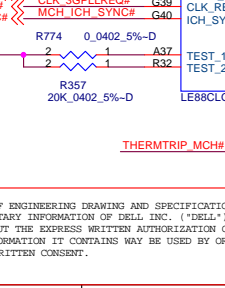
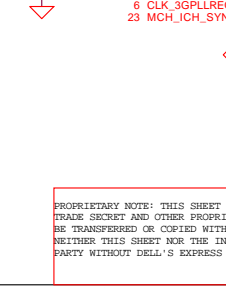
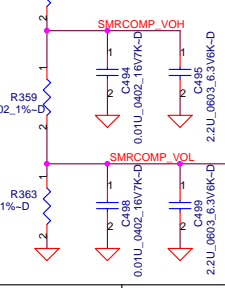
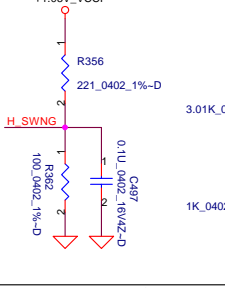
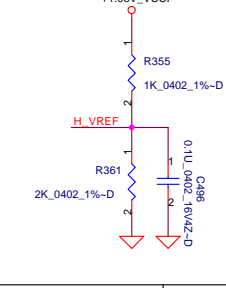
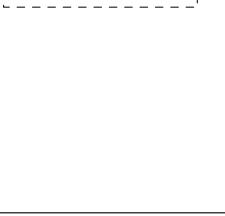


HOST

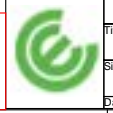
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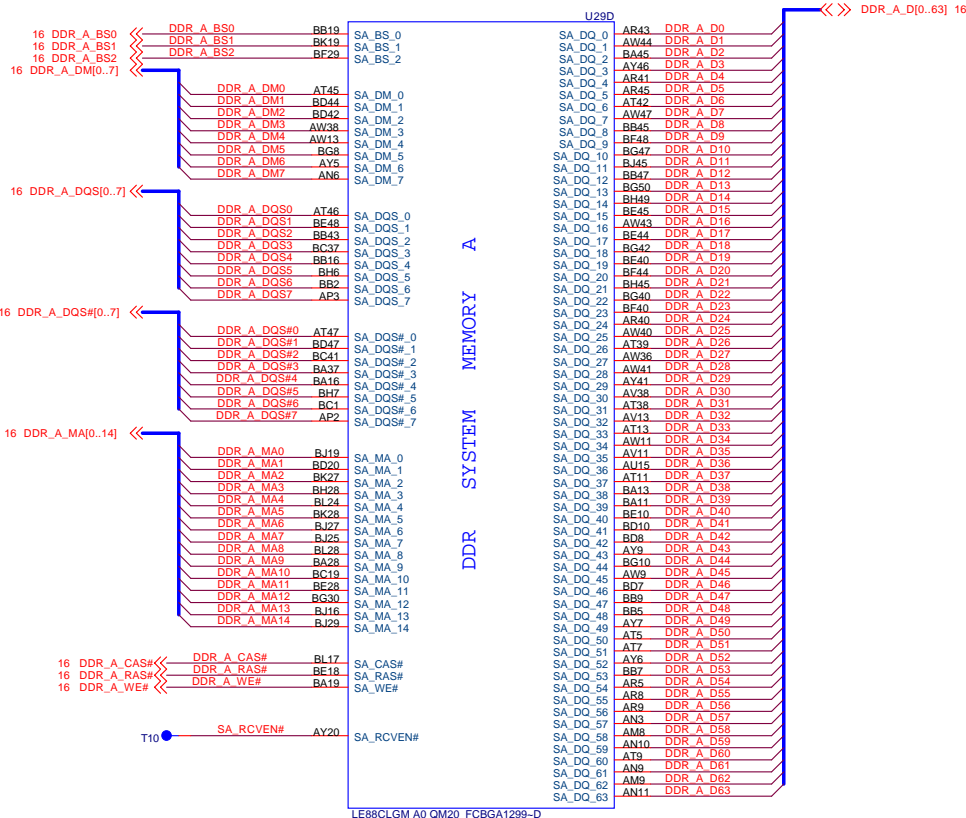
Layout Note: H\_RCOMP trace width and spacing is 10/20



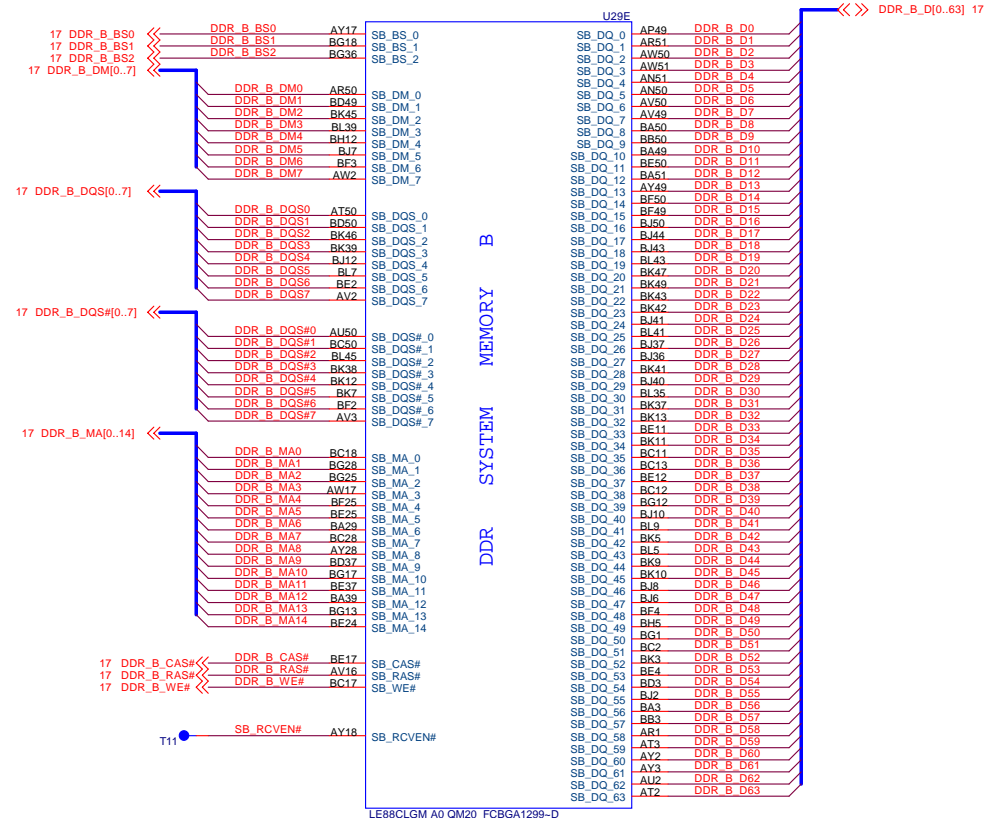
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LE88CLGM A0 QM20\_FCBGA1299-D



LE88CLGM A0 QM20\_FCBGA1299-D

DDR SYSTEM MEMORY A

DDR SYSTEM MEMORY B

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Crestline(2 of 6)

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Size	Document Number	Rev	1.0
	LA-3301P		
Date:	Monday, February 26, 2007	Sheet	11 of 58

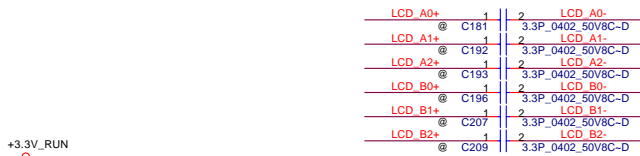
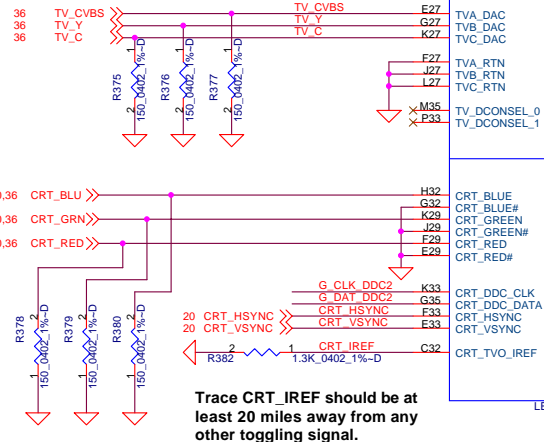
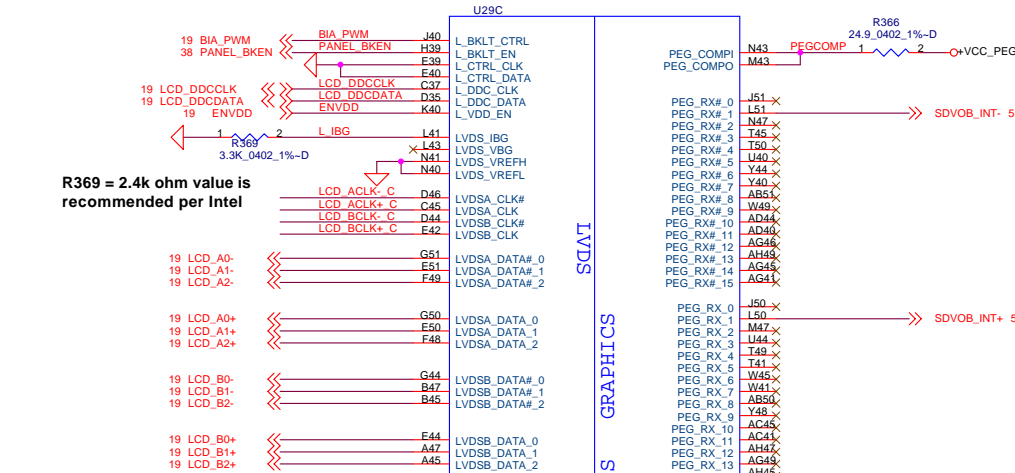
# Strap Pin Table

CFG5	DMI X2 Select	Low = DMI x 2 High = DMI x 4 (Default)
CFG9	PCI Express Graphic Lane	Low = Reverse Lane High = Normal Operation (Default)
CFG16	FSB Dynamic ODT	Low=Dynamic ODT Disable High=Dynamic ODT Enable(default)
CFG19	DMI Lane Reversal	Low=Normal (default) High=Lane Reversed
CFG20	SDVO/PCIE Concurrent Operation	Low=Only SDVO or PCIe1 is operational (defaults) High=SDVO and PCIe1 are operating simultaneously via PEG port
SDVO_CTRL_DATA		Low=No SDVO Device Present High=SDVO Device Present (default)

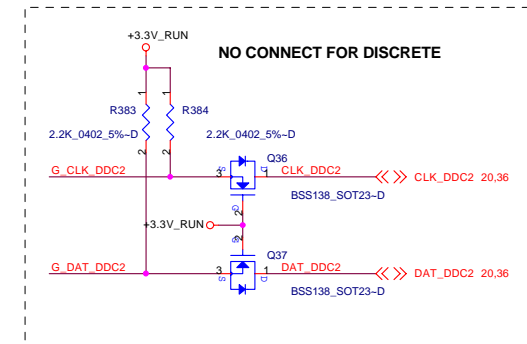
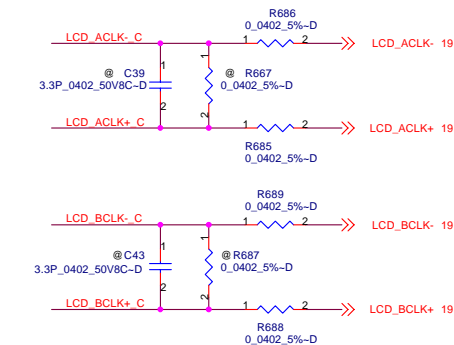
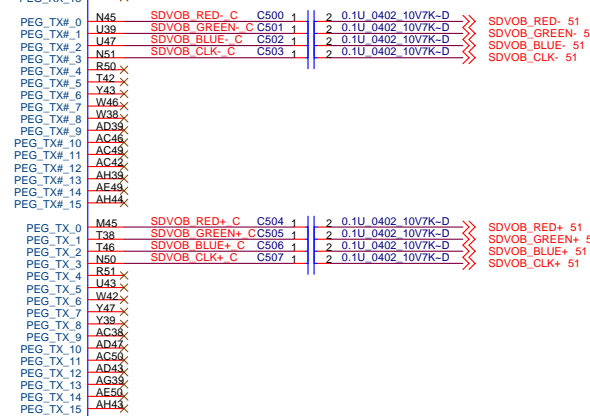


CFG[3:17] have internal pullup

CFG[18:19] have internal pulldown



Keep stub for caps as small as possible



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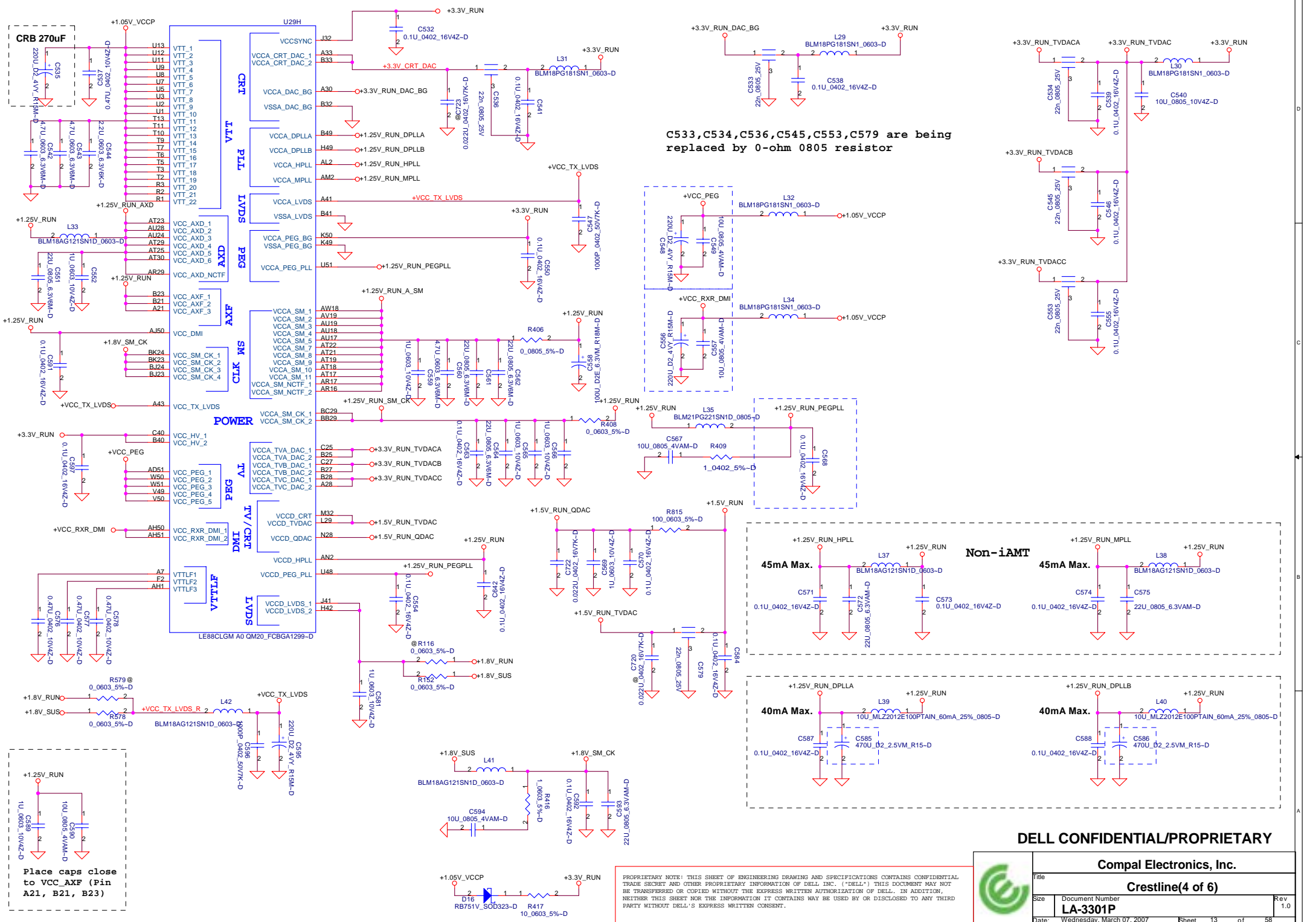


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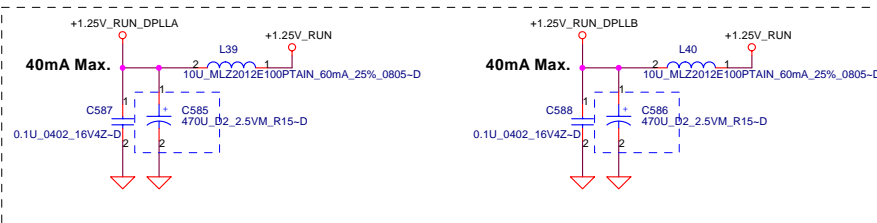
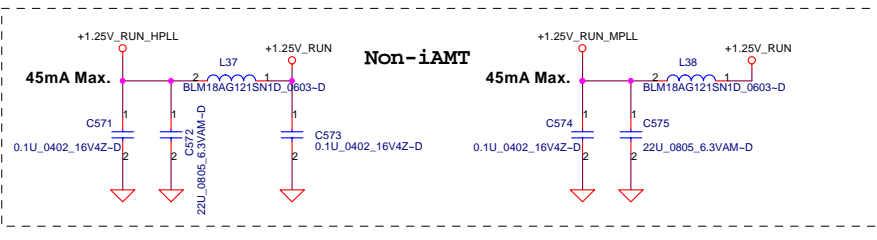
Compal Electronics, Inc.

Crestline(3 of 6)

Title	LA-3301P		
Size	Document Number	Rev	1.0
Date	Monday, February 26, 2007	Sheet	12 of 58




C533, C534, C536, C545, C553, C579 are being replaced by 0-ohm 0805 resistor



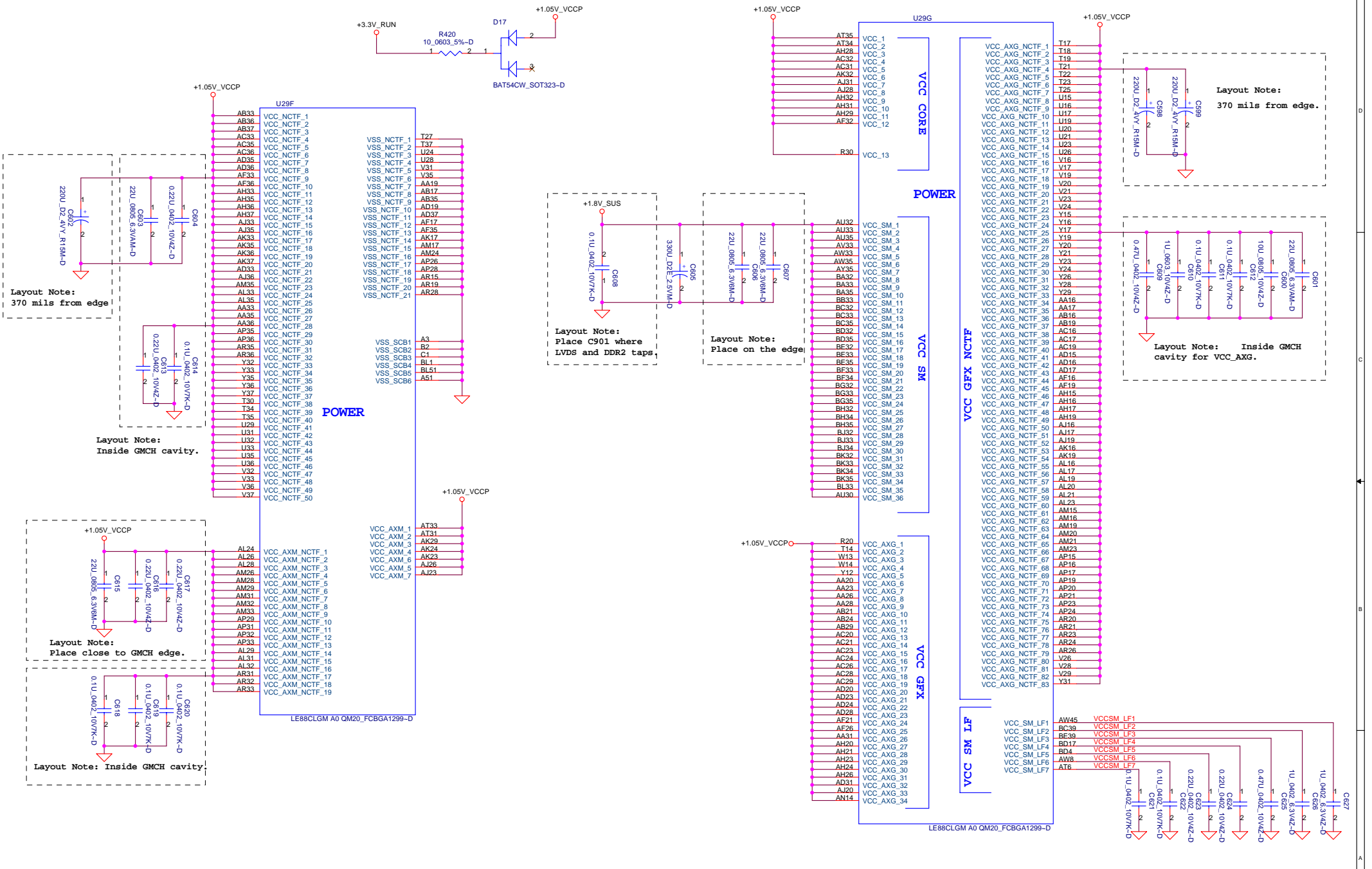
Place caps close to VCC AXF (Pin A21, B21, B23)

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		<b>Crestline(4 of 6)</b>	
Size	Document Number	Rev	
	<b>LA-3301P</b>	1.0	
Date:	Wednesday, March 07, 2007	Sheet	13 of 58





Layout Note:  
370 mils from edge

Layout Note:  
Inside GMCH cavity.

Layout Note:  
Place close to GMCH edge.

Layout Note:  
Inside GMCH cavity.

Layout Note:  
Place C901 where  
LVDS and DDR2 taps

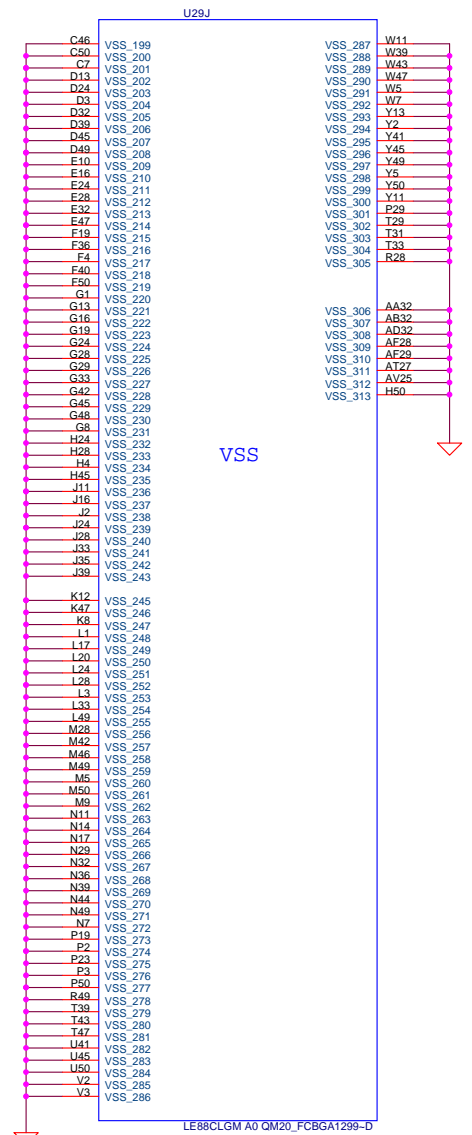
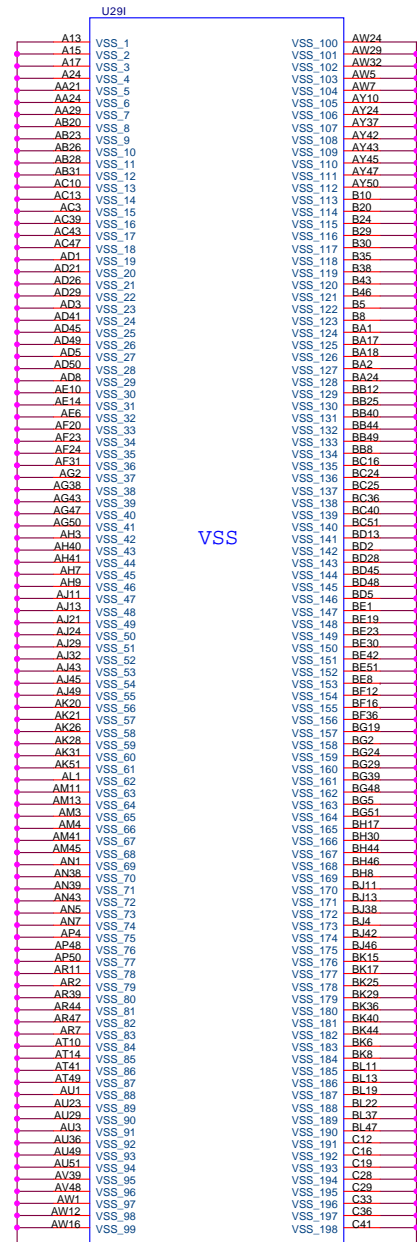
Layout Note:  
Place on the edge

Layout Note:  
370 mils from edge.

Layout Note:  
Inside GMCH  
cavity for VCC\_AXG.

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LE88CLGM A0 QM20\_FCBGA1299-D

LE88CLGM A0 QM20\_FCBGA1299-D

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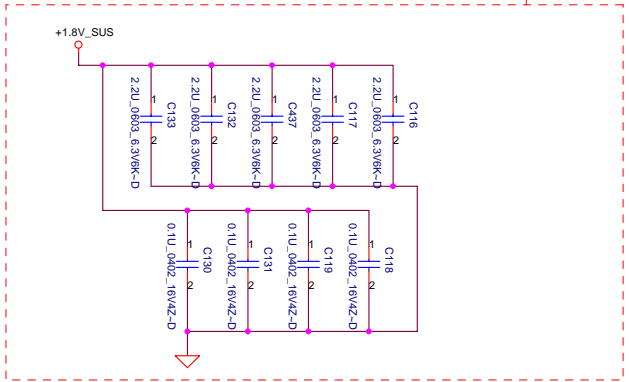
Title		
Crestline(6 of 6)		
Size	Document Number	Rev
	LA-3301P	1.0
Date:	Wednesday, February 14, 2007	Sheet 15 of 58

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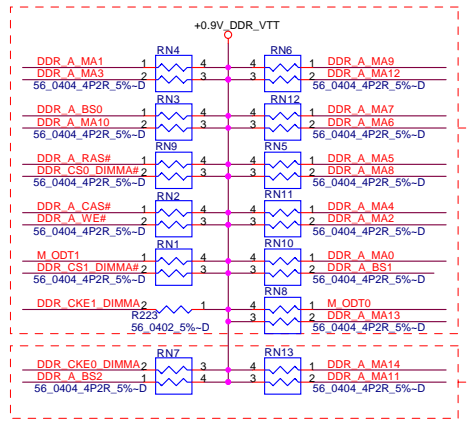
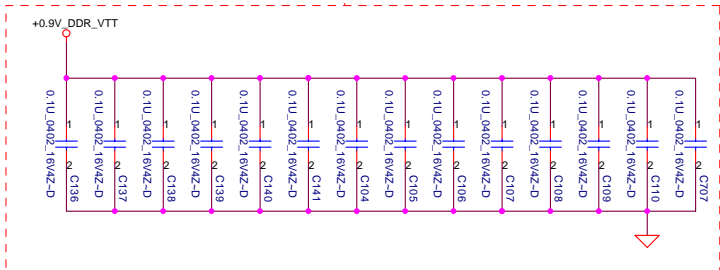


- 11 DDR\_A\_DQS#[0..7] <<>>
- 11 DDR\_A\_D[0..63] <<>>
- 11 DDR\_A\_DM[0..7] <<>>
- 11 DDR\_A\_DQS#[7..K] <<>>
- 11 DDR\_A\_MA[0..14] <<>>

**Layout Note:**  
Place near JDIM1



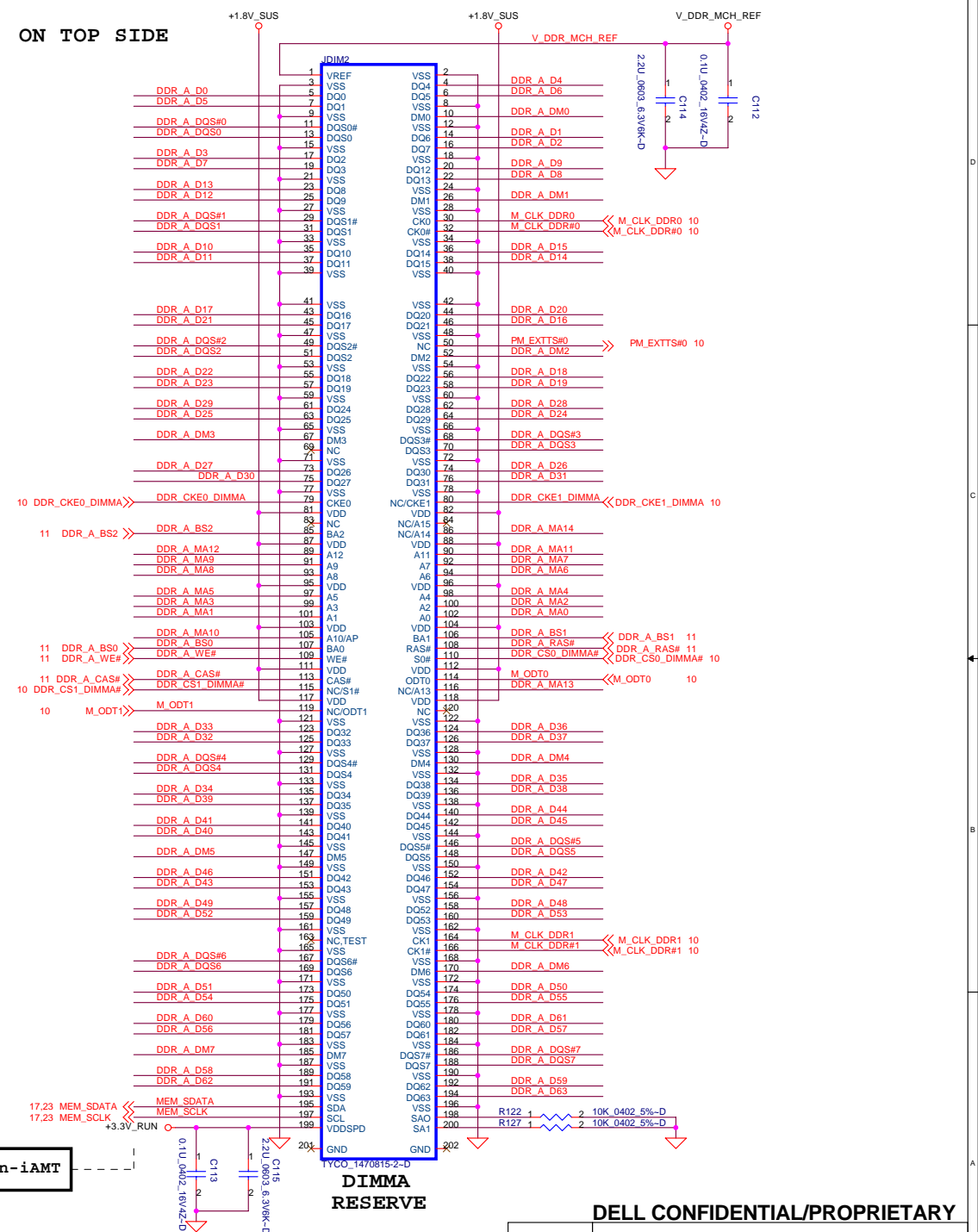
**Layout Note:**  
Place one cap close to every 2 pullup resistors terminated to +0.9V\_DDR\_VTT



**Layout Note:**  
Place these resistor closely DIMM0, all trace length < 750 mil

**Layout Note:**  
Place these resistor closely DIMM0, all trace length Max=1.3"

**ON TOP SIDE**



Non-iAMT

**DIMM RESERVE**

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**DDR11-SODIMM SLOT1**

LA-3301P

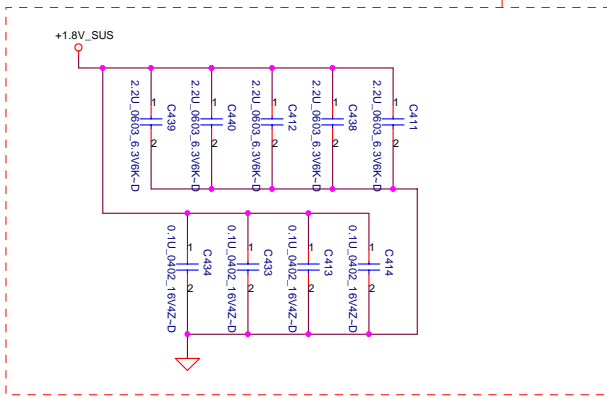
Monday, February 26, 2007

Sheet 16 of 58

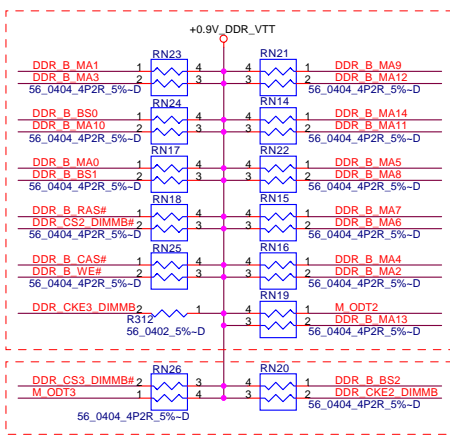
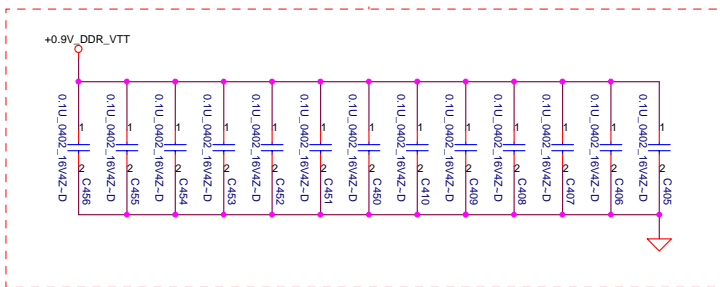


- 11 DDR\_B\_DQS#[0..7] <<>>
- 11 DDR\_B\_DQ[0..63] <<>>
- 11 DDR\_B\_DM[0..7] <<>>
- 11 DDR\_B\_DQS[0..7] <<>>
- 11 DDR\_B\_MA[0..14] <<>>

**Layout Note:**  
Place near JDIM2



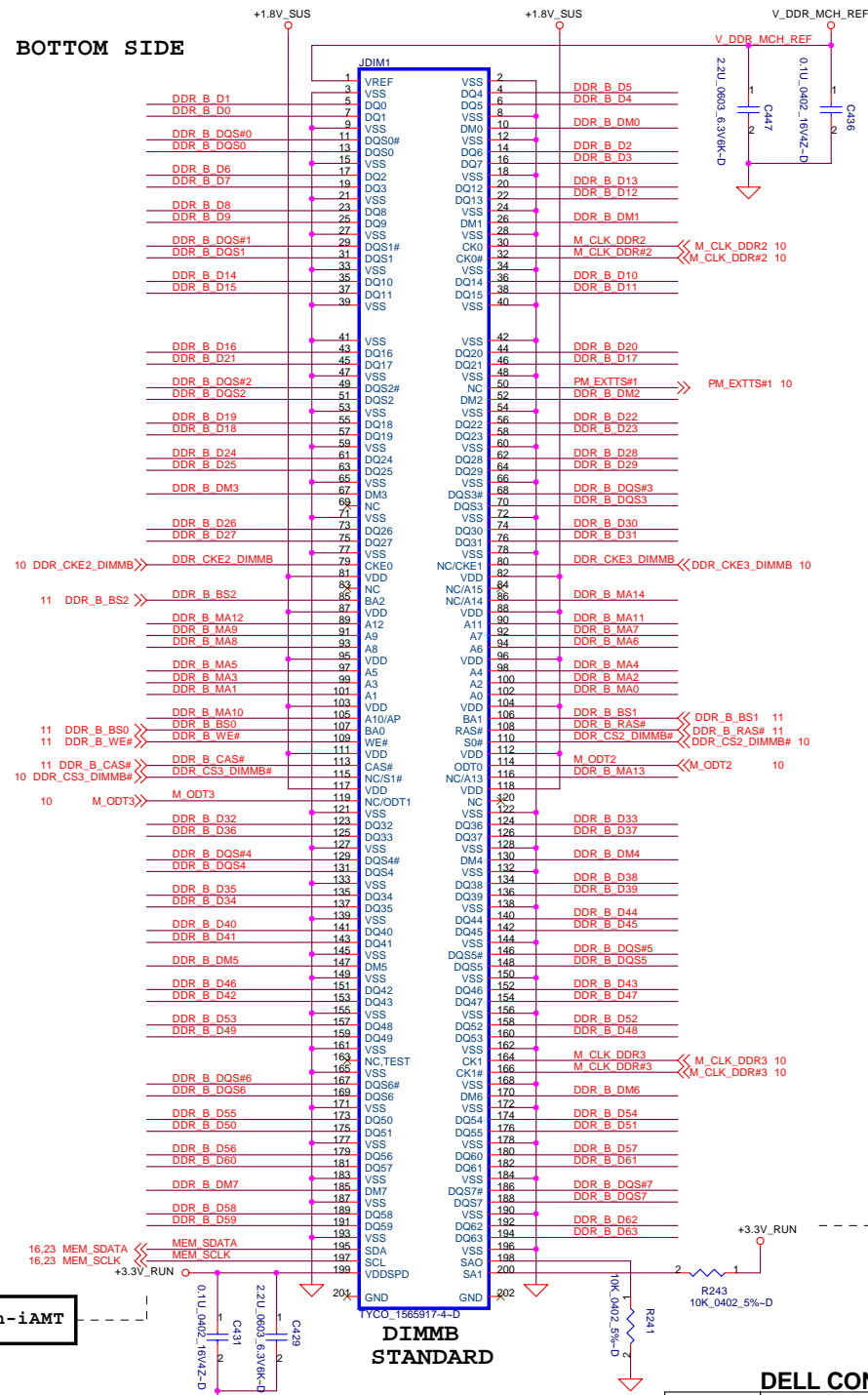
**Layout Note:**  
Place one cap close to every 2 pullup resistors terminated to +0.9V\_DDR\_VTT



**Layout Note:**  
Place these resistor closely DIMM0,all trace length<750 mil

**Layout Note:**  
Place these resistor closely DIMM0,all trace length Max=1.3"

**ON BOTTOM SIDE**



**Non-iAMT**

**Non-iAMT**

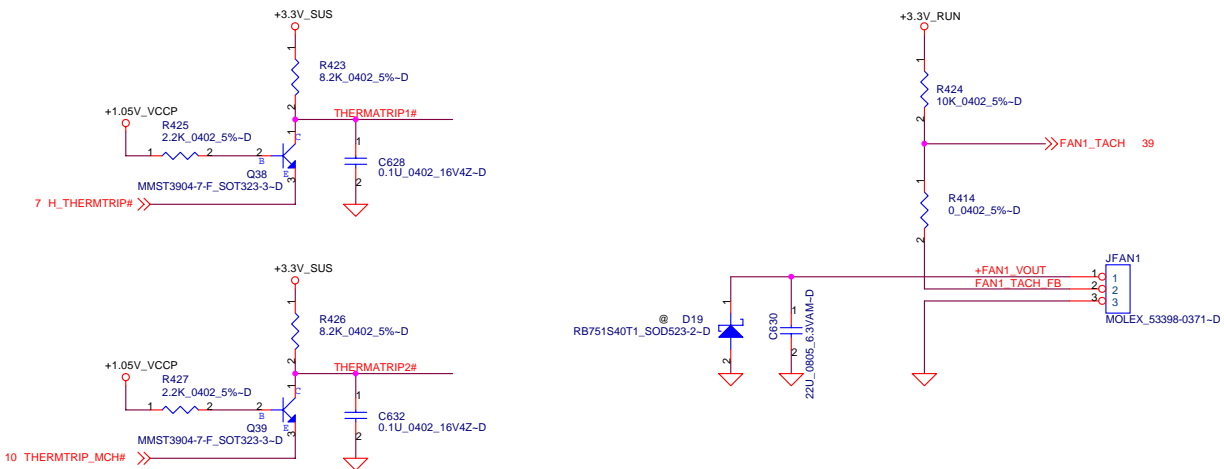
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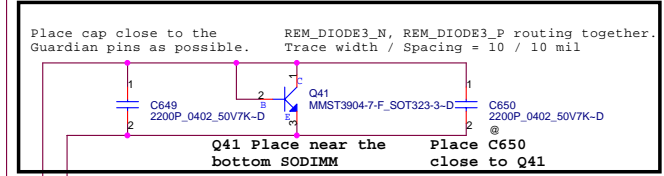
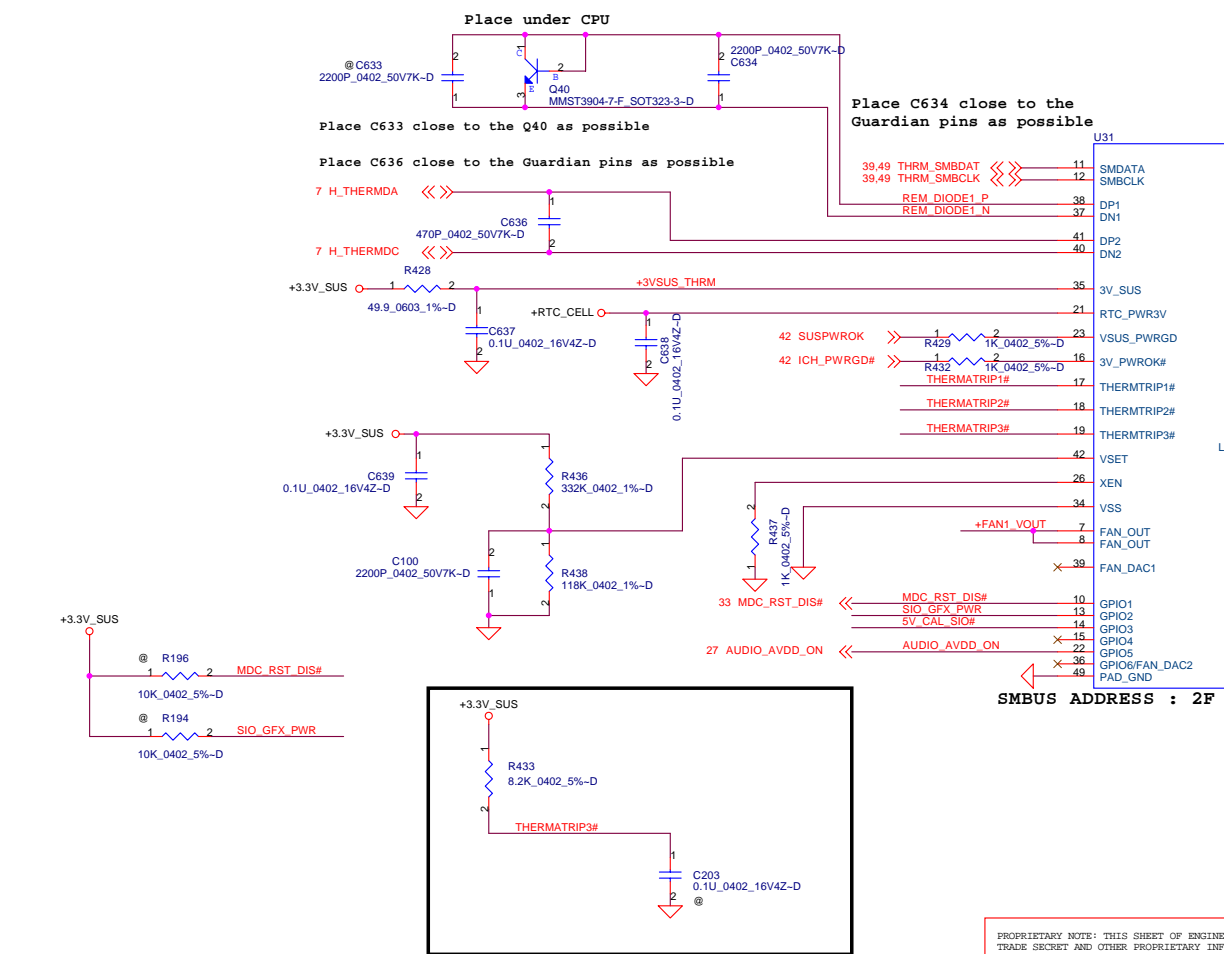
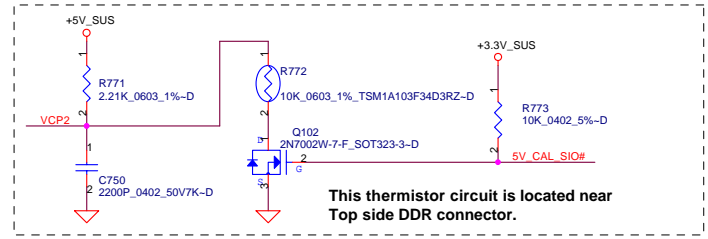
<b>Compal Electronics, Inc.</b>		
<b>DDRII-SODIMM SLOT2</b>		
File	Document Number	Rev
<b>LA-3301P</b>		1.0
Date:	Monday, February 26, 2007	Sheet 17 of 58

# FAN1 Control and Tachometer

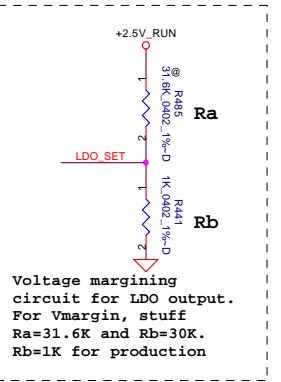


$$VSET = \frac{R438}{R436+R438} \times 3.3V = 0.865V$$

$$VSET = \left( \frac{Tp - 70}{21} \right) \Rightarrow Tp = 88.2 C$$



Diode circuit at DP4/DN4 is used for skin temp sensor (placed optimally between CPU, MCH and MEM).

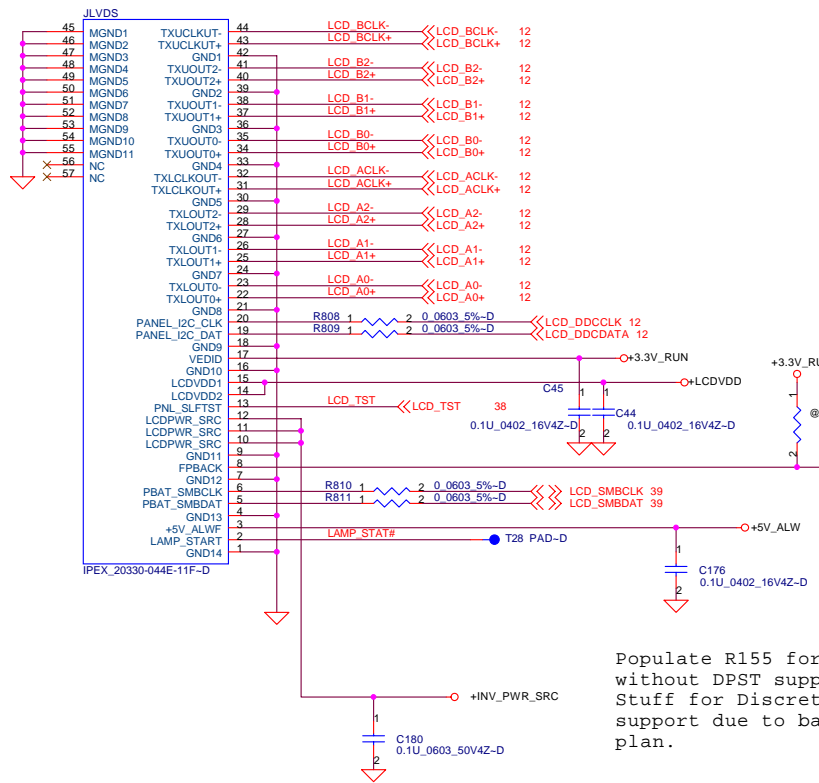


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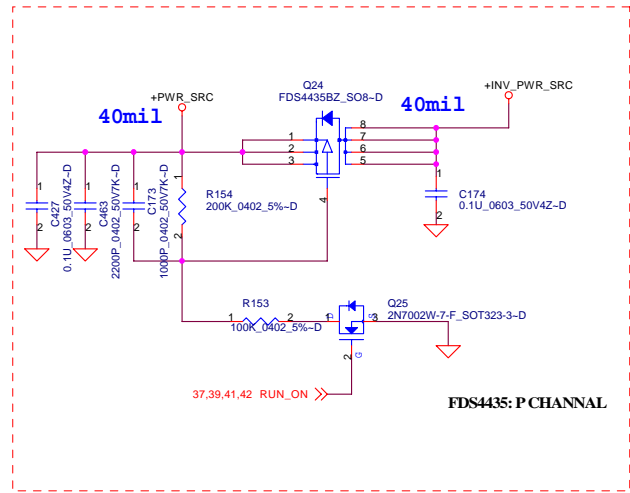
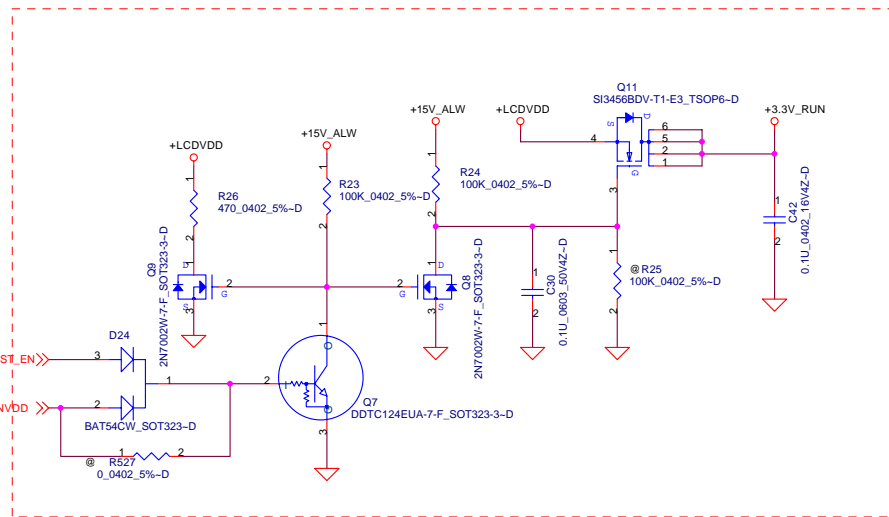
Compal Electronics, Inc.		
Title		
FAN & Thermal Sensor		
Size	Document Number	Rev
	LA-3301P	1.0
Date:	Wednesday, March 07, 2007	Sheet 18 of 58

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Populate R156 for DPST, implementation only.

Populate R155 for platform without DPST support. No Stuff for Discrete DSPT support due to back up plan.



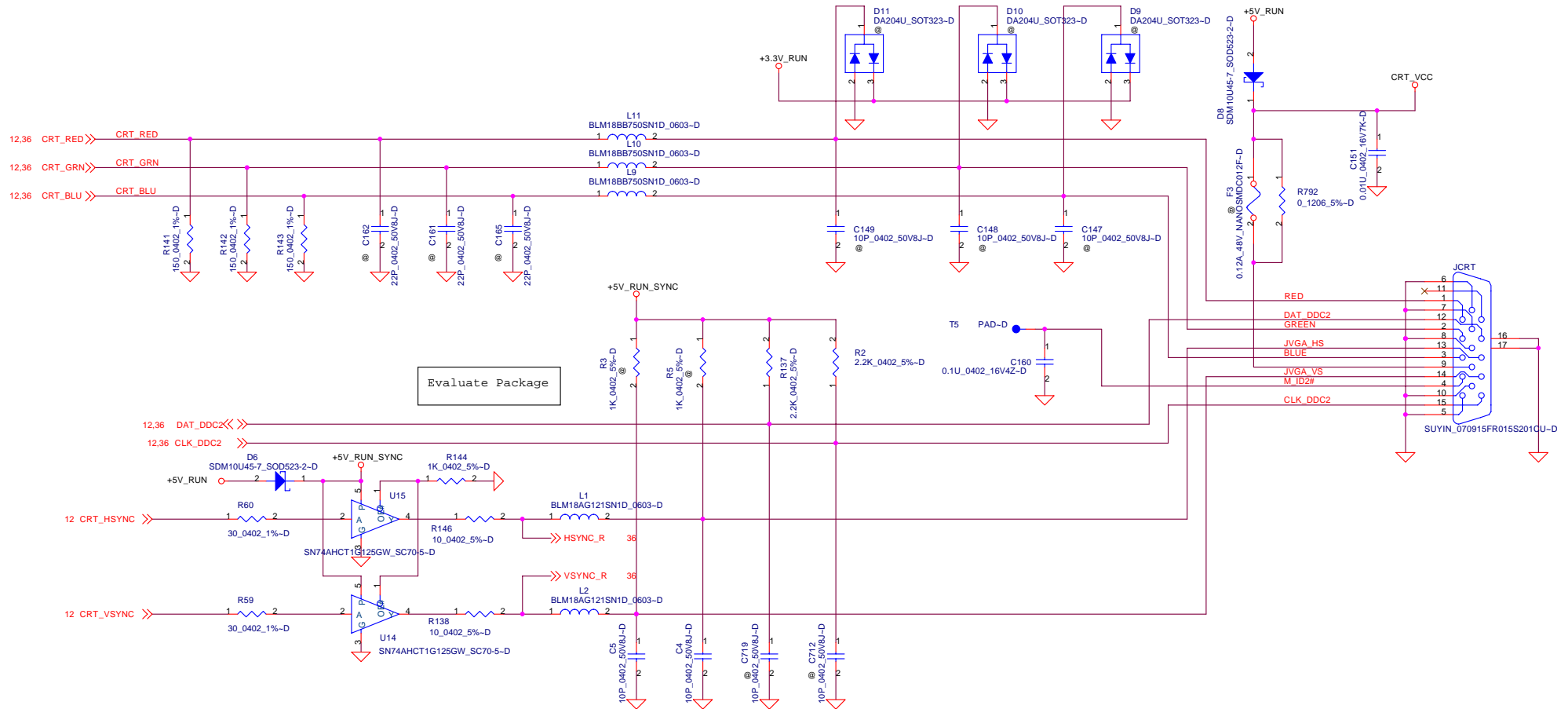
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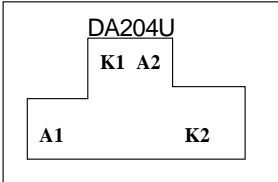
Title		
Internal LVDS		
Size	Document Number	Rev
	LA-3301P	1.0
Date:	Wednesday, February 25, 2007	Sheet 19 of 58

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Evaluate Package



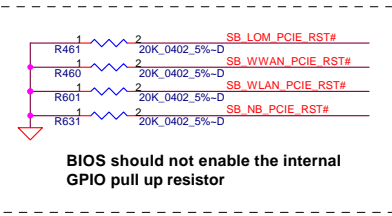
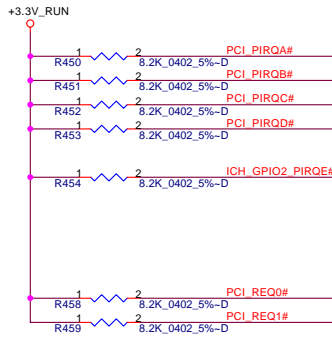
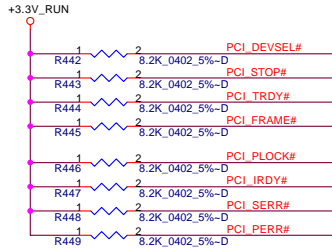
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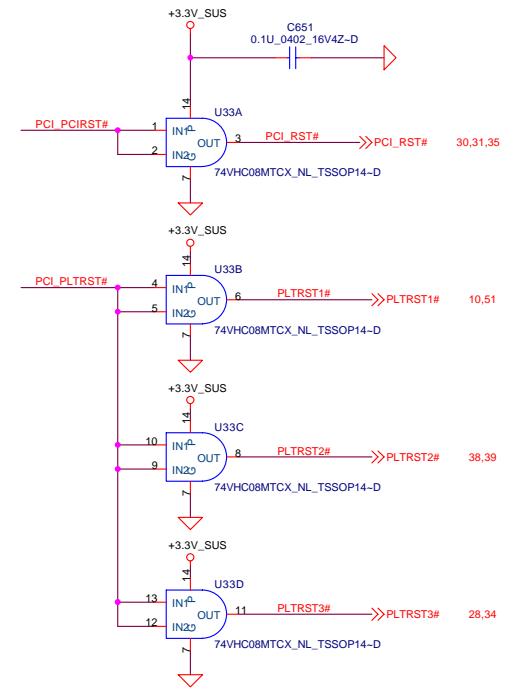
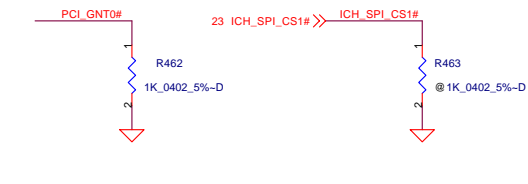
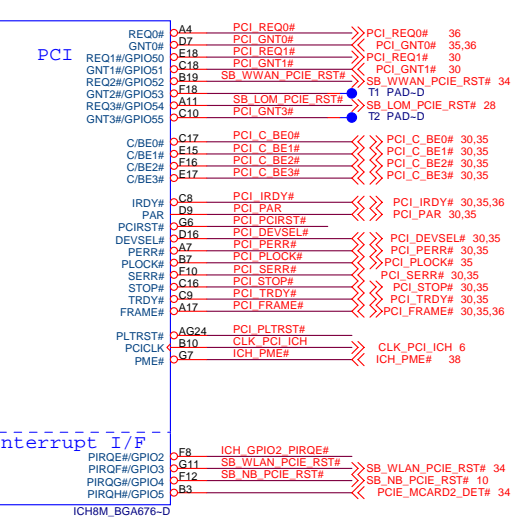
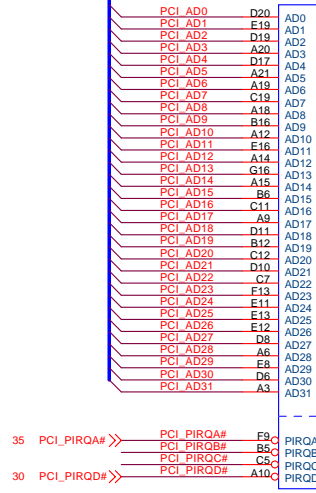
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Title		CRT	
Size	Document Number	Rev	
LA-3301P		1.0	
Date:	Monday, February 26, 2007	Sheet	20 of 58



BIOS should not enable the internal GPIO pull up resistor

30,35 PCI\_AD[0..31] <<>

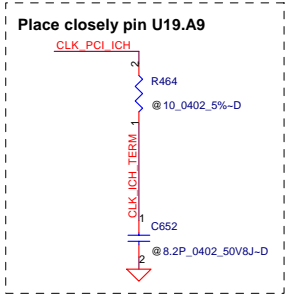


**A16 away override strap.**

PCI_GNT3#	Low = A16 swap override enabled. High = Default.
-----------	---

**Boot BIOS Strap**

PCI_GNT0#	SPI_CS1#	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC



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ICH8(1/4)

Size: Document Number  
**LA-3301P**  
 Date: Monday, February 26, 2007 Sheet 21 of 58

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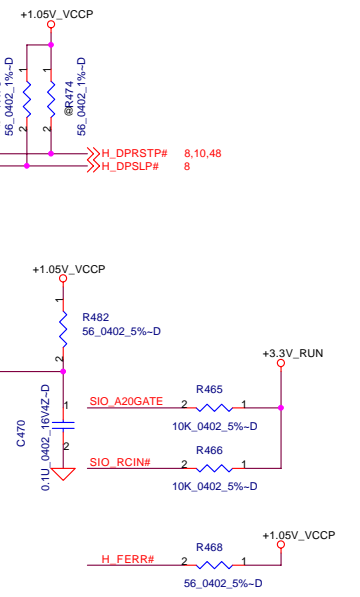
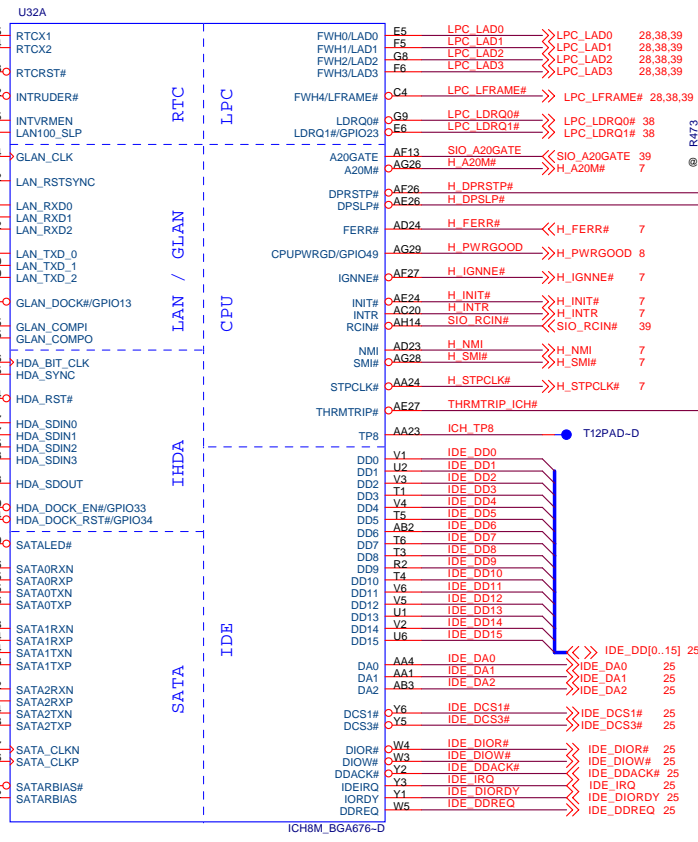
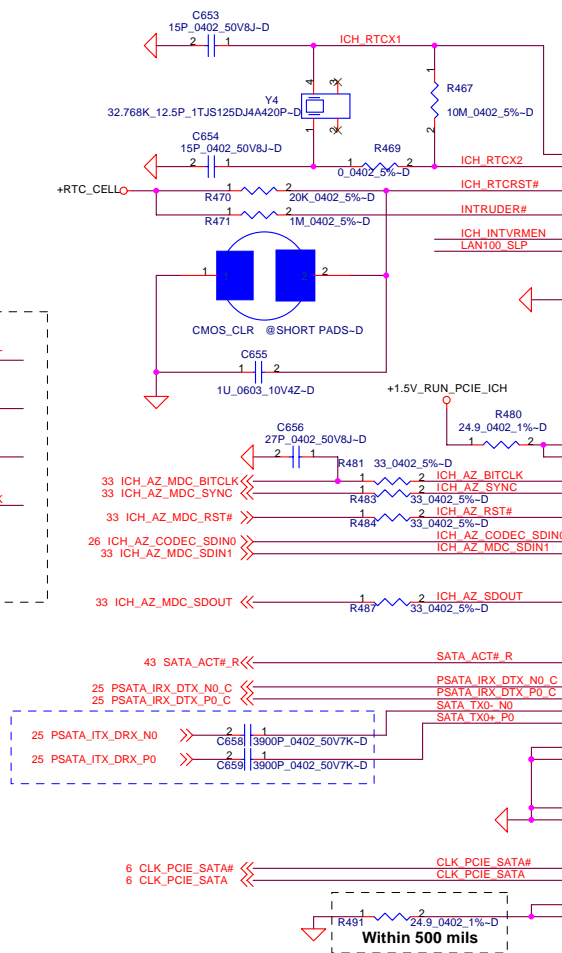
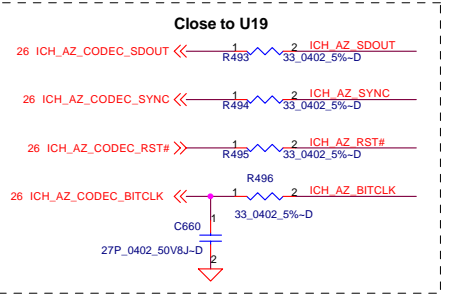
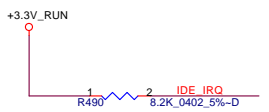
Package  
9.6X4.06 mm

**ICH8M Internal VR Enable Strap**  
(Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)

ICH_INTVRMEN	Low = Internal VR Disabled
	High = Internal VR Enabled(Default)

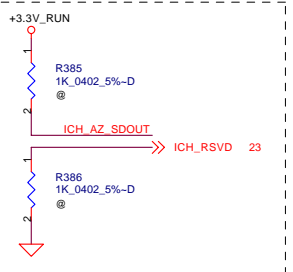
**ICH8M LAN100 SLP Strap**  
(Internal VR for VccLAN1.05 and VccCL1.05)

ICH_LAN100_SLP	Low = Internal VR Disabled
	High = Internal VR Enabled(Default)



**XOR Chain Entrance Strap**

ICH_RSVD	HDA_SDOOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (Default)
1	1	Set PCIE port config bit 1

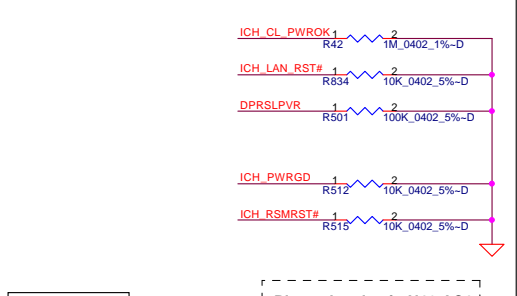
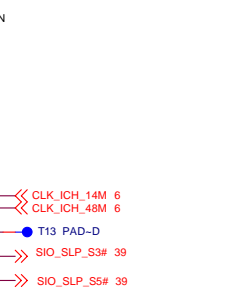
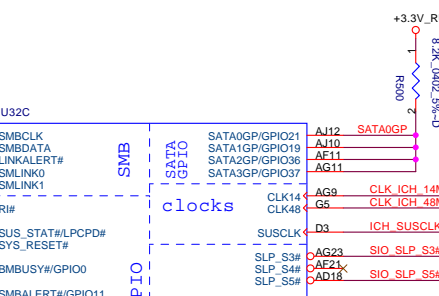
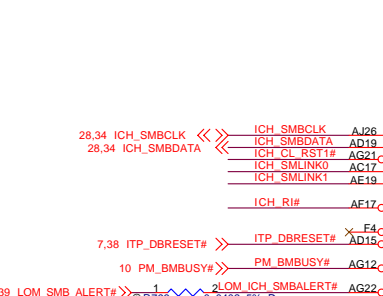
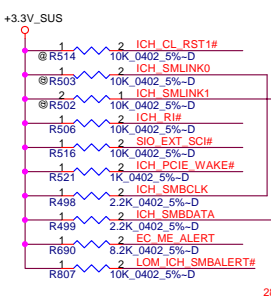
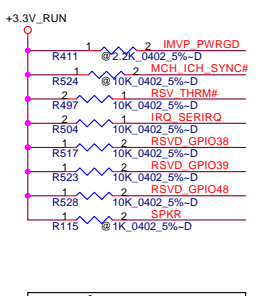


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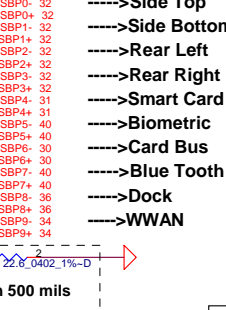
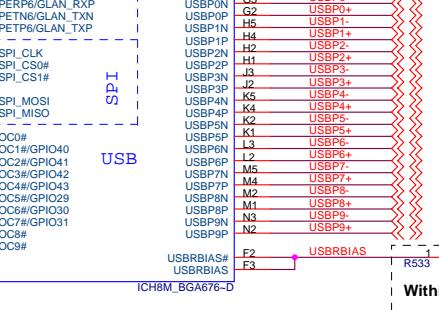
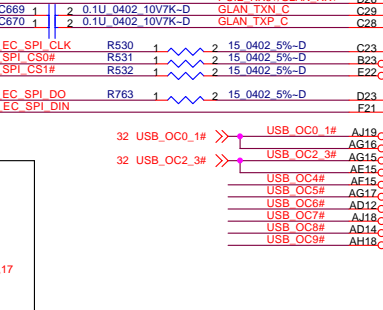
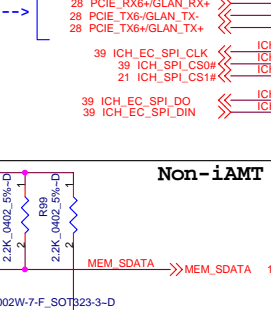
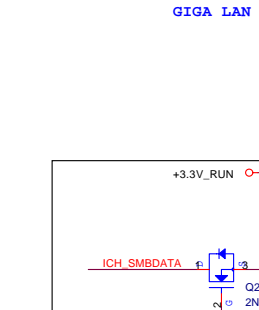
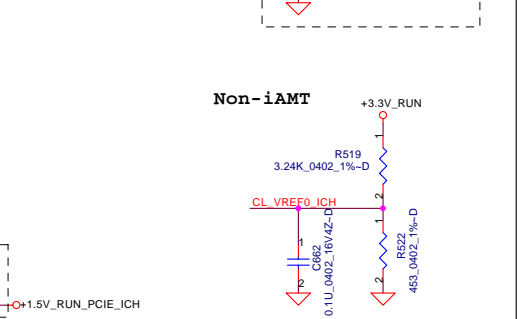
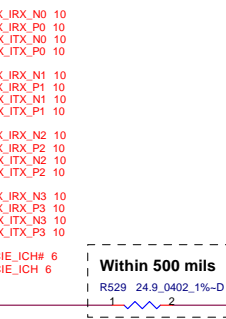
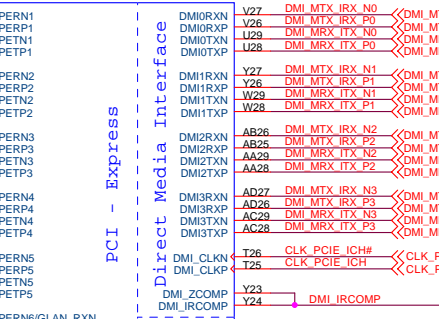
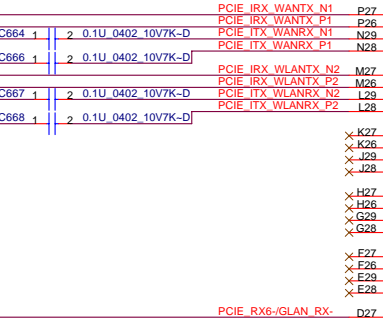
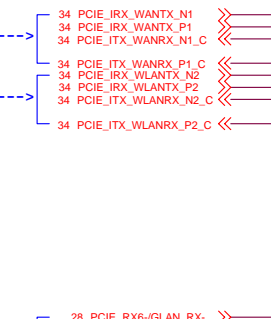
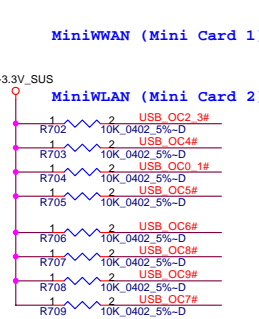
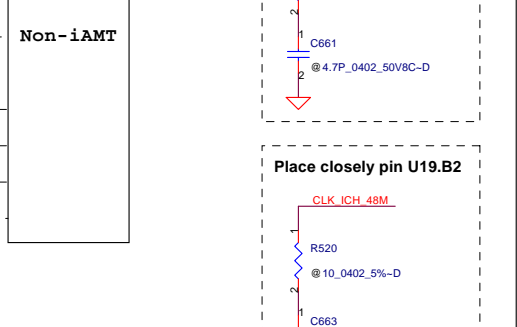
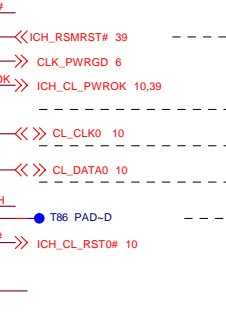
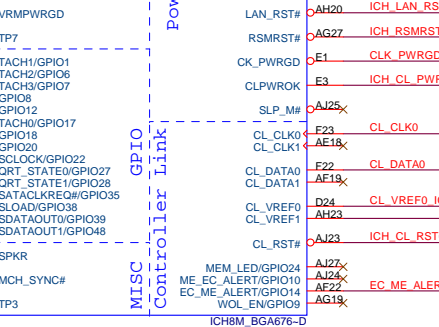
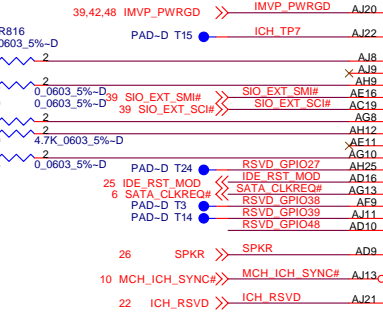
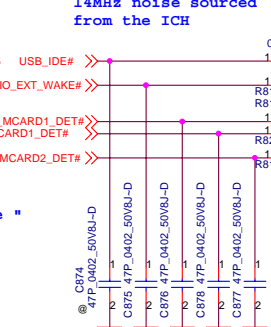
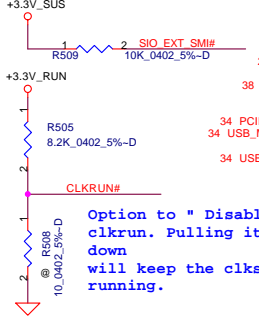


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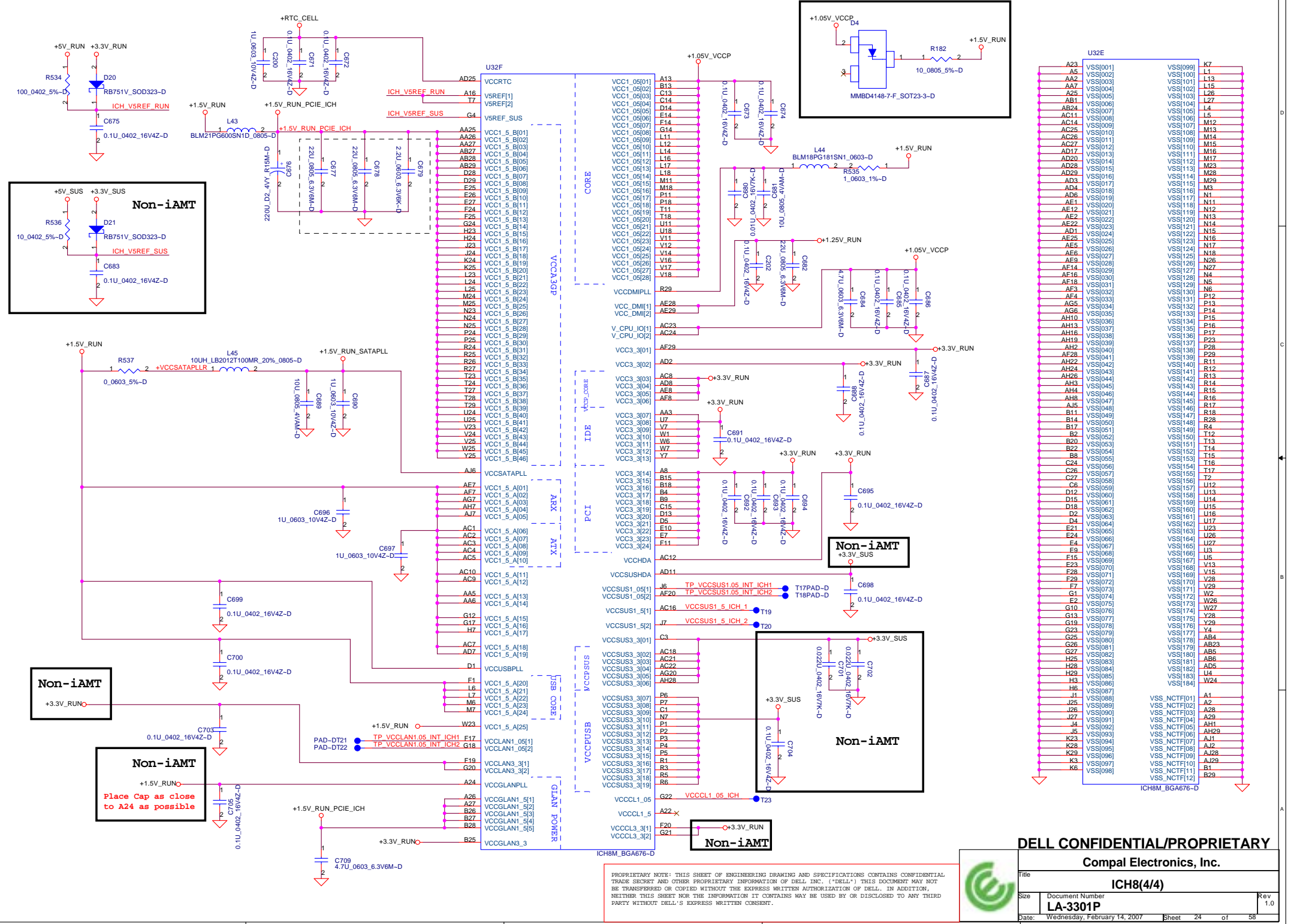
Title <b>ICH8(2/4)</b>		
Size	Document Number <b>LA-3301P</b>	Rev 1.0
Date	Monday, February 26, 2007	Sheet 22 of 58



No Reboot Strap	
SPKR	Low = Default
	High = No Reboot





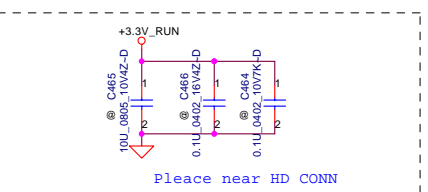
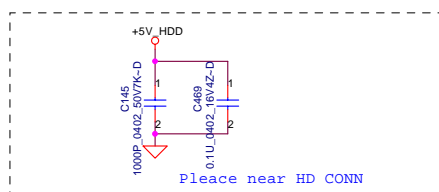
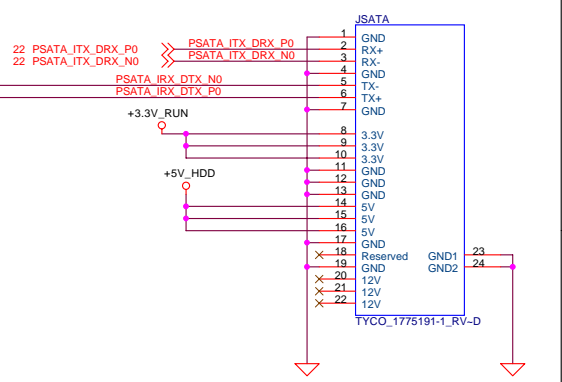
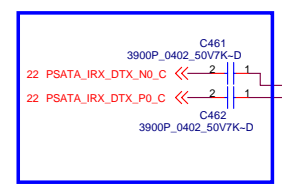
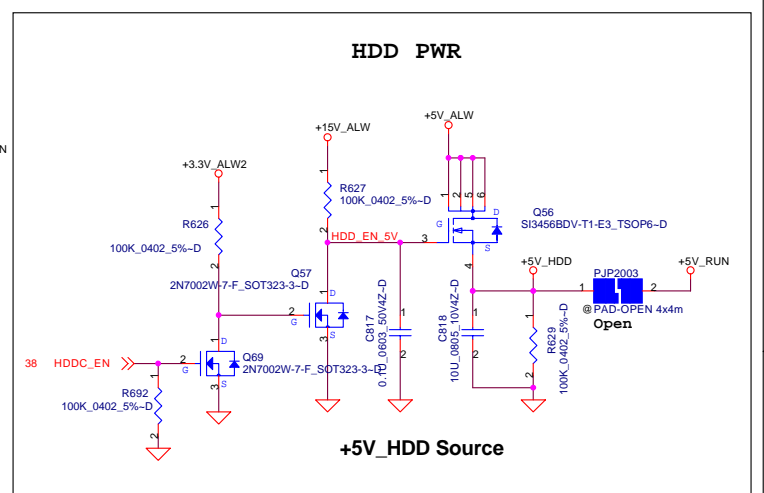
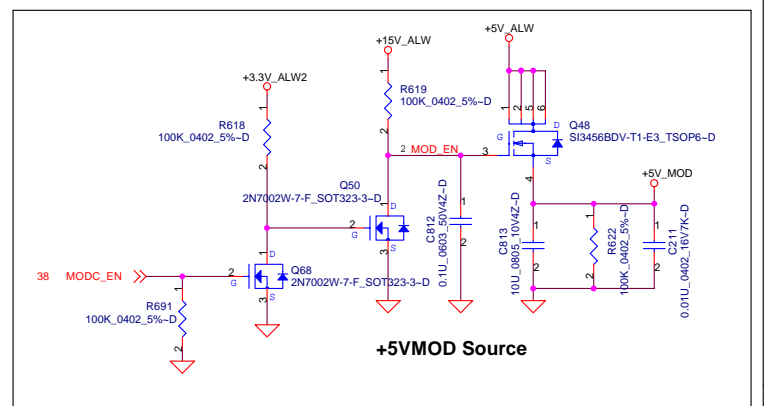
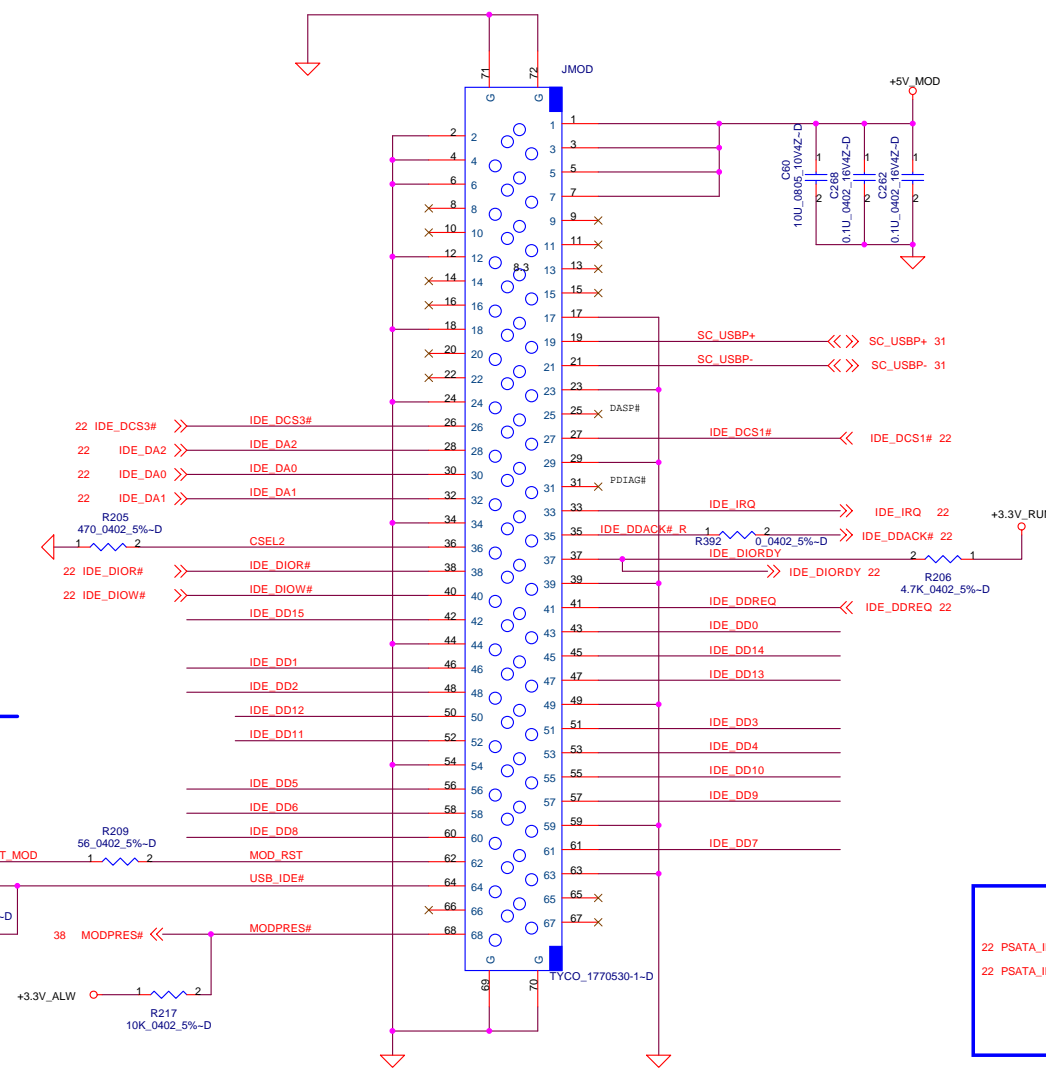
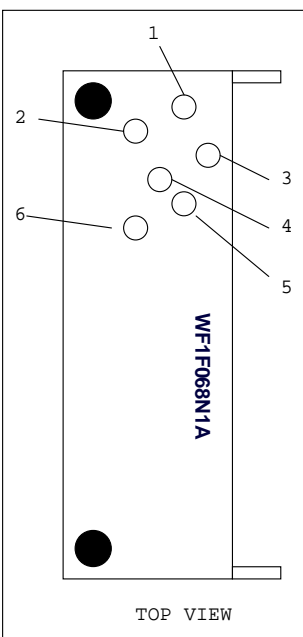


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Title		ICH8(4/4)	
Size	Document Number	LA-3301P	
Date:	Wednesday, February 14, 2007	Sheet	24 of 58
		Rev	1.0

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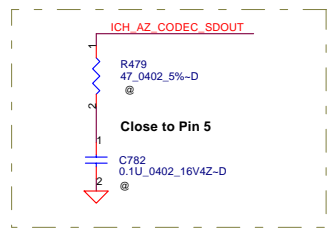
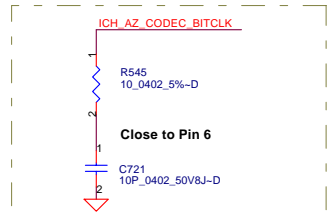
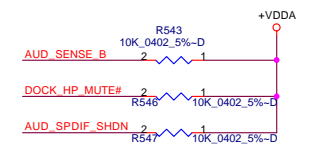
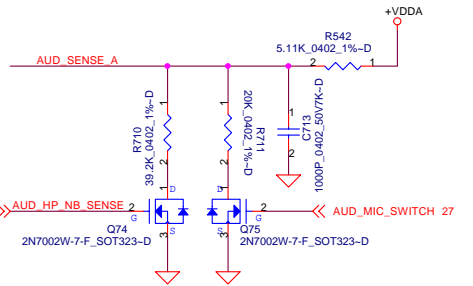
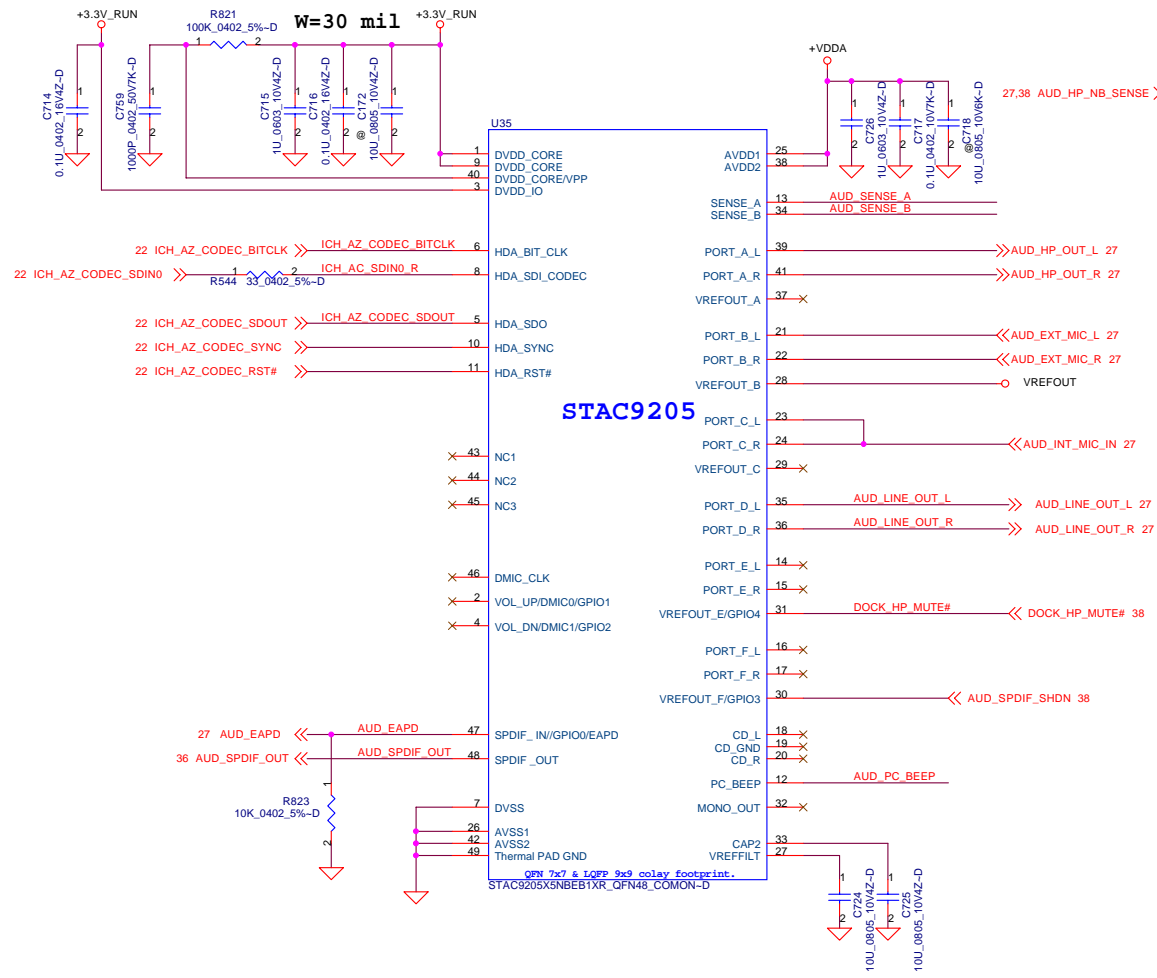
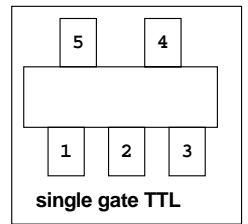
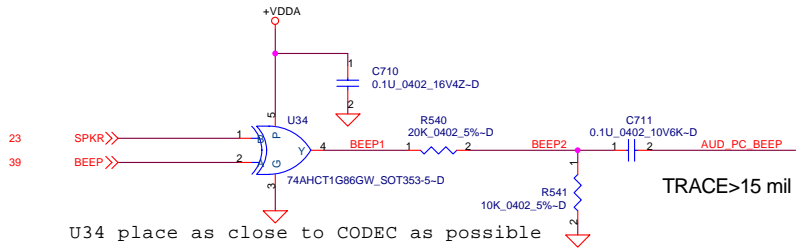
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**DVD MODULE**

LA-3301P

Monday, February 26, 2007

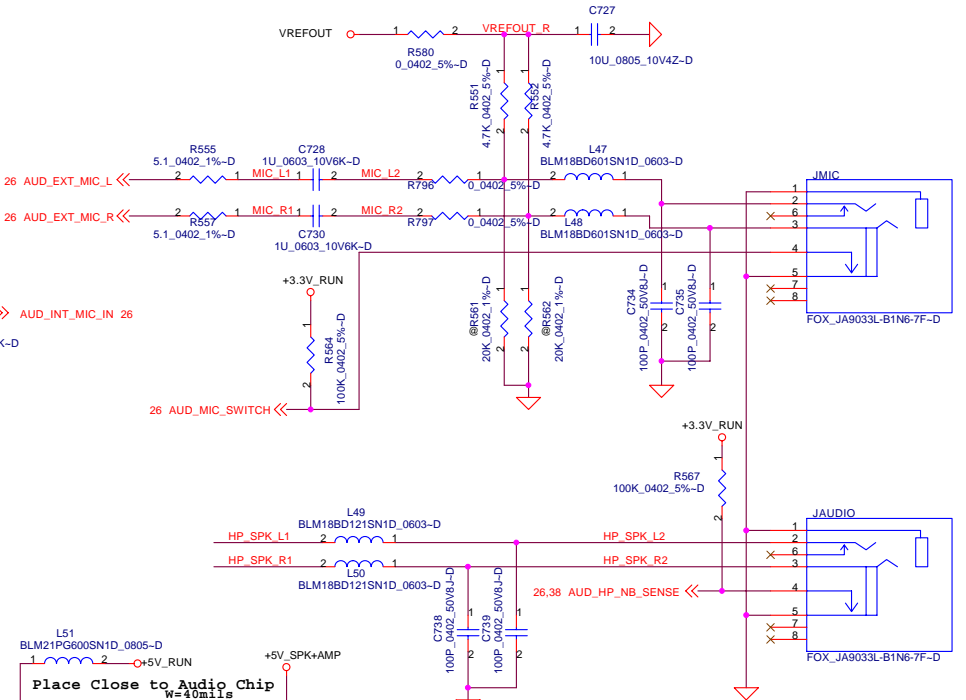
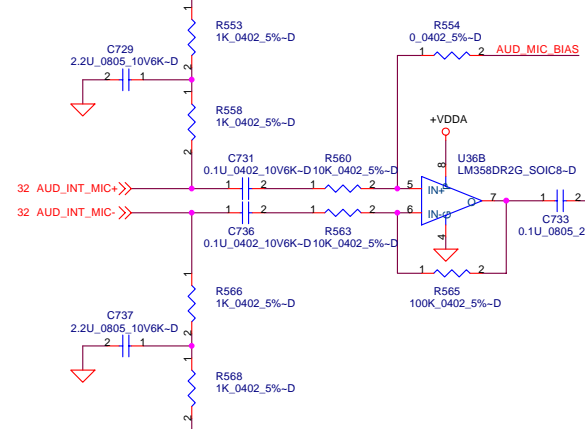
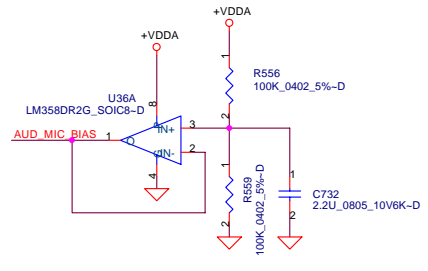


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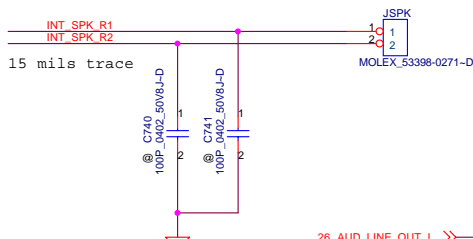


Compal Electronics, Inc.		
Title		
Azalia (HD) Codec		
Size	Document Number	Rev
	LA-3301P	1.0
Date:	Monday, February 26, 2007	Sheet 26 of 58

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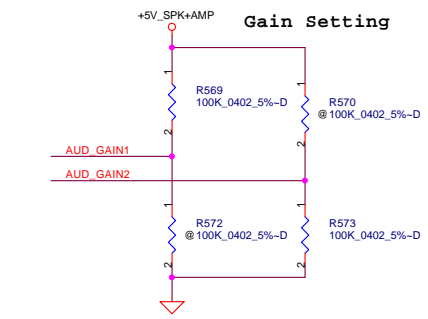
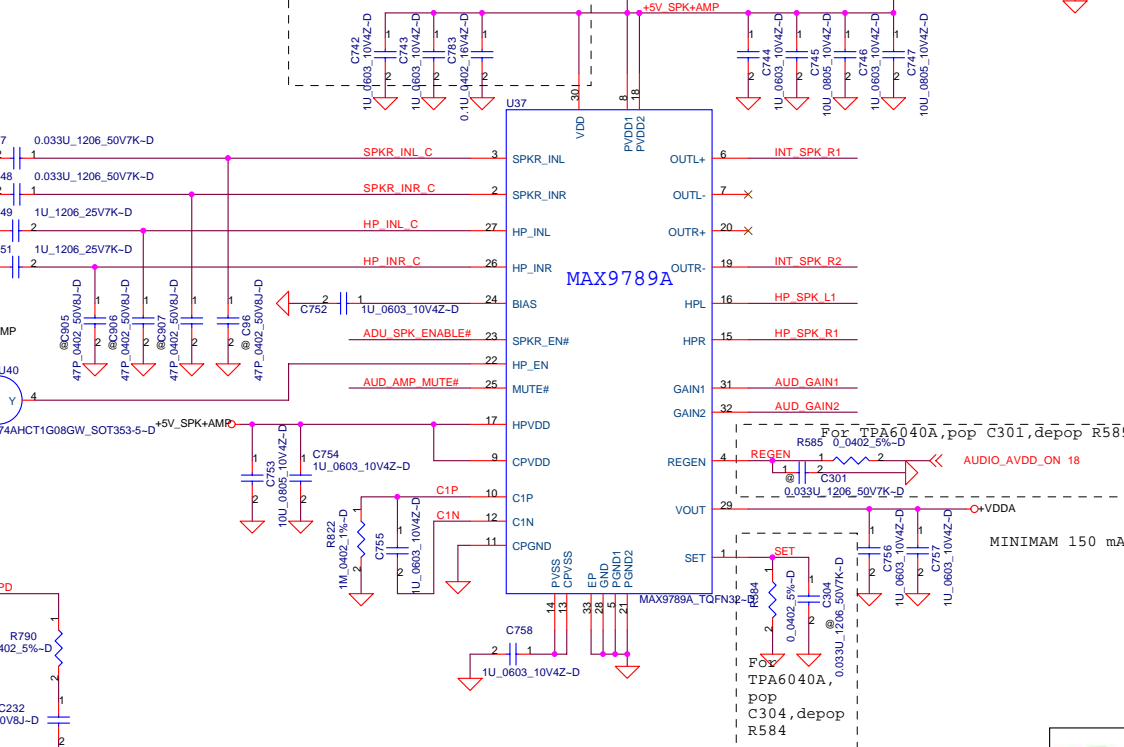
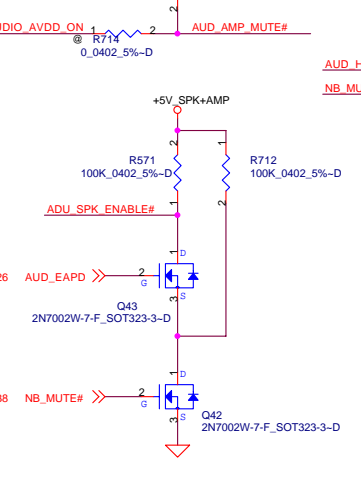


**Speaker Connector**



Place Close to Audio Chip  
W=40mils

For TPA6040A, pop R714, depop R713



GAIN1	GAIN2	AV (inv)	INPUT IMPEDANCE
0	0	6dB	82K ohm
0	1	10dB	66K ohm
1	0	15.6dB	45K ohm
1	1	21.6dB	26K ohm

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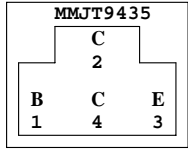
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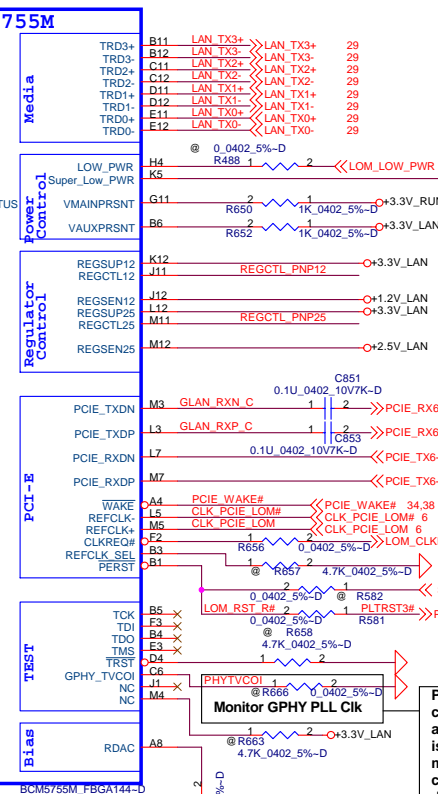
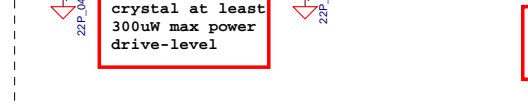
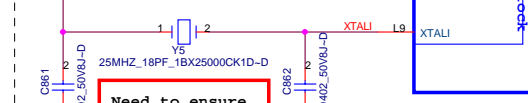
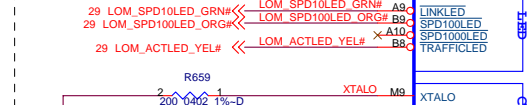
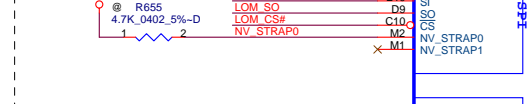
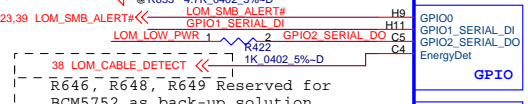
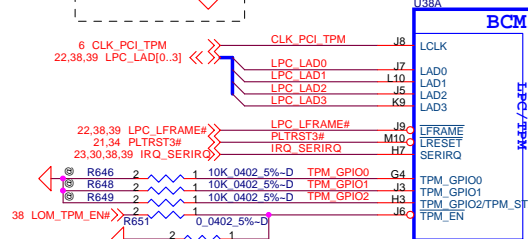
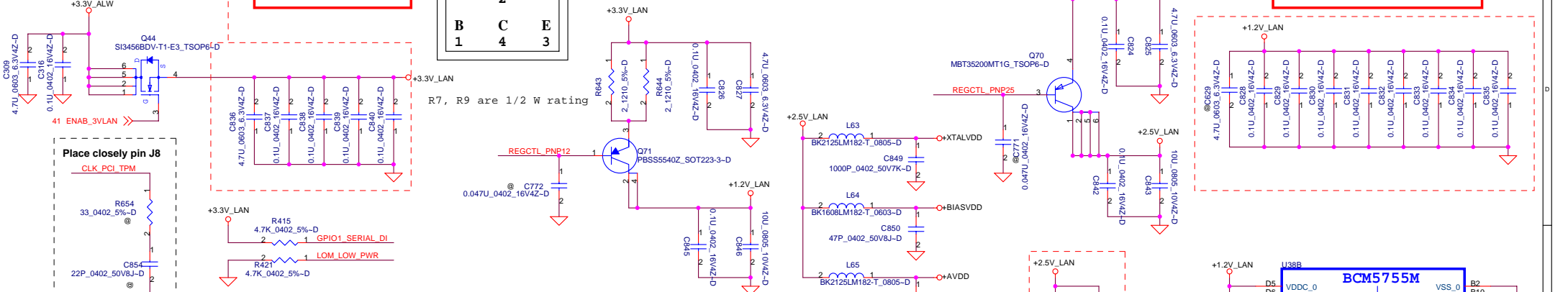
**AMP and PHONE JACK**

LA-3301P  
Date: Wednesday, March 07, 2007 Sheet 27 of 58

Layout Notice : Place as close chip as possible.



Layout Notice : 1.2V filter. Place as close chip as possible.

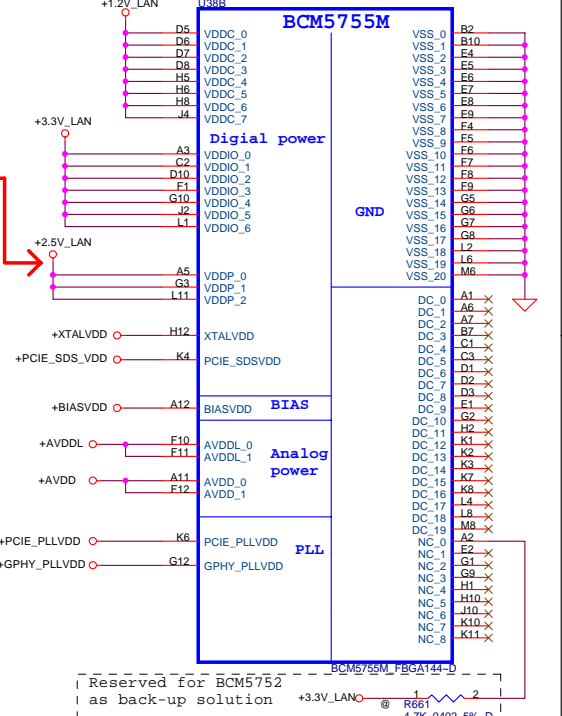


Logic High Voltage must be 0.7V to 2.75V

Place R666 as close to the ASIC as possible. Pad is needed to measure 125MHz clock for debugging

LOM\_CABLE\_DETECT goes to an input on a system microcontroller that can poll this signal periodically and can de-assert the LOM\_LOW\_PWR when LOM\_CABLE\_DETECT signal is high. Connect to an EC GPIOC defined by the GPIO mapping.

Layout Notice : No high speed signal should be routed near RDAC or on adjacent layer to RDAC



Reserved for BCM5752 as back-up solution

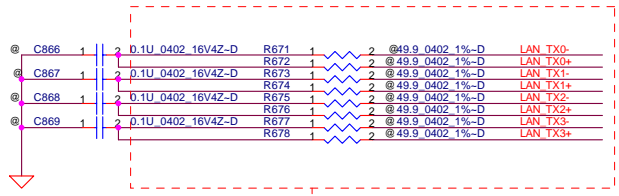
	NV_STRAP1	NV_STRAP0	SO	SI	CS#	SCLK
Auto-Sense Mode (Default)	0	0	0	0	0	0
Atmel AT45BCM021B	0	0	1	0	1	1
ST M45PE20	0	1	1	0	0	1



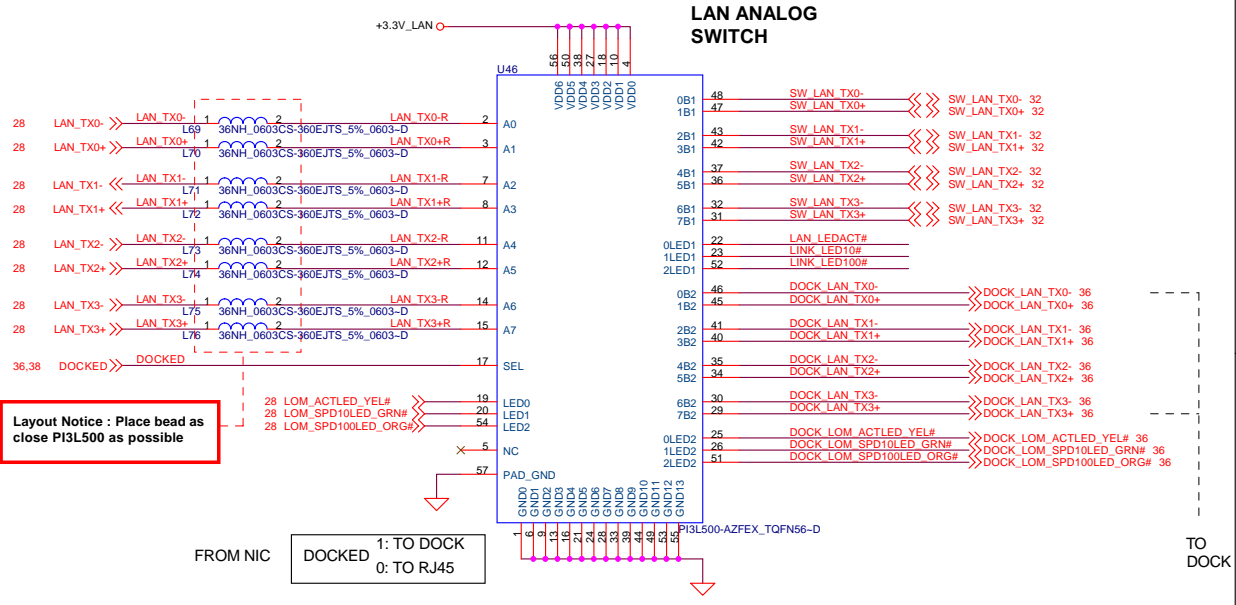
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Title		BCM5755M	
Size	Document Number	Rev	1.0
Date:	Monday, February 26, 2007	Sheet	28 of 58

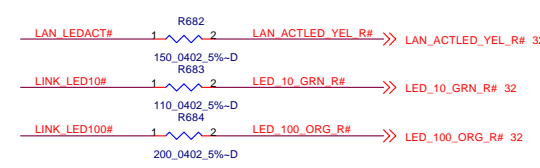
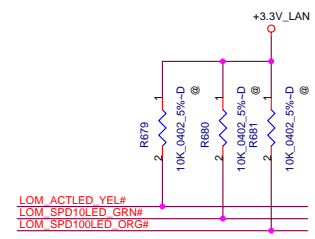
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**Layout Notice : Place termination as close as ASIC as possible**  
The resistors need at least 1/16W



**Layout Notice : Place bead as close PI3L500 as possible**



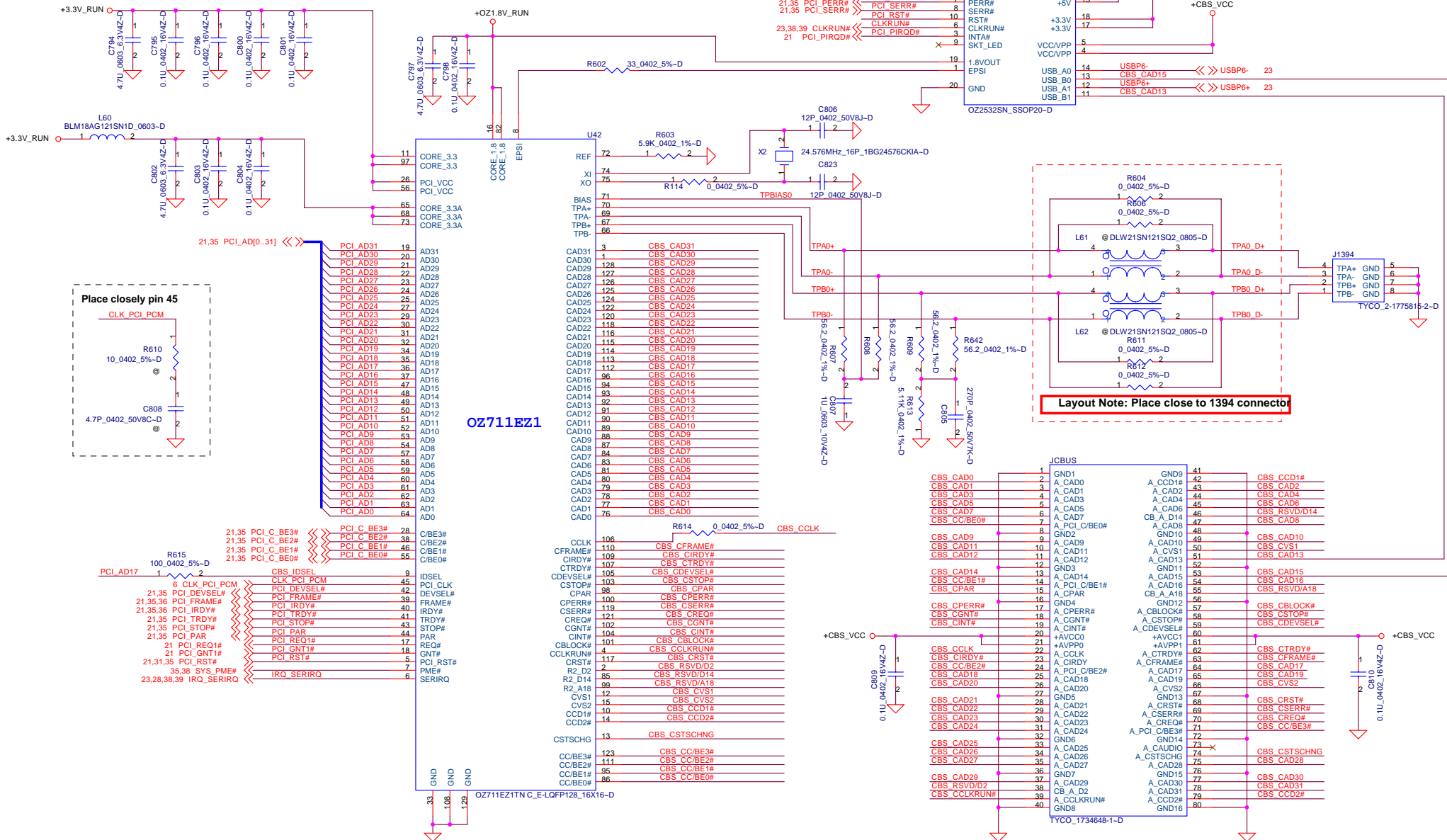
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Title			Rev 1.0
LAN TRANSFORMER			
Size	Document Number	Date: Monday, February 26, 2007	
LA-3301P			Sheet 29 of 58



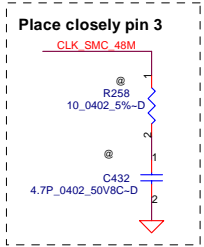
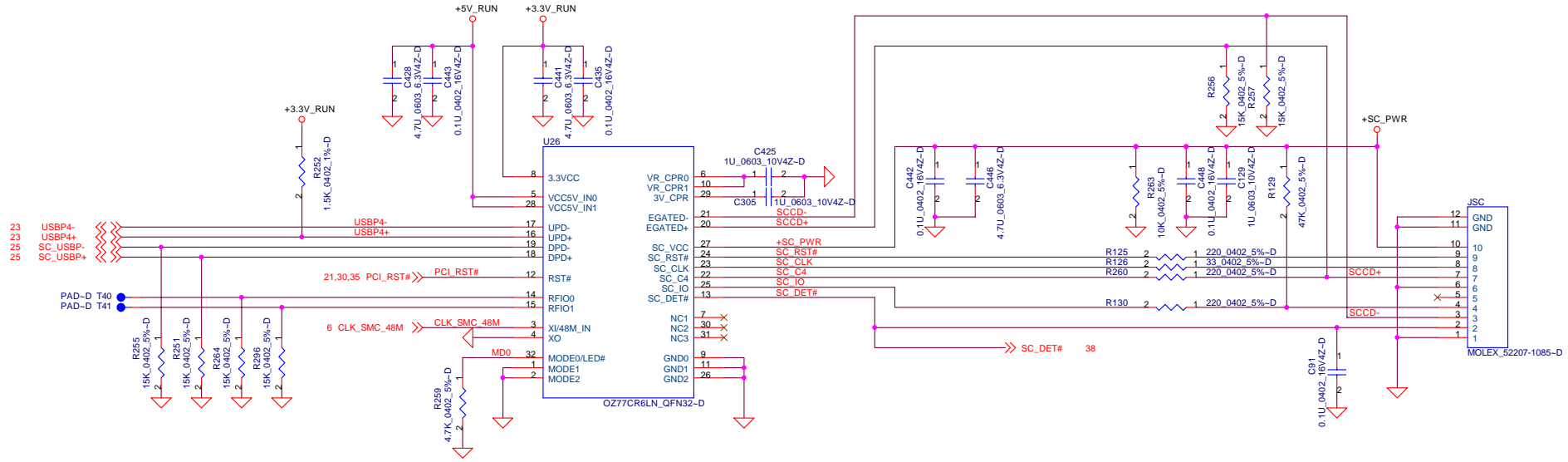
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Cardbus and 1394 OZ711EZ1 Controller  
 LA-3301P  
 Monday, February 26, 2007

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USB SMARTCARD READER.  
 TYPE A (5V), B (3V), AB (5V/3V)  
 & USB SMARTCARDS ARE SUPPORTED.



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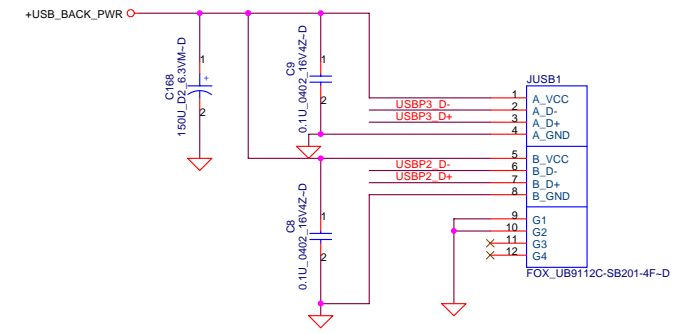
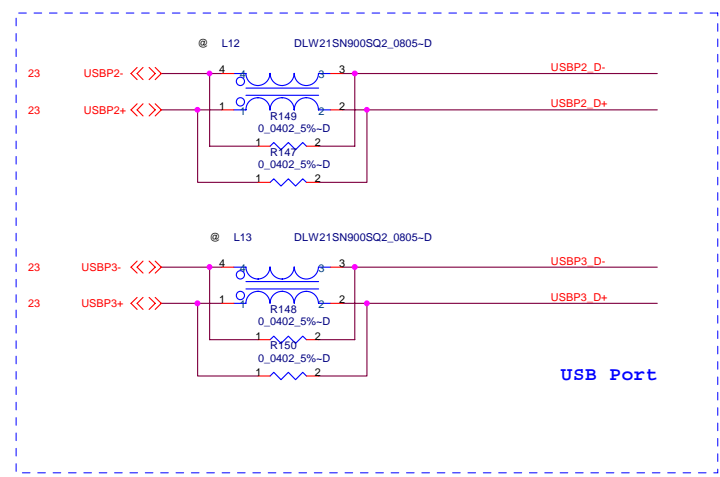
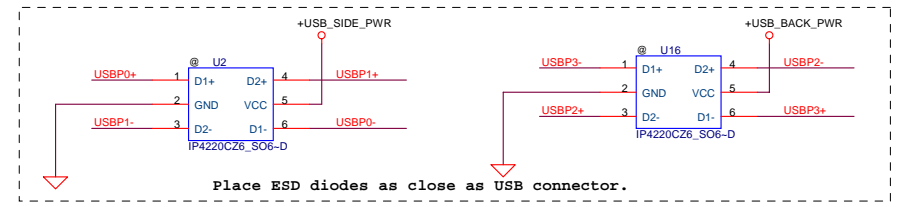
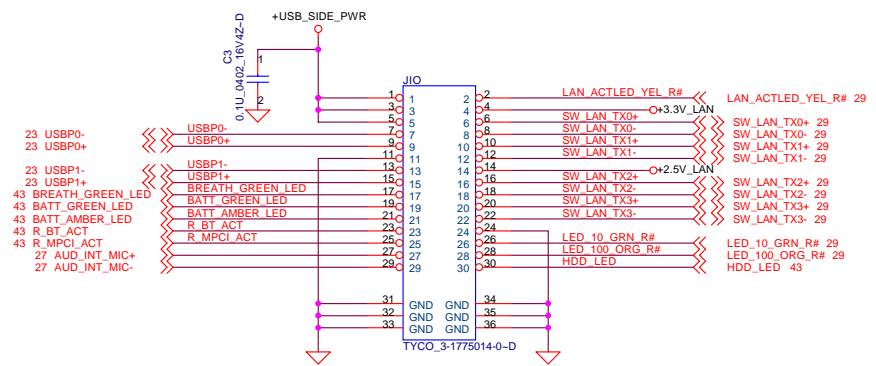
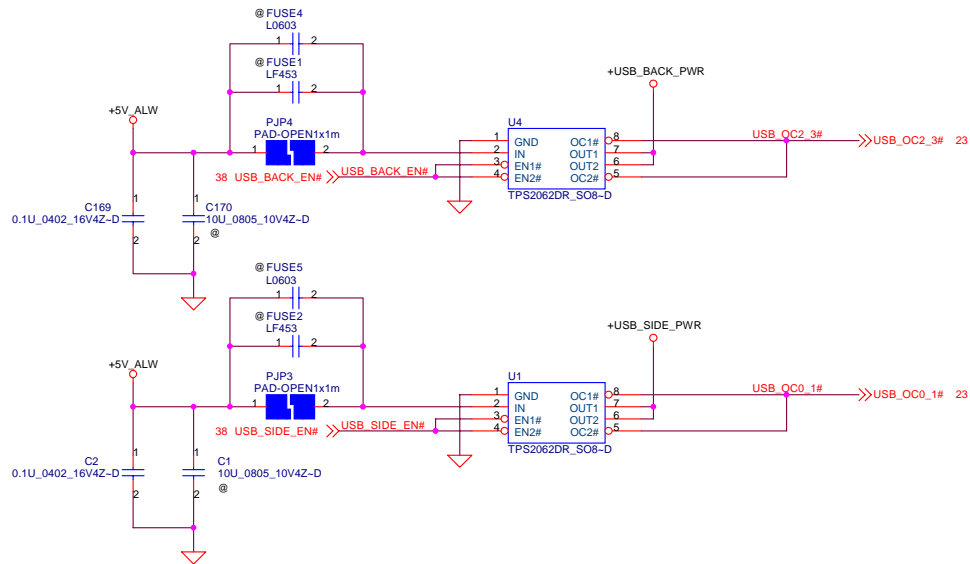


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Title			Smart Card O277CR6		
Size	Document Number		Rev		1.0
Date: Monday, February 26, 2007			Sheet 31		of 58





Rear USB Ports

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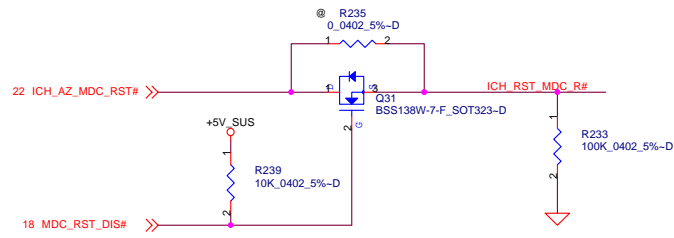
Compal Electronics, Inc.

Title			Rev 1.0
Size			
Document Number			Sheet 32 of 58
LA-3301P			
Date:	Monday, February 26, 2007	Sheet	32 of 58

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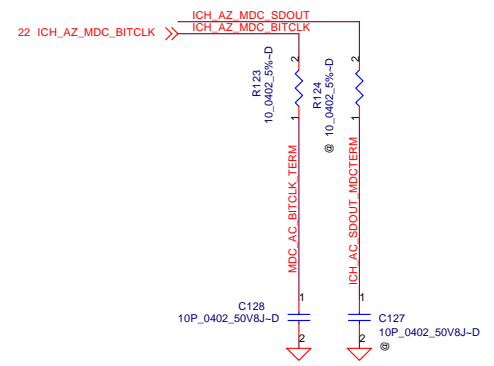
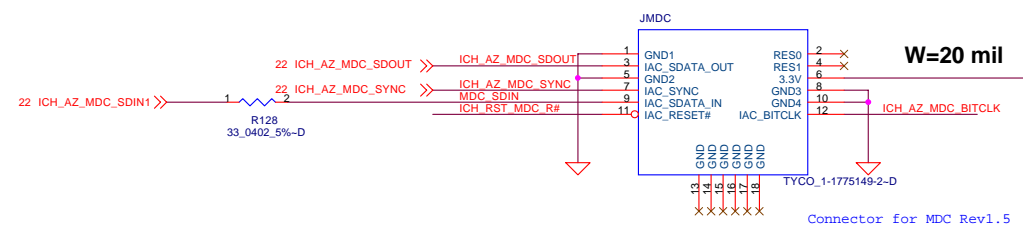






New MDC connector.

1	GND	RES	2
3	IAC_SDATA0	RES	4
5	GND	3.3V	6
7	IAC_SYNC	GND	8
9	IAC_SDATAIN	GND	10
11	IAC_RESET#	IAC_BITCLK	12

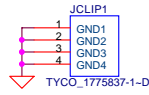
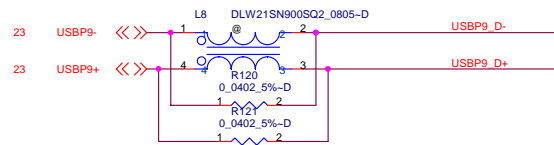


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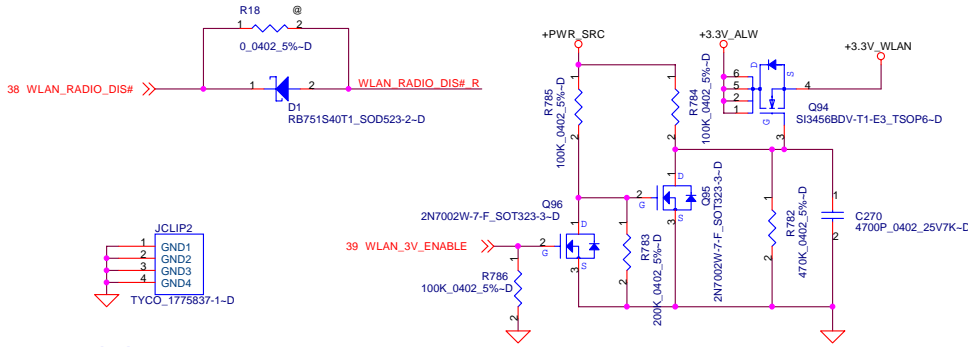
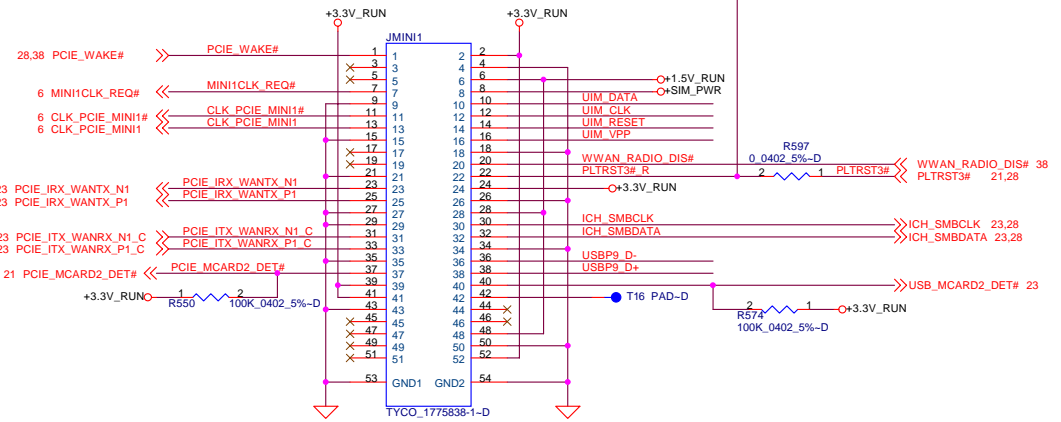


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Title		
BT PORT and MDC		
Size	Document Number	Rev
	LA-3301P	1.0
Date:	Monday, February 26, 2007	Sheet 33 of 58

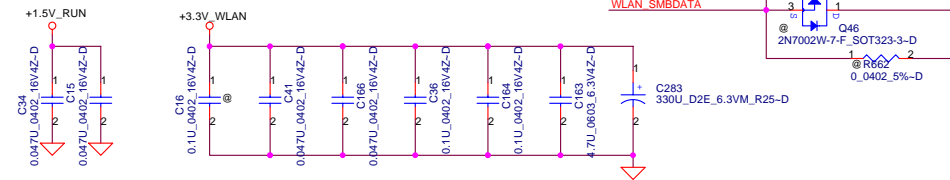
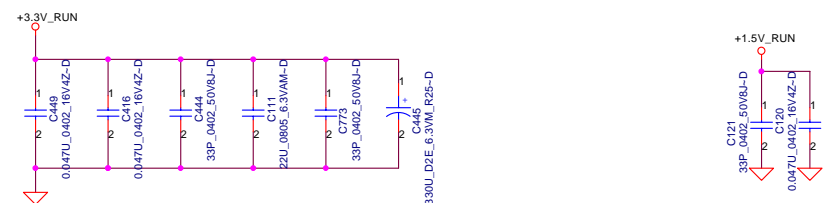
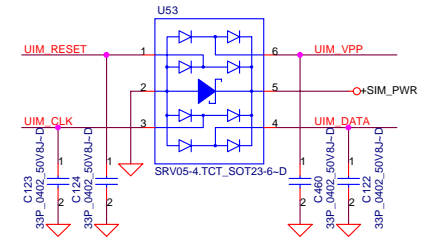
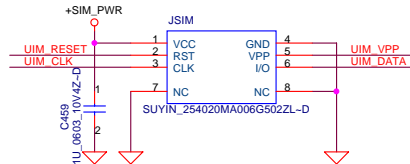
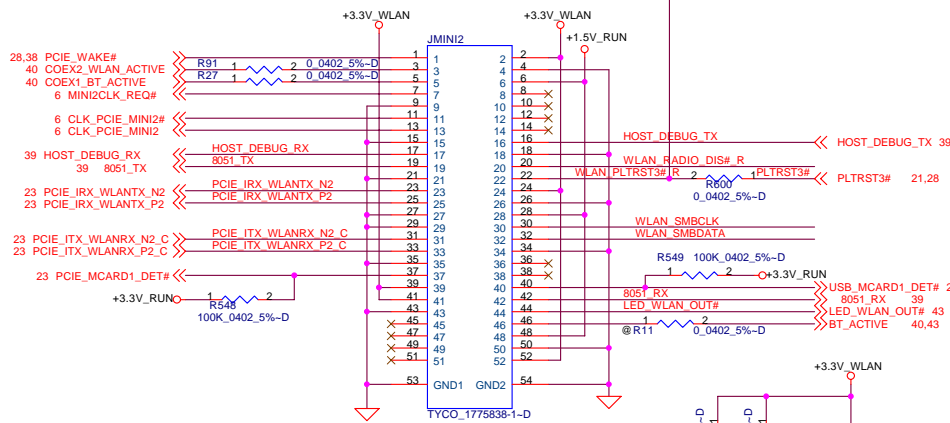


### Mini-Card Latch Mini WWAN



### Mini-Card Latch

### Mini WLAN



PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V	+9%	1000	750	
+3.3Vaux	+9%	330	250	250 (Wake enable) 5 (Not wake enable)
+1.5V	+5%	500	375	NA

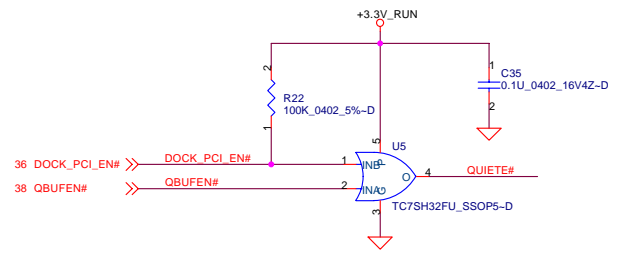
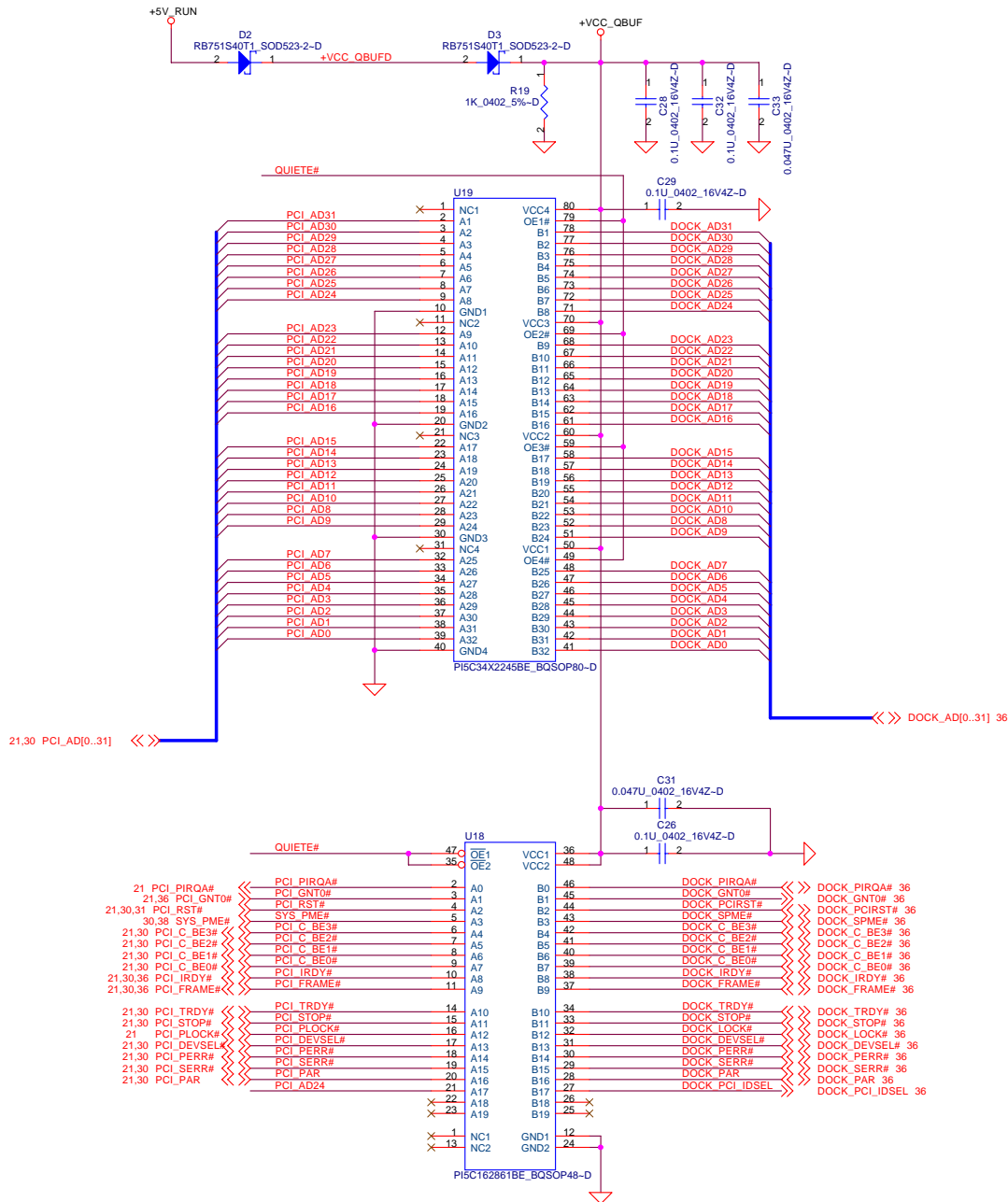
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Size	Document Number	Rev
	LA-3301P	1.0
Date:	Monday, February 26, 2007	Sheet 34 of 58

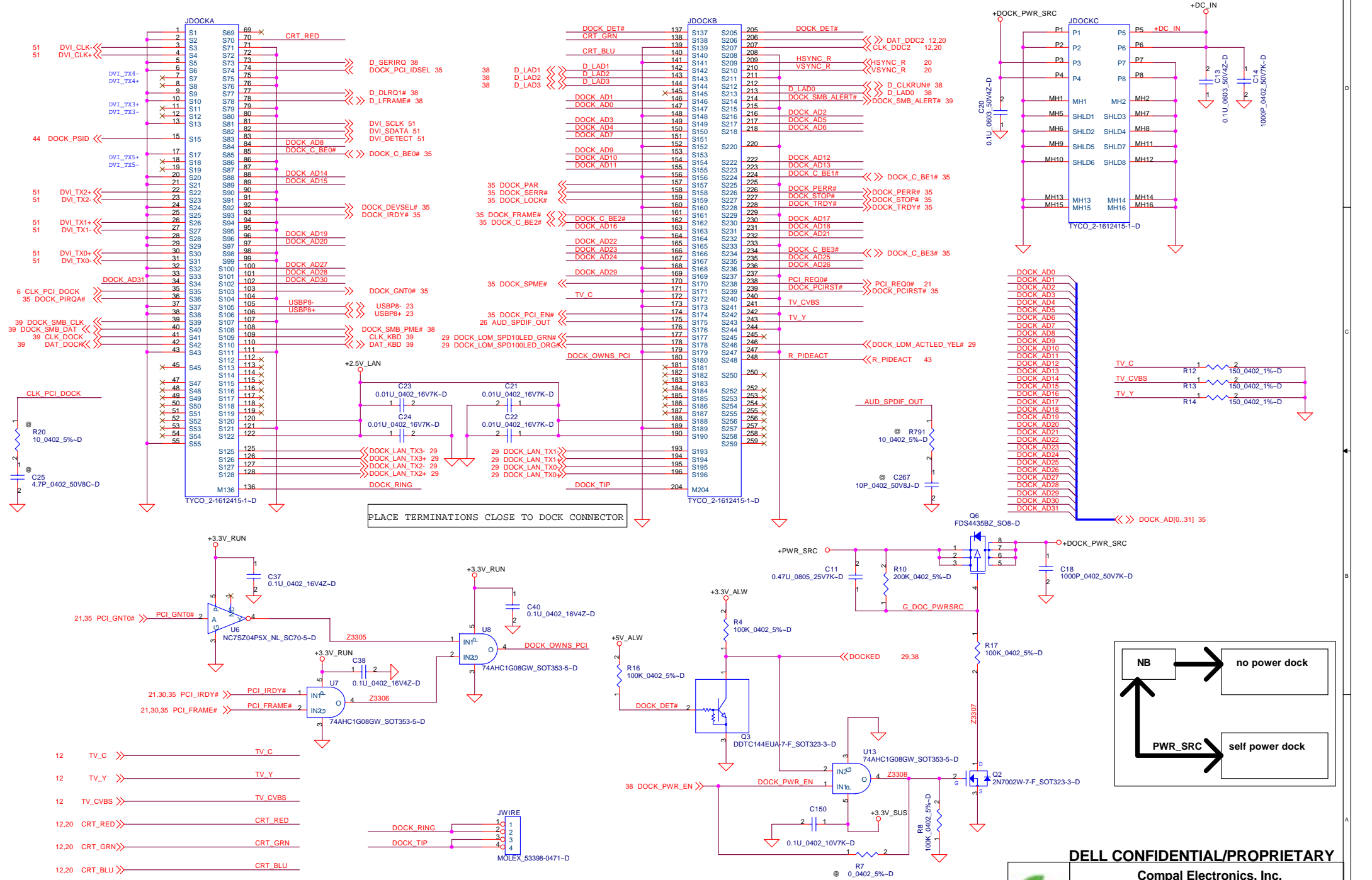


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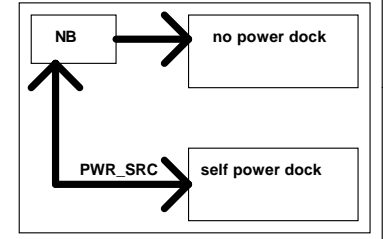
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Date:	Monday, February 26, 2007	Sheet	35	of	58

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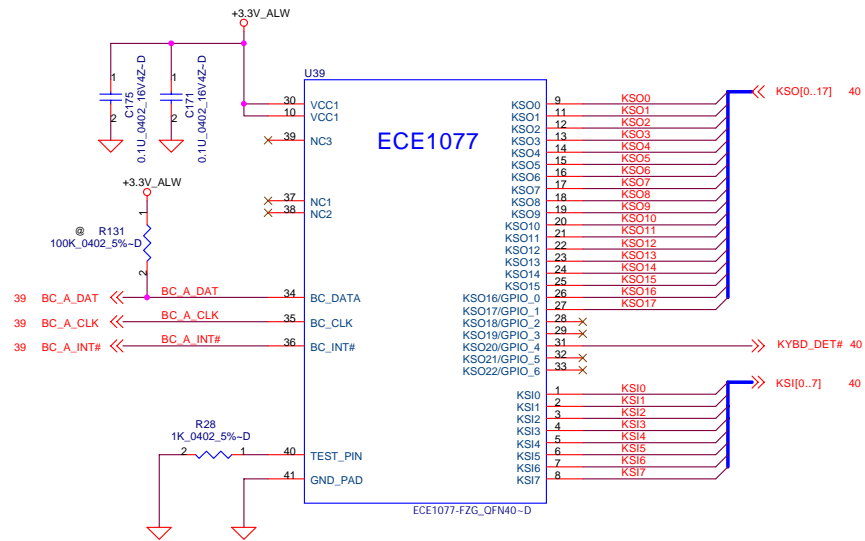
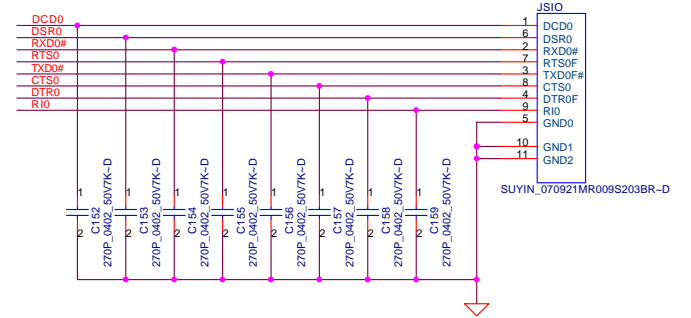
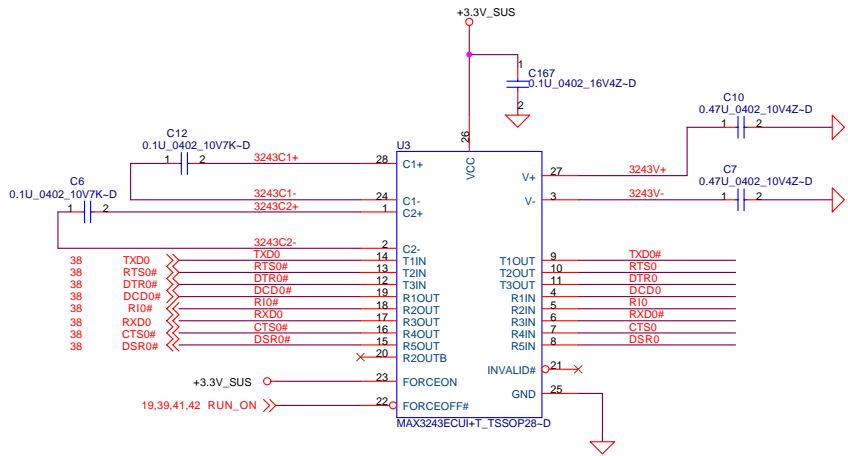
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LA-3301P

Rev 1.0

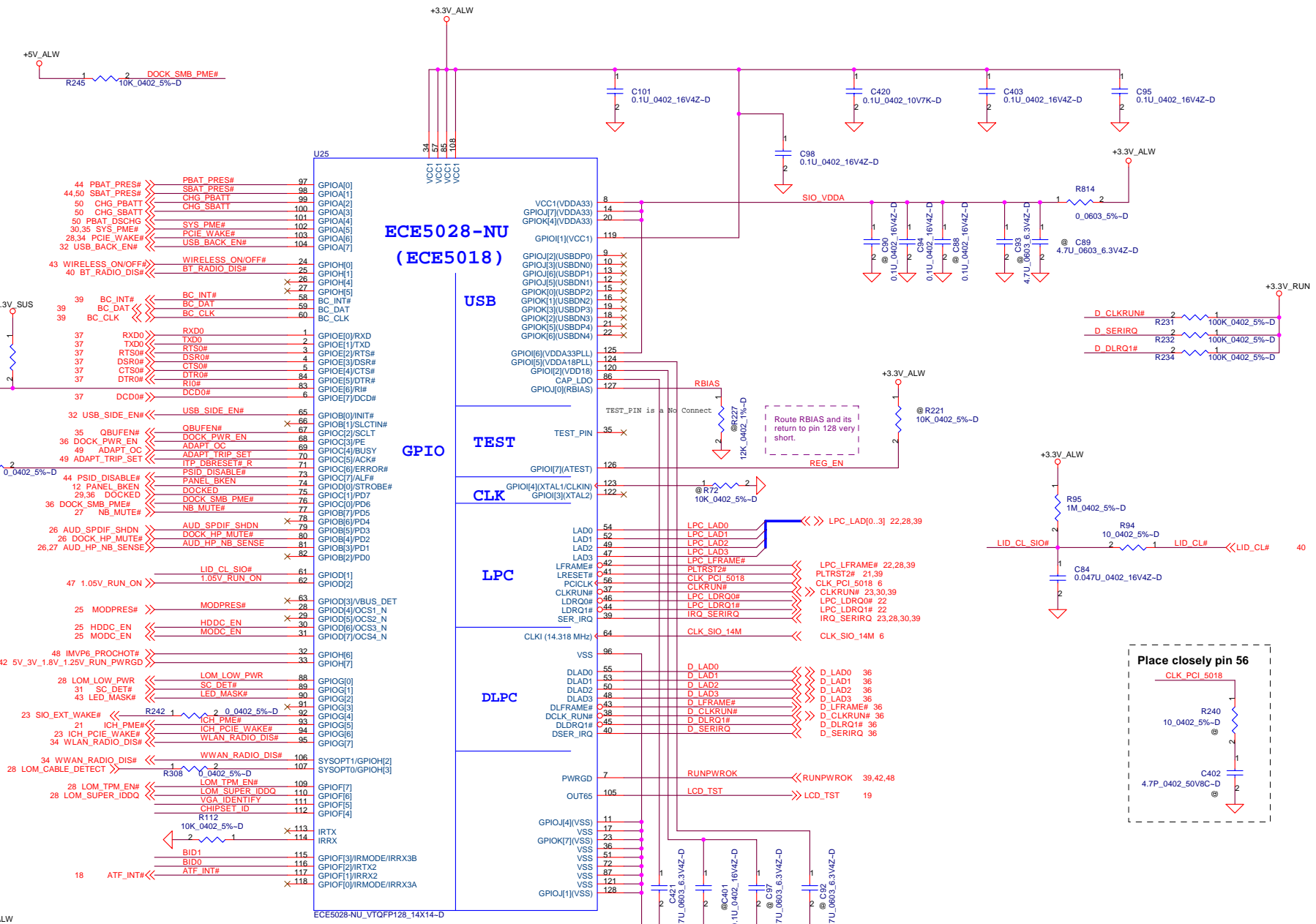
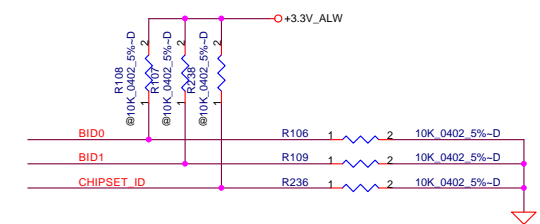
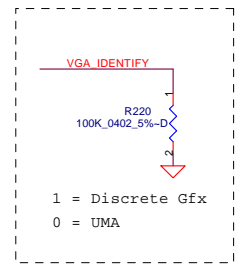
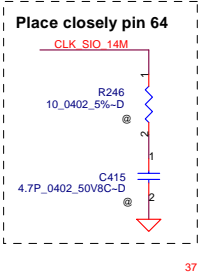
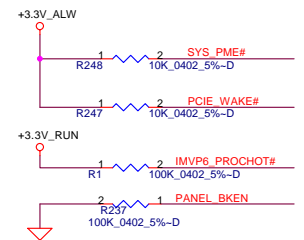
Date: Tuesday, February 27, 2007 Sheet 36 of 58



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<b>Serial &amp; FIR</b>		
<b>LA-3301P</b>		
Date:	Monday, February 26, 2007	Sheet 37 of 58

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44	PBAT_PRES#	PBAT_PRES#	97	GPIOA[0]	
44,50	SBAT_PRES#	SBAT_PRES#	98	GPIOA[1]	
50	CHG_PBAT	CHG_PBAT	99	GPIOA[2]	
50	CHG_SBAT	CHG_SBAT	100	GPIOA[3]	
50	PBAT_DSCHG	SYS_PME#	101	GPIOA[4]	
30,35	SYS_PME#	PCIE_WAKE#	102	GPIOA[5]	
38,34	PCIE_WAKE#	USB_BACK_EN#	103	GPIOA[6]	
32	USB_BACK_EN#	BT_RADIO_DIS#	104	GPIOA[7]	
43	WIRELESS_ON/OFF#	BT_RADIO_DIS#	24	GPIOH[0]	
40	BT_RADIO_DIS#	BC_INT#	25	GPIOH[1]	
		BC_DAT	26	GPIOH[2]	
		BC_CLK	27	GPIOH[3]	
39	BC_INT#	RXD0	28	GPIOH[4]	
39	BC_DAT	TXD0	29	GPIOH[5]	
39	BC_CLK	RTS0#	30	GPIOH[6]	
		DSR0#	31	GPIOH[7]	
37	RXD0	CTS0#	32	GPIOI[0]	
37	TXD0	DTR0#	33	GPIOI[1]	
37	RTS0#	DCD0#	34	GPIOI[2]	
37	DSR0#	USB_SIDE_EN#	35	GPIOI[3]	
37	CTS0#	OBUFEN#	36	GPIOI[4]	
37	DTR0#	DOCK_PWR_EN	37	GPIOI[5]	
37	DCD0#	ADAPT_OC	38	GPIOI[6]	
		ADAPT_TRIP_SET	39	GPIOI[7]	
37	DCD0#	ITP_DBRESET#	40	GPIOJ[0]	
		PSID_DISABLE#	41	GPIOJ[1]	
32	USB_SIDE_EN#	PANEL_BKEN	42	GPIOJ[2]	
		DOCKED	43	GPIOJ[3]	
35	OBUFEN#	DOCK_SMB_PME#	44	GPIOJ[4]	
36	DOCK_PWR_EN	NB_MUTE#	45	GPIOJ[5]	
49	ADAPT_OC	AUD_SPDIF_SHDN	46	GPIOJ[6]	
49	ADAPT_TRIP_SET	DOCK_HP_MUTE#	47	GPIOJ[7]	
		AUD_HP_NB_SENSE	48	GPIOK[0]	
44	PSID_DISABLE#	LID_CL_SIO#	49	GPIOK[1]	
12	PANEL_BKEN	1.05V_RUN_ON	50	GPIOK[2]	
29,36	DOCKED	MODPRES#	51	GPIOK[3]	
36	DOCK_SMB_PME#	HDCC_EN	52	GPIOK[4]	
27	NB_MUTE#	MODC_EN	53	GPIOK[5]	
26	AUD_SPDIF_SHDN	IMVP6_PROCHOT#	54	GPIOK[6]	
26	DOCK_HP_MUTE#	5V_3V_1.8V_1.25V_RUN_PWRGD	55	GPIOK[7]	
26,27	AUD_HP_NB_SENSE	LOM_LOW_PWR	56	GPIOL[0]	
		SC_DET#	57	GPIOL[1]	
		LED_MASK#	58	GPIOL[2]	
47	1.05V_RUN_ON	SIO_EXT_WAKE#	59	GPIOL[3]	
		ICH_PME#	60	GPIOL[4]	
25	MODPRES#	ICH_PCIE_WAKE#	61	GPIOL[5]	
25	HDCC_EN	WLAN_RADIO_DIS#	62	GPIOL[6]	
25	MODC_EN	WWAN_RADIO_DIS#	63	GPIOL[7]	
		LOM_CABLE_DETECT	64	GPIOM[0]	
48	IMVP6_PROCHOT#	LOM_TPM_EN#	65	GPIOM[1]	
42	5V_3V_1.8V_1.25V_RUN_PWRGD	LOM_SUPER_IDDO	66	GPIOM[2]	
		VGA_IDENTIFY	67	GPIOM[3]	
28	LOM_LOW_PWR	CHIPSET_ID	68	GPIOM[4]	
31	SC_DET#		69	GPIOM[5]	
43	LED_MASK#		70	GPIOM[6]	
23	SIO_EXT_WAKE#		71	GPIOM[7]	
21	ICH_PME#		72	GPION[0]	
23	ICH_PCIE_WAKE#		73	GPION[1]	
34	WLAN_RADIO_DIS#		74	GPION[2]	
34	WWAN_RADIO_DIS#		75	GPION[3]	
28	LOM_CABLE_DETECT		76	GPION[4]	
			77	GPION[5]	
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			79	GPION[7]	
			80	GPIOO[0]	
			81	GPIOO[1]	
			82	GPIOO[2]	
			83	GPIOO[3]	
			84	GPIOO[4]	
			85	GPIOO[5]	
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			87	GPIOO[7]	
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			107	GPIOR[3]	
			108	GPIOR[4]	
			109	GPIOR[5]	
			110	GPIOR[6]	
			111	GPIOR[7]	
			112	GPIOS[0]	
			113	GPIOS[1]	
			114	GPIOS[2]	
			115	GPIOS[3]	
			116	GPIOS[4]	
			117	GPIOS[5]	
			118	GPIOS[6]	
			119	GPIOS[7]	
			120	GPIOT[0]	
			121	GPIOT[1]	
			122	GPIOT[2]	
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			124	GPIOT[4]	
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			128	GPIOU[0]	

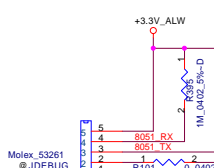
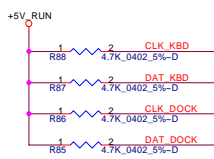
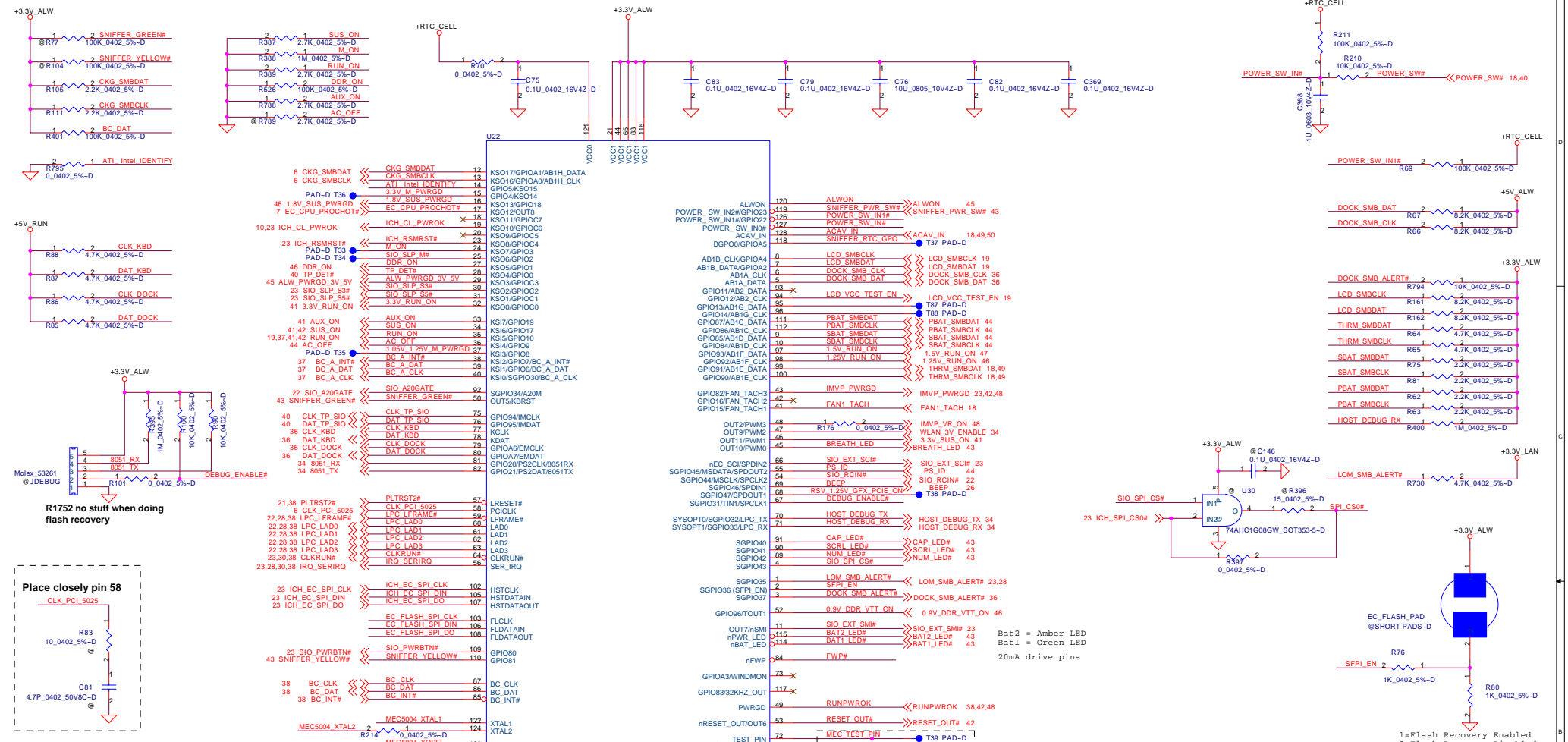
REV	BID1	BID0
X00	0	0
X01	0	1
X02	1	0
X03	1	1
A00	0	0

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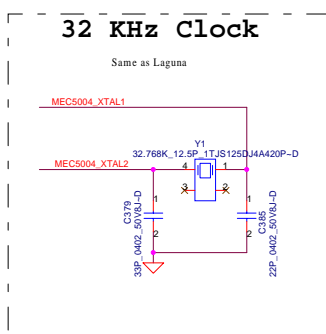
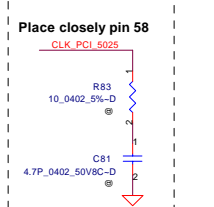


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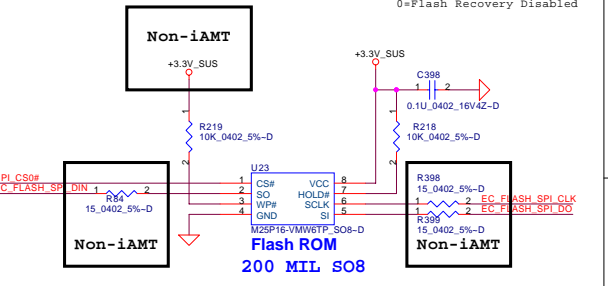
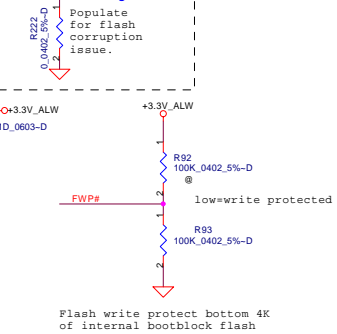
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Title <b>ECE5028</b>			
Size	Document Number	Rev	
	<b>LA-3301P</b>	<b>1.0</b>	
Date:	Monday, February 26, 2007	Sheet	38 of 38



R1752 no stuff when doing flash recovery



Net & Part	AMT Intel	Non-AMT Broacom
3.3V_M_PWRGD	Pin15 of 5025	NC
CH_RSMRST#	Pin23 of 5025	NC
M_ON	Pin24 of 5025	NC
SIO_SLP_M#	Pin25 of 5025	NC
1.05V_1.25V_M_PWRGD	Pin37 of 5025	NC
R238	Pin24 of 5025	NC
LOM_SUPER_IDDQ	NC	Refer to UMA
LOM_LOW_PWR	NC	Refer to UMA
LOM_CABLE_DETECT	NC	Refer to UMA



Layout Note:  
Place R84 within 500 mils from SPI flash.  
Place R398 & R399 within 500 mils of the MEC5025.

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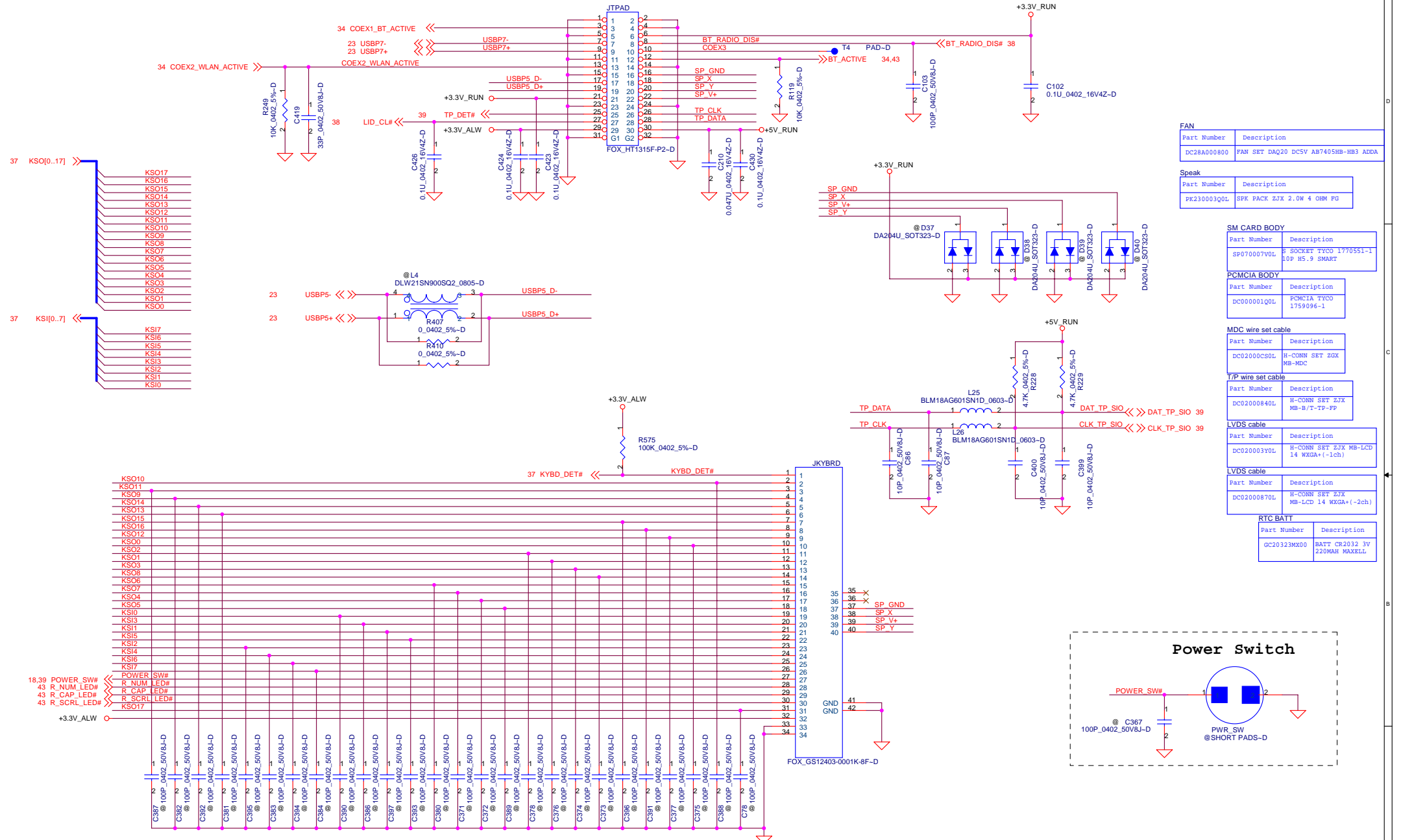
**EMC5025**

**LA-3301P**

Date: Thursday, March 01, 2007 Sheet 39 of 58



# Touch PAD



Part Number	Description
DC28A000800	FAN SET DAQ20 DC5V AB7405HB-HB3 ADDA

Part Number	Description
PK230003Q0L	SPK PACK ZJX 2.0W 4 OHM FG

Part Number	Description
SP070007V0L	S SOCKET TYCO 1779551-1 10P H5.9 SMART

Part Number	Description
DC000001Q0L	PCMCIA TYCO 1759096-1

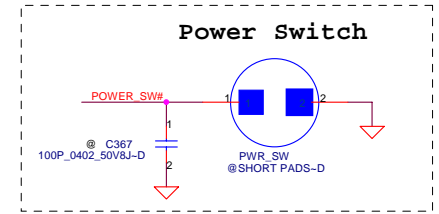
Part Number	Description
DC02000CS0L	H-CONN SBT ZGX MB-MDC

Part Number	Description
DC02000840L	H-CONN SBT ZJX MB-B/T-TP-FP

Part Number	Description
DC020003Y0L	H-CONN SBT ZJX MB-LCD 14 WXGA+(-1ch)

Part Number	Description
DC02000870L	H-CONN SBT ZJX MB-LCD 14 WXGA+(-2ch)

Part Number	Description
GC20323NX00	BATT CR2032 3V 220MAH MAXXLL



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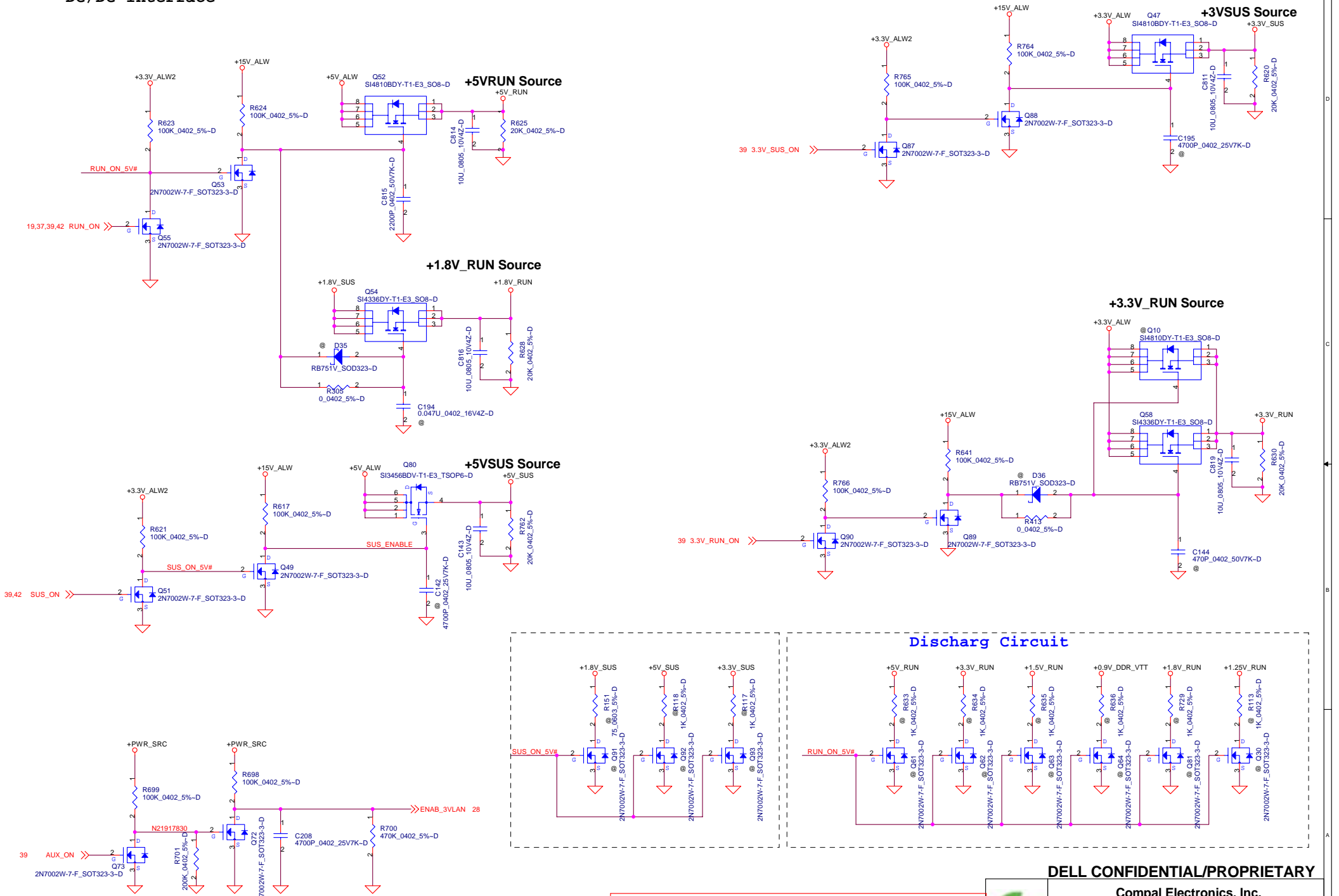


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Date:	Monday, February 26, 2007	Sheet	40	of	58

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# DC/DC Interface



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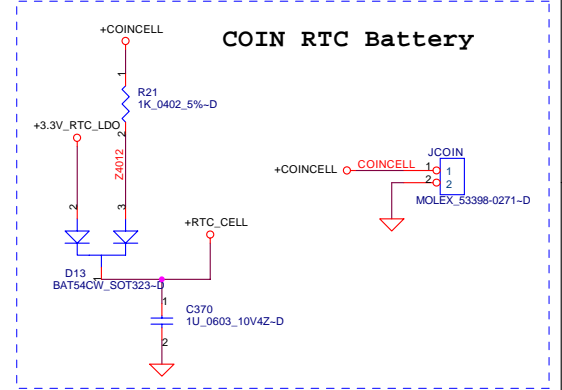
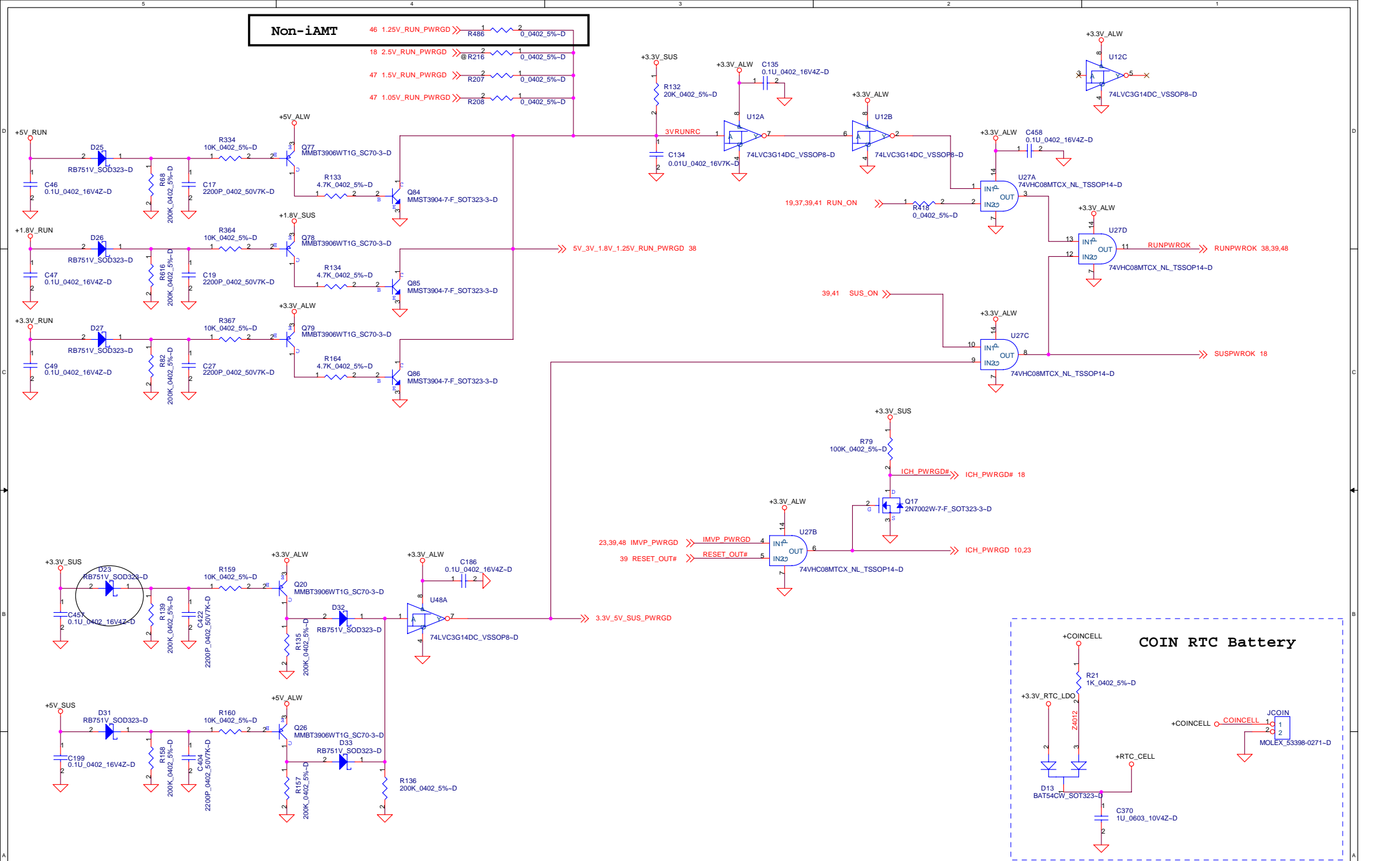
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**POWER CONTROL**

LA-3301P

Monday, February 26, 2007 Sheet 41 of 58

**Non-iAMT**



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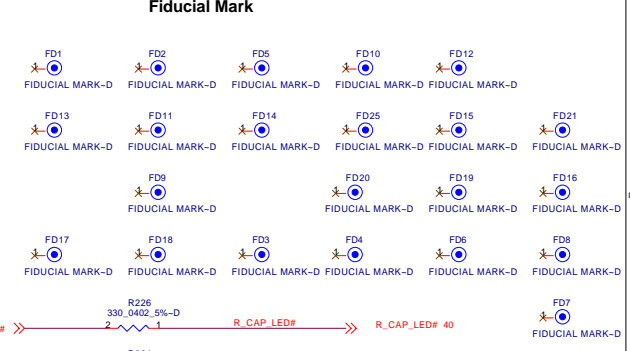
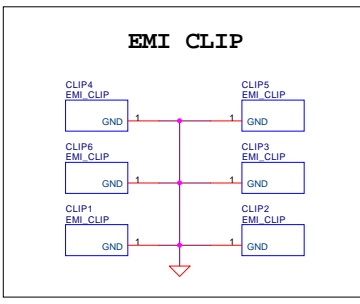
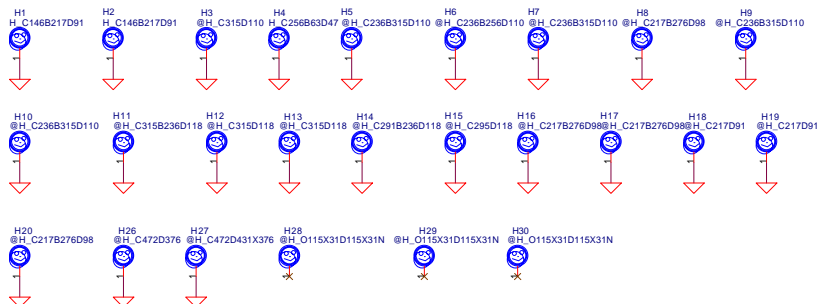
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**Compal Electronics, Inc.**

**Power Good**

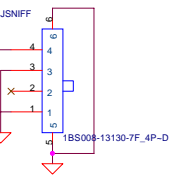
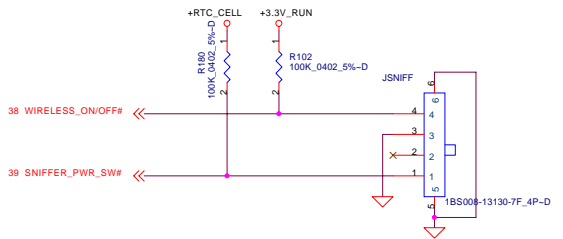
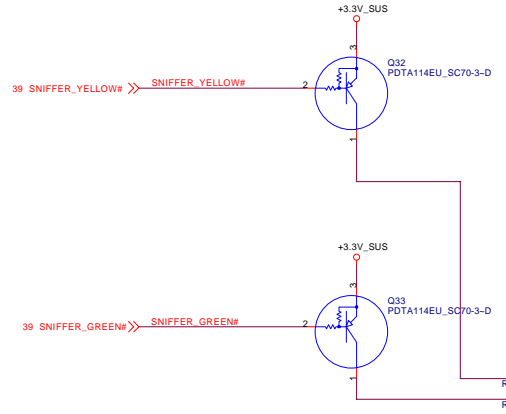
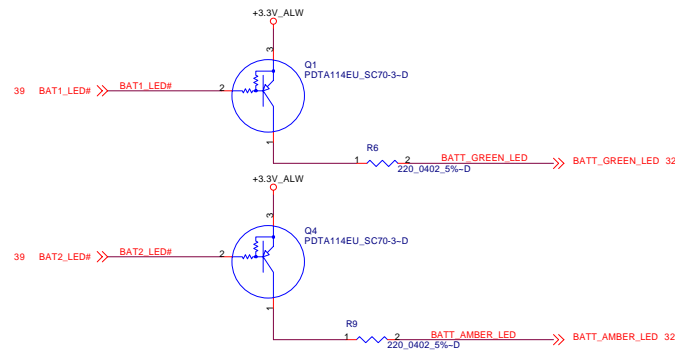
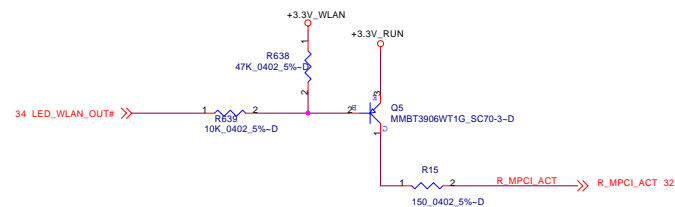
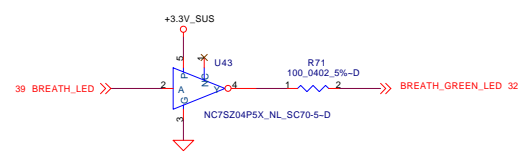
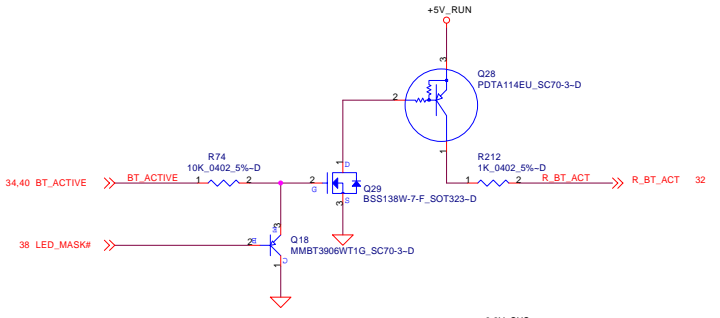
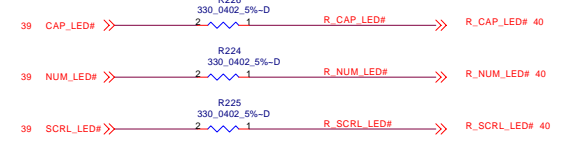
LA-3301P

Monday, February 26, 2007 Sheet 42 of 58



This circuit is only needed if the platform has the SNIFFER.

22 SATA\_ACT#\_R  
38 LED\_MASK#  
HDD\_LED 32  
R\_PIDEACT 36



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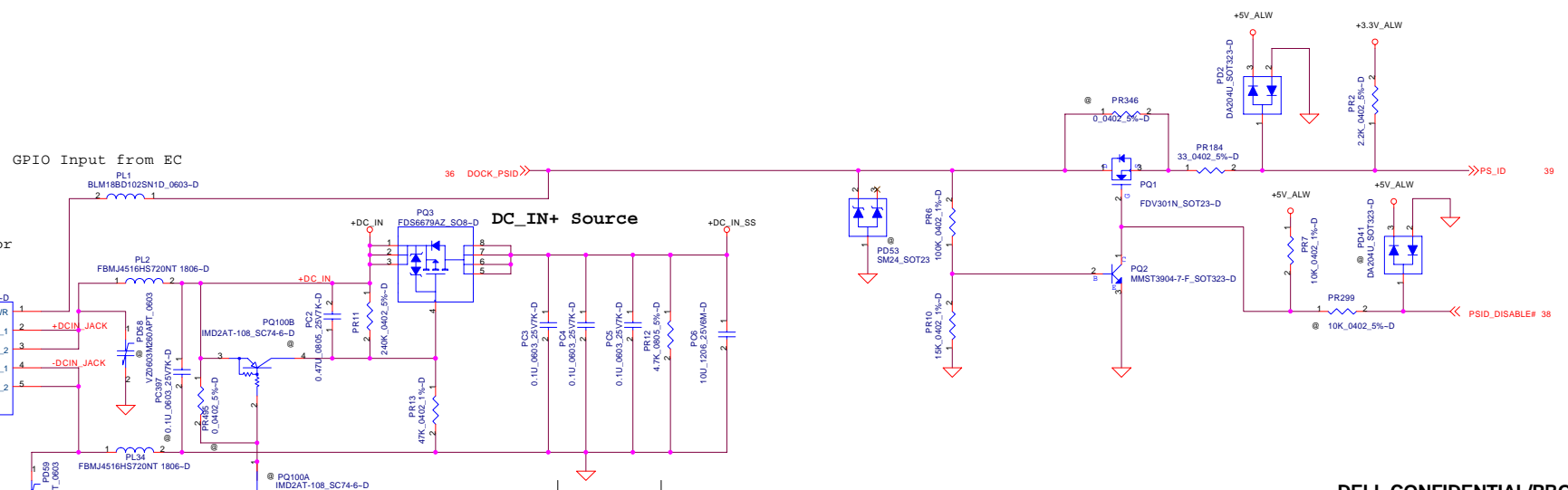
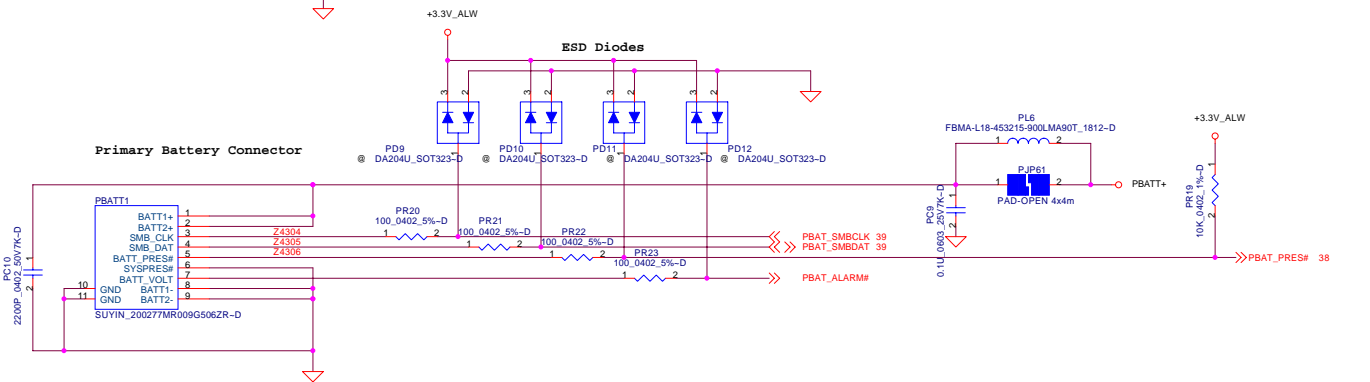
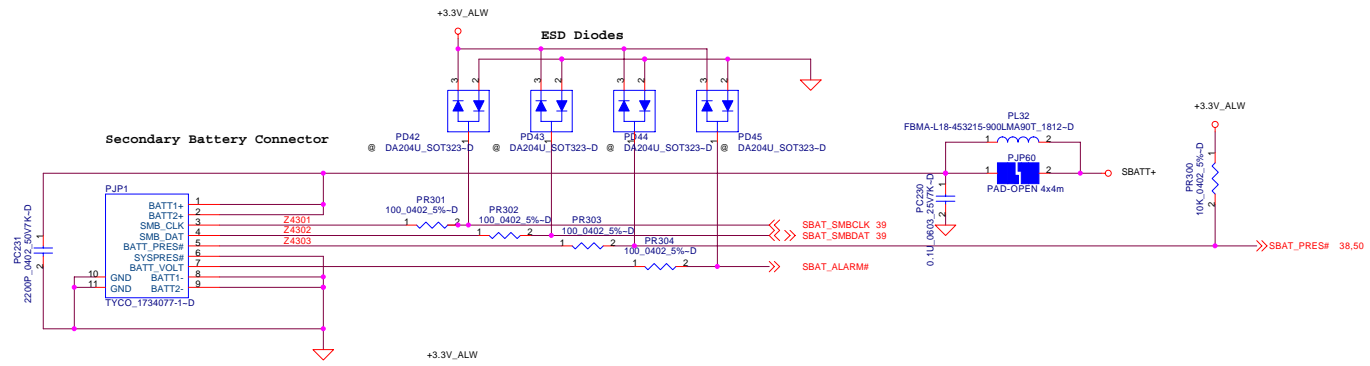
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**PAD and Standoff**

**LA-3301P**

Date: Monday, February 26, 2007 Sheet 43 of 58



Z-series AC Adaptor Connector

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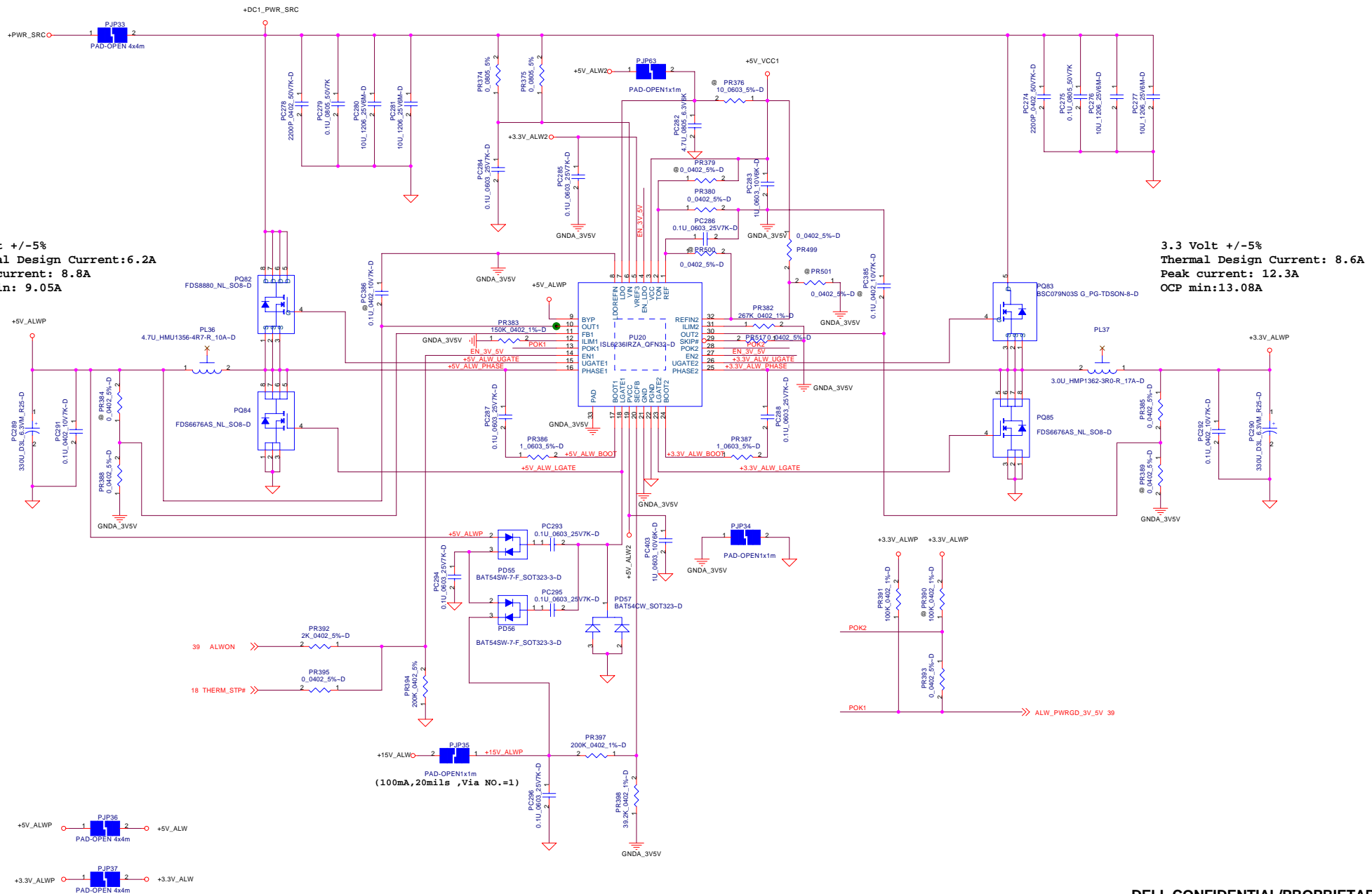
**Compal Electronics, Inc.**

File: **+DCIN**

Size: Document Number **LA-3301P** Rev: 0.0

Date: Monday, February 26, 2007 Sheet 44 of 58

**+3.3V\_ALWP/ +5V\_ALWP/ +5V\_ALW2 / +15V\_ALWP**



5 Volt +/-5%  
 Thermal Design Current: 6.2A  
 Peak current: 8.8A  
 OCP min: 9.05A

3.3 Volt +/-5%  
 Thermal Design Current: 8.6A  
 Peak current: 12.3A  
 OCP min: 13.08A

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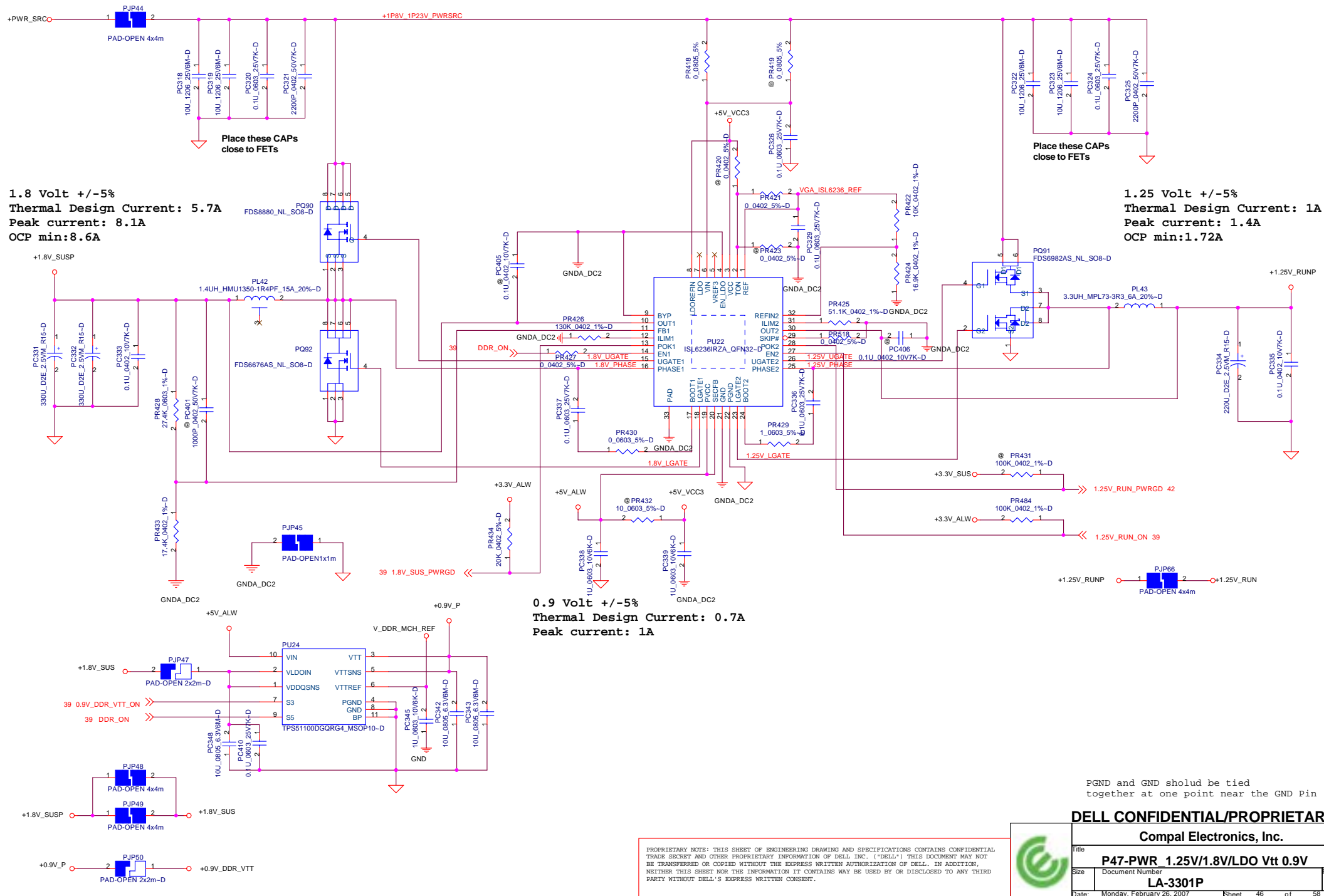
Compal Electronics, Inc.

File: DC/DC +3V/ +5V

Size: Document Number LA-3301P

Date: Monday, February 26, 2007 Sheet 45 of 58

1.8V/1.25V/0.9V VTT



1.8 Volt +/-5%  
 Thermal Design Current: 5.7A  
 Peak current: 8.1A  
 OCP min:8.6A

1.25 Volt +/-5%  
 Thermal Design Current: 1A  
 Peak current: 1.4A  
 OCP min:1.72A

0.9 Volt +/-5%  
 Thermal Design Current: 0.7A  
 Peak current: 1A

PGND and GND should be tied together at one point near the GND Pin

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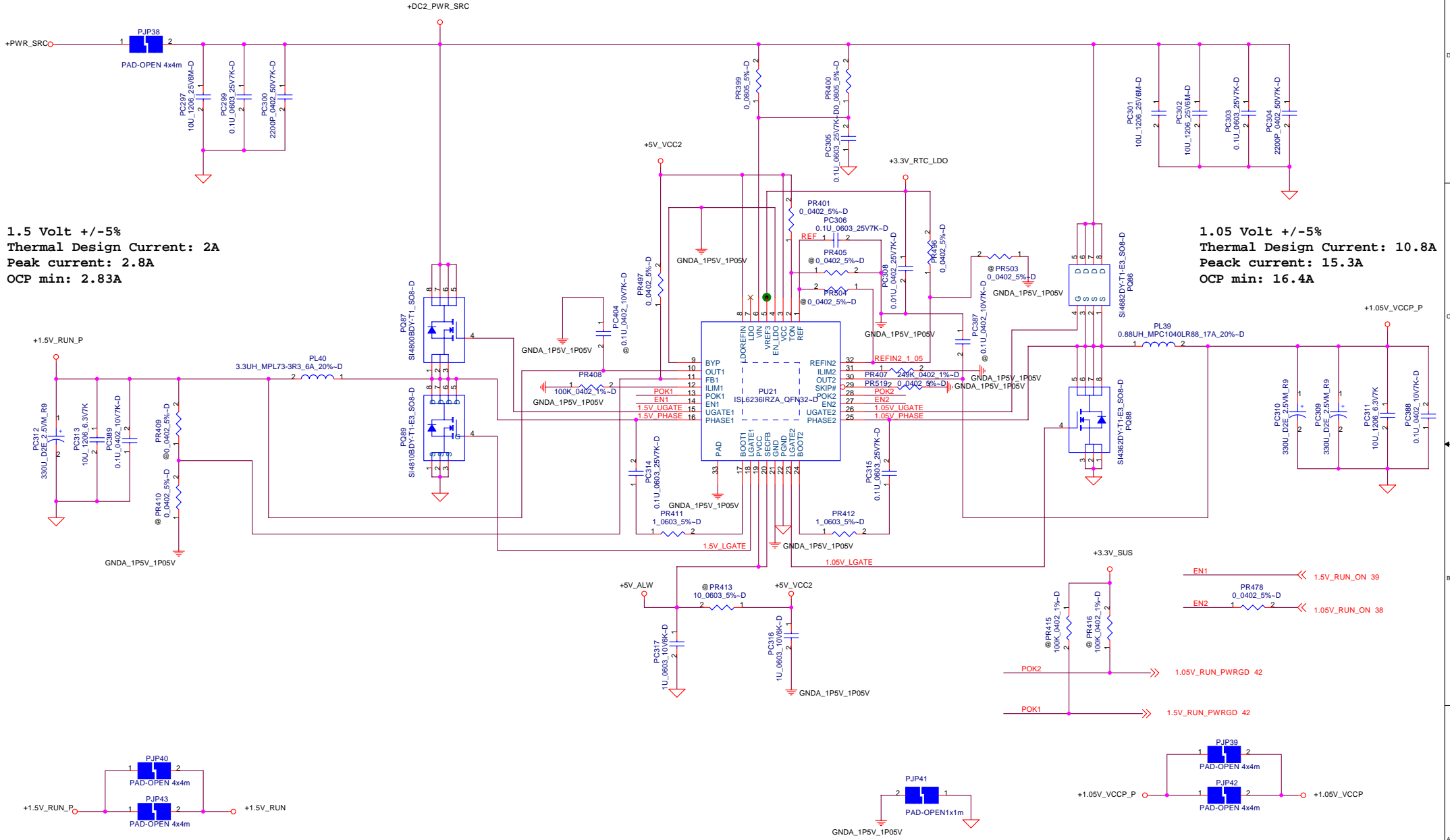
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Title		P47-PWR 1.25V/1.8V/LDO Vtt 0.9V	
Size	Document Number	LA-3301P	
Date	Monday, February 26, 2007	Sheet	46 of 58
Rev	0.0		

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**+1.5V\_RUN / +1.05V\_VCCP / +3.3V\_ALW / +3.3V\_RTC\_LDO**



**1.5 Volt +/-5%**  
**Thermal Design Current: 2A**  
**Peak current: 2.8A**  
**OCP min: 2.83A**

**1.05 Volt +/-5%**  
**Thermal Design Current: 10.8A**  
**Peak current: 15.3A**  
**OCP min: 16.4A**

OK to Short if CAD System can Support

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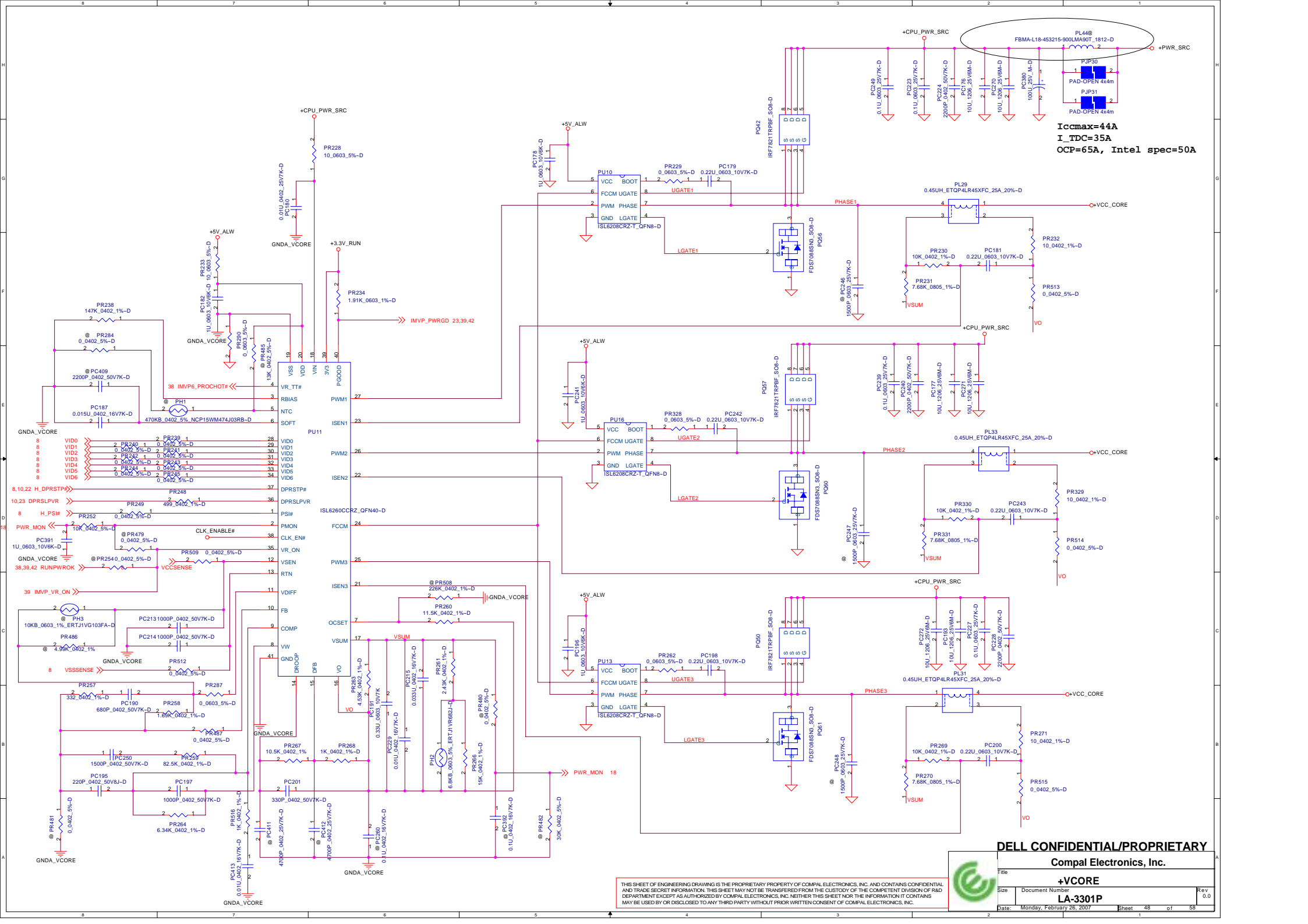


Title <b>+1.5V_RUN / +1.05V_VCCP</b>		
Size	Document Number <b>LA-3301P</b>	Rev 0.0
Date	Monday, February 26, 2007	Sheet 47 of 58

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Iccmax=44A  
 I\_TDC=35A  
 OCP=65A, Intel spec=50A

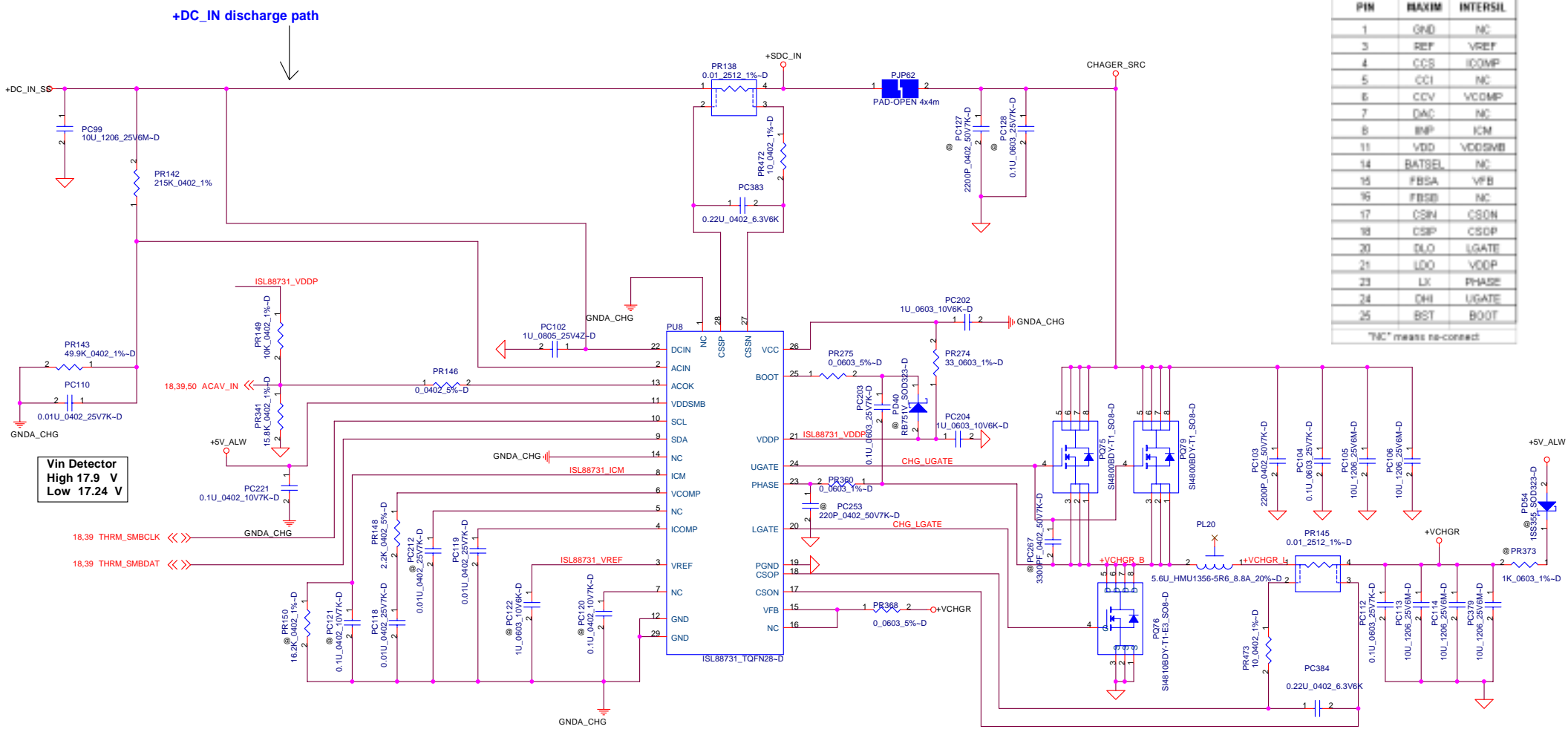
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File		+Vcore	
Size	Document Number	LA-3301P	
Date:	Monday, February 26, 2007	Sheet	48 of 58

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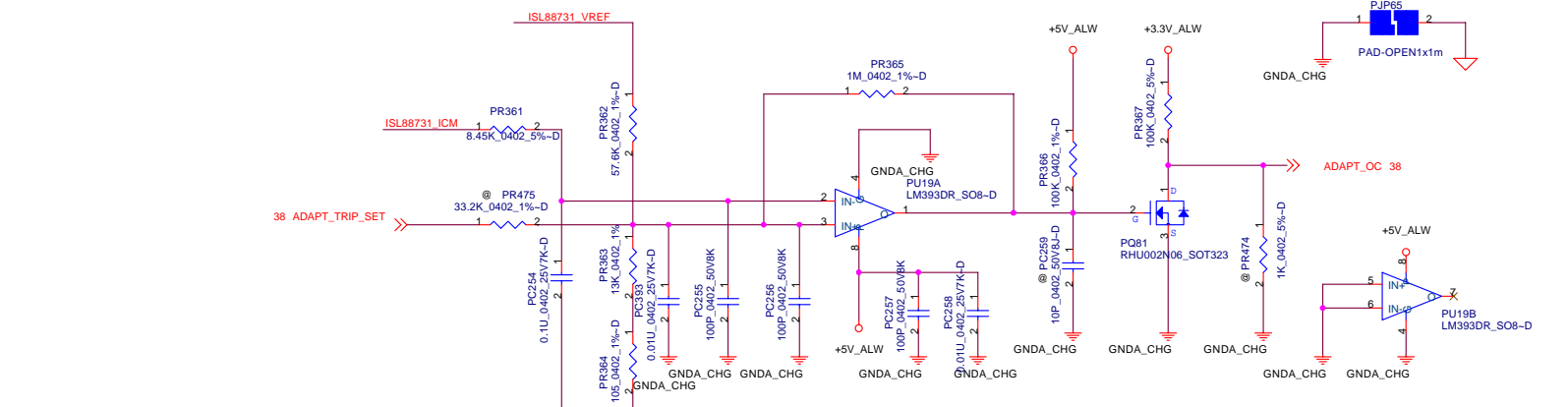
PIN	MAXIM	INTERSIL
1	GN0	NC
3	REF	VREF
4	CCS	ICOMP
5	CCI	NC
6	CCV	VCOMP
7	DAC	NC
8	INP	ICM
11	VDD	VDDSMB
14	BATSEL	NC
15	FBSA	VFB
16	FBSB	NC
17	CSIN	CSON
18	CSP	CSDP
20	DLO	LGATE
21	LOO	VOP
23	LX	PHASE
24	DH	UGATE
25	BST	BOOT

\*"NC" means no-connect



**Vin Detector**  
High 17.9 V  
Low 17.24 V

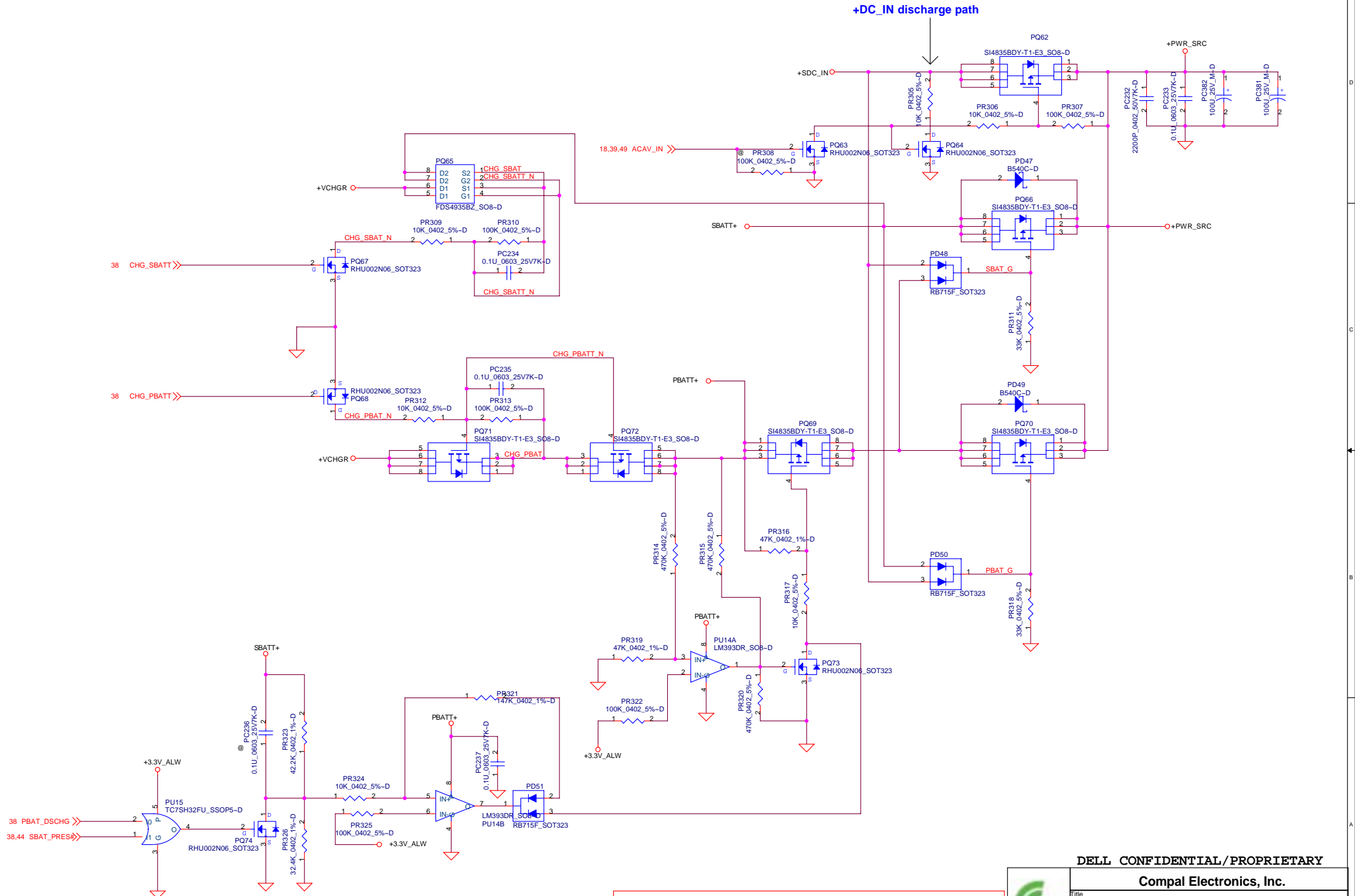
Maximum charging current is 6.24A



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Charger  
LA-3301P

Size	Document Number	Rev
		0.0
Date: Monday, February 26, 2007		Sheet 49 of 58



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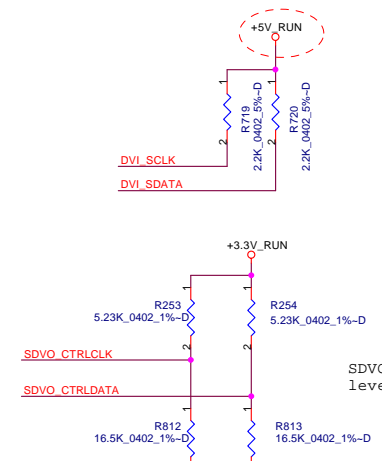
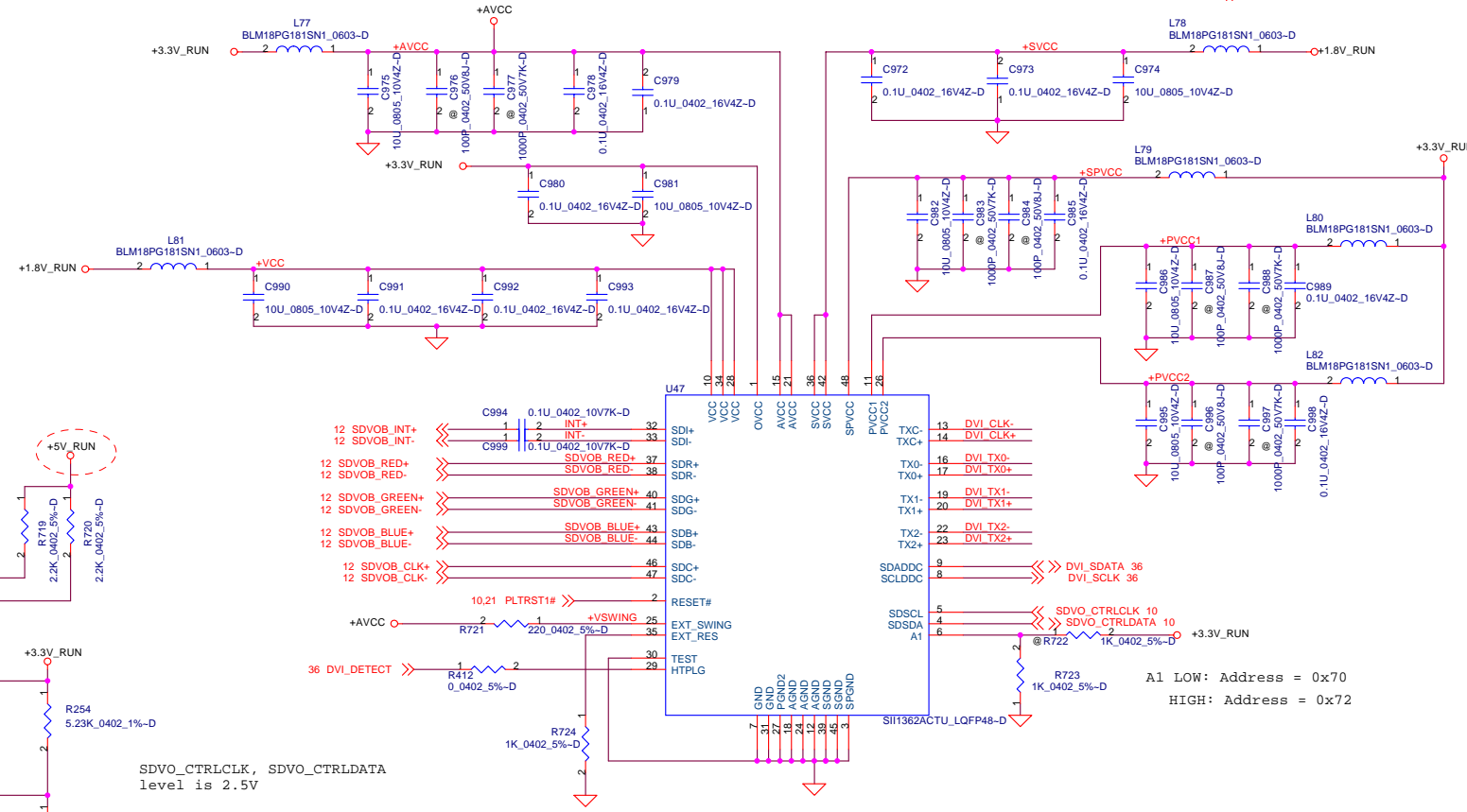
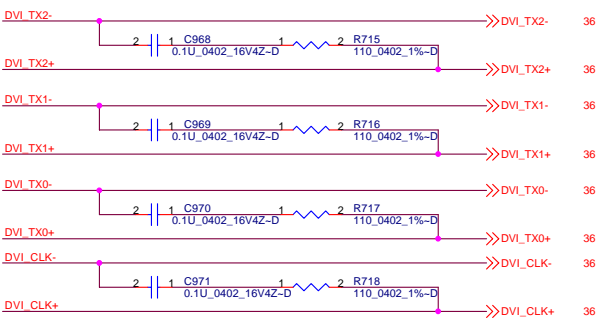
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LA-3301P

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A1 LOW: Address = 0x70  
HIGH: Address = 0x72

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**Internal LVDS**

File	LA-3301P		Rev	1.0
Size	Document Number			
Date:	Monday, February 26, 2007	Sheet	51	of 58

# Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	38	HW	08/2/2006	Compal	BID change to X01	Pop R108, depop R106	X01
2	18	HW	08/10/2006	Compal	Change SOT23 package to SOT323 package	Change Q102, to SOT323 package	X01
3	7	HW	08/21/2006	Compal	BITS issue WI86517 (S5 state back driver issue)	Change R324 pin1 connect from +3.3V_ALW to +3.3V_SUS	X01
4	41	HW	08/21/2006	Compal	Bits issue WI84312 (Derating issue)	Change R151 from 30 ohm to 75 ohm	X01
5	23	HW	08/21/2006	Compal	Bits issue WI86509	Populate R761 and change value from 100k to 10k. Change R761 pin1 connect from +3.3V_ALW to +3.3V_SUS	X01
6	12	HW	08/21/2006	Compal	Bits issue WI86510	Remove R390, R393. Connect LCTLA_CLK and LCTLB_DATA to GND	X01
7	39	HW	08/21/2006	Compal	Bits issue WI86511	Add R401 (100K) for signal BC_DAT pull up to +3.3V_ALW	X01
8	37	HW	08/21/2006	Compal	Bits issue WI86512	Change R131 to no-stuff and from 4.7k to 100k per SMSC	X01
9	23	HW	08/21/2006	Compal	Bits issue WI86516	R509 PU for SIO_EXT_SMI# change from +3.3V_ALW to +3.3V_SUS to prevent backdrive through the ICH in S4/S5	X01
10	38,39	HW	08/21/2006	Compal	Bits issue WI86518	Swap PSID GPIO from ECE5018 pin 71 with MEC5025 ITP_DBRESET#/HDT_RESET# pin 55	X01
11	38,39	HW	08/21/2006	Compal	Bits issue WI86531	Move BEEP (ECE5018 GPIOB[6]) to SGPIO46 of MEC5025	X01
12	18	HW	08/21/2006	Compal	Bits issue WI86752	Change pull-up rail for R773 from +5V_SUS to +3.3V_SUS	X01
13	21	HW	08/30/2006	Compal	Bits issue WI86530	Move SB_NB_PCIE_RST# to GPIO4/PIRQG# pinF12 per M08 design, add R631 (20K ohm) for pull down	X01
14	21	HW	09/7/2006	Compal	Bits issue WI86529	Move SB_WLAN_PCIE_RST# to GPIO3/PIRQF# U32 pin G11 per M08 direction, add test point T1 on pin F18	X01
15	39	HW	09/7/2006	Compal	Bits issue WI86376. Due to increase in number of payloads the BIOS is carrying	Change U23 from ( ST M25P80 8M bit ) to ) MXIC MX25L1605AM2C 16M bit )	X01
16	43	HW	09/11/2006	Compal	Bits issue WI90535	Change Q5 to MMBT3906WT1G, R15 to 150 ohm. Add R638 on LED_WLAN_OUT# pull up to +3.3V_WLAN. Add R639 (10K ohm) in series on LED_WLAN_OUT#	X01
17	7	HW	09/14/2006	Compal	Briscoe ESD/EMI Improvement Requests on PT	Remove ITP port and just keep ITP test point	X01
18	43	HW	09/14/2006	Compal	Bits issue WI90709	Remove R73, R178, C192, and C193	X01
19	34	HW	09/14/2006	Compal	Bits issue WI90705	Add SMBus isolation circuit for WLAN, R640,R645,R660,R662,Q45,Q46	X01
20	34	HW	09/14/2006	Compal	Bits issue WI90691	JMINI1 connect to +3.3V_RUN. Removed C427	X01
21	12	HW	09/14/2006	Compal	Shunt caps on LVDS for improving WWAN	Add C181,C192,C193,C196,C207,C209,R667,R685,R686, R687,R688 cross LVDS signals	X01
22	27	HW	09/14/2006	Compal	Bits issue WI90516	Remove C759 from mic amp bias circuit	X01
23	26	HW	09/14/2006	Compal	Bits issue WI90487	Populate R541to cut BEEP level in half	X01
24	43	HW	09/14/2006	Compal	Bits issue WI89631	populate EMI Clips Clip1, Clip2, Clip3, Clip4, Clip5, Clip6	X01

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Title		
Changed-List History		
Size	Document Number	Rev
	LA-3301P	1.0
Date:	Wednesday, February 14, 2007	
	Sheet	52 of 58

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# Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
25	23	HW	09/14/2006	Compal	Bits issue WI89409	No stuff R516, add R690 (8.2K ohm) for pull up ICH8 pin AF22 to +3.3V_SUS	X01
26	25	HW	09/14/2006	Compal	Bits issue WI89407	Add Q68, Q69, R691, R692 for HDDC_EN and MODC_EN circuits	X01
27	41	HW	09/14/2006	Compal	Bits issue WI89394	Change connect R765 pin1, R623 pin1, R621 pin1, R766 pin1 from +5V_ALW to +5V_ALW2	X01
28	37,39	HW	09/14/2006	Compal	Bits issue WI89379	Change R387,R389 from 1M to 2.7K. Add R778,R779 for AUX_ON,AC_OFF	X01
29	34	HW	09/15/2006	Compal	Bits issue WI90698	No stuff C16	X01
30	39	HW	09/15/2006	Compal	Bits issue WI92249	Change R730 from 100K to 4.7K ohm	X01
31	34	HW	09/15/2006	Compal	Bits issue WI92288,WI90714	R660 and R662 connected to CLK_SCLK and CLK_SDATA.	X01
32	37,22,33,28,19,20	HW	09/15/2006	Compal	EMI solutions	Populate RS232 C152,153,154,155,156,157,158,159. Resume ICH_AZ_MDC_BITCLK C656,R123,C128. Add R790,R791,C232,C267. Change L63,L65 from 0603size to 0805size. Add C309,C316 for LOM. Add C427,C463 for LVDS. Add fuse F3, R792 for CRT. Populate C660, R545 (10 ohm),C721 (10P)	X01
33	23,36	HW	09/18/2006	Compal	Bits issue WI92298	Move SIO_EXT_SCI# from to ICH8 GPIO11/SMBALERT# pin AG22 to GP012 pin AC19. Remove D22 and R761 and net DOCK_DET#	X01
34	23	HW	09/18/2006	Compal	Bits issue WI92299	ICH8 Pin AG22 tie to LOM_ICH_SMBALERT# and LOM_SMB_ALERT#. Change R730 pull up rail from +3.3V_ALW to +3.3V_LAN. Add R807 pull up to +3.3V_SUS for LOM_ICH_SMBALERT#	X01
35	39	HW	09/18/2006	Compal	Bits issue WI92301	Move ALW_PWRGD_3V_5V from MEC5025 pin 18 to MEC5025 pin 29. Remove 3.3V_5V_SUS_PWRGD from MEC5025 pin 29	X01
36	38,39	HW	09/18/2006	Compal	Bits issue WI92305	Swap DOCK_SMB_PME and DOCK_SMB_ALERT# from MEC5025 pin3 and ECE5028 pin76	X01
37	39,42	HW	09/18/2006	Compal	Bits issue WI92308	Removed 3.3V_LAN_PWRGD from MEC5025 KSO15/GPIO5. Remove U52,Q83,D29,R89,R98,R381,C784,C182,C183,C184	X01
38	39	HW	09/18/2006	Compal	Bits issue WI92312	Add R795 (0 ohm) pull down for MEC5025 pin 14	X01
39	29	HW	09/19/2006	Compal	EMI issue	Populate R671-R678 and C866-C869. Change L69-L76 from 24NH to 36NH inductor	X01
40	27	HW	09/19/2006	Compal	Bits issue WI90510	Add R796,R797 (0ohm) between L47/L48 and C728/C730	X01
41	6	HW	09/20/2006	Compal	Bits issue WI93162	NC JITP pin 1,2,3,5,7,11,12,13,15,17,19,21,23. Add test point T47-T52 for ITP_BPM#0-ITP_BPM#5. Remove R322	X01
42	28	HW	09/20/2006	Compal	Bits issue WI92858	Change R669 to from 1.15K to 1.13K. Depop C771 & C772. Change C861 and C862 to 22pF	X01
43	38	HW	09/20/2006	Compal	Bits issue WI92857	Add no-stuff series 0-ohm for ITP_DBRESET# on ECE5028	X01
44	19	HW	09/20/2006	Compal	WWAN noise issue	Add R808,R809,R810,R811 series for LCD_DDCCLK, LCD_DDCDATA, LCD_SMBCLK, LCD_SMBDAT	X01
45	33	HW	09/21/2006	Compal	Bits issue WI93157	Remove R586 and make JMDC pin2 NC	X01

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Title	LA-3301P		
Size	Document Number	Rev	1.0
Date:	Wednesday, February 14, 2007	Sheet	53 of 58

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# Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
46	34	HW	09/21/2006	Compal	Bits issue WI93158	Depop Q45, Q46	X01
47	51	HW	09/22/2006	Compal	Bits issue WI93586	Add R812,R813 (9.09K ohm) and chagne R253,R254 to 2.94K ohm for SDVO_CTRLCLK /DAT voltage divider	X01
48	6	HW	09/25/2006	Compal	Bits issue WI93403	C484 change to 33pF, C861/C862 change to 22pF	X01
49	29	HW	09/26/2006	Compal	Bits issue DF86424	No Populate C866-C869/R671-R678	X01
50	40	HW	09/26/2006	Compal	EMI request	Add D37-D40 for stick point signals	X01
51	32	HW	09/27/2006	Compal	EMI request	Add FUSE4,FUSE5	X01
52	18	HW	10/05/2006	Compal	Bits issue WI94892	Populate R771, C750, R772, Q102, R773	X01
53	30	HW	10/05/2006	Compal	Bits issue WI95910	Change R603 from 6.2k to 5.9k. Change C805 from 820pF to 270pF	X01
54	38,23 12,27,6	HW	10/05/2006	Compal	Bits issue WI95932	No stuff R227, R221, C89, C93, C97, c401, C92, r72, C90, C88. Change R369 to 3.3K 1%. No stuff C775-C781, C785. No stuff R514 (no iAMT). Populate R515.	X01
55	36	HW	10/14/2006	Dell	Bits issue WI97539	Added signal DOCK_DET# to JDOCKBpin137, pin205 and Q3pin2	X02
56	9	HW	10/17/2006	Dell	Bits issue WI97840	Add 0.1 uf (0402) caps on +Vcc_Core to Gnd. Four total, bottom of board. (C870 ~ C873)	X02
57	23	HW	10/18/2006	Dell	Bits issue WI98222 (Change for ASF2.0 due to ICH8M errata )	1. No stuff R502, R503 2. Connect the pad of R503.2 to the pad of R498.2 3. Connect the pad of R502.1 to the pad of R499.2	X02
58	38	HW	10/24/2006	Dell	Board ID Changed to X02	Populated R106, R107. Depopulated R108, R109.	X02
59	13	HW	10/27/2006	Dell	Bits issue WI100037. Intel CRT noise issue	Change L36 to 100 ohm resistor and change C722 to 22nF. Replace C569 with a 0603 1uF cap	X02
60	23	HW	10/30/2006	Dell	Bits issue WI100049	Add R816,C874 for USB_IDE#. R817,C875 for SIO_EXT_WAKE#. R819,C876 for PCIE_MCARD1_DET#. R820,C878 for USB_MCARD1_DET#. R818,C877 for USB_MCARD2_DET#. Remove net RSVD_GPIO6 and R513	X02
61	51	HW	11/2/2006	Dell	Bits issue WI100826	Change Change R812, R813 from 9.09K 1% to 13.7K 1%. Change R253, R254 from 2.94K 1% to 4.32K 1%	X02
62	28	HW	11/7/2006	Dell	Bits issue WI102451	Change L64,L66,L67,L68 from BLM18AG601SN1D to BK1608LM182. Change R668 to L88 BK1608LM182. Change L63, L65 from BLM21AG601SN1D to BK2125LM182. Chagne C850,C852,C856,C858 to 47pF caps. Change C849 to 1000pF. Populate C863, C864	X02
63	6,23,34	HW	11/8/2006	Dell	Bits issue WI103311	Change R309 from 8.2K to 2.2K. No stuff R820. No stuff R550	X02
64	2	HW	11/8/2006	Dell	Correct Block diagram	Correct block diagram	X02
65	39	HW	11/14/2006	Dell	Bits issue WI103986	Change C379 from 22pF to 33pF per KDS X'tal report	X02

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Title		
Changed-List History		
Size	Document Number	Rev
	LA-3301P	1.0
Date:	Wednesday, February 14, 2007	
	Sheet	54 of 58

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# Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
89	19	HW	2/28/2007	Compal	Bits issue WII25145.DPST enablement for UMA	Populate R156 (0_0402_5%)	A00
90	39	HW	3/1/2007	Compal	Bits issue WII25577	Populate R92. Depop R93	A00
91	13	HW	3/1/2007	Compal	Bits issue WII25883	Add note "C533,C534,C536,C545,C553,C579 are being replaced by 0-ohm 0805 resistor" on page 13	A00
92	18	HW	3/7/2007	Compal	Bits issue WII27297	Populate R441	A00
93	27	HW	3/7/2007	Dell	Bits issue WII27300	Change U40 from 74AHC1G08 to 74AHCT1G08	A00

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Date: Wednesday, March 07, 2007 Sheet 55 of 58

LA-3301P Rev 1.0

# Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
66	25,41	HW	11/20/2006	Compal	Bits issue WI105207	Change net name from +5V_ALW2 to +3.3V_ALW2 at R618.1, R626.1, R623.1, R621.1, R766.1, R765.1	X03
67	38,39	HW	11/21/2006	Dell	Bits issue WI105754	Change R794 pin1 from +5V_ALW to +3.3V_ALW. Change R245 pin1 from +3.3V_ALW to +5V_ALW	X03
68	26	HW	11/21/2006	Dell	Bits issue WI105758. Updates for potential Back Drive	Add 100kohm resistor R721 between U35 pin 40 and +3.3V_RUN and 1000pF cap C759	X03
69	51	HW	12/1/2006	Dell	Bits issue WI100826	Change R253, R254 from 2.94K_1% to 5.23K_1%. Change R812, R813 from 9.09K_1% to 16.5K_1%	X03
70	21,23,34	HW	12/1/2006	Dell	Bits issue WI106999	Please populate R820 with a 4.7k-ohm resistor. Move signal PCIE_MCARD2_DET# from ICH8m GPIO20 pinAE11 to PIRQH#/GPIO5 pinB3. Delete R457 and net ICH_GPIO5_PIRQH#. Populate R550	X03
71	41	HW	12/1/2006	Dell	Bits issue WI107466. +2.5V_LAN in-rush current test fai.	Populate C208	X03
72	27	HW	12/6/2006	Dell	Bits issue WI107896	Change R554 from 10K to 0 ohm	X03
73	36,38	HW	12/6/2006	Dell	Bits issue WI108259. Per M08 GPIO map rev A15 Change list	Change net DOCK_SMB_PME to DOCK_SMB_PME#	X03
74	9	HW	12/6/2006	Dell	Bits issue WI108223	Change C177,C179,C178,C366,C338,C365 to EEFSXD221E7 220uF	X03
75	38	HW	12/11/2006	Dell	Change Board ID from X02 to X03	Populate R108, Depop R106	X03
76	39	HW	12/14/2006	Dell	Bits issue WI110179	Add EC_FLASH_PAD pin1 connect to +3.3V_ALW,pin2 connect to R76 pin1 and R80 pin1	X03
77	27	HW	12/15/2006	Dell	Bits issue WI110158	Add R822 (1M_0402) from Pin 10 (C1P) pin of MAX9789A to ground	X03
78	13,14	HW	12/15/2006	Dell	Bits issue WI109712	Change C544,C560,C615,C551,C564,C593 to X6S SPEC	X03
79	26	HW	12/18/2006	Dell	Bits issue WI110749	Add R823 (10K_0402) to ground on pin 47 of STAC9205 (U37)	X03
80	29	HW	12/20/2006	Dell	Bits issue WI111288	Change R683 from 150ohms to 110 ohms, R684from 150ohms to 200ohms	X03
81	12,23,28	HW	12/25/2006	Dell	Change AC Coupling Cap SPEC for PCIE	Change C500-C507,C664,C666-C670,C851,C853,C994,C999 from 0.1uF Y5V to 0.1uF X7R	X03
82	38	HW	1/26/2007	Dell	Bits issue WI115658. M08 GPIO map rev A16 change	Change ECES028 GPIOF4 from BID2 to CHIPSET_ID.	A00
83	38	HW	1/26/2007	Dell	Change BID to from X03 to A00	Depop R107,R108. Populate R106,R109	A00
84	23	HW	2/12/2007	Dell	Bits issue WI121957	Add R834 (1M_0402_1%) for ICH_LAN_RST#	A00
85	27	HW	2/12/2007	Dell	Bits issue WI121438	Change R565 from 10K to 100k ohm	A00
86	41	HW	2/12/2007	Dell	Bits issue DF116813	Depop C194, changed C815 from 4700pF to 2200pF	A00
87	13	HW	2/27/2007	Dell	Bits issue WI109712. Because can't find 2nd source	Change C560 and (C615, C551, C564) Back to X5R	A00
88	23	HW	2/27/2007	Dell	Bits issue WI125173. Per Intel's latest recommendation	Change R834 from 1M to 10K	A00

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Changed-List History

Title	LA-3301P		
Size	Document Number	Rev	1.0
Date:	Wednesday, February 28, 2007	Sheet	55 of 58

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# Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	48/50	PWR	9/14	Elick	change the AL CAP to 2000hr	change PC380 from SF10004M08L to SF000000S8L. change PC381 from SF10004M08L to SF000000S8L. change PC382 from SF10004M08L to SF000000S8L.	0.1
2	45	PWR	9/14	DELL	BITS-WI91007 change to correct part for 15ALW.	change PD55 from SCSB717F08L to SCS00001U8L. change PD56 from SCSB717F08L to SCS00001U8L.	0.1
3	48	PWR	9/14	DELL	change to PSL of DELL	change PH2 from SL20000030L to SL200000F8L	0.1
4	44	PWR	9/14	DELL	change to PSL of DELL	change PL1 from SM01001680L to SM010008U0L.	0.1
5	44	PWR	9/14	DELL	change to PSL of DELL	change PL2 from SM01001418L to SM010009C8L. change PL34 from SM01001418L to SM010009C8L.	0.1
6	46	PWR	9/14	DELL	BITS-WI89364 The 0.9V_DDR_VTT_PWRGD net is not used at the MEC5025. The 0.9V_DDR_VTT_PWRGD net should be no connect at the MEC5025 pin 73.	remove PR437, PR438, PR441, PQ93 and PQ94.	0.1
7	45	PWR	9/14	DELL	BITS-WI90985 following DELL rule	Change PC285 pin 2 pad connection from PGND to AGND.	0.1
8	45	PWR	9/14	DELL	BITS-WI90999 Change PQ83 from FDS8880 to BSC079N03SG PPAK	Change PQ83 from SB000004U8L to SB000004D8L.	0.1
9	45	PWR	9/14	DELL	BITS-WI91012 change to correct current limits	Change PR383 from 124k(SD03412438L) to 150K(SD03415038L). Change PR382 from 187k(SD03418738L) to 226K(SD03422638L).	0.1
10	47	PWR	9/14	DELL	BITS-WI91287 following DELL rule	Depopulate PR415 and PR416 resistors.	0.1
11	47	PWR	9/14	DELL	BITS-WI91288 Change PQ86 from SI4392DY to SI4682DY.	change PQ86 from SB54392008L to SB000006N0L	0.1
12	49	PWR	9/14	DELL	BITS-WI91291 be compliant with the reference schematic.	Change PR274 from 4.7 ohm(SD000006T8L) to 33 ohm(SD014330A8L). Populate PR373 and PD54.	0.1
13	47	PWR	9/14	DELL	BITS-WI91374 following DELL rule	Change PR408 from 75K(SD03475028L) to 82.5K(SD00000278L).	0.1
14	46	PWR	9/14	DELL	BITS-WI91672 Change in 1.25V_RUN_PWRGD circuit.	Change the node name connected to pin 2 of PR431 from +3.3V_ALW to +3.3V_SUS. Depopulate PR431.	0.1
15	44	PWR	9/14	DELL	BITS-WI91689 DC IN schematic changes.	Change PL1 from SM01001680L to SM010008U0L. Change PQ100 from SI2301BDS(SB923010020) to PQ100A depopulated IMD2A(SB000009N8L). Change PQ101 from SI2301BDS(SB923010020) to PQ100B depopulated IMD2A(SB000009N8L). Change PR12 from 10K,0603(SD01310028L) to 4.7K,0805(SD00247018L).	0.1

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Title **Changed-List History 1**

Size Document Number **LA-3301P** Rev **0.6**

Date: Wednesday, February 28, 2007 Sheet 56 of 58

# Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
16	46	PWR	9/15	DELL	BITS-WI92156 correct the current limit on 1.25V output	change PR425 from 39.2K(SD03439228L) to 51.1K (SD03451128L)	0.1
17	46	PWR	9/15	DELL	BITS-WI91655 Add 0.1uF connected to the pins 1 and 2 of PU24	Add PC410(SE042104K8L). One pad connected to the pins 1 and 2 of PU24 . The other pad is connected to PGND.	0.1
18	46	PWR	9/15	DELL	BITS-WI91929 correct the current limit on 1.8V output	change PR426 from 110K(SD03411038L) to 130K (SD03413038L)	0.1
19	48	PWR	9/18	DELL	BITS-WI92465 improve transients at load dump. and reduce jittering.	Add depopulate PR516(SD03410018L) and depopulate PC413(SE076103K8L) between pin 9 of PU11 and AGND. Add depopulated PC411(SE075472K8L),4700pF between pin 14 of PU11 and AGND . Add depopulated PC412(SE075472K8L),4700pF between pin 15 of PU11 and AGND	0.1
20	44	PWR	9/21	DELL	BITS-WI91689 change PL1 from BK1608HM to BLM18BD102SN1D.	change PL1 from SM010008U0L to SM010007C8L.	0.1
21	48/50	PWR	9/21	DELL	BITS-WI87563 change populate PC380 from 25CE100AX to 25CE100LS change PC381 from 25CE100AX to 25CE100LS change PC382 from 25CE100AX to 25CE100LS	change populate PC380 from SF000000S8L to SF000000T8L. change PC381 from SF000000S8L to SF000000T8L. change PC382 from SF000000S8L to SF000000T8L.	0.1
22	49	PWR	9/29	DELL	match Maxim's response time of ICM input to comparator.	change PR361 from 0 Ohm (SD02800008L) to 8.45K (SD00000068L). change PC254 from 0.01uF 25V (SE068103K8L) to 0.1uF 16V (SE076104K8L).	0.1
23	49	PWR	9/29	DELL	ICM is voltage source and does not need this component.	depopulate PR150.	0.1
24	49	PWR	9/29	DELL	Increase BW from 20kHz to 25kHz while maintaining 80degrees phase margin.	change PR148 from 4.7K (SD03447018L) to 10K (SD03410028L).	0.1
25	49	PWR	9/29	DELL	following DELL rule	depopulate PD54 and PR373	0.1
26	48	PWR	10/27	DELL	Add bead to connect +PWR_SRC to +CPU_PWR_SRC	Add PL44(SM01002078L) to parallel PJP30.	0.2
27	45,46,47	PWR	10/27	DELL	BITS-WI99902 This is to add an optional ultrasonic mode in case the regulators experience an audible noise.	Add PR517(SD02800008L) between pin 29 of PU20 and AGND . Add PR518(SD02800008L) between pin 29 of PU22 and AGND . Add PR519(SD02800008L) between pin 29 of PU21 and AGND .	0.2
28	46	PWR	10/31	DELL	BITS-WI100140 Change PR429 from 0 ohm to 1 ohm	change PR429 from 0 Ohm (SD01300008L ) to 1 Ohm(SD013100B8L).	0.2

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Title **Changed-List History 2**

Size Document Number Rev

LA-3301P 0.6

Date: Wednesday, February 28, 2007 Sheet 62 of 62

# Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
29	49	PWR	11/16	DELL	BITS: WI102613 Change PR148 from 10K_0402_1% to 2.2K_0402_5%	change PR148 from 10K 0402 1% (SD03410028L ) to 2.2k 0402 5%(SD02822018L)	0.3
30	45	PWR	11/20	DELL	BITS-WI105401 Add node name +3.3V_ALW2 for the trace connected to the pin 5 (VREF3) of PU20. Populate PC285 with 0.1uF cap.	Add node name +3.3V_ALW2 between pin5 of PU20 and PC285. Populate PC285.	0.3
31	49	PWR	12/06	DELL	BITS-WI106278 make sure that PC113, PC114 and PC379 are X5R/X75 caps, need to stuff PC379.	change PC379 is populated.	0.3
32	48	PWR	12/06	DELL	BITS-WI108223 Change PC187 from 10nF to 15nF. Change PR258 from 2.21K to 1.69K. Populate PR516 with 1K resistor. Populate C413 with 0.01uF.	change PR187 from 10nF(SE076103K8L) to 15nF(SE076153K8L). change PR258 from 2.21K(SD03422118L) to 1.69K(SD00000JB8L). populate PC413. populate PR516.	0.3
33	49	PWR	01/25	ELICK	change to new part number for PSL	change PR138 from SD021100D8L to SD021100D3L(S RES 1W .01 +-1% 2512 FOR M08 PROJECTS) change PR145 from SD021100D8L to SD021100D3L(S RES 1W .01 +-1% 2512 FOR M08 PROJECTS)	0.4
34	45/47	PWR	02/05	DELL	BITS-WI119945 Increase current limits for 3.3V and 1.5V regulators.	change PR382 from 226K to 267k (SD02822018L). Change PR408 from 82.5K to 100K(SD03410038L).	0.4
35	49	PWR	02/06	DELL	additional 1206 resistor on +VCHGR for Maxim solution.	add an unpopulation PR520 (1.8K 1206 1%(SD00000JN8L))between +VCHGR to PGND.	0.4
36	49	PWR	02/12	DELL	delete 1206 resistor on +VCHGR not to implement for Maxim solution.	delete an unpopulate PR520 (1.8K 1206 1%(SD00000JN8L))between +VCHGR to PGND.	0.4

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<b>Changed-List History 3</b>			
Size	Document Number	Rev	
	<b>LA-3301P</b>	0.6	
Date:	Wednesday, February 28, 2007	Sheet	58 of 58