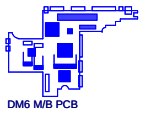


DM6-INTEGRATED

PWA: HP722 (965GM) / HP714 (960GL)
PWB: HP729
SCHEM: HP732
VER : 1B

POWER

- SYSTEM RESET CIRCUIT — PG 38
- BATT SELECTOR — PG 39
- BATT CHARGER — PG 40
- RUN POWER SW — PG 45
  +3.3V_SUS/+5V_SUS
  +5V/+3.3V/+1.8V

AC/BATT CONNECTOR PG 46

Merom
(478 Micro-FCPGA)
PG 3,4
(Symbol Rev.09)

667/800 MHz FSB

POWER

- REGULATOR — PG 41
  +1.5V_RUN/+1.05V_VCCP
- REGULATOR — PG 42
  +1.8V_SUS/+1.25V_RUN /+0.9V_DDR_VTT
- CPU VR — PG 43
- DC/DC — PG 44
  +3.3V_ALW/+5V_ALW/+15V_ALW

CLOCK
CK505
PG 17

Crestline
1299 uFCBGA
PG 5,6,7,8,9,10
(Symbol Rev.09)

- LVDS → **Panel Connector** PG 20
- SDVO → **SI1362** PG 18
- TVOUT → **S-Video** PG 19
- VGA → **CRT CONN.** PG 21

DDR2-SODIMM1 PG 15,16 — 533/667 MHZ DDR II
DDR2-SODIMM2 PG 15,16 — 533/667 MHZ DDR II

DMI interface

- USB2.0 (P0,P1) (EXT SIDE)
- USB2.0 (P2,P3) (EXT BACK)
- USB2.0 (P8)

→ **4 Port USB** PG 31

ICH8-M
676 BGA
PG 11,12,13,14
(Symbol Rev.09)

- IDE / USB2.0 (P4) → **Internal Media Bay** **CD-ROM** PG 22
- SATA → **SATA - HDD** PG 22
- IHDA → **AUDIO/AMP** PG 33,34; **MDC** PG 25
- 33MHz PCI → **CARDBUS/1394** OZ711EZ1TN PG 23
- USB2.0 (P6)
- PCIEx1 → **MINI-CARD** WLAN PG 24
- USB2.0 (P7) → **Bluetooth** PG 30
- PCIEx1 → **BCM5755M /BCM5752** PG 35 → **E-Switch** PI3L500 +3.3V_LAN PG 36 → **I/O Board CONN** PG 31

DOCKING CONNECTOR PG 37

SPI / LPC

S/PDIF for Dock PG 37
S/PDIF for MINI DIN 7 PG 19
Reserved.
Audio Jacks PG 34
RJ11 for Dock PG 37
Tip Ring PG 25

SIO MEC5025 128KB Flash TMKBC
128 Pins VTQFP PG 26

BC

SIO ECE5028
128 Pins VTQFP PG 27

DOCK LPC

Keyboard Controllor ECE1077 PG 29 — BC

SPI / PS/2

- **USER INTERFACE** PG 31
- **Keyboard** PG 29
- **FLASH** PG 29
- **Touchpad/ Stick point** PG 30
- **Serial Port** PG 28
- **IrDA** PG 30

FAN & THERMAL EMC4001 PG 32

QUANTA COMPUTER

Title	Schematic Block Diagram1	
Size	Document Number DM6	Rev 1A
Date: Monday, August 06, 2007	Sheet 1 of 52	

Table of Contents

PAGE	DESCRIPTION
1	Schematic Block Diagram
2	Front Page
3-4	Merom
5-10	Crestline
11-14	ICH8M
15-16	DDRII SO-DIMM(200P)
17	Clock Generator
18-19	VGA
20	LCD Conn. & SSP
21	CRT Conn
22	SATA & IDE Conn
23	PCCARD/Conn
24	Mini Card
25	MDC Conn.
26	SIO (MEC5025)
27	SIO (MEC5028)
28	SERIAL PORT
29	Flash ROM, RTC & ECE1077
30	TP,BT & FIR
31	Switch & LED
32	FAN & Thermal
33-34	Audio CODEC(STAC9205)/Phone Jack
35-36	LOM (Nineveh)/Switch
37	Docking Conn
38	System Reset Circuit
39-40	Battery Selector & Charger
41	1.5VSUS,1.05V(VTT)
42	1.25V,1.8V,0.9V
43	CPU_ISL6260C(3phase)
44	D/D Power
45	RUN Power Switch
46	DCIN,Batt
47	PAD& SCREW
48	SMBUS BLOCK
49	Power Block Diagram

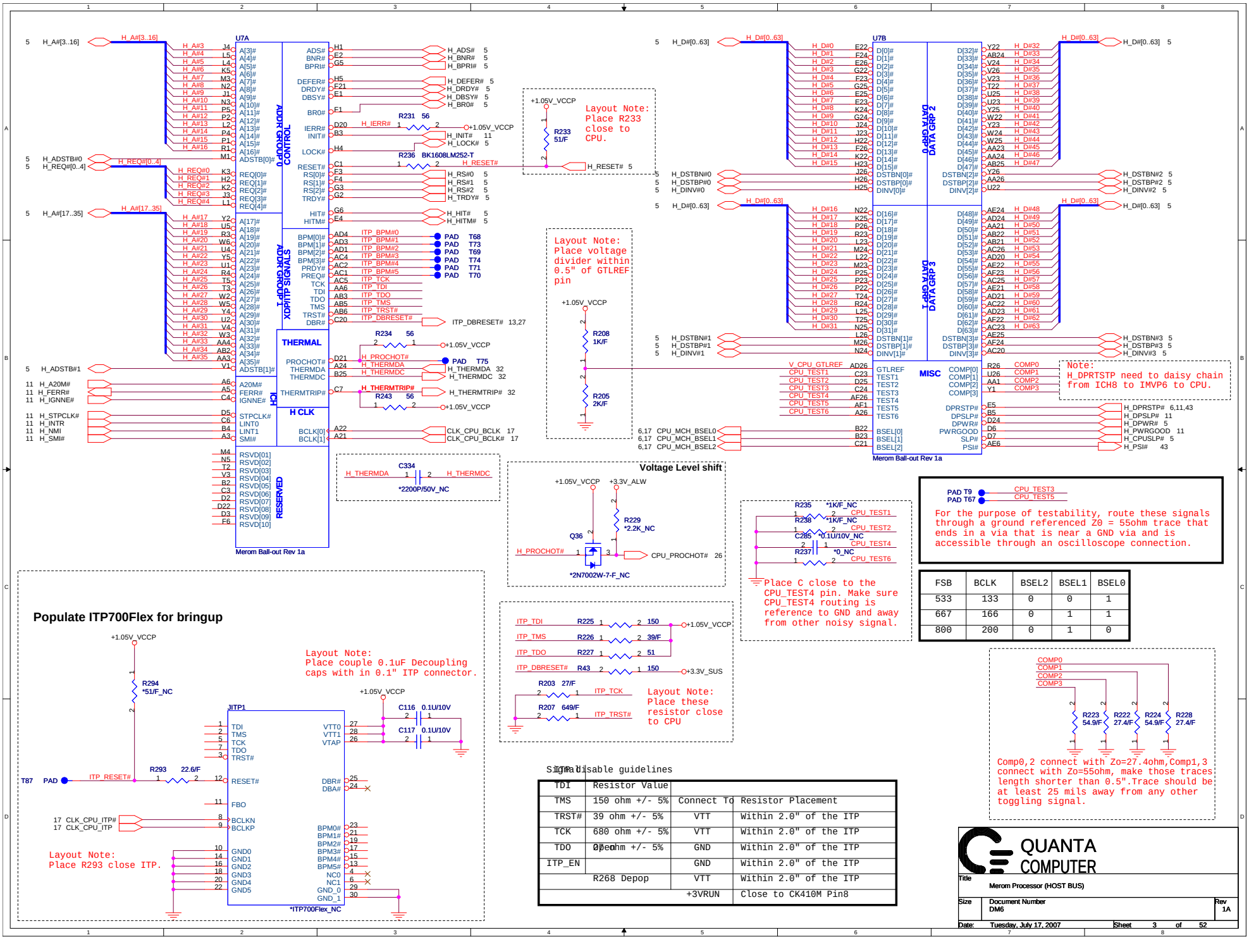
Power States

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	4,20,29,36,37,39,41,42,43,44,47	MAIN POWER		S0~S5
+RTC_CELL	+3.0V~+3.3V	11,14,26,29,31,32	RTC		S0~S5
+3.3V_ALW	+3.3V	3,12,13,17,20,22,26,27,29,31,32,36,37,38,39, 40,42,44,45,46	8051 POWER	ALWON	S0~S5
+5V_ALW	+5V	20,22,26,27,31,37,38,40,41,43,44,46,46	LCD/CHARGE POWER	ALWON	S0~S5
+15V_ALW	+15V	20,22,44,45	LARGE POWER	+5V_ALW	S0~S5
+3.3V_LAN	+3.3V	31,35,36	LAN POWER	AUX_ON	
+5V_SUS	+5V	14,25,32,38,42,45,47	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	3,11,12,13,14,25,27,28,29,31,32,37,38,41,42, 45,47	SLP_S5# CTRLD POWER	3.3V_SUS_ON	
+1.8V_SUS	+1.8V	6,8,9,15,38,42,45,47	SODIMM POWER	DDR_ON	
+0.9V_DDR_VTT	+0.9V	16,42,45	SODIMM POWER	0.9V_DDR_VTT_ON	
+5V_RUN	+5V	14,18,19,21,22,23,26,30,31,32,33,38,43,45	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	6,8,9,11,12,13,14,15,17,18,19,20,21,22,23,27, 30,31,32,33,34,35,36,37,38,43,45,47	SLP_S3# CTRLD POWER	3.3V_RUN_ON	
+1.8V_RUN	+1.8V	18,38,45	SDVO POWER	RUN_ON	
+1.5V_RUN	+1.5V	4,9,14,24,24,41,45,47	CALISTOGA/ICH8 POWER	1.5V_RUN_ON	
+1.25V_RUN	+1.25V	6,9,14,42,45	CALISTOGA/ICH8 POWER	1.25V_RUN_ON	
+1.05V_VCCP	+1.05V	3,4,5,6,8,9,11,14,32,41	CPU/CALISTOGA/ICH8 POWER	1.05V_RUN_ON	
+VCC_CORE	+0.7V~+1.77V	4,43	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	20	LCD Power	LCDVCC_TST_EN & ENVDD	
+5V_MOD	+5V	22	Module Power	MODC_EN#	
+5V_HDD	+5V	22	HDD Power	HDDC_EN#	
+PBATT	+10V~+17V	39,46	MAIN BATTERY	CHG_PBATT	
+SBATT	+10V~+17V	39,46,47	SECOND BATTERY	CHG_SBATT	

GND PLANE	PAGE	DESCRIPTION
8731AGND	40	
AGND_DC/DC	44	
AGND_DC2	41	
GND_DDR	42	
AGND_ISL6260	43	
GND	ALL	

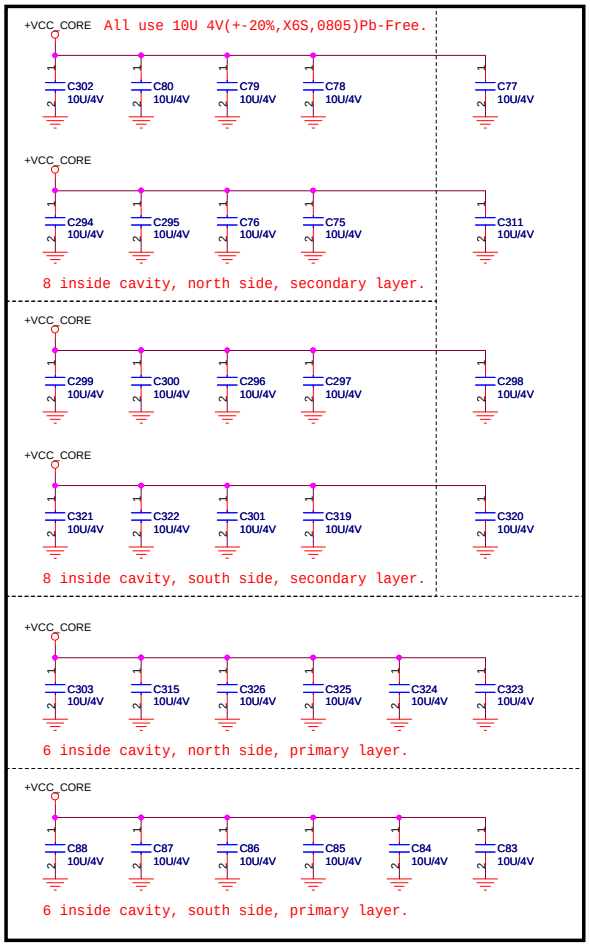
QUANTA COMPUTER

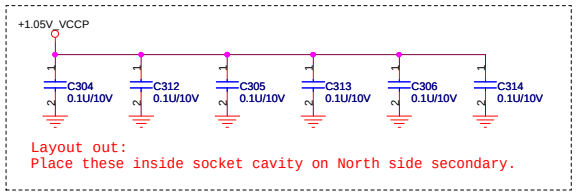
Title	Index & Power Status	
Size	Document Number DM6	Rev 1A
Date: Friday, June 08, 2007	Sheet 2 of 52	

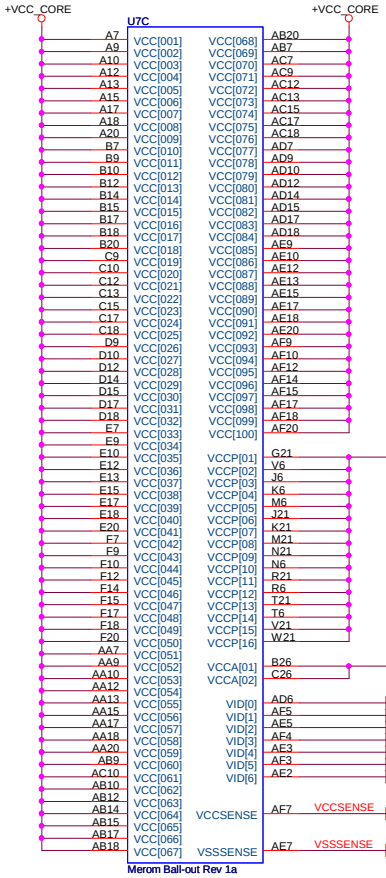


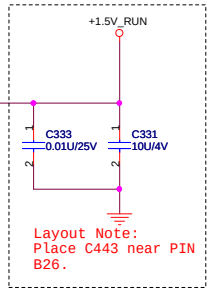
FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0

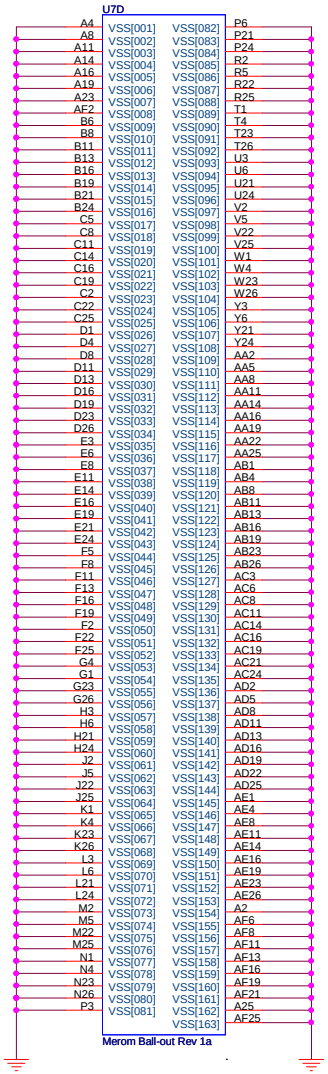
TDI	Resistor Value		
TMS	150 ohm +/- 5%	Connect To	Resistor Placement
TRST#	39 ohm +/- 5%	VTT	Within 2.0" of the ITP
TCK	680 ohm +/- 5%	VTT	Within 2.0" of the ITP
TDO	27 ohm +/- 5%	GND	Within 2.0" of the ITP
ITP_EN		GND	Within 2.0" of the ITP
	R268 Depop	VTT	Within 2.0" of the ITP
		+3VRUN	Close to CK410M Pin8



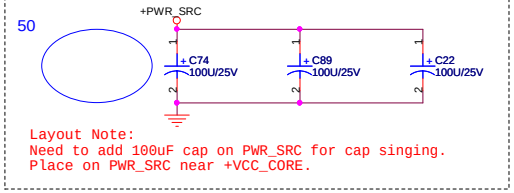


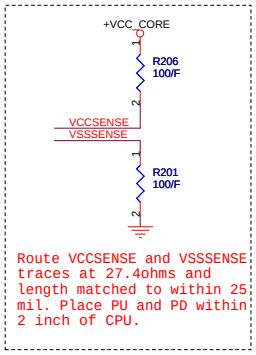






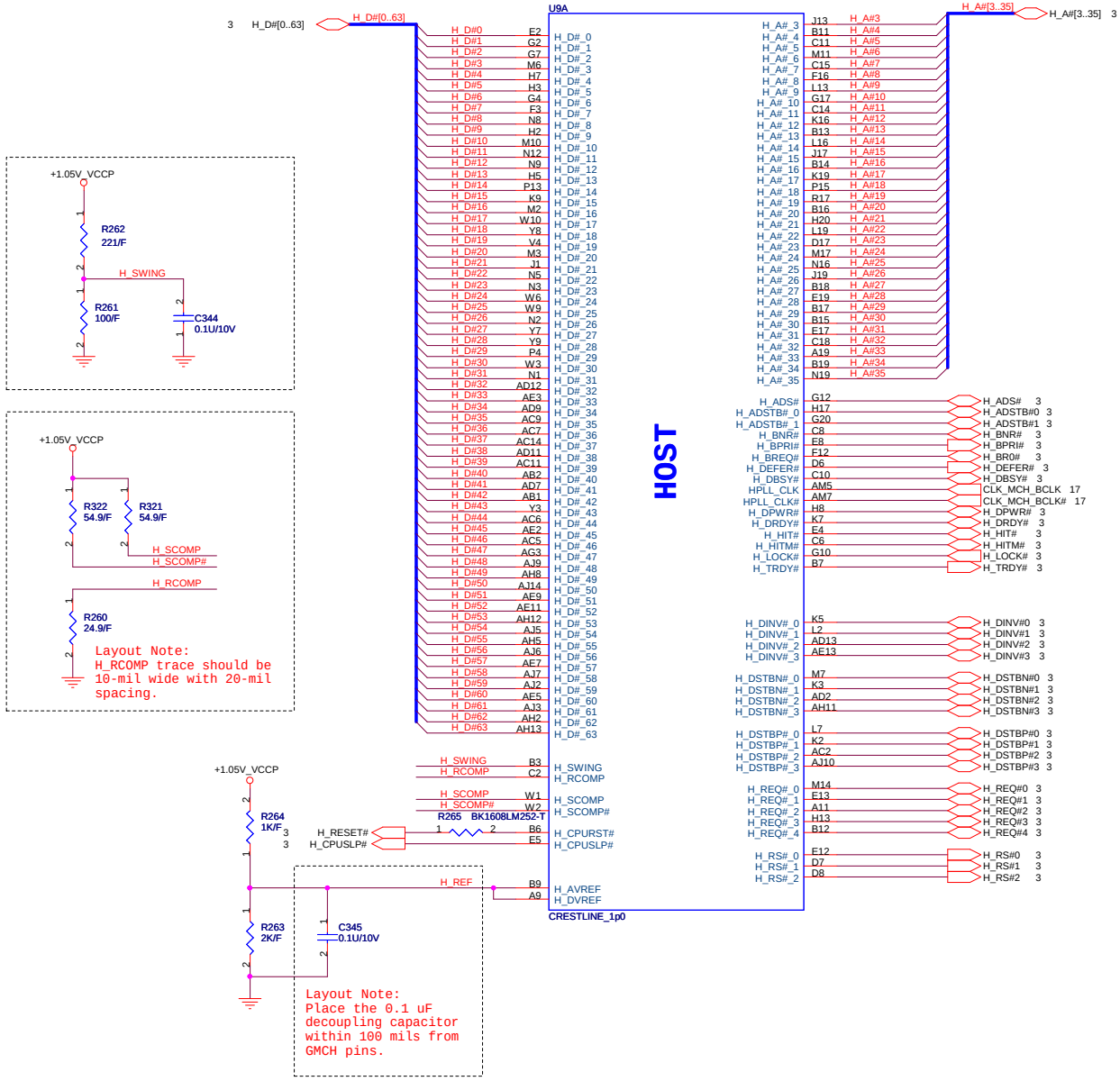
Del C59 on 0525





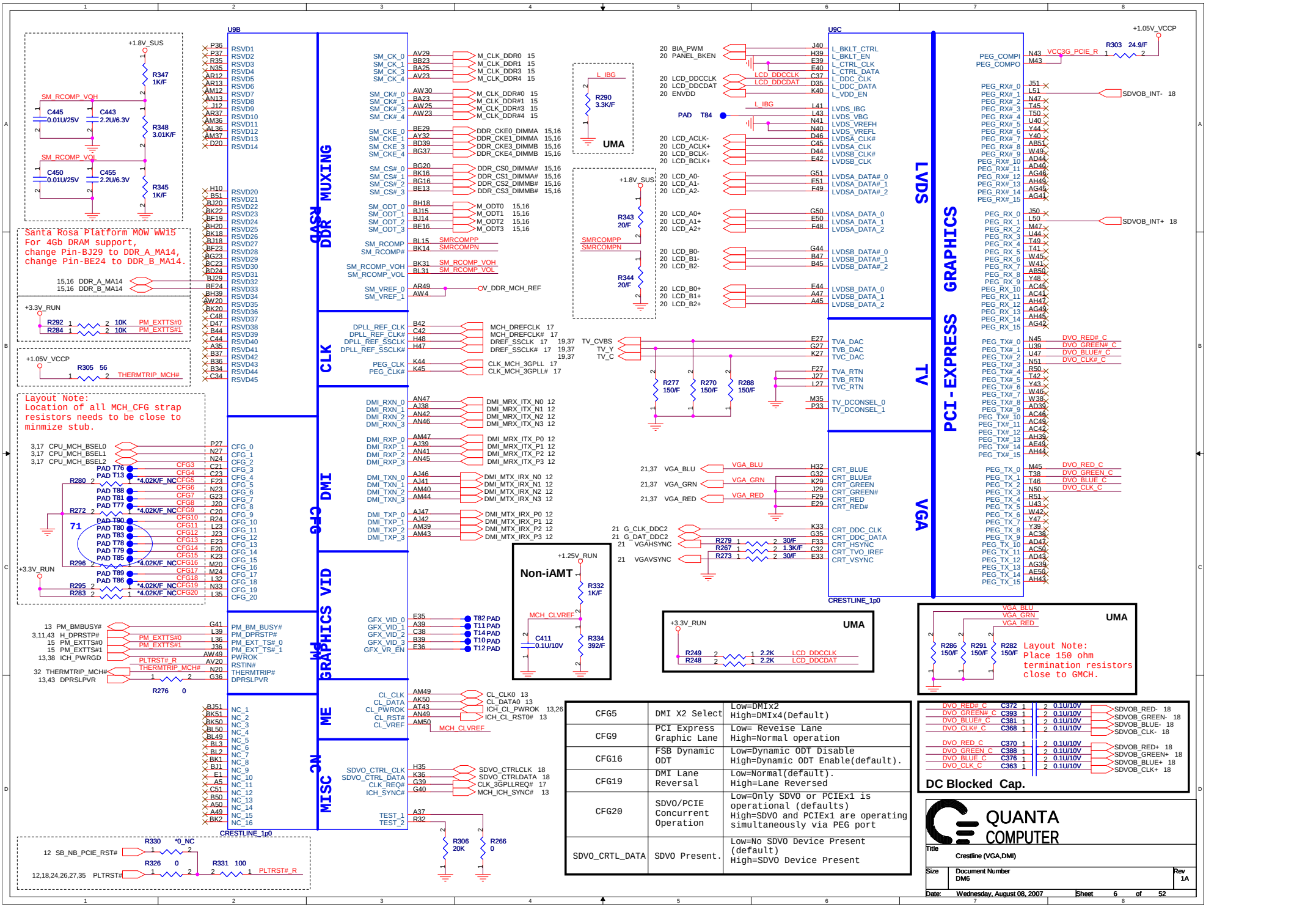
QUANTA COMPUTER

Title	Merom Processor (POWER)	
Size	Document Number DM6	Rev 1A
Date: Friday, June 08, 2007	Sheet 4 of 52	

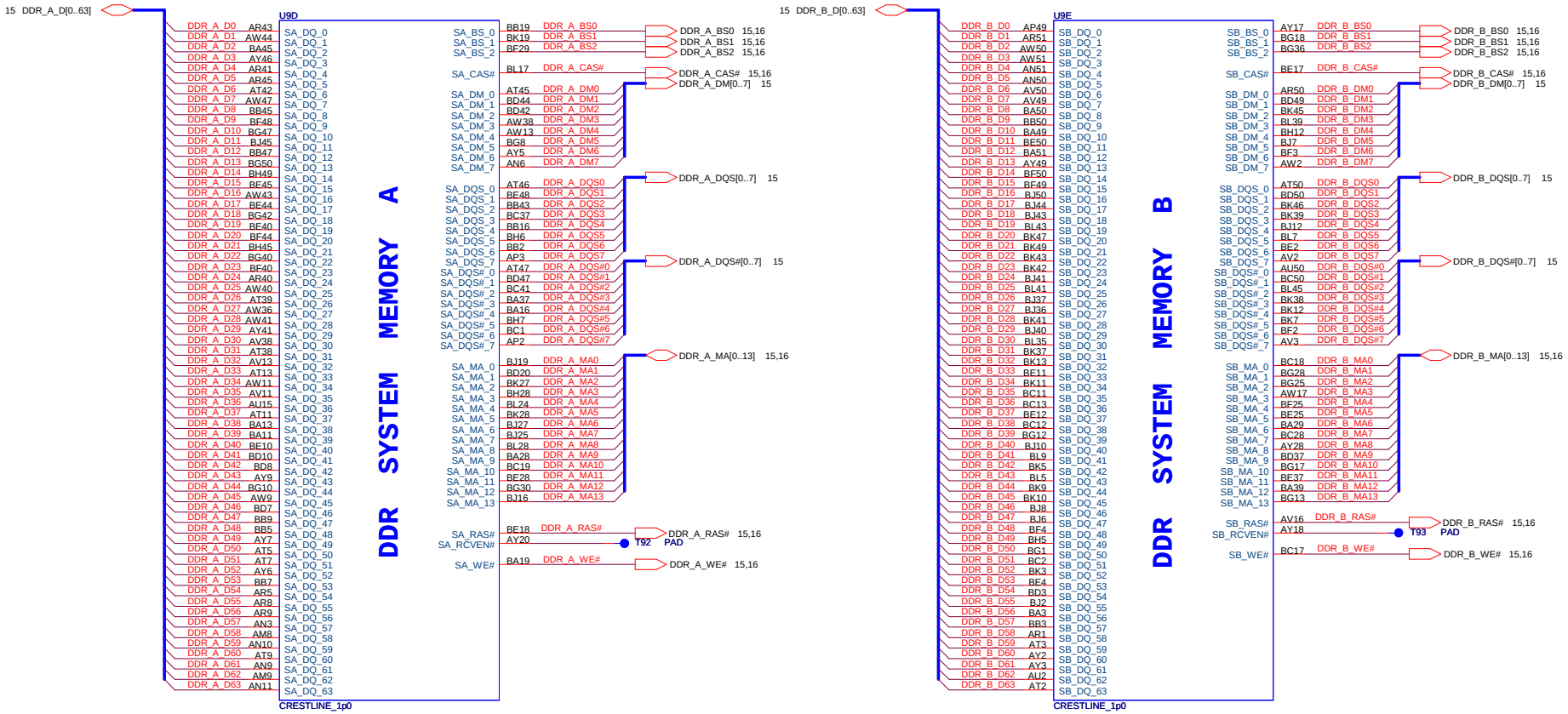


Title	Crestline (HOST)
Size	Document Number DM6 — Rev 1A
Date:	Thursday, August 02, 2007 — Sheet 5 of 52

QUANTA COMPUTER

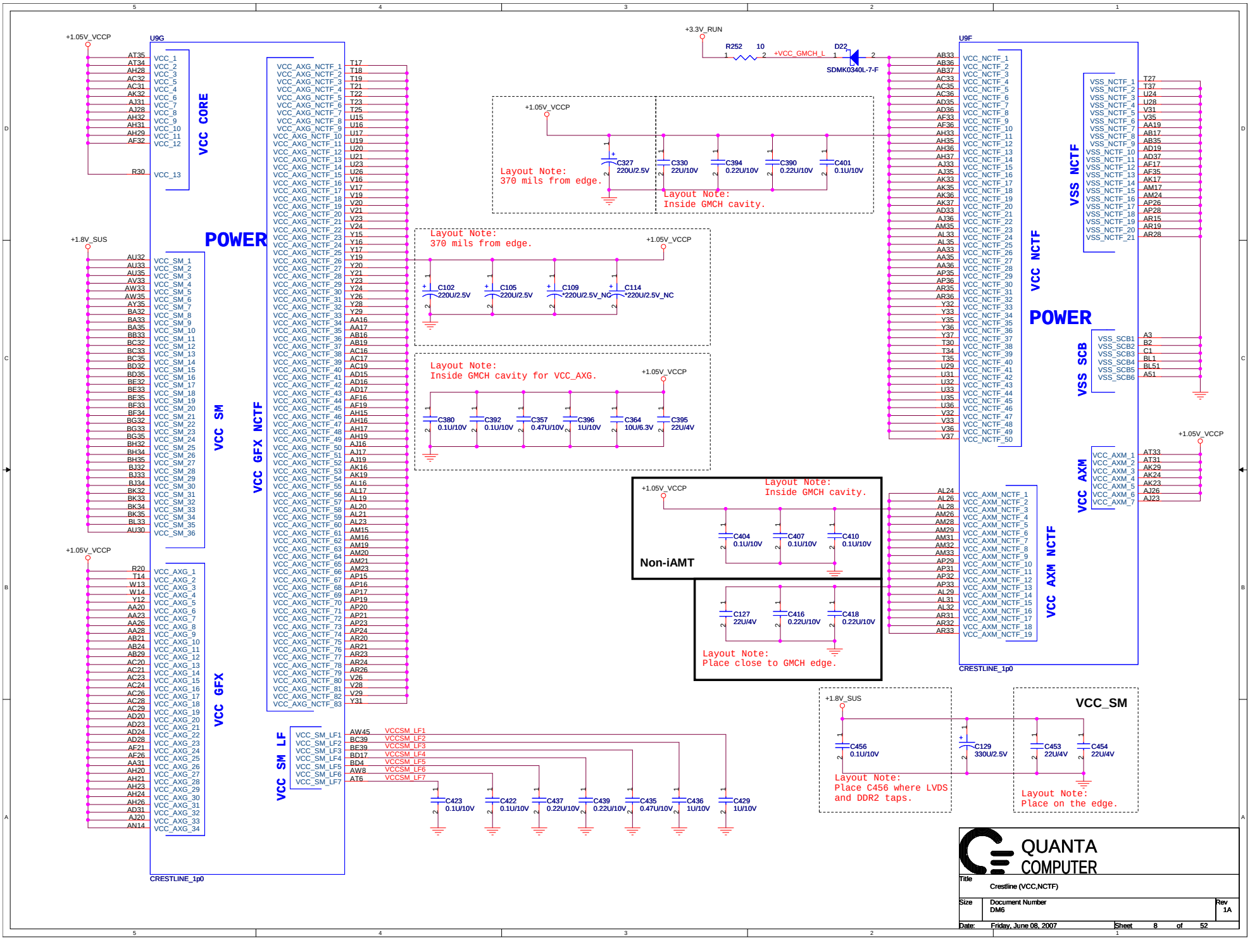


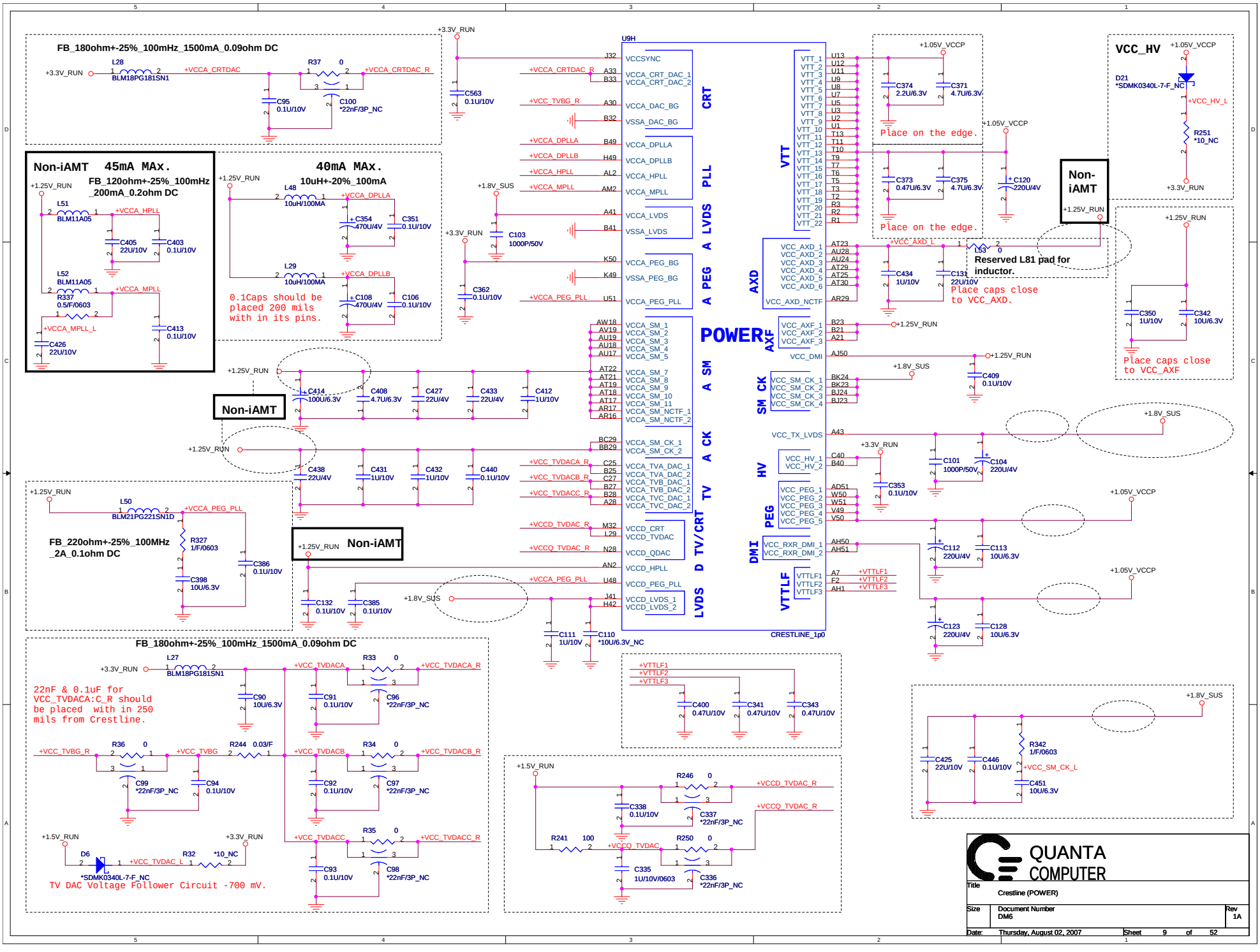
CFG5	DMI X2 Select	Low=DMIx2 High=DMIx4(Default)
CFG9	PCI Express Graphic Lane	Low= Reveise Lane High=Normal operation
CFG16	FSB Dynamic ODT	Low=Dynamic ODT Disable High=Dynamic ODT Enable(default).
CFG19	DMI Lane Reversal	Low=Normal(default). High=Lane Reversed
CFG20	SDVO/PCIE Concurrent Operation	Low=Only SDVO or PCIEx1 is operational (defaults) High=SDVO and PCIEx1 are operating simultaneously via PEG port
SDVO_CRTL_DATA	SDVO Present.	Low=No SDVO Device Present (default) High=SDVO Device Present

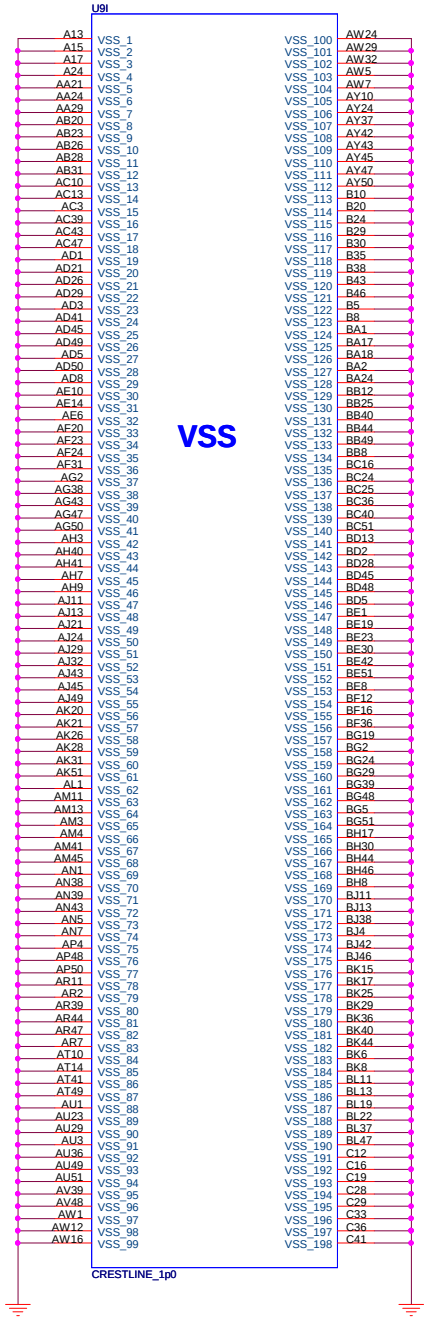


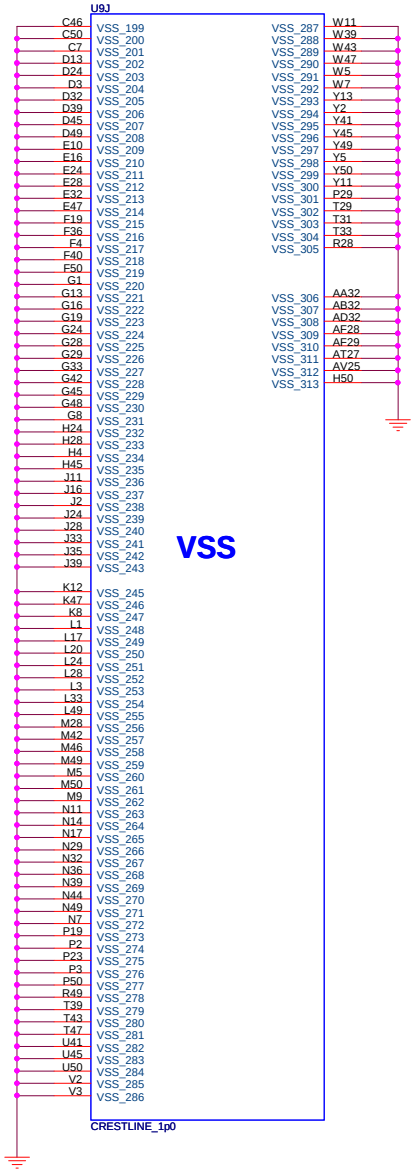
QUANTA COMPUTER

Title	Crestline (DDR2)	
Size	Document Number DM6	Rev 1A
Date: Friday, June 08, 2007	Sheet 7 of 52	


U9G
POWER
VCC CORE
VCC SM
VCC GFX NCTF
VCC GFX
VCC SM LF
CRESTLINE_1p0
+1.05V_VCCP
+1.8V_SUS
+3.3V_RUN
R252 10
D22
SDMK0340L-7-F
+VCC_GMCH_L
U9F
VCC NCTF
VSS NCTF
VSS SCB
VCC AXM
VCC AXM NCTF
CRESTLINE_1p0
Layout Note:
370 mils from edge.
Layout Note:
Inside GMCH cavity.
Layout Note:
Inside GMCH cavity for VCC_AXG.
Non-iAMT
Layout Note:
Place close to GMCH edge.
Layout Note:
Place C456 where LVDS
and DDR2 taps.
Layout Note:
Place on the edge.
VCC_SM
C327 220U/2.5V
C330 22U/10V
C394 0.22U/10V
C390 0.22U/10V
C401 0.1U/10V
C102 220U/2.5V
C105 220U/2.5V
C109 *220U/2.5V_NC
C114 *220U/2.5V_NC
C380 0.1U/10V
C392 0.1U/10V
C357 0.47U/10V
C396 1U/10V
C364 10U/6.3V
C395 22U/4V
C404 0.1U/10V
C407 0.1U/10V
C410 0.1U/10V
C127 22U/4V
C416 0.22U/10V
C418 0.22U/10V
C456 0.1U/10V
C129 330U/2.5V
C453 22U/4V
C454 22U/4V
C423 0.1U/10V
C422 0.1U/10V
C437 0.22U/10V
C439 0.22U/10V
C435 0.47U/10V
C436 1U/10V
C429 1U/10V
QUANTA COMPUTER
Title
Crestline (VCC,NCTF)
Size
Document Number
DM6
Rev
1A
Date:
Friday, June 08, 2007
Sheet
8
of
52

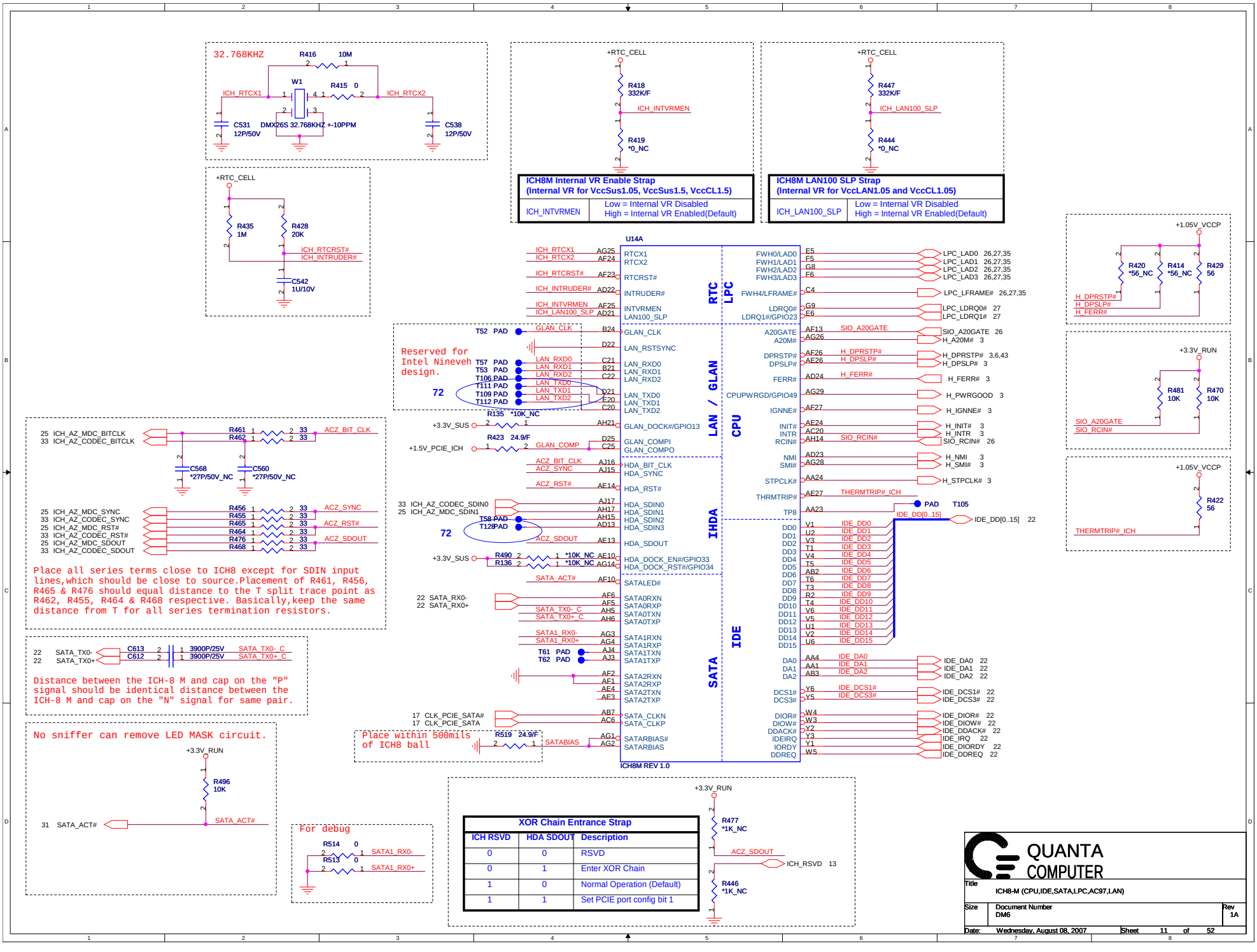

FB_180ohm+-25%_100mHz_1500mA_0.09ohm DC
Non-iAMT 45mA MAx.
FB_120ohm+-25%_100mHz_200mA_0.2ohm DC
40mA MAx.
10uH+-20%_100mA
0.1Caps should be placed 200 mils with in its pins.
Non-iAMT
FB_220ohm+-25%_100MHz_2A_0.1ohm DC
FB_180ohm+-25%_100mHz_1500mA_0.09ohm DC
22nF & 0.1uF for VCC_TVDACA:C_R should be placed with in 250 mils from Crestline.
TV DAC Voltage Follower Circuit -700 mV.
U9H
POWER
CRESTLINE_1p0
Place on the edge.
Place on the edge.
Reserved L81 pad for inductor.
Place caps close to VCC_AXD.
Place caps close to VCC_AXF
VCC_HV
Non-iAMT
Non-iAMT
QUANTA COMPUTER
Crestline (POWER)
Document Number DM6
Rev 1A
Thursday, August 02, 2007
Sheet 9 of 52





QUANTA COMPUTER

Title	Crestline (VSS)		
Size	Document Number DM6		Rev 1A
Date:	Friday, June 08, 2007	Sheet 10 of 52	


32.768KHZ
R416 10M
W1
R415 0
ICH_RTCX1
ICH_RTCX2
C531 12P/50V
DMX26S 32.768KHZ +-10PPM
C538 12P/50V
+RTC_CELL
R435 1M
R428 20K
ICH_RTCRST#
ICH_INTRUDER#
C542 1U/10V
R418 332K/F
ICH_INTVRMEN
R419 *0_NC
ICH8M Internal VR Enable Strap
(Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)
ICH_INTVRMEN
Low = Internal VR Disabled
High = Internal VR Enabled(Default)
R447 332K/F
ICH_LAN100_SLP
R444 *0_NC
ICH8M LAN100 SLP Strap
(Internal VR for VccLAN1.05 and VccCL1.05)
ICH_LAN100_SLP
Low = Internal VR Disabled
High = Internal VR Enabled(Default)
U14A
RTC
LPC
LAN / GLAN
CPU
IHDA
SATA
IDE
ICH8M REV 1.0
Reserved for Intel Nineveh design.
72
72
Place all series terms close to ICH8 except for SDIN input lines,which should be close to source.Placement of R461, R456, R465 & R476 should equal distance to the T split trace point as R462, R455, R464 & R468 respective. Basically,keep the same distance from T for all series termination resistors.
Distance between the ICH-8 M and cap on the "P" signal should be identical distance between the ICH-8 M and cap on the "N" signal for same pair.
No sniffer can remove LED MASK circuit.
Place within 500mils of ICH8 ball
For debug
XOR Chain Entrance Strap
ICH RSVD
HDA SDOUT
Description
0 0 RSVD
0 1 Enter XOR Chain
1 0 Normal Operation (Default)
1 1 Set PCIE port config bit 1
QUANTA COMPUTER
Title
ICH8-M (CPU,IDE,SATA,LPC,AC97,LAN)
Size
Document Number
DM6
Rev
1A
Date: Wednesday, August 08, 2007
Sheet 11 of 52

Place TX DC blocking caps close ICH8.

24 PCIE_TX2-
24 PCIE_TX2+
C524 1 2 0.1U/10V PCIE_TXN2_C
C529 1 2 0.1U/10V PCIE_TXP2_C

35 PCIE_TX6-/GLAN_TX-
35 PCIE_TX6+/GLAN_TX+
C523 1 2 0.1U/10V GLAN_TXN_C
C528 1 2 0.1U/10V GLAN_TXP_C

5

24 PCIE_RX2-
24 PCIE_RX2+
MiniWLAN
PCIE_TXN2_C
PCIE_TXP2_C

2

35 PCIE_RX6-/GLAN_RX-
35 PCIE_RX6+/GLAN_RX+
Giga Bit LOM
GLAN_TXN_C
GLAN_TXP_C

U14D

PCI-Express Direct Media Interface

PERN1 PERP1 PETN1 PETP1
PERN2 PERP2 PETN2 PETP2
PERN3 PERP3 PETN3 PETP3
PERN4 PERP4 PETN4 PETP4
PERN5 PERP5 PETN5 PETP5
PERN6/GLAN_RXN PERP6/GLAN_RXP PETN6/GLAN_TXN PETP6/GLAN_TXP

DMI0RXN DMI0RXP DMI0TXN DMI0TXP
DMI_MTX_IRX_N0 6
DMI_MTX_IRX_P0 6
DMI_MRX_ITX_N0 6
DMI_MRX_ITX_P0 6

DMI1RXN DMI1RXP DMI1TXN DMI1TXP
DMI_MTX_IRX_N1 6
DMI_MTX_IRX_P1 6
DMI_MRX_ITX_N1 6
DMI_MRX_ITX_P1 6

DMI2RXN DMI2RXP DMI2TXN DMI2TXP
DMI_MTX_IRX_N2 6
DMI_MTX_IRX_P2 6
DMI_MRX_ITX_N2 6
DMI_MRX_ITX_P2 6

DMI3RXN DMI3RXP DMI3TXN DMI3TXP
DMI_MTX_IRX_N3 6
DMI_MTX_IRX_P3 6
DMI_MRX_ITX_N3 6
DMI_MRX_ITX_P3 6

DMI_CLKN DMI_CLKP
CLK_PCIE_ICH# 17
CLK_PCIE_ICH 17

DMI_ZCOMP DMI_IRCOMP
DMI_COMP
R442 24.9/F
+1.5V_PCIE_ICH
Place within 500mils of ICH8

SPI

SPI_CLK SPI_CS0# SPI_CS1#
SPI_MOSI SPI_MISO

Layout Note:
Place R438, R431 within 500 mils from ICH.

26 ICH_EC_SPI_CLK
R438 1 2 15
ICH_EC_SPI_CLK_R
ICH_SPI_CS#
ICH_SPI_CS1#_R

26 ICH_EC_SPI_DO
26 ICH_EC_SPI_DIN
R431 1 2 15
ICH_EC_SPI_DO_R

USB

OC0# OC1#/GPIO40 OC2#/GPIO41 OC3#/GPIO42 OC4#/GPIO43 OC5#/GPIO29 OC6#/GPIO30 OC7#/GPIO31 OC8# OC9#

31 USB_OC0_1#
USB_OC0_1#
31 USB_OC2_3#
USB_OC2_3#

USBP0N USBP0P USBP1N USBP1P USBP2N USBP2P USBP3N USBP3P USBP4N USBP4P USBP5N USBP5P USBP6N USBP6P USBP7N USBP7P USBP8N USBP8P USBP9N USBP9P

ICH_USBP0- 31
ICH_USBP0+ 31
ICH_USBP1- 31
ICH_USBP1+ 31
ICH_USBP2- 31
ICH_USBP2+ 31
ICH_USBP3- 31
ICH_USBP3+ 31
ICH_USBP4- 22
ICH_USBP4+ 22
PAD T133
PAD T136
ICH_USBP6- 23
ICH_USBP6+ 23
ICH_USBP7- 30
ICH_USBP7+ 30
ICH_USBP8- 37
ICH_USBP8+ 37
ICH_USBP9- 24
ICH_USBP9+ 24

Ext Side Top
Ext Side Bottom
Rear Top
Rear Bottom
Floppy ODD
Biometric
New Card
Blue Tooth
Dock
WLAN

USBRBIAS# USBRBIAS
USBRBIAS
R506 22.6/F
Short F2 and F3 at the package and keep length to less than 500mils. Trace Impedance should be 60ohms +/- 15%.

ICH8M REV 1.0

+3.3V_ALW
U13
R408 *15_NC
R130 0 *87SH08_NC
R413 15
SPI_CS0#
ICH_SPI_CS#
SIO_SPI_CS# 26

Non-iAMT
RP48 10P8R-10K
+3.3V_SUS
OC6# OC4# OC5# OC7#
OC8# USB_OC2_3# USB_OC0_1# OC9#

PCI Pullups
RP42 RP47 RP46 10P8R-8.2K
+3.3V_RUN
PCI_STOP# PCI_REQ1# PCI_FRAME#
PCI_PIRQD# PCI_DEVSEL# ICH_GPIO2_PIRQE# PCI_TRDY# PCI_SERR#
PCI_PIRQA# PCI_PIRQC# PCI_PERR# PCI_PIRQB# PCI_REQ0# PCI_PLOCK# PCI_IRDY#

Del WWAN Noise - ICH improvements on 0525

5

U14B

PCI

AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7 AD8 AD9 AD10 AD11 AD12 AD13 AD14 AD15 AD16 AD17 AD18 AD19 AD20 AD21 AD22 AD23 AD24 AD25 AD26 AD27 AD28 AD29 AD30 AD31

23 PCI_AD[0..31]

REQ0# GNT0# REQ1#/GPIO50 GNT1#/GPIO51 REQ2#/GPIO52 GNT2#/GPIO53 REQ3#/GPIO54 GNT3#/GPIO55
PCI_REQ0# PCI_GNT0# PCI_REQ1# PCI_GNT1# SB_WWAN_PCIE_RST# PCI_GNT2# SB_LOM_PCIE_RST# PCI_GNT3#
PCI_REQ1# 23
PCI_GNT1# 23
PAD T122
SB_LOM_PCIE_RST# 35
PAD T124

C/BE0# C/BE1# C/BE2# C/BE3#
PCI_C_BE0# 23
PCI_C_BE1# 23
PCI_C_BE2# 23
PCI_C_BE3# 23

IRDY# PAR PCIRST# DEVSEL# PERR# PLOCK# SERR# STOP# TRDY# FRAME#
PCI_IRDY# 23
PCI_PAR 23
PCI_RST#_G
PCI_DEVSEL# 23
PCI_PERR# 23
PCI_PLOCK# 23
PCI_SERR# 23
PCI_STOP# 23
PCI_TRDY# 23
PCI_FRAME# 23

PLTRST# PCICLK PME#
PCI_PLTRST#
CLK_PCI_ICH
CLK_PCI_ICH 17
ICH_PME# 27

Interrupt I/F

PIRQA# PIRQB# PIRQC# PIRQD#
PIRQE#/GPIO2 PIRQF#/GPIO3 PIRQG#/GPIO4 PIRQH#/GPIO5
ICH_GPIO2_PIRQE#
SB_WLAN_PCIE_RST#
SB_NB_PCIE_RST#
PCIE_MCARD2_DET#
SB_WLAN_PCIE_RST# 24
SB_NB_PCIE_RST# 6

3
23 PCI_PIRQD#
PCI_PIRQA# PCI_PIRQB# PCI_PIRQC# PCI_PIRQD#

5
R147 2 1 100K +3.3V_RUN

ICH8M REV 1.0

R505 1K
R430 *1K_NC
ICH_SPI_CS1#_R
PCI_GNT0#

Boot BIOS Strap

		GNT0#	SPI_CS1#
LPC	11	No stuff	No stuff
PCI	10	No stuff	Stuff
SPI	01	Stuff	No stuff

SB_WWAN_PCIE_RST# R448 2 1 20K
SB_WLAN_PCIE_RST# R463 2 1 20K
SB_LOM_PCIE_RST# R137 2 1 20K
SB_NB_PCIE_RST# R474 2 1 20K
BIOS should not enable the internal GPIO pull up resistor.

PCI_GNT3#
R466 *1K_NC

A16 away override strap.

SB_NB_PCIE_RST#	Low = A16 swap override enabled. High = Default.

Non-iAMT
+3.3V_SUS
C517 0.047U/10V
U27 7SH32
PCI_RST# G
PCI_RST# 23
Add Buffers as needed for Loading and fanout concerns.

C516 0.047U/10V
U28 7SH32
PCI_PLTRST#
PLTRST# 6,18,24,26,27,35

DOCK	REQ0	GNT0	PIRQA
Cardbus or Cardbus/1394	REQ1	GNT1	PIRQD
1394/MediaCard	REQ2	GNT2	PIRQC PIRQD

CLK_PCI_ICH
R480 *10_NC
C213 *8.2P/16V_NC
Reserved for EMI.Place resister and cap close to ICH.

QUANTA COMPUTER

Title	ICH8-M (USB,DMI,PCIE,PCI)	
Size	Document Number DM6	Rev 1A
Date: Friday, June 08, 2007	Sheet 12 of 52	

Non-iAMT

+3.3V_SUS

RP45 4P2R-2.2K: 1 ICH_SMBDATA, 2 ICH_SMBDATA, 3 ICH_SMBCLK, 4 ICH_SMBCLK

Non-iAMT

+3.3V_SUS

R445 *10K_NC RSV_ICH_CL_RST1#
R454 10K ICH_RI#
R441 10K SIO_EXT_SCI#
R460 1K ICH_PCIE_WAKE#

Non-iAMT ASF 2.0

+3.3V_SUS

RP44 4P2R-10K_NC: 1 ICH_SMLINK0, 2 ICH_SMLINK0, 3 ICH_SMLINK1, 4 ICH_SMLINK1

ICH_SMBCLK R469 0 ICH_SMLINK0
ICH_SMBDATA R459 0 ICH_SMLINK1

+3.3V_RUN

R491 8.2K
CLKRUN#
R487 *10_NC

Option to " Disable " clkrun. Pulling it down will keep the clks running.

U14C

ICH8M REV 1.0

SMB: SMBCLK AJ26, SMBDATA AD19, LINKALERT# AG21, SMLINK0 AC17, SMLINK1 AE19
SATA GPIO: SATA0GP/GPIO21 AJ12, SATA1GP/GPIO19 AJ10, SATA2GP/GPIO36 AF11, SATA3GP/GPIO37 AG11
Clocks: CLK14 AG9, CLK48 G5, SUSCLK D3
SYS GPIO: RI# AF17, SUS_STAT#/LPCPD# F4, SYS_RESET# AD15, BMBUSY#/GPIO0 AG12, SMBALERT#/GPIO11 AG22, STP_PCI#/GPIO15 AE20, STP_CPU#/GPIO25 AG18, CLKRUN#/GPIO32 AH11, WAKE# AE17, SERIRQ AE12, THRM# AC13, VRMPWRGD AJ20, TP7 AJ22
Power MGT: S4_STATE#/GPIO26 AH27, PWROK AE23, DPRSLPVR/GPIO16 AJ14, BATLOW# AE21, PWRBTN# C2, LAN_RST# AH20, RSMRST# AG27, CK_PWRGD E1, CLPWROK E3, SLP_M# AJ25
GPIO: TACH1/GPIO1 AJ8, TACH2/GPIO6 AJ9, TACH3/GPIO7 AH9, GPIO8 AE16, GPIO12 AC19, TACH0/GPIO17 AG8, GPIO18 AH12, GPIO20 AE11, SCLOCK/GPIO22 AG10, QRT_STATE0/GPIO27 AH25, QRT_STATE1/GPIO28 AD16, SATACLKREQ#/GPIO35 AG13, SLOAD/GPIO38 AF9, SDATAOUT0/GPIO39 AJ11, SDATAOUT1/GPIO48 AD10
Controller Link: CL_CLK0 F23, CL_CLK1 AE18, CL_DATA0 F22, CL_DATA1 AF19, CL_VREF0 D24, CL_VREF1 AH23, CL_RST# AJ23
MISC: SPKR AD9, MCH_SYNC# AJ13, TP3 AJ21
MEM_LED/GPIO24 AJ27, ME_EC_ALERT/GPIO10 AJ24, EC_ME_ALERT/GPIO14 AF22, WOL_EN/GPIO9 AG19

24,35 ICH_SMBCLK
24,35 ICH_SMBDATA
T115 PAD
T126 PAD
T116 PAD
71
T134 PAD
3,27 ITP_DBRESET#
6 PM_BMBUSY#
26,35 LOM_SMB_ALERT# R440 *0_NC
17 H_STP_PCI#
17 H_STP_CPU#
23,26,27 CLKRUN#
27 ICH_PCIE_WAKE#
23,26,27,35 IRQ_SERIRQ
T127 PAD
26,38,43 IMVP_PWRGD
T55 PAD
22 USB_IDE#
T60 PAD
27 SIO_EXT_WAKE#
26 SIO_EXT_SMI#
26 SIO_EXT_SCI#
24 PCIE_MCARD1_DET#
24 USB_MCARD1_DET# R141 4.7K
T130 PAD
T104 PAD
22 IDE_RST_MOD
17 SATA_CLKREQ#
PLTRST_DELAY#
T59 PAD
T132 PAD
33 SPKR
6 MCH_ICH_SYNC# R138 0 MCH_ICH_SYNC#_R
11 ICH_RSVD

ICH_SMBCLK
ICH_SMBDATA
RSV_ICH_CL_RST1#
ICH_SMLINK0
ICH_SMLINK1
ICH_RI#
RSV_LPCPD#
LOM_ICH_SMBALERT#
CLKRUN#
ICH_PCIE_WAKE#
IRQ_SERIRQ
RSV_THRM#
IMVP_PWRGD
RSVD_GPIO6
SIO_EXT_WAKE#
SIO_EXT_SMI#
SIO_EXT_SCI#
PCIE_MCARD1_DET#
USB_MCARD1_R_DET#
USB_MCARD2_DET#
RSV_GPIO27
PLTRST_DELAY#
RSVD_GPIO39
RSVD_GPIO48
SPKR

+3.3V_RUN

R498 *10K_NC PLTRST_DELAY#

+3.3V_RUN

R129 *2.2K_NC IMVP_PWRGD

+3.3V_RUN

R475 10K RSV_THRM#
R485 *10K_NC MCH_ICH_SYNC#_R
R143 10K IRQ_SERIRQ
R145 10K RSVD_GPIO6
R144 10K RSVD_GPIO39
R497 10K RSVD_GPIO48
R148 100K PCIE_MCARD1_DET#
R142 100K USB_MCARD1_R_DET#
R146 100K USB_MCARD2_DET#

+3.3V_SUS

R458 10K SIO_EXT_SMI#
R432 10K LOM_ICH_SMBALERT#
R133 *10K_NC RSV_GPIO27
R449 10K RSV_WOL_EN

+3.3V_RUN

R504 *1K_NC SPKR

No Reboot strap.	
SPKR	Low = Default. High = No Reboot.

SMbus address D2

These are for backdrive issue.

+3.3V_RUN

RP43 4P2R-2.2K

24,35 ICH_SMBDATA — Q46 2N7002W-7-F — MEM_SDATA 15

+3.3V_RUN

24,35 ICH_SMBCLK — Q48 2N7002W-7-F — MEM_SCLK 15

Non-iAMT

+3.3V_RUN

R486 8.2K

CLK_ICH_14M
CLK_ICH_48M
SUSCLK
SLP_S3#
SLP_S4#
SLP_S5#
PWROK
DPRSLPVR
BATLOW#
PWRBTN#
LAN_RST#
RSMRST#
CK_PWRGD
CLPWROK
SLP_M#
CL_CLK0
CL_CLK1
CL_DATA0
CL_DATA1
CL_VREF0
CL_VREF1
CL_RST#
MEM_LED/GPIO24
ME_EC_ALERT/GPIO10
EC_ME_ALERT/GPIO14
WOL_EN/GPIO9

CLK_ICH_14M 17
CLK_ICH_48M 17
ICH_SUSCLK — PAD T135
SIO_SLP_S3# 26 — PAD T119
SIO_SLP_S5# 26
RSV_GPIO26 — PAD T102
ICH_PWRGD 6,38
DPRSLPVR 6,43
R443 8.2K +3.3V_SUS
SIO_PWRBTN# 26 — PAD T56
RSV_ICH_LAN_RST#
ICH_RSMRST# 26
CK_PWRGD 17
ICH_CL_PWROK 6,26 — PAD T103
CL_CLK0 6 — PAD T123
RSV_ICH_CL_DATA1 — PAD T118
71
CL_VREF1 — PAD T110
ICH_CL_RST0# 6
RSV_GPIO24 — PAD T101
RSV_GPIO10 — PAD T54
RSV_GPIO14 — PAD T114
RSV_WOL_EN — PAD T125

R453 8.2K +3.3V_SUS

UMA Package:RC0402-C
Discrete Package: RC0402

Non-iAMT

ICH_PWRGD R436 10K
DPRSLPVR R471 100K
ICH_RSMRST# R411 *10K_NC
RSV_ICH_LAN_RST# R457 10K
ICH_CL_PWROK R503 1M

+3.3V_SUS

RSV_GPIO26 R131 *10K_NC
RSV_GPIO24 R132 *10K_NC
RSV_GPIO10 R134 10K

Place these close to ICH8.

CLK_ICH_48M
R512 *10_NC
C610 *4.7P/50V_NC

CLK_ICH_14M
R499 *10_NC
C607 *4.7P/50V_NC

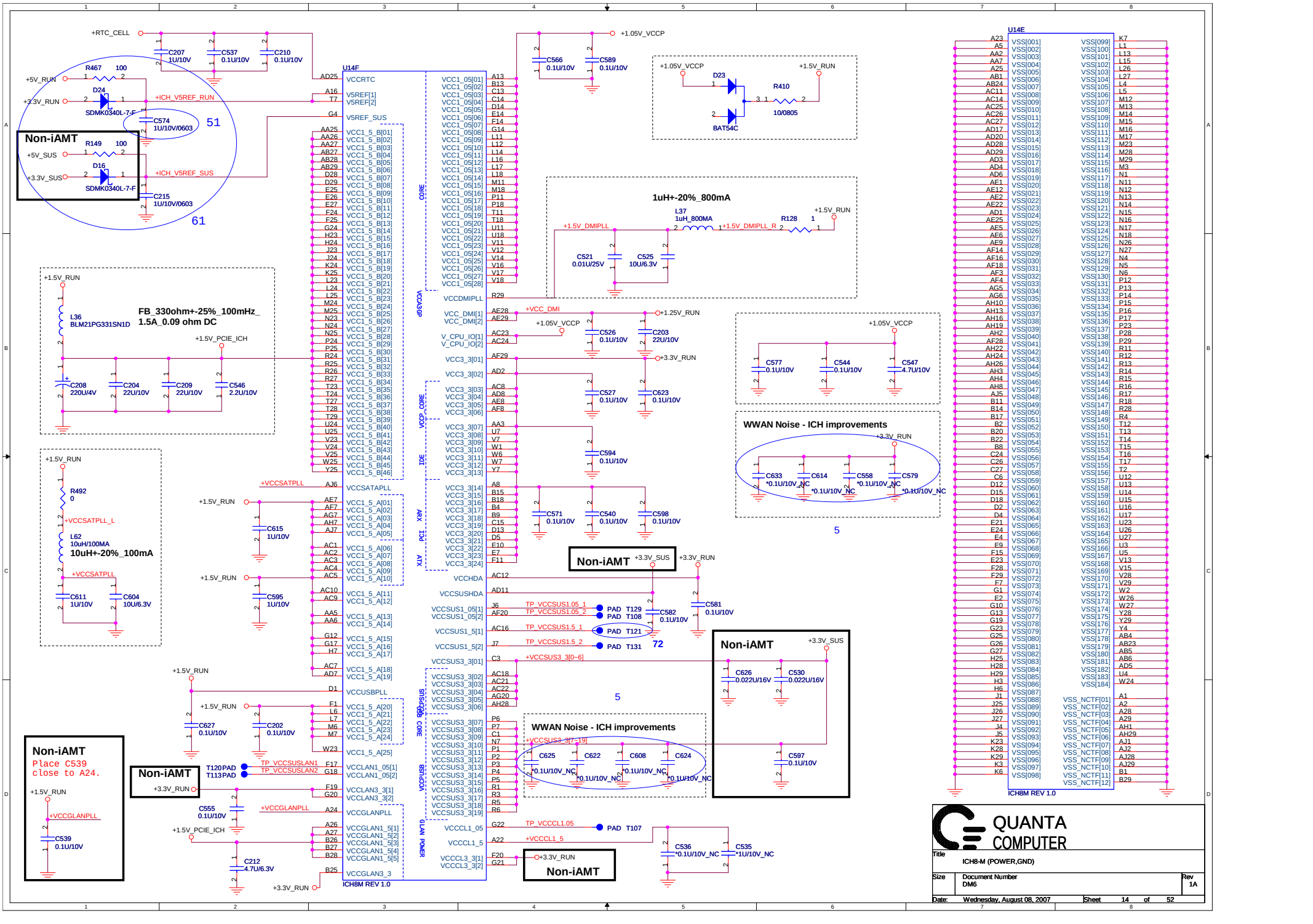
Non-iAMT

+3.3V_RUN +3.3V_ALW

R427 3.24K/F
R437 *3.24K/F_NC
CL_VREF0
CL_VREF1
C541 0.1U/10V
R426 453/F
C550 *0.1U/10V_NC
R433 *453/F_NC

QUANTA COMPUTER

Title	ICH8-M (PM,GPIO,SMB,CL)		
Size	Document Number DM6		Rev 1A
Date:	Wednesday, August 08, 2007	Sheet 13 of 52	


+RTC_CELL
C207 1U/10V
C537 0.1U/10V
C210 0.1U/10V
R467 100
+5V_RUN
+3.3V_RUN
D24
SDMK0340L-7-F
+ICH_V5REF_RUN
C574 1U/10V/0603
51
Non-iAMT
R149 100
+5V_SUS
+3.3V_SUS
D16
SDMK0340L-7-F
+ICH_V5REF_SUS
C215 1U/10V/0603
61
U14F
VCCRTC
V5REF[1]
V5REF[2]
V5REF_SUS
VCC1_5_B[01]
VCC1_5_B[02]
VCC1_5_B[03]
VCC1_5_B[04]
VCC1_5_B[05]
VCC1_5_B[06]
VCC1_5_B[07]
VCC1_5_B[08]
VCC1_5_B[09]
VCC1_5_B[10]
VCC1_5_B[11]
VCC1_5_B[12]
VCC1_5_B[13]
VCC1_5_B[14]
VCC1_5_B[15]
VCC1_5_B[16]
VCC1_5_B[17]
VCC1_5_B[18]
VCC1_5_B[19]
VCC1_5_B[20]
VCC1_5_B[21]
VCC1_5_B[22]
VCC1_5_B[23]
VCC1_5_B[24]
VCC1_5_B[25]
VCC1_5_B[26]
VCC1_5_B[27]
VCC1_5_B[28]
VCC1_5_B[29]
VCC1_5_B[30]
VCC1_5_B[31]
VCC1_5_B[32]
VCC1_5_B[33]
VCC1_5_B[34]
VCC1_5_B[35]
VCC1_5_B[36]
VCC1_5_B[37]
VCC1_5_B[38]
VCC1_5_B[39]
VCC1_5_B[40]
VCC1_5_B[41]
VCC1_5_B[42]
VCC1_5_B[43]
VCC1_5_B[44]
VCC1_5_B[45]
VCC1_5_B[46]
VCCSATAPLL
VCC1_5_A[01]
VCC1_5_A[02]
VCC1_5_A[03]
VCC1_5_A[04]
VCC1_5_A[05]
VCC1_5_A[06]
VCC1_5_A[07]
VCC1_5_A[08]
VCC1_5_A[09]
VCC1_5_A[10]
VCC1_5_A[11]
VCC1_5_A[12]
VCC1_5_A[13]
VCC1_5_A[14]
VCC1_5_A[15]
VCC1_5_A[16]
VCC1_5_A[17]
VCC1_5_A[18]
VCC1_5_A[19]
VCCUSBPLL
VCC1_5_A[20]
VCC1_5_A[21]
VCC1_5_A[22]
VCC1_5_A[23]
VCC1_5_A[24]
VCC1_5_A[25]
VCCLAN1_05[1]
VCCLAN1_05[2]
VCCLAN3_3[1]
VCCLAN3_3[2]
VCCGLANPLL
VCCGLAN1_5[1]
VCCGLAN1_5[2]
VCCGLAN1_5[3]
VCCGLAN1_5[4]
VCCGLAN1_5[5]
VCCGLAN3_3
ICH8M REV 1.0
VCC1_05[01]
VCC1_05[02]
VCC1_05[03]
VCC1_05[04]
VCC1_05[05]
VCC1_05[06]
VCC1_05[07]
VCC1_05[08]
VCC1_05[09]
VCC1_05[10]
VCC1_05[11]
VCC1_05[12]
VCC1_05[13]
VCC1_05[14]
VCC1_05[15]
VCC1_05[16]
VCC1_05[17]
VCC1_05[18]
VCC1_05[19]
VCC1_05[20]
VCC1_05[21]
VCC1_05[22]
VCC1_05[23]
VCC1_05[24]
VCC1_05[25]
VCC1_05[26]
VCC1_05[27]
VCC1_05[28]
VCCDMIPLL
VCC_DMI[1]
VCC_DMI[2]
V_CPU_IO[1]
V_CPU_IO[2]
VCC3_3[01]
VCC3_3[02]
VCC3_3[03]
VCC3_3[04]
VCC3_3[05]
VCC3_3[06]
VCC3_3[07]
VCC3_3[08]
VCC3_3[09]
VCC3_3[10]
VCC3_3[11]
VCC3_3[12]
VCC3_3[13]
VCC3_3[14]
VCC3_3[15]
VCC3_3[16]
VCC3_3[17]
VCC3_3[18]
VCC3_3[19]
VCC3_3[20]
VCC3_3[21]
VCC3_3[22]
VCC3_3[23]
VCC3_3[24]
VCCHDA
VCCSUSHDA
VCCSUS1_05[1]
VCCSUS1_05[2]
VCCSUS1_5[1]
VCCSUS1_5[2]
VCCSUS3_3[01]
VCCSUS3_3[02]
VCCSUS3_3[03]
VCCSUS3_3[04]
VCCSUS3_3[05]
VCCSUS3_3[06]
VCCSUS3_3[07]
VCCSUS3_3[08]
VCCSUS3_3[09]
VCCSUS3_3[10]
VCCSUS3_3[11]
VCCSUS3_3[12]
VCCSUS3_3[13]
VCCSUS3_3[14]
VCCSUS3_3[15]
VCCSUS3_3[16]
VCCSUS3_3[17]
VCCSUS3_3[18]
VCCSUS3_3[19]
VCCCL1_05
VCCCL1_5
VCCCL3_3[1]
VCCCL3_3[2]
VCC3.3DMIPLL
VCC3.3DCPA
VCC3.3DCPA
VCC3.3DCPA

A is required to route to Top SoDIMM for AMTto function. Ch.A SODIMM needs to be populated for Intel AMT support.

TOP

JDIM1

PC4800 DDR2 SDRAM SO-DIMM (200P)

TYC_1775804-2

CLOCK 0,1
CKE 0,1

BOT

JDIM2

PC4800 DDR2 SDRAM SO-DIMM (200P)

FOX_AS0A426-M2SN-7F

CLOCK 2,3
CKE 2,3

Non-iAMT

SMbus address A0

SMbus address A4

Place these Caps near So-Dimm1.

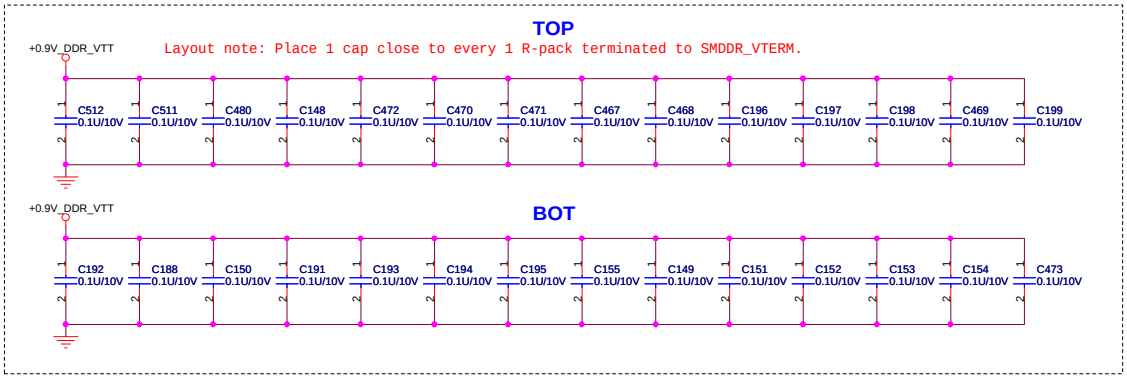
Place these Caps near So-Dimm2.

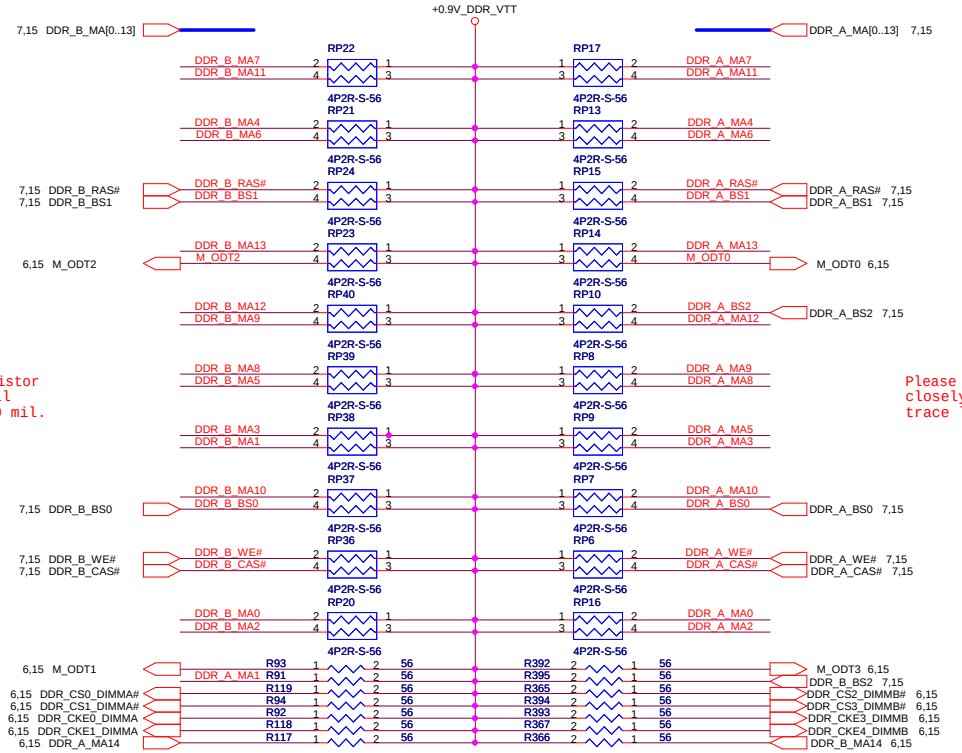
Place these Caps near So-Dimm1.

Place these Caps near So-Dimm2.

QUANTA COMPUTER

Title	DDR2 SO-DIMM (200P) X 2		
Size	Document Number DM6		Rev 1A
Date:	Wednesday, August 08, 2007	Sheet 15 of 52	



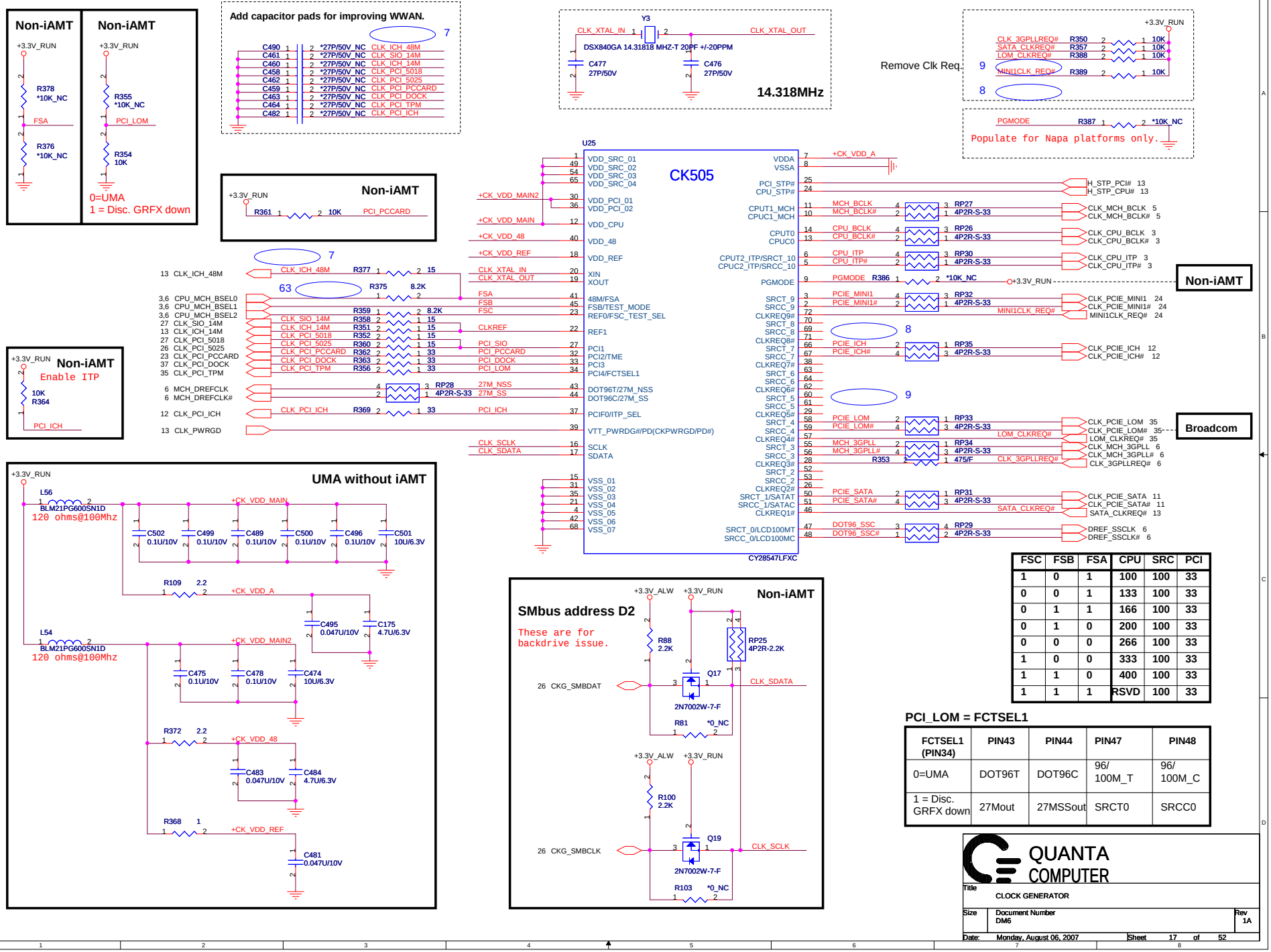


Please these resistor closely DIMMB,all trace length<750 mil.

Please these resistor closely DIMMA,all trace length<750 mil.

QUANTA COMPUTER

Title	DDR2 RES ARRAY	
Size	Document Number DM6	Rev 1A
Date: Friday, June 08, 2007	Sheet 16 of 52	



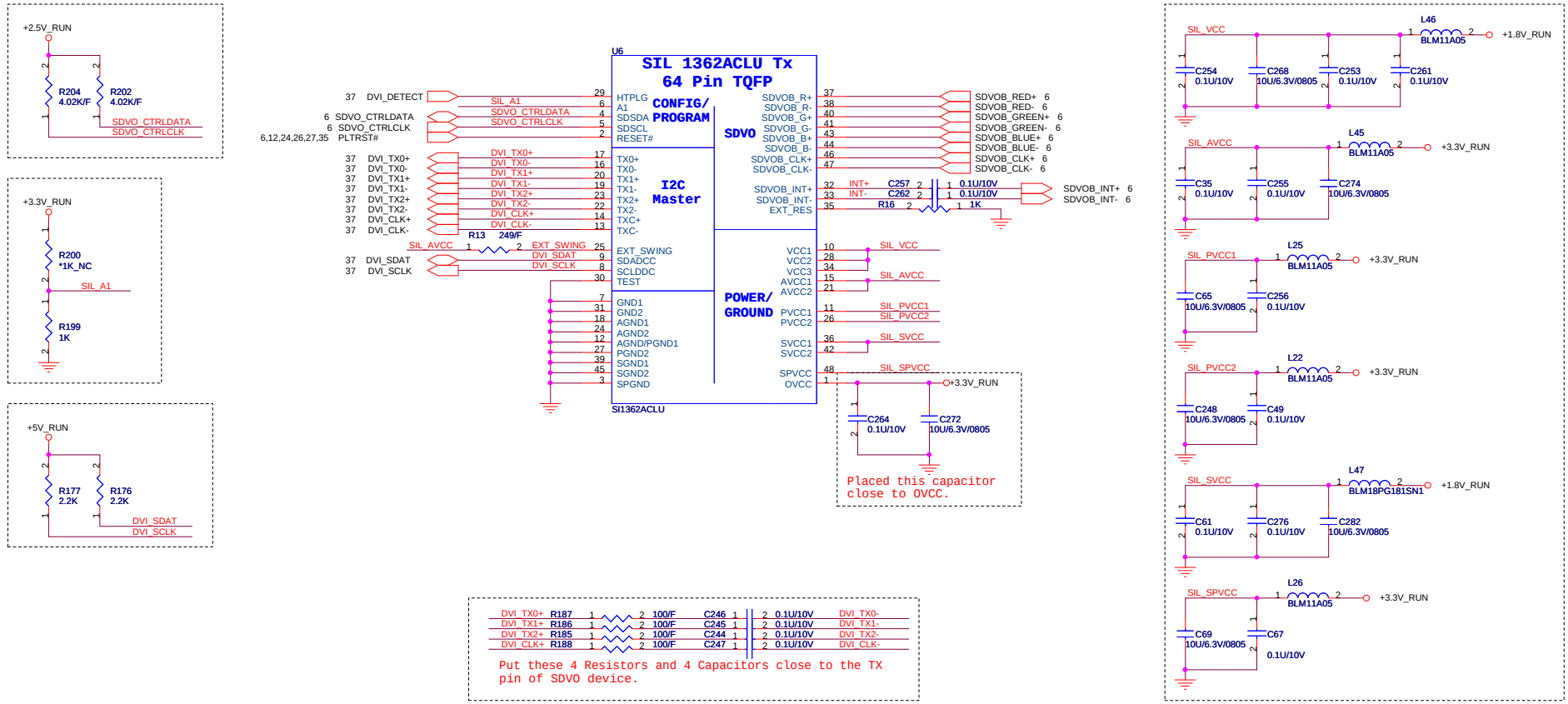
FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

PCI_LOM = FCTSEL1

FCTSEL1 (PIN34)	PIN43	PIN44	PIN47	PIN48
0=UMA	DOT96T	DOT96C	96/ 100M_T	96/ 100M_C
1 = Disc. GRFX down	27Mout	27MSSout	SRCT0	SRCC0

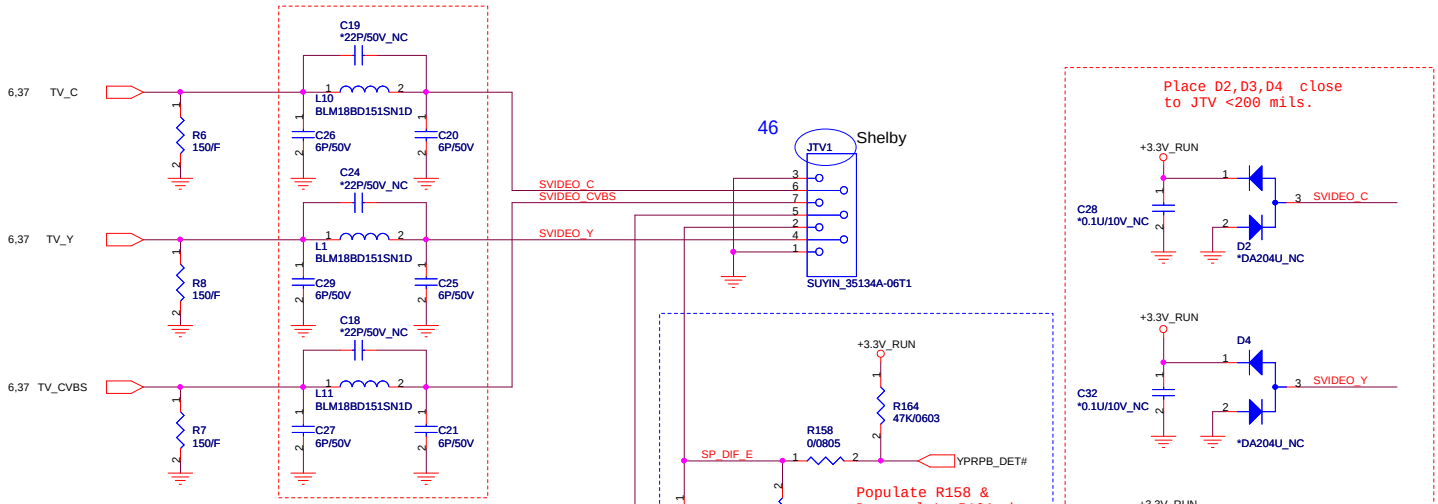
QUANTA COMPUTER

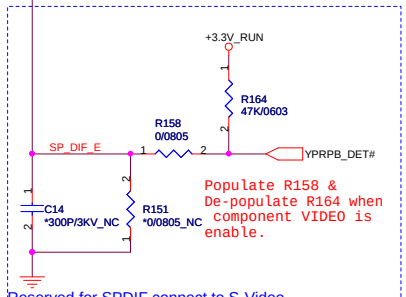
Title	CLOCK GENERATOR	
Size	Document Number DM6	Rev 1A
Date: Monday, August 06, 2007	Sheet 17 of 52	



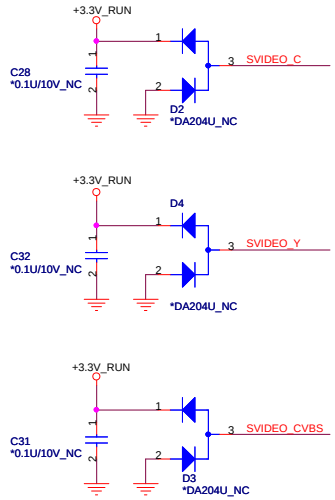
Title	Sil 1362		
Size	Document Number DM6		Rev 1A
Date:	Friday, June 08, 2007	Sheet 18 of 52	

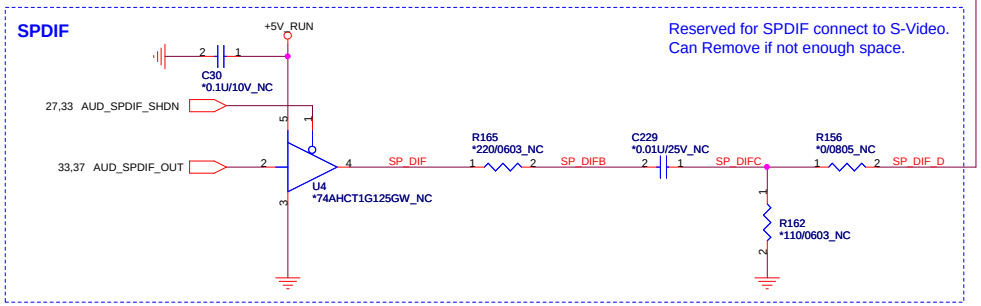
Place All of those
Inductors Caps close
to JTV1 <200 mils





Place D2,D3,D4 close
to JTV <200 mils.

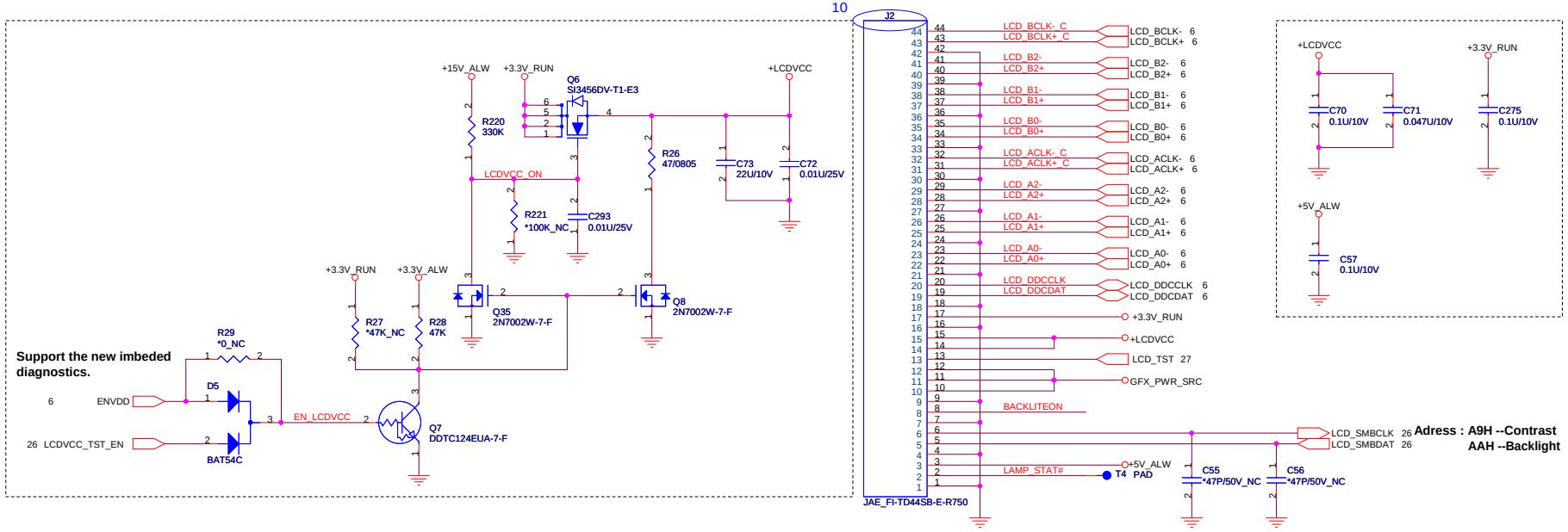




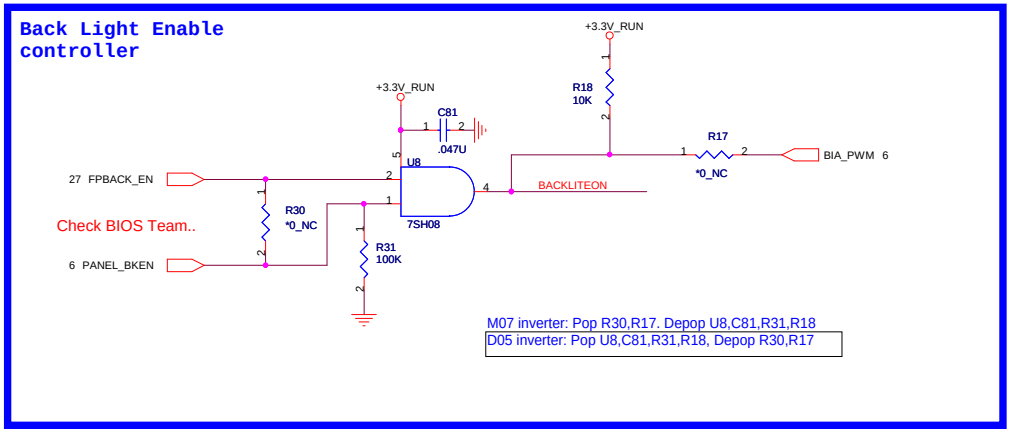
QUANTA COMPUTER

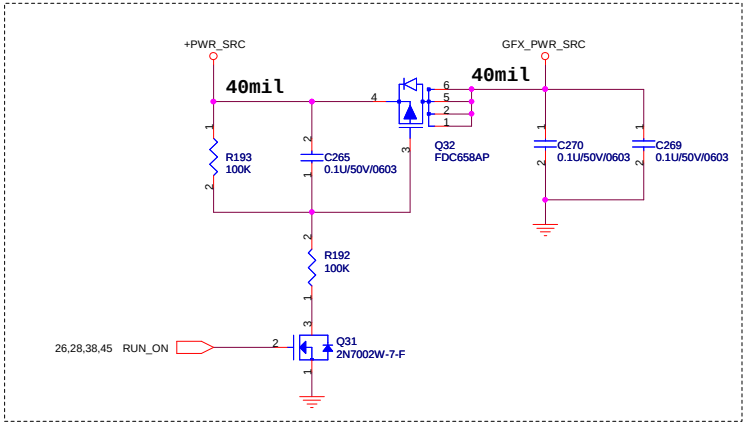
Title	S-Video CONN with SPDIF	
Size	Document Number DM6	Rev 1A
Date: Tuesday, August 07, 2007	Sheet 19 of 52	

10



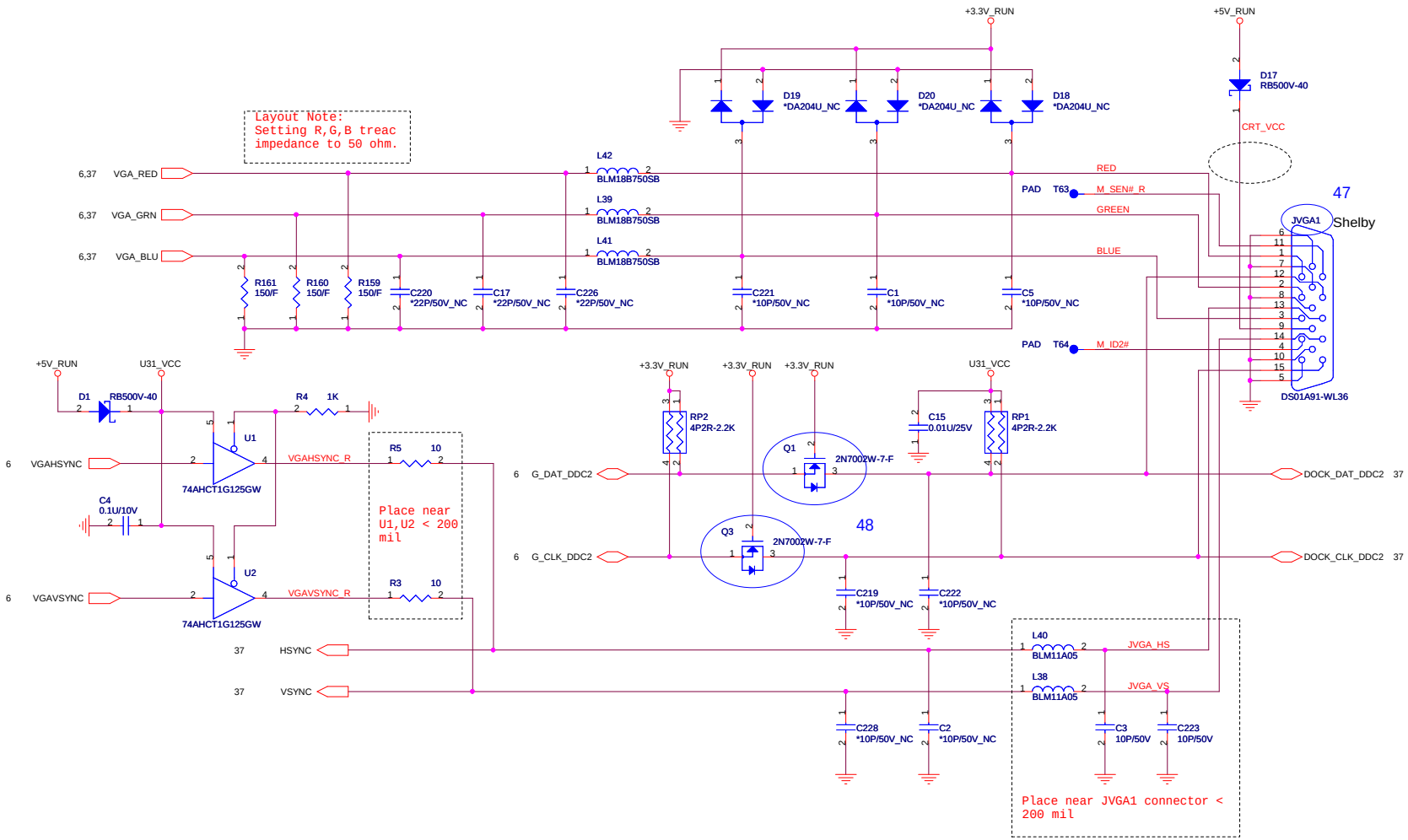
11





QUANTA COMPUTER

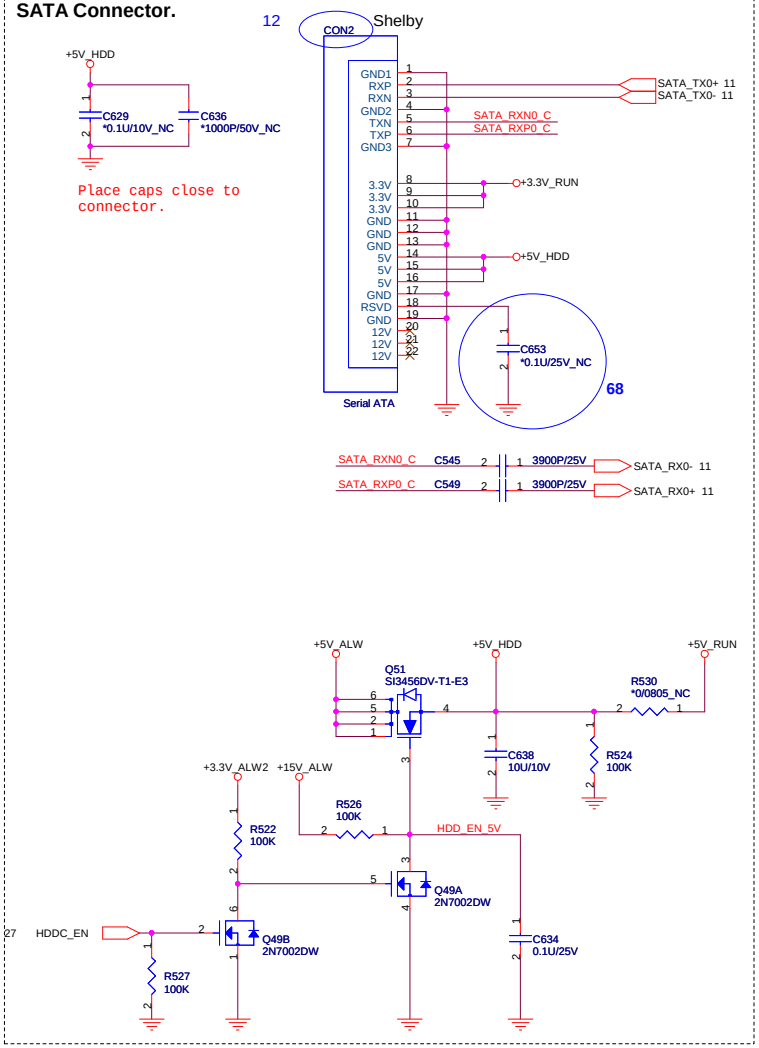
Title	LCD CONN & CK-SSCD	
Size	Document Number DM6	Rev 1A
Date: Wednesday, August 08, 2007	Sheet 20 of 52	



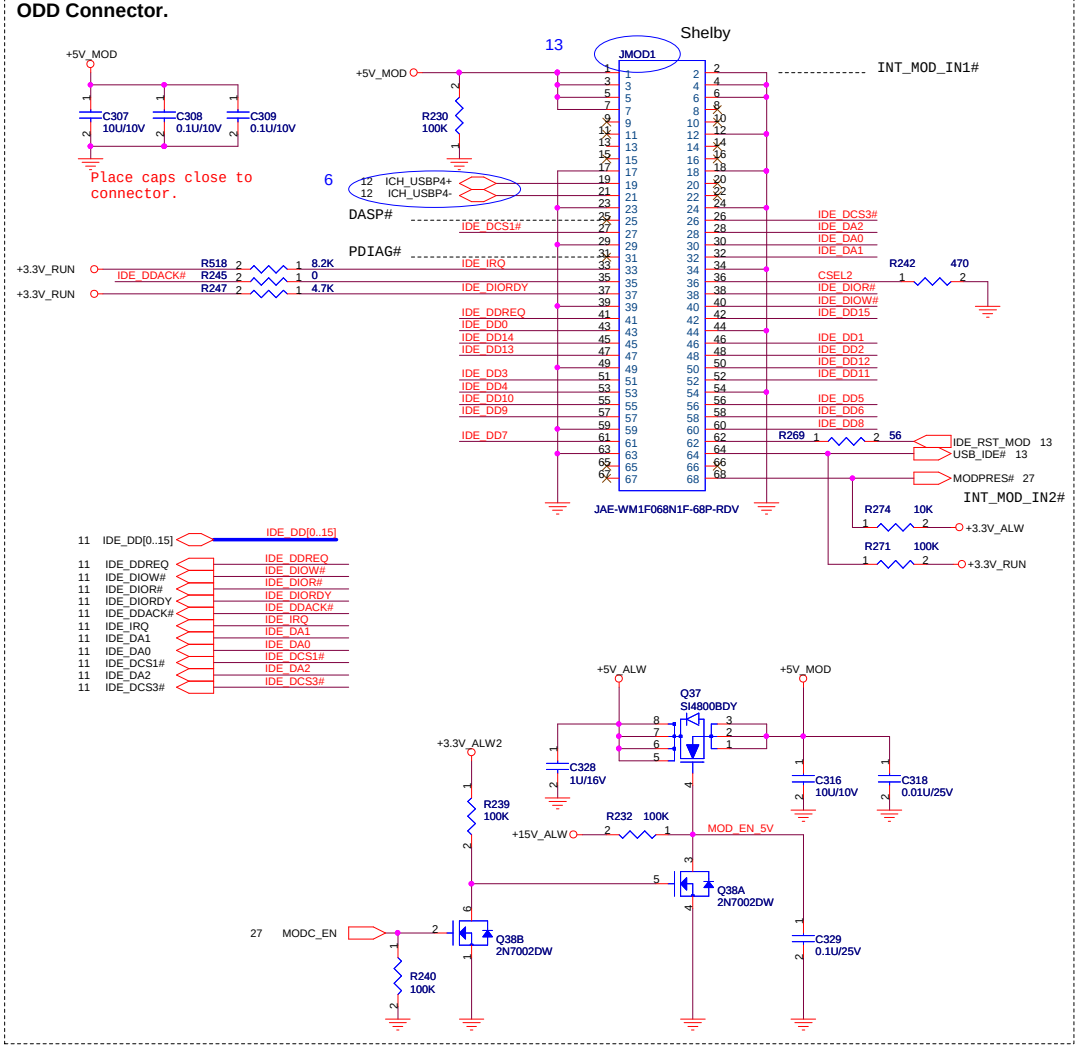
QUANTA COMPUTER

Title	CRT&TV CONN	
Size	Document Number DM6	Rev 1A
Date: Wednesday, August 08, 2007	Sheet 21 of 52	

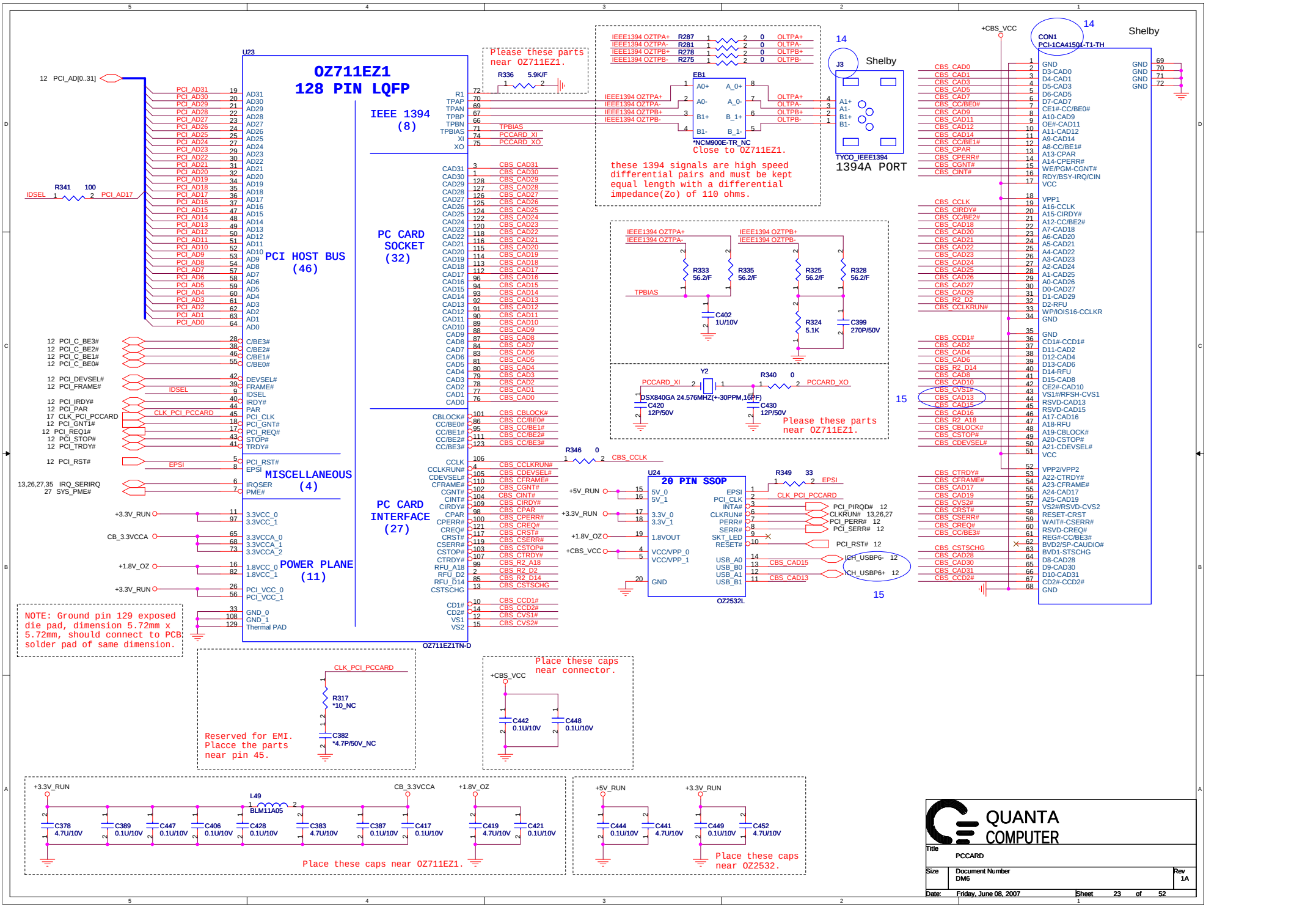
SATA Connector.



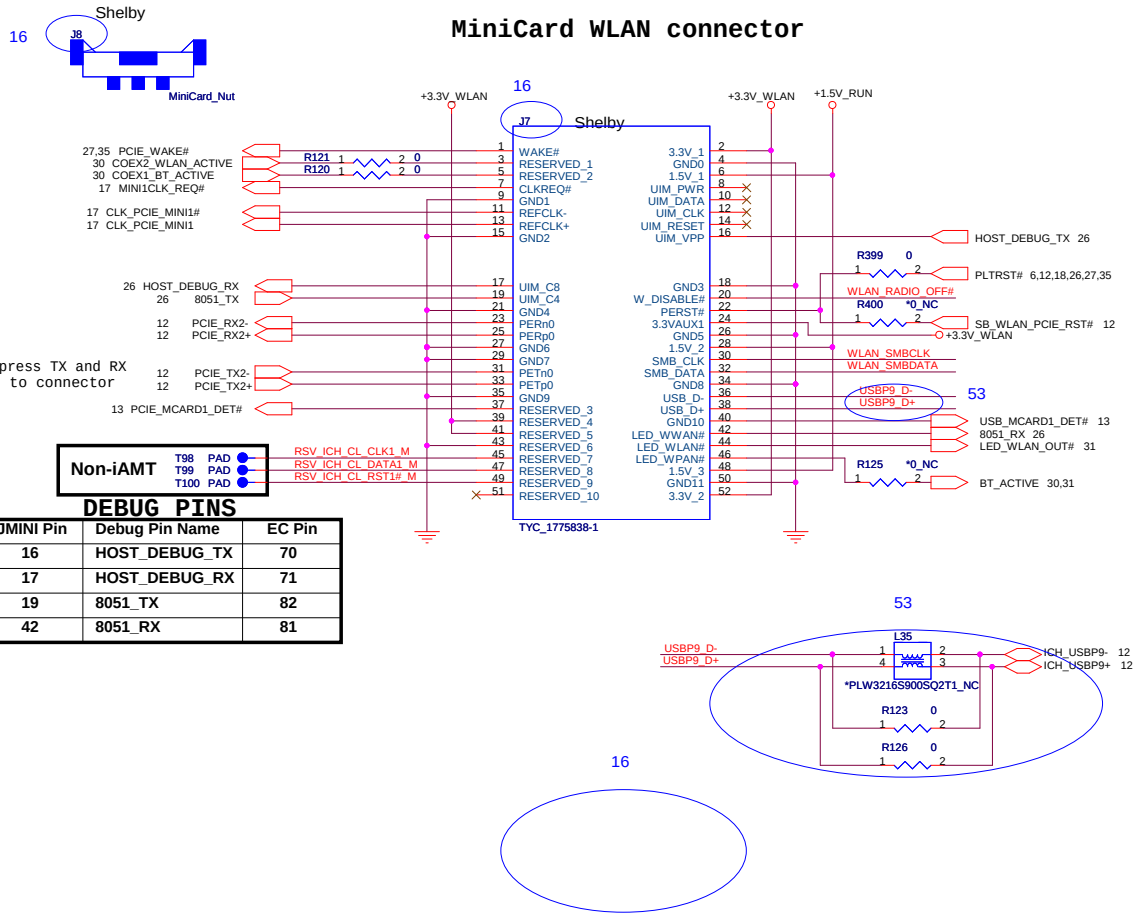
ODD Connector.



QUANTA COMPUTER		
Title: SATA (HDD&CD_ROM)		
Size	Document Number DM6	Rev 1A
Date: Tuesday, August 07, 2007	Sheet 22 of 52	

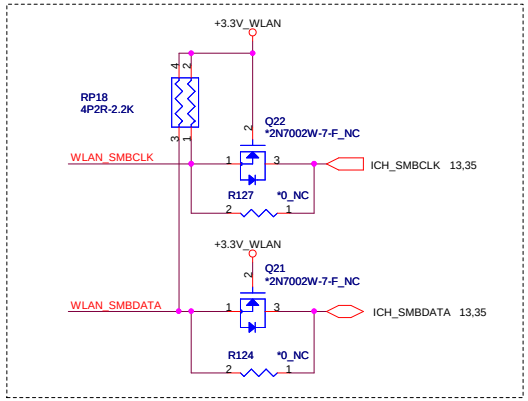

OZ711EZ1
128 PIN LQFP
U23
IEEE 1394 (8)
PC CARD SOCKET (32)
PCI HOST BUS (46)
PC CARD INTERFACE (27)
MISCELLANEOUS (4)
POWER PLANE (11)
Please these parts near OZ711EZ1.
these 1394 signals are high speed differential pairs and must be kept equal length with a differential impedance(Zo) of 110 ohms.
Close to OZ711EZ1.
*NCM900E-TR_NC
TYCO_IEEE1394
1394A PORT
Shelby
CON1
PCI-1CA41501-T1-TH
20 PIN SSOP
U24
OZ2532L
Please these parts near OZ711EZ1.
Please these caps near connector.
Reserved for EMI. Placce the parts near pin 45.
Place these caps near OZ711EZ1.
Place these caps near OZ2532.
NOTE: Ground pin 129 exposed die pad, dimension 5.72mm x 5.72mm, should connect to PCB solder pad of same dimension.
OZ711EZ1TN-D
QUANTA COMPUTER
Title PCCARD
Size Document Number DM6 Rev 1A
Date: Friday, June 08, 2007 Sheet 23 of 52

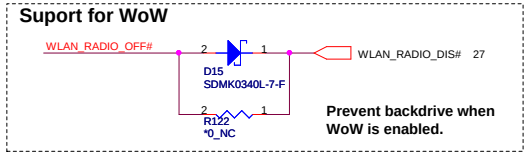
MiniCard WLAN connector

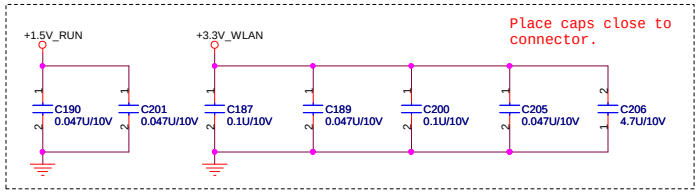


DEBUG PINS

JMINI Pin	Debug Pin Name	EC Pin
16	HOST_DEBUG_TX	70
17	HOST_DEBUG_RX	71
19	8051_TX	82
42	8051_RX	81





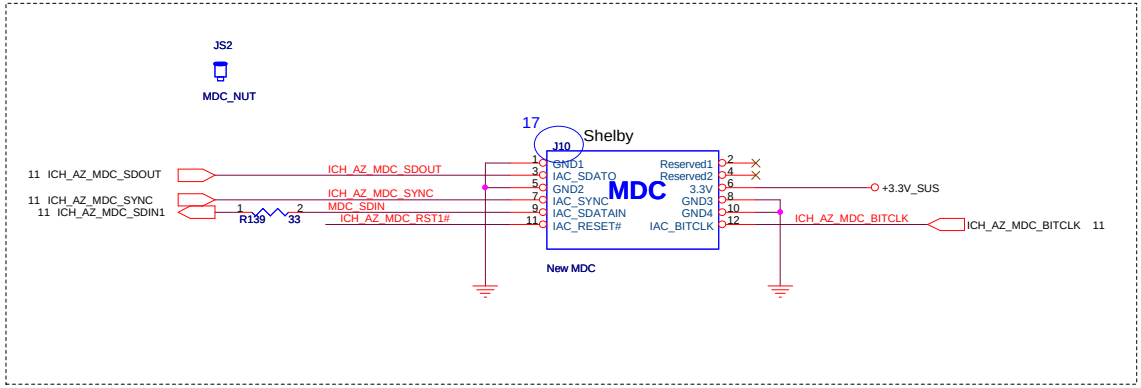


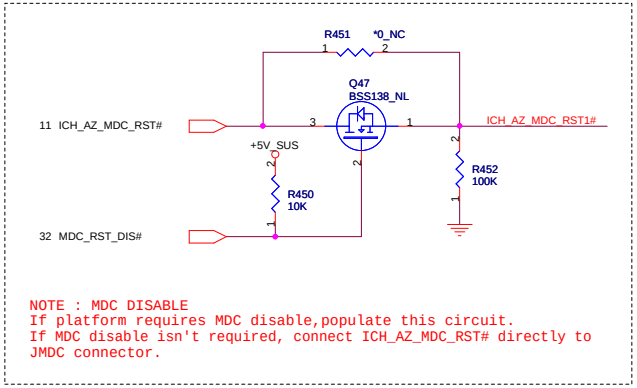
QUANTA COMPUTER

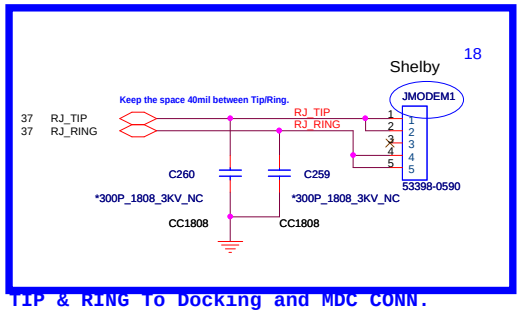
Title	MINI-PCI	
Size	Document Number DM6	Rev 1A
Date: Friday, June 08, 2007	Sheet 24 of 52	

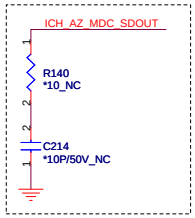
19

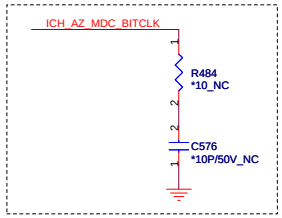
remove RJ11 connector

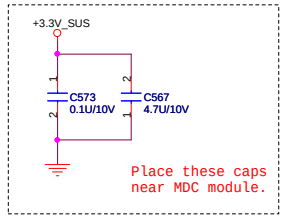






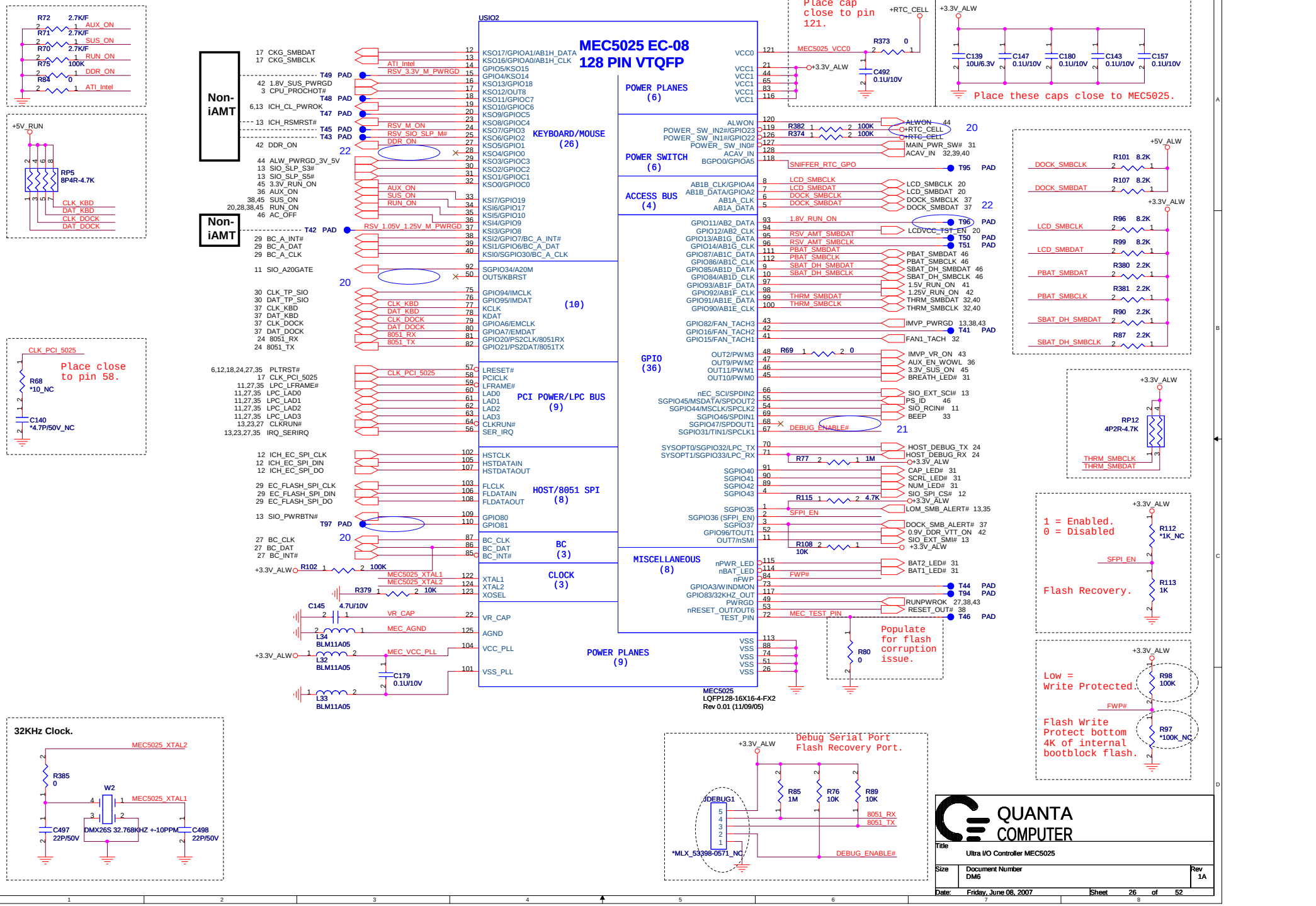


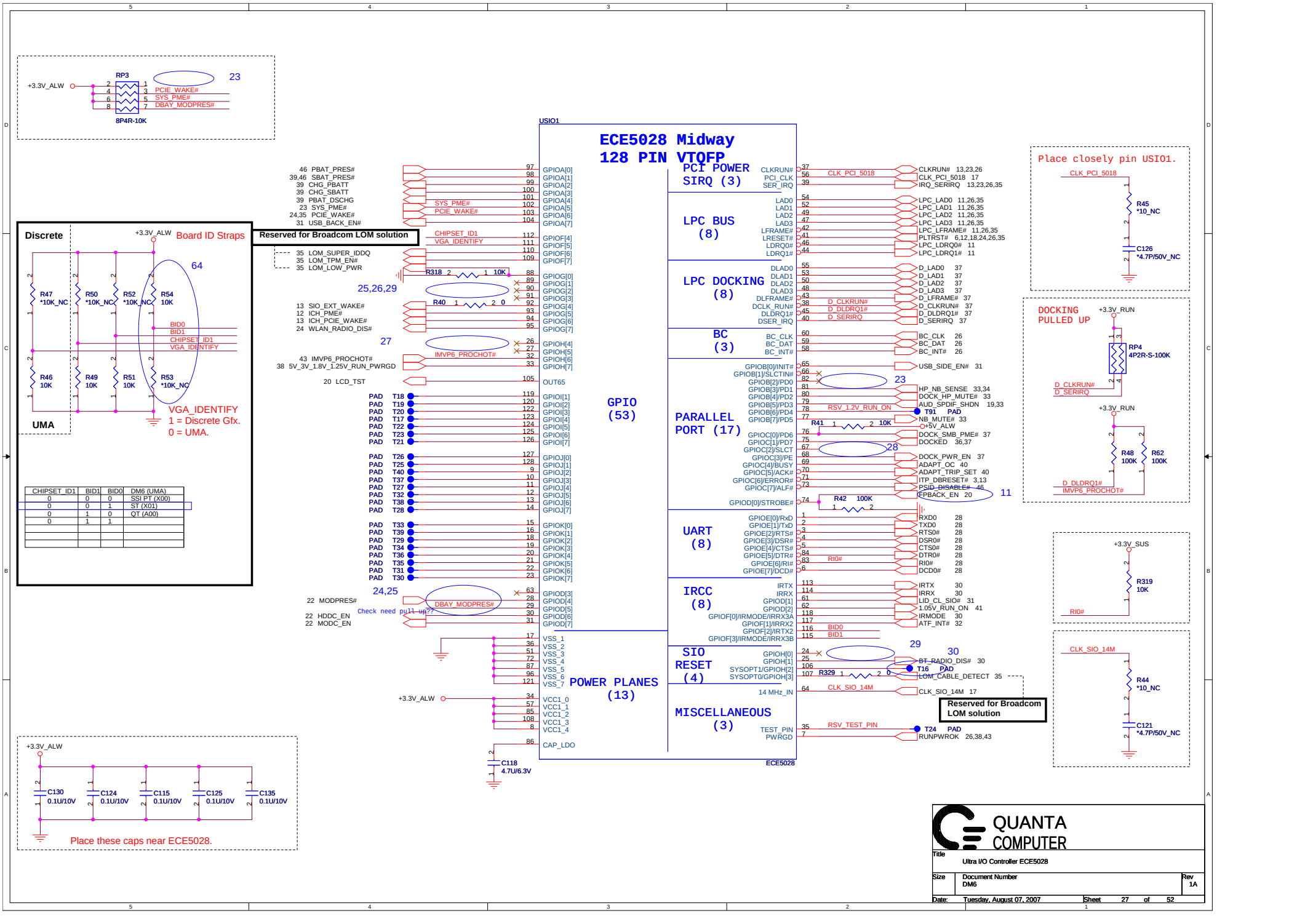


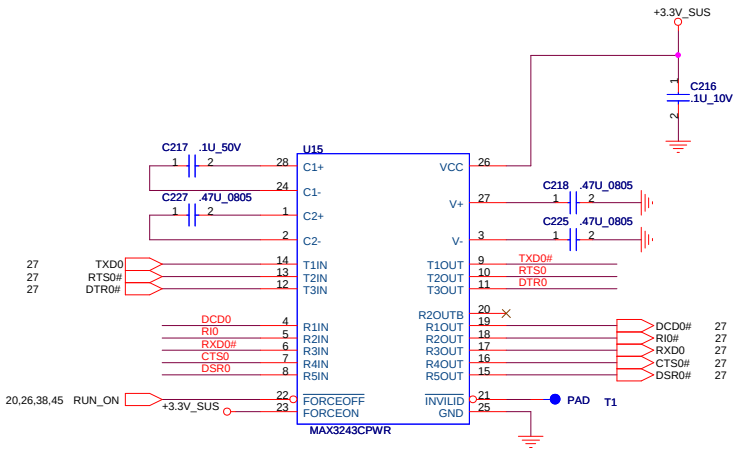


QUANTA COMPUTER

Title	MDC CONN.	
Size	Document Number DM6	Rev 1A
Date: Friday, June 08, 2007	Sheet 25 of 52	

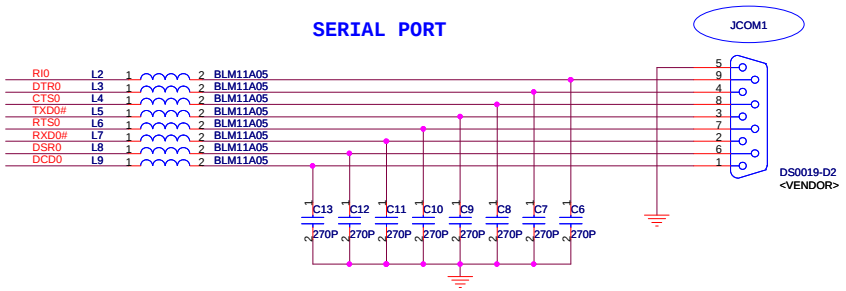

MEC5025 EC-08
128 PIN VTQFP
USIO2
Non-iAMT
Non-iAMT
KEYBOARD/MOUSE (26)
POWER PLANES (6)
POWER SWITCH (6)
ACCESS BUS (4)
GPIO (36)
PCI POWER/LPC BUS (9)
HOST/8051 SPI (8)
BC (3)
CLOCK (3)
MISCELLANEOUS (8)
POWER PLANES (9)
Place cap close to pin 121.
Place these caps close to MEC5025.
Place close to pin 58.
Populate for flash corruption issue.
1 = Enabled.
0 = Disabled
Flash Recovery.
Low = Write Protected
Flash Write Protect bottom 4K of internal bootblock flash.
Debug Serial Port
Flash Recovery Port.
32KHz Clock.
DMX26S 32.768KHZ +-10PPM
*MLX_53398-0571_NC
MEC5025
LQFP128-16X16-4-FX2
Rev 0.01 (11/09/05)
QUANTA COMPUTER
Title
Ultra I/O Controller MEC5025
Size
Document Number
DM6
Rev
1A
Date:
Friday, June 08, 2007
Sheet
26
of
52


RP3
+3.3V_ALW
PCIE_WAKE#
SYS_PME#
DBAY_MODPRES#
8P4R-10K
23
USIO1
ECE5028 Midway
128 PIN VTQFP
PCI POWER
SIRQ (3)
LPC BUS
(8)
LPC DOCKING
(8)
BC
(3)
GPIO
(53)
PARALLEL
PORT (17)
UART
(8)
IRCC
(8)
SIO
RESET
(4)
MISCELLANEOUS
(3)
POWER PLANES
(13)
ECE5028
Discrete
UMA
Board ID Straps
64
VGA_IDENTIFY
1 = Discrete Gfx.
0 = UMA.
Reserved for Broadcom LOM solution
25,26,29
27
24,25
Check need pull up??
28
29
30
Reserved for Broadcom
LOM solution
Place closely pin USIO1.
DOCKING
PULLED UP
Place these caps near ECE5028.
QUANTA
COMPUTER
Ultra I/O Controller ECE5028
Tuesday, August 07, 2007



If MAX3243 pin 22 tied to RUN_ON,then it can not support Ring Out

SERIAL PORT



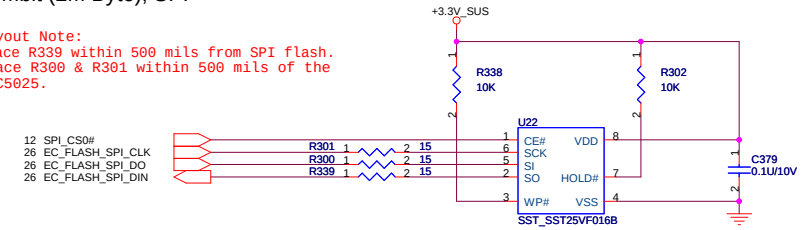
Place them close to serial port

QUANTA COMPUTER

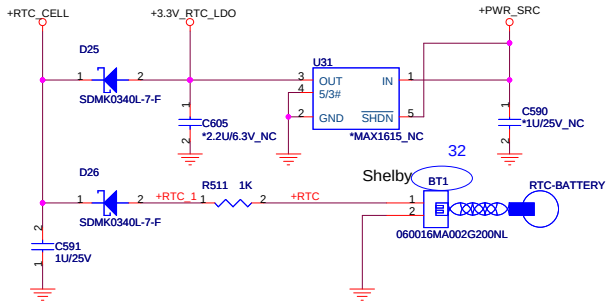
Title	SERIAL PORT & USB		
Size	Document Number DM6		Rev 1A
Date:	Friday, June 08, 2007	Sheet 28 of 52	

16Mbit (2M Byte), SPI

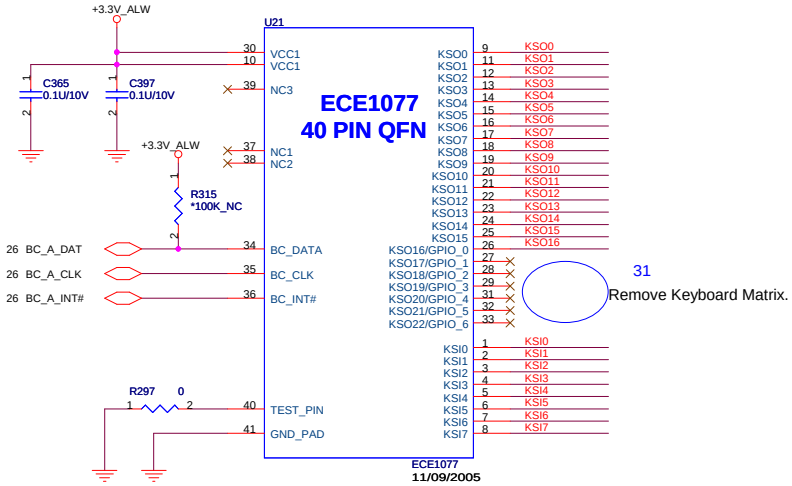
Layout Note:
Place R339 within 500 mils from SPI flash.
Place R300 & R301 within 500 mils of the MEC5025.



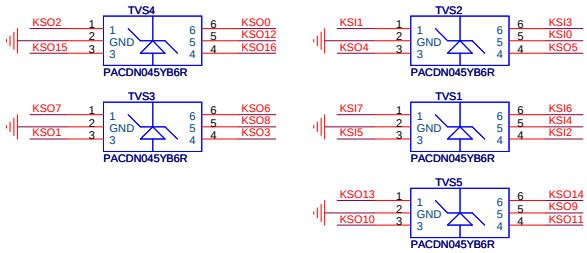
RTC BATTERY

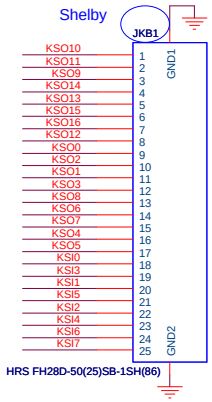


Keyboard Scan Extension



31
Remove Keyboard Matrix.



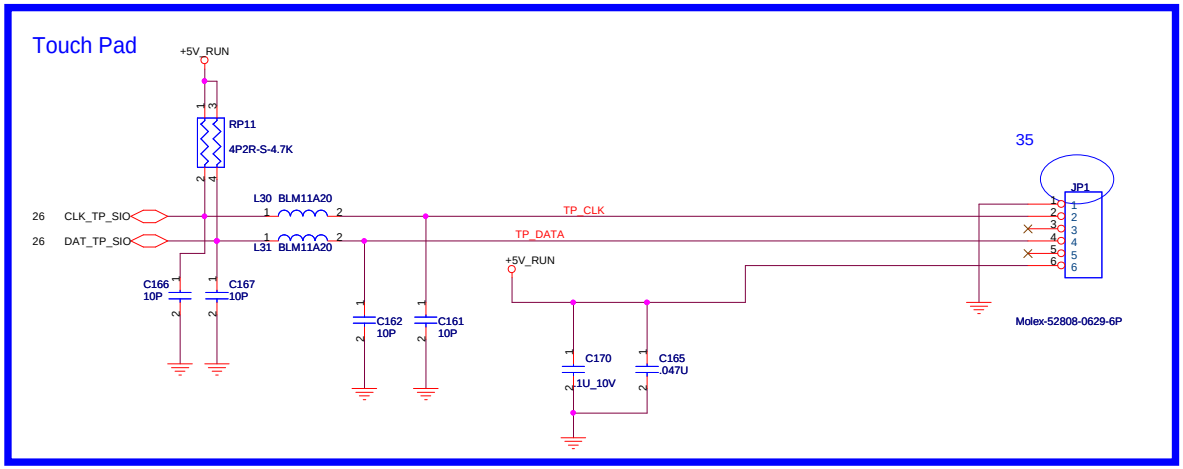


Keyboard CONN

QUANTA COMPUTER

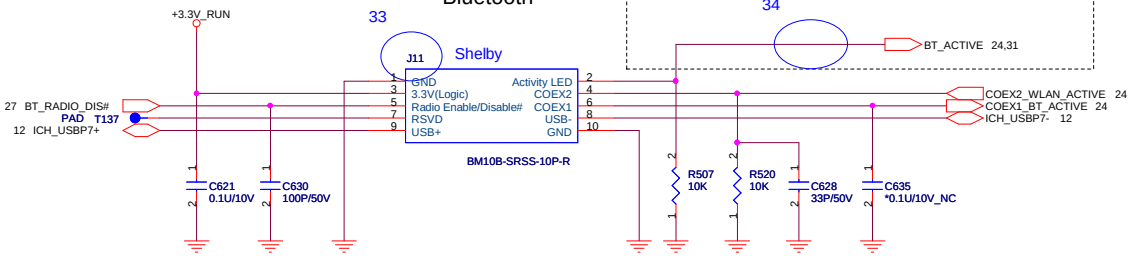
Title	FLASH, RTC & KC		
Size	Document Number DM6		Rev 1A
Date:	Friday, June 08, 2007	Sheet 29 of 52	

Touch Pad

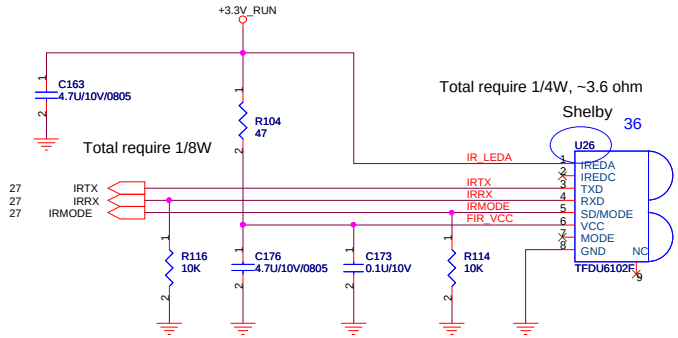


This circuit is only needed if the platform has the SNIFFER.

Bluetooth

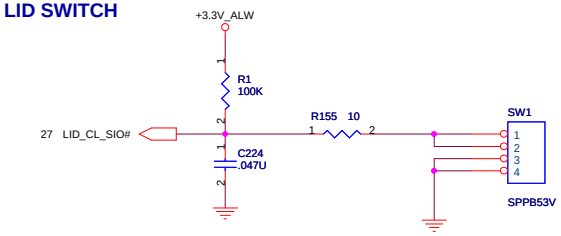


FIR

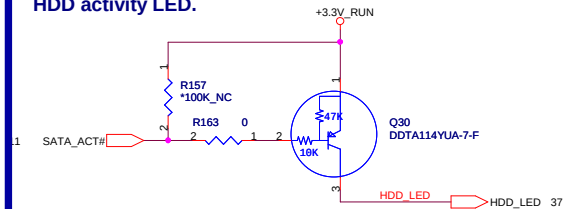


Title	TOUCH PAD, BULE TOOTH & FIR	
Size	Document Number DM6	Rev 1A
Date: Friday, June 08, 2007	Sheet 30 of 52	

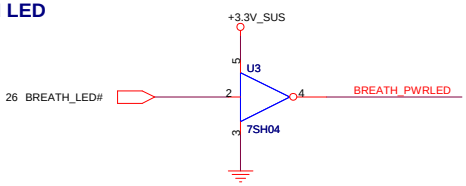
LID SWITCH



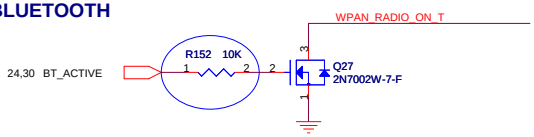
HDD activity LED.



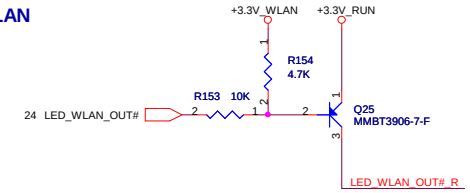
BREATH LED



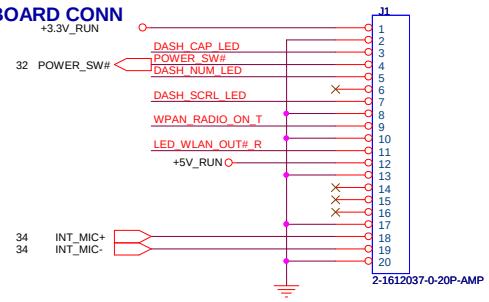
BLUETOOTH



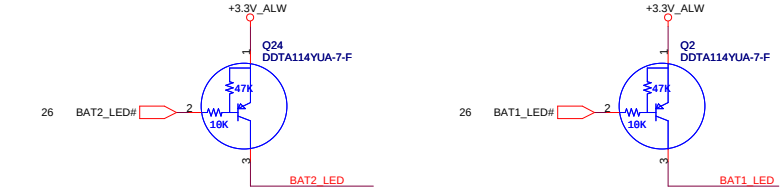
WLAN



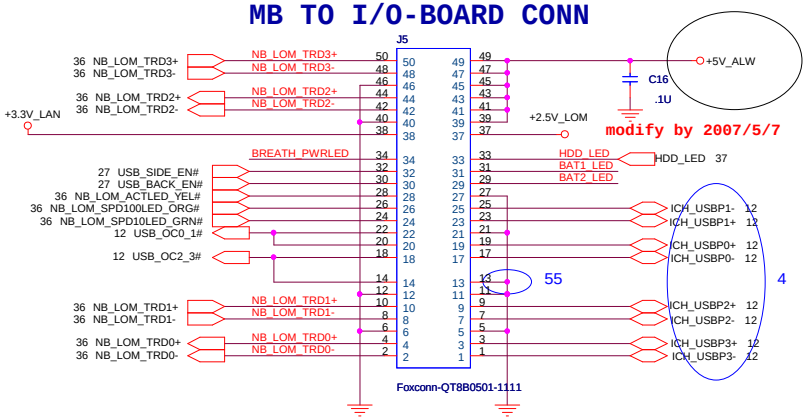
DASH BOARD CONN



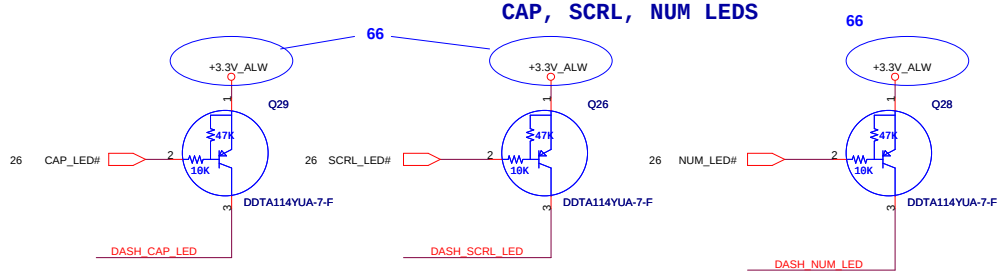
Battery 1,2 LED

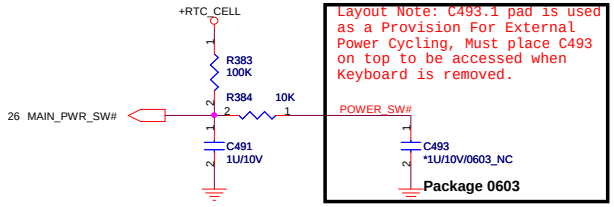


MB TO I/O-BOARD CONN



CAP, SCRL, NUM LEDS

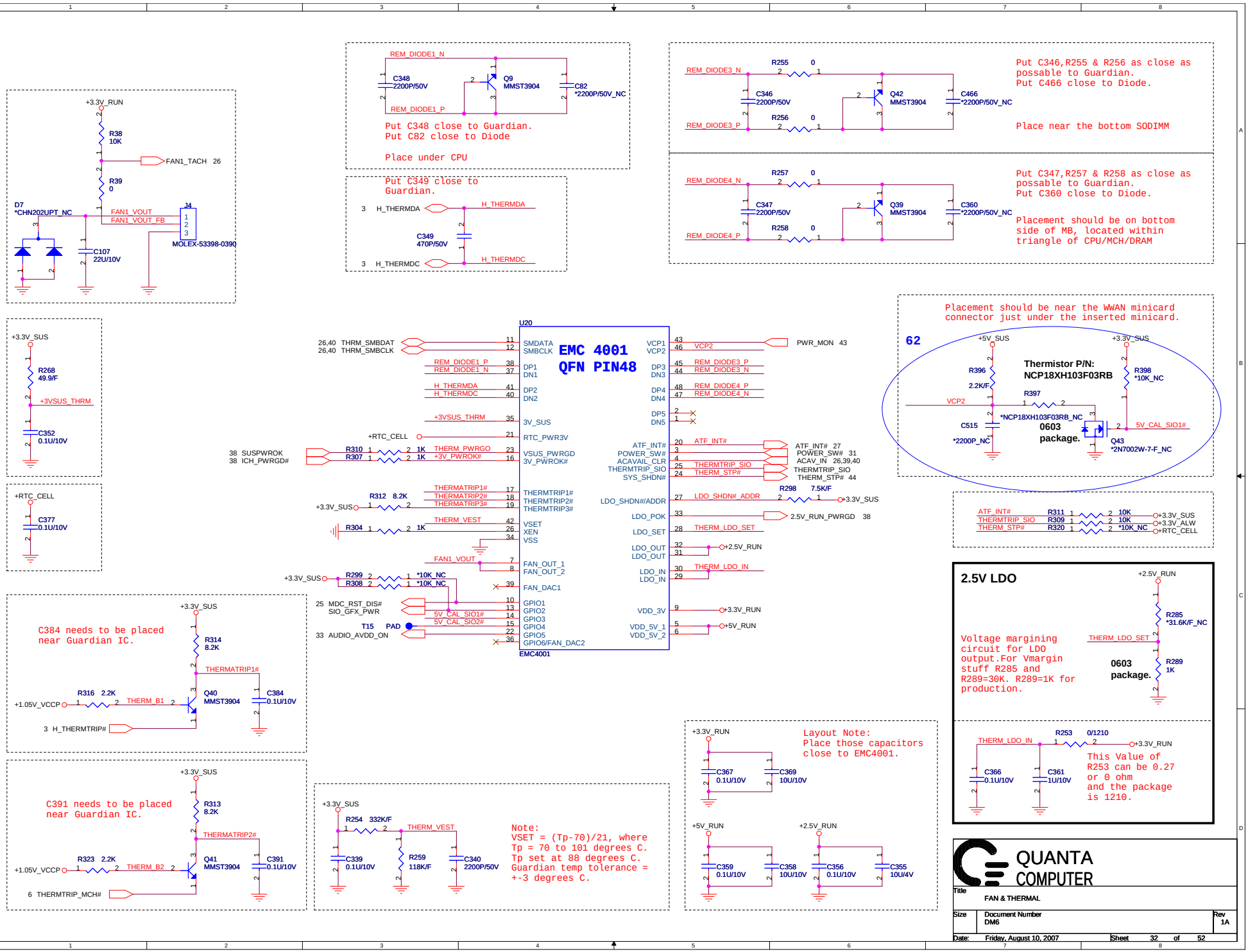




Layout Note: C493.1 pad is used as a Provision For External Power Cycling, Must place C493 on top to be accessed when Keyboard is removed.

QUANTA COMPUTER

Title	SWITCH, KEYBOARD & LED	
Size	Document Number DM6	Rev 1A
Date: Tuesday, August 07, 2007	Sheet 31 of 52	



QUANTA COMPUTER

Title	FAN & THERMAL
Size	Document Number DM6
Rev	1A
Date:	Friday, August 10, 2007
Sheet	32 of 52

INTERNAL SPEAKER AMP

Package 1206 for THD+N performance and Vista Logo requirements.

X7R

AUD_LINE_OUT_L C602 0.033U/200V/1206
AUD_LINE_OUT_R C603 0.033U/200V/1206
AUD_HP_OUT_L C559 2.2U/25V/1206
AUD_HP_OUT_R C556 2.2U/25V/1206

C557 *47P/50V_NC
C561 *47P/50V_NC
C588 *47P/50V_NC
C587 *47P/50V_NC
C551 1U/10V/0603
T117 PAD

U30
MAX9789A
TQFN 32PIN

LIN-
RIN-
HP_OUT_L
HP_OUT_R
AUD_SPK_ENABLE#
AUD_HP_NB_SENSE
AUD_AMP_MUTE#
AUD_AMP_GAIN1
AUD_AMP_GAIN2

SPKR_INL
SPKR_INR
HP_INL
HP_INR
BIAS
SPKR_EN#
HP_EN
MUTE#
GAIN1
GAIN2
HPVDD
CPVDD
C1P
C1N
CPGND
PVSS
CPVSS

OUTL+ AUD_SPK_L1
OUTL- AUD_SPK_L2
OUTR+ AUD_SPK_R1
OUTR- AUD_SPK_R2
HPL AUD_HP_JACK_L 34
HPR AUD_HP_JACK_R 34
REGEN REGEN
SET SET
VOUT +VDDA
VDD VDD
PVDD_8 +5V_SPK_AMP
PVDD_18 +5V_SPK_AMP
GND_28
PGND_5
PGND_21

+5V_SPK_AMP
C584 *10U/10V/0805_NC
C578 1U/10V/0603
C572 1U/16V/0805
C564 1U/16V/0805

MAX9789A

Shelby
JSPK1
AUD_SPK_R1
AUD_SPK_R2
AUD_SPK_L1
AUD_SPK_L2
53398-0490
C649 100P/50V
C650 100P/50V
C651 100P/50V
C652 100P/50V

L35
FB_600ohm+-25%_100MHz
_200mA_0.6ohm DC
+5V_SPK_AMP
VDD
C570 1U/10V/0603
C565 1U/10V/0603
C569 0.1U/10V
Layout Note: Place close U30.

+VDDA
C575 1U/10V/0603
C580 1U/10V/0603
Layout Note: Place close U30.

For TPA6040A, pop R434, depop R439.
+5V_SPK_AMP
R439 100K
R434 *0_NC
AUDIO_AVDD_ON
AUD_AMP_MUTE#

+5V_SPK_AMP
R424 100K
R425 100K
AUD_SPK_ENABLE#
AUD_EAPD
Q45 2N7002W-7-F
NB_MUTE#
Q44 2N7002W-7-F

+5V_SPK_AMP
R494 *100K_NC
R489 100K
AUD_AMP_GAIN1
AUD_AMP_GAIN2
R493 100K
R488 *100K_NC

GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

AUDIO_AVDD_ON
R501 0
REGEN
C592 *0.033U/16V_NC
For TPA6040A, pop C592, depop R501.
AUDIO_AVDD_ON 32

+5V_SPK_AMP
+5V_RUN
L61 BLM21PG600SN1D
C585 *1U/10V/0603_NC
C596 *10U/10V/0805_NC
Layout Note: Place close to pin 8.
FB_60ohm+-25%_100MHz
_3A_0.05ohm DC
+5V_SPK_AMP
C554 1U/10V/0603
C548 10U/10V/0805
Layout Note: Place close to pin 18.

C543 0.1U/10V
+3.3V_RUN
U29
7SH08
AUD_HP_NB_SENSE
HP_NB_SENSE
NB_MUTE#
NB_MUTE# 27

54
R402 0
R525 0
R541 0
R534 0
R542 0
R547 *0_NC
R548 *0_NC
60
For TPA6040A, pop C601, depop R502.
SET
C601 *0.033U/16V_NC
R502 0

AZALIA (HD) CODEC

U33
STAC9205
QFN 48PIN

11 ICH_AZ_CODEC_BITCLK
11 ICH_AZ_CODEC_SDIN0
11 ICH_AZ_CODEC_SDOUT
11 ICH_AZ_CODEC_SYNC
11 ICH_AZ_CODEC_RST#
ICH_AZ_CODEC_BITCLK
R535 33 SDIN
ICH_AZ_CODEC_SDOUT

HDA_BITCLK
HDA_SDI_CODEC
HDA_SDO
HDA_SYNC
HDA_RST#

DMIC_CLK
DMIC0/VOL_UP/GPIO1
DMIC1/VOL_DN/GPIO2

For tuning.
19,37 AUD_SPDIF_OUT
R531 0
AUD_EAPD
SPDIF_OUT
SPDIF_IN/EAPD/GPIO0
SPDIF_OUT

NC_43
NC_44
NC_45

+3.3V_RUN
R523 100K
C637 1000P/50V
DVDD_CORE_1
DVDD_CORE_9
DVDD_CORE_40
DVDD_IO
AVDD_25
AVDD_38
DVSS
AVSS_26
AVSS_42
C643 *10U/10V/0805_NC
C640 0.1U/10V
C645 1U/10V/0603
C642 0.1U/10V
C631 0.1U/16V/0603
C618 1U/10V/0603
C617 *10U/10V/0805_NC
+VDDA

SENSE_A AUD_SENSE_A
SENSE_B AUD_SENSE_B
R517 100K
PORT_A_L AUD_HP_OUT_L
PORT_A_R AUD_HP_OUT_R
VREFOUT_A
PORT_B_L AUD_EXT_MIC_L 34
PORT_B_R AUD_EXT_MIC_R 34
VREFOUT_B AUD_VREFOUT_B 34
PORT_C_L AUD_INT_MIC_IN 34
PORT_C_R
VREFOUT_C
PORT_D_L AUD_LINE_OUT_L
PORT_D_R AUD_LINE_OUT_R
PORT_E_L
PORT_E_R
GPIO4/VREFOUT_E
R516 10K
DOCK_HP_MUTE# 27
PORT_F_L
PORT_F_R
GPIO3/VREFOUT_F
R515 10K
AUD_SPDIF_SHDN 19,27
CD_L
CD_GND
CD_R
PC_BEEP
MONO_OUT
AUD_PC_BEEP
VREFFILT
CAP2
AC97VREFI
C620 10U/6.3V/0603
C619 10U/6.3V/0603

Layout Note: Close to Pin 13.
R536 5.1K/F
+VDDA
AUD_SENSE_A
R529 39.2K/F
R532 20K/F
C644 1000P/50V
27,34 HP_NB_SENSE
HP_NB_SENSE
AUD_MIC_SWITCH 34
Q50 2N7002W-7-F
Q52 2N7002W-7-F

Close to U33.
+VDDA
C646 0.1U/16V/0603
AUD_PC_BEEP
C641 0.1U/10V
BEEP2
R539 20K
BEEP1
R540 10K
BEEP 26
SPKR 13
U34 74LVC1G86GW

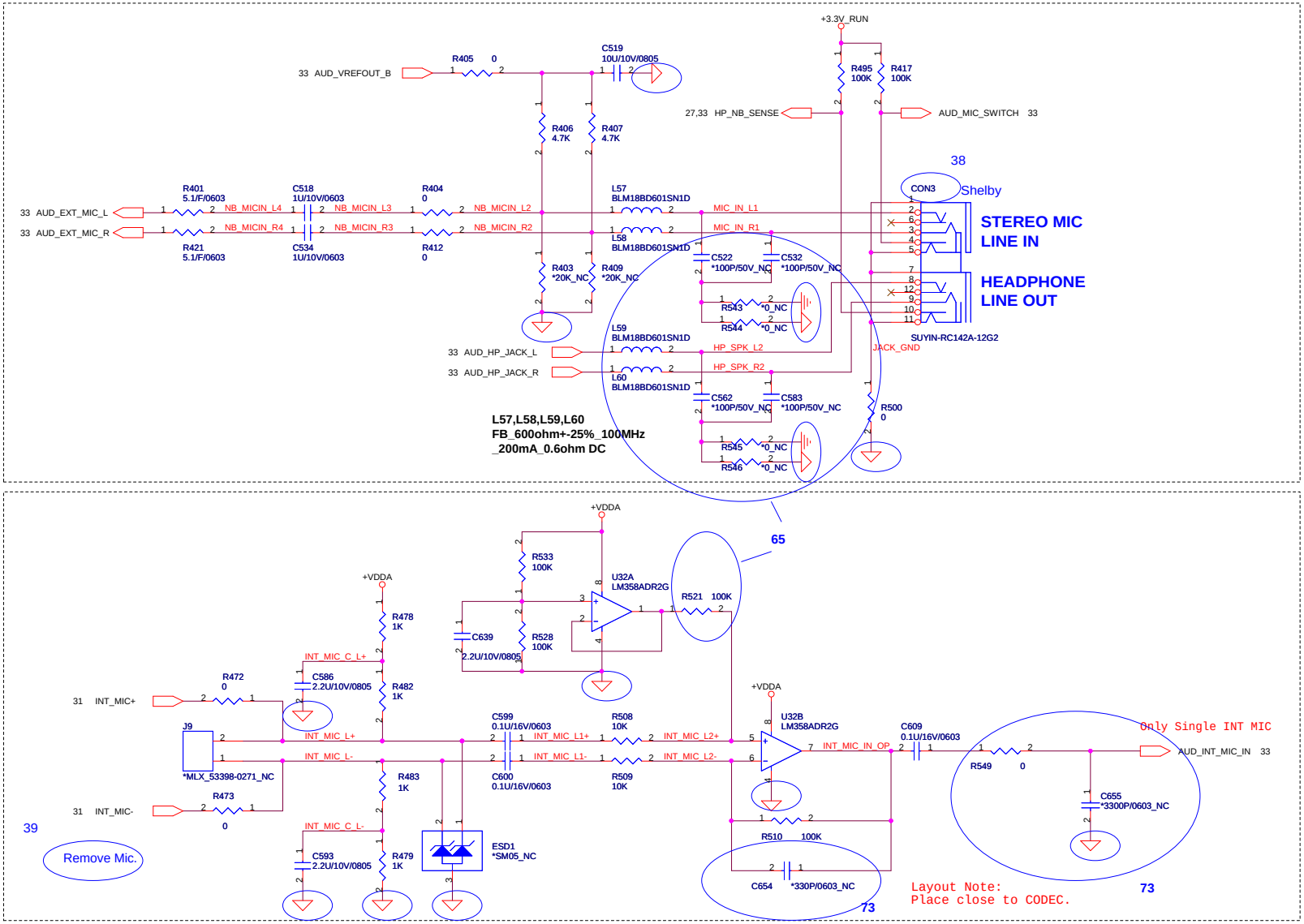
ICH_AZ_CODEC_BITCLK
R537 *47_NC
Close to pin 6.
C647 *0.1U/10V_NC

ICH_AZ_CODEC_SDOUT
R538 *47_NC
Close to pin 5.
C648 *0.1U/10V_NC

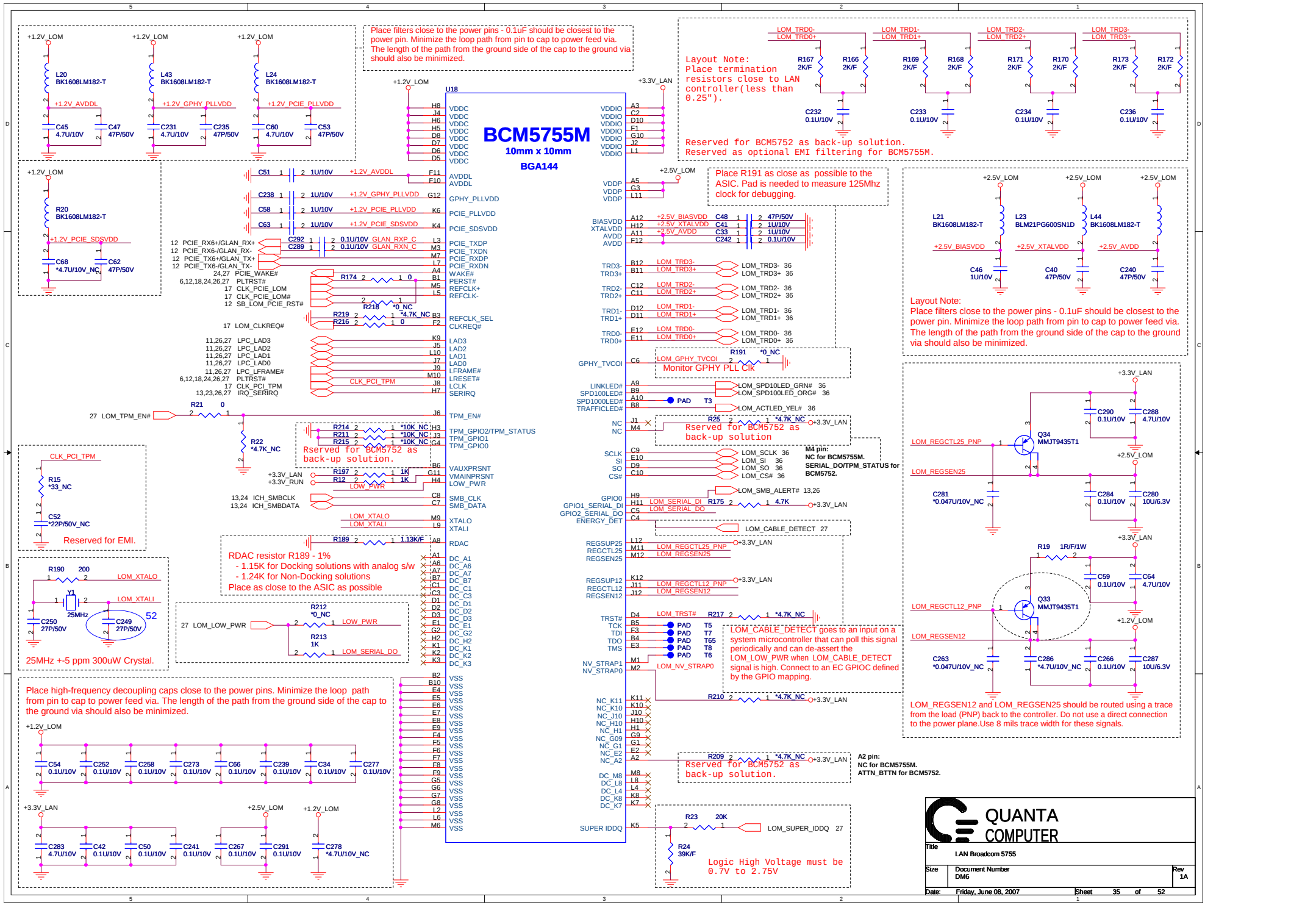
70
STAC9205X5NBEB1XR
Change STA9205 footprint to QFN48-7X7-5-49P-1H.

QUANTA COMPUTER

Title	Azelia CODEC	
Size	Document Number DM6	Rev 1A
Date: Wednesday, August 08, 2007	Sheet 33 of 52	



QUANTA COMPUTER		
Title	AUDIO CONN	
Size	Document Number DM6	Rev 1A
Date: Thursday, August 09, 2007	Sheet 34 of 52	


BCM5755M
10mm x 10mm
BGA144
U18
Place filters close to the power pins - 0.1uF should be closest to the power pin. Minimize the loop path from pin to cap to power feed via. The length of the path from the ground side of the cap to the ground via should also be minimized.
Layout Note:
Place termination resistors close to LAN controller(less than 0.25").
Reserved for BCM5752 as back-up solution.
Reserved as optional EMI filtering for BCM5755M.
Place R191 as close as possible to the ASIC. Pad is needed to measure 125Mhz clock for debugging.
Monitor GPHY PLL Clk
Layout Note:
Place filters close to the power pins - 0.1uF should be closest to the power pin. Minimize the loop path from pin to cap to power feed via. The length of the path from the ground side of the cap to the ground via should also be minimized.
Rserved for BCM5752 as back-up solution
M4 pin:
NC for BCM5755M.
SERIAL_DO/TPM_STATUS for BCM5752.
Reserved for EMI.
RDAC resistor R189 - 1%
- 1.15K for Docking solutions with analog s/w
- 1.24K for Non-Docking solutions
Place as close to the ASIC as possible
25MHz +-5 ppm 300uW Crystal.
LOM_CABLE_DETECT goes to an input on a system microcontroller that can poll this signal periodically and can de-assert the LOM_LOW_PWR when LOM_CABLE_DETECT signal is high. Connect to an EC GPIOC defined by the GPIO mapping.
Rserved for BCM5752 as back-up solution.
A2 pin:
NC for BCM5755M.
ATTN_BTTN for BCM5752.
Logic High Voltage must be 0.7V to 2.75V
LOM_REGSEN12 and LOM_REGSEN25 should be routed using a trace from the load (PNP) back to the controller. Do not use a direct connection to the power plane.Use 8 mils trace width for these signals.
Place high-frequency decoupling caps close to the power pins. Minimize the loop path from pin to cap to power feed via. The length of the path from the ground side of the cap to the ground via should also be minimized.
QUANTA COMPUTER
Title: LAN Broadcom 5755
Size: Document Number DM6
Rev: 1A
Date: Friday, June 08, 2007
Sheet 35 of 52

TRANSFORM+RJ45

36nH is a suggested value.
Actual value will be systgem dependent.
Must use 0603 package for lower DC resistance.

L19 L18 L17 L16 L15 L14 L13 L12 — 0603CS-360EJTS

35 LOM_TRD0- → TRD0N_L → U5 A0
35 LOM_TRD0+ → TRD0P_L → A1
35 LOM_TRD1- → TRD1N_L → A2
35 LOM_TRD1+ → TRD1P_L → A3
35 LOM_TRD2- → TRD2N_L → A4
35 LOM_TRD2+ → TRD2P_L → A5
35 LOM_TRD3- → TRD3N_L → A6
35 LOM_TRD3+ → TRD3P_L → A7

0B1 1B1 2B1 3B1 4B1 5B1 6B1 7B1 → NB_LOM_TRD0- NB_LOM_TRD0+ NB_LOM_TRD1- NB_LOM_TRD1+ NB_LOM_TRD2- NB_LOM_TRD2+ NB_LOM_TRD3- NB_LOM_TRD3+ → NB_LOM_TRD0- 31 … NB_LOM_TRD3+ 31

To IO Board. 49

49

Remove RJ45 connector

35 LOM_ACTLED_YEL# → LOM_ACTLED_YEL# → LED0
35 LOM_SPD10LED_GRN# → LOM_SPD10LED_GRN# → LED1
35 LOM_SPD100LED_ORG# → LOM_SPD100LED_ORG# → LED2

0LED1 1LED1 2LED1 → NB_LOM_ACTLED_YEL# NB_LOM_SPD10LED_GRN# NB_LOM_SPD100LED_ORG# → NB_LOM_ACTLED_YEL# 31 … NB_LOM_SPD100LED_ORG# 31

27,37 DOCKED → SEL (NC)

+3.3V_LAN → VDD_1 VDD_2 VDD_3 VDD_4 VDD_5 VDD_6 VDD_7

GND_1 GND_2 GND_3 GND_4 GND_5 GND_6 GND_7 GND_8 GND_9 GND_10 GND_11 GND_12 GND_13 GND_14

0B2 1B2 2B2 3B2 4B2 5B2 6B2 7B2 → DOCK_LOM_TRD0- DOCK_LOM_TRD0+ DOCK_LOM_TRD1- DOCK_LOM_TRD1+ DOCK_LOM_TRD2- DOCK_LOM_TRD2+ DOCK_LOM_TRD3- DOCK_LOM_TRD3+ → DOCK_LOM_TRD0- 37 … DOCK_LOM_TRD3+ 37

0LED2 1LED2 2LED2 → DOCK_LOM_ACTLED_YEL# DOCK_LOM_SPD10LED_GRN# DOCK_LOM_SPD100LED_ORG# → DOCK_LOM_ACTLED_YEL# 37 … DOCK_LOM_SPD100LED_ORG# 37

U5 **PI3L500-A** PI3L500-A2FE

DOCKED
SEL 0: RJ45.
SEL 1: Dock.

Reserve pull up.

+3.3V_LAN
R11 *10K_NC R9 *10K_NC R10 *10K_NC
LOM_ACTLED_YEL#
LOM_SPD10LED_GRN#
LOM_SPD100LED_ORG#

+PWR_SRC +3.3V_ALW +3.3V_LAN
PQ34 SI3456DV-T1-E3
PR127 100K PR126 100K
PC125 1U/10V PC6 0.1U/10V PC7 4.7U/6.3V
PQ35A 2N7002DW
PQ35B 2N7002DW
26 AUX_ON
PR129 200K PR128 470K PC127 4700P/50V/0603

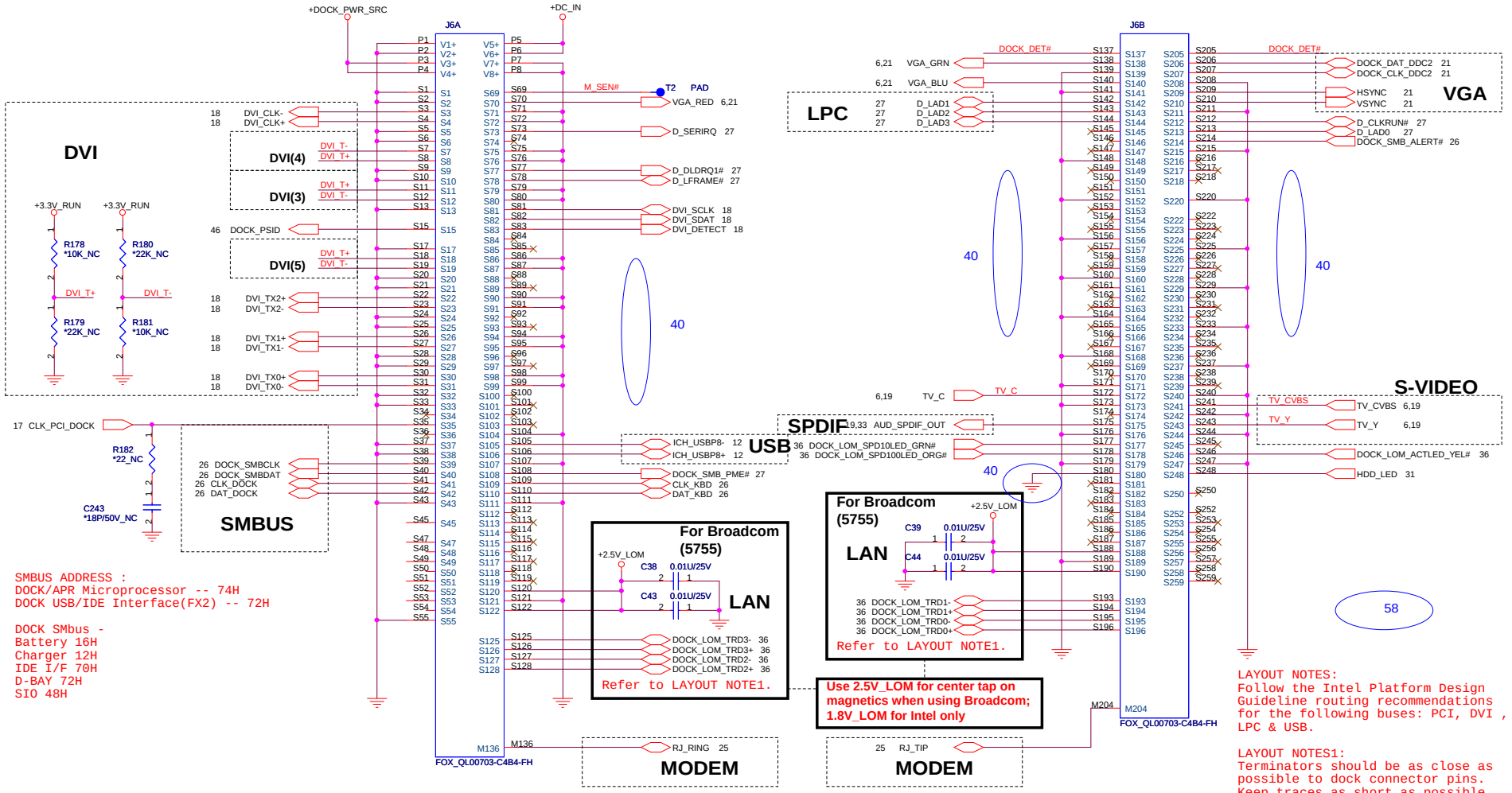
+PWR_SRC +3.3V_ALW +3.3V_WLAN +3.3V_RUN
PQ39 FDC655BN
PR130 *0/1206_NC
PR131 100K PR141 100K
PQ40B 2N7002DW
PQ40A 2N7002DW
26 AUX_EN_WOWL
PR132 200K PR142 470K PC138 *4700P/50V/0603_NC
PR13 100K

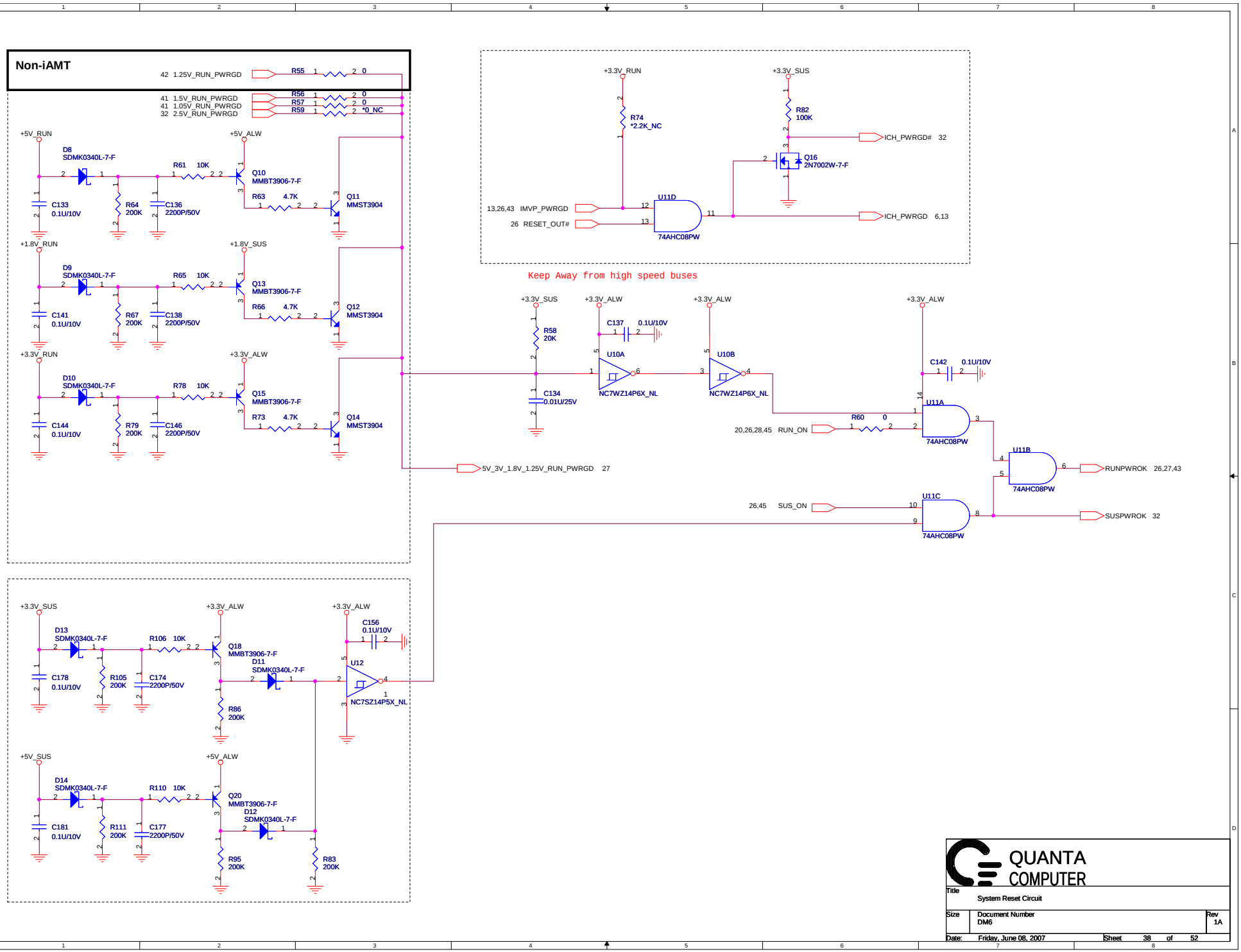
	NV_STRAP1	NV_STRAP0	S0	SI	CS#	SCLK
Auto-Sense Mode	0	0	0	0	0	0
ST M45PE20	0	1	1	0	0	1
Atmel AT45BCM021B	0	0	1	0	1	1

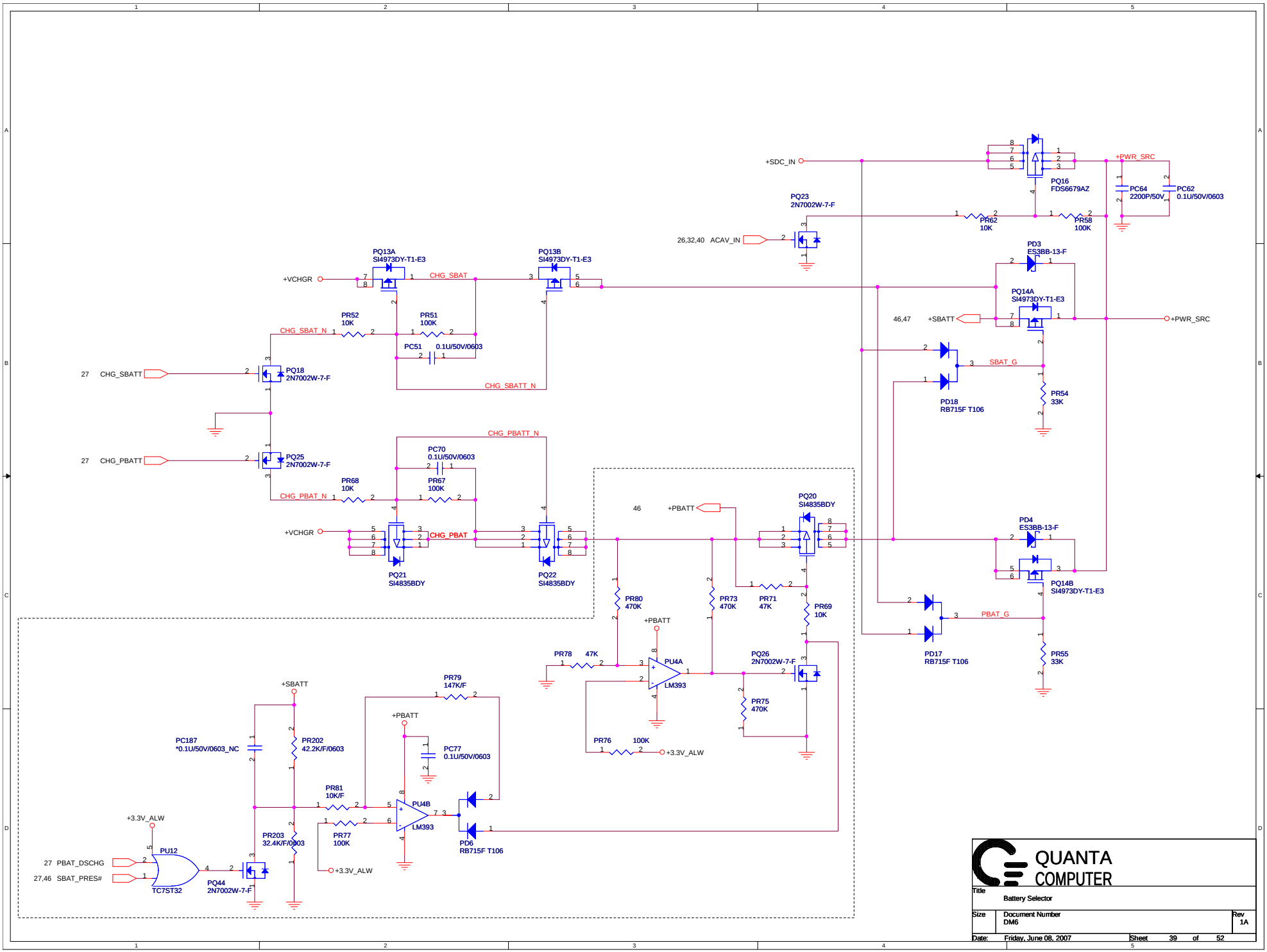
+3.3V_LAN
R196 *4.7K_NC R194 *4.7K_NC R195 *4.7K_NC
35 LOM_SCLK
35 LOM_SI
35 LOM_SO
35 LOM_CS#
U17 SCK SO SI CS# VCC WP# RESET# GND — AT45BCM021B
U19 C Q D S# VCC W# RESET# VSS — *STM45PE20_NC
C237 0.1U/10V

QUANTA COMPUTER

Title	LAN SWITCH	
Size	Document Number DM6	Rev 1A
Date: Friday, June 08, 2007	Sheet 36 of 52	

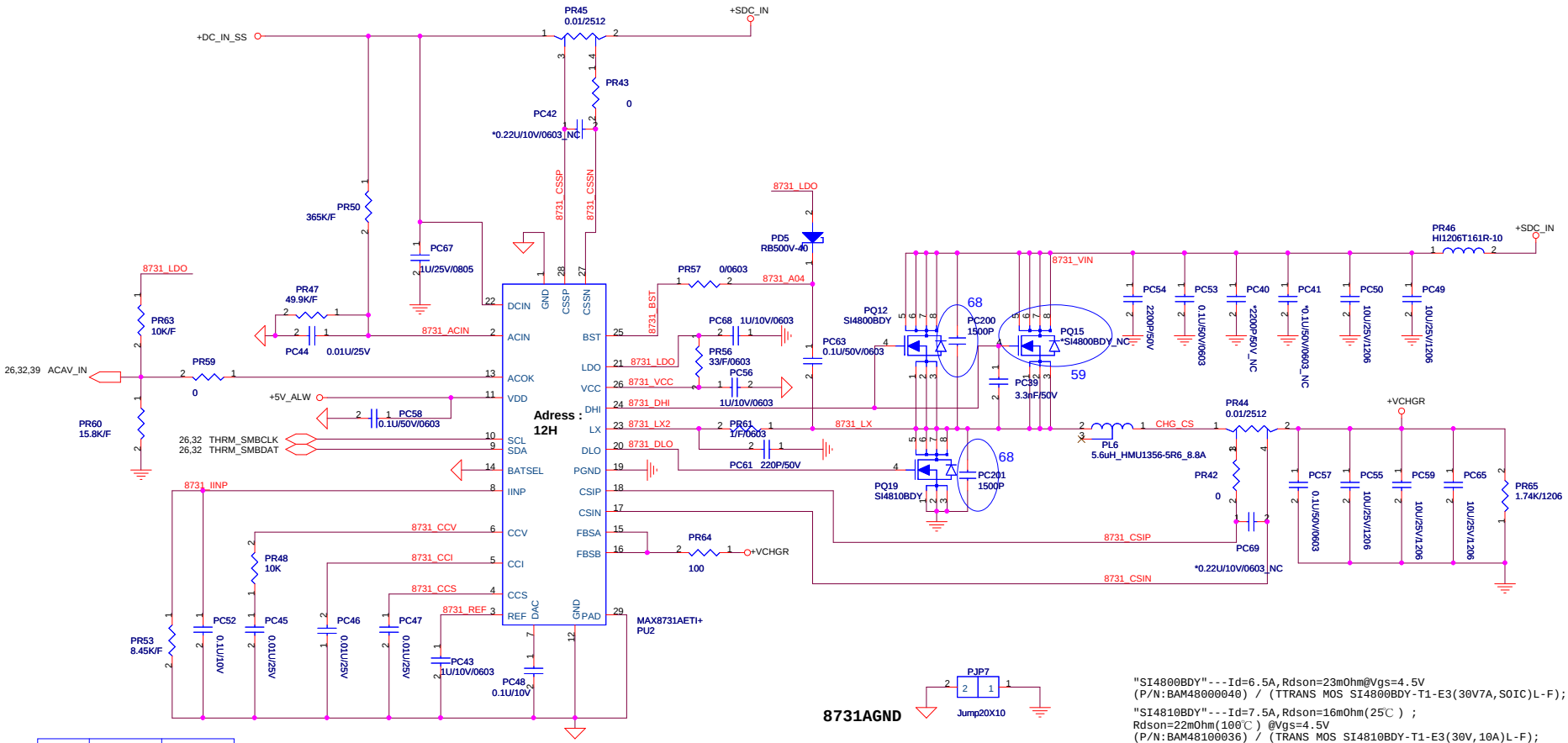

DVI
SMBUS
USB
SPDIF
LPC
VGA
S-VIDEO
LAN
MODEM
For Broadcom (5755)
SMBUS ADDRESS :
DOCK/APR Microprocessor -- 74H
DOCK USB/IDE Interface(FX2) -- 72H
DOCK SMbus -
Battery 16H
Charger 12H
IDE I/F 70H
D-BAY 72H
SIO 48H
Refer to LAYOUT NOTE1.
Use 2.5V_LOM for center tap on magnetics when using Broadcom; 1.8V_LOM for Intel only
LAYOUT NOTES:
Follow the Intel Platform Design Guideline routing recommendations for the following buses: PCI, DVI , LPC & USB.
LAYOUT NOTES1:
Terminators should be as close as possible to dock connector pins. Keep traces as short as possible.
FOX_QL00703-C4B4-FH
QUANTA COMPUTER
Docking Station CONN.
Wednesday, August 08, 2007
37 of 52


Non-iAMT
42 1.25V_RUN_PWRGD
R55 1 2 0
41 1.5V_RUN_PWRGD
41 1.05V_RUN_PWRGD
32 2.5V_RUN_PWRGD
R56 1 2 0
R57 1 2 0
R59 1 2 *0_NC
+5V_RUN
+5V_ALW
D8
SDMK0340L-7-F
R61 10K
Q10
MMBT3906-7-F
C133
0.1U/10V
R64
200K
C136
2200P/50V
R63 4.7K
Q11
MMST3904
+1.8V_RUN
+1.8V_SUS
D9
SDMK0340L-7-F
R65 10K
Q13
MMBT3906-7-F
C141
0.1U/10V
R67
200K
C138
2200P/50V
R66 4.7K
Q12
MMST3904
+3.3V_RUN
+3.3V_ALW
D10
SDMK0340L-7-F
R78 10K
Q15
MMBT3906-7-F
C144
0.1U/10V
R79
200K
C146
2200P/50V
R73 4.7K
Q14
MMST3904
+3.3V_RUN
R74
*2.2K_NC
+3.3V_SUS
R82
100K
ICH_PWRGD# 32
Q16
2N7002W-7-F
13,26,43 IMVP_PWRGD
26 RESET_OUT#
U11D
74AHC08PW
ICH_PWRGD 6,13
Keep Away from high speed buses
+3.3V_SUS
+3.3V_ALW
R58
20K
C137
0.1U/10V
U10A
NC7WZ14P6X_NL
C134
0.01U/25V
U10B
NC7WZ14P6X_NL
C142
0.1U/10V
U11A
74AHC08PW
20,26,28,45 RUN_ON
R60 0
U11B
74AHC08PW
RUNPWROK 26,27,43
5V_3V_1.8V_1.25V_RUN_PWRGD 27
26,45 SUS_ON
U11C
74AHC08PW
SUSPWROK 32
+3.3V_SUS
+3.3V_ALW
D13
SDMK0340L-7-F
R106 10K
Q18
MMBT3906-7-F
C178
0.1U/10V
R105
200K
C174
2200P/50V
D11
SDMK0340L-7-F
R86
200K
C156
0.1U/10V
U12
NC7SZ14P5X_NL
+5V_SUS
+5V_ALW
D14
SDMK0340L-7-F
R110 10K
Q20
MMBT3906-7-F
C181
0.1U/10V
R111
200K
C177
2200P/50V
D12
SDMK0340L-7-F
R95
200K
R83
200K
QUANTA
COMPUTER
Title
System Reset Circuit
Size
Document Number
DM6
Rev
1A
Date: Friday, June 08, 2007
Sheet 38 of 52

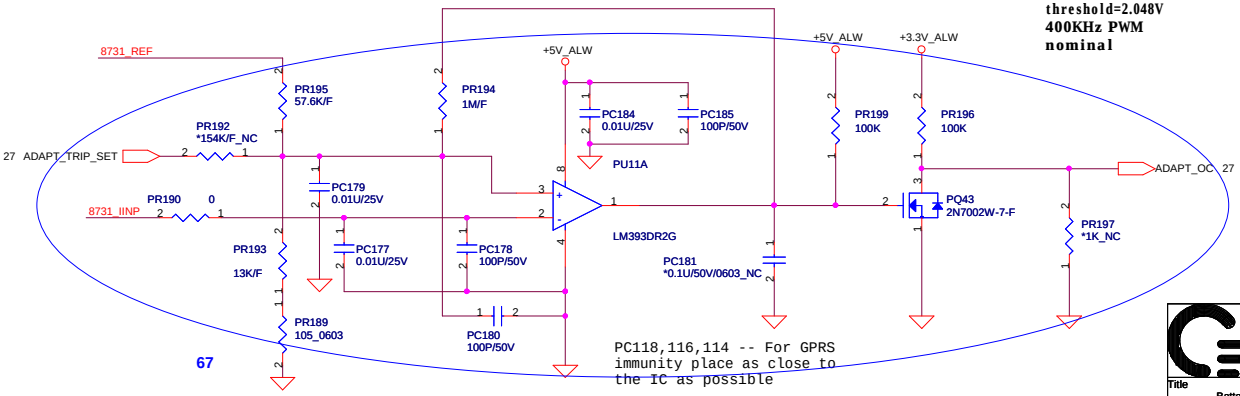


QUANTA COMPUTER

Title	Battery Selector	
Size	Document Number DM6	Rev 1A
Date: Friday, June 08, 2007	Sheet 39 of 52	



	DM6 (965GM)	DM6B (960GL)
PR195	V	X
PR190	V	X
PR193	V	X
PR189	V	X
PR194	V	X
PC179	V	X
PC177	V	X
PC178	V	X
PU11	V	X
PR197	X	V
PC180	V	X
PC184	V	X
PC185	V	X
PR196	V	X
PQ43	V	X
PR199	V	X
PR192	X	X
PC181	X	X



QUANTA COMPUTER		
Title	Battery Charger	
Size	Document Number DM6	Rev 1A
Date: Tuesday, August 07, 2007	Sheet 40 of 52	

M'08
+1.5V_RUN /+1.05V_VCCP /+3.3V_ALW /+3.3_RTC_LDO

Ton:OUT1/OUT2 Switching Frequency
VCC: 200kHz/300kHz
OPEN (REF): 400kHz/300kHz
GND: 400kHz/500kHz

1.5V +/- 5%
Thermal Design Current: 1950mA
Maximum Current: 2785mA
OCP: 3.7A

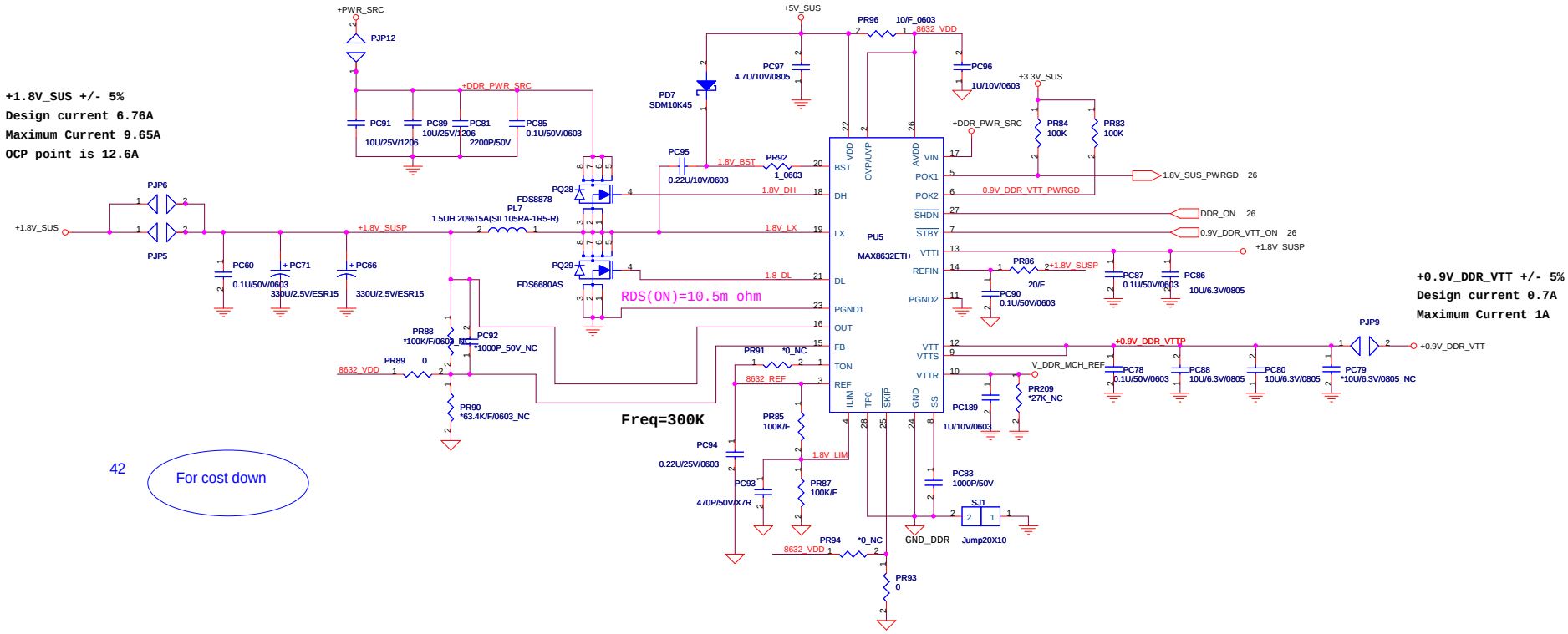
1.05V +/- 5%
Thermal Design Current: 10.7A
Maximum Current:15.29A
OCP: 20A

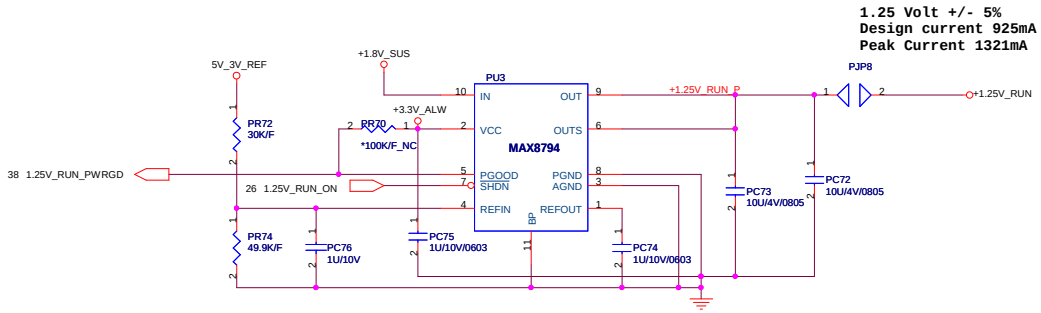
+PWR_SRC
PR19 HI1206T161R-10
PC30 10U/25V/1206
PC29 0.1U/50V/0805
PC28 2200P/50V
+DC2_PWR_SRC
PR151 0/0603
PC146 0.1U/25V/0603
PC18 10U/25V/1206
PC144 10U/25V/1206
PC21 0.1U/50V/0805
PC26 2200P/50V
PC23 0.1U/50V/0805
PC25 2200P/50V
+5V_VCC2
PC145 1U/10V/0805
+3.3V_RTC_LDO
PC148 0.1U/25V/0603
PR149 *0_NC
PR157 0
PR153 *0_NC
PR171 0/0603
PC152 *1U/10V/0805_NC
REF
PR152 *0_NC
PC147 0.1U/25V/0603_NC
PR156 PAD T72
PC157 0.1U/25V/0603
PR161 200K/F/0603
PR176 200K/F/0603
PC154 *0.1U/25V/0603_NC
PC165 0.1U/25V/0603
PC167 0.1U/25V/0603
PR178 1_0603
PR179 1_0603
PR180 10/0603
PR170 0
PC163 *0.1U/25V/0603_NC
PC166 1U/10V/0603
PJP1 Jump20X10
PR33 *178K/F_NC
PR32 *178K/F_NC
+1.5V_RUN
PJP4 POWER_JP
+1.5V_RUN_P
PC34 220U/2.5V
PC171 0.1U/25V/0603
PR165 *0/0603_NC
PR166 *0/0603_NC
PL5 3.8UH,30%6A(SIL104R-3R8PF)
PQ8 SI4914DY-T1-E3
1.5V_DH
1.5V_LX
1.5V_DL
PU10 MAX8778ETJ
LDOREFIN LDO VIN RTC ONLDO VCC TON REF
BYP OUT1 FB1 ILIM1 PGOOD1 EN1 DH1 LX1 PAD PAD PAD PAD
REFIN2 ILIM2 OUT2 SKIP# PGOOD2 EN2 DH2 LX2
BST1 DL1 VDD SECFB GND PGND DL2 BST2
POK1 EN1 POK2 EN2 1.05V_DH 1.05V_LX
1.05V_DL
PQ6 FDS6298
PQ7 FDMS8670S
1.05V_LX
PL4 MPO104-1R0
+1.05V_VCCP_P
+1.05V_VCCP
PJP2 POWER_JP
PJP3 POWER_JP
PC32 0.1U/25V/0603
PC31 330U/2.5V
PC33 330U/2.5V
RDS(ON)=27m ohm
RDS(ON)=5m ohm
+5V_ALV
+3.3V_SUS
POK2 1.05V_RUN_PWRGD 38
POK1 1.05V_RUN_PWRGD 38
EN1 1.5V_RUN_ON 26
EN2 PR175 0 1.05V_RUN_ON 27

Layout Notes:
Place C7 very near U1-pin19 and PU1-pin20.
Place C8 very near U1-pin3.
Place R19 very near U1-pin21.
Minimize loop including Q4, L2, C11, C12 and R19.
Minimize loop including Q2, L3, C17, C18, C19 and R19.
Route GNDA_DC2 using at least 25 mil trace width.
Minimize GNDA_DC2 trace length.
Place C15 near U1-pin7.
Place C20 near U1-pin5.
Place R7 near U1-pin11.
Place R12 near U1-pin31.
Place R3, C10 near U1-pins 24 and 25.
Place R2, C9 near U1-pins 16 and 17.
Route +1.05V_BOOT, +1.05V_BOOST, +1.5V_BOOT, +1.5V_BOOST using 25mil trace width and minimize lengths.
Connect large copper fill areas to PQ1, PQ2, PQ3 and Q4 signals for thermal improvement.
Minimize length of +1.5V_RUN_PL and +1.05V_VCCP_PL.
Place C1, C2, C3, C22 very near Q3-pins 5, 6, 7, 8.
Place C4, C5, C6, C23 very near Q1-pins 5, 6, 7, 8.
Route +DC2_PWR_SRC using 50 mil trace width and minimize length.
Route OUT1 and OUT2 away from inductor and switch-node. Sense Vout directly at output bulk cap.

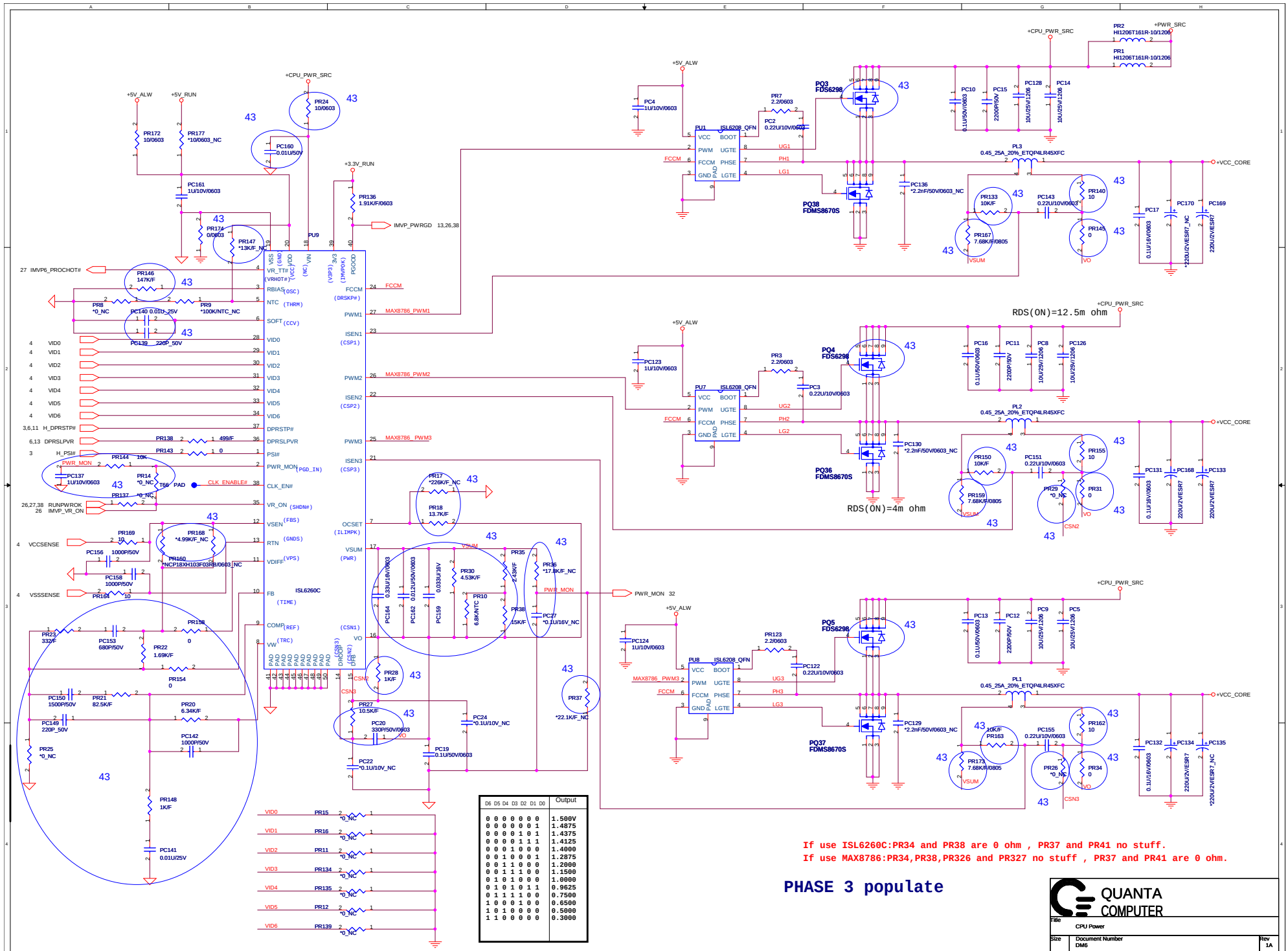
QUANTA COMPUTER

Title	1.5V,1.05V	
Size	Document Number DM6	Rev 1A
Date: Tuesday, August 07, 2007	Sheet 41 of 52	





QUANTA COMPUTER		
Title: 1.8V_SUS,1.5V_RUN,0.9V_VTT		
Size	Document Number: DM6	Rev: 1A
Date: 2005/4/21	Sheet 42 of 52	

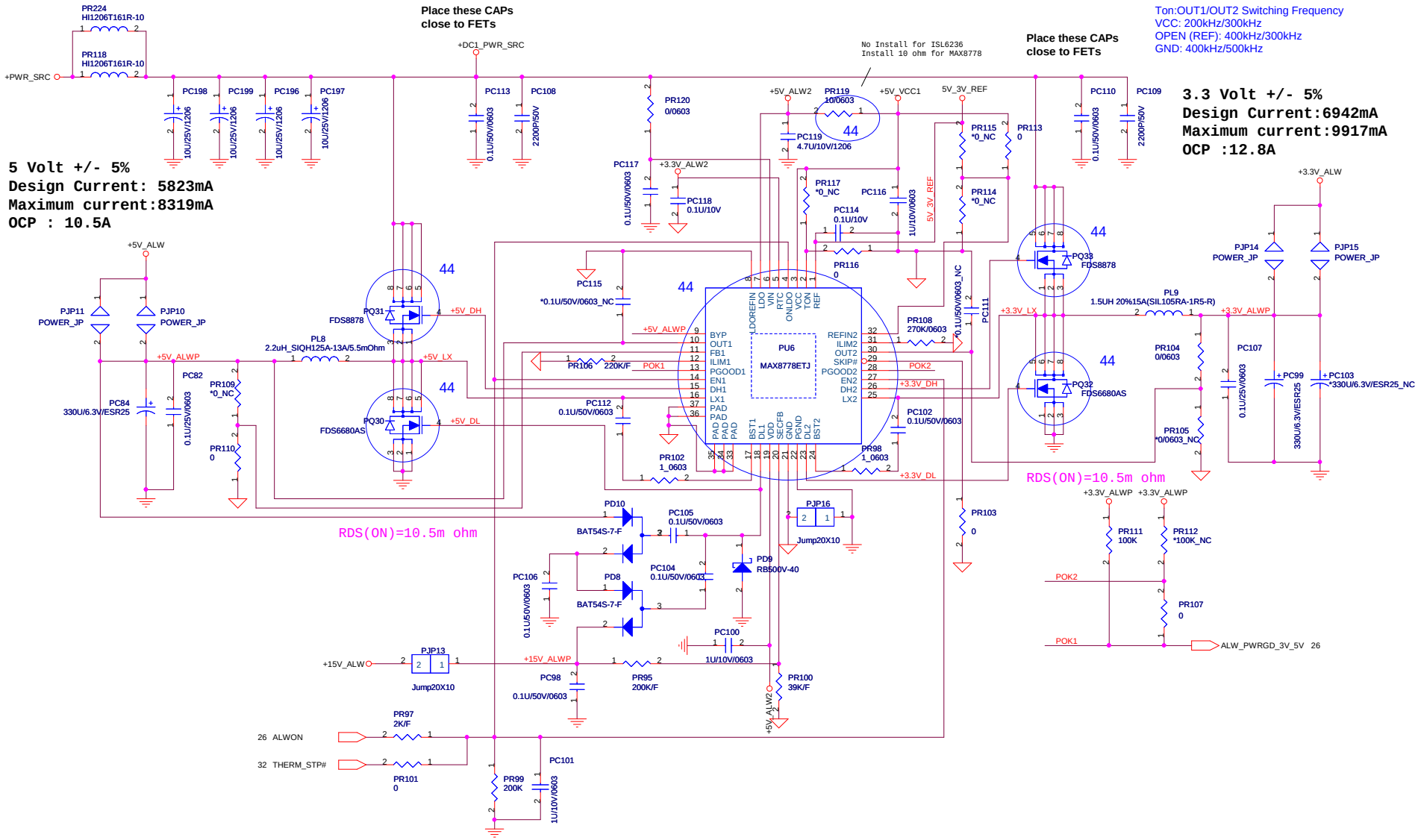


D6 D5 D4 D3 D2 D1 D0	Output
0 0 0 0 0 0 0	1.500V
0 0 0 0 0 0 1	1.4875
0 0 0 0 1 0 1	1.4375
0 0 0 0 1 1 1	1.4125
0 0 0 1 0 0 0	1.4000
0 0 1 0 0 0 1	1.2875
0 0 1 1 0 0 0	1.2000
0 0 1 1 1 0 0	1.1500
0 1 0 1 0 0 0	1.0000
0 1 0 1 0 1 1	0.9625
0 1 1 1 1 0 0	0.7500
1 0 0 0 1 0 0	0.6500
1 0 1 0 0 0 0	0.5000
1 1 0 0 0 0 0	0.3000

QUANTA COMPUTER

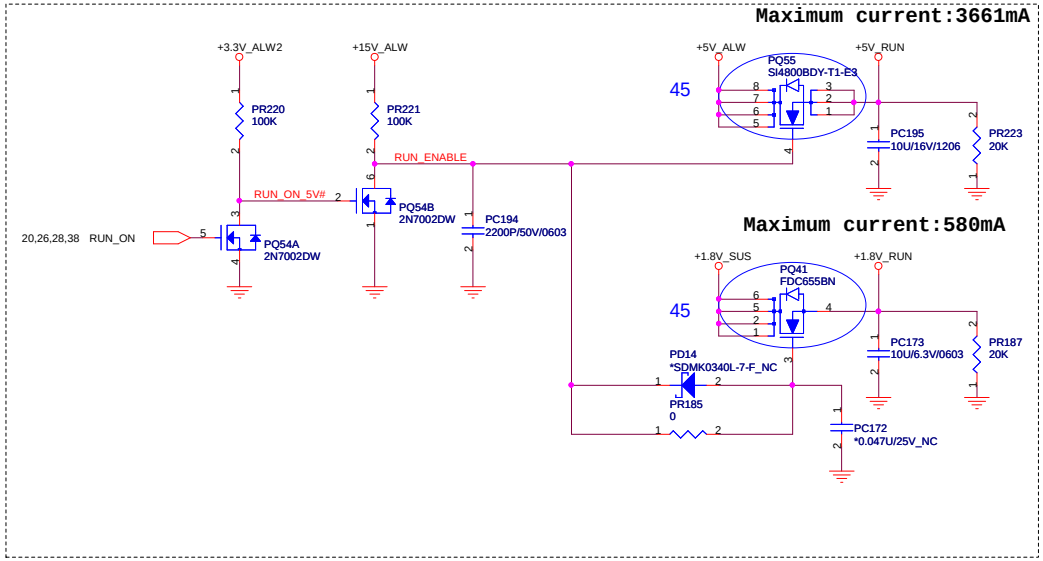
Title	CPU Power	
Size	Document Number DM6	Rev 1A
Date: Thursday, August 09, 2007	Sheet 43 of 52	

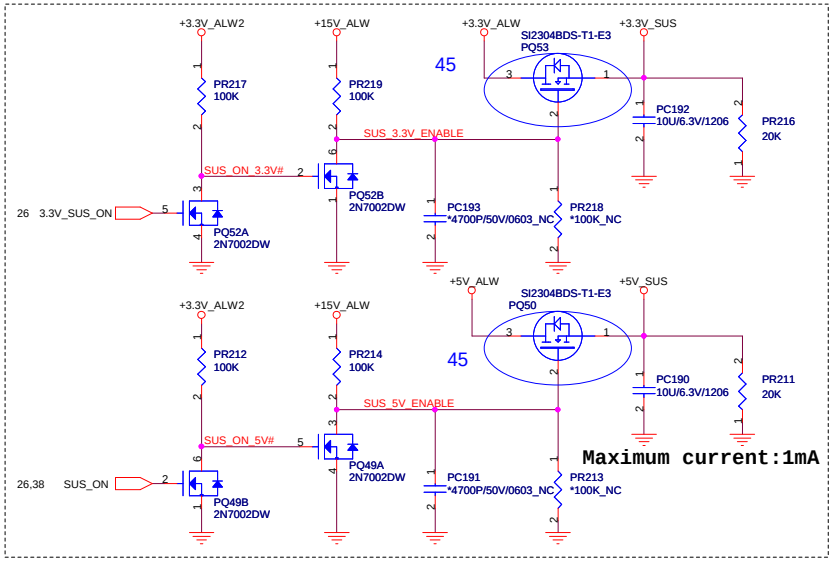
DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+15V_ALW

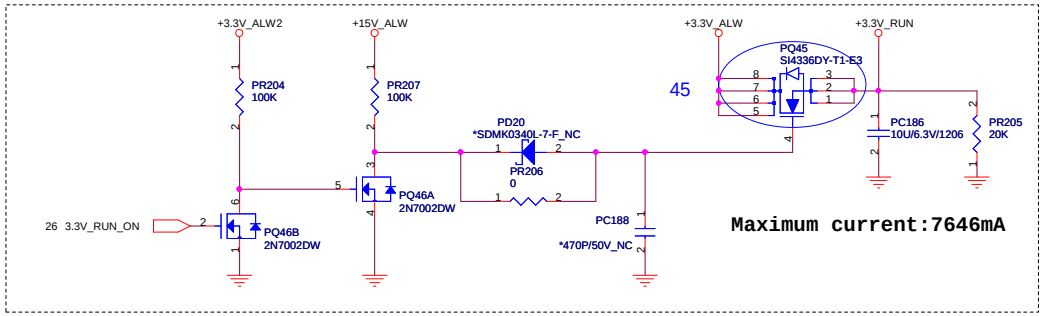


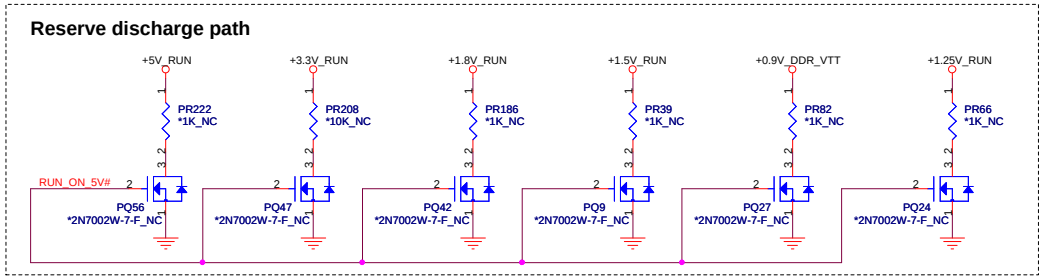
Title	3VALW,5V,3V, Power On
Size	Document Number DM6
Rev	1A
Date:	Friday, June 08, 2007
Sheet	44 of 52

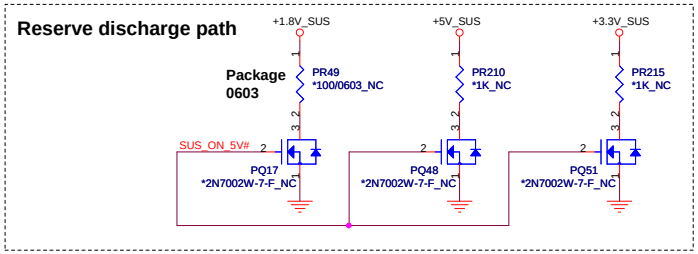
QUANTA COMPUTER





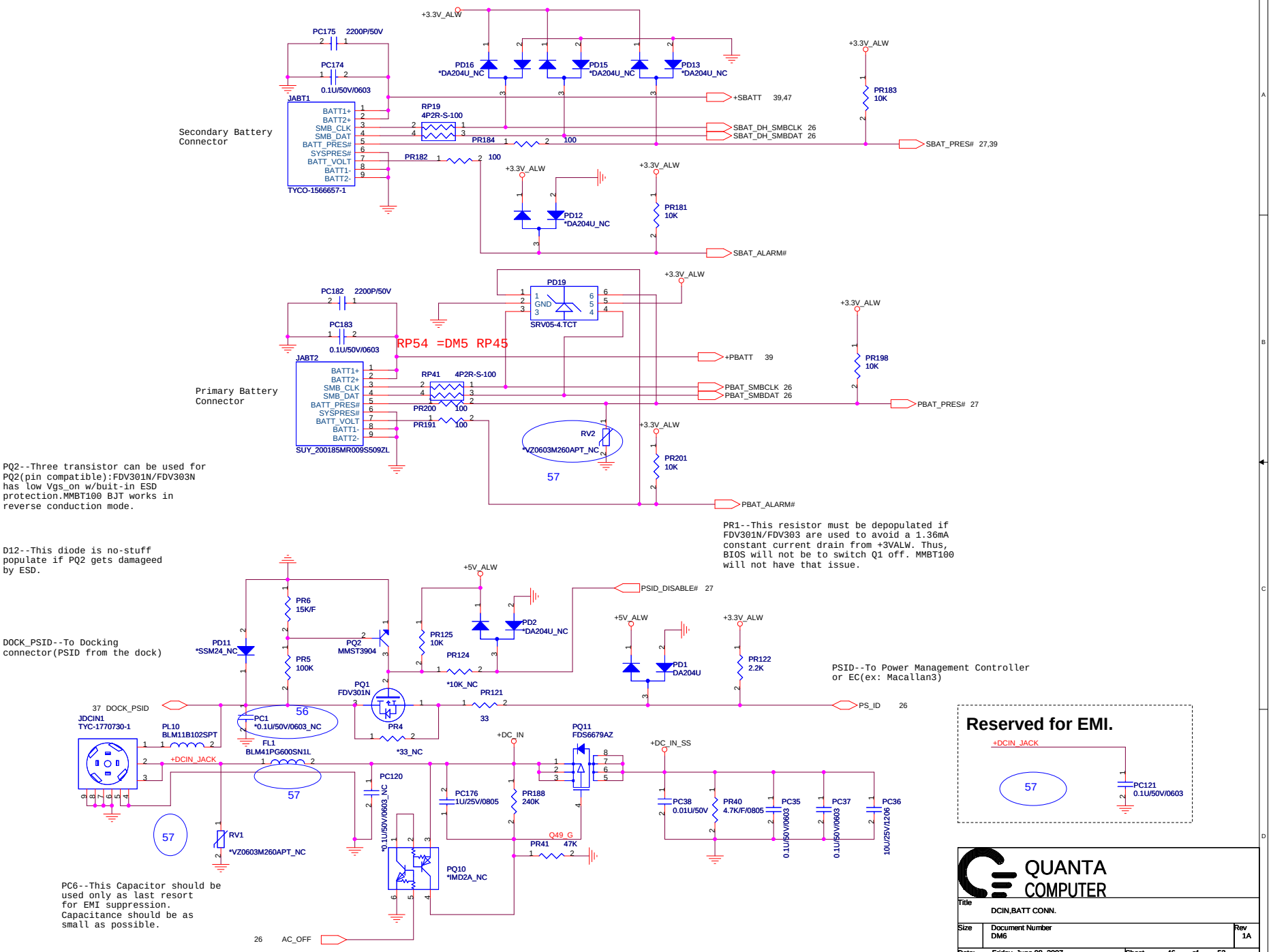






QUANTA COMPUTER

Title	RUN POWER SW	
Size	Document Number DM6	Rev 1A
Date: Friday, June 08, 2007	Sheet 45 of 52	


Secondary Battery Connector
JABT1
TYCO-1566657-1
BATT1+
BATT2+
SMB_CLK
SMB_DAT
BATT_PRES#
SYSPRES#
BATT_VOLT
BATT1-
BATT2-
PC175 2200P/50V
PC174 0.1U/50V/0603
RP19 4P2R-S-100
PR182 100
PR184 100
PR183 10K
PR181 10K
PD16 *DA204U_NC
PD15 *DA204U_NC
PD13 *DA204U_NC
PD12 *DA204U_NC
+3.3V_ALW
+SBATT 39,47
SBAT_DH_SMBCLK 26
SBAT_DH_SMBDAT 26
SBAT_PRES# 27,39
SBAT_ALARM#
Primary Battery Connector
JABT2
SUY_200185MR009S509ZL
PC182 2200P/50V
PC183 0.1U/50V/0603
RP54 =DM5 RP45
RP41 4P2R-S-100
PR200 100
PR191 100
PR198 10K
PR201 10K
PD19 SRV05-4.TCT
RV2 *VZ0603M260APT_NC
+PBATT 39
PBAT_SMBCLK 26
PBAT_SMBDAT 26
PBAT_PRES# 27
PBAT_ALARM#
PQ2--Three transistor can be used for PQ2(pin compatible):FDV301N/FDV303N has low Vgs_on w/buit-in ESD protection.MMBT100 BJT works in reverse conduction mode.
D12--This diode is no-stuff populate if PQ2 gets damageed by ESD.
PR1--This resistor must be depopulated if FDV301N/FDV303 are used to avoid a 1.36mA constant current drain from +3VALW. Thus, BIOS will not be to switch Q1 off. MMBT100 will not have that issue.
DOCK_PSID--To Docking connector(PSID from the dock)
PR6 15K/F
PR5 100K
PQ2 MMST3904
PD11 *SSM24_NC
PR125 10K
PR124 *10K_NC
PD2 *DA204U_NC
PD1 DA204U
PR122 2.2K
PQ1 FDV301N
PR121 33
PR4 *33_NC
PC1 *0.1U/50V/0603_NC
PS_ID 26
PSID_DISABLE# 27
PSID--To Power Management Controller or EC(ex: Macallan3)
37 DOCK_PSID
JDCIN1 TYC-1770730-1
PL10 BLM11B102SPT
FL1 BLM41PG600SN1L
+DCIN_JACK
RV1 *VZ0603M260APT_NC
PC120 *0.1U/50V/0603_NC
PQ10 *IMD2A_NC
PC176 1U/25V/0805
PR188 240K
PR41 47K
Q49_G
PQ11 FDS6679AZ
+DC_IN
+DC_IN_SS
PC38 0.01U/50V
PR40 4.7K/F/0805
PC35 0.1U/50V/0603
PC37 0.1U/50V/0603
PC36 10U/25V/1206
PC6--This Capacitor should be used only as last resort for EMI suppression. Capacitance should be as small as possible.
26 AC_OFF
Reserved for EMI.
+DCIN_JACK
PC121 0.1U/50V/0603
QUANTA COMPUTER
Title DCIN,BATT CONN.
Size Document Number DM6
Rev 1A
Date: Friday, June 08, 2007
Sheet 46 of 52

PV14 PAD138X98XH GND
PV7 PAD138X98XH GND
PV10 PAD138X98XH GND
PV12 PAD138X98XH GND

PV15 PAD138X98XH GND
PV16 PAD138X98XH GND
PV6 PAD138X98XH GND
PV9 *PAD138X98XH_NC GND

PV13 PAD138X98XH GND
PV11 PAD138X98XH GND
PV1 PAD138X98XH GND

PV4 PAD138X98XL GND
PV5 PAD138X98XL GND
PV8 PAD138X98XL GND
PV2 PAD138X98XL GND
PV3 *PAD138X98XL_NC GND

H22 h-c315d126p2-4
H1 h-c315d126p2-4
H21 h-c315d126p2-4
H20 h-c315d126p2-2
H7 h-c236d126p2-4
H16 h-c315d126p2-4
H17 H-C315D110P2-4
H14 h-c315d126p2-2
H18 h-c315d126p2-4
H12 H-C315I166D126P2

+1.05V_VCCP
C479 2200P
C424 2200P
+3.3V_RUN

+1.05V_VCCP C317 2200P +PWR_SRC
+1.5V_RUN C332 2200P +PWR_SRC
+5V_ALW C279 2200P +3.3V_RUN
+1.8V_SUS C465 2200P +PWR_SRC
+1.5V_RUN C494 2200P +1.05V_VCCP

Stitching caps

+SBATT C514 2200P +PWR_SRC
+5V_ALW C119 2200P +PWR_SRC
+5V_ALW C122 2200P +PWR_SRC
+SBATT C457 2200P +PWR_SRC
+1.5V_RUN C616 2200P +PWR_SRC

Stitching caps for IDE traces referencing to SVCC

+3.3V_RUN C552 2200P +3.3V_ALW
+3.3V_RUN C533 2200P +3.3V_ALW
+3.3V_RUN C606 2200P +PWR_SRC
+3.3V_RUN C211 2200P +1.05V_VCCP
+3.3V_RUN C520 2200P +1.05V_VCCP
+3.3V_ALW C553 2200P +PWR_SRC
+1.5V_RUN C632 2200P +PWR_SRC

Stitching caps for PCI traces referencing to SVCC

CPU SCREW HOLES

H5 H-C236D98I142BC276P2
H6 H-C236D98I142BC276P2
H9 H-C236D98I142BC276P2
H8 H-C236D98I142BC276P2

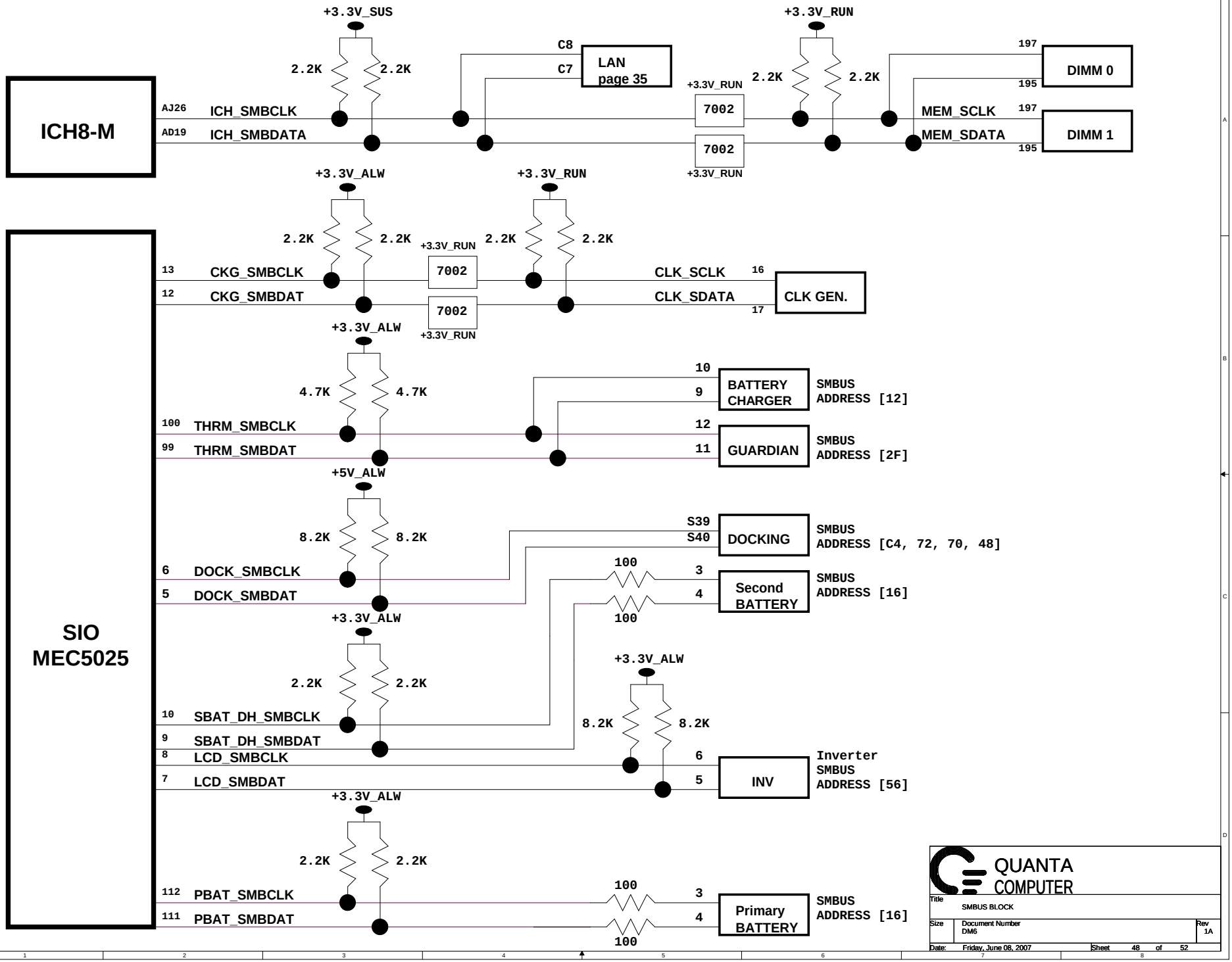
H11 h-c236d110p2-4
H10 h-TC276BC236D110P2-4
H19 h-c315d118p2-4
H13 h-c354d126p2

H4 H-TC276BC236D126P2
H3 H-C276D169P2
H2 H-TC256BC236D126P2

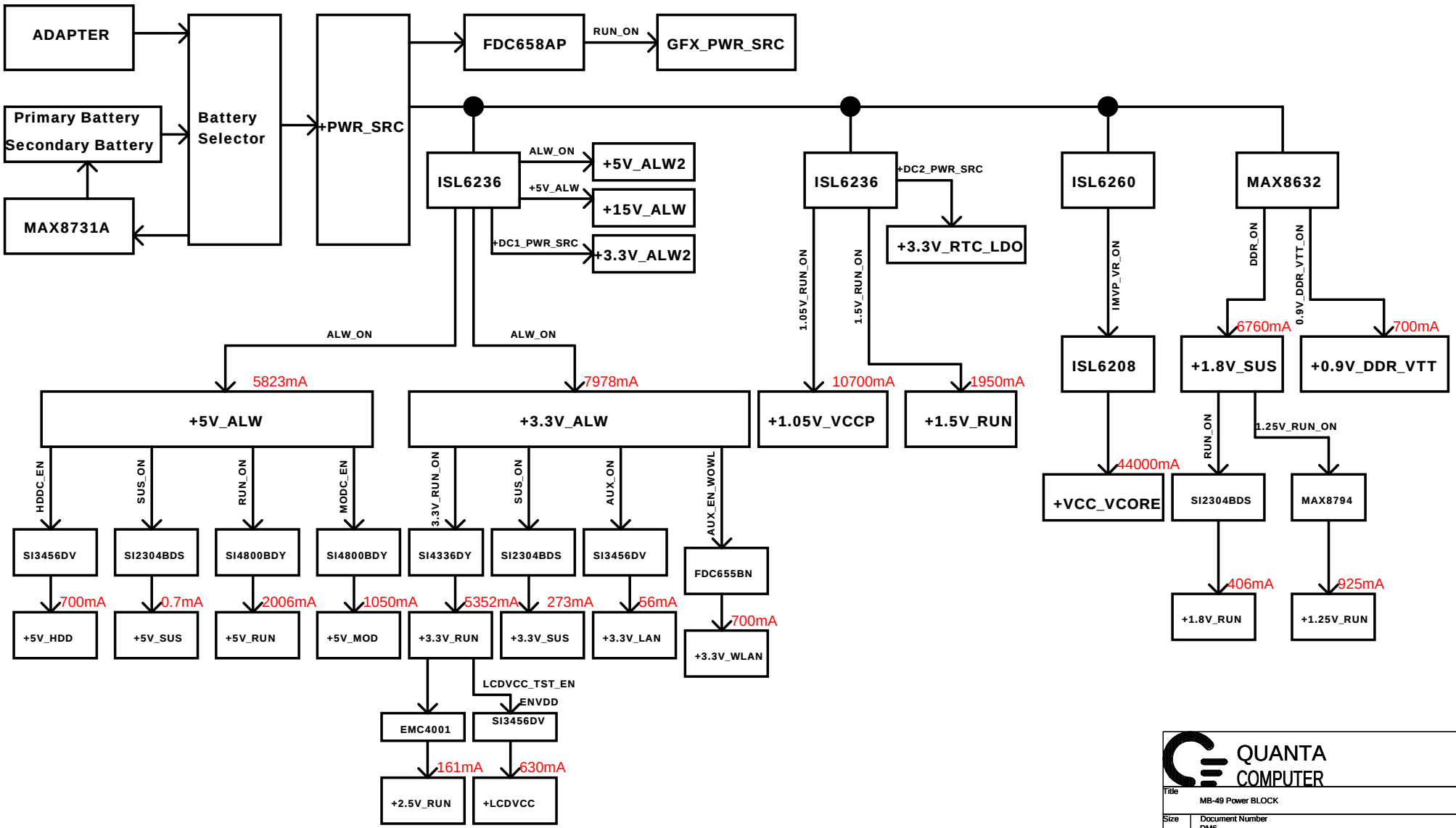
H15 H-OB189X28D189X28N
H24

QUANTA COMPUTER

Title	SCREW PAD	
Size	Document Number DM6	Rev 1A
Date: Friday, June 08, 2007	Sheet 47 of 52	


ICH8-M
AJ26
ICH_SMBCLK
AD19
ICH_SMBDATA
+3.3V_SUS
2.2K
2.2K
C8
C7
LAN
page 35
+3.3V_RUN
7002
7002
+3.3V_RUN
+3.3V_RUN
2.2K
2.2K
197
DIMM 0
195
MEM_SCLK
197
MEM_SDATA
DIMM 1
195
SIO
MEC5025
+3.3V_ALW
2.2K
2.2K
+3.3V_RUN
13
CKG_SMBCLK
12
CKG_SMBDAT
7002
7002
+3.3V_RUN
+3.3V_RUN
2.2K
2.2K
CLK_SCLK
16
CLK_SDATA
17
CLK GEN.
+3.3V_ALW
4.7K
4.7K
100
THRM_SMBCLK
99
THRM_SMBDAT
10
9
BATTERY
CHARGER
SMBUS
ADDRESS [12]
12
11
GUARDIAN
SMBUS
ADDRESS [2F]
+5V_ALW
8.2K
8.2K
6
DOCK_SMBCLK
5
DOCK_SMBDAT
S39
S40
DOCKING
SMBUS
ADDRESS [C4, 72, 70, 48]
100
100
3
4
Second
BATTERY
SMBUS
ADDRESS [16]
+3.3V_ALW
2.2K
2.2K
10
SBAT_DH_SMBCLK
9
SBAT_DH_SMBDAT
8
LCD_SMBCLK
7
LCD_SMBDAT
+3.3V_ALW
8.2K
8.2K
6
5
INV
Inverter
SMBUS
ADDRESS [56]
+3.3V_ALW
2.2K
2.2K
112
PBAT_SMBCLK
111
PBAT_SMBDAT
100
100
3
4
Primary
BATTERY
SMBUS
ADDRESS [16]
QUANTA
COMPUTER
Title
SMBUS BLOCK
Size
Document Number
DM6
Rev
1A
Date:
Friday, June 08, 2007
Sheet
48
of
52

Power Design Block Diagram 2007/5/29



QUANTA COMPUTER

Title	MB-49 Power BLOCK	
Size	Document Number DM6	Rev 1A
Date: Friday, June 08, 2007	Sheet 49 of 52	