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# VENICE

CPU : DOTHAN  
 Chip Set : ALVISO (GMCH)  
 Remarks : 915GM

Model Name : VENICE Main  
 PCB Code : BA41-00454A  
 Dev. Step : QT  
 Revision : A00  
 Update : 2004.12.10

DRAW	CHECK	APPROVAL
SE LEE	MK KIM	BL LEE

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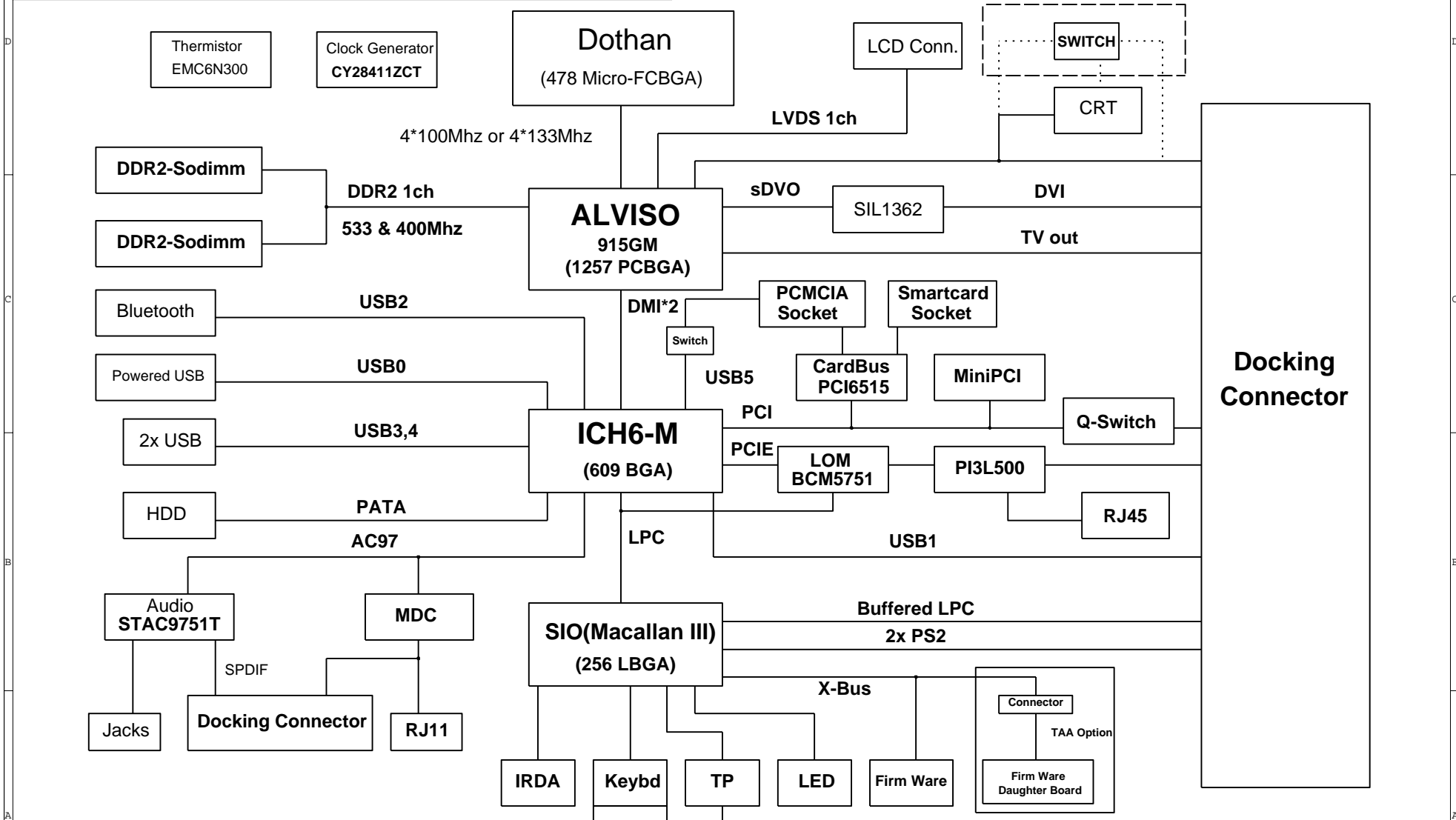
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## SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

### PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
Docking	AD24	0	A
Cardbus	AD17	1	D,C
MiniPCI SLOT	AD19	3	B,D
USB	AD29(internal)		
		Programable	
Hub to PCI	AD30(internal)		
LPC bridge/IDE/AC97/SMBUS	AD31(internal)		
AGP	AD17(internal)		
Internal MAC	AD24(internal)		
AC Link	-		

### I2 C / SMB Address

Devices	Address	Hex	Bus
<b>ICH6</b>	<b>Master</b>	-	<b>SMBUS Master</b>
CK-410M (Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable
SODIMM0	1010 000x	A0h	-
SODIMM1	1010 001X	A2h	-
SSCG	1101-010x	D4h	Spread spectrum Clock Generator
BCM	1100-100x	C8h	-
PWR USB	-	-	-
<b>MAC III</b>	<b>Master</b>	-	
On b'd Diagnostic	1010 001x	A2h	-
Inverter	0101 100x	58h	-
Battery	0001 011h	16h	-
Smart Charger	0001 001x	12h	-
THERMISTER	0101 111x	5Eh	-
<b>GMCH</b>	<b>Master</b>	-	<b>I2C Bus</b>
EDID	1010 000x	A0h	LCD information
DVI	0111 000x	70h	

### USB PORT Assign

PORT NUMBER	ASSIGNED TO
0	SYSTEM PORT (Left, Powered USB)
1	Docking
2	BLUETOOTH
3	SYSTEM PORT #1 (Rear)
4	SYSTEM PORT #2 (Rear)
5	Expresscard
6	RFU
7	RFU

### POWER

P5V_ALW	P3.3V_ALW	P3.3V_LAN	P2.5V_LAN	P5V_AUX	P3.3V_AUX	P1.8V_AUX	P1.5V_AUX	MEM_VREF	P5V	P3.3V	P2.5V	P1.8V	P1.5V	MEM_0.9	VTT	VCC_CORE
MAC III	BCM5751M	ICH6	ICH6	ICH6	G MCH	ICH6	Memory	ICH4	ICH6	GMCH	DVI	MGM	Memory	CPU	CPU	
ICH6-M	LED	USB	MINI-PCI	SODIMM	ICH6	Memory	ICH4	PCI6515	PCI6515	ICH	DVI	ICH6	GMCH	CPU		
Flash Memory		STAC9751	THERMISTOR					MINI-PCI	MINI-PCI							
Thermistor								STAC9751	STAC9751							
								MDC	SODIMM							
								MAC III	MAC III							
								HDD	LED							
								TOUCHPAD	MDC							
								PCI BUFFER	HDD							
									FIR							
									CLOCK							
									BLUETOOTH							

### Voltage Rails

VDC	Primary DC system power supply (9 to 21V)
P5V_ALW	5.0V LDO power rail for MAC III(off in S4-S5 without AC Adapter)
P5V_AUX	5.0V power rail (off in S4-S5)
P3.3V_AUX	3.3V power rail (off in S4-S5)
P3.3V_LAN	3.3V power rail (off in S4-S5 without AC ADAPTER)
P2.5V_LAN	2.5V power rail (off in S4-S5 without AC adapter)
P1.2V_LAN	1.25V power rail (off in S4-S5 without AC adapter)
P3.3V_ALW	3.3V LDO power rail for MAC III(off in S4-S5 without AC Adapter)
P1.8V_AUX	GMCH/DDR II Power Source(off in S4-S5)
VCC_CORE	Core voltage for DOTHAN CPU (0.74-1.30V)
VTT	GMCH core, CPU/GMCH FSB Termination.
P5V	5.0V switched power rail (off in S3-S5)
P1.5V	1.5V switched power rail (off in S3-S5)
P1.8V	1.8V switched power rail (off in S3-S5) SIL1362(DVI)
P2.5V	2.5V switched power rail (off in S3-S5)
P3.3V	3.3V switched power rail (off in S3-S5)
MEM_0.9V	DDR2 Termination (off in S3-S5)

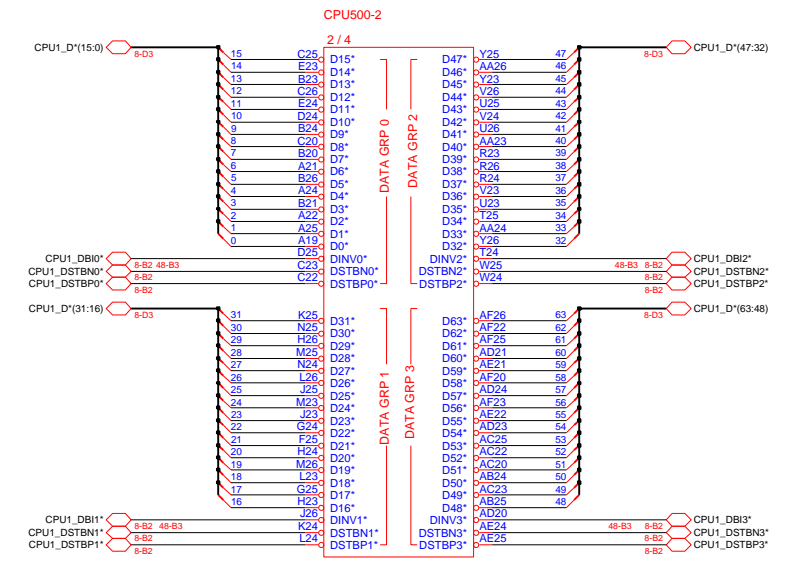
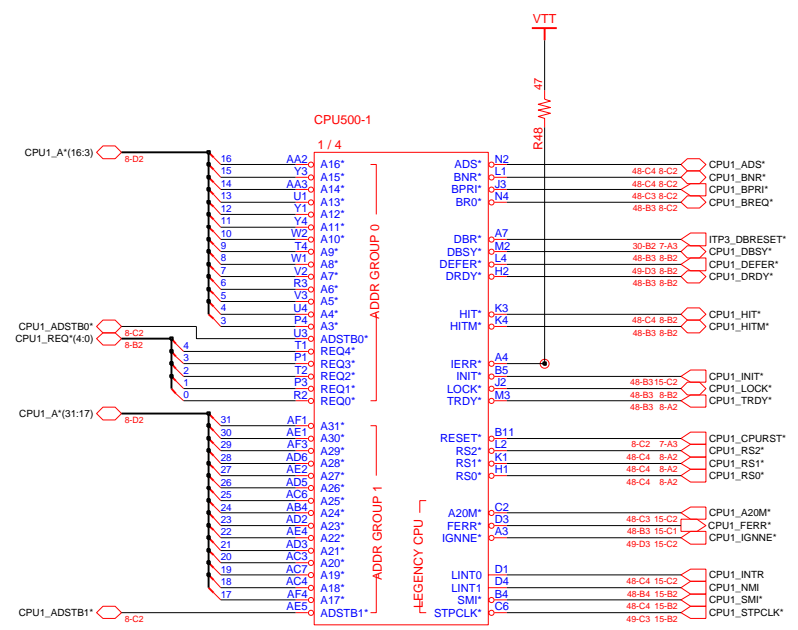
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APPROVAL	LEE, BL	REV	A00			
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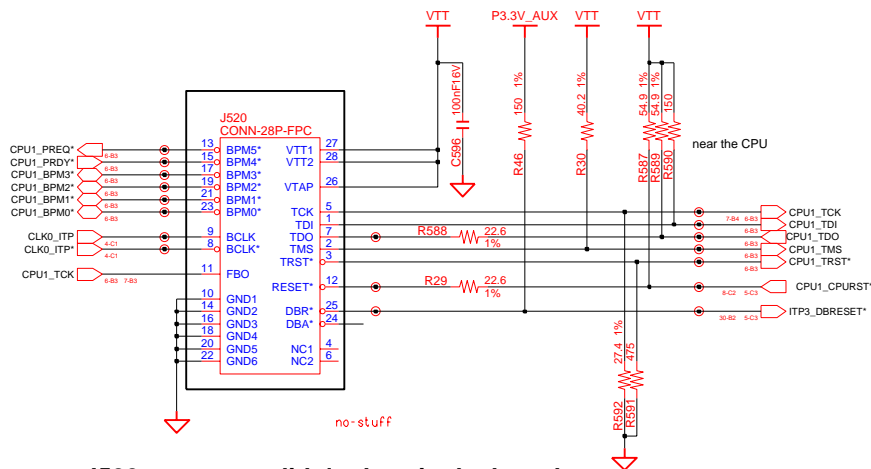
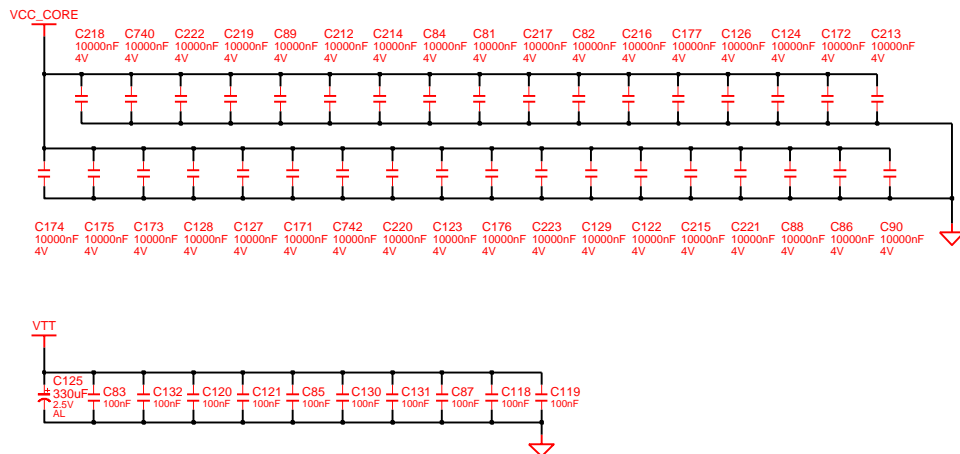
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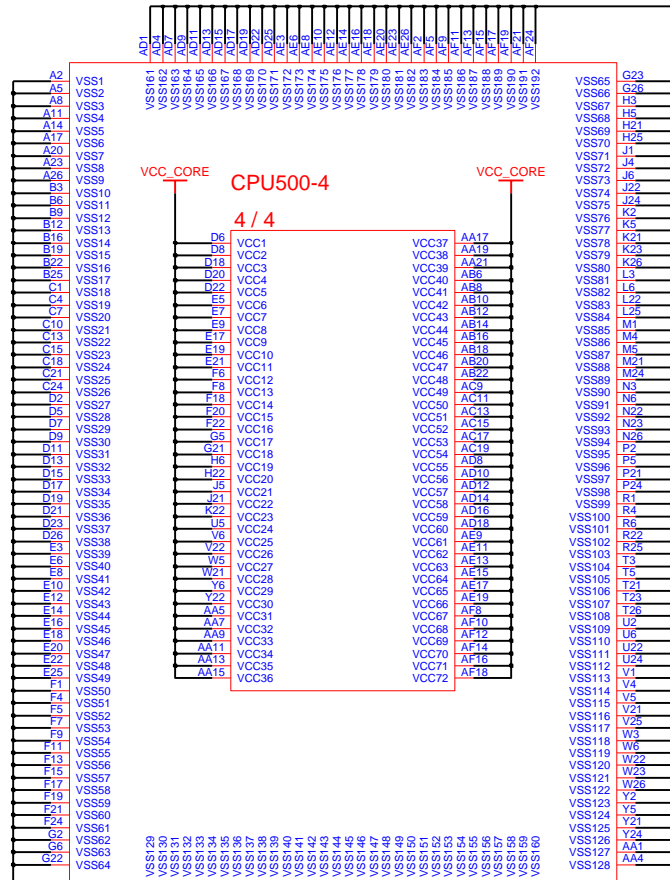
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J520 connector didn't place in the board.



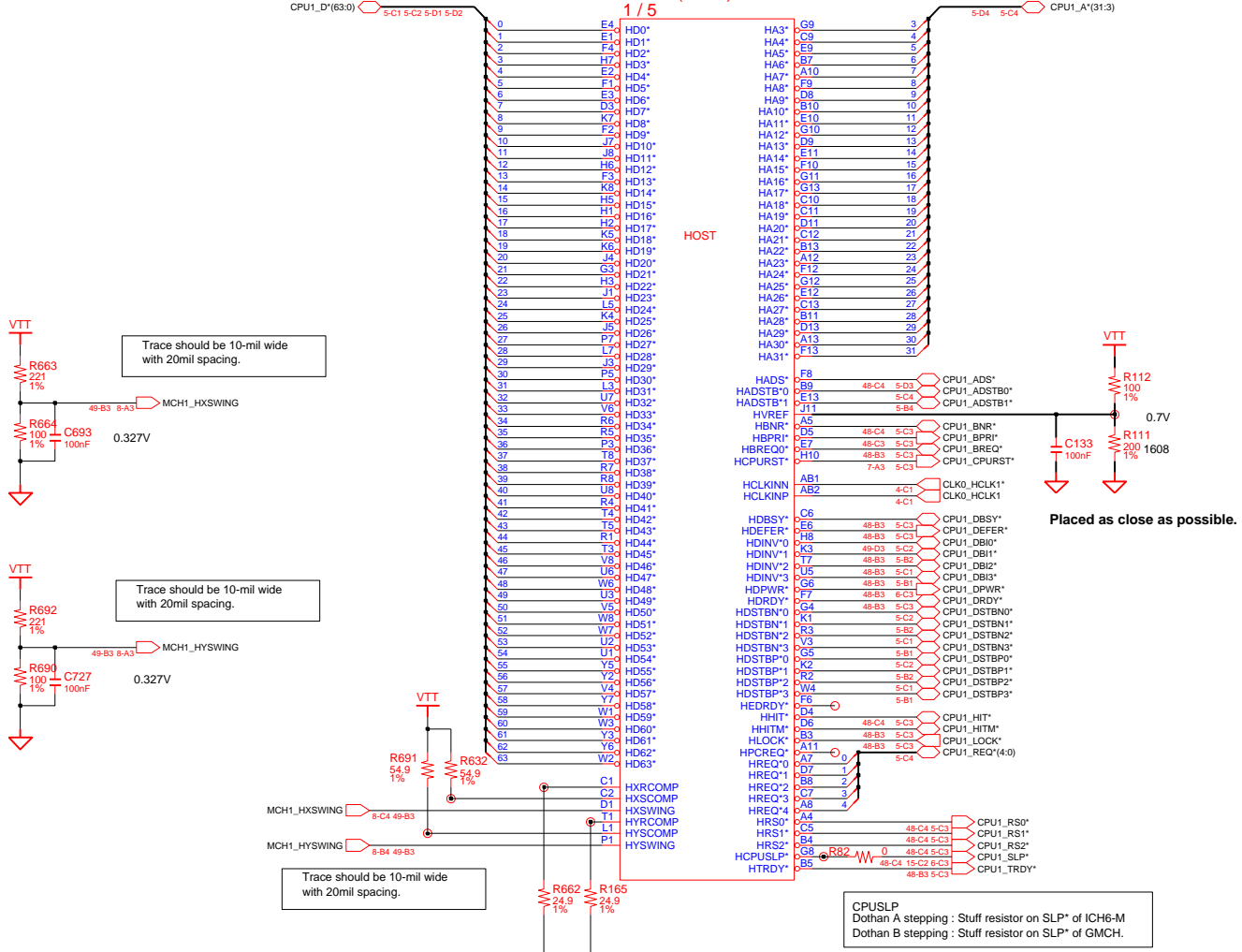
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U514-1  
915GM(DEL)  
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TV DAC		
Component	Composite	
A	Pb	CVBS
B	Y	
C	Pr	

Place 75 ohm termination resistors close to GMCH

RED, GREEN, BLUE are GND referenced

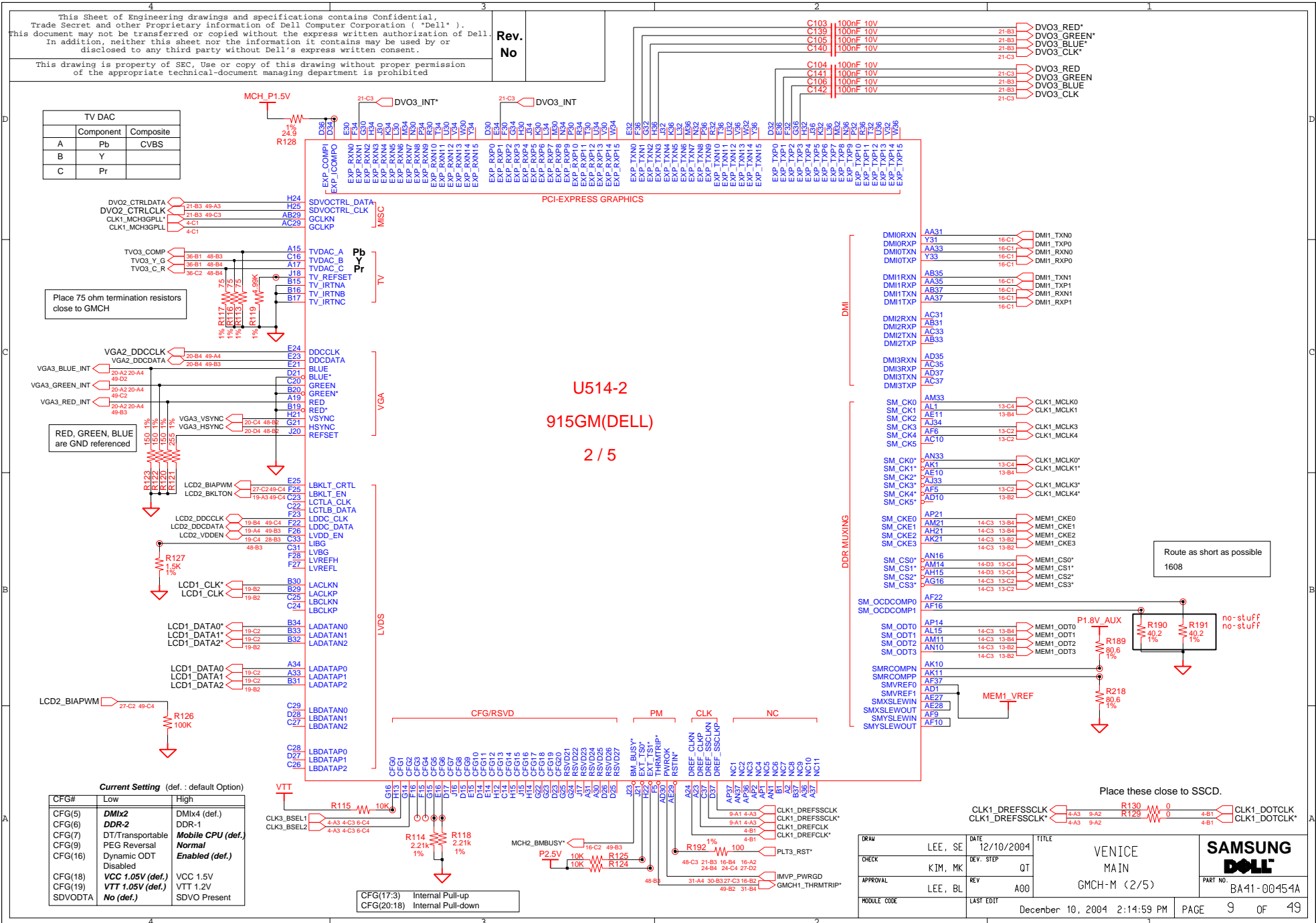
Route as short as possible 1608

Current Setting (def.: default Option)

CFG#	Low	High
CFG(5)	DMix2	DMix4 (def.)
CFG(6)	DDR-2	DDR-1
CFG(7)	DT/transportable	Mobile CPU (def.)
CFG(9)	PEG Reversal	Normal
CFG(16)	Dynamic ODT Disabled	Enabled (def.)
CFG(18)	VCC 1.05V (def.)	VCC 1.5V
CFG(19)	VTT 1.05V (def.)	VTT 1.2V
SDVODTA	No (def.)	SDVO Present

CFG(17:3) Internal Pull-up  
CFG(20:18) Internal Pull-down

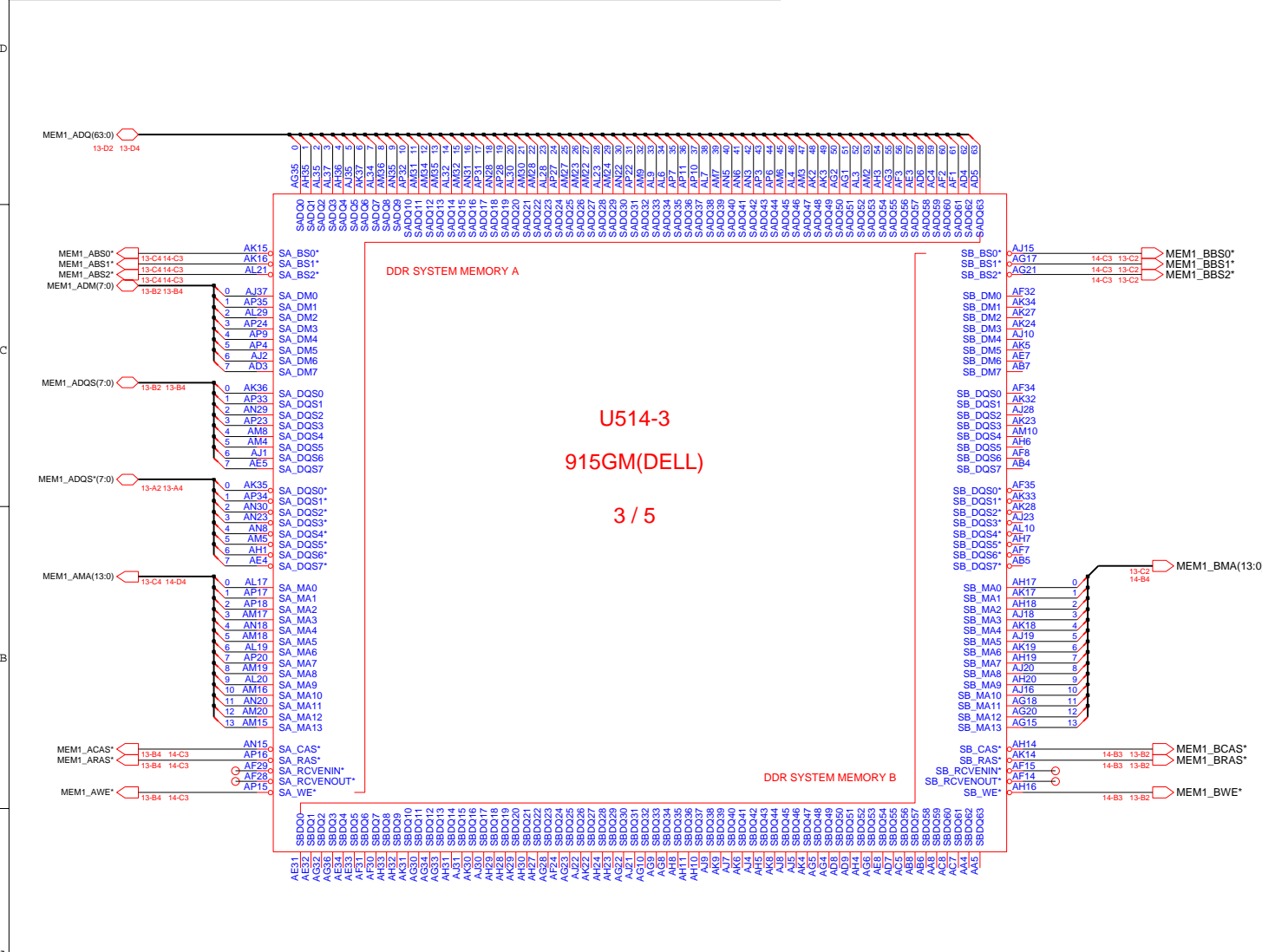
U514-2  
915GM(DELLE)  
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**DDR SYSTEM MEMORY A**

**U514-3**

**915GM(DELL)**

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**DDR SYSTEM MEMORY B**

**DDR/DDR2 Common Signal Mapping**  
**Single Channel Mode Signal Mapping**

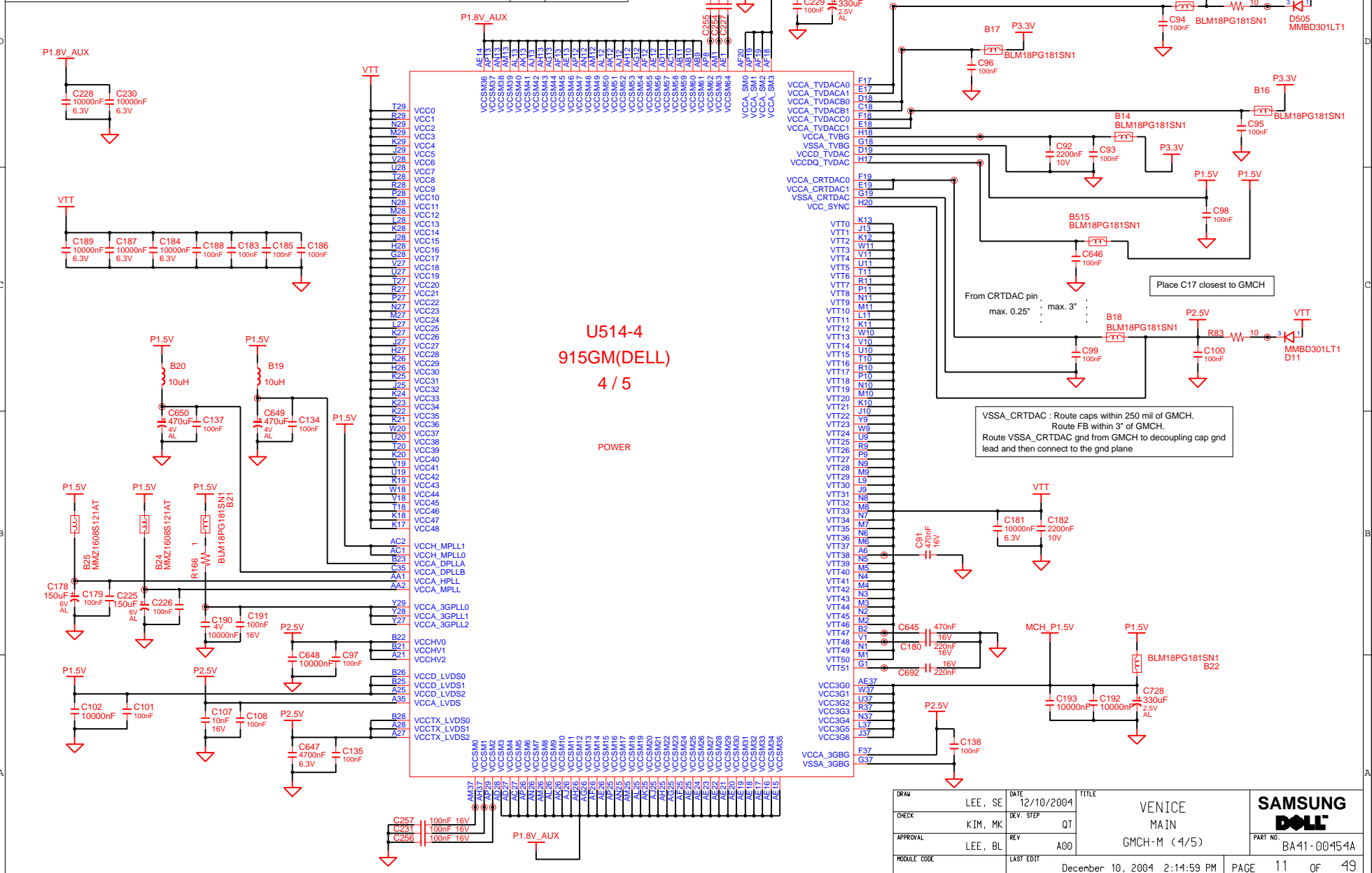
Single Channel Signal Mapping.	
SO-DIMM 0	SO-DIMM 1
SM_CK* [1:0]	SM_CK [4:3]
SM_CK* [1:0] (DDR2 support)	SM_CK* [4:3] (DDR2 support)
SM_CS* [1:0]	SM_CS* [3:2]
SM_CKE [1:0]	SM_CK [3:2]
SM_ODT [1:0] (DDR2 support)	SM_ODT [3:2] (DDR2 support)
SA_BS [2:0]	SB_BS [2:0]
SA_MA [13:0]	SB_MA [13:0]
SA_RAS*	SB_RAS*
SA_CAS*	SB_CAS*
SA_WE*	SB_WE*
SA_DQ [63:0]	
SA_DQS [7:0]	
SA_DQS* [7:0]	
SA_DM [7:0]	

DRAW	LEE, SE	DATE	12/10/2004	TITLE	VENICE MAIN	<b>SAMSUNG</b> <b>DELL</b> PART NO. BA41-00454A
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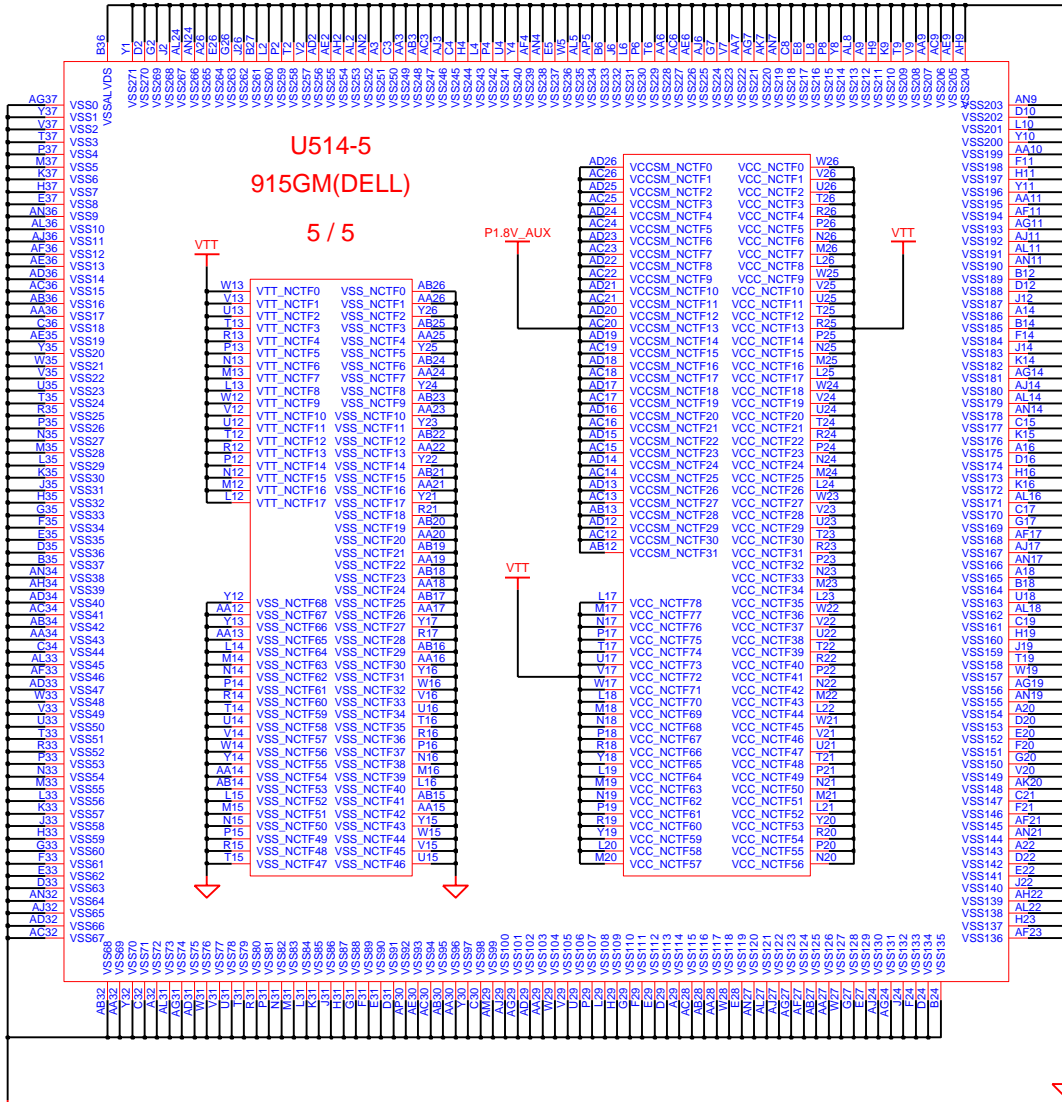
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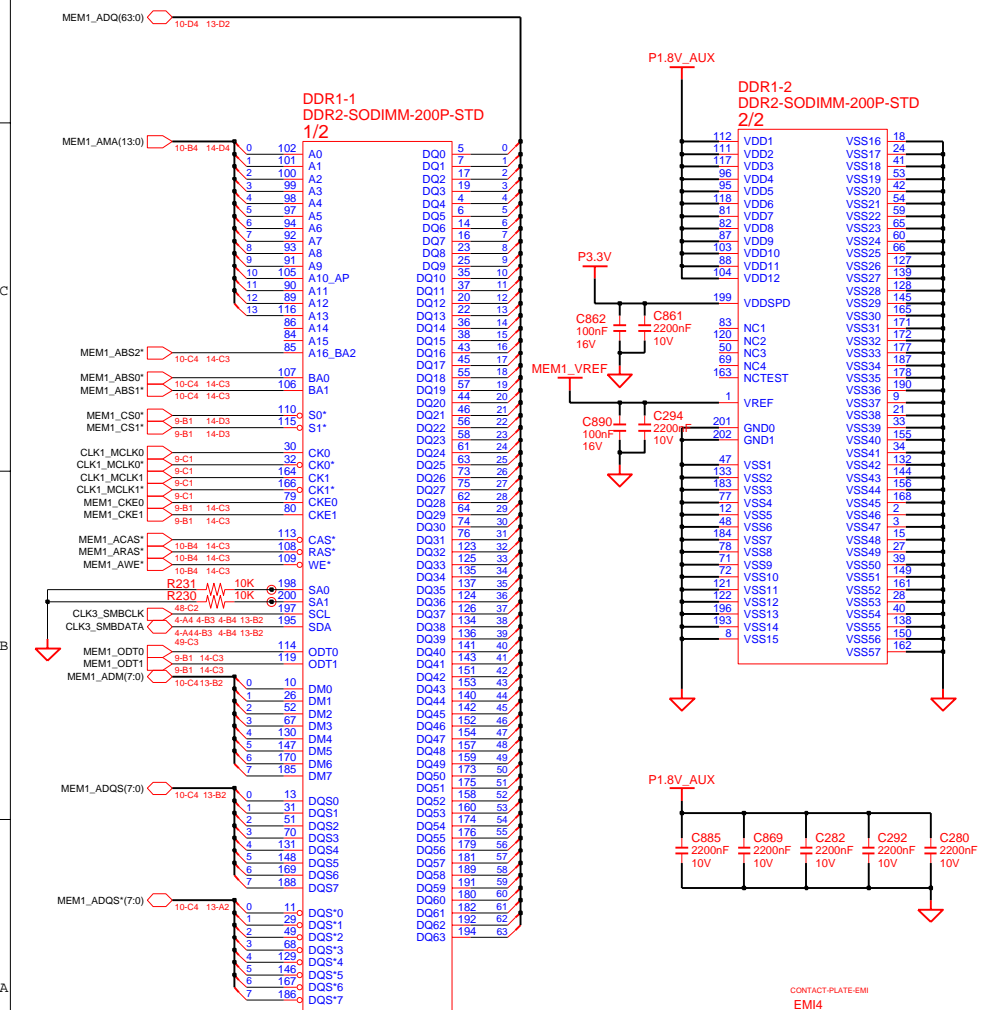
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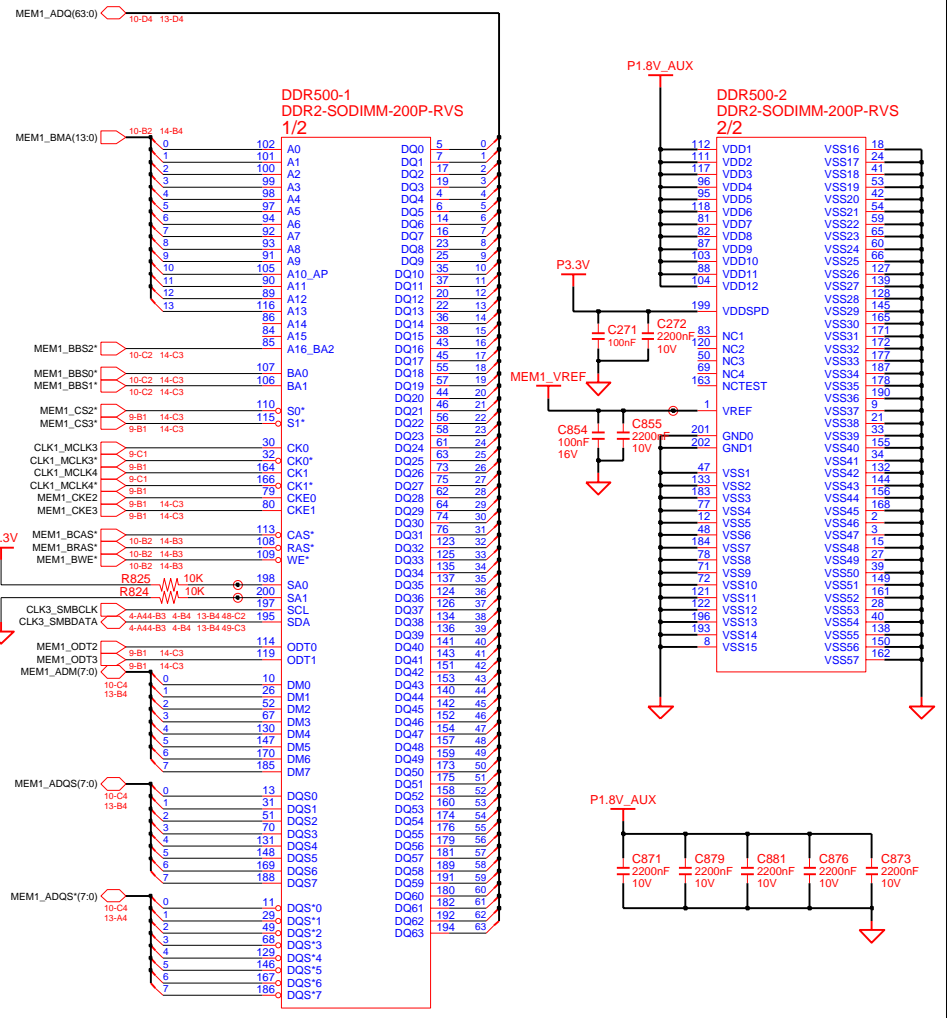
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### DDR2 SO-DIMM #0 Bottom

### DDR2 SO-DIMM #1 Top



SMBUS ADDR " A0h "



SMBUS ADDR " A2h "

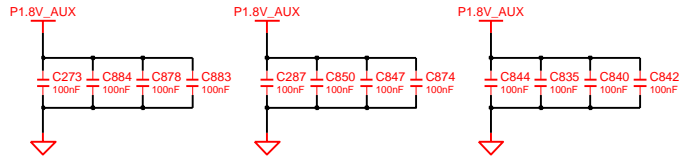
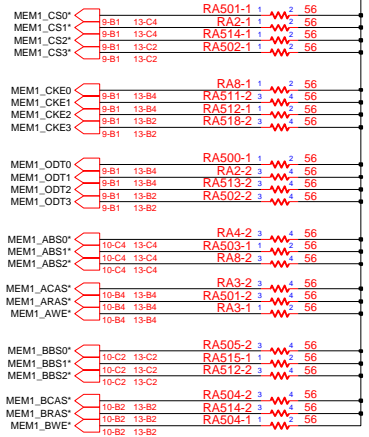
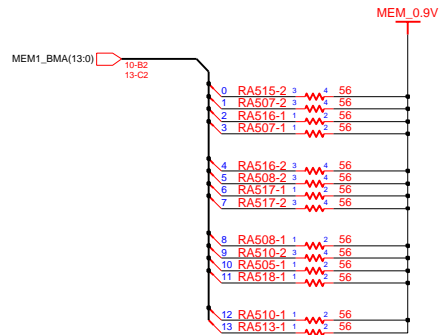
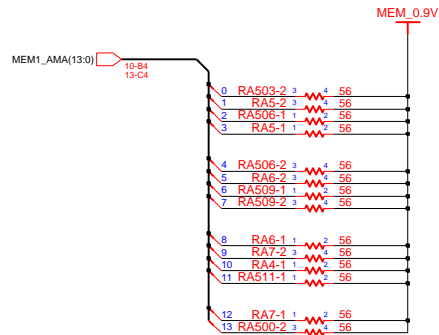
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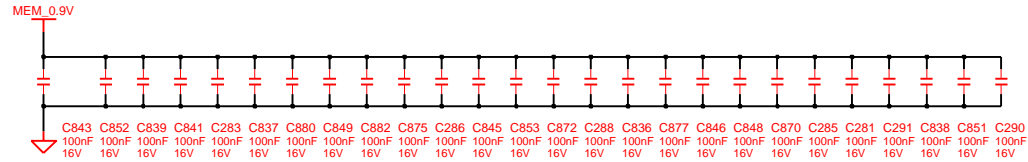
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Array resistors & Single resistors used to improve layout & routing.

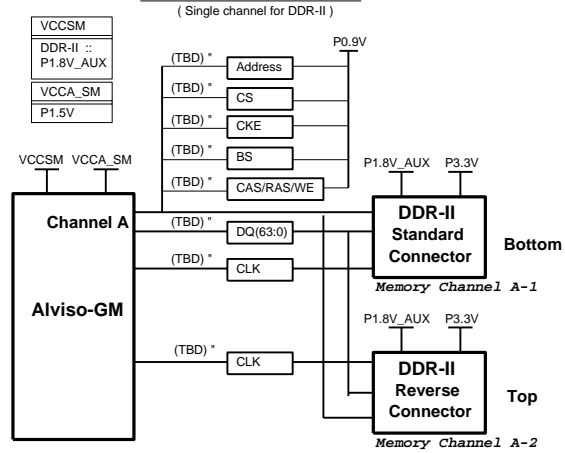


Place near GMCH      Place near SO-DIMM0      Place near SO-DIMM1



Place one cap close to every 2 pull-up resistors terminated to P0.9V

### Memory Topology

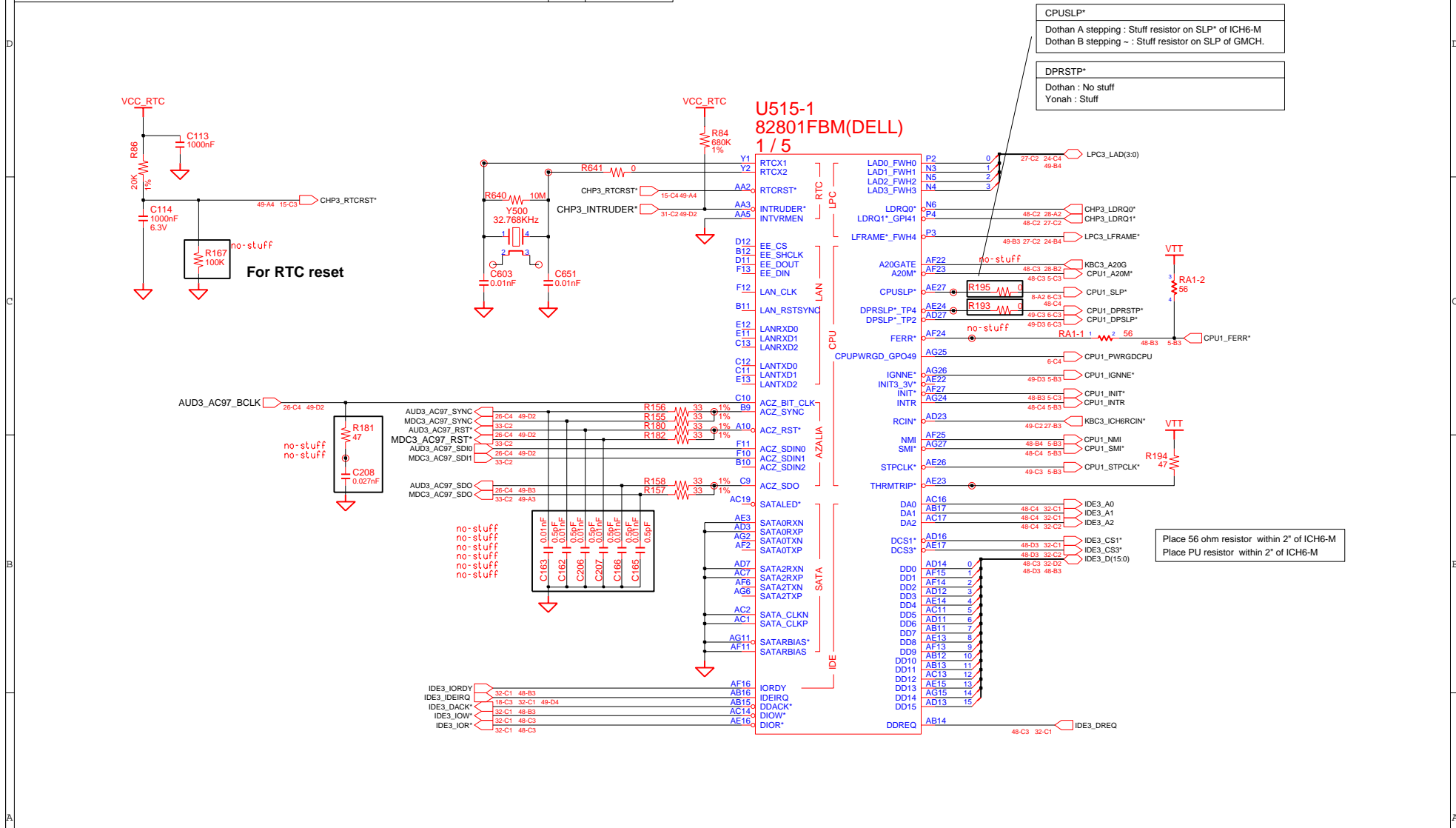


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CPUSLP\*  
Dothan A stepping : Stuff resistor on SLP\* of ICH6-M  
Dothan B stepping - : Stuff resistor on SLP of GMCH.

DPRSTP\*  
Dothan : No stuff  
Yonah : Stuff

Place 56 ohm resistor within 2" of ICH6-M  
Place PU resistor within 2" of ICH6-M

DRAW	LEE, SE	DATE	12/10/2004	TITLE	VENICE MAIN ICH6-M (1/4)	<b>SAMSUNG</b> <b>DELL</b> PART NO. BA41-00454A
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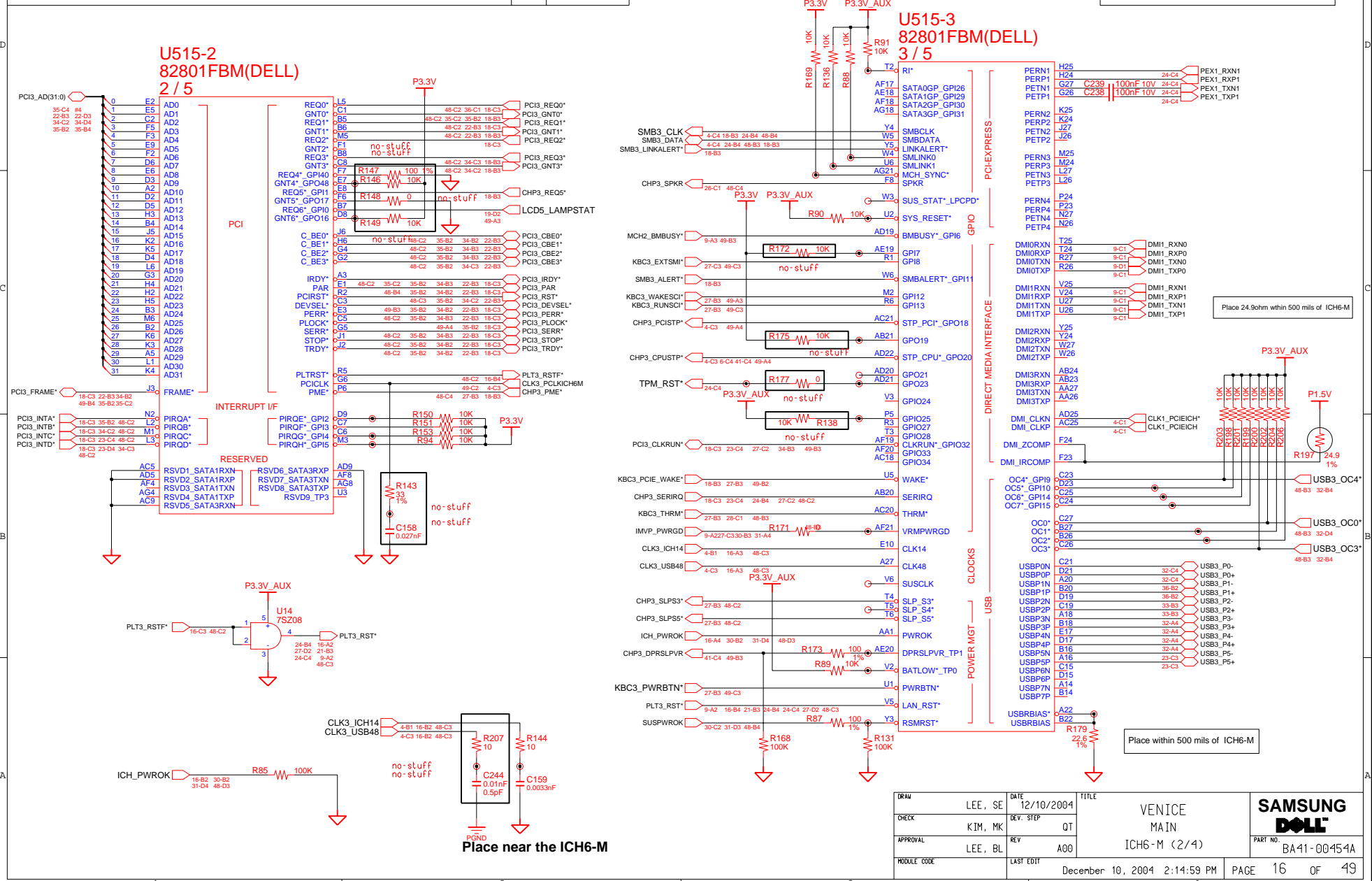


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AC caps : PCIe need to be within 250mils of the driver  
Resistor for Test : Place Stuffing Option to minimize stubs



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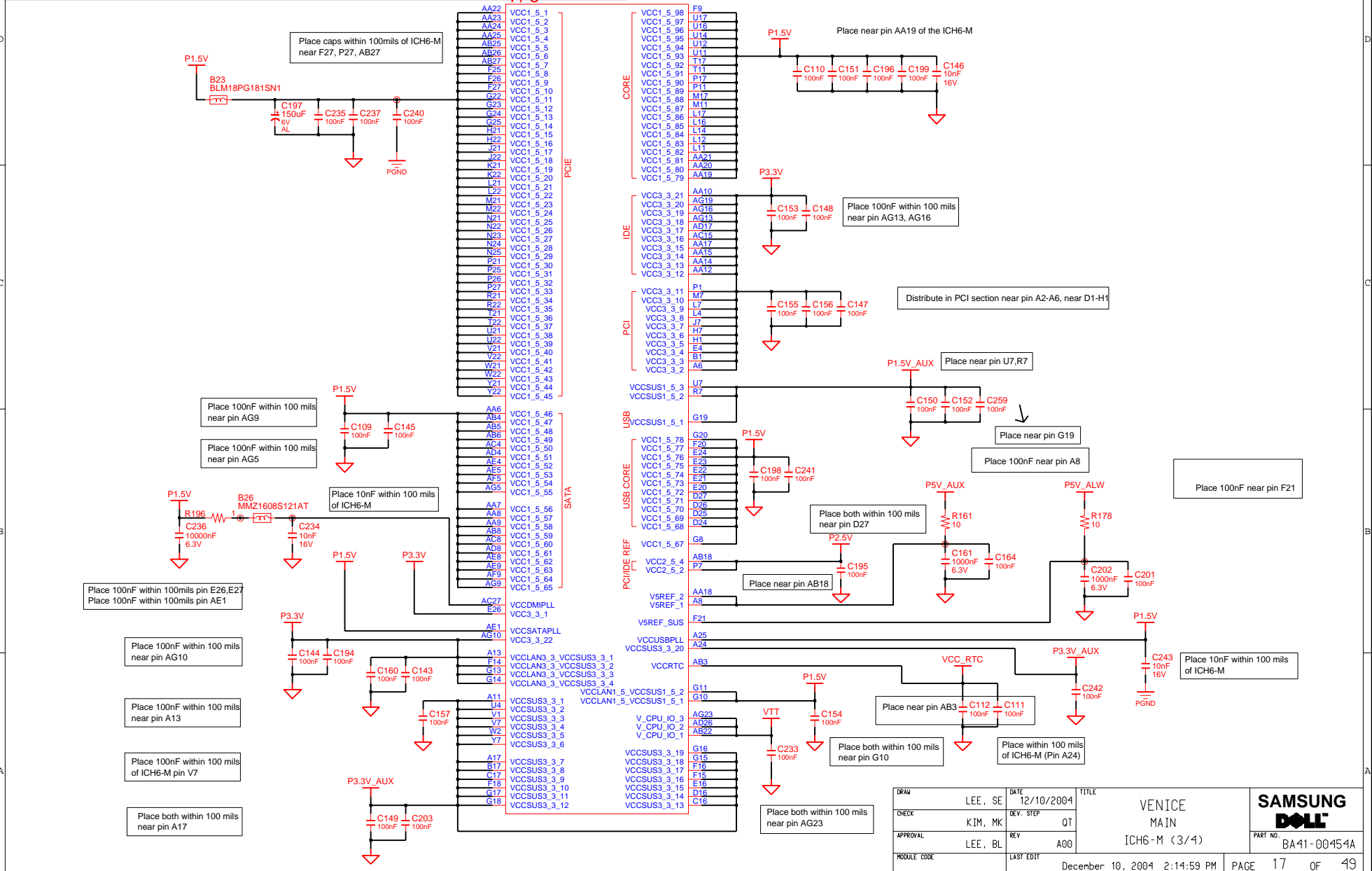


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U515-4  
82801FBM(DELL)



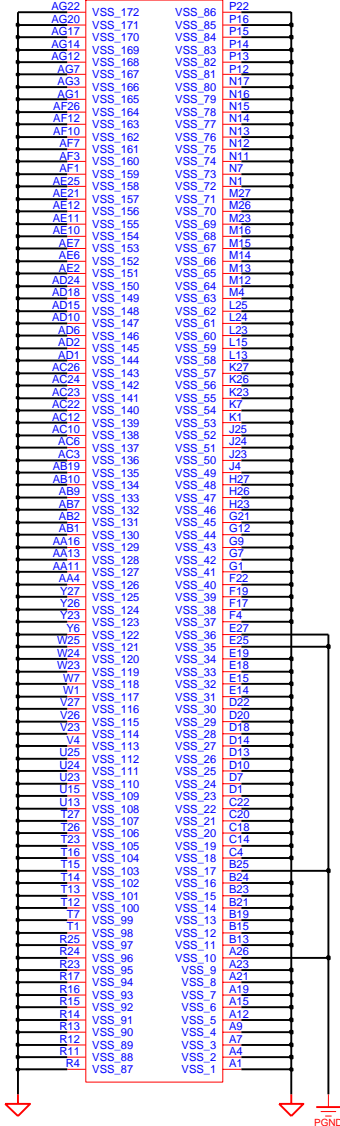
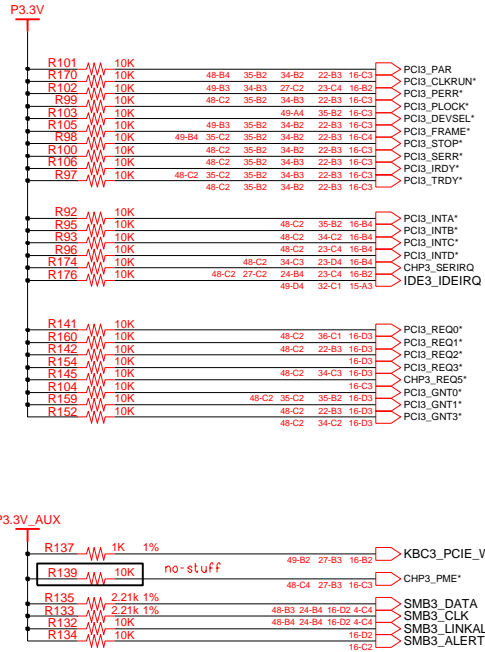
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CHECK	KIM, MK	DEV. STEP	QT			
APPROVAL	LEE, BL	REV	A00			
MODULE CODE		LAST EDIT				
			December 10, 2004 2:14:59 PM	PAGE	17 OF 49	

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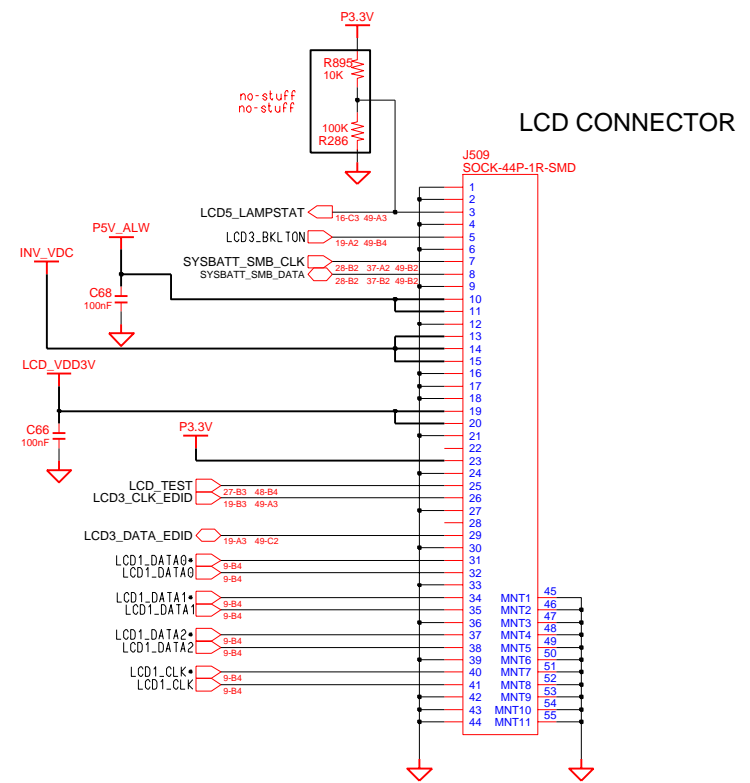
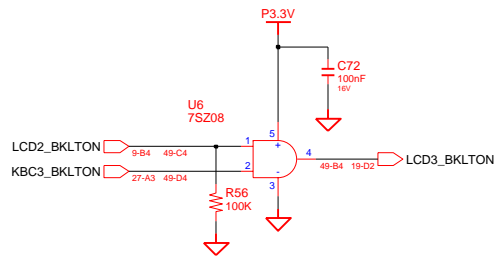
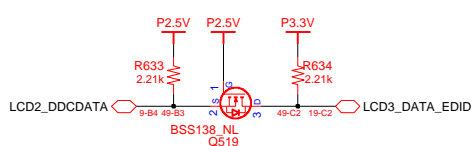
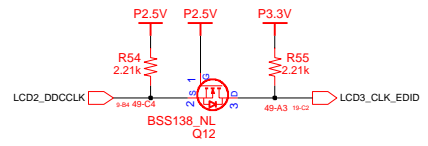
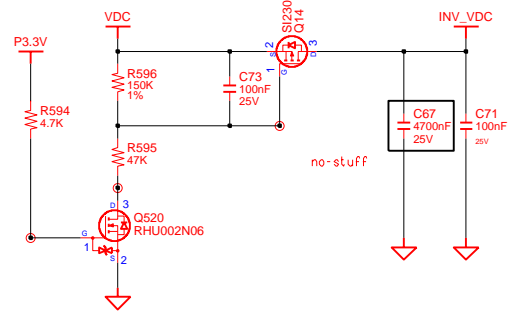
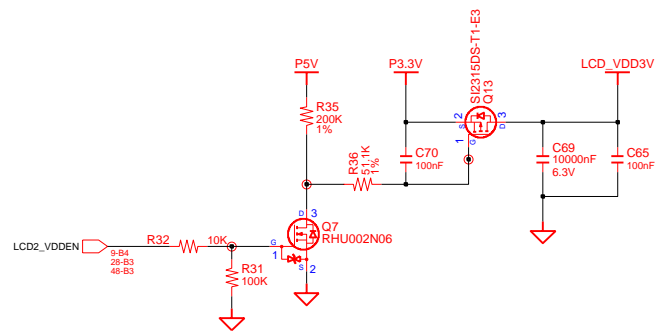


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APPROVAL	LEE, BL	REV	A00	December 10, 2004 2:14:59 PM		PART NO. BA41-00454A
MODULE CODE		LAST EDIT		PAGE	18	OF 49

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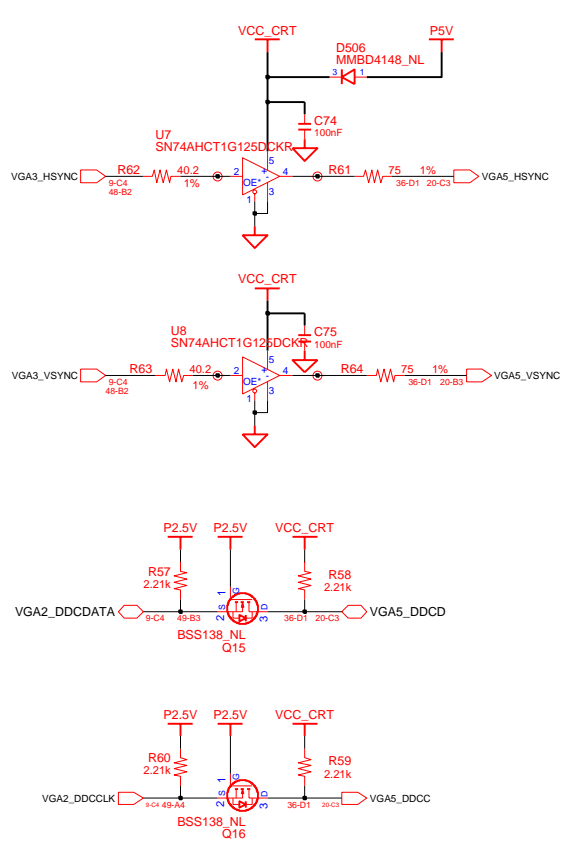


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APPROVAL	LEE, BL	REV	A00			
MODULE CODE		LAST EDIT	December 10, 2004 2:14:59 PM	PAGE	19 OF 49	

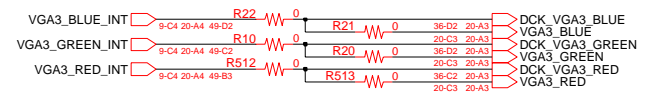
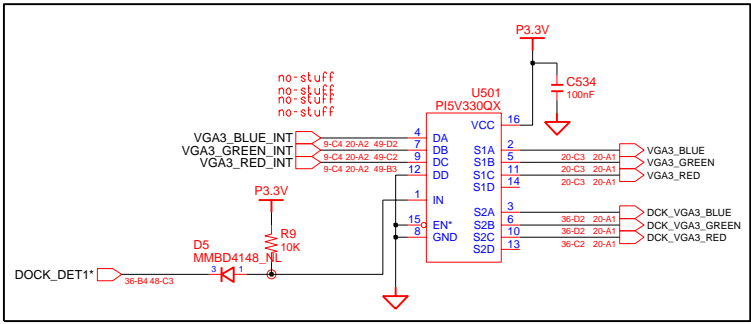
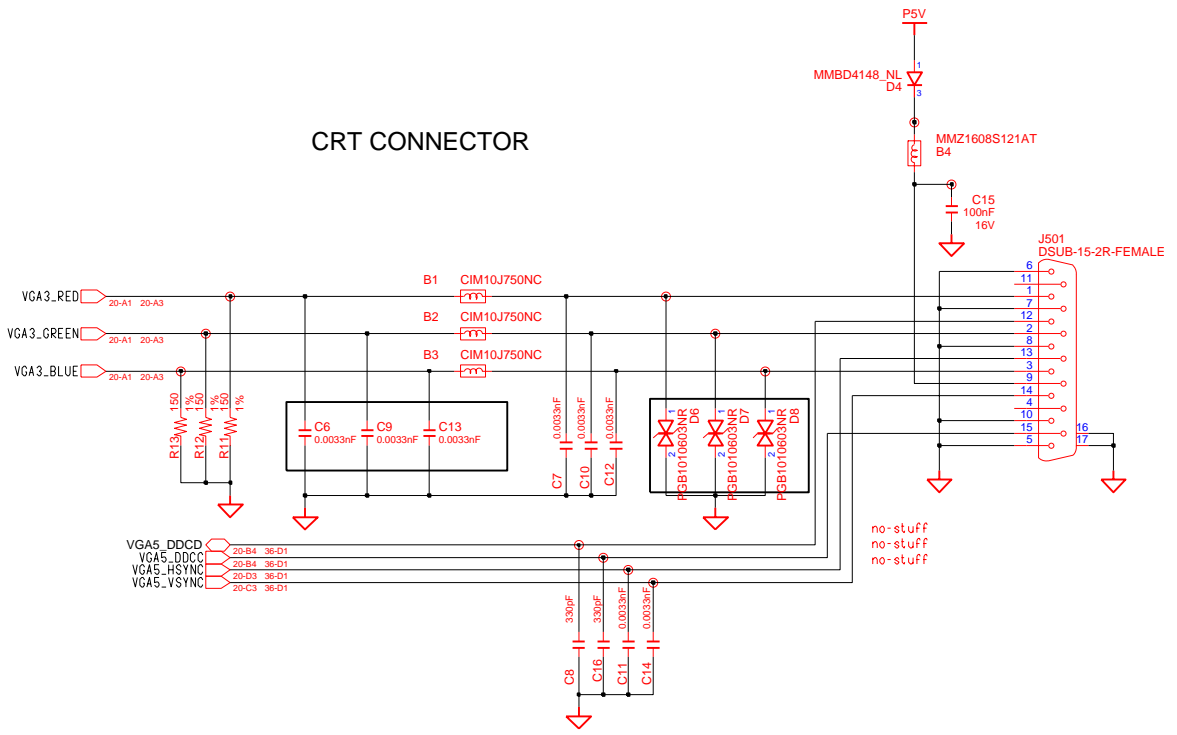
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CRT CONNECTOR

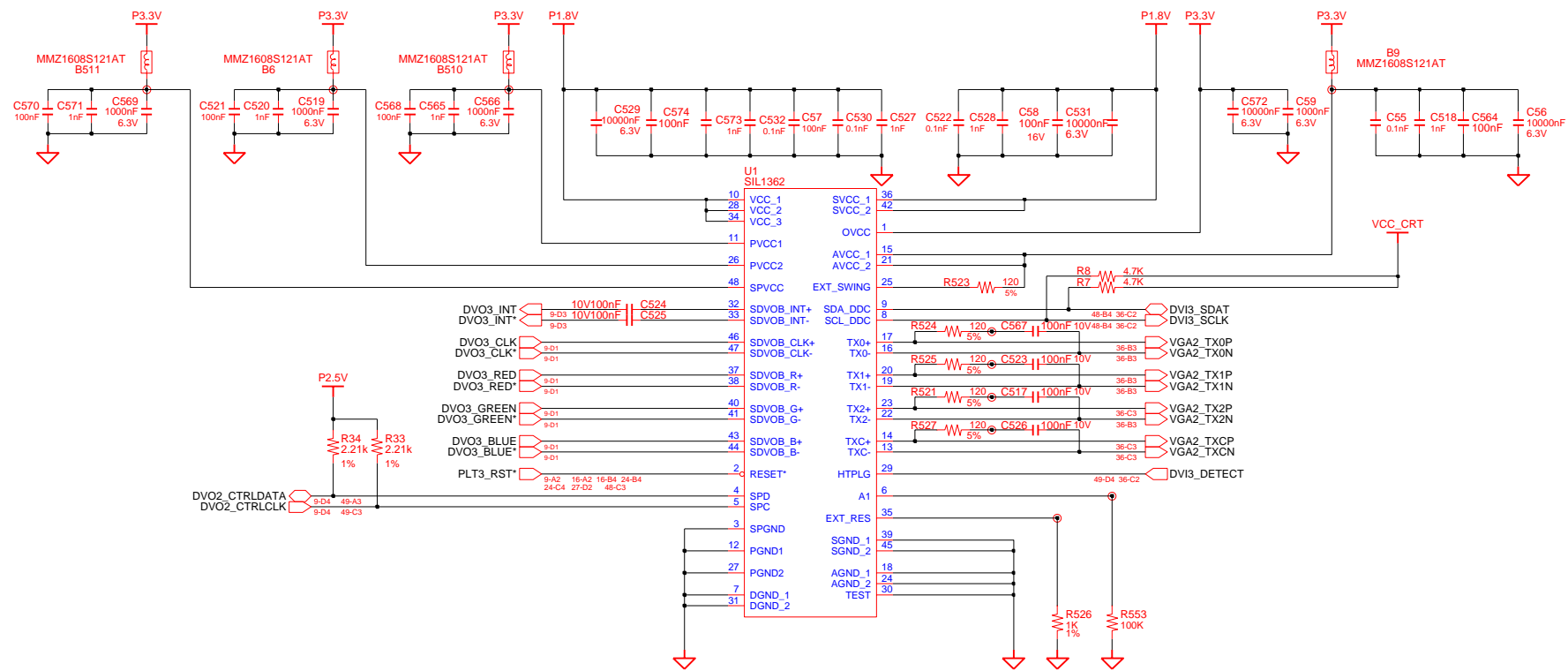


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CHECK	KIM, MK	DEV. STEP	QT	REV	A00	
APPROVAL	LEE, BL	REV	A00	LAST EDIT	December 10, 2004 2:14:59 PM	PAGE 20 OF 49

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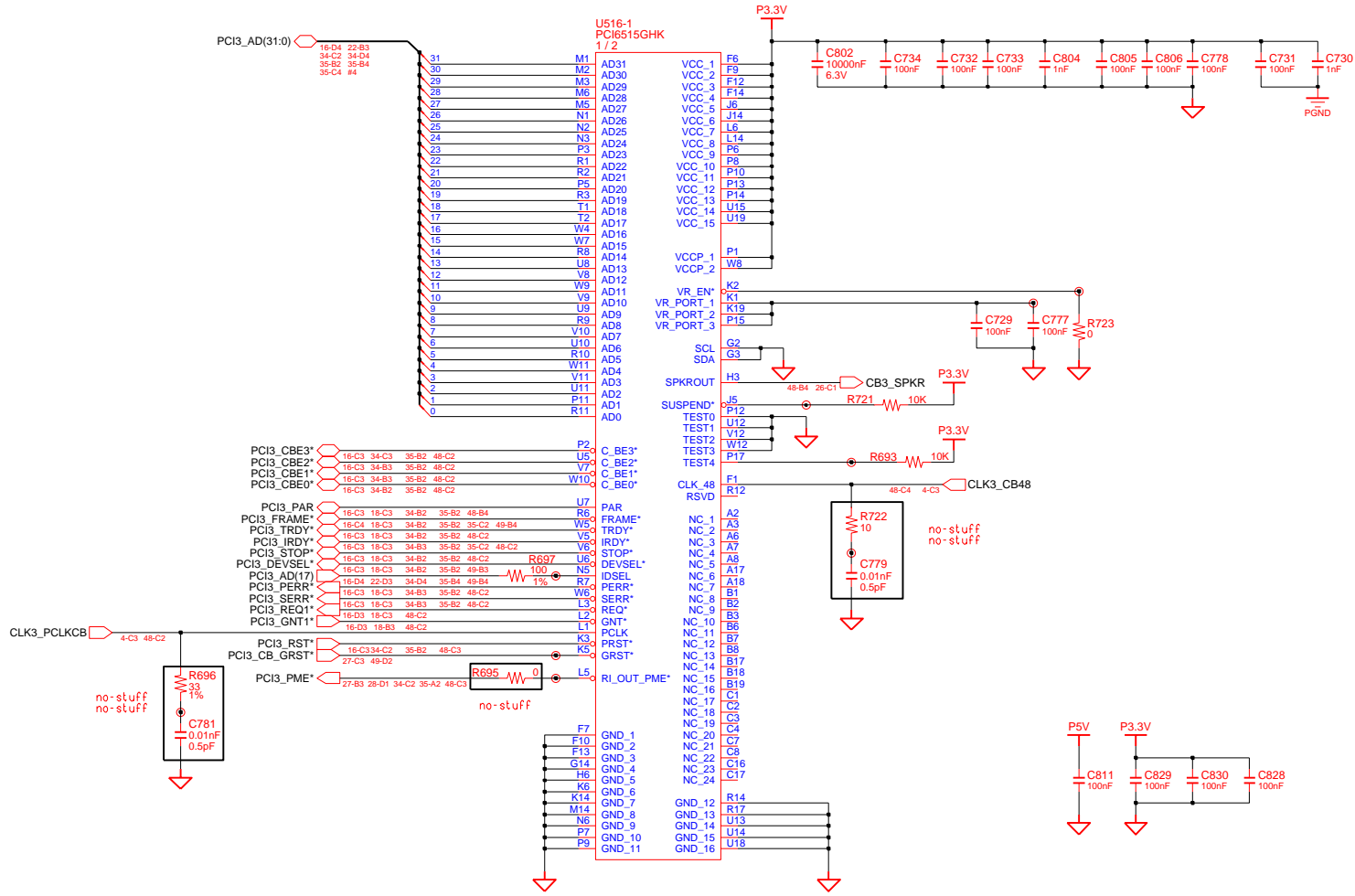


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CHECK	KIM, MK	DEV. STEP	QT			
APPROVAL	LEE, BL	REV	A00			
MODULE CODE		LAST EDIT	December 10, 2004 2:14:59 PM	PAGE	21 OF 49	

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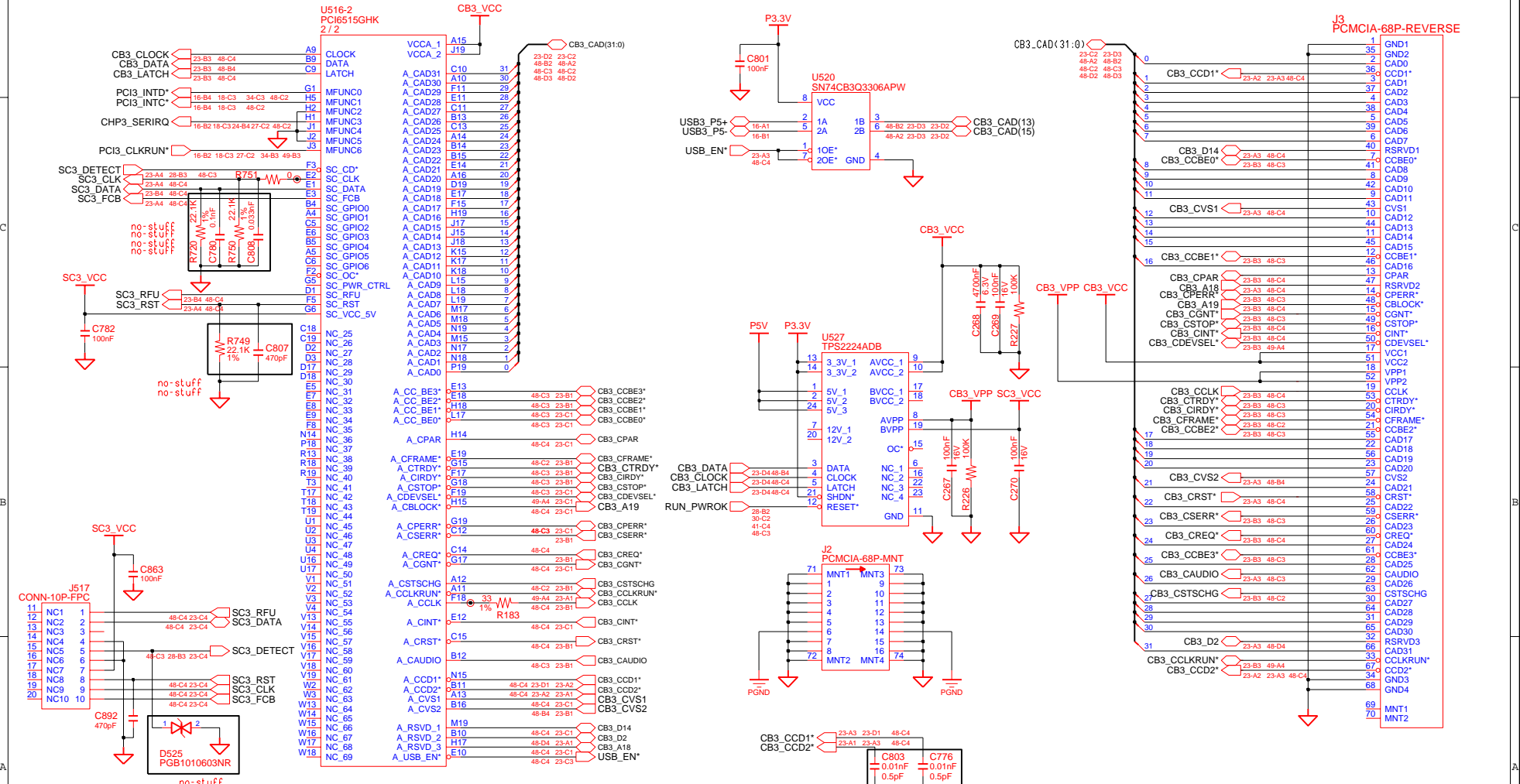
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CHECK	KIM, MK	DEV. STEP	QT			
APPROVAL	LEE, BL	REV	A00			
MODULE CODE		LAST EDIT	December 10, 2004 2:14:59 PM	PAGE	22	OF 49

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Place this near PCI6515 J18,J17  
in order to minimize the stub.  
These signals impedance should be differential 110ohm,  
and are treated like USB2.0 signal.

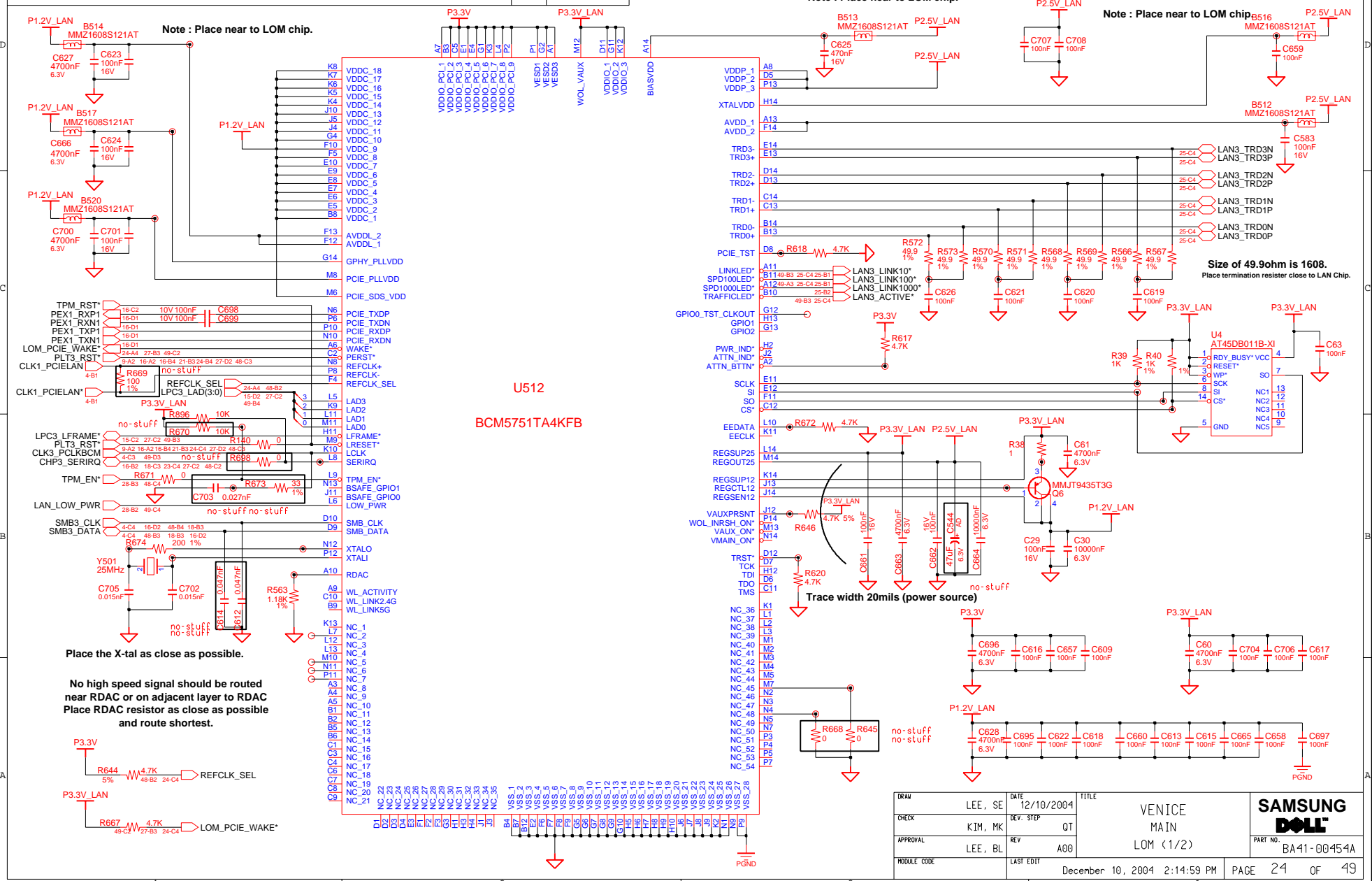


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CHECK	KIM, MK	DEV. STEP	QT	CARDBUS (2/2)	PART NO.	
APPROVAL	LEE, BL	REV	A00	December 10, 2004 2:14:59 PM	PAGE	23 OF 49
MODULE CODE		LAST EDIT				

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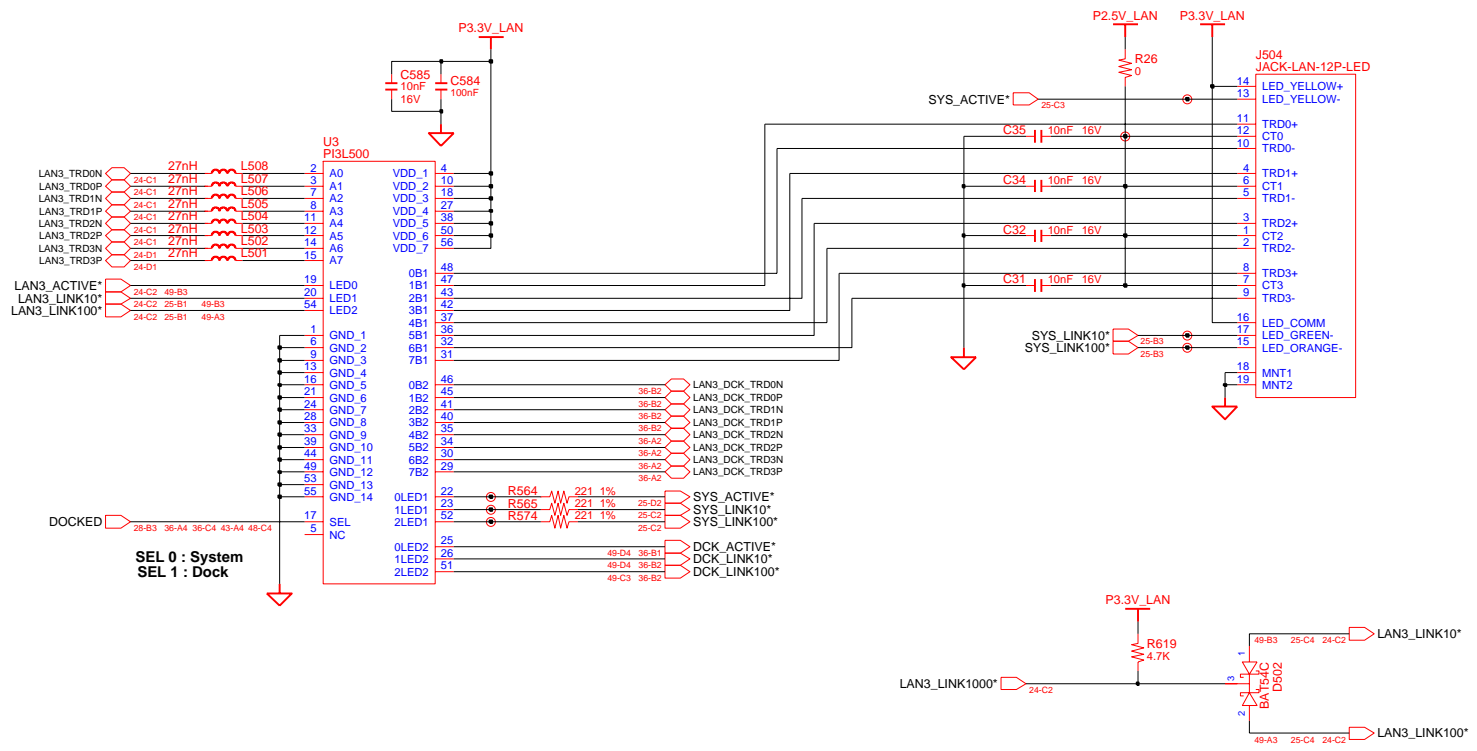
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CHECK	KIM, MK	DEV. STEP	QT			
APPROVAL	LEE, BL	REV	A00			
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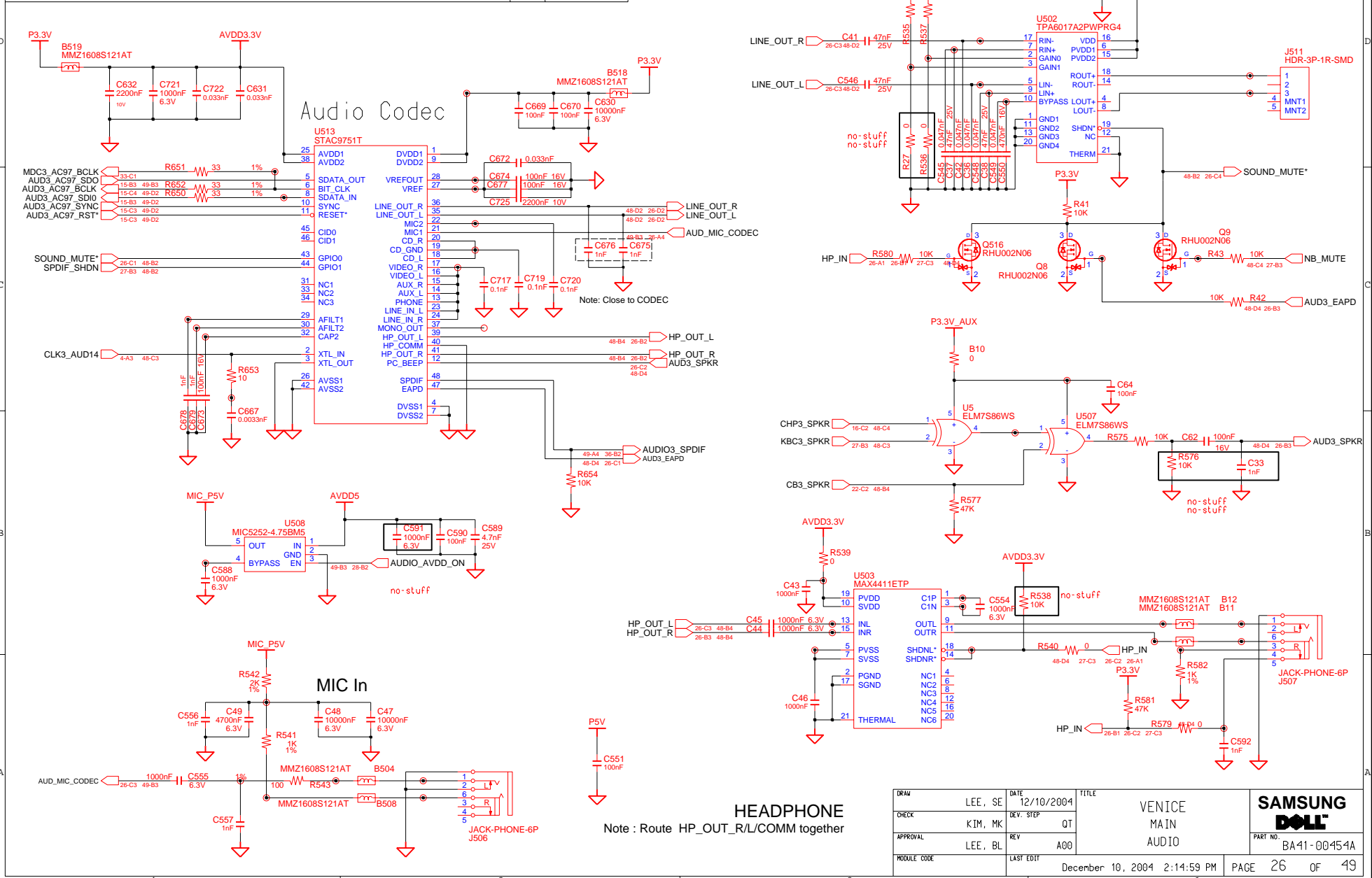


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CHECK	KIM, MK	DEV. STEP	QT			
APPROVAL	LEE, BL	REV	A00			
MODULE CODE		LAST EDIT	December 10, 2004 2:14:59 PM	PAGE	25	OF 49

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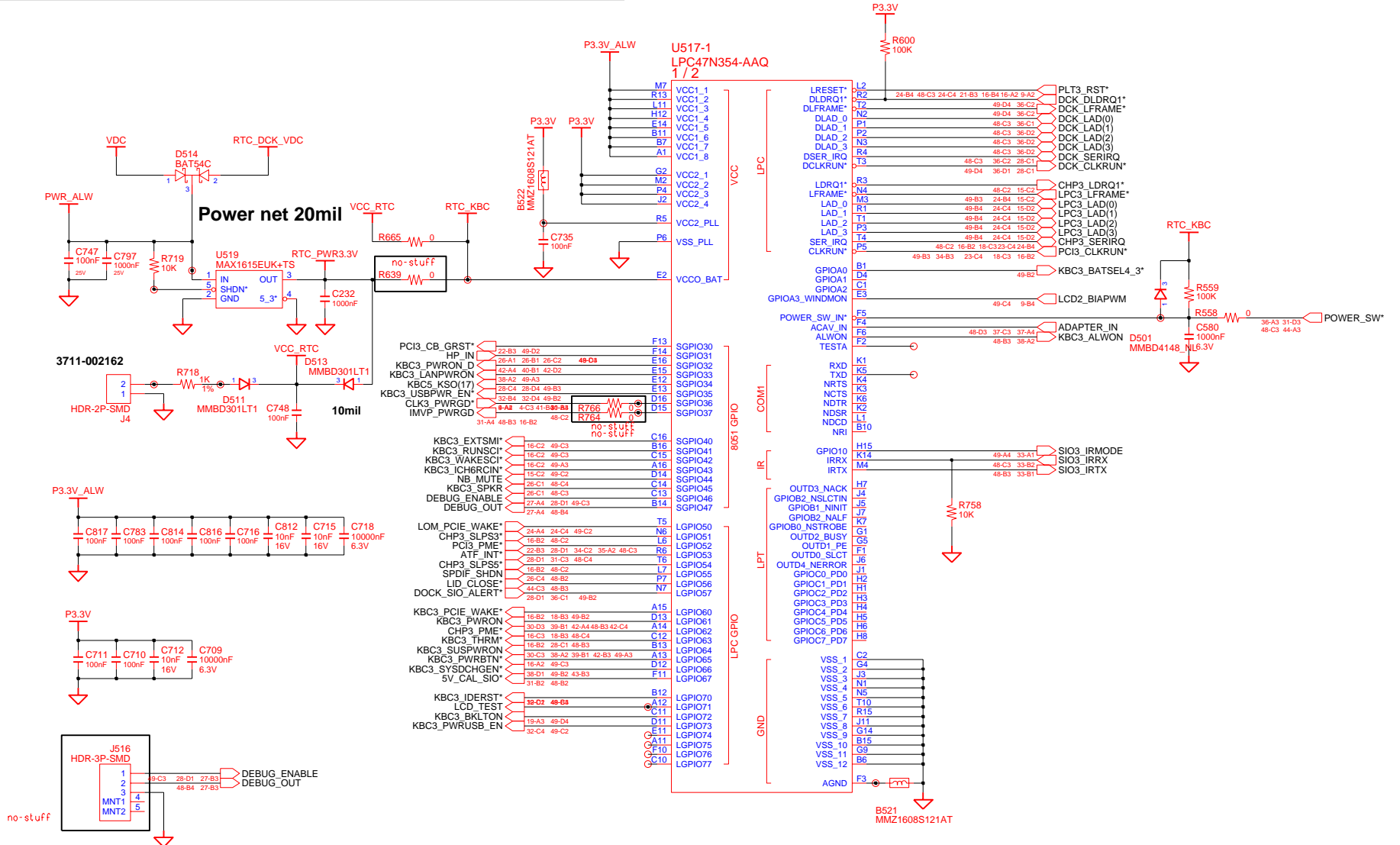


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APPROVAL	LEE, BL	REV	A00			PART NO. BA41-00454A
MODULE CODE		LAST EDIT	December 10, 2004 2:14:59 PM	PAGE	26	OF 49

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PCI3_CB_GRST*	22-B3 49-D2	F13	SGPIO30
KBC3_PWRON_D	28-A1 28-B1 28-C2	F14	SGPIO32
KBC3_LANPWRON	32-A4 40-B1 42-D2	E16	SGPIO33
KBC3_KSO(17)	36-A2 48-A3	E12	SGPIO34
KBC3_USBPWR_EN*	28-C4 28-D4 49-B3	E13	SGPIO35
CLK3_PWRGD*	32-B4 32-D4 49-B2	D16	SGPIO36
IMVP_PWRGD*	3-A4 4-C3 41-B2 43-B3	D15	SGPIO37
KBC3_EXTSMI*	16-C2 49-C3	C16	SGPIO40
KBC3_RUNSCI*	15-C2 49-C3	B16	SGPIO41
KBC3_WAKESCI*	16-C2 49-A3	C15	SGPIO42
KBC3_IH6RCIN*	15-C2 49-C2	D14	SGPIO43
NB_MUTE	26-C1 48-C4	C14	SGPIO44
KBC3_SPKR	26-C1 48-C4	C13	SGPIO45
DEBUG_ENABLE	27-A4 28-D1 49-C3	C13	SGPIO46
DEBUG_OUT	27-A4 48-B4	B14	SGPIO47
LOM_PCIE_WAKE*	24-A4 24-C4 49-C2	T5	LGPIO50
CHP3_SLPS3*	16-B2 49-C2	L6	LGPIO51
PCI3_PME*	22-B3 28-D1 34-C2 35-A2 48-C3	R6	LGPIO52
ATF_INT*	28-D1 31-C3 48-C4	T6	LGPIO53
CHP3_SLPS5*	16-B2 48-C2	L7	LGPIO54
SPDIF_SHDN*	26-C4 48-B2	P7	LGPIO55
LID_CLOSE*	44-C3 48-B3	N7	LGPIO56
DOCK_SIO_ALERT*	28-D1 36-C1 49-B2	N7	LGPIO57
KBC3_PCIE_WAKE*	16-B2 18-B3 49-B2	A15	LGPIO60
KBC3_PWRON	30-C3 39-B1 42-A4 48-B3 42-C4	D13	LGPIO61
CHP3_PME*	16-C3 18-B3 49-C4	C12	LGPIO62
KBC3_THRM*	16-B2 28-C1 48-B3	B13	LGPIO63
KBC3_SUSPWRON	30-C3 38-A2 39-B1 42-B3 49-A3	A13	LGPIO65
KBC3_PWRBTN*	16-A2 49-C3	D12	LGPIO66
KBC3_SYSDCHGEN*	38-D1 49-B2 43-B3	F11	LGPIO67
5V_CAL_SIO*	31-B2 48-B2	F11	LGPIO67
KBC3_IDERST*	39-D2 48-B3	B12	LGPIO70
LCD_TEST		A12	LGPIO71
KBC3_BKLTON	19-A3 49-D4	D11	LGPIO72
KBC3_PWRUSB_EN	32-C4 49-C2	E11	LGPIO73
		A11	LGPIO74
		F10	LGPIO75
		C10	LGPIO76
		C10	LGPIO77

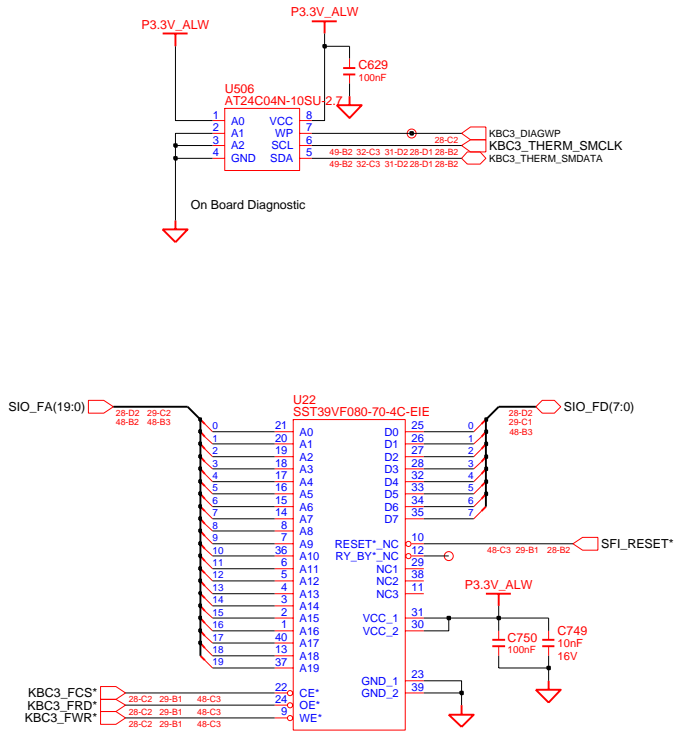
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APPROVAL	LEE, BL	REV	A00	December 10, 2004 2:14:59 PM		PART NO. BA41-00454A
MODULE CODE		LAST EDIT		PAGE 27 OF 49		



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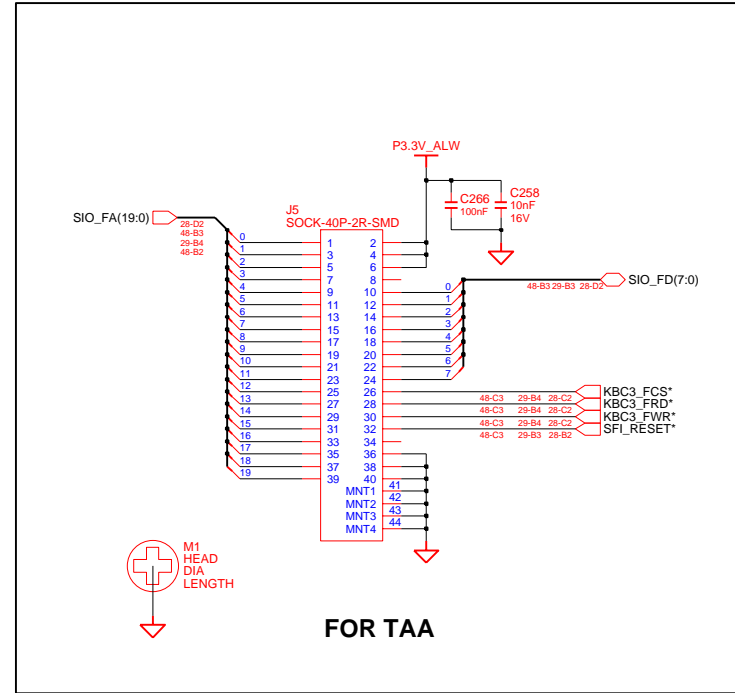
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**AMD : Pin 10 is RESET\* ; Pin12 is RY/BY\*  
SST : Pin 10, 12 are NC.**

1. AMD-29LV081B require MAX 500ms Tready for it's hardware reset. And MAX6326\_UR29 has > 100ms reset timing. So we can tie it's reset\* pin to +3VALW directly.
2. SIO has internal 20ms dela of VCC1\_p\PWROK.



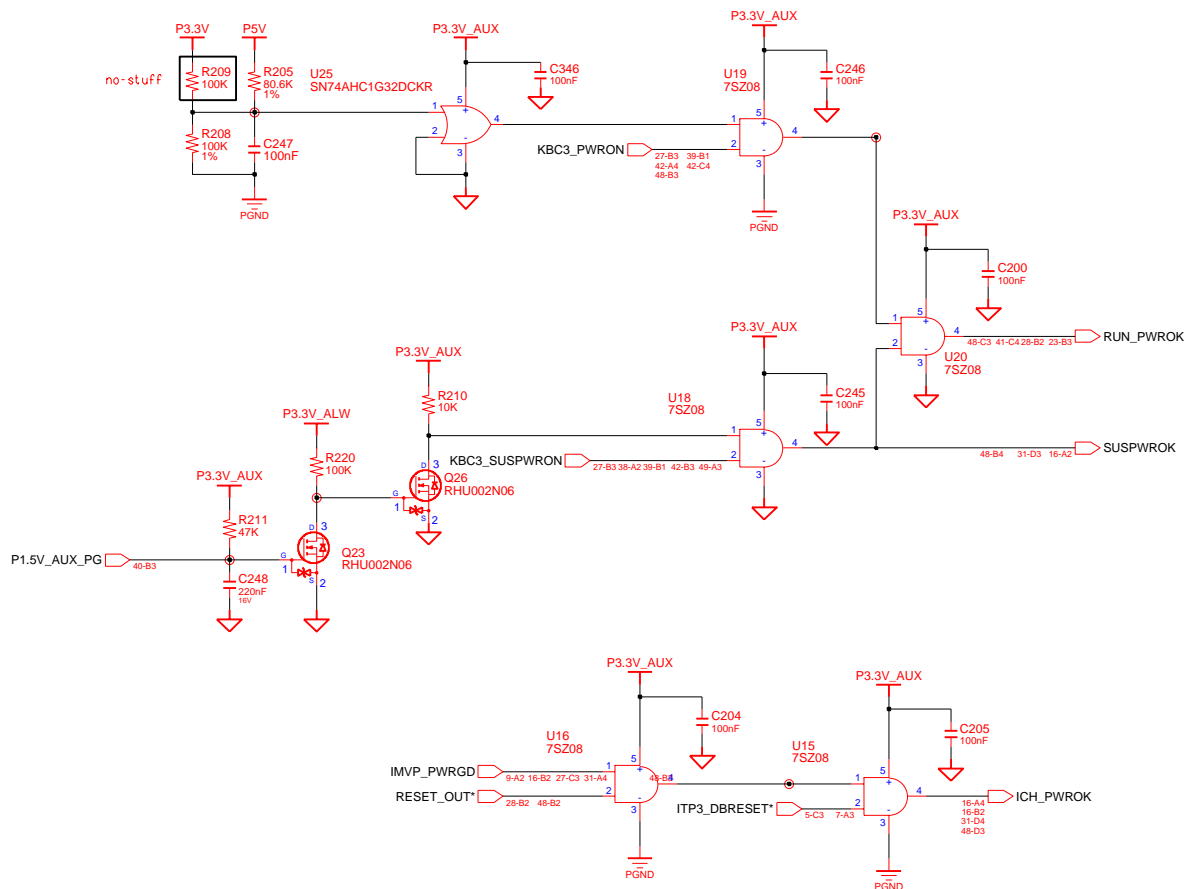
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MODULE CODE	undefined	LAST EDIT		PAGE	29	OF 49

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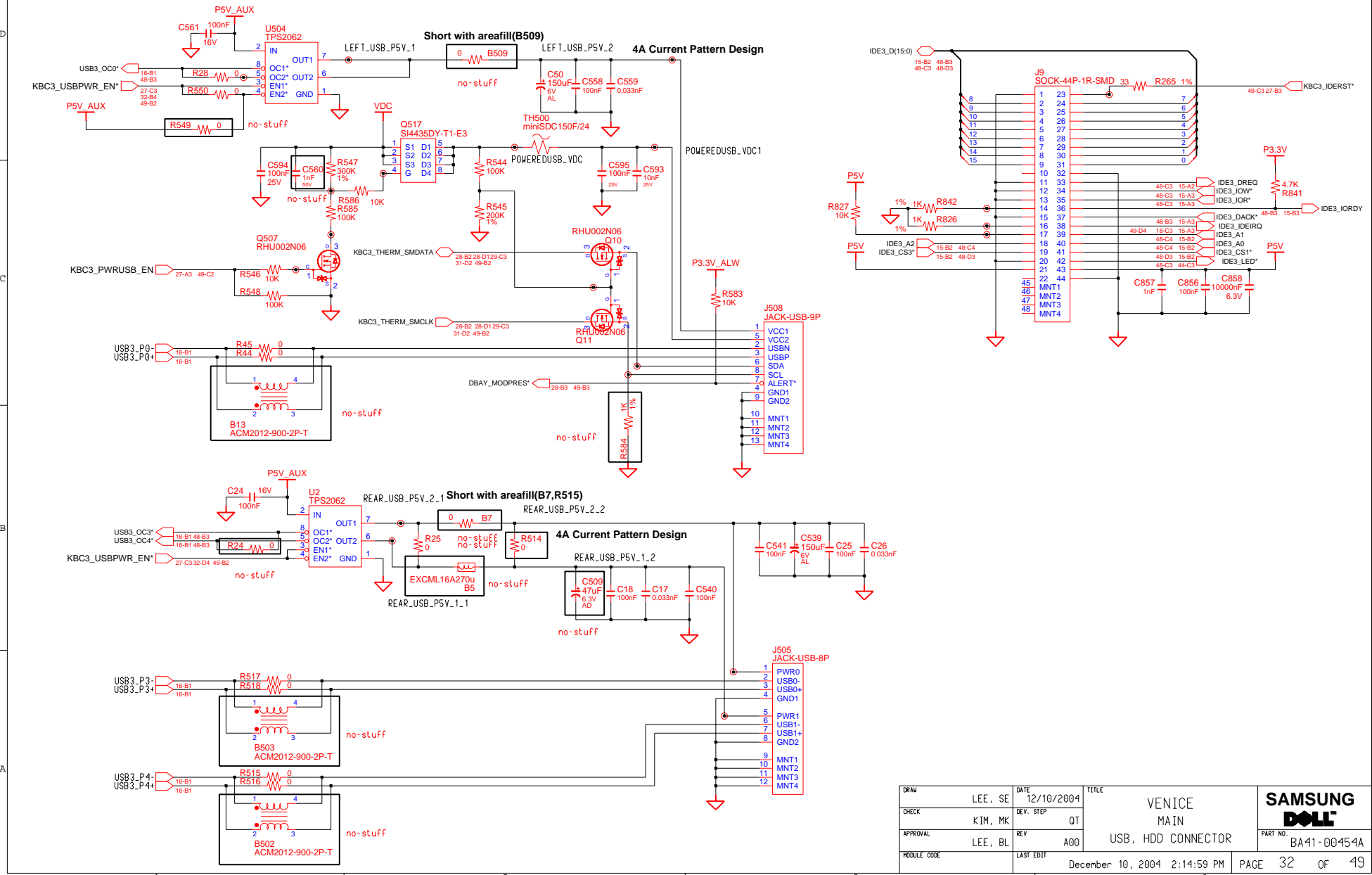
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CHECK	KIM, MK	DEV. STEP	QT	REV		
APPROVAL	LEE, BL	REV	A00	LAST EDIT	December 10, 2004 2:14:59 PM	PAGE 30 OF 49



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DRAW	LEE, SE	DATE	12/10/2004	TITLE	VENICE MAIN USB, HDD CONNECTOR	<b>SAMSUNG</b> <b>DELL</b> PART NO. BA41-00454A
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APPROVAL	LEE, BL	REV	A00			
MODULE CODE		LAST EDIT	December 10, 2004 2:14:59 PM	PAGE	32 OF 49	

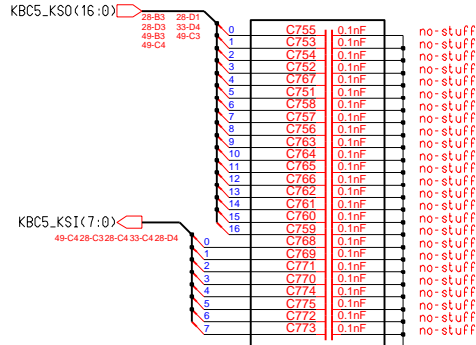
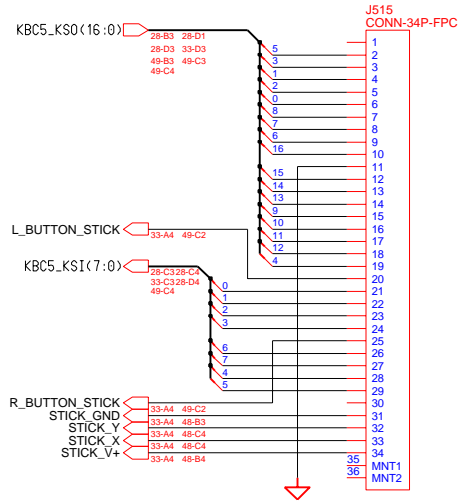


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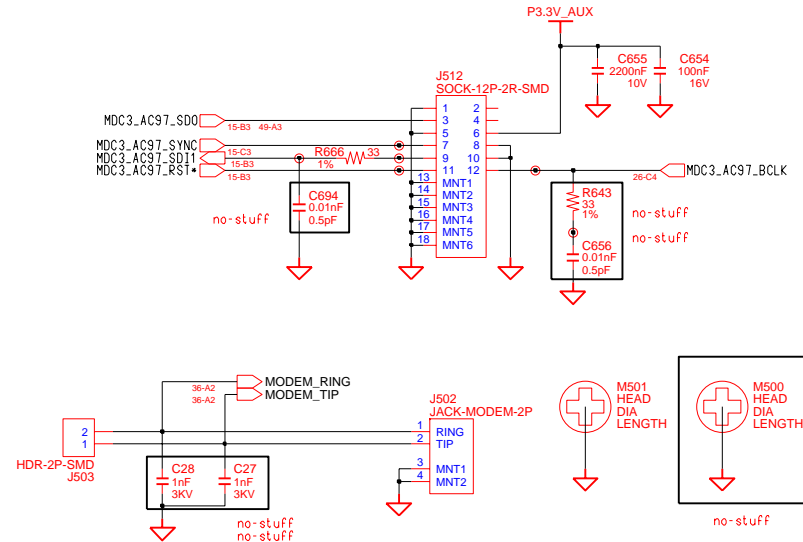
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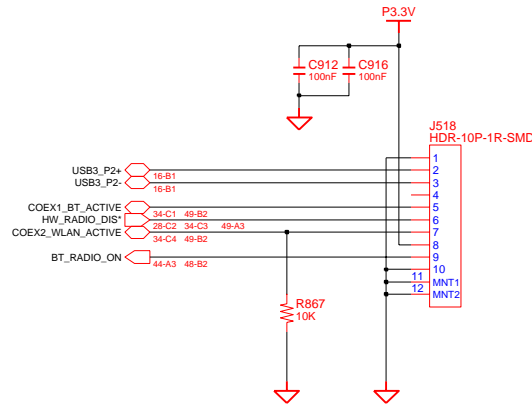
### KEYBOARD



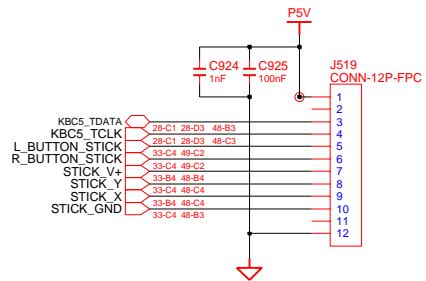
### MDC connector



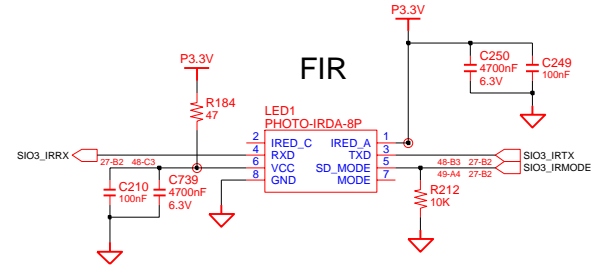
### Bluetooth (Type A Module)



### TOUCHPAD IF BD



### FIR



DRAW	LEE, SE	DATE	12/10/2004	TITLE	VENICE MAIN	SAMSUNG DELL
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APPROVAL	LEE, BL	REV	A00	PART NO. BA41-00454A		
MODULE CODE	LAST EDIT		December 10, 2004 2:14:59 PM	PAGE	33	OF 49

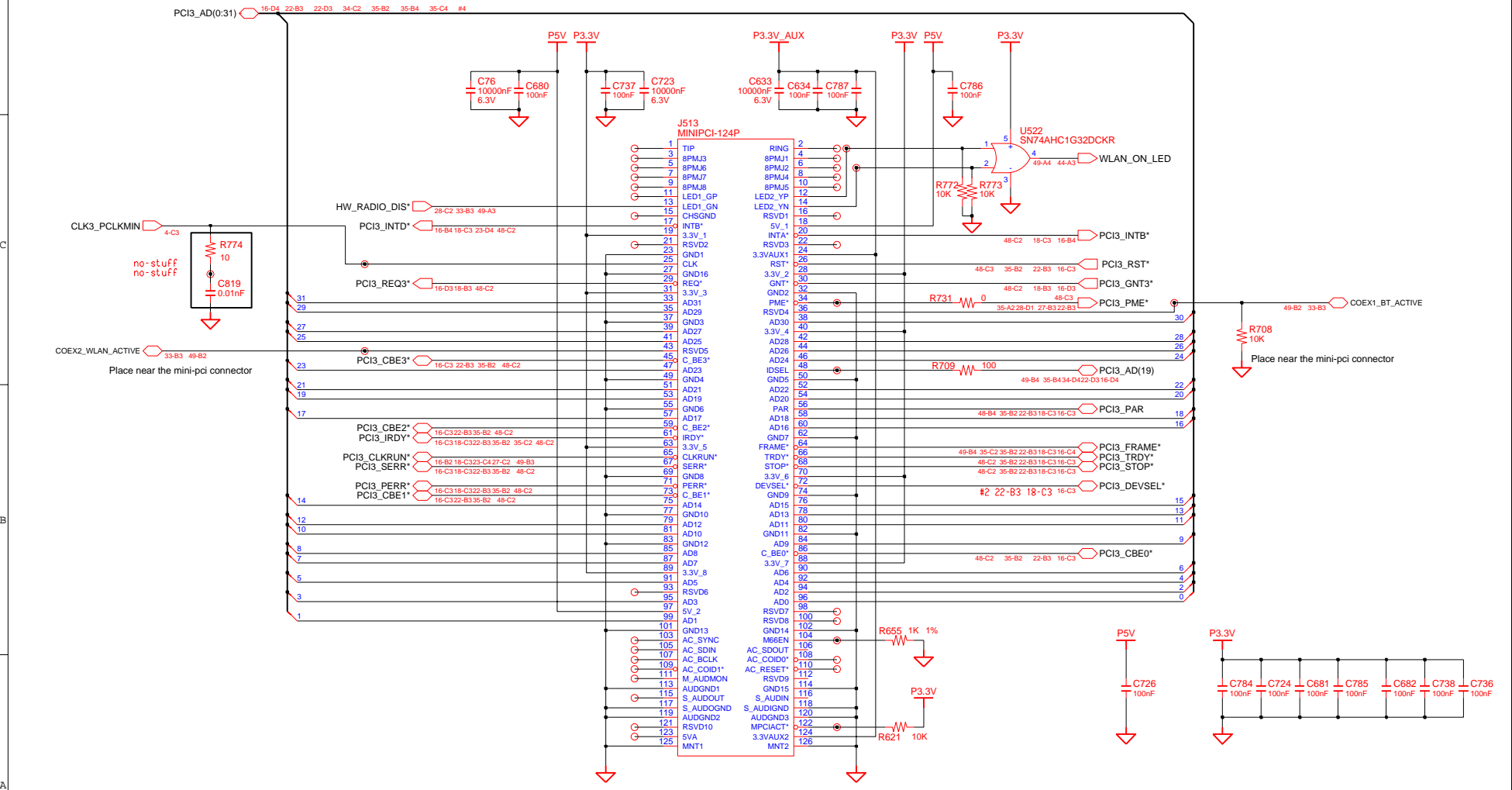
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# MINIPCI

No Wake On Wireless LAN

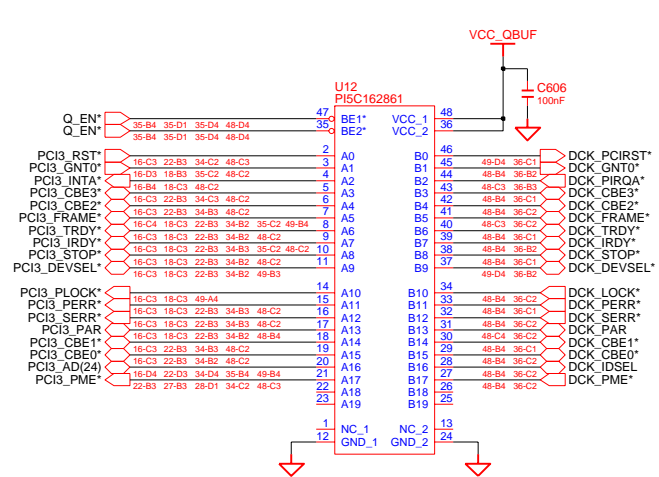
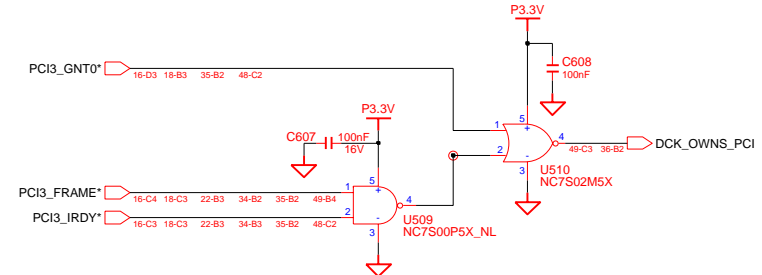
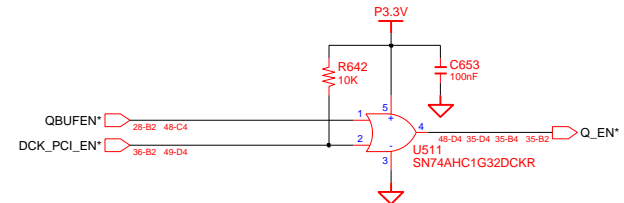
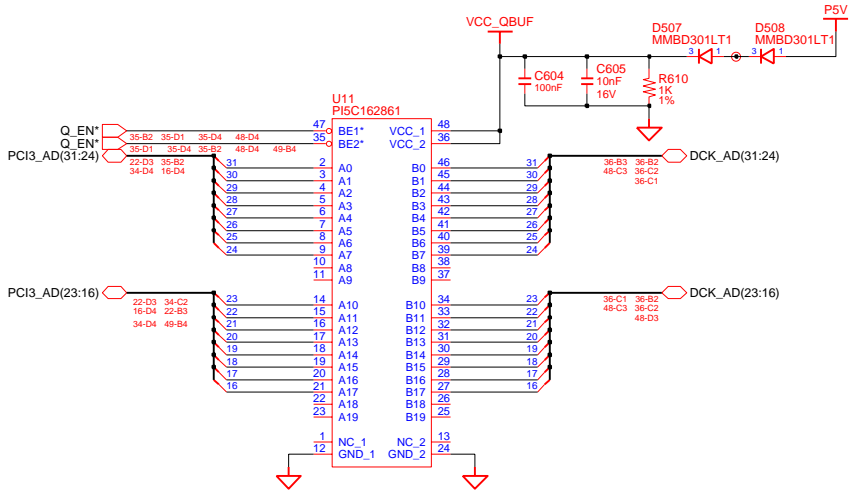
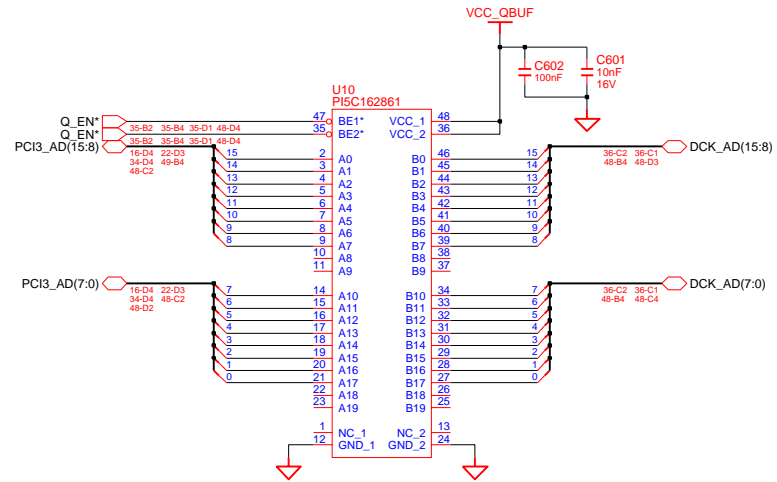


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MODULE CODE		LAST EDIT		December 10, 2004 2:14:59 PM	PAGE	34 OF 49

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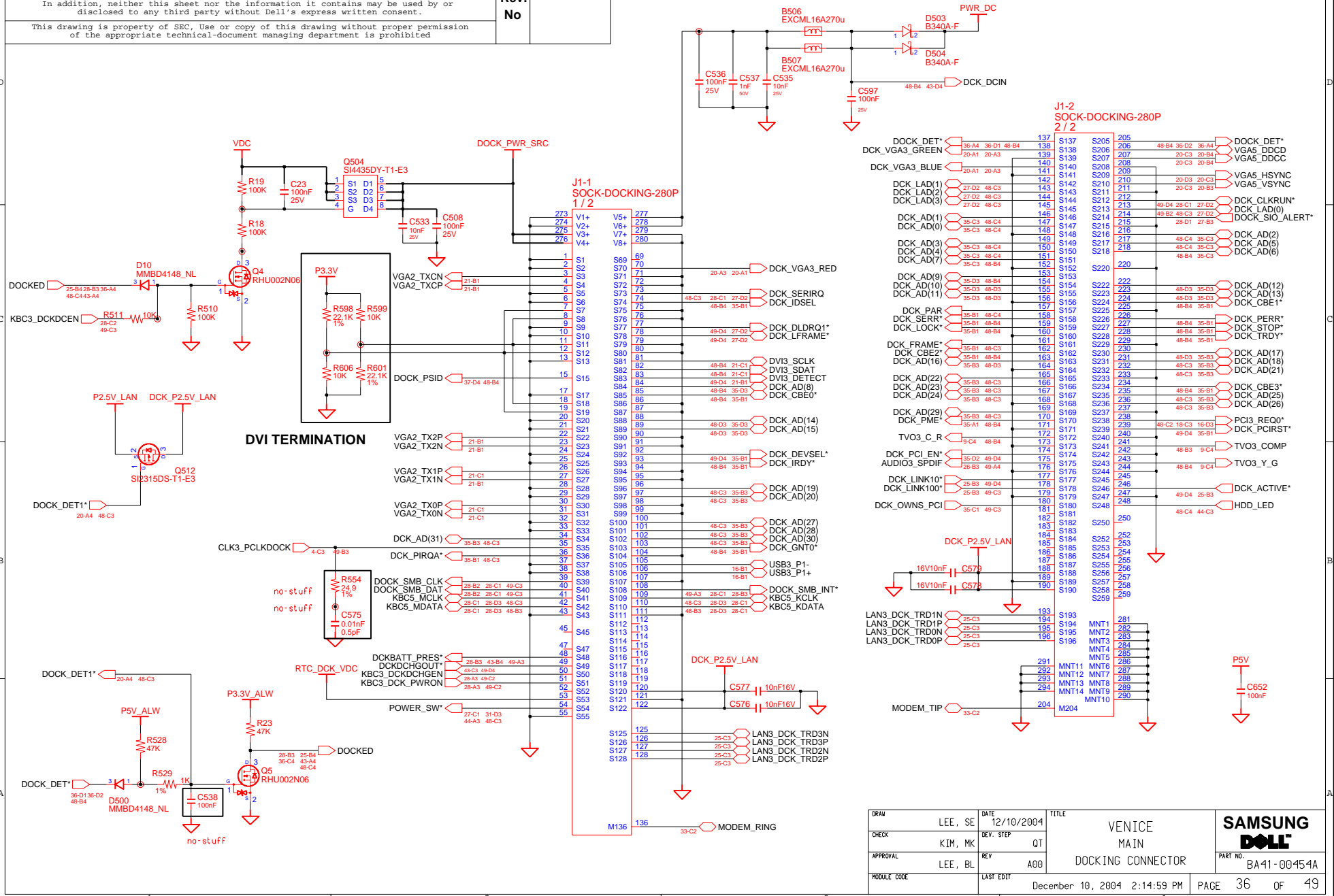


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APPROVAL	LEE, BL	REV	A00			
MODULE CODE		LAST EDIT	December 10, 2004 2:14:59 PM	PAGE	35 OF 49	

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DRAW	LEE, SE	DATE	12/10/2004	TITLE	VENICE MAIN DOCKING CONNECTOR	<b>SAMSUNG</b> <b>DELL</b> PART NO. BA41-00454A
CHECK	KIM, MK	DEV. STEP	QT			
APPROVAL	LEE, BL	REV	A00			
MODULE CODE		LAST EDIT				
			December 10, 2004 2:14:59 PM	PAGE	36 OF 49	

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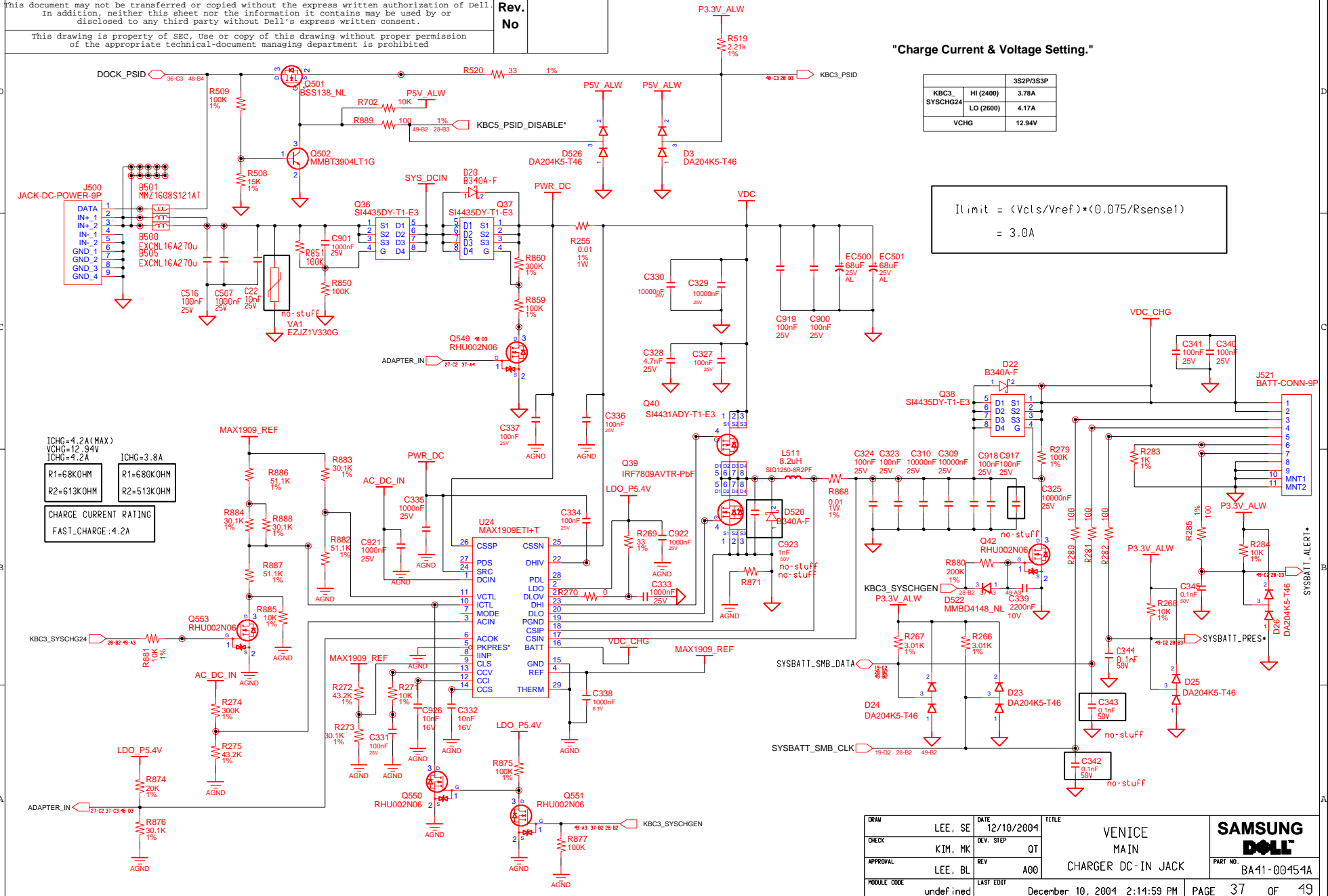
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Rev.  
No

"Charge Current & Voltage Setting."

	3S2P/3S3P
KBC3_SYSCHG24	HI (2400) 3.78A
	LO (2600) 4.17A
VCHG	12.94V

$$I_{limit} = (V_{cls}/V_{ref}) * (0.075/R_{sense1}) = 3.0A$$

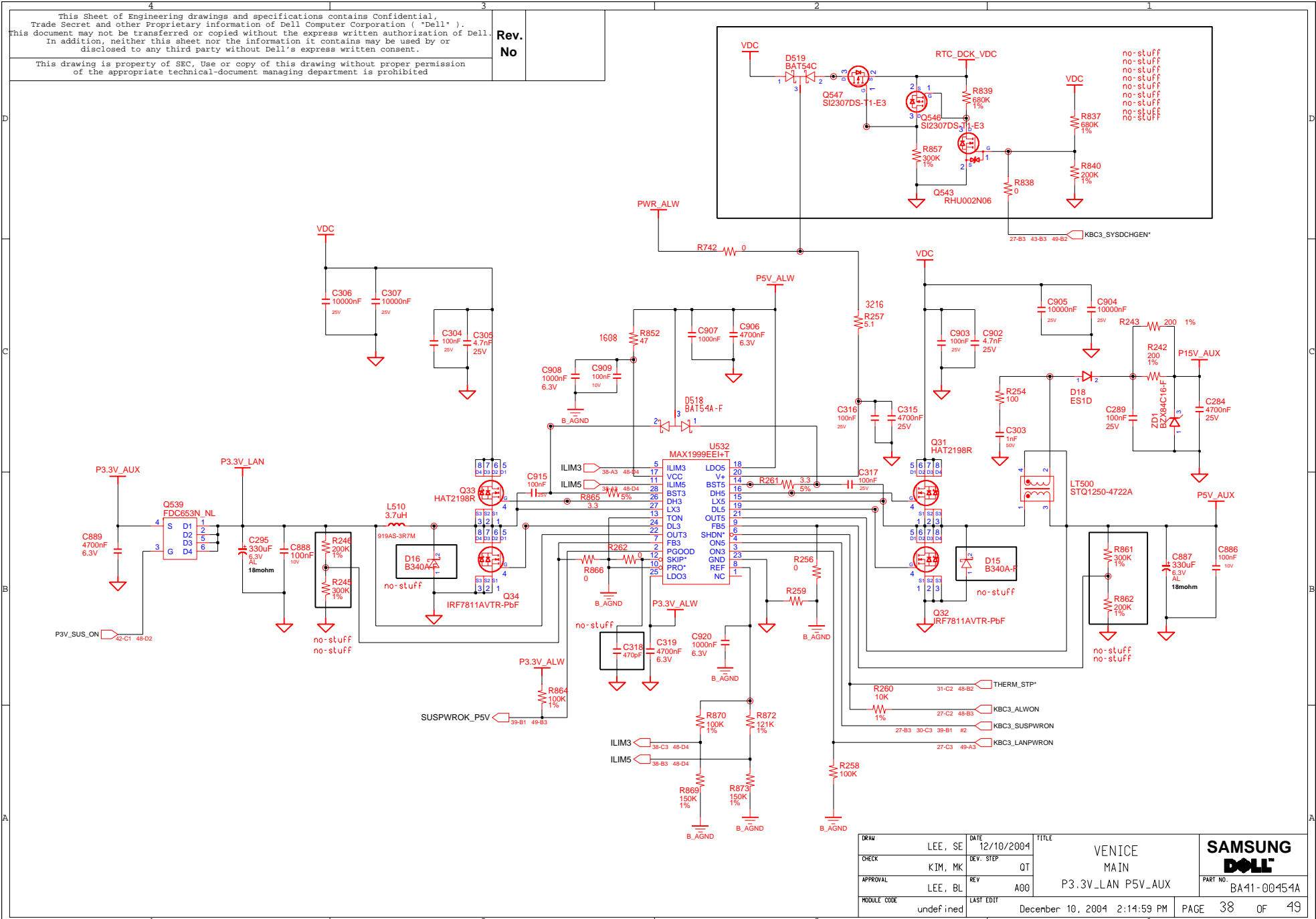


DRAW	LEE, SE	DATE	12/10/2004	TITLE	VENICE MAIN CHARGER DC-IN JACK	<b>SAMSUNG</b> <b>DELL</b> PART NO. BA41-00454A
CHECK	KIM, MK	DEV. STEP	QT			
APPROVAL	LEE, BL	REV	A00			
MODULE CODE	undef:ned	LAST EDIT	December 10, 2004 2:14:59 PM	PAGE	37 OF 49	

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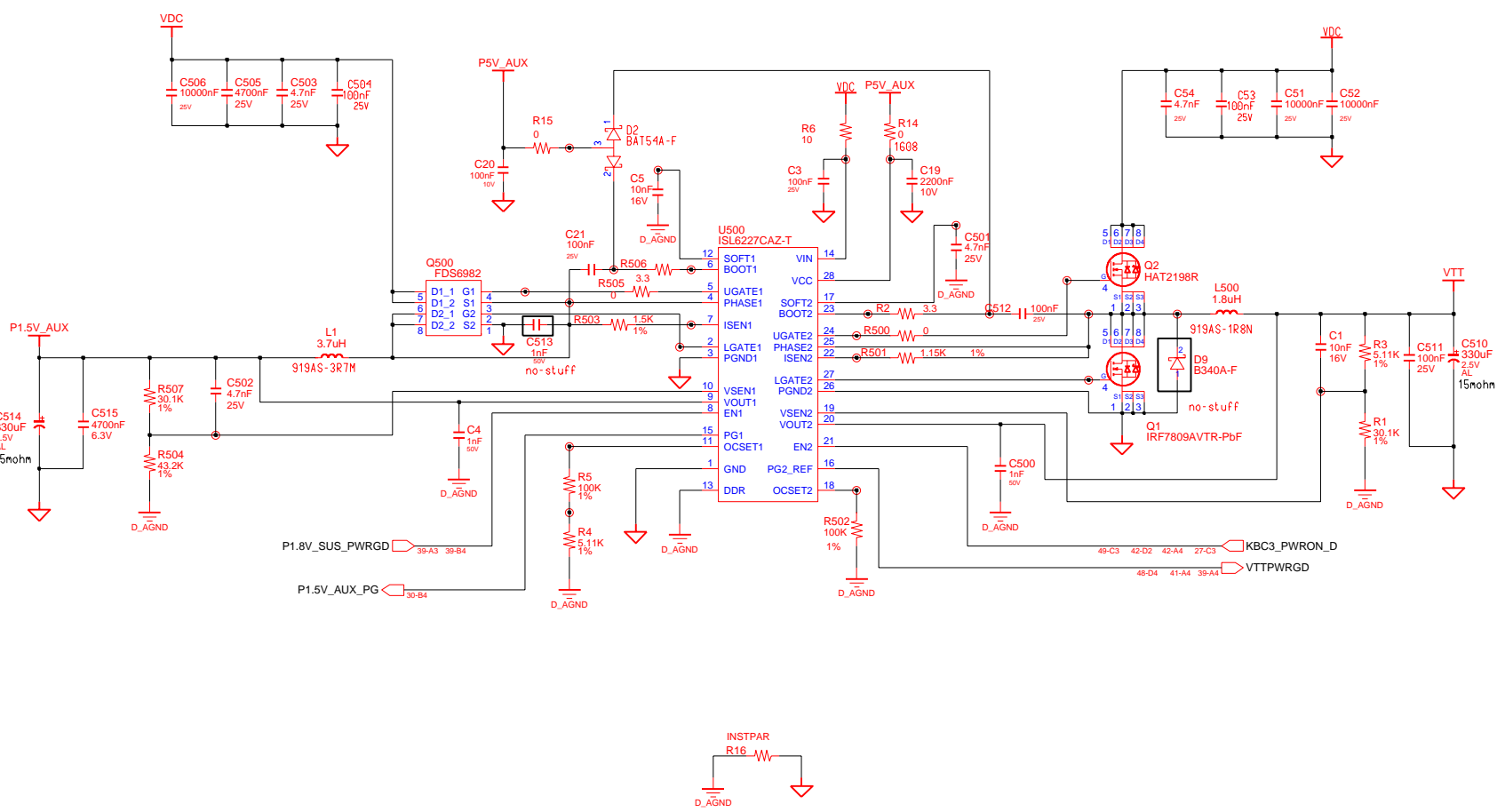
DRAW	LEE, SE	DATE	12/10/2004	TITLE	VENICE MAIN P3.3V_LAN P5V_AUX	<b>SAMSUNG</b> <b>DELL</b> PART NO. BA41-00454A
CHECK	KIM, MK	DEV. STEP	0T			
APPROVAL	LEE, BL	REV	A00			
MODULE CODE	undefined	LAST EDIT	December 10, 2004 2:14:59 PM	PAGE	38 OF 49	



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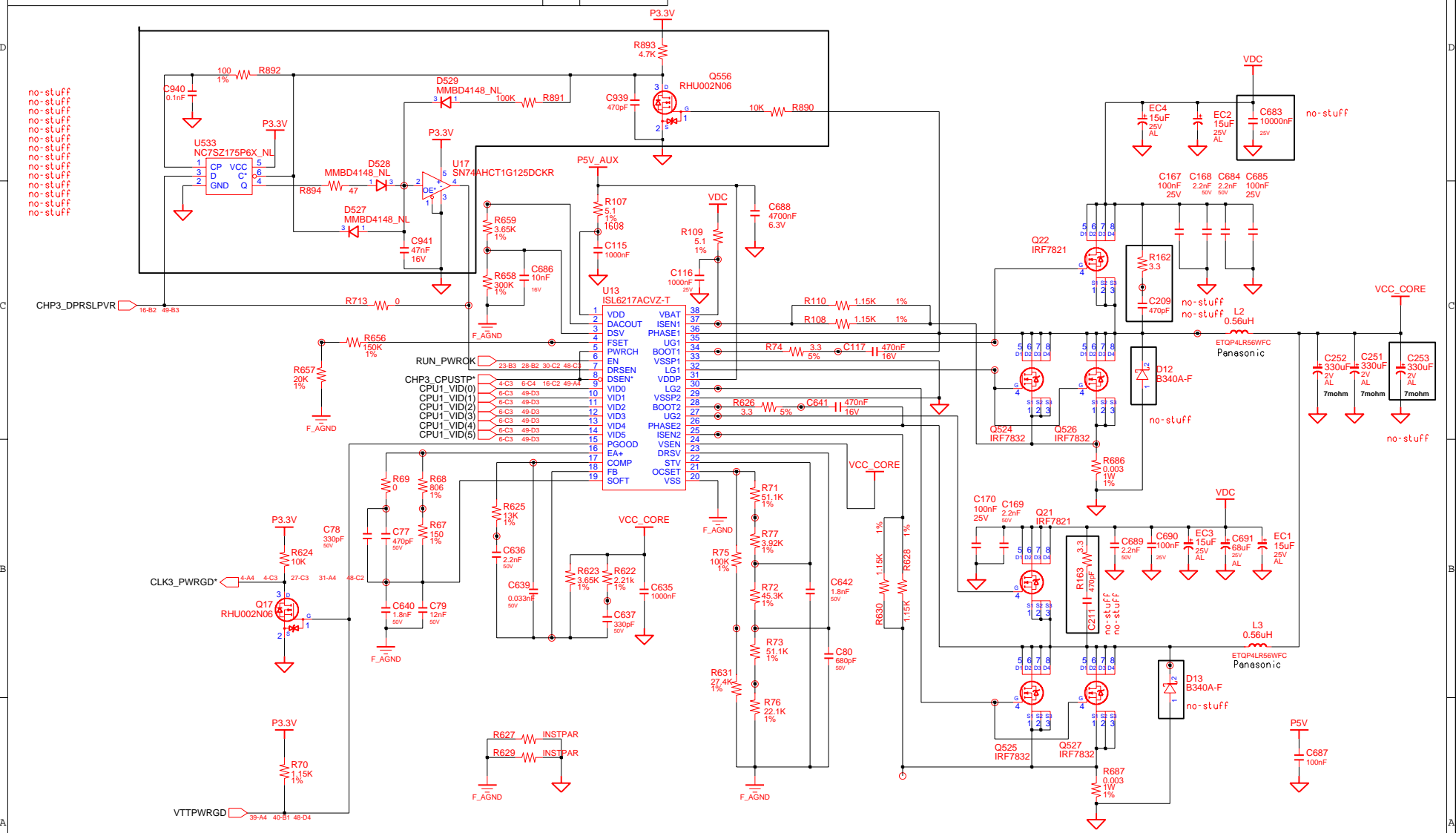
DRAW	LEE, SE	DATE	12/10/2004	TITLE	VENICE MAIN VTT/P1.5V_AUX	<b>SAMSUNG</b> <b>DELL</b> PART NO. BA41-00454A
CHECK	KIM, MK	DEV. STEP	QT	APPROVAL	LEE, BL	
MODULE CODE	undefined	LAST EDIT	December 10, 2004 2:14:59 PM	PAGE	40	OF 49



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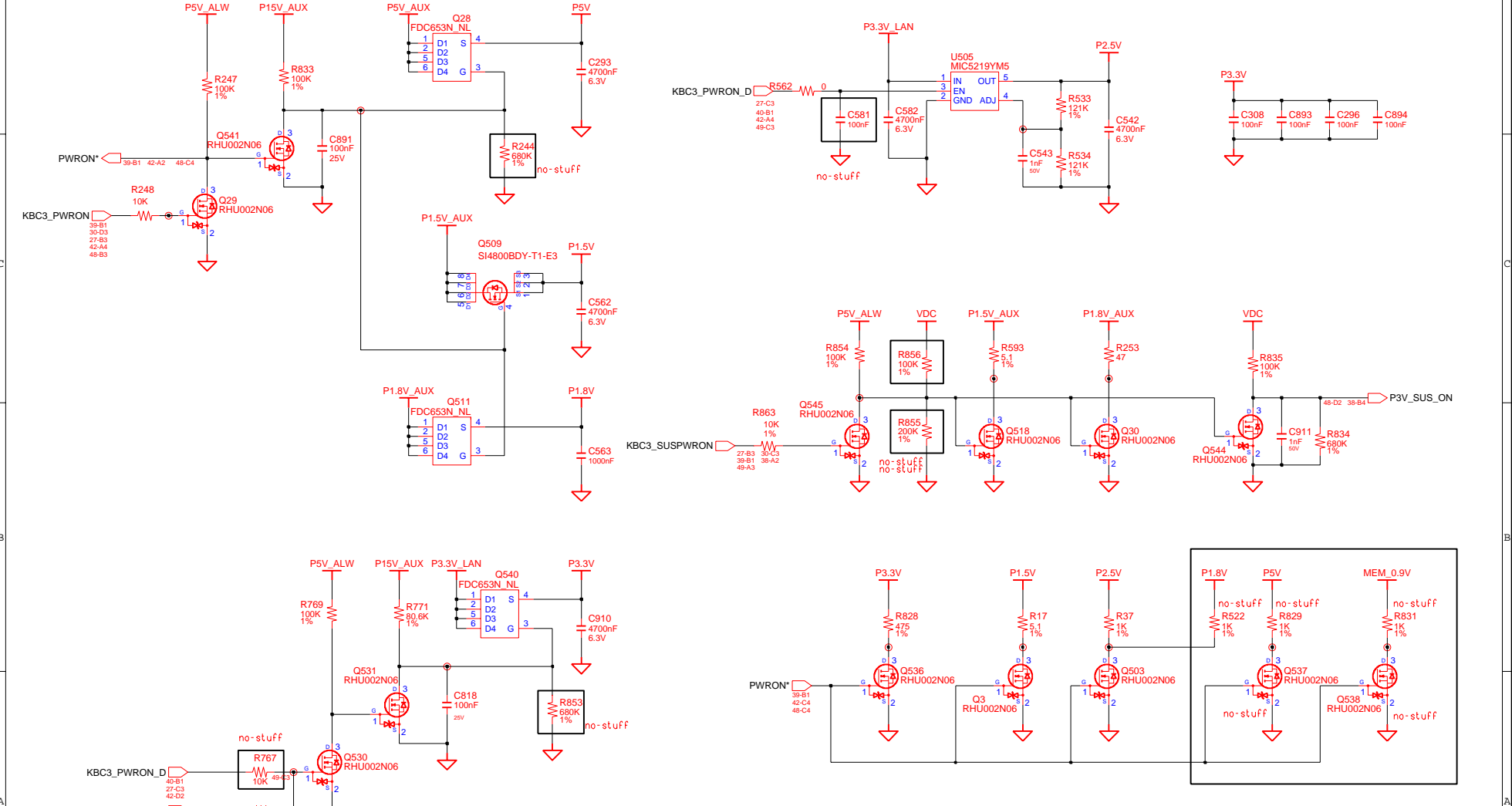


DRAW	LEE, SE	DATE	12/10/2004	TITLE	VENICE MAIN VCC_CORE	<b>SAMSUNG</b> <b>DELL</b> PART NO. BA41-00454A
CHECK	KIM, MK	DEV. STEP	QT			
APPROVAL	LEE, BL	REV	A00			
MODULE CODE		LAST EDIT	December 10, 2004 2:14:59 PM	PAGE	41 OF 49	

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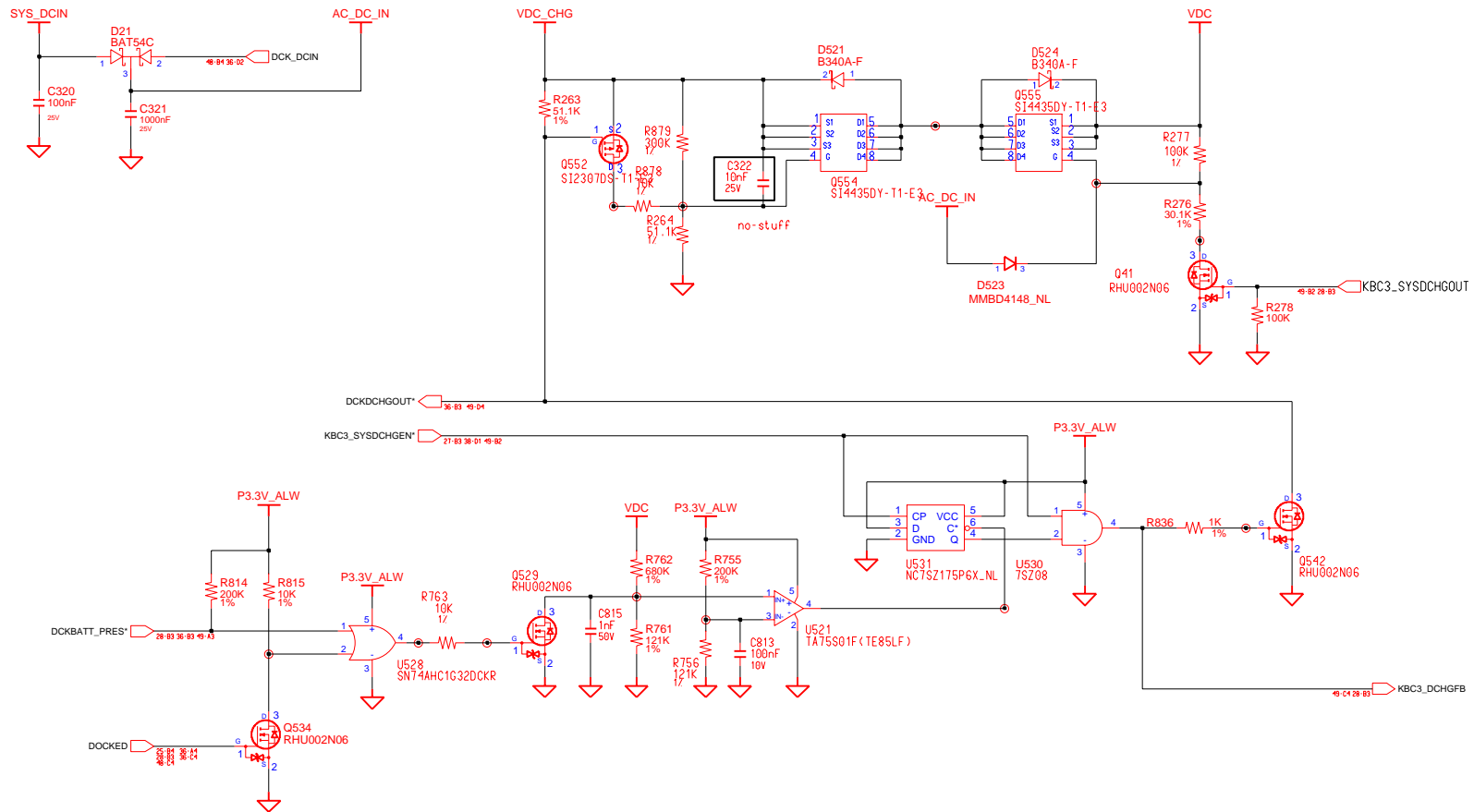


DRAW	LEE, SE	DATE	12/10/2004	TITLE	VENICE MAIN Switched Power	<b>SAMSUNG</b> <b>DELL</b> PART NO. BA41-00454A
CHECK	KIM, MK	DEV. STEP	QT			
APPROVAL	LEE, BL	REV	A00			
MODULE CODE	undefined	LAST EDIT	December 10, 2004 2:14:59 PM	PAGE	42 OF 49	

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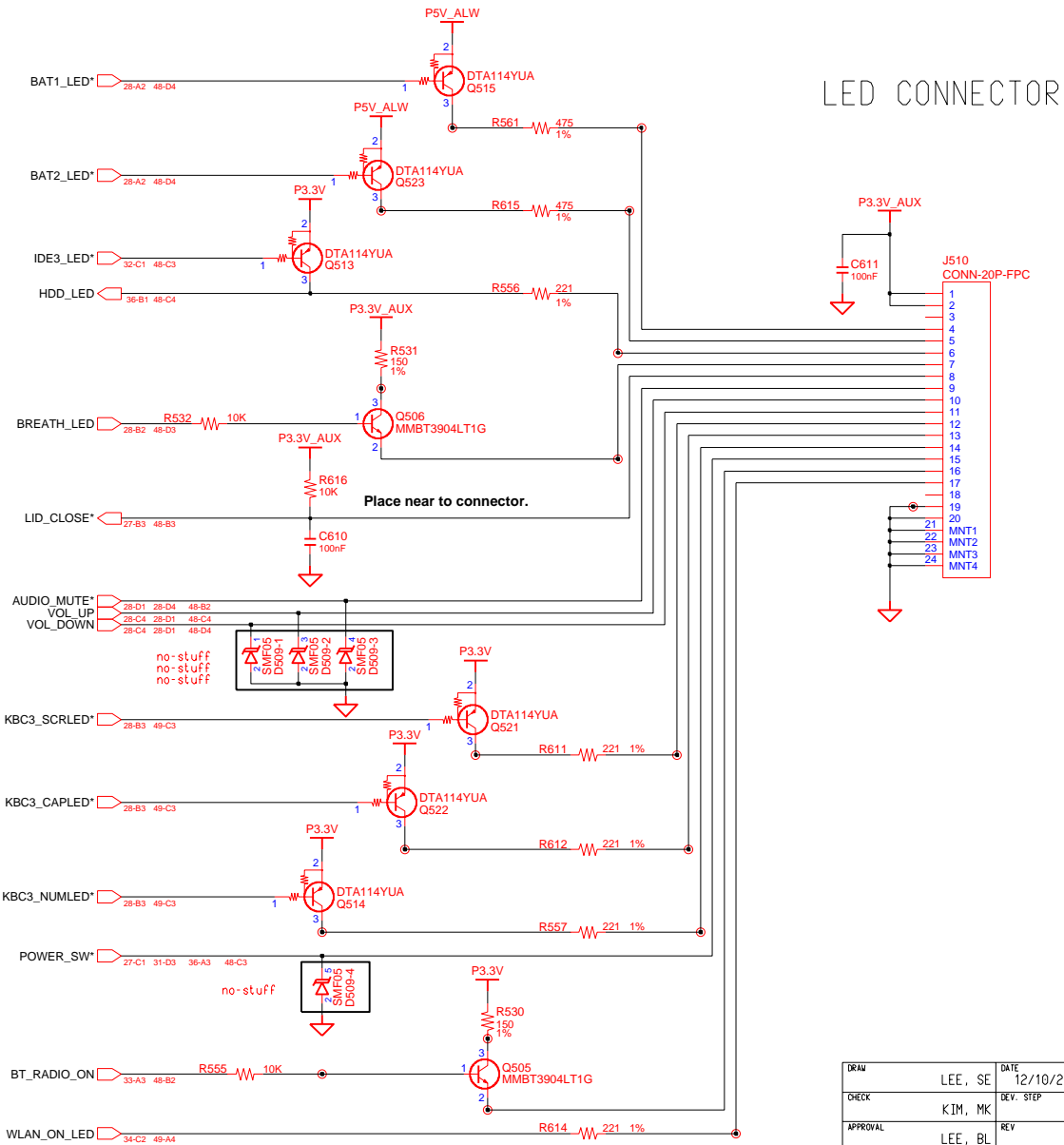


DRAW	LEE, SE	DATE	12/10/2004	TITLE	VENICE MAIN	SAMSUNG DELL
CHECK	KIM, MK	DEV. STEP	QT	Sequent ial Changing		
APPROVAL	LEE, BL	REV	A00			PART NO. BA41-00454A
MODULE CODE	undefined	LAST EDIT	December 10, 2004 2:14:59 PM	PAGE	43	OF 49

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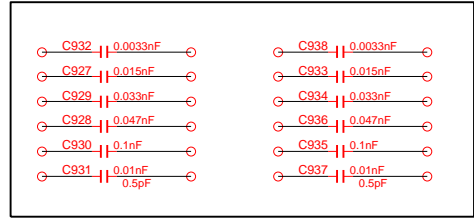
LED CONNECTOR

DRAW	LEE, SE	DATE	12/10/2004	TITLE	VENICE MAIN LED Connector	<b>SAMSUNG</b> <b>DELL</b> PART NO. BA41-00454A
CHECK	KIM, MK	DEV. STEP	QT			
APPROVAL	LEE, BL	REV	A00			
MODULE CODE	undefined	LAST EDIT	December 10, 2004 2:14:59 PM	PAGE	44	OF 49

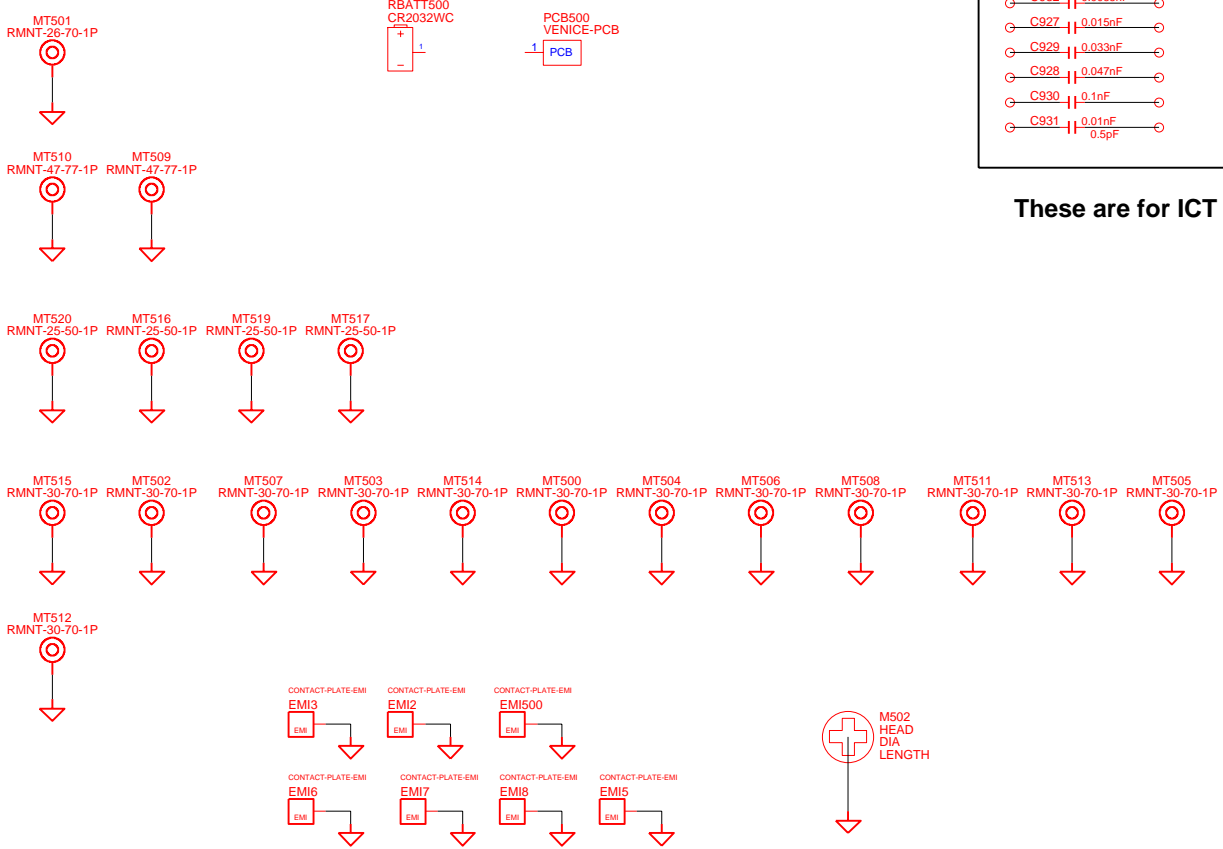
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These are for ICT using.



PCB REVISION CONTROL ( ICT )				
NO	CONNECTION	DATE(Y/M/DD)	REVISION	STEP
1	N.C.	04/04/02	0.1	X00
2	1-2			
3	2-3			
4	3-1			
5	1-2-3			
6	N.C.			
7	1-2			
8	2-3			
9	3-1			
10	1-2-3			

REV500  
1 ○  
2 ○ ○3

DRAW	LEE, SE	DATE	12/10/2004	TITLE	VENICE MAIN MOUNT HOLE	<b>SAMSUNG</b> <b>DOLL</b> PART NO. BA41-00454A
CHECK	KIM, MK	DEV. STEP	QT			
APPROVAL	LEE, BL	REV	A00			
MODULE CODE		LAST EDIT	December 10, 2004 2:14:59 PM	PAGE 45 OF 49		

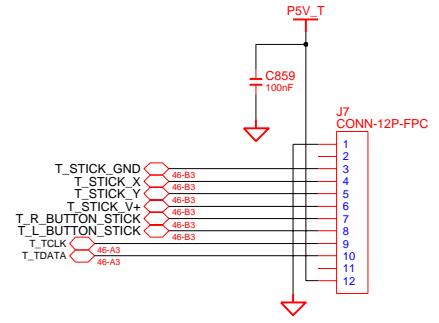
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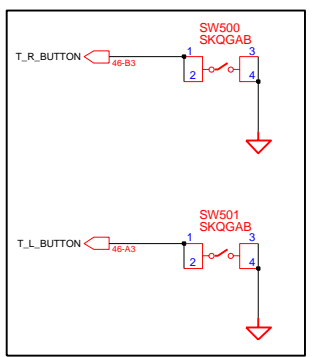
Rev.  
No

# # TOUCHPAD IF BOARD

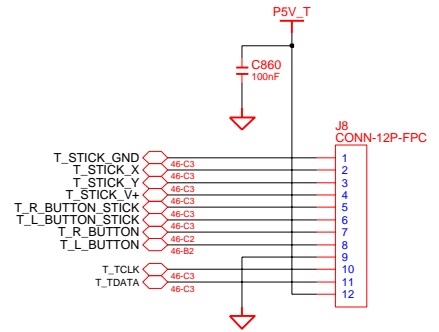
## Main to Touchpad IF board



## Place on Top side



## Touchpad IF board to Touchpad



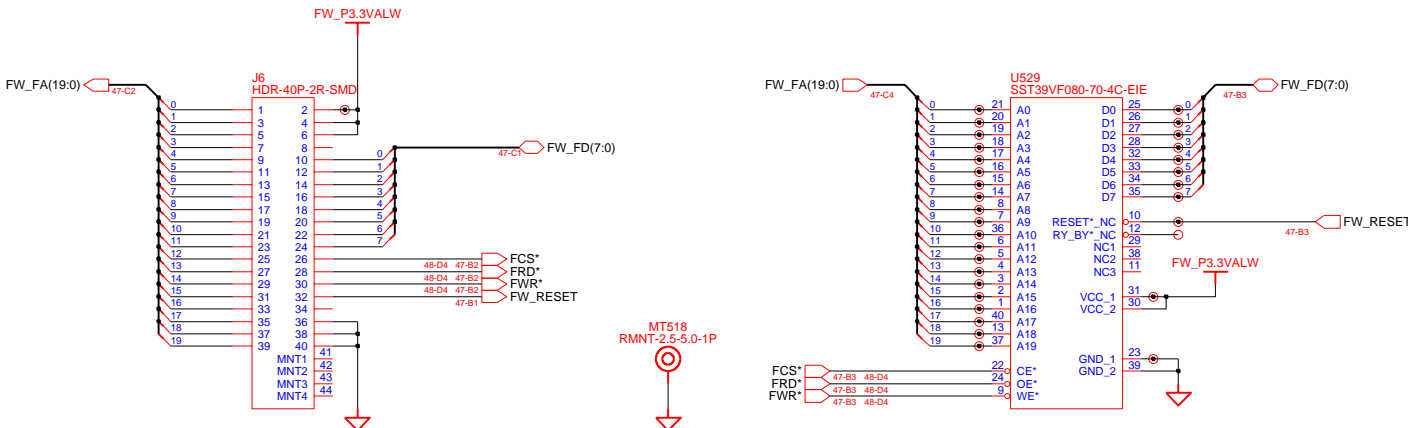
DRAW	LEE, SE	DATE	12/10/2004	TITLE	VENICE MAIN	<b>SAMSUNG</b> <b>DELL</b>
CHECK	KIM, MK	DEV. STEP	QT	TOUCHPAD IF BOARD		
APPROVAL	LEE, BL	REV	A00			PART NO. BA41-00454A
MODULE CODE	LAST EDIT		December 10, 2004 2:14:59 PM	PAGE	46	OF 49

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# Firm Ware Daughter Board



**AMD : Pin 10 is RESET\* ; Pin12 is RY/BY\*  
SST : Pin 10, 12 are NC.**

DRAW	LEE, SE	DATE	12/10/2004	TITLE	VENICE MAIN	SAMSUNG DELL
CHECK	KIM, MK	DEV. STEP	QT	Firmware DAUGHTER BOARD		
APPROVAL	LEE, BL	REV	A00			PART NO. BA41-00454A
MODULE CODE	undefined	LAST EDIT	December 10, 2004 2:14:59 PM	PAGE	47	OF 49

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No

- FCS\*
- FRD\*
- FMR\*
- HP\_IN
- ILIM3
- ILIM5
- OLEN\*
- CB3\_D2
- DOCKED
- PWON\*
- SC3\_CLK
- SC3\_FCB
- SC3\_RFU
- SC3\_RST
- VOL\_UP
- CB3\_A18
- CB3\_A19
- CB3\_D14
- DCK\_PAR
- CHDD\_LED
- IDE3\_A0
- IDE3\_A1
- IDE3\_A2
- MB\_MUTE
- CBUFEN\*
- SC3\_DATA
- STICK\_X
- STICK\_Y
- TPM\_EN\*
- USB\_EN\*
- ATF\_INT\*
- CB3\_CLK
- CB3\_CPAR
- CB3\_CVS1
- CB3\_CVS2
- CB3\_DATA
- CB3\_SPKR
- CPUI\_NMI
- DCK\_DCIN
- DCK\_PME\*
- HP\_OUT\_L
- HP\_OUT\_R
- LCD\_TEST
- PC13\_PAR
- SMB3\_CLK
- STICK\_V+
- SUSPWROK
- TV03\_C\_R
- TV03\_Y\_G
- VOL\_DOWN
- VTTPWROK
- AUD3\_EAPD
- AUD3\_SPKR
- BAT1\_LED\*
- BAT2\_LED\*
- BOARD\_ID0
- BOARD\_ID1
- BOARD\_ID2
- BOARD\_ID3
- CB3\_CCD1
- CB3\_CCD2\*
- CB3\_CCNT\*
- CB3\_CINT\*
- CB3\_CLOCK
- CB3\_CRS1\*
- CB3\_LATCH
- CHP3\_PME\*
- CHP3\_SPKR
- CLK3\_CS48
- CPUI\_ADS\*
- CPUI\_BNR\*
- CPUI\_HIT\*
- CPUI\_INTR
- CPUI\_RS0\*
- CPUI\_RS1\*
- CPUI\_RS2\*
- CPUI\_SLP\*
- CPUI\_SW1\*
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- DCK\_AD(1)
- DCK\_AD(2)
- DCK\_AD(3)
- DCK\_AD(4)
- DCK\_AD(5)
- DCK\_AD(6)
- DCK\_AD(7)
- DCK\_AD(8)
- DCK\_AD(9)
- DCK\_GNT0\*
- DCK\_IDSEL
- DCK\_IRDY\*
- DCK\_LOCK\*
- DCK\_PERR\*
- DCK\_STOP\*
- DCK\_TRDY\*
- DEBUG\_OUT
- DCK\_PSID
- DV13\_SCLK
- DV13\_SDA1
- FAN3\_TACH
- ICH\_PWROK
- IDE3\_CS1\*
- IDE3\_CS3\*
- IDE3\_D(0)
- IDE3\_D(1)
- IDE3\_D(2)
- IDE3\_D(3)
- IDE3\_D(4)
- IDE3\_D(5)
- IDE3\_D(6)
- IDE3\_D(7)
- IDE3\_D(8)
- IDE3\_D(9)
- IDE3\_D(9)
- IDE3\_D(9)
- IDE3\_DREQ
- IDE3\_I0\*
- IDE3\_I0I\*
- IDE3\_LED\*
- KBC3\_A20C
- KBC3\_FCS\*
- KBC3\_FRD\*
- KBC3\_FWE\*
- KBC3\_PSID
- KBC3\_SPKR
- KBC5\_KCLK
- KBC5\_MCLK
- KBC5\_TCLK
- PC13\_PME\*
- PC13\_RST\*
- PL13\_RST\*
- POWER\_SW\*
- RUN\_PWROK
- SC3\_DETECT
- SFI\_RESET\*
- SI03\_IREX
- SI03\_IRTX
- SI0\_FA(0)
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- SI0\_FA(2)
- SI0\_FA(3)
- SI0\_FA(4)
- SI0\_FA(5)
- SI0\_FA(6)
- SI0\_FA(7)
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- SI0\_FA(9)
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- SI0\_FD(2)
- SI0\_FD(3)
- SI0\_FD(4)
- SI0\_FD(5)
- SI0\_FD(6)
- SI0\_FD(7)
- SMB3\_DATA
- STICK\_GND
- TV03\_COMP
- USB3\_OC0\*
- USB3\_OC3\*
- USB3\_OC4\*
- ADAPTER\_IN
- BREATH\_LED
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- CB3\_CAD(2)
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- CB3\_CAD(9)
- CB3\_CAUDIO
- CB3\_CCBE0\*
- CB3\_CCBE1\*
- CB3\_CCBE2\*
- CB3\_CCBE3\*
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- CB3\_CPERR\*
- CB3\_CSERR\*
- CB3\_CSTOP\*
- CB3\_CTRDY\*
- DCK\_AD(10)
- DCK\_AD(11)
- DCK\_AD(12)
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- DCK\_AD(14)
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- DCK\_AD(19)
- DCK\_AD(20)
- DCK\_AD(21)
- DCK\_AD(22)
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- DCK\_AD(25)
- DCK\_AD(26)
- DCK\_AD(27)
- DCK\_AD(30)
- DCK\_AD(31)
- DCK\_FRAME\*
- DCK\_LAD(0)
- DCK\_LAD(1)
- DCK\_LAD(2)
- DCK\_LAD(3)
- DCK\_PIRQ\*
- DCK\_SERIRQ
- DOCK\_DET1\*
- IDE3\_D(10)
- IDE3\_D(11)
- IDE3\_D(12)
- IDE3\_D(13)
- IDE3\_D(14)
- IDE3\_D(15)
- IDE3\_DACK\*
- IDE3\_IORDY\*
- IMVP\_PWRGD
- KBC3\_ALWON
- KBC3\_PWROK
- KBC3\_THRM\*
- KBC5\_KDATA
- KBC5\_MDATA
- KBC5\_TDATA
- LCD2\_VDDEN
- LID\_CLOSE\*
- VGA3\_HSYNC
- VGA3\_VSYNC
- SV\_CAL\_SJ0\*
- AUDIO\_MUTE\*
- BT\_RADIO\_ON
- CB3\_CAD(10)
- CB3\_CAD(11)
- CB3\_CAD(12)
- CB3\_CAD(13)
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- CB3\_CAD(15)
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- CB3\_CFRAME\*
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- CHP3\_LDR0\*
- CHP3\_LDR01\*
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- CHP3\_SLPSS\*
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- PC13\_AD(7)
- PC13\_AD(8)
- PC13\_AD(9)
- PC13\_CBE0\*
- PC13\_CBE1\*
- PC13\_CBE2\*
- PC13\_CBE3\*
- PC13\_GNT0\*
- PC13\_GNT1\*
- PC13\_GNT3\*
- PC13\_INTA\*
- PC13\_INTB\*
- PC13\_INT\*
- PC13\_INTD\*
- PC13\_IRDY\*
- PC13\_PERR\*
- PC13\_RE0\*
- PC13\_RE01\*
- PC13\_RE03\*
- PC13\_SERR\*
- PC13\_STOP\*
- PC13\_TRDY\*
- PL13\_RSTF\*
- REFCLK\_SEL
- RESET\_OUT\*
- SI0\_FA(10)
- SI0\_FA(11)
- SI0\_FA(12)
- SI0\_FA(13)
- SI0\_FA(14)
- SI0\_FA(15)
- SI0\_FA(16)
- SI0\_FA(17)
- SI0\_FA(18)
- SI0\_FA(19)
- SOUND\_MUTE\*
- SPDIF\_SHDN
- THERM\_STP\*
- P3V\_SUS\_ON
- CLK3\_PCLKCB
- CLK3\_PWRGD\*
- CLK3\_SMBCLK

DRAW	LEE, SE	DATE	12/10/2004	TITLE	VENICE MAIN TEST POINT	<b>SAMSUNG</b> <b>DELL</b> PART NO. BA41-00454A
CHECK	KIM, MK	DEV. STEP	QT	APPROVAL	LEE, BL	
MODULE CODE		LAST EDIT	December 10, 2004 2:14:59 PM	PAGE	48	OF 49



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<p>           ○DCKDCHGOUT*            ○DCK_ACTIVE*            ○DCK_CLKRUN*            ○DCK_DEVSEL*            ○DCK_DLRQ1*            ○DCK_LFRAME*            ○DCK_LINK10*            ○DCK_PCIRST*            ○DCK_PC1EN*            ○DV13_DETECT              ○IDE3_IDEIRQ              ○KBC3_BKLTON            ○KBC3_DCHGFB            ○KBC3_FANPWM            ○KBC5_KSI(0)            ○KBC5_KSI(1)            ○KBC5_KSI(2)            ○KBC5_KSI(3)            ○KBC5_KSI(4)            ○KBC5_KSI(5)            ○KBC5_KSI(6)            ○KBC5_KSI(7)              ○KBC5_KSO(1)            ○KBC5_KSO(2)            ○KBC5_KSO(3)            ○KBC5_KSO(4)            ○KBC5_KSO(5)            ○KBC5_KSO(6)            ○KBC5_KSO(7)            ○KBC5_KSO(8)            ○KBC5_KSO(9)              ○LAN_LOW_PWR              ○LCD2_BIAPWM            ○LCD2_BKLTON            ○LCD2_DDCCLK            ○LCD3_BKLTON            ○LPC3_LAD(0)            ○LPC3_LAD(1)            ○LPC3_LAD(2)            ○LPC3_LAD(3)            ○PC13_AD(10)            ○PC13_AD(11)            ○PC13_AD(12)            ○PC13_AD(13)            ○PC13_AD(14)            ○PC13_AD(15)            ○PC13_AD(16)            ○PC13_AD(17)            ○PC13_AD(18)            ○PC13_AD(19)            ○PC13_AD(20)            ○PC13_AD(21)            ○PC13_AD(22)            ○PC13_AD(23)            ○PC13_AD(24)            ○PC13_AD(25)            ○PC13_AD(26)            ○PC13_AD(27)            ○PC13_AD(28)            ○PC13_AD(29)            ○PC13_AD(30)            ○PC13_AD(31)            ○PC13_FRAME*            ○PC13_PLCK*            ○SI03_IRMODE              ○THERMTRIP1*            ○THERMTRIP2*              ○VGA2_DDCCLK            ○WLAN_ON_LED            ○AUD103_SPDIF*            ○CB3_CLKRUN*            ○CB3_CODESEL*            ○CHP3_CPUS1P*            ○CHP3_CPUS1P*            ○CHP3_RTORST*         </p>	<p>           ○CPU1_DEFER*            ○CPU1_DPSLP*            ○CPU1_IGNNE*            ○CPU1_VID(0)            ○CPU1_VID(1)            ○CPU1_VID(2)            ○CPU1_VID(3)            ○CPU1_VID(4)            ○CPU1_VID(5)            ○CLK3_AUD14_1            ○CLK3_PCLKBOM            ○CLK3_PCLKSIO            ○CLK3_SMBDATA              ○CPU1_DPRSTP*            ○CPU1_STPCLK*            ○CPU2_THERMDA            ○CPU2_THERMDC            ○DCK_LINK100*            ○DCK_DWNS_PC1              ○DEBUG_ENABLE            ○DCK_SMB_CLK            ○DCK_SMB_DAT            ○DV02_CTRLCLK            ○KBC3_CAPLED*            ○KBC3_DCKDCEN            ○KBC3_EXISMT*            ○KBC3_IDERS1*            ○KBC3_NUMLED*            ○KBC3_PWRBTN*            ○KBC3_PWRON_D            ○KBC3_RUNSCT*            ○KBC3_SCRLED*            ○KBC5_KSO(10)            ○KBC5_KSO(11)            ○KBC5_KSO(12)            ○KBC5_KSO(13)            ○KBC5_KSO(14)            ○KBC5_KSO(15)            ○KBC5_KSO(16)            ○KBC5_KSO(17)            ○LAN3_ACTIVE*            ○LAN3_LINK10*              ○LCD2_DDCDATA            ○LPC3_LFRAME*            ○MCH1_HXSWING            ○MCH1_HYSWING            ○MCH2_BMBUS*            ○PC13_CLKRUN*            ○PC13_DEVSEL*            ○SUSPWROK_P5V              ○VGA2_DDCDATA            ○VGA3_RED_INT            ○AUD3_AC97_SDO            ○AUDIO_AVDD_ON            ○AUD_MIC_CODEC            ○CHP3_DPRSLPVR              ○CLK3_PCLKDOCK            ○CPU1_PROGHOT*            ○DBAY_MODPRES*            ○DCKBATT_PRES*              ○DCK_SMB_INT*            ○DV02_CTRLDATA            ○HW_RADIO_DIS*            ○KBC3_LANPWON            ○KBC3_PROGHOT*            ○KBC3_SUSPWROK            ○KBC3_SYSG24            ○KBC3_SYSG24            ○KBC3_SYSGCHEN            ○KBC3_WAKEESC*            ○LAN3_LINK10*            ○LCD3_CLK_EDID            ○LCD5_LAMPSTAT            ○MDC3_AC97_SDO         </p>	<p>           ○PC13_CB_GRST*            ○SYSBATT_PRES*            ○THERMTRIP_SIO            ○VGA3_BLUE_INT            ○AUD3_AC97_BCLK            ○AUD3_AC97_RST*            ○AUD3_AC97_SDO10            ○AUD3_AC97_SYNC            ○CHP3_INTRUDER*              ○CLK3_PCLKICHGM            ○CPU1_THRMTRIP*              ○KBC3_DCKDCHGEN            ○KBC3_DCK_PWRON            ○KBC3_ICHERCIN*            ○KBC3_PWRUSB_EN              ○LCD3_DATA_EDID            ○LOM_PCIE_WAKE*            ○L_BUTTON_STICK              ○R_BUTTON_STICK            ○SYSBATT_ALERT*            ○VGA3_GREEN_INT              ○COEX1_BT_ACTIVE            ○DOCK_SIO_ALERT*            ○CMCH1_THRMTRIP*            ○KBC3_BATSEL_4_3*            ○KBC3_PCIE_WAKE*            ○KBC3_SYSDCHGEN*            ○KBC3_SYSDCHGOUT            ○KBC3_USBPWR_EN*              ○SYSBATT_SMB_CLK            ○KBC3_THERM_SMCLK            ○SYSBATT_SMB_DATA              ○COEX2_WLAN_ACTIVE            ○KBC3_THERM_SMDATA            ○KBC5_PSTD_DISABLE*            ○AGND              ○AVDD              ○AVDD5              ○AC_DC_IN         </p>	<p>           ○AVDD3_3V              ○B_AGND              ○C_AGND              ○CB3_VCC              ○CB3_VPP              ○D_AGND              ○DOCK_PWR_SRC              ○DOCK_P2_5V_LAN              ○F_AGND            ○INV_VDC            ○LCD_VDD3V            ○LDO_P5_4V            ○MEM_0_3V            ○MCH_P1_5V            ○MAX1909_REF            ○PGND            ○P1_5V              ○P1_8V            ○P2_5V            ○PWR_DC            ○P5V_ALW            ○P5V_AUX            ○P15V_AUX            ○P1_2V_LAN            ○P1_5V_AUX            ○P1_8V_AUX            ○P2_5V_LAN            ○P3_3V_ALW            ○P3_3V_AUX            ○P3_3V_LAN            ○RTC_DCK_VDC            ○RTC_PWR3_3V            ○SC3_VCC            ○SYS_DCIN            ○WDC            ○WTT            ○VCC_RTC            ○VCC_CHG            ○VCC_CORE            ○VCC_OBUF         </p>

DRAW	LEE, SE	DATE	12/10/2004	TITLE	VENICE MAIN TEST POINT	<b>SAMSUNG</b> <b>DELL</b> PART NO. BA41-00454A
CHECK	KIM, MK	DEV. STEP	QT			
APPROVAL	LEE, BL	REV	A00			
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