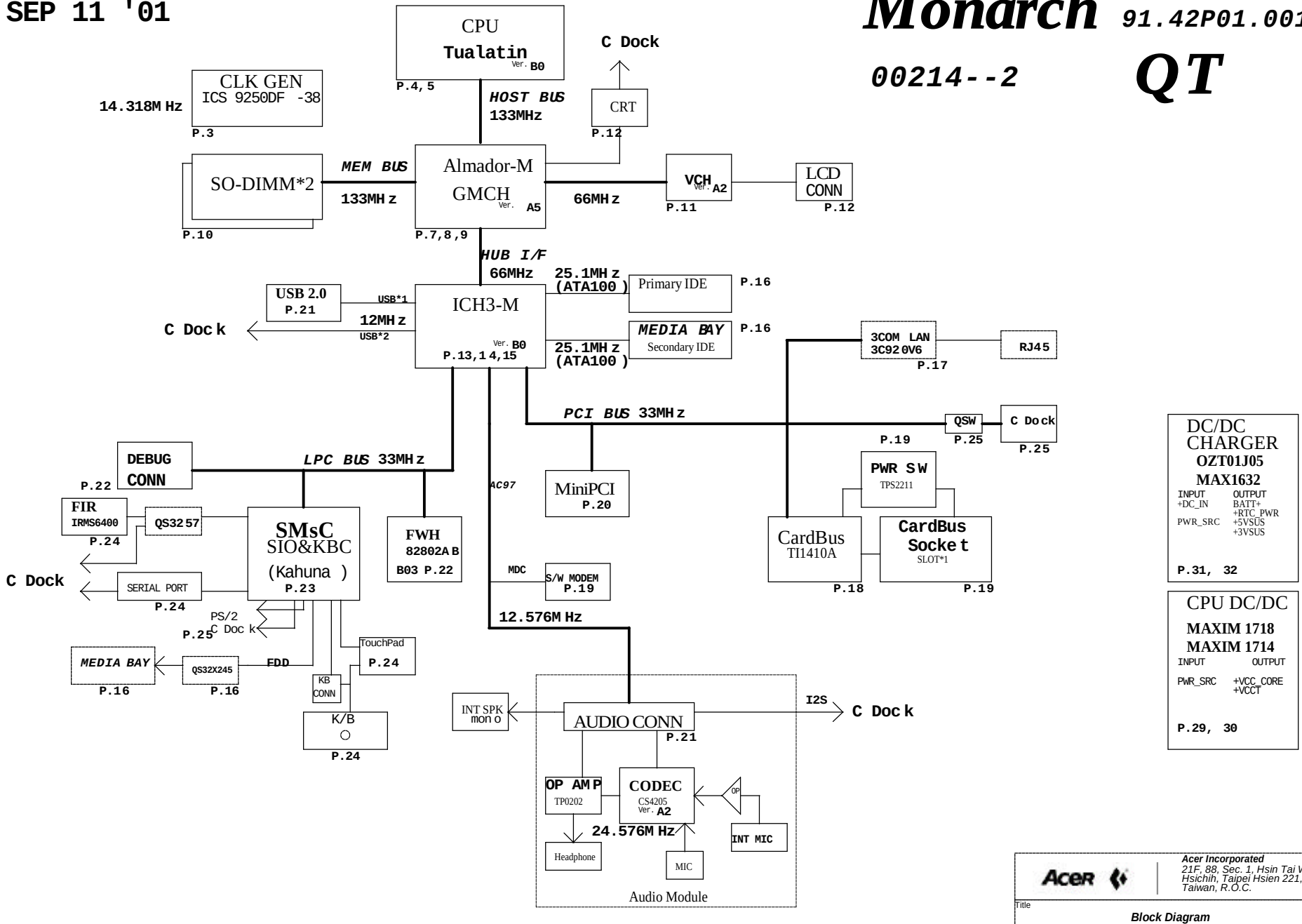
SEP 11 '01

Monarch 91.42P01.001

00214--2 QT



DC/DC CHARGER
OZT01J05
MAX1632

INPUT	OUTPUT
+DC_IN	BATT+
	+RTC_PWR
PWR_SRC	+5VSUS
	+3VSUS

P.31, 32

CPU DC/DC
MAXIM 1718
MAXIM 1714

INPUT	OUTPUT
PWR_SRC	+VCC_CORE
	+VCCT

P.29, 30

Acer Incorporated
21F, 88, Sec. 1, Hsin Tai Wu Rd.,
Hsichih, Taipei Hsien 221,
Taiwan, R.O.C.

Title: Block Diagram

Size: Custom | Document Number: MONARCH -- 00214 | Rev: -1

Date: ¬´¤ ,¤¤ 31, 2002 | Sheet 1 of 33

CG_* : CPU GTL+
CC_* : CPU CMOS
M_* : MEMO RY BUS
G_* : AG P BUS
P_* : PC I BUS
HL_* : HUB L INK I/F
LPC_* : LP C I/F
ICH_AC_* : AC'97 LINK I/F
IDE_* : ID E BUS

PCI TABLE

DEVIC E	IDSE L	IRQ	REQ# / G NT#	DREQ/D GNT
PCMCIA T I1410	AD17	PIRQ D#	REQB# / G NTB#	REQ1# / G NT1#
LAN 3COM- 3C920	AD16	PIRQ C#		REQ4# / G NT4#
MINIPCI SLOT	AD19	PIRQ B# PIRQ D#		REQ3# / G NT3#
C-DO CK		PIRQ B# PIRQ C#		REQ0# / G NT0#

Cu-T & Tualatin SPEC Summary

5 15 ' 01

	QS/ Prod uction
Tuala tin	VCC >= 1.40V (pe rf mode)/ 1.15V (ba tt mode) R274 R306 R303 R275 R279 0R3 0R3 100KR3 10 0KR3 100KR3 VCCT = 1.25V +/- 5 % (static) +/- 9% (transient) R188 R187 2K49R3F 1 0KR3F Tj (min) = 0C
Cu-T	VCC = 1.7V (per f Mode)/ 1.35V (Ba tt Mode) R274 R306 R303 R275 R279 0R3 0R3 0R3 0R3 100KR3 VCCT = 1.25V +/- 5 % (static) +/- 9% (transient)
GMC H	VCC/ VTT = 1.25 V +/- 5%

+SDC_IN +SDC_IN 30,32
+DC_IN +DC_IN 25,30,32
DOCK_DC_IN DOCK_DC_IN 25
PWR_SRC PWR_SRC 12,25,28,29,30,31
DOCK_PWR_SRC DOCK_PWR_SRC 25
+VCCT +VCCT 4,5,6,9,27,30
+VCC_CORE +VCC_CORE 4,5,27,29
+1.5VRUN +1.5VRUN 4,5,6,7,8,9,11,15,22,30
+1.8VRUN +1.8VRUN 4,8,9,11,13,15,28
+1.8VSUS +1.8VSUS 6,15,28,30
+1.5VRUN +1.5VRUN 4,5,6,7,8,9,11,15,22,30
+3VRUN +3VRUN 3,6,8,9,11,12,13,14,15,16,17,19,20,21,22,23,24,25,26,27,28,29,33
+3VSUS +3VSUS 3,6,9,10,12,13,14,15,18,19,20,22,23,27,28,29,30,31
+3VALW +3VALW 6,14,21,23,27
+3.3VRTC +3.3VRTC 14,23,27,28,32
+5VRUN +5VRUN 3,12,15,16,19,20,23,24,25,26,27,28,29,33
+5VSUS_DOCK +5VSUS_DOCK 25
+5VSUS +5VSUS 6,12,14,15,17,19,21,24,25,26,27,28,30,31,33
+5VALW +5VALW 12,23,24,25,26,27,32
+5V_QDOCK +5V_QDOCK 24,25
+3VAUX_LAN +3VAUX_LAN 17,20
+12V +12V 6,12,19,25,28,30,31,33
BATT+ BATT+ 30,32

+5VHDD +5VHDD 16,28
+5VFDD +5VFDD 16,28
+5VMOD +5VMOD 16,28
HUBREF HUBREF 7,9,13
LCDVDD LCDVDD 12
USBPWR1 USBPWR1 21
AC97_5V AC97_5V 19
AC97_3V AC97_3V 19
CRT_VCC CRT_VCC 12
S_VCC S_VCC 18,19

S_VPP S_VPP 19

S_VCCF S_VCCF 19

ICH_VBIAS ICH_VBIAS 14
VCC_LAN1.8 VCC_LAN1.8 15
VCC_LAN3.3 VCC_LAN3.3 15
VCC_RTC VCC_RTC 13,14,15

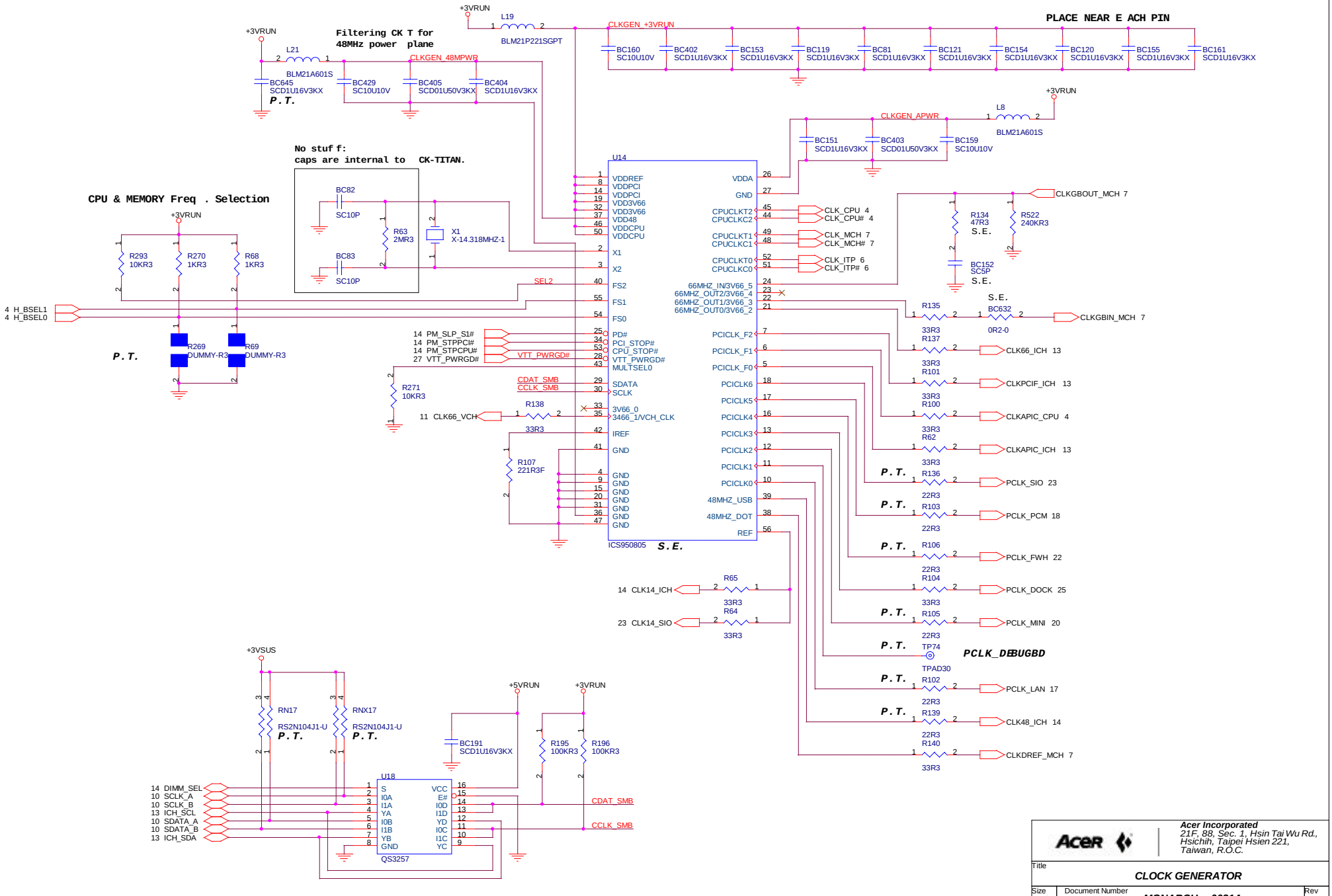
+RTCSRC +RTCSRC 28,30
+RTC_PWR +RTC_PWR 27,28,33

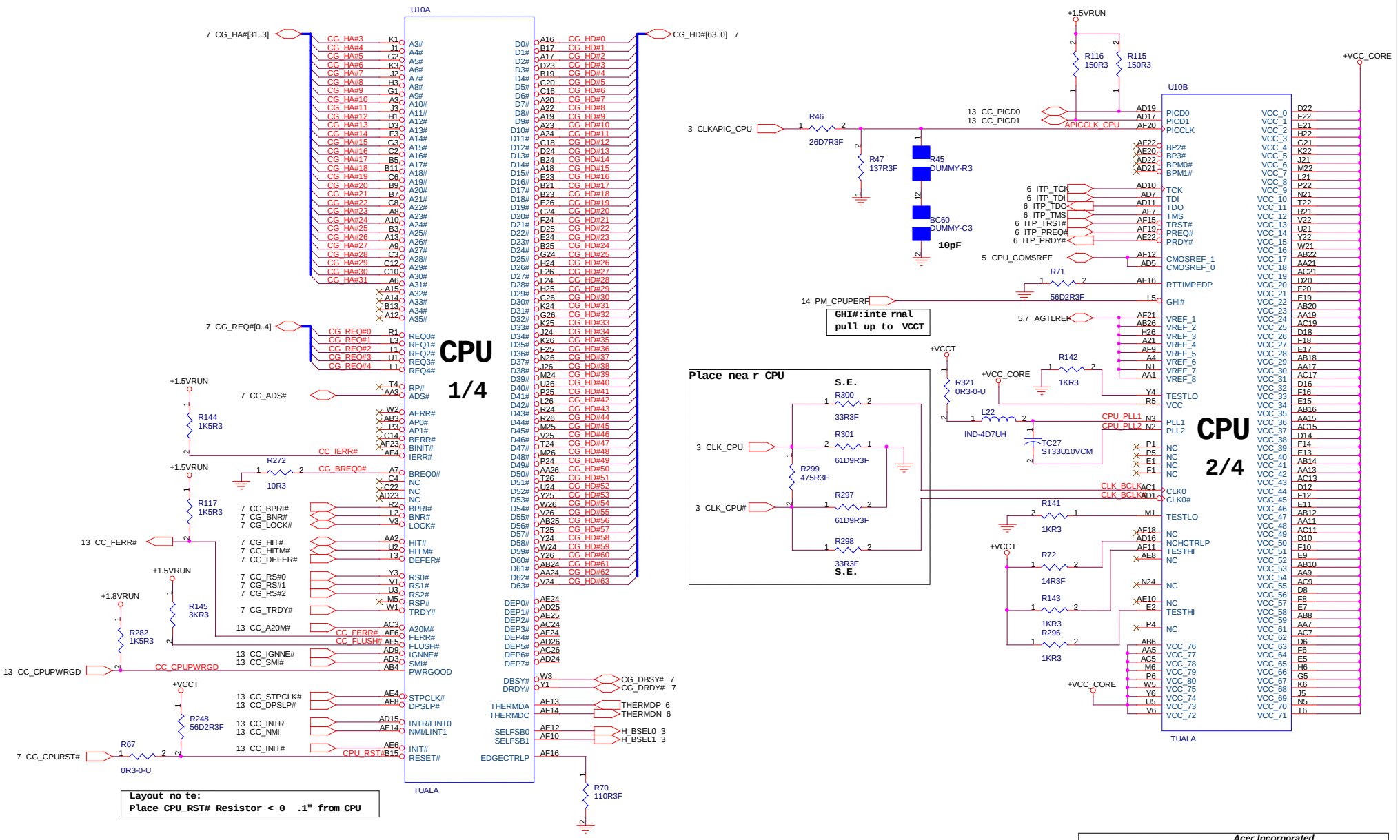
Acer Incorporated
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: ***TABLE OF CONTENT***

Size: A3 | Document Number: ***MONARCH -- 00214*** | Rev: ***-1***

Date: ¬ ´ ¤ , ¤ ¤ 11, 2001 | Sheet 2 of 33


PLACE NEAR E ACH PIN
Filtering CK T for 48MHz power plane
No stuf f: caps are internal to CK-TITAN.
CPU & MEMORY Freq . Selection
U14
ICS950805
S.E.
P.T.
PCLK_DEBUGBD
U18
QS3257
Acer Incorporated
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
CLOCK GENERATOR
Size A3
Document Number MONARCH -- 00214
Rev -1
Date: 11, 2001
Sheet 3 of 33

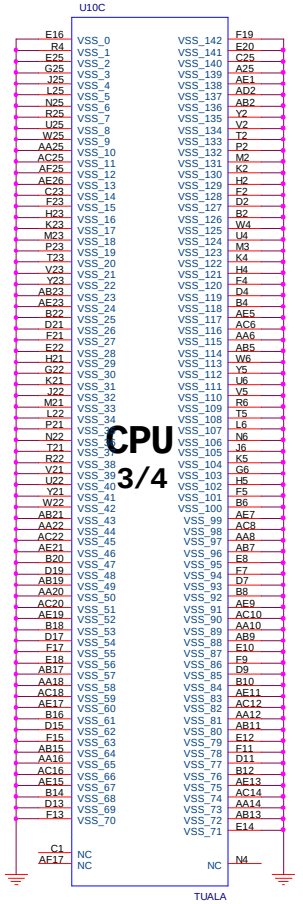


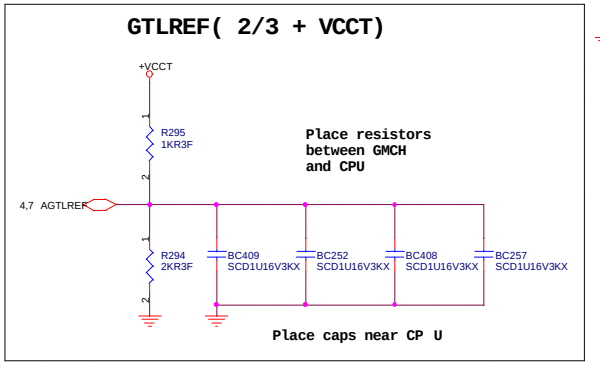
Acer Incorporated
21F, 88, Sec. 1, Hsin Tai Wu Rd.,
Hsichih, Taipei Hsien 221,
Taiwan, R.O.C.

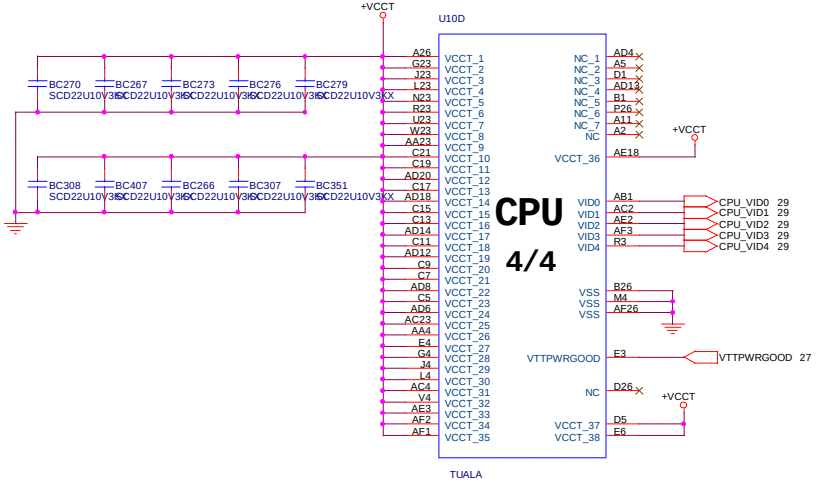
Title: CPU

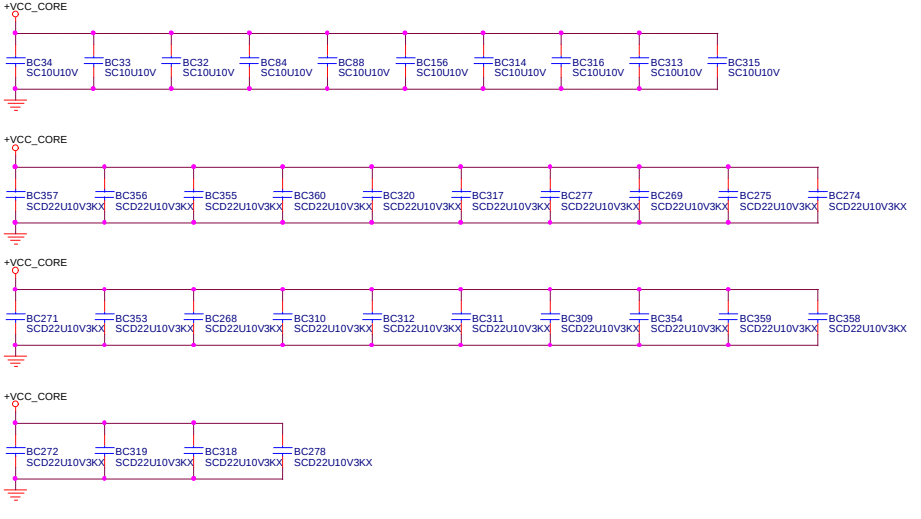
Size: A3 | Document Number: MONARCH -- 00214 | Rev: -1

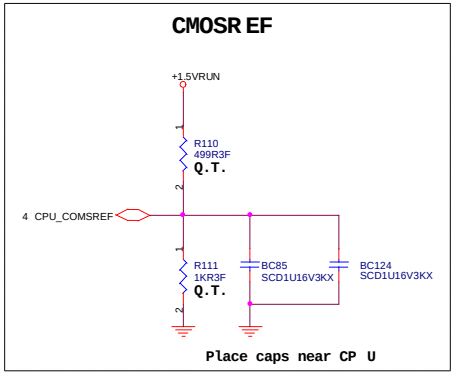
Date: 11, 2001 | Sheet 4 of 33











Decouping Recommendation

				Monarch	Kodiak Ver. 0.5
VCC_CORE	Underneath balls on solder side	0.47uF * 24	Use 2-3 vias per pad for reduced inductance during layout	0.1uF * 24	10uF / 6.3V * 12
	On the peripheral near balls	10uF / 6.3V * 10	Placement should be near processor for all	10uF / 10V * 10	10uF / 6.3V * 10 + 6 * NS
	Bulk Caps			220uF / 2.5V * 8	150uF / 4V * 12 + 2 * NS
VCCT	Place close to processor for all	1uF * 10	Use 2 vias per pad for reduced inductance during layout	1uF * 10	1uF * 10 + 2 * NS
	Bulk Caps			220uF / 2.5V * 2	150uF / 4V * 5 + 1 * NS

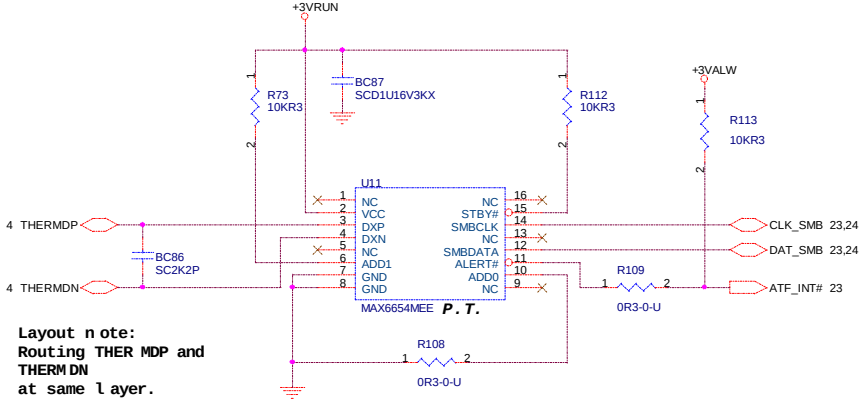
Acer Incorporated
21F, 88, Sec. 1, Hsin Tai Wu Rd.,
Hsichih, Taipei Hsien 221,
Taiwan, R.O.C.

Title: CPU CONFIGURATION

Size: Custom | Document Number: MONARCH -- 00214 | Rev: -1

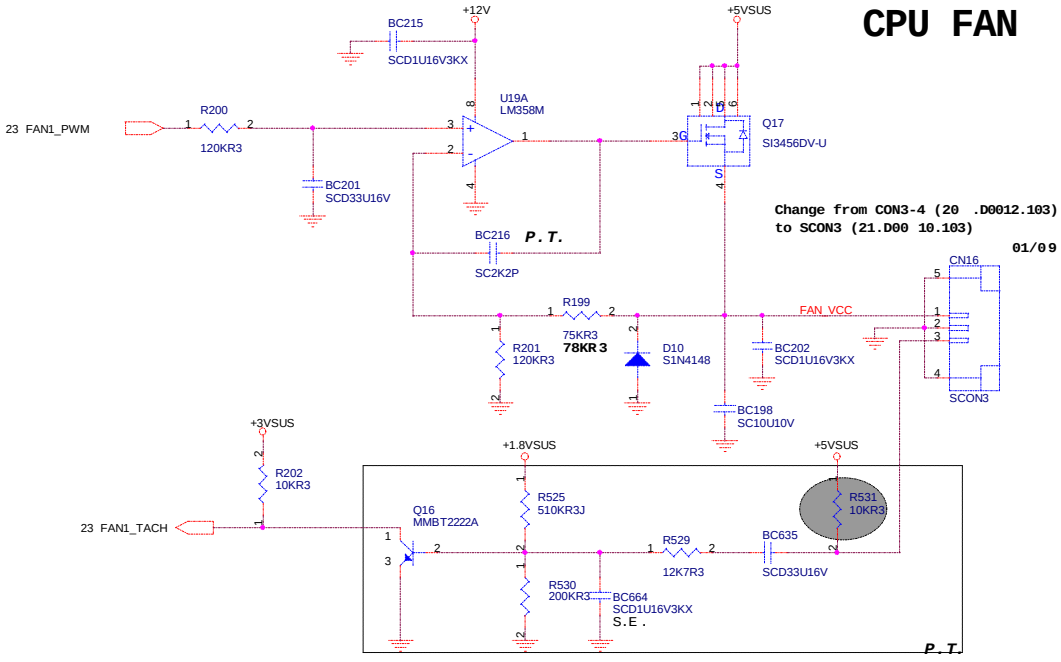
Date: 11, 2001 | Sheet 5 of 33

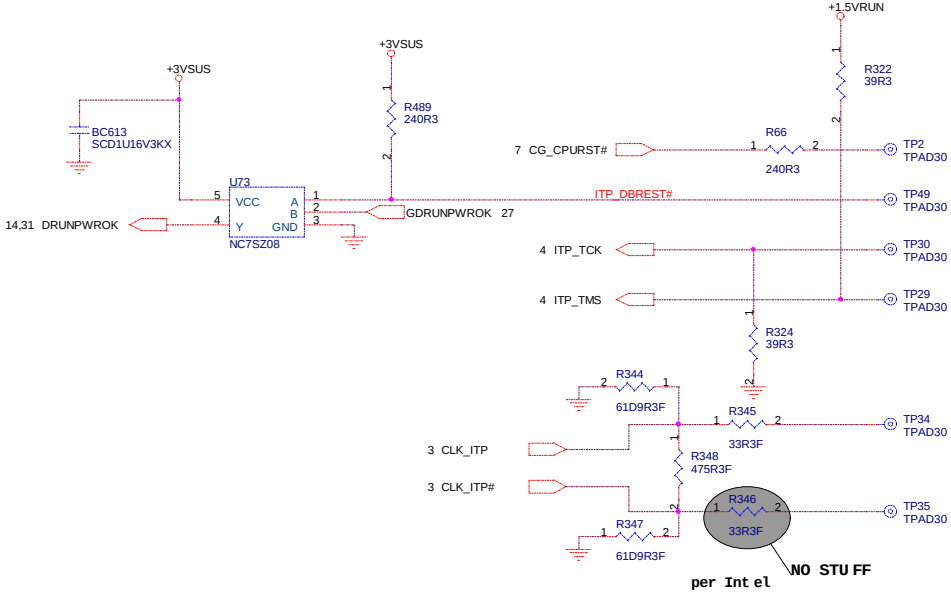
THERMAL SENSOR MAX6654

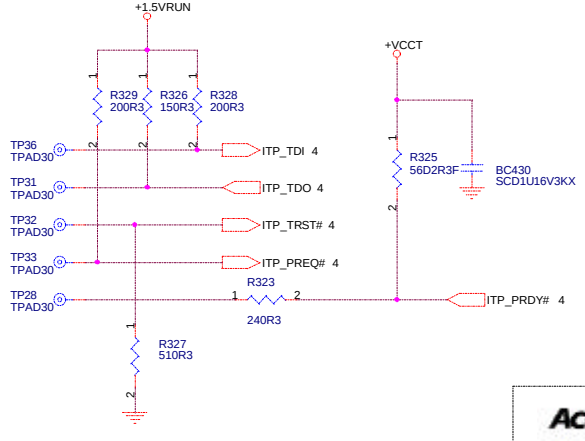


Layout note:
Routing THERMDP and THERMDN at same layer.

CPU FAN



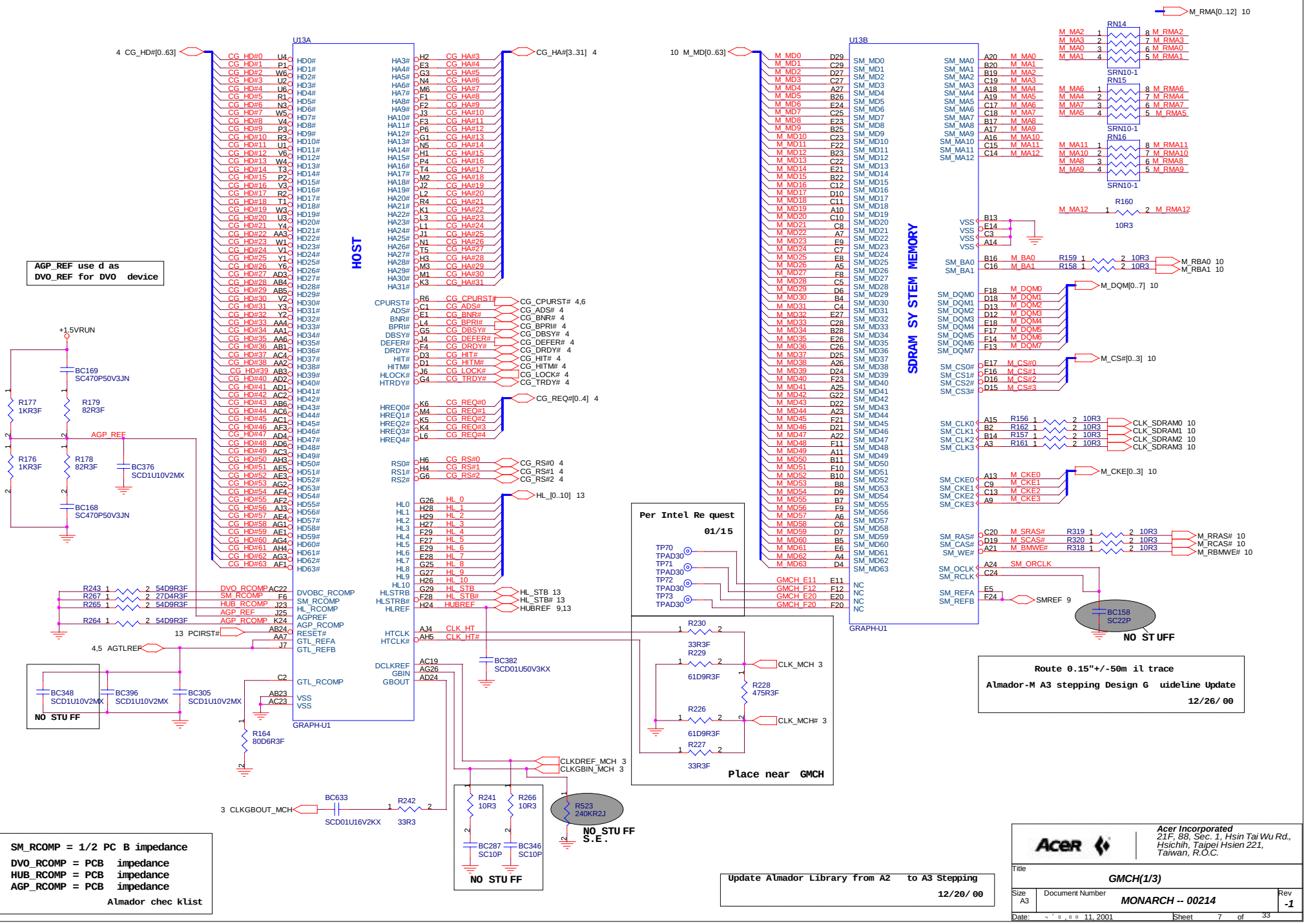




PULLUP RESISTOR<1"FROM ITP PORT PINS

Acer Incorporated
21F, 88, Sec. 1, Hsin Tai Wu Rd.,
Hsichih, Taipei Hsien 221,
Taiwan, R.O.C.

Title	MAX1617A, FAN CONTROL & ITP	
Size A3	Document Number MONARCH -- 00214	Rev -1
Date: 11, 2001	Sheet 6 of 33	


U13A
HOST
GRAPH-U1
U13B
SDRAM SY STEM MEMORY
GRAPH-U1
AGP_REF use d as
DVO_REF for DVO device
Per Intel Re quest
01/15
Place near GMCH
NO STU FF
NO STU FF
NO_STU FF
S.E.
NO ST UFF
Route 0.15"+/-50m il trace
Almador-M A3 stepping Design G uideline Update
12/26/ 00
SM_RCOMP = 1/2 PC B impedance
DVO_RCOMP = PCB impedance
HUB_RCOMP = PCB impedance
AGP_RCOMP = PCB impedance
Almador chec klist
Update Almador Library from A2 to A3 Stepping
12/20/ 00
Acer Incorporated
21F, 88, Sec. 1, Hsin Tai Wu Rd.,
Hsichih, Taipei Hsien 221,
Taiwan, R.O.C.
Title
GMCH(1/3)
Size A3
Document Number
MONARCH -- 00214
Rev -1
Date: 11, 2001
Sheet 7 of 33

AGP_P AR	Pull-up 8.2K to 1.5VRUN	AGP device at tached
	Pull-down 2.2K to GND	DVO device at tached

Strapping Option for SW detection of AGP or DVO device

ALM checklist ver.0.5 P.32 said this is require d. ???
and KODIAK 0.7b P14 als o has this.

DVOA_D5 Int. P /D	0 = DESK TOP 1 = MOB ILE	Pull-up 2.2K to V1.5S
DVOA_D6 Int. P /D	0 = Dual ended term. 1 = Single ende d term.	Pull-up 2.2K to V1.5S
DVOA_D0 Int. P /U	0 = 200 MHz 1 = 133 MHz	Pull-down 2.2K to GND
DVOA_D1 Int. P /U	0 : IOQD = 1 1 : IOQD = 8	Pull-down 2.2K to GND
DVOA_D7 Int. P /D	0 : Normal mode 1 : Invoking the XOR Cha in test mode	
DVOA_D8 Int. P /D	0 : Normal mode 1 : Tri-stating all GMCH output s when ICH3-M is in XOR Chain mode.	

Per Intel GMCH EDS Rev0.7 12/22/2K

U13D

U13C

AGP, GPIO, DISPLAY, LOCAL MEMORY

GRAPH-U1

+1.5VRUN R37 100KR3

9/13 per I ntel

R61 255R3F close to Ball

DVO_D[0..11] 11

+3VRUN +1.5VRUN R239 10KR3 R240 10KR3 R60 100KR3

R244 15R3F DVO_STALL 11

R245 75R3F 9/13 per Intel

DVO port of G MCH is +1.5V Power plane

DVO port of VCH is +1.8V Power plane

RN21 SRN8K2-1 RN22 SRN8K2-1

R521 8K2R3 No Stu ff P.T.

R99 330R3 P.T.

R95 2K2R3

R122 10KR3

R133 2K2R3 R41 10KR3 R40 10KR3

+1.8VRUN R247 576R3F R246 2KR3F

+1.5VRUN DVO_D5 R236 2K2R3 DVO_D6 R237 2K2R3 NO STU FF DVO_D0 R234 2K2R3 DVO_D7 R511 2K2R3 DVO_D1 R235 2K2R3 DVO_D8 R512 2K2R3 NO STU FF

DVO_INT R#	Pull-up 100K to 1.5VRUN	Pull-up/down r equired if DVOA not implement ed.
DVO_FIE LD	Pull-down 100K to GND	
DVO_CLK IN	Pull-up 100K to 1.5VRUN	

DDC1CL K DDC1DA T	Pull-up 2.2K to +5VRUN	Non-5V tole rant, Q-Switch requi red for 5V supp ort
DDC2CL K DDC2DA T	Pull-up 10K to +5VRUN	
I2CCL K I2CDAT A	Pull-up 10K to +3VRUN	

+3VRUN OSC1 NC GND VDD OUT OSC-32.768KHZ-1 R130 732R3F R129 604R3F

KODIAK 0.7b P.9 3 3MHz OSC
9/13 change to 32K OSC per Intel

Pull-up req uired for ext. AG P GFX and int. DV O GFX

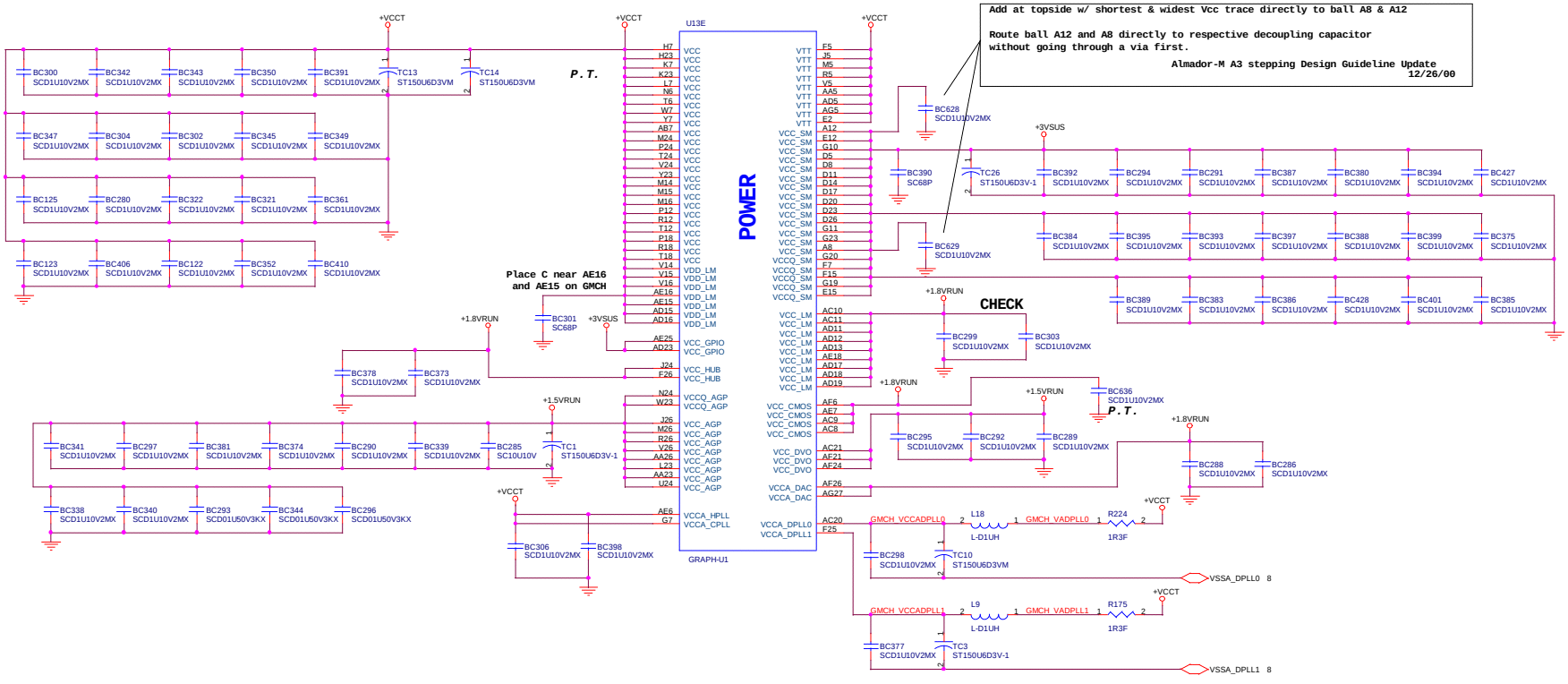
Connect pin AE20, G24(VSSA_ DPLL[0,1]) to the respective decoupling caps of pin AC20, F25(VCCA_DP LL[0,1])

Acer Incorporated
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: GMCH(2/3)

Size: A3 | Document Number: MONARCH -- 00214 | Rev: -1

Date: 11, 2001 | Sheet 8 of 33

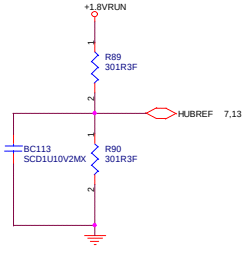


Decouping Recommendati on

				Monarch	Kodiak Ver. 0.5
V1.2S_GMCH	Decoupling Caps	0.1uF * 20	Distribute as close as possible to GMCH-M processor Quadrant	0.1uF * 20 100uF / 10V * 2 68pF * 1	1uF * 20
	Bulk Caps				150uF / 4V * 5 + 1 * NS
V1.2S_GMCHCORE	Decoupling Caps	68pF * 1	Close to VDD_LM, near pins AE15 and AE16 on Almador		68pF * 1
		0.1uF * 40			1uF * 40
	Bulk Caps				150uF / 4V * 10 + 1 * NS
V1.5S_GMCH	Decoupling Caps	0.1uF * 9 82pF * 4	Distribute as close as possible to GMCH-M AGP/DVO Quadrant	0.1uF * 8 0.01uF * 3 10uF / 10V * 1	0.1uF * 9 82pF * 4
	Bulk Caps			100uF / 10V * 1	22uF / 20V * 1
V1.8S_GMCH	Decoupling Caps	0.1uF * 4 + 4 82pF * 2	Distribute as close as possible to GMCH-M Local Memory Quadrant Additional 4* 0.1uF shall be distributed as close as possible to VCCPCMOS_LM	0.1uF * 2	0.1uF * 4 + 2 82pF * 2 22uF / 20V * 2
	Bulk Caps				68uF / 10V * 5
V3_GMCH	Decoupling Caps	0.1uF * 12 + 2 82pF * 4	Distribute as close as possible to GMCH-M System Memory Quadrant Additional 4* 0.1uF shall be distributed as close as possible to IO Quadrant	0.1uF * 20 100uF / 10V * 1	0.1uF * 12 + 2 82pF * 4 22uF / 20V * 2
	Bulk Caps				

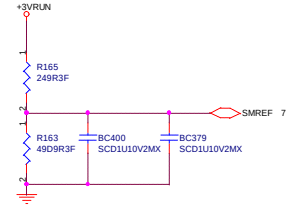
Almador-M Checklist Ver. 0.5 8/28

HUB INTERFACE RE F 1/2*1.8V



Layout Note:
Place divider pair in middle of bus.
Place capacitors near GMCH.

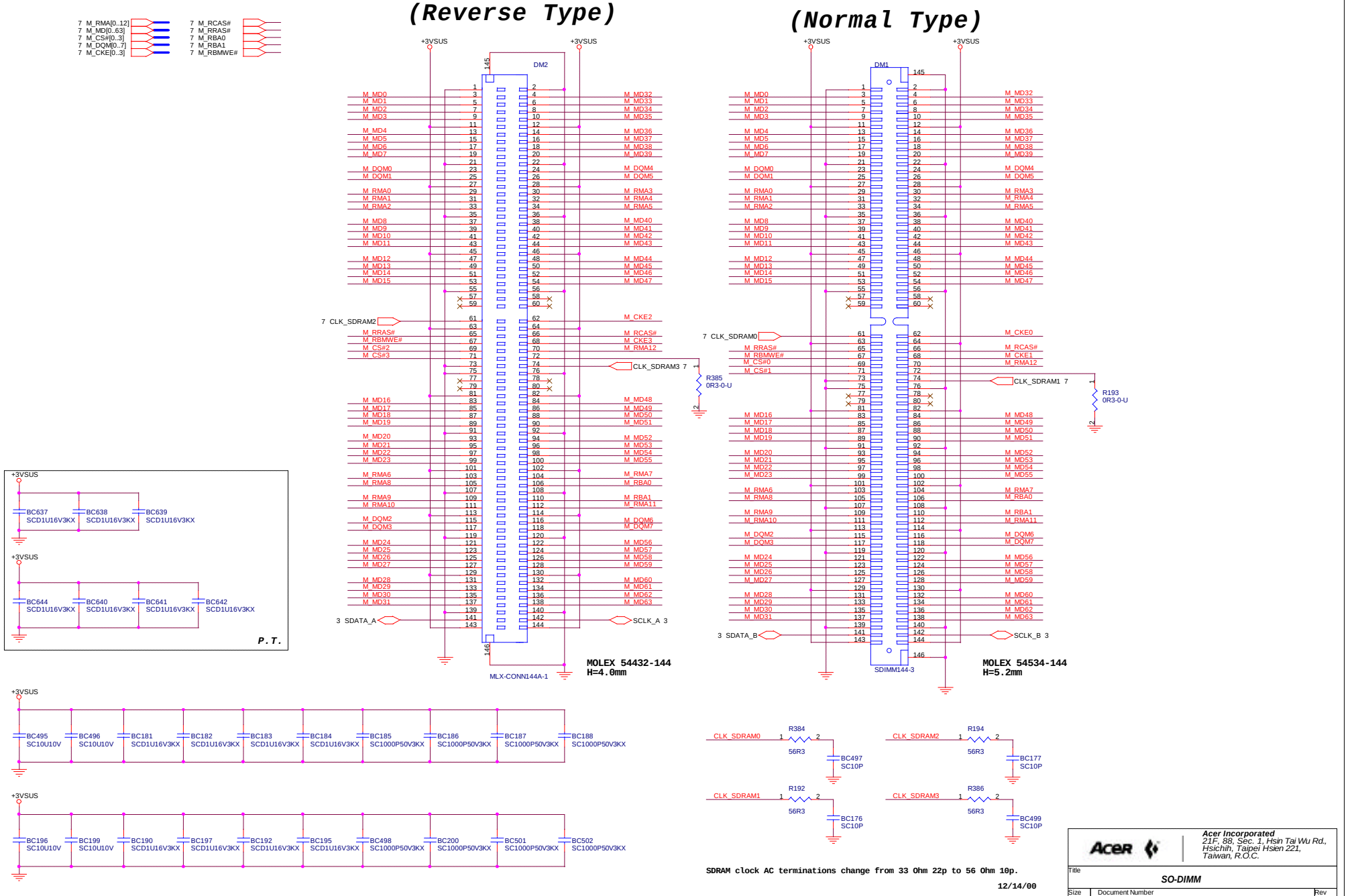
SYSTEM MEMOR Y REF 0.55V

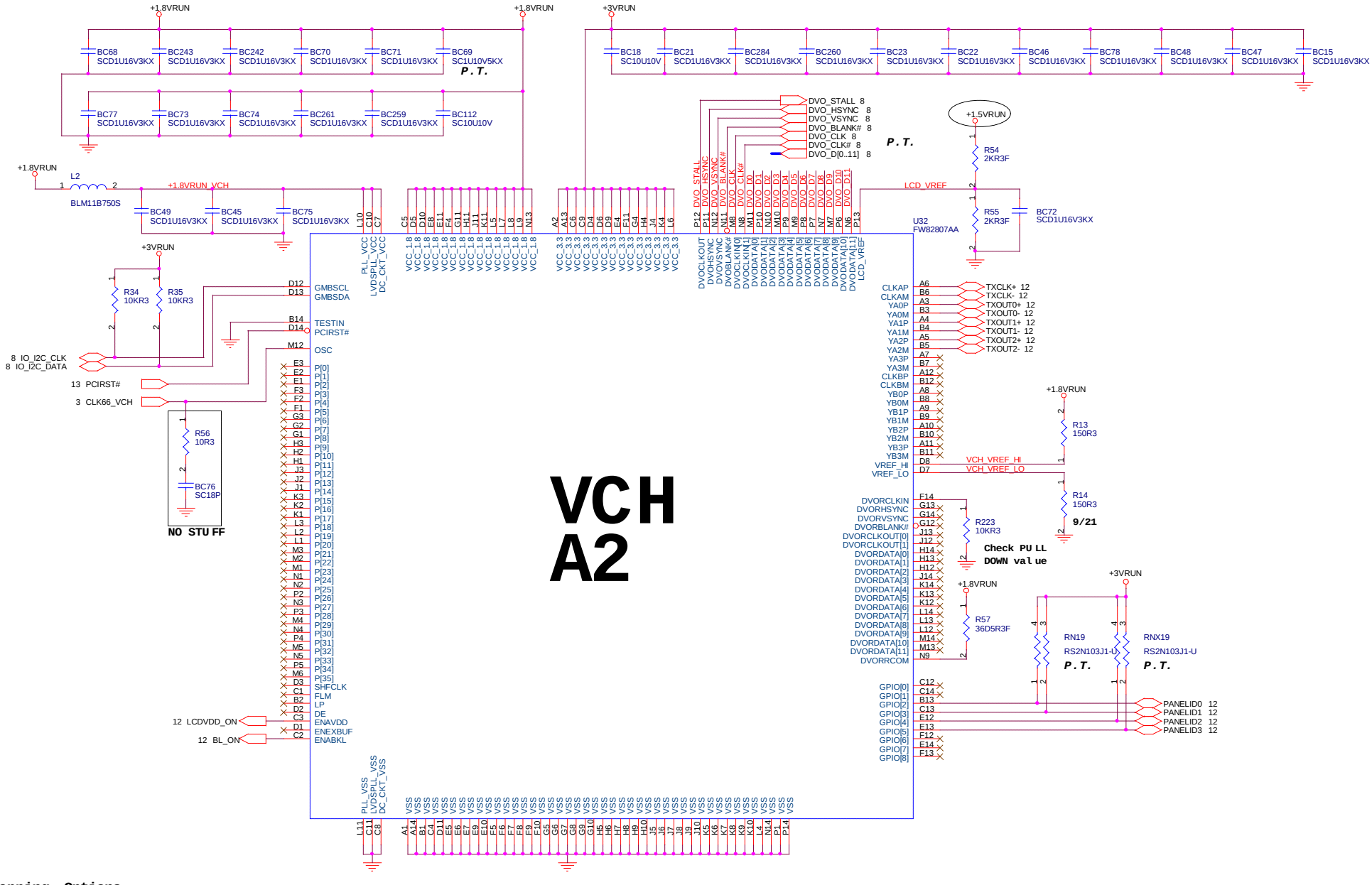


Place capacitor near GMCH ball E5 & F24.

Acer Incorporated
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: GMCH(3/3)
Size: Custom | Document Number: MONARCH -- 00214 | Rev: -1
Date: 11, 2001 | Sheet 9 of 33


(Reverse Type)
(Normal Type)
7 M_RMA[0..12]
7 M_MD[0..63]
7 M_CS#[0..3]
7 M_DQM[0..7]
7 M_CKE[0..3]
7 M_RCAS#
7 M_RRAS#
7 M_RBA0
7 M_RBA1
7 M_RBMWE#
+3VSUS
DM2
DM1
7 CLK_SDRAM2
7 CLK_SDRAM0
CLK_SDRAM3 7
CLK_SDRAM1 7
R385 0R3-0-U
R193 0R3-0-U
3 SDATA_A
SCLK_A 3
3 SDATA_B
SCLK_B 3
MLX-CONN144A-1
SDIMM144-3
MOLEX 54432-144
H=4.0mm
MOLEX 54534-144
H=5.2mm
BC637 SCD1U16V3KX
BC638 SCD1U16V3KX
BC639 SCD1U16V3KX
BC644 SCD1U16V3KX
BC640 SCD1U16V3KX
BC641 SCD1U16V3KX
BC642 SCD1U16V3KX
P.T.
BC495 SC10U10V
BC496 SC10U10V
BC181 SCD1U16V3KX
BC182 SCD1U16V3KX
BC183 SCD1U16V3KX
BC184 SCD1U16V3KX
BC185 SC1000P50V3KX
BC186 SC1000P50V3KX
BC187 SC1000P50V3KX
BC188 SC1000P50V3KX
BC196 SC10U10V
BC199 SC10U10V
BC190 SCD1U16V3KX
BC197 SCD1U16V3KX
BC192 SCD1U16V3KX
BC195 SCD1U16V3KX
BC498 SC1000P50V3KX
BC200 SC1000P50V3KX
BC501 SC1000P50V3KX
BC502 SC1000P50V3KX
CLK_SDRAM0
CLK_SDRAM1
CLK_SDRAM2
CLK_SDRAM3
R384 56R3
R192 56R3
R194 56R3
R386 56R3
BC497 SC10P
BC176 SC10P
BC177 SC10P
BC499 SC10P
SDRAM clock AC terminations change from 33 Ohm 22p to 56 Ohm 10p.
12/14/00
Acer Incorporated
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
SO-DIMM
Size Custom
Document Number MONARCH -- 00214
Rev -1
Date: 11, 2001
Sheet 10 of 33



Strapping Options

GPIO[5:2]	10 - 4.7K Ohm	Can be used for panel ID select. Default state is GPI w/ int. weak pu ll down.
GPIO6	10 - 4.7K Ohm	For normal VCH operation pin has t o be read as low. Default state is GPI w/ int. w eak pull down.
GPIO[8:7]	10 - 4.7K Ohm	Used for GMBus base address selec t. Default state is GPI w/ int. weak p ull down.

Almador check ver.0.5

PANEL ID TA BLE (S.E.)

	ID0	ID1	ID2	ID3
LG	1	1	0	0
SAMSUN G	0	0	1	0
RFU				

Acer Incorporated
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: VCH

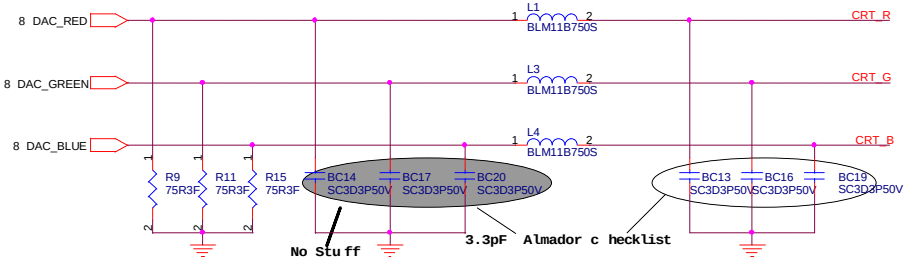
Size: A3 | Document Number: MONARCH -- 00214 | Rev: -1

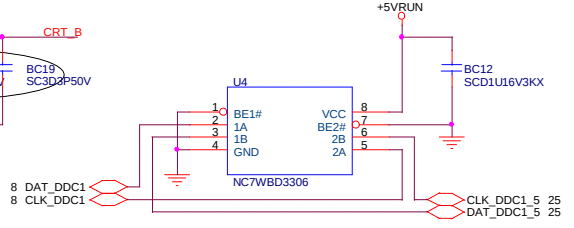
Date: 11, 2001 | Sheet 11 of 33

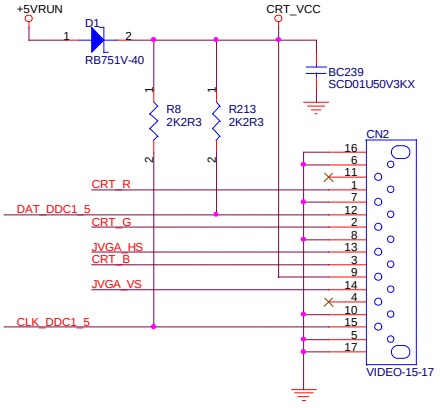
Change from VIDEO-15-7-U (21.B00 6.015) SMT type
to VIDEO-15-17 (20.20235.0 15) DIP type
01/09/' 01

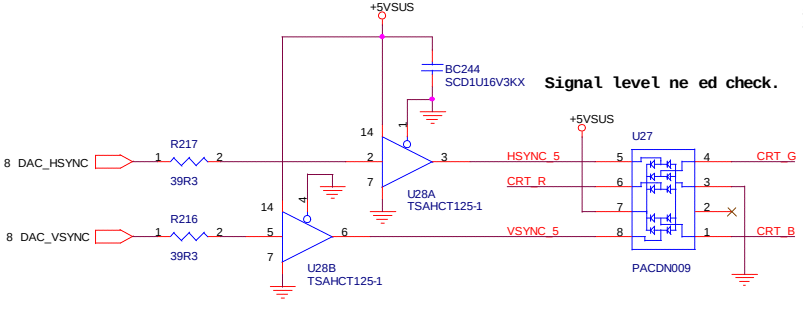
CRT

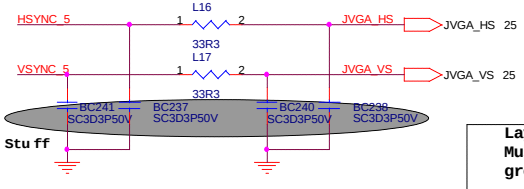
Ferrite bead impedance:
75ohm@1 00MHz

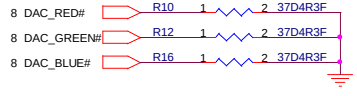








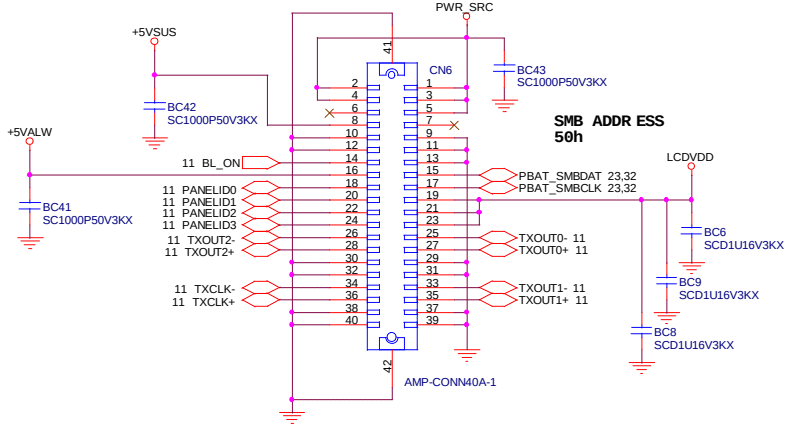


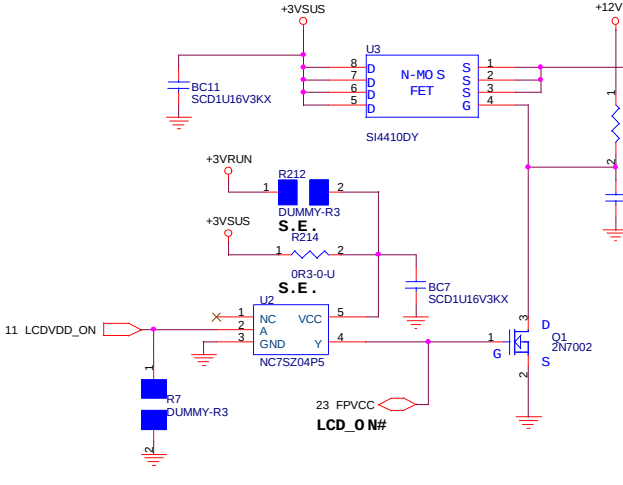


Layout N ote:
Must be a ground return pa th between this ground and the ground on t he VGA connector.

37.4_1% resistors must be pl aced after RGB pi filter ,near CRT connector.

LCD/INVERTER CONN





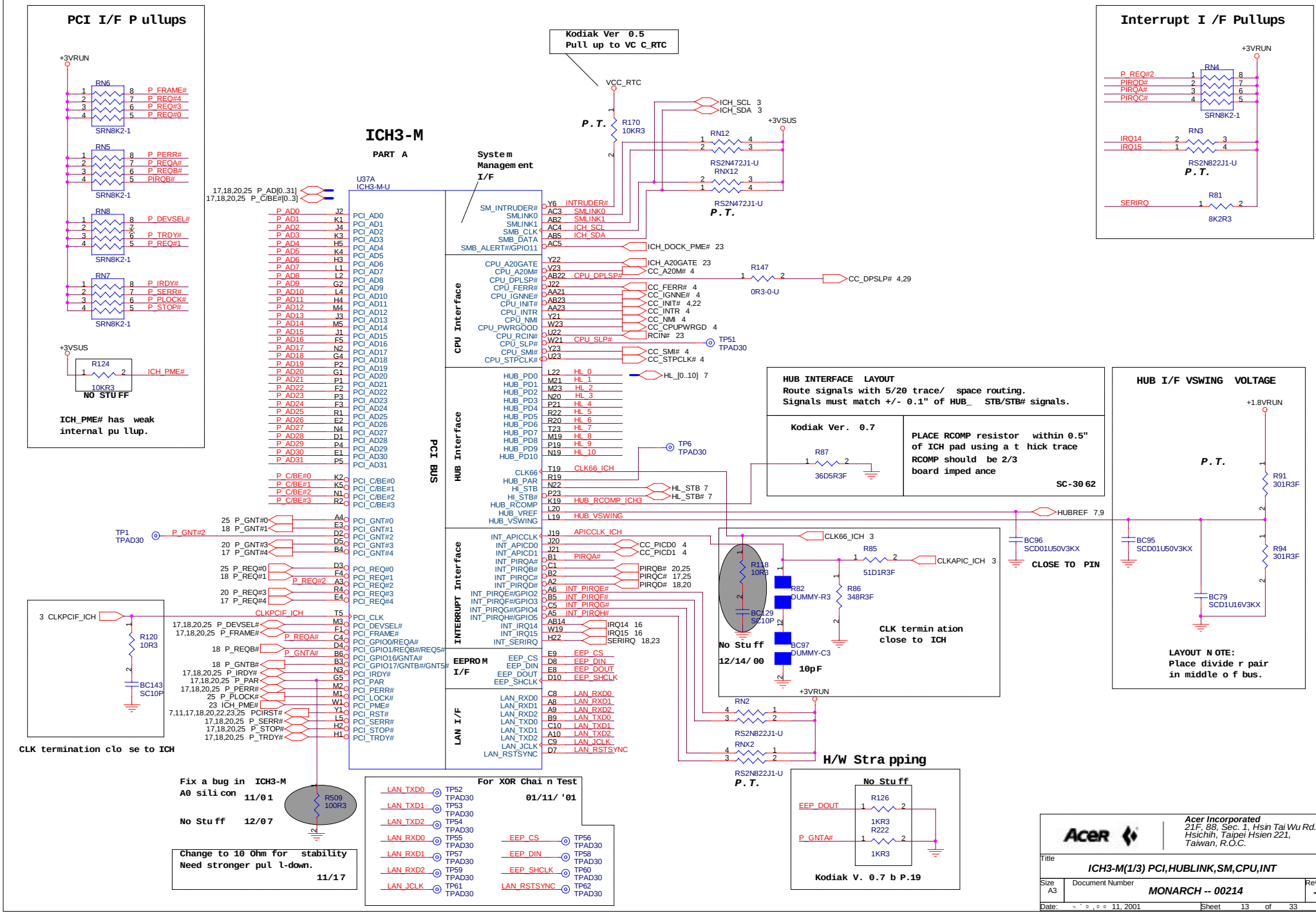
DIFFERENTIAL GND MUST LAY AROUND SIGNAL AND CAN'T USE THE SAME P ATH WITH PWR GND

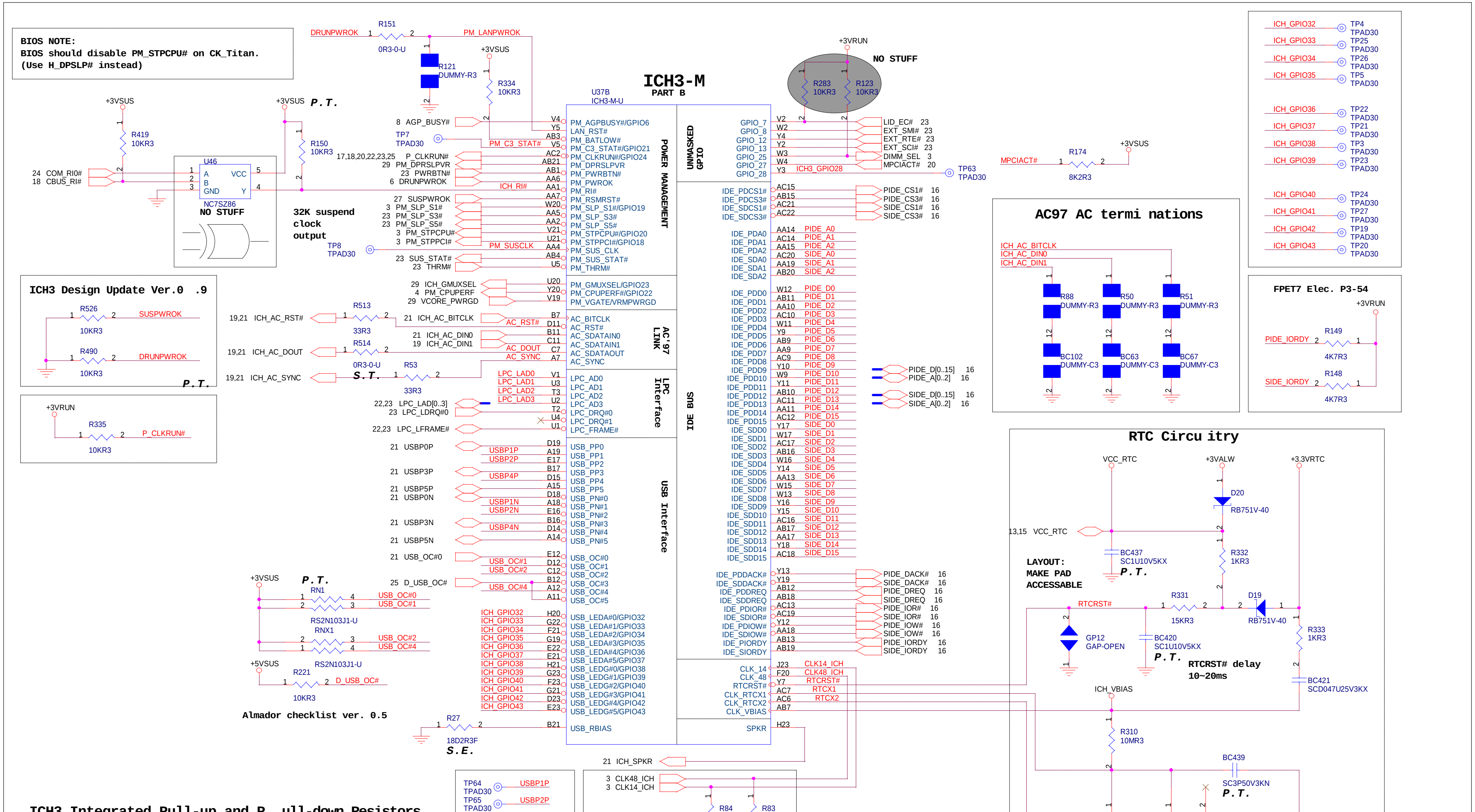
Acer Incorporated
21F, 88, Sec. 1, Hsin Tai Wu Rd.,
Hsichih, Taipei Hsien 221,
Taiwan, R.O.C.

Title: LVDS/ LCD I/F CONN

Size: A3 | Document Number: MONARCH -- 00214 | Rev: -1

Date: ¬ ´ ¤ ¸ ¤ ¤ 11, 2001 | Sheet 12 of 33


PCI I/F P ullups
+3VRUN
RN6
P_FRAME#
P_REQ#4
P_REQ#3
P_REQ#0
SRN8K2-1
RN5
P_PERR#
P_REQA#
P_REQB#
PIRQB#
SRN8K2-1
RN8
P_DEVSEL#
P_TRDY#
P_REQ#1
SRN8K2-1
RN7
P_IRDY#
P_SERR#
P_PLOCK#
P_STOP#
SRN8K2-1
+3VSUS
R124
10KR3
ICH_PME#
NO STU FF
ICH_PME# has weak internal pu llup.
Kodiak Ver 0.5
Pull up to VC C_RTC
VCC_RTC
P.T.
R170
10KR3
ICH-M
PART A
System Managem ent I/F
U37A
ICH3-M-U
17,18,20,25 P_AD[0..31]
17,18,20,25 P_C/BE#[0..3]
PCI BUS
SM_INTRUDER#
SMLINK0
SMLINK1
SMB_CLK
SMB_DATA
SMB_ALERT#/GPIO11
INTRUDER#
SMLINK0
SMLINK1
ICH_SCL
ICH_SDA
ICH_DOCK_PME# 23
ICH_SCL 3
ICH_SDA 3
+3VSUS
RN12
RS2N472J1-U
RNX12
RS2N472J1-U
P.T.
CPU Interface
CPU_A20GATE
CPU_A20M#
CPU_DPLSP#
CPU_FERR#
CPU_IGNNE#
CPU_INIT#
CPU_INTR
CPU_NMI
CPU_PWRGOOD
CPU_RCIN#
CPU_SLP#
CPU_SMI#
CPU_STPCLK#
ICH_A20GATE 23
CC_A20M# 4
CPU_DPLSP#
CC_FERR# 4
CC_IGNNE# 4
CC_INIT# 4,22
CC_INTR 4
CC_NMI 4
CC_CPUPWRGD 4
RCIN# 23
CPU_SLP#
CC_SMI# 4
CC_STPCLK# 4
R147
0R3-0-U
CC_DPLSP# 4,29
TP51
TPAD30
HUB Interface
HUB_PD0
HUB_PD1
HUB_PD2
HUB_PD3
HUB_PD4
HUB_PD5
HUB_PD6
HUB_PD7
HUB_PD8
HUB_PD9
HUB_PD10
HL_[0..10] 7
TP6
TPAD30
CLK66
HUB_PAR
HI_STB
HI_STB#
HUB_RCOMP
HUB_VREF
HUB_VSWING
HL_STB 7
HL_STB# 7
HUB_RCOMP_ICH3
HUB INTERFACE LAYOUT
Route signals with 5/20 trace/ space routing.
Signals must match +/- 0.1" of HUB_ STB/STB# signals.
Kodiak Ver. 0.7
R87
36D5R3F
PLACE RCOMP resistor within 0.5" of ICH pad using a t hick trace
RCOMP should be 2/3 board imped ance
SC-30 62
HUBREF 7,9
BC96
SCD01U50V3KX
CLOSE TO PIN
HUB I/F VSWING VOLTAGE
+1.8VRUN
P.T.
R91
301R3F
R94
301R3F
BC95
SCD01U50V3KX
BC79
SCD1U16V3KX
LAYOUT N OTE:
Place divide r pair in middle o f bus.
INTERRUPT Interface
INT_APICCLK
INT_APICD0
INT_APICD1
INT_PIRQA#
INT_PIRQB#
INT_PIRQC#
INT_PIRQD#
INT_PIRQE#/GPIO2
INT_PIRQF#/GPIO3
INT_PIRQG#/GPIO4
INT_PIRQH#/GPIO5
INT_IRQ14
INT_IRQ15
INT_SERIRQ
APICCLK_ICH
CC_PICD0 4
CC_PICD1 4
PIRQA#
PIRQB# 20,25
PIRQC# 17,25
PIRQD# 18,20
INT_PIRQE#
INT_PIRQF#
INT_PIRQG#
INT_PIRQH#
IRQ14 16
IRQ15 16
SERIRQ 18,23
CLK66_ICH 3
R118
10R3
R85
51D1R3F
CLKAPIC_ICH 3
R82
DUMMY-R3
R86
348R3F
BC129
SC10P
BC97
DUMMY-C3
10pF
No Stu ff
12/14/ 00
CLK termin ation close to ICH
+3VRUN
RN2
RS2N822J1-U
RNX2
RS2N822J1-U
P.T.
EEPROM I/F
EEP_CS
EEP_DIN
EEP_DOUT
EEP_SHCLK
LAN I/F
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2
LAN_JCLK
LAN_RSTSYNC
H/W Stra pping
No Stu ff
R126
1KR3
R222
1KR3
EEP_DOUT
P_GNTA#
Kodiak V. 0.7 b P.19
Interrupt I /F Pullups
+3VRUN
RN4
P_REQ#2
PIRQD#
PIRQA#
PIRQC#
SRN8K2-1
RN3
IRQ14
IRQ15
RS2N822J1-U
P.T.
R81
SERIRQ
8K2R3
TP1
TPAD30
P_GNT#2
25 P_GNT#0
18 P_GNT#1
20 P_GNT#3
17 P_GNT#4
25 P_REQ#0
18 P_REQ#1
20 P_REQ#3
17 P_REQ#4
3 CLKPCIF_ICH
R120
10R3
BC143
SC10P
CLK termination clo se to ICH
Fix a bug in ICH3-M A0 sili con 11/01
No Stu ff 12/07
R509
100R3
Change to 10 Ohm for stability
Need stronger pul l-down.
11/17
For XOR Chai n Test
01/11/ '01
LAN_TXD0
LAN_TXD1
LAN_TXD2
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_JCLK
TP52
TP53
TP54
TP55
TP57
TP59
TP61
TPAD30
EEP_CS
EEP_DIN
EEP_SHCLK
LAN_RSTSYNC
TP56
TP58
TP60
TP62
Acer Incorporated
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH3-M(1/3) PCI,HUBLINK,SM,CPU,INT
Size A3
Document Number MONARCH -- 00214
Rev -1
Date: 11, 2001
Sheet 13 of 33



ICH3 Integrated Pull-up and P ull-down Resistors

EE_DIN , EE_DOUT , LDRQ[1:0] , PME# GNT[B:A]#/GNT[5]#/GPIO[17:16] , LAD[3:0]#/FWH[3:0]# , PWRBTN#	ICH3 internal 24K pull-ups
LAN_RXD[2:0]	ICH3 internal 9K pull-ups
AC_BITCLK, AC_SDIN[0], AC_SDOUT, AC_SDIN[1]/GPIO[9], AC_SYNC,	ICH3 internal 20K pull-downs
SPKR	ICH3 internal 24K pull-downs
PDD[7]/SDD[7], PDDREQ / SDDREQ	ICH3 internal 5.9K pull-downs
DPRSLPVR	ICH3 internal TBD K pull-downs

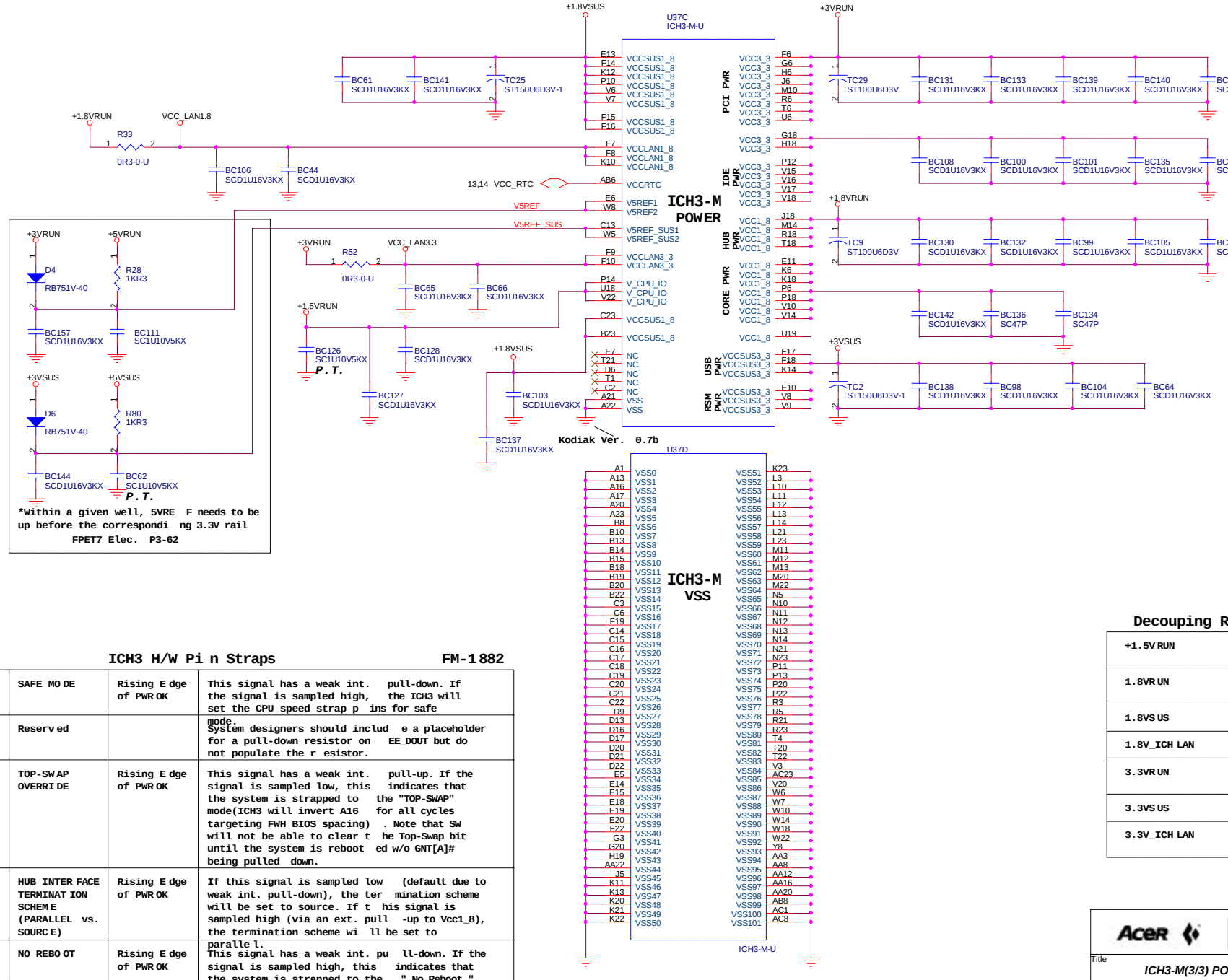
FM-1882 P4-1, 2

Acer Incorporated
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH3-M(2/3) PM,USB,AC'97,LPC,IDE,RTC

Size: Custom | Document Number: MONARCH -- 00214 | Rev: -1

Date: 11, 2001 | Sheet 14 of 33



ICH3 H/W Pi n Straps FM-1882

AC_SDO UT	SAFE MO DE	Rising E dge of PWR OK	This signal has a weak int. pull-down. If the signal is sampled high, the ICH3 will set the CPU speed strap p ins for safe mode.
EE_DOU T	Reserv ed		System designers should includ e a placeholder for a pull-down resistor on EE_DOUT but do not populate the r esistor.
GNT[A] #	TOP-SW AP OVERRI DE	Rising E dge of PWR OK	This signal has a weak int. pull-up. If the signal is sampled low, this indicates that the system is strapped to the "TOP-SWAP" mode(ICH3 will invert A16 for all cycles targeting FWH BIOS spacing) . Note that SW will not be able to clear t he Top-Swap bit until the system is reboot ed w/o GNT[A]# being pulled down.
DPRSLP VR	HUB INTER FACE TERMINAT ION SCHEM E (PARALLEL vs. SOURC E)	Rising E dge of PWR OK	If this signal is sampled low (default due to weak int. pull-down), the ter mination scheme will be set to source. If t his signal is sampled high (via an ext. pull -up to Vcc1_8), the termination scheme wi ll be set to paralle l.
SPKR	NO REBO OT	Rising E dge of PWR OK	This signal has a weak int. pu ll-down. If the signal is sampled high, this indicates that the system is strapped to the " No Reboot " mode (ICH3 will disable the T XO Timer system reboot feat ure).

Decouping Rec ommendation

+1.5V RUN	0.1uF * 2 1uF / 16V * 1
1.8VR UN	0.1uF * 5 47pF * 2
1.8VS US	0.1uF * 3
1.8V_ICH LAN	0.1uF * 2
3.3VR UN	0.1uF * 13 47pF * 5
3.3VS US	0.1uF * 8
3.3V_ICH LAN	0.1uF * 2 47pF * 1

From Kris 8/10

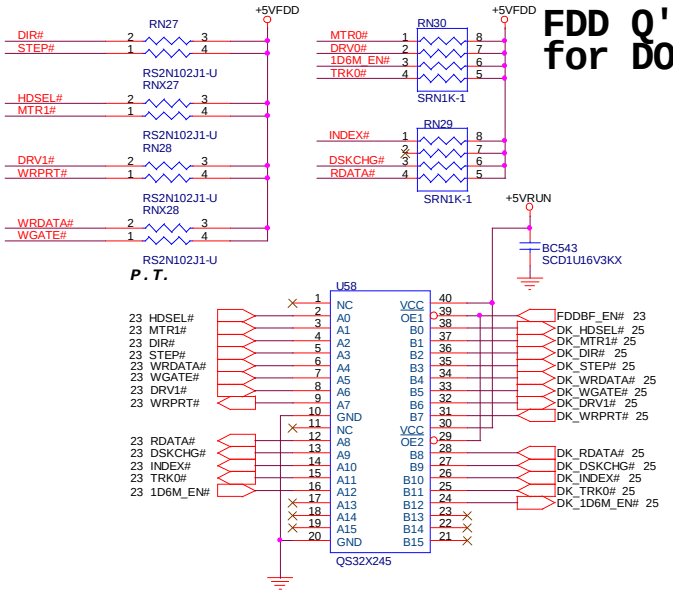
Acer Incorporated
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

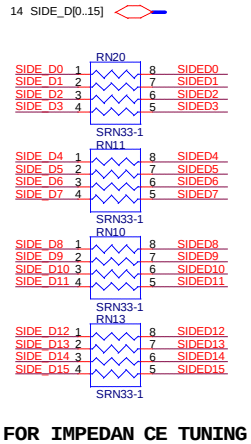
Title: ICH3-M(3/3) POWER,VSS,BYPASS CAPS

Size: A3 | Document Number: MONARCH -- 00214 | Rev: -1

Date: 11, 2001 | Sheet 15 of 33

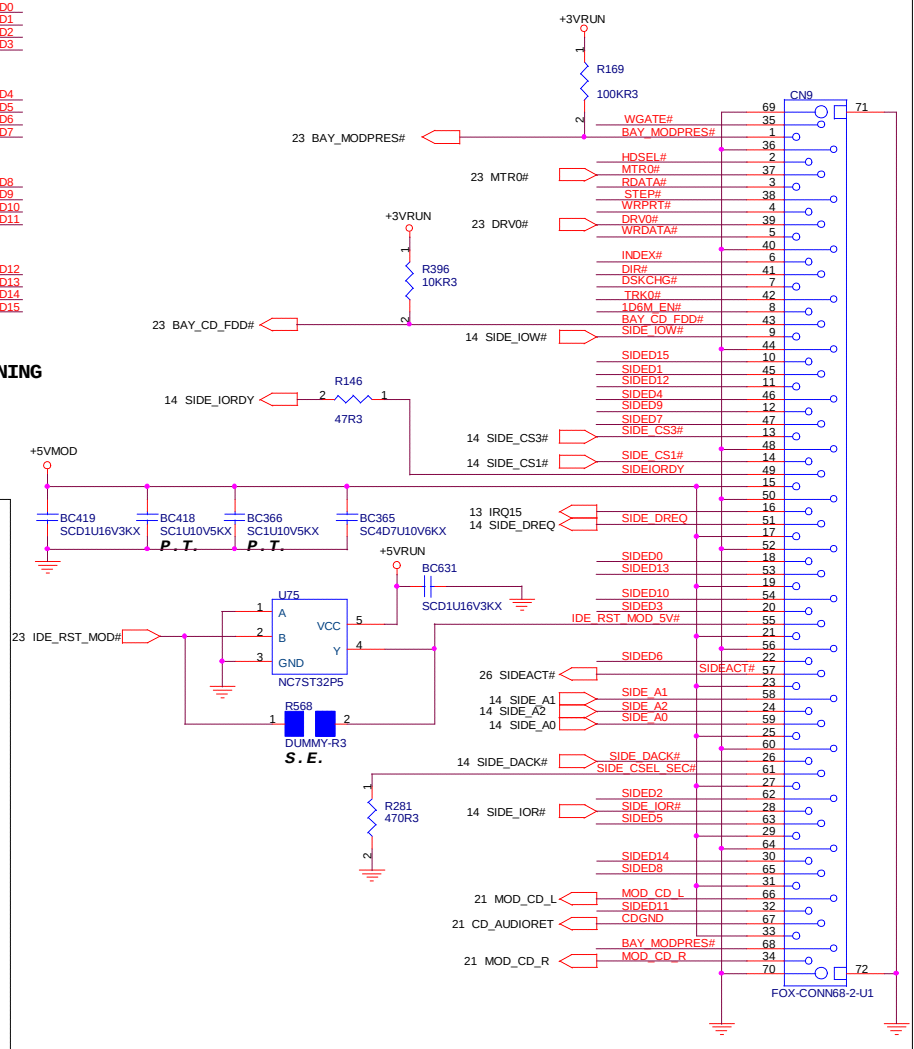
FDD Q'SW for DOCK



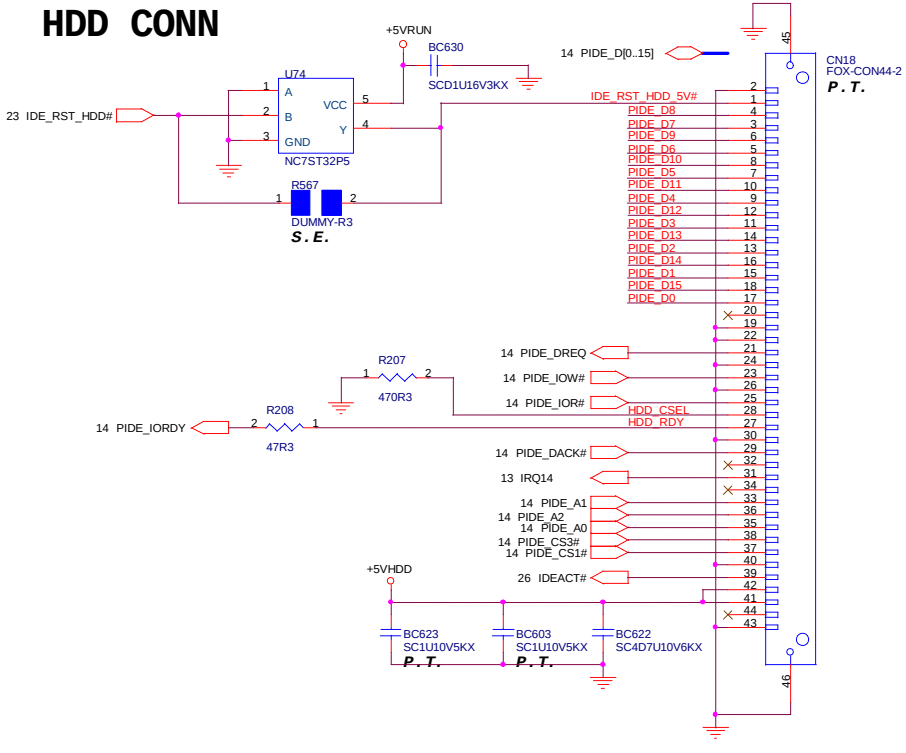


FOR IMPEDAN CE TUNING

Ext. MEDIA BAY CONN



HDD CONN

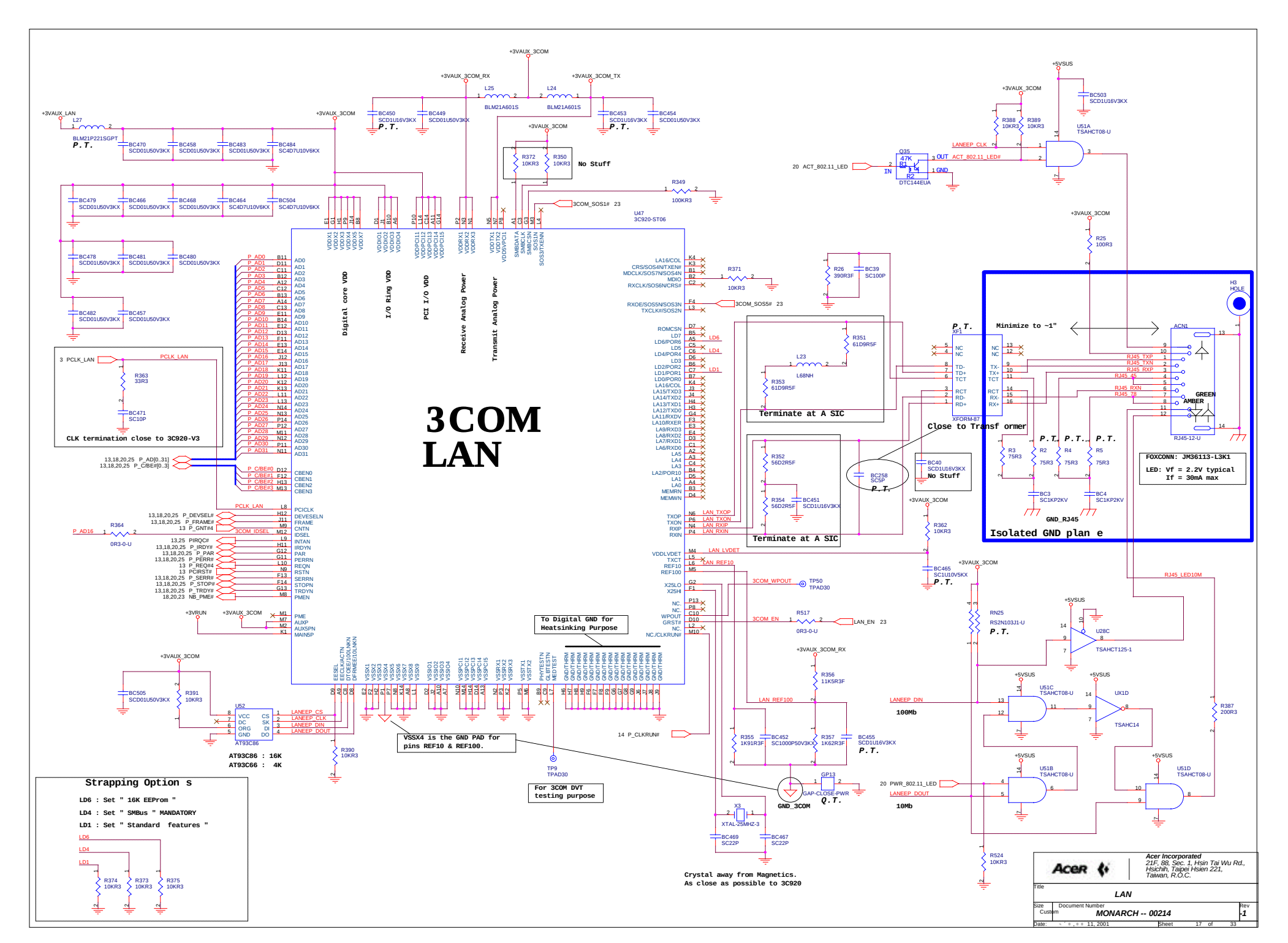


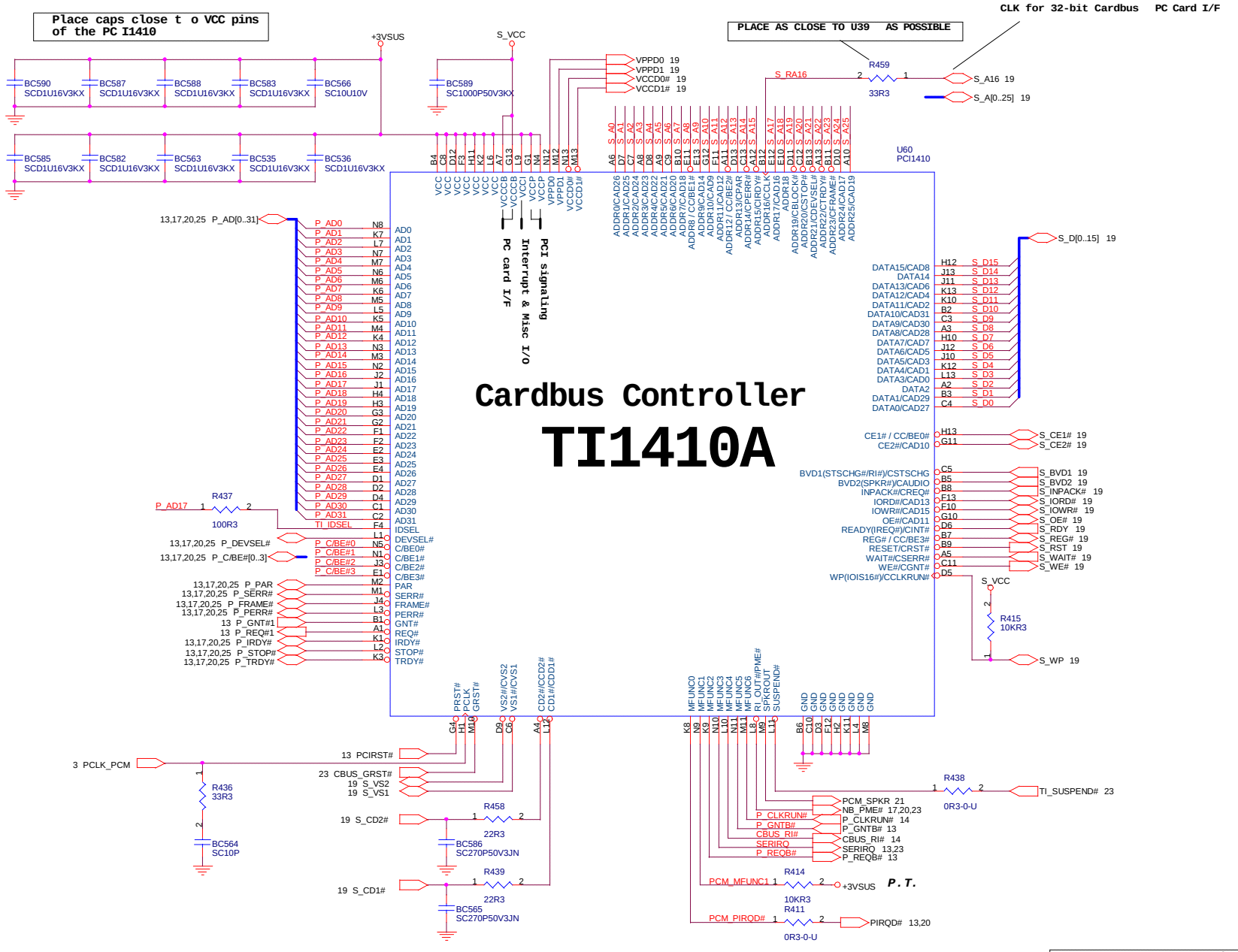
Acer Incorporated
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: ***HDD, MEDIA BAY CONN, FDD Q'SW***

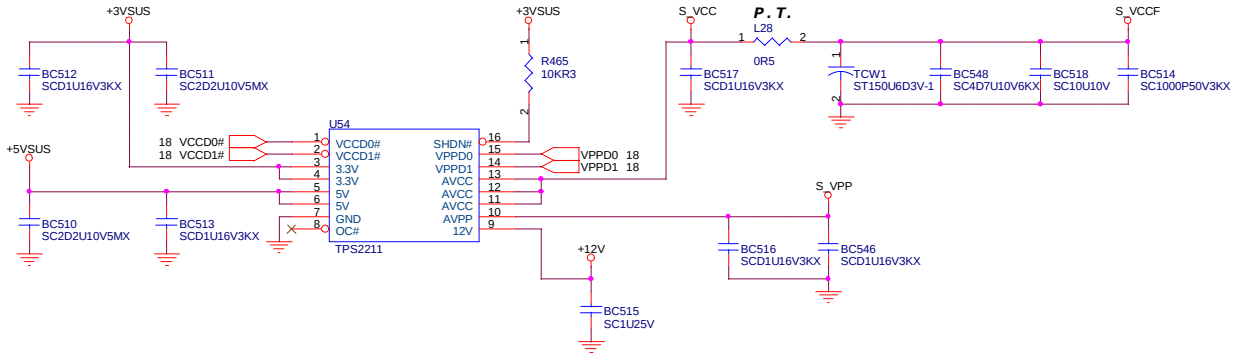
Size: A3 | Document Number: ***MONARCH -- 00214*** | Rev: ***-1***

Date: 11, 2001 | Sheet 16 of 33

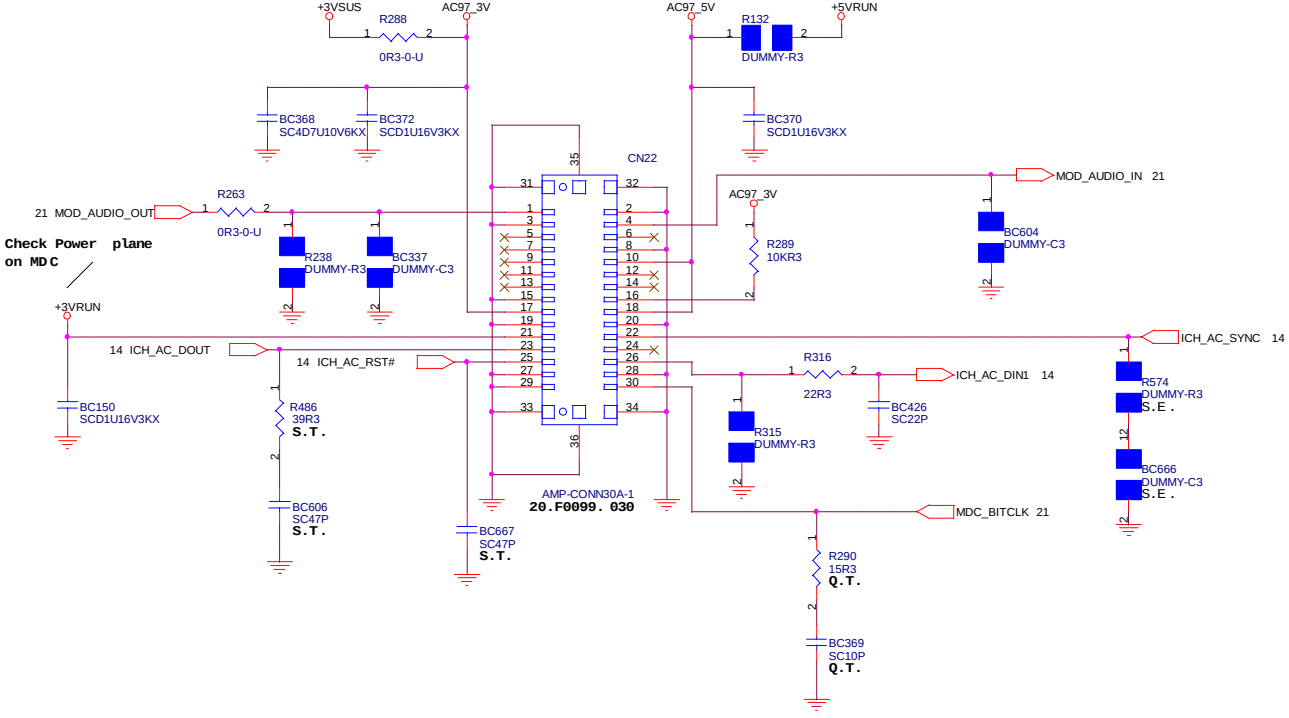

3COM LAN
Digital core VDD
I/O Ring VDD
PCI I/O VDD
Receive Analog Power
Transmit Analog Power
U47 3C920-ST06
CLK termination close to 3C920-V3
Terminate at A SIC
Terminate at A SIC
Close to Transf ormer
Minimize to ~1"
Isolated GND plan e
FOXCONN: JM36113-L3K1
LED: Vf = 2.2V typical
If = 30mA max
To Digital GND for Heatsinking Purpose
VSSX4 is the GND PAD for pins REF10 & REF100.
For 3COM DVT testing purpose
Crystal away from Magnetics. As close as possible to 3C920
AT93C86 : 16K
AT93C66 : 4K
100Mb
10Mb
No Stuff
Strapping Option s
LD6 : Set " 16K EEProm "
LD4 : Set " SMBus " MANDATORY
LD1 : Set " Standard features "
Acer Incorporated
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
LAN
MONARCH -- 00214
Date: 11, 2001
Sheet 17 of 33

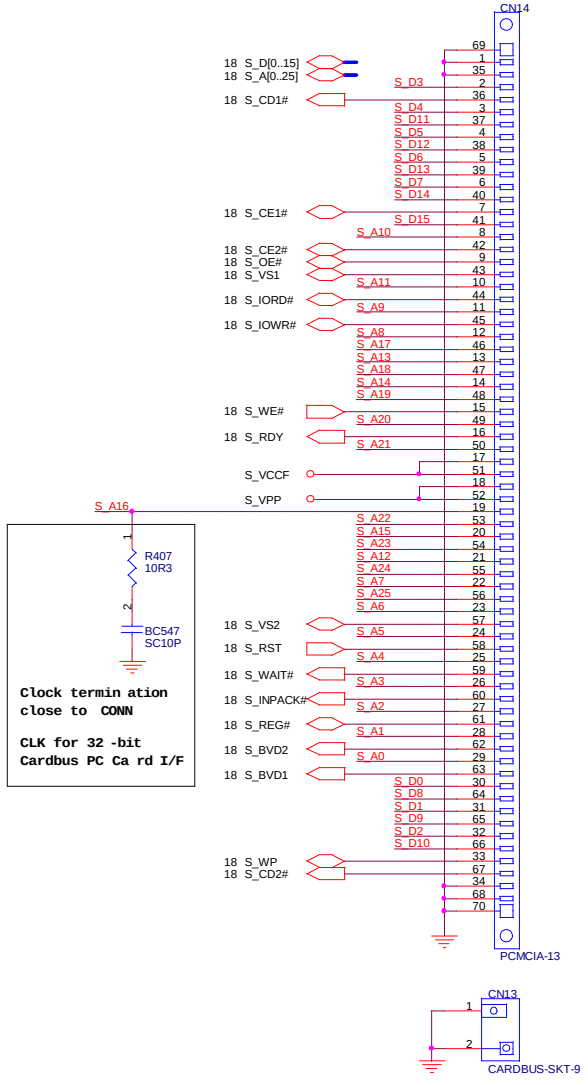


Acer	Acer Incorporated 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	CARBUS CONTROLLER TI1410
Size A3	Document Number MONARCH -- 00214 Rev -1
Date: 11, 2001	Sheet 18 of 33



Modem Connector





Acer Incorporated
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

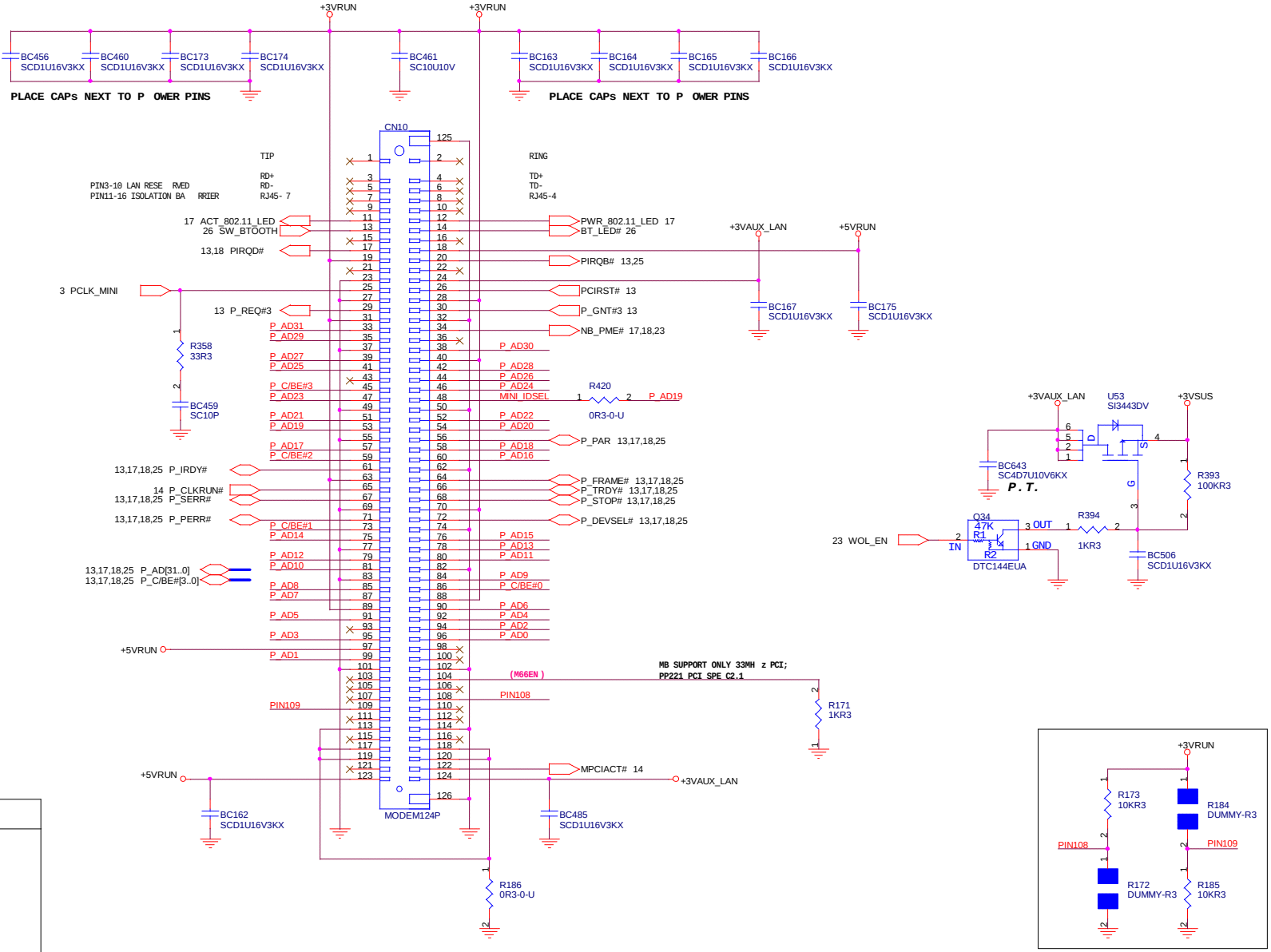
Title: ***CARBUS CONNECTOR & POWER SWITCH***

Size	Document Number	Rev
A3	***MONARCH -- 00214***	***-1***

Date: 11, 2001 Sheet 19 of 33

MINIPCI SLOT

Support 802.11 or 802.11+Bluetooth Combo Module ONLY



MINIPCI SPEC.

Pin#	Signal	Pin#	Signal
101	GND	102	GND
103	AC_SYNC	104	M66EN
105	AC_SDATA_INA	106	AC_SDATA_OUT
107	AC_BIT_CLK	108	AC_SDATA_INB
109	AC_PRIMARY#	110	AC_RESET#
111	MOD_AUDIO_MON	112	RESERVED
113	AUDIO_GND	114	GND
115	SYS_AUDIO_OUT	116	SYS_AUDIO_IN
117	SYS_AUDIO_OUT_GND	118	SYS_AUDIO_IN_GND
119	AUDIO_GND	120	AUDIO_GND
121		122	MPCIACT#
123	VCC5A	124	3.3VAUX

POWER REQUIREMENT TOTAL = 2W
+5VRUN = 1000 mA
+3VAUX = 375 mAMPMAX

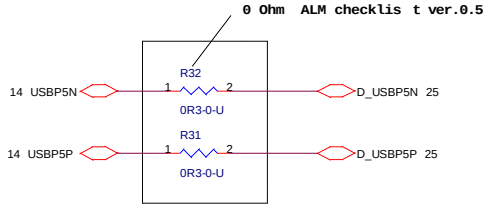
Acer Incorporated
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: ***MINIPCI CONN***

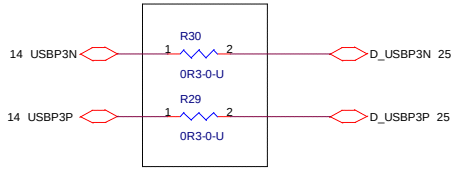
Size: A3 | Document Number: ***MONARCH -- 00214*** | Rev: ***-1***

Date: 11, 2001 | Sheet 20 of 33

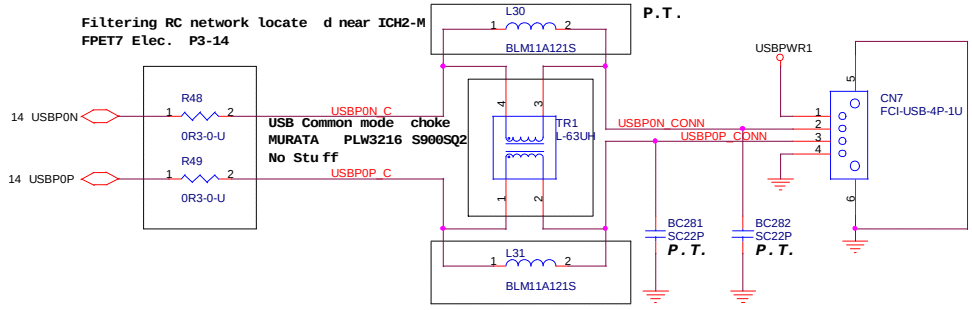
USB

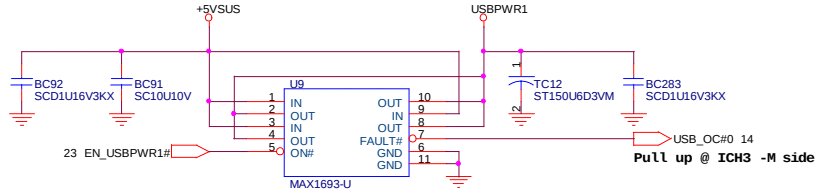


15 Ohm Serie R and 15K Ohm Pull-down R had been integrated i nto ICH3-M

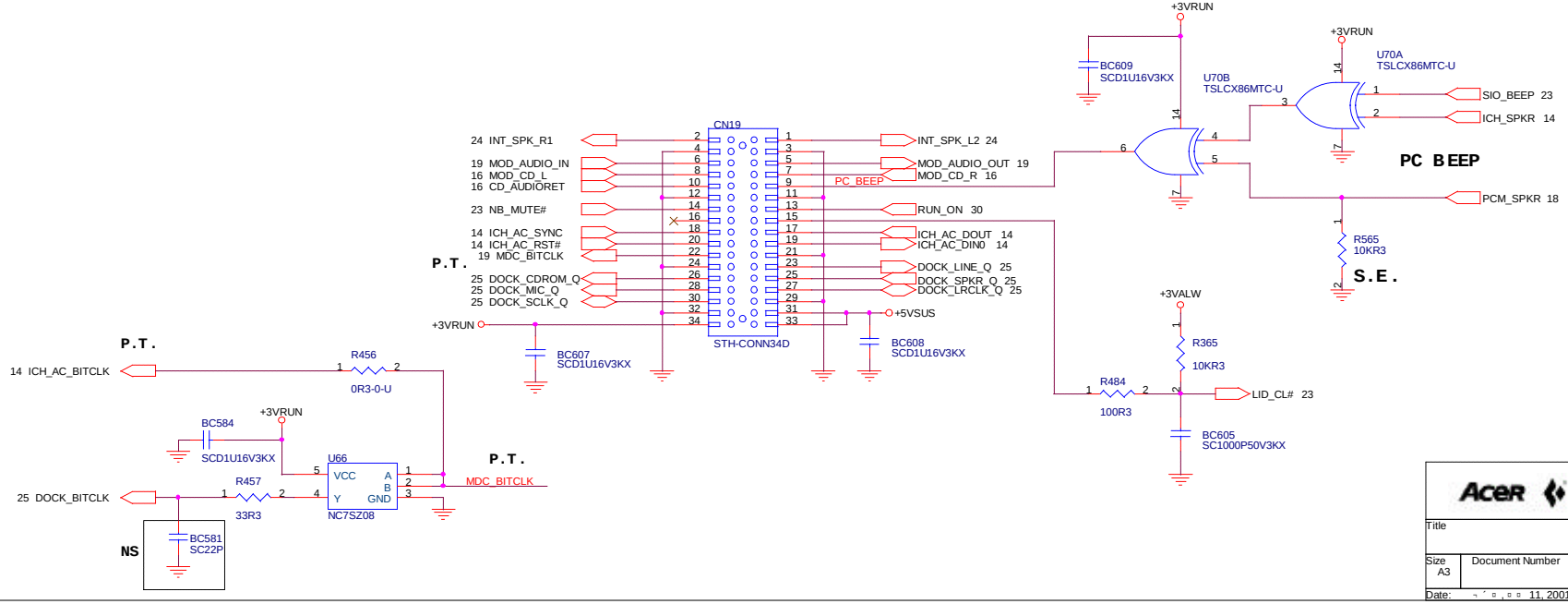


TO C DOCK





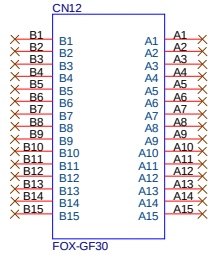
AUDIO BOARD CONN



Acer Incorporated
21F, 88, Sec. 1, Hsin Tai Wu Rd.,
Hsichih, Taipei Hsien 221,
Taiwan, R.O.C.

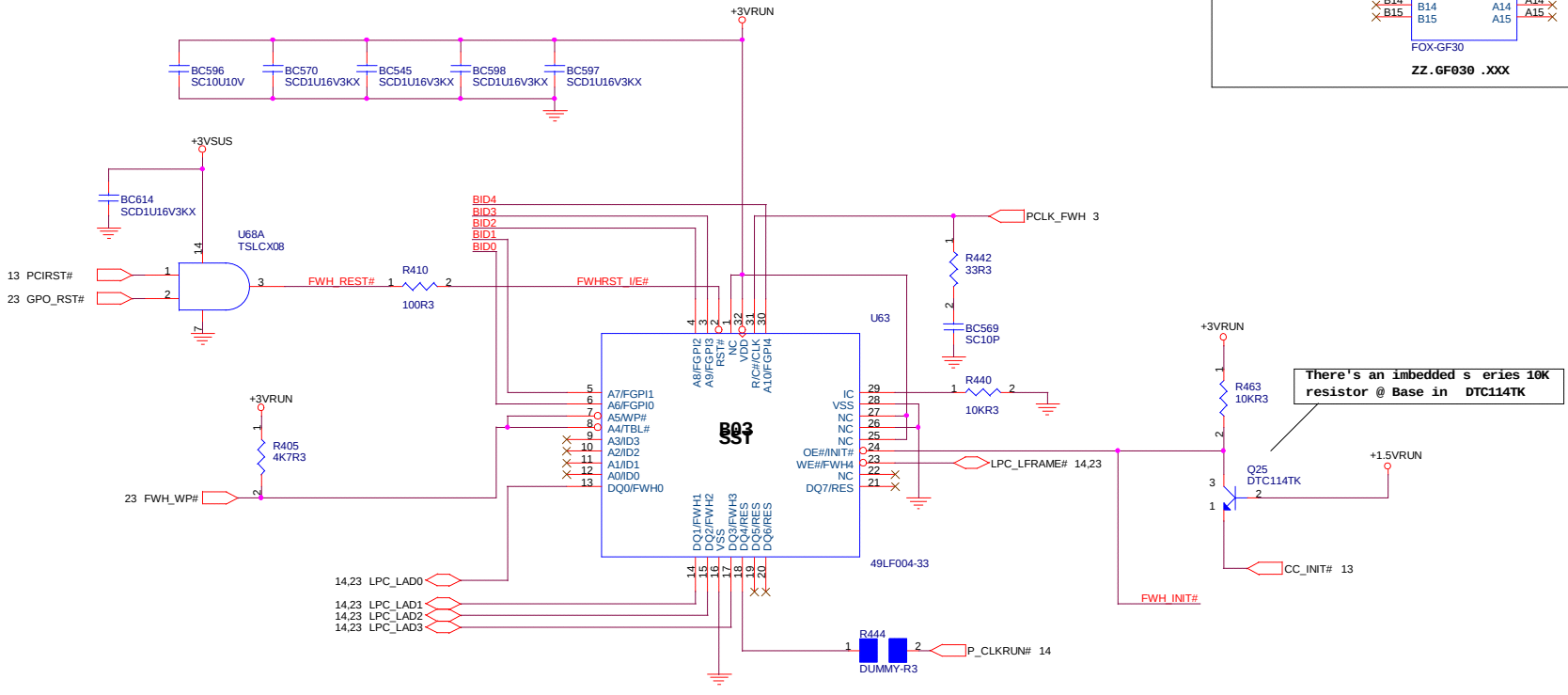
Title	USB/LED CONN	
Size A3	Document Number MONARCH -- 00214	Rev -1
Date: 11, 2001	Sheet 21 of 33	

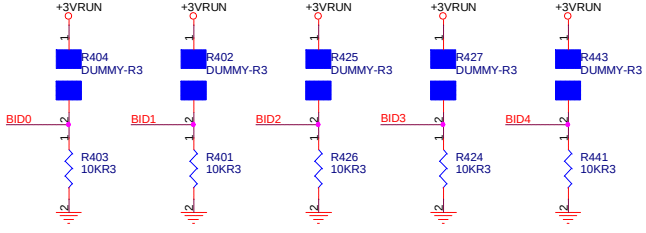
GOLDEN FINGER FOR DEBUG BOARD
No use on P.T.



ZZ.GF030 .XXX

Verify security feature sett ings and pinout





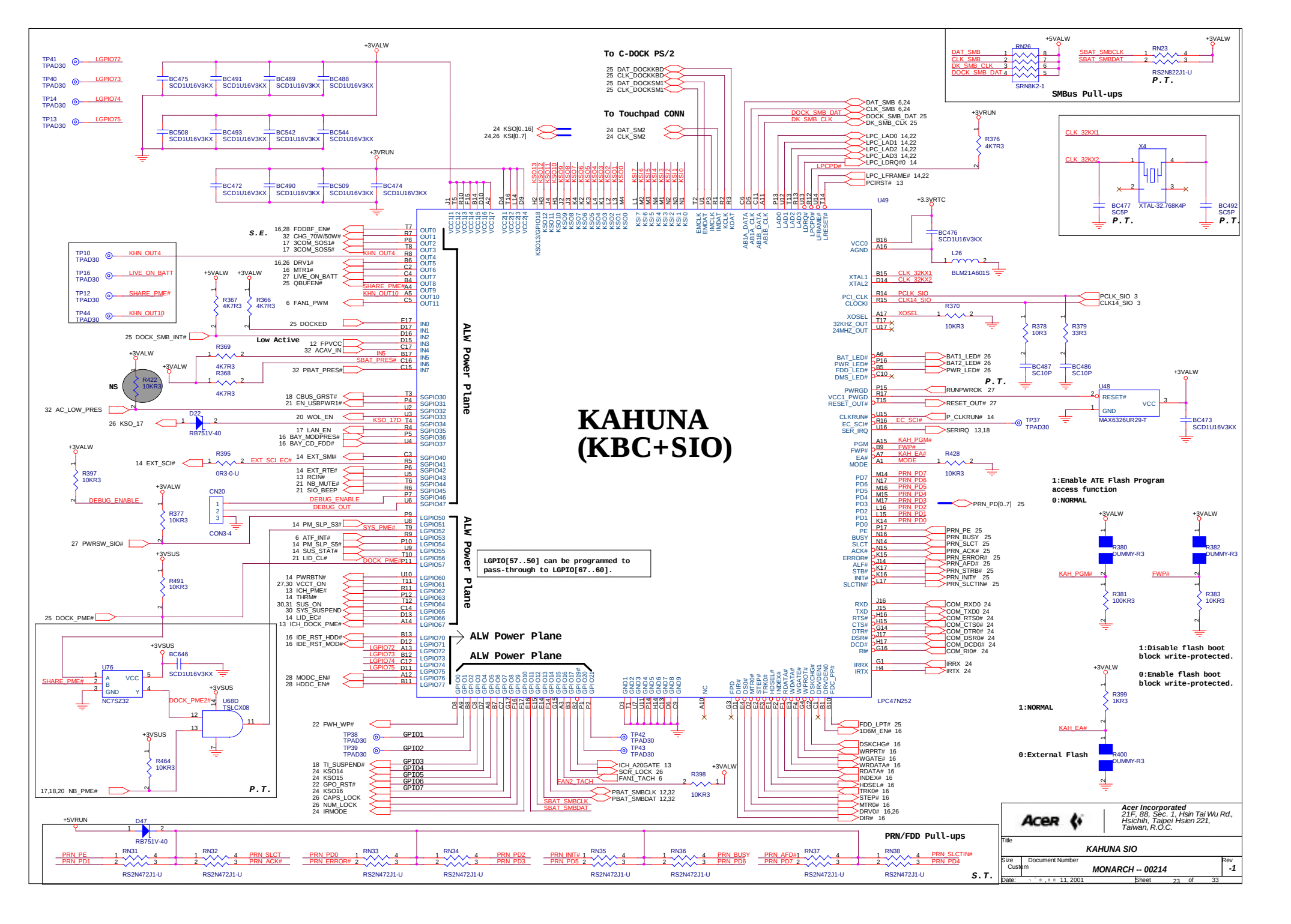
Boot Device must have ID [3:0] = 0000
Has internal pull-dow n resistors
FPET7 Elec. P3-46

Acer Incorporated
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

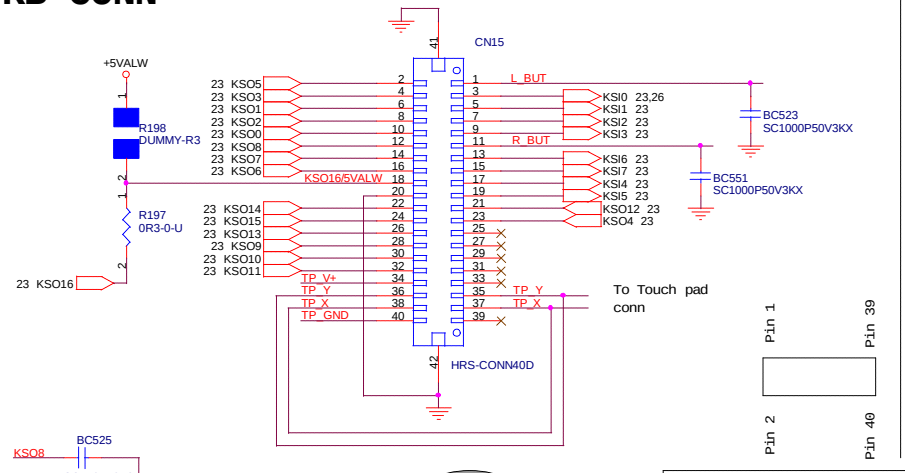
Title: **FIRMWARE HUB / DEBUG BD**

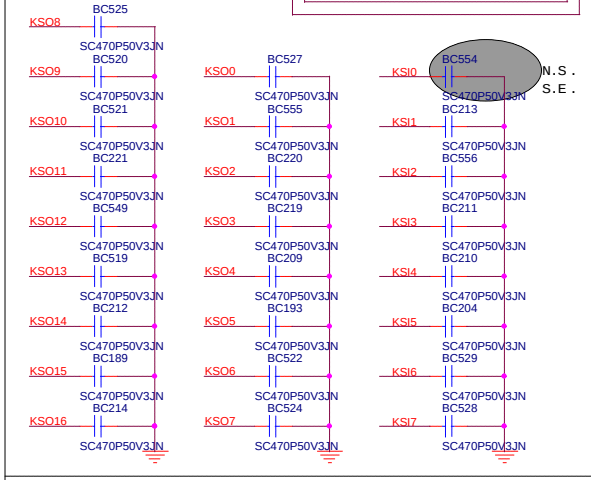
Size	Document Number	Rev
A3	*MONARCH -- 00214*	*-1*

Date: 11, 2001 Sheet 22 of 33

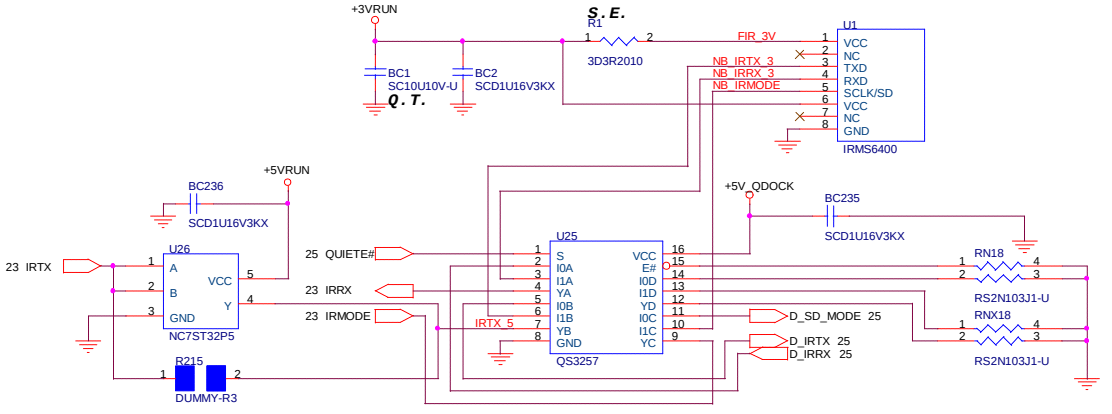

KAHUNA
(KBC+SIO)
To C-DOCK PS/2
To Touchpad CONN
SMBus Pull-ups
PRN/FDD Pull-ups
ALW Power Plane
ALW Power Plane
ALW Power Plane
ALW Power Plane
LPC47N252
U49
Low Active
NS
S.E.
LGPIO[57..50] can be programmed to pass-through to LGPIO[67..60].
1:Enable ATE Flash Program access function
0:NORMAL
1:Disable flash boot block write-protected.
0:Enable flash boot block write-protected.
1:NORMAL
0:External Flash
Acer Incorporated
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
KAHUNA SIO
MONARCH -- 00214
-1
11, 2001
23 of 33

KB CONN

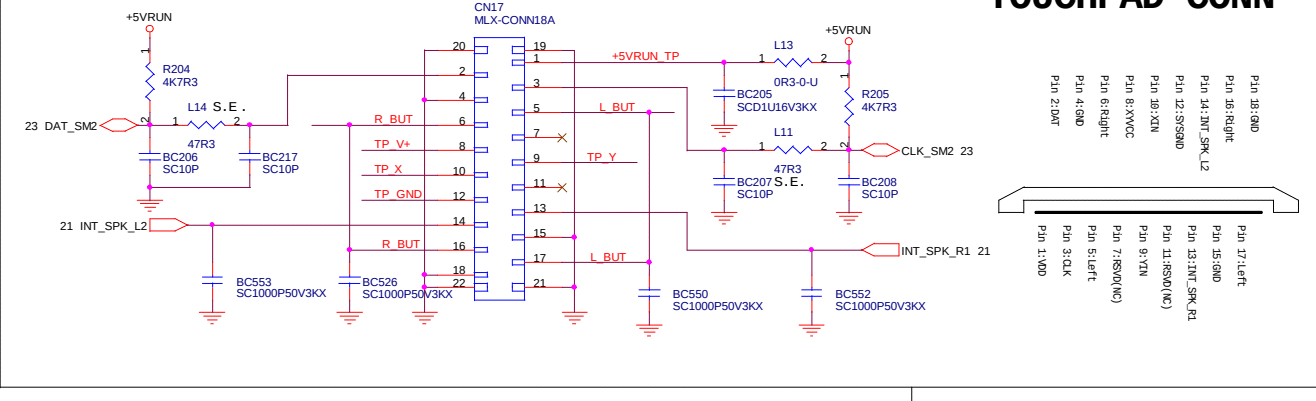




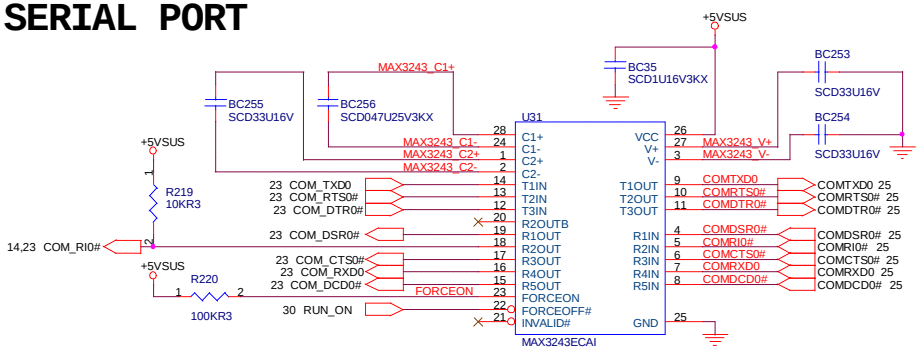
FIR

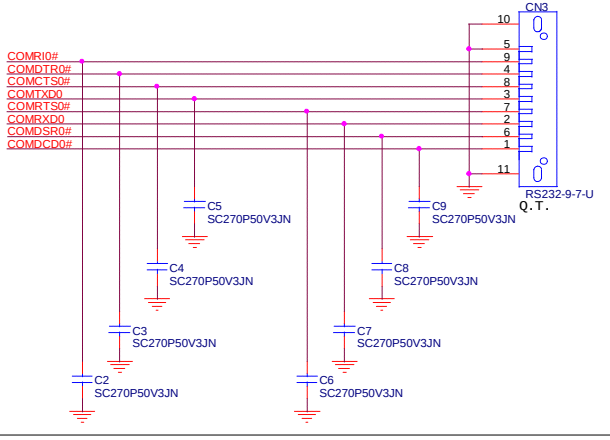


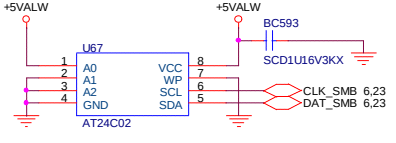
TOUCHPAD CONN



SERIAL PORT





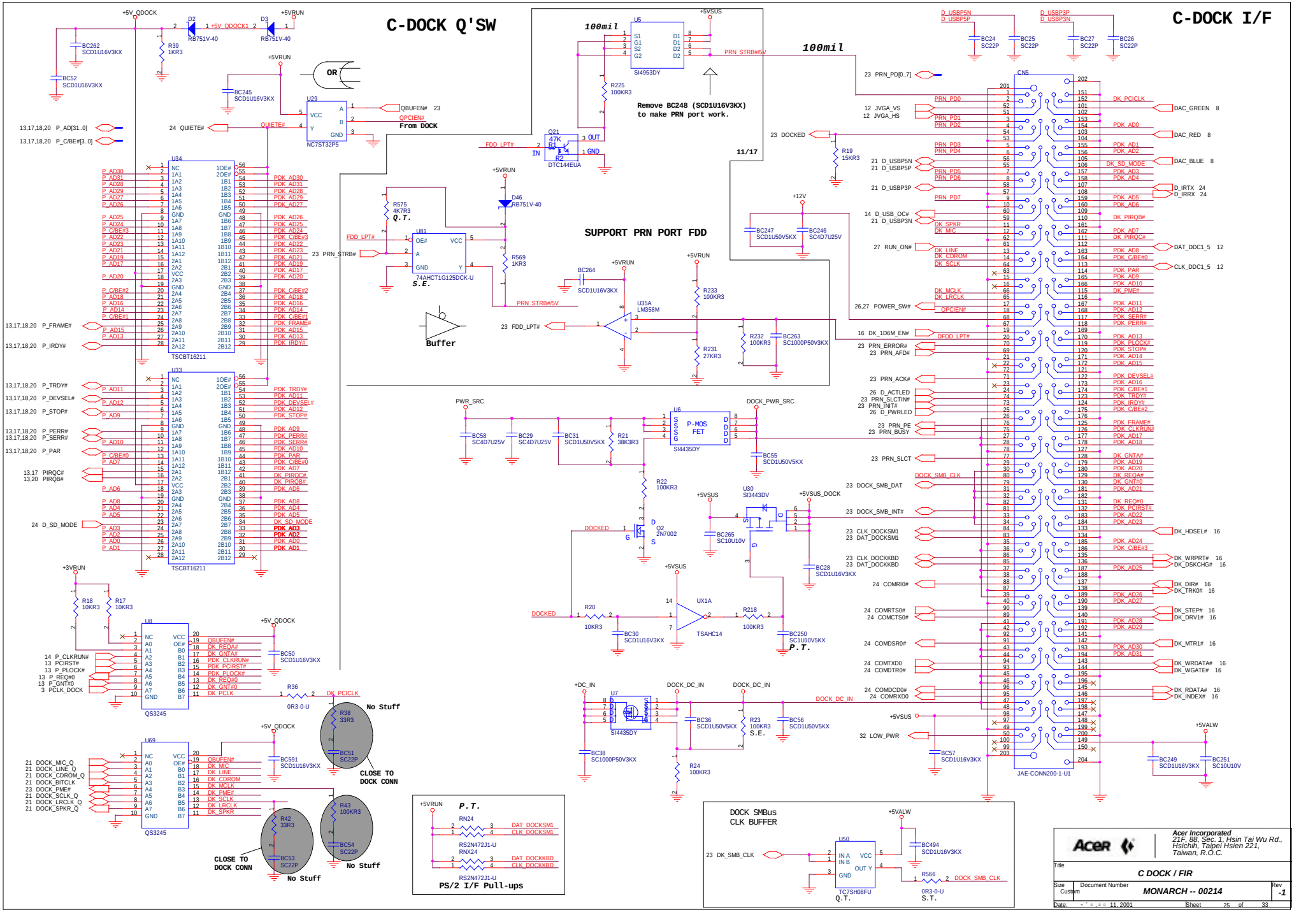


Acer Incorporated
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

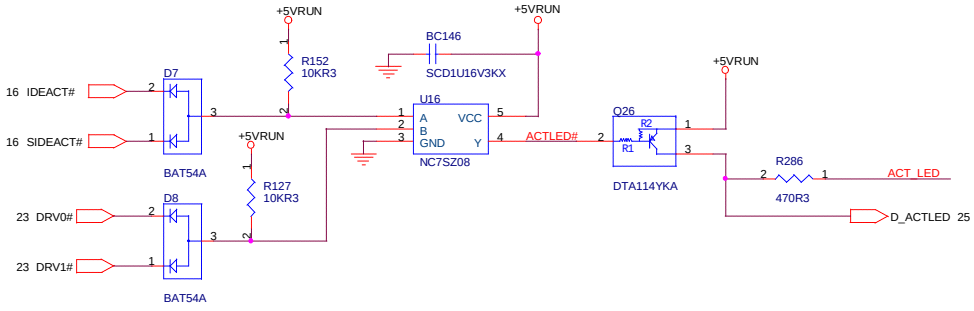
Title: TOUCHPAD, KB CONN, EEPROM

Size	Document Number	Rev
A3	MONARCH -- 00214	-1

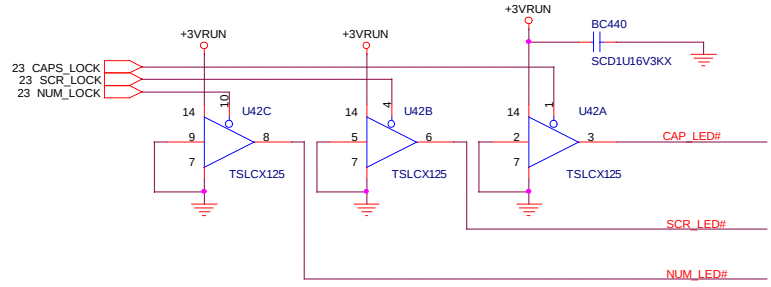
Date: 11, 2001 Sheet 24 of 33


C-DOCK Q'SW
C-DOCK I/F
SUPPORT PRN PORT FDD
Buffer
OR
From DOCK
Remove BC248 (SCD1U16V3KX) to make PRN port work.
100mil
11/17
Q.T.
S.E.
P.T.
No Stuff
CLOSE TO DOCK CONN
PS/2 I/F Pull-ups
DOCK SMBus CLK BUFFER
JAE-CONN200-1-U1
TSCBT16211
QS3245
74AHCT1G125DCK-U
TC7SH08FU
SI4953DY
SI4435DY
SI3443DV
TSAHC14
LM358M
NC7ST32P5
DTC144EUA
RB751V-40
Acer Incorporated
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
C DOCK / FIR
MONARCH -- 00214
-1
Sheet 25 of 33

HDD, CDROM , FDD LED

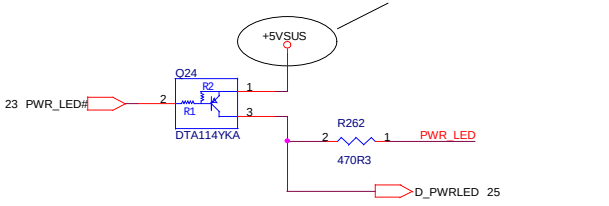


CAPS LOCK, NUM LOCK , SCROLL LOCK LED

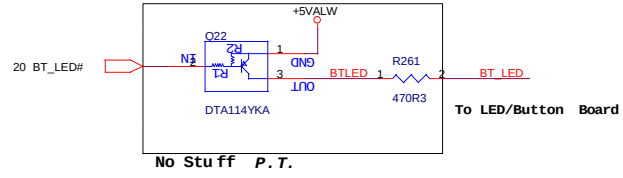


POWER LED

Check +5VSUS or +5VALW

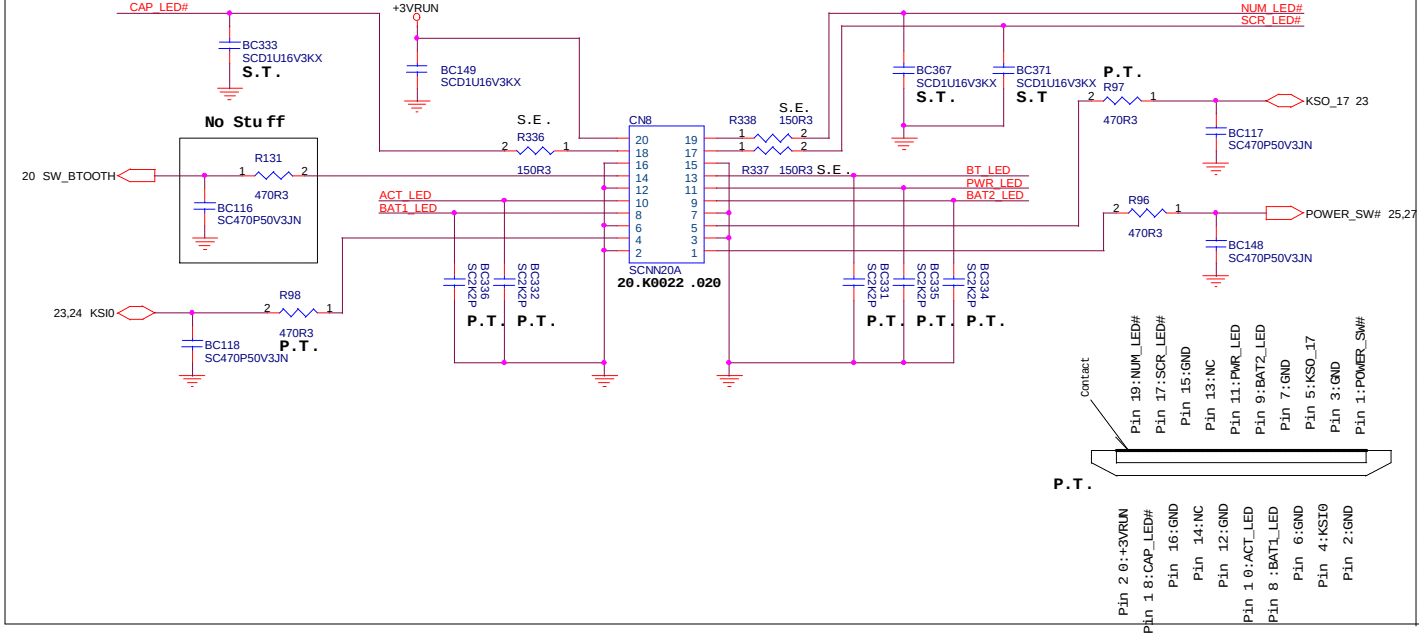


BLUETOOT H LED

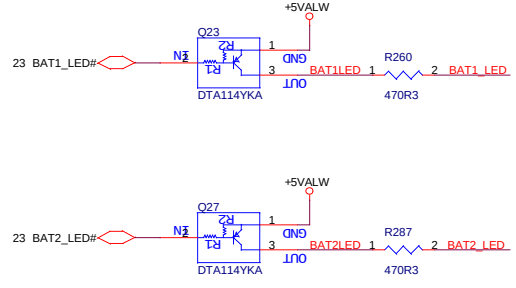


No Stuff P.T.

LED & BUTTON BD CONN

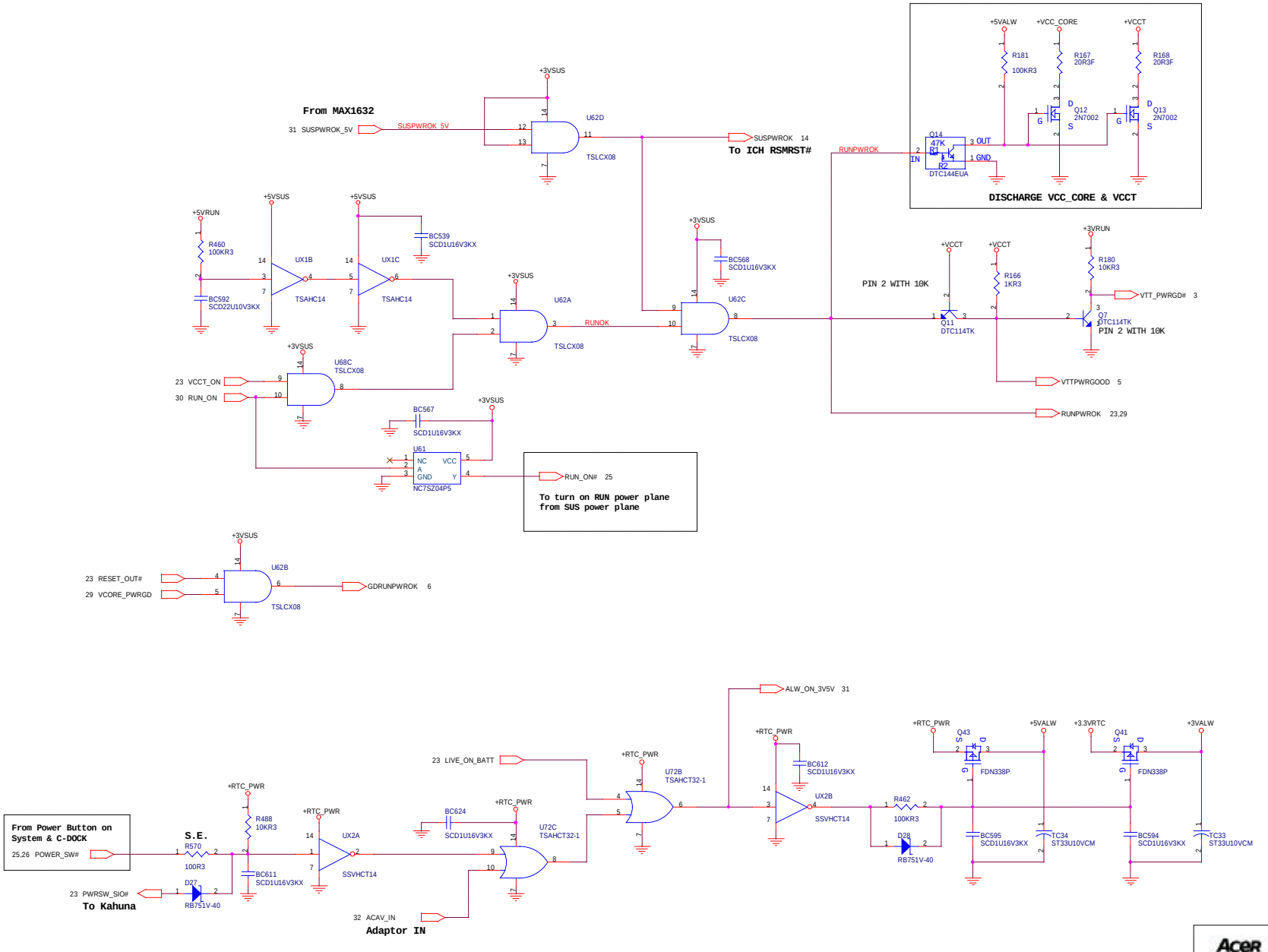


BATTER Y LED



Acer Incorporated
21F, 88, Sec. 1, Hsin Tai Wu Rd.,
Hsichih, Taipei Hsien 221,
Taiwan, R.O.C.

Title	LED BUTTON BD CONN	
Size A3	Document Number MONARCH -- 00214	Rev -1
Date: 11, 2001	Sheet 26 of 33	

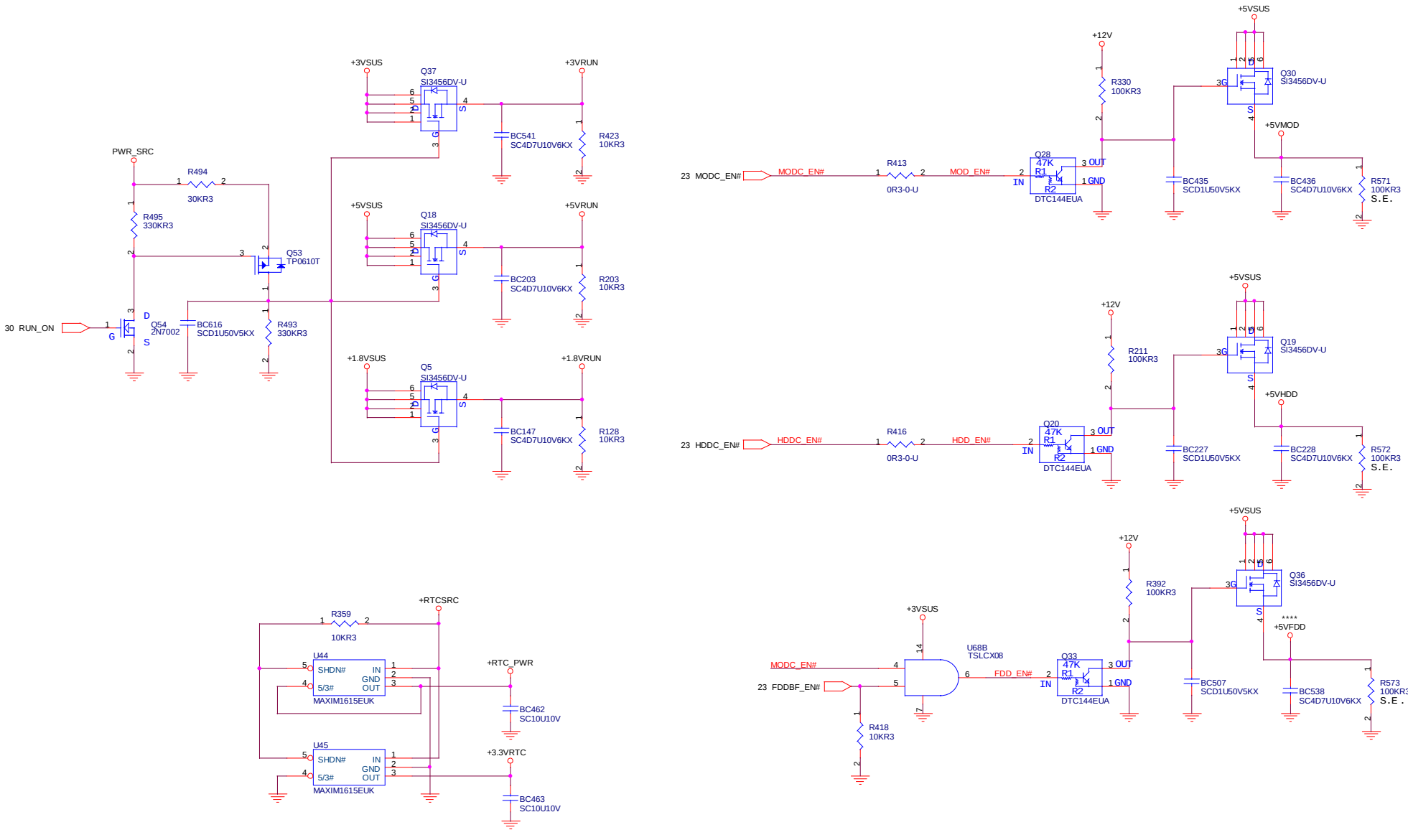


Acer Incorporated
21F, 88, Sec. 1, Hsin Tai Wu Rd.,
Hsichih, Taipei Hsien 221,
Taiwan, R.O.C.

Title: POWER-ON RESET LOGIC

Size	Document Number	Rev
Custom	MONARCH -- 00214	-1

Date: 11, 2001 Sheet 27 of 33



Acer Incorporated
21F, 88, Sec. 1, Hsin Tai Wu Rd.,
Hsichih, Taipei Hsien 221,
Taiwan, R.O.C.

Title

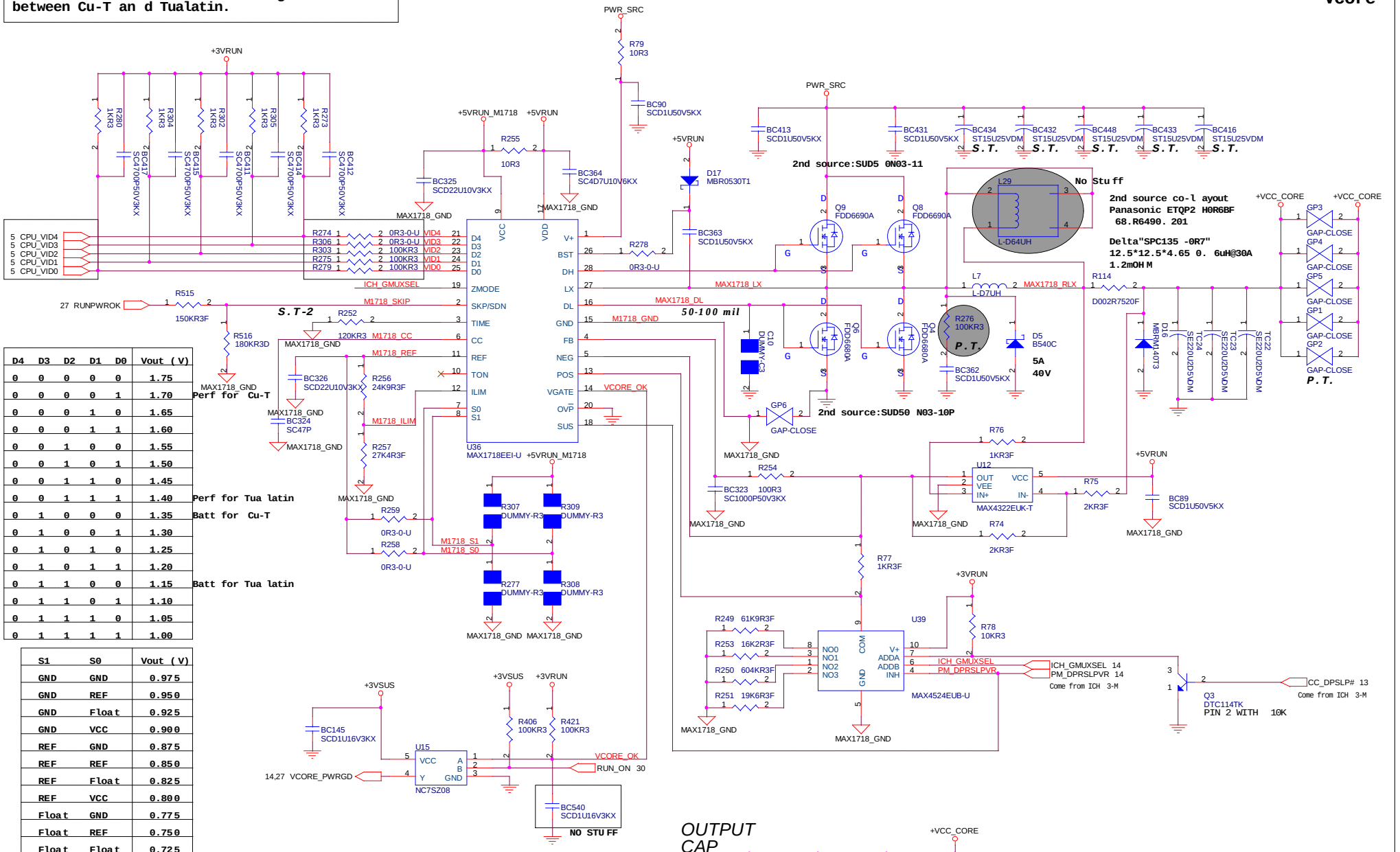
POWER PLANE ENABLES

Size	Document Number	Rev
A3	**MONARCH -- 00214**	**-1**

Date: 11, 2001 Sheet 28 of 33

Plz refer to P.2 for th e Setting Difference between Cu-T an d Tualatin.

Vcore



D4	D3	D2	D1	D0	Vout (V)	
0	0	0	0	0	1.75	
0	0	0	0	1	1.70	
0	0	0	1	0	1.65	
0	0	0	1	1	1.60	
0	0	1	0	0	1.55	
0	0	1	0	1	1.50	
0	0	1	1	0	1.45	
0	0	1	1	1	1.40	Perf for Tua latin
0	1	0	0	0	1.35	Batt for Cu-T
0	1	0	0	1	1.30	
0	1	0	1	0	1.25	
0	1	0	1	1	1.20	
0	1	1	0	0	1.15	Batt for Tua latin
0	1	1	0	1	1.10	
0	1	1	1	0	1.05	
0	1	1	1	1	1.00	

S1	S0	Vout (V)
GND	GND	0.975
GND	REF	0.950
GND	Float	0.925
GND	VCC	0.900
REF	GND	0.875
REF	REF	0.850
REF	Float	0.825
REF	VCC	0.800
Float	GND	0.775
Float	REF	0.750
Float	Float	0.725
Float	VCC	0.700
VCC	GND	0.675
VCC	REF	0.650
VCC	Float	0.625
VCC	VCC	0.600

ZMODE	SUS	Vout Determin ed by:
GND	GND	Logic Level of D0 - D4
VCC	GND	Impedance of D 0 - D4
X	VCC	Logic Level of S0, S1

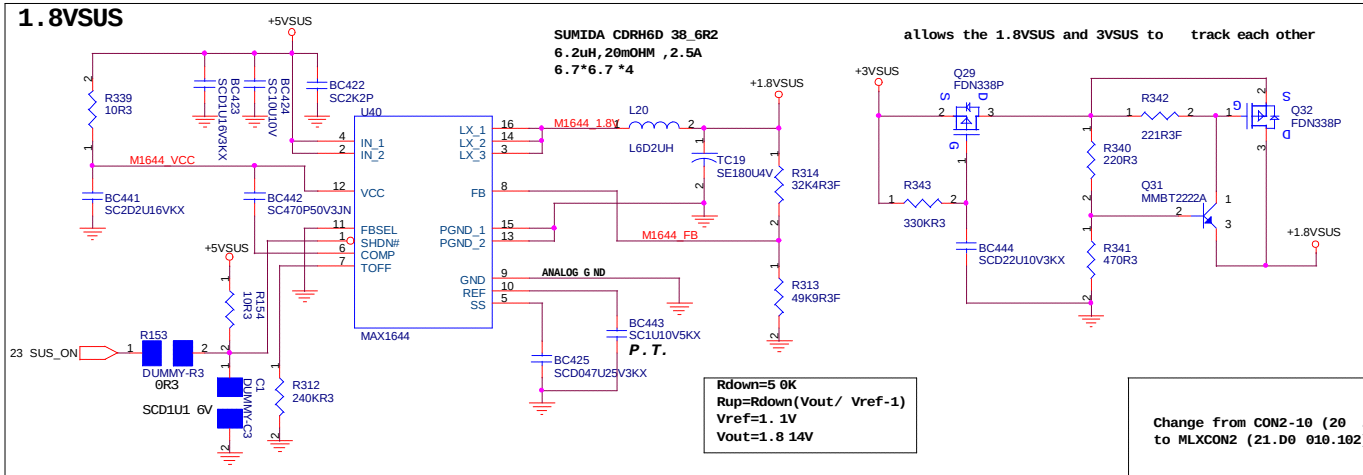
Acer Incorporated
21F, 88, Sec. 1, Hsin Tai Wu Rd.,
Hsichih, Taipei Hsien 221,
Taiwan, R.O.C.

Title: CPU VCORE/VCCT

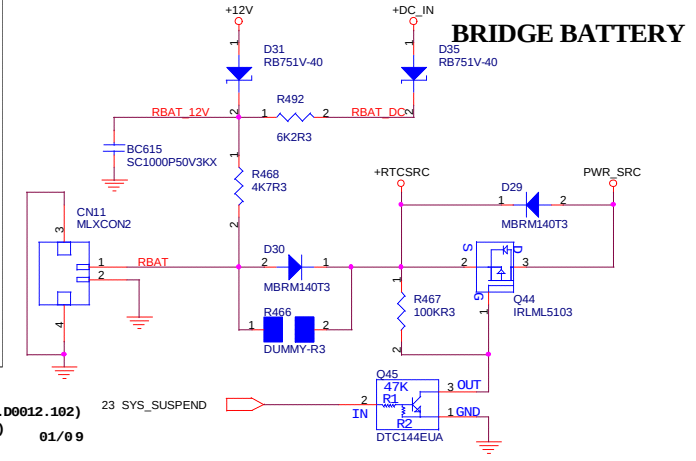
Size: A3 | Document Number: MONARCH -- 00214 | Rev: -1

Date: 11, 2001 | Sheet 29 of 33

1.8VSUS

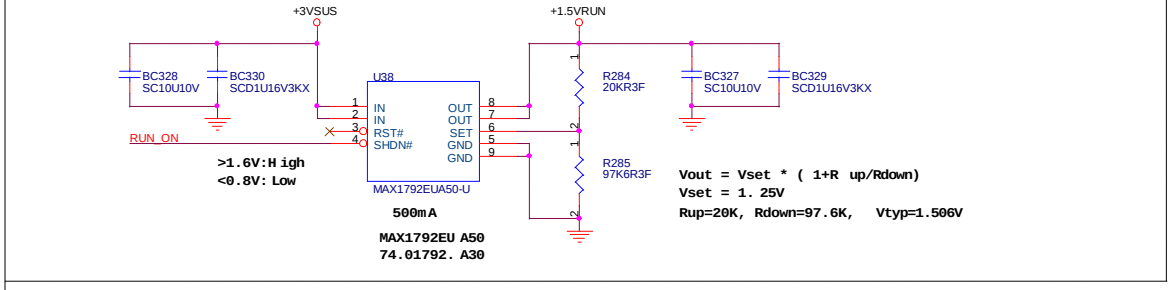


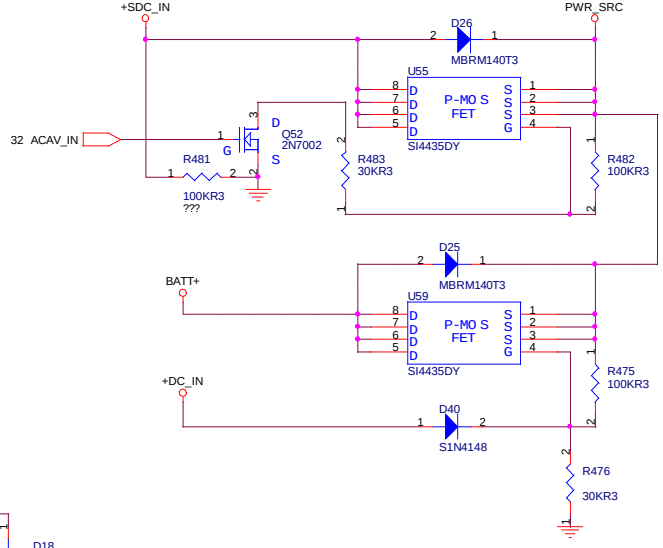
Rdown=5 0K
Rup=Rdown(Vout/ Vref-1)
Vref=1. 1V
Vout=1.8 14V



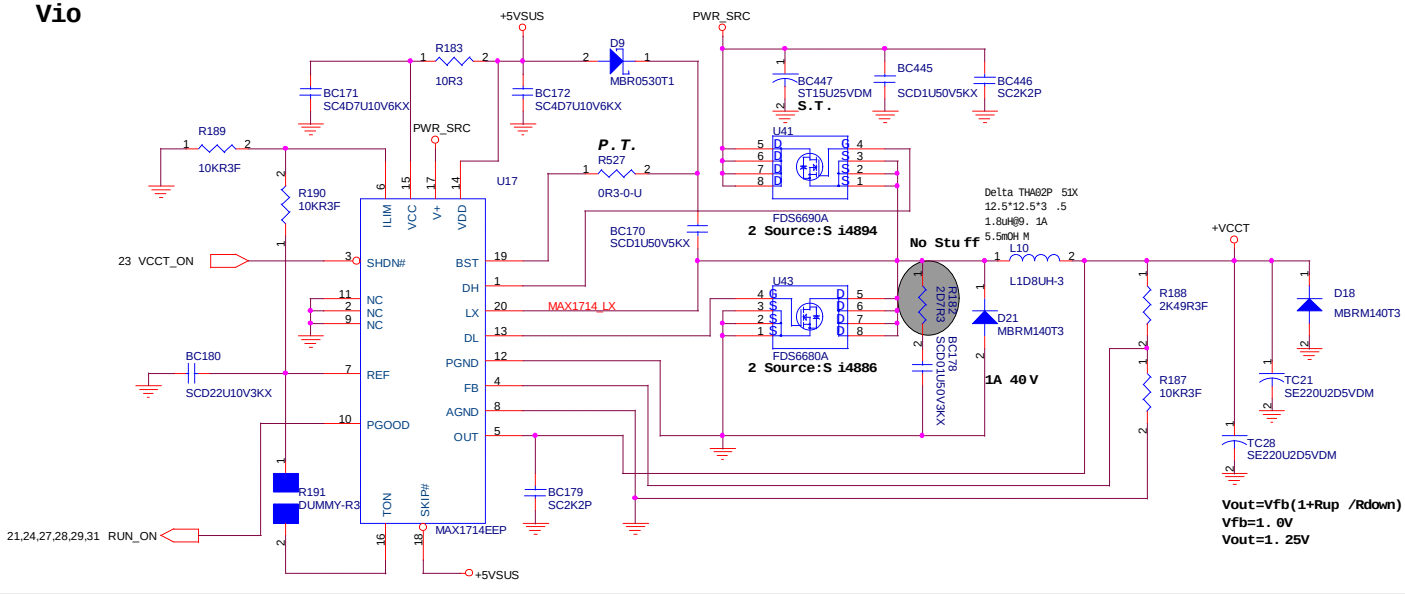
Change from CON2-10 (20 .D0012.102)
to MLXCON2 (21.D0 010.102)
01/09

1.5VSUS





Vio

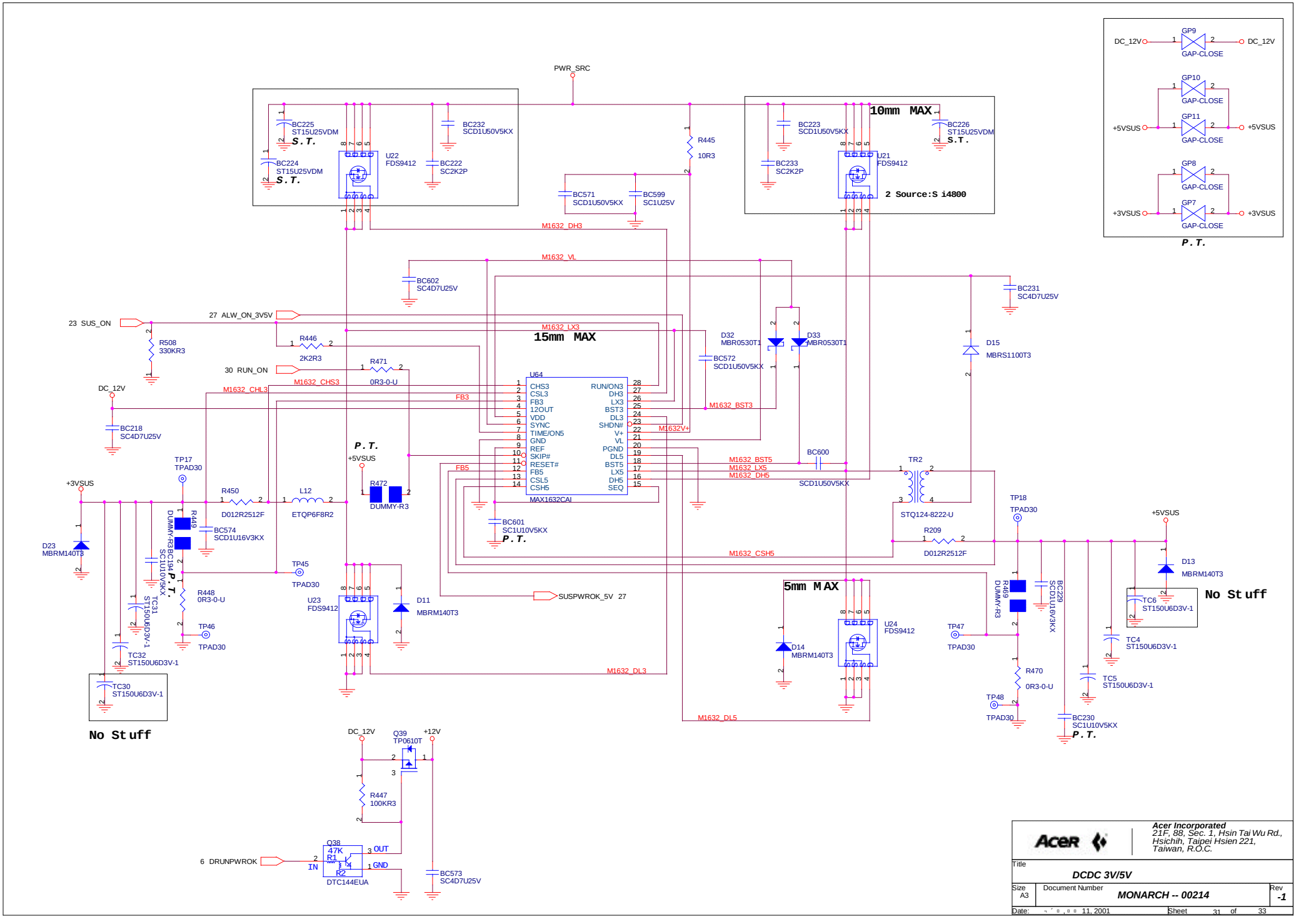


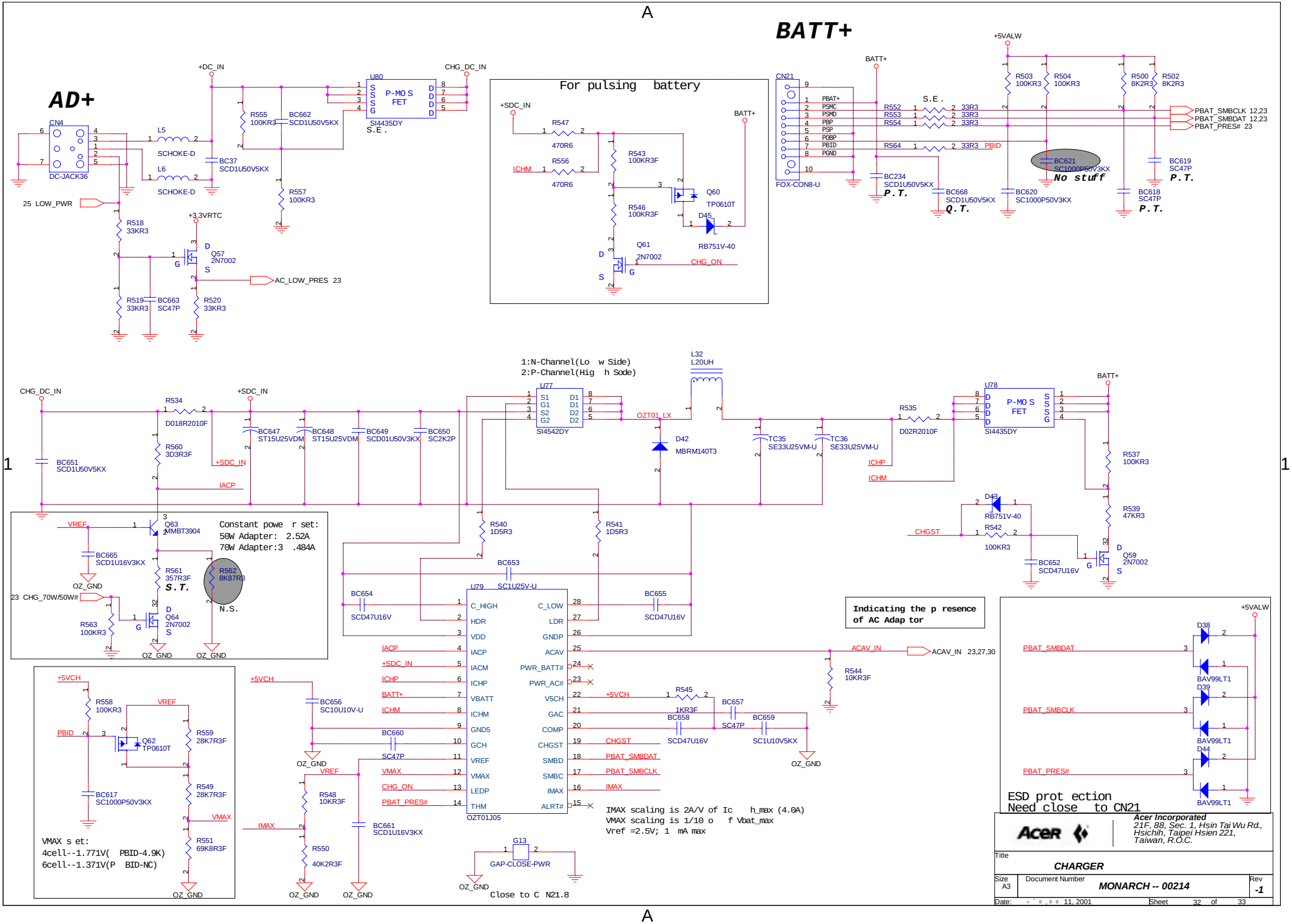
Acer Incorporated
21F, 88, Sec. 1, Hsin Tai Wu Rd.,
Hsichih, Taipei Hsien 221,
Taiwan, R.O.C.

Title: CPU IO, 1.5V, 1.8V & 12V

Size: A3 | Document Number: MONARCH -- 00214 | Rev: -1

Date: 11, 2001 | Sheet 30 of 33


PWR_SRC
10mm MAX
2 Source:S i4800
15mm MAX
5mm MAX
P.T.
No Stuff
No Stuff
U64
MAX1632CAI
U22 FDS9412
U21 FDS9412
U23 FDS9412
U24 FDS9412
Q39 TP0610T
Q38 DTC144EUA
TR2 STQ124-8222-U
GP9 GAP-CLOSE
GP10 GAP-CLOSE
GP11 GAP-CLOSE
GP8 GAP-CLOSE
GP7 GAP-CLOSE
DC_12V
+5VSUS
+3VSUS
+12V
23 SUS_ON
27 ALW_ON_3V5V
30 RUN_ON
6 DRUNPWROK
SUSPWROK_5V 27
M1632_DH3
M1632_VL
M1632_LX3
M1632_CHL3
M1632_CHS3
M1632_BST3
M1632V+
M1632_BST5
M1632_LX5
M1632_DH5
M1632_CSH5
M1632_DL3
M1632_DL5
FB3
FB5
R445 10R3
R446 2K2R3
R471 0R3-0-U
R508 330KR3
R450 D012R2512F
R472 DUMMY-R3
R449 DUMMY-R3
R448 0R3-0-U
R209 D012R2512F
R456 DUMMY-R3
R470 0R3-0-U
R447 100KR3
L12 ETQP6F8R2
D11 MBRM140T3
D13 MBRM140T3
D14 MBRM140T3
D15 MBRS1100T3
D23 MBRM140T3
D32 MBR0530T1
D33 MBR0530T1
BC225 ST15U25VDM
BC224 ST15U25VDM
BC232 SCD1U50V5KX
BC222 SC2K2P
BC223 SCD1U50V5KX
BC233 SC2K2P
BC226 ST15U25VDM
BC571 SCD1U50V5KX
BC599 SC1U25V
BC602 SC4D7U25V
BC231 SC4D7U25V
BC218 SC4D7U25V
BC572 SCD1U50V5KX
BC600 SCD1U50V5KX
BC574 SCD1U16V3KX
BC601 SC1U10V5KX
BC229 SCD1U16V3KX
BC230 SC1U10V5KX
BC573 SC4D7U25V
TC30 ST150U6D3V-1
TC31 ST150U6D3V-1
TC32 ST150U6D3V-1
TC4 ST150U6D3V-1
TC5 ST150U6D3V-1
TC6 ST150U6D3V-1
TP17 TPAD30
TP18 TPAD30
TP45 TPAD30
TP46 TPAD30
TP47 TPAD30
TP48 TPAD30
Acer Incorporated
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
DCDC 3V/5V
Size A3
Document Number MONARCH -- 00214
Rev -1
Date: 11, 2001
Sheet 31 of 33


AD+
BATT+
For pulsing battery
1:N-Channel(Lo w Side)
2:P-Channel(Hig h Sode)
Constant powe r set:
50W Adapter: 2.52A
70W Adapter:3 .484A
Indicating the p resence of AC Adap tor
VMAX s et:
4cell--1.771V(PBID-4.9K)
6cell--1.371V(P BID-NC)
IMAX scaling is 2A/V of Ic h_max (4.0A)
VMAX scaling is 1/10 o f Vbat_max
Vref =2.5V; 1 mA max
ESD prot ection
Need close to CN21
Close to C N21.8
Acer Incorporated
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
CHARGER
MONARCH -- 00214
-1
11, 2001
32 of 33

Impedance measurement coupon

Trace length >= 4 inches

Trace width / Spacin g = 5 / 5 mil

L1 — R510 — R511

L10 — R512 — R513

Trace width / Spacin g = 4 / 5 mil

L3 — R514 — R515

L4 — R516 — R517

L7 — R518 — R519

L8 — R520 — R521

USB Diff. pair Twidth/Tsp acing = 5/7 mil

L3 — R522 — R523

L3 — R524 — R525

Diff. pair for LVD S, CLK, LAN
Twidth/Tspacing = 4/7 mil

L3 — R526 — R527

L3 — R528 — R529

L4 — R530 — R531

L4 — R532 — R533

L7 — R534 — R535

L7 — R536 — R537

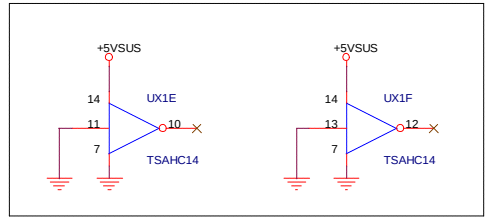
L8 — R538 — R539

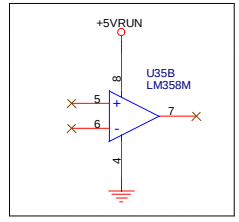
L8 — R540 — R541

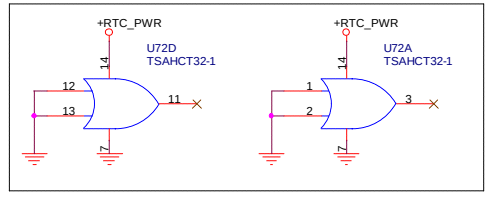
CRT signal Trace Twidth/Ts pacing = 8/5 mil

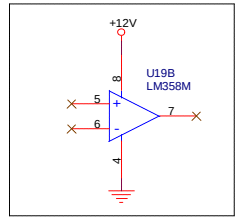
Ln — R542 — R543

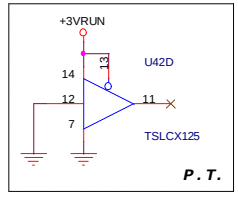
4 " = 1 " (L1) + 2" (L2) + 1" (L8)

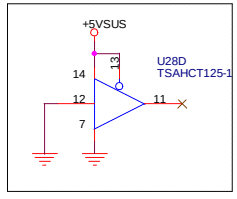


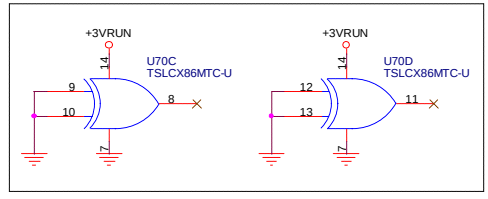


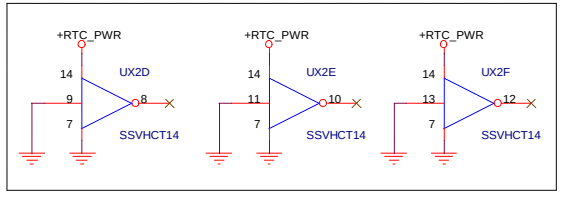


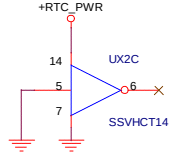


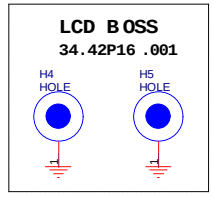


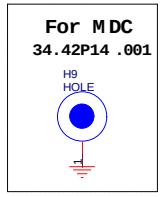


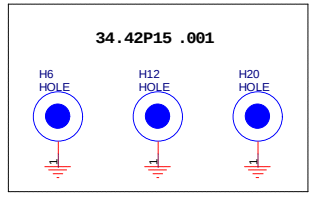


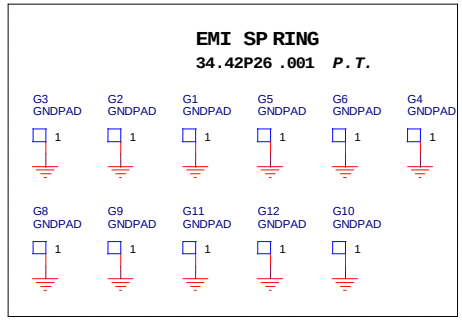


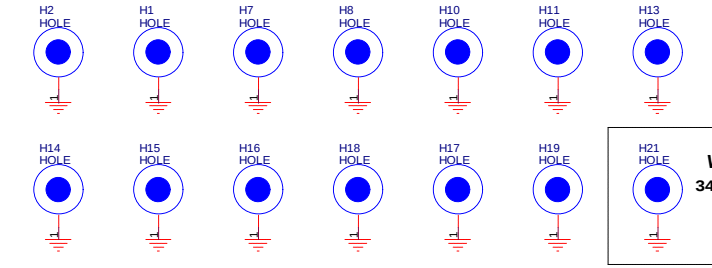


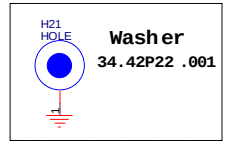












Acer Incorporated
21F, 88, Sec. 1, Hsin Tai Wu Rd.,
Hsichih, Taipei Hsien 221,
Taiwan, R.O.C.

Title: HOLES,GND PADS

Size: A3 | Document Number: MONARCH -- 00214 | Rev: -1

Date: 11, 2001 | Sheet 33 of 33