

MOLOKAI Block Diagram

SPR.01.2004

Project Code:91.43E01.001

03249-SC

PCB LAYER

- L1 : COMPONENT
- L2 : GND
- L3 : SIGNAL1
- L4 : SIGNAL2
- L5 : VCC
- L6 : GND
- L7 : SIGNAL3
- L8 : COMPONENT

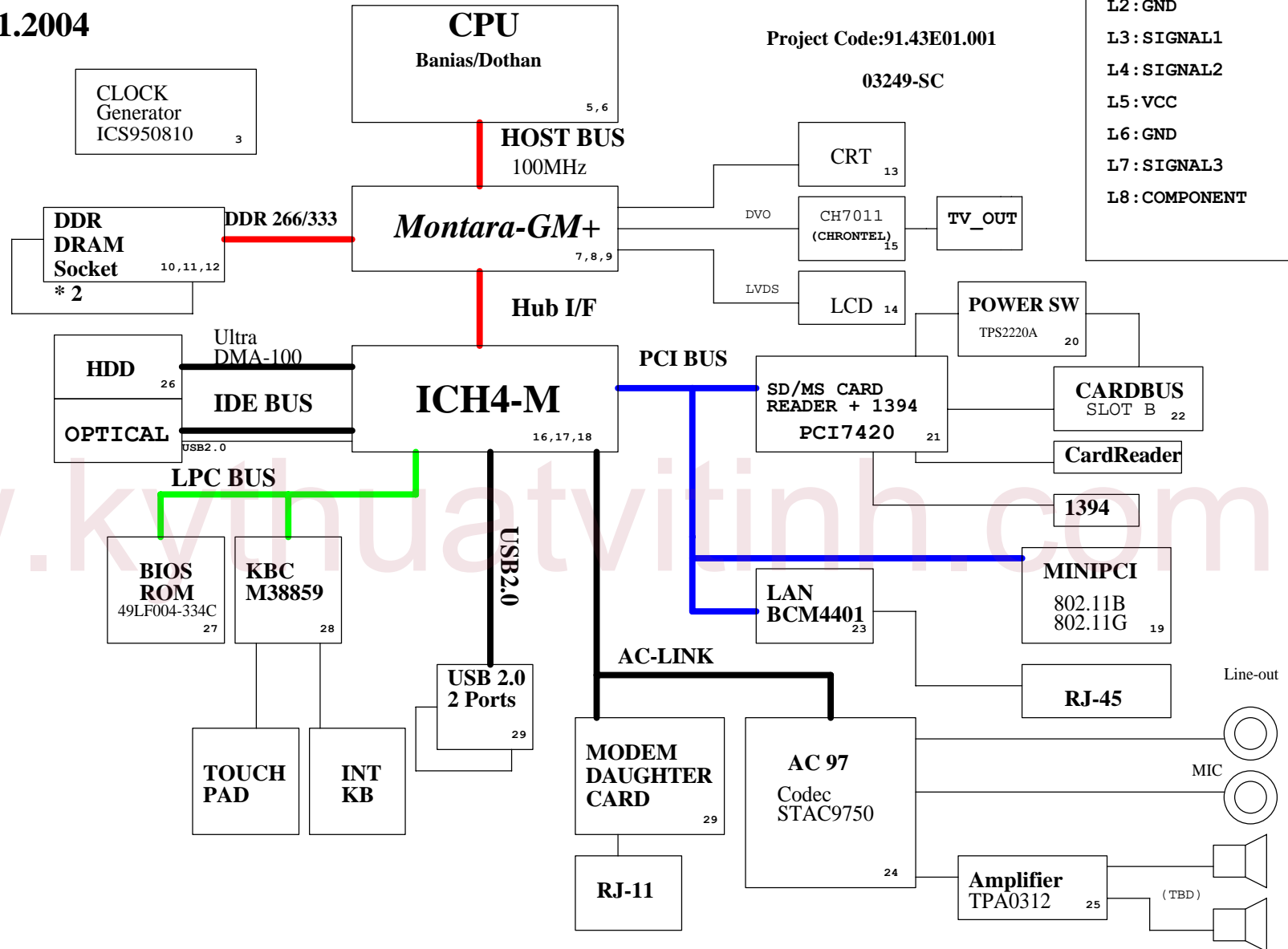
DC/DC IMVP4	
Switching Power ISL6218 32	
INPUTS	OUTPUT
DCBATOUT	VCC_CORE

SYSTEM DC/DC	
MAX1715 34	
INPUTS	OUTPUTS
DCBATOUT	1D35V_S0 2D5V_S3

DC/DC&CHARGER	
MAX1645 35	
INPUTS	OUTPUTS
AD+	BT+

DC/DC	
MAX1999 33	
INPUTS	OUTPUTS
DCBATOUT	3D3V_S5 5V_S5

G913C/APL1085	
APL5331kAC/G1211X 38	
INPUTS	OUTPUTS
3D3V_S0	1D8V_VCCA_S0
3D3V_S5	1D5V_S5
3D3V_S0	1D5V_S0
2D5V_S3	1D25V_S0
1D35V_S0	VCC_IO_S0



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Title: **BLOCK DIAGRAM**

Size: A3 Document Number: **MOLOKAI** Rev: **SC**

Date: Monday, April 05, 2004 Sheet 1 of 39

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S5

5V_S5 ○—○ 5V_S5 18,33,34,36
 3D3V_S5 ○—○ 3D3V_S5 4,16,17,18,28,30,31,33,36,38,39
 1D5V_S5 ○—○ 1D5V_S5 18,38
 VCC_RTC_S5 ○—○ VCC_RTC_S5 17

AC-IN / BAT-IN

AD+ ○—○ AD+ 35,37,39
 DCBATOUT ○—○ DCBATOUT 14,32,33,34,35,36,38,39

OTHERS

5V_AUX ○—○ 5V_AUX 30,31,33,35,37,38,39
 3D3V_AUX ○—○ 3D3V_AUX 14,17,33

 3D3V_RTC ○—○ 3D3V_RTC 17,28
 ICH_VBIAS ○—○ ICH_VBIAS 17
 MAX1999_REF ○—○ MAX1999_REF 33,38
 MAX1999_VCC ○—○ MAX1999_VCC 33

S3

3D3V_S3 ○—○ 3D3V_S3 14,25,28,30,34,36,39
 2D5V_S3 ○—○ 2D5V_S3 7,9,10,11,34,38,39
 1D25V_DDRVREF_S3 ○—○ 1D25V_DDRVREF_S3 7,10,34

LAN-AC

3D3V_LAN_S5AC ○—○ 3D3V_LAN_S5AC 23,29,36,37

S0

5V_S0 ○—○ 5V_S0 13,14,17,18,19,20,24,26,28,30,32,34,36,38,39
 3D3V_S0 ○—○ 3D3V_S0 3,7,8,9,10,13,14,15,16,17,18,19,20,21,22,24,25,26,27,29,30,31,32,36,38,39

 1D5V_S0 ○—○ 1D5V_S0 7,8,9,15,16,18,27,38,39
 1D25V_S0 ○—○ 1D25V_S0 11,12,38
 1D35V_S0 ○—○ 1D35V_S0 7,9,34,38,39
 VCC_CORE_S0 ○—○ VCC_CORE_S0 6,32,39
 VCC_IO_S0 ○—○ VCC_IO_S0 4,5,6,7,9,17,18,32,38,39
 1D8V_VCCA_S0 ○—○ 1D8V_VCCA_S0 5,38

5VA_AUD_S3 ○—○ 5VA_AUD_S3 24 → **AUDIO**

 3D3V_LCD_S0 ○—○ 3D3V_LCD_S0 14 → **LCD**
 CRT_VCC_S0 ○—○ CRT_VCC_S0 13 → **CRT**

 TV3D3V1_S0 ○—○ TV3D3V1_S0 15 → **TV-OUT**
 TV3D3VA_S0 ○—○ TV3D3VA_S0 15
 TV3D3V2_S0 ○—○ TV3D3V2_S0 15
 TV1D5V_S0 ○—○ TV1D5V_S0 15

PCI TABLE

DEVICE	IDSEL	IRQ	REQ# / GNT#
SD/MS CARD READER+1394 PCI7420	AD20	PIRQB# PIROC# PIRQF#	REQ#1 / GNT#1
MINI PCI 802.11B/G	AD17	PIRQE# PIRQG#	REQ#0 / GNT#0
LAN BCM4401	AD21	PIRQD#	REQ#4 / GNT#4

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Title: **Table of Content**

Size: A3 Document Number: **MOLOKAI** Rev: **SC**

Date: Saturday, April 17, 2004 Sheet 2 of 39



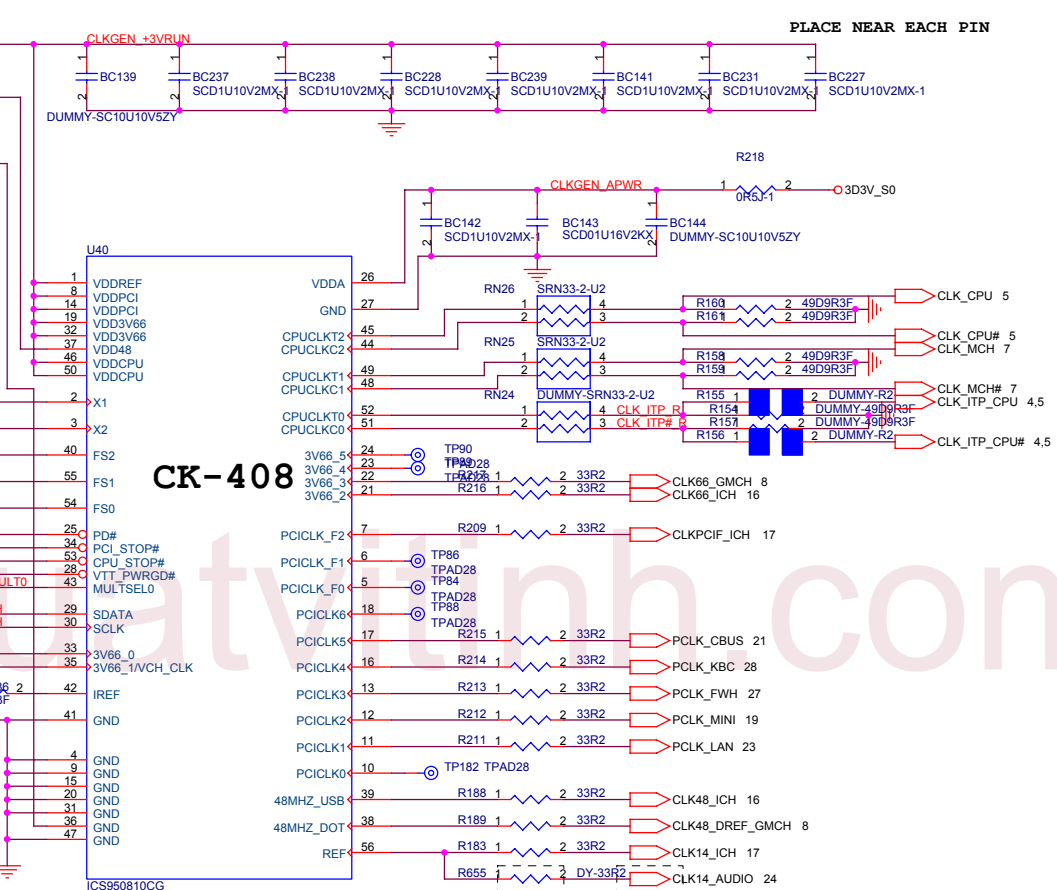
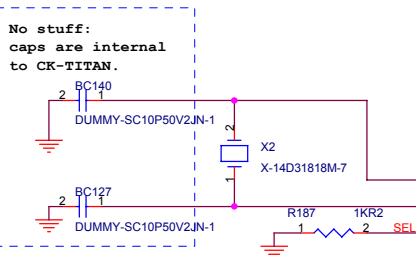
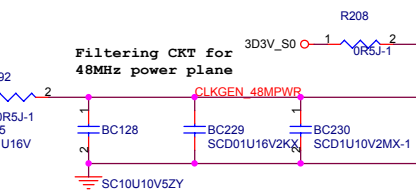
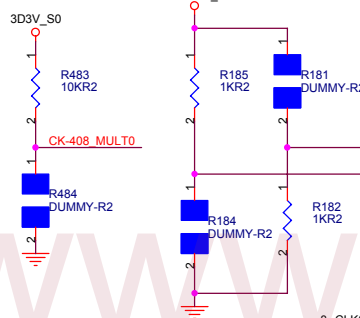
Host Freq. Setting

FS1/0 = 00 166MHz
 FS1/0 = 01 100MHz
 FS1/0 = 10 200MHz
 FS1/0 = 11 133MHz

FS2 = 0 unbuffer mode (disable 66MHz-IN)
 FS2 = 1 buffer mode

Mult0 = 0 Rr=221,Iref=5mA =>Vswing=1.0V@50ohm
 Mult0 = 1 Rr=475,Iref=2.32mA =>Vswing=0.7V@50ohm

CPU & MEMORY Freq. Selection

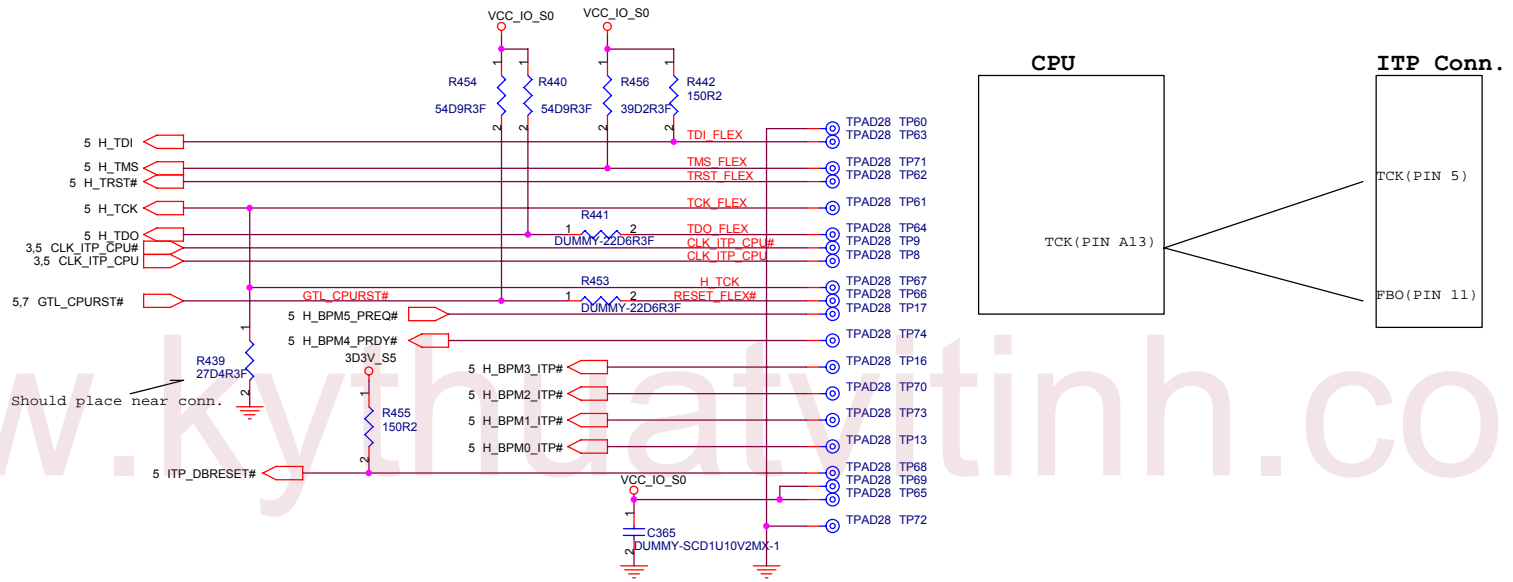


CK-408

SC:Because codec change to use crystal so dummy CLK source
 01/15/2004

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Title: Clock GEN.			
Size: A3	Document Number: MOLOKAI	Rev: SC	
Date: Thursday, April 15, 2004	Sheet: 3	of	39

ITP Debug Pad



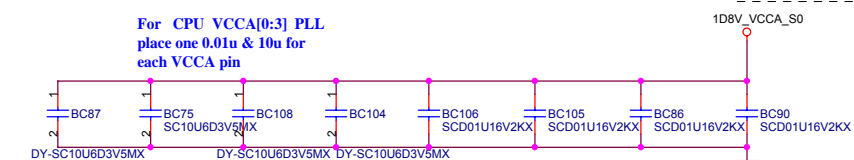
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ITP			
Size	Document Number		Rev
A3	MOLOKAI		SC
Date:	Thursday, April 15, 2004	Sheet	4 of 39

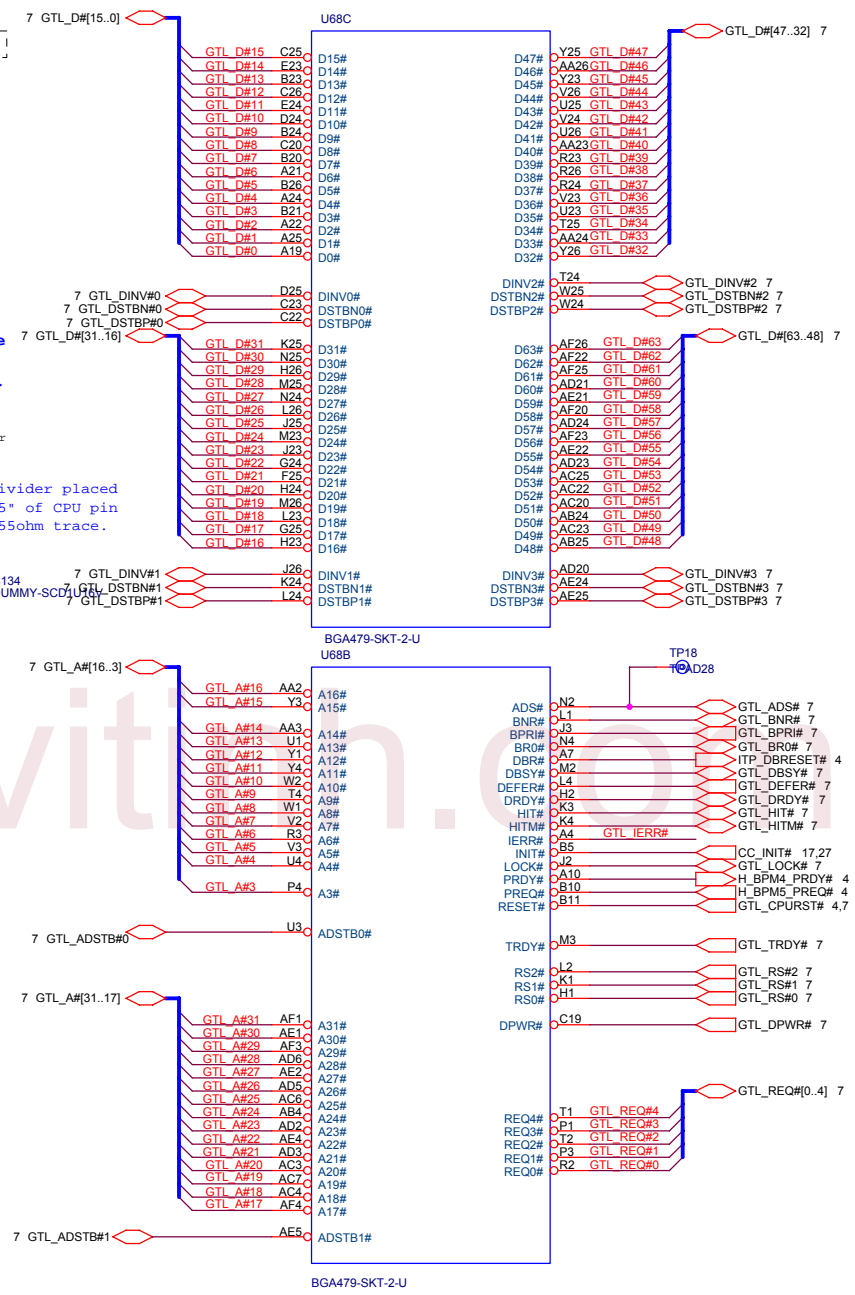
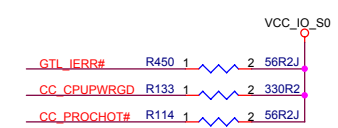
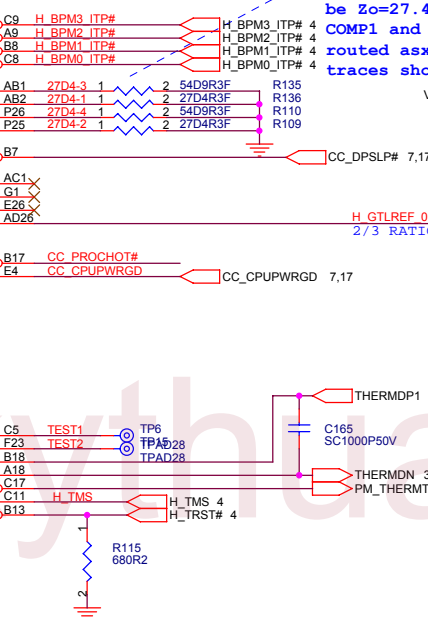
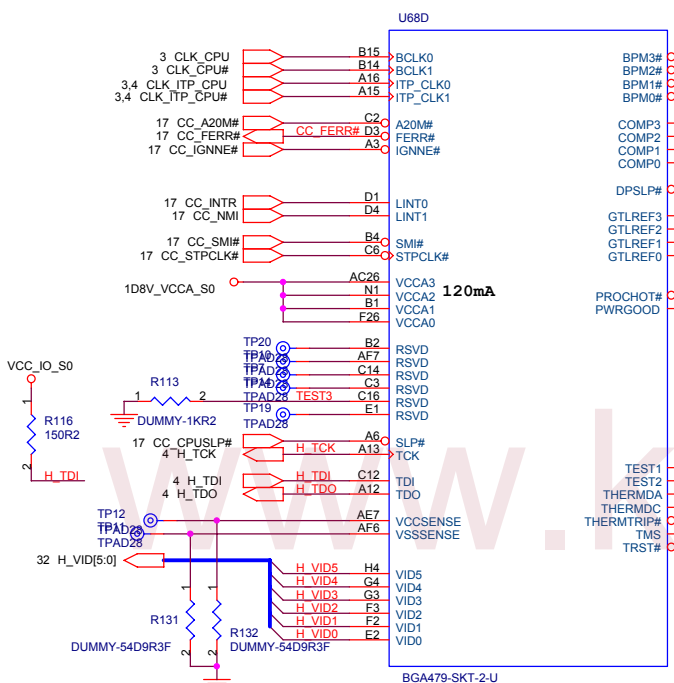
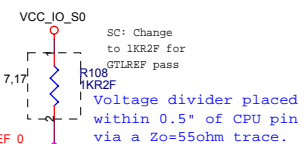
CPU VCCA POWER:

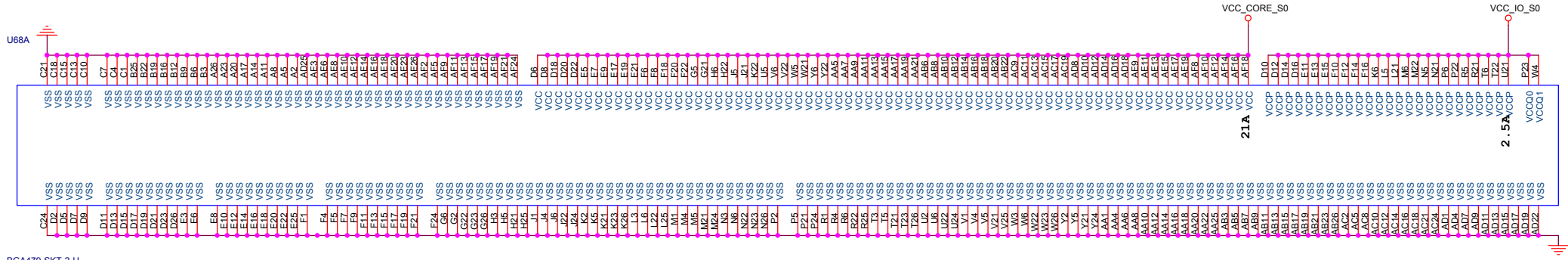
At Dothan CPU application, POWER is 1.5V or 1.8V.

For CPU VCCA[0:3] PLL
place one 0.01u & 10u for
each VCCA pin

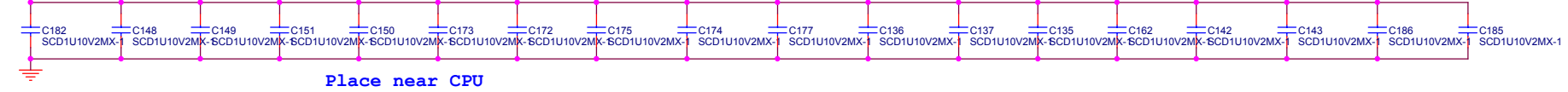


Layout note:
COMP0 and COMP2 need to
be $Z_o=27.4\text{ohm}$ traces.
COMP1 and COMP3 should be
routed as $Z_o=54.9\text{ohm}$,
traces shorter than 0.5".

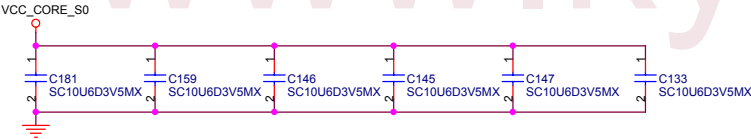
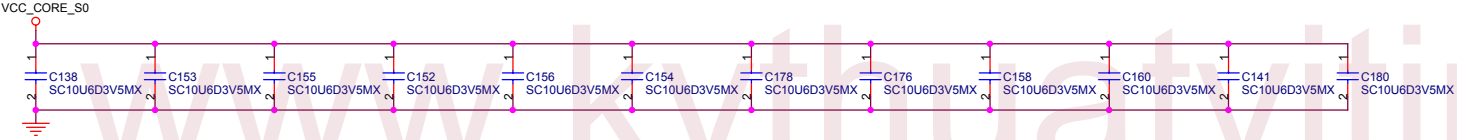




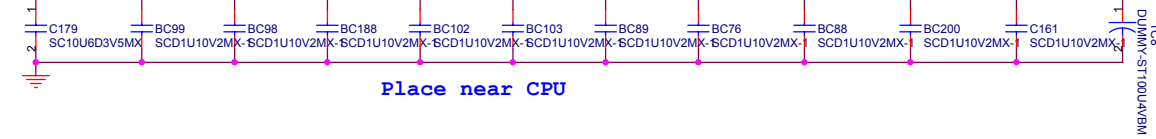
10uF_6.3V *18 ,0805,X5R 0.1uF_10V *18 ,0402,X7R



Place near CPU

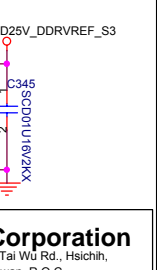
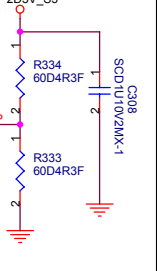
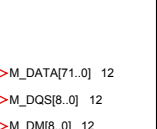
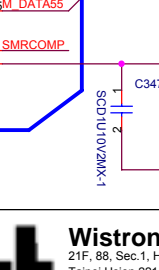
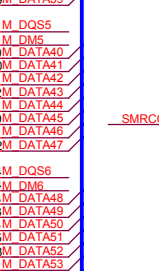
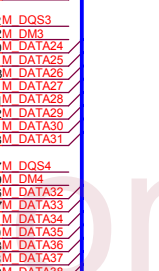
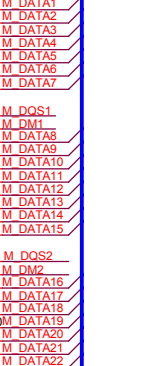
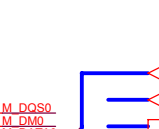
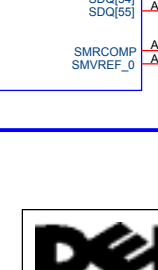
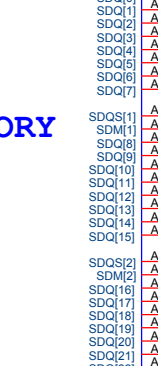
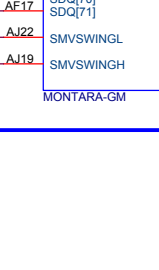
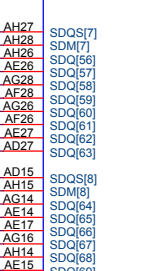
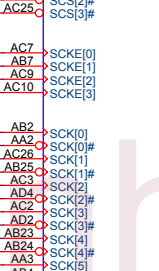
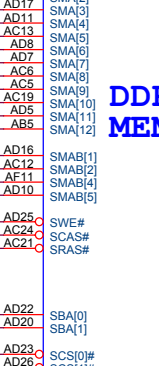
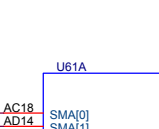
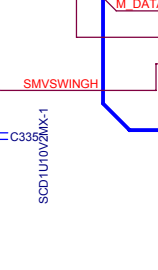
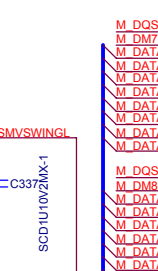
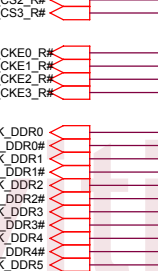
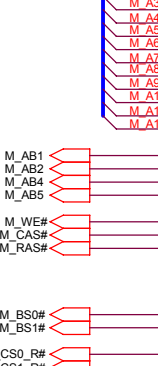
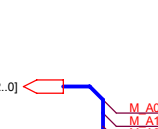
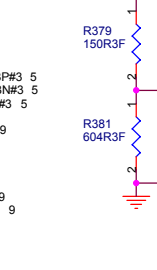
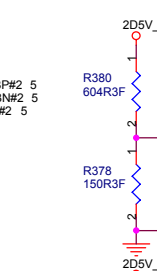
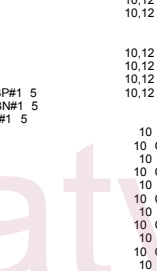
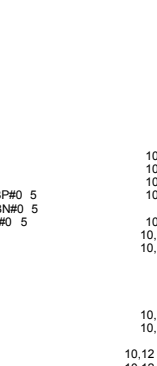
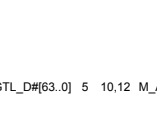
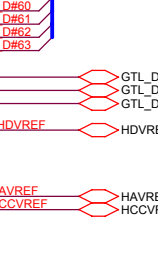
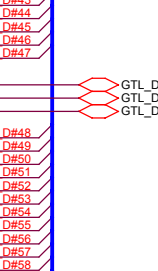
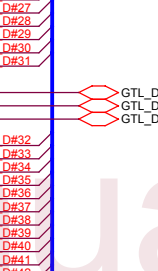
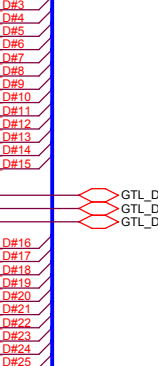
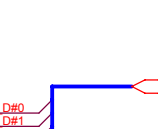
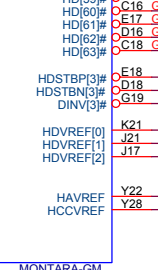
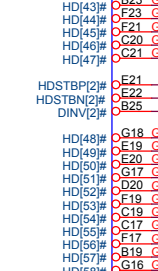
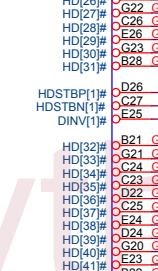
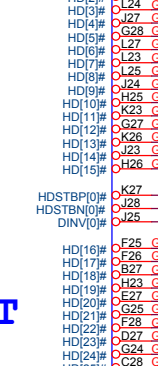
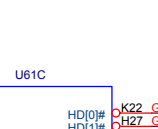
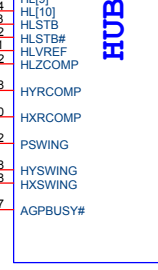
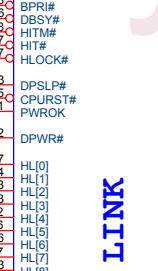
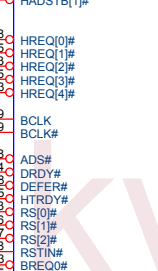
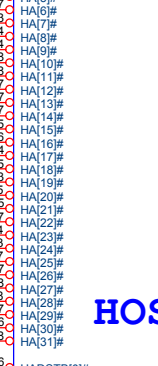
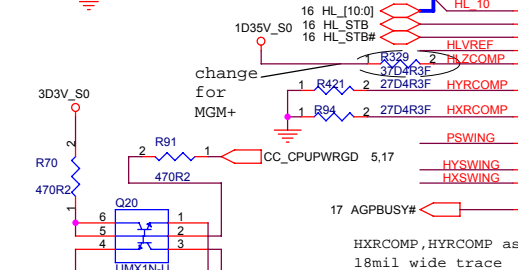
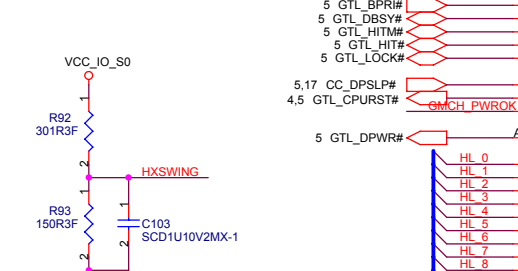
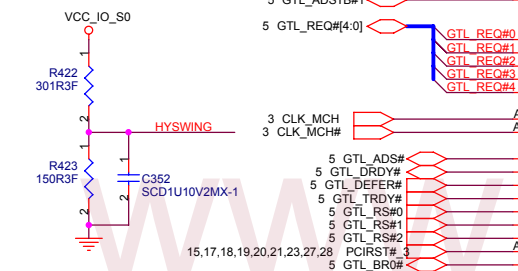
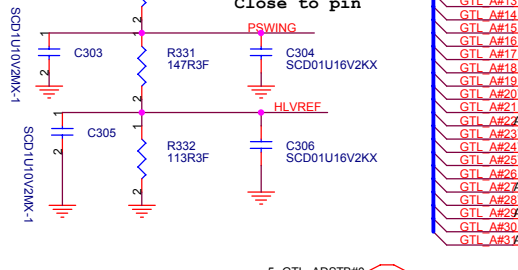
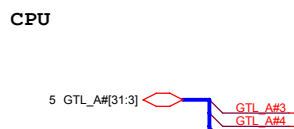
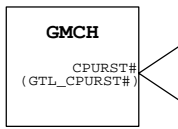


10uF_10V *1 ,0805,X5R 0.1uF_10V *10 ,0402,X7R POSCAP 100uF_4V*1



Place near CPU

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Size A3	Document Number MOLOKAI	Rev SC
Date: Thursday, April 15, 2004	Sheet 6 of 39	

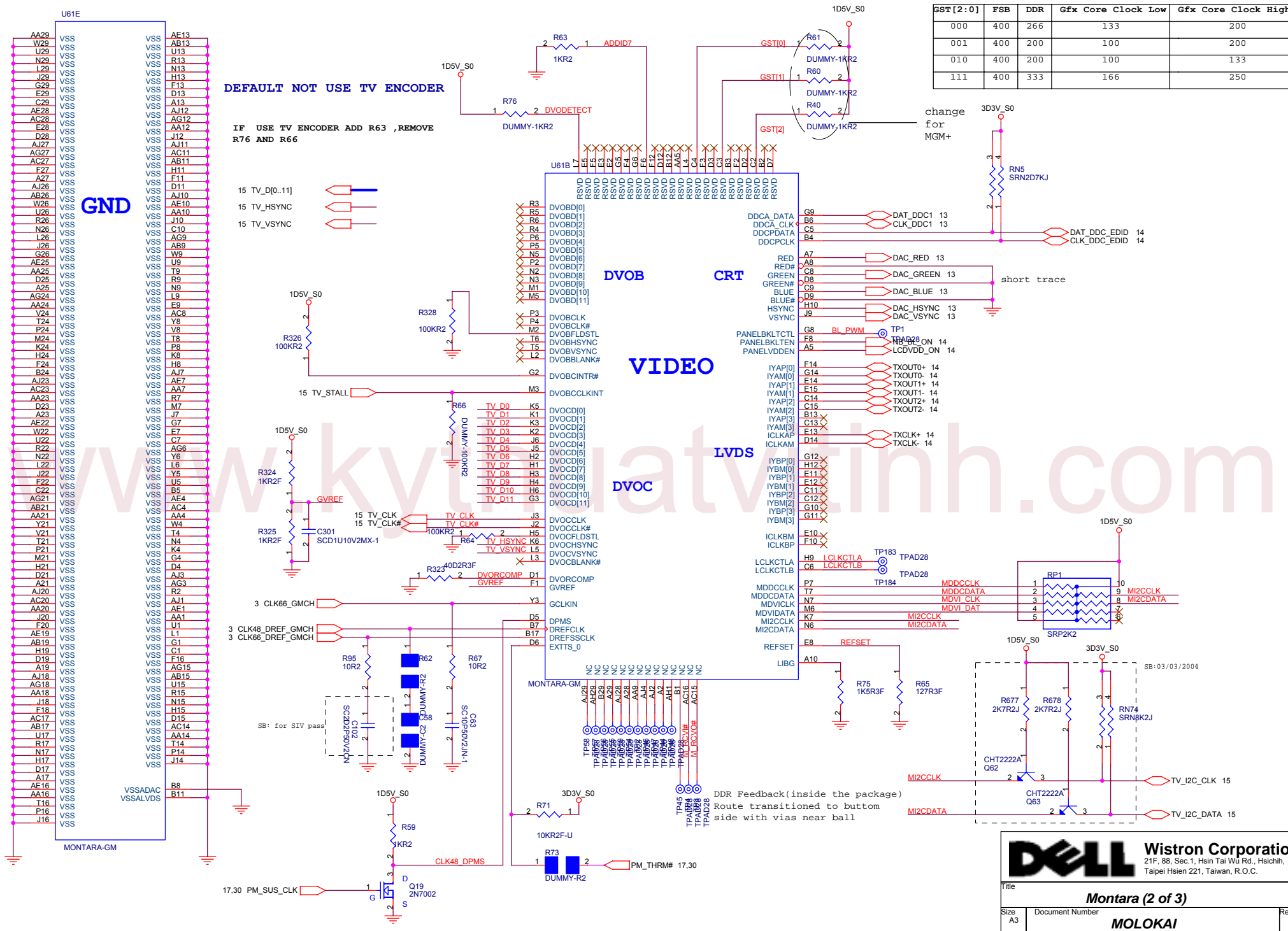


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Title: **Montara (1 of 3)**

Size A3	Document Number	Rev SC
	MOLOKAI	

Date: Thursday, April 15, 2004 Sheet 7 of 39



FOR MGM+ internal pull down

GST[2:0]	FSB	DDR	Gfx Core Clock Low	Gfx Core Clock High
000	400	266	133	200
001	400	200	100	200
010	400	200	100	133
111	400	333	166	250

DEFAULT NOT USE TV ENCODER

IF USE TV ENCODER ADD R63 ,REMOVE R76 AND R66

- 15_TV_D[0..11]
- 15_TV_HSYNC
- 15_TV_VSYNC

VIDEO

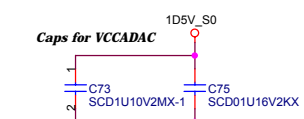
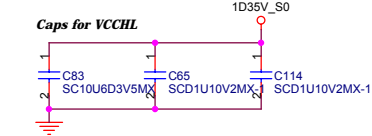
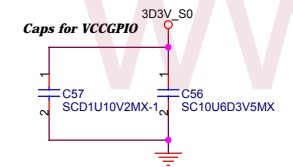
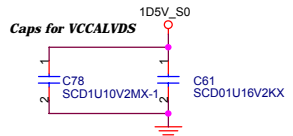
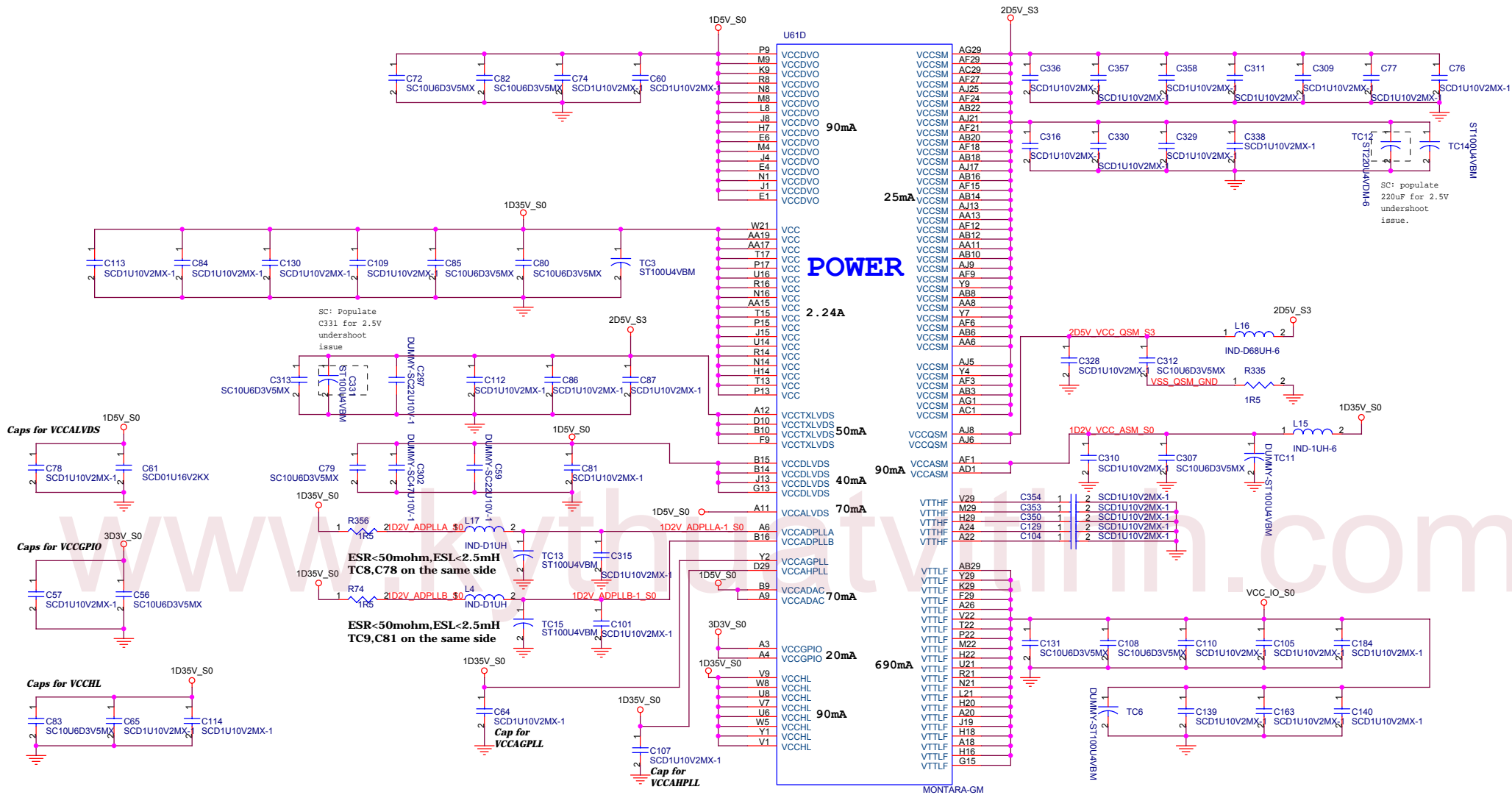
LVDS

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Title: **Montara (2 of 3)**

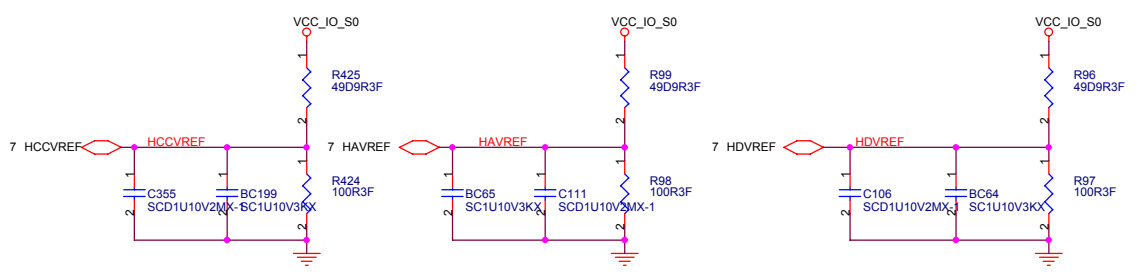
Size: A3 Document Number: **MOLOKAI** Rev: **SC**

Date: Thursday, April 15, 2004 Sheet 8 of 39



This two cap should connect to VSSADAC first then to GND

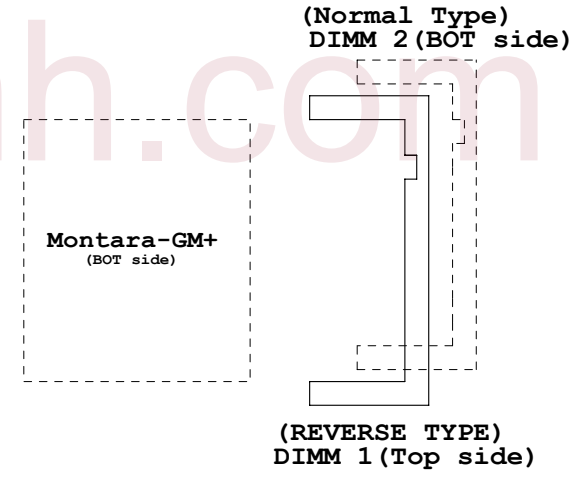
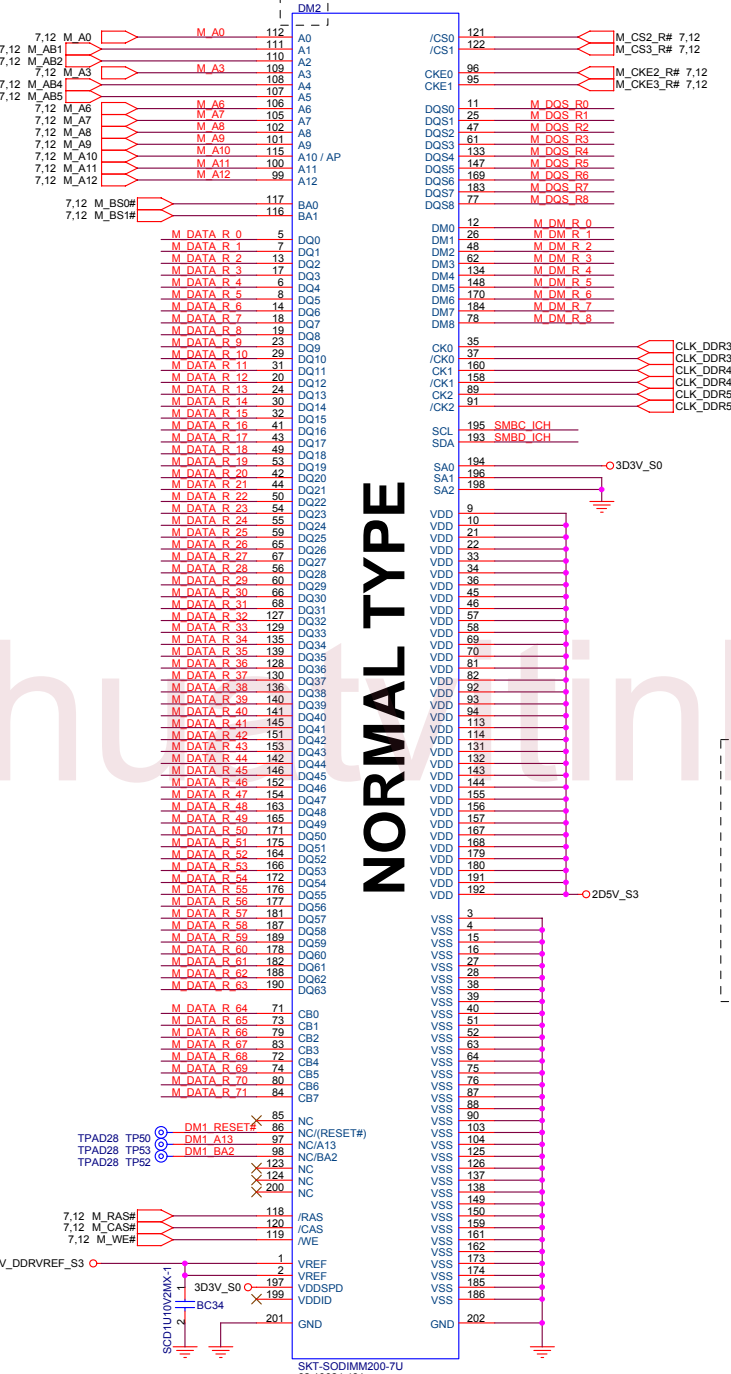
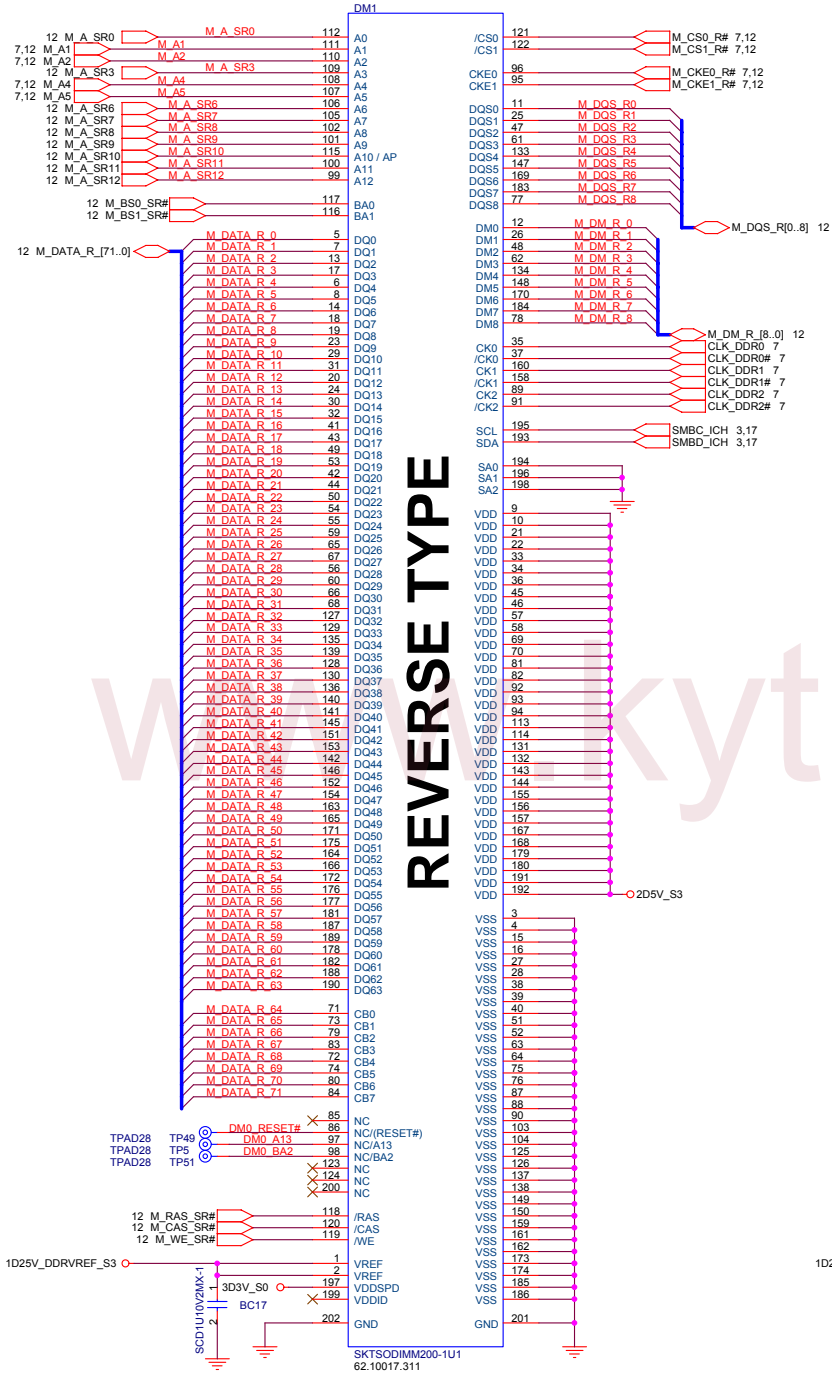
Reference Voltage: 2/3 Vcc_IO_S0



DIMM1

DIMM2

Use old symbol change FN only

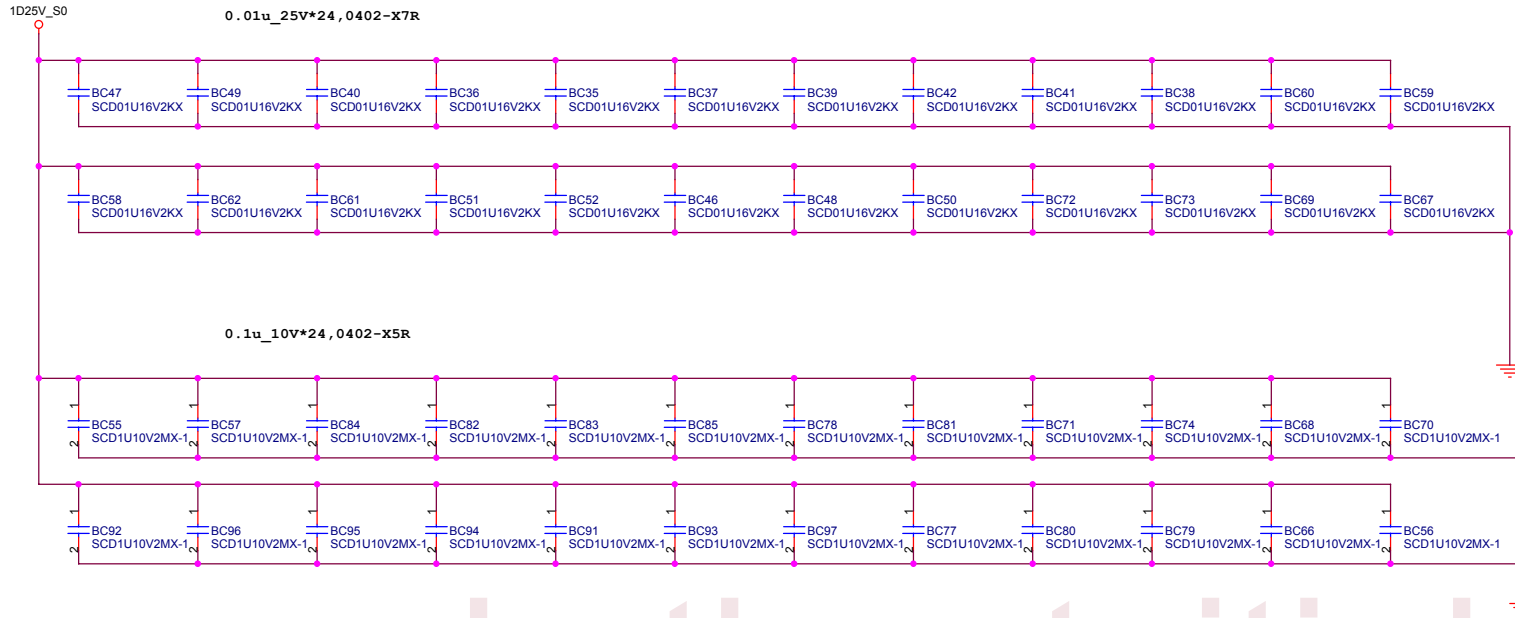


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Taipei Hsien 221, Taiwan, R.O.C.

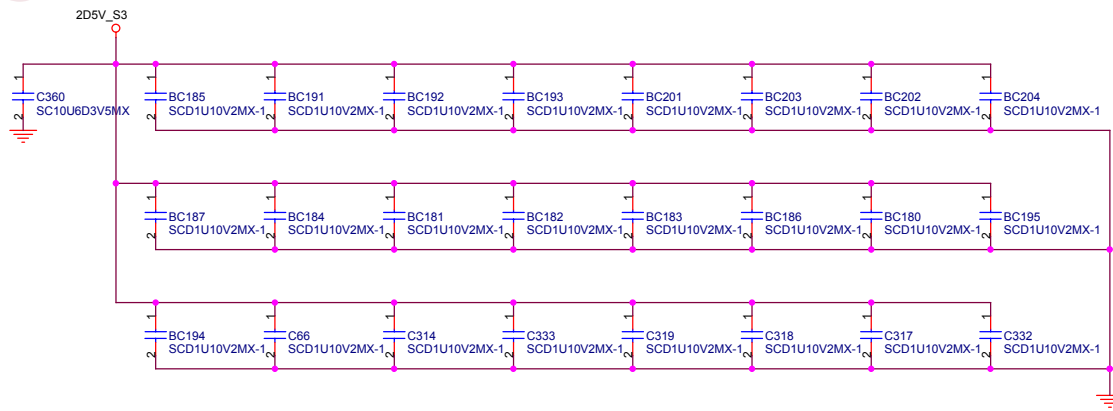
Title: **DDR Socket**

Size: Document Number: **MOLOKA** Rev: **SC**

Date: Thursday, April 15, 2004 Sheet 10 of 39



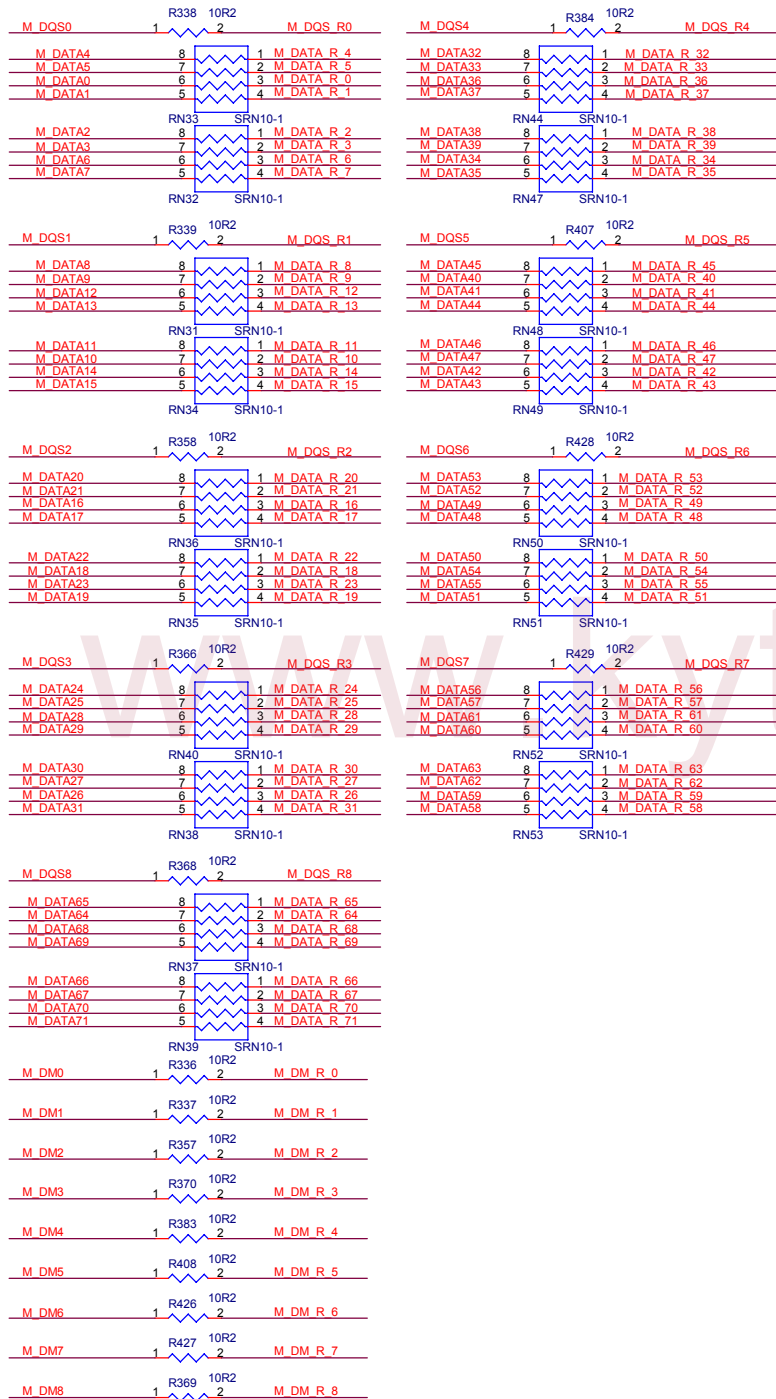
FOR DDR SKTS POWER PIN
 10u_6.3V*1,0805-X5R
 0.1u_10V*24,0402-X5R



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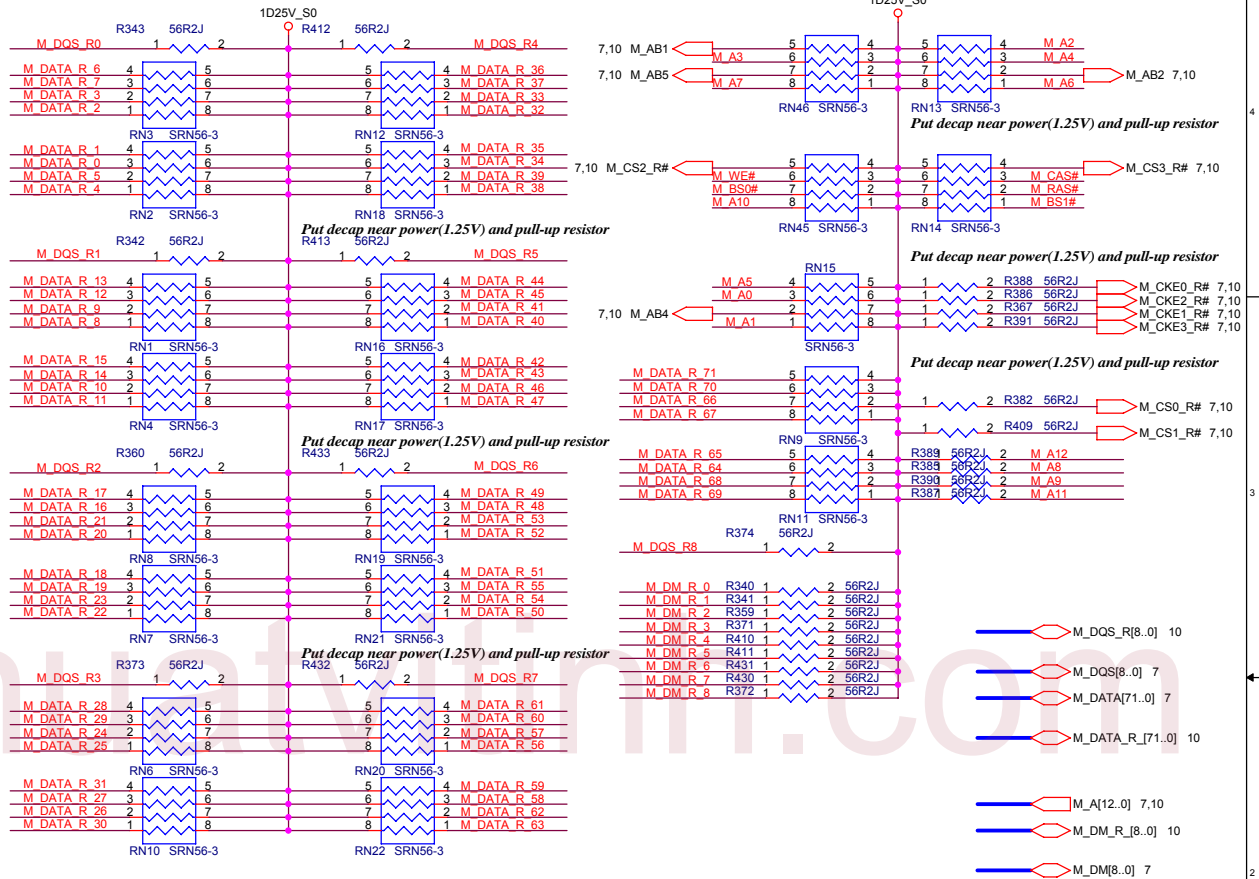
DELL		Wistron Corporation	
		21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
DDR Decoupling CPA			
Size	Document Number	Rev	
A3	MOLOKAI	SC	
Date:	Thursday, April 15, 2004	Sheet	11 of 39

SERIES DAMPING

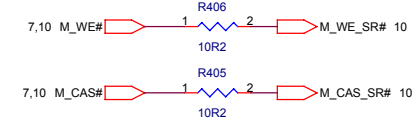


PARALLEL TERMINATION

Put decap near power(1.25V) and pull-up resistor



Command Signals USE Topology 2



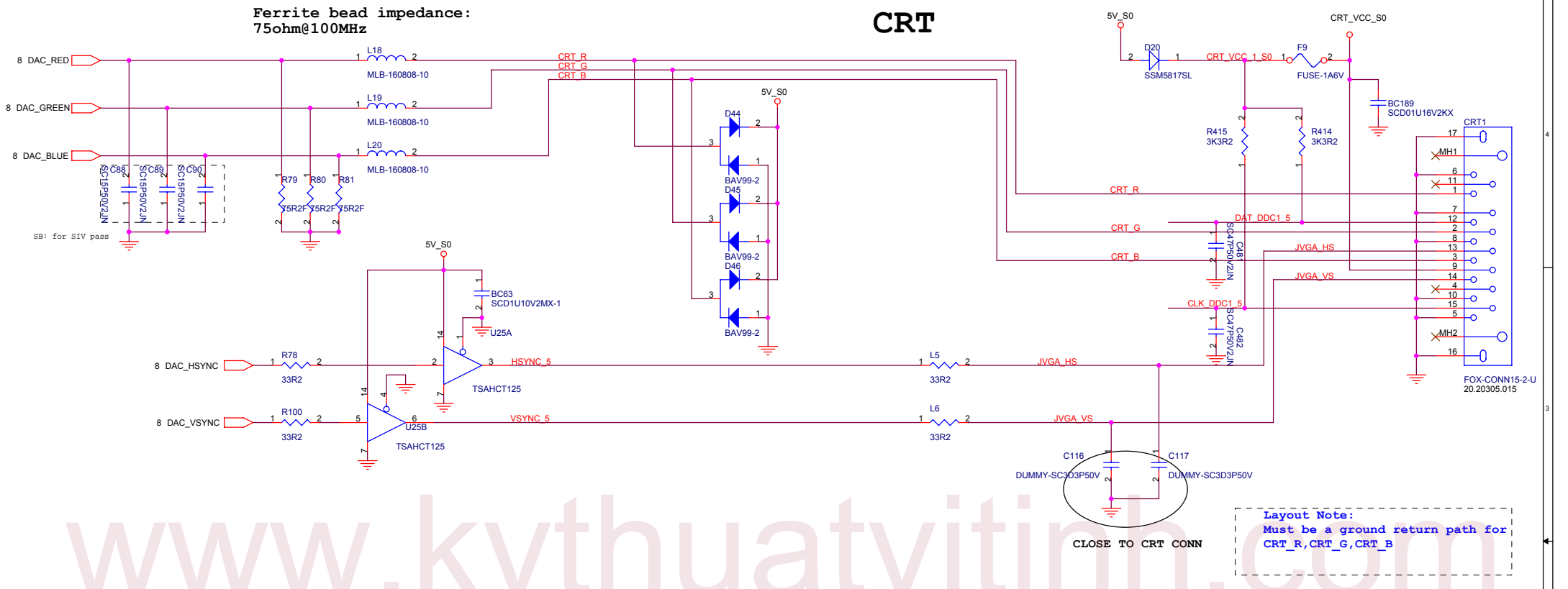
DELL Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title _____
DDR Serial/Terminator Resistor

Size A3 Document Number **MOLOKAI** Rev **SC**
 Date: Thursday, April 15, 2004 Sheet 12 of 39

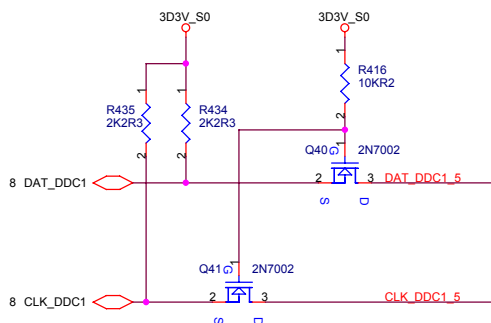
Ferrite bead impedance:
75ohm@100MHz

CRT



Layout Note:
Must be a ground return path for
CRT_R, CRT_G, CRT_B

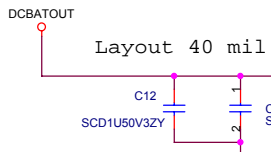
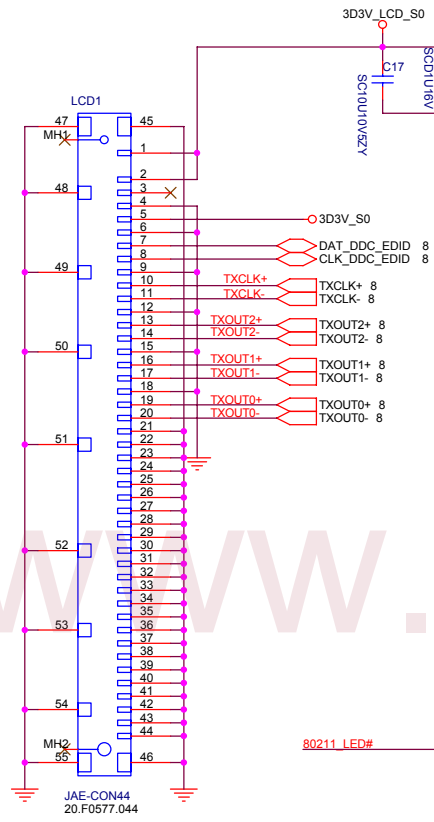
DDC_CLK & DATE LEVEL SHIFT



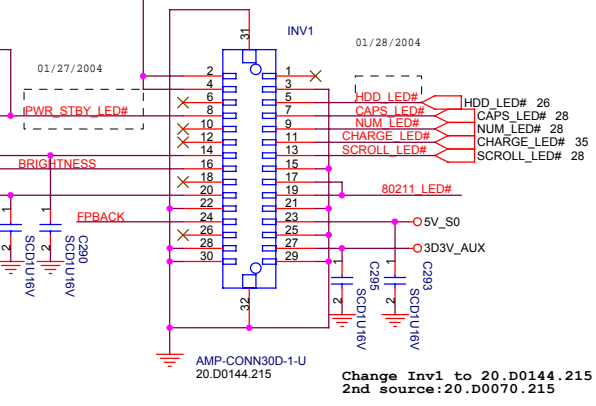
CLOSE TO CRT CONN

DELL		Wistron Corporation	
		21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
CRT CONN.			
Size	Document Number	Rev	
A3	MOLOKAI	SC	
Date:	Thursday, April 15, 2004	Sheet	13 of 39

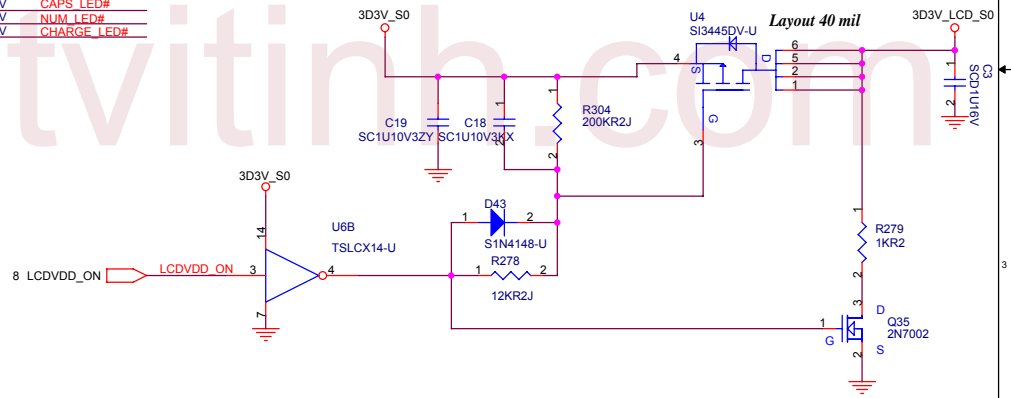
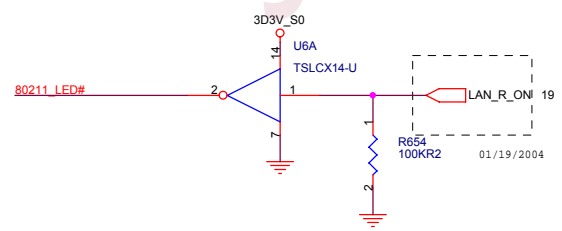
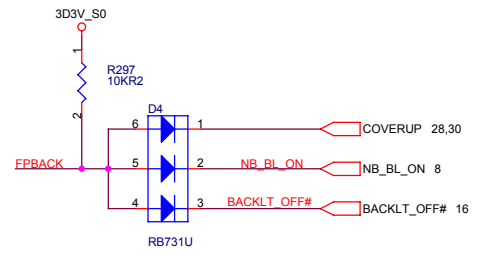
LCD CONN



INVERTER/LED



- C284 SC1000P50V PWR_STBY_LED#
- C286 SC1000P50V 80211_LED#
- C294 SC1000P50V FPBACK
- C291 2 SCD1U16V BRIGHTNESS
- C283 SC1000P50V HDD_LED#
- C285 SC1000P50V CAPS_LED#
- C287 SC1000P50V NUM_LED#
- C289 SC1000P50V CHARGE_LED#



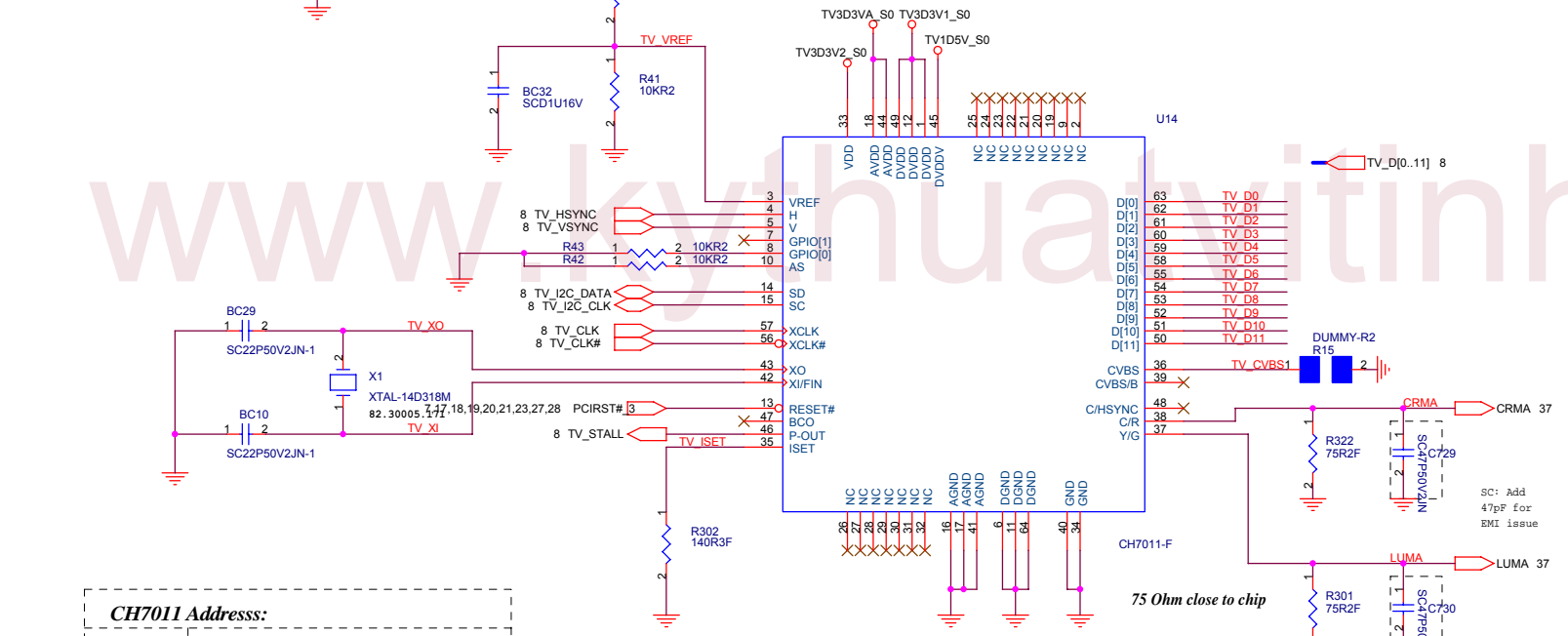
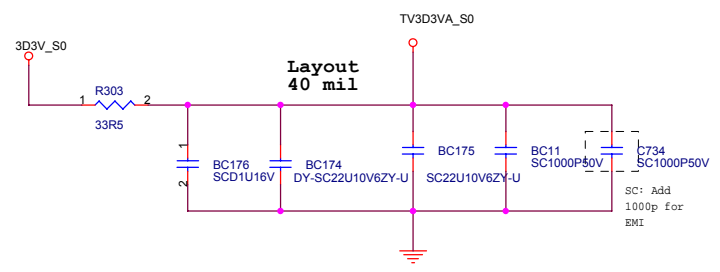
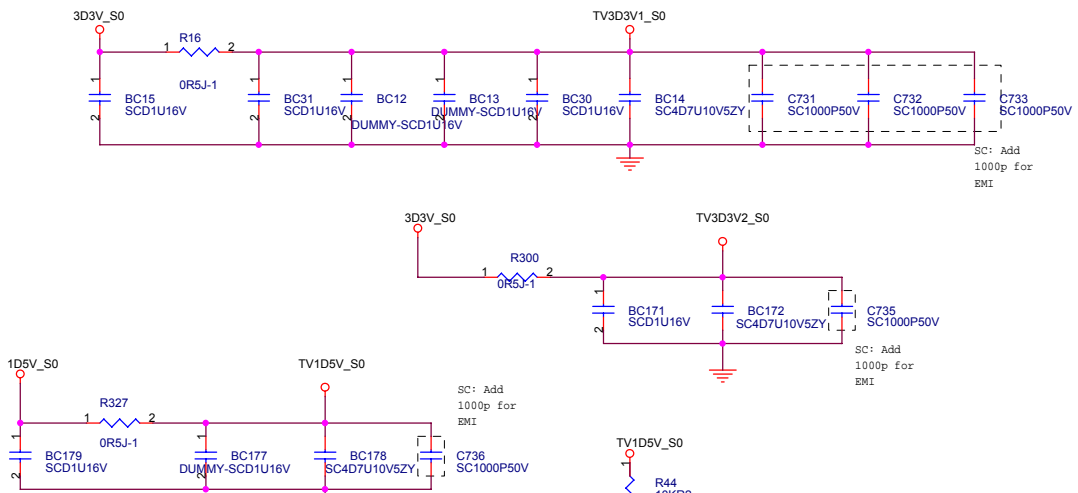
	S0/S1	S3	S4	S5	Functions	when LID is closed
Power On / Battery Low LED (PWR_LED#)	LOW	HIGH	HIGH	HIGH		readable
Sleep / Waking LED (STDBY_LED#)	HIGH	LOW	HIGH	HIGH	(Don't flash during waking)	readable
Disk Media (MEDIA_LED#)					HDD,ODD access indicator	not readable
Charging LED (CHARGE_LED#)					On when charging. Flashing when charging error is occurred.	not readable
Wireless LED (80211_LED#)					On when wireless is On	not readable
NUM Lock (NUM_LED#)					On when Number key is locked	not readable
CAPS Lock (MEDIA_LED#)					On when Caps lock is On	not readable

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Title: **LCD CONN & INVERTER**

Size: A3 Document Number: **MOLOKAI** Rev: **SC**

Date: Thursday, April 15, 2004 Sheet 14 of 39

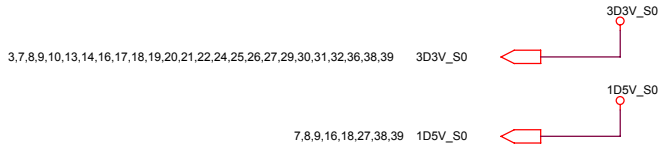


CH7011 Address:

0X75	AS pull-up	(int. pull-up)
0X76	AS pull-down	

Power up default:

NTSC	GPIO0 pull-down
PAL	GPIO0 pull-up (int. pull-up)

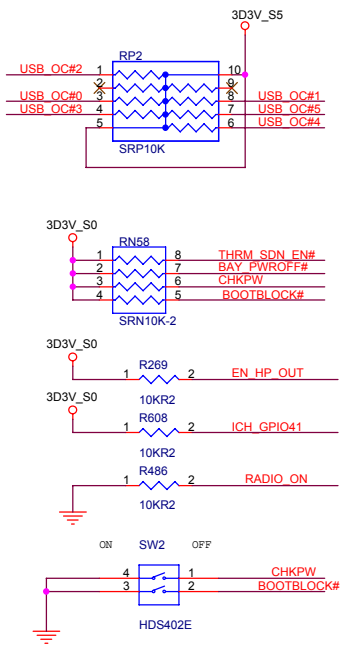


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 Taipei Hsien 221, Taiwan, R.O.C.

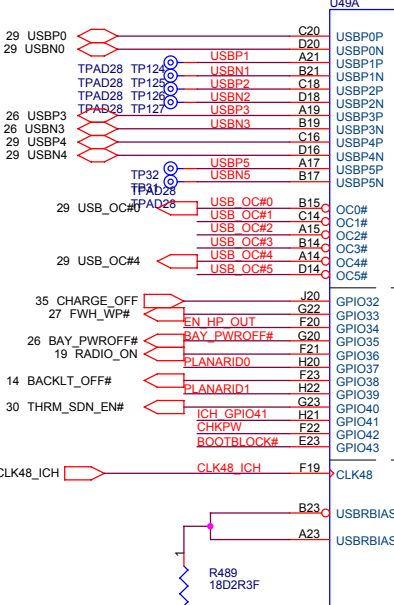
Title: **TV_ENCODER**

Size A3	Document Number	Rev SC
MOLOKAI		

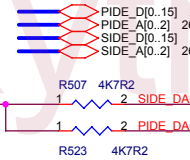
Date: Thursday, April 15, 2004 Sheet 15 of 39



	SW1-4	SW2-3
CHKPW ENABLE	ON	X
BOOTBLOCK ENABLE	X	ON



Place R220 near S/B

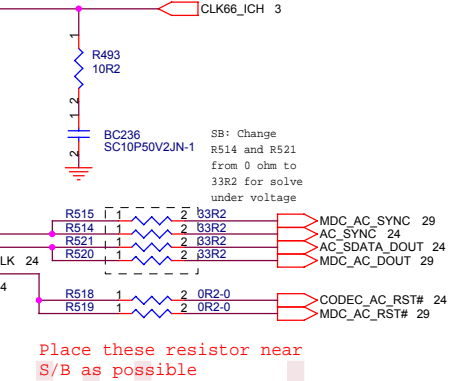
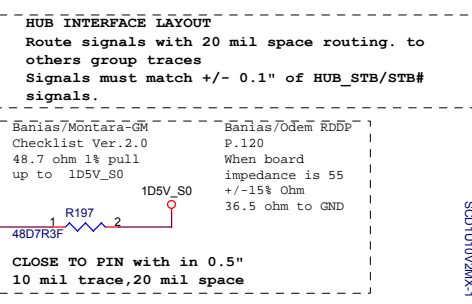
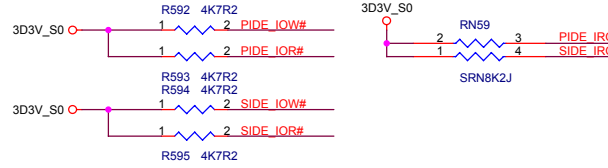


ICH4 Integrated Pull-up and Pull-down Resistors

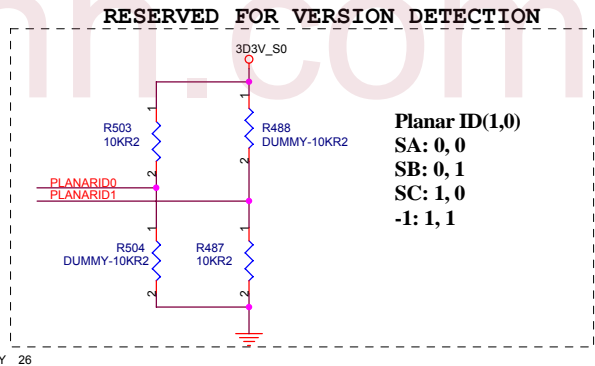
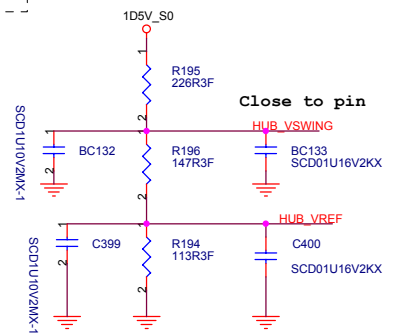
EE_DIN, EE_DOUT, PME#, PWRBTN#	ICH4 internal 20K pull-ups
GNT[B:A]#/GNT[5]#/GPIO[17:16], LAD[3:0]#/FWH[3:0]#, LDRQ[1:0],	
LAN_RXD[2:0]	ICH4 internal 10K pull-ups
AC_BITCLK, AC_RST#, AC_SDIN[2:0], AC_SDOUT, AC_SYNC, DPRSLPVR, SPKR	ICH4 internal 20K pull-downs
USB[5:0][P,N]	ICH4 internal 15K pull-downs
PDD[7]/SDD[7], PDDREQ/SDDREQ	ICH4 internal 11.5K pull-downs
LANCLK	ICH4 internal 100K pull-downs

ICH4 IDE Integrated Series Termination Resistors

PDD[15:0], SDD[15:0], PDIOW#, SDIOW#, PDIOR#, PDIOW#, PDREQ, SDREQ, PDDACK#, SDDACK#, PIORDY, SIORDY, PDA[2:0], SDA[2:0], PDCS1#, SDCS1#, PDCS3#, SDCS3#, IRQ14, IRQ15,	approximately 33 ohm
---	----------------------



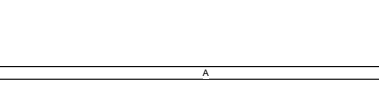
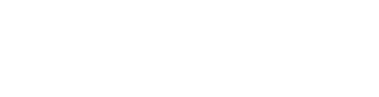
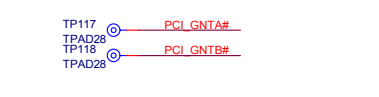
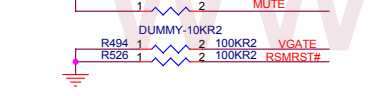
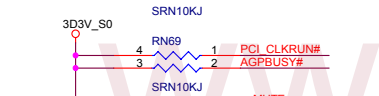
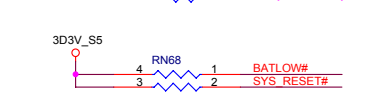
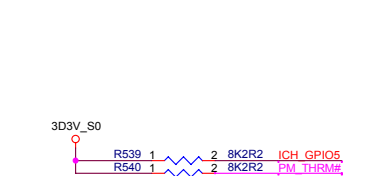
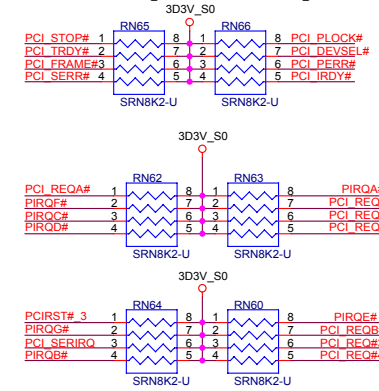
Place these resistor near S/B as possible



Planar ID(1,0)
SA: 0, 0
SB: 0, 1
SC: 1, 0
-1: 1, 1

DELL			Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title				
ICM4-M (1 of 3)				
Size A3	Document Number			Rev SC
Date: Thursday, April 15, 2004				

PCI/Interrupt I/F Pullups

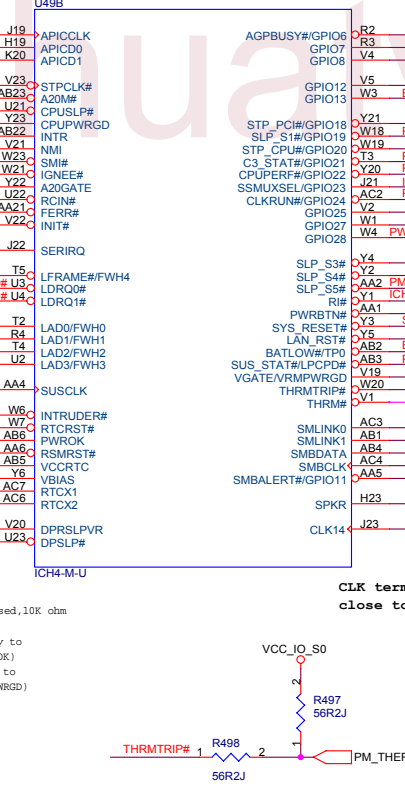


Should go high no sooner than 10mS after both +3V3RUN and +1.5VVRUN have reach their nominal voltage

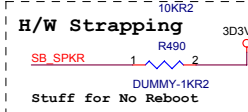
Should go high no sooner than 10mS after both +3V3SUS and +1.5VSUS have reach their nominal voltage

If ICH-4 LAN not used, 10K ohm pd or connect directly to ---RSMRST#(SUSPWROK) But in Bon connect to PWROK(Delay_IMP_PWROK)

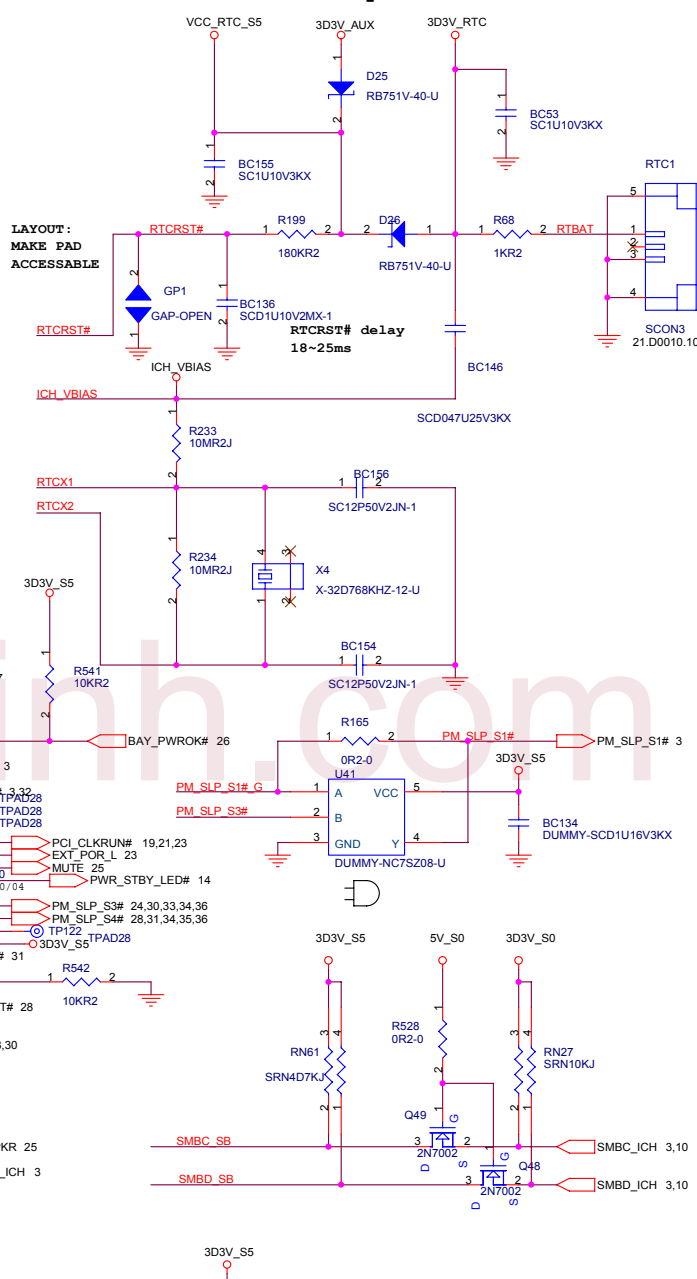
BIOS NOTE:
BIOS should disable PM_STPCPU# on CK_Titan.
(Use H_DPSLP# instead)



CLK termination close to ICH4



RTC Circuitry



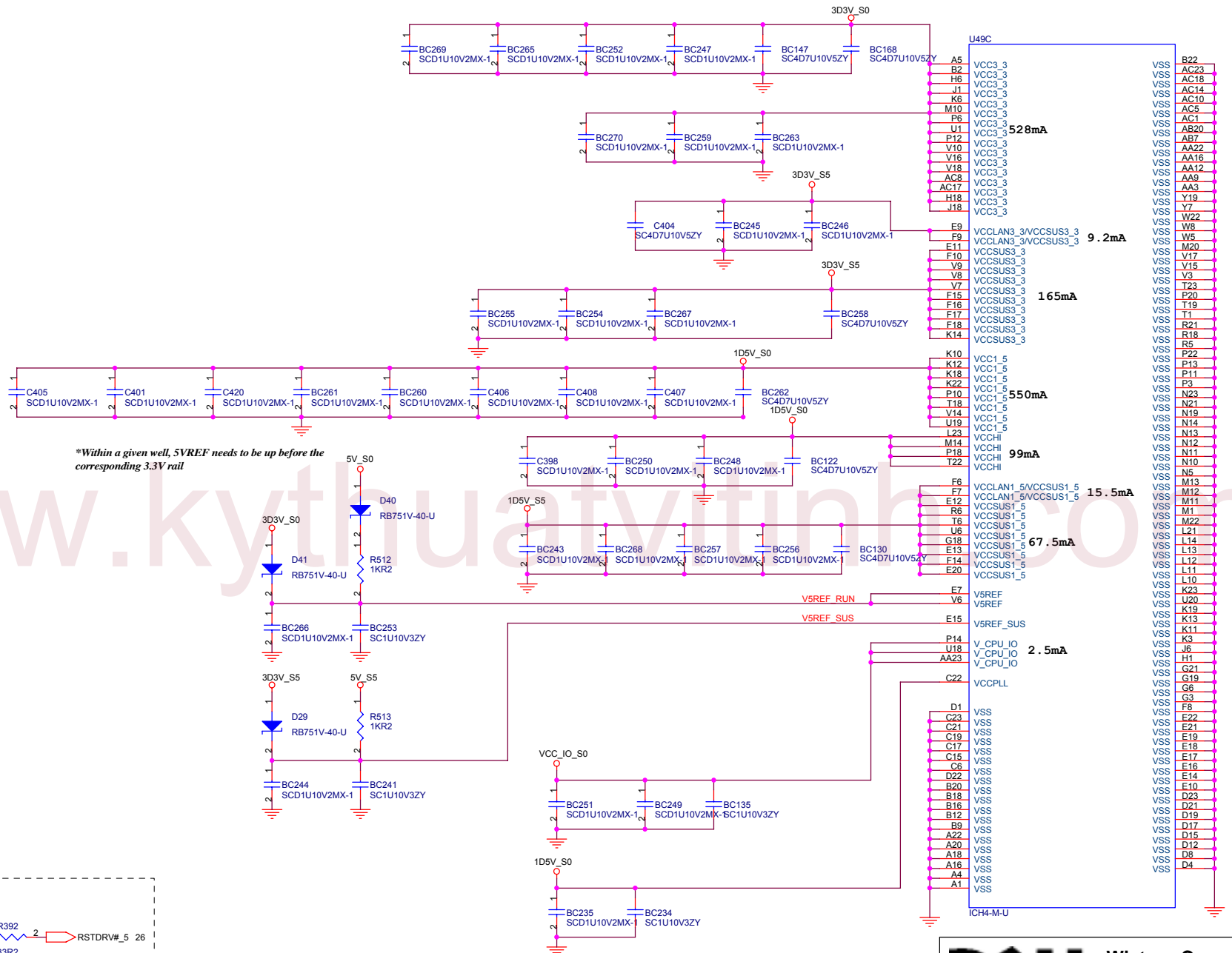
LAYOUT: MAKE PAD ACCESSABLE

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File: **ICH4-M (2 of 3)**

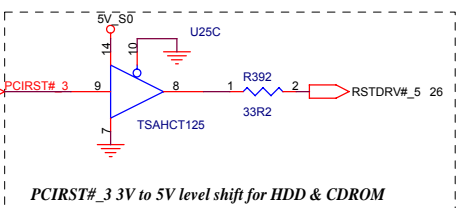
Size	Document Number	Rev
Custpm	MOLOKAI	SC

Date: Thursday, April 15, 2004 Sheet 17 of 39



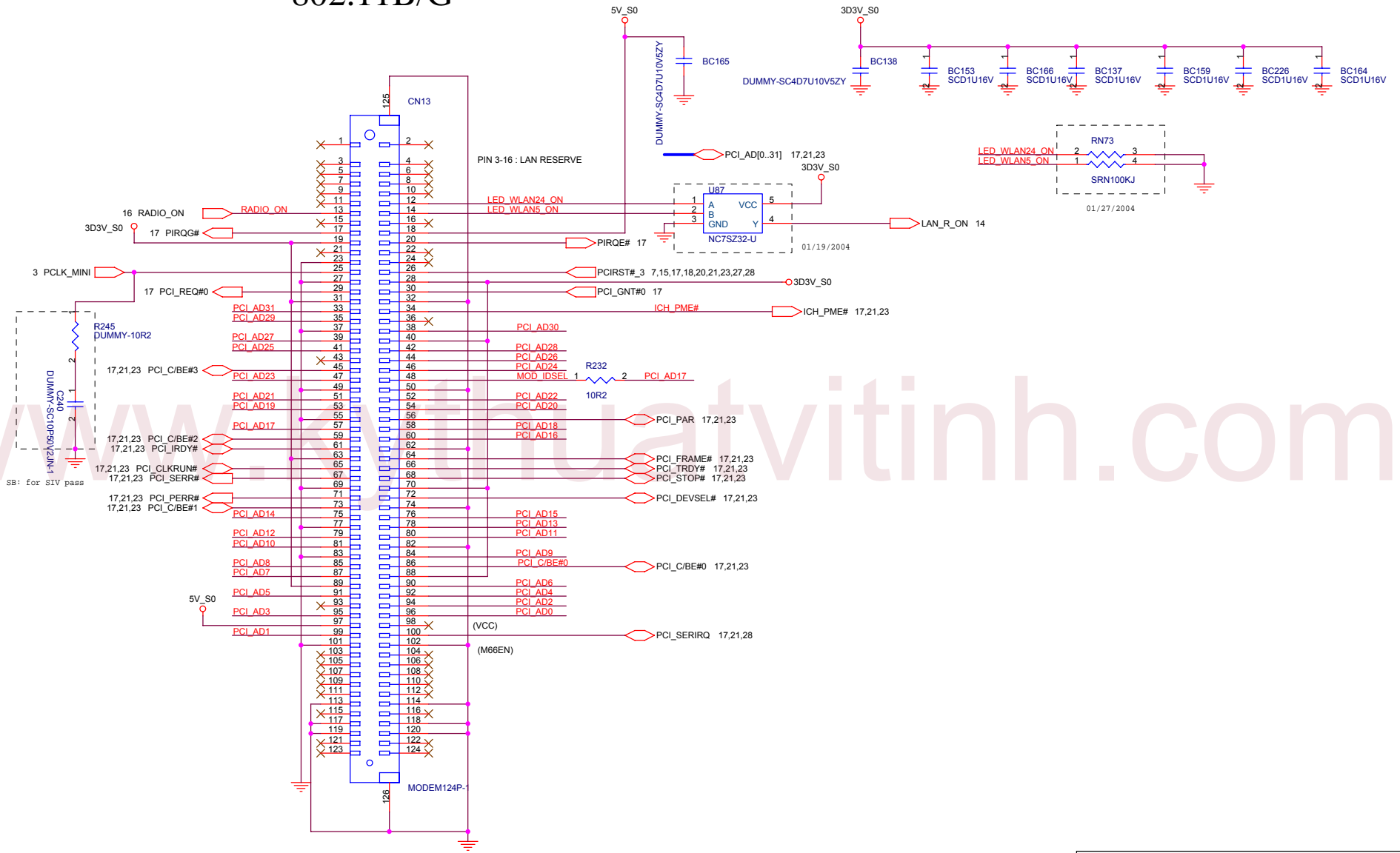
A5	VCC3_3	B22	VSS
B2	VCC3_3	AC23	VSS
H6	VCC3_3	AC18	VSS
J1	VCC3_3	AC14	VSS
K6	VCC3_3	AC10	VSS
M10	VCC3_3	AC5	VSS
P6	VCC3_3	AC1	VSS
U1	VCC3_3	AB20	VSS
P12	VCC3_3	AB7	VSS
V10	VCC3_3	AA22	VSS
V16	VCC3_3	AA16	VSS
V18	VCC3_3	AA12	VSS
AC8	VCC3_3	AA9	VSS
AC17	VCC3_3	AA3	VSS
H18	VCC3_3	Y19	VSS
J18	VCC3_3	Y7	VSS
E9	VCCLAN3_3VCCSUS3_3	W22	VSS
F9	VCCLAN3_3VCCSUS3_3	W8	VSS
E11	VCCSUS3_3	W5	VSS
F10	VCCSUS3_3	M20	VSS
V9	VCCSUS3_3	V17	VSS
V8	VCCSUS3_3	V15	VSS
V7	VCCSUS3_3	V3	VSS
F15	VCCSUS3_3	T23	VSS
F16	VCCSUS3_3	P20	VSS
F17	VCCSUS3_3	T19	VSS
F18	VCCSUS3_3	T1	VSS
K14	VCCSUS3_3	R21	VSS
K10	VCC1_5	R18	VSS
K12	VCC1_5	R5	VSS
K18	VCC1_5	P22	VSS
K22	VCC1_5	P13	VSS
P10	VCC1_5	P3	VSS
T18	VCC1_5	N23	VSS
V14	VCC1_5	N21	VSS
U19	VCC1_5	N19	VSS
L23	VCCCHI	N14	VSS
M14	VCCCHI	N13	VSS
P18	VCCCHI	N12	VSS
T22	VCCCHI	N11	VSS
F6	VCCLAN1_5VCCSUS1_5	N10	VSS
E12	VCCLAN1_5VCCSUS1_5	N5	VSS
R6	VCCSUS1_5	M13	VSS
T6	VCCSUS1_5	M12	VSS
U6	VCCSUS1_5	M11	VSS
G18	VCCSUS1_5	M1	VSS
E13	VCCSUS1_5	M22	VSS
F14	VCCSUS1_5	L21	VSS
E20	VCCSUS1_5	L14	VSS
E7	V5REF	L13	VSS
V6	V5REF	L12	VSS
E15	V5REF_SUS	L11	VSS
P14	V_CPU_IO	L10	VSS
U8	V_CPU_IO	K23	VSS
AA23	V_CPU_IO	U20	VSS
C22	VCCPLL	K19	VSS
D1	VSS	K13	VSS
C23	VSS	K11	VSS
C21	VSS	K3	VSS
C19	VSS	H1	VSS
C17	VSS	J6	VSS
C15	VSS	G21	VSS
C6	VSS	G19	VSS
D22	VSS	G6	VSS
B20	VSS	G3	VSS
B18	VSS	F8	VSS
B16	VSS	E22	VSS
B12	VSS	E21	VSS
B9	VSS	E19	VSS
A22	VSS	E18	VSS
A20	VSS	E17	VSS
A18	VSS	E16	VSS
A16	VSS	E14	VSS
A4	VSS	E10	VSS
A1	VSS	D23	VSS
		D21	VSS
		D19	VSS
		D17	VSS
		D15	VSS
		D12	VSS
		D8	VSS
		D4	VSS

*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail



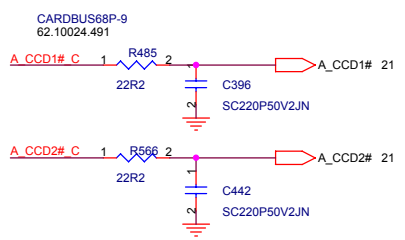
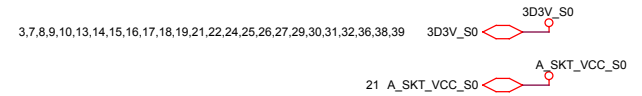
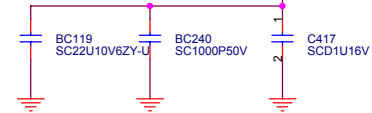
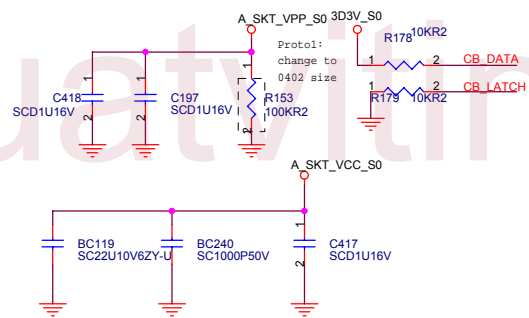
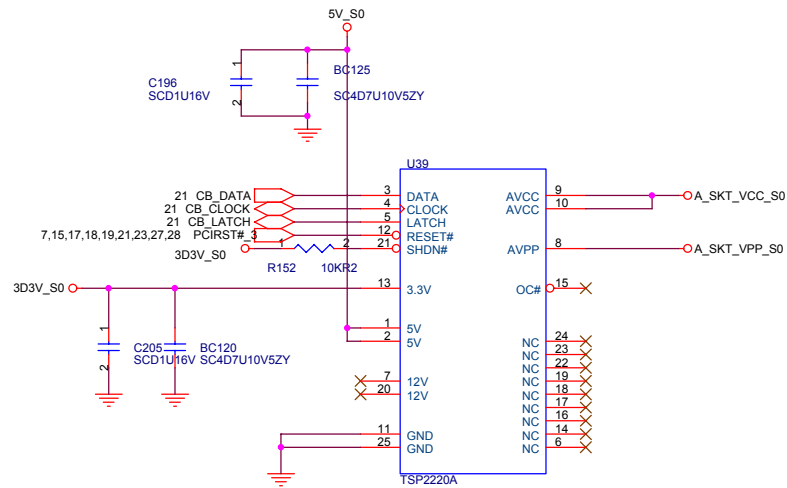
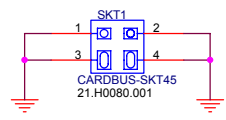
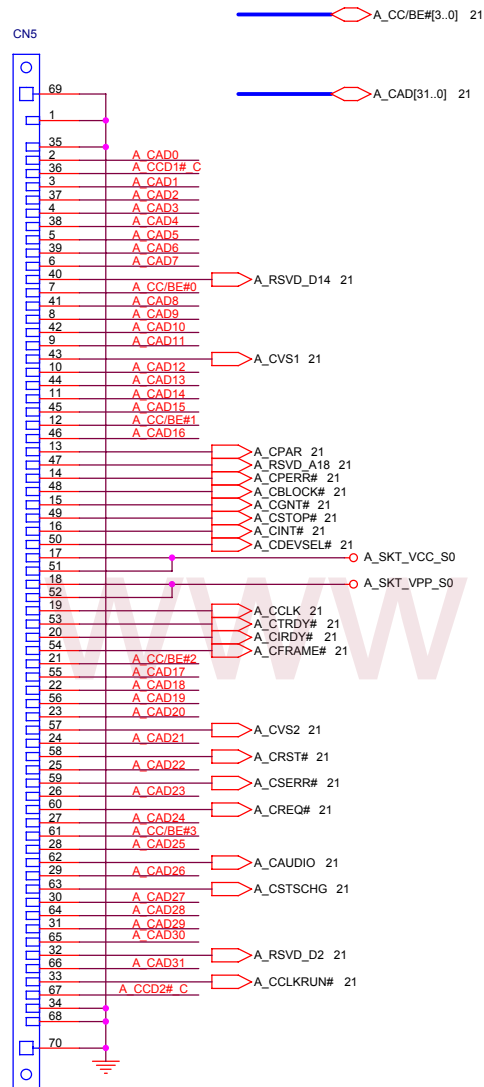
PCIRST#_3 3V to 5V level shift for HDD & CDROM

Mini PCI 802.11B/G

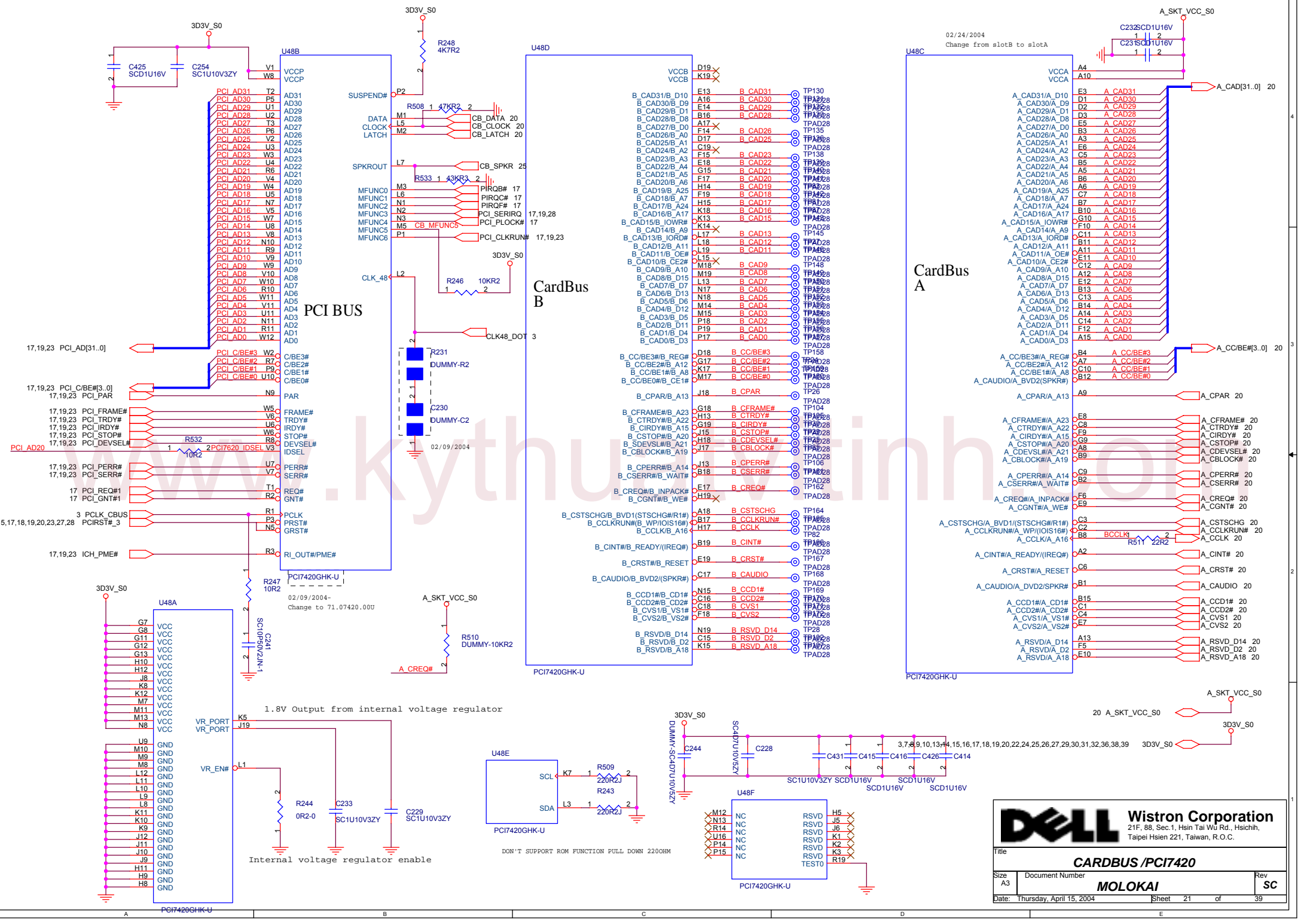


		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
		Title Mini PCI Socket	
Size A3	Document Number MOLOKAI	Rev SC	
Date: Thursday, April 15, 2004		Sheet 19 of 39	

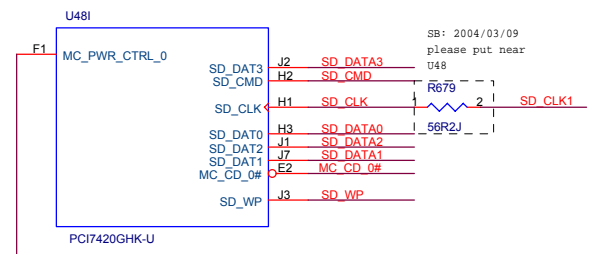
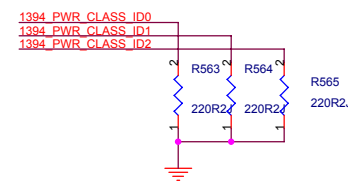
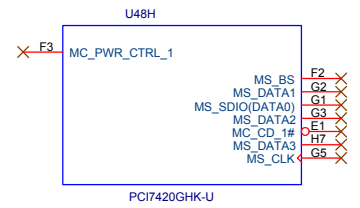
PCMCIA socket



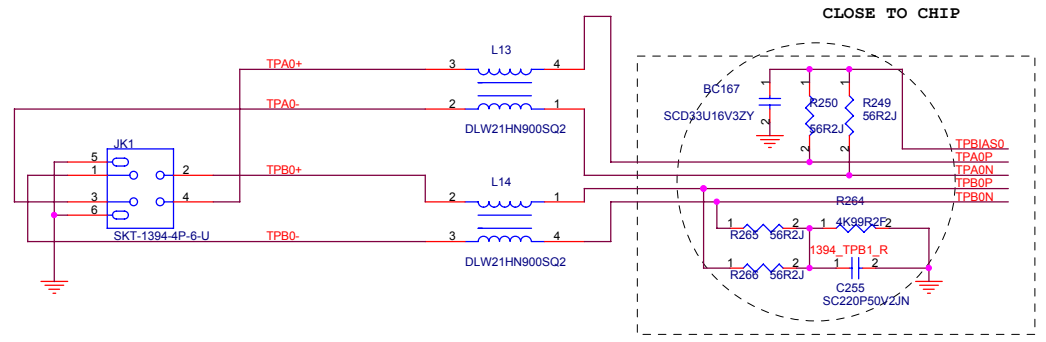
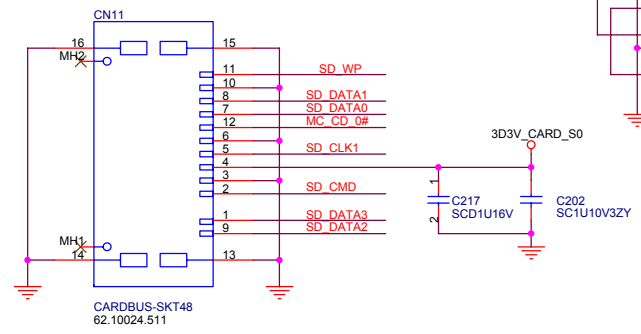
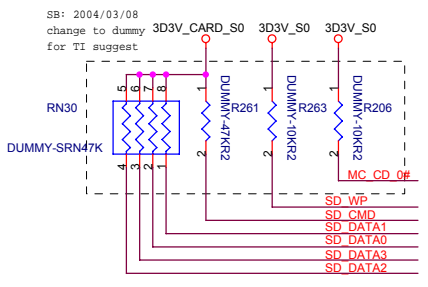
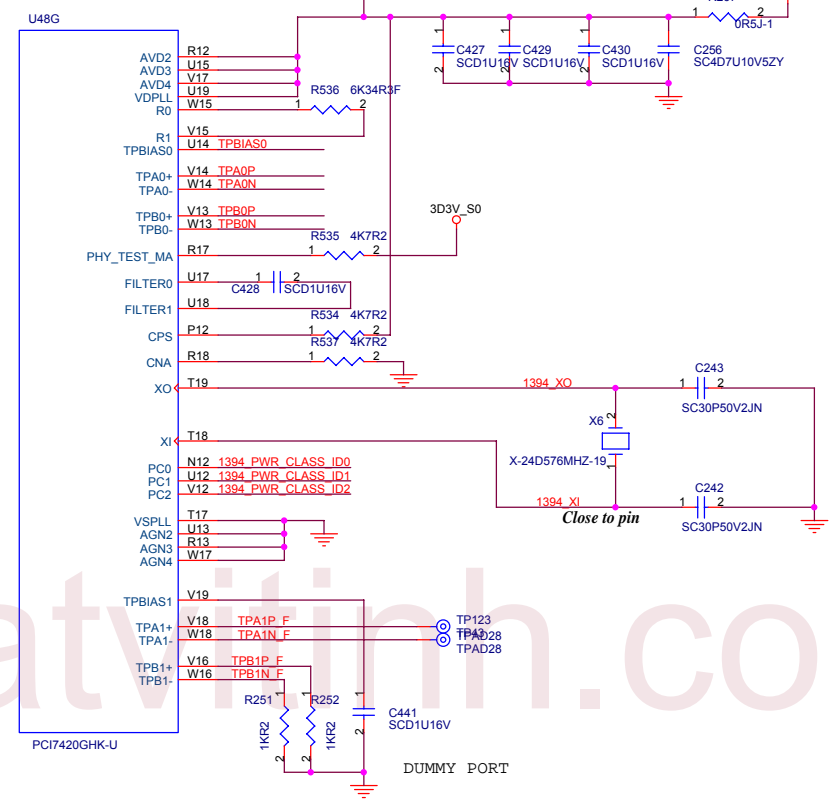
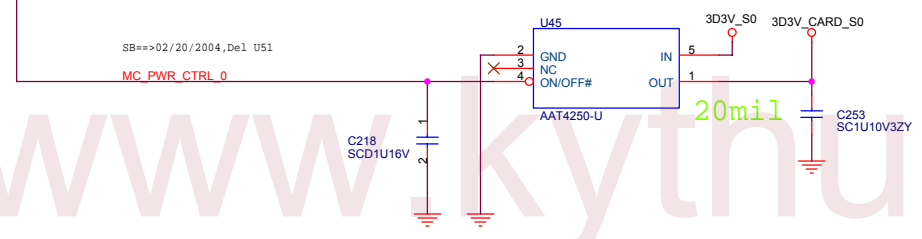
DELL Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: CARDBUS CONN / PWR SW	
Size: A3	Document Number: MOLOKAI
Date: Wednesday, April 14, 2004	Sheet 20 of 39



Title		CARBUS/PCI7420	
Size	Document Number	Rev	
A3	MOLOKAI	SC	
Date:	Thursday, April 15, 2004	Sheet	21 of 39



For SD/MS Card Power



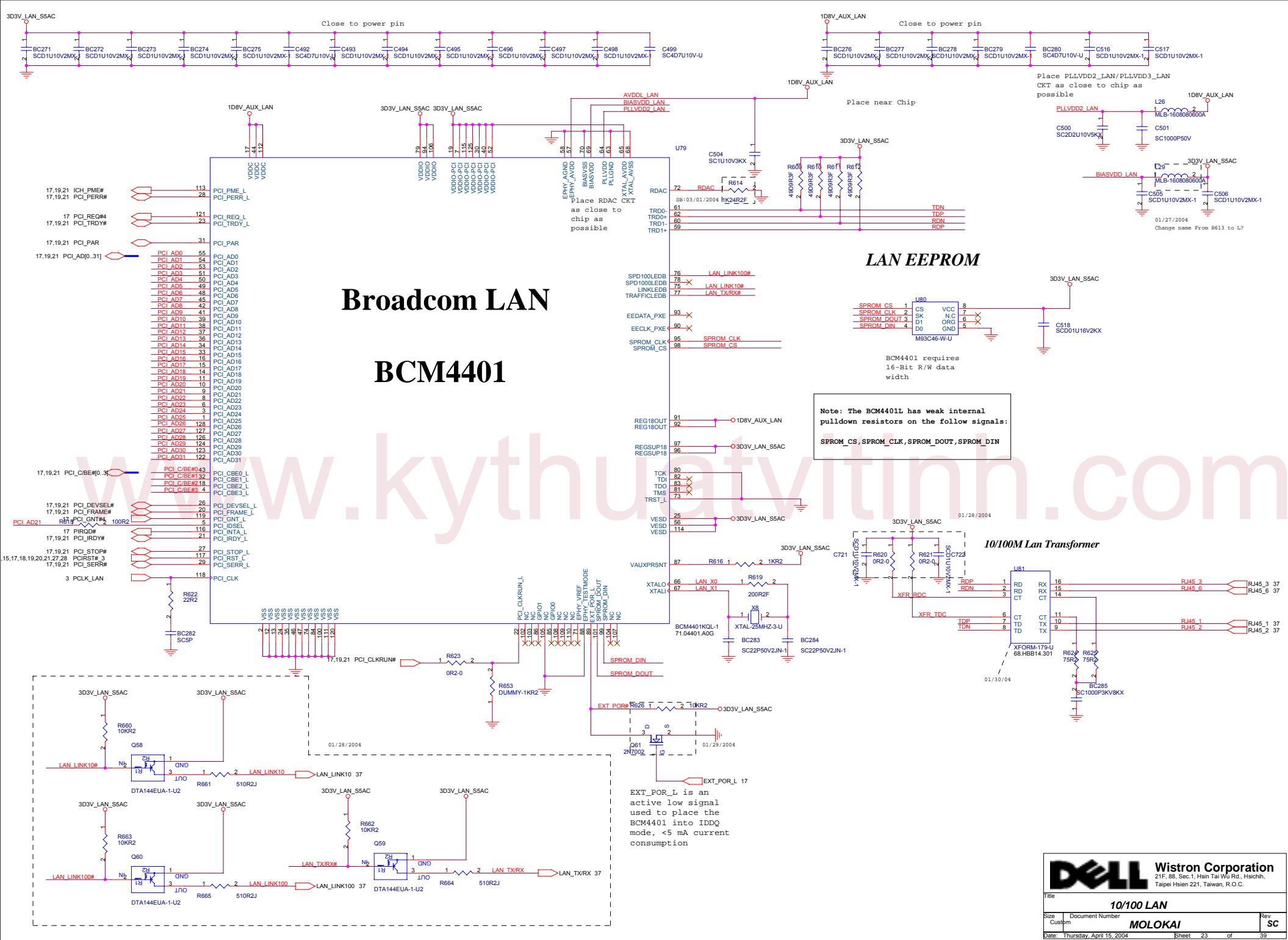
DELL Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **SD/MS CARD READER AND 1394**

Size A3	Document Number	Rev
	MOLOKAI	SC

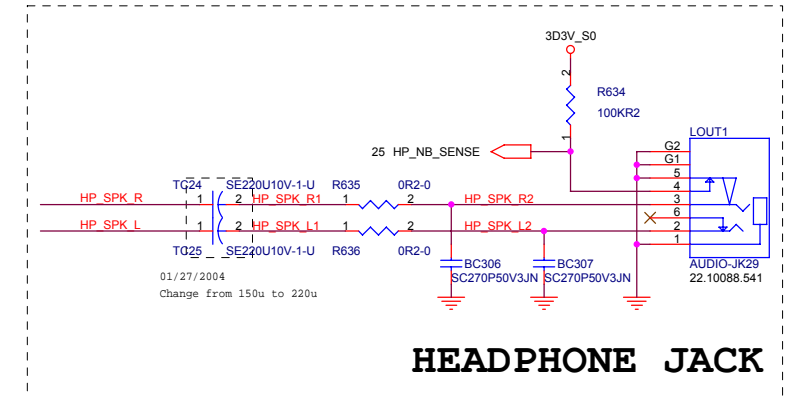
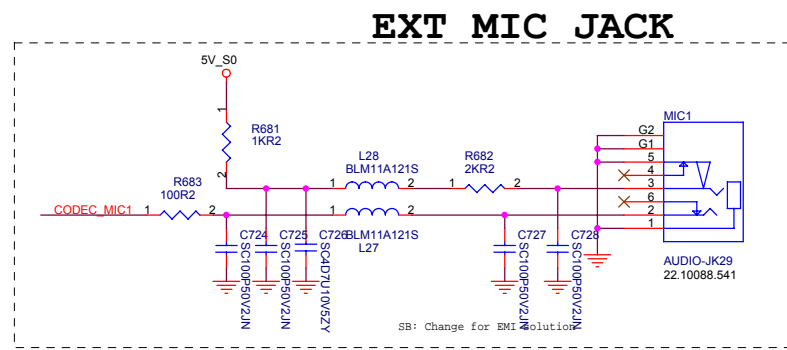
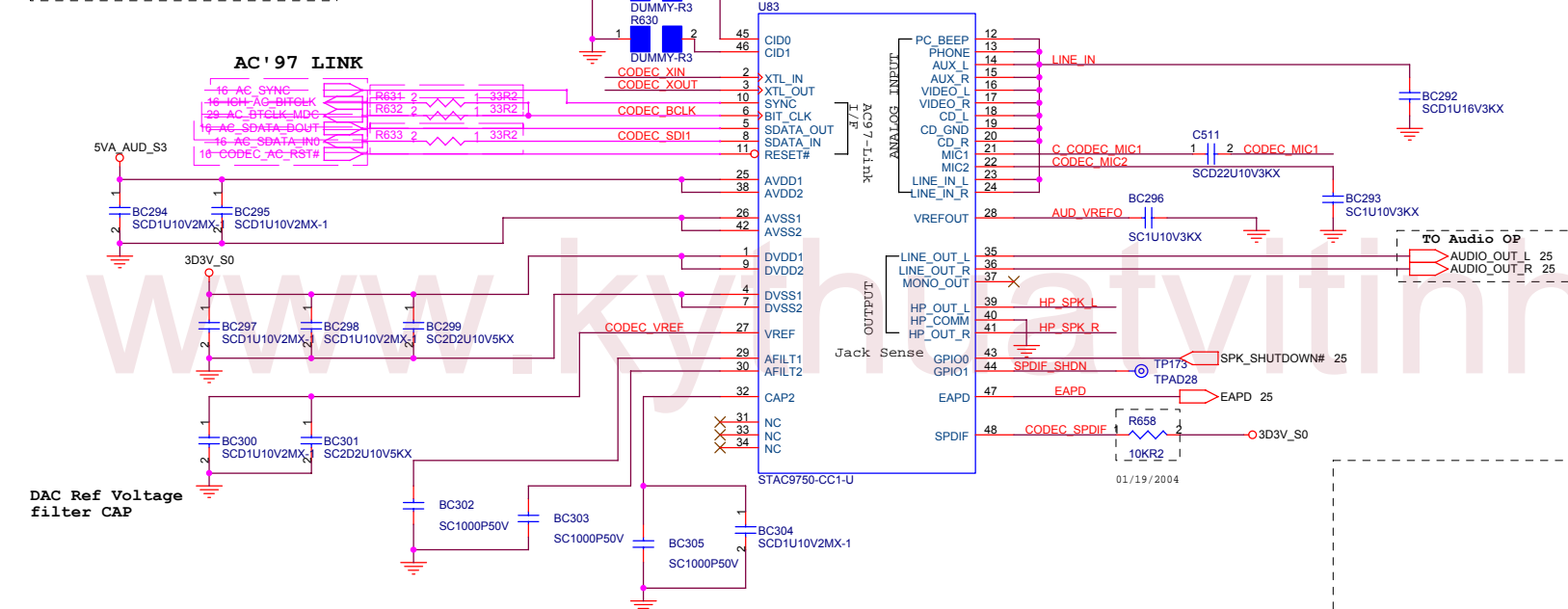
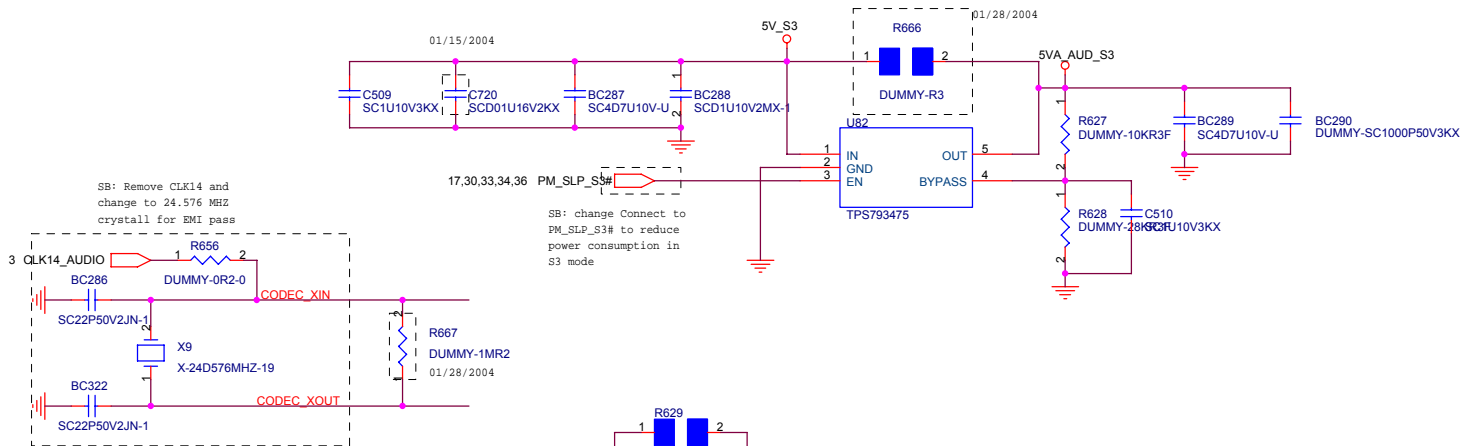
Date: Thursday, April 15, 2004 Sheet 22 of 39

Broadcom LAN BCM4401



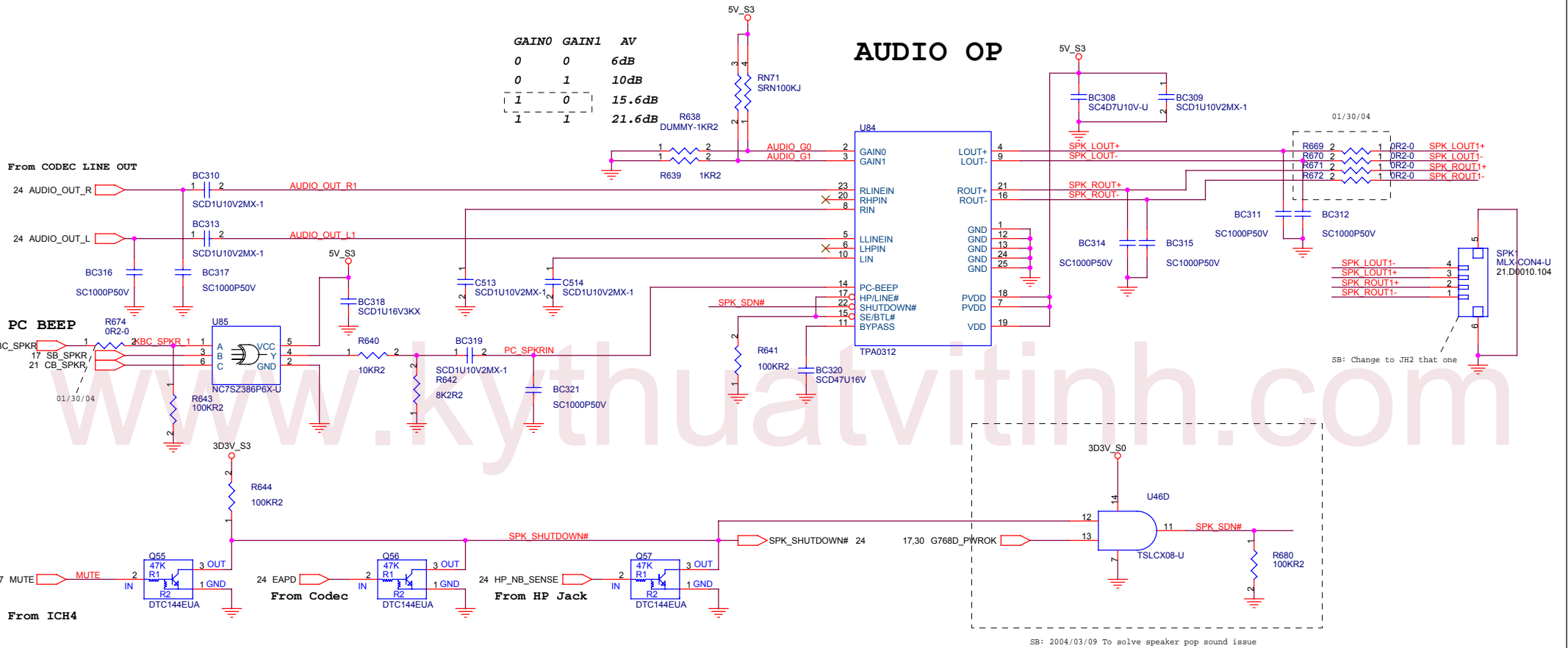
Note: The BCM4401L has weak internal pulldown resistors on the follow signals:
SPROM_CS, SPROM_CLK, SPROM_DOUT, SPROM_DIN

EXT_POR_L is an active low signal used to place the BCM4401 into IDDQ mode, <5 mA current consumption



AUDIO OP

GAIN0	GAIN1	AV
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

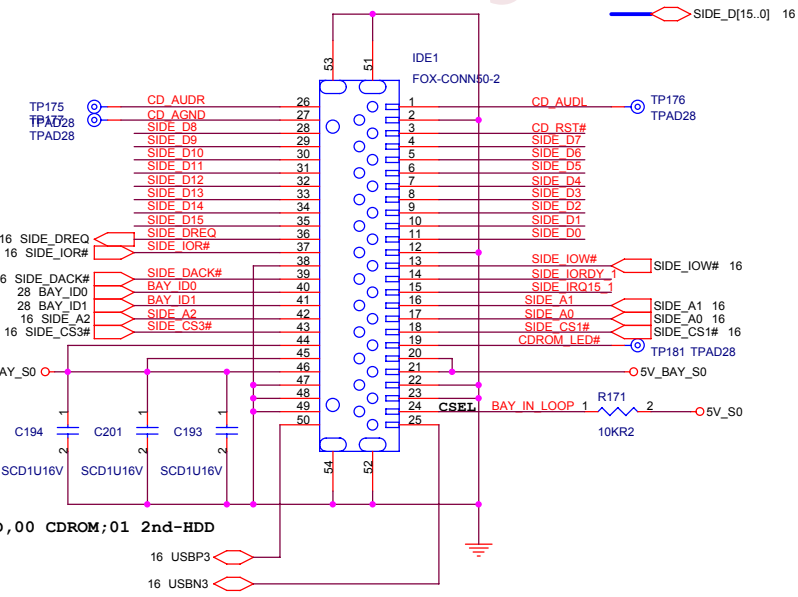
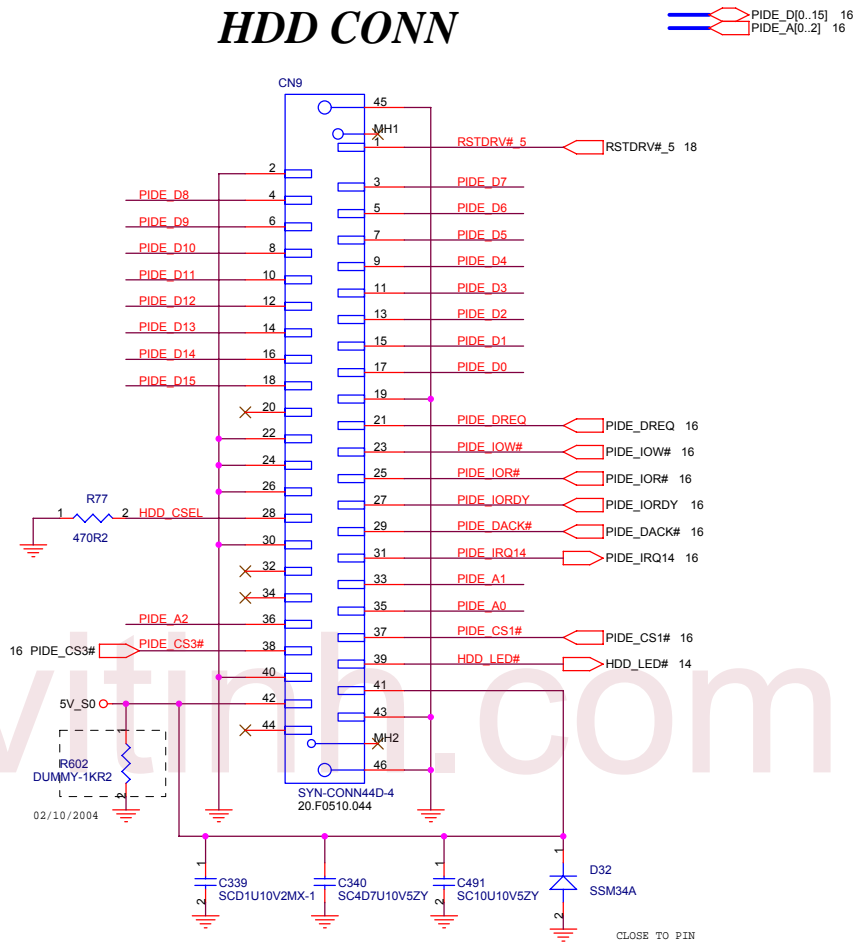
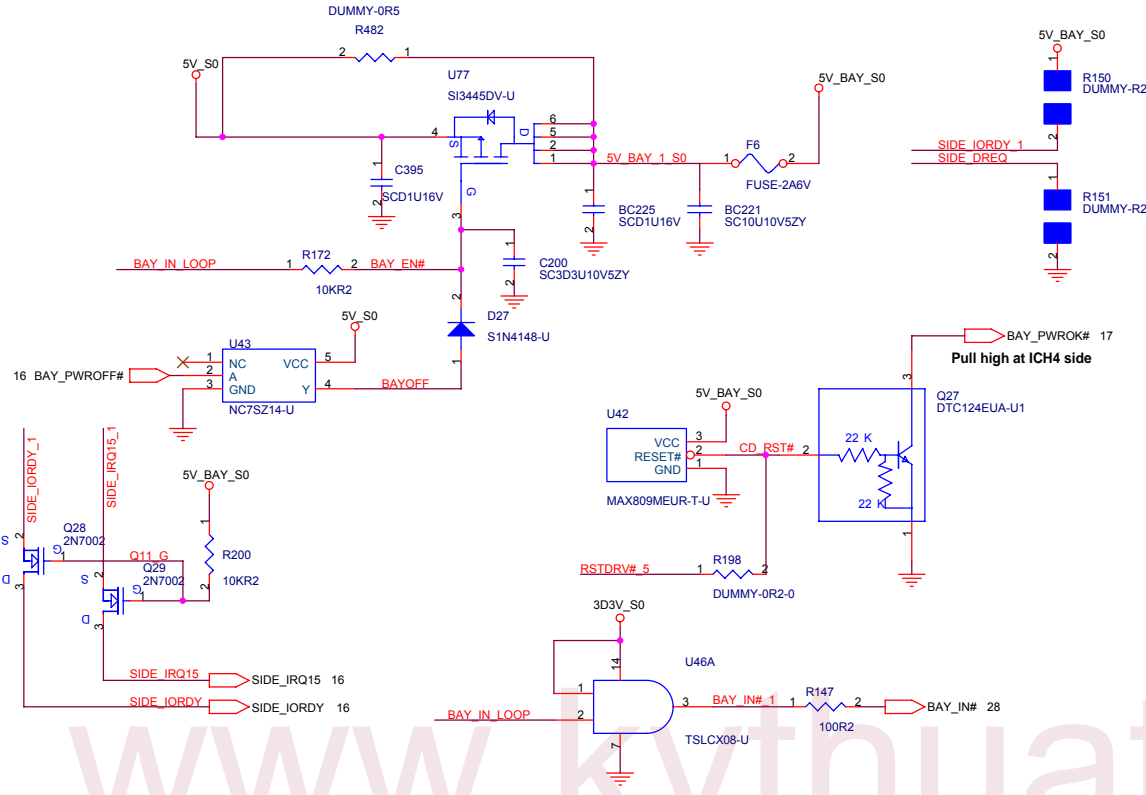


01/30/04

SB: Change to JH2 that one

SB: 2004/03/09 To solve speaker pop sound issue

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
		Title	
AUDIO (2 of 2) -Phone Jack			
Size	Document Number	Rev	
A3	MOLOKAI	SC	
Date:	Thursday, April 15, 2004	Sheet	25 of 39



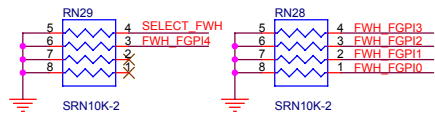
DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **HDD/CD ROM**

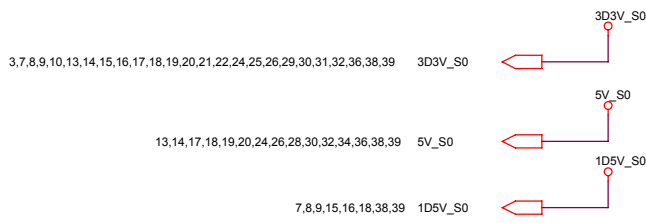
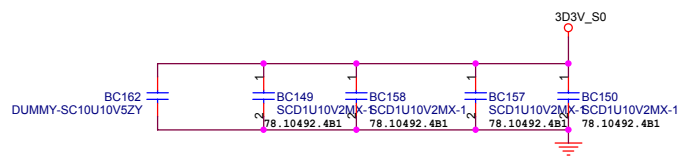
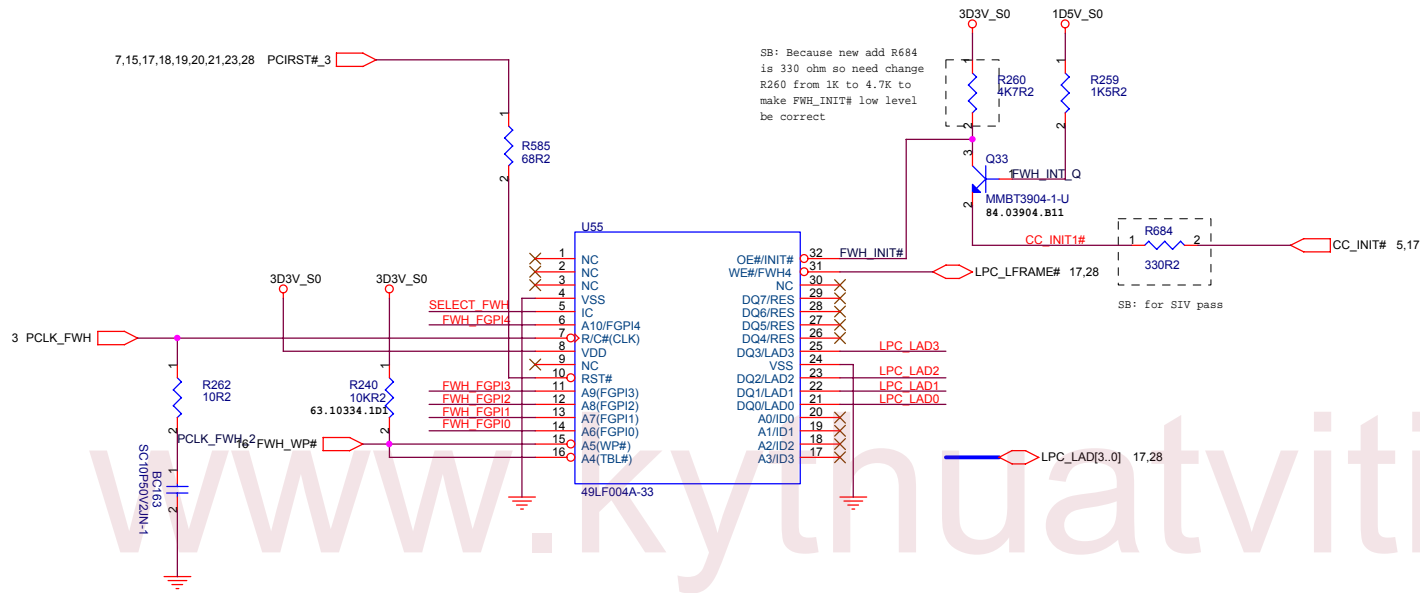
Size A3 Document Number: **MOLOKAI** Rev: **SC**

Date: Thursday, April 15, 2004 Sheet 26 of 39

Boot Device must have ID[3:0] = 0000
 Has internal pull-down resistors
 All may be left floated
 FPET7 Elec. P3-46



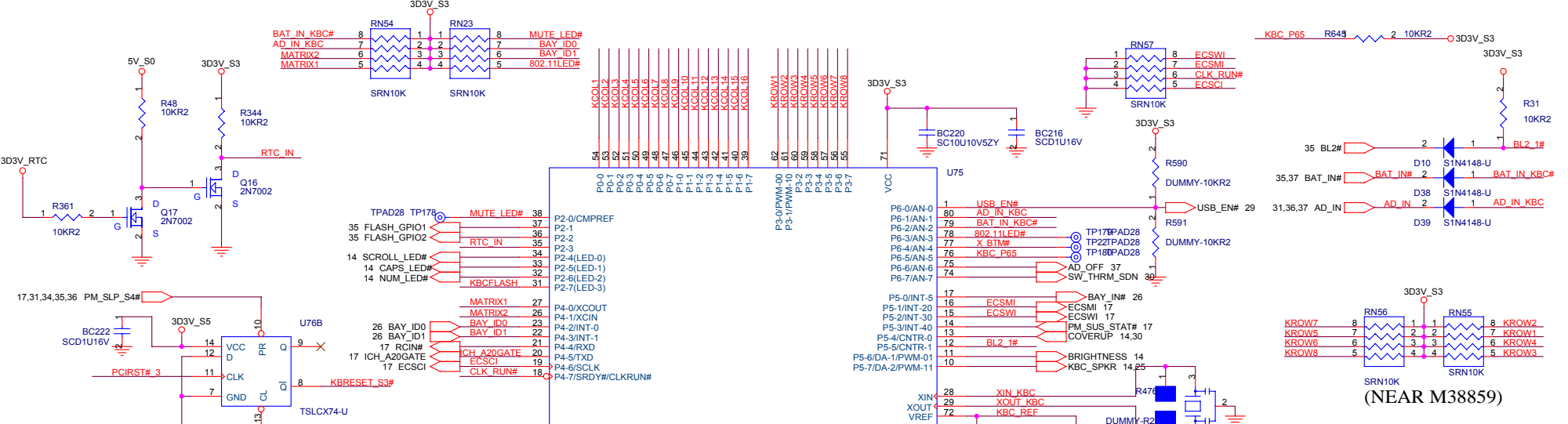
Unused FGPI pins must not be float



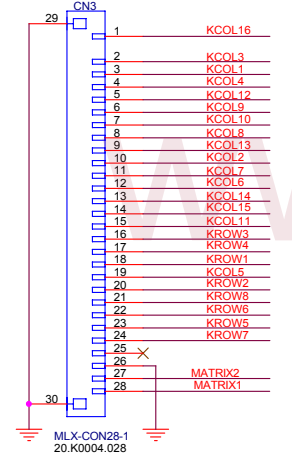
DELL Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **FWH/Debug Port**

Size: A3	Document Number: MOLOKAI	Rev: SC
Date: Thursday, April 15, 2004	Sheet: 27	of: 39



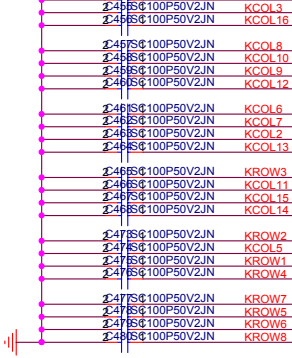
Internal Keyboard Connector



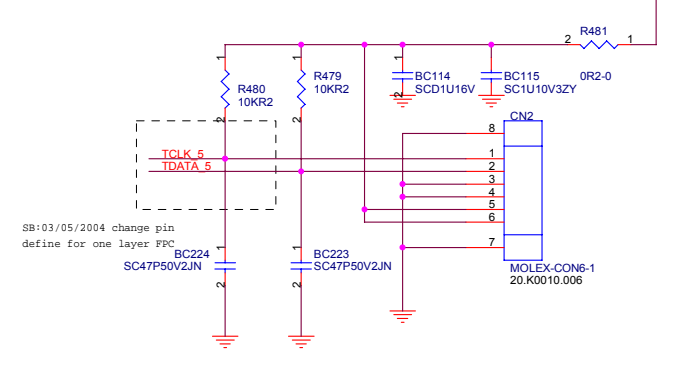
Keyboard Matrix

	US	JAP	Europe
MATRIX1	LOW	LOW	HIGH
MATRIX2	LOW	HIGH	LOW

For EMI



TouchPad Connector



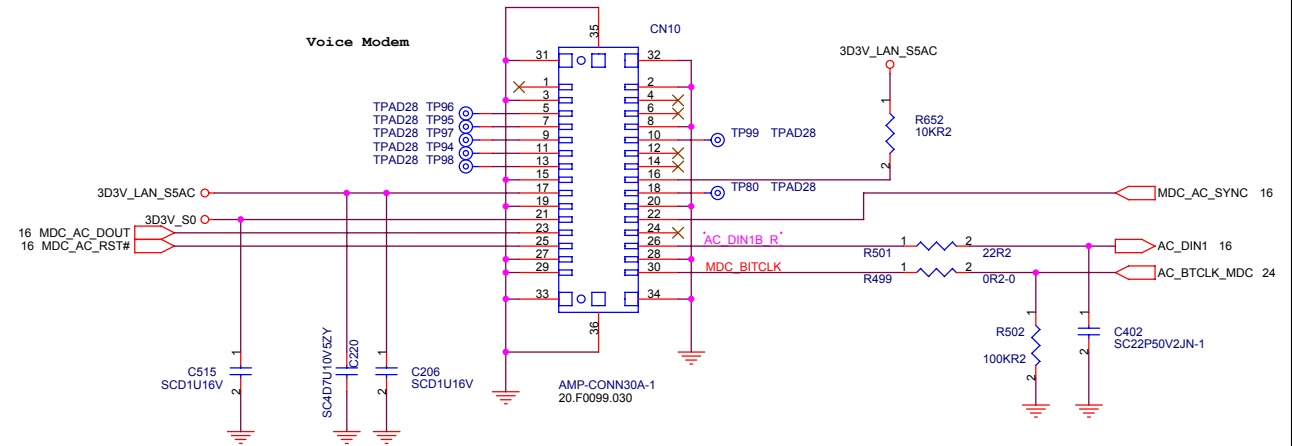
DELL Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **KBC/KB&TPAD CONN**

Size	Document Number	Rev
Custbm	MOLOKAI	SC

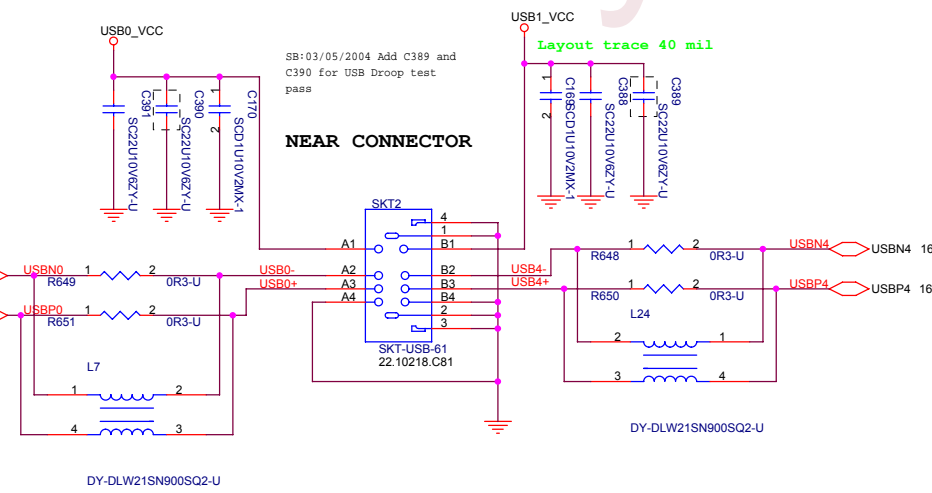
Date: Thursday, April 15, 2004 Sheet 28 of 39

MDC CONN



USB PORT

Dual USB switch



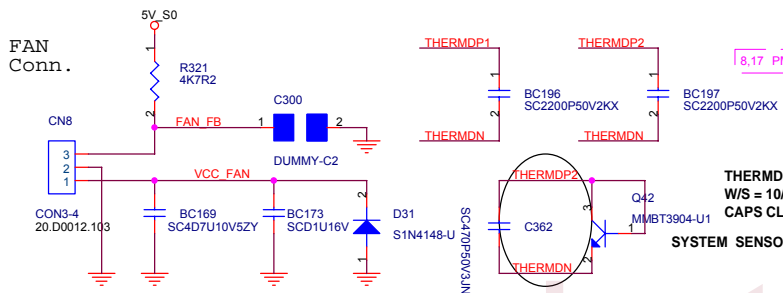
DELL Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **MDC CONN & USB CONN**

Size A3	Document Number	Rev SC
Date: Thursday, April 15, 2004		Sheet 29 of 39

240 ms after VCC_G768 > 4.38v

FAN Conn.

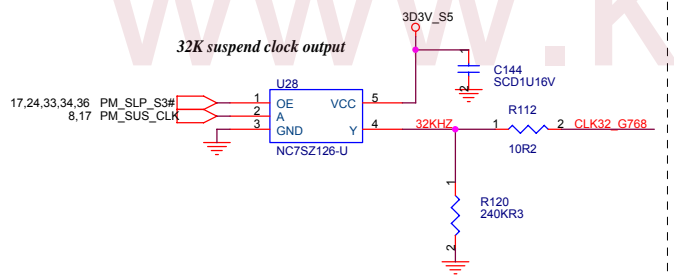


THERMDP1/DP2/THERMDN ON THE SAME LAYER
W/S = 10/5 MIL, 12 MIL AWAY FROM OTHERS
CAPS CLOSE TO G768D

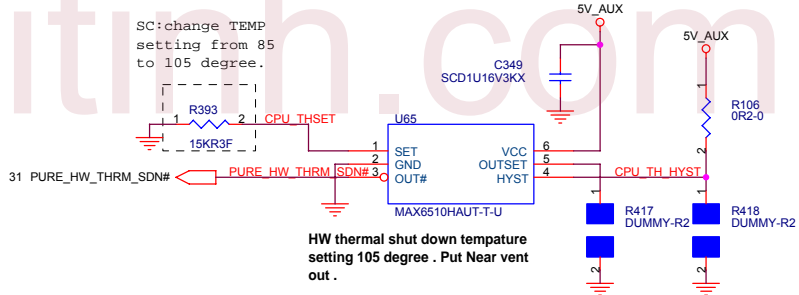
SYSTEM SENSOR

put together

32K suspend clock output

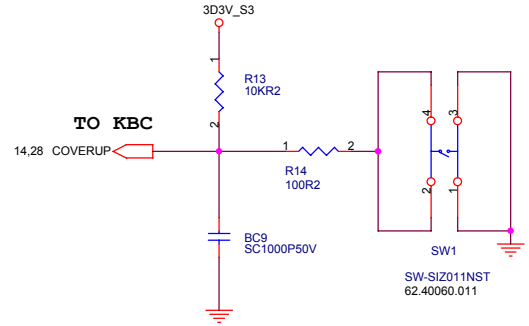


SC: change TEMP setting from 85 to 105 degree.

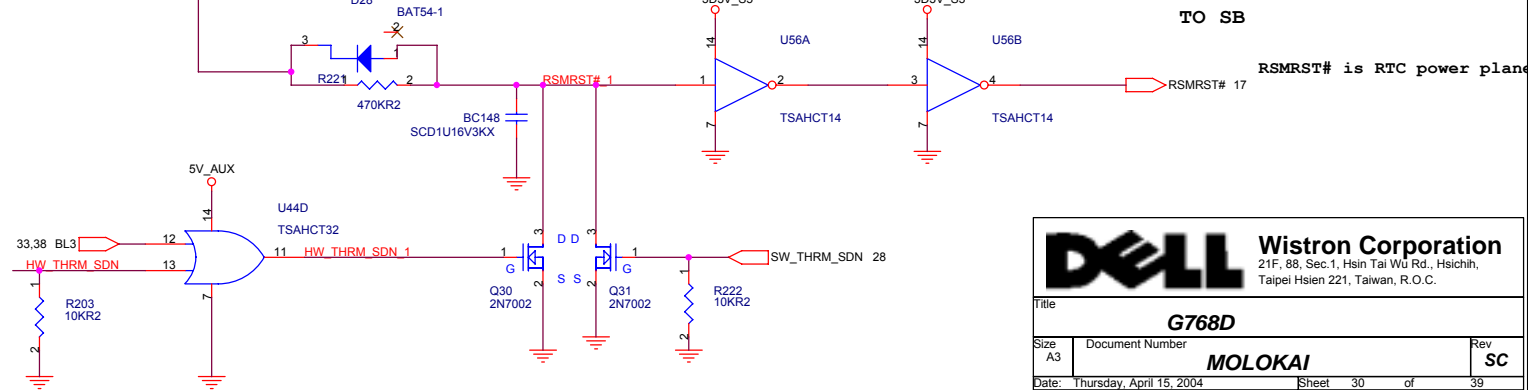


HW thermal shut down temperature setting 105 degree . Put Near vent out .

COVER SWITCH



RESUME RESET



TO SB

RSMRST# is RTC power plane

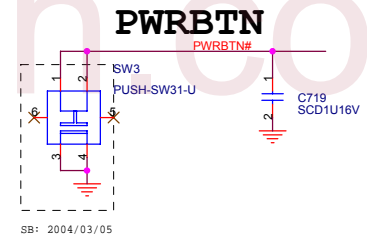
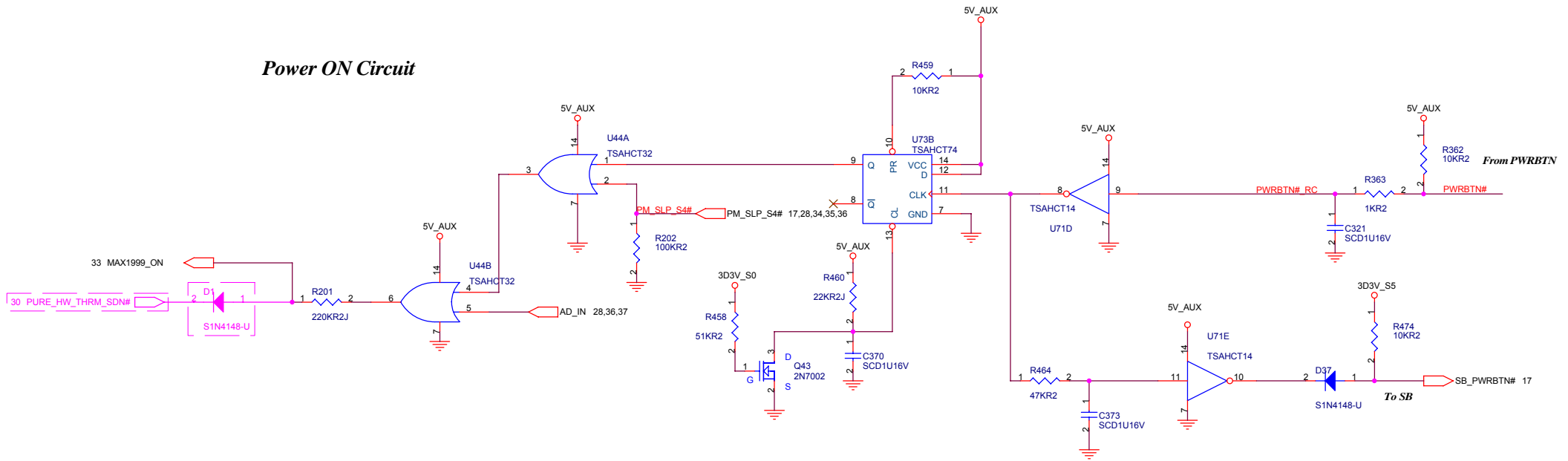
DELL Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **G768D**

Size A3 Document Number **MOLOKAI** Rev **SC**

Date: Thursday, April 15, 2004 Sheet 30 of 39

Power ON Circuit



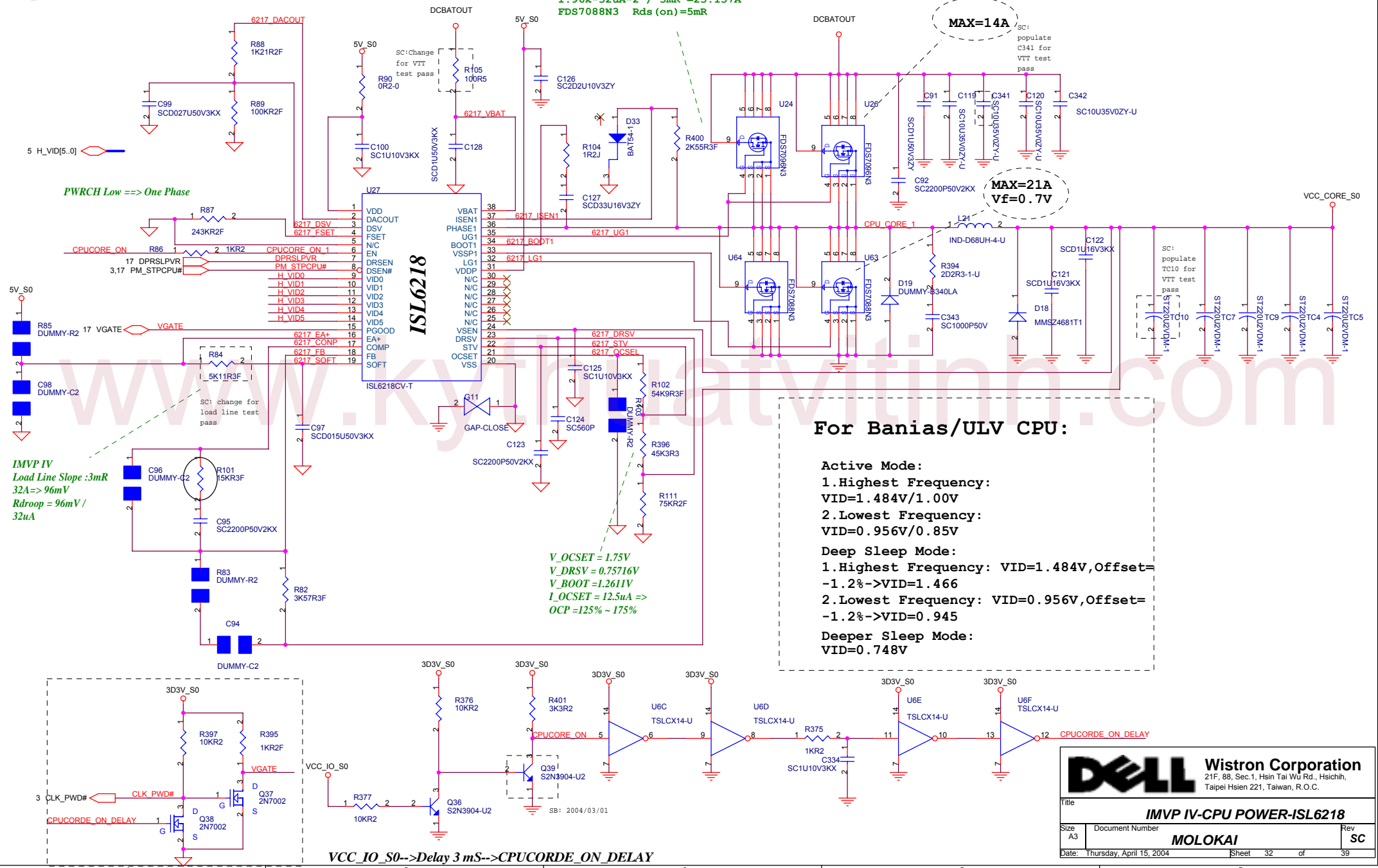
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Deep Sleep
 $100k/(100k+1.21k)=98.79\%$
 OffSet= 1.21%

Active Deep Deeper
 DPRSLPVR 0 0 1
 STP_CPU# 1 0 0

$$IFL = (RISEN * 32\mu A * n) / R_{ds(on)} = 1.96k * 32\mu A * 2 / 5mR = 25.157A$$

FDS7088N3 $R_{ds(on)} = 5mR$



For Banias/ULV CPU:

- Active Mode:**
- 1. Highest Frequency: VID=1.484V/1.00V
 - 2. Lowest Frequency: VID=0.956V/0.85V
- Deep Sleep Mode:**
- 1. Highest Frequency: VID=1.484V, Offset=-1.2% -> VID=1.466
 - 2. Lowest Frequency: VID=0.956V, Offset=-1.2% -> VID=0.945
- Deeper Sleep Mode:**
- VID=0.748V

$V_{OCSET} = 1.75V$
 $V_{DRSV} = 0.75716V$
 $V_{BOOT} = 1.2611V$
 $I_{OCSET} = 12.5\mu A \Rightarrow$
 $OCP = 125\% - 175\%$

VCC_IO_S0-->Delay 3mS-->CPUCORDE_ON_DELAY

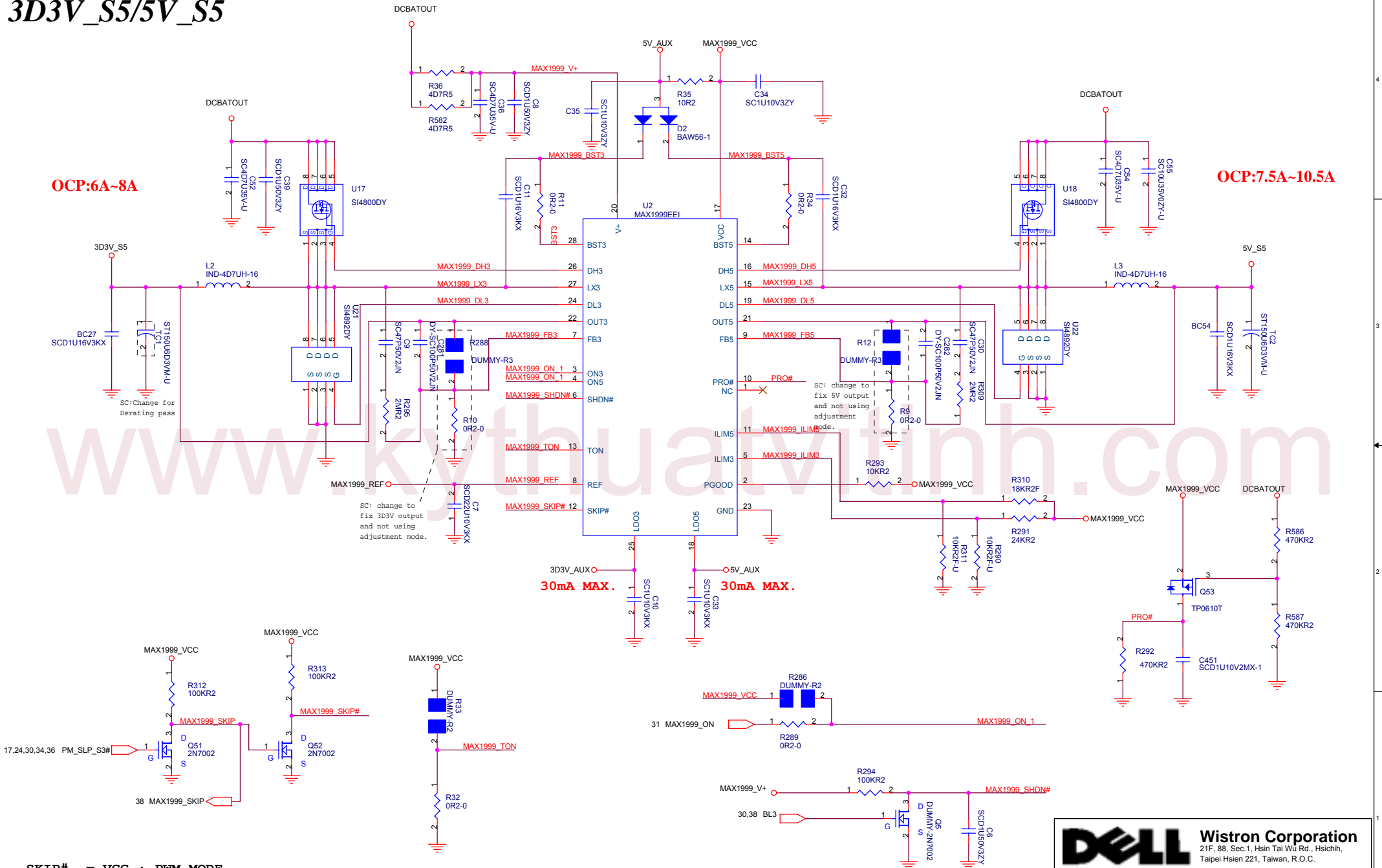
DELL Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **IMVP IV-CPU POWER-ISL6218**

Size A3	Document Number	MOLOKAI	Rev SC
Date: Thursday, April 15, 2004	Sheet	32	of 39

SYSTEM DC/DC

3D3V_S5/5V_S5



SKIP# = VCC : PWM MODE
SKIP# = GND : SKIP MODE
SKIP# = REF/FloatING : Ultrasonic MODE
(25KHz min)

Ton = VCC : 200KHz/300KHz
Ton = GND : 400KHz/500KHz
(5V/3D3V)

Wistron Corporation
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 Taipei Hsien 221, Taiwan, R.O.C.

Title: **MAX1999/3D3V_S5/5V_S5**

Size	Document Number	Rev	SC
A3	MOLOKAI		

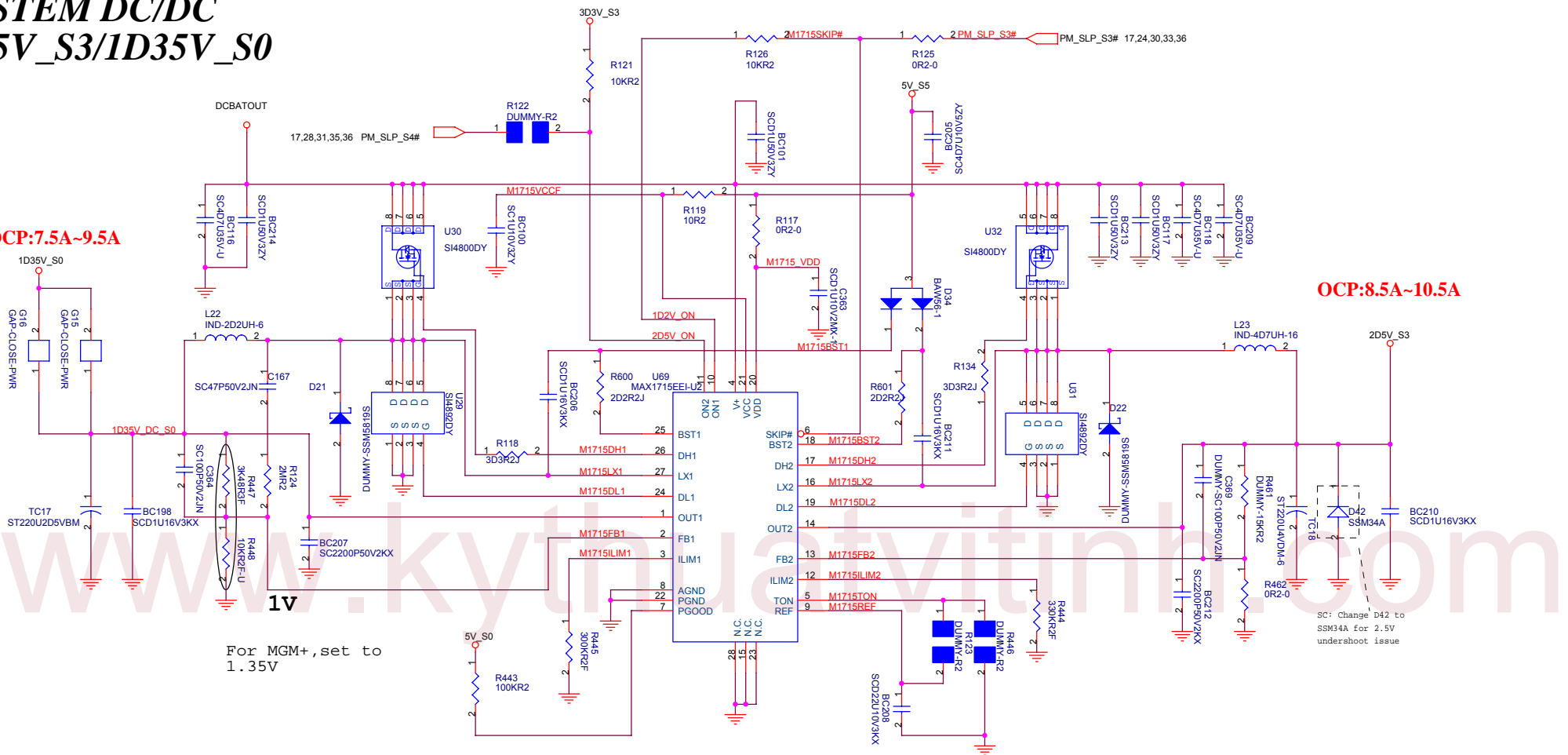
Date: Thursday, April 15, 2004 Sheet 33 of 39

SYSTEM DC/DC

2D5V_S3/1D35V_S0

OCP:7.5A~9.5A

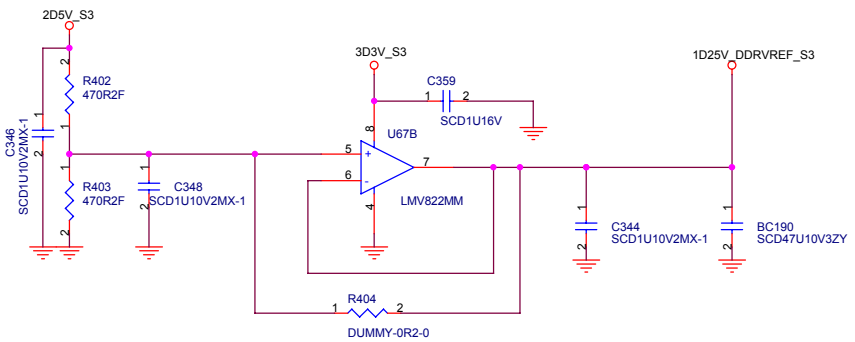
OCP:8.5A~10.5A



For MGM+, set to 1.35V

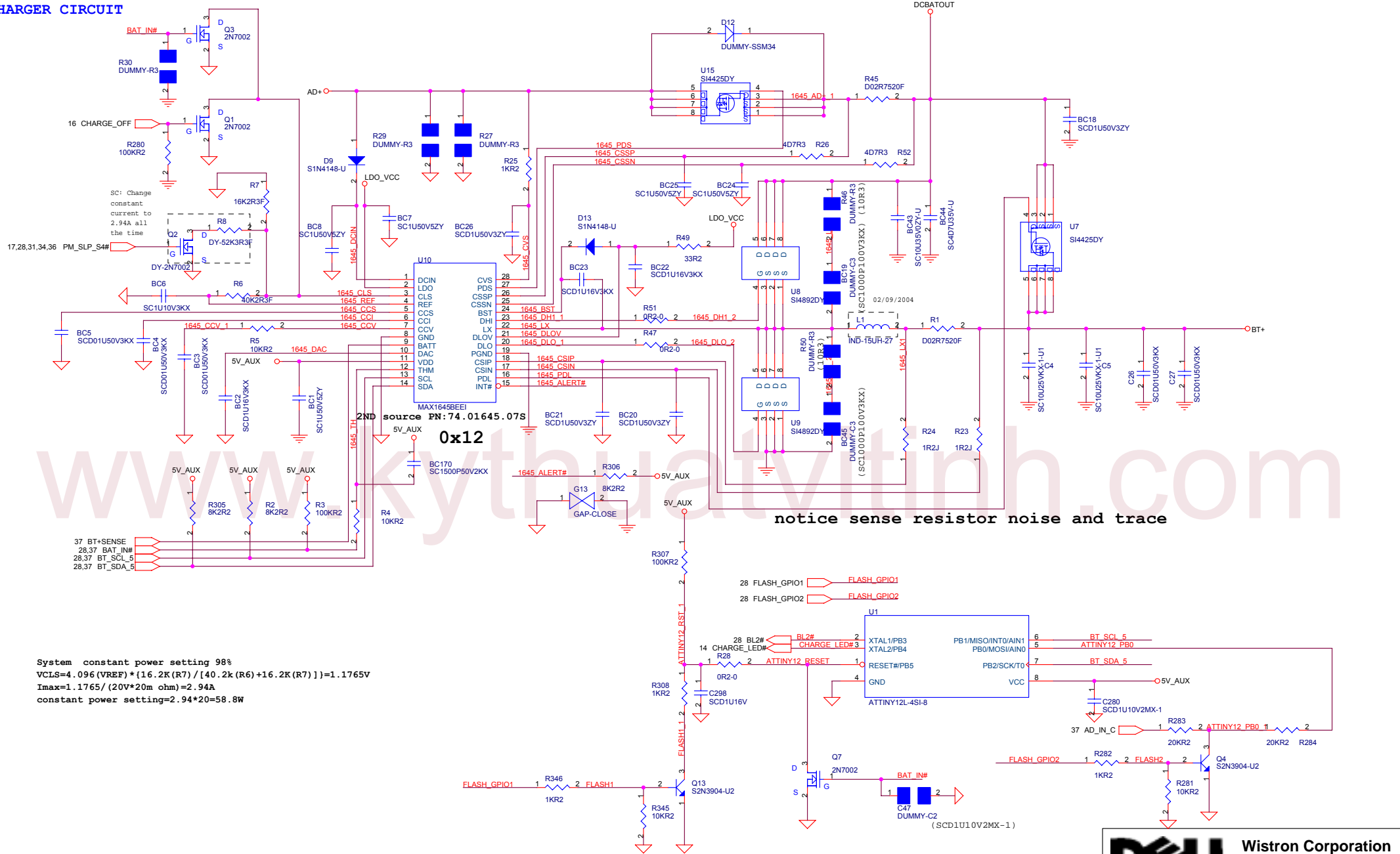
SC: Change D42 to SSM34A for 2.5V undershoot issue

1D25V_DDRVREF_S3 need 10 mil and must near NB/DIMM



		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
		Title MAX1715/2D5V_S3/1D35V_S0	
Size A3	Document Number MOLOKAI	Rev SC	Date: Thursday, April 15, 2004
Sheet 34 of 39		Date: Thursday, April 15, 2004	

CHARGER CIRCUIT



System constant power setting 98%
 $V_{CLS} = 4.096 (V_{REF}) * \{ [16.2k (R7)] / [40.2k (R6) + 16.2k (R7)] \} = 1.1765V$
 $I_{max} = 1.1765 / (20V * 20m\ \Omega) = 2.94A$
 constant power setting = $2.94 * 20 = 58.8W$

notice sense resistor noise and trace

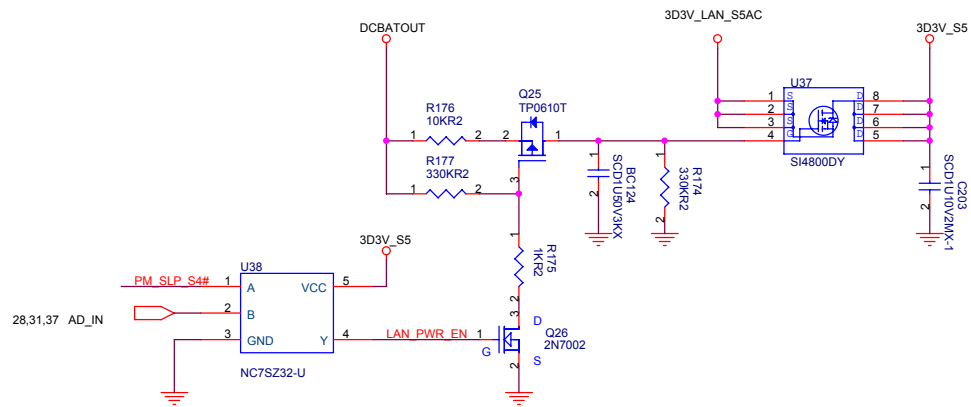
DELL Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **CHARGER&MicroP**

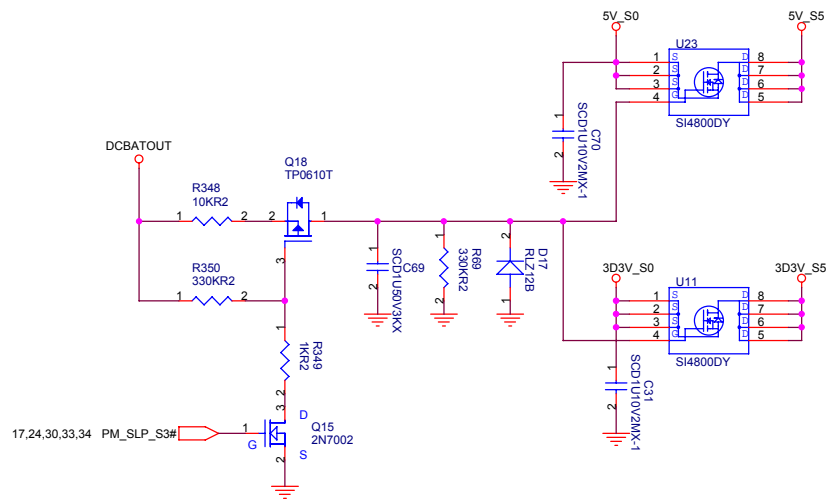
Size: Document Number **MOLOKAI** Rev: **SC**

Date: Thursday, April 15, 2004 Sheet 35 of 39

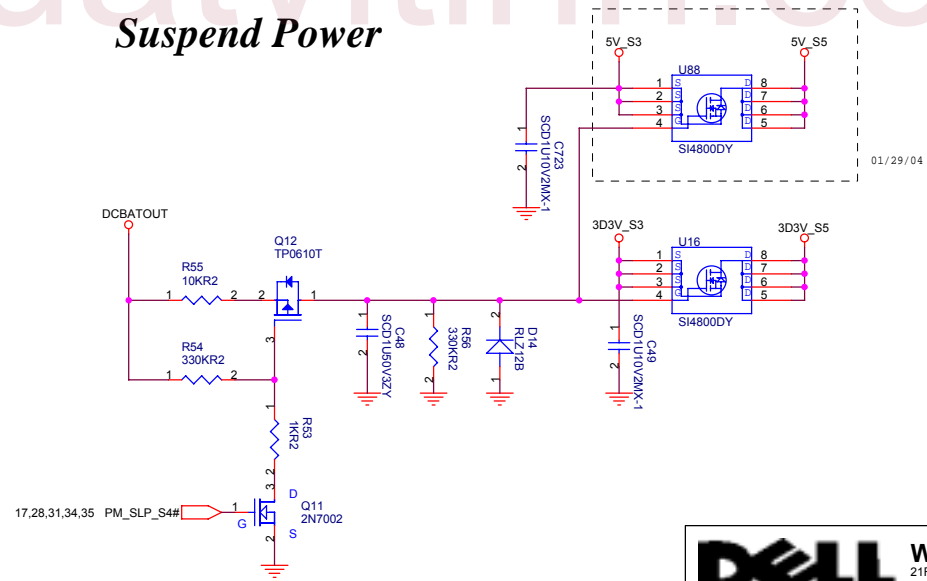
LAN Power




Run Power



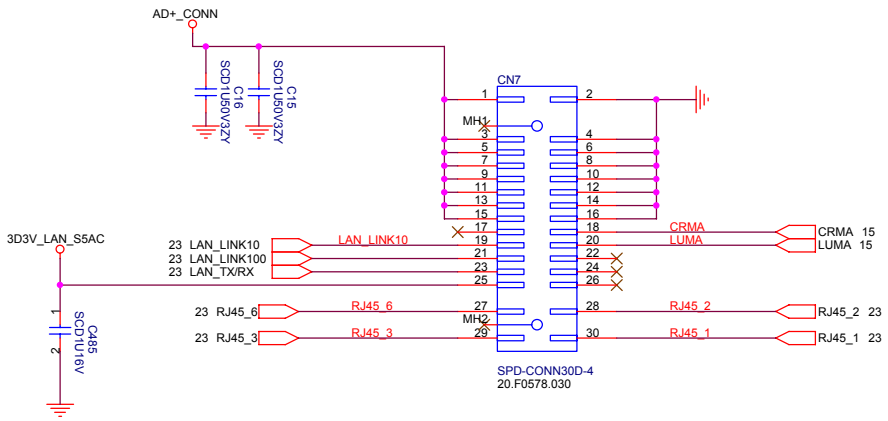
Suspend Power



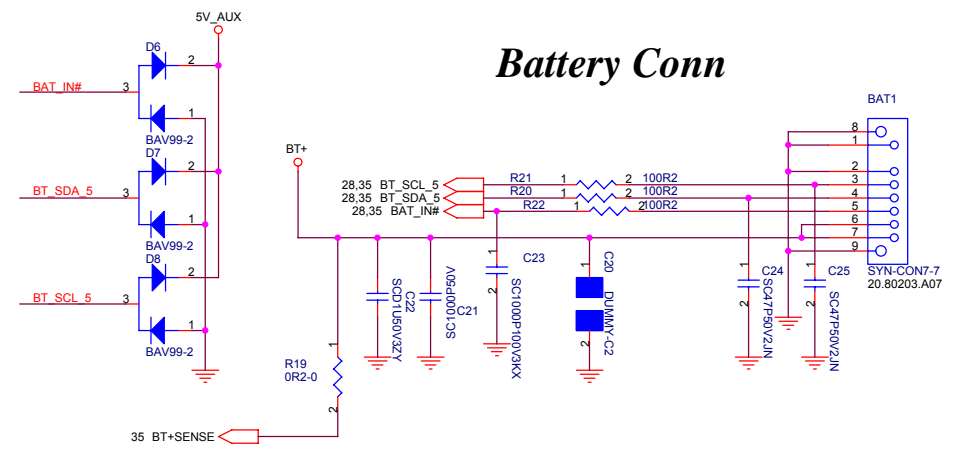
 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		Title	
		PWR Plane SW / VCC_IO_S0	
Size	Document Number	Rev	
A3	MOLOKAI	SC	
Date:	Thursday, April 15, 2004	Sheet	36 of 39

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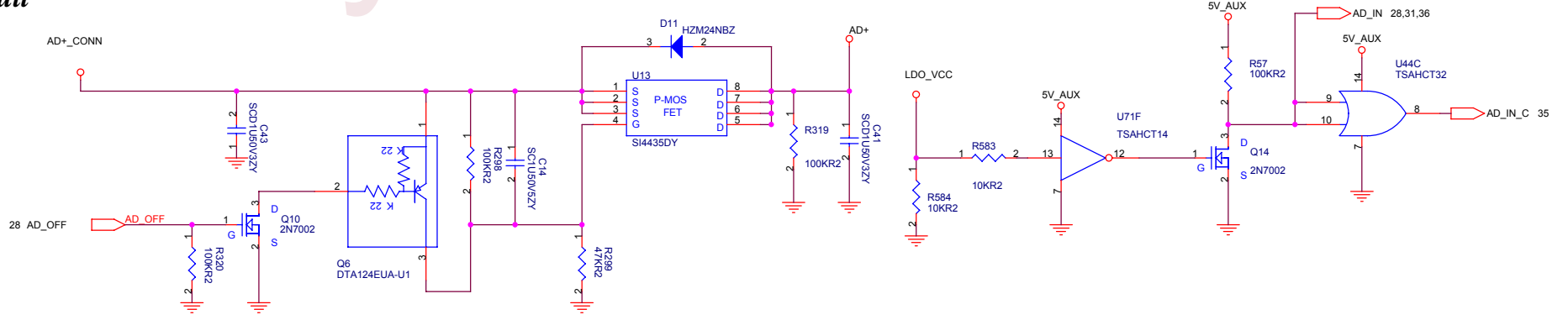
TV BD Conn



Battery Conn



Adaptor In Circuit

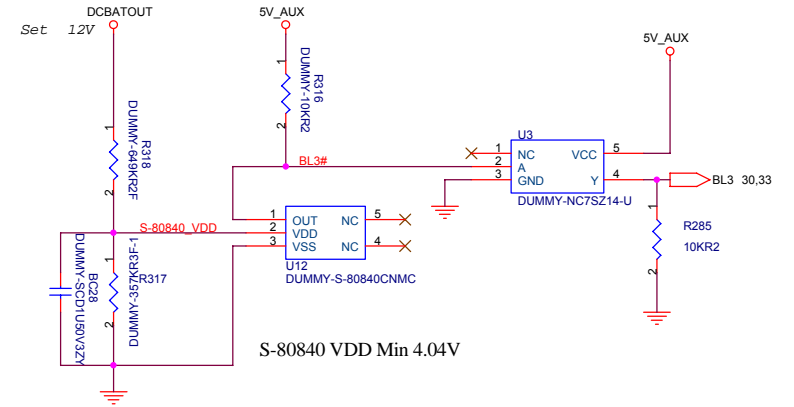


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 Taipei Hsien 221, Taiwan, R.O.C.

Title: **Battery Conn/TV BD Conn/Adaptor In Circuit**

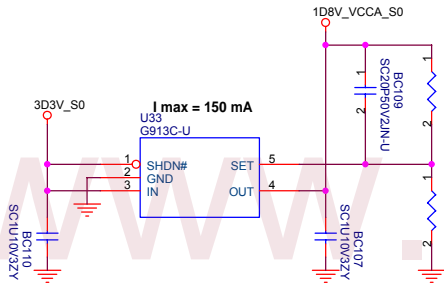
Size: A3	Document Number: MOLOKAI	Rev: SC
Date: Thursday, April 15, 2004	Sheet: 37	of: 39

BATTERY LOW3 DETECTOR

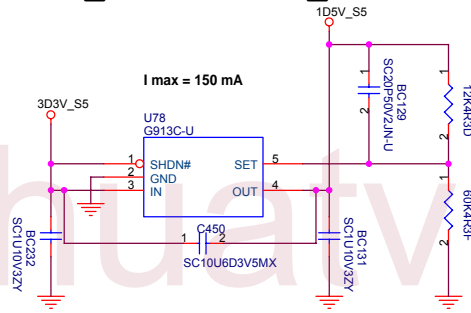


At Dothan CPU application, POWER is 1.5V or 1.8V.

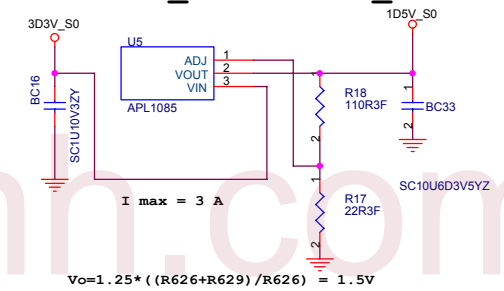
3D3V_S0 --> 1D8V_VCCA_S0 (For CPU VCCA)



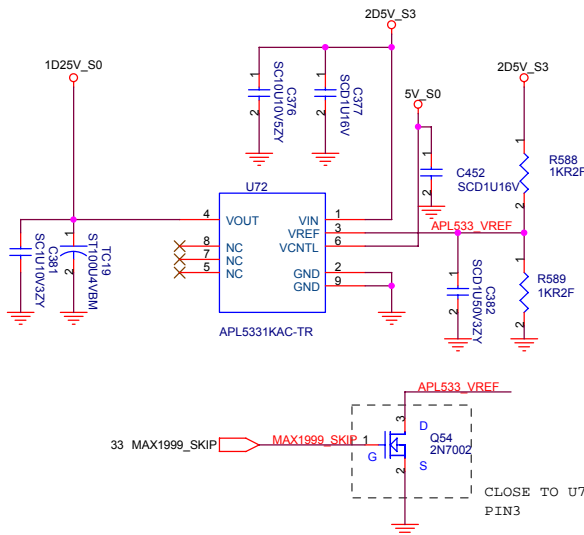
3D3V_S5 --> 1D5V_S5



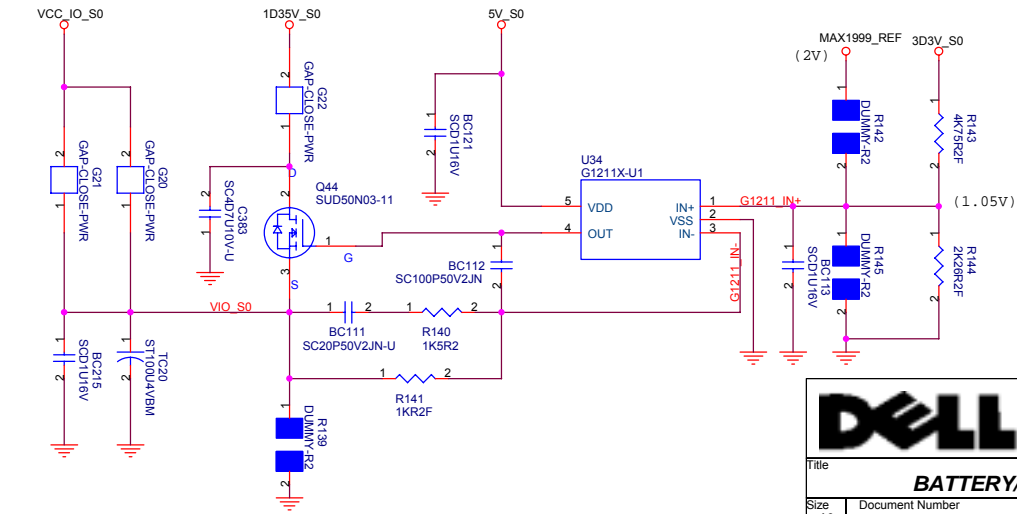
3D3V_S0 → 1D5V_S0



2D5V_S3 → 1D25V_S0

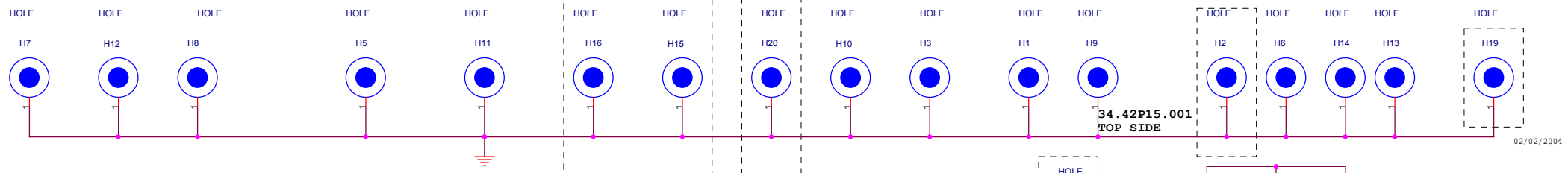
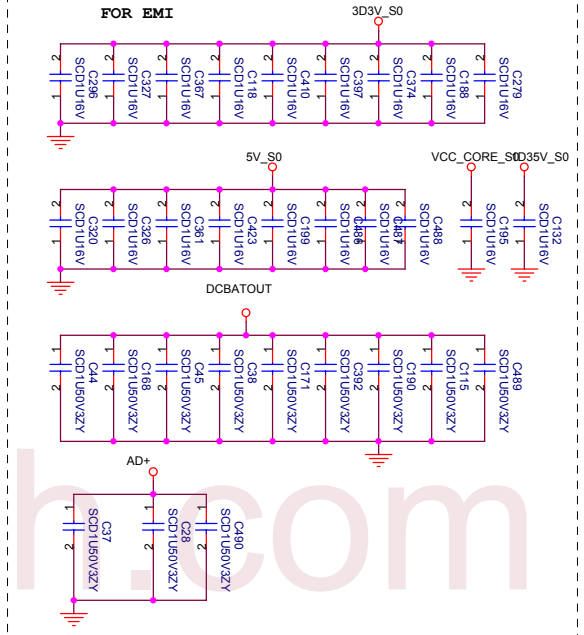
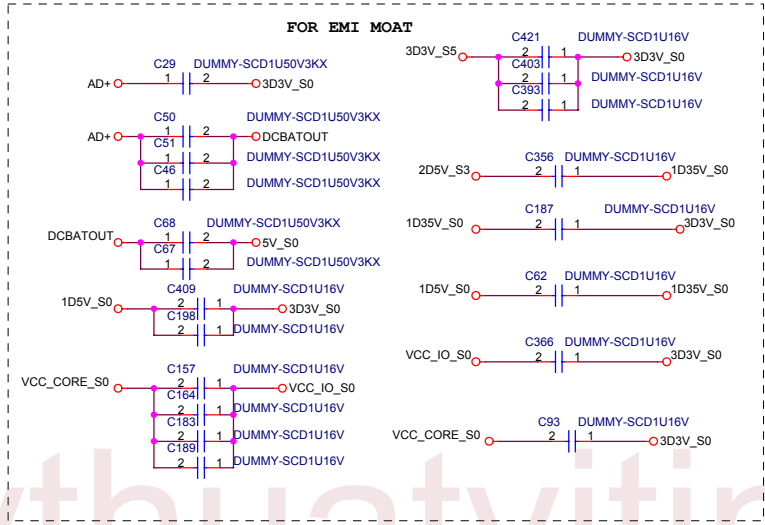
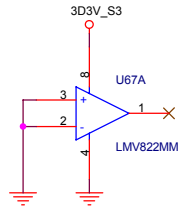
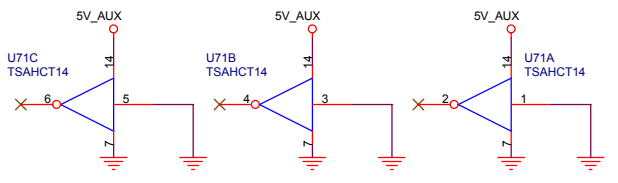
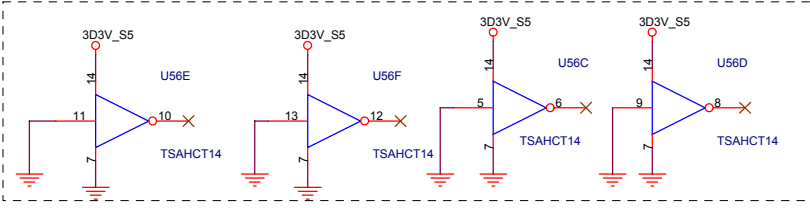
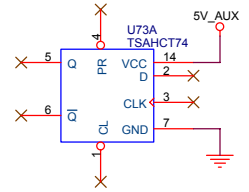
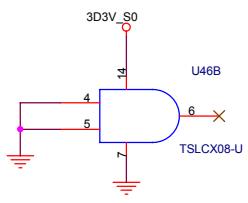


1D35V_S0 → VCC_IO_S0 (1.05V)



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Taipei Hsien 221, Taiwan, R.O.C.

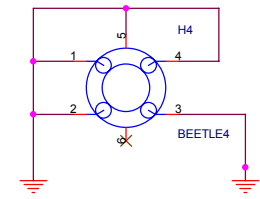
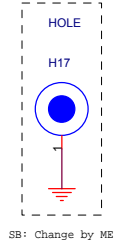
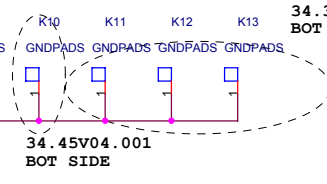
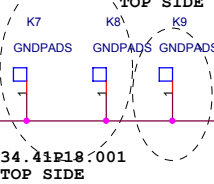
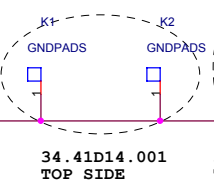
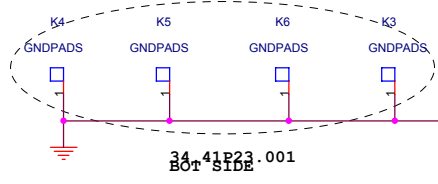
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Date:	Thursday, April 15, 2004	Sheet 38 of 39



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Date: Thursday, April 15, 2004 | Sheet: 39 of 39