MOLOKAI Block Diagram

SPR.01.2004

Project Code:91.43E01.001

03249-SC

PCB LAYER
L1:COMPONENT
L2:GND
L3:SIGNAL1
L4:SIGNAL2
L5:VCC
L6:GND
L7:SIGNAL3
L8:COMPONENT

DC/DC IMVP4
Switching Power
ISL6218 32

INPUTS	OUTPUT
DCBATOUT	VCC_CORE

SYSTEM DC/DC
MAX1715 34

INPUTS	OUTPUTS
DCBATOUT	1D35V_S0 2D5V_S3

DC/DC&CHARGER
MAX1645 35

INPUTS	OUTPUTS
AD+	BT+

DC/DC
MAX1999 33

INPUTS	OUTPUTS
DCBATOUT	3D3V_S5 5V_S5

G913C/APL1085
APL5331kAC/G1211X 38

INPUTS	OUTPUTS
3D3V_S0	1D8V_VCCA_S0
3D3V_S5	1D5V_S5
3D3V_S0	1D5V_S0
2D5V_S3	1D25V_S0
1D35V_S0	VCC_IO_S0

CLOCK Generator ICS950810 3

CPU
Banias/Dothan 5,6

HOST BUS
100MHz

DDR DRAM Socket 10,11,12
*** 2**

DDR 266/333

Montara-GM+ 7,8,9

DVO → CH7011 (CHRONTEL) 15 → TV_OUT

CRT 13

LVDS → LCD 14

Hub I/F

ICH4-M 16,17,18

Ultra DMA-100

HDD 26

OPTICAL

IDE BUS

USB2.0

PCI BUS

SD/MS CARD READER + 1394
PCI7420 21

POWER SW
TPS2220A 20

CARDBUS
SLOT B 22

CardReader

1394

LPC BUS

BIOS ROM
49LF004-334C 27

KBC M38859 28

USB2.0

USB 2.0
2 Ports 29

TOUCH PAD

INT KB

LAN BCM4401 23

MINIPCI
802.11B
802.11G 19

AC-LINK

RJ-45

Line-out

MIC

MODEM DAUGHTER CARD 29

RJ-11

AC 97
Codec
STAC9750 24

Amplifier
TPA0312 25

(TBD)

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Title		
BLOCK DIAGRAM		
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S5

5V_S5 — 5V_S5 18,33,34,36
3D3V_S5 — 3D3V_S5 4,16,17,18,28,30,31,33,36,38,39
1D5V_S5 — 1D5V_S5 18,38
VCC_RTC_S5 — VCC_RTC_S5 17

S3

3D3V_S3 — 3D3V_S3 14,25,28,30,34,36,39
2D5V_S3 — 2D5V_S3 7,9,10,11,34,38,39
1D25V_DDRVREF_S3 — 1D25V_DDRVREF_S3 7,10,34

S0

5V_S0 — 5V_S0 13,14,17,18,19,20,24,26,28,30,32,34,36,38,39
3D3V_S0 — 3D3V_S0 3,7,8,9,10,13,14,15,16,17,18,19,20,21,22,24,25,26,27,29,30,31,32,36,38,39
1D5V_S0 — 1D5V_S0 7,8,9,15,16,18,27,38,39
1D25V_S0 — 1D25V_S0 11,12,38
1D35V_S0 — 1D35V_S0 7,9,34,38,39
VCC_CORE_S0 — VCC_CORE_S0 6,32,39
VCC_IO_S0 — VCC_IO_S0 4,5,6,7,9,17,18,32,38,39
1D8V_VCCA_S0 — 1D8V_VCCA_S0 5,38

AC-IN / BAT.-IN

AD+ — AD+ 35,37,39
DCBATOUT — DCBATOUT 14,32,33,34,35,36,38,39

LAN-AC

3D3V_LAN_S5AC — 3D3V_LAN_S5AC 23,29,36,37

5VA_AUD_S3 — 5VA_AUD_S3 24 → AUDIO

3D3V_LCD_S0 — 3D3V_LCD_S0 14 → LCD

CRT_VCC_S0 — CRT_VCC_S0 13 → CRT

TV3D3V1_S0 — TV3D3V1_S0 15
TV3D3VA_S0 — TV3D3VA_S0 15
TV3D3V2_S0 — TV3D3V2_S0 15
TV1D5V_S0 — TV1D5V_S0 15
→ TV-OUT

OTHERS

5V_AUX — 5V_AUX 30,31,33,35,37,38,39
3D3V_AUX — 3D3V_AUX 14,17,33

3D3V_RTC — 3D3V_RTC 17,28
ICH_VBIAS — ICH_VBIAS 17
MAX1999_REF — MAX1999_REF 33,38

MAX1999_VCC — MAX1999_VCC 33

PCI TABLE

DEVICE	IDSEL	IRQ	REQ# / GNT#
SD/MS CARD READER+1394 PCI7420	AD20	PIRQB# PIRQC# PIRQF#	REQ#1 / GNT#1
MINI PCI 802.11B/G	AD17	PIRQE# PIRQG#	REQ#0 / GNT#0
LAN BCM4401	AD21	PIRQD#	REQ#4 / GNT#4

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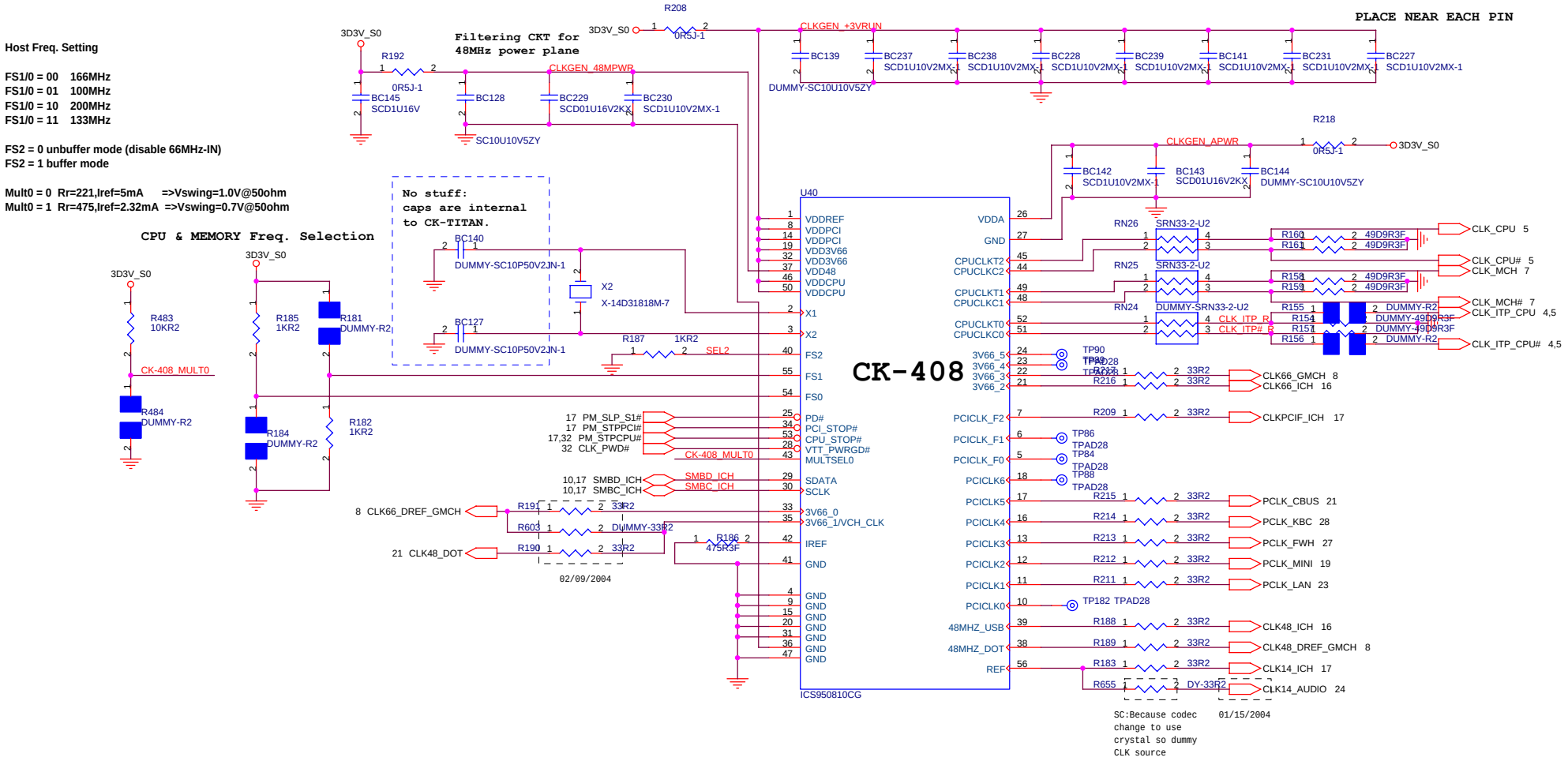

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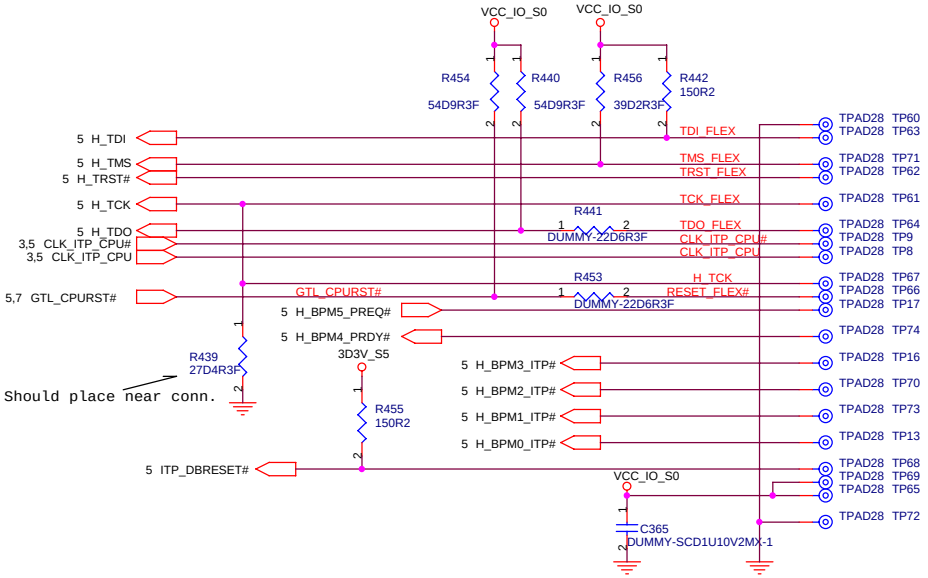
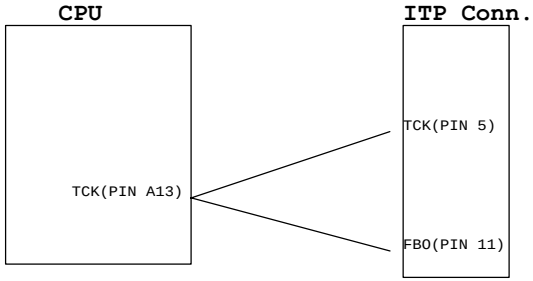
ITP Debug Pad





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CPU VCCA POWER:

At Dothan CPU application, POWER is 1.5V or 1.8V.

For CPU VCCA[0:3] PLL place one 0.01u & 10u for each VCCA pin

1D8V_VCCA_S0

BC87 DY-SC10U6D3V5MX
BC75 SC10U6D3V5MX
BC108 DY-SC10U6D3V5MX
BC104 DY-SC10U6D3V5MX
BC106 SCD01U16V2KX
BC105 SCD01U16V2KX
BC86 SCD01U16V2KX
BC90 SCD01U16V2KX

Layout note:
COMP0 and COMP2 need to be Zo=27.4ohm traces.
COMP1 and COMP3 should be routed asx Zo=54.9ohm, traces shorter than 0.5".

U68D

3 CLK_CPU → BCLK0
3 CLK_CPU# → BCLK1
3,4 CLK_ITP_CPU → ITP_CLK0
3,4 CLK_ITP_CPU# → ITP_CLK1

17 CC_A20M# → A20M#
17 CC_FERR# → CC_FERR# → FERR#
17 CC_IGNNE# → IGNNE#

17 CC_INTR → LINT0
17 CC_NMI → LINT1

17 CC_SMI# → SMI#
17 CC_STPCLK# → STPCLK#

1D8V_VCCA_S0 → VCCA3 **120mA**, VCCA2, VCCA1, VCCA0

RSVD, TPAD28, TEST3, TDI, TDO, VCCSENSE, VSSSENSE

32 H_VID[5:0] → H_VID5, H_VID4, H_VID3, H_VID2, H_VID1, H_VID0 → VID5, VID4, VID3, VID2, VID1, VID0

R131 DUMMY-54D9R3F, R132 DUMMY-54D9R3F

BPM3#, BPM2#, BPM1#, BPM0# → H_BPM3_ITP#, H_BPM2_ITP#, H_BPM1_ITP#, H_BPM0_ITP#

COMP3 AB1 27D4-3 R135 54D9R3F
COMP2 AB2 27D4-1 R136 27D4R3F
COMP1 P26 27D4-4 R110 54D9R3F
COMP0 P25 27D4-2 R109 27D4R3F

DPSLP# → CC_DPSLP# 7,17

GTLREF3, GTLREF2, GTLREF1, GTLREF0 → H_GTLREF 0

PROCHOT# → CC_PROCHOT#
PWRGOOD → CC_CPUPWRGD 7,17

VCC_IO_S0
R108 1KR2F
SC: Change to 1KR2F for GTLREF pass
Voltage divider placed within 0.5" of CPU pin via a Zo=55ohm trace.
H_GTLREF 0 2/3 RATIO
R107 2KR3F
C134 DUMMY-SCD01U16V

R116 150R2 H_TDI
R113 DUMMY-1KR2
17 CC_CPUSLP# 4 H_TCK → H_TCK → TCK
4 H_TDI 4 H_TDO → H_TDI, H_TDO

TEST1, TEST2 → TP6 TPAD28
THERMDA, THERMDC, THERMTRIP#, TMS, TRST#
THERMDP1 30 → C165 SC1000P50V → THERMDN 30
PM_THERMTRIP# 17
H_TMS 4, H_TRST# 4
R115 680R2

VCC_IO_S0
GTL_IERR# R450 56R2J
CC_CPUPWRGD R133 330R2
CC_PROCHOT# R114 56R2J

U68C

7 GTL_D#[15..0] → D15# … D0#
GTL_D#15 C25 … GTL_D#0 A19

7 GTL_DINV#0, 7 GTL_DSTBN#0, 7 GTL_DSTBP#0 → D25, C23, C22
7 GTL_D#[31..16] → D31# … D16#
GTL_D#31 K25 … GTL_D#16 H23

7 GTL_DINV#1, 7 GTL_DSTBN#1, 7 GTL_DSTBP#1 → J26, K24, L24

D47# … D32# → Y25 GTL_D#47 … Y26 GTL_D#32 → GTL_D#[47..32] 7

DINV2#, DSTBN2#, DSTBP2# → T24, W25, W24 → GTL_DINV#2 7, GTL_DSTBN#2 7, GTL_DSTBP#2 7

D63# … D48# → AF26 GTL_D#63 … AB25 GTL_D#48 → GTL_D#[63..48] 7

DINV3#, DSTBN3#, DSTBP3# → AD20, AE24, AE25 → GTL_DINV#3 7, GTL_DSTBN#3 7, GTL_DSTBP#3 7

BGA479-SKT-2-U

U68B

7 GTL_A#[16..3] → A16# … A3#
GTL_A#16 AA2 … GTL_A#3 P4

7 GTL_ADSTB#0 → U3 ADSTB0#

7 GTL_A#[31..17] → A31# … A17#
GTL_A#31 AF1 … GTL_A#17 AF4

7 GTL_ADSTB#1 → AE5 ADSTB1#

TP18 TPAD28

ADS# → N2 GTL_ADS# 7
BNR# → L1 GTL_BNR# 7
BPRI# → J3 GTL_BPRI# 7
BR0# → N4 GTL_BR0# 7
DBR# → A7 ITP_DBRESET# 4
DBSY# → M2 GTL_DBSY# 7
DEFER# → L4 GTL_DEFER# 7
DRDY# → H2 GTL_DRDY# 7
HIT# → K3 GTL_HIT# 7
HITM# → K4 GTL_HITM# 7
IERR# → A4 GTL_IERR#
INIT# → B5 CC_INIT# 17,27
LOCK# → J2 GTL_LOCK# 7
PRDY# → A10 H_BPM4_PRDY# 4
PREQ# → B10 H_BPM5_PREQ# 4
RESET# → B11 GTL_CPURST# 4,7

TRDY# → M3 GTL_TRDY# 7
RS2# → L2 GTL_RS#2 7
RS1# → K1 GTL_RS#1 7
RS0# → H1 GTL_RS#0 7
DPWR# → C19 GTL_DPWR# 7

REQ4# … REQ0# → T1 GTL_REQ#4 … R2 GTL_REQ#0 → GTL_REQ#[0..4] 7

BGA479-SKT-2-U

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Title: **Banias CPU (1 of 2)**

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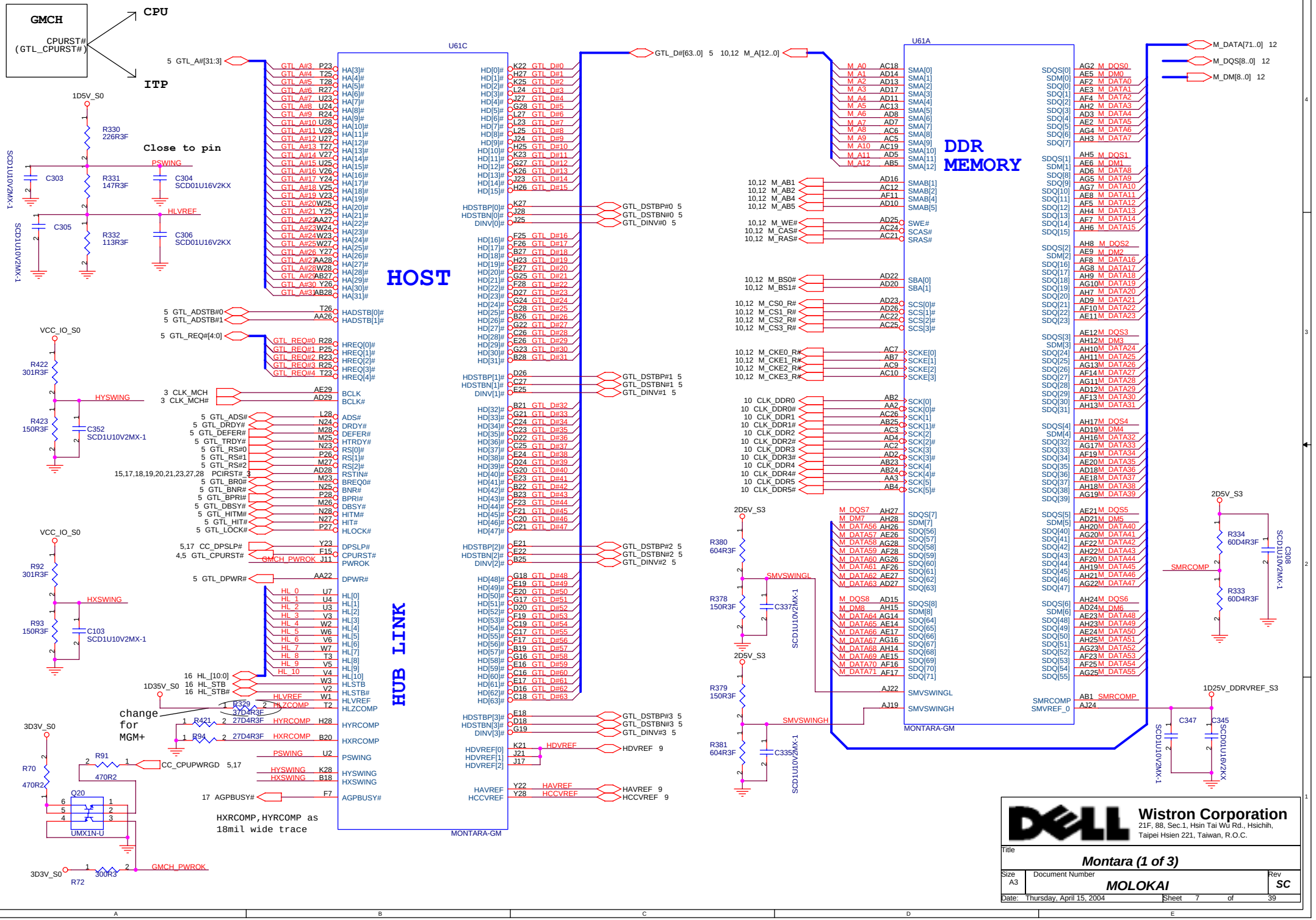
GMCH
CPURST#
(GTL_CPURST#)
CPU
ITP
HOST
HUB LINK
U61C
MONTARA-GM
U61A
DDR MEMORY
MONTARA-GM
Close to pin
change for MGM+
HXRCOMP,HYRCOMP as 18mil wide trace
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Title
Montara (1 of 3)
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FOR MGM+ internal pull down

GST[2:0]	FSB	DDR	Gfx Core Clock Low	Gfx Core Clock High
000	400	266	133	200
001	400	200	100	200
010	400	200	100	133
111	400	333	166	250

DEFAULT NOT USE TV ENCODER

IF USE TV ENCODER ADD R63 ,REMOVE R76 AND R66

change for MGM+

short trace

DDR Feedback(inside the package) Route transitioned to buttom side with vias near ball

SB: for SIV pass

SB:03/03/2004

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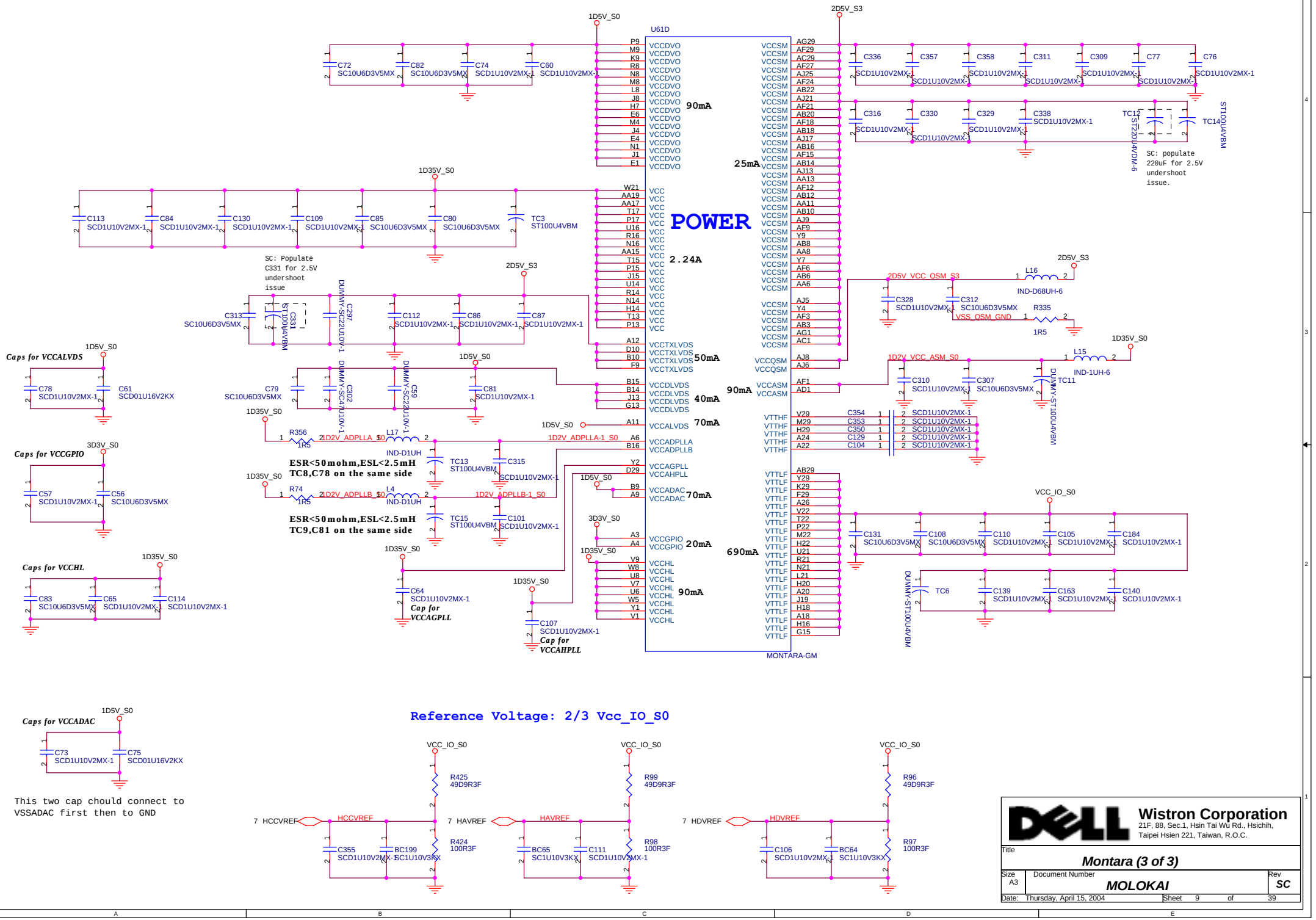
U61D
POWER
MONTARA-GM
1D5V_S0
2D5V_S3
1D35V_S0
3D3V_S0
VCC_IO_S0
90mA
25mA
2.24A
50mA
40mA
70mA
20mA
690mA
Caps for VCCALVDS
Caps for VCCGPIO
Caps for VCCHL
Caps for VCCADAC
Caps for VCCAGPLL
Caps for VCCAHPLL
ESR<50mohm,ESL<2.5mH
TC8,C78 on the same side
ESR<50mohm,ESL<2.5mH
TC9,C81 on the same side
SC: Populate C331 for 2.5V undershoot issue
SC: populate 220uF for 2.5V undershoot issue.
This two cap chould connect to VSSADAC first then to GND
Reference Voltage: 2/3 Vcc_IO_S0
HCCVREF
HAVREF
HDVREF
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DIMM1

DM1

REVERSE TYPE

SKTSODIMM200-1U1
62.10017.311

Top Side

DIMM2

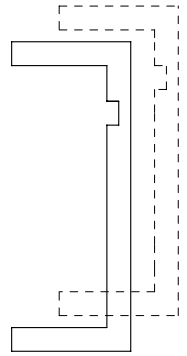
Use old symbol change PN only

DM2

NORMAL TYPE

SKT-SODIMM200-7U
62.10024.481

BOT side



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1D25V_S0

0.01u_25V*24,0402-X7R

BC47 SCD01U16V2KX
BC49 SCD01U16V2KX
BC40 SCD01U16V2KX
BC36 SCD01U16V2KX
BC35 SCD01U16V2KX
BC37 SCD01U16V2KX
BC39 SCD01U16V2KX
BC42 SCD01U16V2KX
BC41 SCD01U16V2KX
BC38 SCD01U16V2KX
BC60 SCD01U16V2KX
BC59 SCD01U16V2KX

BC58 SCD01U16V2KX
BC62 SCD01U16V2KX
BC61 SCD01U16V2KX
BC51 SCD01U16V2KX
BC52 SCD01U16V2KX
BC46 SCD01U16V2KX
BC48 SCD01U16V2KX
BC50 SCD01U16V2KX
BC72 SCD01U16V2KX
BC73 SCD01U16V2KX
BC69 SCD01U16V2KX
BC67 SCD01U16V2KX

0.1u_10V*24,0402-X5R

BC55 SCD1U10V2MX-1
BC57 SCD1U10V2MX-1
BC84 SCD1U10V2MX-1
BC82 SCD1U10V2MX-1
BC83 SCD1U10V2MX-1
BC85 SCD1U10V2MX-1
BC78 SCD1U10V2MX-1
BC81 SCD1U10V2MX-1
BC71 SCD1U10V2MX-1
BC74 SCD1U10V2MX-1
BC68 SCD1U10V2MX-1
BC70 SCD1U10V2MX-1

BC92 SCD1U10V2MX-1
BC96 SCD1U10V2MX-1
BC95 SCD1U10V2MX-1
BC94 SCD1U10V2MX-1
BC91 SCD1U10V2MX-1
BC93 SCD1U10V2MX-1
BC97 SCD1U10V2MX-1
BC77 SCD1U10V2MX-1
BC80 SCD1U10V2MX-1
BC79 SCD1U10V2MX-1
BC66 SCD1U10V2MX-1
BC56 SCD1U10V2MX-1

FOR DDR SKTS POWER PIN
10u_6.3V*1,0805-X5R
0.1u_10V*24,0402-X5R

2D5V_S3

C360 SC10U6D3V5MX
BC185 SCD1U10V2MX-1
BC191 SCD1U10V2MX-1
BC192 SCD1U10V2MX-1
BC193 SCD1U10V2MX-1
BC201 SCD1U10V2MX-1
BC203 SCD1U10V2MX-1
BC202 SCD1U10V2MX-1
BC204 SCD1U10V2MX-1

BC187 SCD1U10V2MX-1
BC184 SCD1U10V2MX-1
BC181 SCD1U10V2MX-1
BC182 SCD1U10V2MX-1
BC183 SCD1U10V2MX-1
BC186 SCD1U10V2MX-1
BC180 SCD1U10V2MX-1
BC195 SCD1U10V2MX-1

BC194 SCD1U10V2MX-1
C66 SCD1U10V2MX-1
C314 SCD1U10V2MX-1
C333 SCD1U10V2MX-1
C319 SCD1U10V2MX-1
C318 SCD1U10V2MX-1
C317 SCD1U10V2MX-1
C332 SCD1U10V2MX-1

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Title: ***DDR Decoupling CPA***

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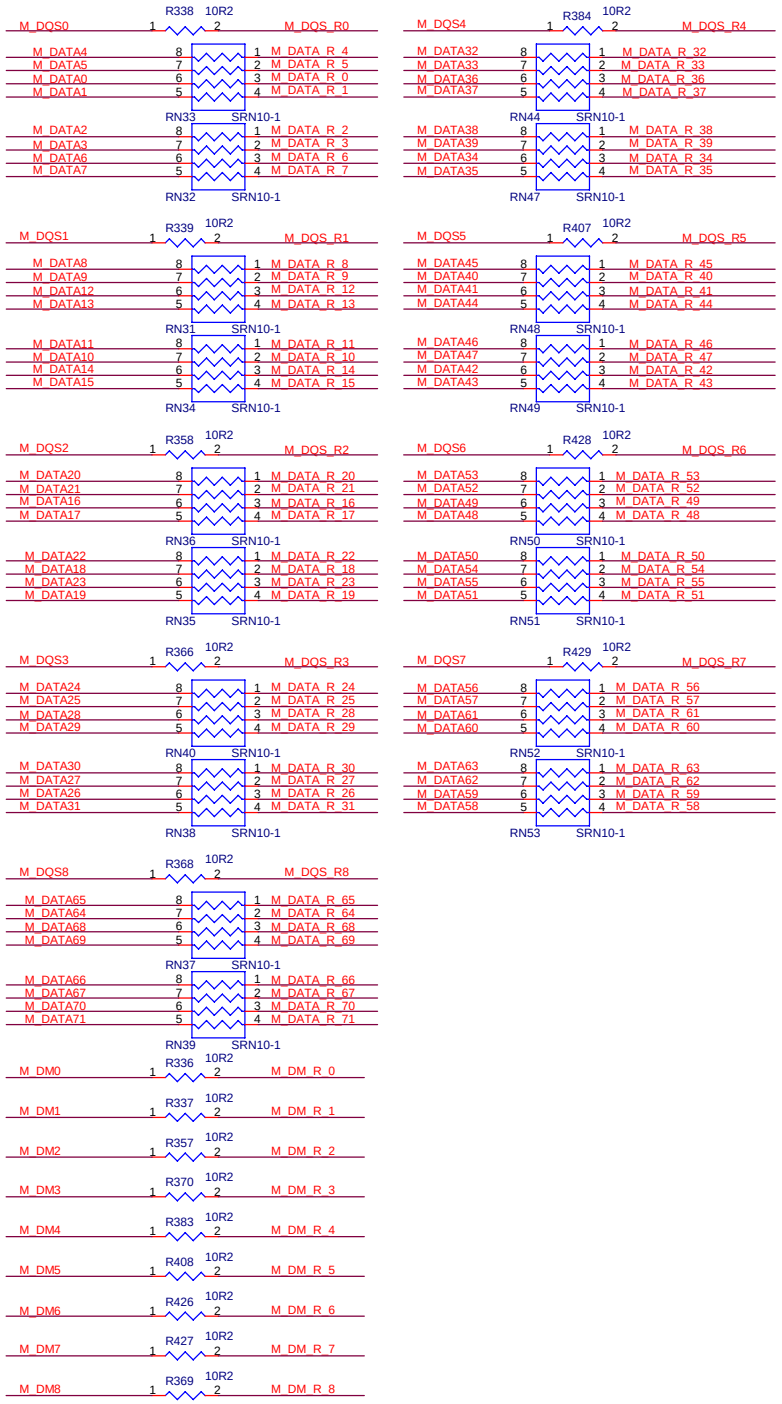
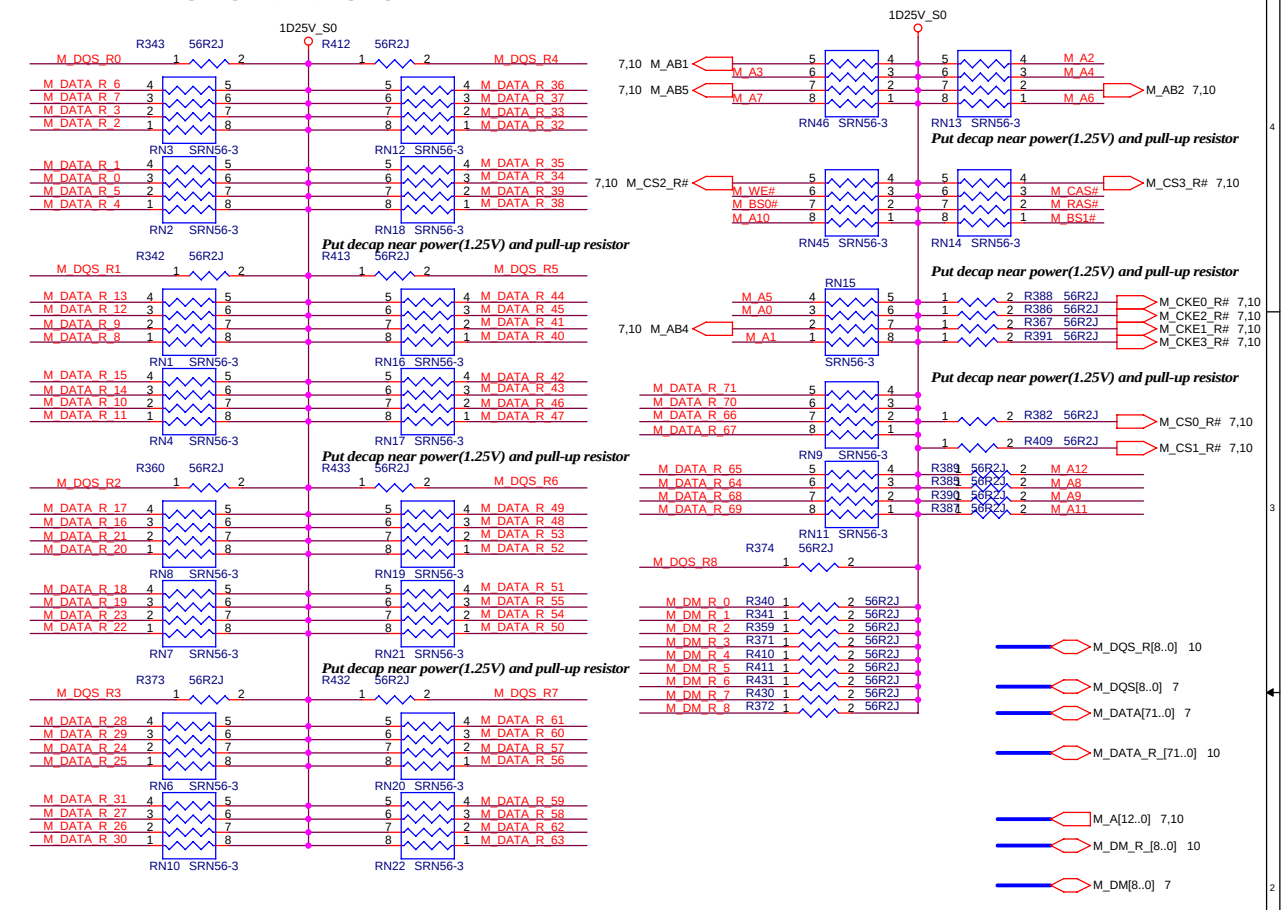
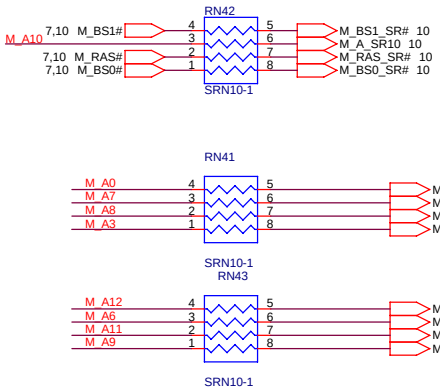
SERIES DAMPING



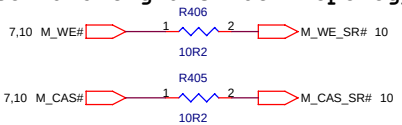
PARALLEL TERMINATION

Put decap near power(1.25V) and pull-up resistor





Command Signals USE Topology 2



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Title: *DDR Serial/Terminator Resistor*

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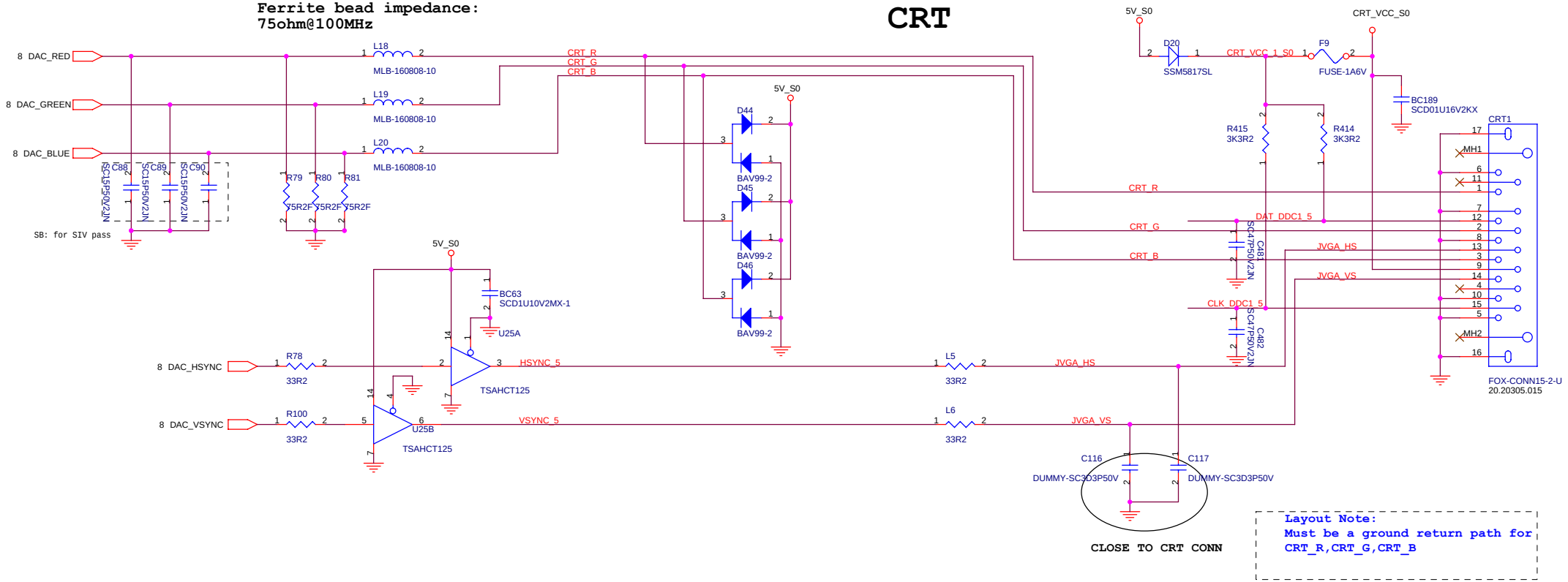
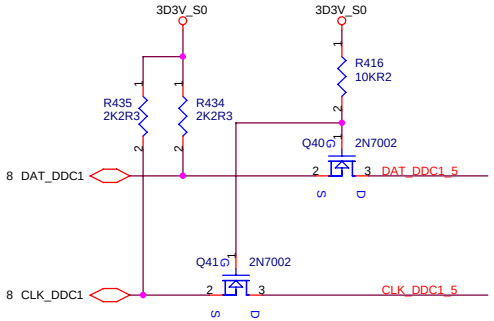
CRT

Ferrite bead impedance:
75ohm@100MHz



Layout Note:
Must be a ground return path for CRT_R,CRT_G,CRT_B

DDC_CLK & DATE LEVEL SHIFT



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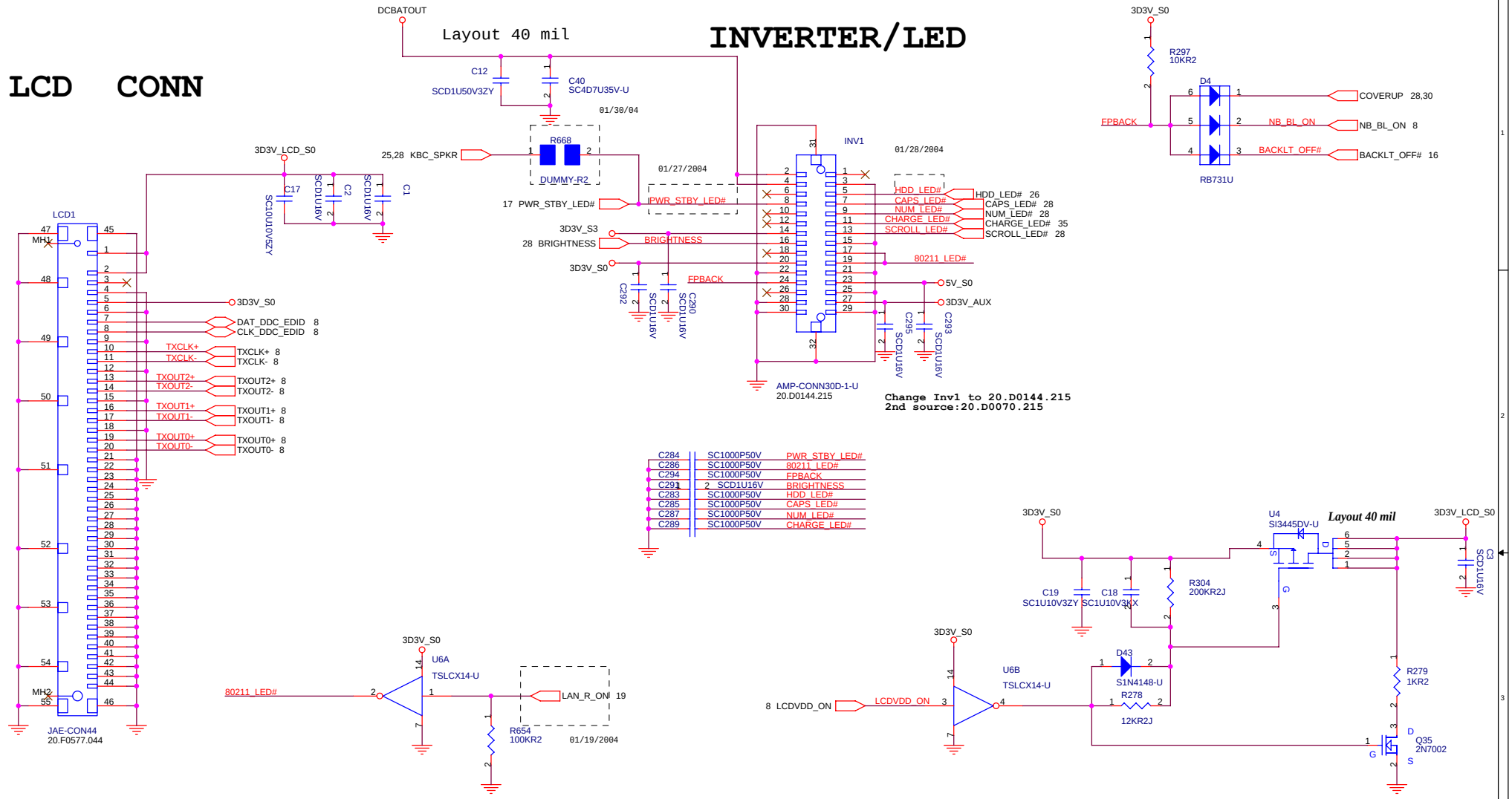
LCD CONN

INVERTER/LED



	S0/S1	S3	S4	S5	Functions	when LID is closed
Power On / Battery Low LED (PWR_LED#)	LOW	HIGH	HIGH	HIGH		readable
Sleep / Waking LED (STDBY_LED#)	HIGH	LOW	HIGH	HIGH	(Don't flash during waking)	readable
Disk Media (MEDIA_LED#)					HDD,ODD access indicator	not readable
Charging LED (CHARGE_LED#)					On when charging. Flashing when charging error is occured.	not readable
Wireless LED (80211_LED#)					On when wireless is On	not readable
NUM Lock (NUM_LED#)					On when Number key is locked	not readable
CAPS Lock (MEDIA_LED#)					On when Caps lock is On	not readable

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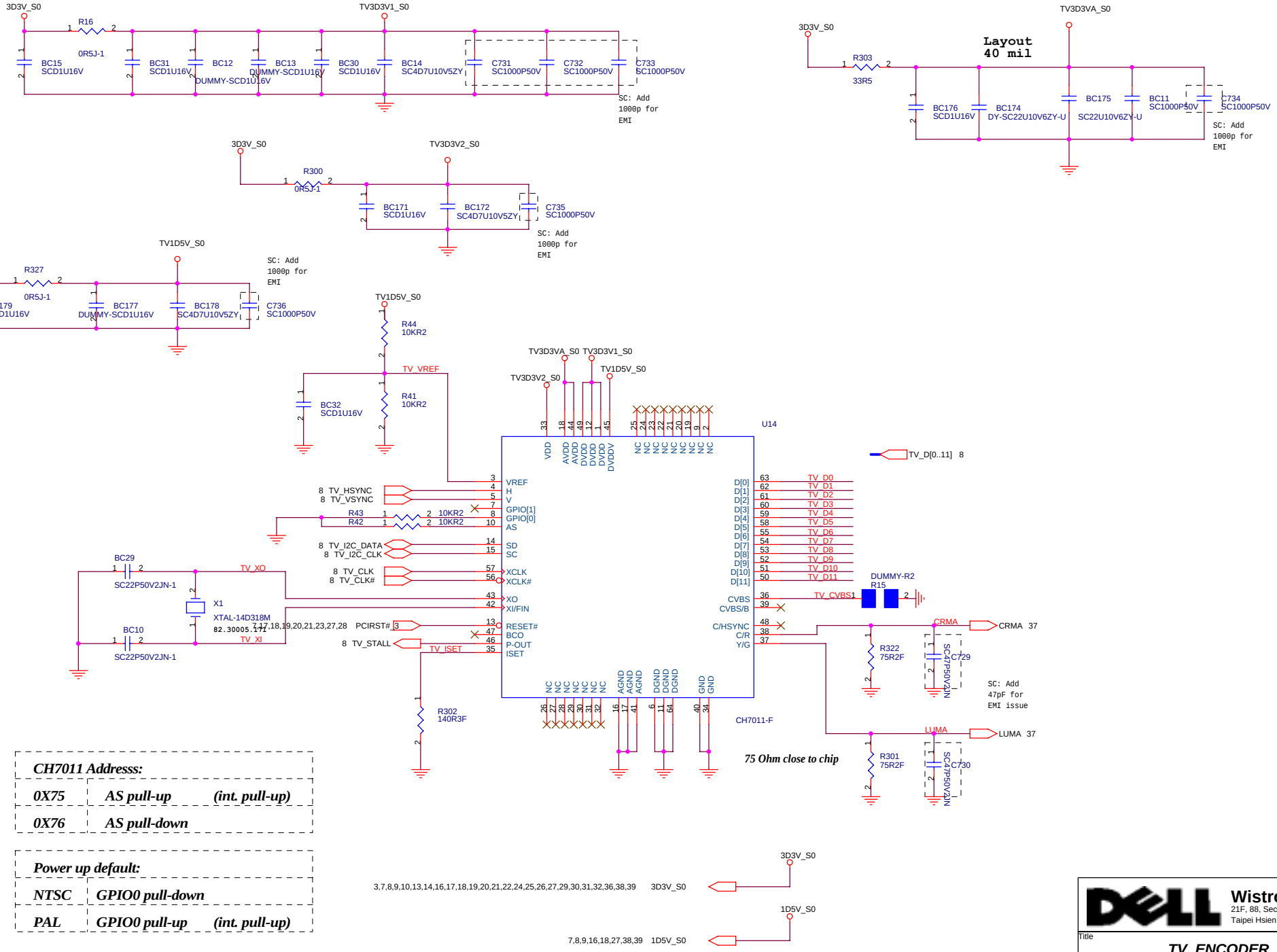
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD CONN & INVERTER

Size: A3 | Document Number: MOLOKAI | Rev: SC

Date: Thursday, April 15, 2004 | Sheet 14 of 39



CH7011 Addresss:		
0X75	AS pull-up	(int. pull-up)
0X76	AS pull-down	

Power up default:		
NTSC	GPIO0 pull-down	
PAL	GPIO0 pull-up	(int. pull-up)

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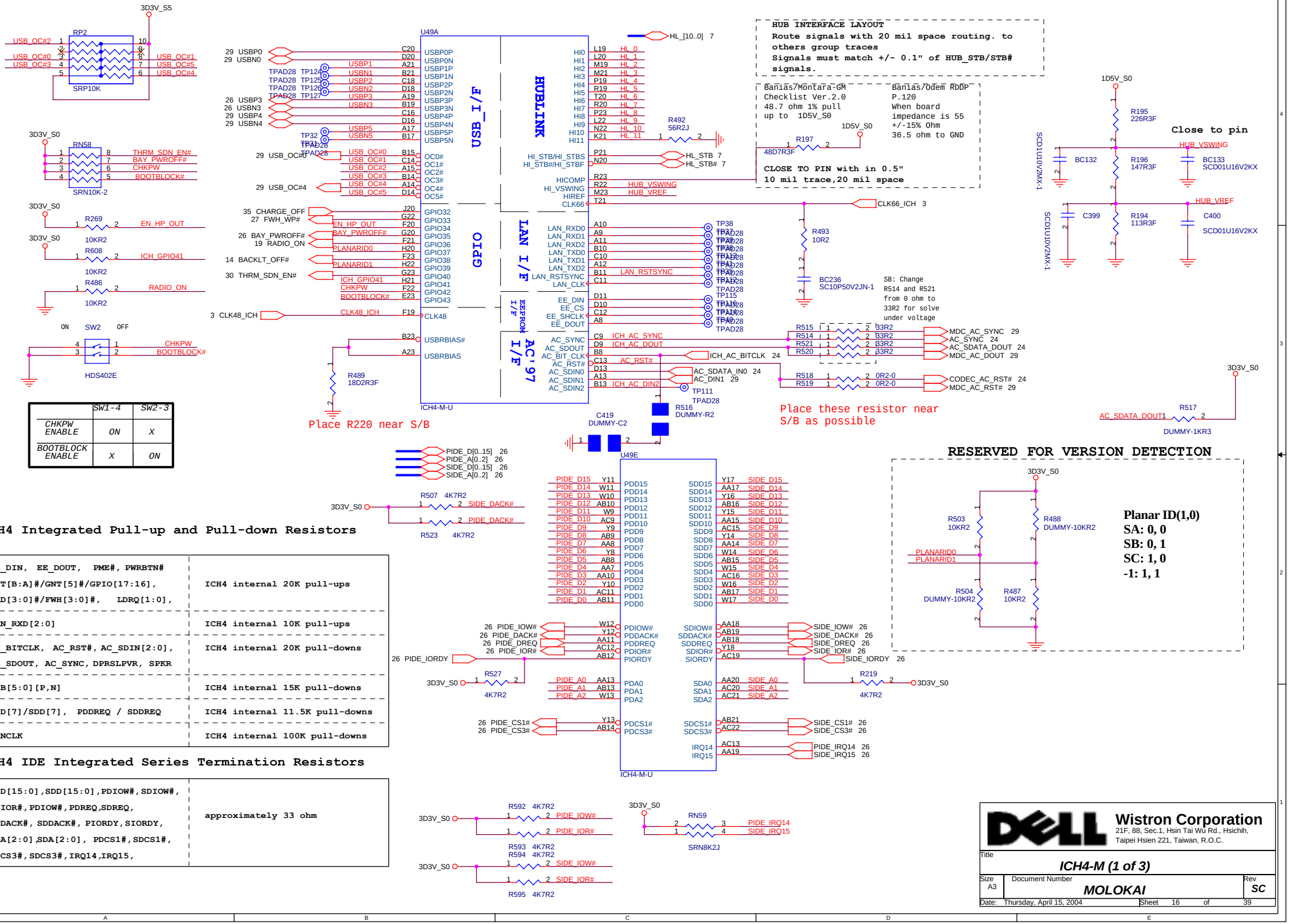
Taipei Hsien 221, Taiwan, R.O.C.

Title: TV_ENCODER

Size: A3 | Document Number: MOLOKAI | Rev: SC

Date: Thursday, April 15, 2004 | Sheet 15 of 39

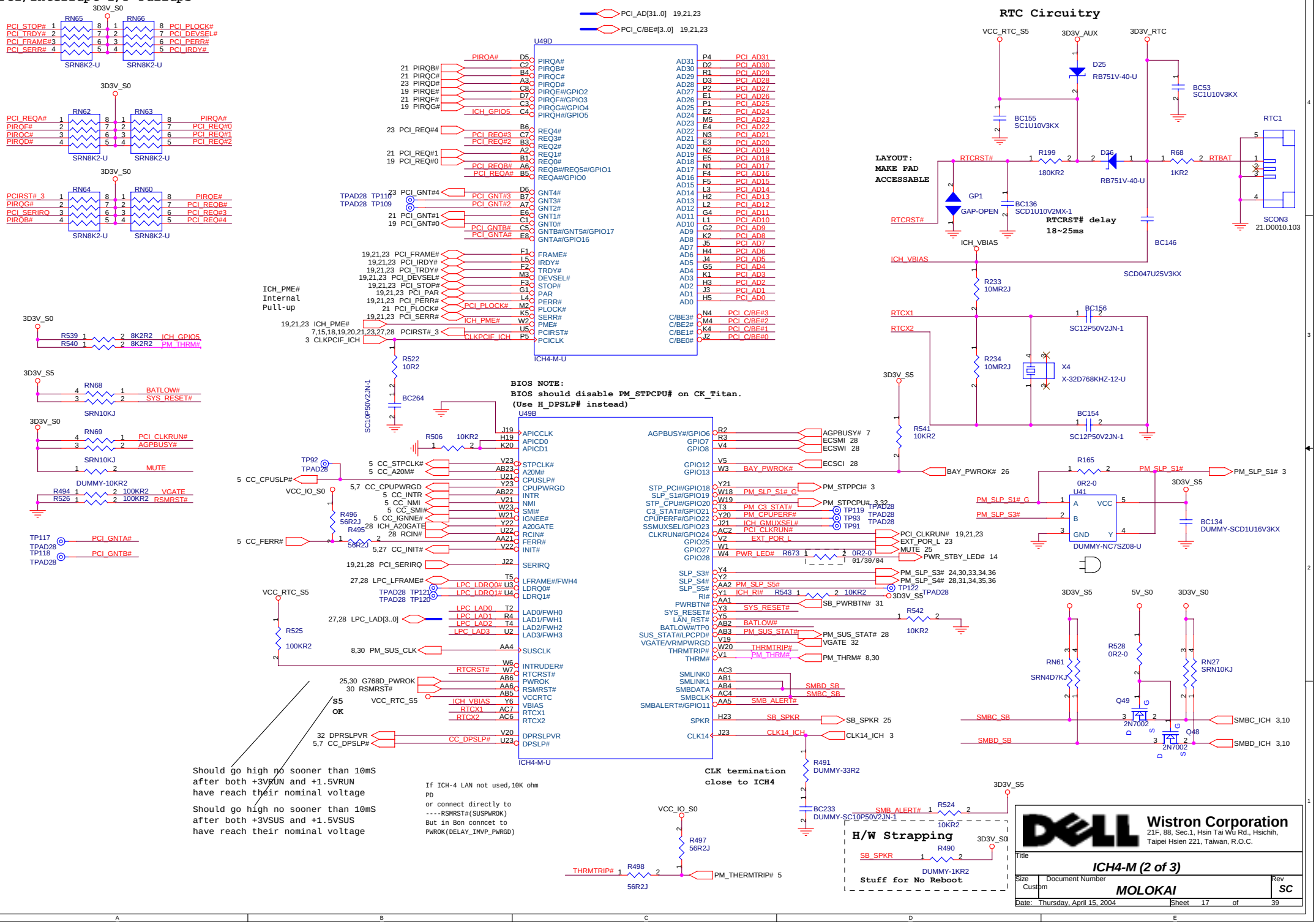


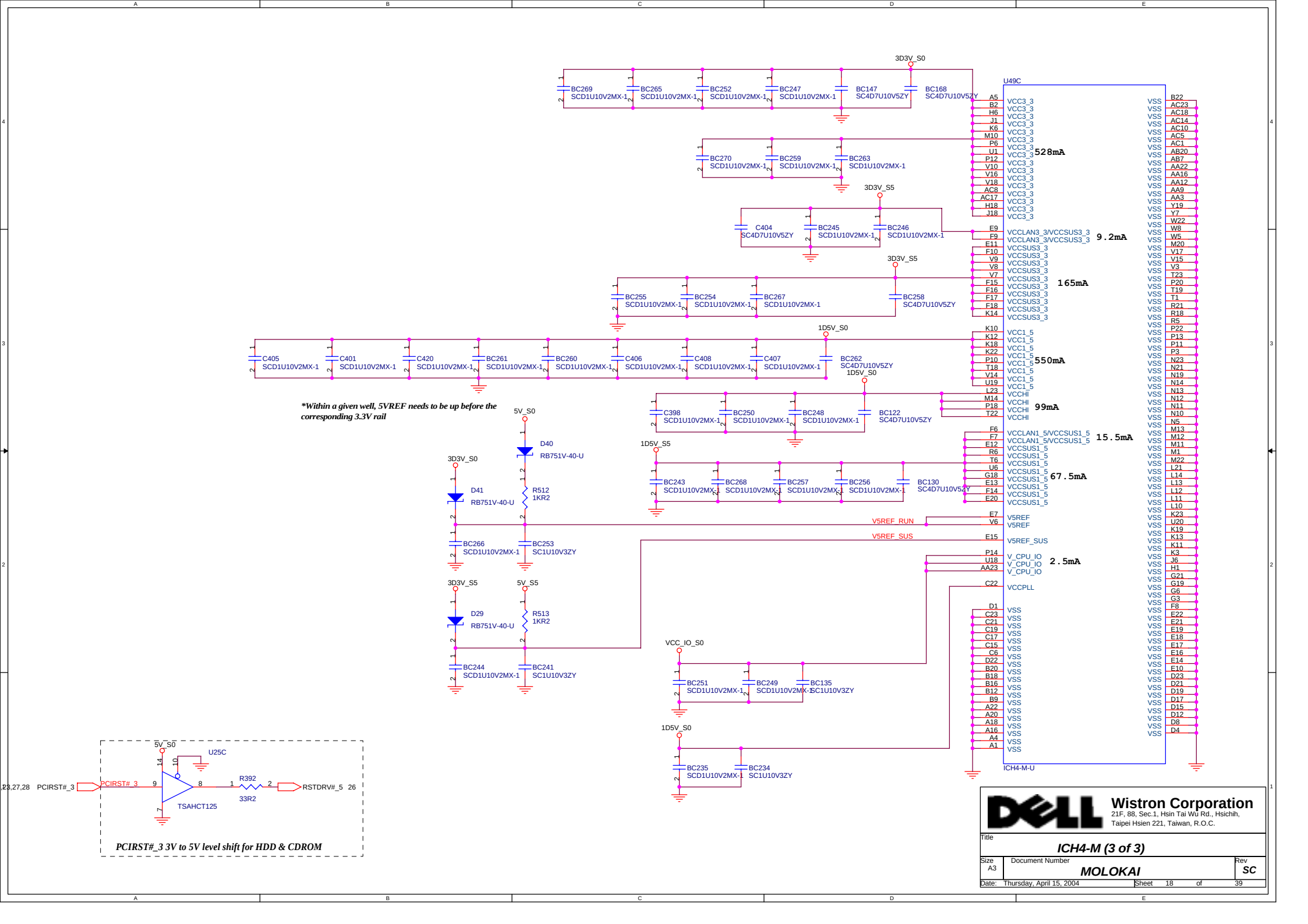
	SW1-4	SW2-3
CHKPW ENABLE	ON	X
BOOTBLOCK ENABLE	X	ON

EE_DIN, EE_DOUT, PME#, PWRBTN# GNT[B:A]#/GNT[5]#/GPIO[17:16], LAD[3:0]#/FWH[3:0]#, LDRQ[1:0],	ICH4 internal 20K pull-ups
LAN_RXD[2:0]	ICH4 internal 10K pull-ups
AC_BITCLK, AC_RST#, AC_SDIN[2:0], AC_SDOUT, AC_SYNC, DPRSLPVR, SPKR	ICH4 internal 20K pull-downs
USB[5:0][P,N]	ICH4 internal 15K pull-downs
PDD[7]/SDD[7], PDDREQ / SDDREQ	ICH4 internal 11.5K pull-downs
LANCLK	ICH4 internal 100K pull-downs

PDD[15:0],SDD[15:0],PDIOW#,SDIOW#, PDIOR#,PDIOW#,PDREQ,SDREQ, PDDACK#, SDDACK#, PIORDY,SIORDY, PDA[2:0],SDA[2:0], PDCS1#,SDCS1#, PDCS3#,SDCS3#,IRQ14,IRQ15,	approximately 33 ohm

PCI/Interrupt I/F Pullups





Wistron Corporation
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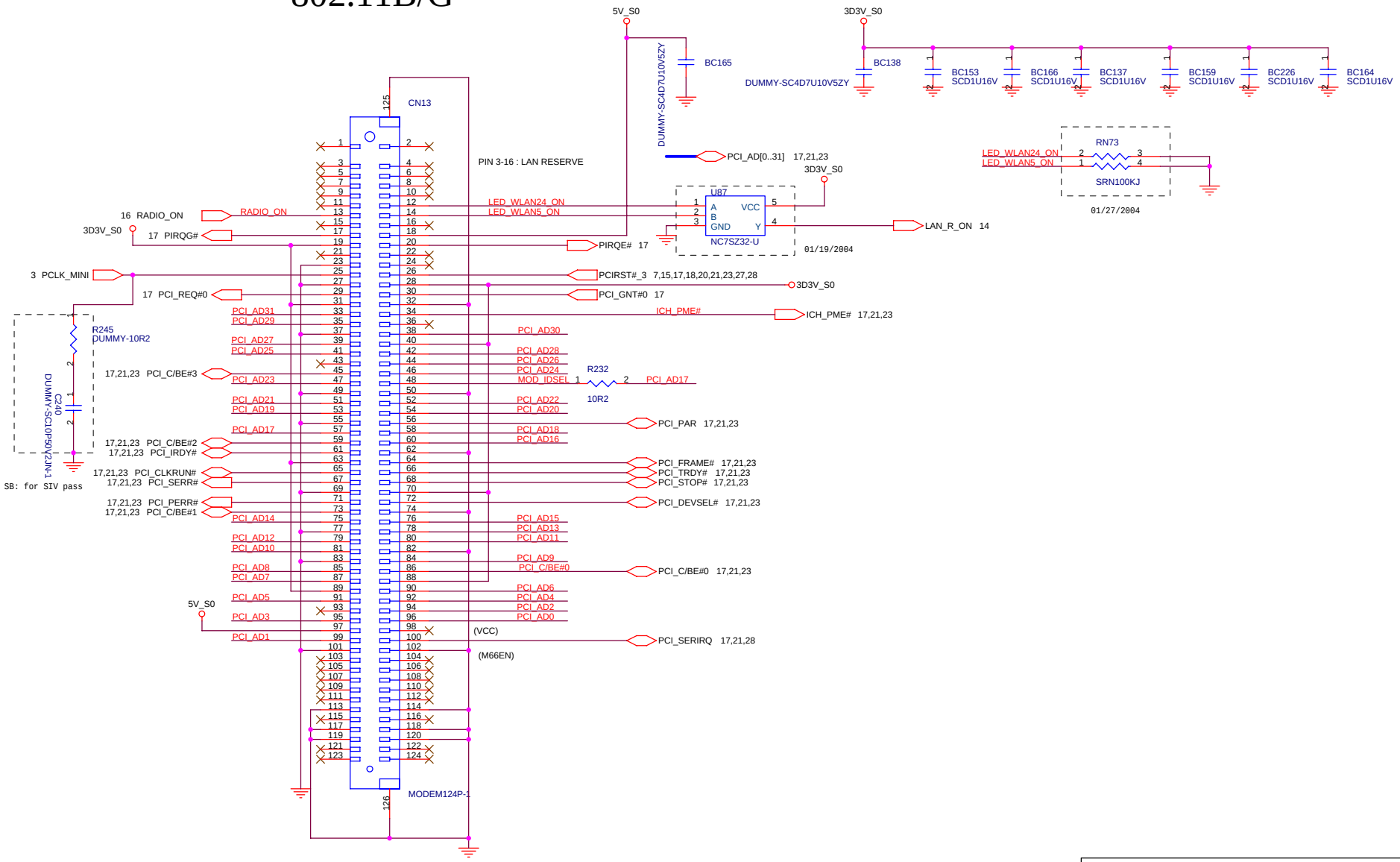
Title: ICH4-M (3 of 3)

Size: A3 | Document Number: MOLOKAI | Rev: SC

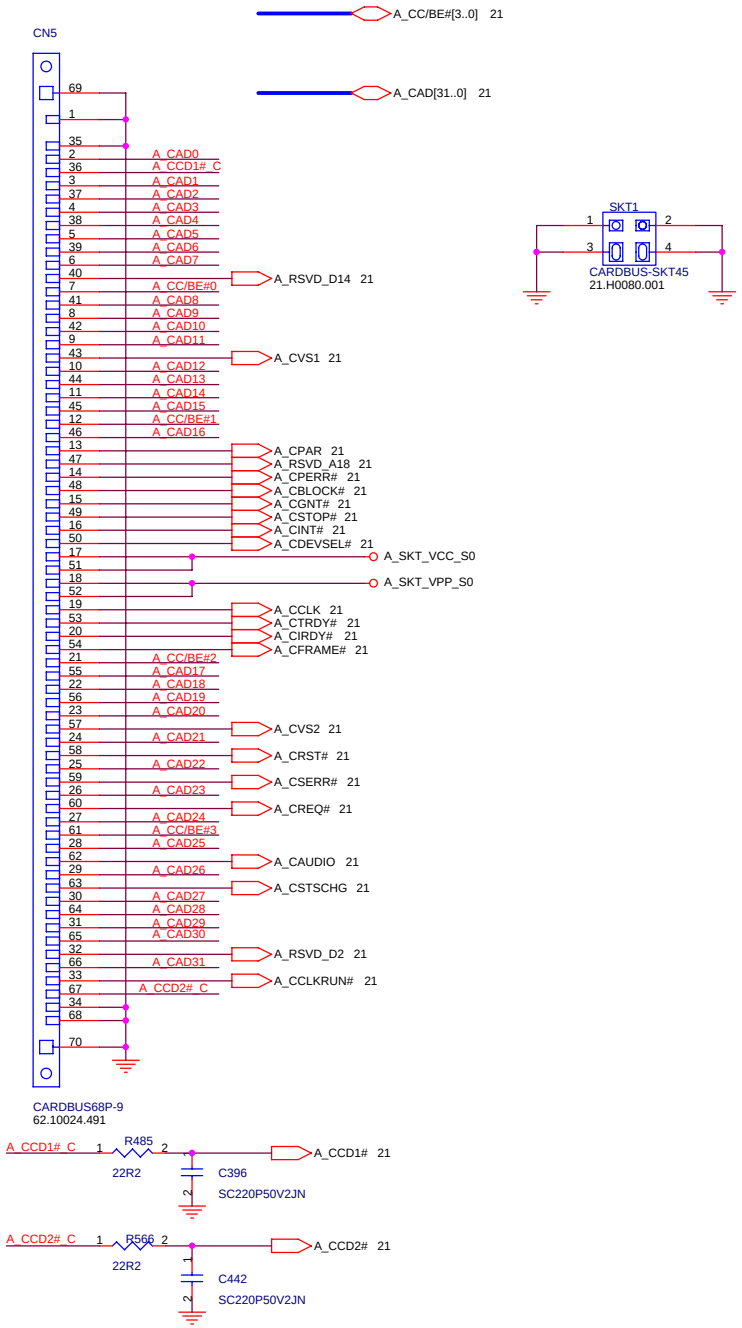
Date: Thursday, April 15, 2004 | Sheet 18 of 39

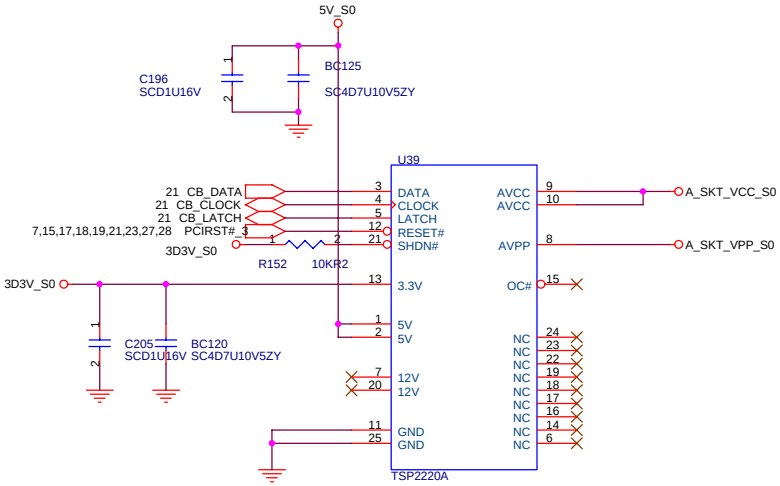
Mini PCI
802.11B/G

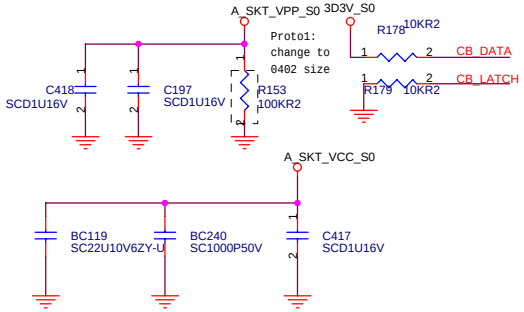


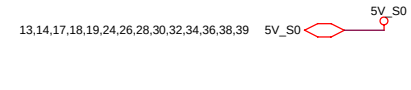
Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *Mini PCI Socket*		
Size: A3	Document Number: *MOLOKAI*	Rev: *SC*
Date: Thursday, April 15, 2004	Sheet 19 of 39	

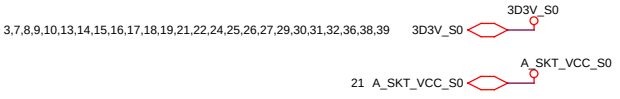
PCMCIA socket











Wistron Corporation
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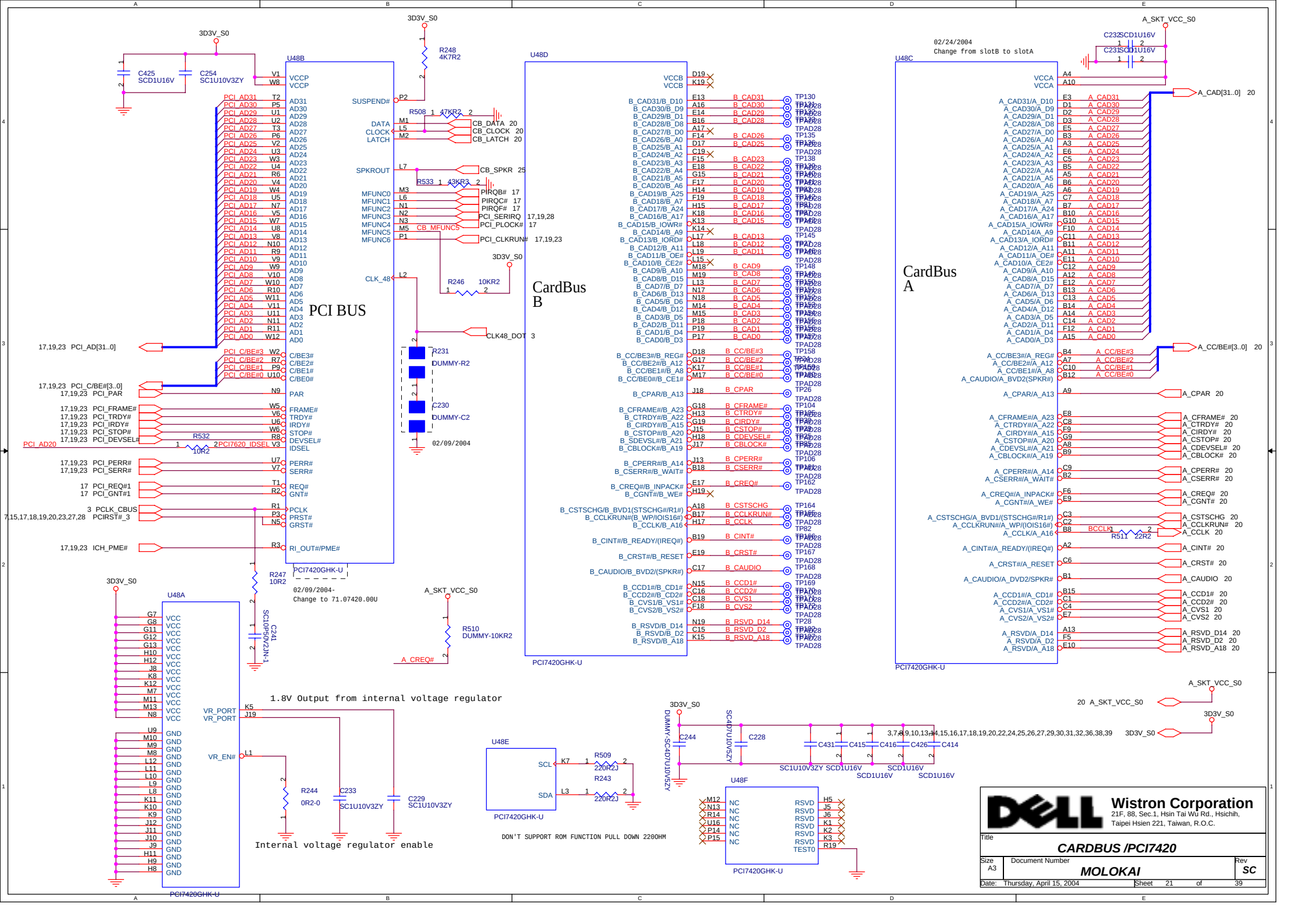
Taipei Hsien 221, Taiwan, R.O.C.

Title	***CARDBUS CONN / PWR SW***	
Size: A3	Document Number: ***MOLOKAI***	Rev: ***SC***
Date: Wednesday, April 14, 2004	Sheet 20 of 39	


PCI BUS
U48B
PCI7420GHK-U
CardBus B
U48D
CardBus A
U48C
02/24/2004
Change from slotB to slotA
02/09/2004-
Change to 71.07420.00U
02/09/2004
U48A
1.8V Output from internal voltage regulator
Internal voltage regulator enable
U48E
U48F
DON'T SUPPORT ROM FUNCTION PULL DOWN 220OHM
Wistron Corporation
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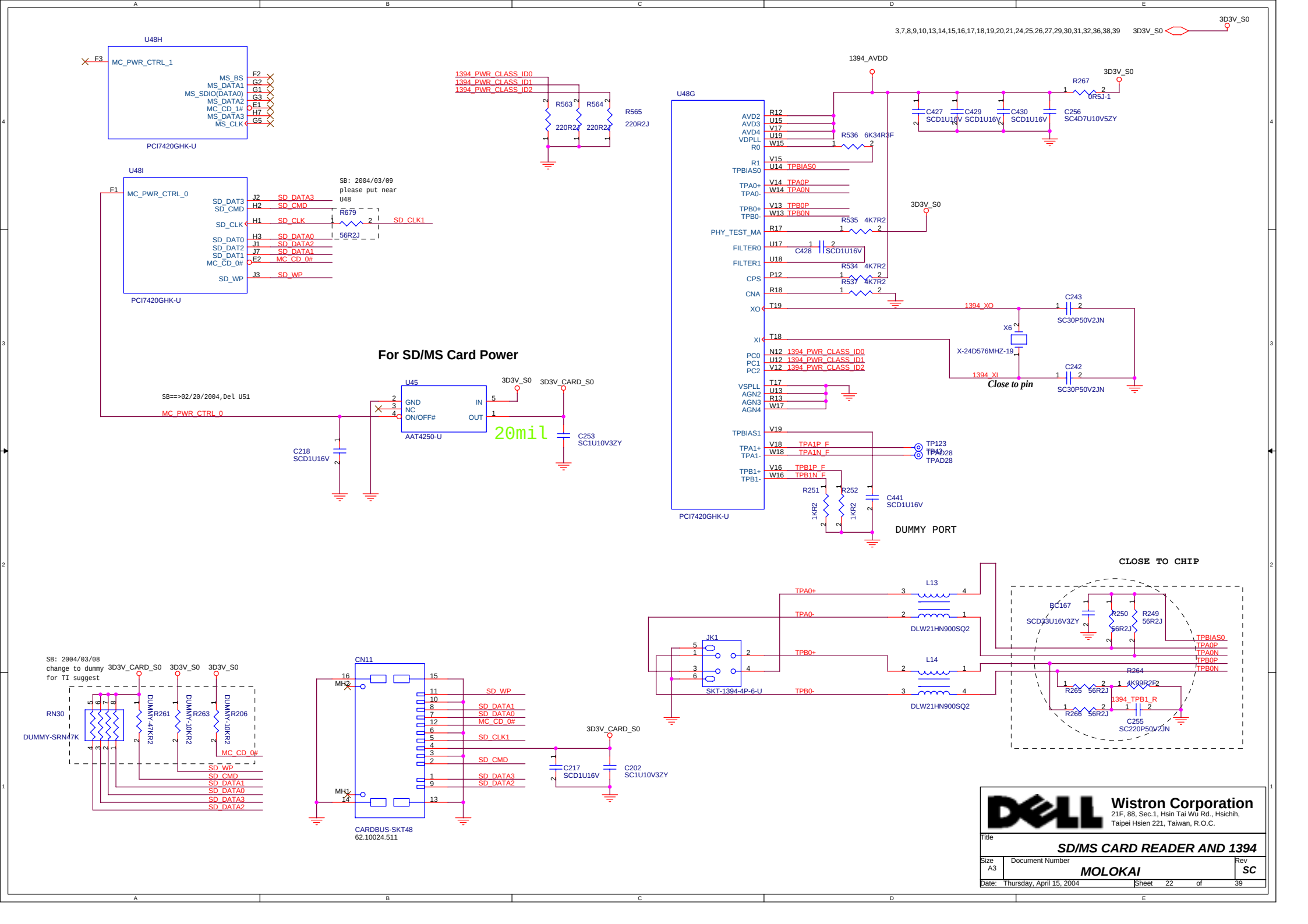
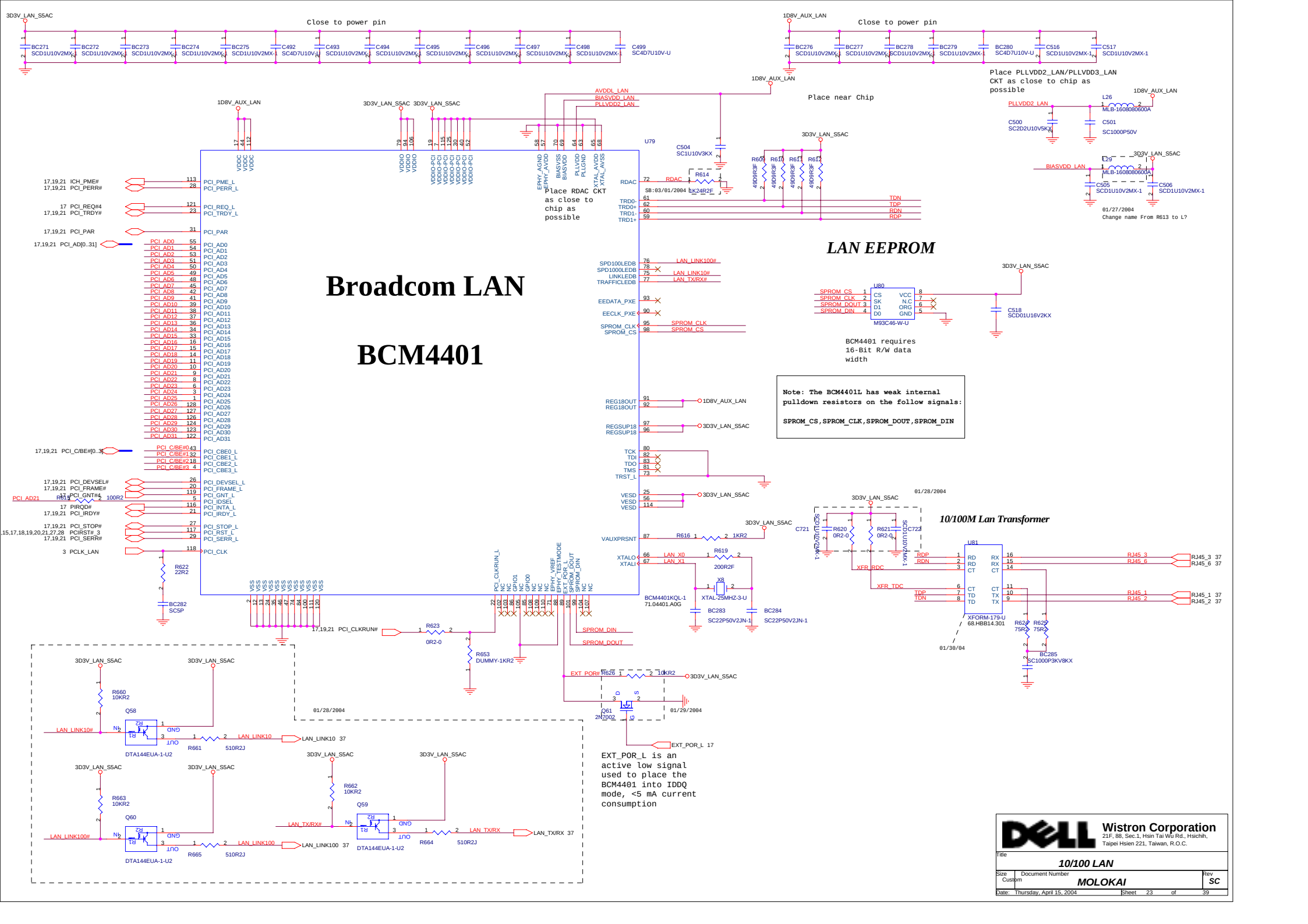
Taipei Hsien 221, Taiwan, R.O.C.
Title
CARDBUS /PCI7420
Size A3
Document Number
MOLOKAI
Rev SC
Date: Thursday, April 15, 2004
Sheet 21 of 39


3D3V_S0
3,7,8,9,10,13,14,15,16,17,18,19,20,21,24,25,26,27,29,30,31,32,36,38,39
3D3V_S0
U48H
F3
MC_PWR_CTRL_1
MS_BS F2
MS_DATA1 G2
MS_SDIO(DATA0) G1
MS_DATA2 G3
MC_CD_1# E1
MS_DATA3 H7
MS_CLK G5
PCI7420GHK-U
1394_PWR_CLASS_ID0
1394_PWR_CLASS_ID1
1394_PWR_CLASS_ID2
R563 220R2J
R564 220R2J
R565 220R2J
1394_AVDD
3D3V_S0
R267 0R5J-1
U48G
AVD2 R12
AVD3 U15
AVD4 V17
VDPLL U19
R0 W15
R536 6K34R3F
C427 SCD1U16V
C429 SCD1U16V
C430 SCD1U16V
C256 SC4D7U10V5ZY
R1 V15
TPBIAS0 U14 TPBIAS0
TPA0+ V14 TPA0P
TPA0- W14 TPA0N
TPB0+ V13 TPB0P
TPB0- W13 TPB0N
PHY_TEST_MA R17
R535 4K7R2
3D3V_S0
FILTER0 U17
C428 SCD1U16V
FILTER1 U18
R534 4K7R2
CPS P12
R537 4K7R2
CNA R18
XO T19
1394_XO
C243 SC30P50V2JN
X6
X-24D576MHZ-19
XI T18
1394_XI
C242 SC30P50V2JN
Close to pin
PC0 N12 1394_PWR_CLASS_ID0
PC1 U12 1394_PWR_CLASS_ID1
PC2 V12 1394_PWR_CLASS_ID2
VSPLL T17
AGN2 U13
AGN3 R13
AGN4 W17
TPBIAS1 V19
TPA1+ V18 TPA1P_F
TPA1- W18 TPA1N_F
TP123 TPA2
TPAD28
TPB1+ V16 TPB1P_F
TPB1- W16 TPB1N_F
R251 1KR2
R252 1KR2
C441 SCD1U16V
PCI7420GHK-U
DUMMY PORT
U48I
F1
MC_PWR_CTRL_0
SD_DAT3 J2 SD_DATA3
SD_CMD H2 SD_CMD
SD_CLK H1 SD_CLK
R679 56R2J
SD_CLK1
SD_DAT0 H3 SD_DATA0
SD_DAT2 J1 SD_DATA2
SD_DAT1 J7 SD_DATA1
MC_CD_0# E2 MC_CD_0#
SD_WP J3 SD_WP
PCI7420GHK-U
SB: 2004/03/09
please put near
U48
For SD/MS Card Power
SB==>02/20/2004,Del U51
MC_PWR_CTRL_0
U45
GND
NC
ON/OFF#
IN
OUT
AAT4250-U
3D3V_S0
3D3V_CARD_S0
20mil
C218 SCD1U16V
C253 SC1U10V3ZY
CLOSE TO CHIP
TPA0+
TPA0-
TPB0+
TPB0-
L13
L14
DLW21HN900SQ2
DLW21HN900SQ2
JK1
SKT-1394-4P-6-U
BC167 SCD33U16V3ZY
R250 56R2J
R249 56R2J
R264 4K99R2F2
R265 56R2J
R266 56R2J
1394_TPB1_R
C255 SC220P50V2JN
TPBIAS0
TPA0P
TPA0N
TPB0P
TPB0N
SB: 2004/03/08
change to dummy
for TI suggest
3D3V_CARD_S0
3D3V_S0
3D3V_S0
RN30
DUMMY-SRN47K
DUMMY-47KR2
R261
DUMMY-10KR2
R263
DUMMY-10KR2
R206
MC_CD_0#
SD_WP
SD_CMD
SD_DATA1
SD_DATA0
SD_DATA3
SD_DATA2
CN11
MH2
MH1
CARDBUS-SKT48
62.10024.511
SD_WP
SD_DATA1
SD_DATA0
MC_CD_0#
SD_CLK1
SD_CMD
SD_DATA3
SD_DATA2
3D3V_CARD_S0
C217 SCD1U16V
C202 SC1U10V3ZY
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
SD/MS CARD READER AND 1394
Size A3
Document Number
MOLOKAI
Rev SC
Date: Thursday, April 15, 2004
Sheet 22 of 39


Broadcom LAN
BCM4401
LAN EEPROM
10/100M Lan Transformer
Close to power pin
Place near Chip
Place RDAC CKT as close to chip as possible
Place PLLVDD2_LAN/PLLVDD3_LAN CKT as close to chip as possible
BCM4401 requires 16-Bit R/W data width
Note: The BCM4401L has weak internal pulldown resistors on the follow signals:
SPROM_CS,SPROM_CLK,SPROM_DOUT,SPROM_DIN
EXT_POR_L is an active low signal used to place the BCM4401 into IDDQ mode, <5 mA current consumption
Wistron Corporation
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10/100 LAN
MOLOKAI
Thursday, April 15, 2004
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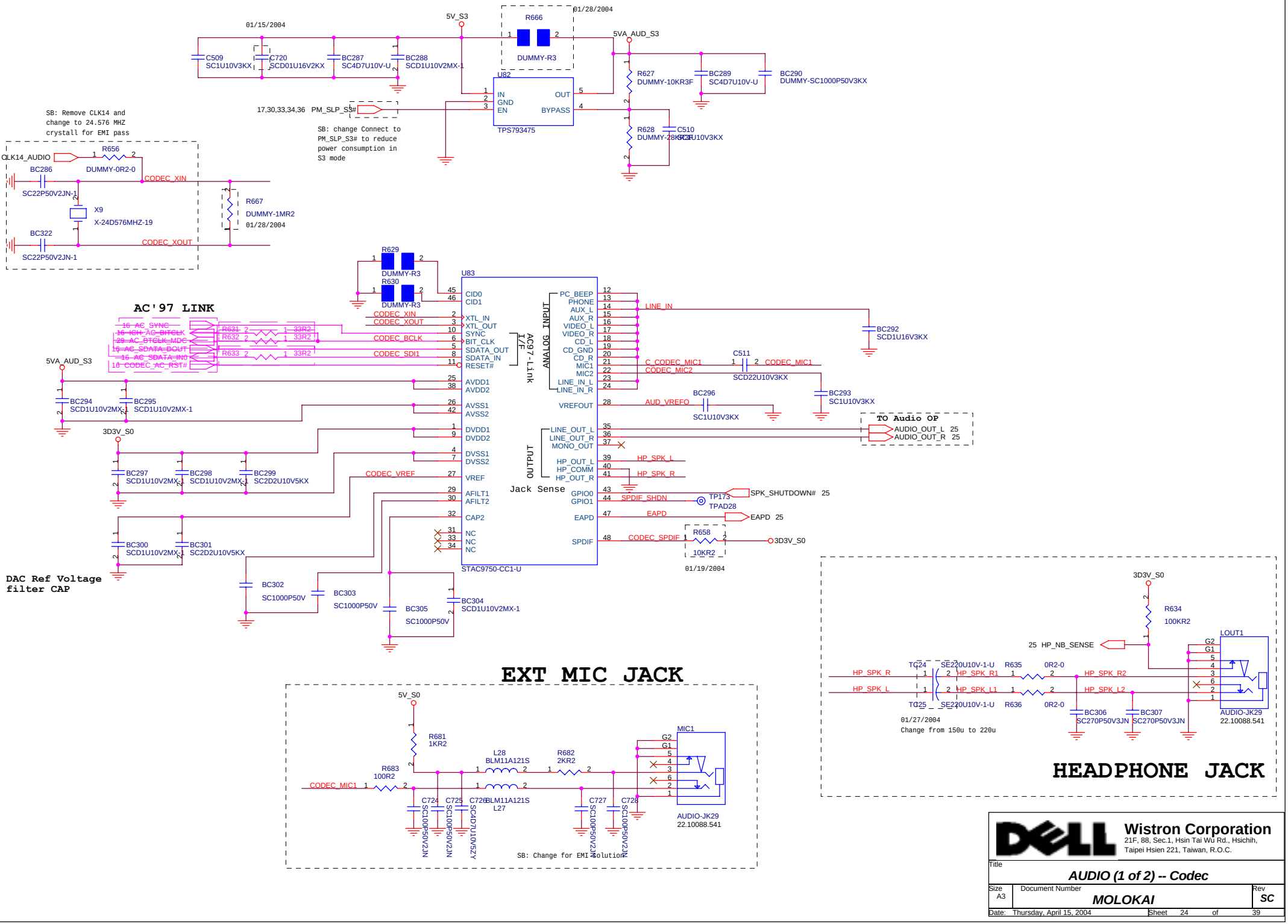
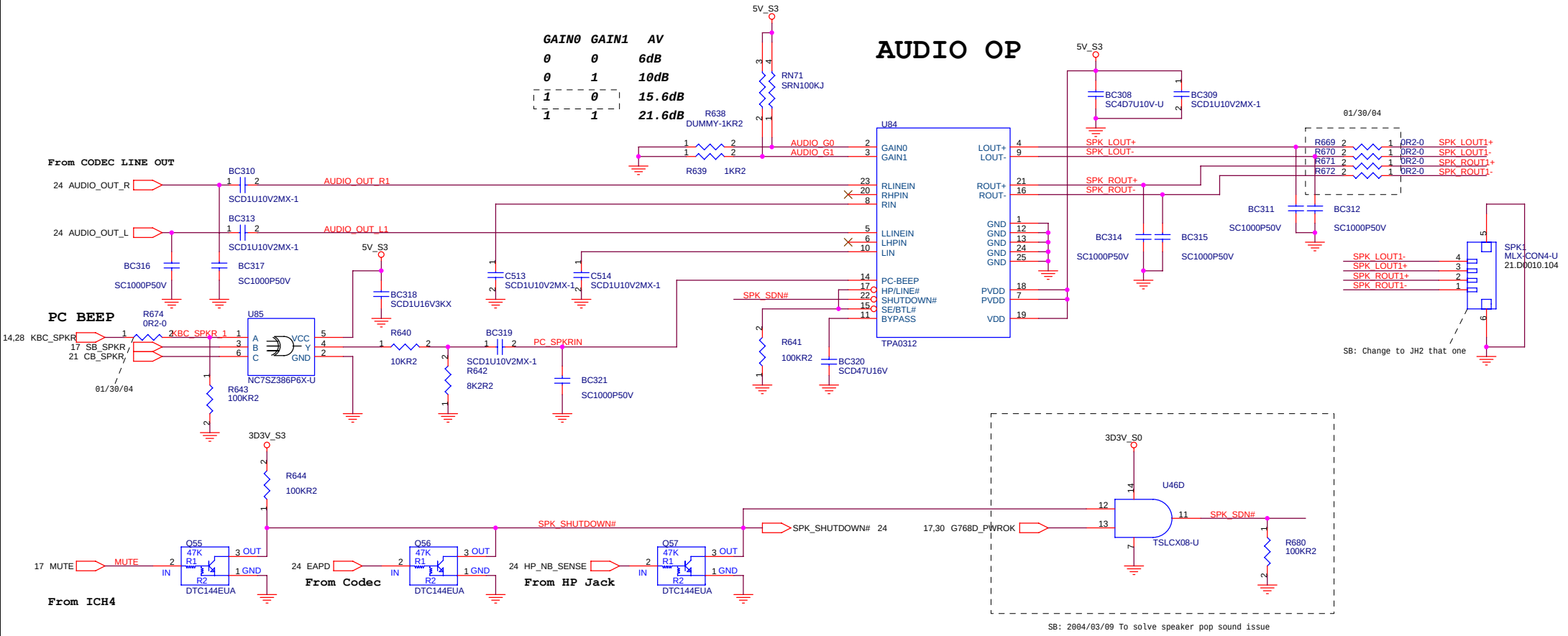
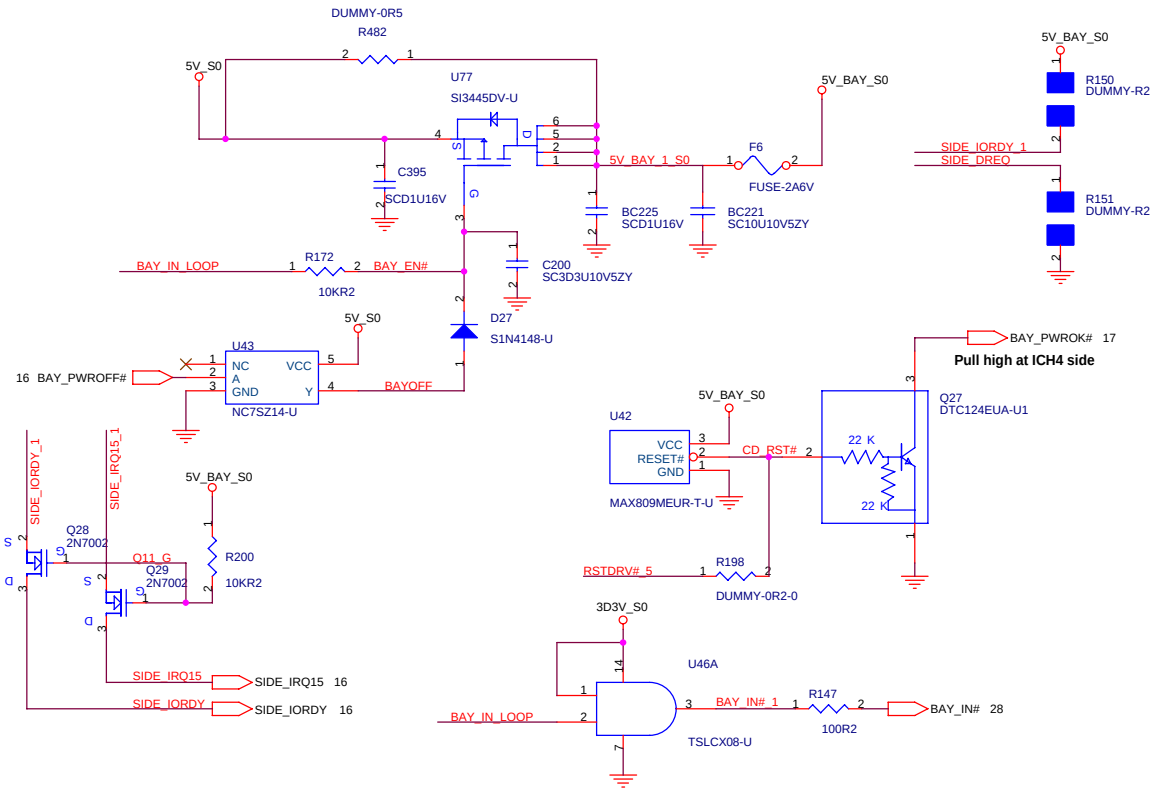
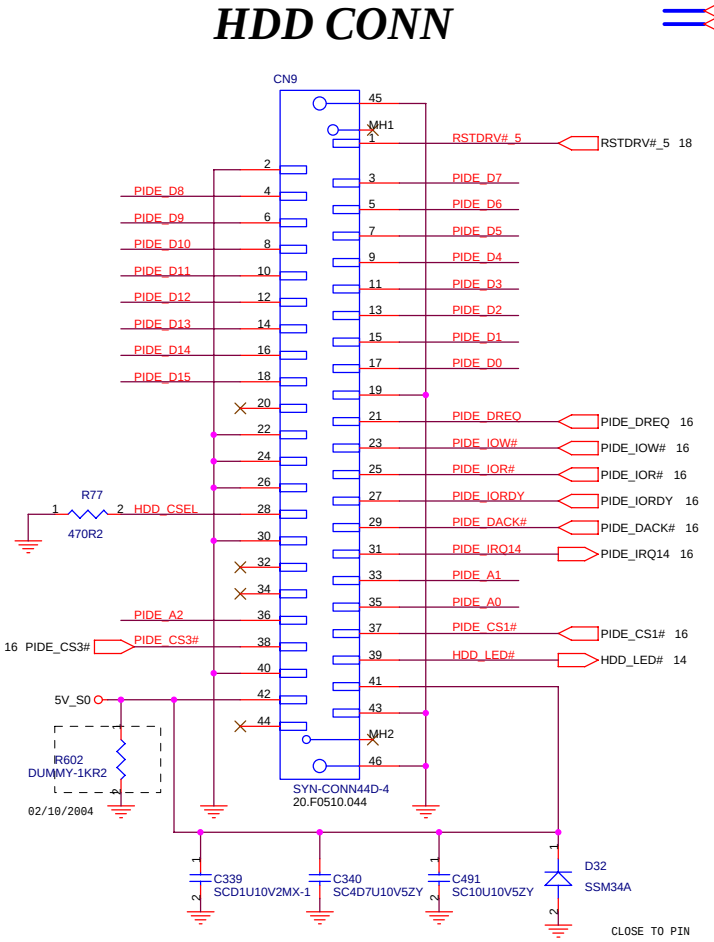

01/15/2004
5V_S3
R666
01/28/2004
5VA_AUD_S3
C509 SC1U10V3KX
C720 SCD01U16V2KX
BC287 SC4D7U10V-U
BC288 SCD1U10V2MX-1
DUMMY-R3
U82
IN
GND
EN
OUT
BYPASS
TPS793475
R627 DUMMY-10KR3F
BC289 SC4D7U10V-U
BC290 DUMMY-SC1000P50V3KX
17,30,33,34,36 PM_SLP_S3#
SB: change Connect to PM_SLP_S3# to reduce power consumption in S3 mode
R628 DUMMY-28KR3F
C510 SC1U10V3KX
SB: Remove CLK14 and change to 24.576 MHZ crystall for EMI pass
3 CLK14_AUDIO
R656 DUMMY-0R2-0
BC286 SC22P50V2JN-1
CODEC_XIN
X9 X-24D576MHZ-19
R667 DUMMY-1MR2 01/28/2004
BC322 SC22P50V2JN-1
CODEC_XOUT
AC'97 LINK
16 AC_SYNC
16 ICH_AC_BITCLK
29 AC_BITCLK_MDC
16 AC_SDATA_OUT
16 AC_SDATA_IN0
16 CODEC_AC_RST#
R631 33R2
R632 33R2
R633 33R2
CODEC_BCLK
CODEC_SDI1
R629 DUMMY-R3
R630 DUMMY-R3
U83
CID0
CID1
CODEC_XIN
CODEC_XOUT
XTL_IN
XTL_OUT
SYNC
BIT_CLK
SDATA_OUT
SDATA_IN
RESET#
AC97-LINK
ANALOG_INPUT
PC_BEEP
PHONE
AUX_L
AUX_R
VIDEO_L
VIDEO_R
CD_L
CD_GND
CD_R
MIC1
MIC2
LINE_IN_L
LINE_IN_R
LINE_IN
C_CODEC_MIC1
CODEC_MIC2
C511 SCD22U10V3KX
CODEC_MIC1
BC292 SCD1U16V3KX
BC293 SC1U10V3KX
BC296 SC1U10V3KX
AUD_VREFO
VREFOUT
5VA_AUD_S3
BC294 SCD1U10V2MX-1
BC295 SCD1U10V2MX-1
AVDD1
AVDD2
AVSS1
AVSS2
DVDD1
DVDD2
DVSS1
DVSS2
3D3V_S0
BC297 SCD1U10V2MX-1
BC298 SCD1U10V2MX-1
BC299 SC2D2U10V5KX
CODEC_VREF
VREF
AFILT1
AFILT2
CAP2
NC
NC
NC
OUTPUT
LINE_OUT_L
LINE_OUT_R
MONO_OUT
HP_OUT_L
HP_COMM
HP_OUT_R
HP_SPK_L
HP_SPK_R
Jack Sense
GPIO0
GPIO1
SPDIF_SHDN
TP173 TPAD28
SPK_SHUTDOWN# 25
EAPD
EAPD 25
SPDIF
CODEC_SPDIF
R658 10KR2
3D3V_S0
01/19/2004
STAC9750-CC1-U
TO Audio OP
AUDIO_OUT_L 25
AUDIO_OUT_R 25
DAC Ref Voltage filter CAP
BC300 SCD1U10V2MX-1
BC301 SC2D2U10V5KX
BC302 SC1000P50V
BC303 SC1000P50V
BC305 SC1000P50V
BC304 SCD1U10V2MX-1
EXT MIC JACK
5V_S0
R681 1KR2
R683 100R2
CODEC_MIC1
L28 BLM11A121S
L27 BLM11A121S
R682 2KR2
C724 SC100P50V2JN
C725 SC100P50V2JN
C726 SC4D7U10V5ZY
C727 SC100P50V2JN
C728 SC100P50V2JN
MIC1
AUDIO-JK29 22.10088.541
SB: Change for EMI solution
3D3V_S0
R634 100KR2
25 HP_NB_SENSE
LOUT1
HP_SPK_R
HP_SPK_L
TC24 SE220U10V-1-U
TC25 SE220U10V-1-U
HP_SPK_R1
HP_SPK_L1
R635 0R2-0
R636 0R2-0
HP_SPK_R2
HP_SPK_L2
BC306 SC270P50V3JN
BC307 SC270P50V3JN
AUDIO-JK29 22.10088.541
01/27/2004
Change from 150u to 220u
HEADPHONE JACK
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
AUDIO (1 of 2) -- Codec
Size A3
Document Number
MOLOKAI
Rev SC
Date: Thursday, April 15, 2004
Sheet 24 of 39



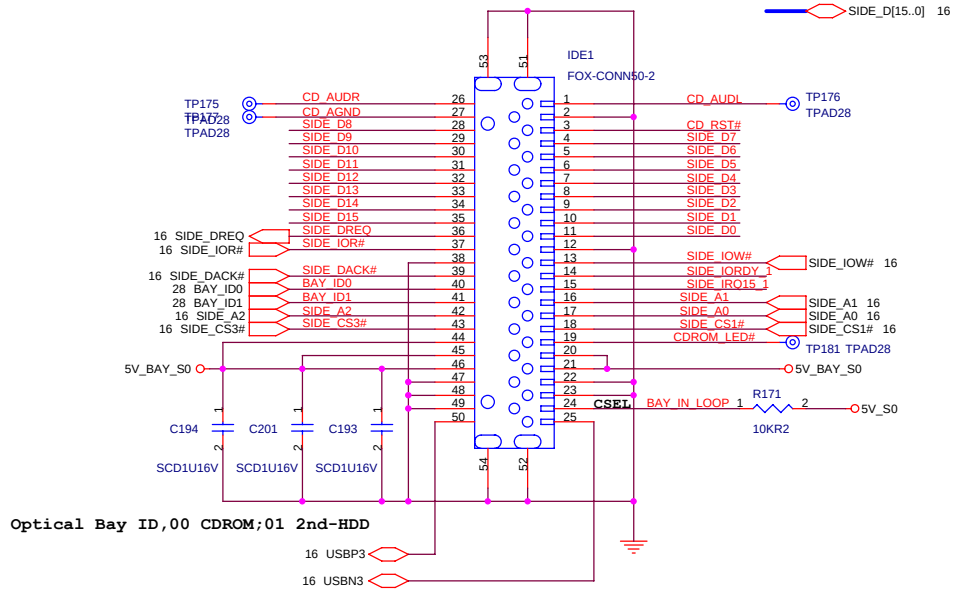
Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	AUDIO (2 of 2) --Phone Jack
Size A3	Document Number MOLOKAI
Rev	SC
Date: Thursday, April 15, 2004	Sheet 25 of 39

HDD CONN





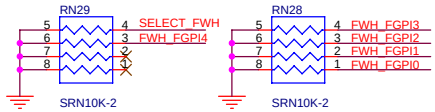
CDROM



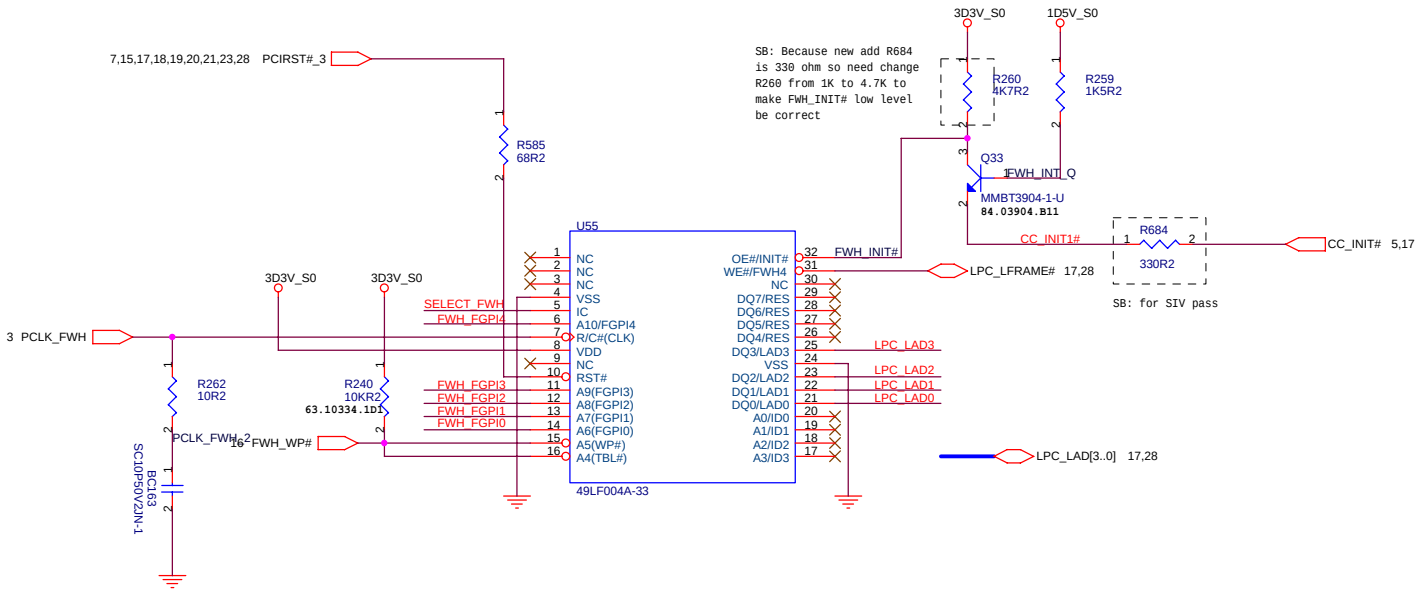
Optical Bay ID,00 CDROM;01 2nd-HDD

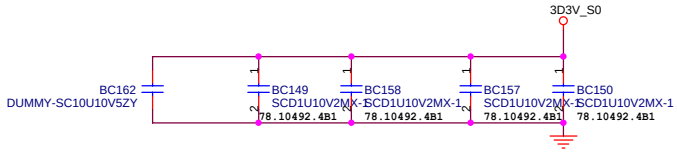
Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: HDD/CD ROM		
Size: A3	Document Number: MOLOKAI	Rev: SC
Date: Thursday, April 15, 2004	Sheet 26 of 39	

Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46



Unused FGPI pins must not be float





Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: FWH/Debug Port

Size	Document Number	Rev
A3	MOLOKAI	SC

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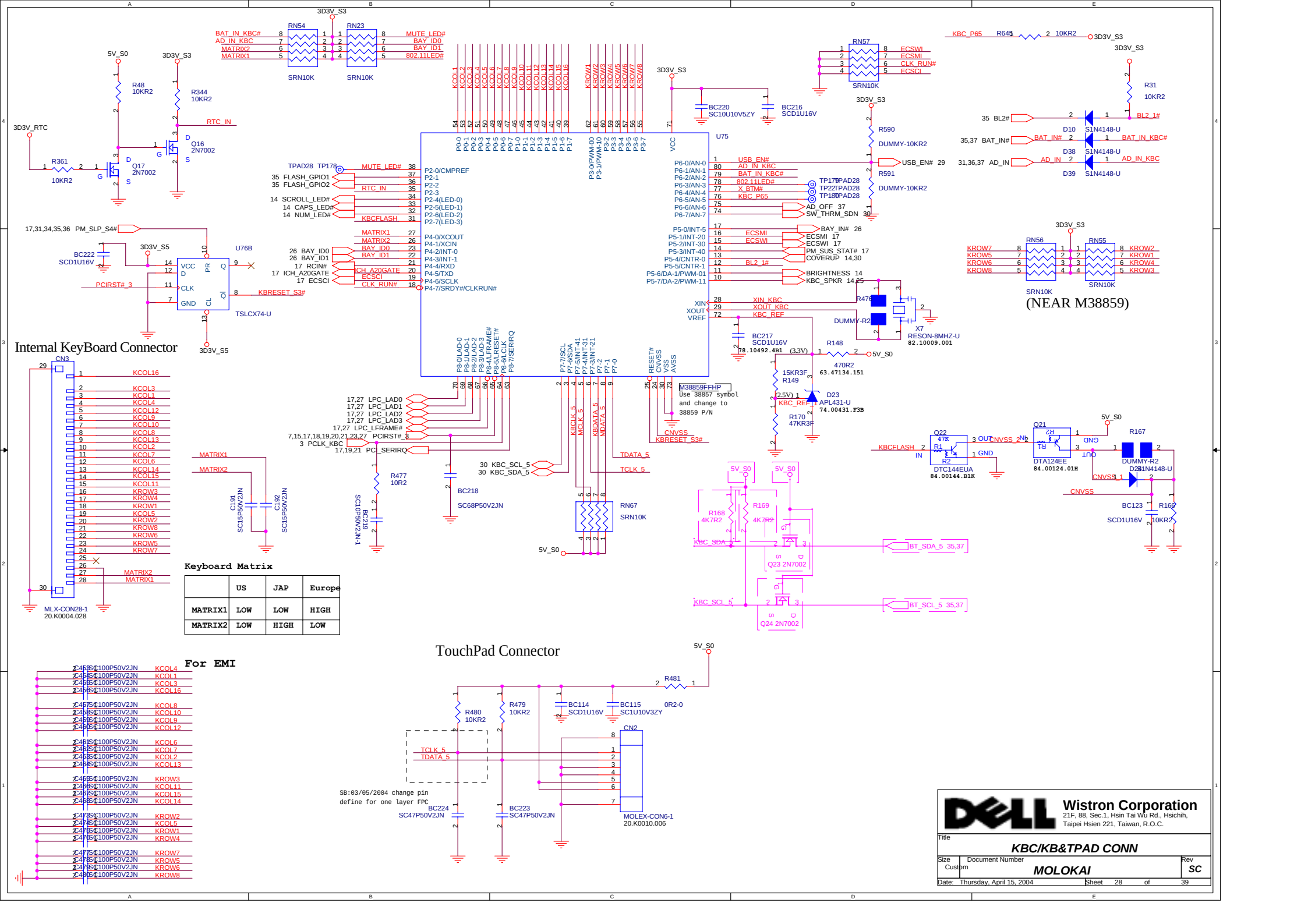
Internal KeyBoard Connector
(NEAR M38859)
TouchPad Connector
For EMI
Keyboard Matrix
US JAP Europe
MATRIX1 LOW LOW HIGH
MATRIX2 LOW HIGH LOW
M38859FFHP
Use 38857 symbol
and change to
38859 P/N
SB:03/05/2004 change pin
define for one layer FPC
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
KBC/KB&TPAD CONN
Size Custom
Document Number
MOLOKAI
Rev
SC
Date: Thursday, April 15, 2004
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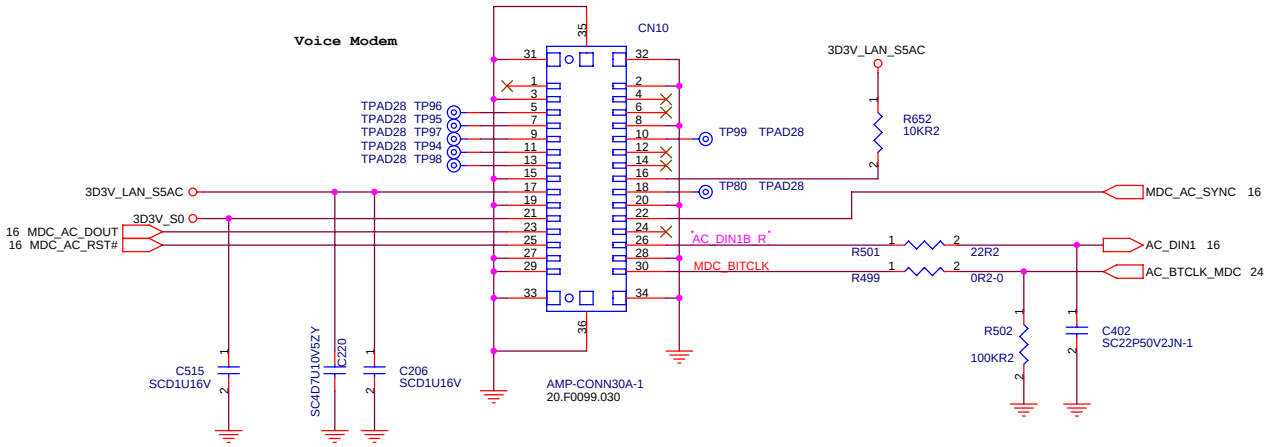
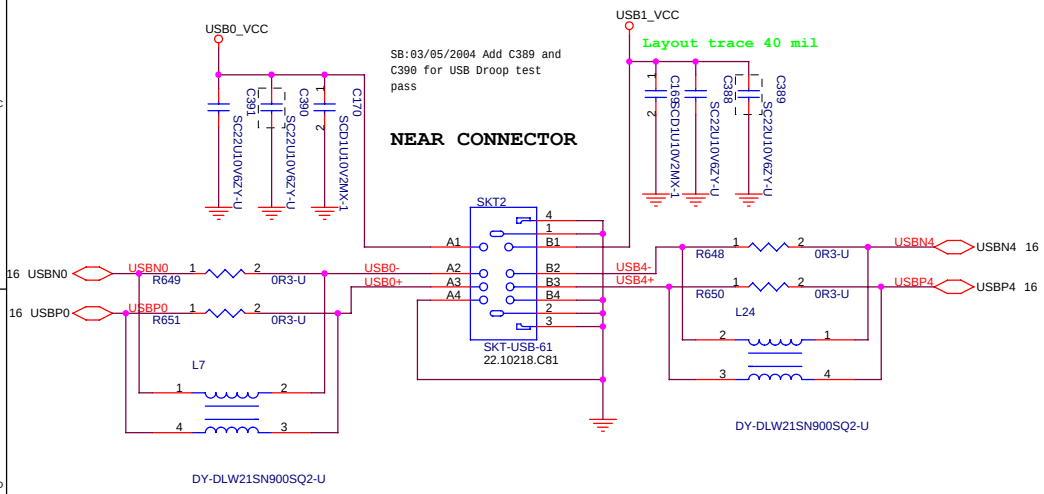
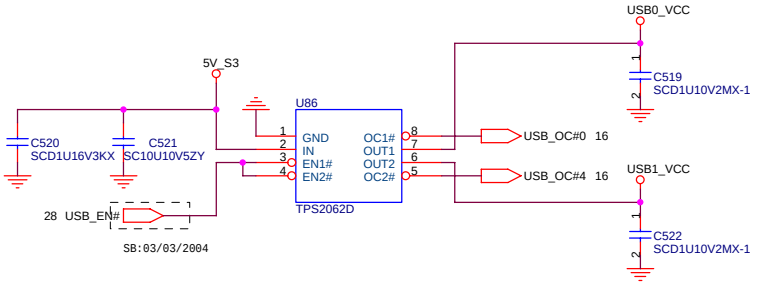
MDC CONN



USB PORT



Dual USB switch



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Title	MDC CONN & USB CONN	
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240 ms after VCC_G768 > 4.38v

Check default setting, default enable is preferred

FAN Conn.

THERMDP1/DP2/THERMDN ON THE SAME LAYER
W/S = 10/5 MIL, 12 MIL AWAY FROM OTHERS
CAPS CLOSE TO G768D

SYSTEM SENSOR

put together

32K suspend clock output

SC:change TEMP setting from 85 to 105 degree.

HW thermal shut down tempature setting 105 degree . Put Near vent out .

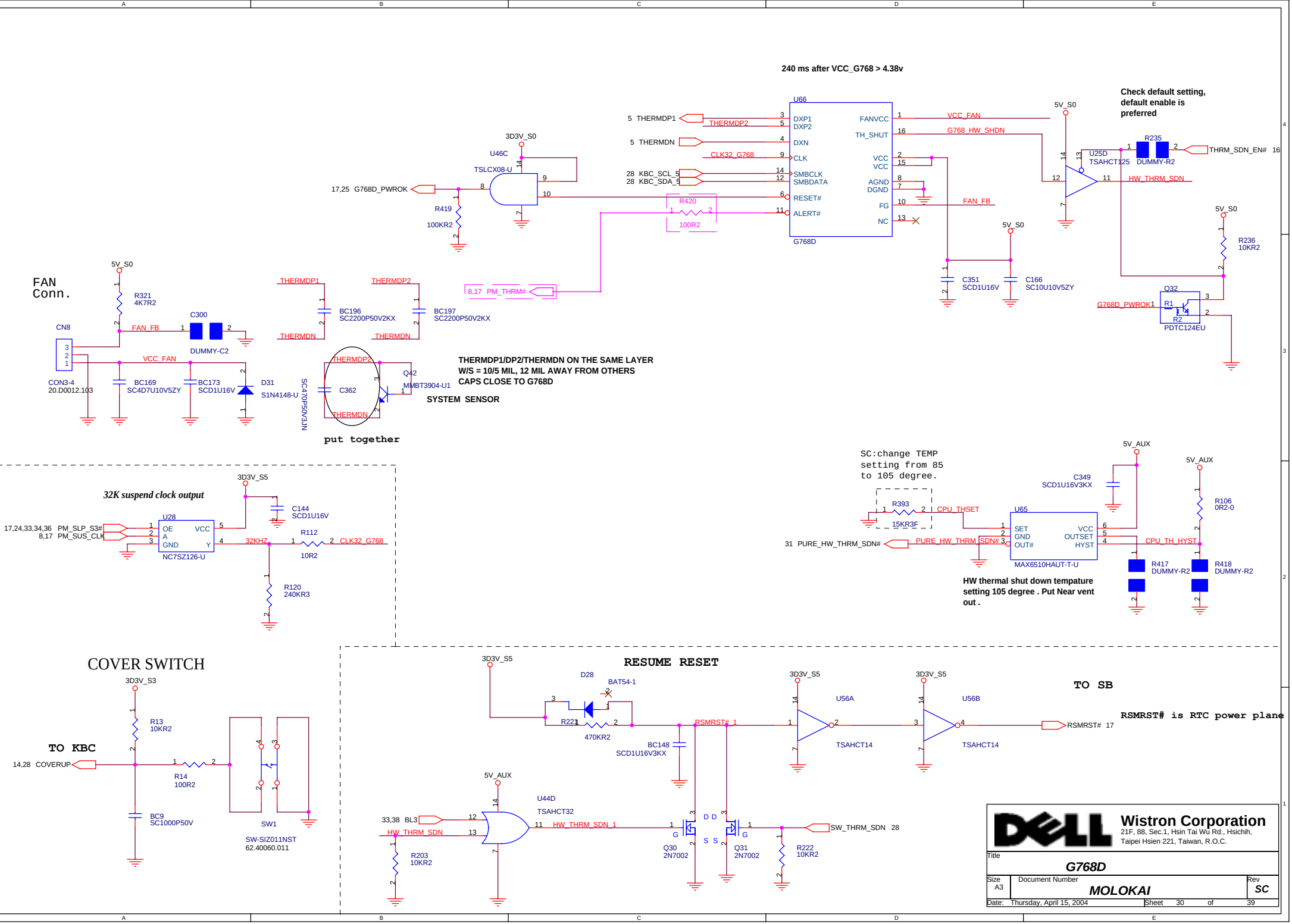
COVER SWITCH

TO KBC

RESUME RESET

TO SB

RSMRST# is RTC power plane



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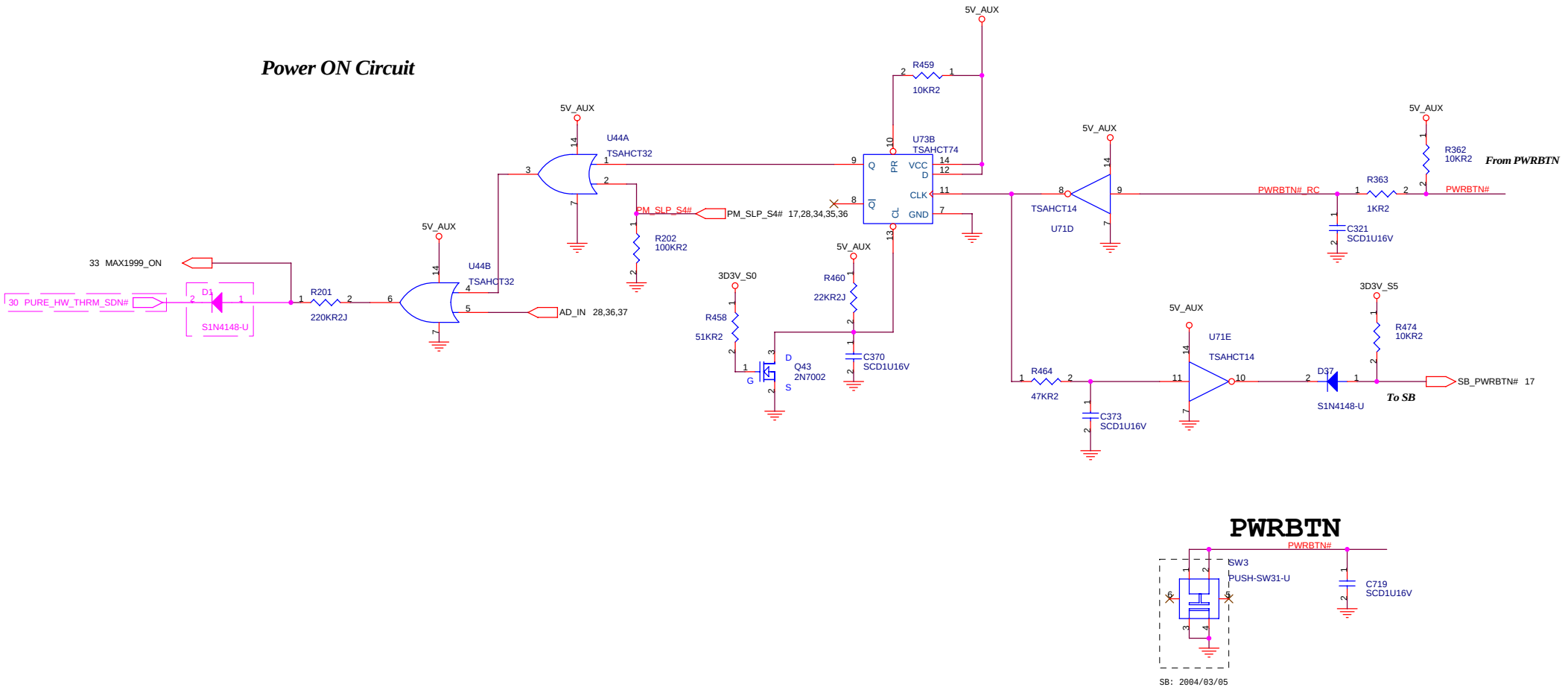
Title: G768D		
Size: A3	Document Number: MOLOKAI	Rev: SC
Date: Thursday, April 15, 2004	Sheet 30 of 39	



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Title: POWER ON CIRCUIT		
Size: A3	Document Number: MOLOKAI	Rev: SC
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Deep Sleep
100k/(100k+1.21k)=98.79%
OffSet= 1.21%

	Active	Deep	Deeper
DPRSLPVR	0	0	1
STP_CPU#	1	0	0

IFL=(RISEN*32uA*n) / Rds(on)=
1.96k*32uA*2 / 5mR =25.157A
FDS7088N3 Rds(on)=5mR

MAX=14A

SC: populate C341 for VTT test pass

MAX=21A
Vf=0.7V

SC:Change for VTT test pass

SC: change for load line test pass

SC: populate TC10 for VTT test pass

PWRCH Low ==> One Phase

IMVP IV
Load Line Slope :3mR
32A=> 96mV
Rdroop = 96mV /
32uA

V_OCSET = 1.75V
V_DRSV = 0.75716V
V_BOOT =1.2611V
I_OCSET = 12.5uA =>
OCP =125% ~ 175%

For Banias/ULV CPU:

Active Mode:
1.Highest Frequency:
VID=1.484V/1.00V
2.Lowest Frequency:
VID=0.956V/0.85V

Deep Sleep Mode:
1.Highest Frequency: VID=1.484V,Offset=-1.2%->VID=1.466
2.Lowest Frequency: VID=0.956V,Offset=-1.2%->VID=0.945

Deeper Sleep Mode:
VID=0.748V

VCC_IO_S0-->Delay 3 mS-->CPUCORDE_ON_DELAY

SB: 2004/03/01

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Title	*IMVP IV-CPU POWER-ISL6218*	
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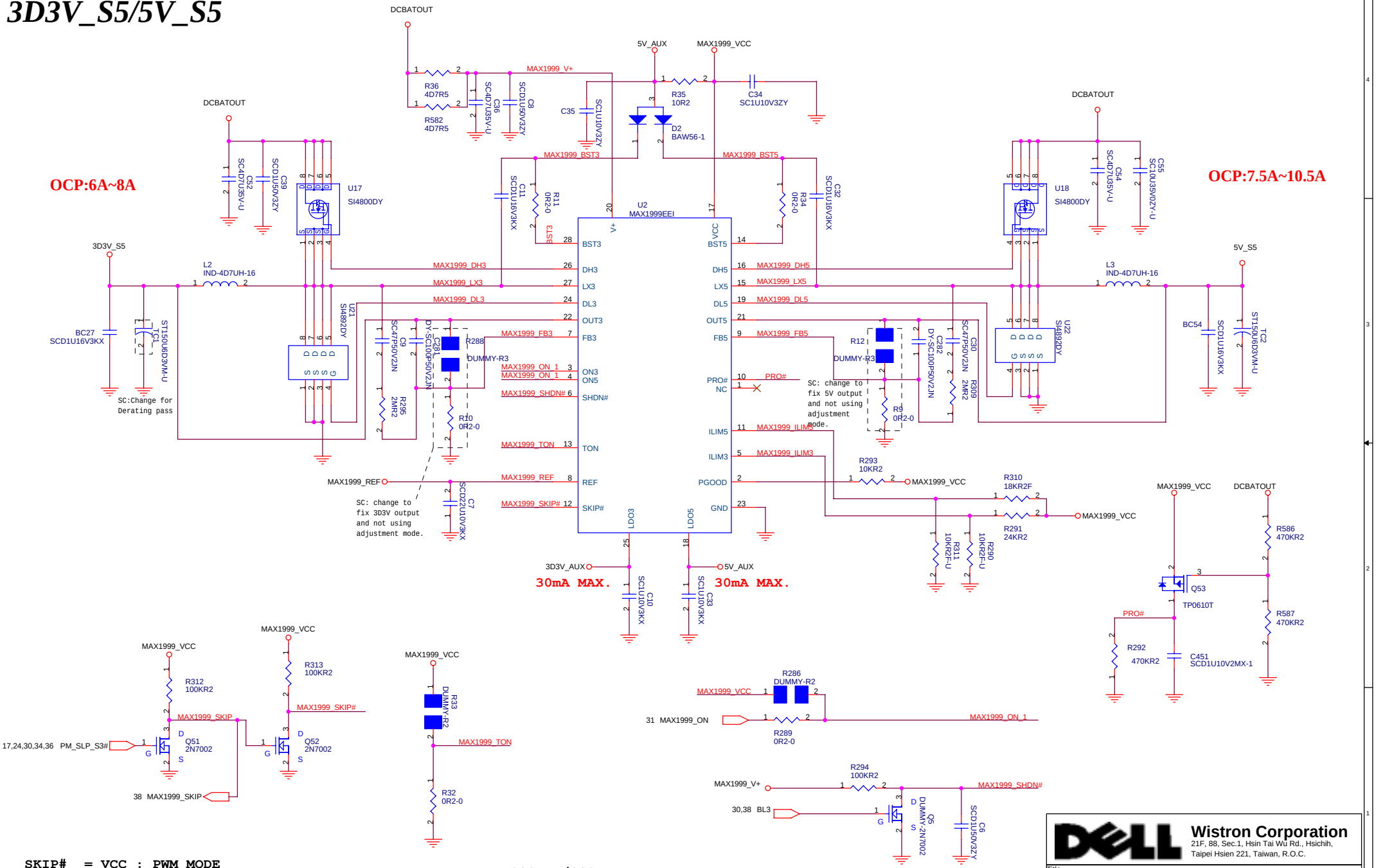
SYSTEM DC/DC
3D3V_S5/5V_S5



SKIP# = VCC : PWM MODE
SKIP# = GND : SKIP MODE
SKIP# = REF/FloatING : Ultrasonic MODE (25KHz min)

Ton = VCC : 200KHz/300KHz
Ton = GND : 400KHz/500KHz (5V/3D3V)

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Title: MAX1999/3D3V_S5/5V_S5		
Size: A3	Document Number: MOLOKAI	Rev: SC
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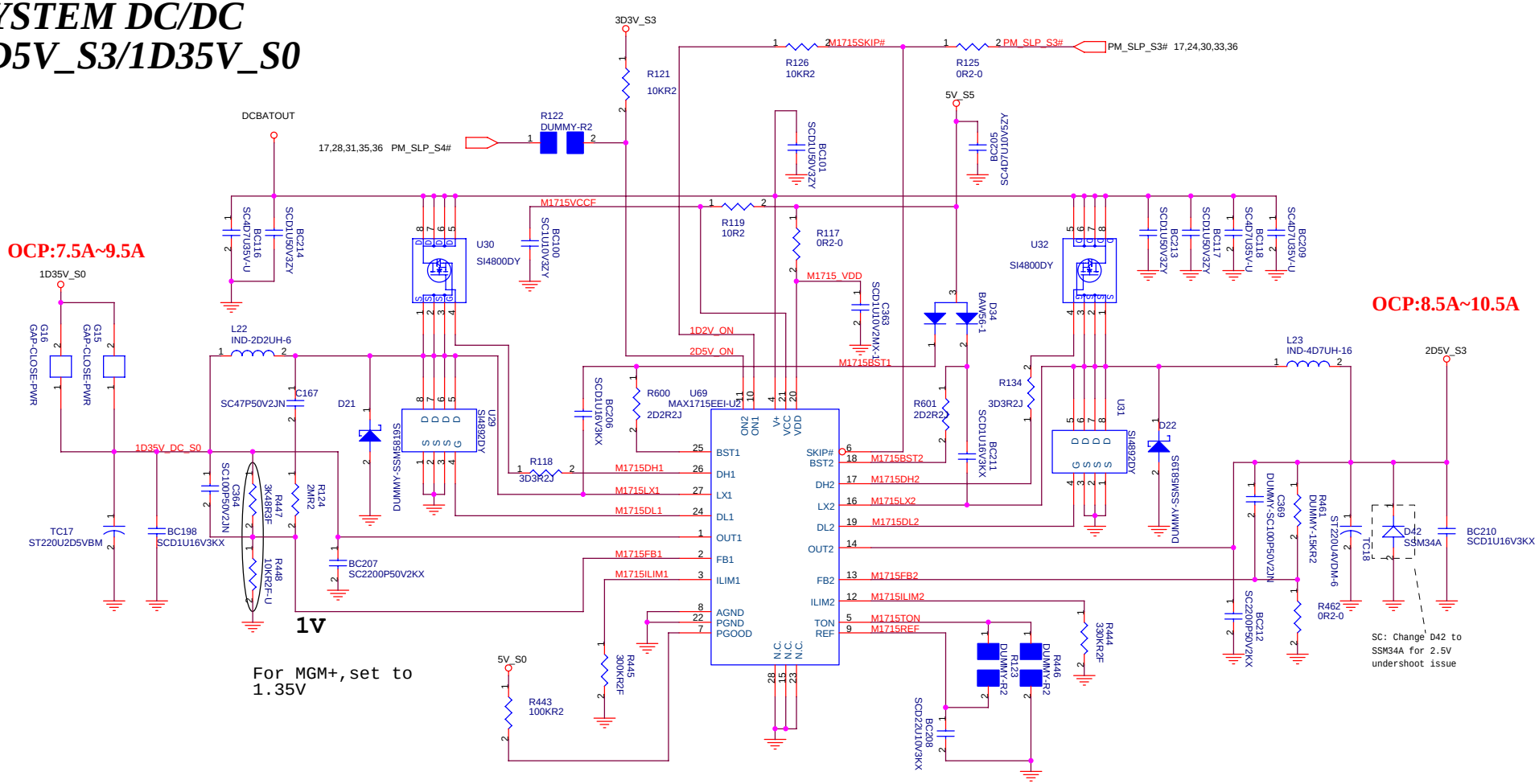
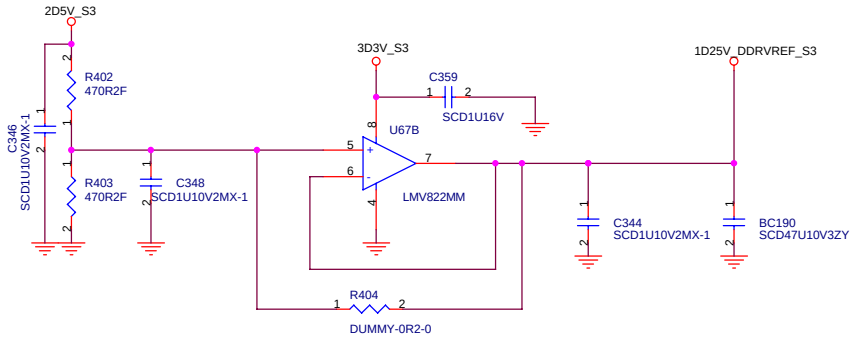
SYSTEM DC/DC
2D5V_S3/1D35V_S0



1D25V_DDRVREF_S3 need 10 mil and must near NB/DIMM



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Title	MAX1715/2D5V_S3/1D35V_S0	
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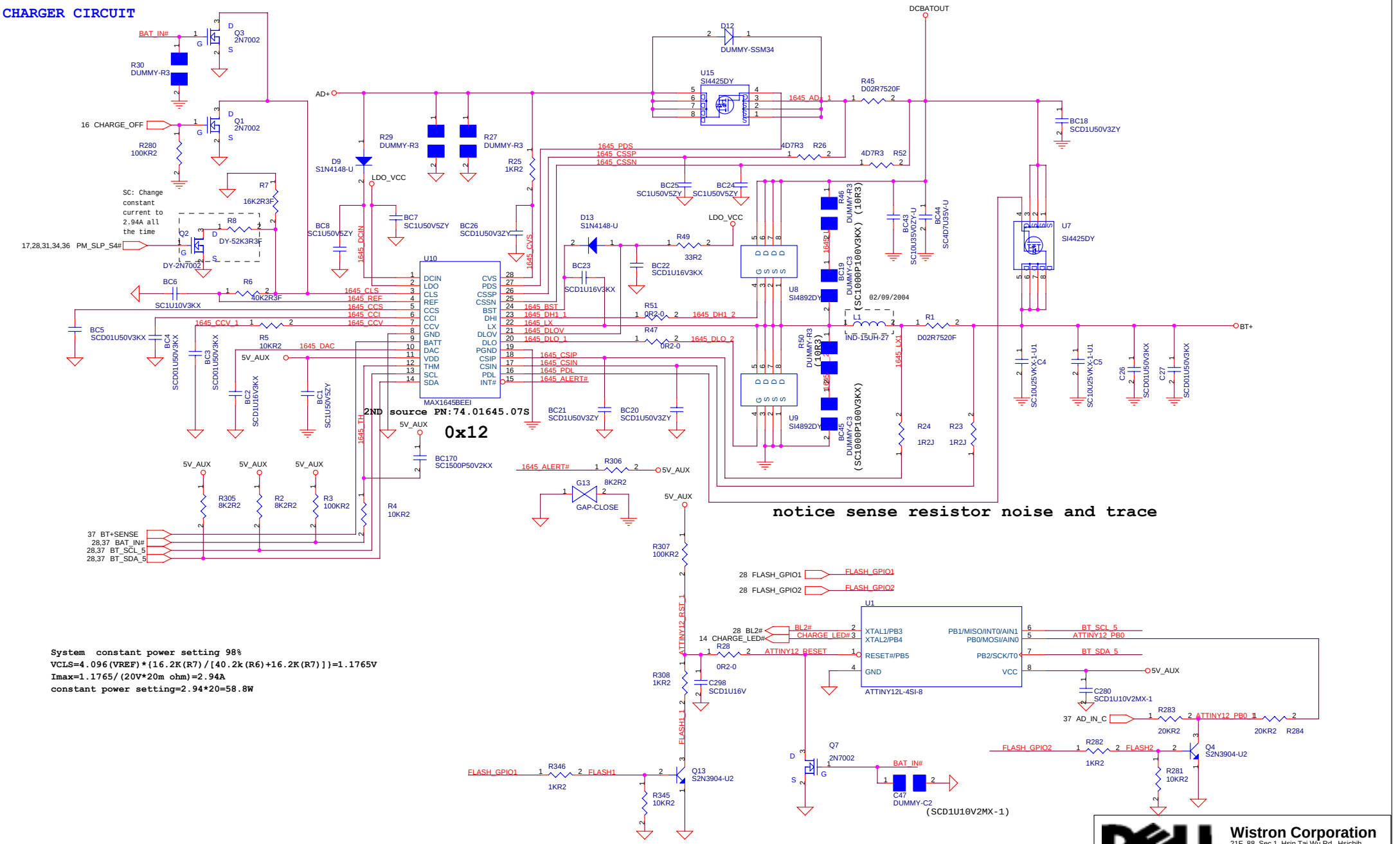
CHARGER CIRCUIT



System constant power setting 98%
VCLS=4.096(VREF)*{16.2K(R7)/[40.2k(R6)+16.2K(R7)]}=1.1765V
Imax=1.1765/(20V*20m ohm)=2.94A
constant power setting=2.94*20=58.8W

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Title: CHARGER&MicroP			
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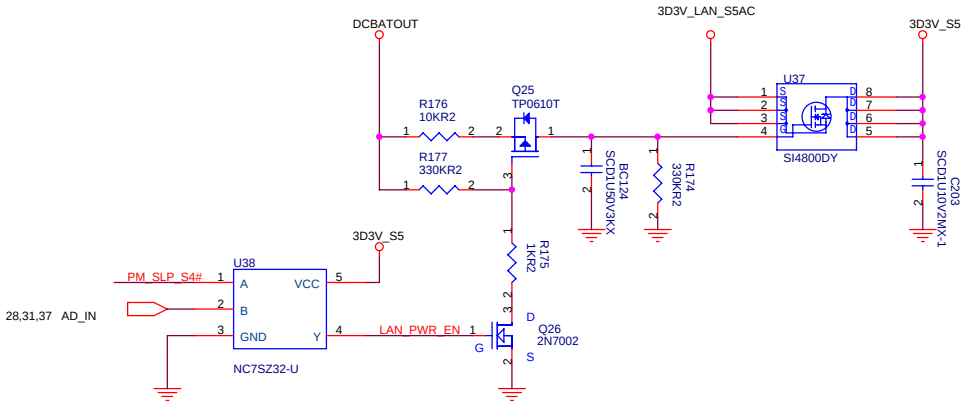
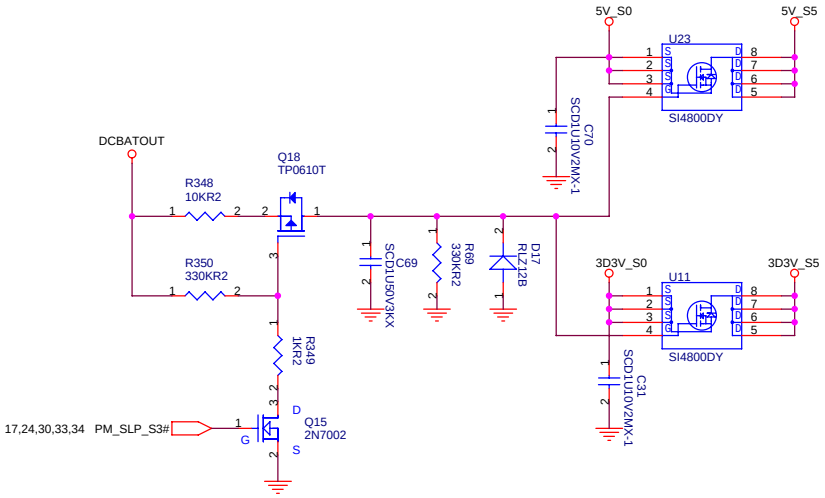
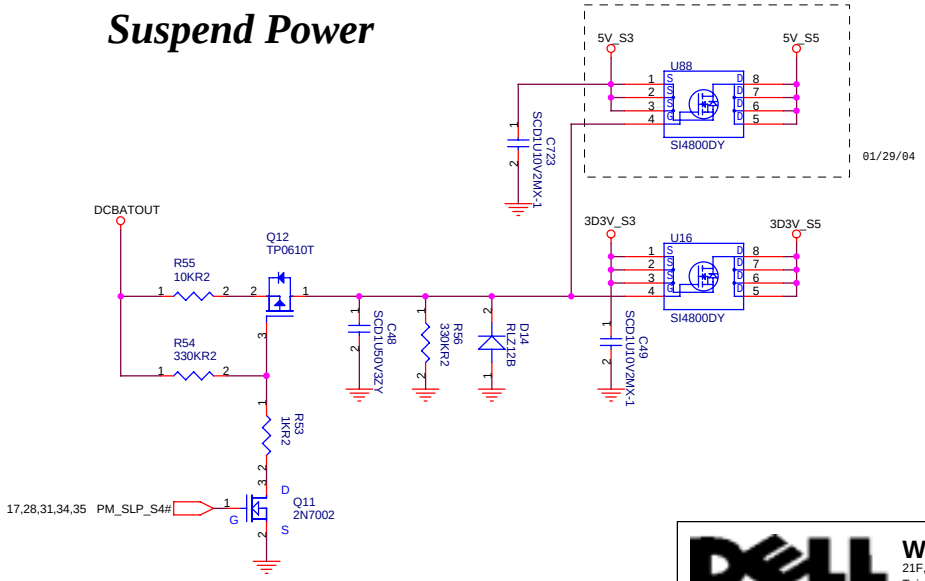
LAN Power



Run Power



Suspend Power



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Title	***PWR Plane SW / VCC_IO_S0***	
Size A3	Document Number ***MOLOKAI***	Rev ***SC***
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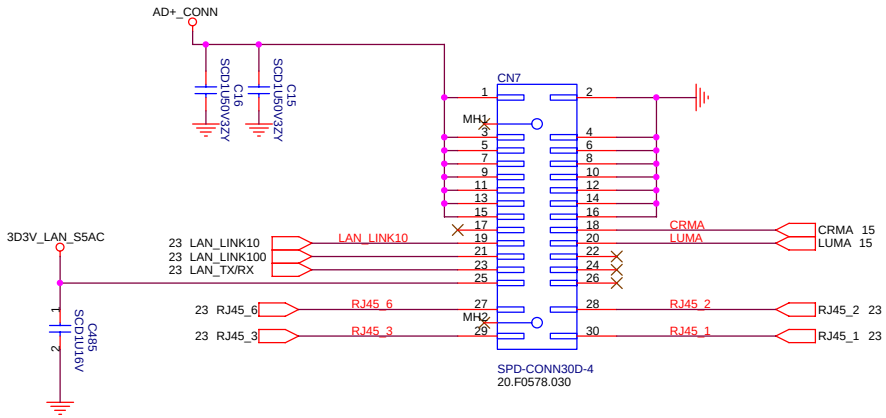
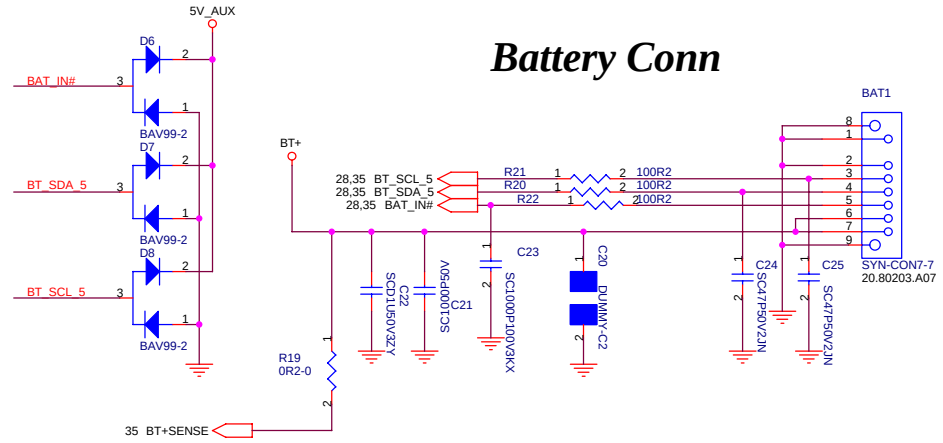
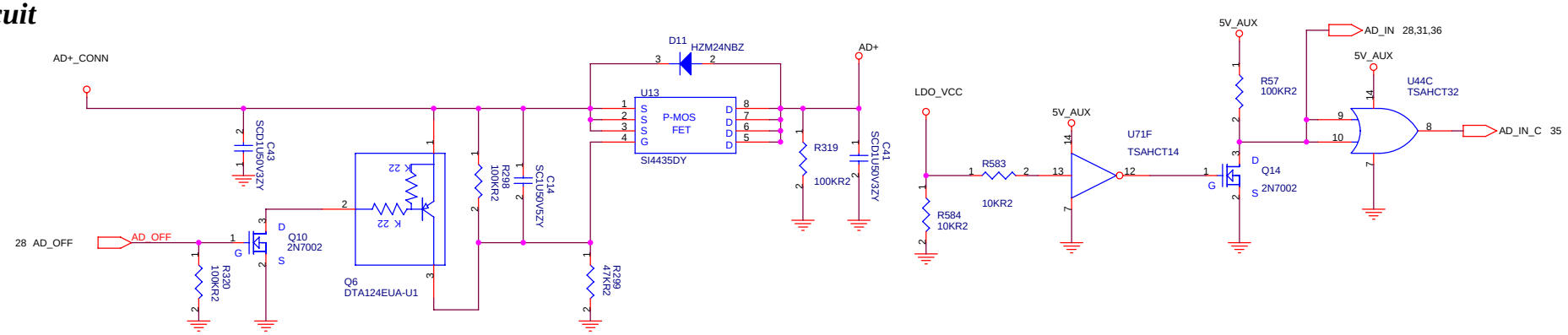
TV BD Conn



Battery Conn



Adaptor In Circuit



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Title: *Battery Conn/TV BD Conn/Adaptor In Circuit*		
Size: A3	Document Number: *MOLOKAI*	Rev: *SC*
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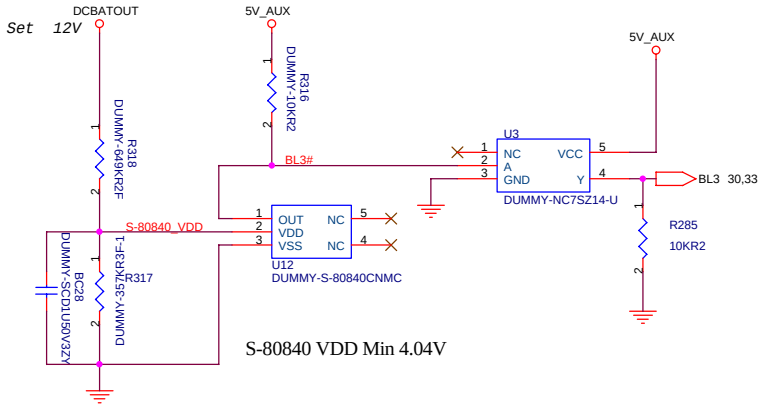
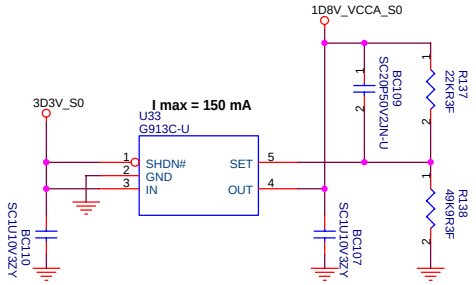
BATRERY LOW3 DETECTOR



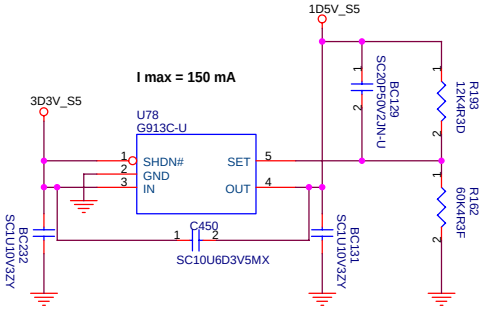
S-80840 VDD Min 4.04V

At Dothan CPU application, POWER is 1.5V or 1.8V.

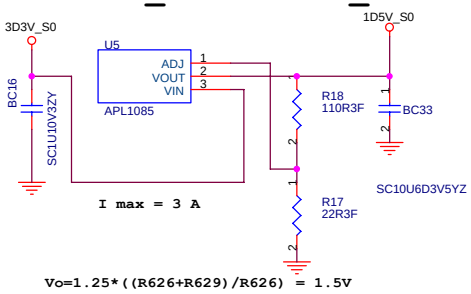
3D3V_S0 --> 1D8V_VCCA_S0 (For CPU VCCA)



3D3V_S5 --> 1D5V_S5

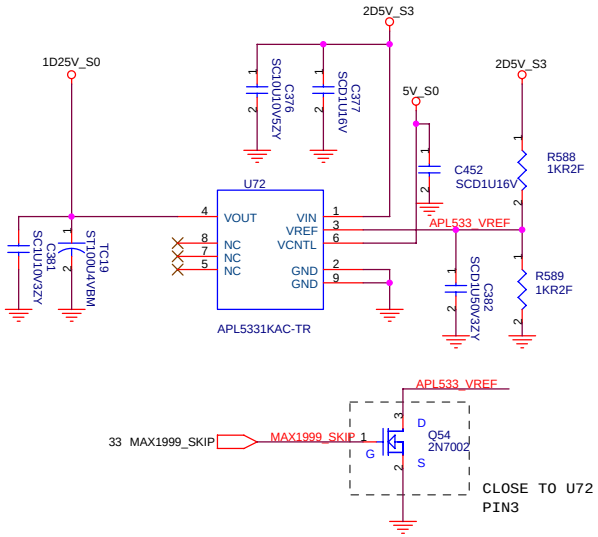


3D3V_S0 → 1D5V_S0

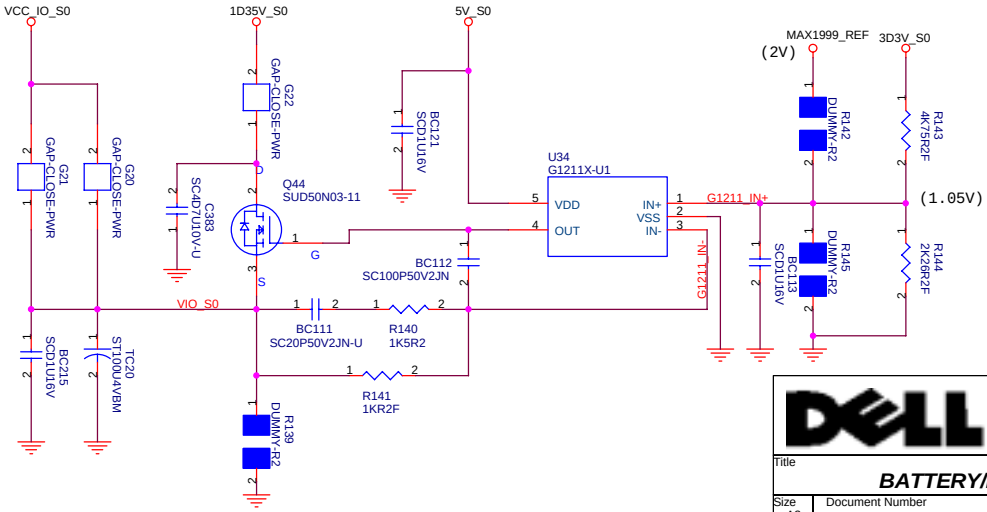


Vo=1.25*((R626+R629)/R626) = 1.5V

2D5V_S3 → 1D25V_S0



1D35V_S0 → VCC_IO_S0(1.05V)



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Title	***BATTERY/LDO/Adaptor In***	
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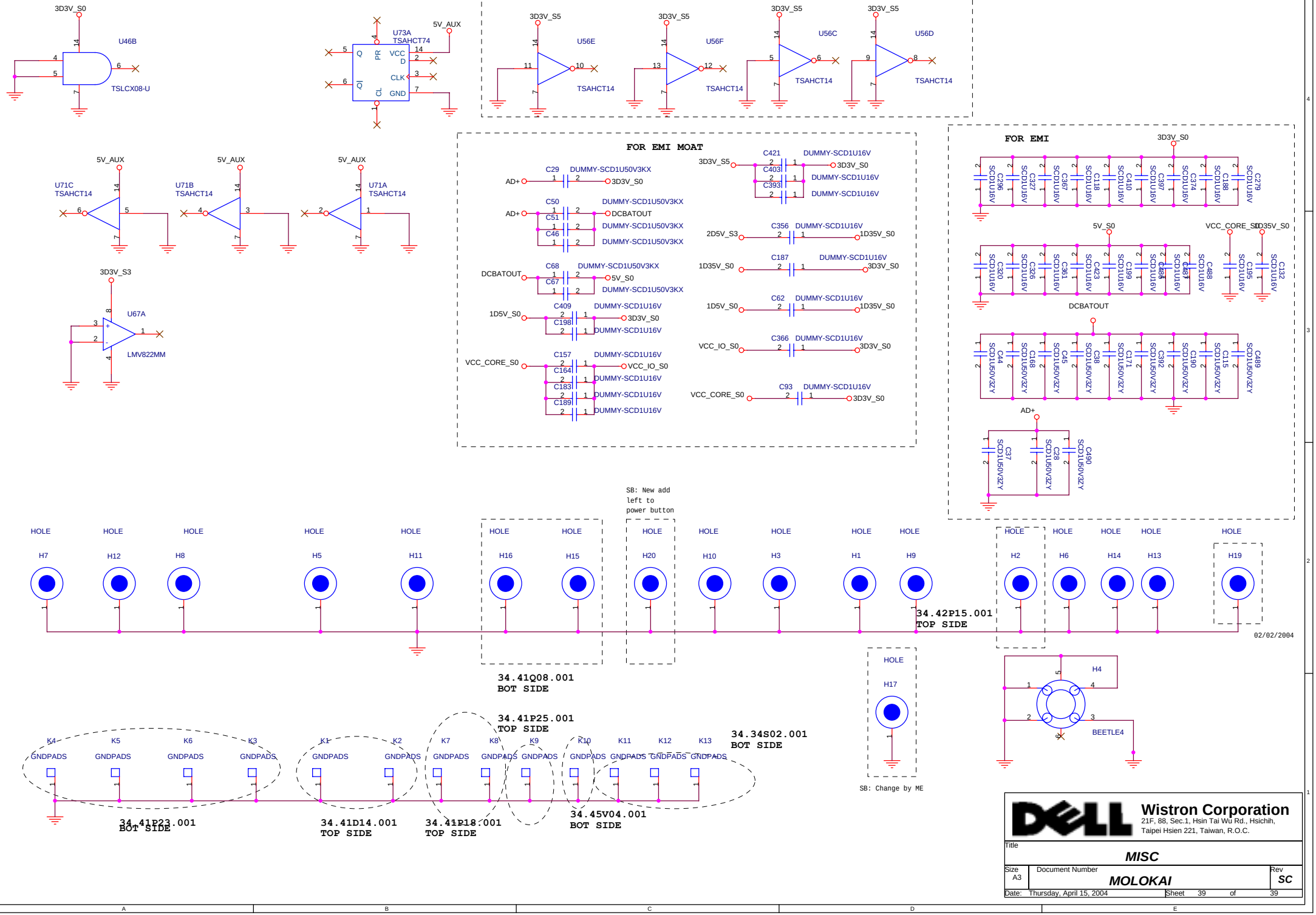

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Title: MISC		
Size: A3	Document Number: MOLOKAI	Rev: SC
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