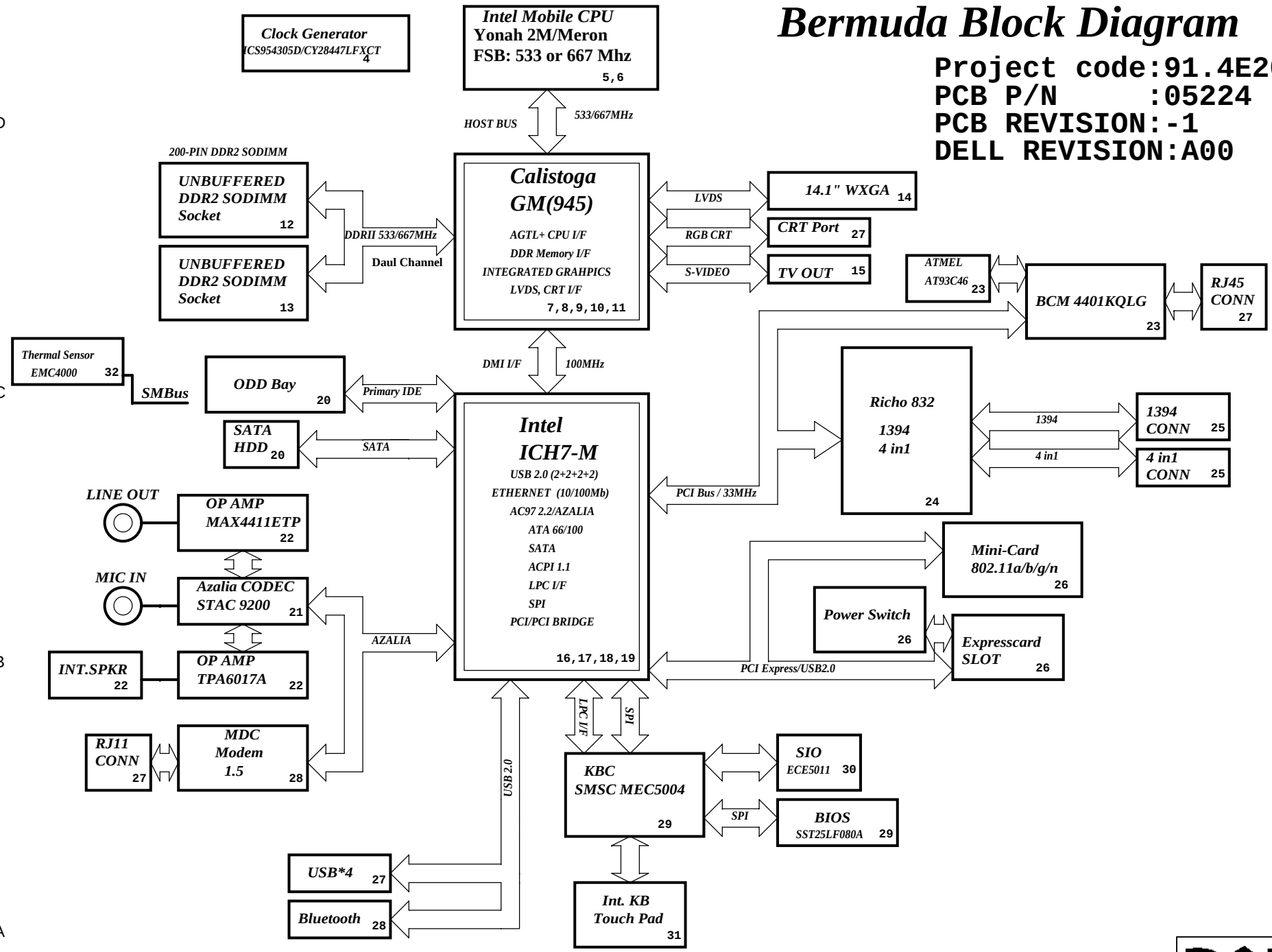
Bermuda Block Diagram

Project code:91.4E201.001
PCB P/N :05224
PCB REVISION:-1
DELL REVISION:A00



System DC/DC TPS51120 39	
INPUTS	OUTPUTS
PWR_SRC	+5VSUS +3VSUS
Battery Charger MAX8731 42	
PWR_SRC	BATT+
System DC/DC TPS51483 40	
PWR_SRC	+1.05VRUN +1.5VRUN
CPU DC/DC ADP3207 +ADP3419 38	
PWR_SRC	VCC_CORE
DDR2 DC/DC SC480 41	
PWR_SRC	+1.8VSUS +0.9VRUN +0.9VSUS_DDR2VREF

PCB LAYER
L1:TOP
L2:GND
L3:Signal
L4:Signal
L5:VCC
L6:Signal
L7:GND
L8:BOT

1208-1500

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title		
System Block Diagram		
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Wistron/Dell confidential

ICH7M Functional Strap Definitions

page 16

Signal	Usage/When Sampled	Comment
ACZ_SDOUT	XOR Chain Entrance/ PCIE Port Config bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h)
ACZ_SYNC	PCIE bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
EE_CS	Reserved	This signal should not be pull high.
EE_DOUT	Reserved	This signal should not be pull low.
GNT2#	Reserved	This signal should not be pull low.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT5#/ GPIO17#, GNT4#/ GPIO48	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT5# is MSB, 01-SPI, 10-PCI, 11-LPC.
DPRSLPVR	Reserved	This signal should not be pull high.
GPIO25	Reserved. Rising Edge of RSMRST#.	This signal should not be pull low.
INTVRMEN	Integrated VccSus1_05 VRM Enable/Disable. Always sampled.	Enables integrated VccSus1_05 VRM when sampled high
LINKALERT#	Reserved	Requires an external pull-up resistor.
REQ[4:1]#	XOR Chain Selection. Rising Edge of PWROK.	TBD, Chapter 8.
SATALED#	Reserved	This signal should not be pull low.
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH7 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.

Calistoga Strapping Signals and Configuration

* is Default setting

CFG Strap	Low	High
CFG 5	DMI X 2	DMI X 4 *
CFG 6	Moby Dick	Calistoga *
CFG 7	DT/Transportable CPU	Mobile CPU *
CFG 9	Reserved Lane	Normal Operation *
CFG 10	Reserved	Mobility *
CFG 11	Calistoga *	Reserved
CFG 16 FSB Dynamic ODT	Disabled	Enabled *
CFG 18 VCC Select	1.05V *	1.5V
CFG 19 DMI Lane Reserved	Normal Operation *	Reserved Lane
CFG 20 PCIE/SDVO Select	Only PCIE or SDVO is operation *	PCIE and SDVO are operation simu
SDVO_CTRLDATA	No SDVO Device present *	SDVO Device present

	CFG[13:12]
LL	Reserved
LH	XOR Mode Enabled
HL	All Z Mode Enabled
HH	Normal Operation *

ICH7M Integrated Pull-up and Pull-down Resistors

ICH7-M EDS 17837 1.5V1

EE_DIN, EE_DOUT, GNT[3:0], GPIO[25], GNT[4]#/GPIO48, GNT[5]#/GPO17, PME#, LAD[3:0]#/FHW[3:0]#, LAN_RXD[2:0] LDRQ[0], LDRQ[1]/GPIO[41], PWRBTN#, TP[3]	ICH7 internal 20K pull-ups
DD[7], DDREQ	ICH7 internal 11.5K pull-downs
ACZ_BIT_CLK, ACZ_RST#, ACZ_SDIN[2:0], ACZ_SDOUT, ACZ_SYNC, DPRSLPVR/GPIO16, EE_CS, SPI_ARB, SPI_CLK, SPKR,	ICH7 internal 20K pull-downs
USB[7:0][P,N]	ICH7 internal 15K pull-downs
SATALED#	ICH7 internal 15K pull-up
LAN_CLK	ICH7 internal 100K pull-down

954305D 27Mhz/LCDCLK Spread and Frequency Selection Table

page 3

SS3 Byte9 bit 7	SS2 bit6	SS1 bit5	SS0 bit4	Spread Amount%
0	0	0	0	-0.50 Down
0	0	0	1	-1.00 Down
0	0	1	0	-1.50 Down
0	0	1	1	-2.00 Down
0	1	0	0	-0.75 Down
0	1	0	1	-1.25 Down
0	1	1	0	-1.75 Down
0	1	1	1	-2.25 Down
1	0	0	0	+-0.25 Center
1	0	0	1	+-0.5 Center
1	0	1	0	+-0.75 Center
1	0	1	1	+-1.0 Center
1	1	0	0	+-0.25 Center
1	1	0	1	+-0.5 Center
1	1	1	0	+-0.75 Center
1	1	1	1	+-1.0 Center

PCI Routing

page 16

	IDSEL	IRQ	REQ/GNT
R5C832	AD17		
LAN	AD16		

ICH7M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm

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Title: Table of Content

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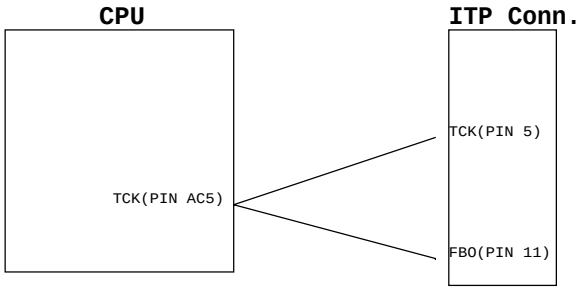

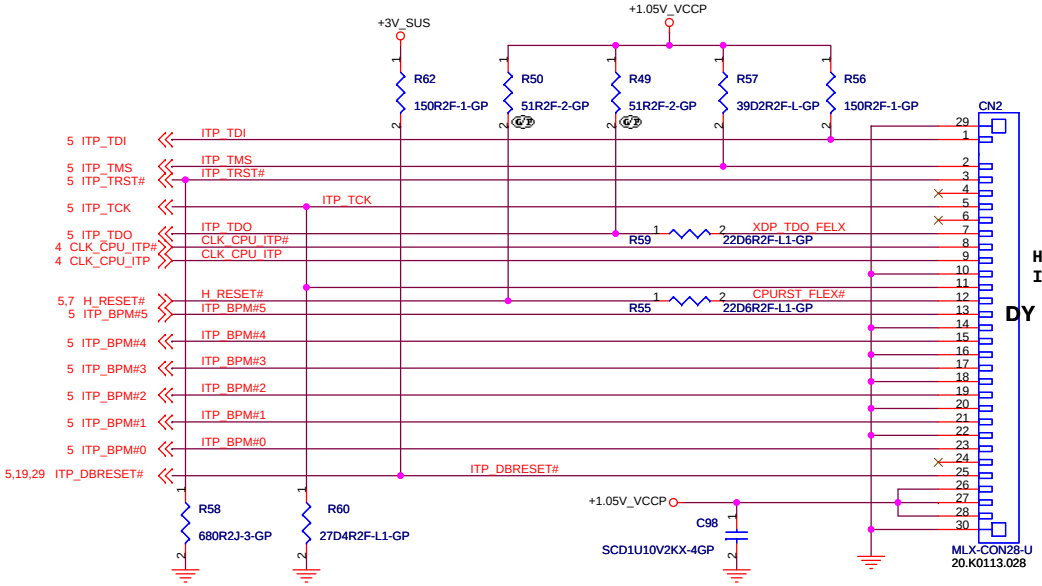

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max)

DY

+1.05VRUN use Decoupling Capacitor close
ITP connector 100 mil (max)

ITP Debug Conn.

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Title	ITP Debug	
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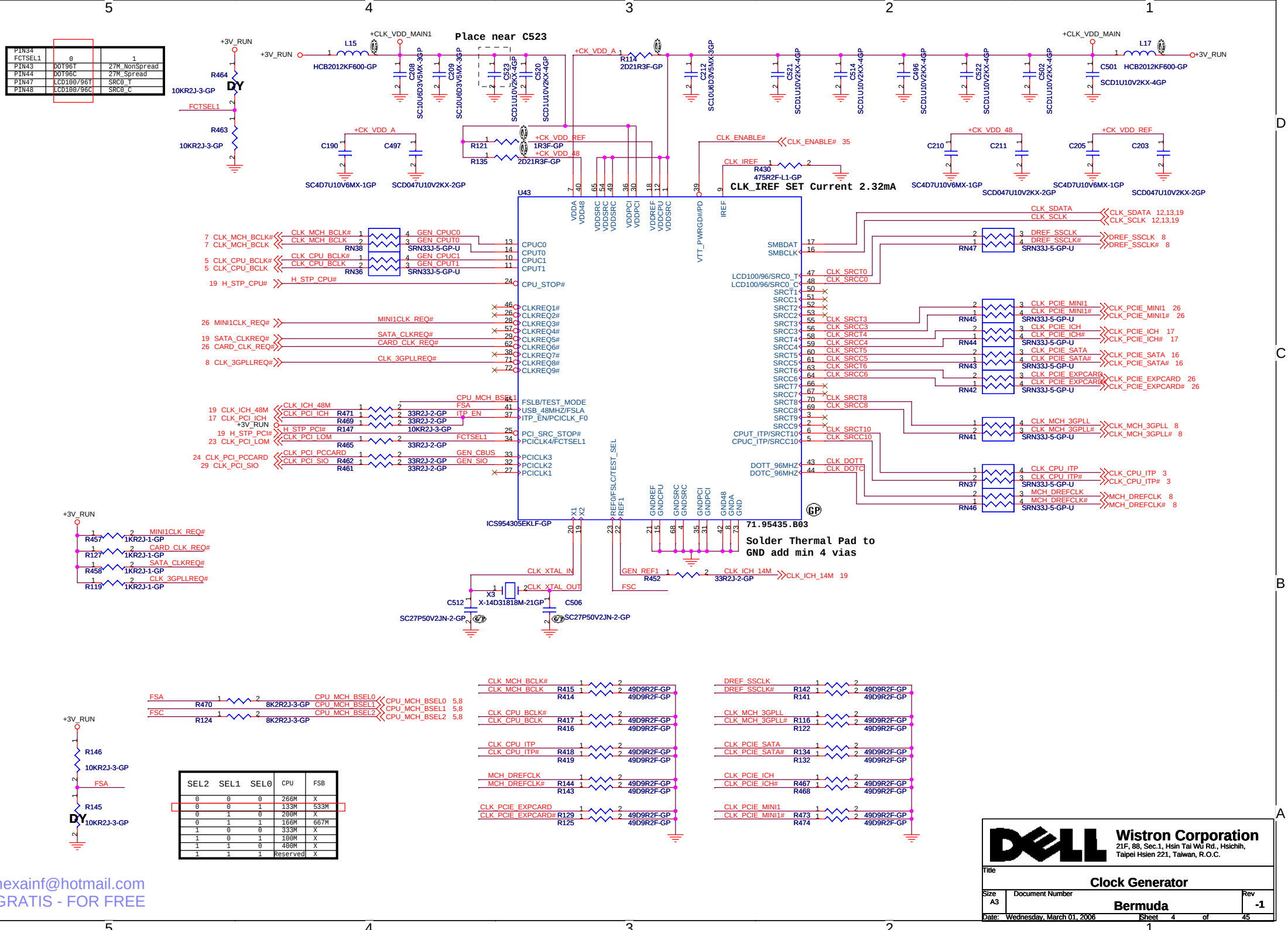

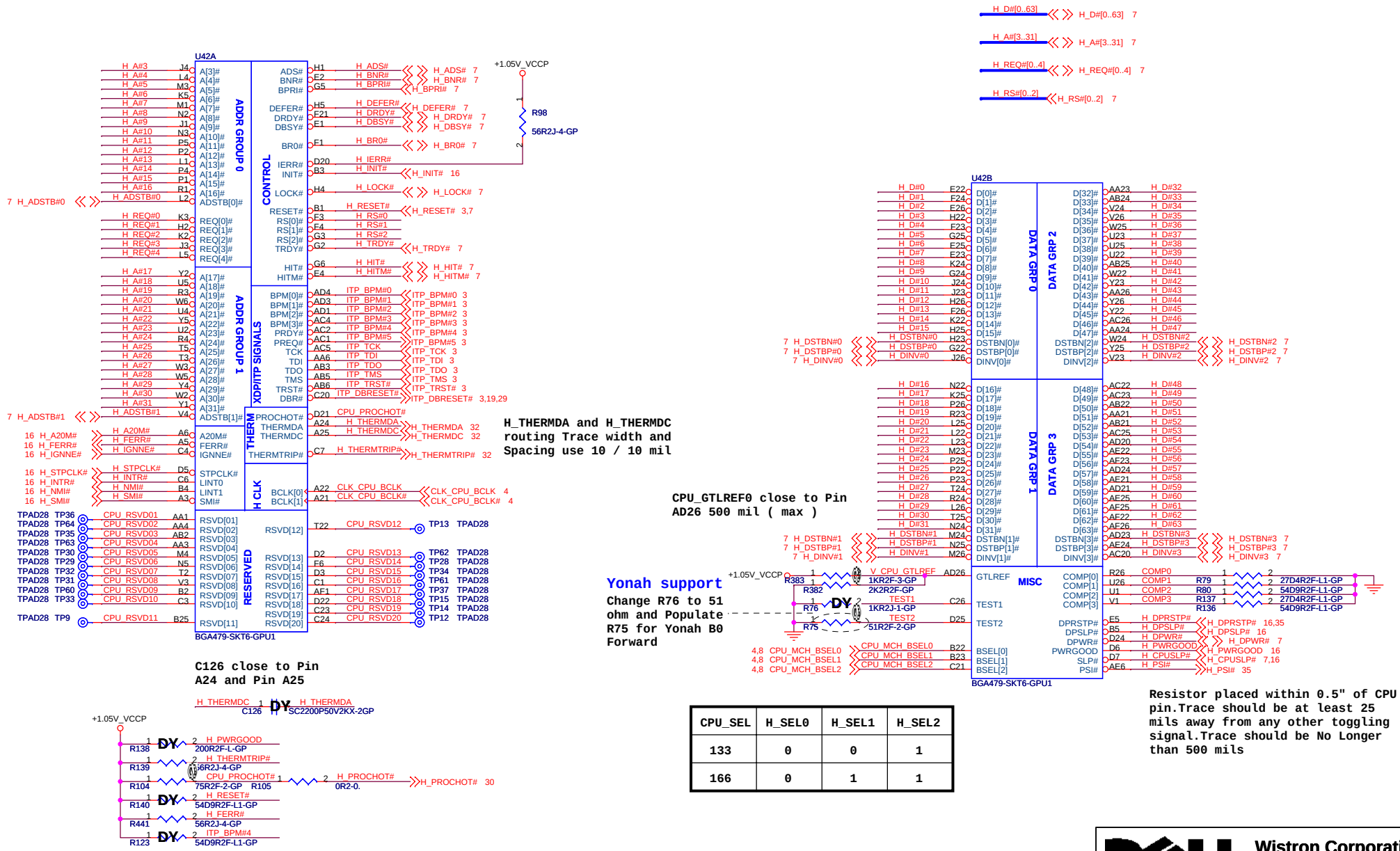

CPU_SEL	H_SEL0	H_SEL1	H_SEL2
133	0	0	1
166	0	1	1

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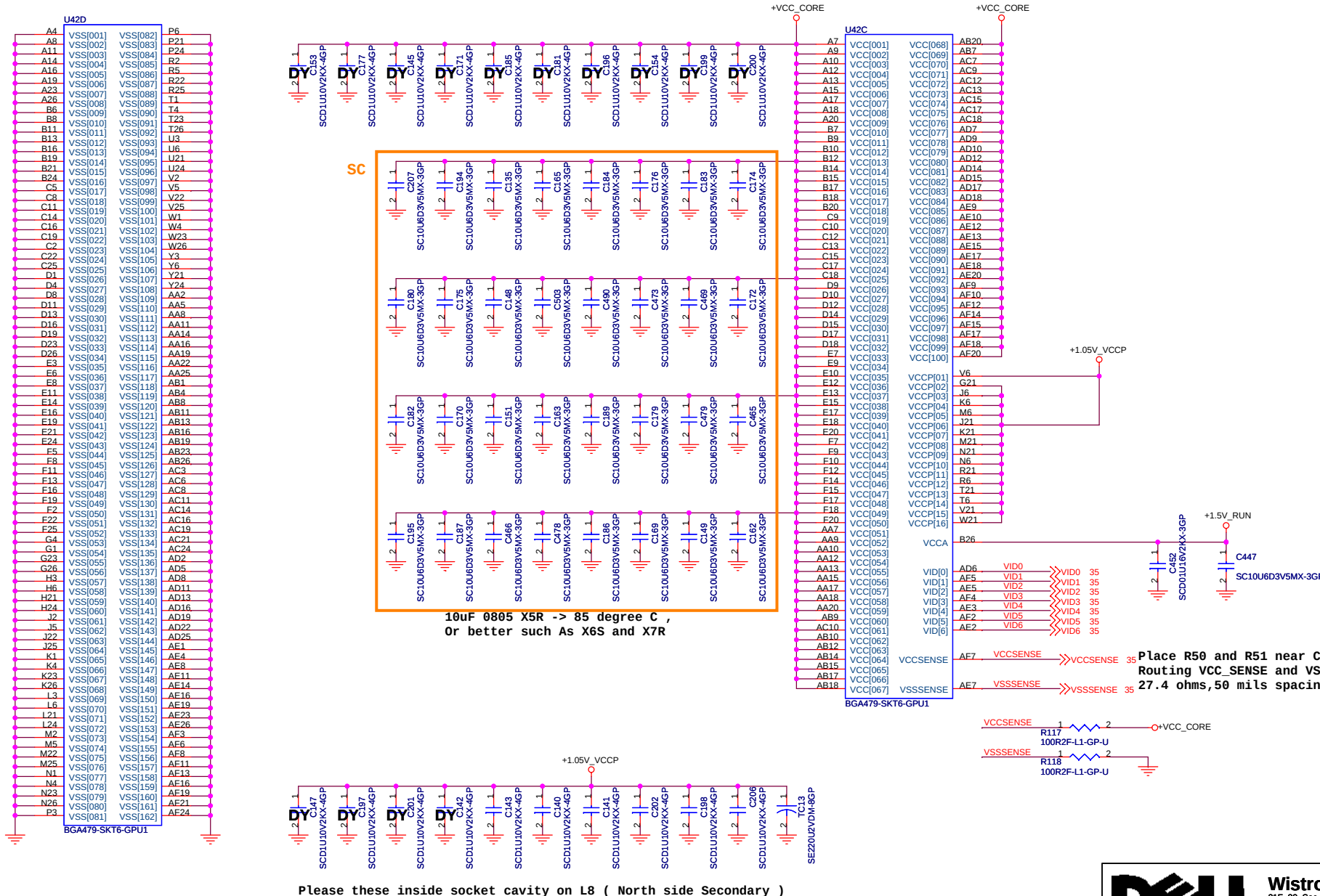
Title: CPU - 01 - Yonah - FSB

Size	Document Number	Rev
A3	Bermuda	-1

Date: Wednesday, March 01, 2006 Sheet 5 of 45



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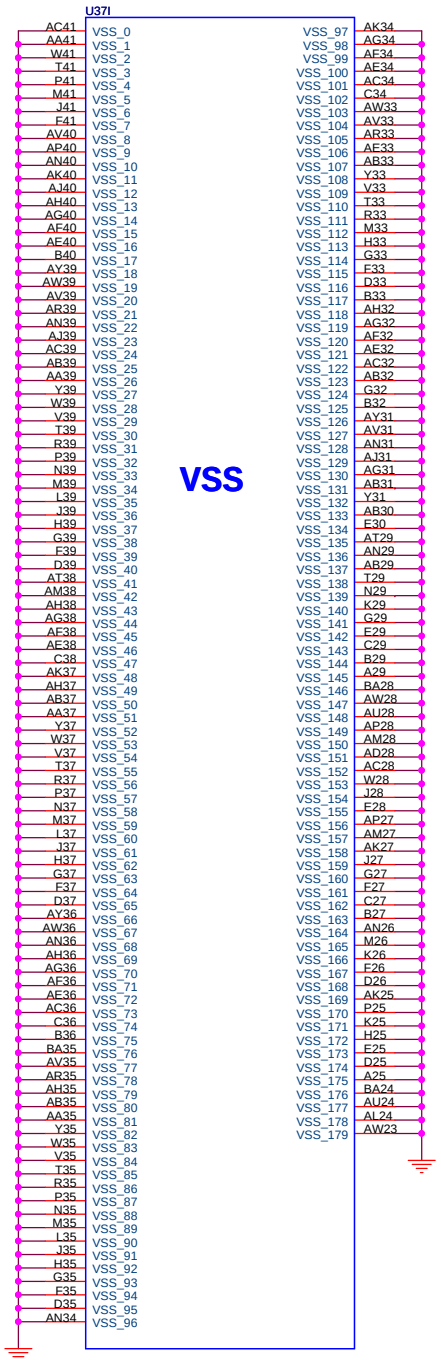
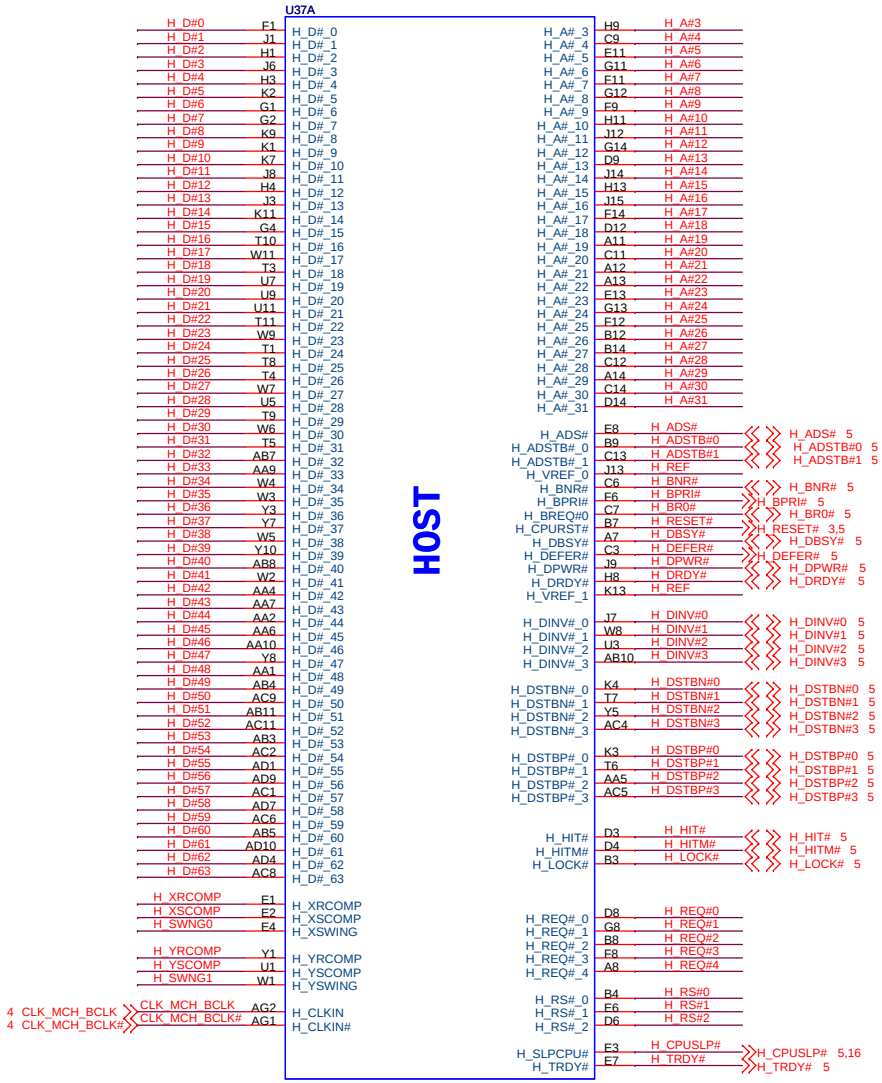
Title: CPU - 02 - Yonah - POWER

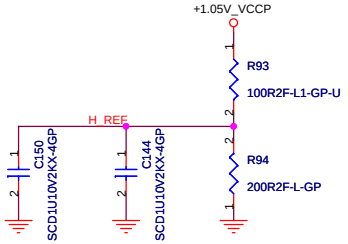
Size	Document Number	Rev
A3	Bermuda	-1

Date: Wednesday, March 01, 2006 Sheet 6 of 45

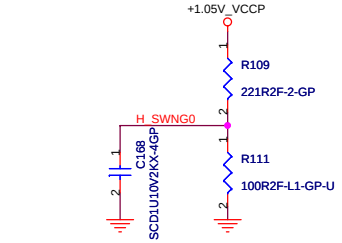




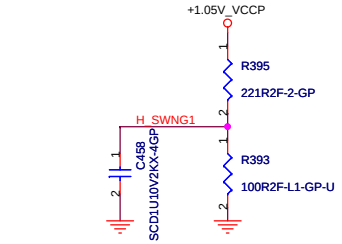
H_REF Decoupling Capacitors close Caliistoga 100 mil



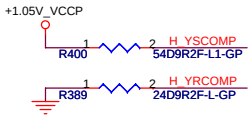
H_XSWING and H_YSWING routing Trace width and Spacing use 10 / 20 mil



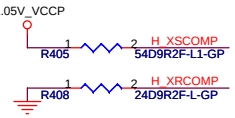
H_XSWING and H_YSWING Resistors and Capacitors close Caliistoga 500 mil (MAX)



H_XRCOMP and H_YRCOMP routing Trace width and Spacing use 10 / 20 mil



H_XSCOMP and H_YSCOMP Resistors and Capacitors close Caliistoga 500 mil (MAX)



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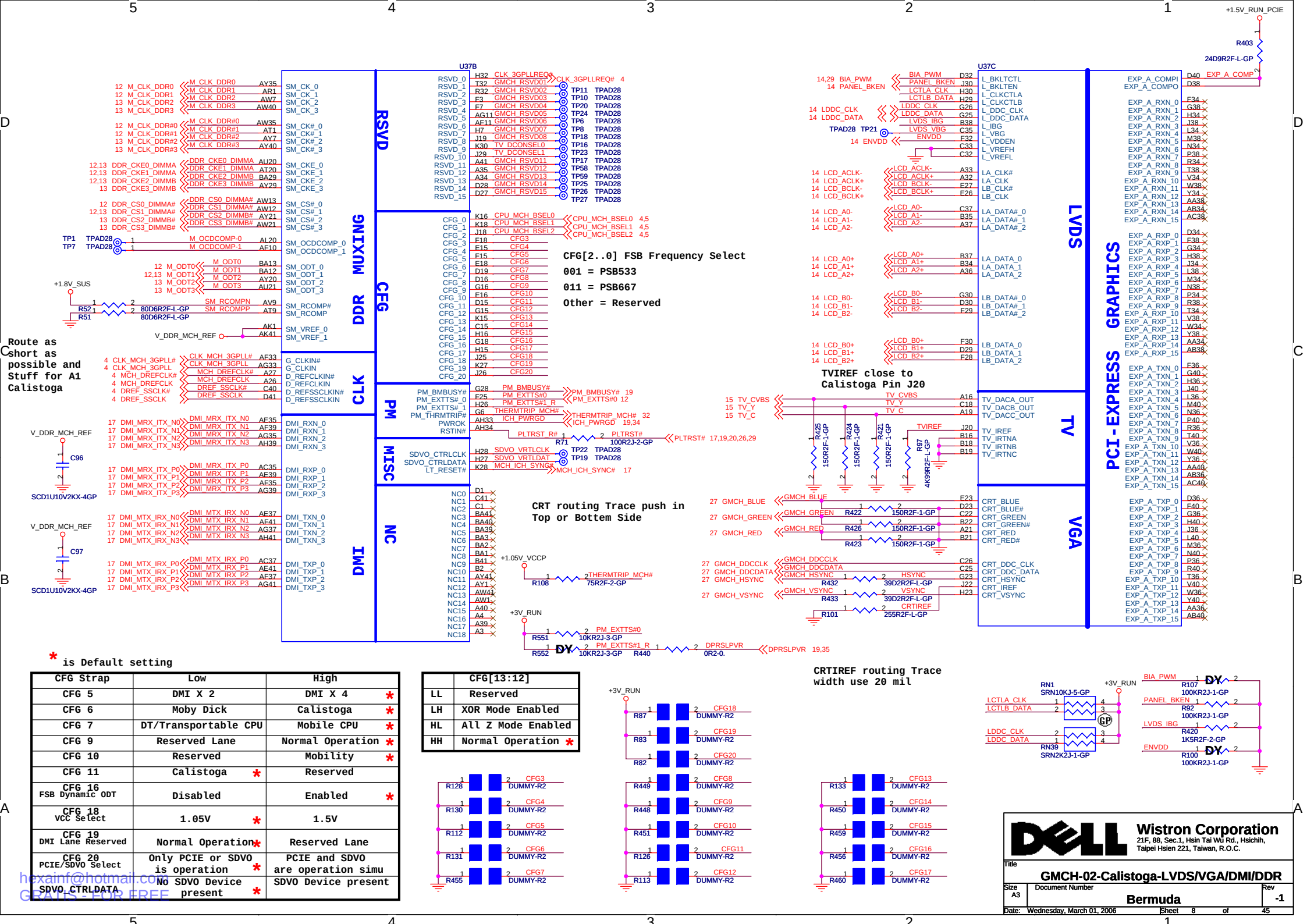
Title: GMCH - 01 - Calistoga - FSB

Size	Document Number	Rev
A3	Bermuda	-1

Date: Wednesday, March 01, 2006 Sheet 7 of 45



* is Default setting

CFG Strap	Low	High
CFG 5	DMI X 2	DMI X 4 *
CFG 6	Moby Dick	Calistoga *
CFG 7	DT/Transportable CPU	Mobile CPU *
CFG 9	Reserved Lane	Normal Operation *
CFG 10	Reserved	Mobility *
CFG 11	Calistoga *	Reserved
CFG 16 FSB Dynamic ODT	Disabled	Enabled *
CFG 18 VCC Select	1.05V *	1.5V
CFG 19 DMI Lane Reserved	Normal Operation *	Reserved Lane
CFG 20 PCIE/SDVO Select	Only PCIE or SDVO is operation *	PCIE and SDVO are operation simu
SDVO_CTRLDATA	No SDVO Device present *	SDVO Device present

	CFG[13:12]
LL	Reserved
LH	XOR Mode Enabled
HL	All Z Mode Enabled
HH	Normal Operation *

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Title: GMCH-02-Calistoga-LVDS/VGA/DMI/DDR

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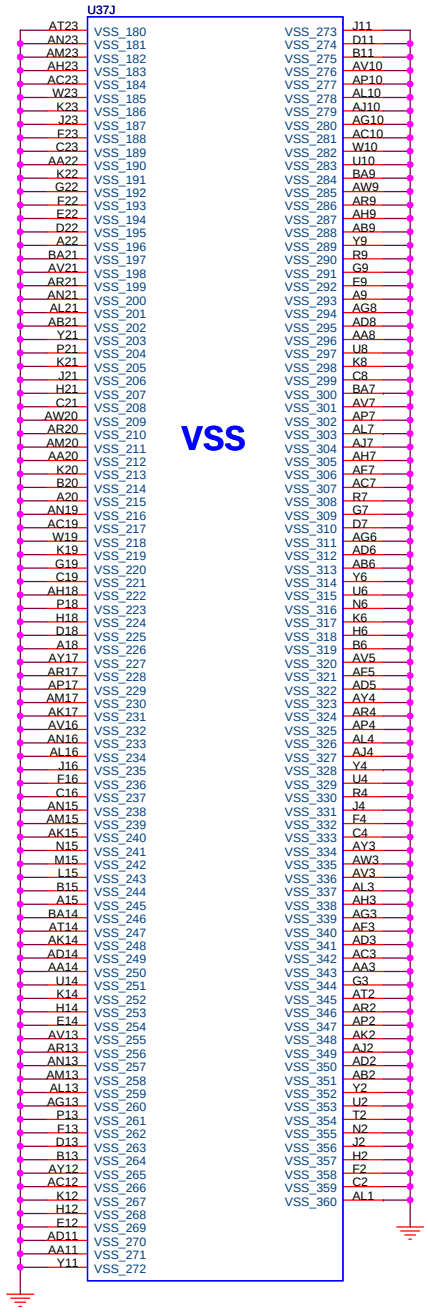
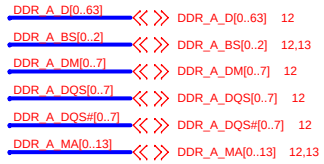
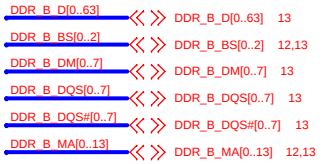
Date: Wednesday, March 01, 2006 | Sheet 8 of 45







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Title: GMCH - 03 - Calistoga - DDR

Size	Document Number	Rev
A3	Bermuda	-1

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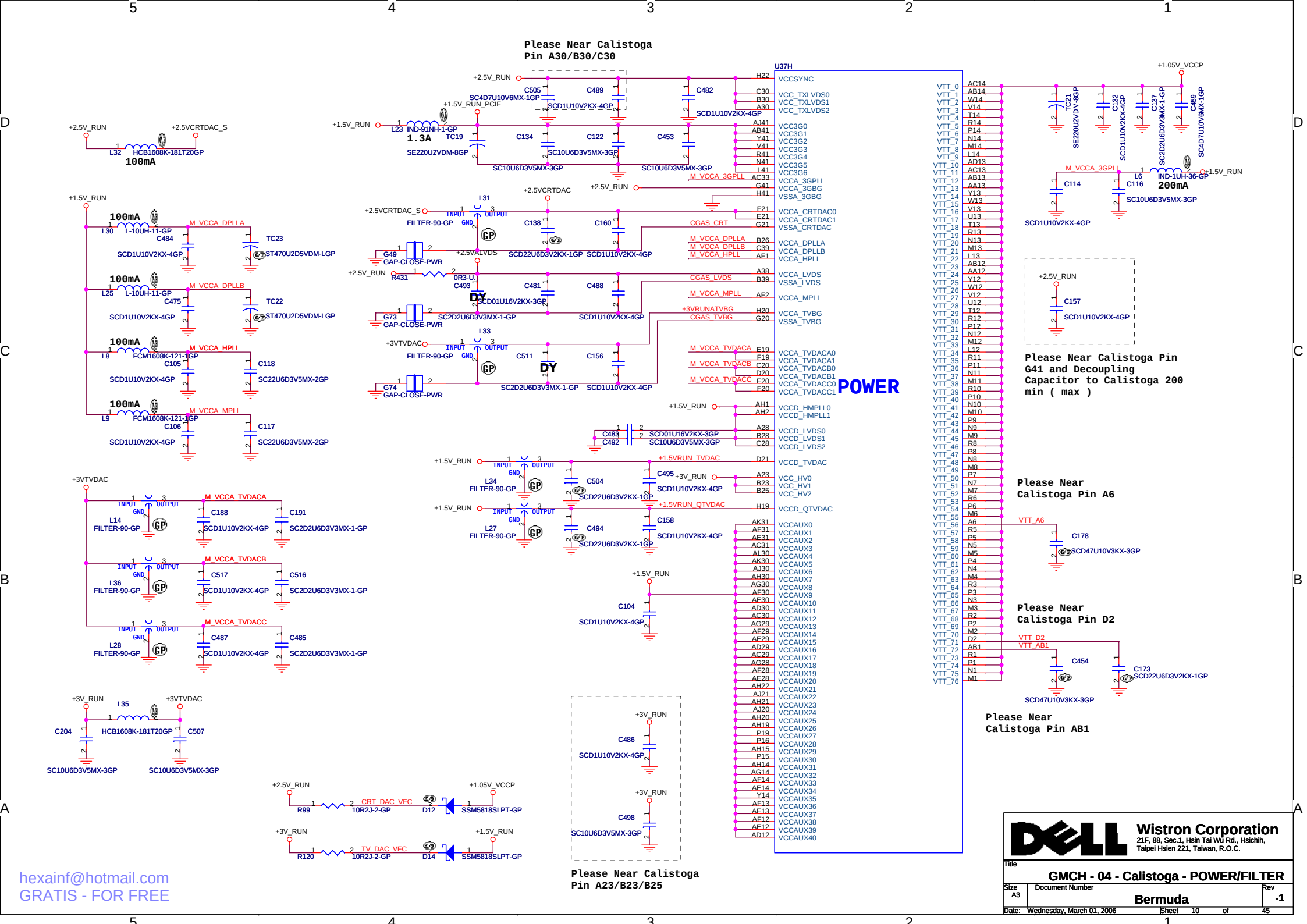
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Pin A30/B30/C30
U37H
POWER
+2.5V_RUN
+2.5VCRTDAC_S
L32 HCB1608K-181T20GP
100mA
+1.5V_RUN
+1.5V_RUN_PCIE
L23 IND-91NH-1-GP
1.3A
TC19
SE220U2VDM-8GP
C305
SC4D7U10V6MX-1GP
C489
C482
SCD1U10V2KX-4GP
C134
C122
C453
SC10U6D3V5MX-3GP
M_VCCA_3GPLL
+2.5VCRTDAC
L31
FILTER-90-GP
C138
C160
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CGAS_CRT
G49 GAP-CLOSE-PWR
+2.5VALVDS
R431 0R3-U
C493
DY
SCD01U16V2KX-3GP
C481
C488
CGAS_LVDS
M_VCCA_MPLL
G73 GAP-CLOSE-PWR
SC2D2U6D3V3MX-1-GP
+3VRUNATVBG
CGAS_TVBG
+3VTVDAC
C511
C156
G74 GAP-CLOSE-PWR
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M_VCCA_TVDACB
M_VCCA_TVDACC
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TC23
ST470U2D5VDM-LGP
L25 L-10UH-11-GP
C475
TC22
L8 FCM1608K-121-1GP
C105
C118
SC22U6D3V5MX-2GP
L9 FCM1608K-121-1GP
C106
C117
L14 FILTER-90-GP
C188
C191
L36 FILTER-90-GP
C517
C516
L28 FILTER-90-GP
C487
C485
+3V_RUN
L35 HCB1608K-181T20GP
C204
C507
+1.5V_RUN
L33
L34 FILTER-90-GP
C504
C495
+3V_RUN
+1.5VRUN_TVDAC
L27 FILTER-90-GP
C494
C158
+1.5VRUN_QTVDAC
C104
+2.5V_RUN
R99 CRT_DAC_VFC 10R2J-2-GP
D12 SSM5818SLPT-GP
+1.05V_VCCP
R120 TV_DAC_VFC 10R2J-2-GP
D14 SSM5818SLPT-GP
+3V_RUN
C486
C498
SC10U6D3V5MX-3GP
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Pin A23/B23/B25
VCCSYNC
VCC_TXLVDS0
VCC_TXLVDS1
VCC_TXLVDS2
VCC3G0
VCC3G1
VCC3G2
VCC3G3
VCC3G4
VCC3G5
VCC3G6
VCCA_3GPLL
VCCA_3GBG
VSSA_3GBG
VCCA_CRTDAC0
VCCA_CRTDAC1
VSSA_CRTDAC
VCCA_DPLLA
VCCA_DPLLB
VCCA_HPLL
VCCA_LVDS
VSSA_LVDS
VCCA_MPLL
VCCA_TVBG
VSSA_TVBG
VCCA_TVDACA0
VCCA_TVDACA1
VCCA_TVDACB0
VCCA_TVDACB1
VCCA_TVDACC0
VCCA_TVDACC1
VCCD_HMPLL0
VCCD_HMPLL1
VCCD_LVDS0
VCCD_LVDS1
VCCD_LVDS2
VCCD_TVDAC
VCC_HV0
VCC_HV1
VCC_HV2
VCCD_QTVDAC
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VCCAUX3
VCCAUX4
VCCAUX5
VCCAUX6
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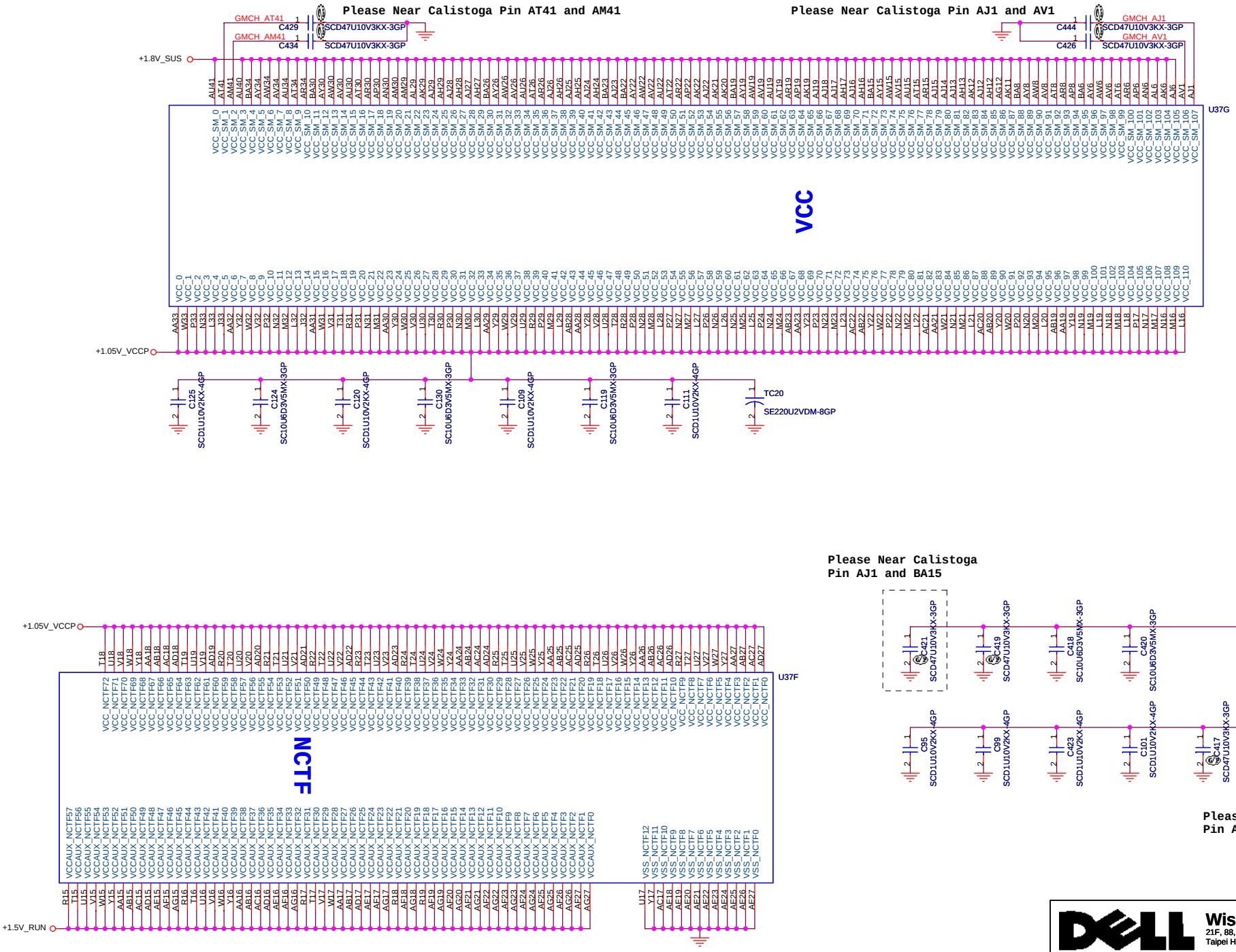
VTT_75
VTT_76
+1.05V_VCCP
TC21
SE220U2VDM-8GP
C132
SCD1U10V2KX-4GP
C137
SC2D2U6D3V3MX-1-GP
C459
SC4D7U10V6MX-1GP
M_VCCA_3GPLL
L6 IND-1UH-36-GP
200mA
C114
C116
SC10U6D3V5MX-3GP
SCD1U10V2KX-4GP
+2.5V_RUN
C157
SCD1U10V2KX-4GP
Please Near Calistoga Pin
G41 and Decoupling
Capacitor to Calistoga 200
min (max)
Please Near
Calistoga Pin A6
VTT_A6
C178
SCD47U10V3KX-3GP
Please Near
Calistoga Pin D2
VTT_D2
VTT_AB1
C454
C173
SCD22U6D3V2KX-1GP
SCD47U10V3KX-3GP
Please Near
Calistoga Pin AB1
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
GMCH - 04 - Calistoga - POWER/FILTER
Size A3
Document Number
Bermuda
Rev -1
Date: Wednesday, March 01, 2006
Sheet 10 of 45
hexainf@hotmail.com
GRATIS - FOR FREE



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Title: GMCH - 05 - Calistoga - POWER

Size	Document Number	Rev
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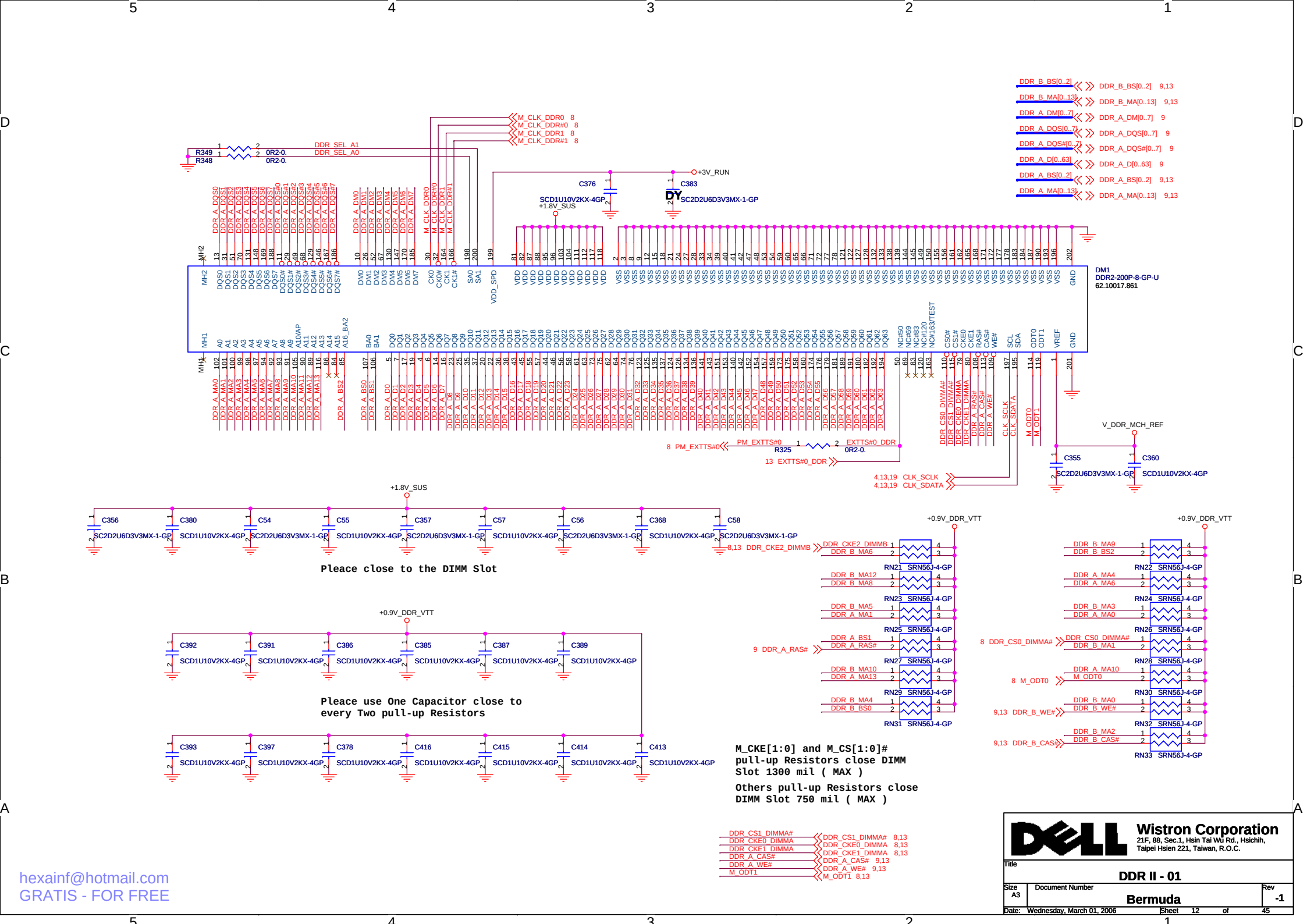
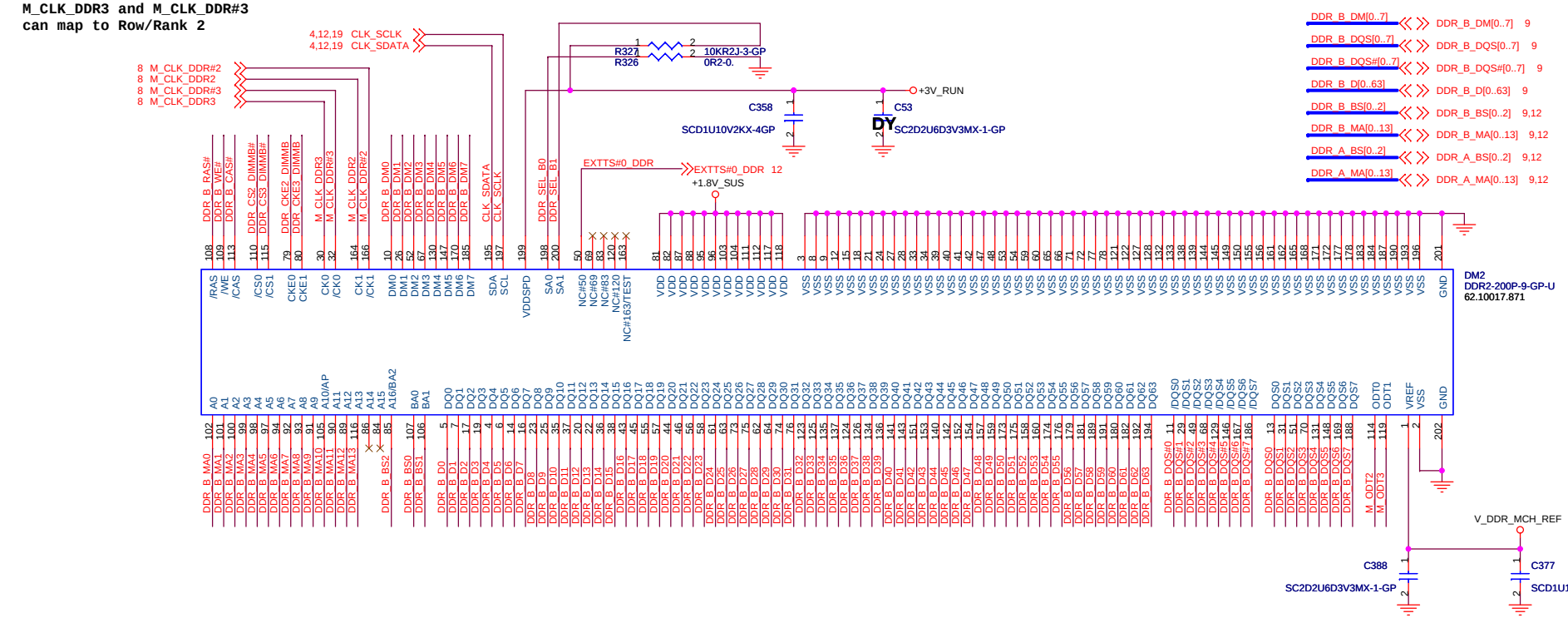
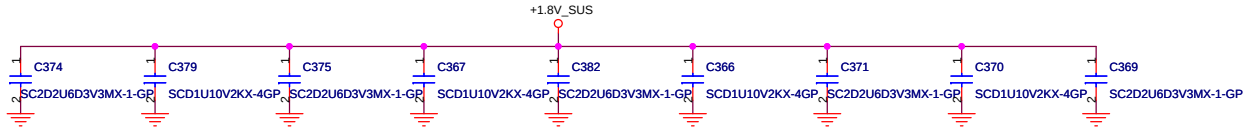
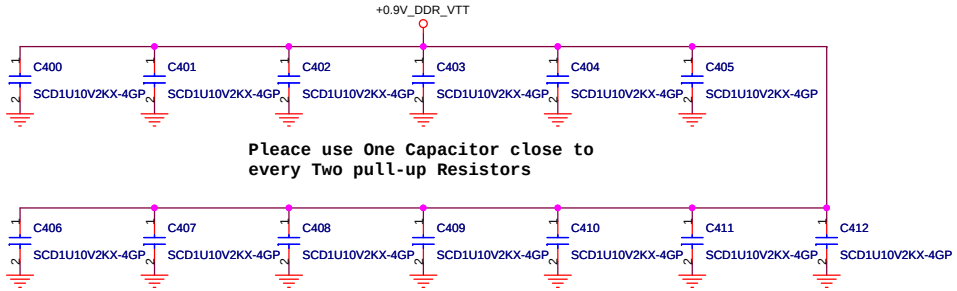


M_CLK_DDR3 and M_CLK_DDR#3
can map to Row/Rank 2

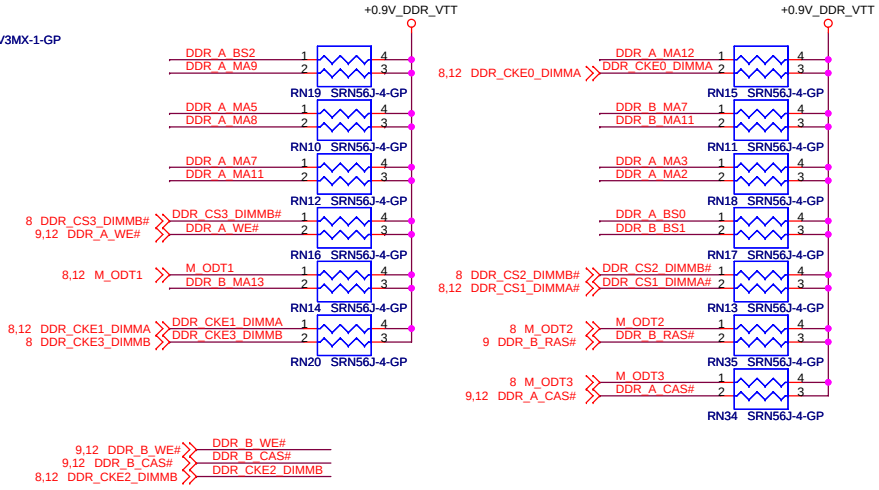




Please close to the DIMM Slot



Please use One Capacitor close to
every Two pull-up Resistors



M_CKE[3:2] and M_CS[3:2]#
pull-up Resistors close DIMM
Slot 1300 mil (MAX)

Others pull-up Resistors close
DIMM Slot 750 mil (MAX)

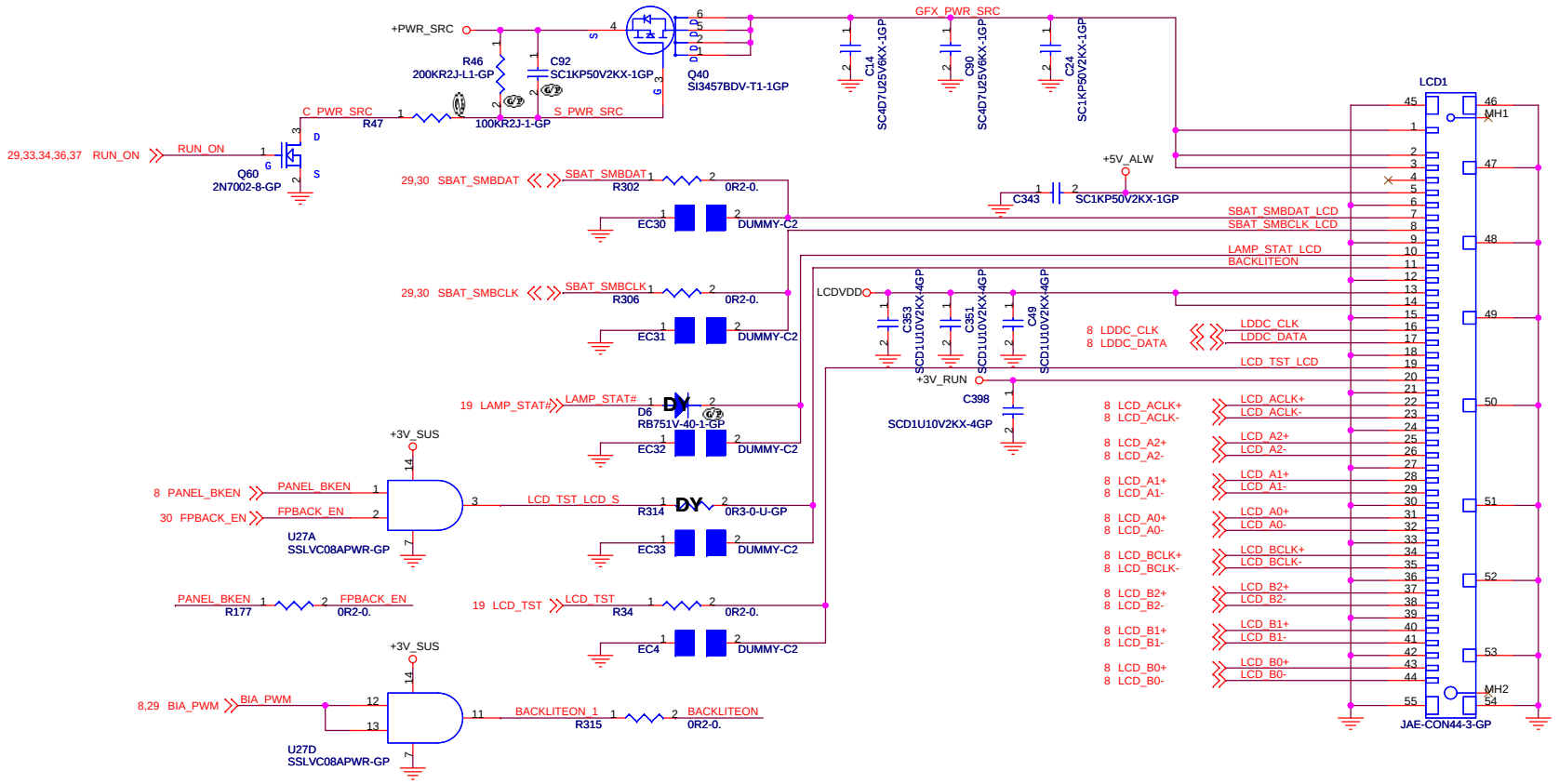
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR II - 02

Size	Document Number	Rev
A3	Bermuda	-1

Date: Wednesday, March 01, 2006 Sheet 13 of 45

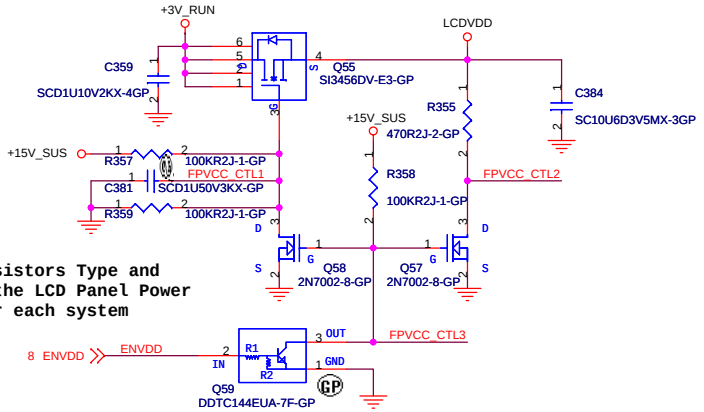
SSID = VIDEO



M00 support D05 Inverter

M'07 Inverter support : Populate this Two Resister and De-populate this SSLVC08APWR

D'05 Inverter support : De-populate this Two Resister and Populate this SSLVC08APWR

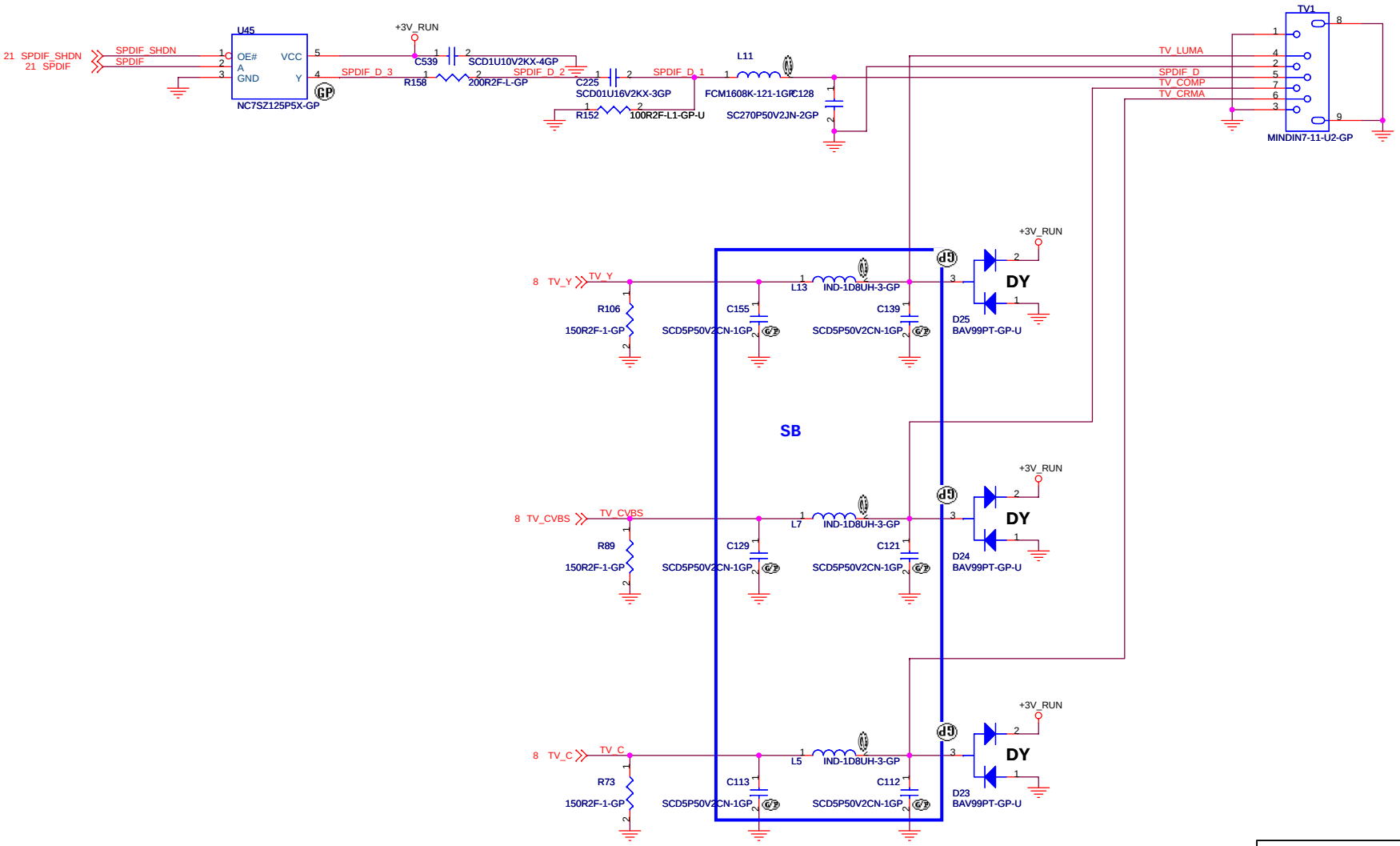


Choose the Transistors Type and Rating base on the LCD Panel Power requirements for each system

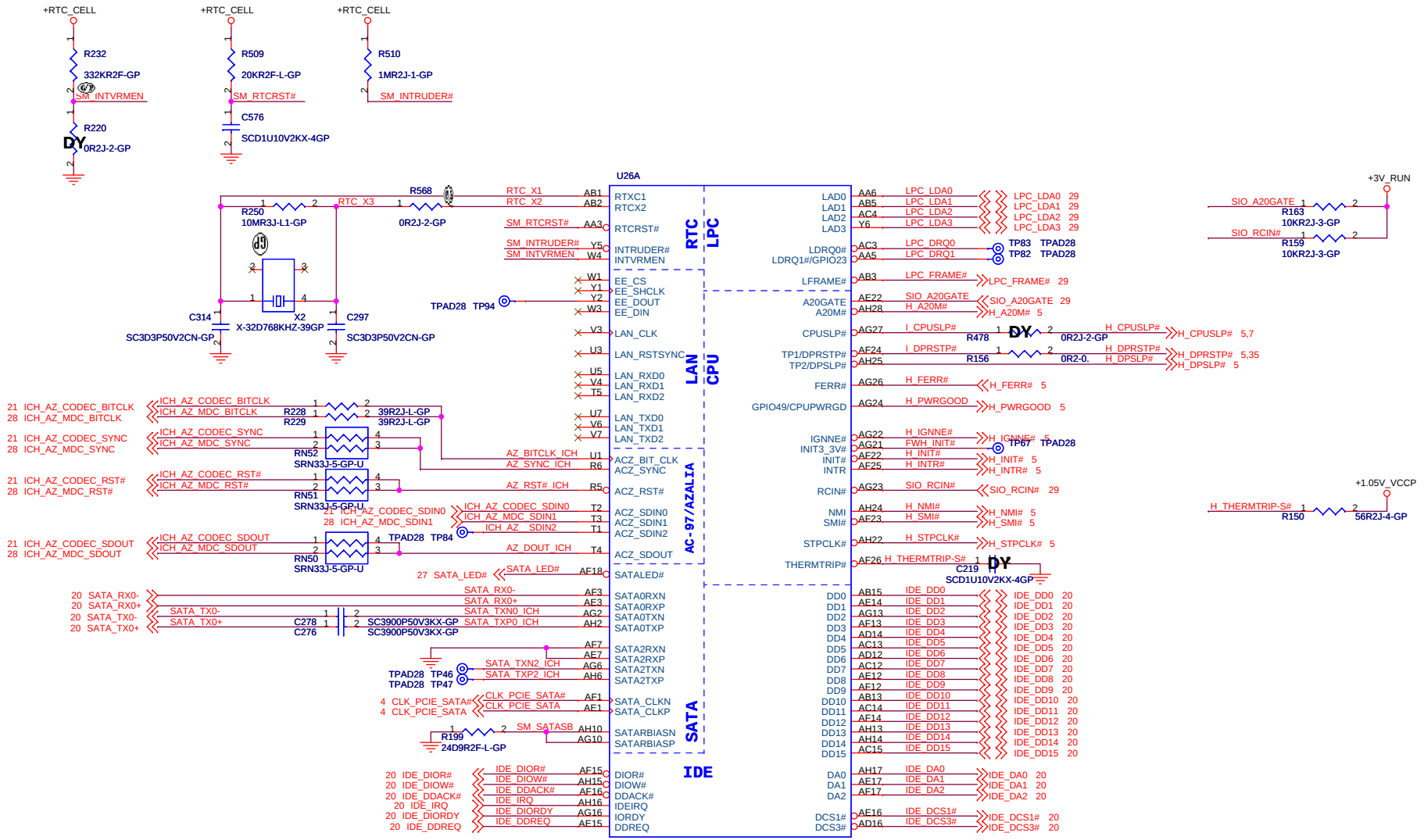
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	LCD	
Size: A3	Document Number: Bermuda	Rev: -1
Date: Wednesday, March 01, 2006	Sheet 14 of 45	

SSID = VIDEO



Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	TV OUT
Size: A3	Document Number: Bermuda
Rev	-1
Date: Wednesday, March 01, 2006	Sheet 15 of 45

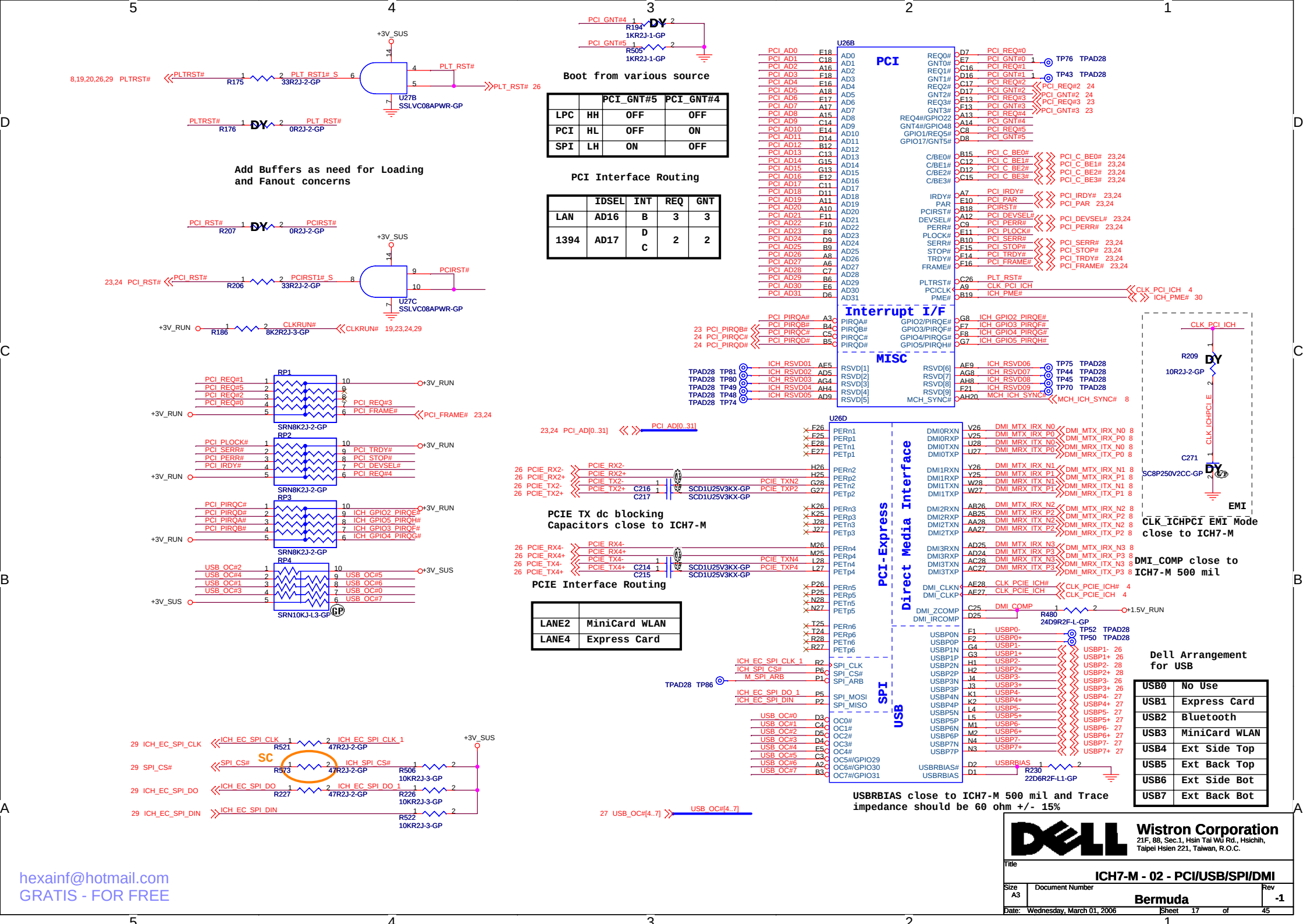


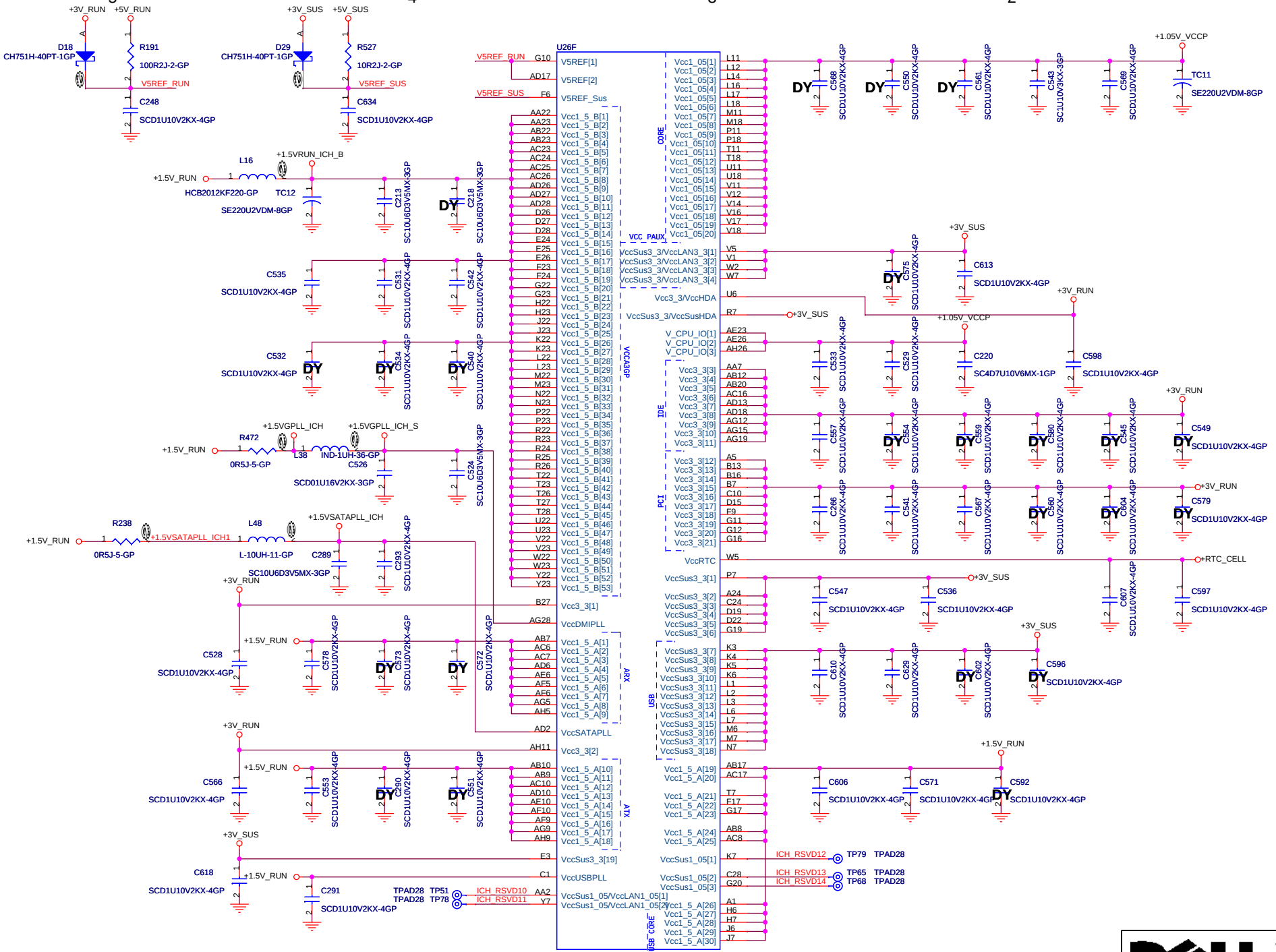
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH7-M - 01 - PM/IDE/LPC/AC97

Size	Document Number	Rev
A3	Bermuda	-1

Date: Wednesday, March 01, 2006 Sheet 16 of 45



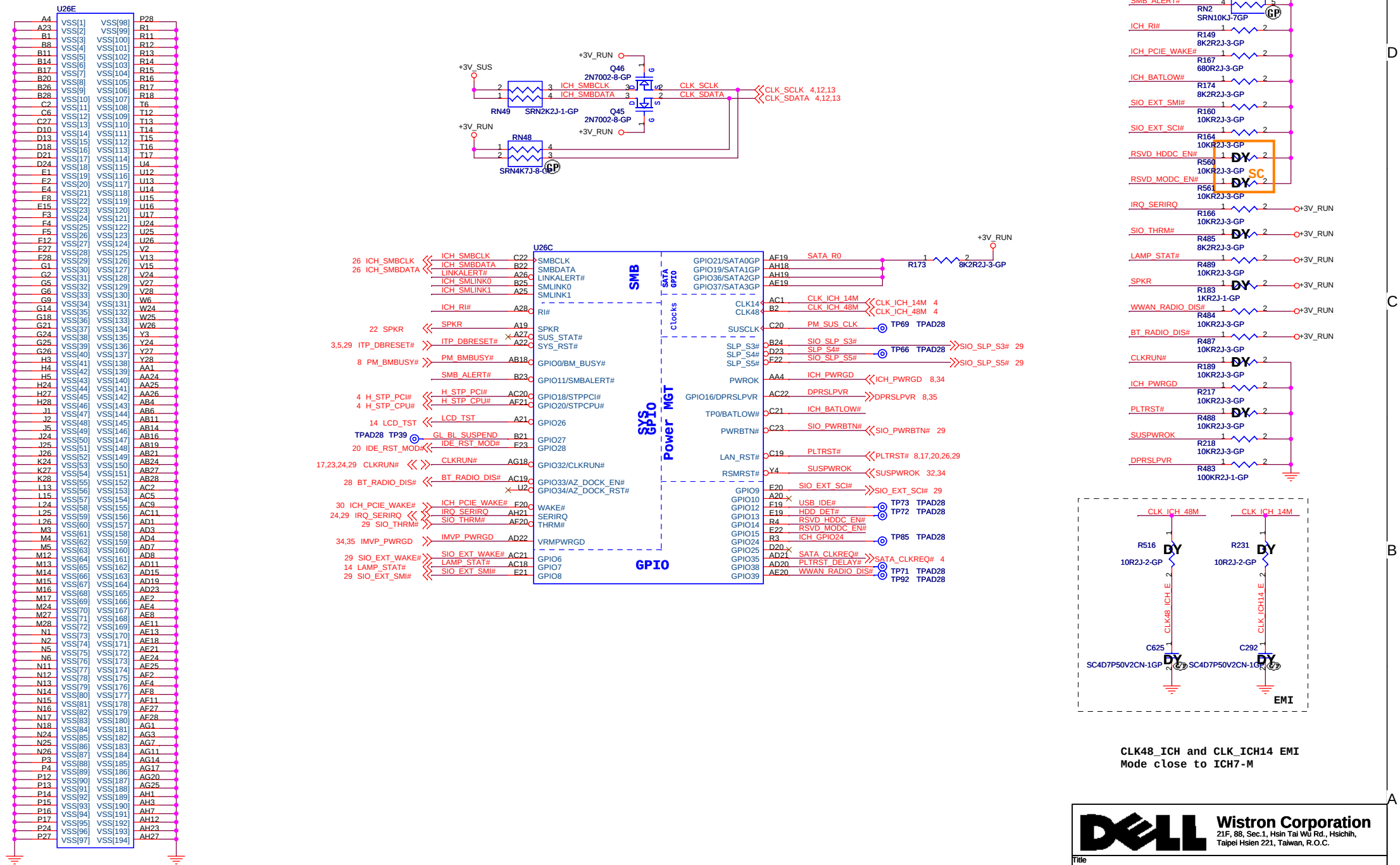


Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH7-M - 03 - POWER

Size	Document Number	Rev
A3	Bermuda	-1

Date: Wednesday, March 01, 2006 Sheet 18 of 45



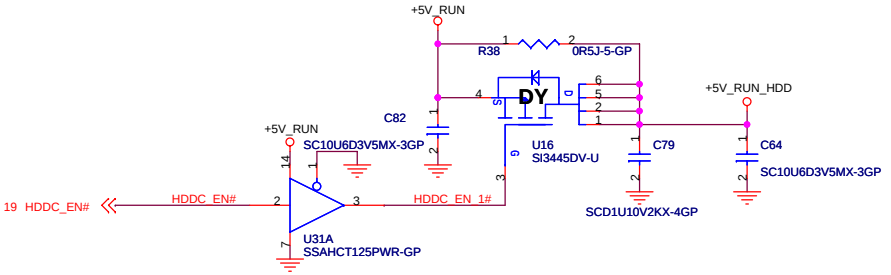
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

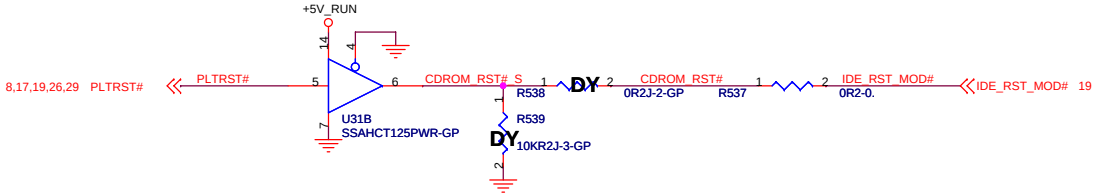
Title: ICH7-M - 04 - PM/GPIO

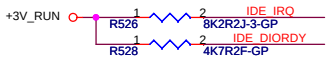
Size	Document Number	Rev
A3	Bermuda	-1

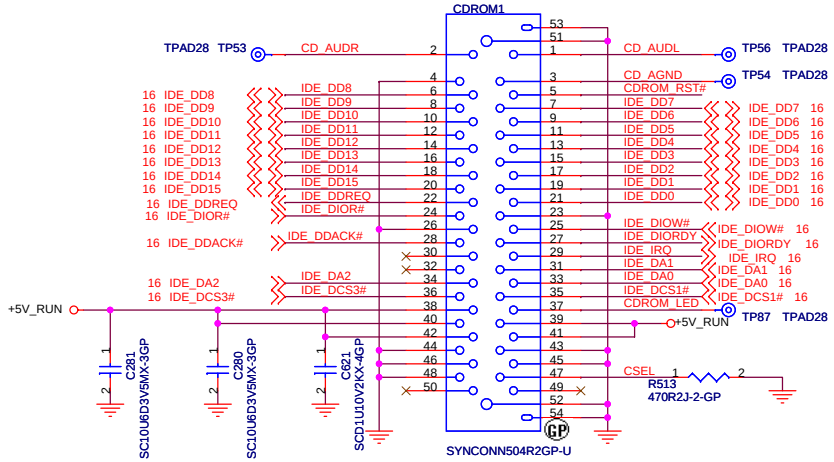
Date: Wednesday, March 01, 2006 Sheet 19 of 45

SSID = IDE & SATA

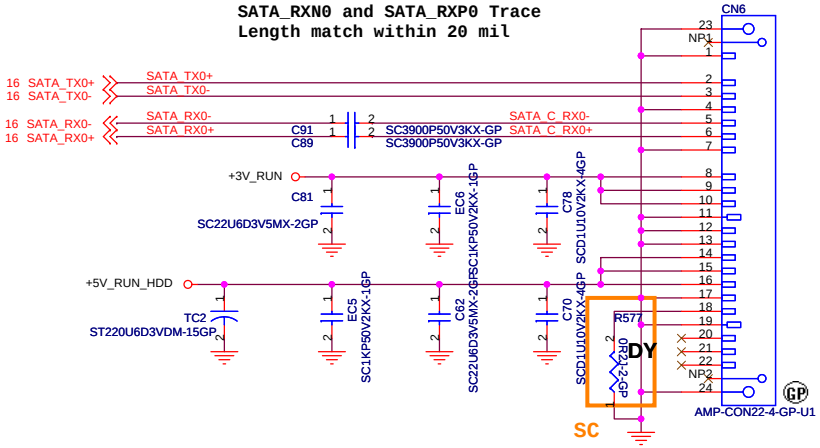








SATA_RXN0 and SATA_RXP0 Trace Length match within 20 mil

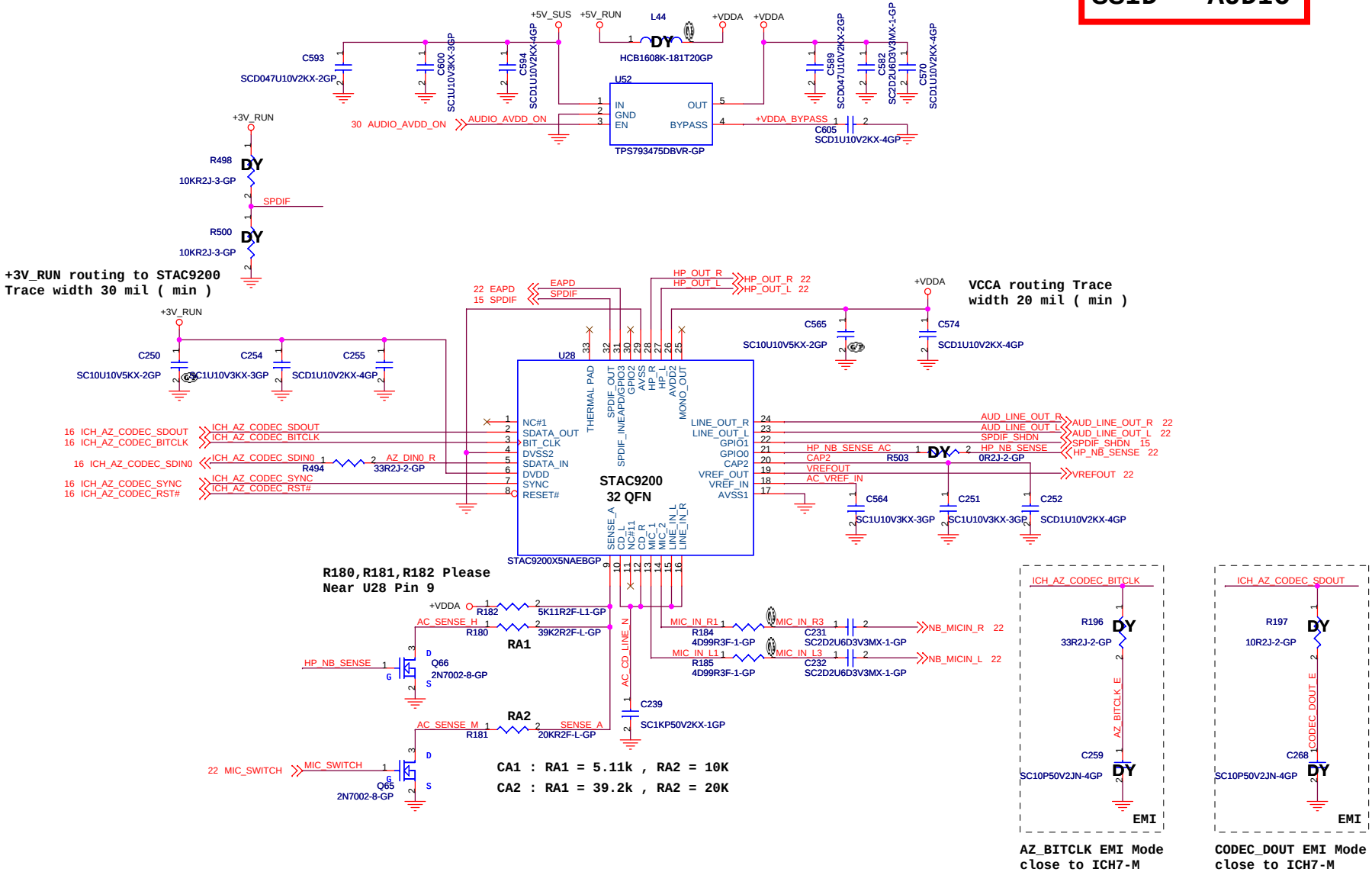


SATA HD Connector

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	SATA IDE & CD-ROM	
Size A3	Document Number Bermuda	Rev -1
Date: Wednesday, March 01, 2006	Sheet 20 of 45	

SSID = AUDIO



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO - 01 - STAC9200

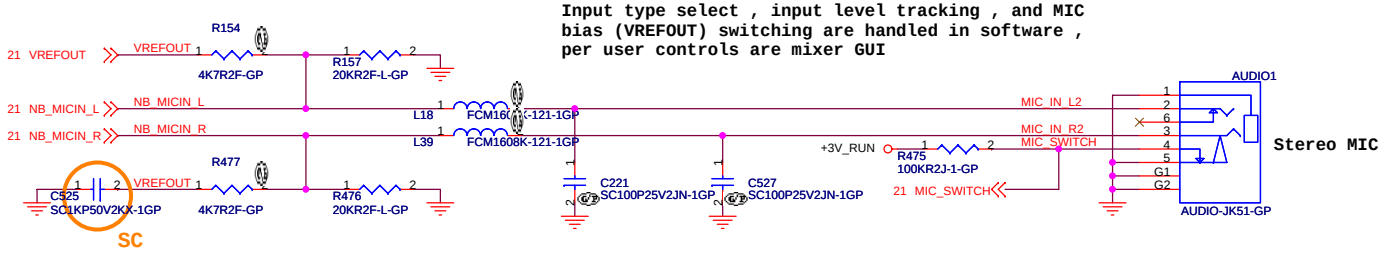
Size	Document Number	Rev
A3	Bermuda	-1

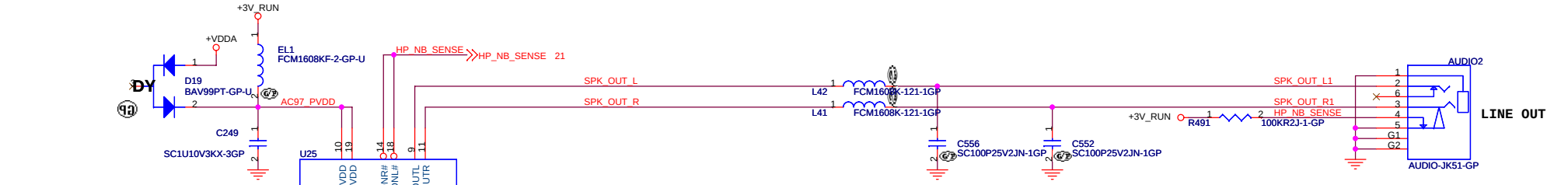
Date: Wednesday, March 01, 2006 Sheet 21 of 45

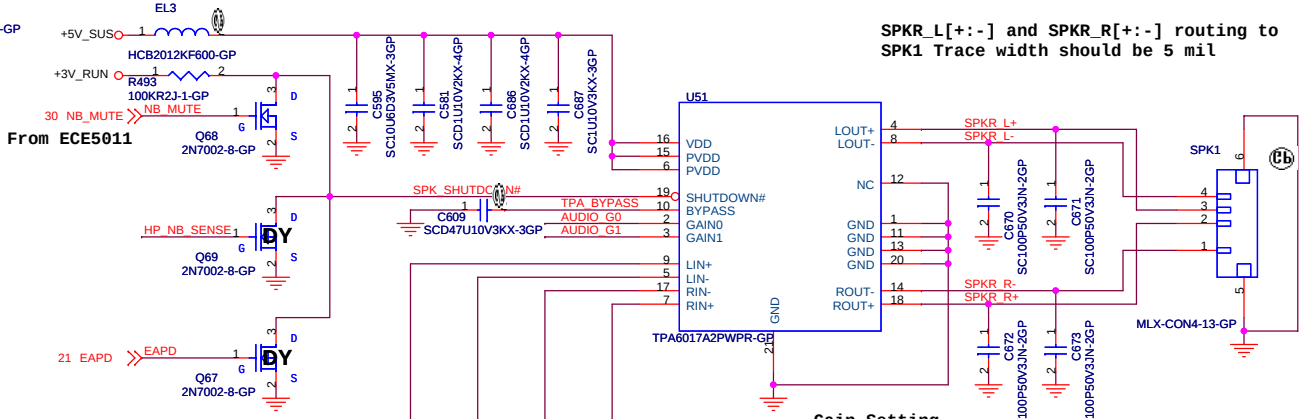
SSID = AUDIO

NOTE :

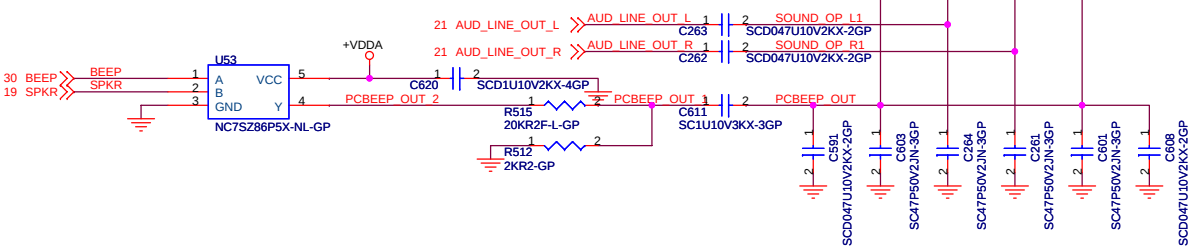
Input type select , input level tracking , and MIC bias (VREFOUT) switching are handled in software , per user controls are mixer GUI





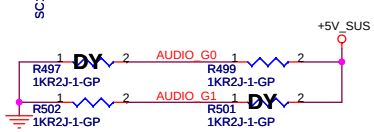


SPKR_L[+:-] and SPKR_R[+:-] routing to SPK1 Trace width should be 5 mil



Gain Setting

AV	GAIN0	GAIN1
6dB	0	0
10dB	0	1
15.6dB	1	0
21.6dB	1	1



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **ADUIO - 02 - SPK/MIC/LINE-OUT**

Size: A3 | Document Number: **Bermuda** | Rev: **-1**

Date: Wednesday, March 01, 2006 | Sheet 22 of 45

Broadcom LAN

BCM4401

SSID = LOM

R246 ~ R249 use 1/16 Watt Resistors

This Capacitor close to BCM4401 Pin 65

The BCM4401L has weak internal pulldown resistors on the follow signals :

LAN_EECLK, LAN_EEDATA, SPROMDOUT, SPROMDIN

U48 2nd use 72.93C46.N01

EXT_POR_L is an active low signal used to place the BCM4401 into IDDQ mode, <5 mA current consumption

BCM4401KQLG-GP

U30

U48

AT93C46-10SU-1GP

Q51 Q52 Q53 DTA144EUA-2-GP

Wistron Corporation
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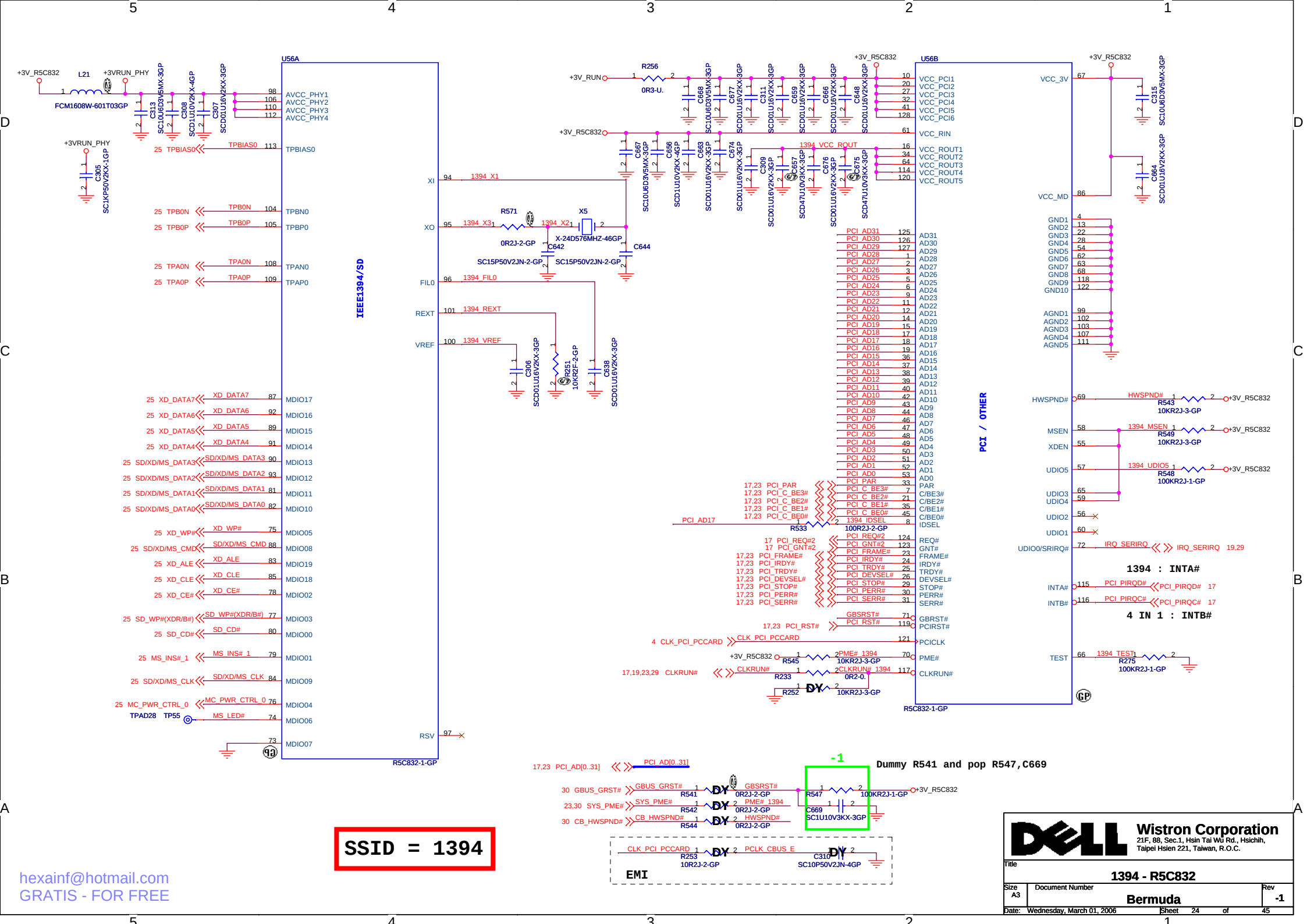
Taipei Hsien 221, Taiwan, R.O.C.

Title		
LAN - BCM4401		
Size: A3	Document Number: Bermuda	Rev: -1
Date: Wednesday, March 01, 2006	Sheet 23 of 45	



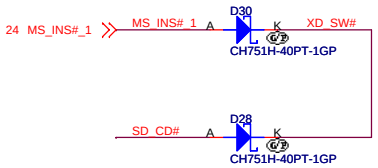
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

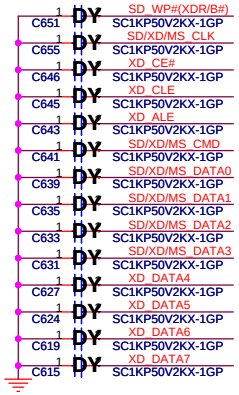
Title: 1394 - R5C832

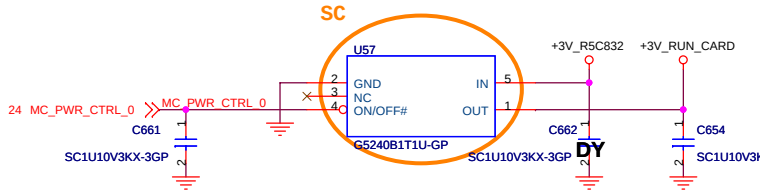
Size: A3 | Document Number: Bermuda | Rev: -1

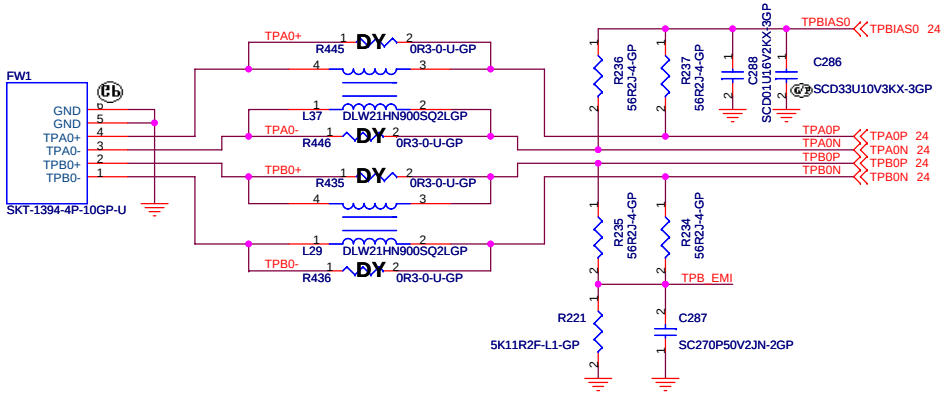
Date: Wednesday, March 01, 2006 | Sheet 24 of 45

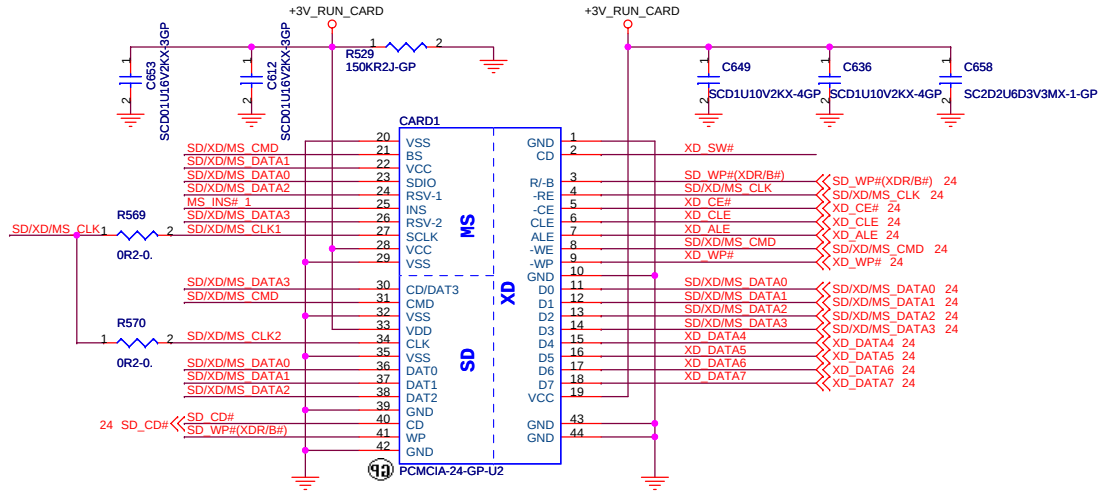
SSID = 1394











Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 1394 - 4 IN 1 Connector

Size	Document Number	Rev
A3	Bermuda	-1

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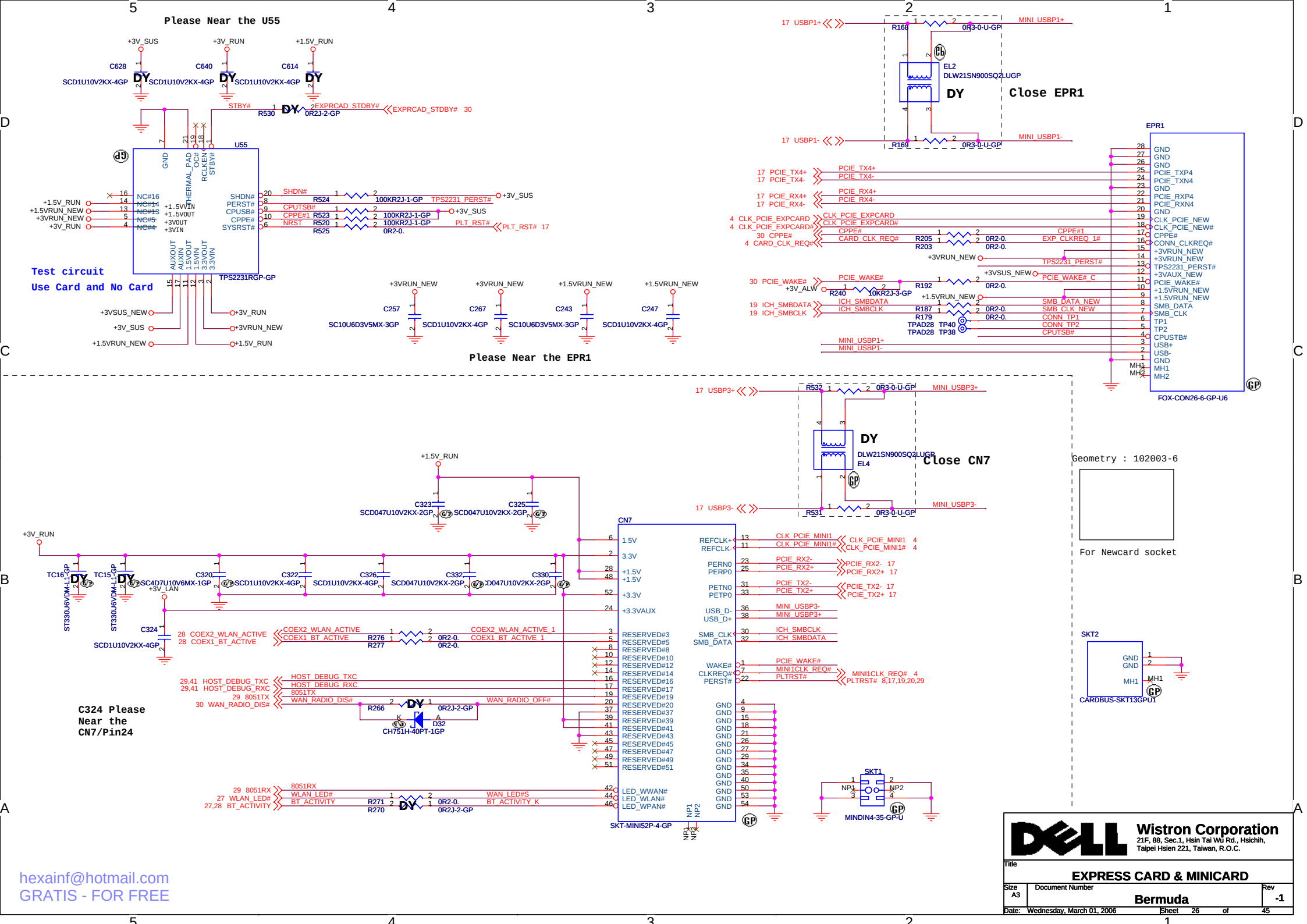
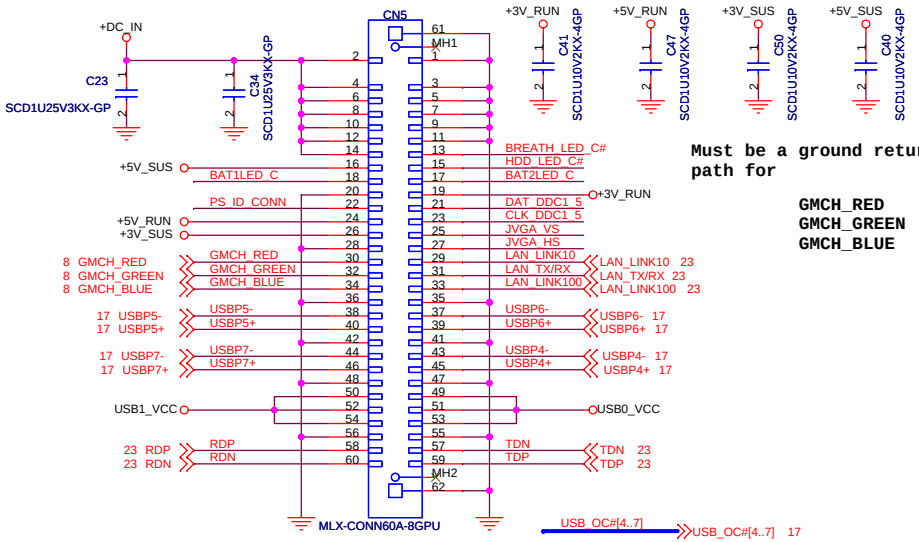
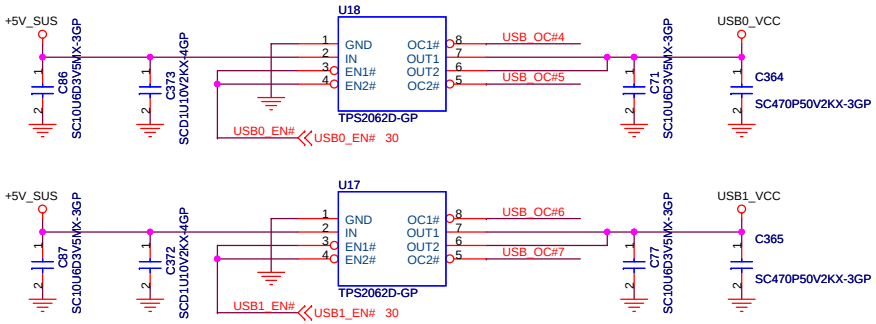


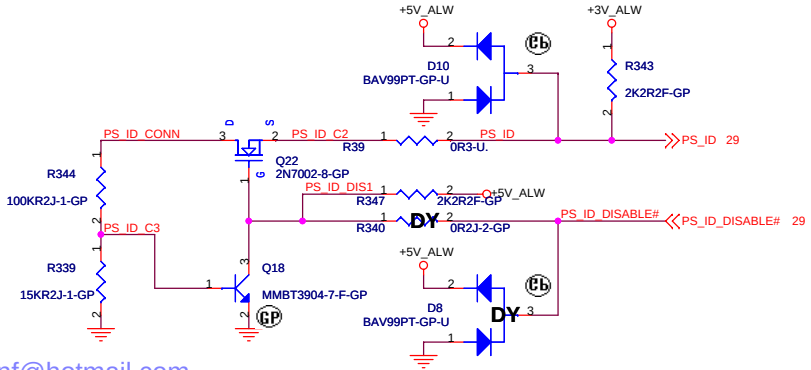
CRT BD Conn



Must be a ground return path for

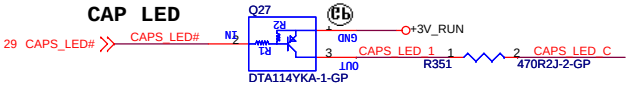
GMCH_RED
GMCH_GREEN
GMCH_BLUE



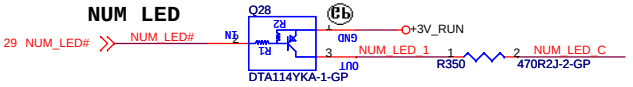


hexainf@hotmail.com
GRATIS - FOR FREE

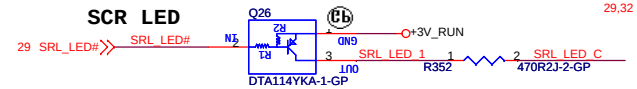
CAP LED



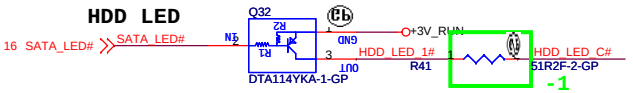
NUM LED



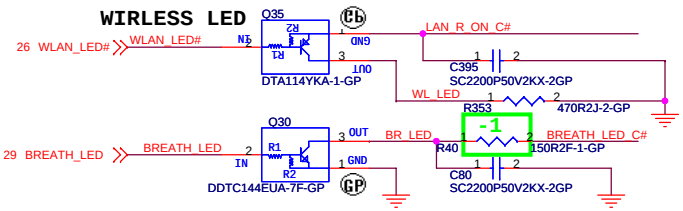
SCR LED

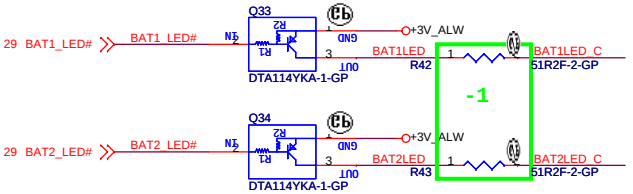


HDD LED

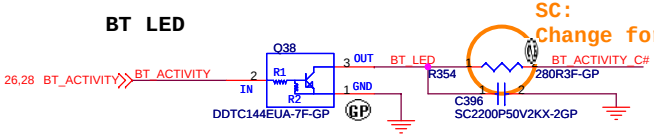


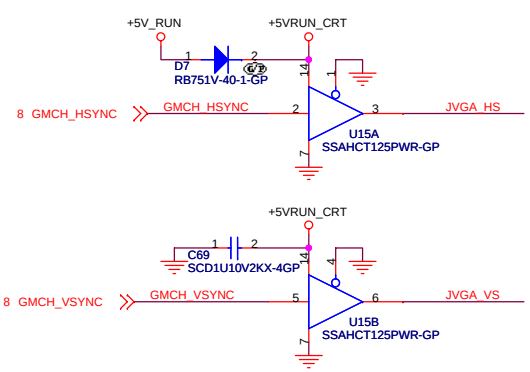
WIRLESS LED

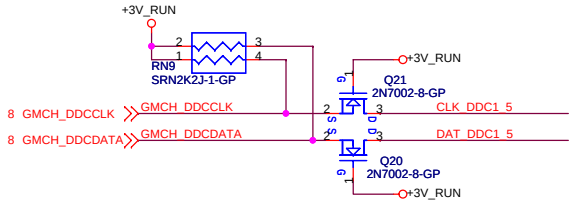


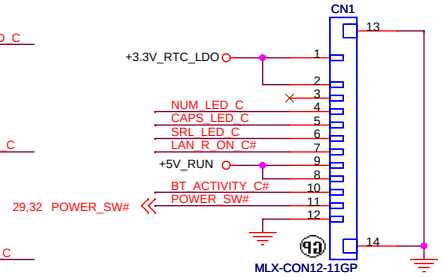


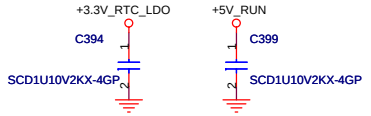
BT LED











Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT BD CONN & LED

Size	Document Number	Rev
A3	Bermuda	-1

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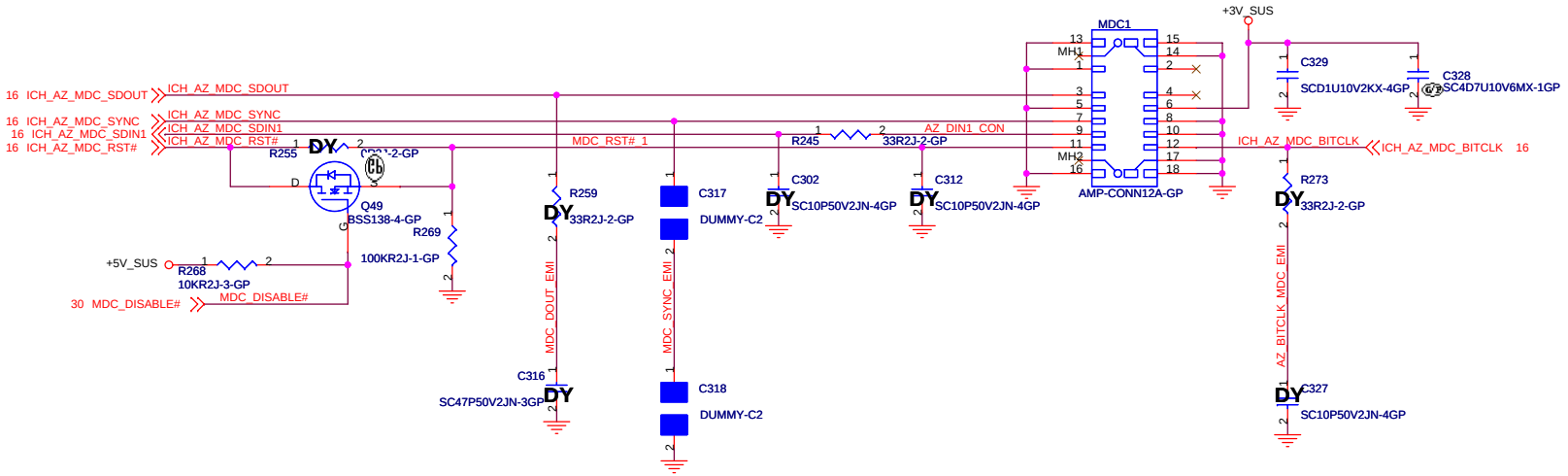
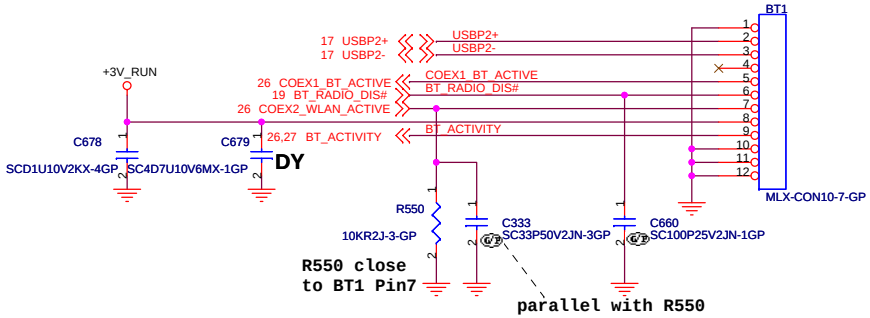
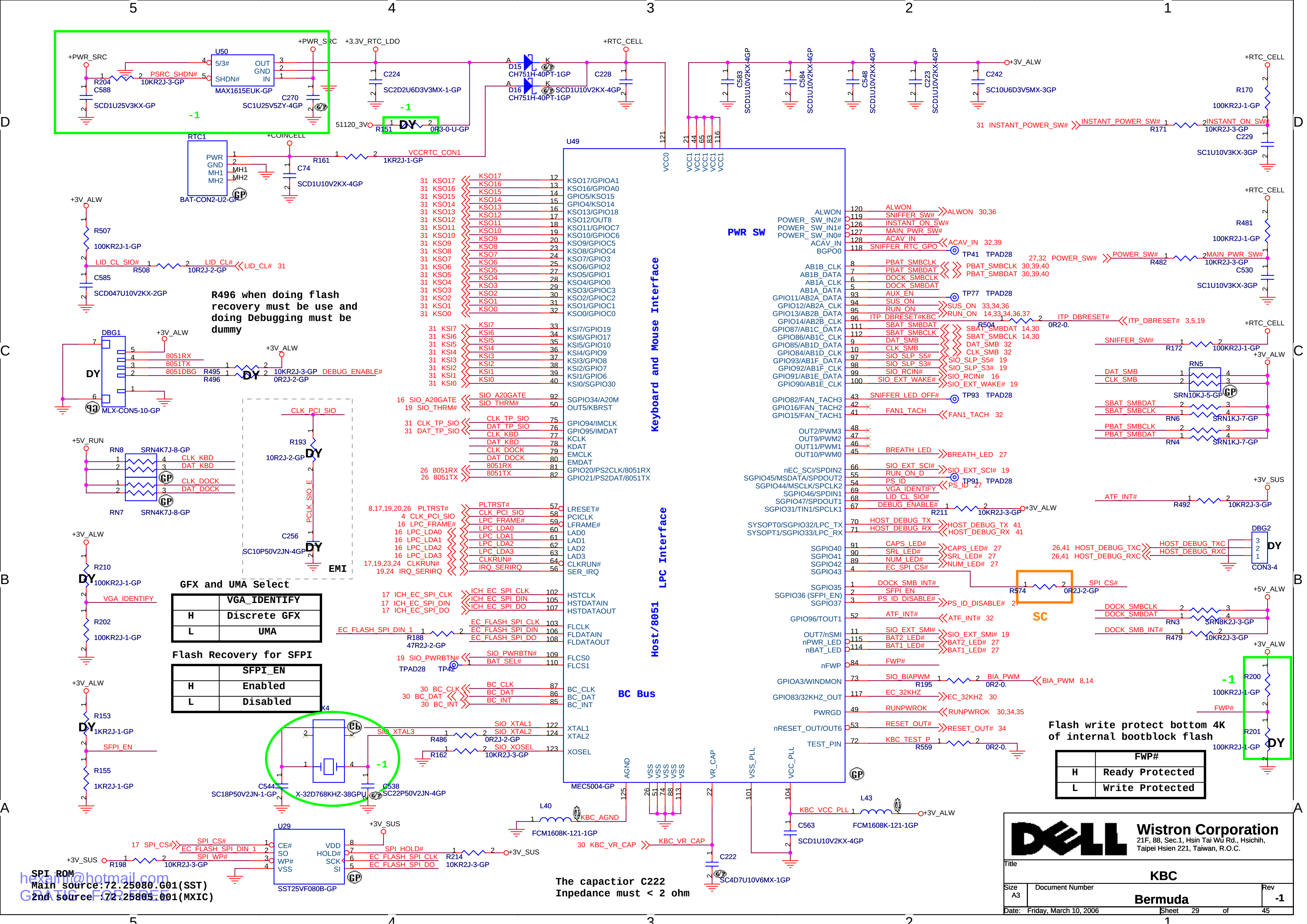
Modem Connector
(Not Standard Type)



Bluetooth Module conn.



Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: MDC & BT		
Size: A3	Document Number: Bermuda	Rev: -1
Date: Wednesday, March 01, 2006	Sheet 28 of 45	



R496 when doing flash recovery must use and doing Debugging must be dummy

GFX and UMA Select

	VGA_IDENTIFY
H	Discrete GFX
L	UMA

Flash Recovery for SFPI

	SFPI_EN
H	Enabled
L	Disabled

Flash write protect bottom 4K of internal bootblock flash

	FWP#
H	Ready Protected
L	Write Protected

SPI ROM
Main source:72.25080.G01(SST)
2nd source :72.25805.001(MXIC)

The capactior C222
Inpedance must < 2 ohm

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: KBC
Size: A3 Document Number: Bermuda Rev: -1
Date: Friday, March 10, 2006 Sheet 29 of 45

Board ID Strap

REV	KBC_BID0	KBC_BID1	KBC_BID2	KBC_BID3
X00	0	0	0	0
X01	1	0	0	0
X02	0	1	0	0
X03	1	1	0	0
X04	0	0	1	0

PLEASE NEAR KBC

5004 WORK AROUND

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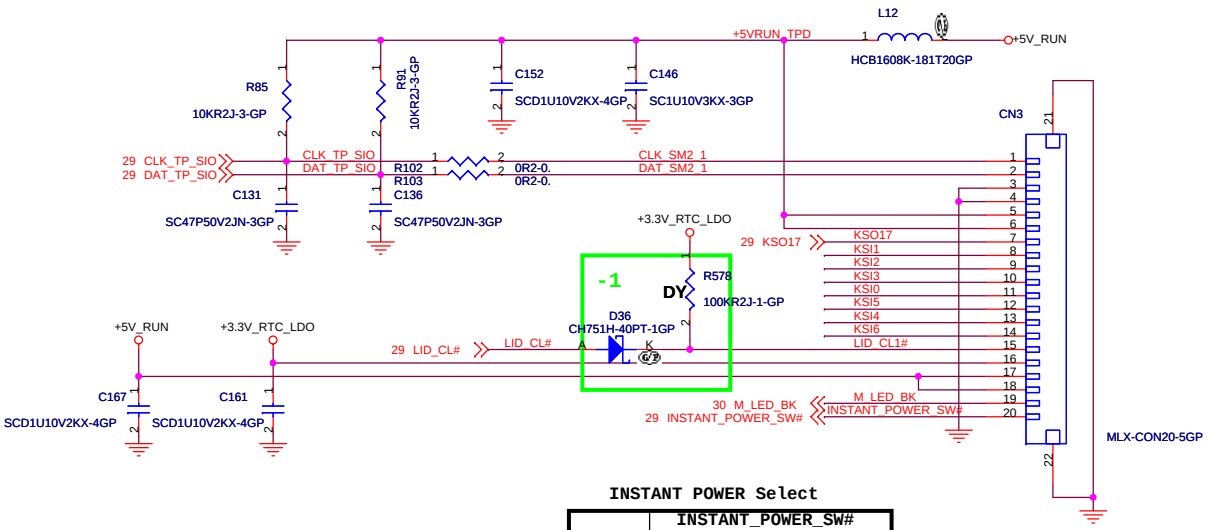
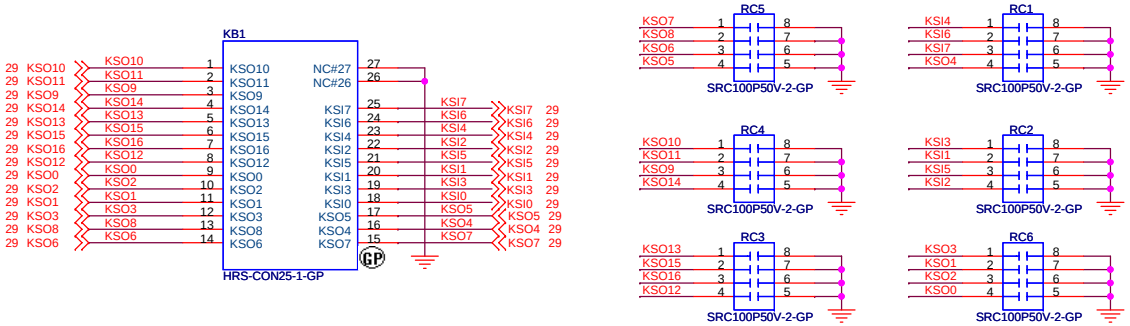
Title		
SIO		
Size: A3	Document Number: Bermuda	Rev: -1
Date: Wednesday, March 01, 2006	Sheet 30 of 45	



INSTANT POWER Select

	INSTANT_POWER_SW#
H	Power On Function
L	Regular Play Function

Media PlayBack / TouchPAD Connector



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Title: KB & TPAD

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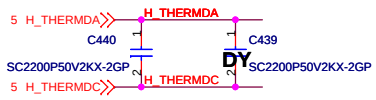
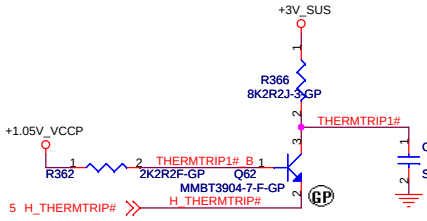
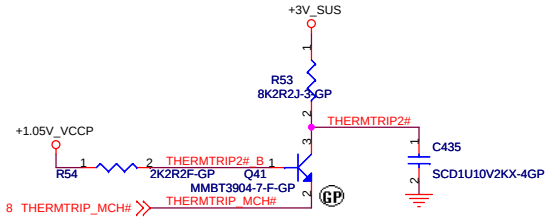
SSID = THERMAL

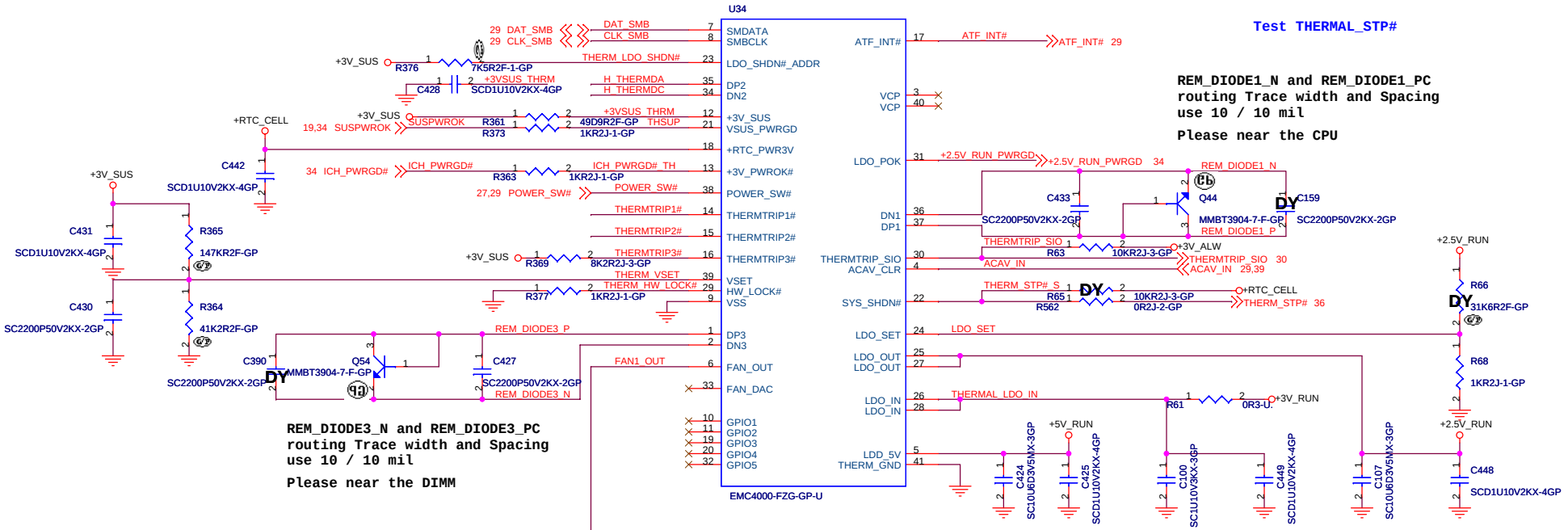
H_THERMDA and H_THERMDC routing Trace width and Spacing use 10 / 10 mil

Reserve area near CPU for a cap between DP2/DN2









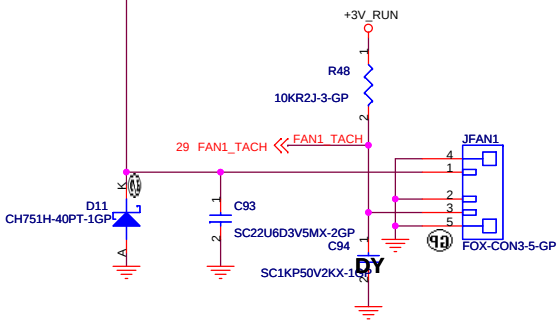
Test THERMAL_STP#

REM_DIODE1_N and REM_DIODE1_PC routing Trace width and Spacing use 10 / 10 mil

Please near the CPU

REM_DIODE3_N and REM_DIODE3_PC routing Trace width and Spacing use 10 / 10 mil

Please near the DIMM



Note :

VSET = (Tp - 70) / 21
3.3 * (R364 / R365 + R364) = (Tp - 70) / 21
Where Tp = 70 to 101 degrees C
Tp set at 85 degrees C
Guardian temp tolerance = +/- 3 degrees C

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Title: THERMAL Sensor & FAN

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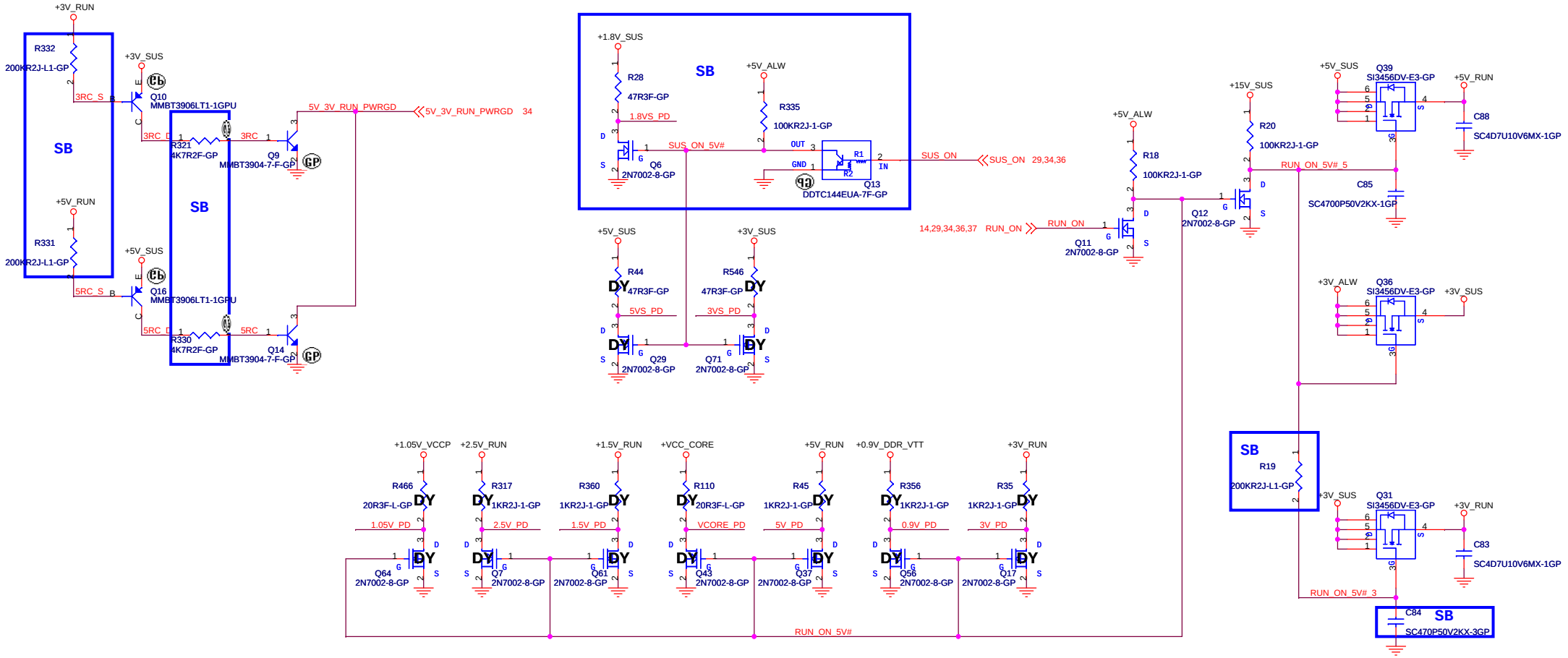

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Title: POWER PLANE ENABLE

Size	Document Number	Rev
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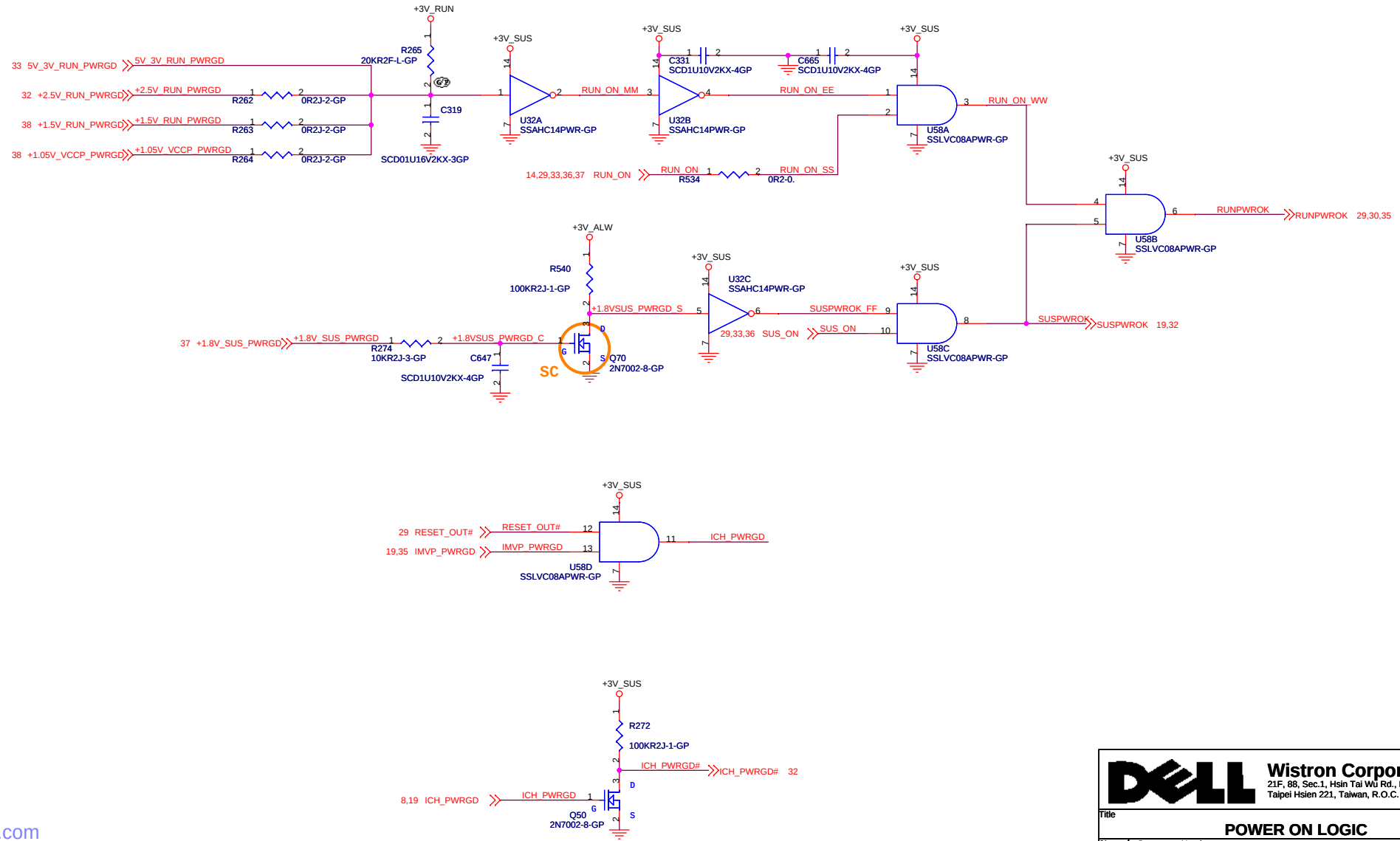

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Title: POWER ON LOGIC

Size	Document Number	Rev
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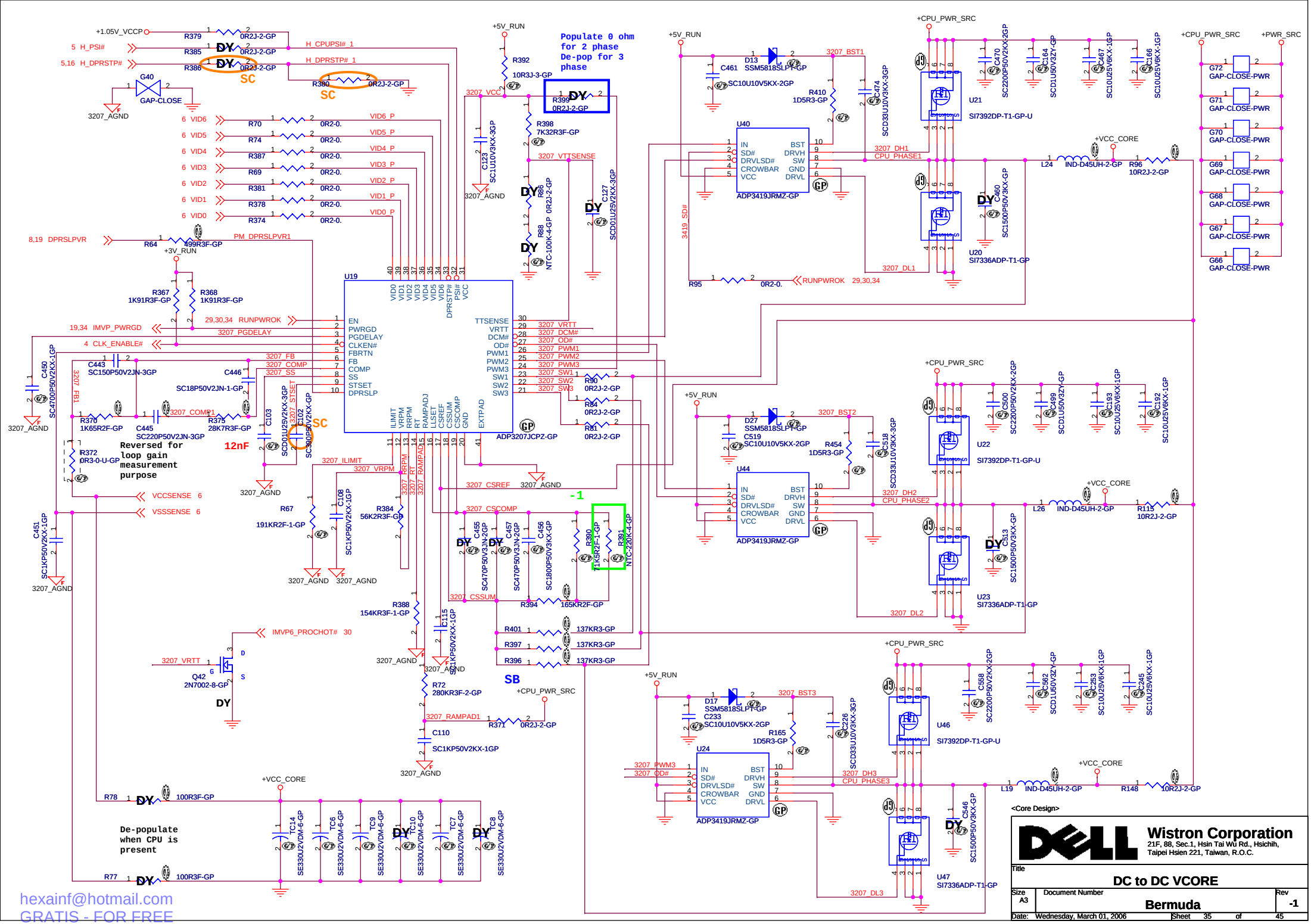

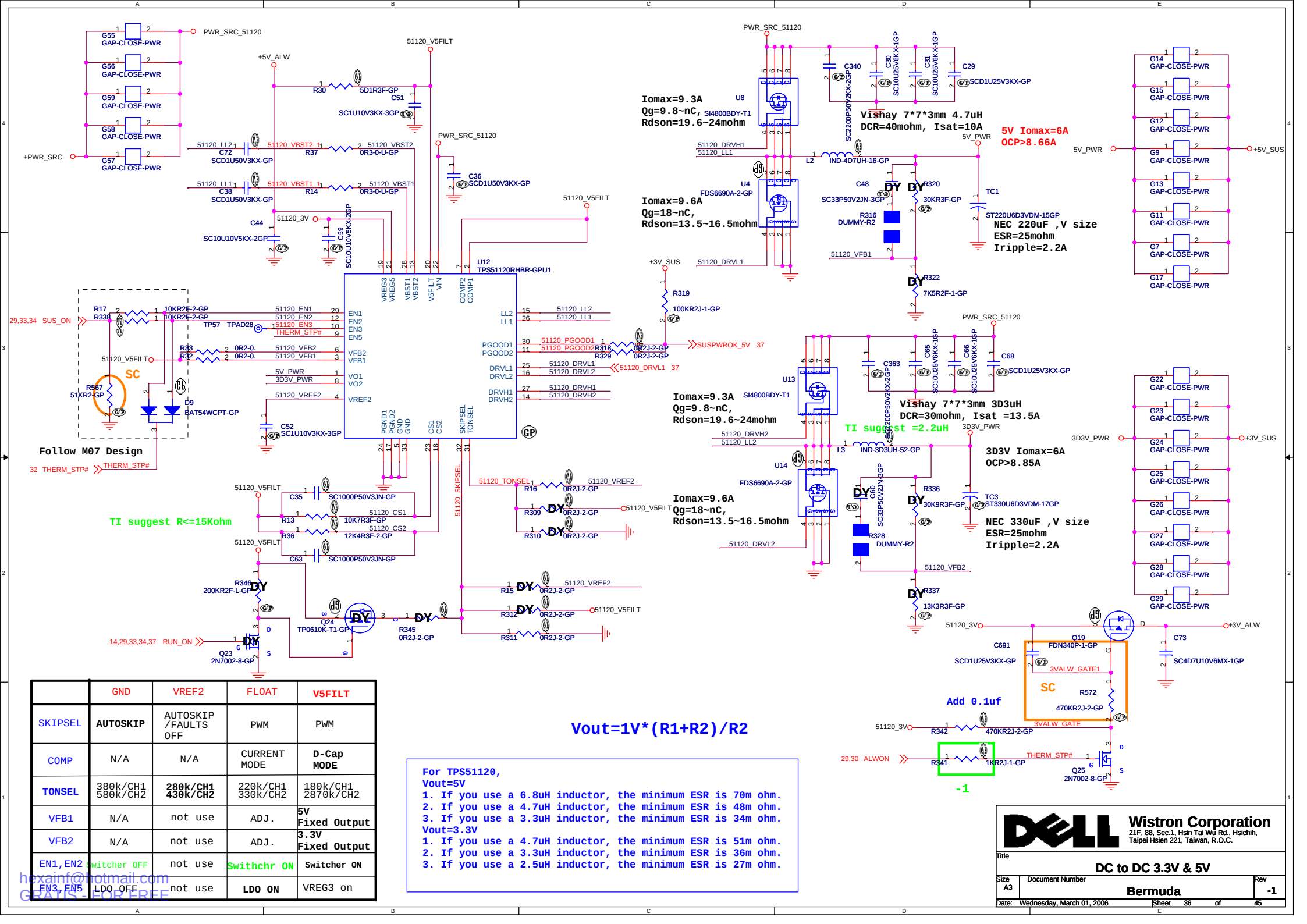

	GND	VREF2	FLOAT	V5FILT
SKIPSEL	AUTOSKIP	AUTOSKIP /FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	D-Cap MODE
TONSEL	380k/CH1 580k/CH2	280k/CH1 430k/CH2	220k/CH1 330k/CH2	180k/CH1 2870k/CH2
VFB1	N/A	not use	ADJ.	5V Fixed Output
VFB2	N/A	not use	ADJ.	3.3V Fixed Output
EN1,EN2	Switcher OFF	not use	Swithchr ON	Switcher ON
EN3, EN5	LDO OFF	not use	LDO ON	VREG3 on

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Title: DC to DC 3.3V & 5V

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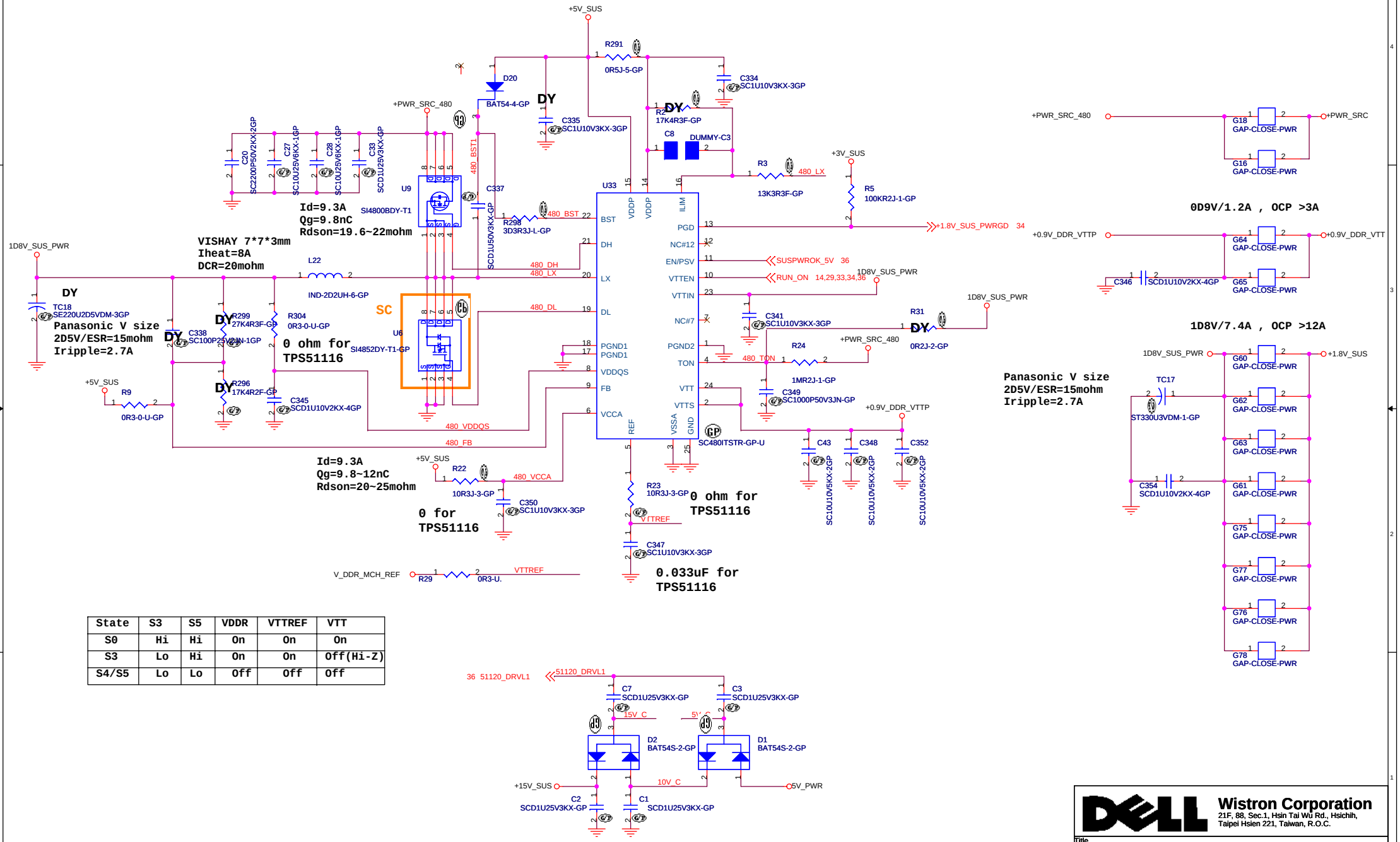
SC480 for 1D8V and 0D9V



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

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Title: DC to DC 1.8V & 0.9V & 15V

Size: A3 | Document Number: Bermuda | Rev: -1

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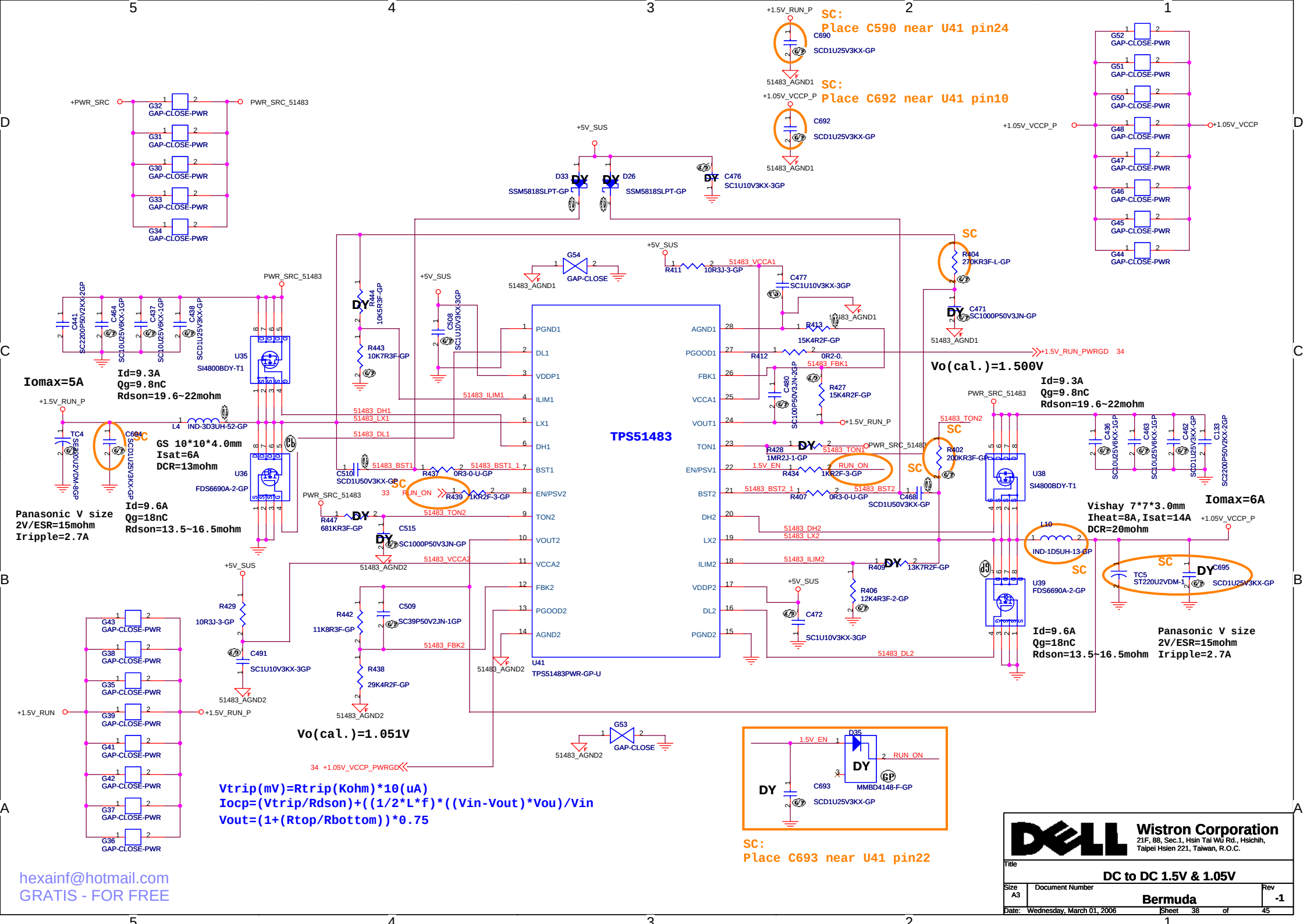
TPS51483
U41
TPS51483PWR-GP-U
PGND1
DL1
VDDP1
ILIM1
LX1
DH1
BST1
EN/PSV1
TON2
VOUT2
VCCA2
FBK2
PGOOD2
AGND2
AGND1
PGOOD1
FBK1
VCCA1
VOUT1
TON1
EN/PSV1
BST2
DH2
LX2
ILIM2
VDDP2
DL2
PGND2
SC:
Place C590 near U41 pin24
SC:
Place C692 near U41 pin10
SC:
Place C693 near U41 pin22
Iomax=5A
Id=9.3A
Qg=9.8nC
Rdson=19.6~22mohm
GS 10*10*4.0mm
Isat=6A
DCR=13mohm
Id=9.6A
Qg=18nC
Rdson=13.5~16.5mohm
Panasonic V size
2V/ESR=15mohm
Iripple=2.7A
Vo(cal.)=1.500V
Id=9.3A
Qg=9.8nC
Rdson=19.6~22mohm
Iomax=6A
Vishay 7*7*3.0mm
Iheat=8A,Isat=14A
DCR=20mohm
Id=9.6A
Qg=18nC
Rdson=13.5~16.5mohm
Panasonic V size
2V/ESR=15mohm
Iripple=2.7A
Vo(cal.)=1.051V
Vtrip(mV)=Rtrip(Kohm)*10(uA)
Iocp=(Vtrip/Rdson)+((1/2*L*f)*((Vin-Vout)*Vou)/Vin
Vout=(1+(Rtop/Rbottom))*0.75
+1.5V_RUN_P
+5V_SUS
+1.05V_VCCP_P
+1.05V_VCCP
+PWR_SRC
PWR_SRC_51483
+1.5V_RUN
+1.5V_RUN_PWRGD
34
34 +1.05V_VCCP_PWRGD
51483_AGND1
51483_AGND2
51483_VCCA1
51483_VCCA2
51483_FBK1
51483_FBK2
51483_ILIM1
51483_ILIM2
51483_DH1
51483_DH2
51483_LX1
51483_LX2
51483_DL1
51483_DL2
51483_BST1
51483_BST1_1
51483_BST2
51483_BST2_1
51483_TON1
51483_TON2
1.5V_EN
RUN_ON
33
U35
SI4800BDY-T1
U36
FDS6690A-2-GP
U38
SI4800BDY-T1
U39
FDS6690A-2-GP
L4
IND-3D3UH-52-GP
L10
IND-1D5UH-13-GP
D33
SSM5818SLPT-GP
D26
SSM5818SLPT-GP
D35
MMBD4148-F-GP
TC4
SSCD-VDN-B6GP
TC5
ST220U2VDM-1
R404
270KR3F-L-GP
R402
200KR3F-GP
R411
10R3J-3-GP
R412
0R2-0.
R413
15K4R2F-GP
R427
15K4R2F-GP
R428
1MR2J-1-GP
R434
1KR2F-3-GP
R407
0R3-0-U-GP
R409
13K7R2F-GP
R406
12K4R2F-2-GP
R437
0R3-0-U-GP
R439
1KR2F-3-GP
R447
681KR3F-GP
R443
10K7R3F-GP
R444
10K5R3F-GP
R429
10R3J-3-GP
R442
11K8R3F-GP
R438
29K4R2F-GP
C691
SC1U10V3KX-3GP
C509
SC39P50V2JN-1GP
C510
SCD1U50V3KX-GP
C515
SC1000P50V3JN-GP
C471
SC1000P50V3JN-GP
C480
SC100P50V3JN-2GP
C468
SCD1U50V3KX-GP
C472
SC1U10V3KX-3GP
C693
SCD1U25V3KX-GP
C695
SCD1U25V3KX-GP
C690
SCD1U25V3KX-GP
C692
SCD1U25V3KX-GP
C476
SC1U10V3KX-3GP
C477
SC1U10V3KX-3GP
C441
SC2200P50V2KX-2GP
C464
SC10U25V6KX-1GP
C437
SC10U25V6KX-1GP
C438
SCD1U25V3KX-GP
C508
SC1U10V3KX-3GP
C436
SC10U25V6KX-1GP
C463
SC10U25V6KX-1GP
C462
SCD1U25V3KX-GP
C133
SC2200P50V2KX-2GP
G32
G31
G30
G33
G34
G52
G51
G50
G48
G47
G46
G45
G44
G43
G38
G35
G39
G41
G42
G37
G36
G54
G53
GAP-CLOSE-PWR
GAP-CLOSE
DY
SC
hexainf@hotmail.com
GRATIS - FOR FREE
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Title
DC to DC 1.5V & 1.05V
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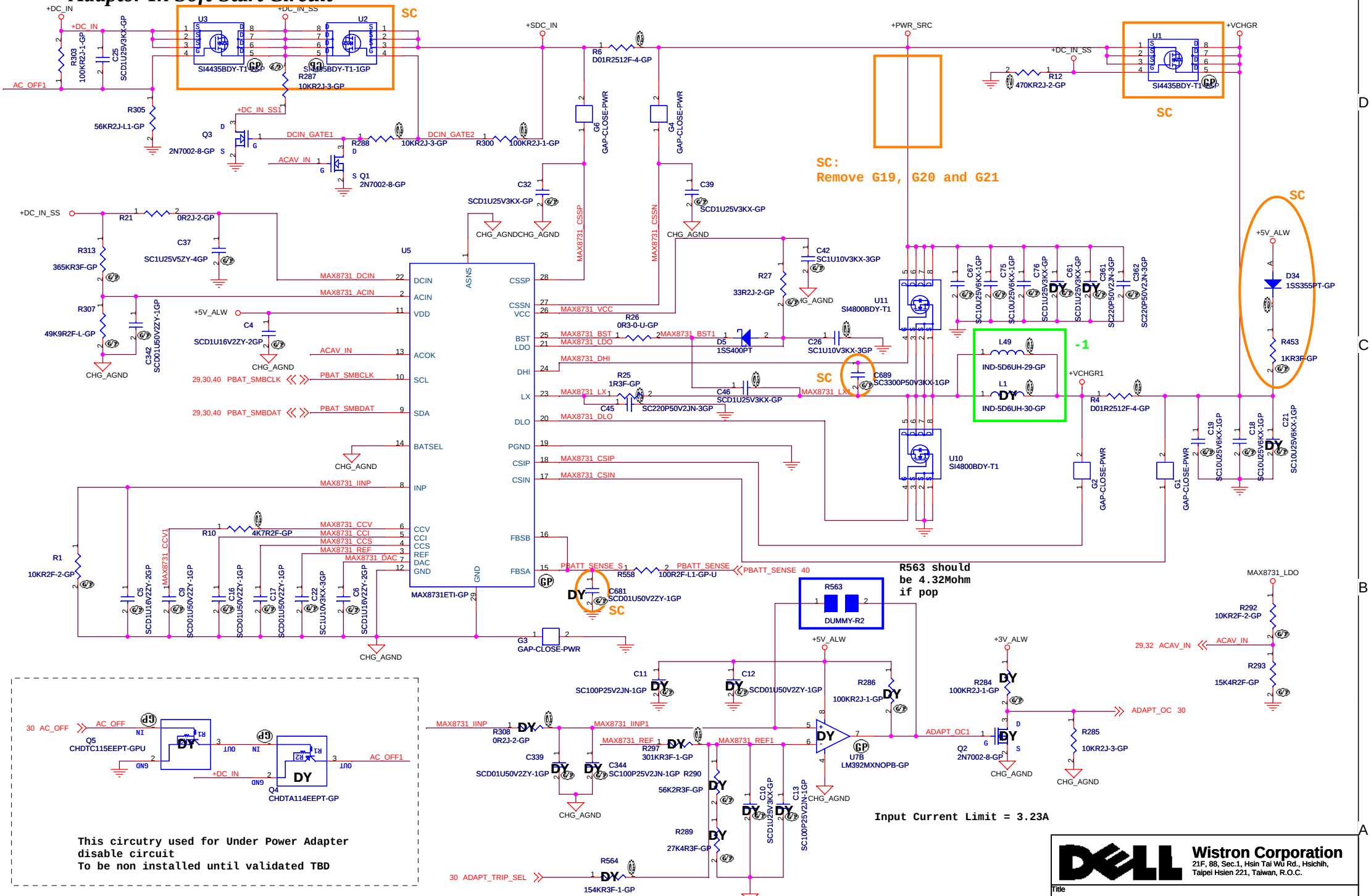
Adaptor In Soft-Start Circuit



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Title: CHARGER		
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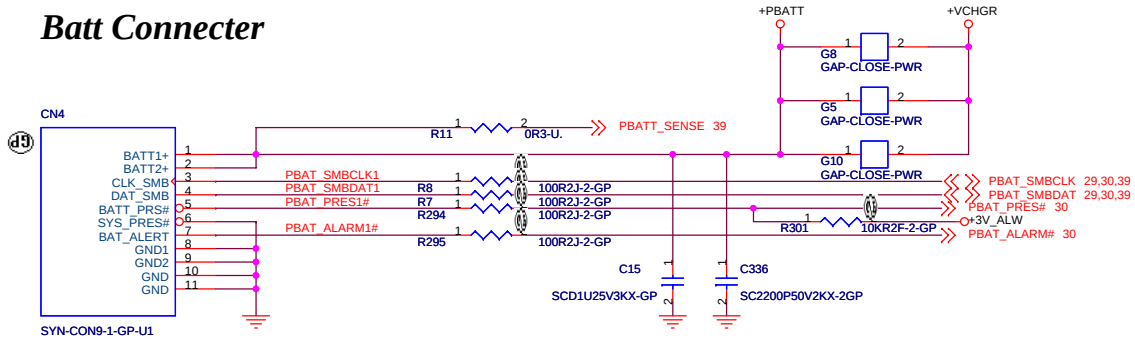
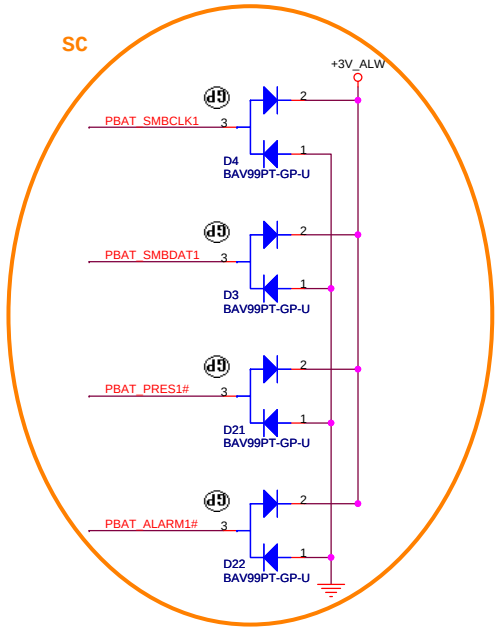
Batt Connecter





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Title: BAT Connector

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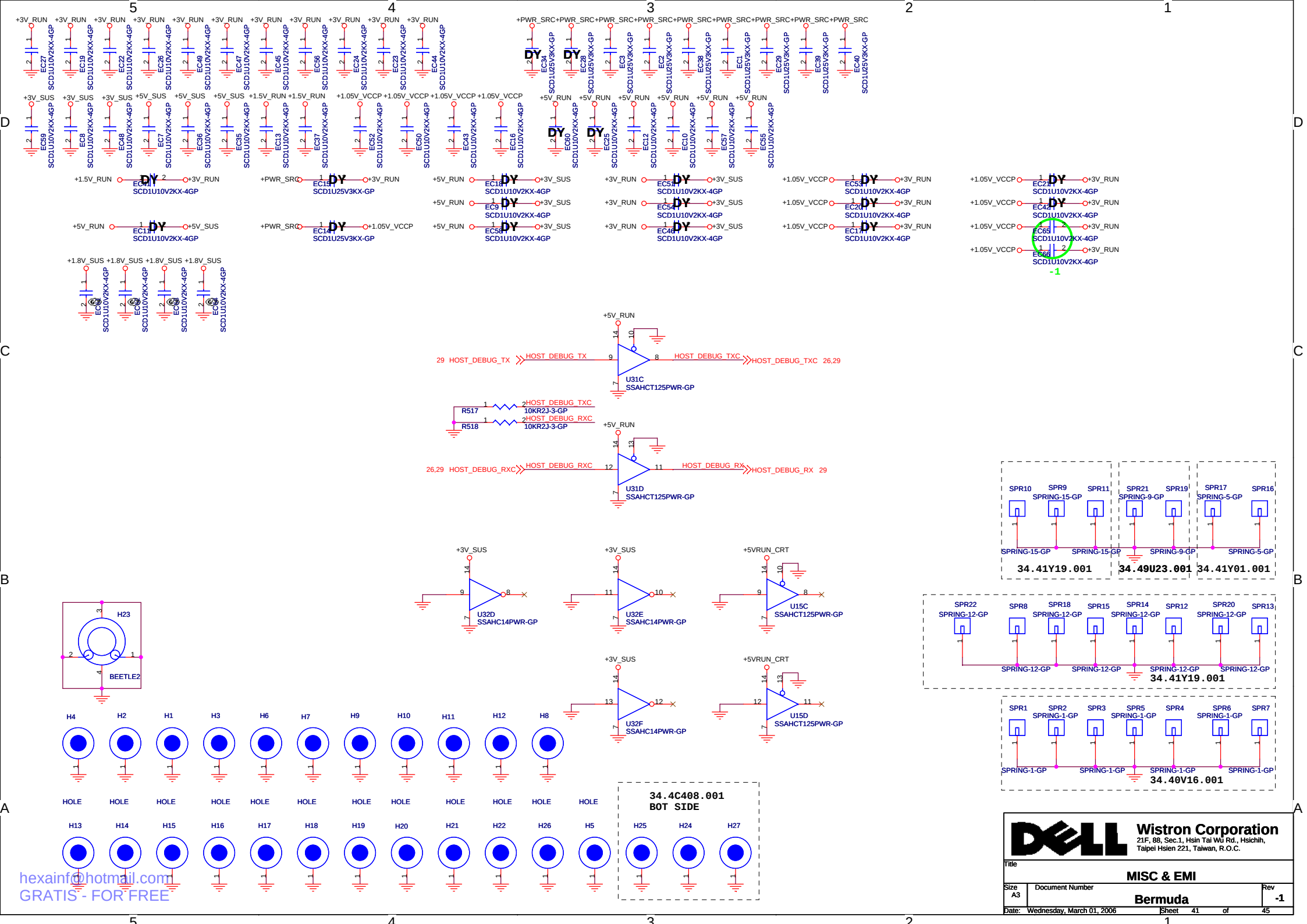

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Title: MISC & EMI

Size	Document Number	Rev
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CPU_Core
ADP3207+ADP3419

Input signal	Output Signal
EN	PWRGD
FBRTN	
FB	CLKEN#
DPRSLP	
PSI#	
DPRSTP#	
VID0~6	
Input Power	**Output Power**
VCC	

RUNPWROK
VSSSENSE
VCCSENSE
DPRSLPVR
H_PSI#
H_DPRSTP#
VID0~6
+5V_RUN

IMVP_PWRGD
CLK_ENABLE#
+VCC_CORE

5V/3D3V
TI TPS51120

Input signal	Output Signal
EN1	VREG2
EN2	VREG3
EN3	VREG5
EN5	PGOOD1
SKIPSEL	PGOOD2
TONSEL	
VO1	
VO2	
Input Power	**Output Power**
VIN	

SUS_ON / THERM_STP#
SUS_ON / THERM_STP#
SUS_ON / THERM_STP#
GND
51120_VREF2
5V_PWR
3D3V_PWR
PWR_SRC_51120

51120_VREF2
51120_3V
+5V_ALW
SUSPWROK_5V
SUSPWROK_5V
5V_PWR
3D3V_PWR

1D8V/0D9V
TPS51116

Input signal	Output Signal
EN/PSV (5V)	
VTTEN (5V)	PGD
TON (<5V)	
VDDP (5V)	
Input Power	**Output Power**
VTTIN	
VTTS	VTT
VDDQS	
VCCA	

SUSPWROK_5V
RUN_ON_D
1D8V_SUS_PWR
+5V_SUS
1D8V_SUS_PWR
+0.9V_DDR_VTTP
1D8V_SUS_PWR
+5V_SUS

+1.8V_SUS_PWRGD
1D8V_SUS_PWR
+0.9V_DDR_VTTP

1D5V/1D05V
TI TP51483

Input signal	Output Signal
EN/PSV2 (5V)	PGOOD2
TON2 (5V)	PGOOD1
EN/PSV1 (5V)	
TON1 (5V)	
Input Power	**Output Power**
VOUT2	
VCCA2	
VDDP2	
VOUT1	
VCCA1	
VDDP1	

RUN_ON_DC
51483_TON2
RUN_ON_DC
51483_TON1
+1.05V_VCCP_P
+5V_SUS
+5V_SUS
+1.5V_RUN_P
+5V_SUS
+5V_SUS

+1.05V_VCCP_PWRGD
+1.5V_RUN_PWRGD
+1.5V_RUN_P
+1.05V_VCCP_P

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Title: POWER DIAGRAM

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DATE	VERSON	ITEM	PAGE	Modify List	Issue Description	OWNER
2005/11/03	X00 to X01	1	37	U33 Pin10 change connect from RUN_ON_D to RUN_ON	Follow M07 design	EE
		2	26,29,41	HOST_DEBUG_TX and HOST_DEBUG_RX connect to U31 first then connect to connecter(DBG2)	TX,RX need add buffer for debug	EE,SW
		3	8	Del RN40 and add R551,R552(10k ohm) then Pop R440	Implement C4E feature on DPRSLPVR	EE
		4	14,29	Smbus which connect to LCD connecter change to SBAT_SMBDAT and SBAT_SMBCLK	This is follow M07 design	EE
		5	15	C112,C113,C121,C129,C139,C155 change from 82p to 0.5p	For TV EA measurement pass	EE
		6	16	R228,R229 change from 33 ohm to 39 ohm	For Azalia EA measurement pass	EE
		7	16	Add R568(0 ohm) for X2(Crystal for ICH7M)	This is follow COE's suggestion	EE
		8	16	C297,C314 change from 4.7P to 3.3P for X2(Crystal for ICH7M)	CRYTAL Vendor suggestion	EE
		9	18	Change R472 to 0805 size and add L48(10UH)	This is follow COE's suggestion	EE
		10	19	Add R560,R561(100k)	Follow M07 design	EE
		11	21,22	Change C250 to 10uF and add C686(0.1u),C687(1u)	This is follow COE's suggestion	EE
		12	23	X1 change from 20p to 18p type crystal	By Broadcom's suggestion,Lan crystal need use 18p type	EE
		13	24	C642,C644 change from 18P to 15P for X5(Crystal for R5C832)	CRYTAL Vendor suggestion	EE
		14	25	Swap connection for CARD1 pin22 and pin23	Card pin22 and pin23 need swap for MS card function work normally	EE
		15	25	Change L29 and L37 to 110 ohm impedance type for 1394	X00 already use 110 ohm type only forget to modify schematic	EE
		16	26	Add D32 and depop R266 to prevent leakage from WAN_RADIO_DIS#	Follow M07 design	EE
		17	27	Change R353 connection from U35 pin1 to U35 pin3	COE's suggestion to prevent the wireless LED light strength not enough	EE
		18	27	R42,R43 change to 220ohm;R40 change to 470ohm	LED light strength need change to avoid light leak	EE
		19	27	Q33 and Q34 Pin1 from +5V_ALW to +3V_ALW	Change to +3VALW for battery LED work normally	EE
		20	29	RN4 and RN6 change from 8.2K to 1K and add R323,R324,R333,R334,C682,C683,C684,C686	For SMBUS EA measurement pass	EE
		21	29	C538,C544 change from 20P to 27P for X4(Crystal for MEC5004)	CRYTAL Vendor suggestion	EE
		22	29	Reversed R553,R554,R555,R556,R557,Q72,Q73,D31,C680,R560	KBC Work Around Circuit for MEC5004 Rev "C"	EE
		23	29	Add R559(0 ohm) to GND	To Fix Rev "C" KBC bug	EE
		24	30	Pop R244 and depop R225	Change BOARD ID to X01	EE
		25	32	Add R562(0 ohm) in EMC4000 pin 22	Easily debug for THERM_STP# signal	EE
		26	33	R321,R330 from 20K ohm to 4K7 ohm R331,R332 from 10K ohm to 200K ohm	To prevent leakage from +3V_SUS to +3V_RUN when in suspend	EE
		27	33	Pop R28,R335,Q6,Q13	For 1.8V_SUS discharge more quickly	EE
		28	33	Change R19 to 200k and C84 to 470pF	For IMVP_PWRGD glitch issue,need make +5V_RUN more faster than +3V_RUN when boot up	EE
		29	33	REMOVE Q8,Q15,R323,R324,R333,R334	Follow M07 design	EE
		30	35	Change R394 to 165K and R396,R397,R401 to 137K then depop C457	This is changed for Vcore load line test fail	Power
		31	35	Change R410,R454 and R165 to 1.5 ohm	This is changed for Vcore's ring over spec	Power
		32	36	Add R565 and R566 for SUS_ON unstable when plug adapter	This is recommended by TDC Lawrence	Power
		33	36	Change TC3 to another source	This is recommended by power team	Power
		34	37	Depop TC18 and change TC17 to 330uF;change D20 to BAT54;change R3 to 13K3 ohm;change R298 to 3D3 ohm	This is recommended by power team	Power
		35	37	New add 4 gaps G75,G76,G77,G78 for 1.8V	This is requested by EMI	EMI
		36	38	Change R427 to 15K4 ohm	This is recommended by power team	Power
		37	39	Add R558,C682 in U5 pin15 pin16 for PBATT_SENSE	To prevent Charger damage when plug battery	Power
		38	39	ADD ADAPT_TRIP_SEL circuit	Follow M07 schematic	Power
		39	41	Add EC61,EC62,EC63.EC64,SPR22 and depop EC41,EC11,EC15,EC14,EC9,EC18,EC58,EC46 ,EC51,EC54,EC17,EC20,EC53,EC21,EC42	This is for EMI	EMI

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Title: HISTORY from X00 to X01

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DATE	VERSON	ITEM	PAGE	Modify List	Issue Description	OWNER
2006/01/03	X01 to X02	1	6	Change CPU 22uF to 10uF for power noise,total 32 pieces	Power team suggestion	Power
		2	17,29	Add R573(47 ohm) and R574 (0 ohm) during ICH7M and KBC for SPI_CS# to verify signal quality	Suggestion by COE	EE
		3	19	Change R560 and R561 to no pop	Suggestion by COE	EE
		4	20	Reversed Pad for R577(0 ohm),because Seagate SATA HDD driver will make S3 resume issue on spin-up mode	Suggestion by COE	EE
		5	22	Pop C525 for VREFOUT	Suggestion by COE	EE
		6	25	Change U57 to G5240 for OCP Issue	Suggestion by COE	EE
		7	29	Pop R200 and de-pop R201	Enable internal bootblock flash function	EE
		8	30	Pop R243 and R225, de-pop R244 and R224	Change Board ID to X02	EE
		9	30	New add R575 and R576 for HDDC_EN# and MODC_EN#	Suggestion by COE	EE
		10	34	Change Q70 from 3904 to 2N7002	Suggestion by COE	EE
		11	35	De-pop R386 and pop R380	Power team suggestion	Power
		12	35	Change C102 from 680PF to 390PF	Power team suggestion	Power
		13	36	Add R567(51k ohm) from SUS_ON to GND to avoid SUS_ON glitch issue	Power team suggestion	Power
		14	36	Add C691 and R572 for +3V_ALW soft-start	Power team suggestion	Power
		15	37	Change U6 to SI4852DY	Power team suggestion	Power
		16	38	Change the enable pin of TPS51483 connection from RUN_ON_D to RUN_ON	Power team suggestion	Power
		17	38	Change R402 to 200k and R404 to 270K and L10 to 1D5UH	Power team suggestion	Power
		18	38	Add C690,C692,C694 and reversed C695 for 1.5V noise issue	Power team suggestion	Power
		19	38	Reversed C693 and D35 for 1.5V enable signal	Power team suggestion	Power
		20	39	Change U1,U2 and U3 to SI4435BDY	Power team suggestion: AOS is not in Dell QVL	Power
		21	39	Remove G19, G20 and G21	Power team suggestion	Power
		22	39	New add C689 (3300 PF)	Suggestion by MAXIM	Power
		23	39	New add D34 and R453 to solve MAX8731 can't charge battery when battery voltage lower than 2.5V	Suggestion by MAXIM	Power
		24	39	De-pop C681	Power team suggestion	Power
		25	40	Change D3,D4,D21,D22 connection way,before is after resistors but now change to connect battery connecter first then to resistors	This is ESD issue,the ESD diode need to be placed near to battery connecter	EMI
		26	29	Change X4 to XTAL 32.768K 6PF10PPM	This is because Barbados lesson learn,old crystal sometimes will make system can not boot.	EE

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		1	24	De-pop R541 and pop R547 and C669 for GBSRST#	Suggestion by COE	EE
		2	29	Change X4 to XTAL 32.768K 12.5P10PPM DMX26S and sloe change C544 to 18P and C538 to 22P	Suggestion by KDS and Epson	EE
		3	30	Depop R225 and pop R244 for Board ID change	Change Board ID to X03	EE
		4	31	Add D36 and reversed R578 for leakage issue	To prevent leakage issue	EE
		5	35	Change R391 vendor from MURATA to MITSUBISHI	Suggestion by Power Team	Power
		6	36	Change R341 from 10K ohm to 1K ohm	Suggestion by Power Team	Power
		7	39	Depop L1 and pop L49 for DFX issue	Suggestion by Power Team	Power
		8	41	Add EC65 and EC66 for EMI's request	EMI's request	EMI
		9	27	For BREATH LED==>R40 change to 150 ohm For HDD LED==>R41 change to 51 ohm For battery LED==>R42 and R43 change to 51 ohm	Change brightness of LED	EE
2006/02/22	X02 to A00					

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