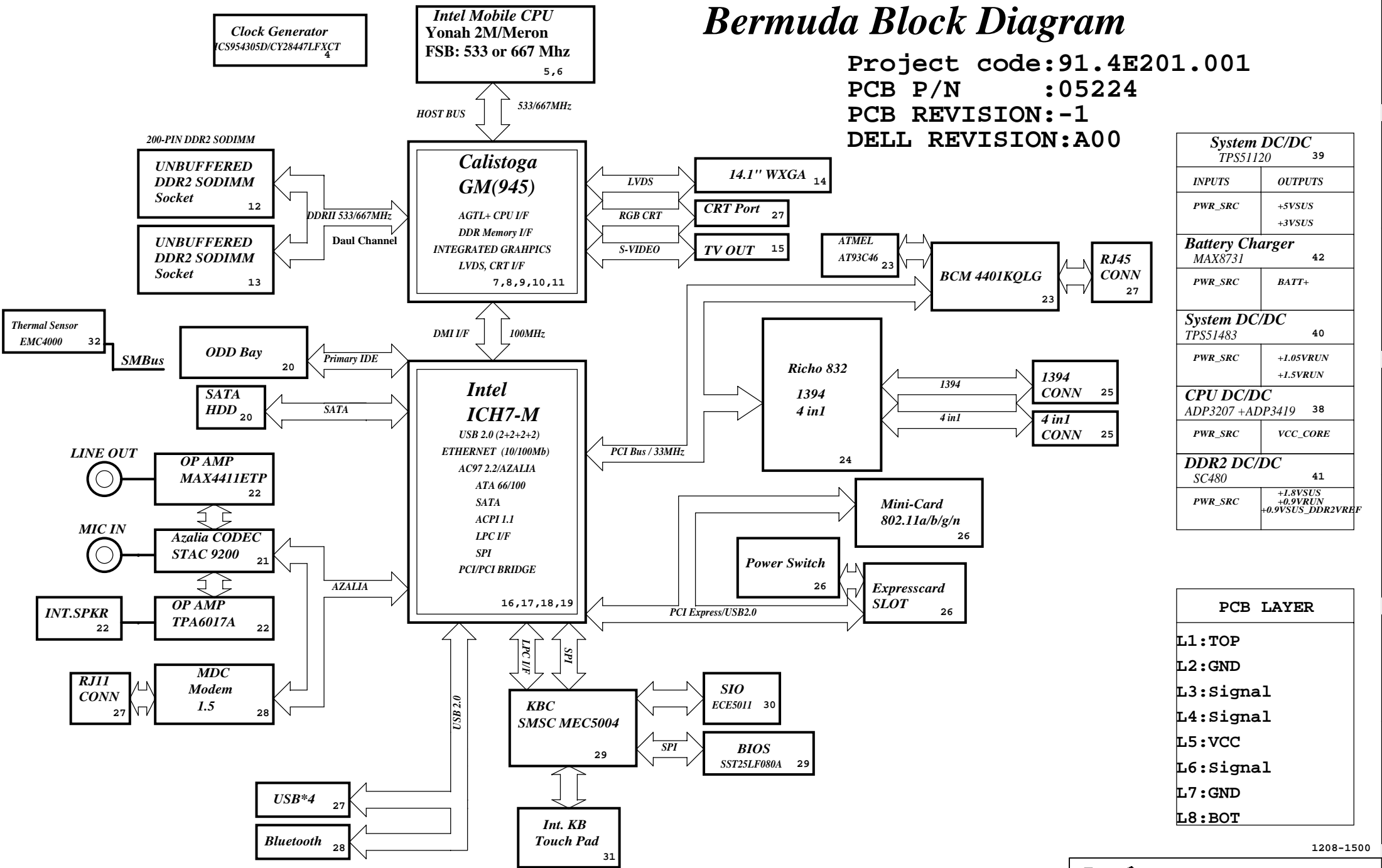


Bermuda Block Diagram

Project code: 91.4E201.001
 PCB P/N : 05224
 PCB REVISION: -1
 DELL REVISION: A00



System DC/DC TPS51120 39	
INPUTS	OUTPUTS
PWR_SRC	+5VSUS +3VSUS
Battery Charger MAX8731 42	
PWR_SRC	BATT+
System DC/DC TPS51483 40	
PWR_SRC	+1.05VRUN +1.5VRUN
CPU DC/DC ADP3207 +ADP3419 38	
PWR_SRC	VCC_CORE
DDR2 DC/DC SC480 41	
PWR_SRC	+1.8VSUS +0.9VRUN +0.9VSUS_DDR2VREF

PCB LAYER	
L1:	TOP
L2:	GND
L3:	Signal
L4:	Signal
L5:	VCC
L6:	Signal
L7:	GND
L8:	BOT

Wistron/Dell confidential

hexainf@hotmail.com
 GRATIS - FOR FREE

1208-1500

Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title System Block Diagram		
Size A3	Document Number Bermuda	Rev -1
Date: Wednesday, March 01, 2006	Sheet 1 of 45	

ICH7M Functional Strap Definitions

Signal	Usage/When Sampled	Comment
ACZ_SDOUT	XOR Chain Entrance/ PCIE Port Config bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC(Config Registers: offset 224h)
ACZ_SYNC	PCIE bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
EE_CS	Reserved	This signal should not be pull high.
EE_DOUT	Reserved	This signal should not be pull low.
GNT2#	Reserved	This signal should not be pull low.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT5#/ GPIO17#, GNT4#/ GPIO48	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT5# is MSB, 01-SPI, 10-PCI, 11-LPC.
DPRSLPVR	Reserved	This signal should not be pull high.
GPIO25	Reserved. Rising Edge of RSMRST#.	This signal should not be pull low.
INTVRMEN	Integrated VccSus1_05 VRM Enable/Disable. Always sampled.	Enables integrated VccSus1_05 VRM when sampled high
LINKALERT#	Reserved	Requires an external pull-up resistor.
REQ[4:1]#	XOR Chain Selection. Rising Edge of PWROK.	TBD, Chapter 8.
SATALED#	Reserved	This signal should not be pull low.
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH7 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.

Calistoga Strapping Signals and Configuration

* is Default setting

CFG Strap	Low	High
CFG 5	DMI X 2	DMI X 4 *
CFG 6	Moby Dick	Calistoga *
CFG 7	DT/Transportable CPU	Mobile CPU *
CFG 9	Reserved Lane	Normal Operation*
CFG 10	Reserved	Mobility *
CFG 11	Calistoga *	Reserved
CFG 16 FSB Dynamic ODT	Disabled	Enabled *
CFG 18 VCC Select	1.05V *	1.5V
CFG 19 DMI Lane Reserved	Normal Operation*	Reserved Lane
CFG 20 PCIE/SDVO Select	Only PCIE or SDVO is operation *	PCIE and SDVO are operation simu
SDVO_CTRLDATA	No SDVO Device present *	SDVO Device present

	CFG[13:12]
LL	Reserved
LH	XOR Mode Enabled
HL	All Z Mode Enabled
HH	Normal Operation*

ICH7M Integrated Pull-up and Pull-down Resistors

ICH7-M EDS 17837 1.5V1

EE_DIN, EE_DOUT, GNT[3:0], GPIO[25], GNT[4]#/GPIO48, GNT[5]#/GPIO17, PME#, LAD[3:0]#/FWH[3:0]#, LAN_RXD[2:0] LDRQ[0], LDRQ[1]/GPIO[41], PWRBTN#, TP[3]	ICH7 internal 20K pull-ups
DD[7], DDREQ	ICH7 internal 11.5K pull-downs
ACZ_BIT_CLK, ACZ_RST#, ACZ_SDIN[2:0], ACZ_SDOUT, ACZ_SYNC, DPRSLPVR/GPIO16, EE_CS, SPI_ARB, SPI_CLK, SPKR,	ICH7 internal 20K pull-downs
USB[7:0][P,N]	ICH7 internal 15K pull-downs
SATALED#	ICH7 internal 15K pull-up
LAN_CLK	ICH7 internal 100K pull-down

954305D 27Mhz/LCDCLK Spread and Frequency Selection Table

page 3

SS3 Byte9 bit 7	SS2 bit6	SS1 bit5	SS0 bit4	Spread Amount%
0	0	0	0	-0.50 Down
0	0	0	1	-1.00 Down
0	0	1	0	-1.50 Down
0	0	1	1	-2.00 Down
0	1	0	0	-0.75 Down
0	1	1	0	-1.75 Down
0	1	1	1	-2.25 Down
1	0	0	0	+0.25 Center
1	0	0	1	+0.5 Center
1	0	1	0	+0.75 Center
1	0	1	1	+1.0 Center
1	1	0	0	+0.25 Center
1	1	0	1	+0.5 Center
1	1	1	0	+0.75 Center
1	1	1	1	+1.0 Center

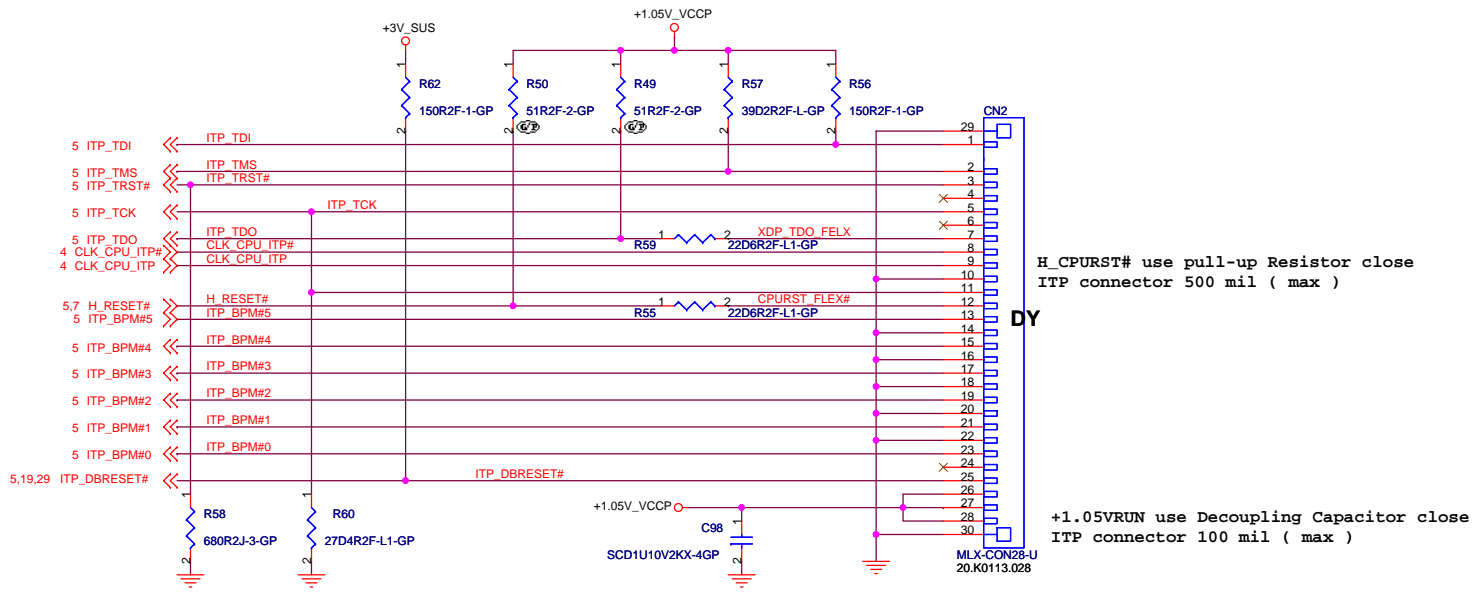
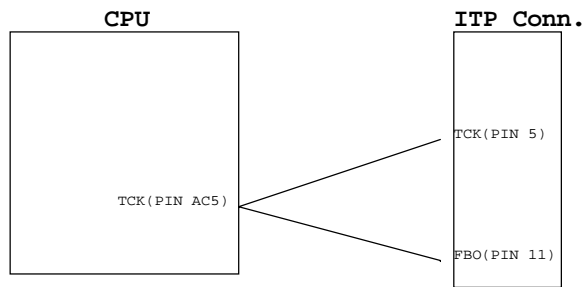
PCI Routing

page 16

	IDSEL	IRQ	REQ/GNT
R5C832	AD17		
LAN	AD16		

ICH7M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm
--	----------------------

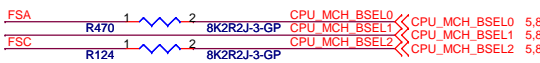
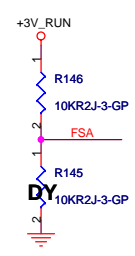
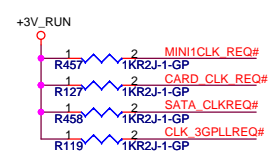
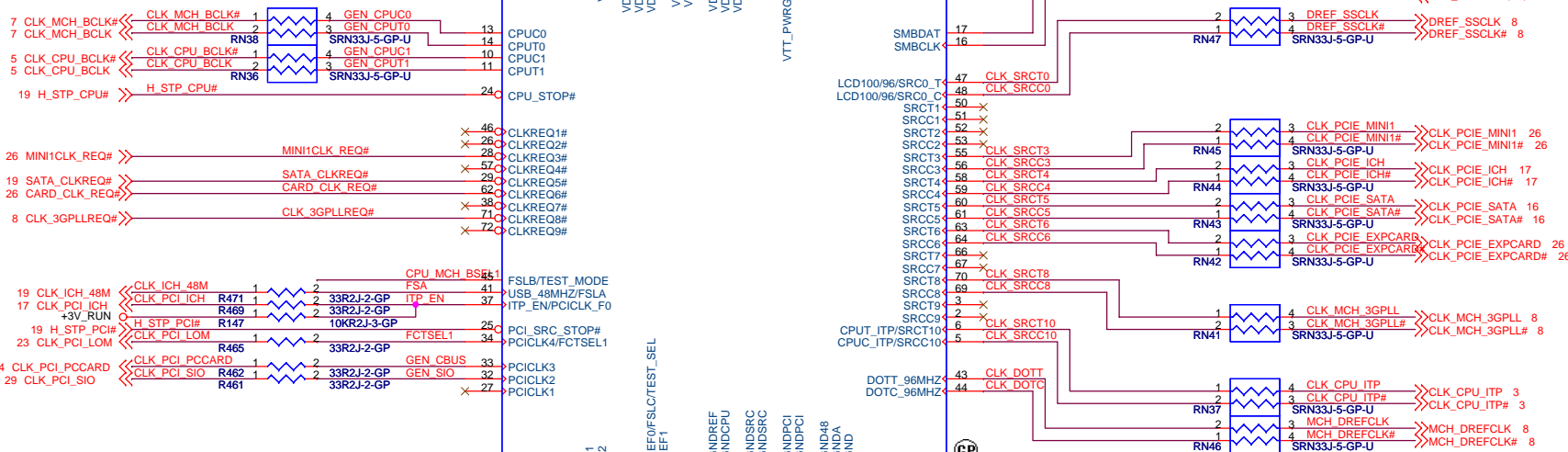
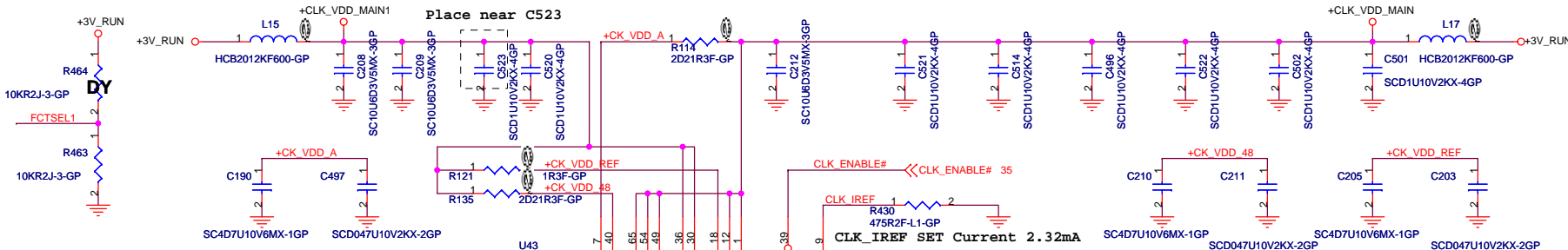


H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max)

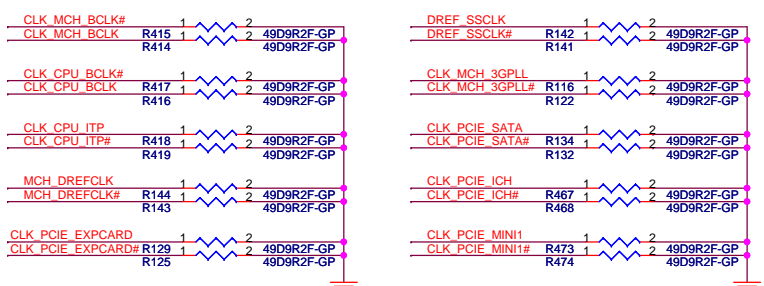
+1.05VRUN use Decoupling Capacitor close
ITP connector 100 mil (max)

ITP Debug Conn.

PIN34	FCTSEL1	0	1
PIN43	DOT96T	27M_NonSpread	
PIN44	DOT96C	27M_Spread	
PIN47	LCD100/96T	SRC0_T	
PIN48	LCD100/96C	SRC0_C	



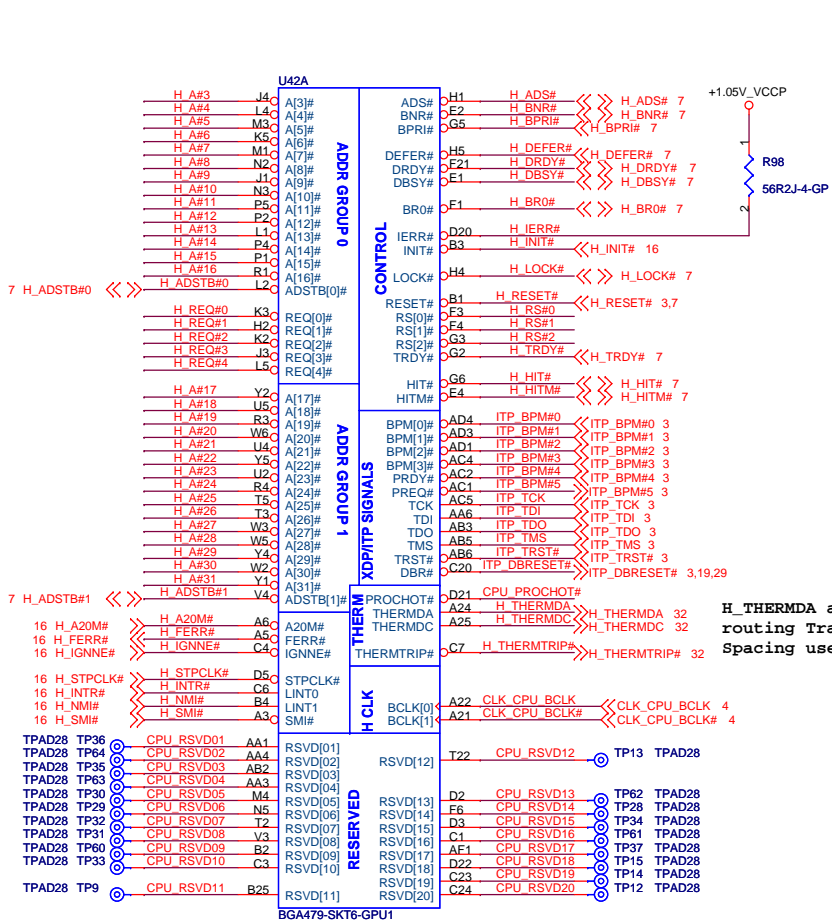
SEL2	SEL1	SEL0	CPU	FSB
0	0	0	266M	X
0	0	1	133M	533M
0	1	0	200M	X
0	1	1	166M	667M
1	0	0	333M	X
1	0	1	100M	X
1	1	0	400M	X
1	1	1	Reserved	X



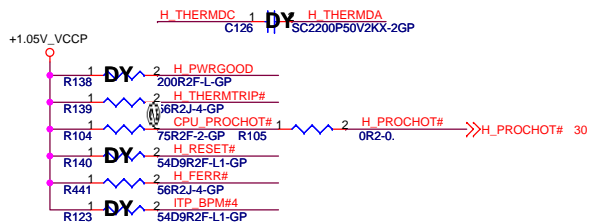
Solder Thermal Pad to GND add min 4 vias



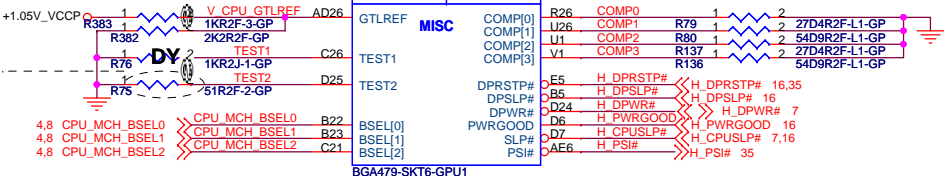
Title			
Clock Generator			
Size	Document Number	Rev	
A3	Bermuda	-1	
Date:	Wednesday, March 01, 2006	Sheet	4 of 45



C126 close to Pin A24 and Pin A25

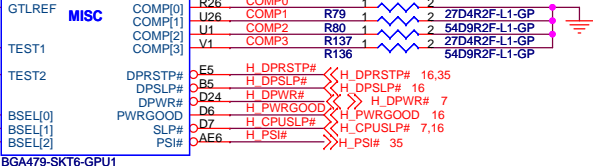
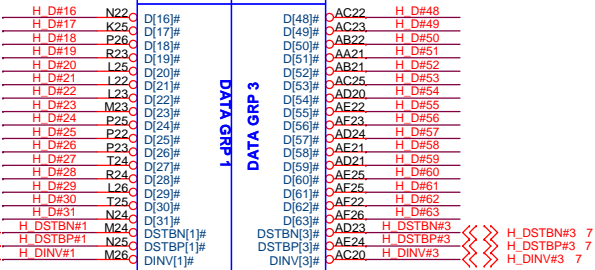
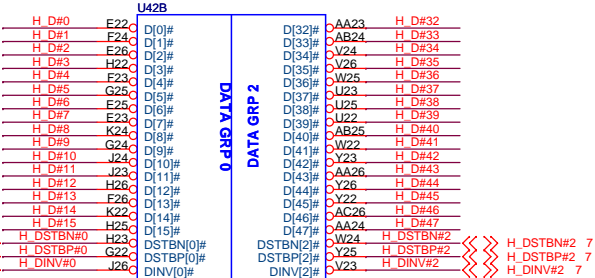
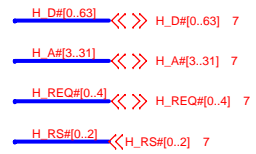


CPU_GTLREF0 close to Pin AD26 500 mil (max)



Yonah support
Change R76 to 51 ohm and Populate R75 for Yonah B0 Forward

CPU_SEL	H_SEL0	H_SEL1	H_SEL2
133	0	0	1
166	0	1	1



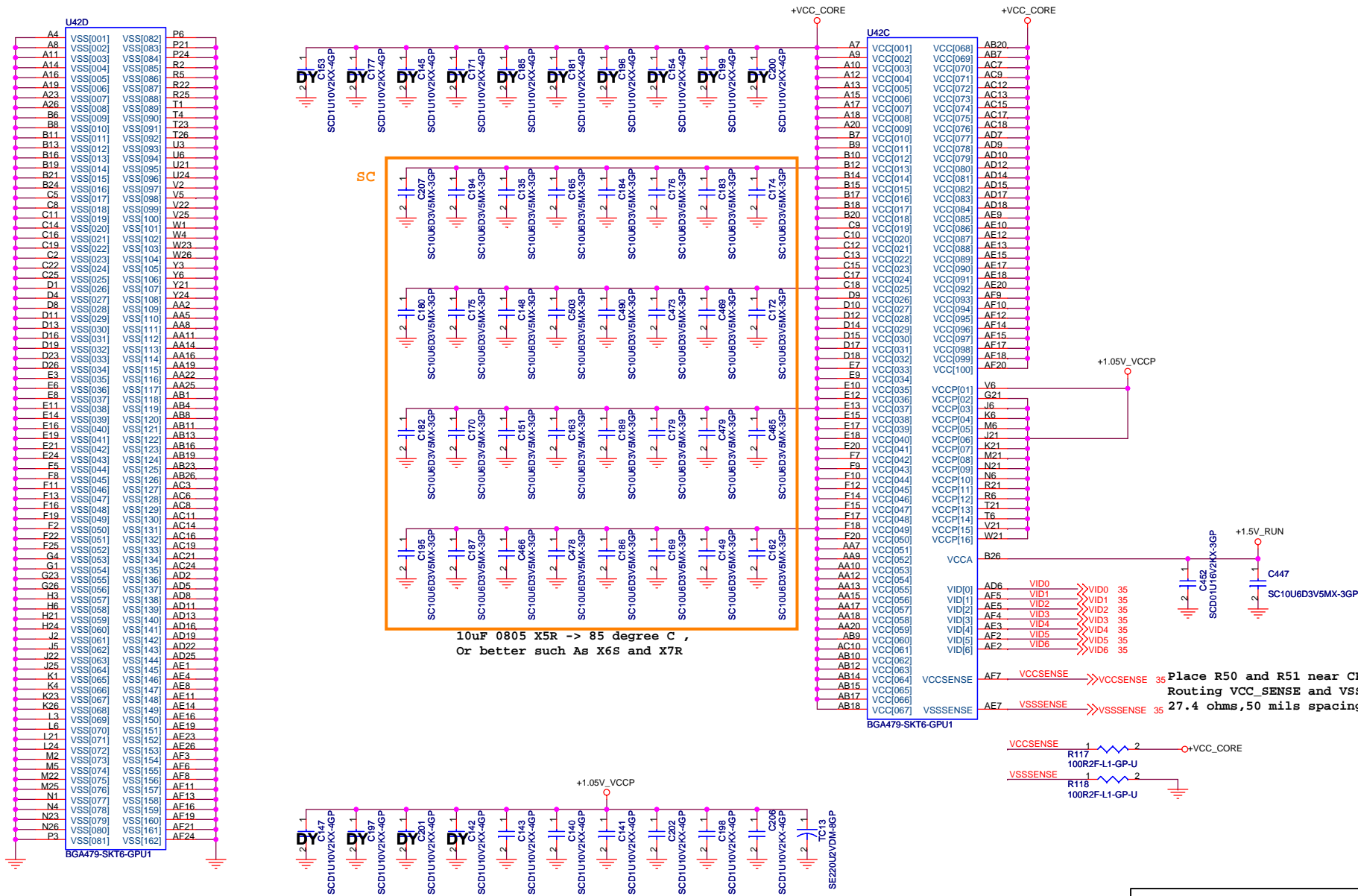
Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. Trace should be No Longer than 500 mils

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU - 01 - Yonah - FSB**

Size: A3 Document Number: **Bermuda** Rev: -1

Date: Wednesday, March 01, 2006 Sheet: 5 of 45



Please these inside socket cavity on L8 (North side Secondary)

Place R50 and R51 near CPU
Routing VCC_SENSE and VSS_SENSE at
27.4 ohms, 50 mils spacing, 1 inch.

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU - 02 - Yonah - POWER

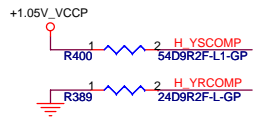
Size A3 Document Number: Bermuda Rev -1

Date: Wednesday, March 01, 2006 Sheet 6 of 45

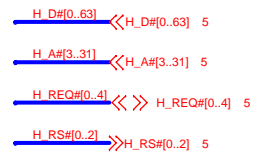
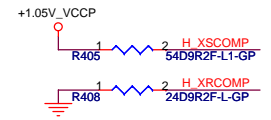
U371		VSS		AK34	
AC41	VSS_0	VSS_97	AK34		
AA41	VSS_1	VSS_98	AG34		
W41	VSS_2	VSS_99	AF34		
T41	VSS_3	VSS_100	AE34		
P41	VSS_4	VSS_101	AC34		
M41	VSS_5	VSS_102	C34		
F41	VSS_6	VSS_103	AW33		
AV40	VSS_7	VSS_104	AR33		
AP40	VSS_8	VSS_105	AE33		
AN40	VSS_9	VSS_106	AB33		
AK40	VSS_10	VSS_107	Y33		
AJ40	VSS_11	VSS_108	V33		
AH40	VSS_12	VSS_109	T33		
AG40	VSS_13	VSS_110	R33		
AF40	VSS_14	VSS_111	M33		
AE40	VSS_15	VSS_112	H33		
B40	VSS_16	VSS_113	G33		
AY39	VSS_17	VSS_114	F33		
AV39	VSS_18	VSS_115	E33		
AR39	VSS_19	VSS_116	D33		
AN39	VSS_20	VSS_117	B33		
AJ39	VSS_21	VSS_118	AH32		
AC39	VSS_22	VSS_119	AG32		
AB39	VSS_23	VSS_120	AF32		
AA39	VSS_24	VSS_121	AE32		
Y39	VSS_25	VSS_122	AC32		
W39	VSS_26	VSS_123	AB32		
V39	VSS_27	VSS_124	G32		
U39	VSS_28	VSS_125	B32		
T39	VSS_29	VSS_126	AY31		
R39	VSS_30	VSS_127	AV31		
P39	VSS_31	VSS_128	AN31		
N39	VSS_32	VSS_129	AJ31		
M39	VSS_33	VSS_130	AG31		
L39	VSS_34	VSS_131	AB31		
J39	VSS_35	VSS_132	Y31		
H39	VSS_36	VSS_133	W6		
G39	VSS_37	VSS_134	T5		
F39	VSS_38	VSS_135	E0		
D39	VSS_39	VSS_136	AT29		
AT38	VSS_40	VSS_137	AN29		
AM38	VSS_41	VSS_138	AB29		
AH38	VSS_42	VSS_139	W3		
AG38	VSS_43	VSS_140	T29		
AF38	VSS_44	VSS_141	N29		
AE38	VSS_45	VSS_142	K29		
C38	VSS_46	VSS_143	G29		
AK37	VSS_47	VSS_144	E29		
AH37	VSS_48	VSS_145	C29		
AB37	VSS_49	VSS_146	B29		
AA37	VSS_50	VSS_147	A29		
Y37	VSS_51	VSS_148	BA28		
W37	VSS_52	VSS_149	AW28		
V37	VSS_53	VSS_150	AJ28		
U37	VSS_54	VSS_151	AP28		
T37	VSS_55	VSS_152	AM28		
R37	VSS_56	VSS_153	AD28		
P37	VSS_57	VSS_154	AC28		
N37	VSS_58	VSS_155	W28		
M37	VSS_59	VSS_156	J28		
L37	VSS_60	VSS_157	E28		
J37	VSS_61	VSS_158	AM27		
H37	VSS_62	VSS_159	AK27		
G37	VSS_63	VSS_160	J27		
F37	VSS_64	VSS_161	G27		
D37	VSS_65	VSS_162	F27		
AY36	VSS_66	VSS_163	E27		
AW36	VSS_67	VSS_164	C27		
AN36	VSS_68	VSS_165	H25		
AH36	VSS_69	VSS_166	E25		
AG36	VSS_70	VSS_167	M26		
AF36	VSS_71	VSS_168	K26		
AE36	VSS_72	VSS_169	F26		
AC36	VSS_73	VSS_170	E26		
C36	VSS_74	VSS_171	AK25		
B36	VSS_75	VSS_172	P25		
BA35	VSS_76	VSS_173	K25		
AV35	VSS_77	VSS_174	H25		
AR35	VSS_78	VSS_175	E25		
AH35	VSS_79	VSS_176	D25		
AB35	VSS_80	VSS_177	A25		
AA35	VSS_81	VSS_178	BA24		
Y35	VSS_82	VSS_179	AJ24		
W35	VSS_83	VSS_180	AL24		
V35	VSS_84	VSS_181	AW23		
U35	VSS_85				
T35	VSS_86				
R35	VSS_87				
N35	VSS_88				
M35	VSS_89				
L35	VSS_90				
J35	VSS_91				
H35	VSS_92				
G35	VSS_93				
F35	VSS_94				
D35	VSS_95				
AN34	VSS_96				

U37A		HOSI	
H_D#0	F1	H_A#_3	H9
H_D#1	J1	H_A#_4	C9
H_D#2	H1	H_A#_5	E11
H_D#3	J6	H_A#_6	G11
H_D#4	H3	H_A#_7	E12
H_D#5	K2	H_A#_8	G12
H_D#6	G1	H_A#_9	F9
H_D#7	G2	H_A#_10	H11
H_D#8	K9	H_A#_11	G12
H_D#9	K1	H_A#_12	H12
H_D#10	K7	H_A#_13	D9
H_D#11	J8	H_A#_14	J14
H_D#12	H4	H_A#_15	H13
H_D#13	J3	H_A#_16	J15
H_D#14	K11	H_A#_17	F14
H_D#15	G4	H_A#_18	D12
H_D#16	T10	H_A#_19	A11
H_D#17	W11	H_A#_20	C11
H_D#18	T3	H_A#_21	A12
H_D#19	U7	H_A#_22	A13
H_D#20	J9	H_A#_23	E13
H_D#21	U11	H_A#_24	G13
H_D#22	T11	H_A#_25	F12
H_D#23	W9	H_A#_26	B12
H_D#24	T1	H_A#_27	B14
H_D#25	T8	H_A#_28	C12
H_D#26	T4	H_A#_29	A14
H_D#27	W7	H_A#_30	C14
H_D#28	U5	H_A#_31	D14
H_D#29	T9		
H_D#30	W6		
H_D#31	T5		
H_D#32	AB7		
H_D#33	AA9		
H_D#34	WA		
H_D#35	W3		
H_D#36	Y3		
H_D#37	Y7		
H_D#38	W5		
H_D#39	Y10		
H_D#40	AB8		
H_D#41	W2		
H_D#42	AA4		
H_D#43	AA7		
H_D#44	AA2		
H_D#45	AA6		
H_D#46	AA10		
H_D#47	Y8		
H_D#48	AA1		
H_D#49	AB4		
H_D#50	AC9		
H_D#51	AB11		
H_D#52	AC11		
H_D#53	AB3		
H_D#54	AD1		
H_D#55	AD7		
H_D#56	AD9		
H_D#57	AC1		
H_D#58	AD7		
H_D#59	AC6		
H_D#60	AB5		
H_D#61	AD10		
H_D#62	AD4		
H_D#63	AC8		
H_XRCOMP	E1	H_XRCOMP	E1
H_XSCOMP	E2	H_XSCOMP	E2
H_SWNG0	E4	H_SWNG0	E4
H_YRCOMP	Y1	H_YRCOMP	Y1
H_YSCOMP	U1	H_YSCOMP	U1
H_SWNG1	W1	H_SWNG1	W1
CLK_MCH_BCLK	AG2	CLK_MCH_BCLK	AG2
CLK_MCH_BCLK#	AG1	CLK_MCH_BCLK#	AG1
H_CLKIN		H_CLKIN	
H_CLKIN#		H_CLKIN#	

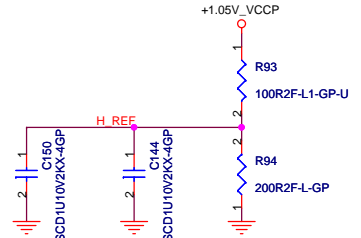
H_XRCOMP and H_YRCOMP Routing Trace width and Spacing use 10 / 20 mil



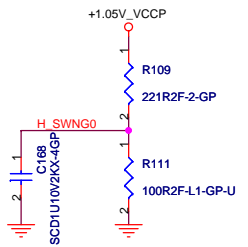
H_XSCOMP and H_YSCOMP Resistors and Capacitors close Caliistoga 500 mil (MAX)



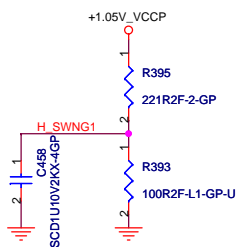
H_REF Decoupling Capacitors close Caliistoga 100 mil



H_XSWING and H_YSWING routing Trace width and Spacing use 10 / 20 mil



H_XSWING and H_YSWING Resistors and Capacitors close Caliistoga 500 mil (MAX)

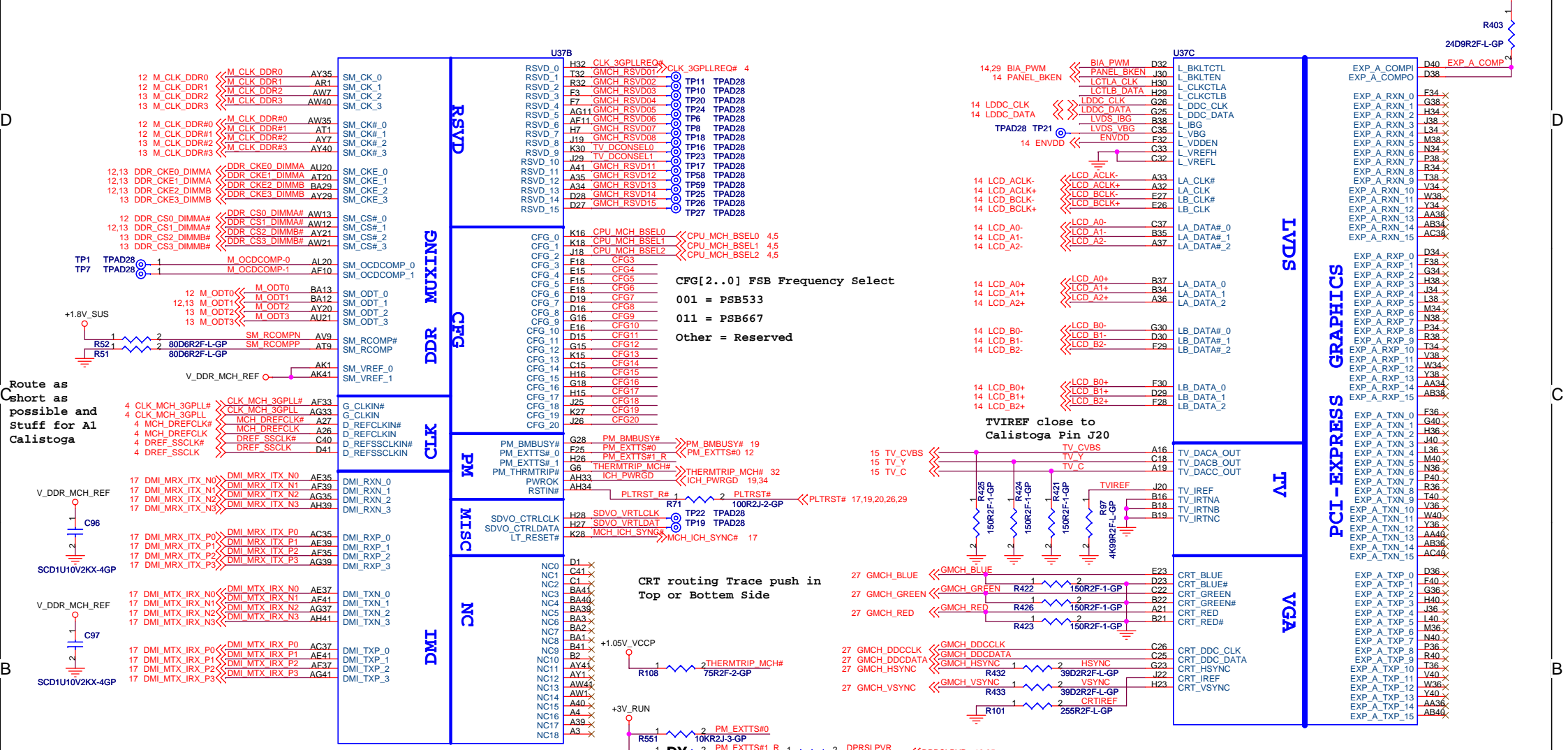


DELL Wistron Corporation
 21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **GMCH - 01 - Calistoga - FSB**

Size: A3 Document Number: **Bermuda** Rev: -1

Date: Wednesday, March 01, 2006 Sheet 7 of 45



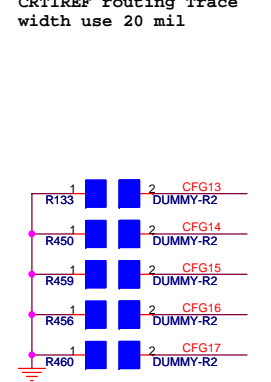
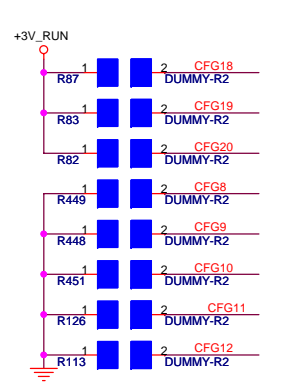
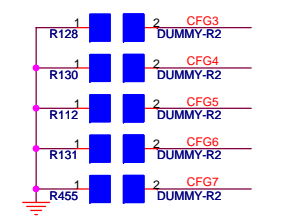
Route as short as possible and Stuff for A1 Calistoga

B

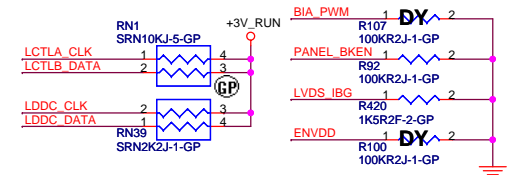
* is Default setting

CFG Strap	Low	High
CFG 5	DMI X 2	DMI X 4 *
CFG 6	Moby Dick	Calistoga *
CFG 7	DT/Transportable CPU	Mobile CPU *
CFG 9	Reserved Lane	Normal Operation *
CFG 10	Reserved	Mobility *
CFG 11	Calistoga *	Reserved
CFG 16	FSB Dynamic ODT	Disabled
CFG 18	VCC Select	1.05V *
CFG 19	DMI Lane Reserved	Normal Operation *
CFG 20	PCIE/SDVO Select	Only PCIE or SDVO is operation *
	SDVO_CTRLDATA	No SDVO Device present *
		PCIE and SDVO are operation simu present *

CFG[13:12]	Value
LL	Reserved
LH	XOR Mode Enabled
HL	All Z Mode Enabled
HH	Normal Operation *



CRTIREF routing Trace width use 20 mil



DELL Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **GMCH-02-Calistoga-LVDS/VGA/DMI/DDR**

Size: A3 Document Number: **Bermuda** Rev: -1

Date: Wednesday, March 01, 2006 Sheet: 8 of 45

U37J

AT23	VSS 180	VSS 273	J11
AN23	VSS 181	VSS 274	D11
AM23	VSS 182	VSS 275	B11
AH23	VSS 183	VSS 276	AW10
AC23	VSS 184	VSS 277	AP10
W23	VSS 185	VSS 278	AL10
K23	VSS 186	VSS 279	AJ10
J23	VSS 187	VSS 280	AG10
F23	VSS 188	VSS 281	AC10
G23	VSS 189	VSS 282	W10
AA22	VSS 190	VSS 283	LI10
K22	VSS 191	VSS 284	BA9
G22	VSS 192	VSS 285	AW9
F22	VSS 193	VSS 286	AR9
E22	VSS 194	VSS 287	AH9
D22	VSS 195	VSS 288	AB9
BA21	VSS 196	VSS 289	Y9
AV21	VSS 197	VSS 290	G9
AR21	VSS 198	VSS 291	E9
AN21	VSS 200	VSS 293	A9
AL21	VSS 201	VSS 294	AG8
AB21	VSS 202	VSS 295	AD8
Y21	VSS 203	VSS 296	AA8
P21	VSS 204	VSS 297	UB8
K21	VSS 205	VSS 298	K8
J21	VSS 206	VSS 299	C8
H21	VSS 208	VSS 300	BA7
C21	VSS 209	VSS 301	AV7
AW20	VSS 210	VSS 302	AP7
AR20	VSS 211	VSS 303	AL7
AM20	VSS 212	VSS 304	AJ7
AA20	VSS 213	VSS 305	AH7
B20	VSS 214	VSS 306	AF7
A20	VSS 215	VSS 307	AC7
AN19	VSS 216	VSS 308	AR7
AC19	VSS 217	VSS 309	G7
W19	VSS 218	VSS 310	D7
K19	VSS 219	VSS 311	AG6
G19	VSS 220	VSS 312	AD6
C19	VSS 221	VSS 313	AB6
AW18	VSS 222	VSS 314	Y6
AR18	VSS 223	VSS 315	UB6
H18	VSS 224	VSS 316	UB6
D18	VSS 225	VSS 317	UB6
A18	VSS 226	VSS 318	UB6
AY17	VSS 227	VSS 319	B6
AR17	VSS 228	VSS 320	AV5
AP17	VSS 229	VSS 321	AD5
AM17	VSS 230	VSS 322	AF4
AK17	VSS 231	VSS 323	AY4
AV16	VSS 232	VSS 324	AR4
AN16	VSS 233	VSS 325	AP4
AL16	VSS 234	VSS 326	AL4
J16	VSS 235	VSS 327	AJ4
F16	VSS 236	VSS 328	Y4
C16	VSS 237	VSS 329	UB4
AN15	VSS 238	VSS 330	R4
AM15	VSS 239	VSS 331	J4
AK15	VSS 240	VSS 332	F4
N15	VSS 241	VSS 333	C4
M15	VSS 242	VSS 334	AW3
L15	VSS 243	VSS 335	AW3
B15	VSS 244	VSS 336	AW3
A15	VSS 245	VSS 337	AW3
BA14	VSS 246	VSS 338	AH3
AT14	VSS 247	VSS 339	AG3
AK14	VSS 248	VSS 340	AF3
AD14	VSS 249	VSS 341	AD3
AA14	VSS 250	VSS 342	AC3
U14	VSS 251	VSS 343	AA3
K14	VSS 252	VSS 344	G3
H14	VSS 253	VSS 345	AT2
E14	VSS 254	VSS 346	AR2
AV13	VSS 255	VSS 347	AR2
AR13	VSS 256	VSS 348	AK2
AN13	VSS 257	VSS 349	AK2
AM13	VSS 258	VSS 350	AJ2
AL13	VSS 259	VSS 351	AD2
AG13	VSS 260	VSS 352	AD2
F13	VSS 261	VSS 353	Y2
D13	VSS 262	VSS 354	L2
B13	VSS 263	VSS 355	I2
AY12	VSS 264	VSS 356	H2
AC12	VSS 265	VSS 357	F2
K12	VSS 266	VSS 358	C2
H12	VSS 267	VSS 359	C2
E12	VSS 268	VSS 360	AL1
AD11	VSS 269		
AA11	VSS 270		
Y11	VSS 271		
	VSS 272		

VSS

U37D

DDR A D0	AJ35	SA_DQ0
DDR A D1	AJ34	SA_DQ1
DDR A D2	AM31	SA_DQ2
DDR A D3	AM32	SA_DQ3
DDR A D4	AM33	SA_DQ4
DDR A D5	AK35	SA_DQ5
DDR A D6	AJ32	SA_DQ6
DDR A D7	AH31	SA_DQ7
DDR A D8	AN35	SA_DQ8
DDR A D9	AP33	SA_DQ9
DDR A D10	AR31	SA_DQ10
DDR A D11	AP31	SA_DQ11
DDR A D12	AN38	SA_DQ12
DDR A D13	AM36	SA_DQ13
DDR A D14	AM34	SA_DQ14
DDR A D15	AN33	SA_DQ15
DDR A D16	AK26	SA_DQ16
DDR A D17	AL27	SA_DQ17
DDR A D18	AM26	SA_DQ18
DDR A D19	AN24	SA_DQ19
DDR A D20	AK28	SA_DQ20
DDR A D21	AL28	SA_DQ21
DDR A D22	AM24	SA_DQ22
DDR A D23	AP26	SA_DQ23
DDR A D24	AP23	SA_DQ24
DDR A D25	AL22	SA_DQ25
DDR A D26	AP21	SA_DQ26
DDR A D27	AN20	SA_DQ27
DDR A D28	AL23	SA_DQ28
DDR A D29	AP24	SA_DQ29
DDR A D30	AP20	SA_DQ30
DDR A D31	AT21	SA_DQ31
DDR A D32	AR12	SA_DQ32
DDR A D33	AR14	SA_DQ33
DDR A D34	AP13	SA_DQ34
DDR A D35	AP12	SA_DQ35
DDR A D36	AT13	SA_DQ36
DDR A D37	AT12	SA_DQ37
DDR A D38	AL14	SA_DQ38
DDR A D39	AL12	SA_DQ39
DDR A D40	AK9	SA_DQ40
DDR A D41	AN7	SA_DQ41
DDR A D42	AK8	SA_DQ42
DDR A D43	AK7	SA_DQ43
DDR A D44	AP9	SA_DQ44
DDR A D45	AN9	SA_DQ45
DDR A D46	AT5	SA_DQ46
DDR A D47	AL5	SA_DQ47
DDR A D48	AY2	SA_DQ48
DDR A D49	AW2	SA_DQ49
DDR A D50	AF1	SA_DQ50
DDR A D51	AN2	SA_DQ51
DDR A D52	AV2	SA_DQ52
DDR A D53	AT3	SA_DQ53
DDR A D54	AN1	SA_DQ54
DDR A D55	AL2	SA_DQ55
DDR A D56	AG7	SA_DQ56
DDR A D57	AF9	SA_DQ57
DDR A D58	AG4	SA_DQ58
DDR A D59	AF6	SA_DQ59
DDR A D60	AG9	SA_DQ60
DDR A D61	AH6	SA_DQ61
DDR A D62	AF4	SA_DQ62
DDR A D63	AF8	SA_DQ63

DDR SYSTEM MEMORY A

DDR A D[0..63] << >> DDR_A_D[0..63] 12
 DDR A BS[0..2] << >> DDR_A_BS[0..2] 12,13
 DDR A DM[0..7] << >> DDR_A_DM[0..7] 12
 DDR A DQS[0..7] << >> DDR_A_DQS[0..7] 12
 DDR A DQS# [0..7] << >> DDR_A_DQS#[0..7] 12
 DDR A MA[0..13] << >> DDR_A_MA[0..13] 12,13

SA_BS_0	AY12	DDR A BS0	SA_BS_0
SA_BS_1	AV14	DDR A BS1	SA_BS_1
SA_BS_2	BA20	DDR A BS2	SA_BS_2
SA_CAS#	AY13	DDR A CAS#	SA_CAS#
SA_DM_0	AJ33	DDR A DM0	SA_DM_0
SA_DM_1	AM35	DDR A DM1	SA_DM_1
SA_DM_2	AL26	DDR A DM2	SA_DM_2
SA_DM_3	AN22	DDR A DM3	SA_DM_3
SA_DM_4	AM14	DDR A DM4	SA_DM_4
SA_DM_5	AL9	DDR A DM5	SA_DM_5
SA_DM_6	AR3	DDR A DM6	SA_DM_6
SA_DM_7	AH4	DDR A DM7	SA_DM_7
SA_DQS_0	AK33	DDR A DQS0	SA_DQS_0
SA_DQS_1	AT33	DDR A DQS1	SA_DQS_1
SA_DQS_2	AN28	DDR A DQS2	SA_DQS_2
SA_DQS_3	AM22	DDR A DQS3	SA_DQS_3
SA_DQS_4	AN8	DDR A DQS4	SA_DQS_4
SA_DQS_5	AP3	DDR A DQS5	SA_DQS_5
SA_DQS_6	AG5	DDR A DQS6	SA_DQS_6
SA_DQS_7	AG5	DDR A DQS7	SA_DQS_7
SA_DQS#_0	AK32	DDR A DQS#0	SA_DQS#_0
SA_DQS#_1	AU33	DDR A DQS#1	SA_DQS#_1
SA_DQS#_2	AN27	DDR A DQS#2	SA_DQS#_2
SA_DQS#_3	AM21	DDR A DQS#3	SA_DQS#_3
SA_DQS#_4	AM12	DDR A DQS#4	SA_DQS#_4
SA_DQS#_5	AL8	DDR A DQS#5	SA_DQS#_5
SA_DQS#_6	AN3	DDR A DQS#6	SA_DQS#_6
SA_DQS#_7	AH5	DDR A DQS#7	SA_DQS#_7
SA_MA_0	AY16	DDR A MA0	SA_MA_0
SA_MA_1	AU14	DDR A MA1	SA_MA_1
SA_MA_2	AW16	DDR A MA2	SA_MA_2
SA_MA_3	BA16	DDR A MA3	SA_MA_3
SA_MA_4	BA17	DDR A MA4	SA_MA_4
SA_MA_5	AU16	DDR A MA5	SA_MA_5
SA_MA_6	AV17	DDR A MA6	SA_MA_6
SA_MA_7	AW17	DDR A MA7	SA_MA_7
SA_MA_8	AW16	DDR A MA8	SA_MA_8
SA_MA_9	AT16	DDR A MA9	SA_MA_9
SA_MA_10	AU13	DDR A MA10	SA_MA_10
SA_MA_11	AT17	DDR A MA11	SA_MA_11
SA_MA_12	AV20	DDR A MA12	SA_MA_12
SA_MA_13	AV12	DDR A MA13	SA_MA_13

SA_RAS# << >> AY14 <>> TP3 RAS# TPAD28
 SA_RCVENIN# << >> AK23 <>> TP4 RAS# TPAD28
 SA_RCVENOUT# << >> AK24 <>> TP4 RAS# TPAD28
 SA_WE# << >> AY14 <>> TP4 WE# TPAD28

DDR B D[0..63] << >> DDR_B_D[0..63] 13
 DDR B BS[0..2] << >> DDR_B_BS[0..2] 12,13
 DDR B DM[0..7] << >> DDR_B_DM[0..7] 13
 DDR B DQS[0..7] << >> DDR_B_DQS[0..7] 13
 DDR B DQS# [0..7] << >> DDR_B_DQS#[0..7] 13
 DDR B MA[0..13] << >> DDR_B_MA[0..13] 12,13

U37E

DDR B D0	AK39	SB_DQ0
DDR B D1	AJ37	SB_DQ1
DDR B D2	AP39	SB_DQ2
DDR B D3	AR41	SB_DQ3
DDR B D4	AJ38	SB_DQ4
DDR B D5	AK38	SB_DQ5
DDR B D6	AN41	SB_DQ6
DDR B D7	AP41	SB_DQ7
DDR B D8	AT40	SB_DQ8
DDR B D9	AV41	SB_DQ9
DDR B D10	AU38	SB_DQ10
DDR B D11	AP38	SB_DQ11
DDR B D12	AR40	SB_DQ12
DDR B D13	AW38	SB_DQ13
DDR B D14	AY38	SB_DQ14
DDR B D15	AY38	SB_DQ15
DDR B D16	BA38	SB_DQ16
DDR B D17	AV36	SB_DQ17
DDR B D18	AR36	SB_DQ18
DDR B D19	AP36	SB_DQ19
DDR B D20	BA36	SB_DQ20
DDR B D21	AU36	SB_DQ21
DDR B D22	AP36	SB_DQ22
DDR B D23	AV36	SB_DQ23
DDR B D24	AP34	SB_DQ24
DDR B D25	BA33	SB_DQ25
DDR B D26	AT31	SB_DQ26
DDR B D27	AU29	SB_DQ27
DDR B D28	AU31	SB_DQ28
DDR B D29	AW31	SB_DQ29
DDR B D30	AV29	SB_DQ30
DDR B D31	AW29	SB_DQ31
DDR B D32	AM19	SB_DQ32
DDR B D33	AL19	SB_DQ33
DDR B D34	AP14	SB_DQ34
DDR B D35	AN14	SB_DQ35
DDR B D36	AN17	SB_DQ36
DDR B D37	AM16	SB_DQ37
DDR B D38	AP15	SB_DQ38
DDR B D39	AL15	SB_DQ39
DDR B D40	AJ11	SB_DQ40
DDR B D41	AH10	SB_DQ41
DDR B D42	AJ9	SB_DQ42
DDR B D43	AN10	SB_DQ43
DDR B D44	AK13	SB_DQ44
DDR B D45	AH11	SB_DQ45
DDR B D46	AK10	SB_DQ46
DDR B D47	AJ8	SB_DQ47
DDR B D48	BA10	SB_DQ48
DDR B D49	AW10	SB_DQ49
DDR B D50	BA4	SB_DQ50
DDR B D51	AW4	SB_DQ51
DDR B D52	AY10	SB_DQ52
DDR B D53	AY9	SB_DQ53
DDR B D54	AW6	SB_DQ54
DDR B D55	AY5	SB_DQ55
DDR B D56	AV4	SB_DQ56
DDR B D57	BA4	SB_DQ57
DDR B D58	AK4	SB_DQ58
DDR B D59	AK3	SB_DQ59
DDR B D60	AT4	SB_DQ60
DDR B D61	AK5	SB_DQ61
DDR B D62	AJ8	SB_DQ62
DDR B D63	AJ3	SB_DQ63

DDR SYSTEM MEMORY B

SB_BS_0	AT24	DDR B BS0
SB_BS_1	AV23	DDR B BS1
SB_BS_2	AY28	DDR B BS2
SB_CAS#	AR24	DDR B CAS#
SB_DM_0	AK36	DDR B DM0
SB_DM_1	AR38	DDR B DM1
SB_DM_2	AT36	DDR B DM2
SB_DM_3	BA31	DDR B DM3
SB_DM_4	AL17	DDR B DM4
SB_DM_5	AH8	DDR B DM5
SB_DM_6	BA5	DDR B DM6
SB_DM_7	AN4	DDR B DM7
SB_DQS_0	AM39	DDR B DQS0
SB_DQS_1	AT39	DDR B DQS1
SB_DQS_2	AU35	DDR B DQS2
SB_DQS_3	AR29	DDR B DQS3
SB_DQS_4	AR16	DDR B DQS4
SB_DQS_5	AR10	DDR B DQS5
SB_DQS_6	AR7	DDR B DQS6
SB_DQS_7	AN5	DDR B DQS7
SB_DQS#_0	AM40	DDR B DQS#0
SB_DQS#_1	AT35	DDR B DQS#1
SB_DQS#_2	AP29	DDR B DQS#2
SB_DQS#_3	AP29	DDR B DQS#3
SB_DQS#_4	AP16	DDR B DQS#4
SB_DQS#_5	AT10	DDR B DQS#5
SB_DQS#_6	AT7	DDR B DQS#6
SB_DQS#_7	AP5	DDR B DQS#7
SB_MA_0	AY23	DDR B MA0
SB_MA_1	AW24	DDR B MA1
SB_MA_2	AY24	DDR B MA2
SB_MA_3	AR28	DDR B MA3
SB_MA_4	AT27	DDR B MA4
SB_MA_5	AT28	DDR B MA5
SB_MA_6	AU27	DDR B MA6
SB_MA_7	AV28	DDR B MA7
SB_MA_8	AV27	DDR B MA8
SB_MA_9	AW27	DDR B MA9
SB_MA_10	AV24	DDR B MA10
SB_MA_11	BA27	DDR B MA11
SB_MA_12	AY27	DDR B MA12
SB_MA_13	AR23	DDR B MA13
SB_RAS#	AU23	DDR B RAS#
SB_RCVENIN#	AK16	M B RCVENIN# TP5
SB_RCVENOUT#	AK18	M B RCVENOUT# TP2
SB_WE#	AR27	DDR B WE#



Wistron Corporation
 21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

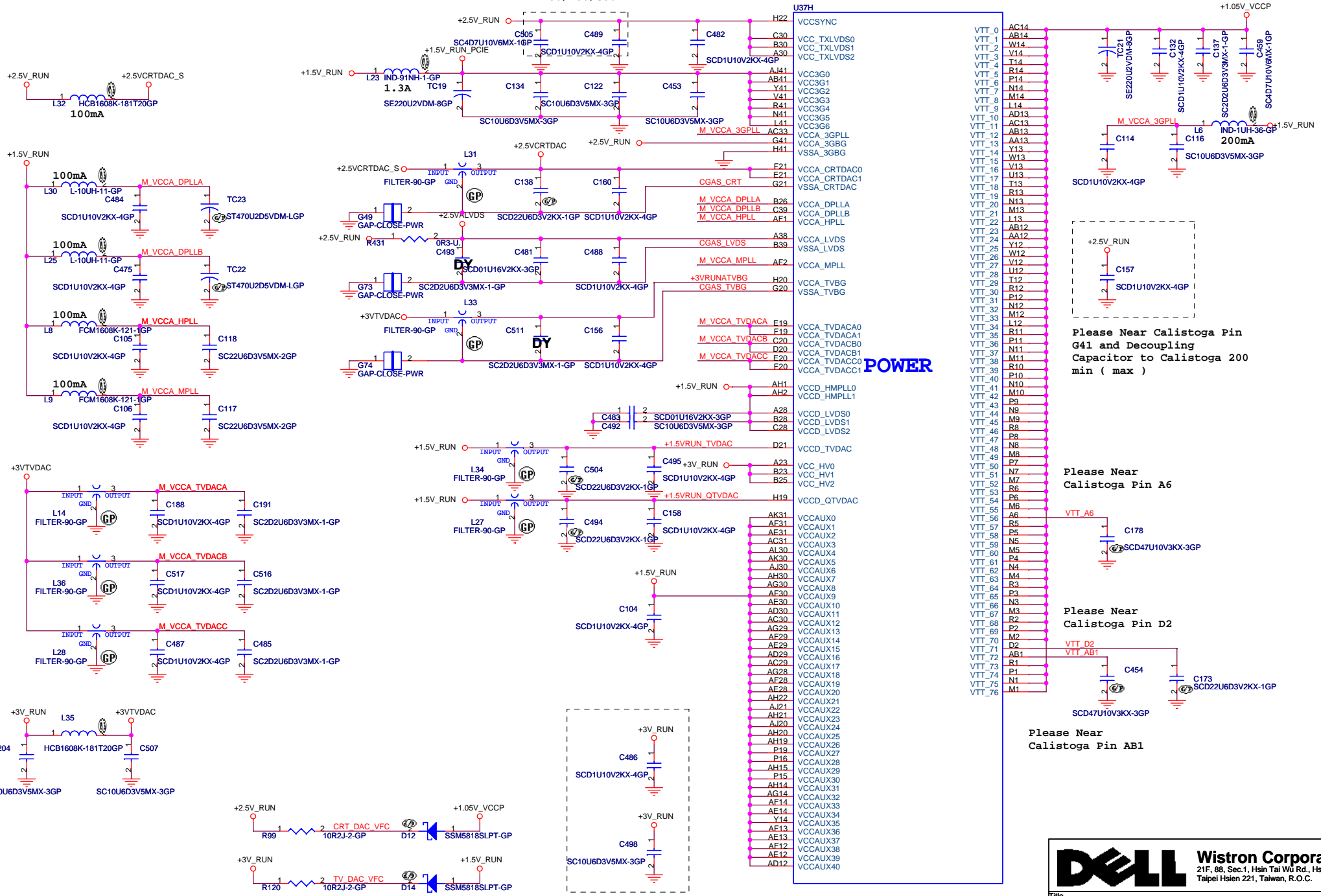
Title: **GMCH - 03 - Calistoga - DDR**

Size: A3 | Document Number: **Bermuda** | Rev: -1

Date: Wednesday, March 01, 2006 | Sheet 9 of 45

hexainf@hotmail.com
 GRATIS - FOR FREE

Please Near Calistoga
Pin A30/B30/C30

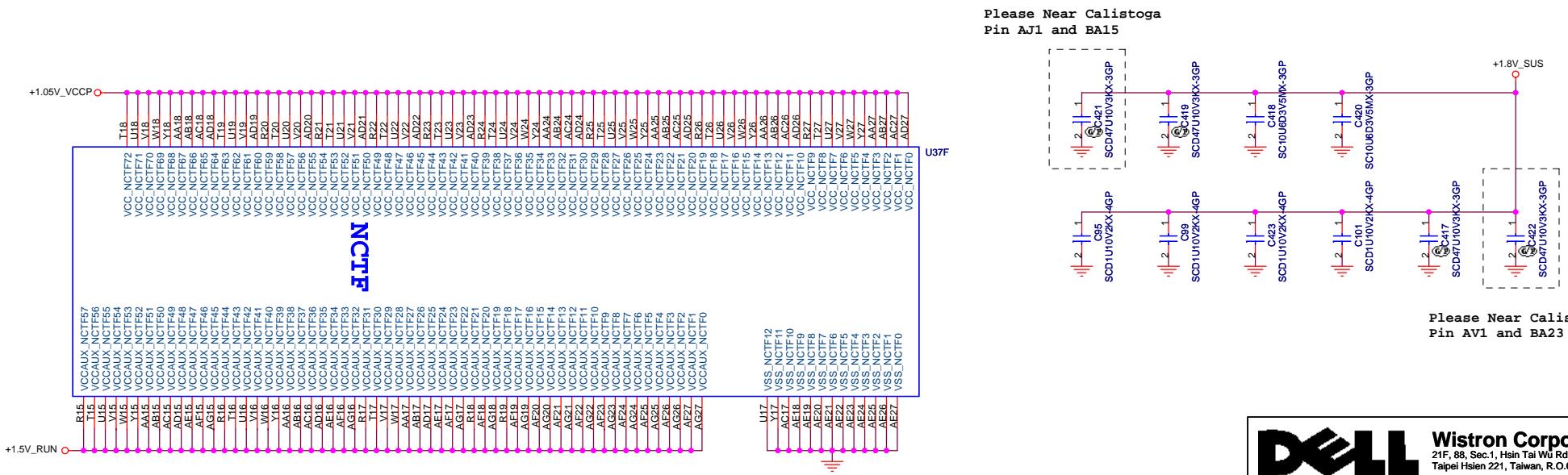
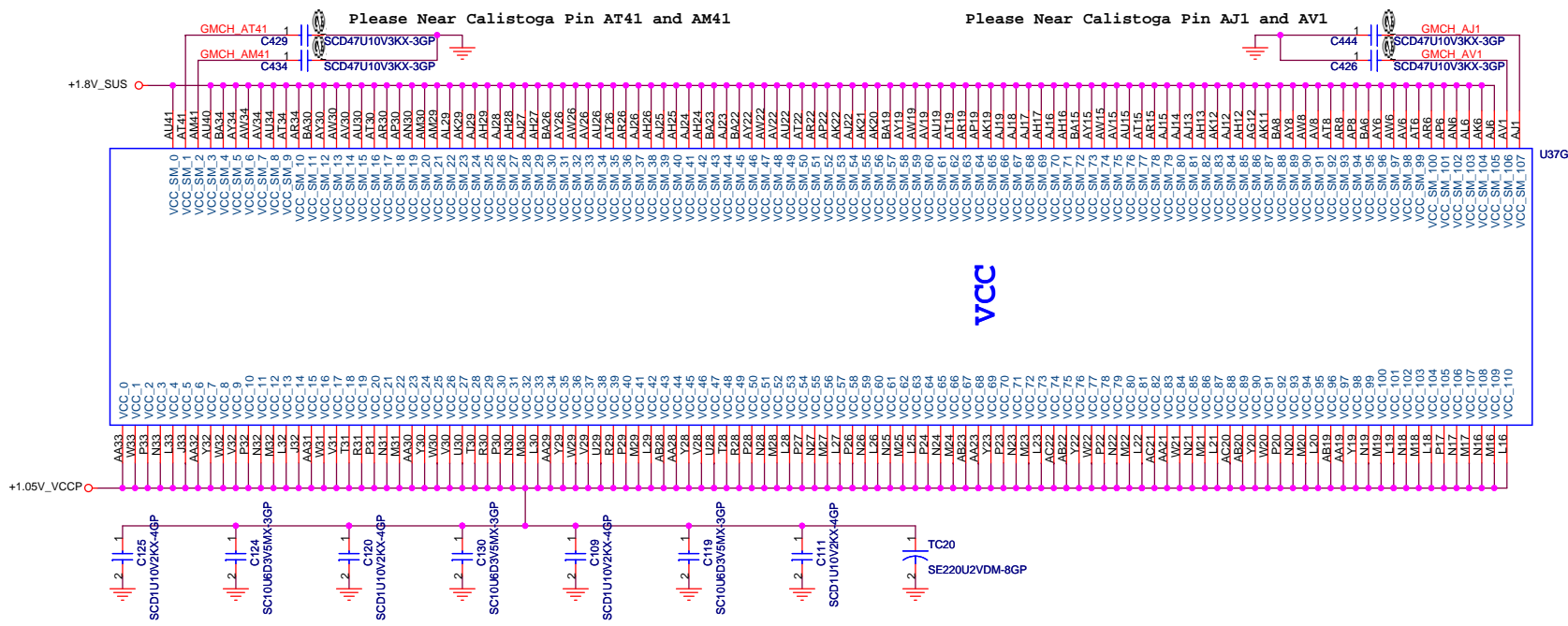


Please Near Calistoga
Pin A23/B23/B25



Title			
GMCH - 04 - Calistoga - POWER/FILTER			
Size	Document Number	Rev	
A3		-1	
Date:	Wednesday, March 01, 2006	Sheet	10 of 45

hexainf@hotmail.com
GRATIS - FOR FREE



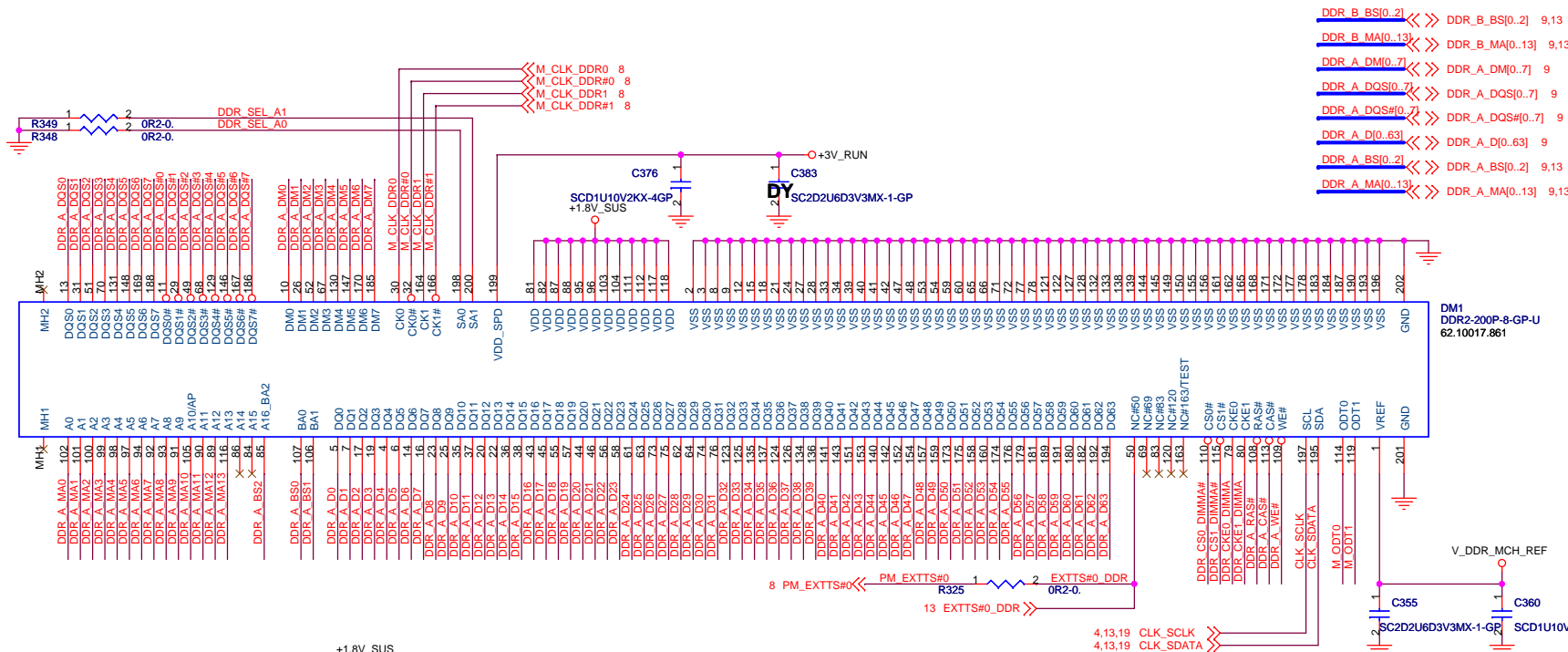
DELL Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **GMCH - 05 - Calistoga - POWER**

Size: A3 Document Number: **Bermuda** Rev: -1

Date: Wednesday, March 01, 2006 Sheet 11 of 45

hexainf@hotmail.com
 GRATIS - FOR FREE



- DDR_B_BS[0..2] <<> DDR_B_BS[0..2] 9,13
- DDR_B_MA[0..13] <<> DDR_B_MA[0..13] 9,13
- DDR_A_DM[0..7] <<> DDR_A_DM[0..7] 9
- DDR_A_DQS[0..7] <<> DDR_A_DQS[0..7] 9
- DDR_A_DQS#[0..7] <<> DDR_A_DQS#[0..7] 9
- DDR_A_DI[0..63] <<> DDR_A_DI[0..63] 9
- DDR_A_BS[0..2] <<> DDR_A_BS[0..2] 9,13
- DDR_A_MA[0..13] <<> DDR_A_MA[0..13] 9,13

Please close to the DIMM Slot

Please use One Capacitor close to every Two pull-up Resistors

M_CKE[1:0] and M_CS[1:0]# pull-up Resistors close DIMM Slot 1300 mil (MAX)
Others pull-up Resistors close DIMM Slot 750 mil (MAX)

- DDR_CS1_DIMMA# <<> DDR_CS1_DIMMA# 8,13
- DDR_CKE0_DIMMA <<> DDR_CKE0_DIMMA 8,13
- DDR_CKE1_DIMMA <<> DDR_CKE1_DIMMA 8,13
- DDR_A_CAS# <<> DDR_A_CAS# 9,13
- DDR_A_WE# <<> DDR_A_WE# 9,13
- M_ODT1 <<> M_ODT1 8,13

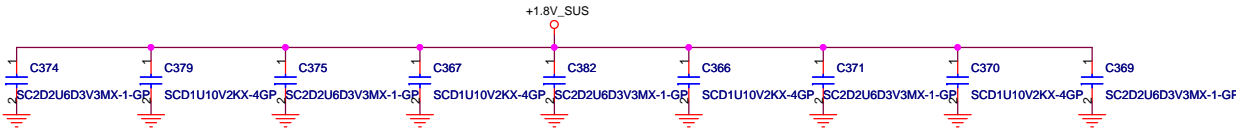
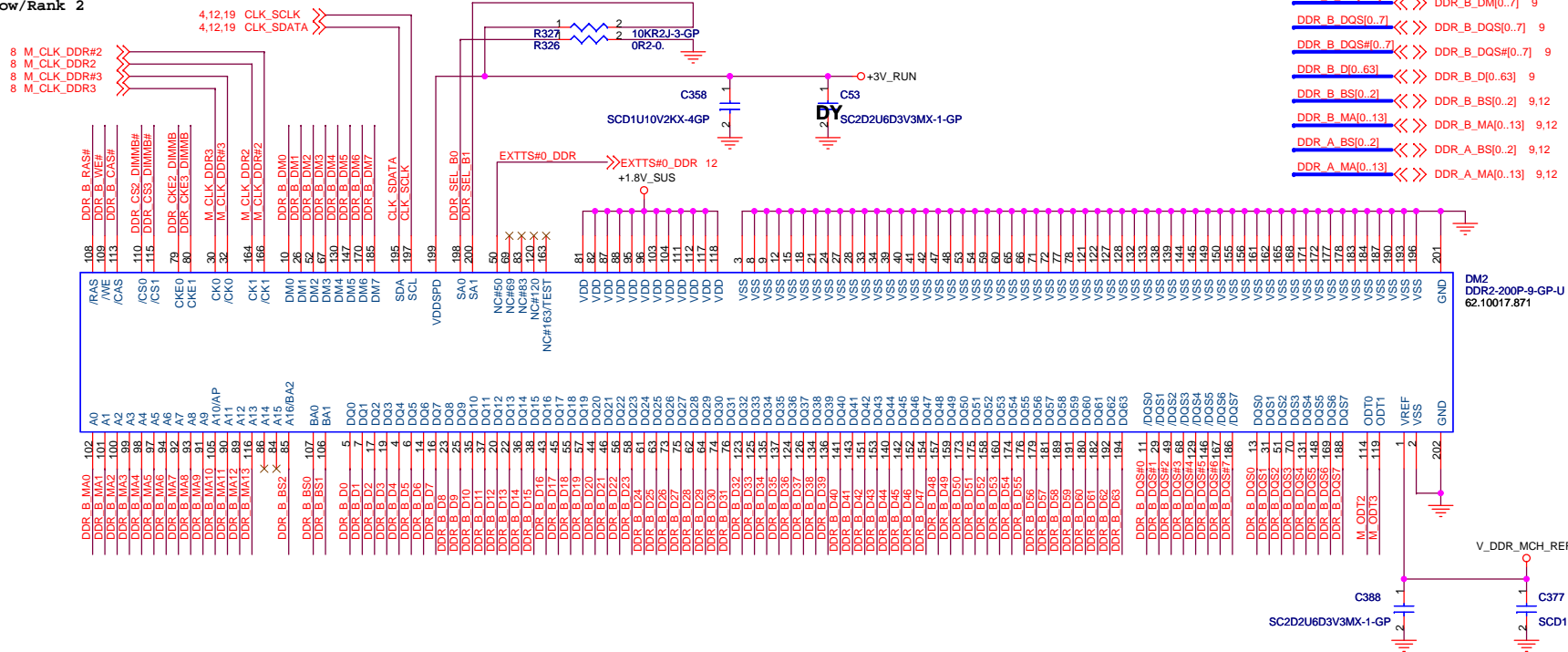
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **DDR II - 01**

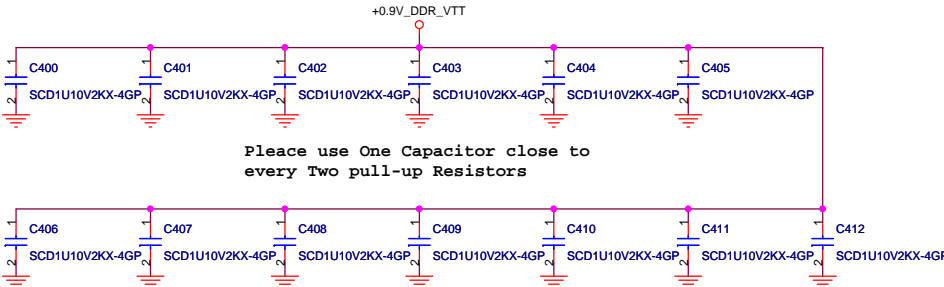
Size A3	Document Number	Rev
	Bermuda	-1

Date: Wednesday, March 01, 2006 Sheet 12 of 45

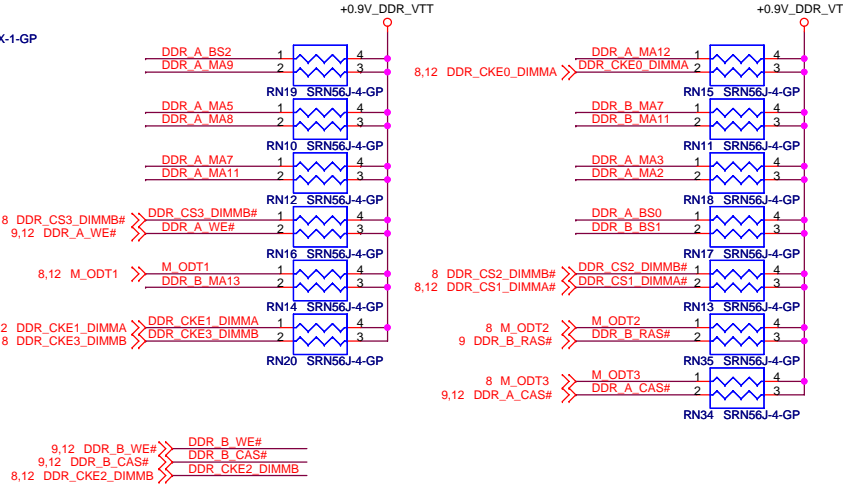
M_CLK_DDR3 and M_CLK_DDR#3
can map to Row/Rank 2



Please close to the DIMM Slot



Please use One Capacitor close to every Two pull-up Resistors



M_CKE[3:2] and M_CS[3:2]#
pull-up Resistors close DIMM
Slot 1300 mil (MAX)
Others pull-up Resistors close
DIMM slot 750 mil (MAX)

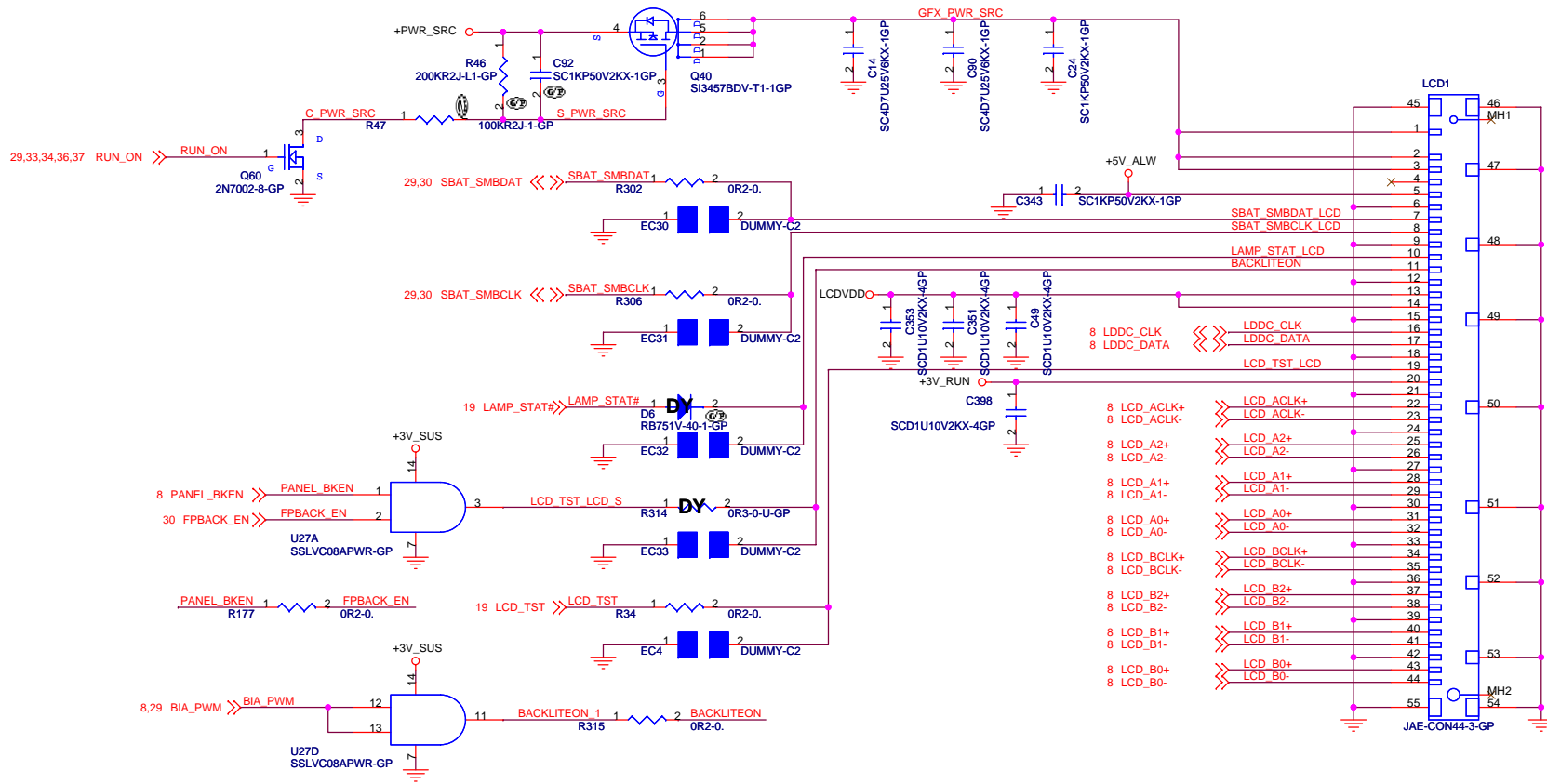
DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **DDR II - 02**

Size A3 Document Number: **Bermuda** Rev: **-1**

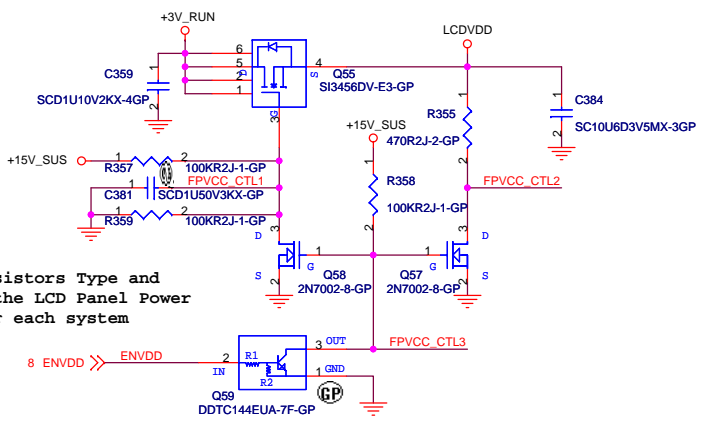
Date: Wednesday, March 01, 2006 Sheet 13 of 45

SSID = VIDEO



M00 support D05 Inverter

- M'07 Inverter support : Populate this Two Resister and De-populate this SSLVC08APWR
- D'05 Inverter support : De-populate this Two Resister and Populate this SSLVC08APWR

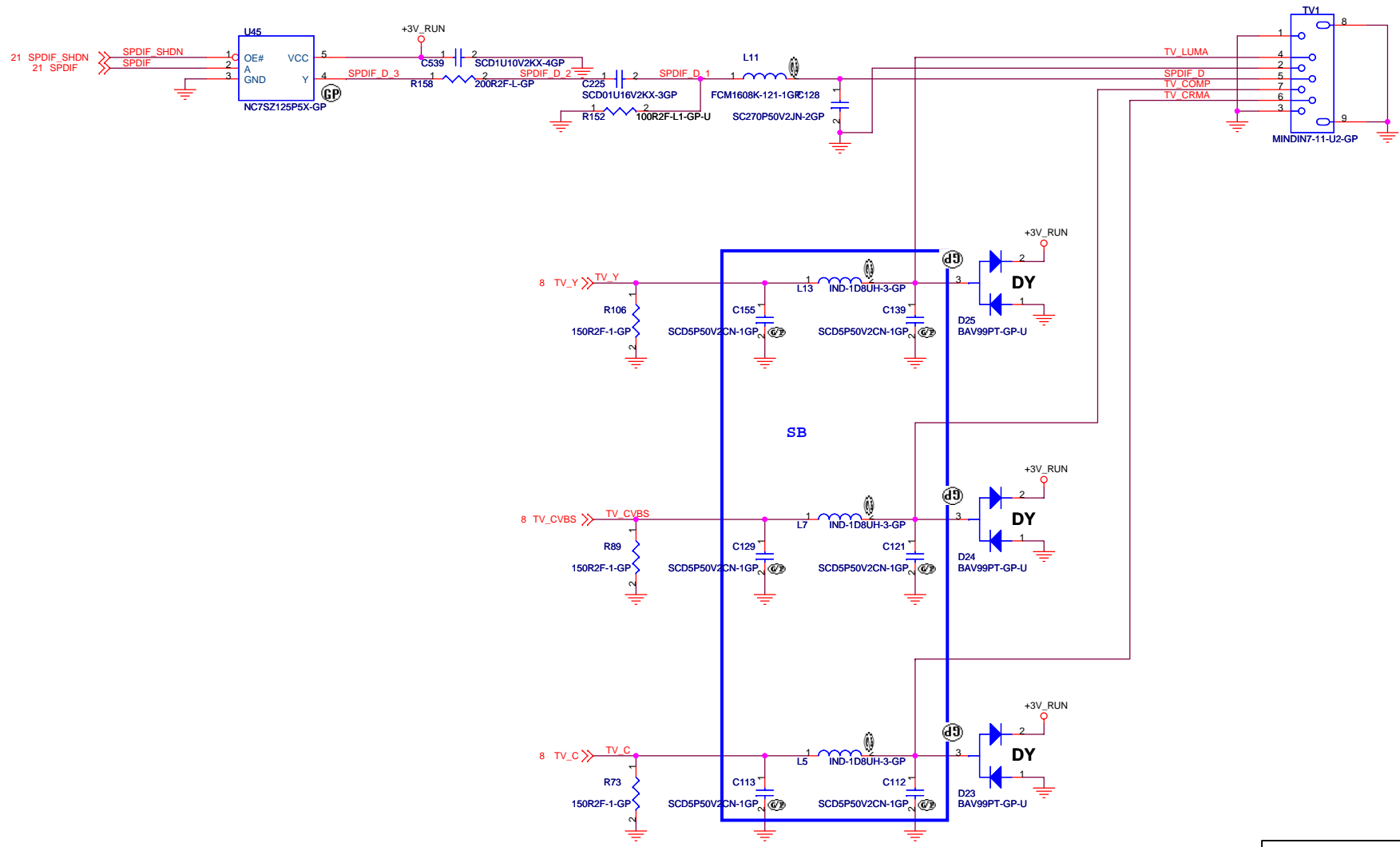


Choose the Transistors Type and Rating base on the LCD Panel Power requirements for each system

DELL Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

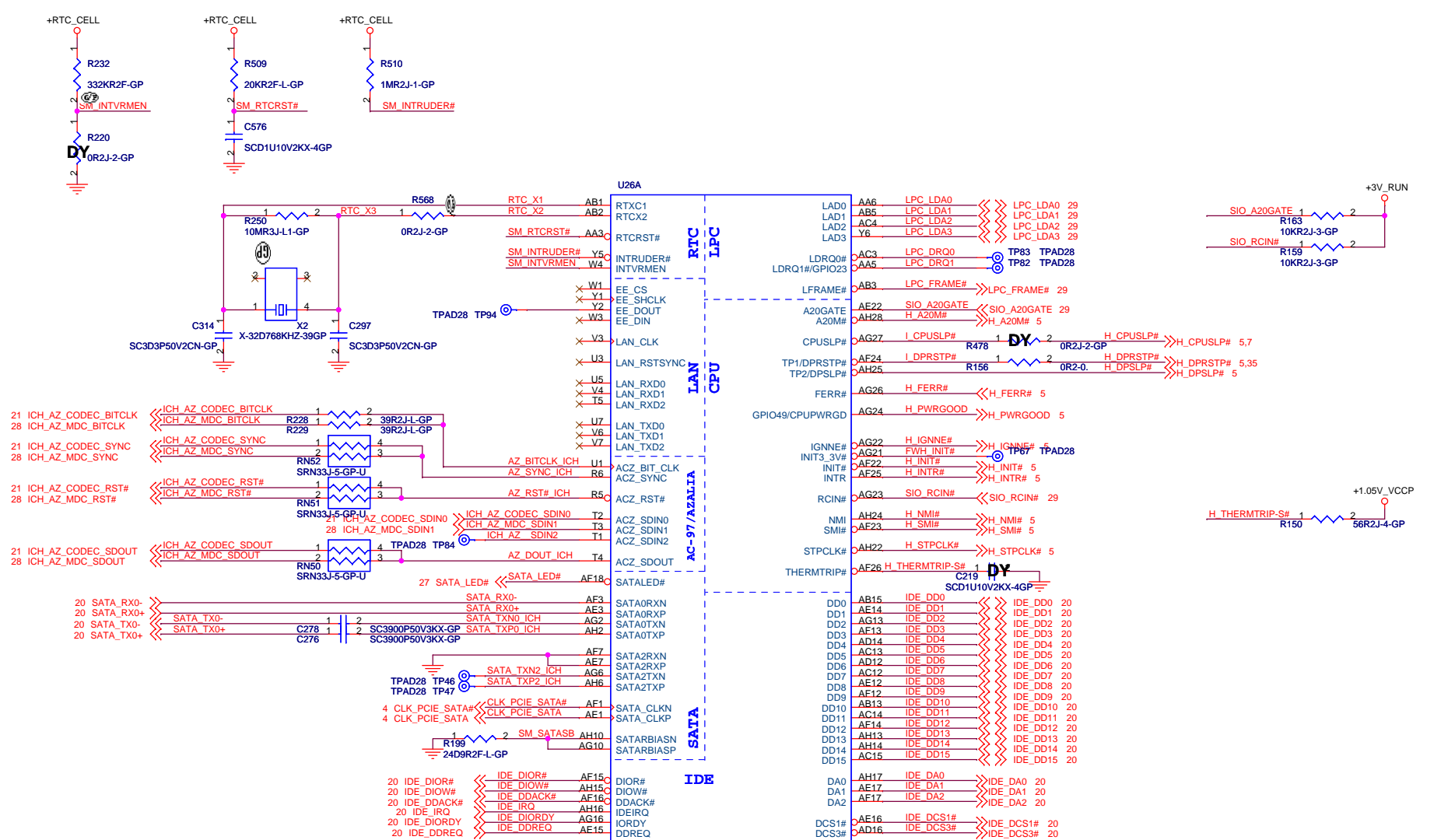
Title LCD		
Size A3	Document Number Bermuda	Rev -1
Date: Wednesday, March 01, 2006 Sheet 14 of 45		

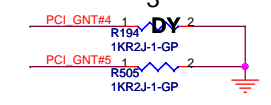
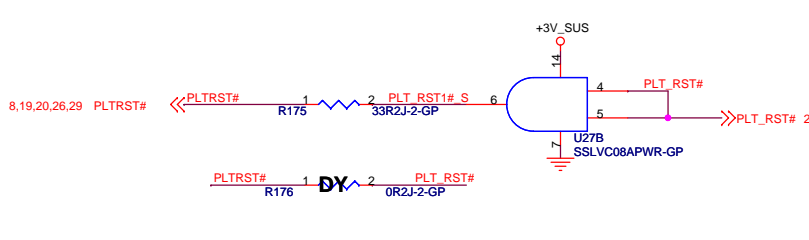
SSID = VIDEO



DELL Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title			TV OUT
Size	Document Number	Rev	
A3		-1	
Date:	Wednesday, March 01, 2006	Sheet	15 of 45

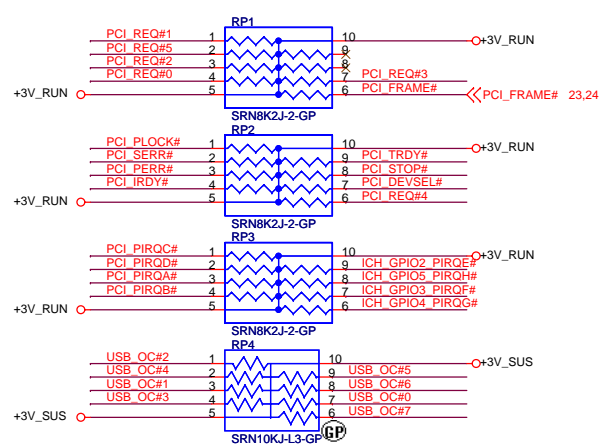
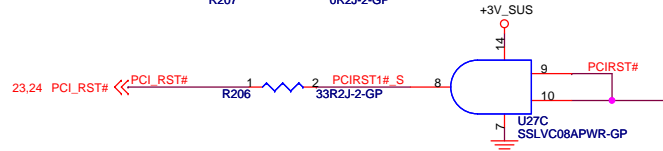




Boot from various source

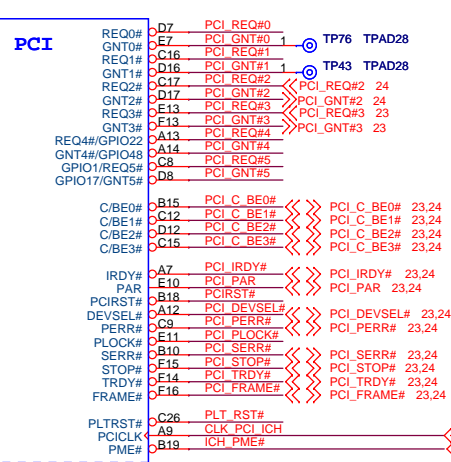
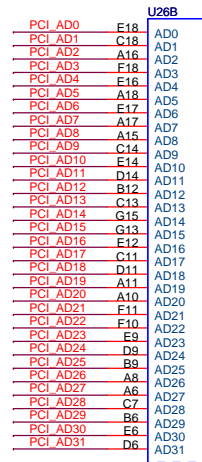
	PCI_GNT#5	PCI_GNT#4
LPC	HH	OFF
PCI	HL	OFF
SPI	LH	ON

Add Buffers as need for Loading and Fanout concerns

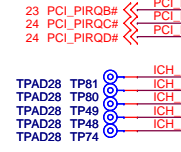


PCI Interface Routing

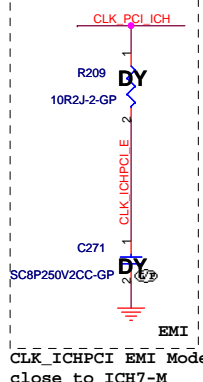
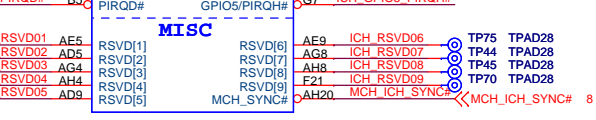
	IDSEL	INT	REQ	GNT
LAN	AD16	B	3	3
1394	AD17	D	2	2



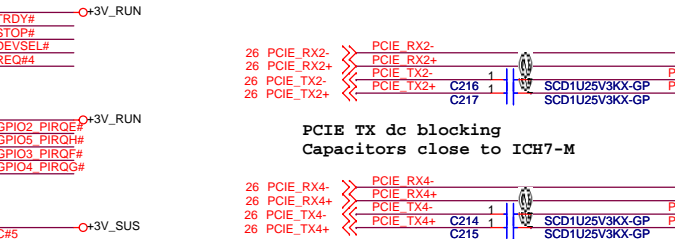
Interrupt I/F



MISC

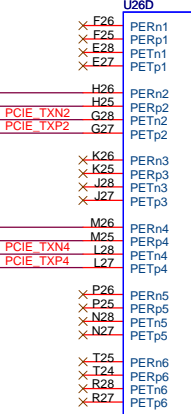


PCIE TX dc blocking Capacitors close to ICH7-M

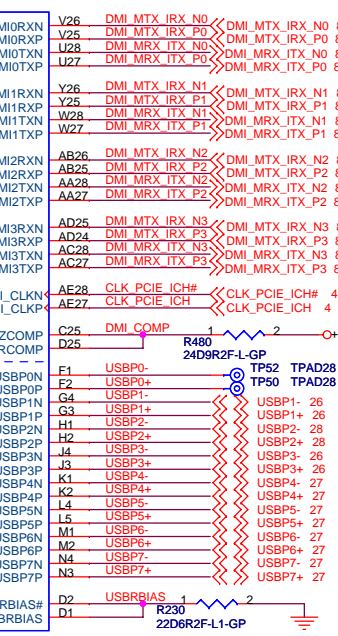


PCIE Interface Routing

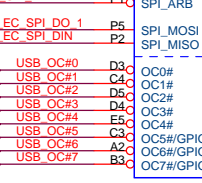
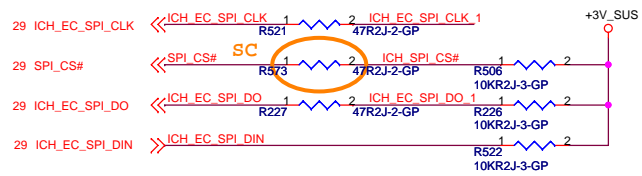
LANE2	MiniCard WLAN
LANE4	Express Card



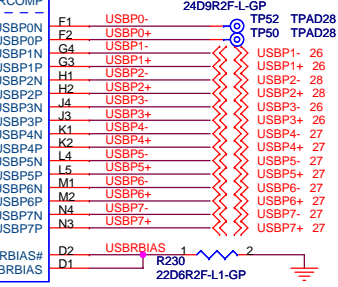
Direct Media Interface



DMI_COMP close to ICH7-M 500 mil



USB

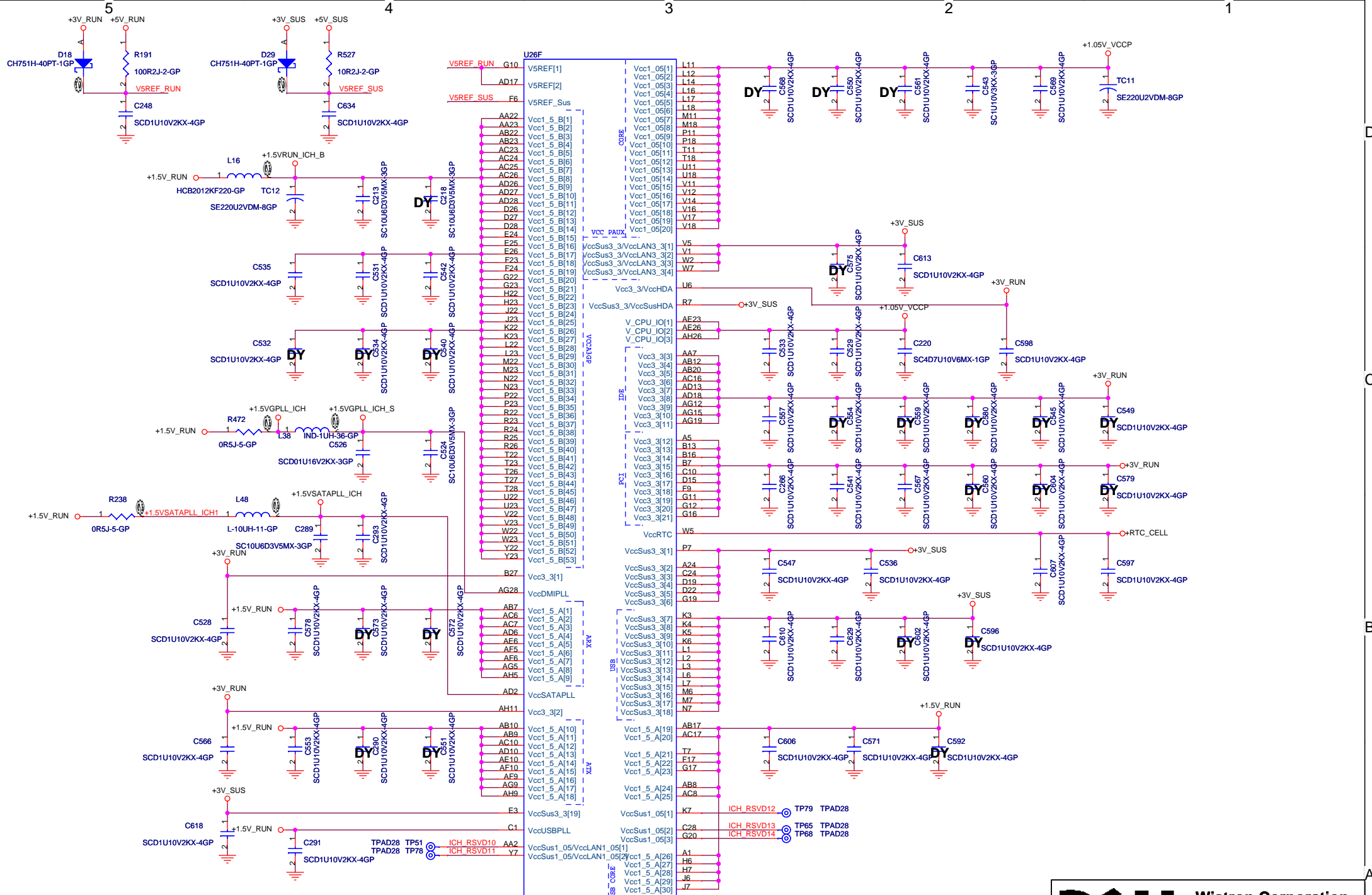


USBRRBIAS close to ICH7-M 500 mil and Trace impedance should be 60 ohm +/- 15%

Dell Arrangement for USB

USB0	No Use
USB1	Express Card
USB2	Bluetooth
USB3	MiniCard WLAN
USB4	Ext Side Top
USB5	Ext Back Top
USB6	Ext Side Bot
USB7	Ext Back Bot





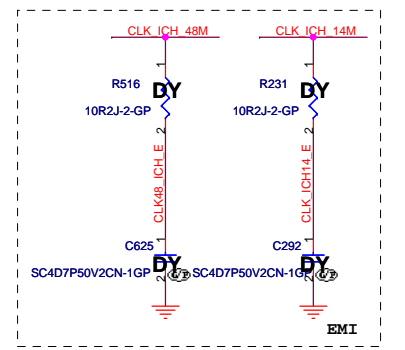
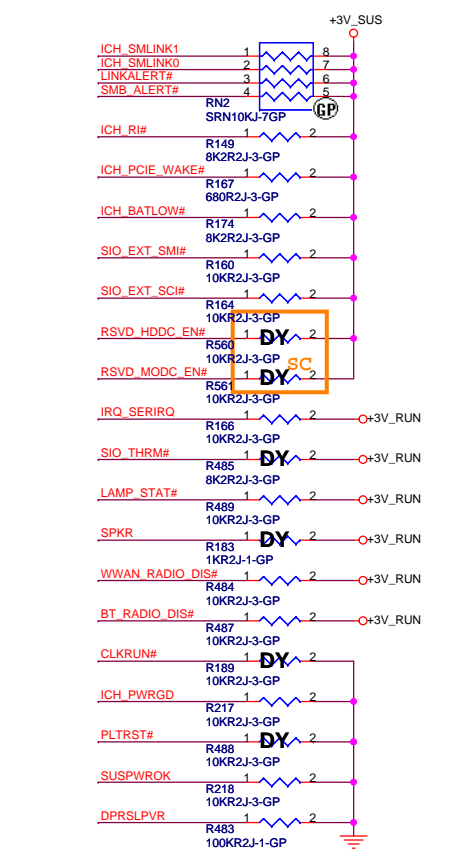
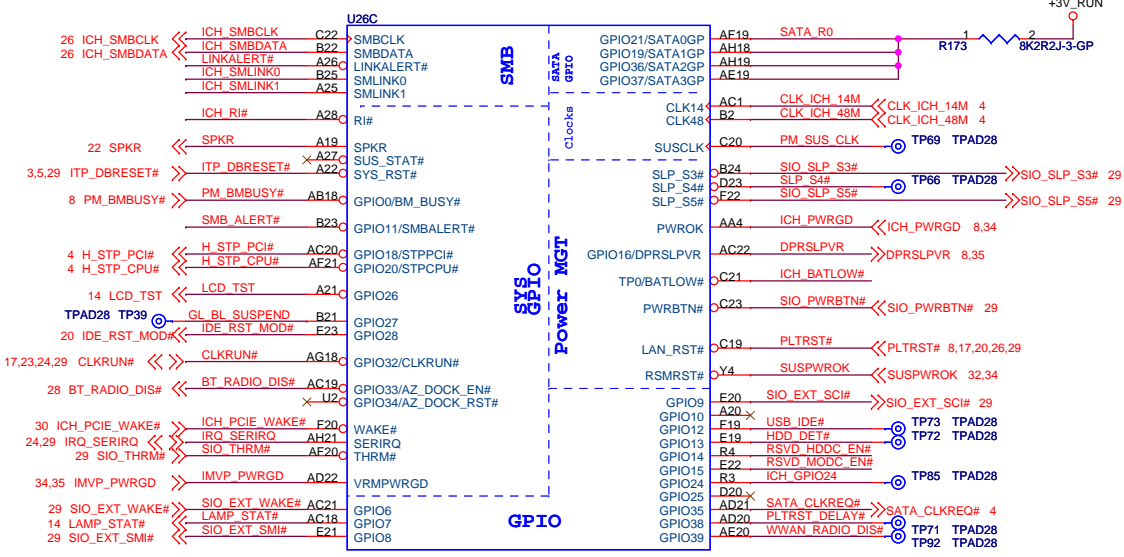
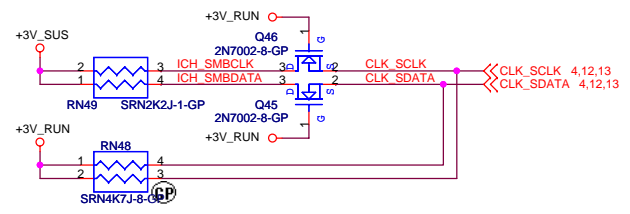
DELL Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **ICH7-M - 03 - POWER**

Size: A3 Document Number: **Bermuda** Rev: -1

Date: Wednesday, March 01, 2006 Sheet 18 of 45

U26E		
A4	VSS[1]	P28
A23	VSS[2]	R1
B1	VSS[3]	R11
B8	VSS[4]	R12
B11	VSS[5]	R13
B14	VSS[6]	R14
B17	VSS[7]	R15
B20	VSS[8]	R16
B26	VSS[9]	R17
B28	VSS[10]	R18
C2	VSS[11]	T6
C6	VSS[12]	T12
C27	VSS[13]	T13
D10	VSS[14]	T14
D13	VSS[15]	T15
D18	VSS[16]	T16
D21	VSS[17]	T17
D24	VSS[18]	U4
E1	VSS[19]	U12
E2	VSS[20]	U13
E4	VSS[21]	U14
E8	VSS[22]	U15
F3	VSS[23]	U16
F4	VSS[24]	U17
F5	VSS[25]	U24
F12	VSS[26]	U25
F27	VSS[27]	U26
F28	VSS[28]	V2
F28	VSS[29]	V13
G1	VSS[30]	V15
G2	VSS[31]	V16
G5	VSS[32]	V27
G8	VSS[33]	V6
G9	VSS[34]	W6
G14	VSS[35]	W24
G18	VSS[36]	W25
G21	VSS[37]	W26
G24	VSS[38]	Y3
G25	VSS[39]	Y24
G26	VSS[40]	Y27
H3	VSS[41]	Y28
H4	VSS[42]	AA1
H5	VSS[43]	AA24
H24	VSS[44]	AA25
H27	VSS[45]	AA26
H28	VSS[46]	AA4
J1	VSS[47]	AB6
J2	VSS[48]	AB11
J5	VSS[49]	AB14
J24	VSS[50]	AB16
J25	VSS[51]	AB19
K26	VSS[52]	AB21
K24	VSS[53]	AB24
K27	VSS[54]	AB27
K28	VSS[55]	AB28
L13	VSS[56]	AC2
L15	VSS[57]	AC5
L24	VSS[58]	AC9
L25	VSS[59]	AD5
L26	VSS[60]	AD11
M3	VSS[61]	AD3
M4	VSS[62]	AD4
M5	VSS[63]	AD7
M12	VSS[64]	AD8
M13	VSS[65]	AD14
M14	VSS[66]	AD15
M15	VSS[67]	AD19
M16	VSS[68]	AD23
M17	VSS[69]	AE2
M24	VSS[70]	AE4
M27	VSS[71]	AE8
M28	VSS[72]	AE11
N1	VSS[73]	AE13
N2	VSS[74]	AE18
N5	VSS[75]	AE21
N6	VSS[76]	AE24
N11	VSS[77]	AE25
N12	VSS[78]	AE2
N13	VSS[79]	AE4
N14	VSS[80]	AE8
N15	VSS[81]	AE11
N16	VSS[82]	AE27
N17	VSS[83]	AE28
N18	VSS[84]	AG1
N24	VSS[85]	AG3
N25	VSS[86]	AG7
N26	VSS[87]	AG11
P3	VSS[88]	AG14
P4	VSS[89]	AG17
P12	VSS[90]	AG20
P13	VSS[91]	AG25
P14	VSS[92]	AH1
P15	VSS[93]	AH3
P16	VSS[94]	AH7
P17	VSS[95]	AH12
P24	VSS[96]	AH23
P27	VSS[97]	AH27



CLK48_ICH and CLK_ICH14 EMI Mode close to ICH7-M

hexainf@hotmail.com
GRATIS - FOR FREE

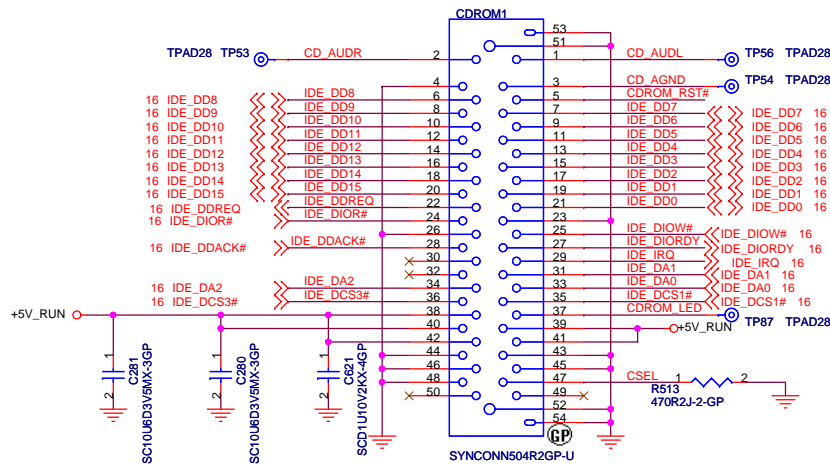
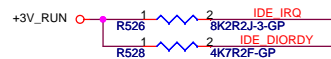
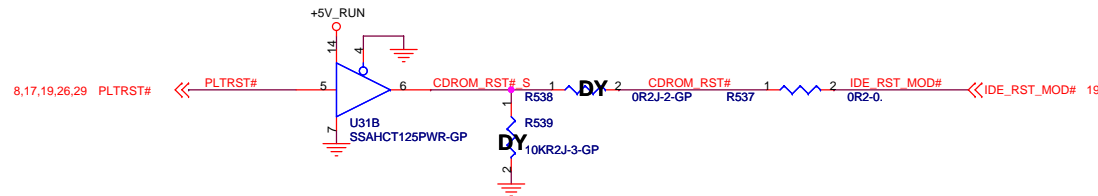
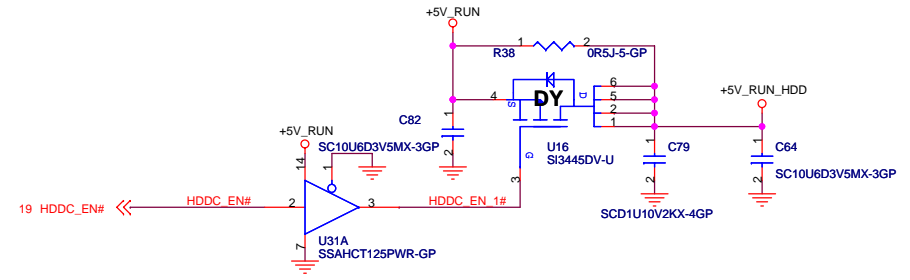
DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **ICH7-M - 04 - PM/GPIO**

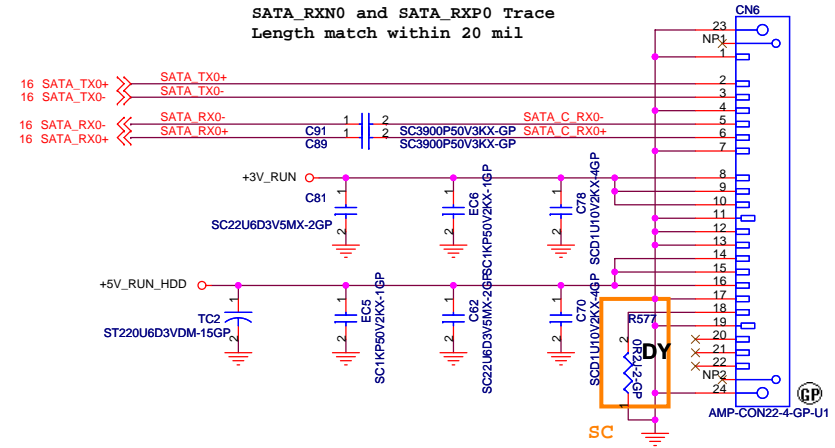
Size: A3 Document Number: **Bermuda** Rev: -1

Date: Wednesday, March 01, 2006 Sheet 19 of 45

SSID = IDE & SATA



SATA_RXN0 and SATA_RXP0 Trace
Length match within 20 mil



SATA HD Connector

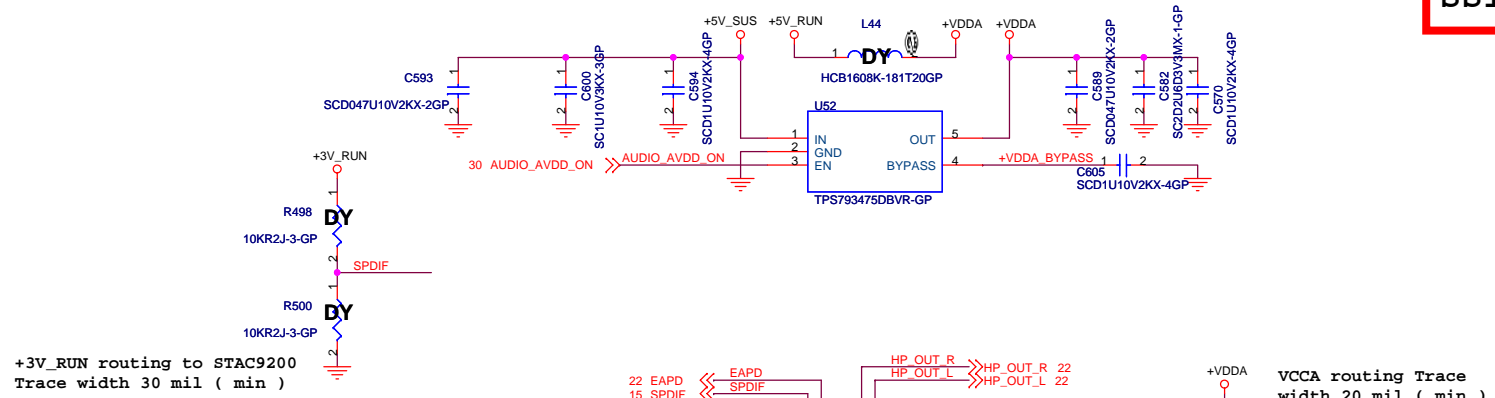
DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **SATA IDE & CD-ROM**

Size: A3 Document Number: **Bermuda** Rev: -1

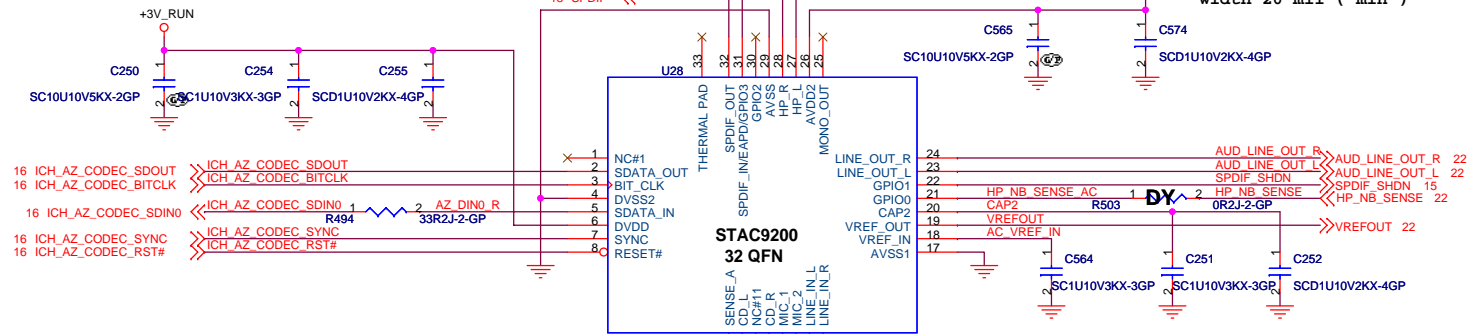
Date: Wednesday, March 01, 2006 Sheet 20 of 45

SSID = AUDIO



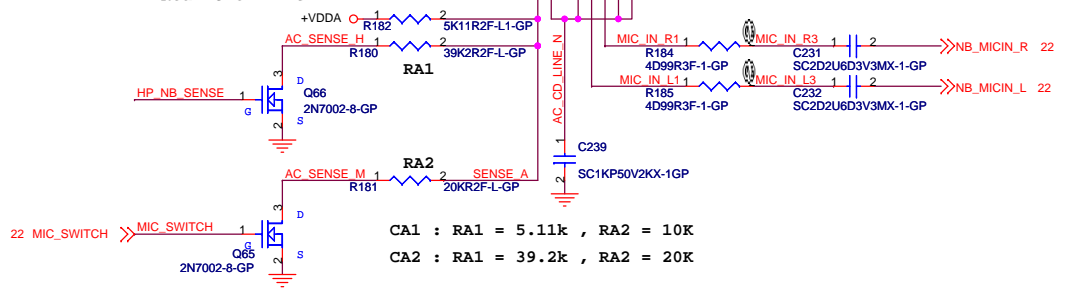
+3V_RUN routing to STAC9200
Trace width 30 mil (min)

VCCA routing Trace
width 20 mil (min)

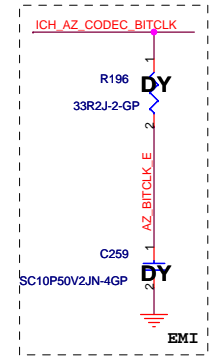


- 16 ICH_AZ_CODEC_SDOUT >> ICH_AZ_CODEC_SDOUT
- 16 ICH_AZ_CODEC_BITCLK >> ICH_AZ_CODEC_BITCLK
- 16 ICH_AZ_CODEC_SDINO >> ICH_AZ_CODEC_SDINO
- 16 ICH_AZ_CODEC_SYNC >> ICH_AZ_CODEC_SYNC
- 16 ICH_AZ_CODEC_RST# >> ICH_AZ_CODEC_RST#

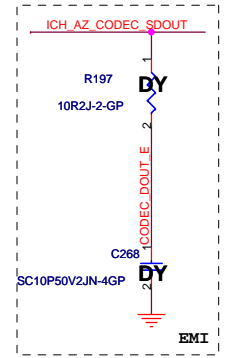
R180,R181,R182 Please
Near U28 Pin 9



CA1 : RA1 = 5.11k , RA2 = 10K
CA2 : RA1 = 39.2k , RA2 = 20K



AZ_BITCLK EMI Mode
close to ICH7-M



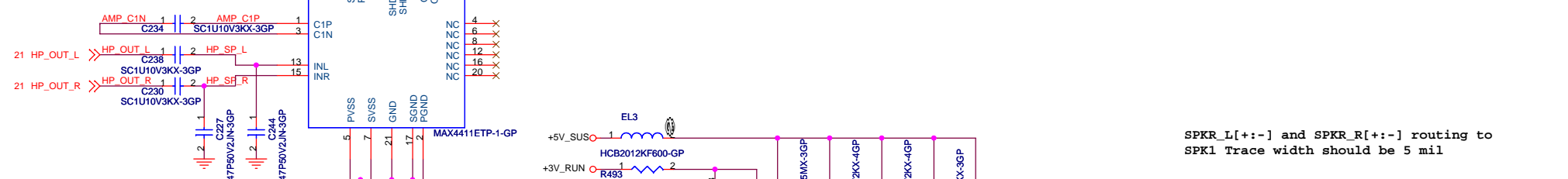
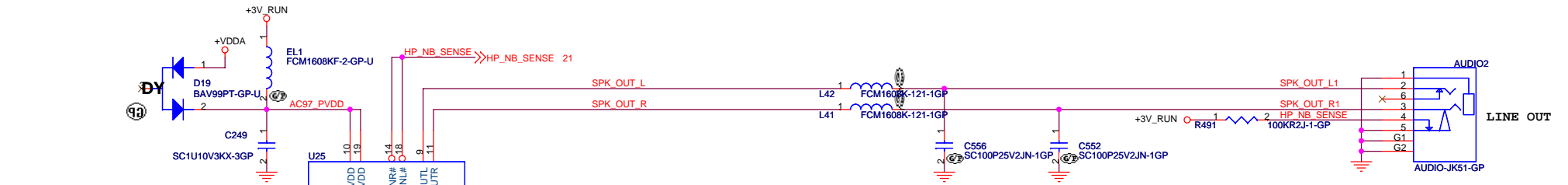
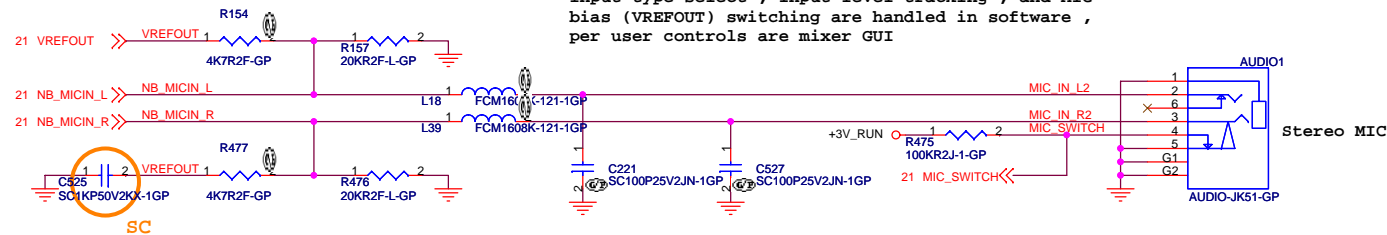
CODEC_DOUT EMI Mode
close to ICH7-M

HD audio port presence detect .Transistors are not required
if jacks implement isolated, normally open switches

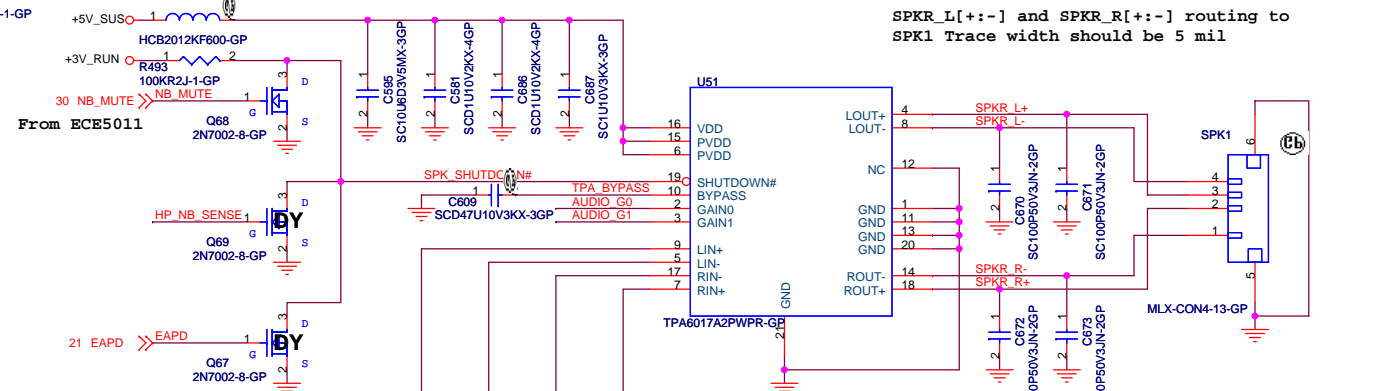
SSID = AUDIO

NOTE :

Input type select , input level tracking , and MIC bias (VREFOUT) switching are handled in software , per user controls are mixer GUI

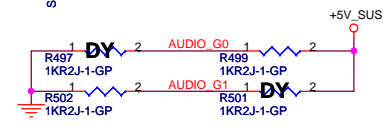


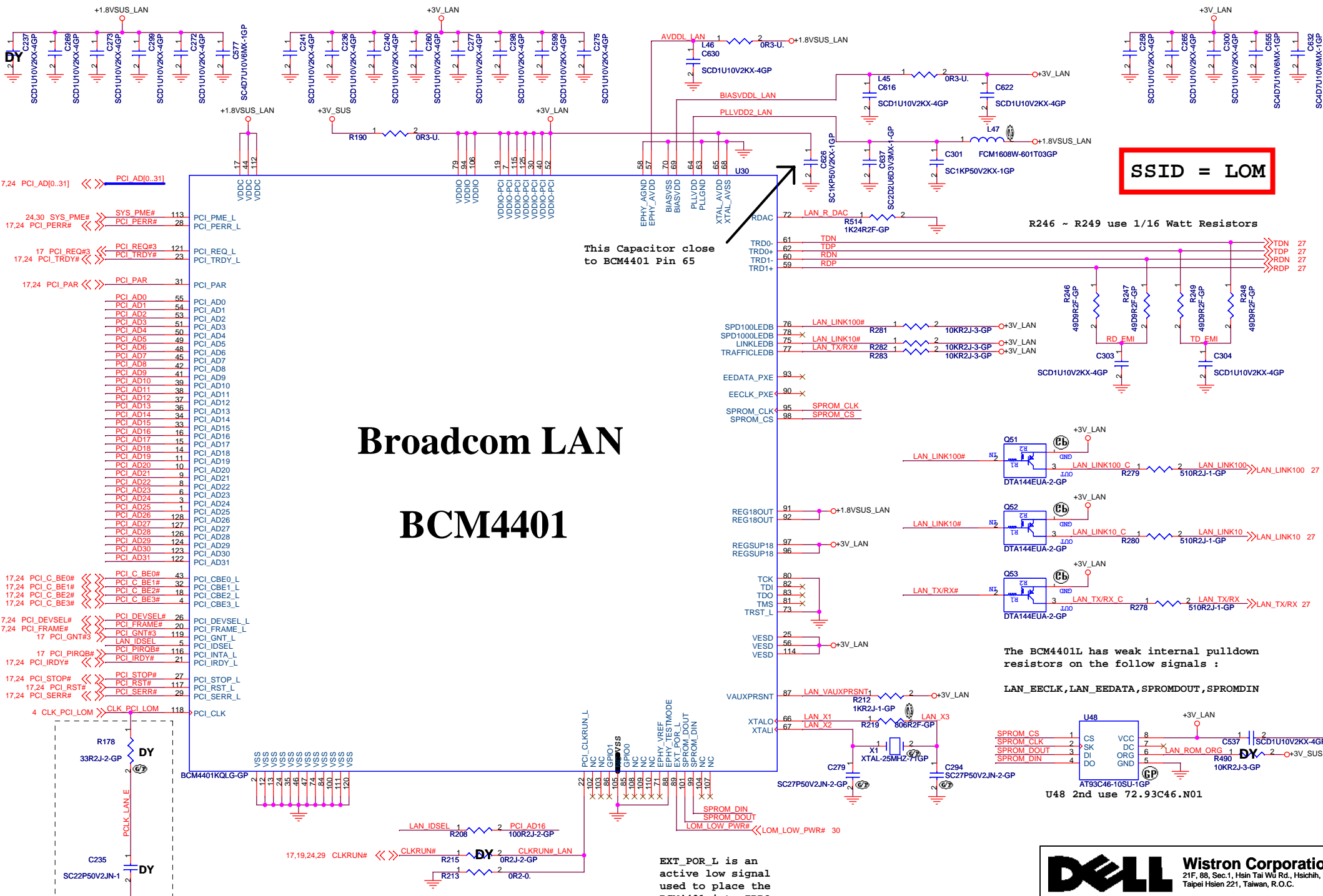
SPKR_L[+:-] and SPKR_R[+:-] routing to SPK1 Trace width should be 5 mil



Gain Setting

AV	GAIN0	GAIN1
6dB	0	0
10dB	0	1
15.6dB	1	0
21.6dB	1	1





Broadcom LAN BCM4401

SSID = LOM

This Capacitor close to BCM4401 Pin 65

R246 ~ R249 use 1/16 Watt Resistors

The BCM4401L has weak internal pulldown resistors on the follow signals :
LAN_EECLK, LAN_EEDATA, SPROMDOUT, SPROMDIN

EXT_POR_L is an active low signal used to place the BCM4401 into IDDQ mode, <5 mA current consumption

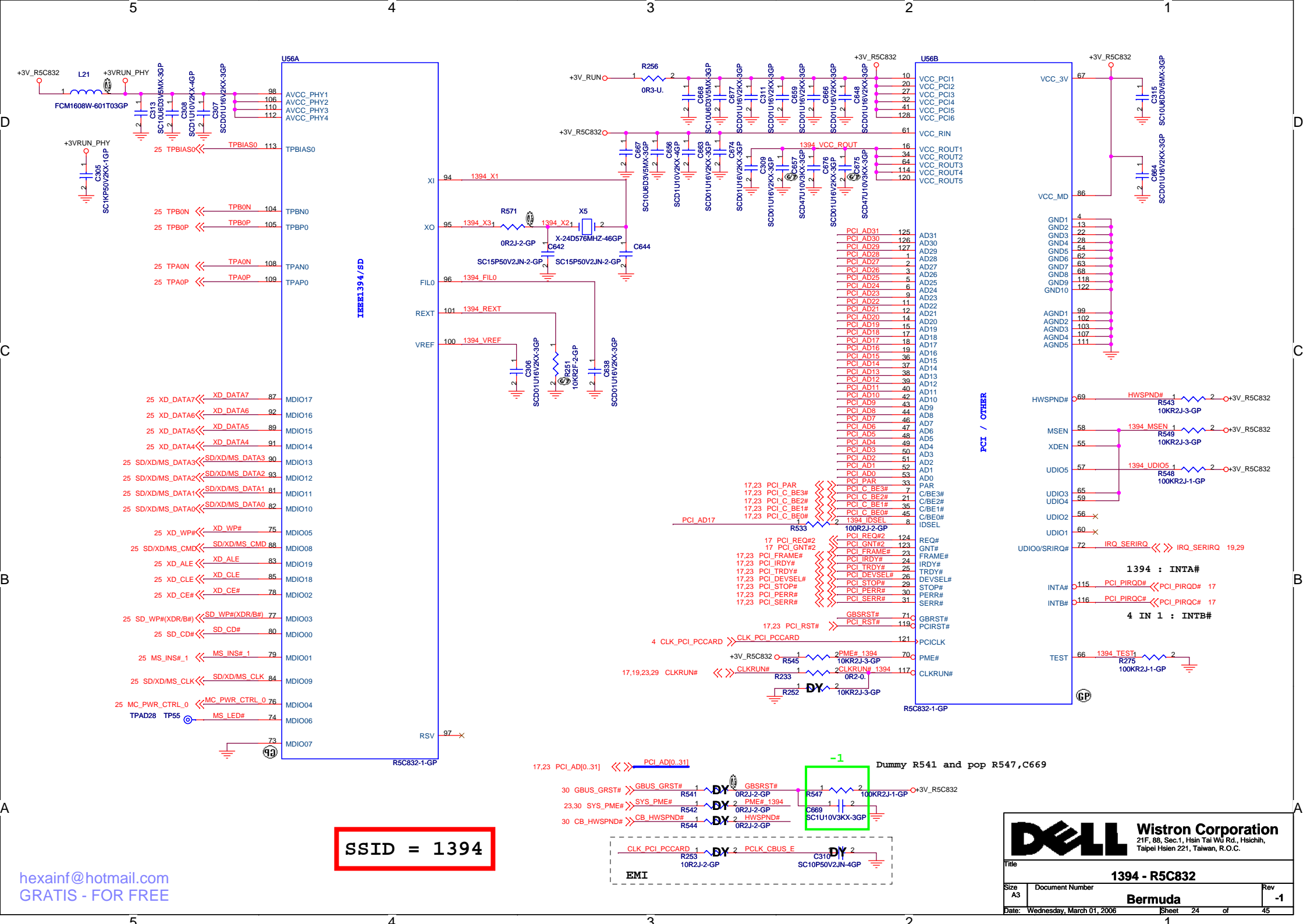
DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN - BCM4401**

Size: A3 Document Number: **Bermuda** Rev: -1

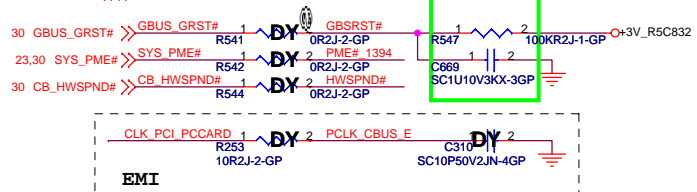
Date: Wednesday, March 01, 2006 Sheet: 23 of 45

hexainf@hotmail.com
GRATIS - FOR FREE



SSID = 1394

17,23 PCI_AD[0..31] <<<> PCI_AD[0..31] Dummy R541 and pop R547, C669



hexainf@hotmail.com
GRATIS - FOR FREE

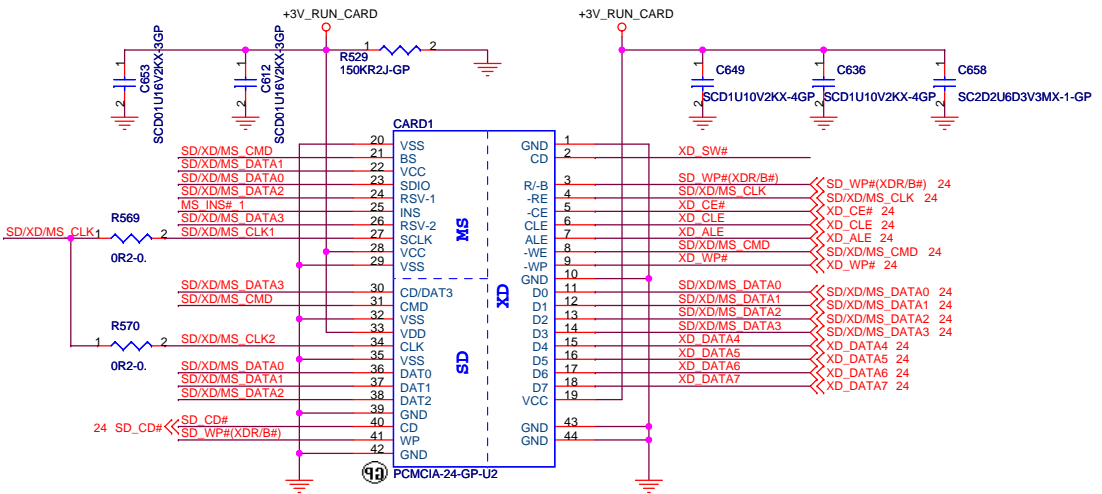
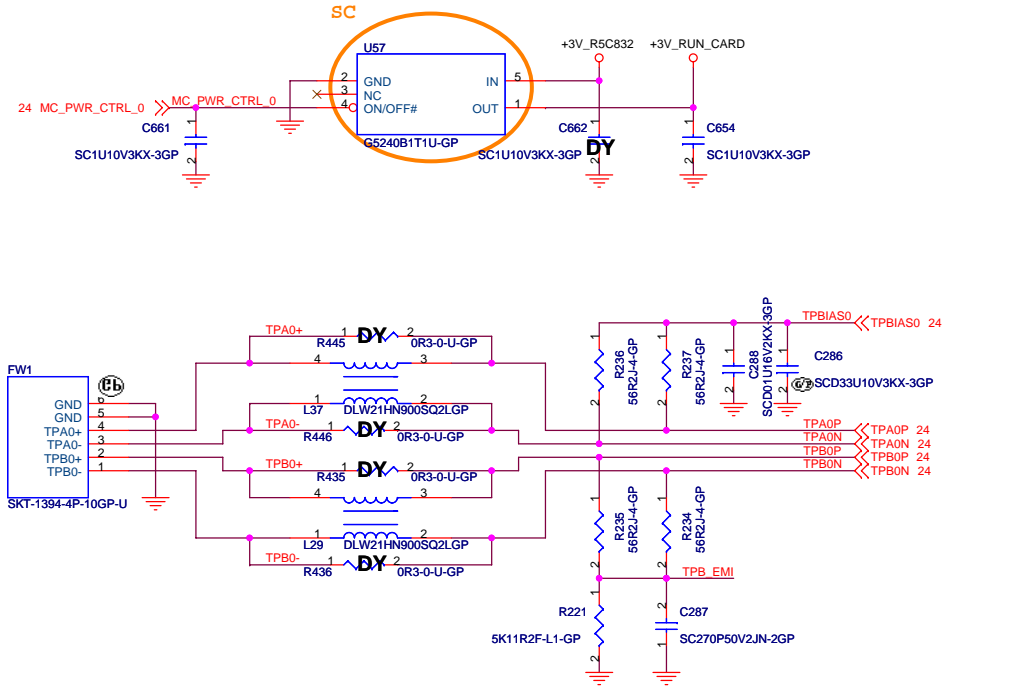
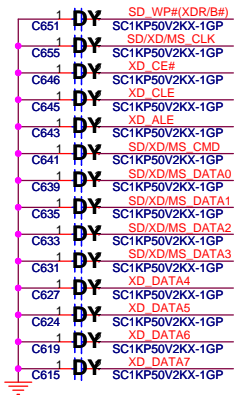
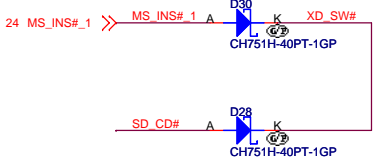
DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
1394 - R5C832

Size A3 Document Number **Bermuda** Rev -1

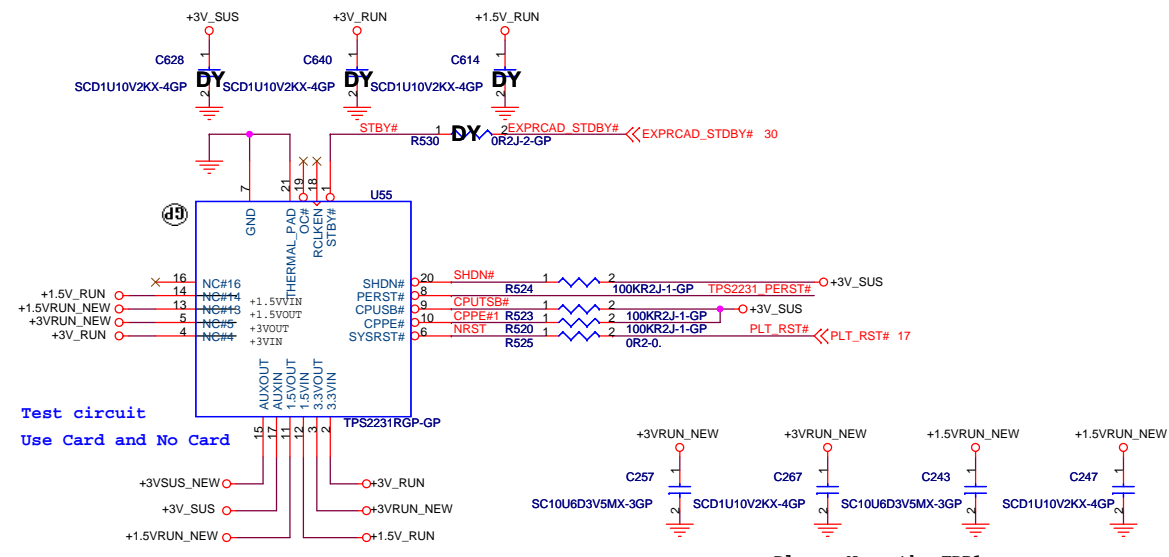
Date: Wednesday, March 01, 2006 Sheet 24 of 45

SSID = 1394

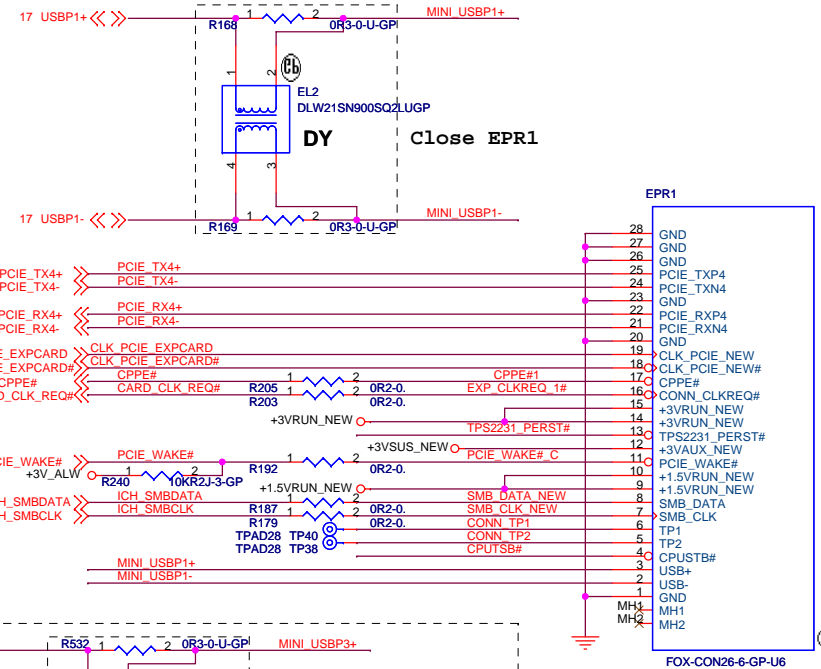


Title		
1394 - 4 IN 1 Connector		
Size	Document Number	Rev
A3	Bermuda	-1
Date:	Wednesday, March 01, 2006	Sheet 25 of 45

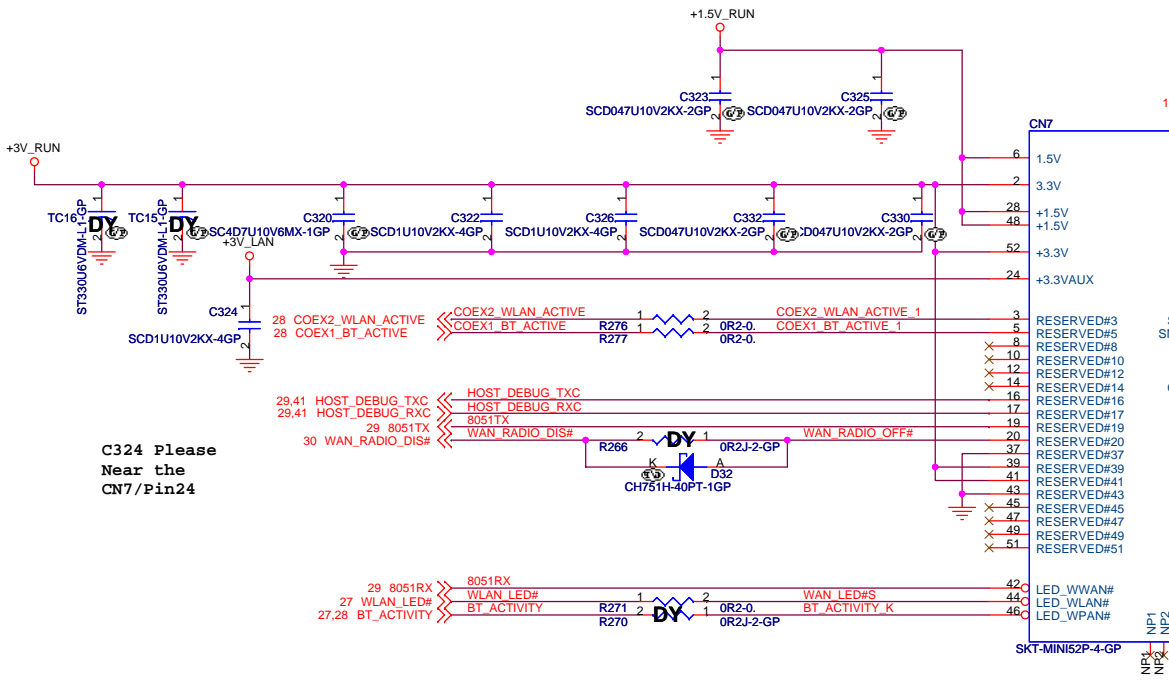
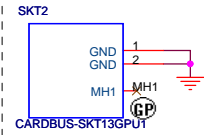
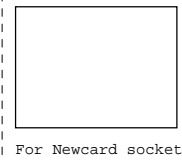
Please Near the U55



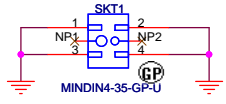
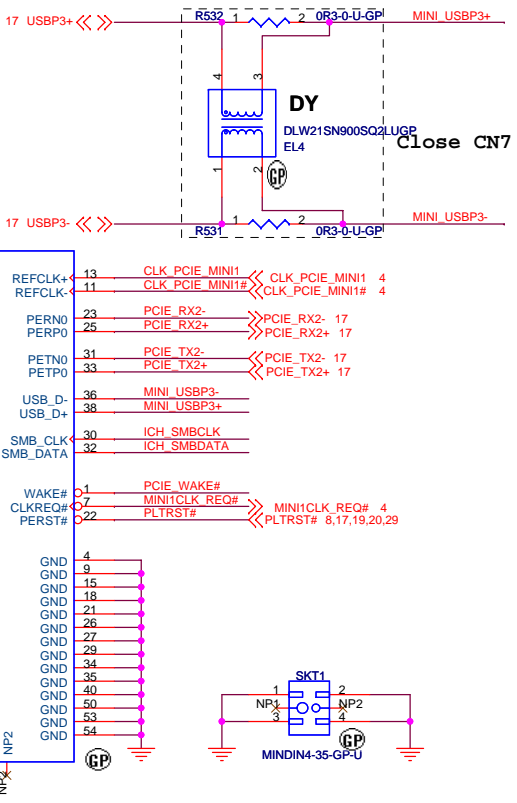
Please Near the EPR1



Geometry : 102003-6



C324 Please Near the CN7/Pin24



hexainf@hotmail.com
GRATIS - FOR FREE

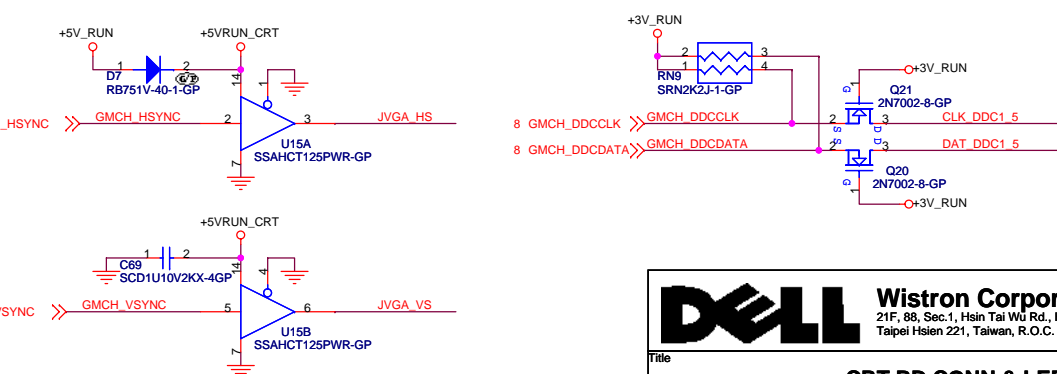
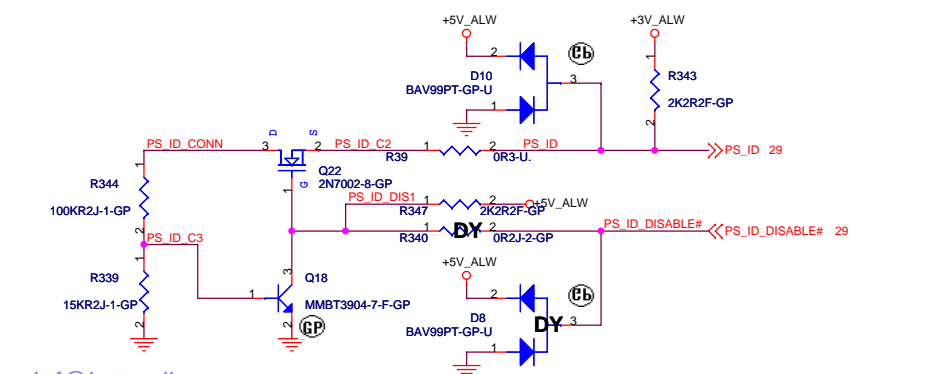
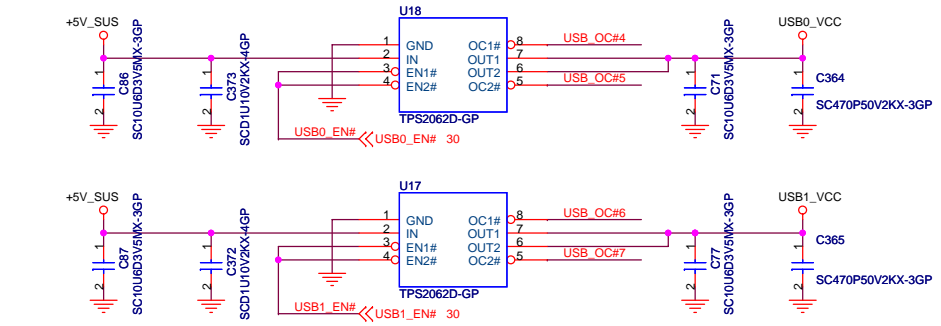
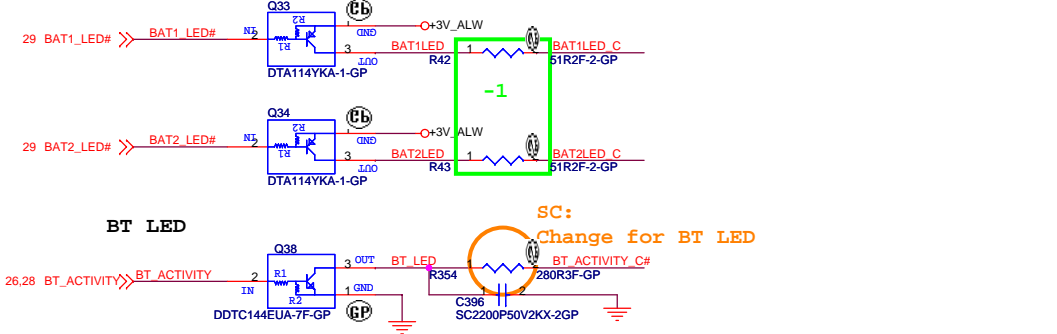
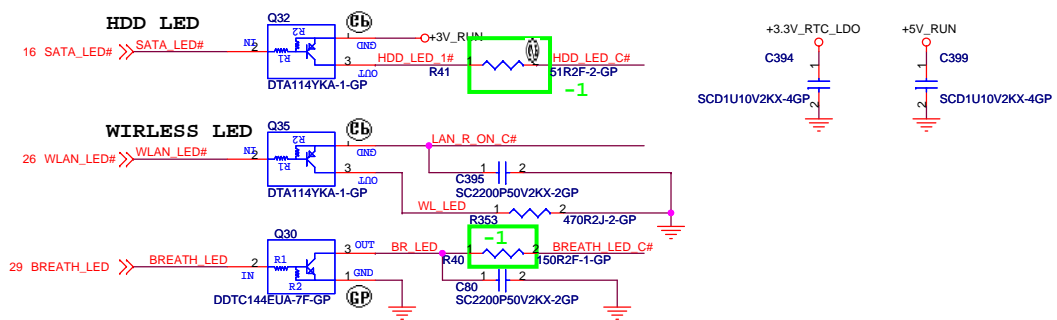
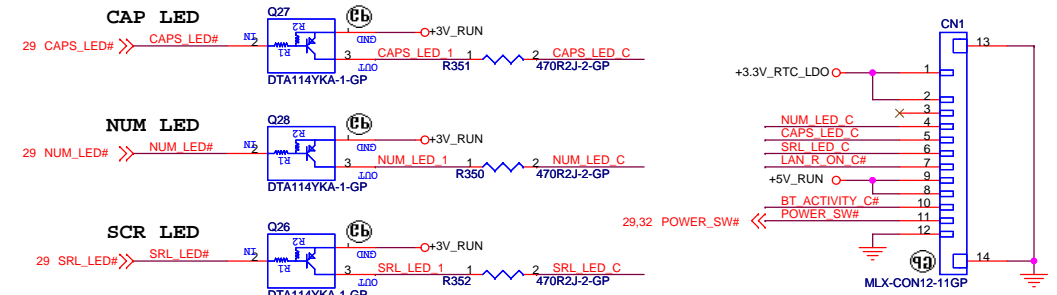
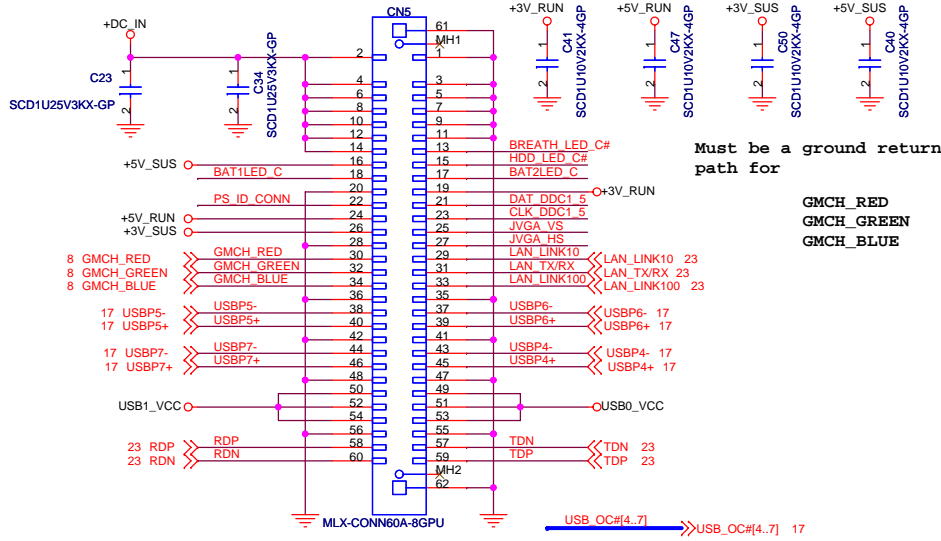
DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **EXPRESS CARD & MINICARD**

Size A3 Document Number: **Bermuda** Rev -1

Date: Wednesday, March 01, 2006 Sheet 26 of 45

CRT BD Conn



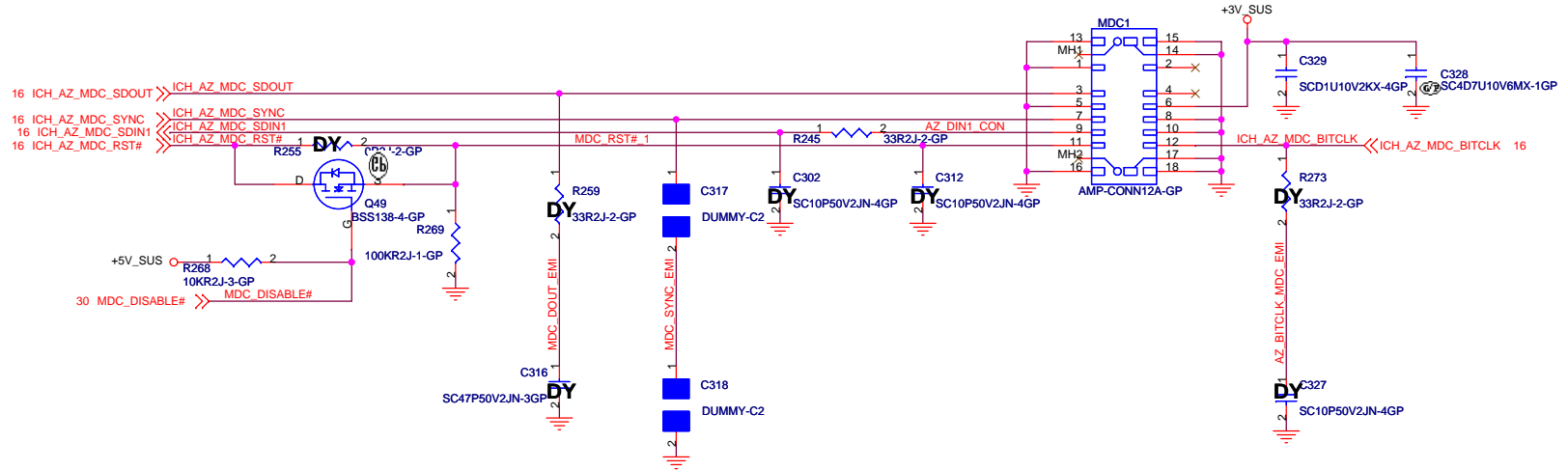
DELL Wistron Corporation
21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **CRT BD CONN & LED**

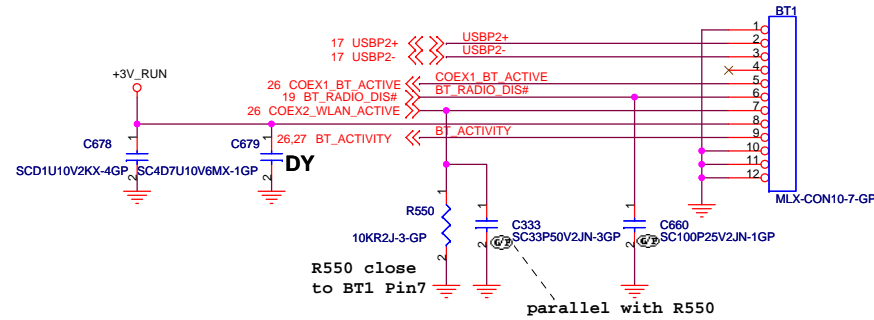
Size A3 Document Number: **Bermuda** Rev: **-1**

Date: Wednesday, March 01, 2006 Sheet 27 of 45

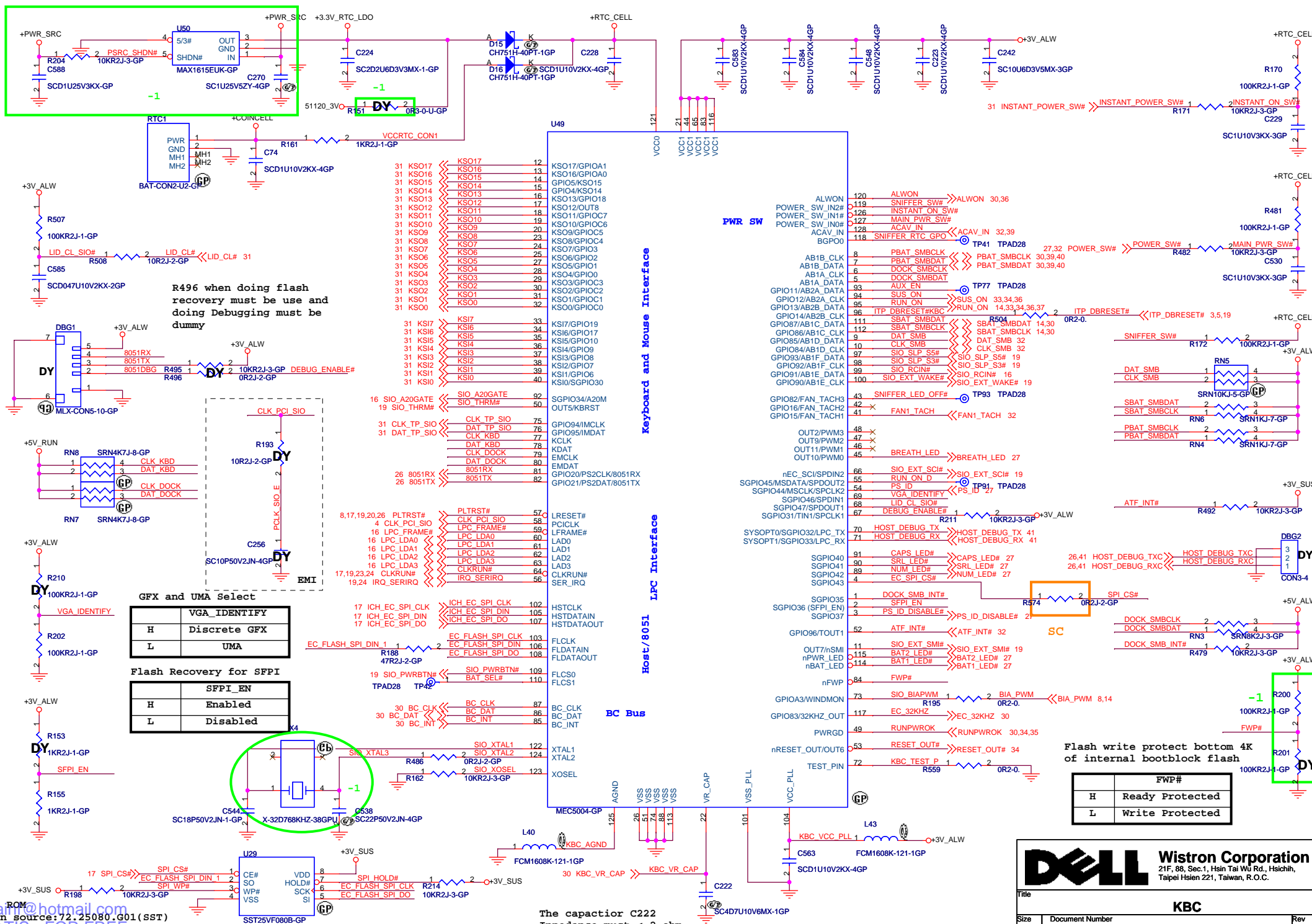
Modem Connector (Not Standard Type)



Bluetooth Module conn.



DELL		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: MDC & BT			
Size: A3	Document Number: Bermuda	Rev: -1	
Date: Wednesday, March 01, 2006			
Sheet 28 of 45			



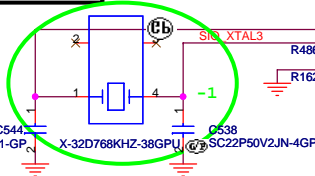
R496 when doing flash recovery must be use and doing Debugging must be dummy

GFX and UMA Select

VGA_IDENTIFY	
H	Discrete GFX
L	UMA

Flash Recovery for SFPI

SFPI_EN	
H	Enabled
L	Disabled



The capacitor C222 Impedance must < 2 ohm

Flash write protect bottom 4K of internal bootblock flash

FWP#	
H	Ready Protected
L	Write Protected

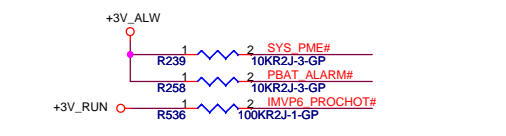
SPI ROM
Main source : 72.25080.G01 (SST)
2nd source : 72.250805.001 (MXIC)

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

KBC

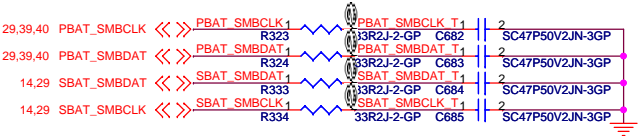
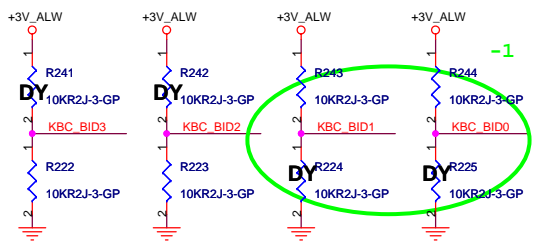
Size A3 Document Number **Bermuda** Rev -1

Date: Friday, March 10, 2006 Sheet 29 of 45

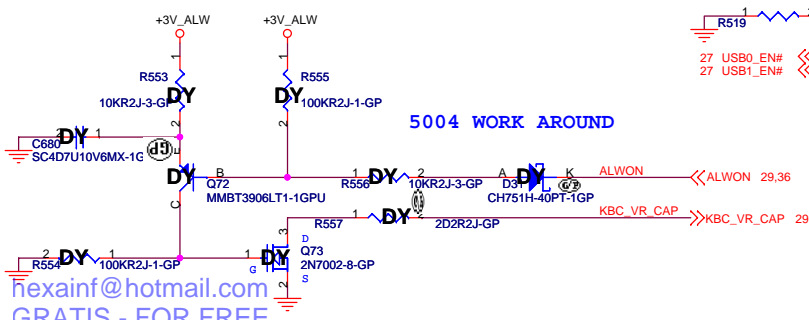
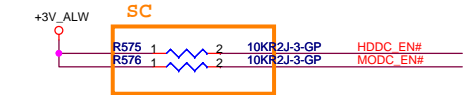


Board ID Strap

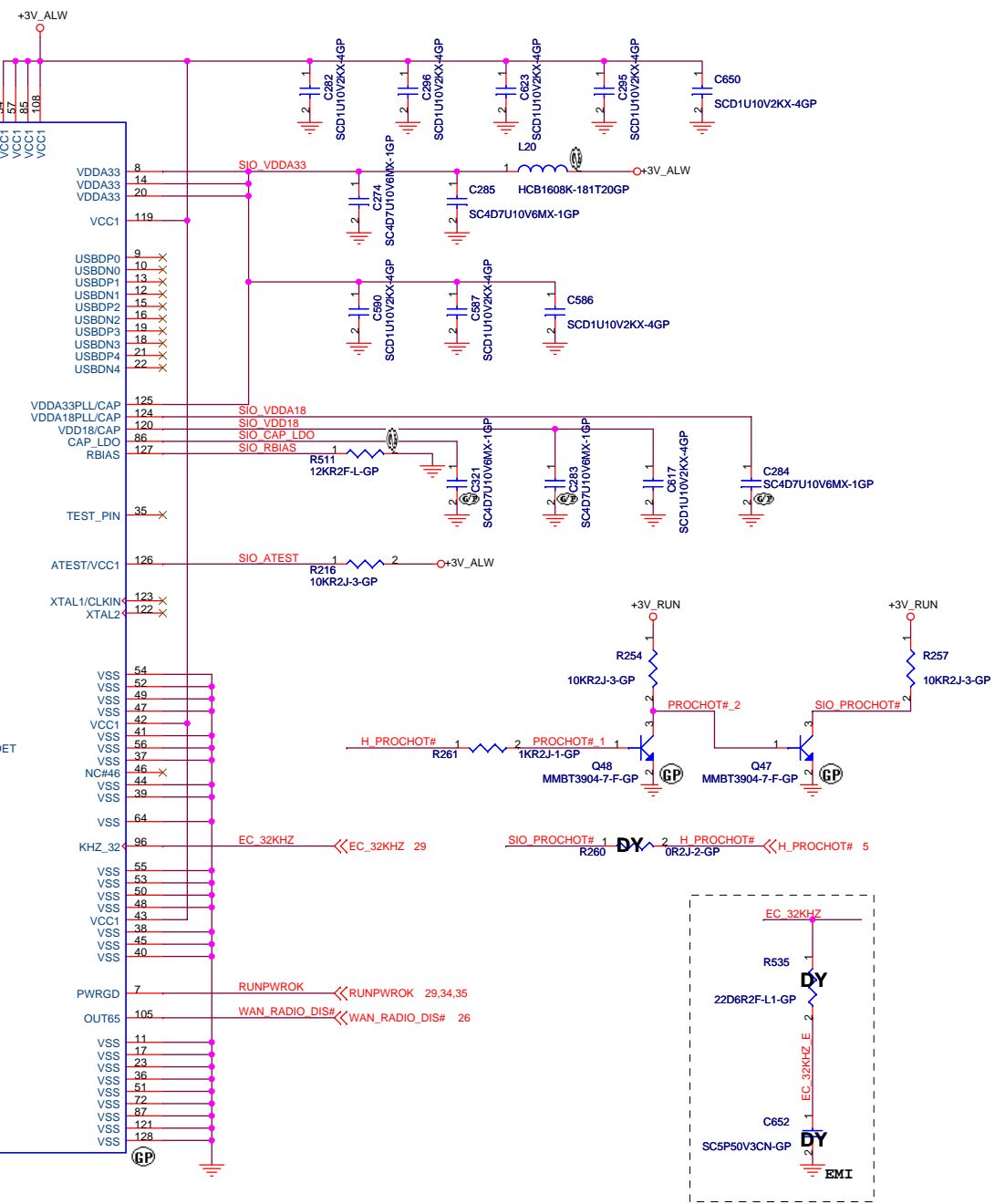
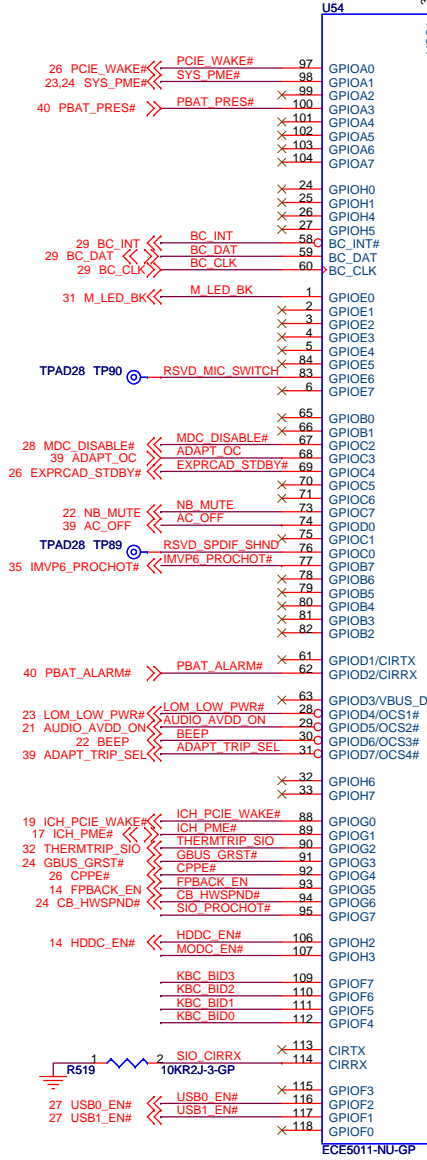
REV	KBC_BID0	KBC_BID1	KBC_BID2	KBC_BID3
X00	0	0	0	0
X01	1	0	0	0
X02	0	1	0	0
X03	1	1	0	0
X04	0	0	1	0



PLEASE NEAR KBC



hexainf@hotmail.com
GRATIS - FOR FREE

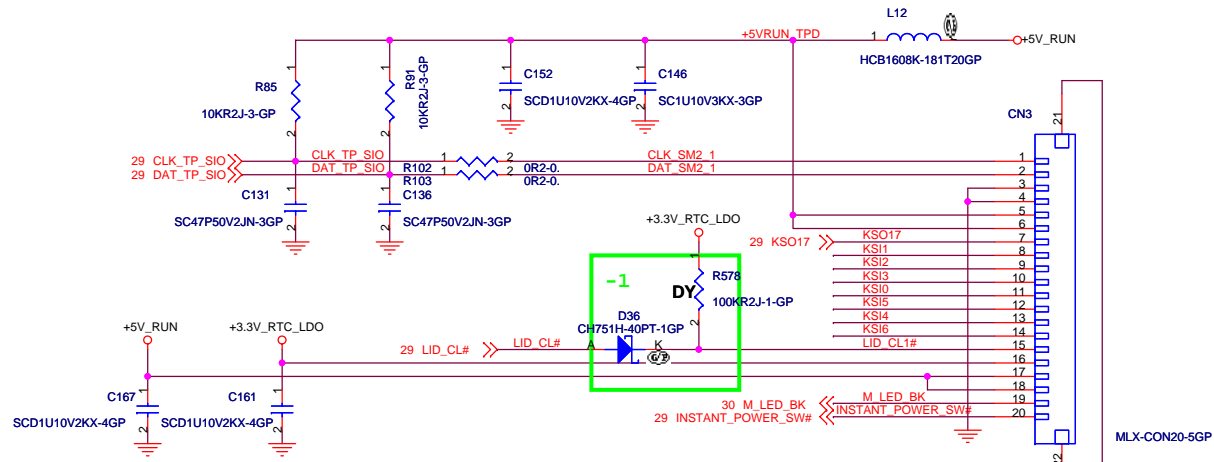


DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **SIO**

Size: A3 Document Number: **Bermuda** Rev: -1

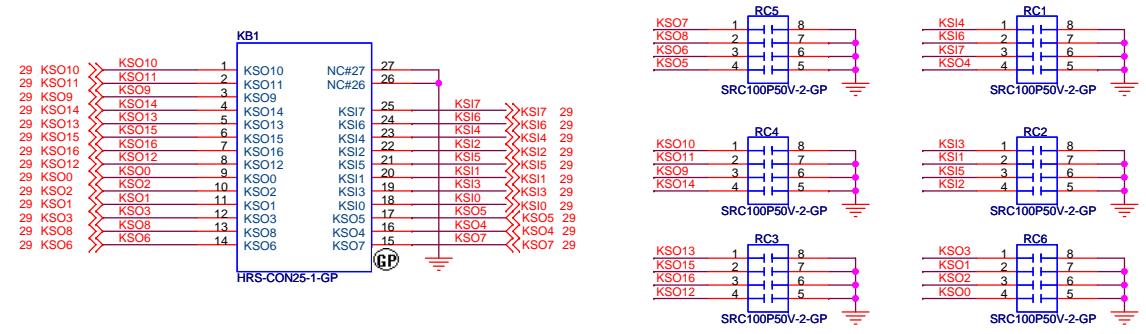
Date: Wednesday, March 01, 2006 Sheet: 30 of 45



INSTANT POWER Select

	INSTANT_POWER_SW#
H	Power On Function
L	Regular Play Function

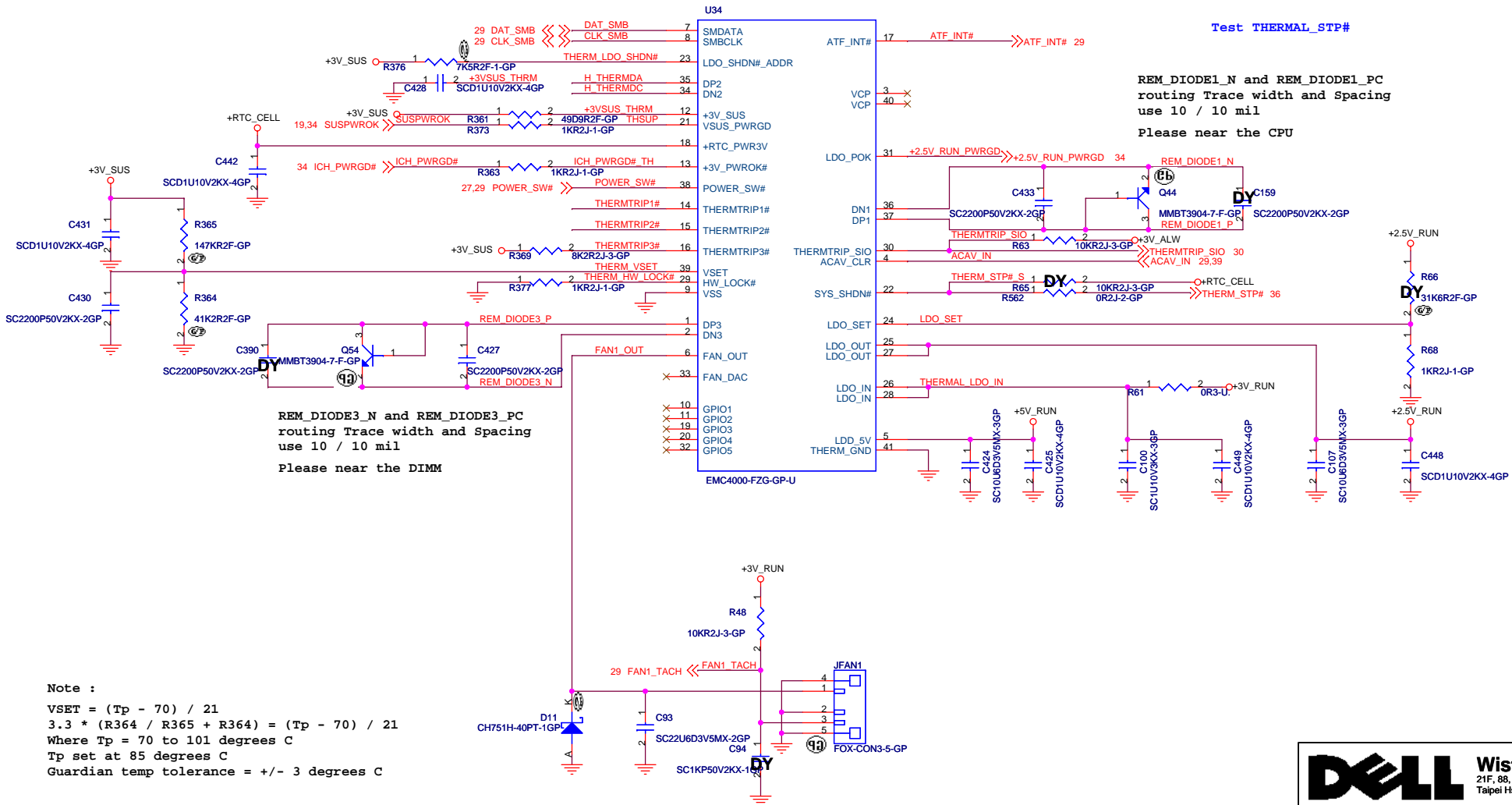
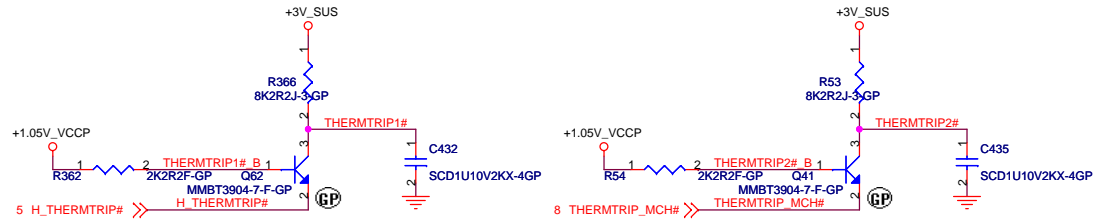
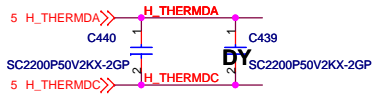
Media PlayBack / TouchPAD Connector



SSID = THERMAL

H_THERMDA and H_THERMDC routing Trace width and Spacing use 10 / 10 mil

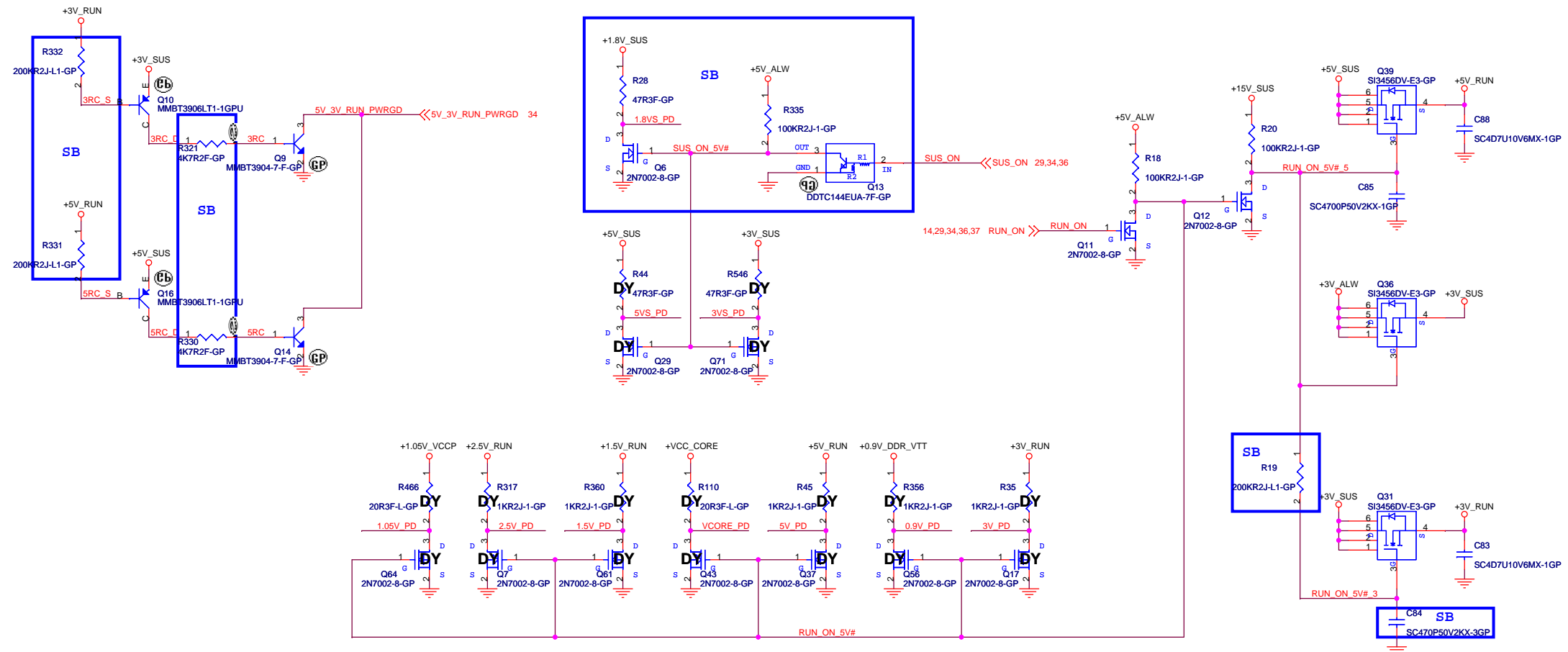
Reserve area near CPU for a cap between DP2/DN2

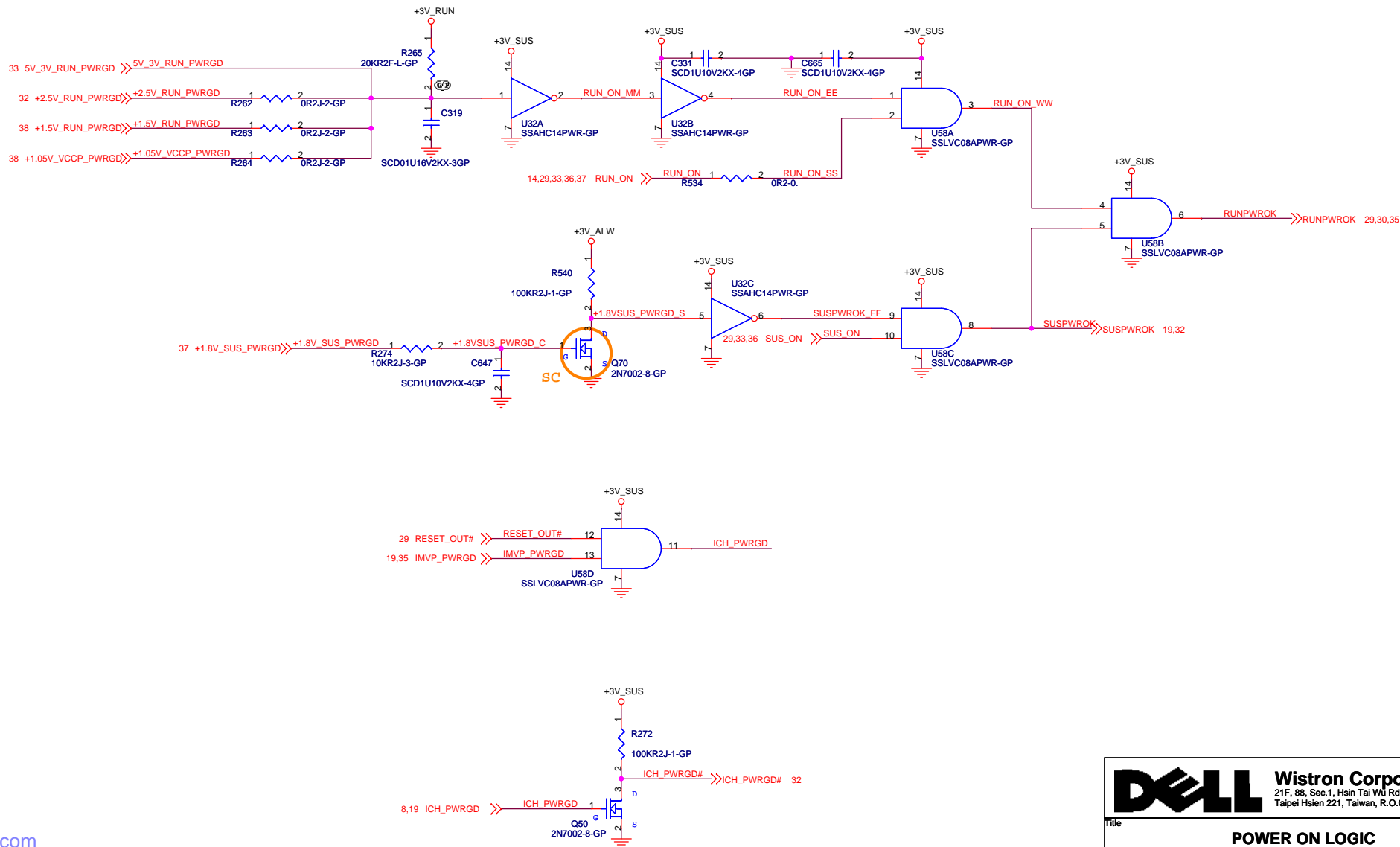


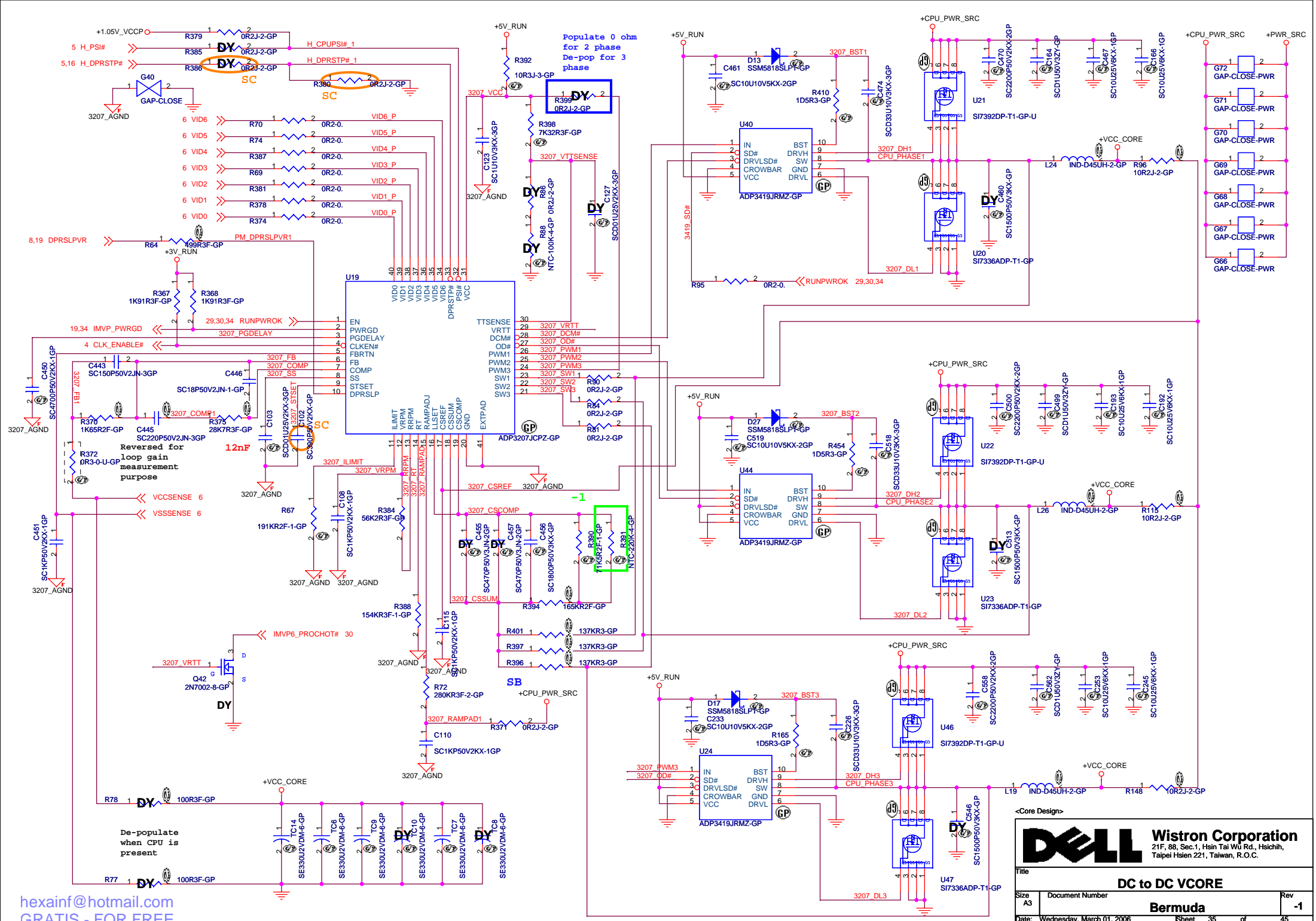
REM_DIODE3_N and REM_DIODE3_PC routing Trace width and Spacing use 10 / 10 mil
Please near the DIMM

Test THERMAL_STP#
REM_DIODE1_N and REM_DIODE1_PC routing Trace width and Spacing use 10 / 10 mil
Please near the CPU

Note :
 $VSET = (T_p - 70) / 21$
 $3.3 * (R364 / R365 + R364) = (T_p - 70) / 21$
 Where $T_p = 70$ to 101 degrees C
 T_p set at 85 degrees C
 Guardian temp tolerance = +/- 3 degrees C







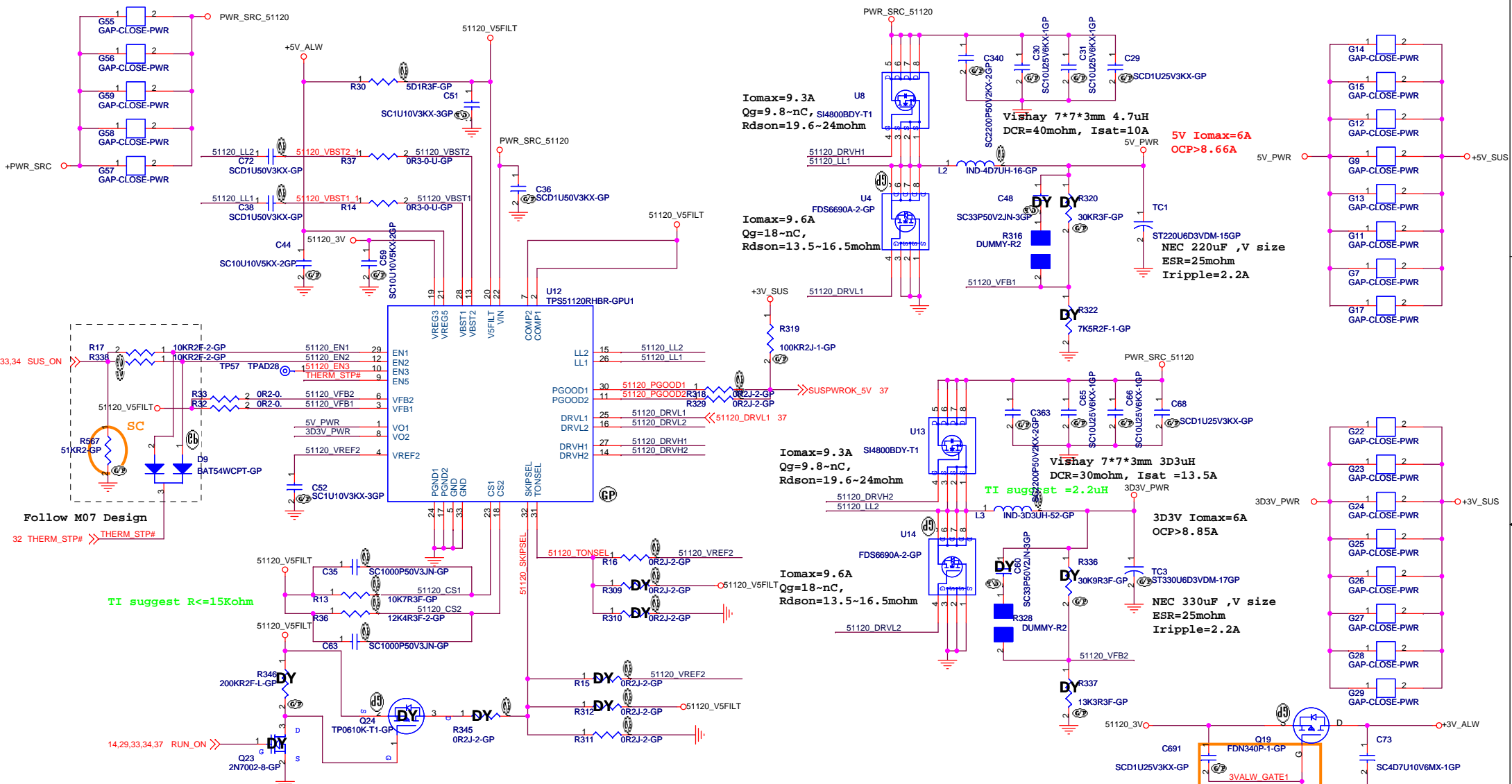
hexainf@hotmail.com
GRATIS - FOR FREE

<Core Design>

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

DC to DC Vcore

Title	Document Number	Rev
Size A3		-1
Date: Wednesday, March 01, 2006	Sheet 35 of 45	



Follow M07 Design

TI suggest R<=15Kohm

$$V_{out} = 1V \cdot (R1 + R2) / R2$$

For TPS51120,
 $V_{out} = 5V$

1. If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
2. If you use a 4.7uH inductor, the minimum ESR is 48m ohm.
3. If you use a 3.3uH inductor, the minimum ESR is 34m ohm.

$V_{out} = 3.3V$

1. If you use a 4.7uH inductor, the minimum ESR is 51m ohm.
2. If you use a 3.3uH inductor, the minimum ESR is 36m ohm.
3. If you use a 2.5uH inductor, the minimum ESR is 27m ohm.

	GND	VREF2	FLOAT	V5FILT
SKIPSEL	AUTOSKIP	AUTOSKIP / FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	D-Cap MODE
TONSEL	380k/CH1 580k/CH2	280k/CH1 430k/CH2	220k/CH1 330k/CH2	180k/CH1 2870k/CH2
VFB1	N/A	not use	ADJ.	5V Fixed Output
VFB2	N/A	not use	ADJ.	3.3V Fixed Output
EN1, EN2	Switcher OFF	not use	Switchchr ON	Switcher ON
EN3, EN5	LDO OFF	not use	LDO ON	VREG3 on

hexainf@hotmail.com
 GET IT FOR FREE

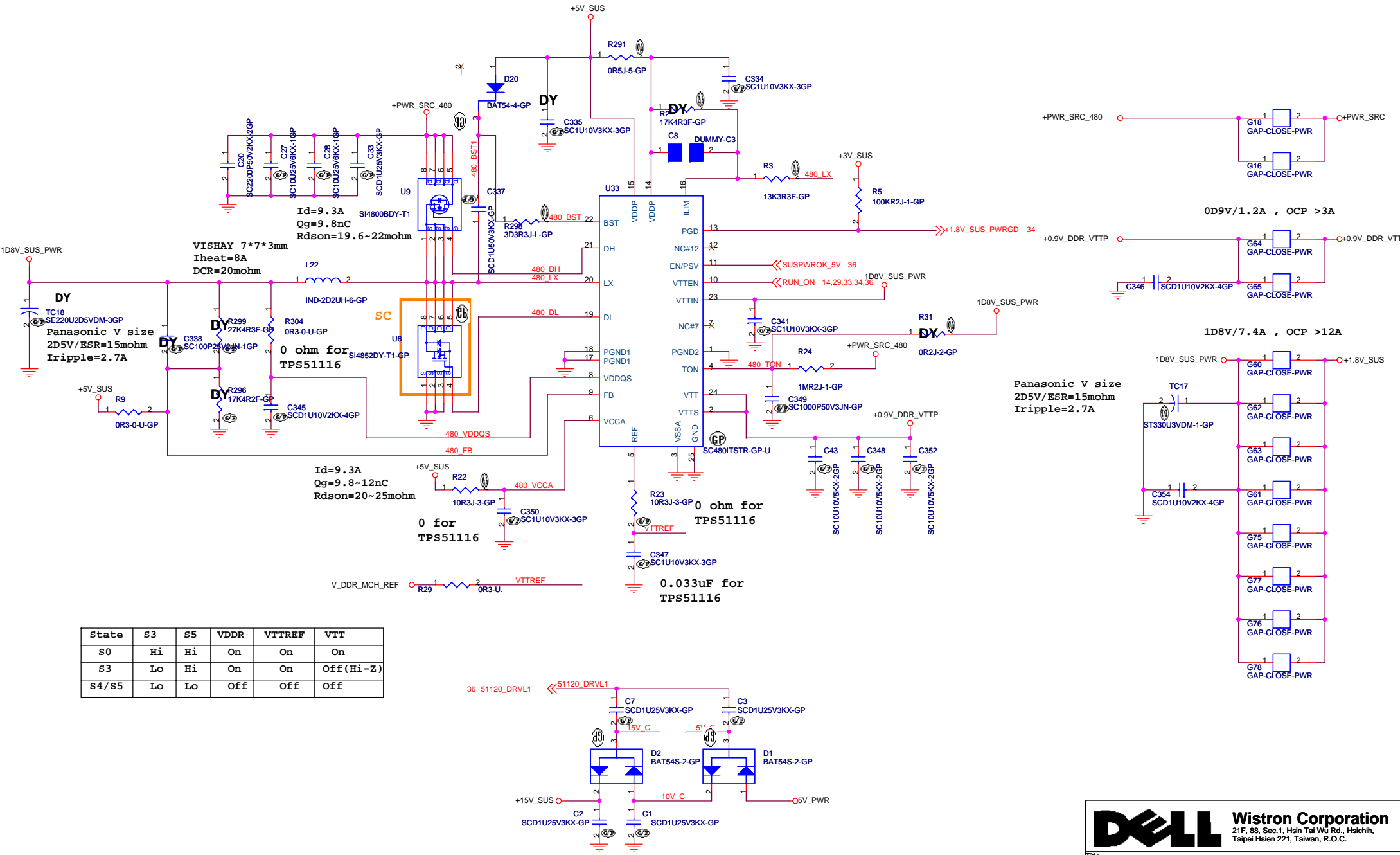
DELL Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **DC to DC 3.3V & 5V**

Size A3 Document Number **Bermuda** Rev **-1**

Date: Wednesday, March 01, 2006 Sheet 36 of 45

SC480 for 1D8V and 0D9V

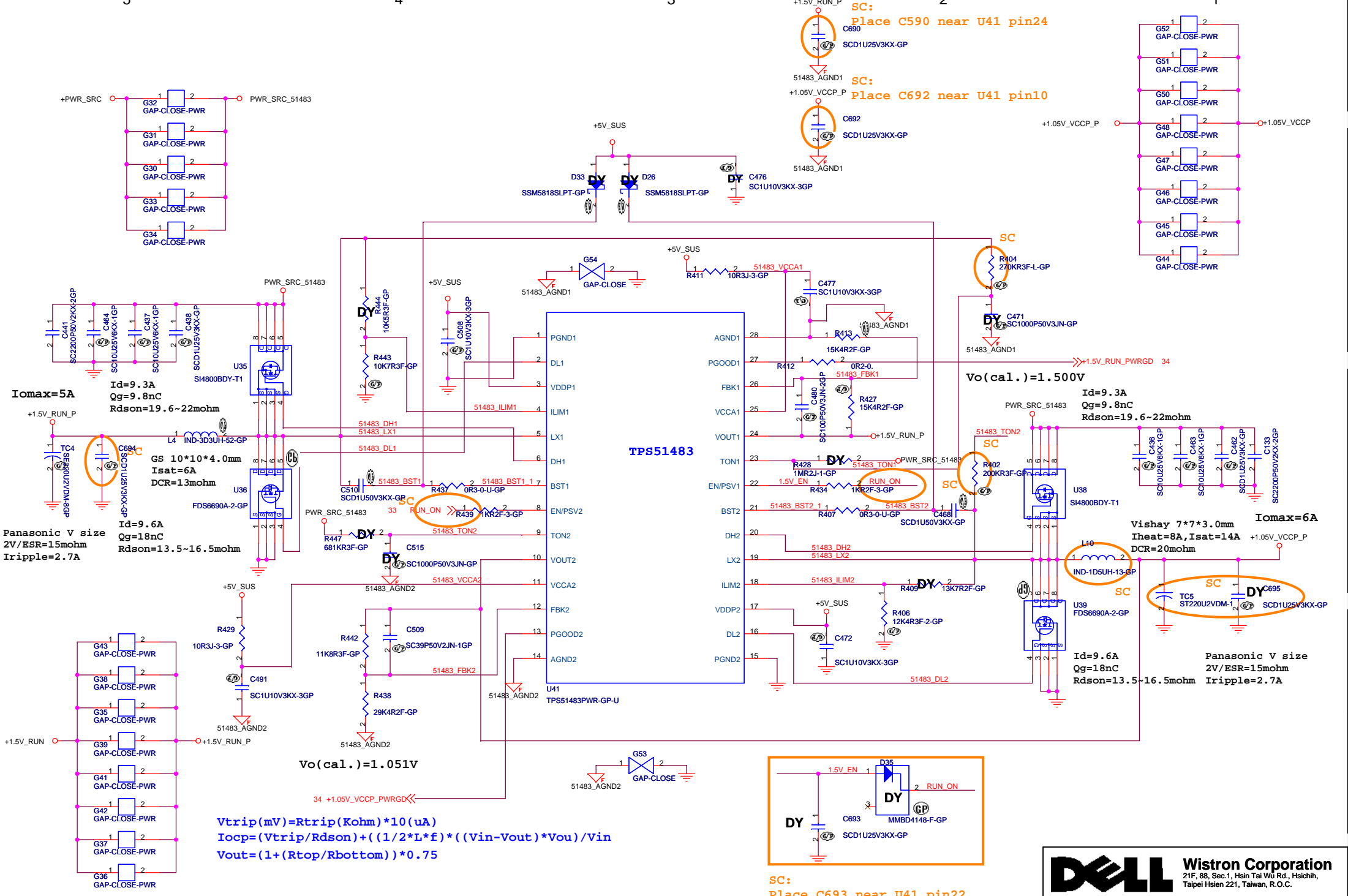


State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

Panasonic V size
2D5V/ESR=15mohm
Iripple=2.7A

0D9V/1.2A , OCP >3A

1D8V/7.4A , OCP >12A



I_omax=5A
 Id=9.3A
 Qg=9.8nC
 R_{ds(on)}=19.6~22mohm

GS 10*10*4.0mm
 Isat=6A
 DCR=13mohm

Id=9.6A
 Qg=18nC
 R_{ds(on)}=13.5~16.5mohm

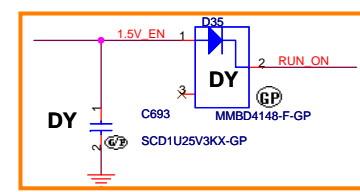
Panasonic V size
 2V/ESR=15mohm
 Tripple=2.7A

I_omax=6A
 I_{heat}=8A, Isat=14A
 DCR=20mohm

Id=9.6A
 Qg=18nC
 R_{ds(on)}=13.5~16.5mohm

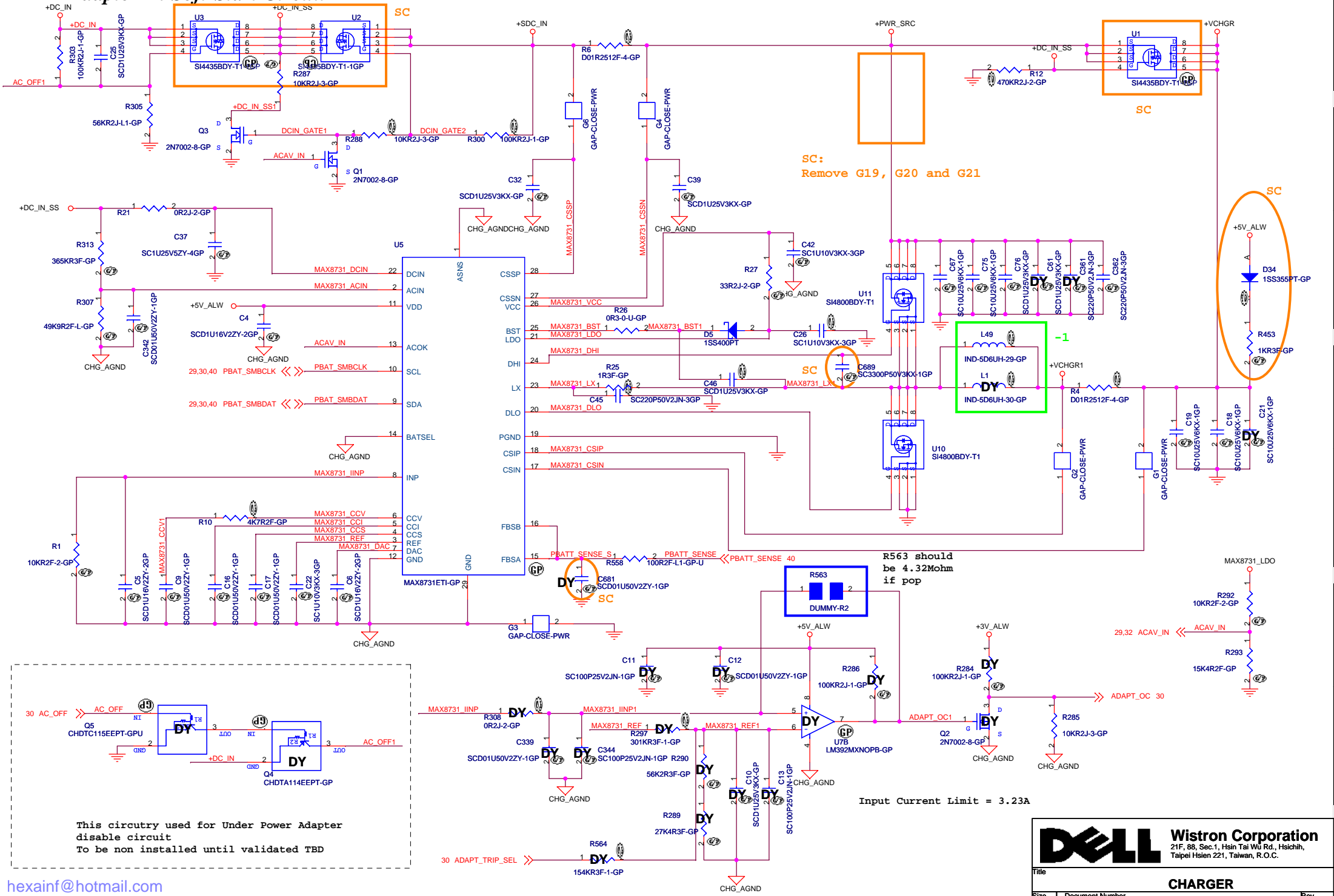
Panasonic V size
 2V/ESR=15mohm
 Tripple=2.7A

$V_{trip}(mV) = R_{trip}(Kohm) * 10(uA)$
 $I_{ocp} = (V_{trip}/R_{ds(on)}) + ((1/2 * L * f) * ((V_{in} - V_{out}) * V_{ou}) / V_{in})$
 $V_{out} = (1 + (R_{top}/R_{bottom})) * 0.75$



SC:
 Place C693 near U41 pin22

Adaptor In Soft-Start Circuit



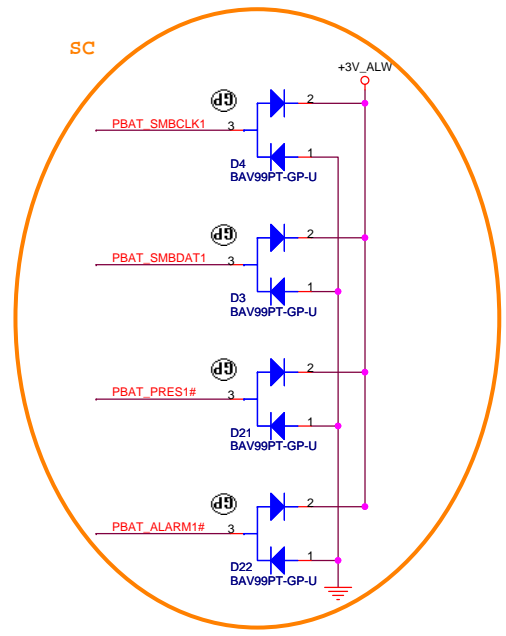
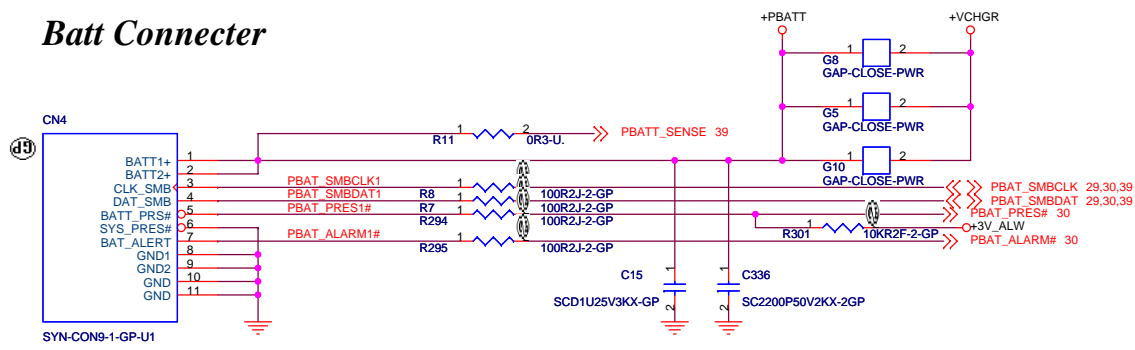
hexainf@hotmail.com
GRATIS - FOR FREE

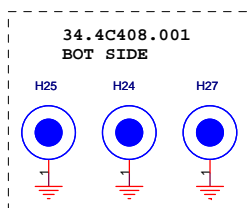
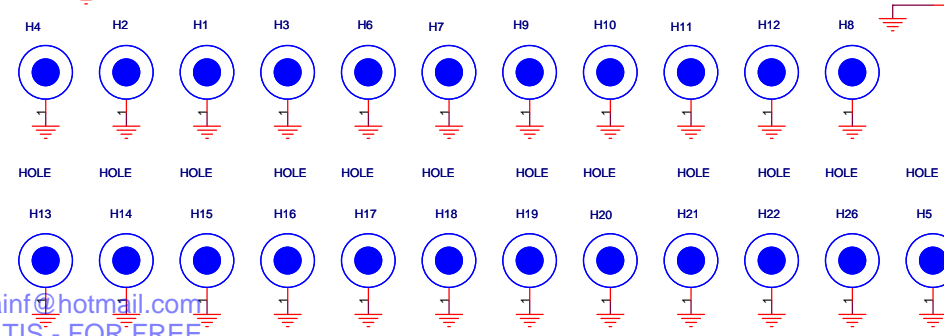
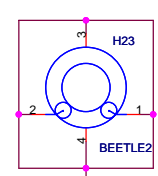
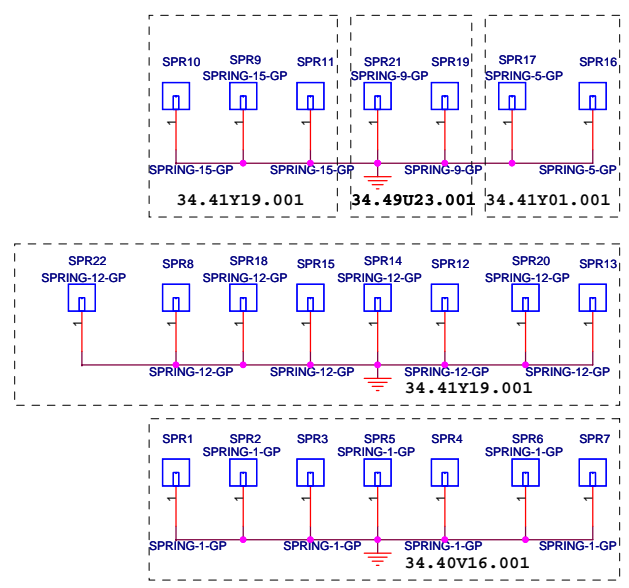
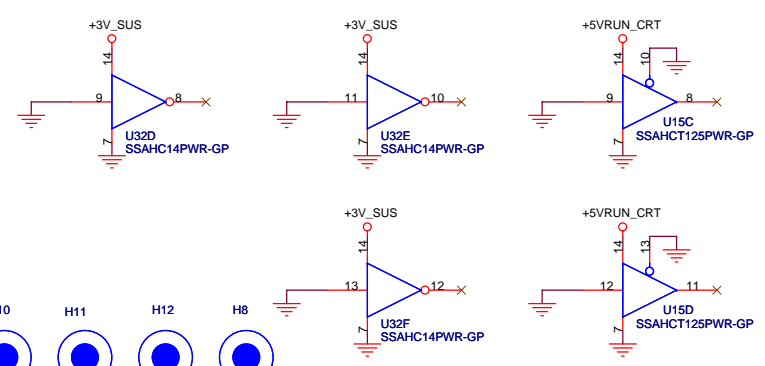
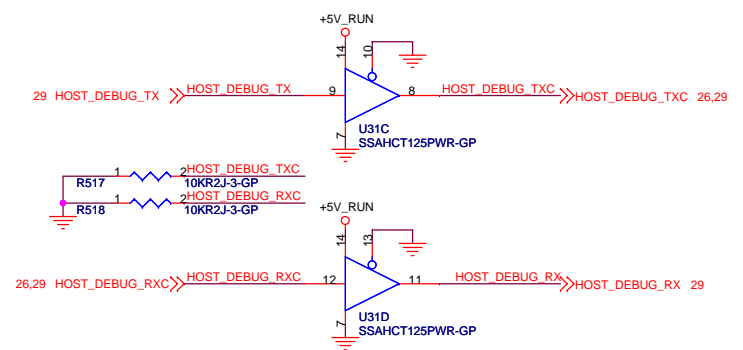
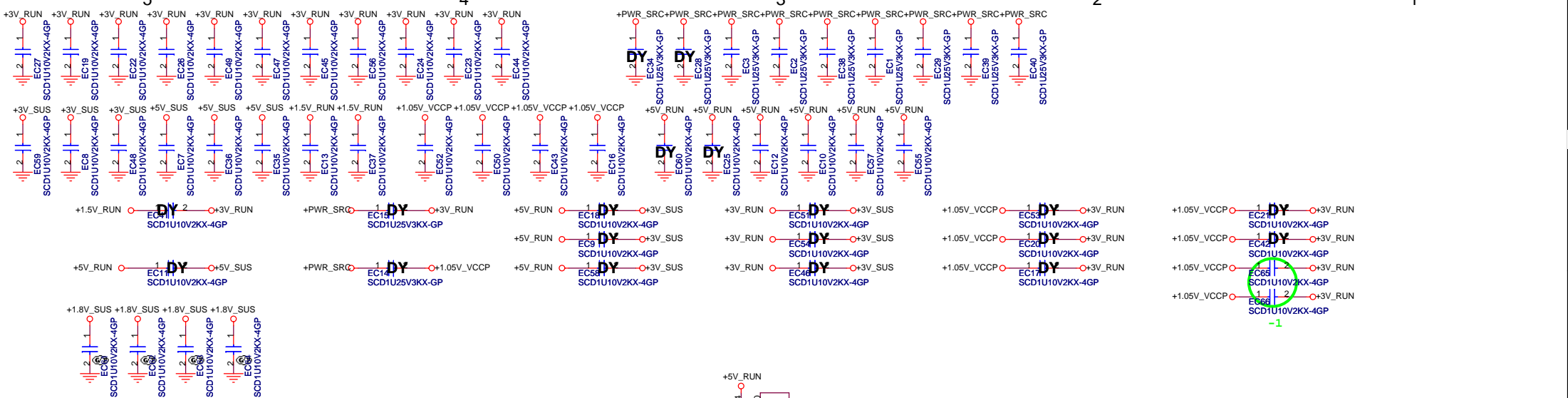
This circuitry used for Under Power Adaptor disable circuit
To be non installed until validated TBD

Input Current Limit = 3.23A

		Wistron Corporation 21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
		CHARGER	
Title	Size A3	Document Number	Rev -1
Date: Friday, March 10, 2006		Sheet 39 of 45	

Batt Connector





DELL Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

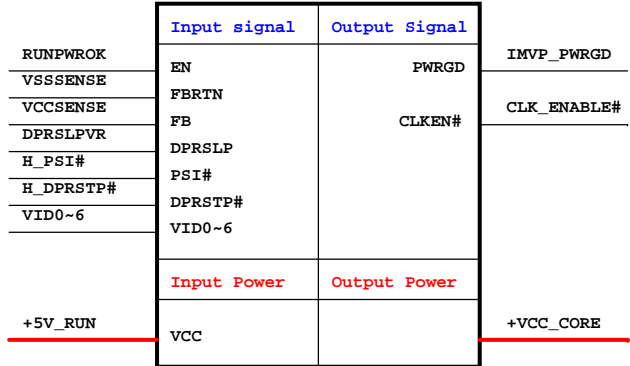
Title: **MISC & EMI**

Size: A3 Document Number: **Bermuda** Rev: **-1**

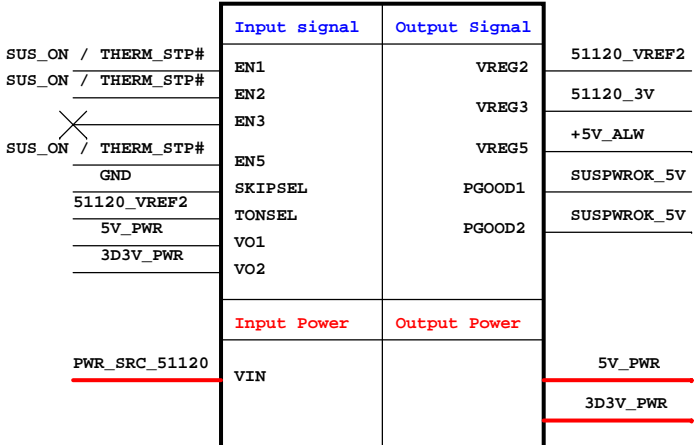
Date: Wednesday, March 01, 2006 Sheet: 41 of 45

hexainf@hotmail.com
 GRATIS - FOR FREE

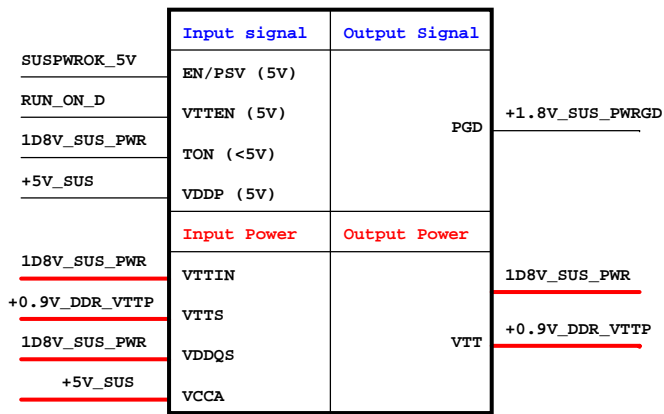
CPU_Core
ADP3207+ADP3419



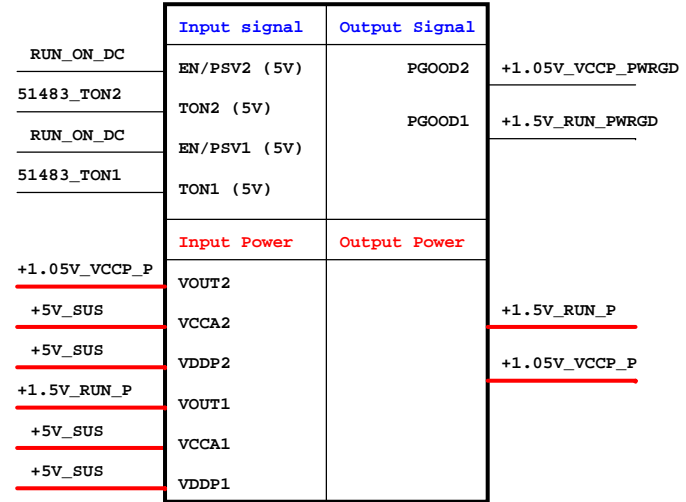
5V/3D3V
TI TPS51120



1D8V/0D9V
TPS51116



1D5V/1D05V
TI TP51483



DELL		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
POWER DIAGRAM			
Size	Document Number	Rev	
A3		-1	
Date: Wednesday, March 01, 2006		Sheet	of
		1	45

DATE	VERSION	ITEM	PAGE	Modify List	Issue Description	OWNER
		1	37	U33 Pin10 change connect from RUN_ON_D to RUN_ON	Follow M07 design	EE
		2	26,29,41	HOST_DEBUG_TX and HOST_DEBUG_RX connect to U31 first then connect to connector(DBG2)	TX,RX need add buffer for debug	EE,SW
		3	8	Del RN40 and add R551,R552(10k ohm) then Pop R440	Implement C4E feature on DPRSLPVR	EE
		4	14,29	Smbus which connect to LCD connector change to SBAT_SMBDAT and SBAT_SMBCLK	This is follow M07 design	EE
		5	15	C112,C113,C121,C129,C139,C155 change from 82p to 0.5p	For TV EA measurement pass	EE
		6	16	R228,R229 change from 33 ohm to 39 ohm	For Azalia EA measurement pass	EE
		7	16	Add R568(0 ohm) for X2(Crystal for ICH7M)	This is follow COE's suggestion	EE
		8	16	C297,C314 change from 4.7P to 3.3P for X2(Crystal for ICH7M)	CRYTAL Vendor suggestion	EE
		9	18	Change R472 to 0805 size and add L48(10UH)	This is follow COE's suggestion	EE
		10	19	Add R560,R561(100k)	Follow M07 design	EE
		11	21,22	Change C250 to 10uF and add C686(0.1u),C687(1u)	This is follow COE's suggestion	EE
		12	23	X1 change from 20p to 18p type crystal	By Broadcom's suggestion,Lan crystal need use 18p type	EE
		13	24	C642,C644 change from 18P to 15P for X5(Crystal for R5C832)	CRYTAL Vendor suggestion	EE
		14	25	Swap connection for CARD1 pin22 and pin23	Card pin22 and pin23 need swap for MS card function work normally	EE
2005/11/03	X00 to X01	15	25	Change L29 and L37 to 110 ohm impedance type for 1394	X00 already use 110 ohm type only forget to modify schematic	EE
		16	26	Add D32 and depop R266 to prevent leakage from WAN_RADIO_DIS#	Follow M07 design	EE
		17	27	Change R353 connection from U35 pin1 to U35 pin3	COE's suggestion to prevent the wireless LED light strength not enough	EE
		18	27	R42,R43 change to 220ohm;R40 change to 470ohm	LED light strength need change to avoid light leak	EE
		19	27	Q33 and Q34 Pin1 from +5V_ALW to +3V_ALW	Change to +3VALW for battery LED work normally	EE
		20	29	RN4 and RN6 change from 8.2K to 1K and add R323,R324,R333,R334,C682,C683,C684,C686	For SMBUS EA measurement pass	EE
		21	29	C538,C544 change from 20P to 27P for X4(Crystal for MEC5004)	CRYTAL Vendor suggestion	EE
		22	29	Reversed R553,R554,R555,R556,R557,Q72,Q73,D31,C680,R560	KBC Work Around Circuit for MEC5004 Rev "C"	EE
		23	29	Add R559(0 ohm) to GND	To Fix Rev "C" KBC bug	EE
		24	30	Pop R244 and depop R225	Change BOARD ID to X01	EE
		25	32	Add R562(0 ohm) in EMC4000 pin 22	Easily debug for THERM_STP# signal	EE
		26	33	R321,R330 from 20K ohm to 4K7 ohm R331,R332 from 10K ohm to 200K ohm	To prevent leakage from +3V_SUS to +3V_RUN when in suspend	EE
		27	33	Pop R28,R335,Q6,Q13	For 1.8V_SUS discharge more quickly	EE
		28	33	Change R19 to 200k and C84 to 470pF	For IMVP_PWRGD glitch issue,need make +5V_RUN more faster than +3V_RUN when boot up	EE
		29	33	REMOVE Q8,Q15,R323,R324,R333,R334	Follow M07 design	EE
		30	35	Change R394 to 165K and R396,R397,R401 to 137K then depop C457	This is changed for Vcore load line test fail	Power
		31	35	Change R410,R454 and R165 to 1.5 ohm	This is changed for Vcore's ring over spec	Power
		32	36	Add R565 and R566 for SUS_ON unstable when plug adapter	This is recommended by TDC Lawrence	Power
		33	36	Change TC3 to another source	This is recommended by power team	Power
		34	37	Depop TC18 and change TC17 to 330uF;change D20 to BAT54;change R3 to 13K3 ohm;change R298 to 3D3 ohm	This is recommended by power team	Power
		35	37	New add 4 gaps G75,G76,G77,G78 for 1.8V	This is requested by EMI	EMI
		36	38	Change R427 to 15K4 ohm	This is recommended by power team	Power
		37	39	Add R558,C682 in U5 pin15 pin16 for PBATT_SENSE	To prevent Charger damage when plug battery	Power
		38	39	ADD ADAPT_TRIP_SEL circuit	Follow M07 schematic	Power
		39	41	Add EC61,EC62,EC63,EC64,SPR22 and depop EC41,EC11,EC15,EC14,EC9,EC18,EC58,EC46,EC51,EC54,EC17,EC20,EC53,EC21,EC42	This is for EMI	EMI

hexainf@hotmail.com
GRATIS - FOR FREE

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
HISTORY from X00 to X01			
Title			
Size A3	Document Number	Rev	
	Bermuda	-1	
Date: Wednesday, March 01, 2006	Sheet	43	of 45

DATE	VERSON	ITEM	PAGE	Modify List	Issue Description	OWNER
		1	6	Change CPU 22uF to 10uF for power noise,total 32 pieces	Power team suggestion	Power
		2	17,29	Add R573(47 ohm) and R574 (0 ohm) during ICH7M and KBC for SPI_CS# to verify signal quality	Suggestion by COE	EE
		3	19	Change R560 and R561 to no pop	Suggestion by COE	EE
		4	20	Reversed Pad for R577(0 ohm),because Seagate SATA HDD driver will make S3 resume issue on spin-up mode	Suggestion by COE	EE
		5	22	Pop C525 for VREFOUT	Suggestion by COE	EE
		6	25	Change U57 to G5240 for OCP Issue	Suggestion by COE	EE
		7	29	Pop R200 and de-pop R201	Enable internal bootblock flash function	EE
		8	30	Pop R243 and R225, de-pop R244 and R224	Change Board ID to X02	EE
		9	30	New add R575 and R576 for HDDC_EN# and MODC_EN#	Suggestion by COE	EE
		10	34	Change Q70 from 3904 to 2N7002	Suggestion by COE	EE
		11	35	De-pop R386 and pop R380	Power team suggestion	Power
		12	35	Change C102 from 680PF to 390PF	Power team suggestion	Power
		13	36	Add R567(51k ohm) from SUS_ON to GND to avoid SUS_ON glitch issue	Power team suggestion	Power
		14	36	Add C691 and R572 for +3V_ALW soft-start	Power team suggestion	Power
		15	37	Change U6 to SI4852DY	Power team suggestion	Power
2006/01/03	X01 to X02	16	38	Change the enable pin of TPS51483 connection from RUN_ON_D to RUN_ON	Power team suggestion	Power
		17	38	Change R402 to 200k and R404 to 270K and L10 to 1D5UH	Power team suggestion	Power
		18	38	Add C690,C692,C694 and reversed C695 for 1.5V noise issue	Power team suggestion	Power
		19	38	Reversed C693 and D35 for 1.5V enable signal	Power team suggestion	Power
		20	39	Change U1,U2 and U3 to SI4435BDY	Power team suggestion: AOS is not in Dell QVL	Power
		21	39	Remove G19, G20 and G21	Power team suggestion	Power
		22	39	New add C689 (3300 PF)	Suggestion by MAXIM	Power
		23	39	New add D34 and R453 to solve MAX8731 can't charge battery when battery voltage lower than 2.5V	Suggestion by MAXIM	Power
		24	39	De-pop C681	Power team suggestion	Power
		25	40	Change D3,D4,D21,D22 connection way,before is after resistors but now change to connect battery connector first then to resistors	This is ESD issue,the ESD diode need to be placed near to battery connector	EMI
		26	29	Change X4 to XTAL 32.768K 6PF10PPM	This is because Barbados lesson learn,old crystal sometimes will make system can not boot.	EE

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **HISTORY from X01 to X02**

Size: A3 Document Number: **Bermuda** Rev: -1

Date: Wednesday, March 01, 2006 Sheet: 44 of 45

DATE	VERSION	ITEM	PAGE	Modify List	Issue Description	OWNER
		1	24	De-pop R541 and pop R547 and C669 for GBSRST#	Suggestion by COE	EE
		2	29	Change X4 to XTAL 32.768K 12.5P10PPM DMX26S and slope change C544 to 18P and C538 to 22P	Suggestion by KDS and Epson	EE
		3	30	Depop R225 and pop R244 for Board ID change	Change Board ID to X03	EE
		4	31	Add D36 and reversed R578 for leakage issue	To prevent leakage issue	EE
		5	35	Change R391 vendor from MURATA to MITSUBISHI	Suggestion by Power Team	Power
		6	36	Change R341 from 10K ohm to 1K ohm	Suggestion by Power Team	Power
		7	39	Depop L1 and pop L49 for DFX issue	Suggestion by Power Team	Power
		8	41	Add EC65 and EC66 for EMI's request	EMI's request	EMI
		9	27	For BREATH LED==>R40 change to 150 ohm For HDD LED==>R41 change to 51 ohm For battery LED==>R42 and R43 change to 51 ohm	Change brightness of LED	EE
2006/02/22	X02 to A00					

hexainf@hotmail.com
GRATIS - FOR FREE

		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: HISTORY from X02 to X03			
Size: A3	Document Number:	Bermuda	Rev: -1
Date: Wednesday, March 01, 2006		Sheet: 45	of: 45