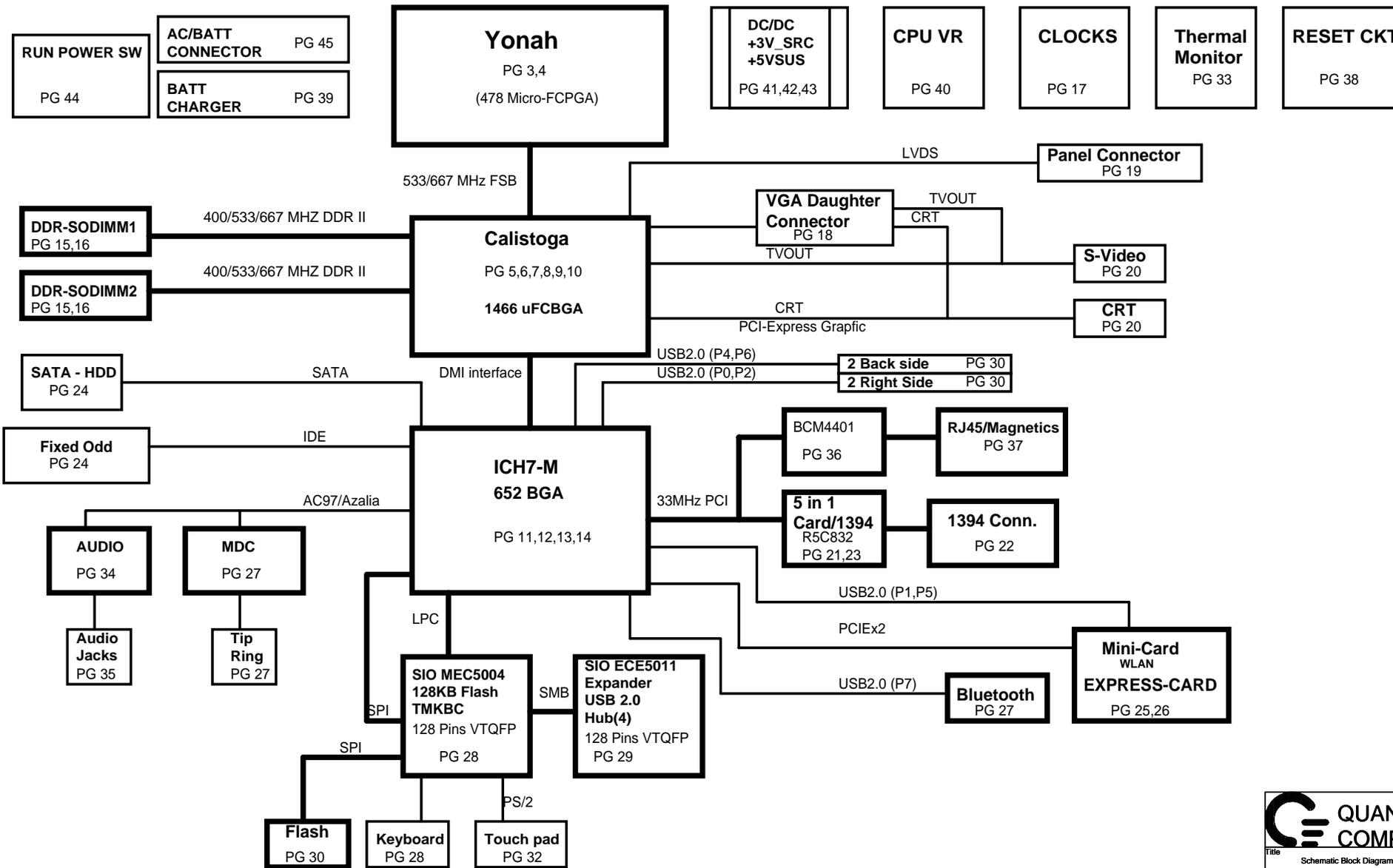


KEYLARGO-Integrate

VER : 2A

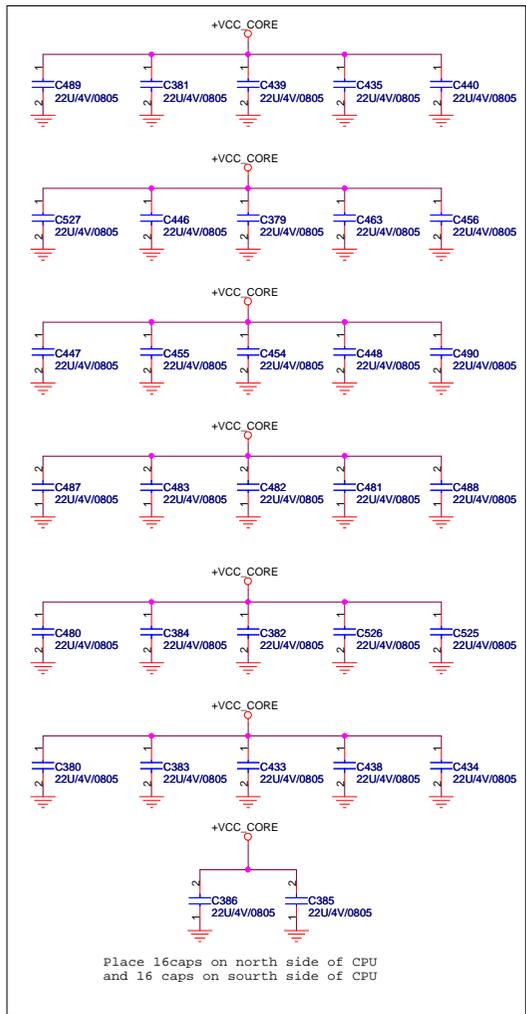


INDEX

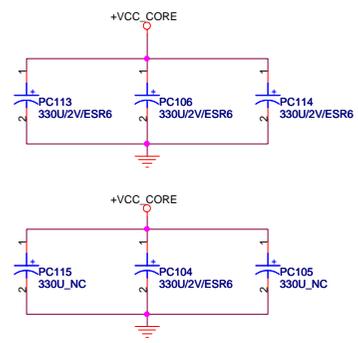
Pg#	Description	DNI LIST
1	Schematic Block Diagram 1	
2	Blank Page	
3	Front Page	
4-5	Dothan	
6-10	Alviso	
11-13	ICH6	
14-15	DDRII SO-DIMM(200P)	
16	Clock Generator	
17	CH7306/7	
18-19	Blank Pages	
20	LCD Conn. & SSP	
21	CRT & TV Conn.	
22	SATA & IDE Conn.	
23	Screw Hole	
24	TI PIC6515	
25	Mini PCI Conn.	
26	MDC Conn.	
27-28	SIO (LPC47N354)	
29	SERIAL PORT & USB	
30	PARALLEL CONN.	
31	Flash ROM	
32	TOUCH PAD & BLUE TOOTH	
33	Switch Board Conn. & LED	
34	FAN & Thermal	
35-36	Audio CODEC (STAC9751) & Phone Jack	
37-38	LOM (BCM5751), Switch	
39	FIR	
40-41	Docking Conn. & Q-Switch	
42	Power Good	
43-44	Battery Selector & Charger	
45	CPU Power	
46	1.8V,0.9V,1.5V,1.05V	
47	3VALW/5V/3V/Power ON	
48	RUN Power Switch	
49	VGA DC/DC	
50	DCIN/Batt Conn.	

Power & Ground

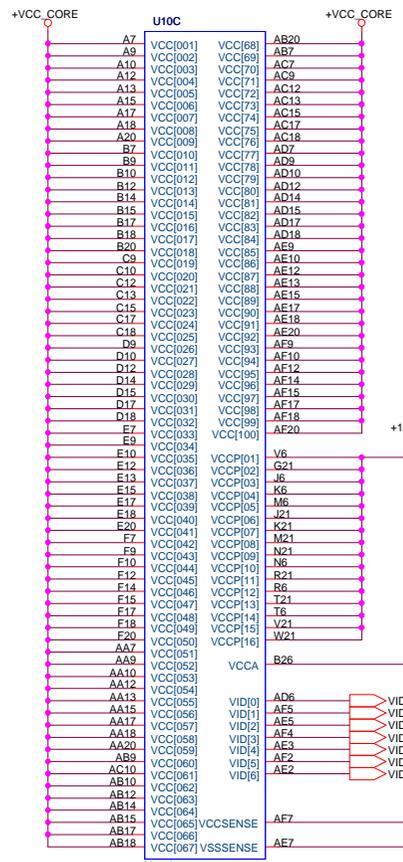
Label	Pg#	Description	Control Signal
DC_IN+		AC ADAPTER (20V)	
PBATT+		MAIN BATTERY + (10~17V)	
PWR_SRC		MAIN POWER (10~20V)	
RTC_PWR3_3V		RTC & PCL POWER (3_3V)	
+12V		+12V	DRUNPWROK
VHCORE		CPU CORE POWER (1.25/1.15V)	RUNPWROK
V1_2RUN		AGTL+ POWER (1.2V)	RUNPWROK
+3VRUN		SLP_S3# CTRLD POWER	RUN_ON
+3VSUS		SLP_S5# CTRLD POWER	SUS_ON
+5VALW		8051 POWER (5V)	
+5VRUN		SLP_S3# CTRLD POWER	RUN_ON
+5VSUS		SLP_S5# CTRLD POWER	SUS_ON
+5VHDD		HDD POWER (5V)	HDDC_EN#
+5VMOD		MODULE POWER (5V)	MODC_EN#
STRB#5V		EXTERNAL FDD POWER (5V)	FDD/LPT#
+5VFAN1, +5VFAN2		FAN POWER (5V)	FAN_OFF/ON#
VDDA		AUDIO ANALOG POWER (5V)	RUN_ON
1_8VSUS		RESUME WELL IN ICH	
1_8VRUN		SLP_S3# CTRLD POWER	
+3VALW		8051 POWER (3V)	
V1_5RUN		AGP I/O POWER	
 GND	ALL PAGES	DIGITAL GROUND	
 GNDP		CPU POWER GND	
 CGNDP		CHARGER GND	
 DGNDP		DC/DC POWER GND	
 LANGND		COMBO CONN GND	



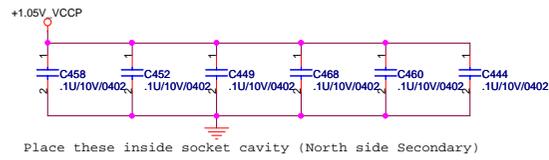
Place 16caps on north side of CPU and 16 caps on south side of CPU



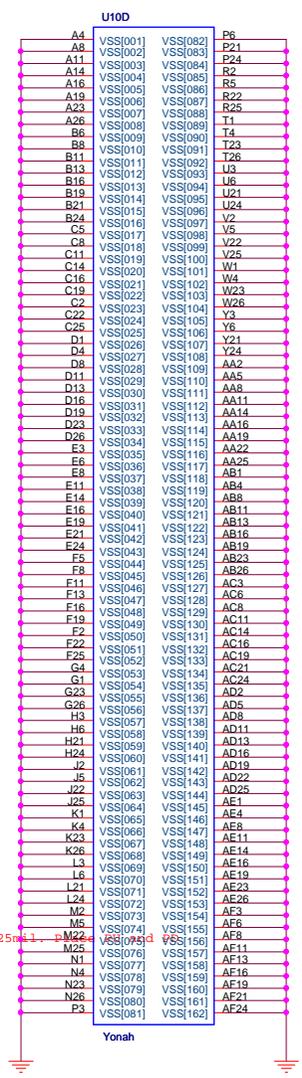
Total caps = 2684 uF
ESR = 6m ohm/4 // 3m ohm/32



Route VCCSENSE and VSSSENSE traces at 27.4ohms with 10mil spacing and for other signals keep 25mil spacing and length match within 2 inch of CPU.



Place these inside socket cavity (North side Secondary)

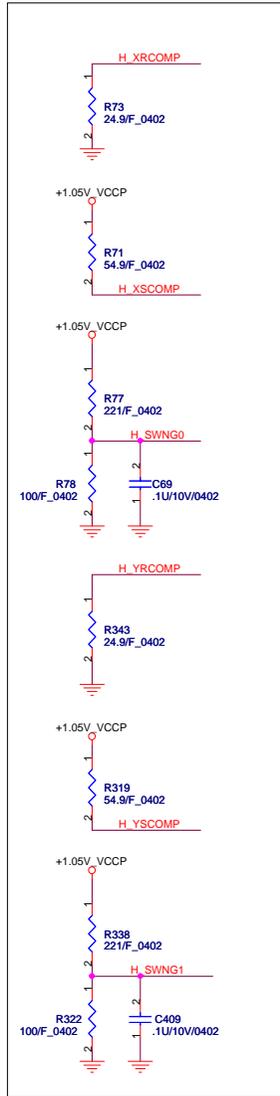


YONAH COMPUTER

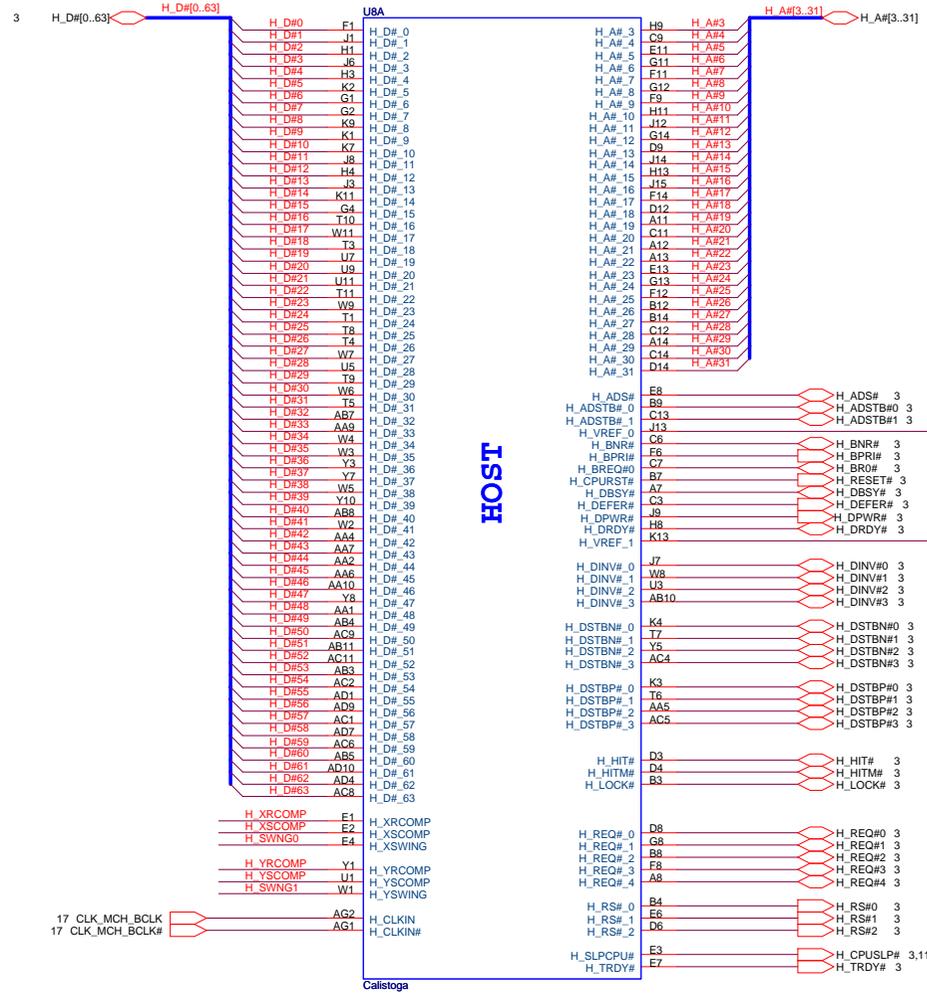
Title: Yonah Processor (POWER)

Size: FM1	Document Number: FM1	Rev: 2A
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Date: Tuesday, September 06, 2005 Sheet: 4 of 51



H_XRCOMP, H_XSCOMP, H_YRCOMP, H_YSCOMP,
H_SWNG0, H_SWNG1 used W:10/S:20 mil.
R & C of HXRCOMP, HXSCOMP, HYRCOMP, HYSCOMP,
H_SWNG0, H_SWNG1 trace length less 0.5" from
U3



**QUANTA
COMPUTER**

Title: Callistoga (Host)

Size	Document Number	Rev
	FM1	2A

Date: Tuesday, September 06, 2005 Sheet 5 of 51

15 DDR_A_D[0..63]

DDR_A_D0	AJ35	SA_D00
DDR_A_D1	AJ34	SA_D01
DDR_A_D2	AM31	SA_D02
DDR_A_D3	AM33	SA_D03
DDR_A_D4	AK35	SA_D06
DDR_A_D5	AJ36	SA_D05
DDR_A_D6	AJ32	SA_DM_1
DDR_A_D7	AH31	SA_DM_2
DDR_A_D8	AP33	SA_DM_3
DDR_A_D9	AN35	SA_DM_4
DDR_A_D10	AR31	SA_DM_5
DDR_A_D11	AP31	SA_DM_6
DDR_A_D12	AN38	SA_DM_7
DDR_A_D13	AM36	SA_DQ0_0
DDR_A_D14	AM34	SA_DQ0_1
DDR_A_D15	AN33	SA_DQ0_2
DDR_A_D16	AK26	SA_DQ0_3
DDR_A_D17	AL27	SA_DQ0_4
DDR_A_D18	AM26	SA_DQ0_5
DDR_A_D19	AN24	SA_DQ0_6
DDR_A_D20	AK28	SA_DQ0_7
DDR_A_D21	AL28	SA_DQS#_0
DDR_A_D22	AM24	SA_DQS#_1
DDR_A_D23	AP26	SA_DQS#_2
DDR_A_D24	AP23	SA_DQS#_3
DDR_A_D25	AL22	SA_DQS#_4
DDR_A_D26	AM12	SA_DQS#_5
DDR_A_D27	AN20	SA_DQS#_6
DDR_A_D28	AL23	SA_DQS#_7
DDR_A_D29	AP24	SA_MA_0
DDR_A_D30	AP21	SA_MA_1
DDR_A_D31	AT21	SA_MA_2
DDR_A_D32	AR12	SA_MA_3
DDR_A_D33	AR14	SA_MA_4
DDR_A_D34	AP13	SA_MA_5
DDR_A_D35	AP12	SA_MA_6
DDR_A_D36	AT13	SA_MA_7
DDR_A_D37	AT12	SA_MA_8
DDR_A_D38	AL14	SA_MA_9
DDR_A_D39	AL12	SA_MA_10
DDR_A_D40	AK9	SA_MA_11
DDR_A_D41	AN7	SA_MA_12
DDR_A_D42	AK9	SA_MA_13
DDR_A_D43	AK7	SA_RAS#
DDR_A_D44	AP9	SA_RCVENOUT#
DDR_A_D45	AN9	SA_WE#
DDR_A_D46	AL5	
DDR_A_D47	AT5	
DDR_A_D48	AY2	
DDR_A_D49	AW2	
DDR_A_D50	AP1	
DDR_A_D51	AV2	
DDR_A_D52	AN2	
DDR_A_D53	AT3	
DDR_A_D54	AN1	
DDR_A_D55	AL2	
DDR_A_D56	AG7	
DDR_A_D57	AF9	
DDR_A_D58	AG4	
DDR_A_D59	AF6	
DDR_A_D60	AG9	
DDR_A_D61	AH6	
DDR_A_D62	AF4	
DDR_A_D63	AF8	

DDR SYSTEM MEMORY A

SA_BS_0	AU12
SA_BS_1	AV14
SA_BS_2	BA20
SA_CAS#	AY13
SA_DM_0	AJ33
SA_DM_1	AM35
SA_DM_2	AL26
SA_DM_3	AN22
SA_DM_4	AM14
SA_DM_5	AL8
SA_DM_6	AR3
SA_DM_7	AH4
SA_DQS_0	AK33
SA_DQS_1	AT33
SA_DQS_2	AN28
SA_DQS_3	AM22
SA_DQS_4	AN12
SA_DQS_5	AN8
SA_DQS_6	AP3
SA_DQS_7	AG5
SA_DQS#_0	AK32
SA_DQS#_1	AU33
SA_DQS#_2	AN27
SA_DQS#_3	AM21
SA_DQS#_4	AM12
SA_DQS#_5	AL8
SA_DQS#_6	AN3
SA_DQS#_7	AH5
SA_MA_0	AY16
SA_MA_1	AU14
SA_MA_2	AW16
SA_MA_3	BA15
SA_MA_4	BA17
SA_MA_5	AU16
SA_MA_6	AV17
SA_MA_7	AU17
SA_MA_8	AW17
SA_MA_9	AT16
SA_MA_10	AU13
SA_MA_11	AT17
SA_MA_12	AV20
SA_MA_13	AV12
SA_RAS#	AW14
SA_RCVENOUT#	AK23
SA_WE#	AK24



UBD

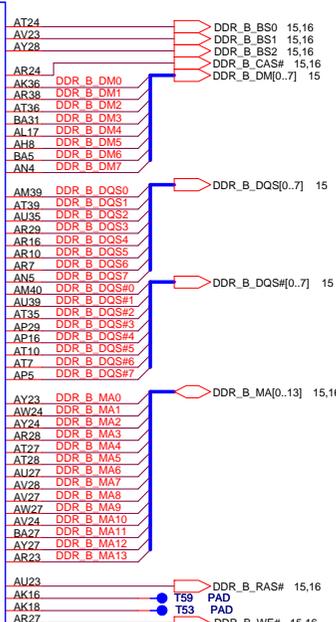
Calistoga

15 DDR_B_D[0..63]

DDR_B_D0	AK38	SB_D00
DDR_B_D1	AL37	SB_D01
DDR_B_D2	AP39	SB_D02
DDR_B_D3	AR41	SB_D03
DDR_B_D4	AK38	SB_D06
DDR_B_D5	AJ38	SB_D05
DDR_B_D6	AN41	SB_DM_0
DDR_B_D7	AP41	SB_DM_1
DDR_B_D8	AT40	SB_DM_2
DDR_B_D9	AV41	SB_DM_3
DDR_B_D10	AU38	SB_DM_4
DDR_B_D11	AV38	SB_DM_5
DDR_B_D12	AP38	SB_DM_6
DDR_B_D13	AR40	SB_DM_7
DDR_B_D14	AW38	SB_DQ0_0
DDR_B_D15	AY38	SB_DQ0_1
DDR_B_D16	BA38	SB_DQ0_2
DDR_B_D17	AV36	SB_DQ0_3
DDR_B_D18	AR36	SB_DQ0_4
DDR_B_D19	AP36	SB_DQ0_5
DDR_B_D20	BA36	SB_DQ0_6
DDR_B_D21	AU36	SB_DQ0_7
DDR_B_D22	AP34	SB_DQS#_0
DDR_B_D23	AP34	SB_DQS#_1
DDR_B_D24	AY33	SB_DQS#_2
DDR_B_D25	BA33	SB_DQS#_3
DDR_B_D26	AT31	SB_DQS#_4
DDR_B_D27	AU29	SB_DQS#_5
DDR_B_D28	AU31	SB_DQS#_6
DDR_B_D29	AW31	SB_DQS#_7
DDR_B_D30	AY29	SB_MA_0
DDR_B_D31	AW29	SB_MA_1
DDR_B_D32	AM19	SB_MA_2
DDR_B_D33	AL19	SB_MA_3
DDR_B_D34	AP14	SB_MA_4
DDR_B_D35	AN14	SB_MA_5
DDR_B_D36	AN17	SB_MA_6
DDR_B_D37	AM16	SB_MA_7
DDR_B_D38	AP15	SB_MA_8
DDR_B_D39	AL12	SB_MA_9
DDR_B_D40	AJ11	SB_MA_10
DDR_B_D41	AH10	SB_MA_11
DDR_B_D42	AJ9	SB_MA_12
DDR_B_D43	AN10	SB_MA_13
DDR_B_D44	AK13	SB_RAS#
DDR_B_D45	AH11	SB_RCVENOUT#
DDR_B_D46	AK10	SB_WE#
DDR_B_D47	AJ8	
DDR_B_D48	BA10	
DDR_B_D49	AW10	
DDR_B_D50	BA4	
DDR_B_D51	AW4	
DDR_B_D52	AY5	
DDR_B_D53	AY9	
DDR_B_D54	AW5	
DDR_B_D55	AY5	
DDR_B_D56	AV4	
DDR_B_D57	AR5	
DDR_B_D58	AK4	
DDR_B_D59	AK3	
DDR_B_D60	AT4	
DDR_B_D61	AK5	
DDR_B_D62	AJ5	
DDR_B_D63	AJ3	

DDR SYSTEM MEMORY B

SB_BS_0	AT24
SB_BS_1	AV23
SB_BS_2	AY28
SB_CAS#	AR24
SB_DM_0	AK36
SB_DM_1	AR38
SB_DM_2	AT36
SB_DM_3	BA31
SB_DM_4	AL17
SB_DM_5	AH8
SB_DM_6	BA5
SB_DM_7	AN4
SB_DQS_0	AM39
SB_DQS_1	AT39
SB_DQS_2	AU35
SB_DQS_3	AR29
SB_DQS_4	AR16
SB_DQS_5	AR10
SB_DQS_6	AK7
SB_DQS_7	AN5
SB_DQS#_0	AM40
SB_DQS#_1	AU39
SB_DQS#_2	AT35
SB_DQS#_3	AP29
SB_DQS#_4	AP16
SB_DQS#_5	AT10
SB_DQS#_6	AT7
SB_DQS#_7	AP5
SB_MA_0	AY23
SB_MA_1	AW24
SB_MA_2	AY24
SB_MA_3	AR28
SB_MA_4	AT27
SB_MA_5	AT28
SB_MA_6	AU28
SB_MA_7	AV27
SB_MA_8	AV27
SB_MA_9	AV24
SB_MA_10	BA27
SB_MA_11	AY27
SB_MA_12	AY27
SB_MA_13	AR23
SB_RAS#	AU23
SB_RCVENOUT#	AK16
SB_WE#	AK18



UBE

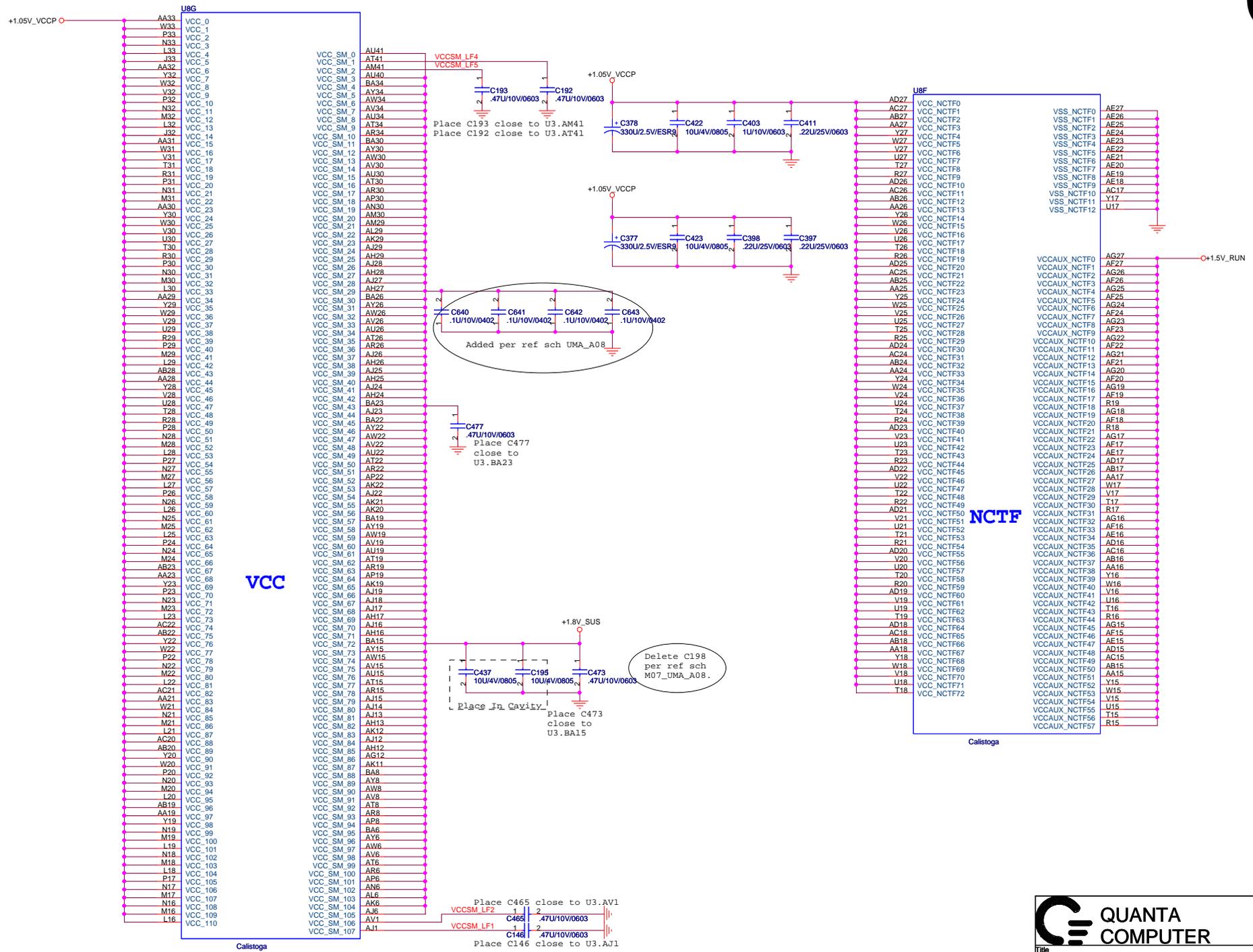
Calistoga

QUANTA COMPUTER

Title: Calistoga (DDR2)

Size	Document Number	Rev
	FM1	2A

Date: Tuesday, September 06, 2005 Sheet 7 of 51

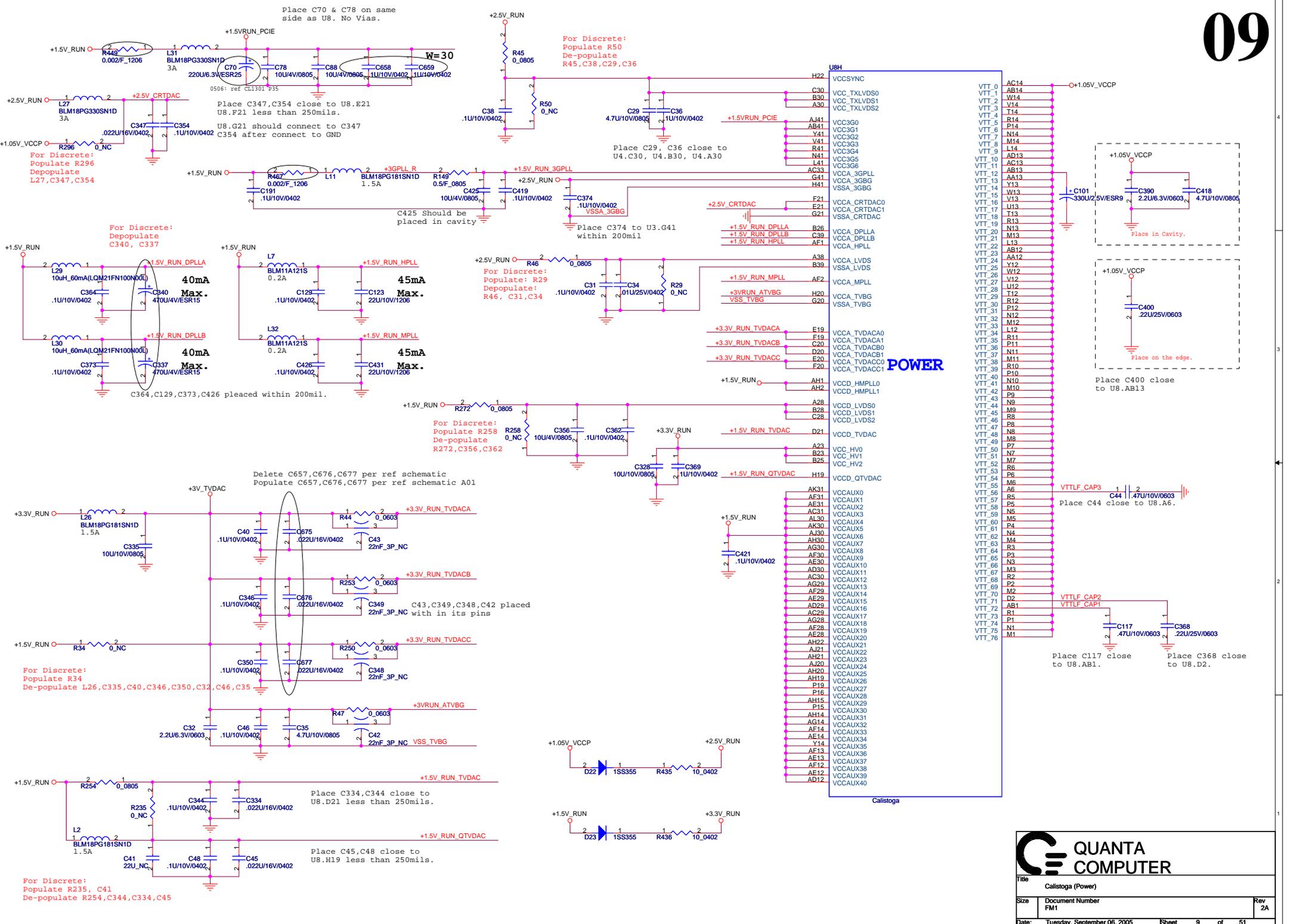


QUANTA COMPUTER

Title: Callistoga (VCC, NCTF)

Size	Document Number	Rev
	FM1	2A

Date: Tuesday, September 06, 2005 Sheet 8 of 51



For Discrete:
Populate R50
De-populate
R45, C38, C29, C36

Place C29, C36 close to
U4. C30, U4. B30, U4. A30

Place C374 to U3. G41
within 200m11

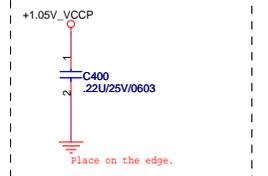
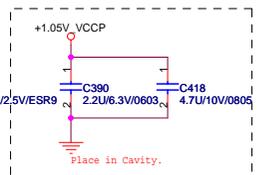
For Discrete:
Populate R258
De-populate
R272, C356, C362

Delete C657, C676, C677 per ref schematic
Populate C657, C676, C677 per ref schematic A01

For Discrete:
Populate R34
De-populate L26, C335, C40, C346, C350, C32, C46, C35

For Discrete:
Populate R235, C41
De-populate R254, C344, C334, C45

POWER



Place C400 close to
U8. AB13



Place C44 close to
U8. A6.



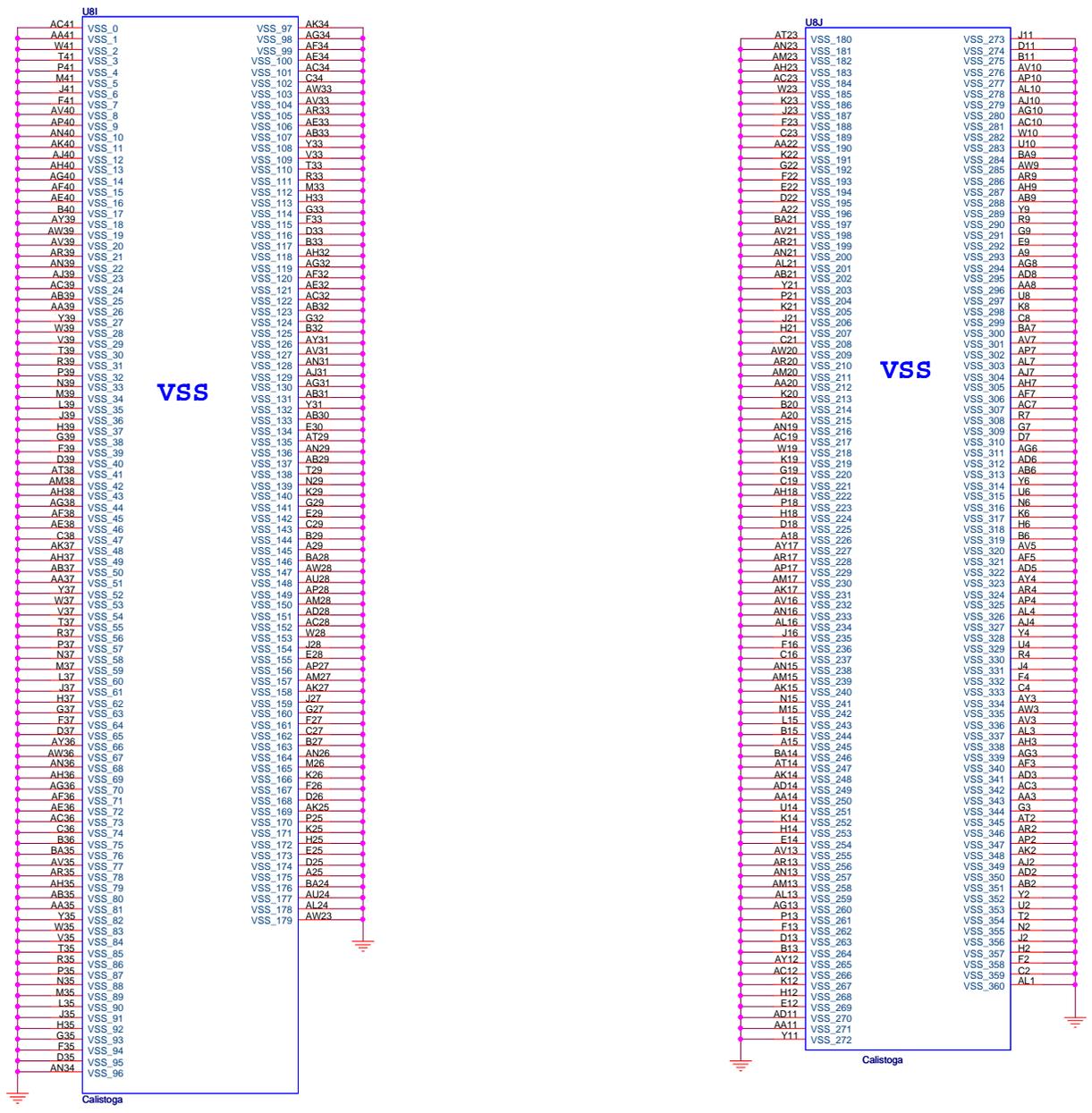
Place C117 close
to U8. AB1.

Place C368 close
to U8. D2.

QUANTA COMPUTER

Title: Calistoga (Power)

Size: Document Number FM1	Rev: 2A
Date: Tuesday, September 06, 2005	Sheet: 9 of 51

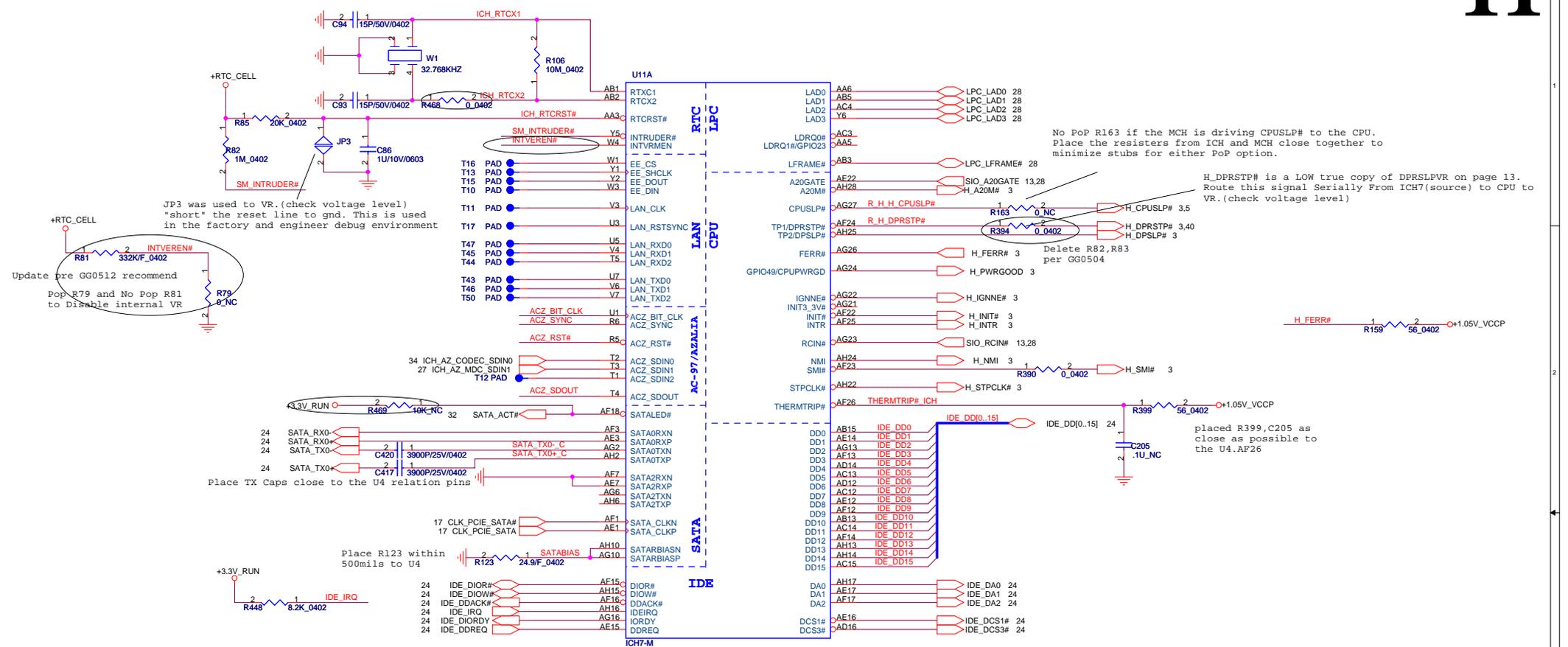


QUANTA COMPUTER

Title: Calistoga (VSS,NCTF)

Size	Document Number	Rev
	FM1	2A

Date: Tuesday, September 06, 2005 Sheet 10 of 51



JP3 was used to VR.(check voltage level)
"short" the reset line to gnd. This is used
in the factory and engineer debug environment

Update pre GG0512 recommend
Pop R79 and No Pop R81
to Disable internal VR

Place TX Caps close to the U4 relation pins

Place R123 within
500mils to U4

No PoP R163 if the MCH is driving CPUSLP# to the CPU.
Place the resistors from ICH and MCH close together to
minimize stubs for either PoP option.

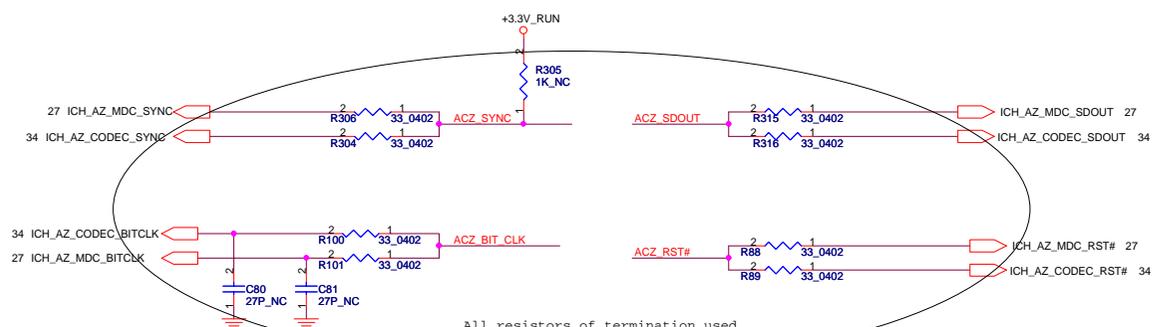
H_DPRSTP# is a LOW true copy of DPRSLPVR on page 13.
Route this signal Serially From ICH7(source) to CPU to
VR.(check voltage level)

Delete R82,R83
per GG0504

placed R399,C205 as
close as possible to
the U4.AF26

X1,X2 Docking

IAC_SYNC	Port X Line	R126
1	1X2, 2X1	STUFF
0	4X1	UNSTUFF

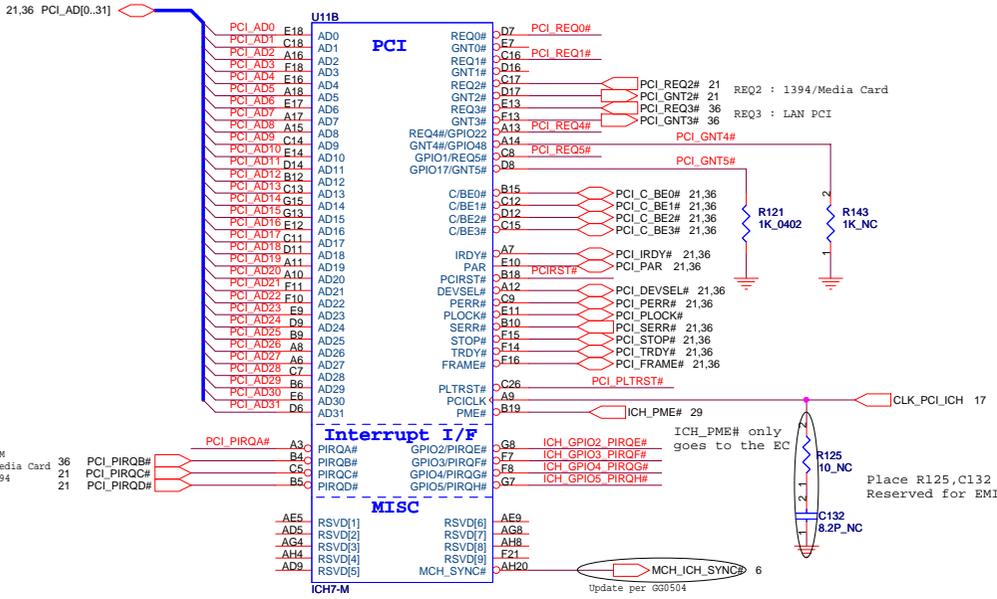
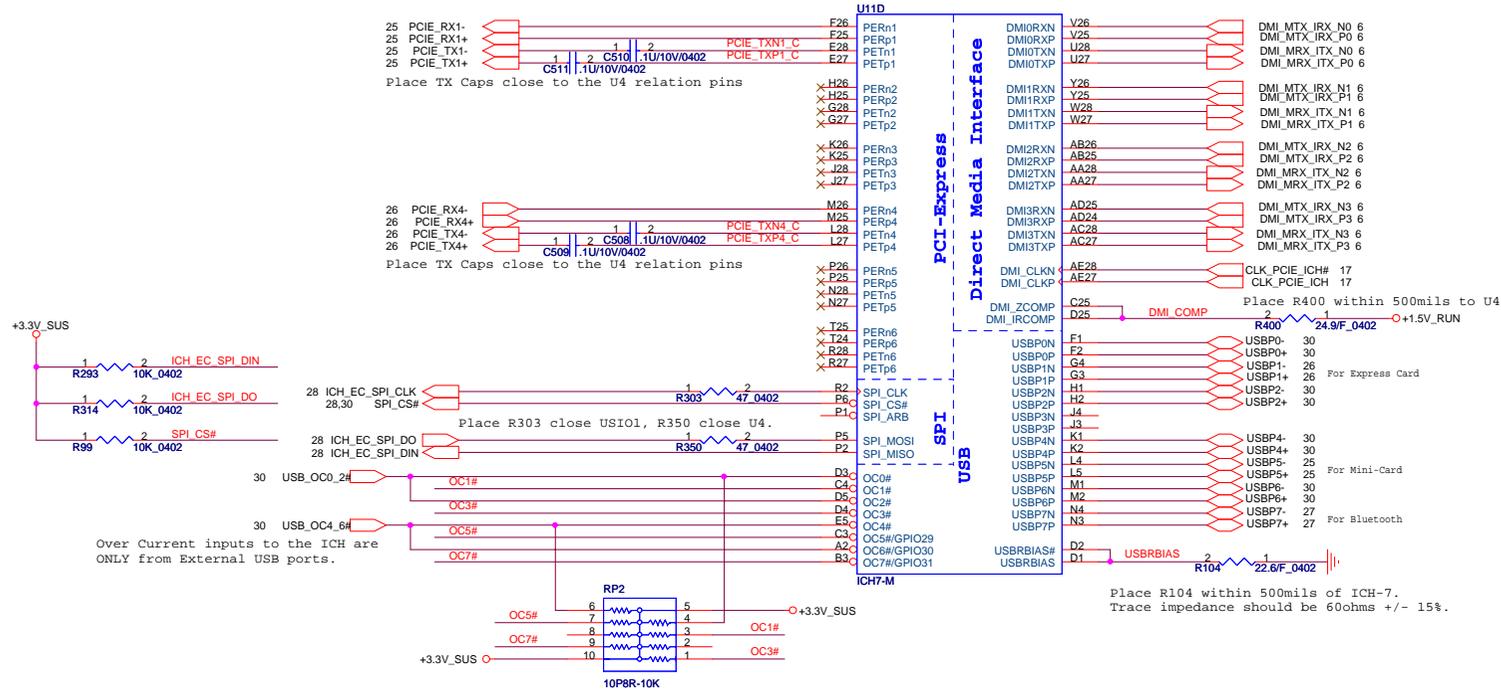


All resistors of termination used
of "T" type routing need tuned
equal and close to the source.

**QUANTA
COMPUTER**

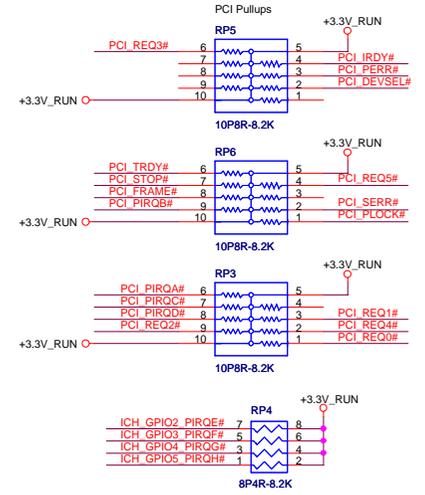
Title: ICH7-M (CPU,IDE,SATA,LPC,AC97)

Size: Document Number FM1	Rev: 2A
Date: Tuesday, September 06, 2005	Sheet: 11 of 51



Register pop options to boot from various sources

		GNT5# R121	GNT4# R143
LPC	11	Not Stuff	Not Stuff
PCI	10	Not Stuff	Stuff
SPI	01	Stuff	Not Stuff

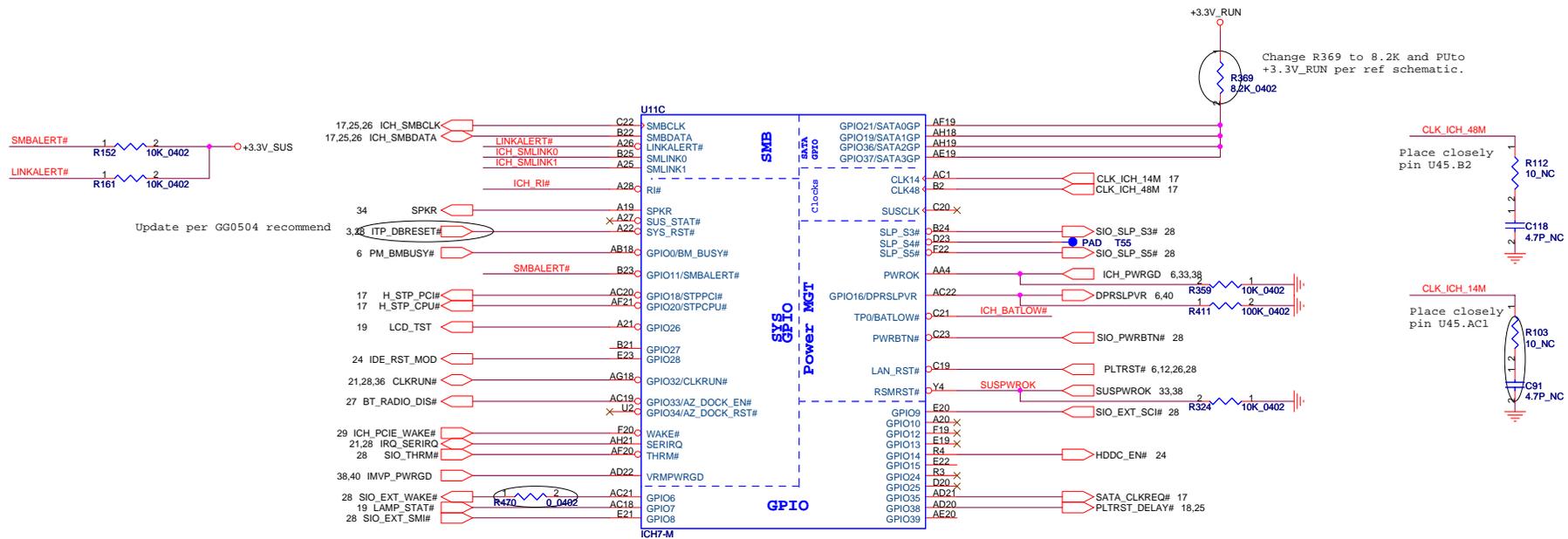


QUANTA COMPUTER

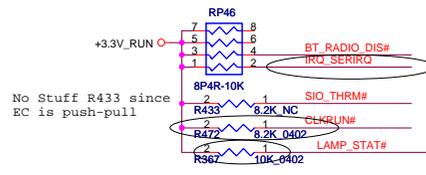
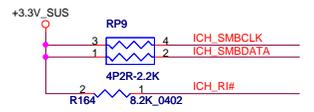
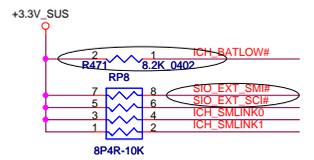
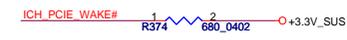
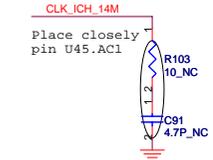
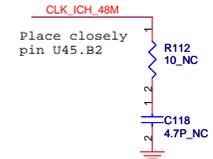
Title: ICH7-M (USB,DMI,PCIE,PCI)

Size	Document Number	Rev
	FM1	2A

Date: Tuesday, September 06, 2005 Sheet 12 of 51

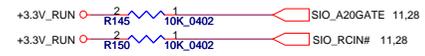


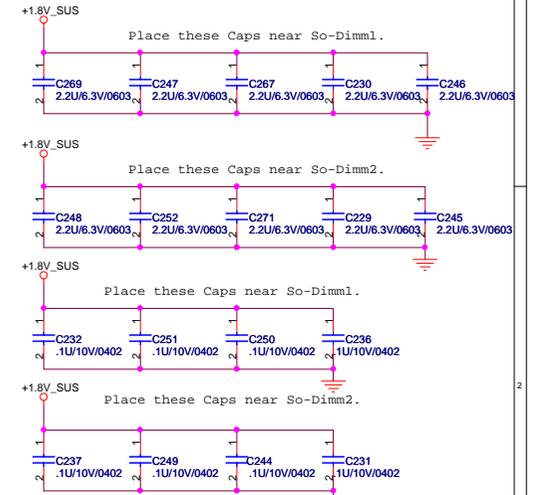
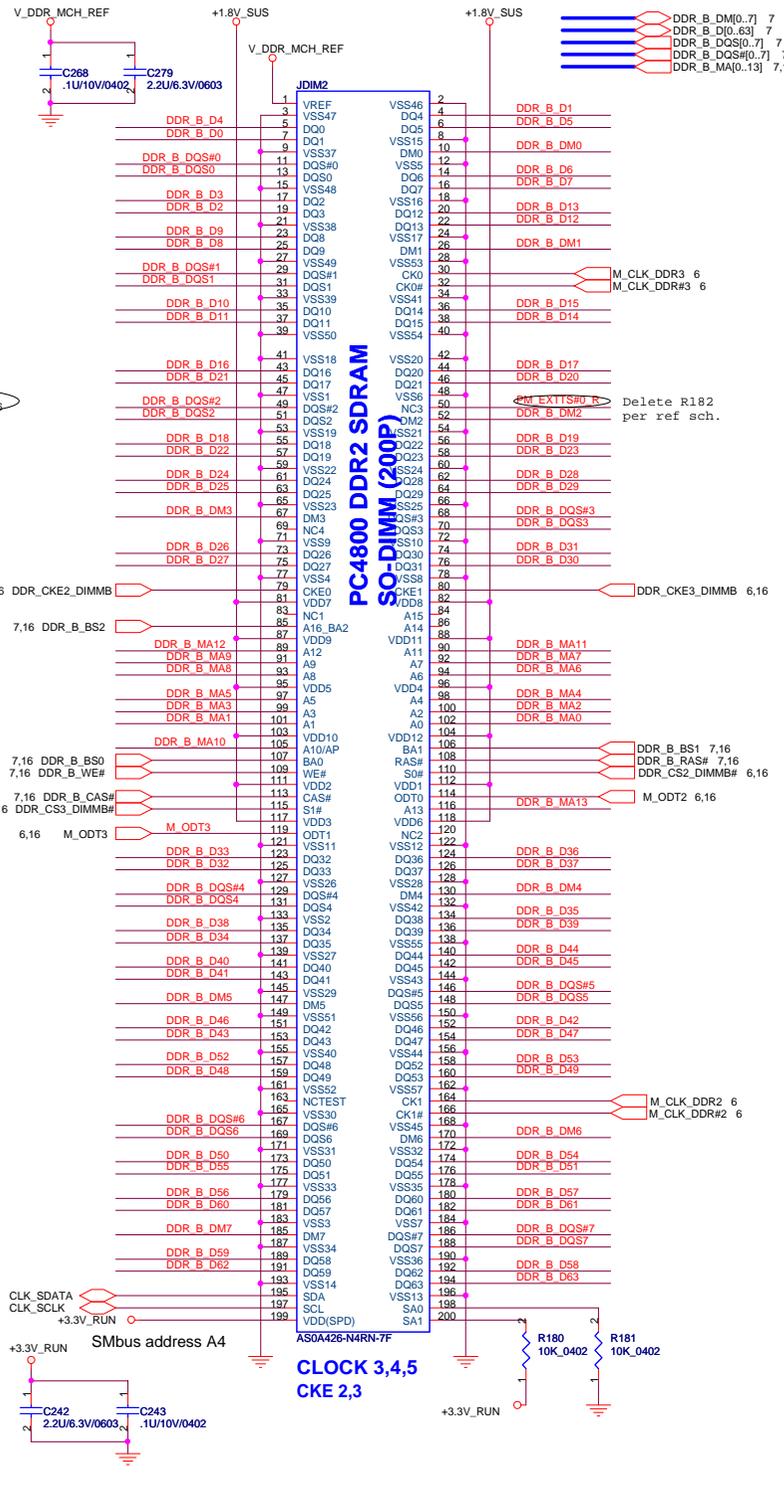
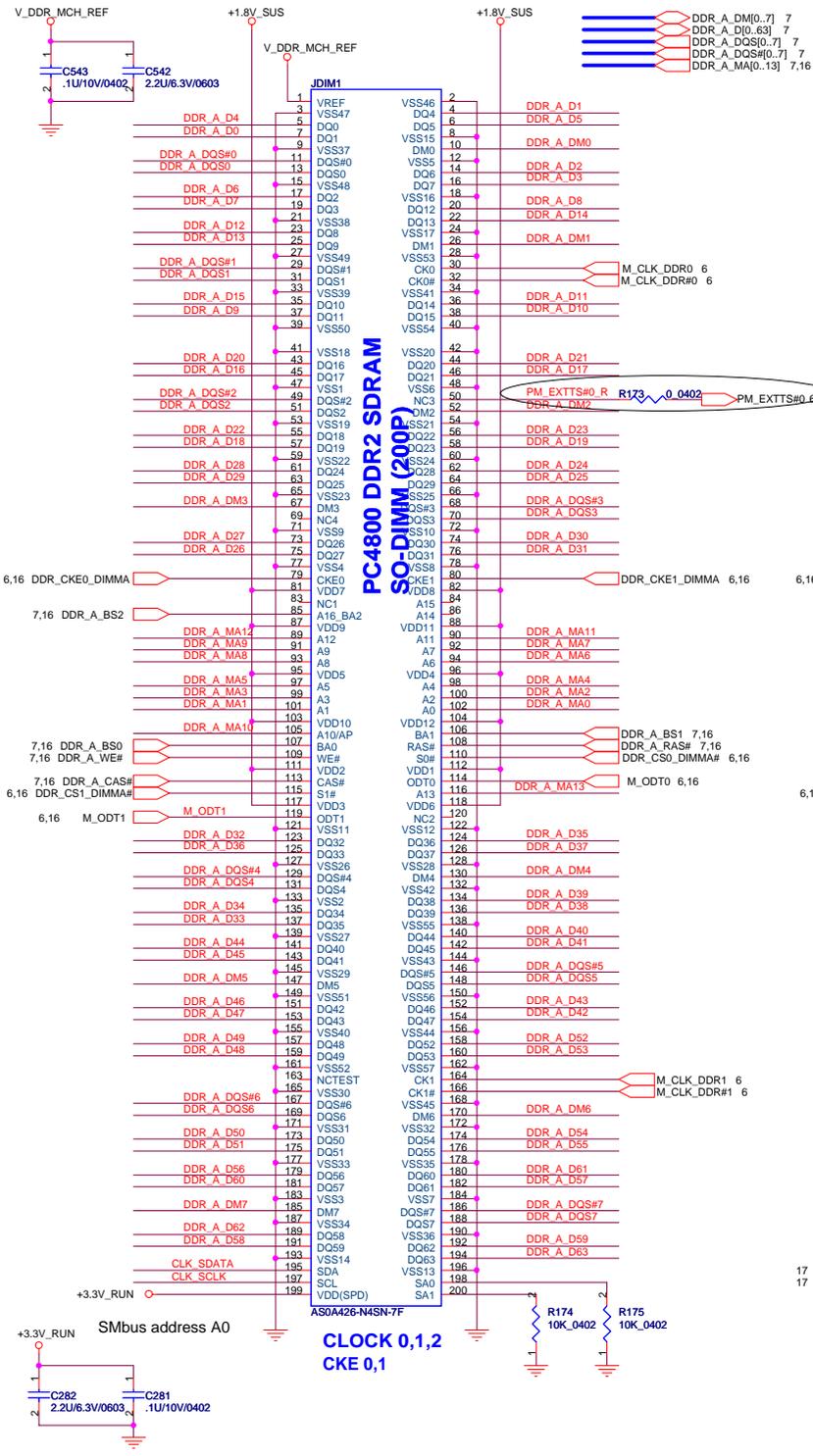
+3.3V_RUN
 R369 8.2K_0402
 Change R369 to 8.2K and PUTO +3.3V_RUN per ref schematic.



No Stuff R433 since EC is push-pull

Change R367 from 8.2K to 10K per ref schematic.
 Change power rail from +3.3V_SUS to +3.3V_RUN per ref schematic.
 Option to "Disable" clkrun. Pulling down will keep the clks running



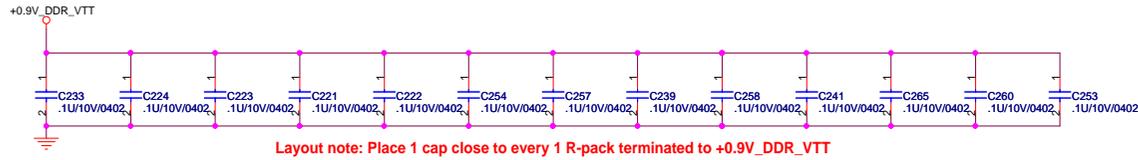
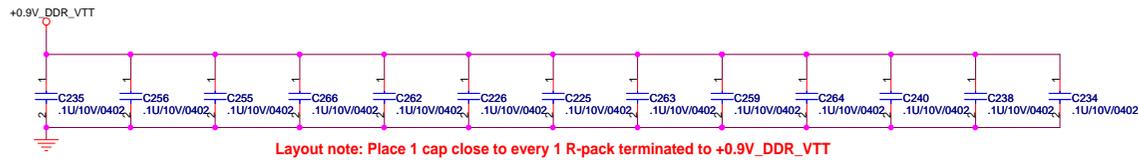


QUANTA COMPUTER

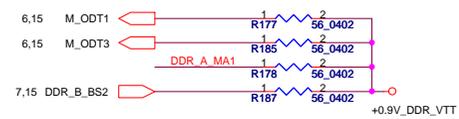
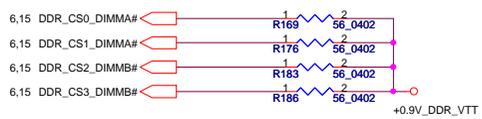
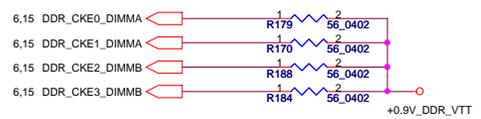
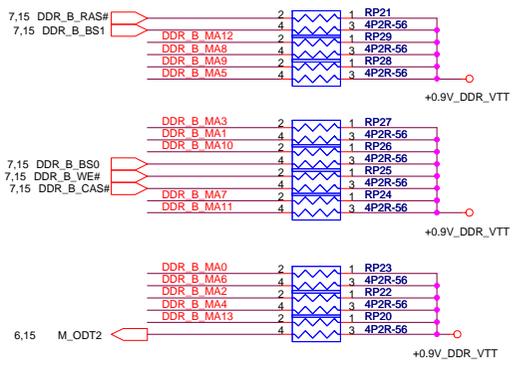
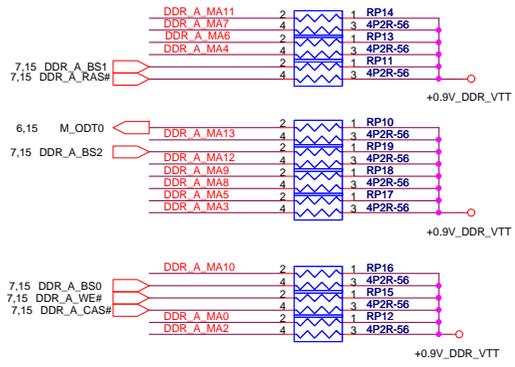
Title: System DRAM Expansion (200P-DDR_SODIMM X 2)

Size: Document Number FM1 Rev 2A

Date: Tuesday, September 06, 2005 Sheet 15 of 51

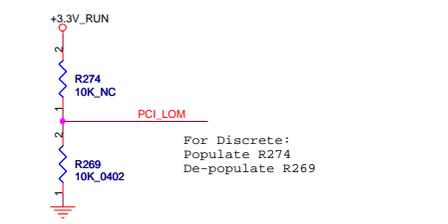
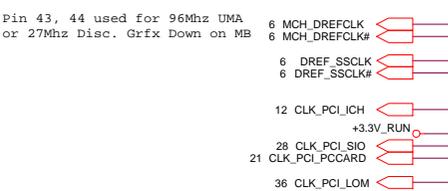
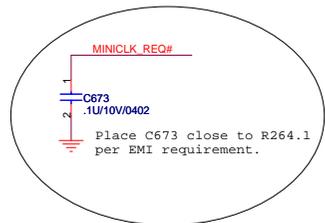
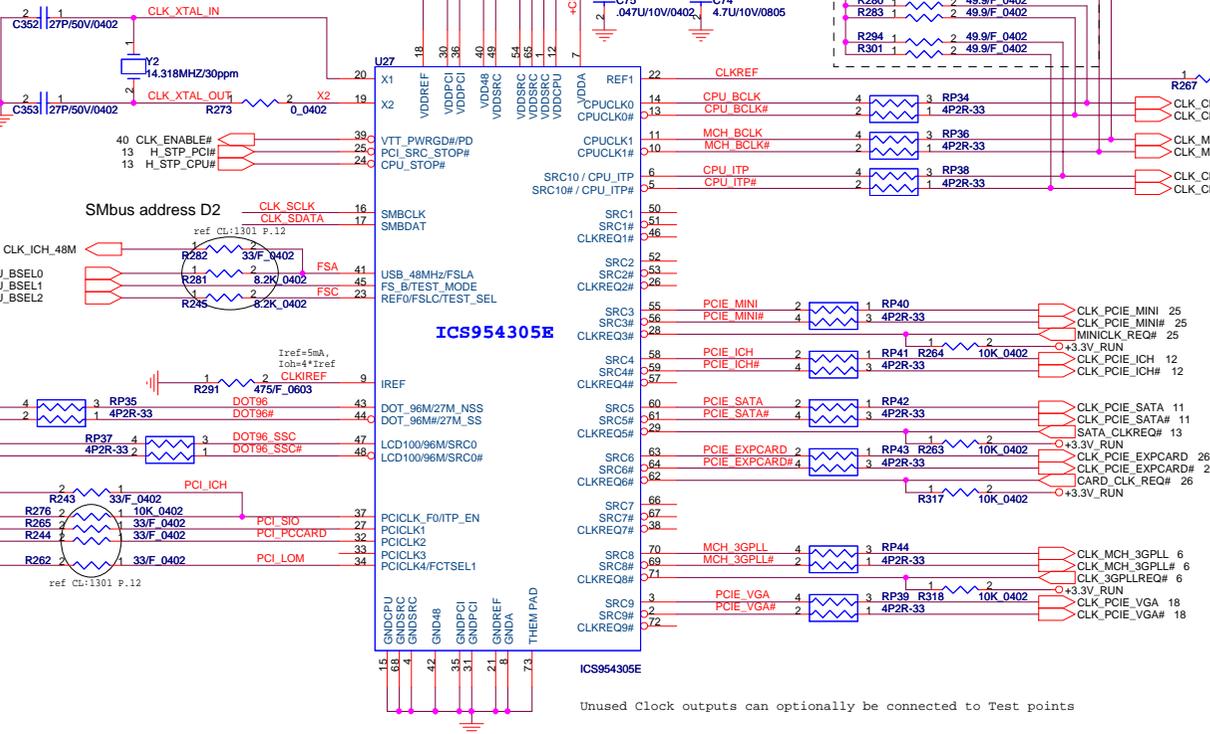
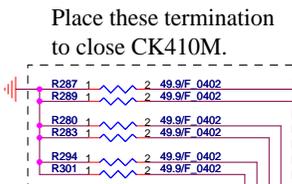
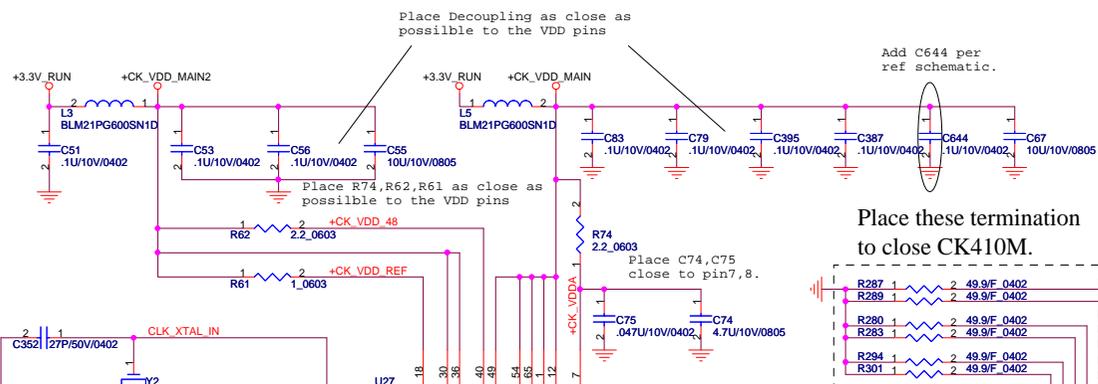
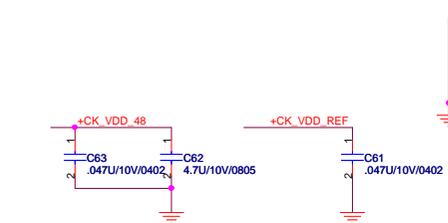


Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V_DDR_VTT

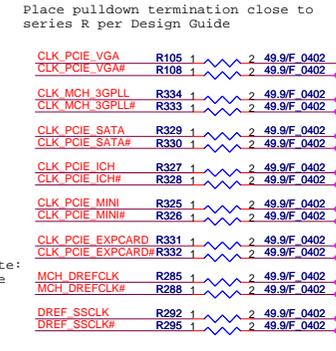
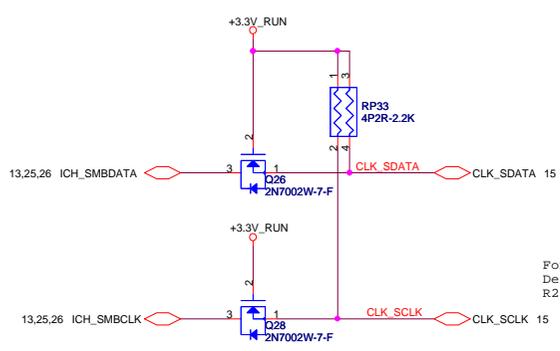


Frequency	bSEL0/FSA	bSEL2/FSC	bSEL1/FSB
100	1	0	1
133	0	0	1
166	0	1	1
200	0	1	0

Trace length between R277, R278 to UJ42 = <50mils



FCTSEL1 (PIN34)	PIN43	PIN44	PIN47	PIN48
0 = UMA	DOT96T	DOT96C	96/100M_T	96/100M_C
1 = Disc. GRFX down	27Mout	27MSSout	SRCT0	SRCC0



These are for backdrive issue

Place these termination to close CK410M.

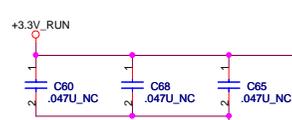
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Size: Document Number FM1 Rev 2A

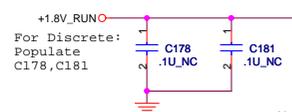
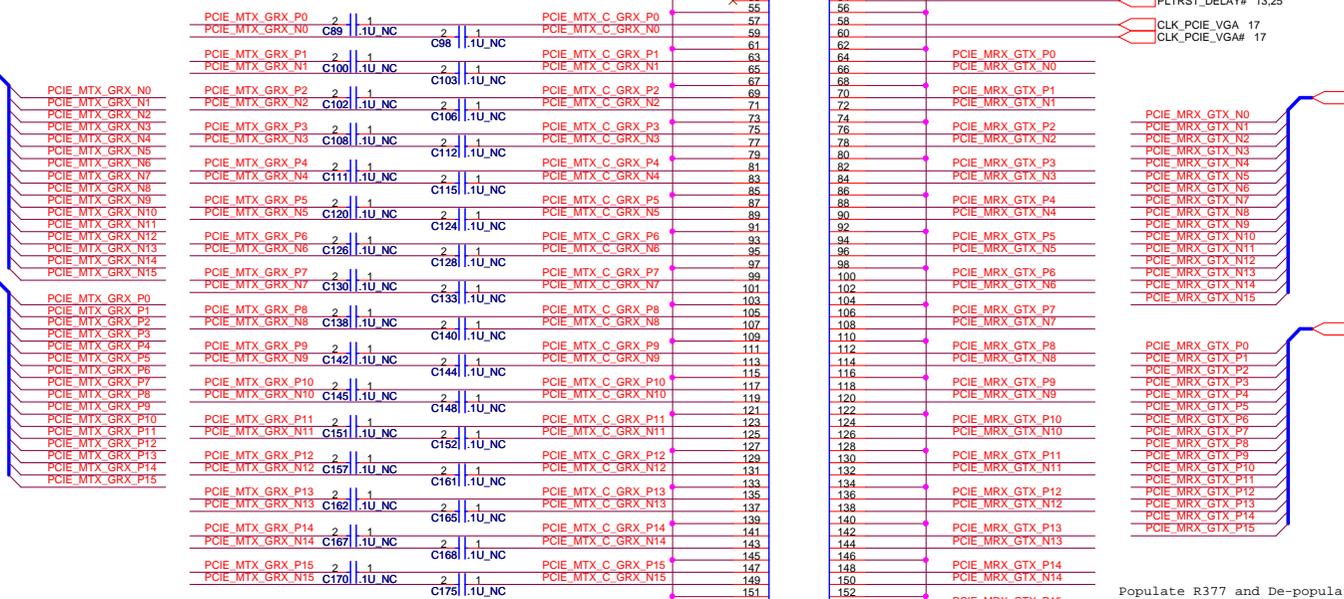
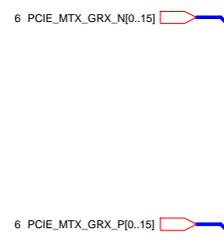
Date: Tuesday, September 06, 2005 Sheet 17 of 51

Populate JVDO1 for discrete. YPRPB_DET: SIGNAL FROM SVIDEO CONNECTOR, TO SWITCH TO COMPONENT OUT.

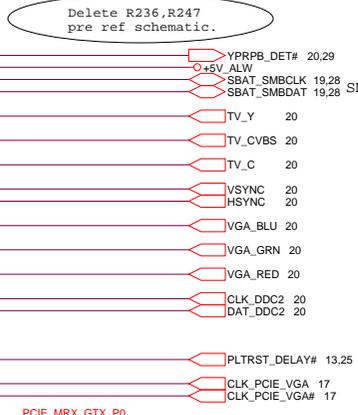


For Discrete: Populate C60,C68,C65

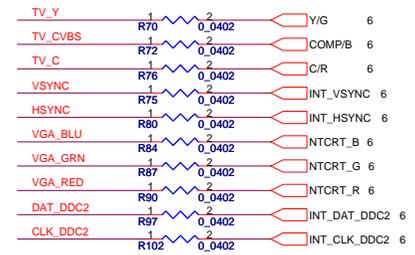
For Discrete: Populate C89,C98,C100,C103,C102,C106,C108,C112,C111,C115,C120,C124,C126,C128,C130,C133,C138,C140,C142,C144,C145,C148,C151,C152,C157,C161,C162,C165,C167,C168,C170,C175



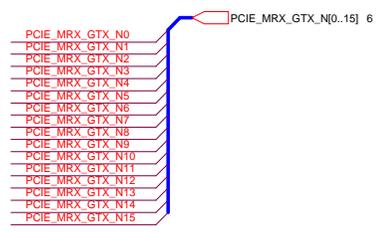
For Discrete: Populate C178,C181



Delete R236,R247 pre ref schematic.

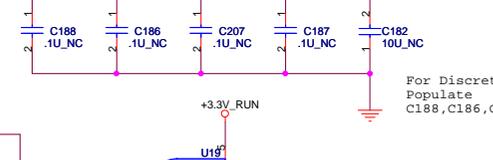
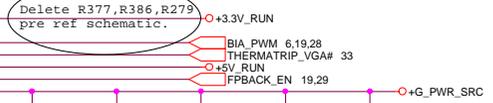


For Discrete: De-populate R70,R72,R76,R75,R80,R84,R87,R90,R97,R02

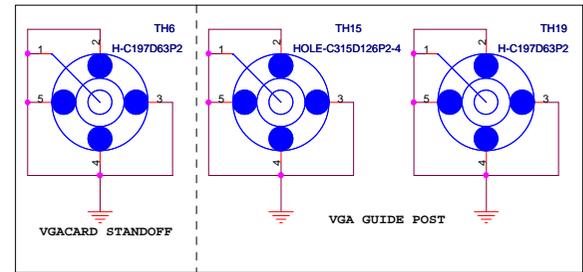


Populate R377 and De-populate R386, R279. for Protocol build(old VGA card)

Delete R377,R386,R279 pre ref schematic.



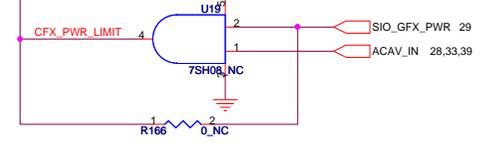
For Discrete: Populate C188,C186,C207,C187,C182,U19



For Discrete: Populate TH6,TH15,TH19

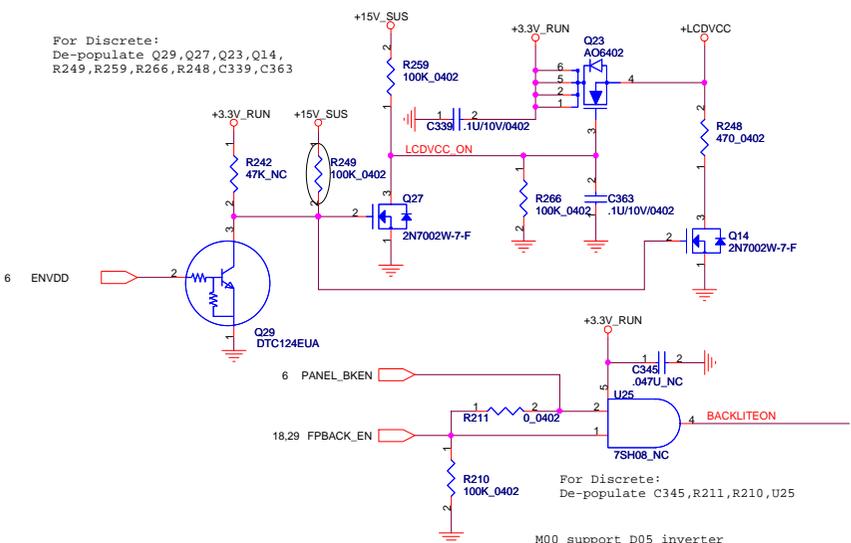
TOP Side

HONDA LFP-SC200SMYGA+_NC

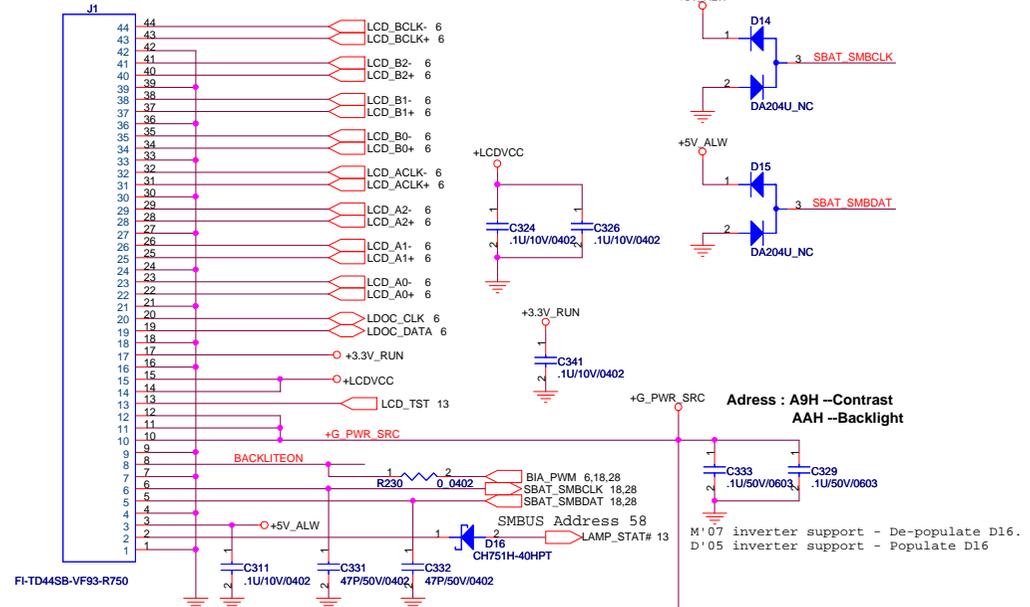
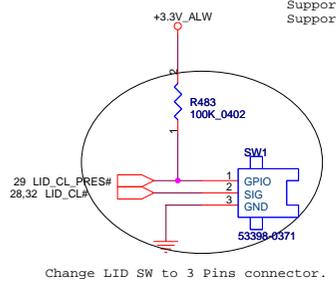


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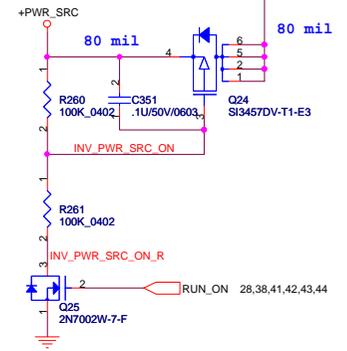
For Discrete:
De-populate Q29, Q27, Q23, Q14,
R249, R259, R266, R248, C339, C363

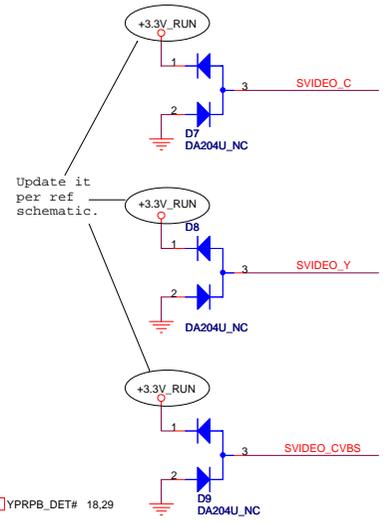
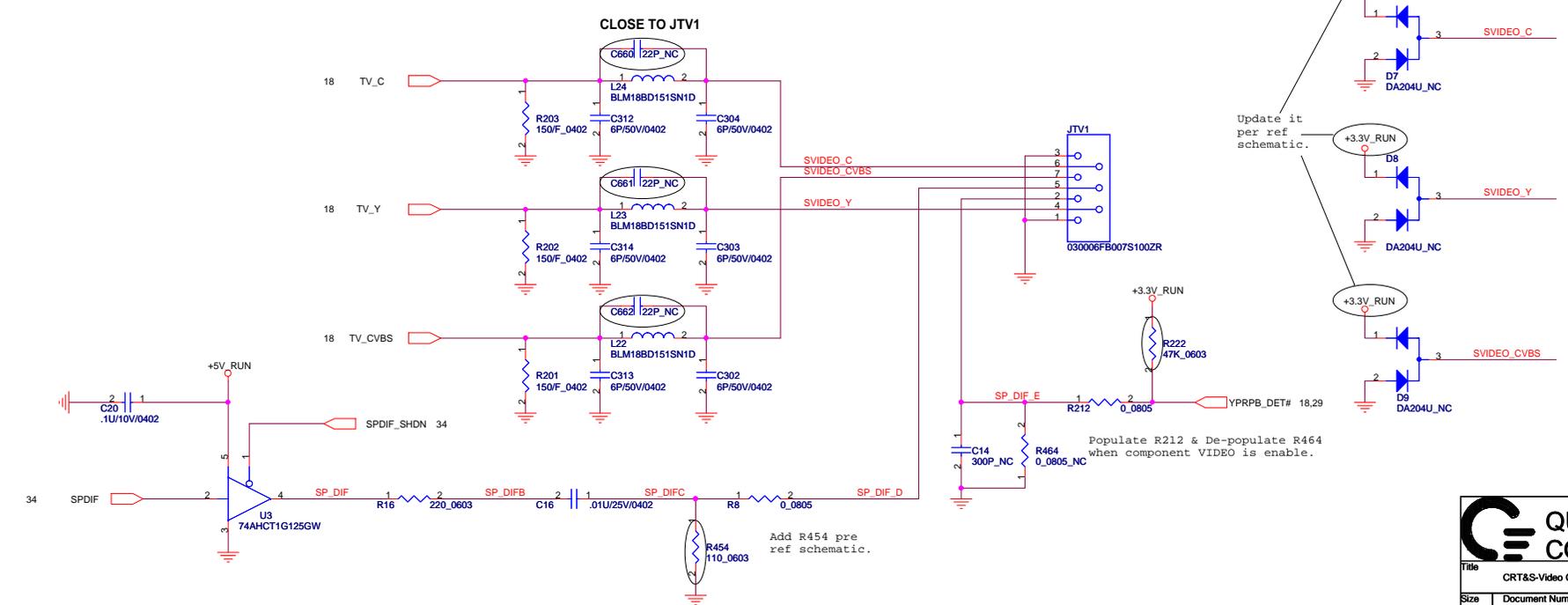
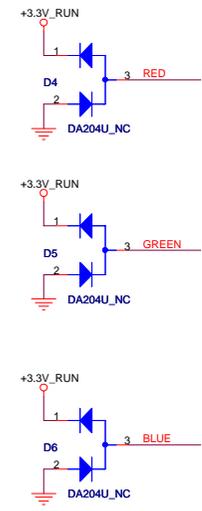
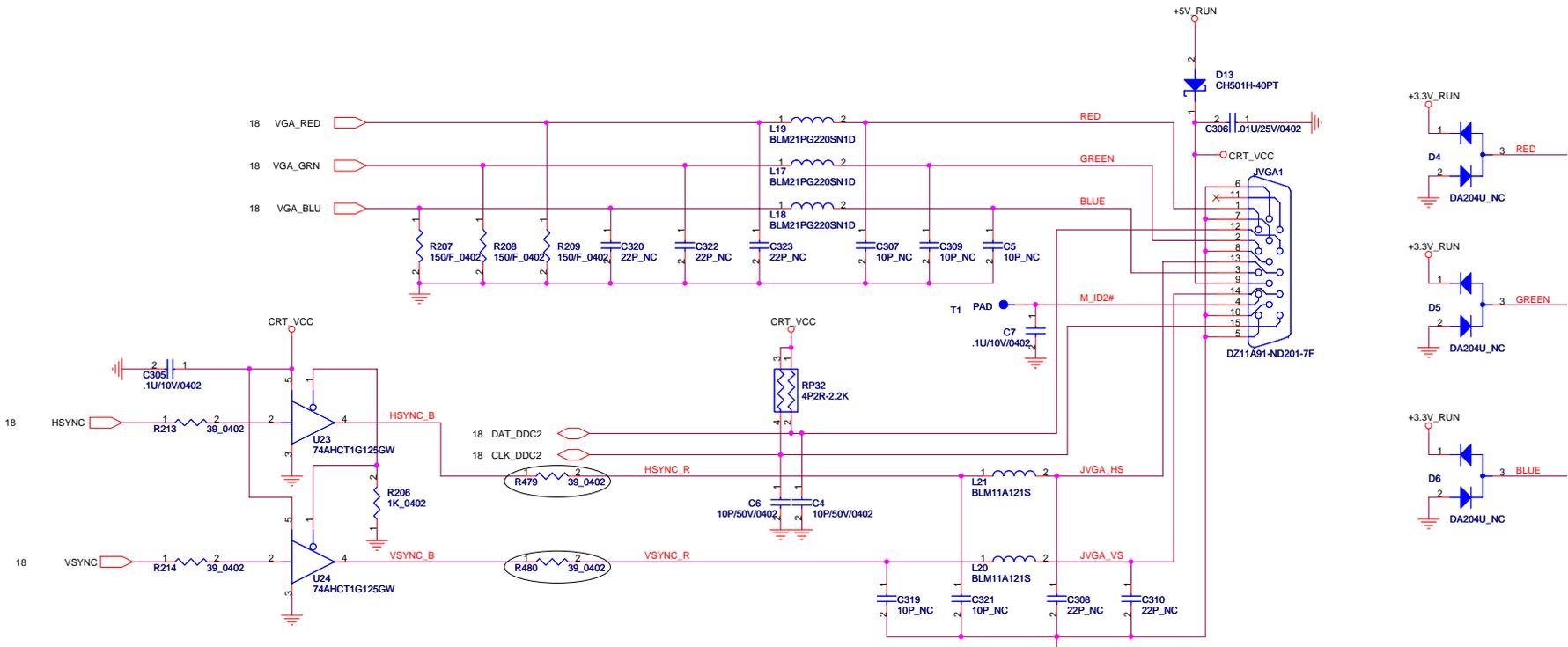


M00 support D05 inverter
Support M07-Inverter: Populate R230, R211 and Depopulate U8, C345.
Support D05-Inverter: Depopulate R230, R211 and Populate U8, C345.



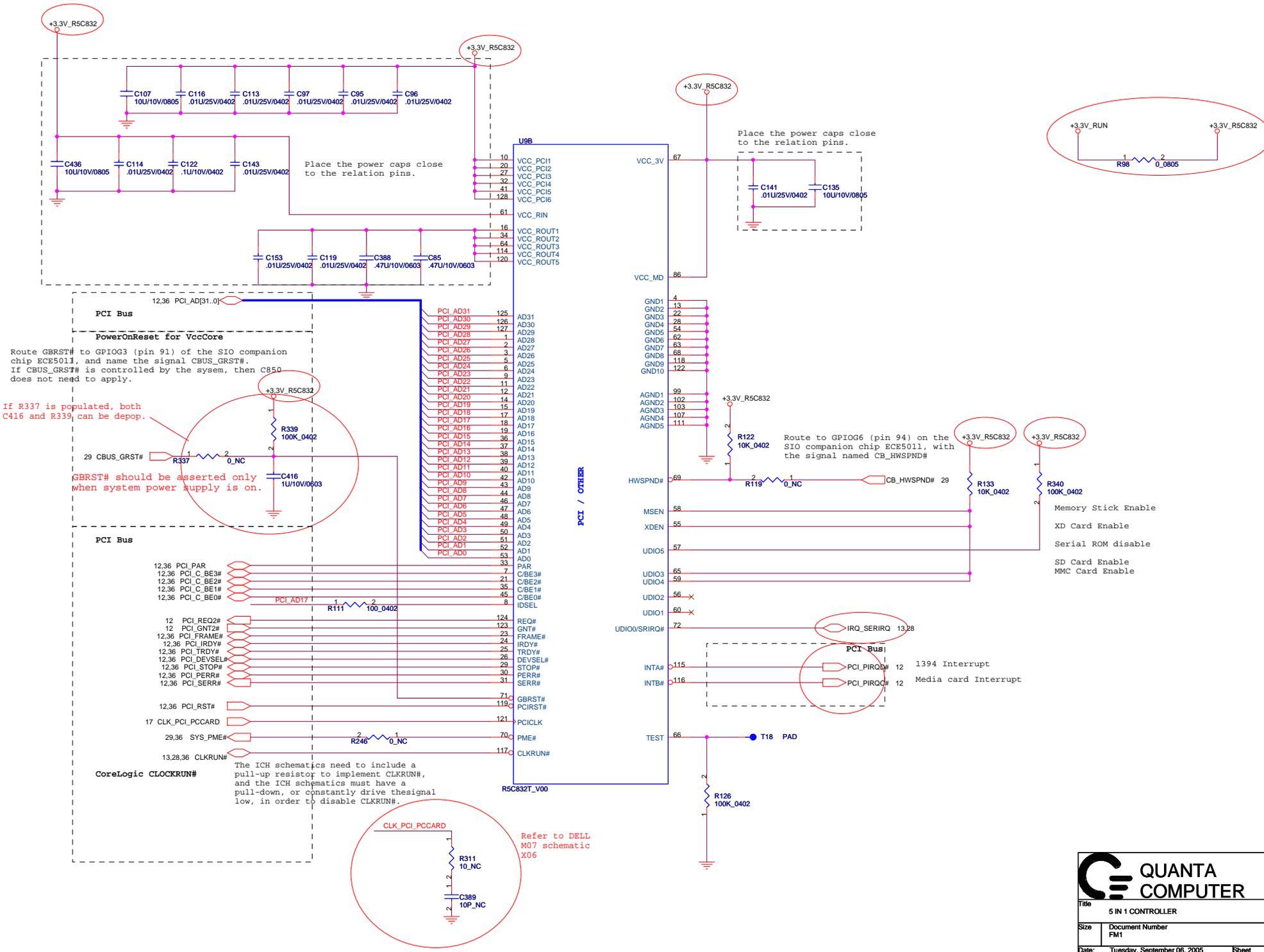
For Discrete:
De-populate J1, R230, C311, C331, C332, D16, C333, C329, C341, C324, C326





Update it per ref schematic.

Populate R212 & De-populate R464 when component VIDEO is enable.

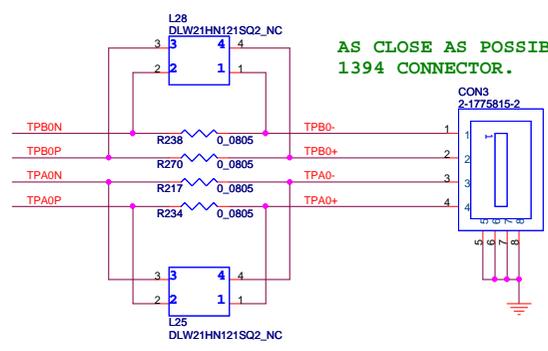
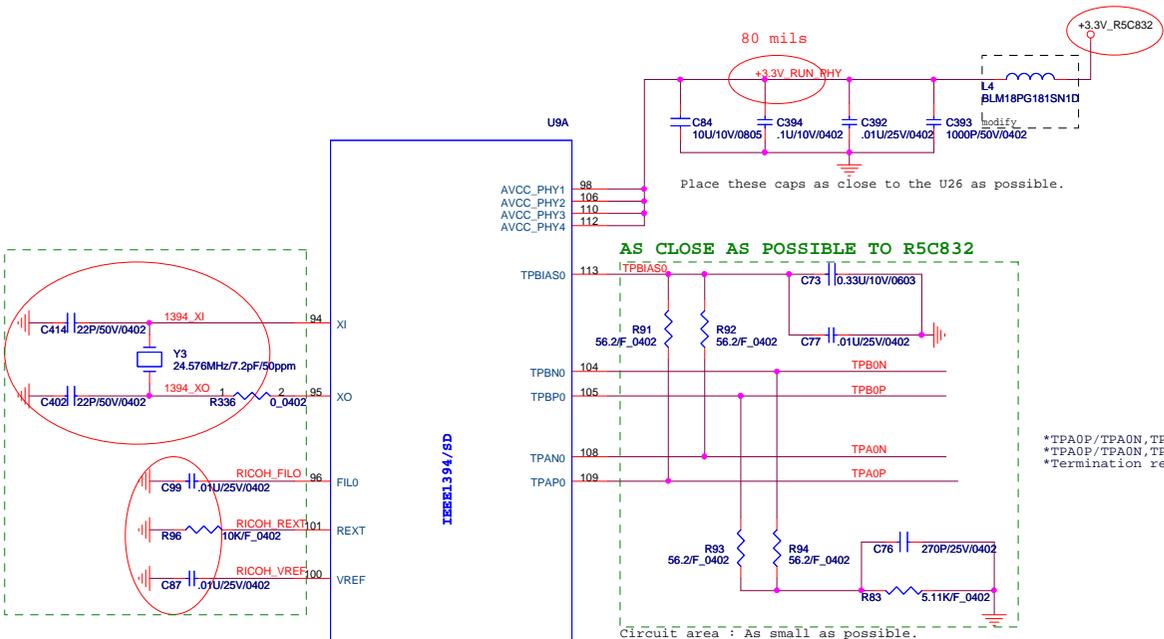


QUANTA COMPUTER

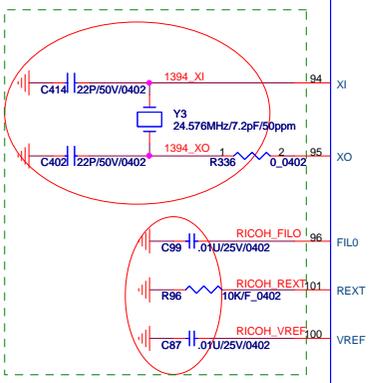
Title: 5 IN 1 CONTROLLER

Size	Document Number	Rev
	FM1	2A

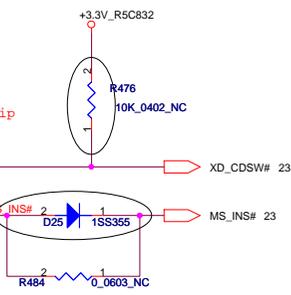
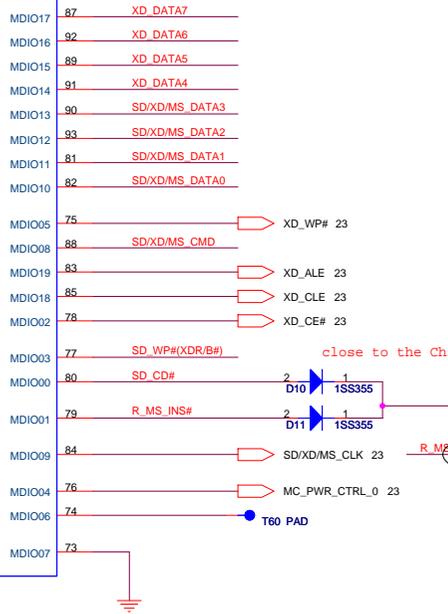
Date: Tuesday, September 06, 2005 Sheet 21 of 51

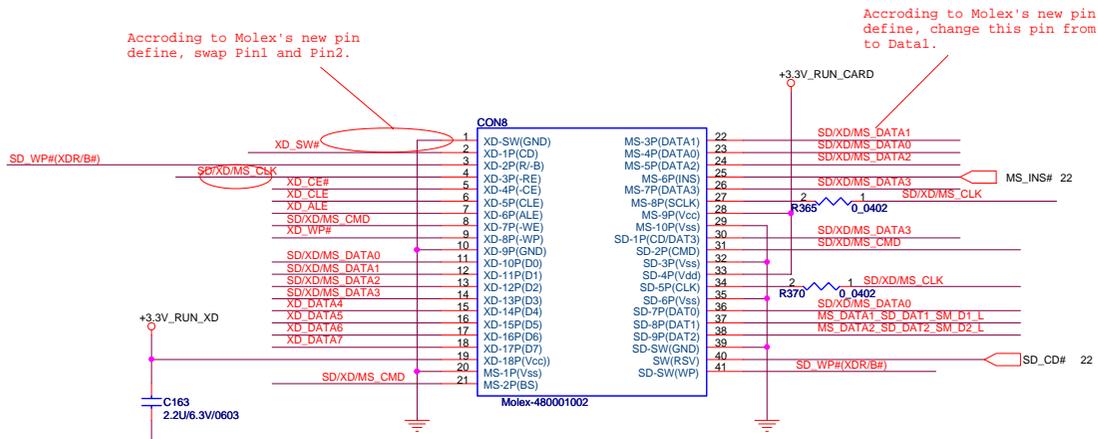


*TPA0P/TPA0N,TPB0P/TPB0N pair trace : As close as possible.
 *TPA0P/TPA0N,TPB0P/TPB0N pair trace : Same length electrically.
 *Termination resistor for TPA+/- TPB+/- : As close as possible to its cable driver (device pin out).



Place these caps as close to the U26 as possible.

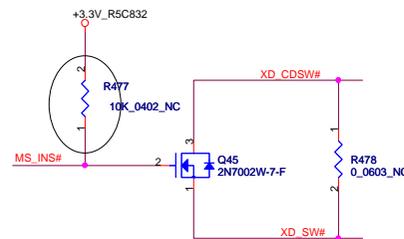




5 IN1 CARD READER

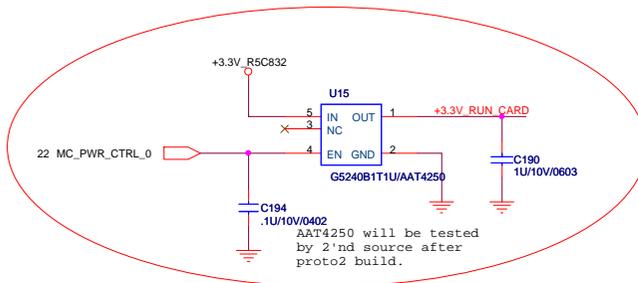
Refer to M07, connect C163 to +3VRUN_XD.

- 22 XD_CDSW#
- 22 SD_WP#(XDR/B#)
- 22 XD_DATA7
- 22 XD_DATA6
- 22 XD_DATA5
- 22 XD_DATA4
- 22 SD/XD/MS_DATA3
- 22 SD/XD/MS_DATA2
- 22 SD/XD/MS_DATA1
- 22 SD/XD/MS_DATA0
- 22 SD/XD/MS_CMD
- 22 XD_WP#
- 22 XD_ALE
- 22 XD_CLE
- 22 XD_CE#
- 22 SD/XD/MS_CLK

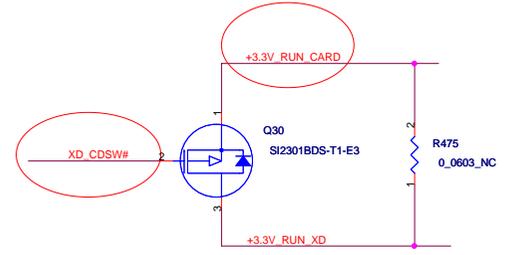
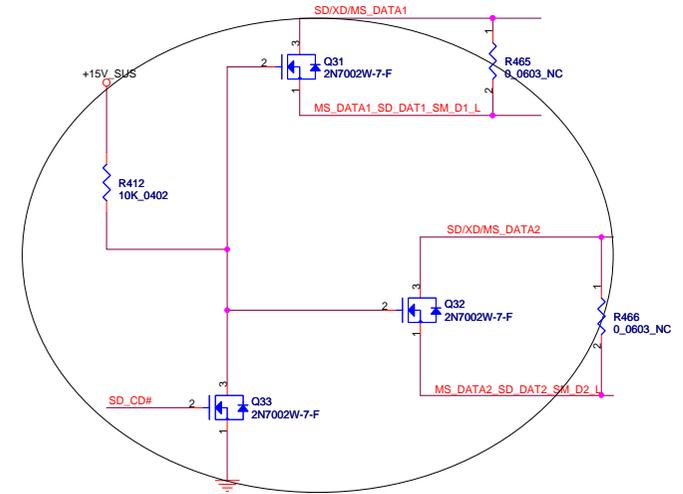
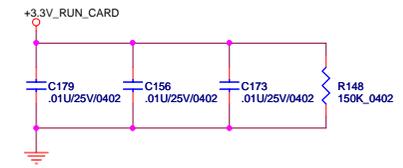


For SD/MS power

For XD power



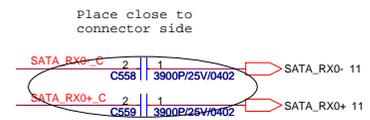
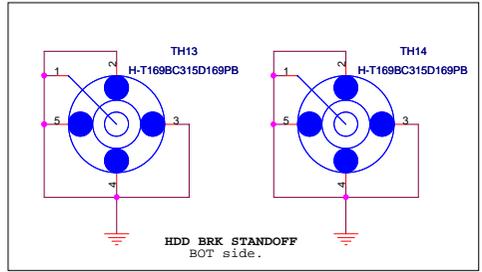
AAT4250 will be tested by 2'nd source after proto2 build.



QUANTA COMPUTER

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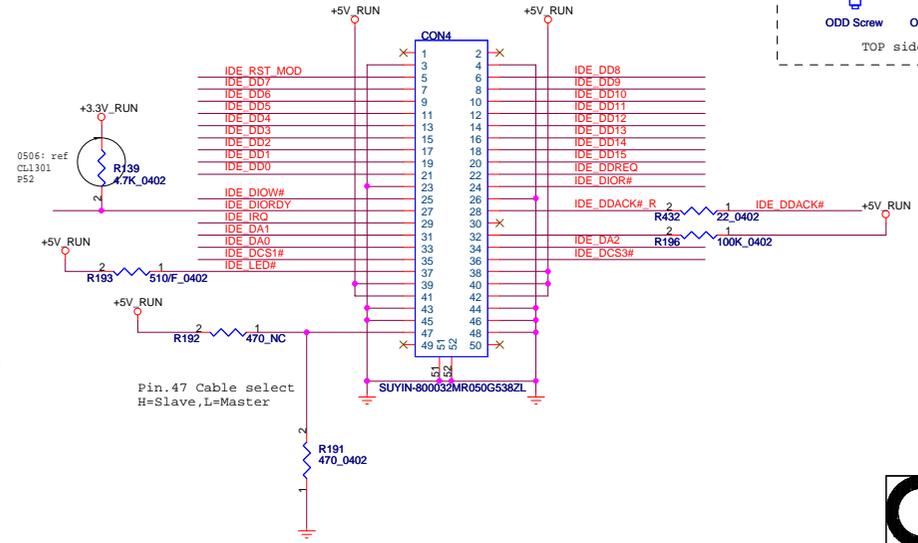
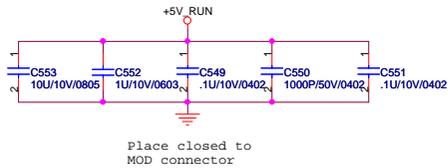
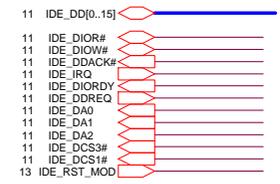
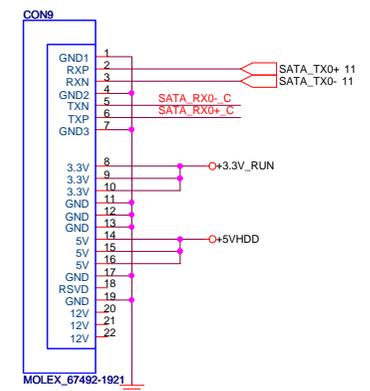
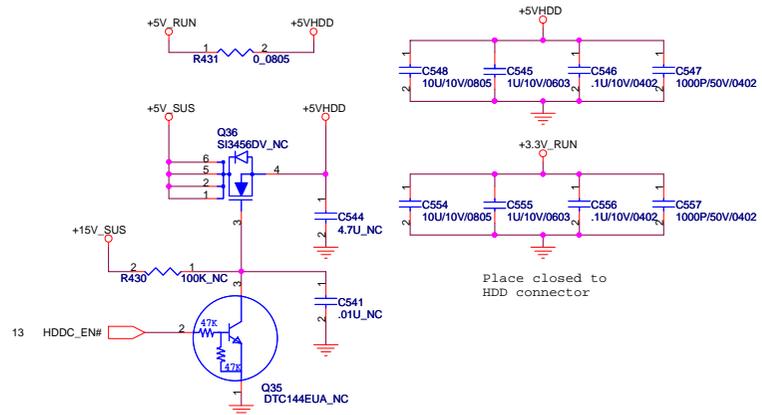
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Date: Tuesday, September 06, 2005	Sheet: 23	of 51

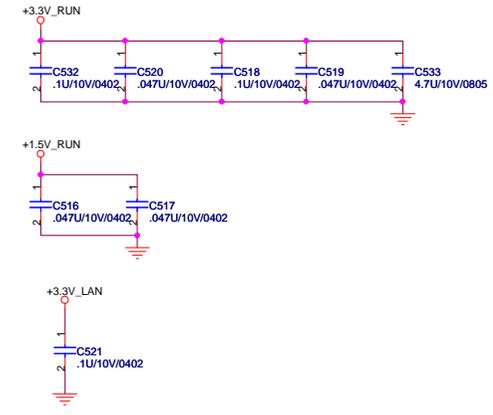
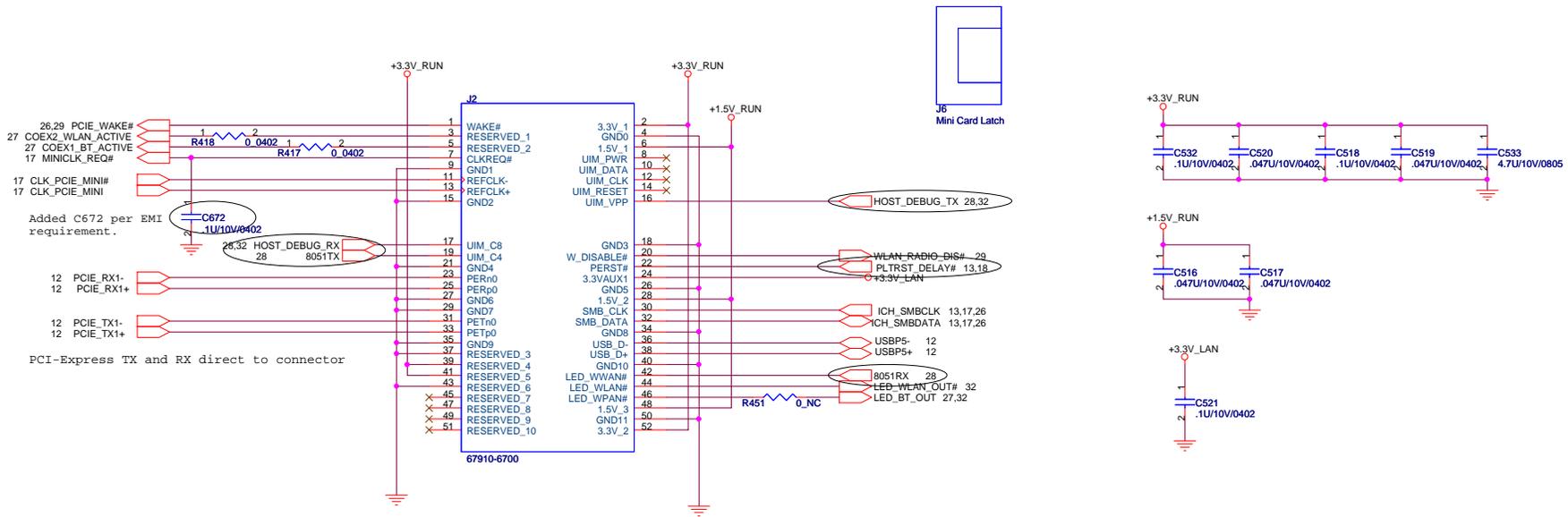


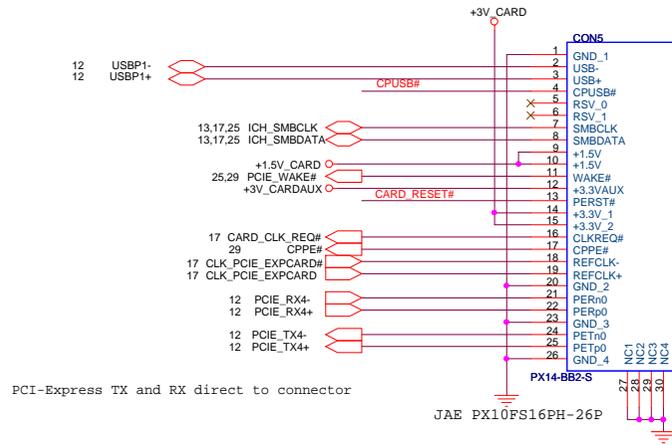
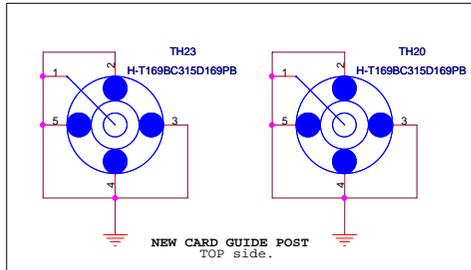
Locate caps C558, C559 near HDD Conn.
Length match SATA_C_RX0- & SATA_C_RX0+ within 20mils.

SATA drive vendors will use only 5V supply from the system and will derive 3.3V on the drive. If drive power goals are not achieved, drive vendors will use both 5V and 3.3V supplies from the system. Initial power saving using 3.3V from system is less than 5%.

Power Estimate:
SATA drive power consumption estimate at MobileMark is 1.1W. An additional 150mW can be saved using Intel's IMST driver.

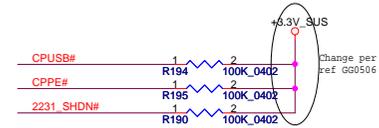
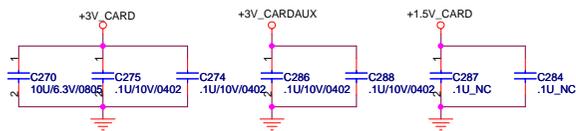




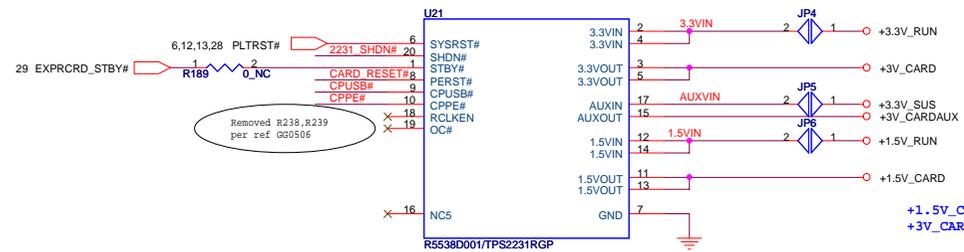


PCI-Express TX and RX direct to connector

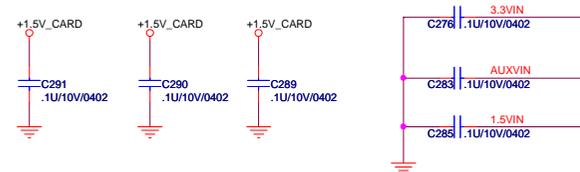
JAE PX10FS16PH-26P



+1.5V_CARD Max. 650mA, Average 500mA
+3V_CARD Max. 1300mA, Average 1000mA

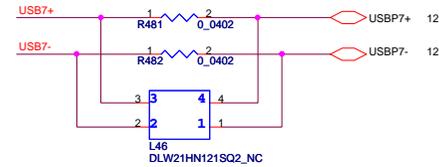
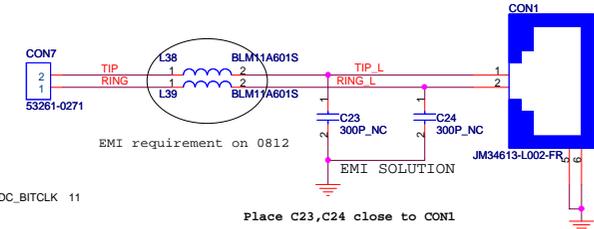
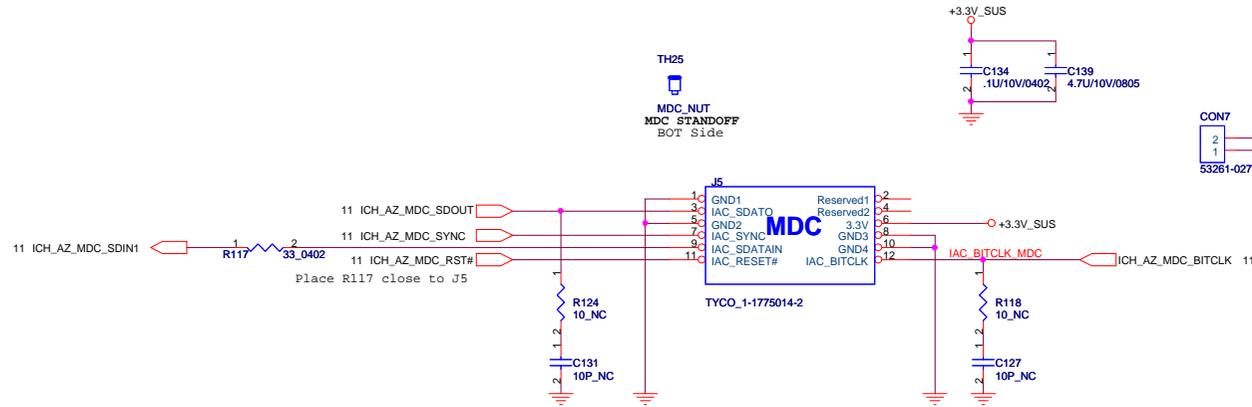


+1.5V_CARD Max. 650mA, Average 500mA
+3V_CARD Max. 1300mA, Average 1000mA

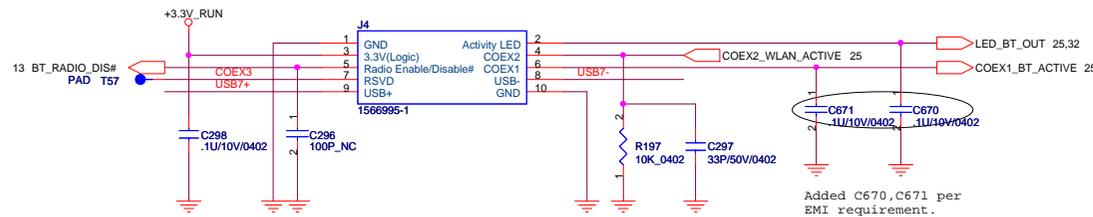


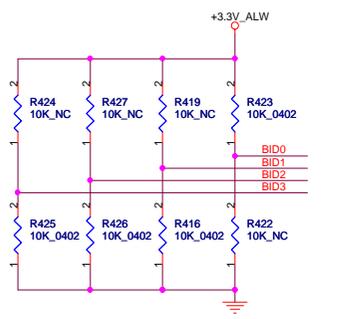
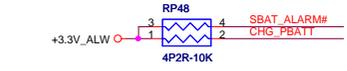
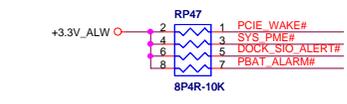
MDC Layout Notes

1. Tip and Ring trace width = 25 mils
2. Spacing between Tip and Ring = 25 mils
3. Tip and Ring connector pitch = 25 mils
4. Keep out area from Tip and Ring to other signals = 100 mils
5. Power and Ground minimum trace width to connector = 20 mils
6. Route Tip and Ring on one layer only (top or bottom)
7. Modem internal cable wire size = 26 AWG (stranded or twisted pair wire)

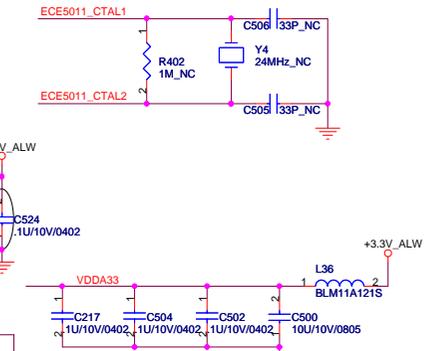
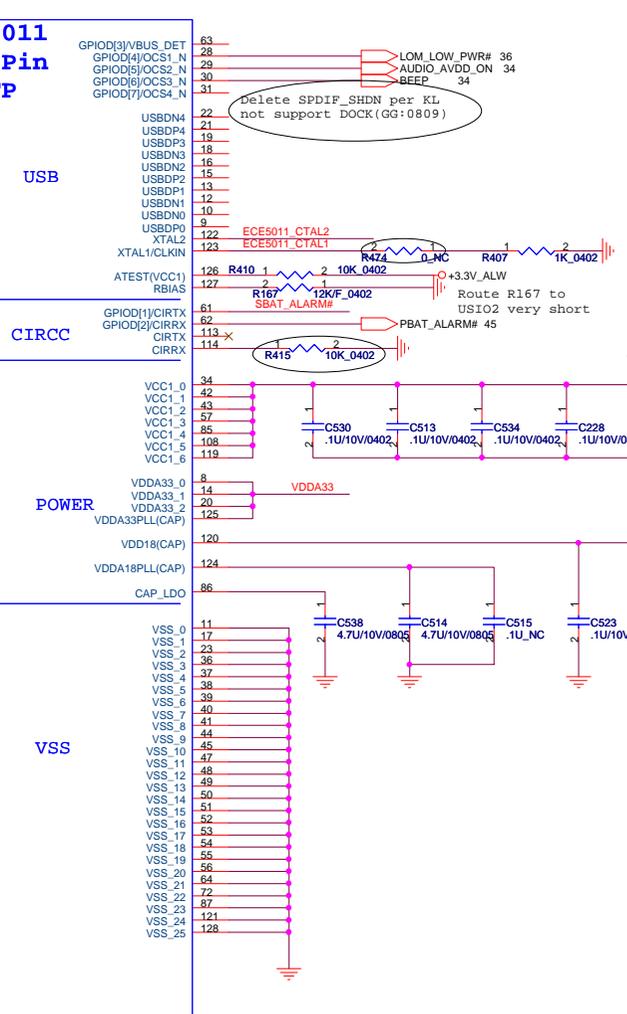
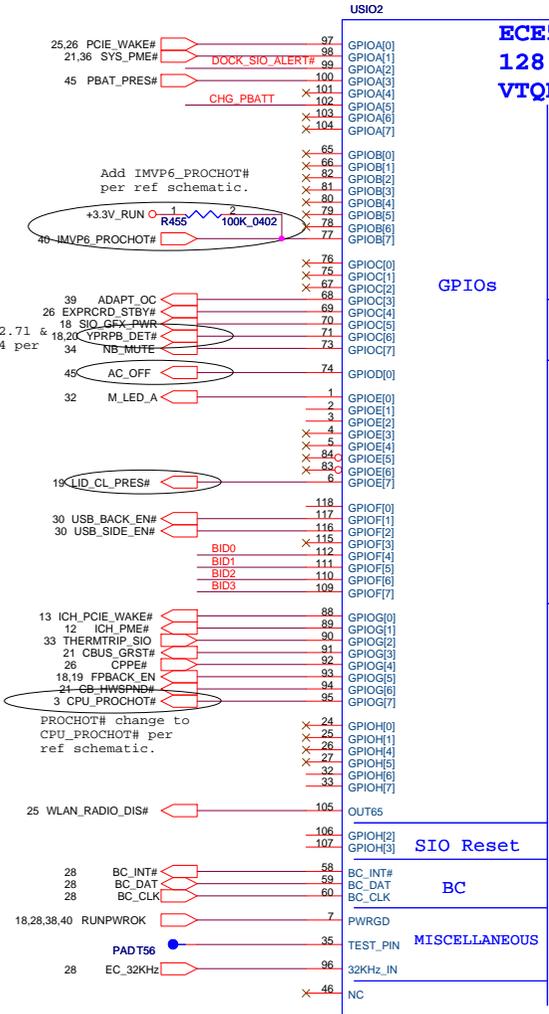


Bluetooth

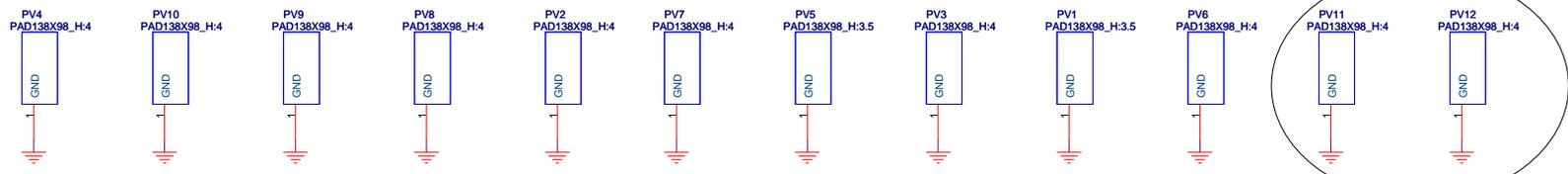
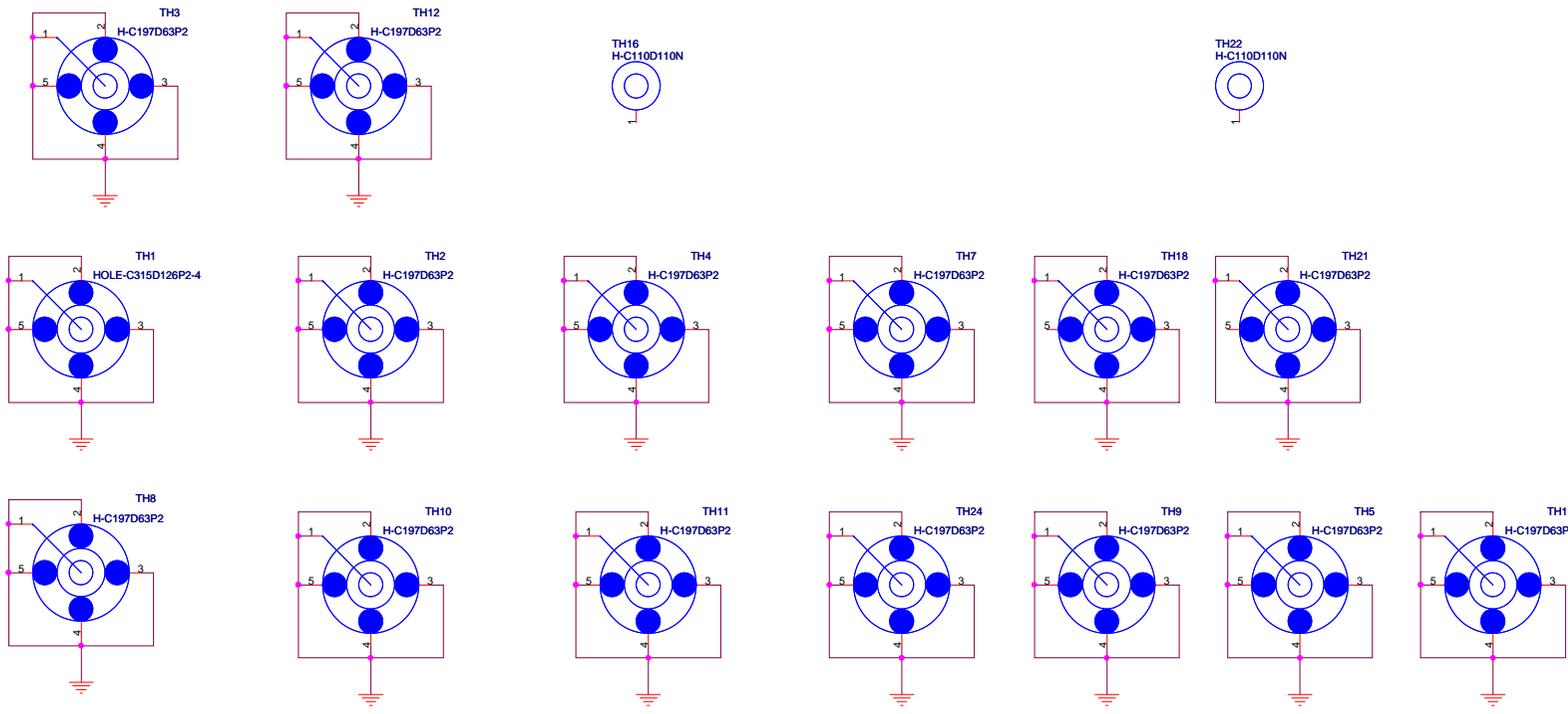




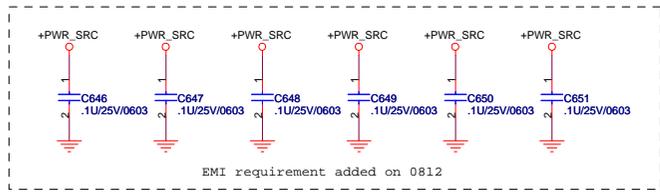
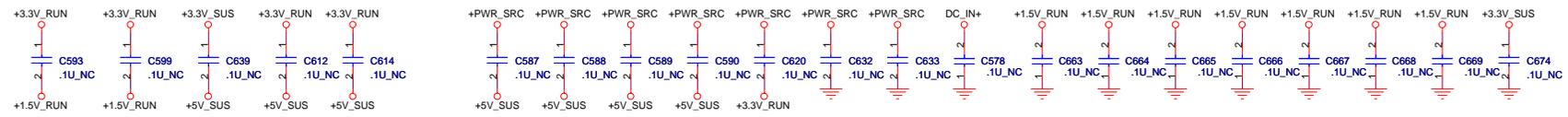
BID3	BID2	BID1	BID0	Board Revision
0	0	0	0	PROTO1 (X00)
0	0	0	1	PROTO2 (X01)
0	0	1	0	PROTO3 (X02)
0	0	1	1	QT(X03)
0	1	0	0	A00 PVB/A01 PWA



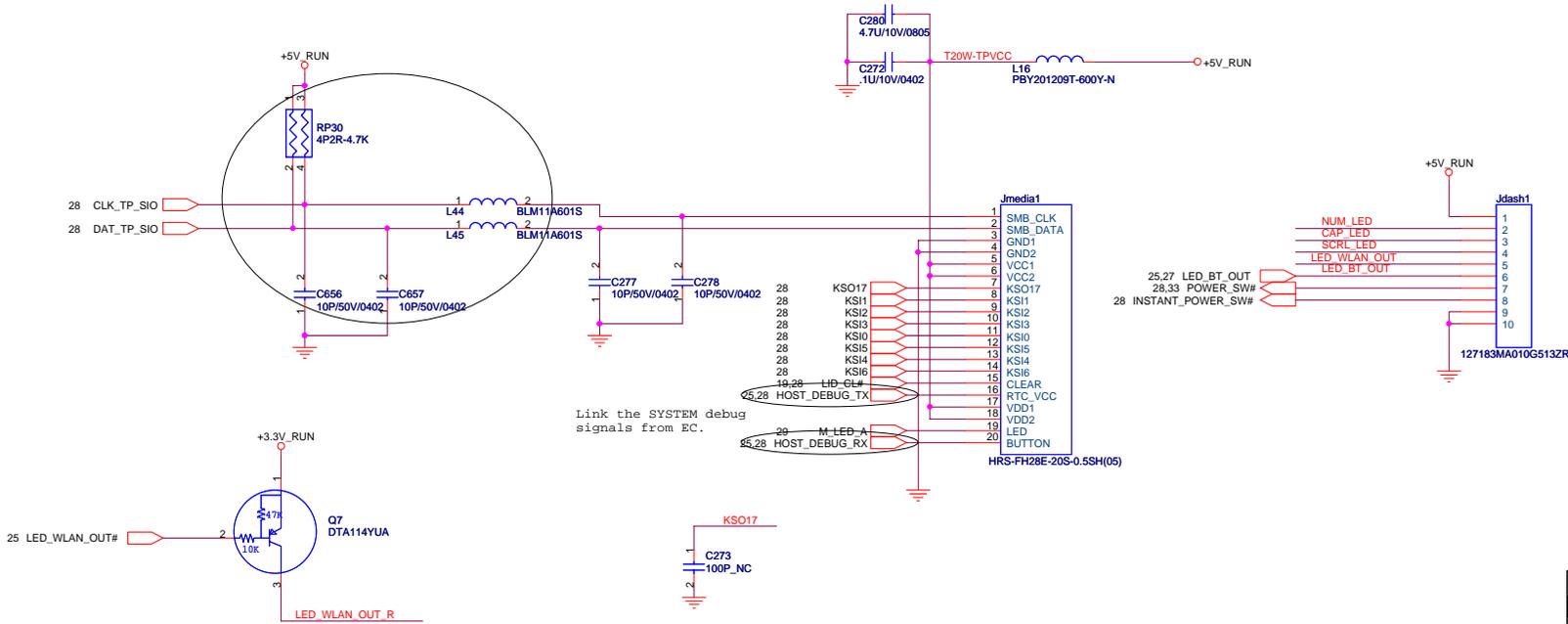
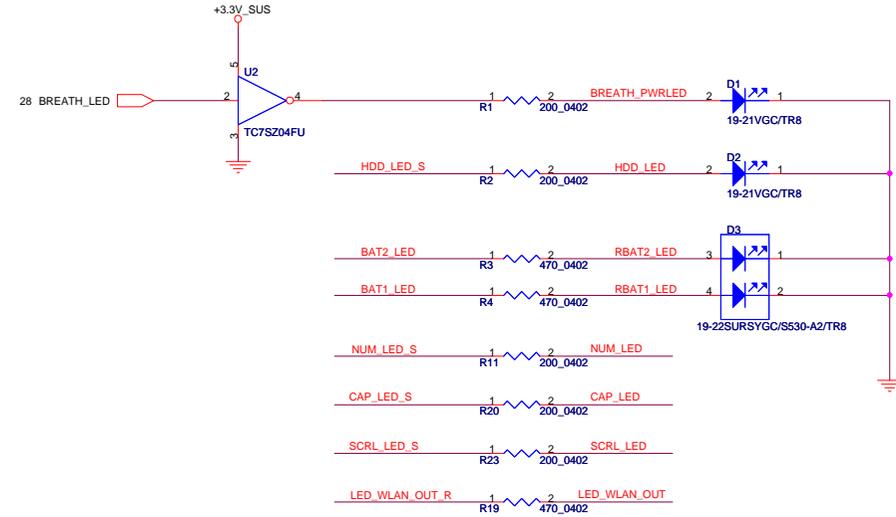
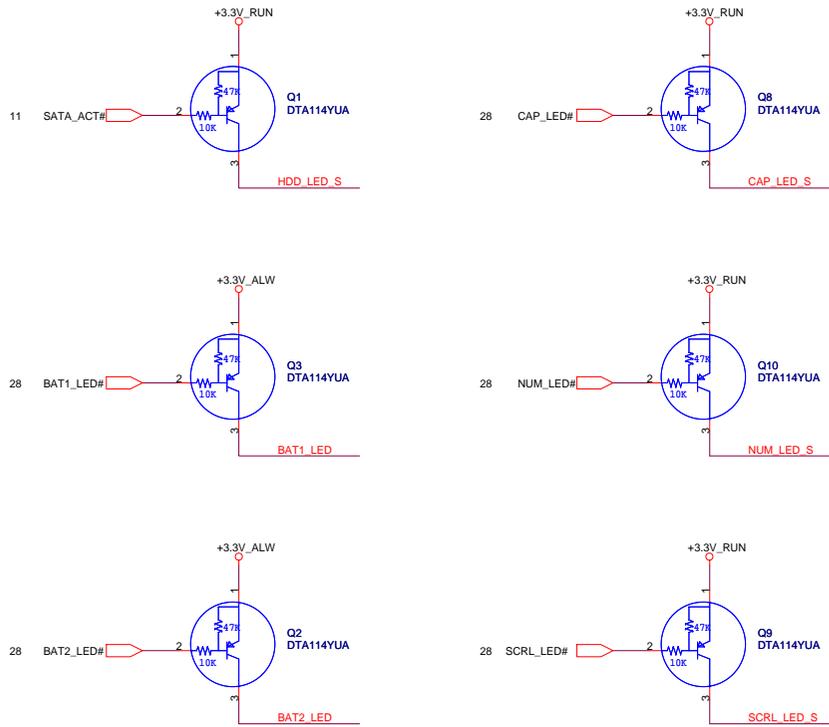
ECE5011-NU

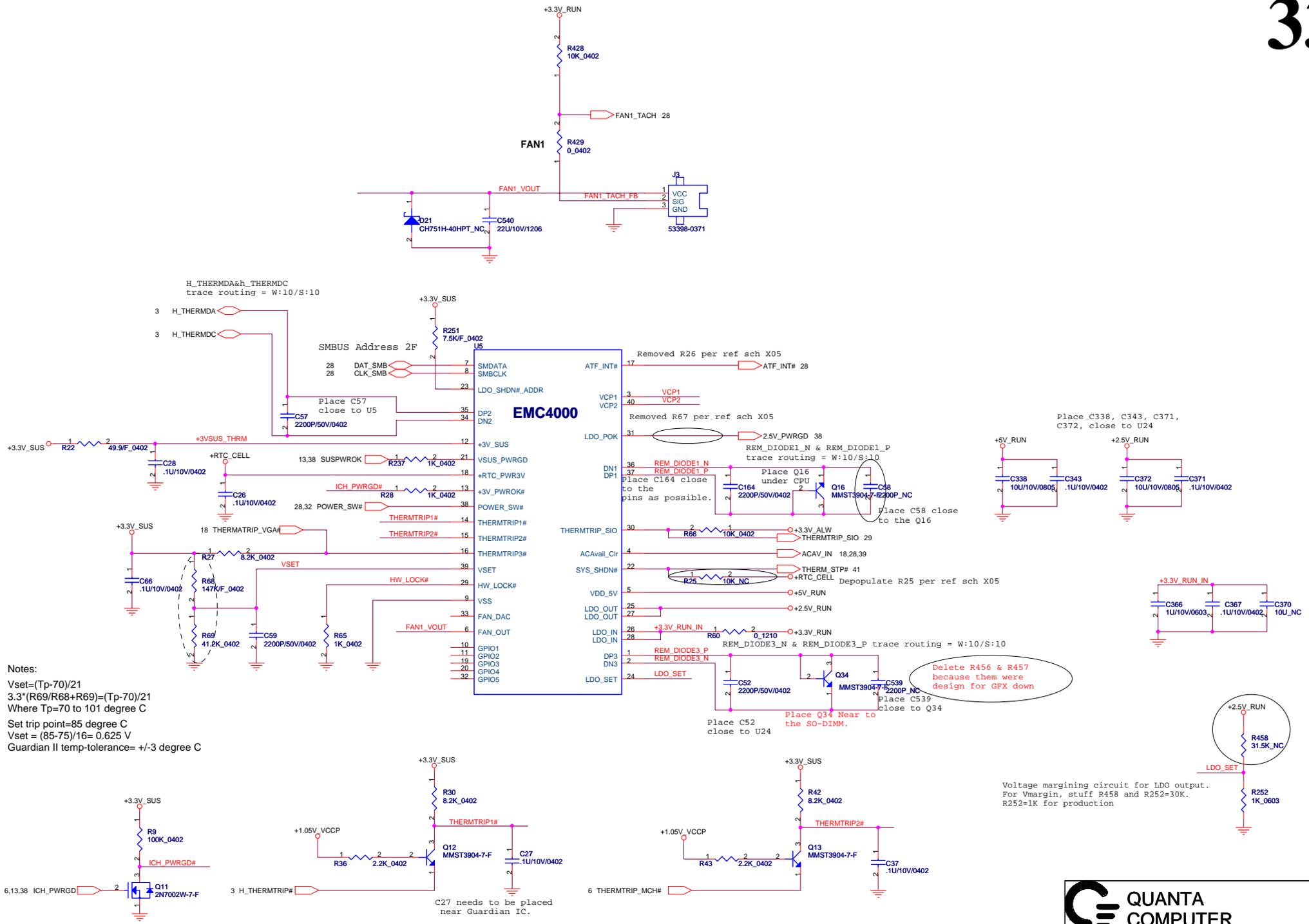


EMI requirement added on 0812

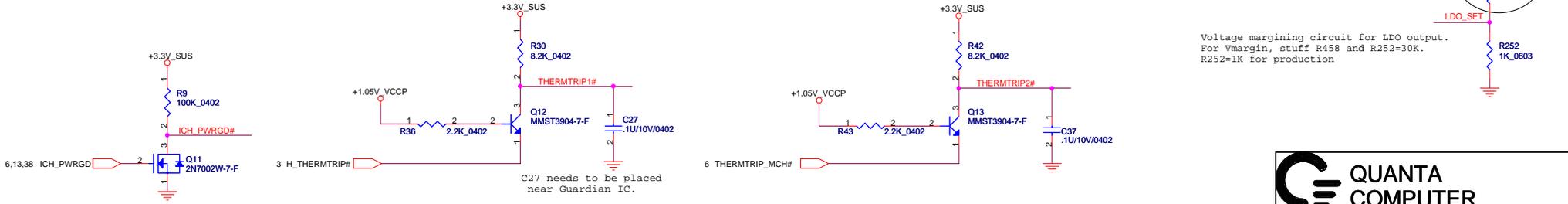


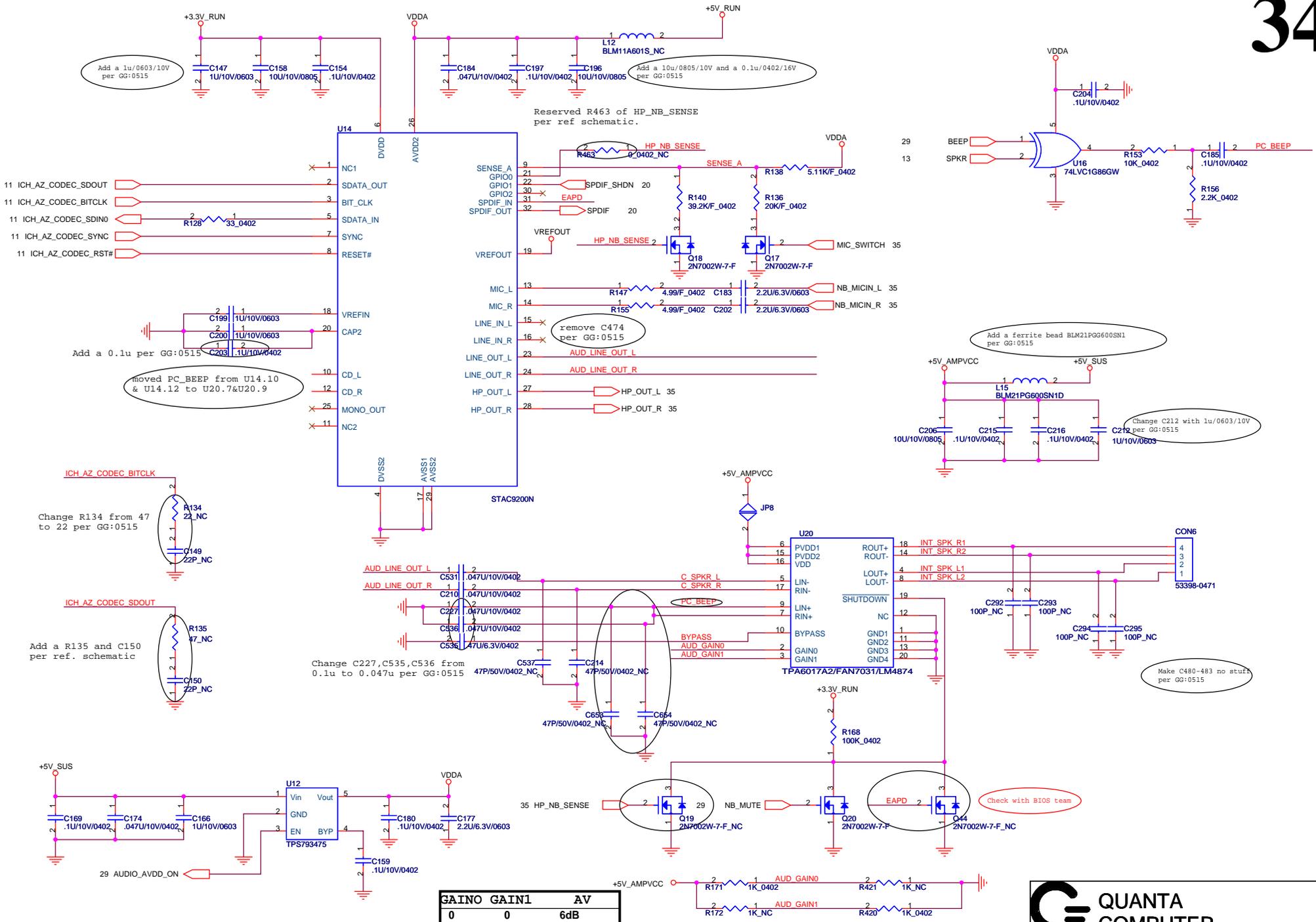
QUANTA COMPUTER
 Title: EMI & Screw hole
 Size: Document Number FM1 Rev 2A
 Date: Tuesday, September 06, 2005 Sheet 31 of 51





Notes:
 $V_{set} = (T_p - 70) / 21$
 $3.3 \cdot (R_{69} / R_{68} + R_{69}) = (T_p - 70) / 21$
 Where $T_p = 70$ to 101 degree C
 Set trip point = 85 degree C
 $V_{set} = (85 - 75) / 16 = 0.625$ V
 Guardian II temp-tolerance = ± 3 degree C





Add a 1u/0603/10V per GG:0515

Add a 10u/0805/10V and a 0.1u/0402/16V per GG:0515

Add a 0.1u per GG:0515

moved PC_BEEP from U14.10 & U14.12 to U20.7&U20.9

Change R134 from 47 to 22 per GG:0515

Add a R135 and C150 per ref. schematic

Change C227, C535, C536 from 0.1u to 0.047u per GG:0515

Add a ferrite bead BLM21PG600SN1 per GG:0515

Change C212 with 1u/0603/10V per GG:0515

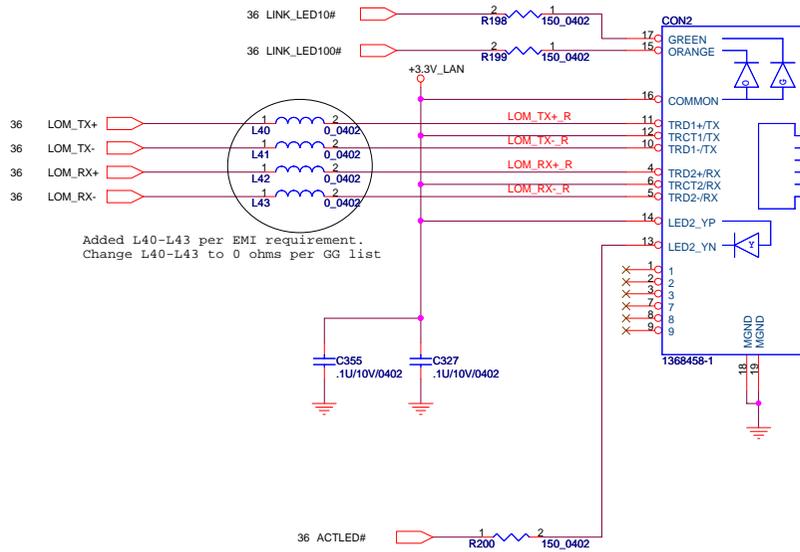
Make C480-483 no stuff per GG:0515

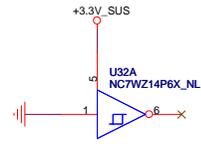
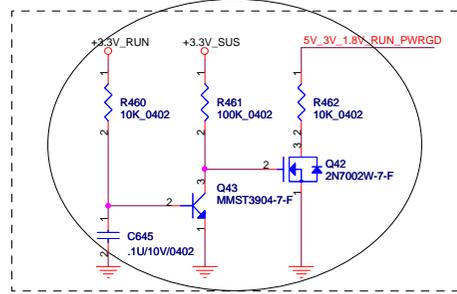
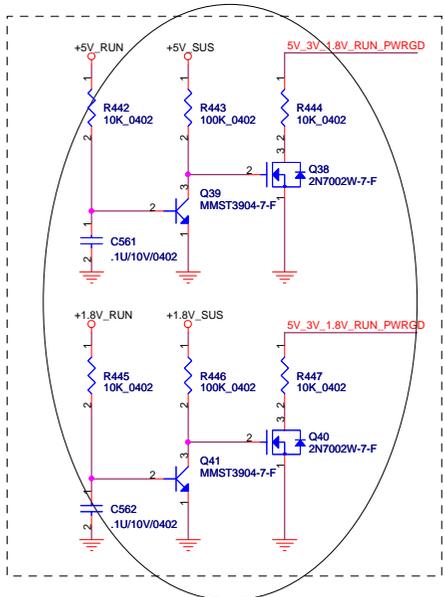
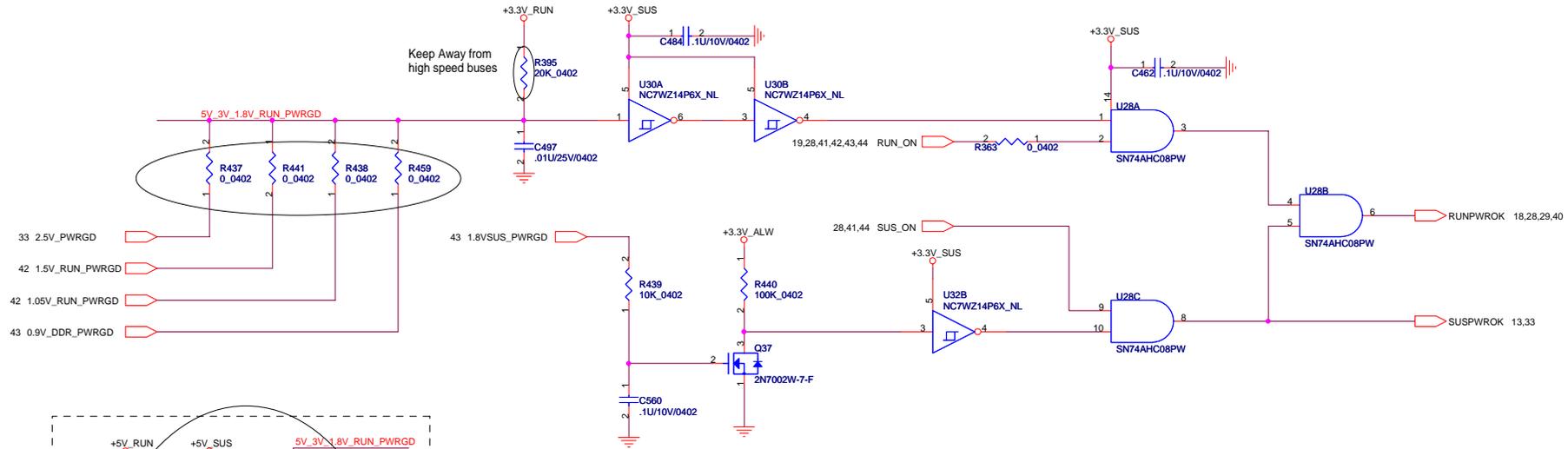
Check with BIOS team

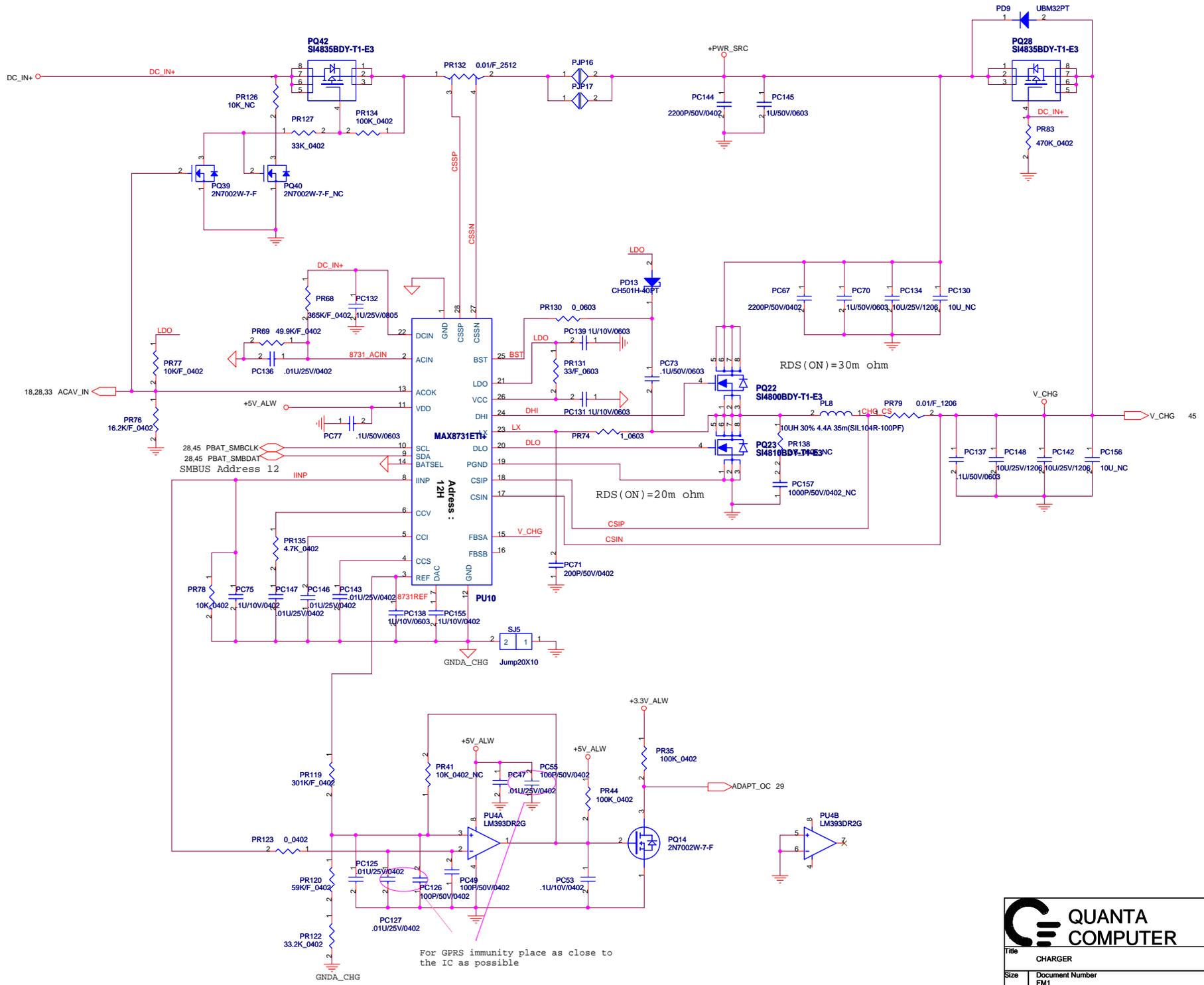
Change RP55 from 100K to 1k per ref. schematic

GAIN0	GAIN1	AV
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

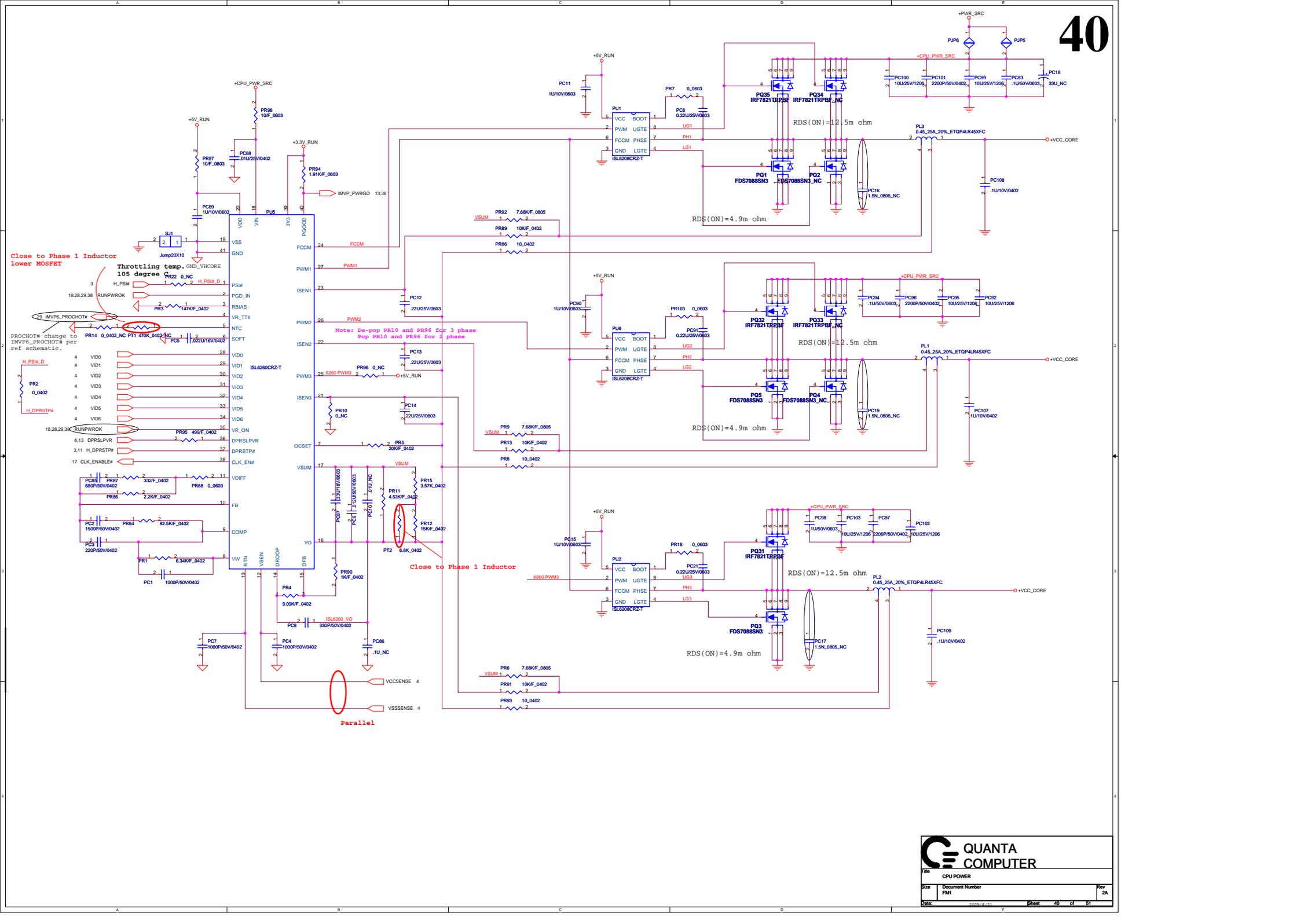








For GPRS immunity place as close to the IC as possible



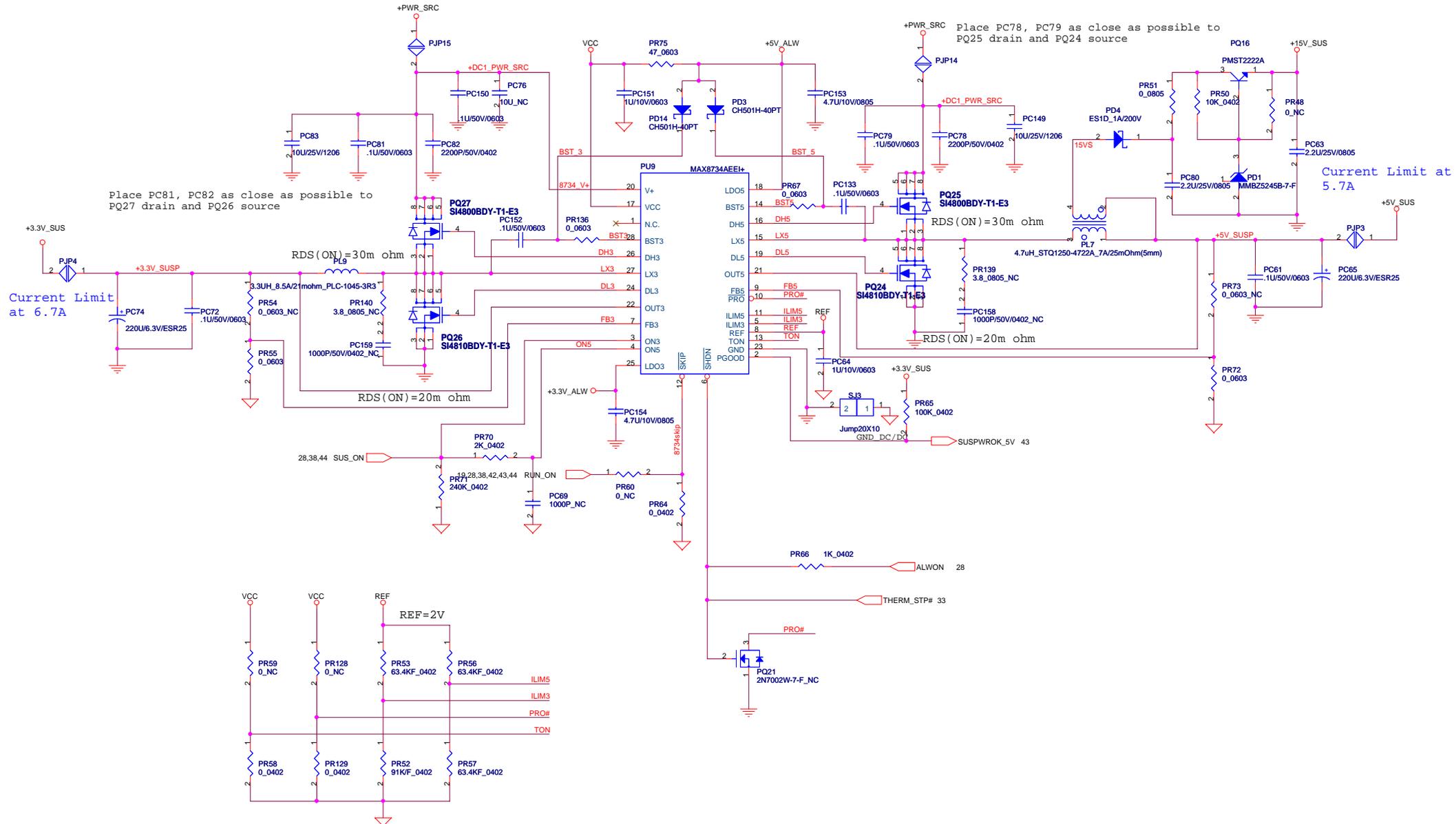
Close to Phase 1 Inductor lower MOSFET

Throttling temp. 105 degree

Note: De-pop PR10 and PR96 for 3 phase Pop PR10 and PR96 for 2 phase

Close to Phase 1 Inductor

Parallel



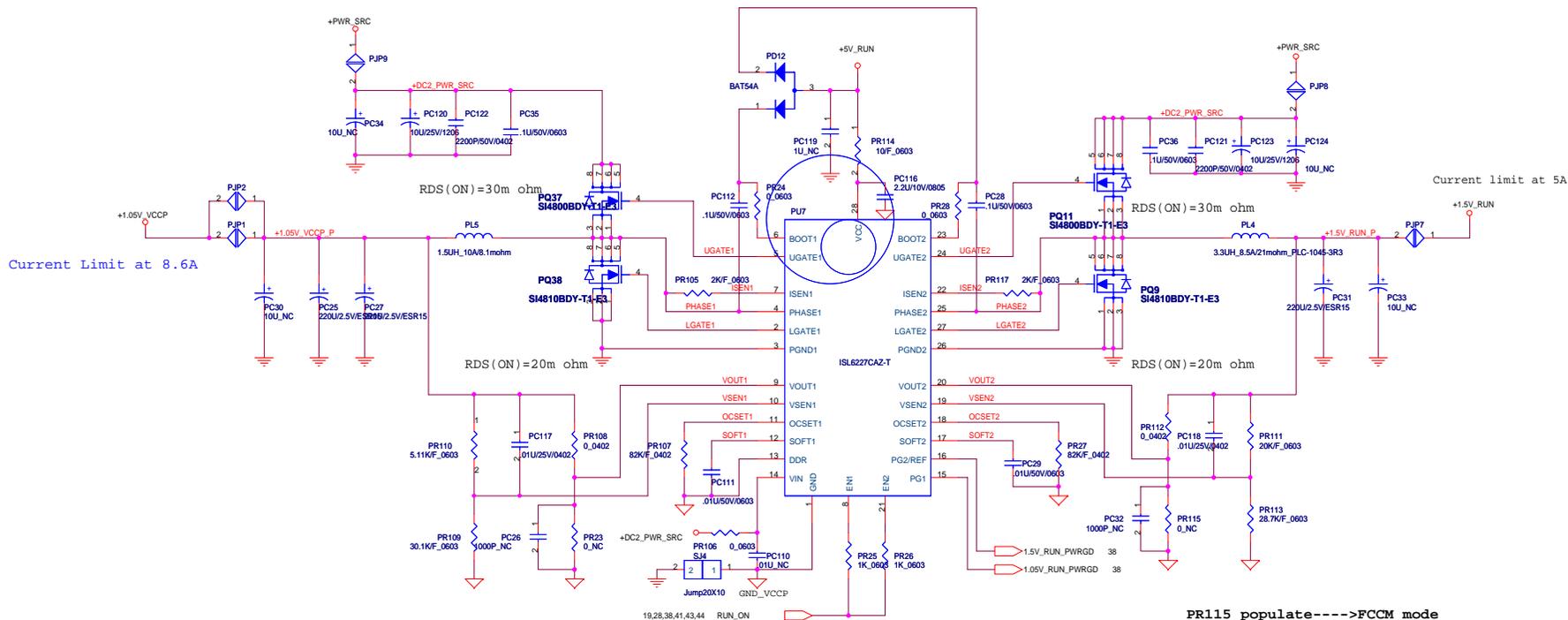
Place PC81, PC82 as close as possible to PQ27 drain and PQ26 source

place PC78, PC79 as close as possible to PQ25 drain and PQ24 source

Current Limit at 5.7A

Current Limit at 6.7A

 QUANTA COMPUTER		Title	
		3VALW,5VALW,5V,3V	
Size	Document Number	Rev	
FM1		2A	
Date:	3005/4/21	Sheet	41 of 51

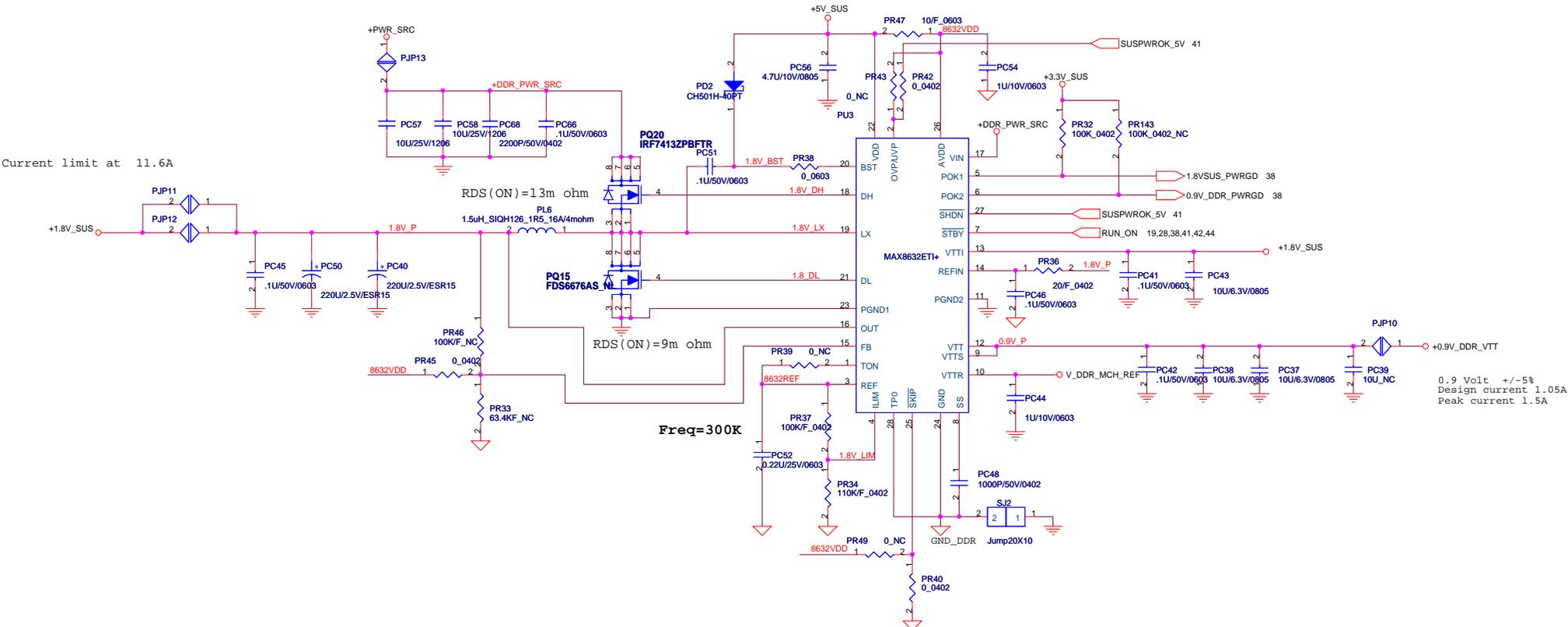


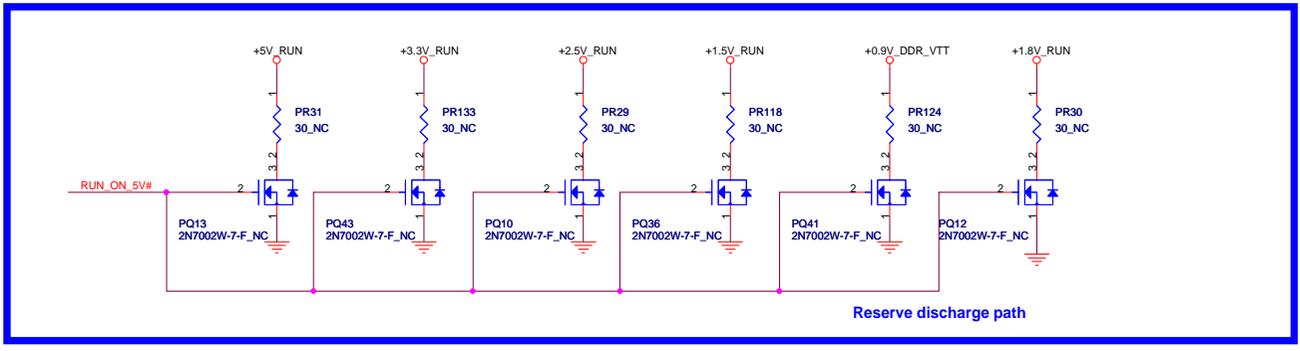
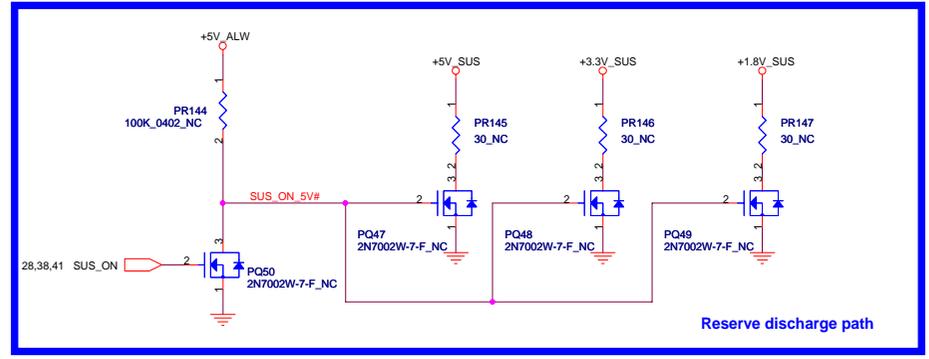
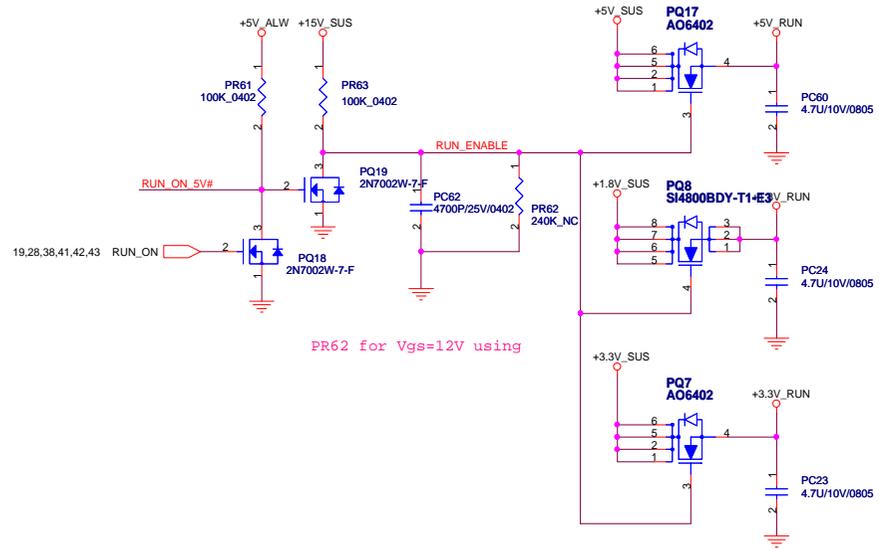
Current Limit at 8.6A

Current limit at 5A

PR23 populate---->FCCM mode
PR108 populate---->Hysteretic/FCCM mode.

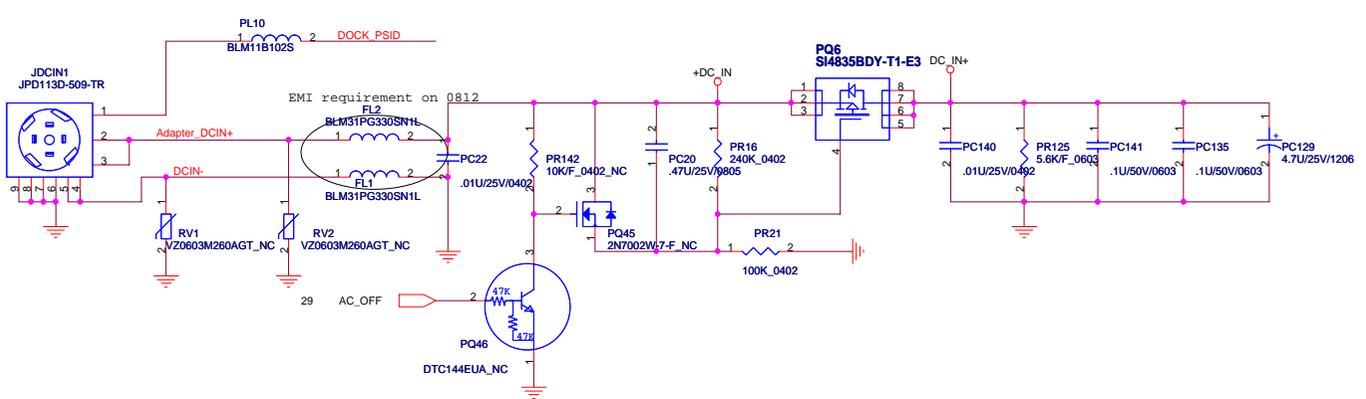
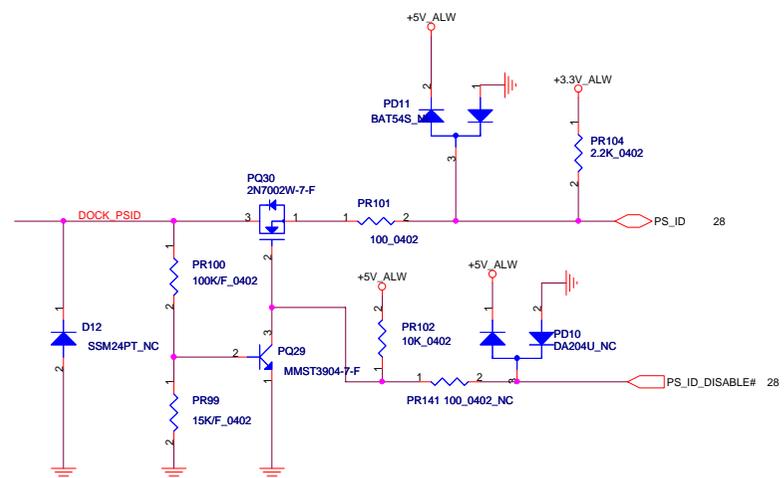
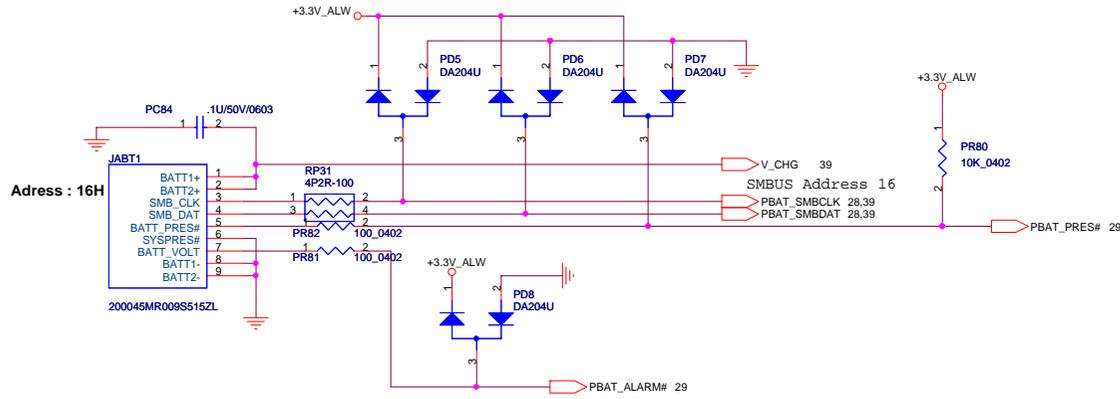
PR115 populate---->FCCM mode
PR112 populate---->Hysteretic/FCCM mode.





**QUANTA
COMPUTER**

Title	RUN POWER SW	
Size	Document Number FM1	Rev 2A
Date:	2005/4/21	Sheet 44 of 51



<p>Title: DCIN,BATT CONNECTOR</p>		
<p>Size: FM1</p>	<p>Document Number: Rev 2A</p>	<p>Date: 2005/4/21</p>
<p>Sheet 45 of 51</p>		<p>Rev 2A</p>