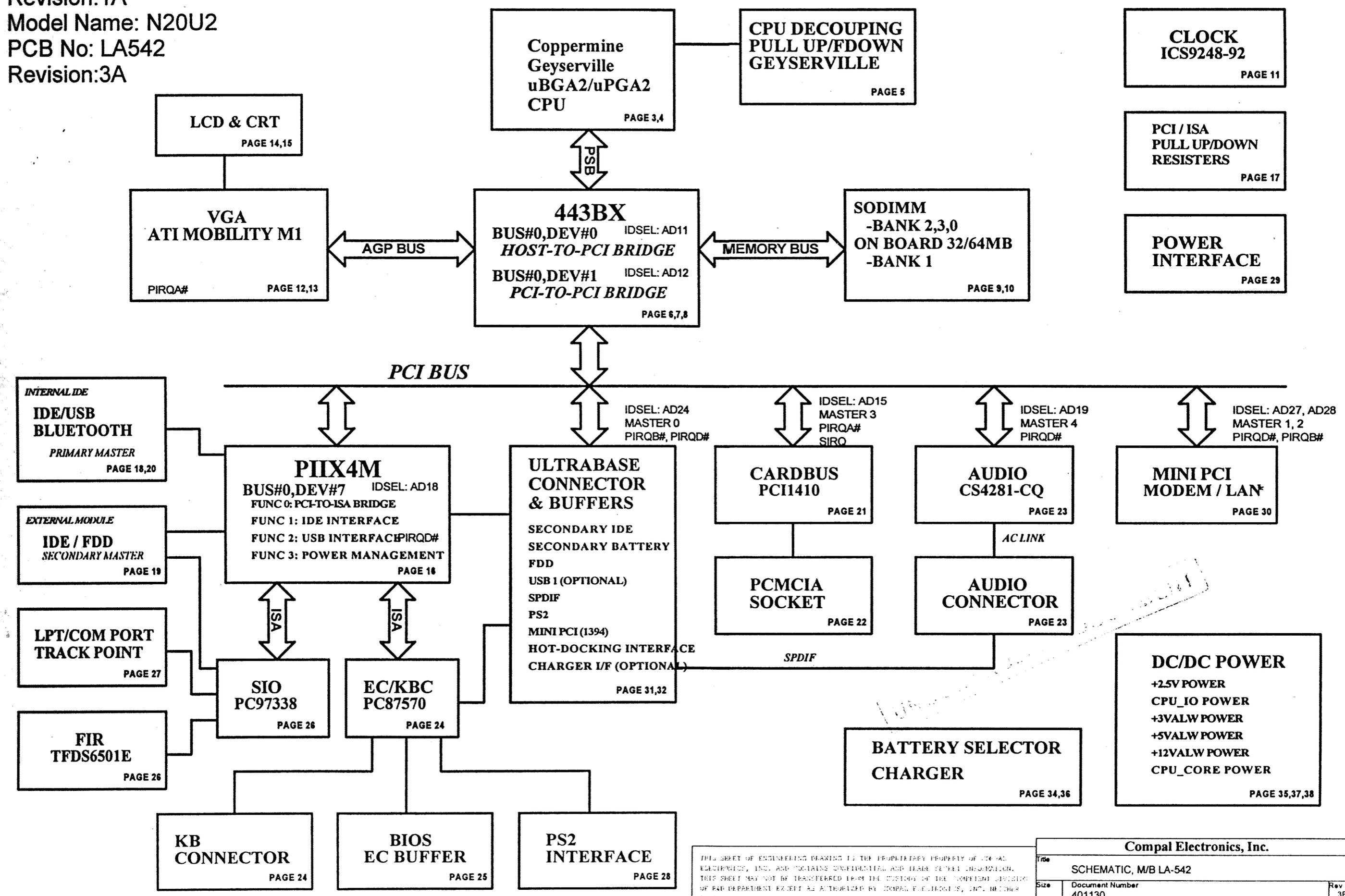


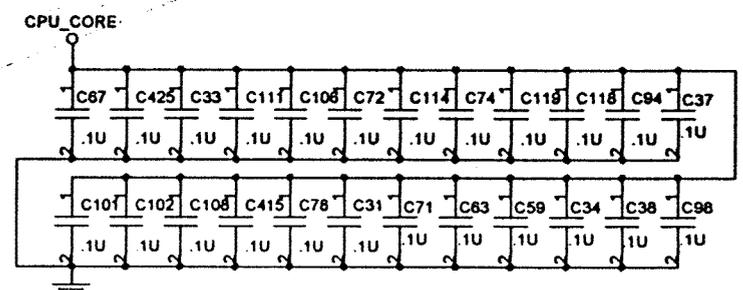
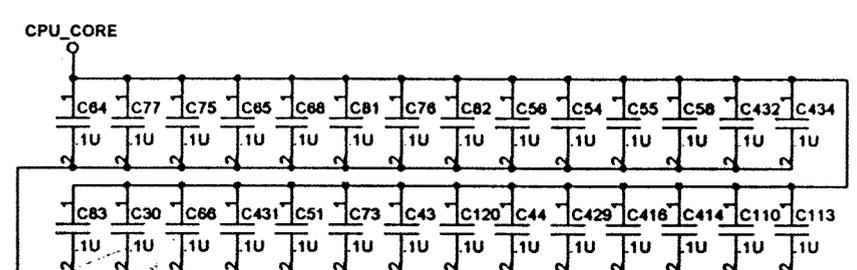
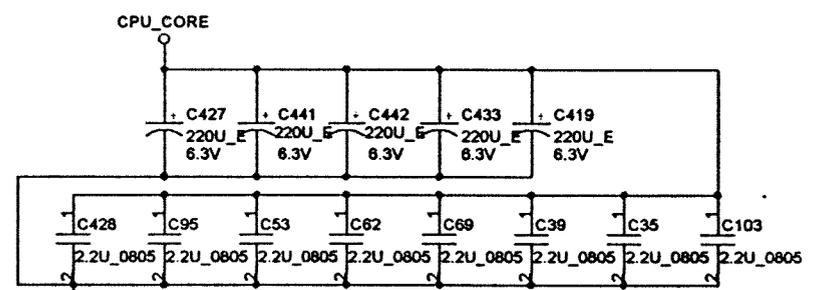
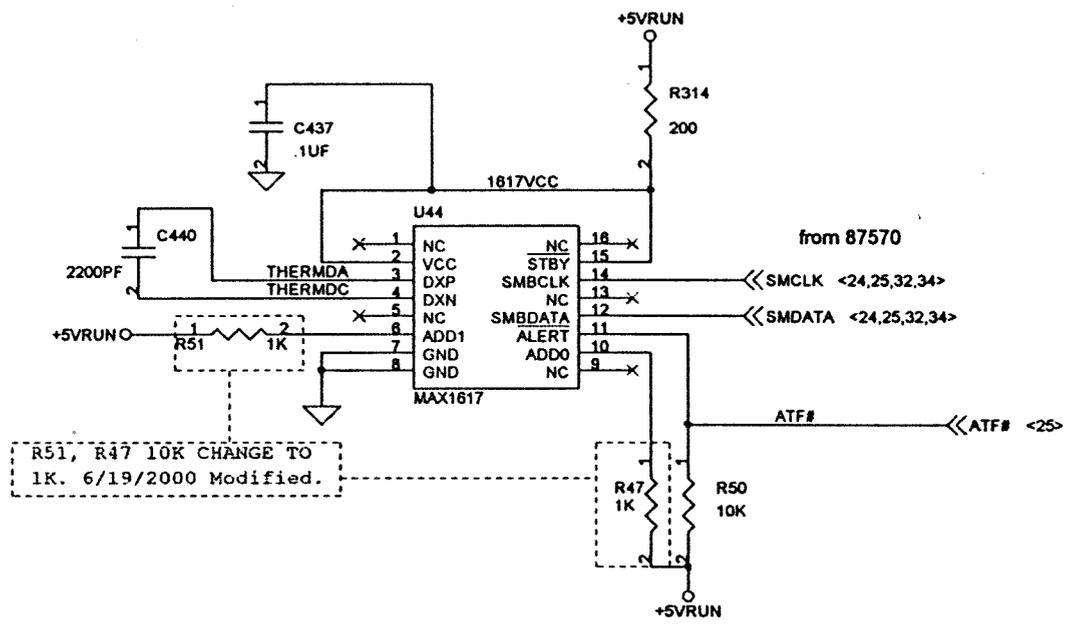
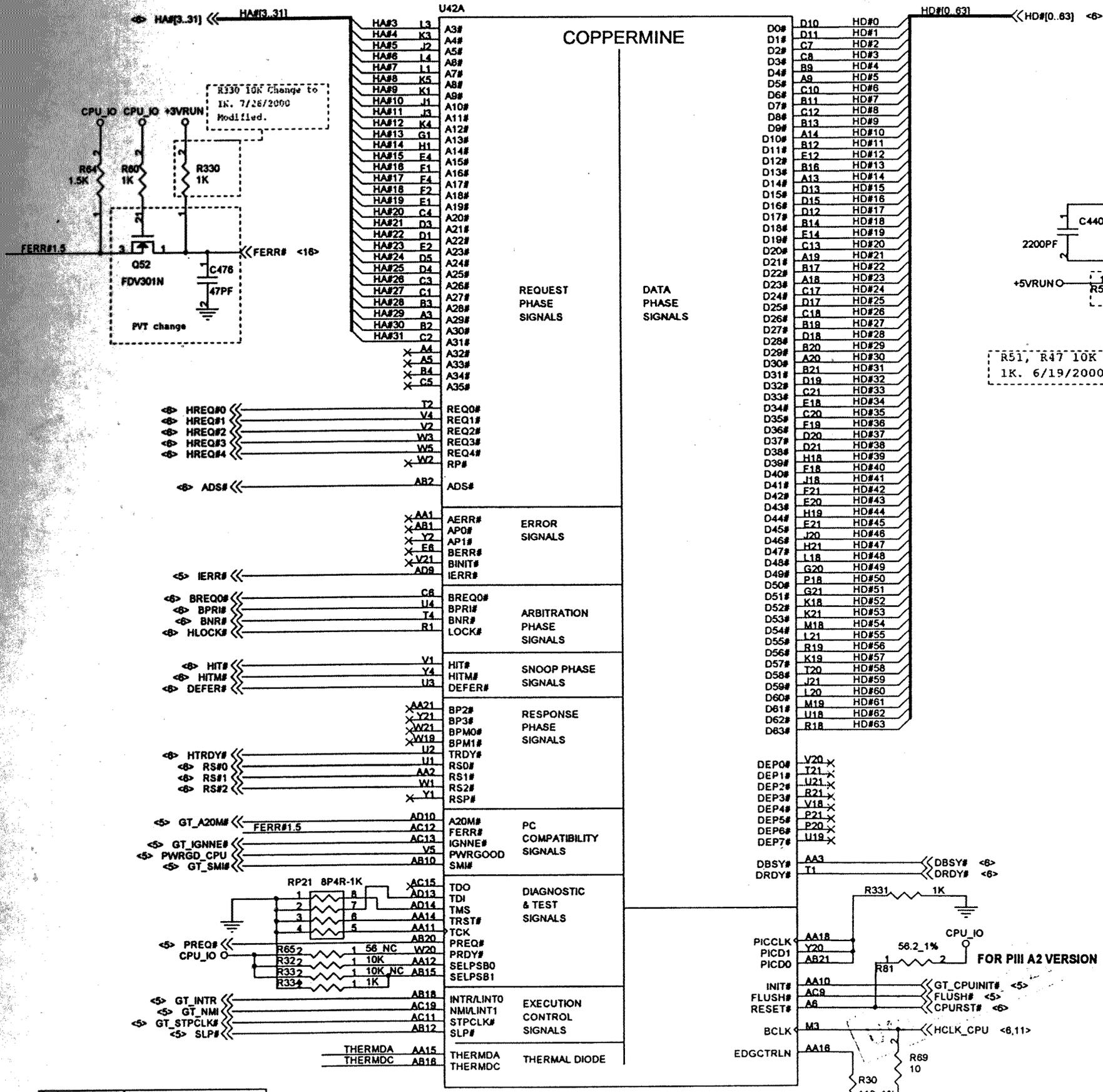
Model Name: N20U  
 PCB No: LA542  
 Revision: 1A  
 Model Name: N20U2  
 PCB No: LA542  
 Revision: 3A

# N20U BLOCK DIAGRAM



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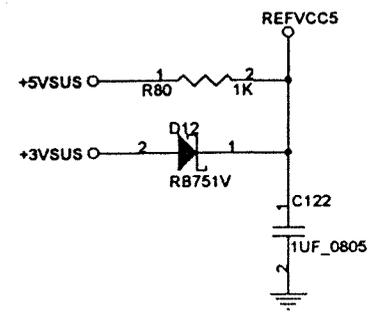
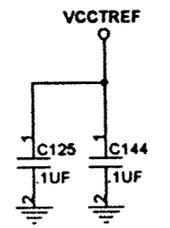
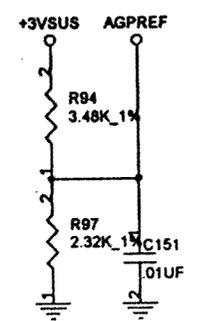
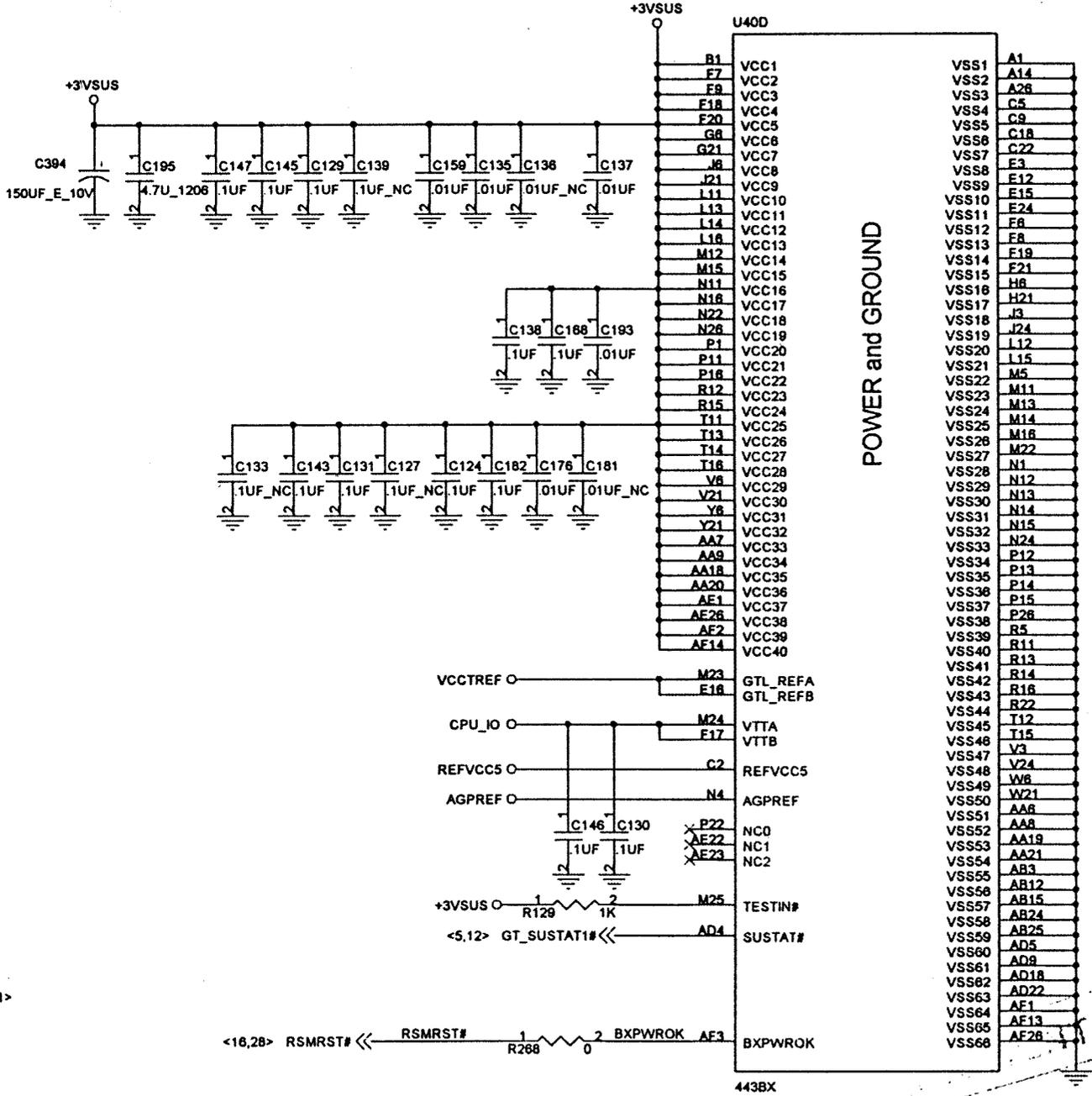
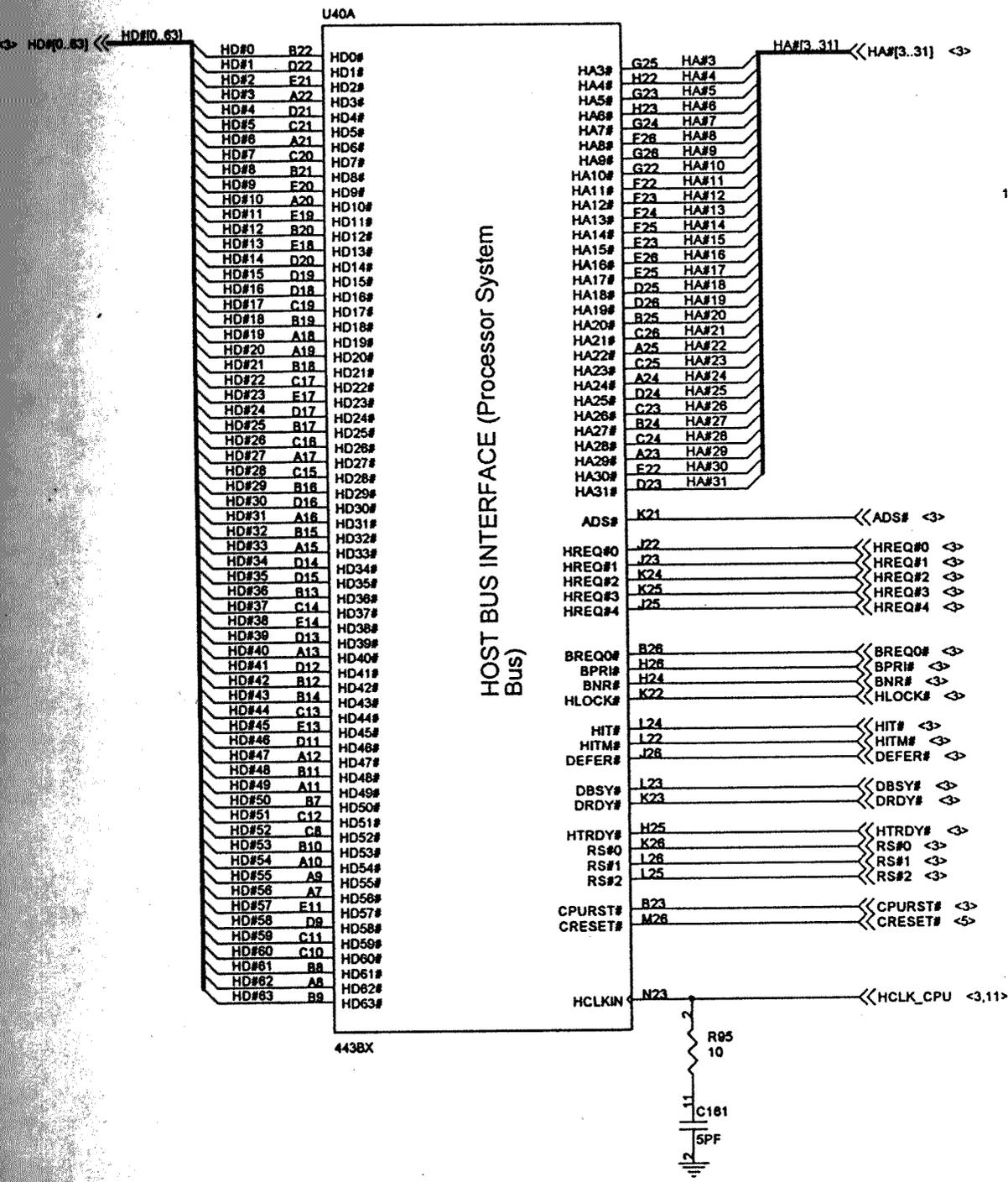


SELPSB(1:0)	STSEM BUS FREQUENCY
00	66MHZ
01	100MHZ
10	RESERVED
11	133MHZ

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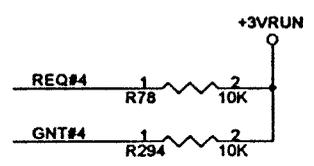
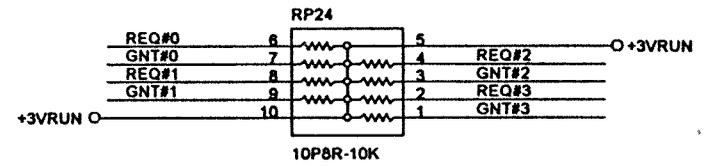
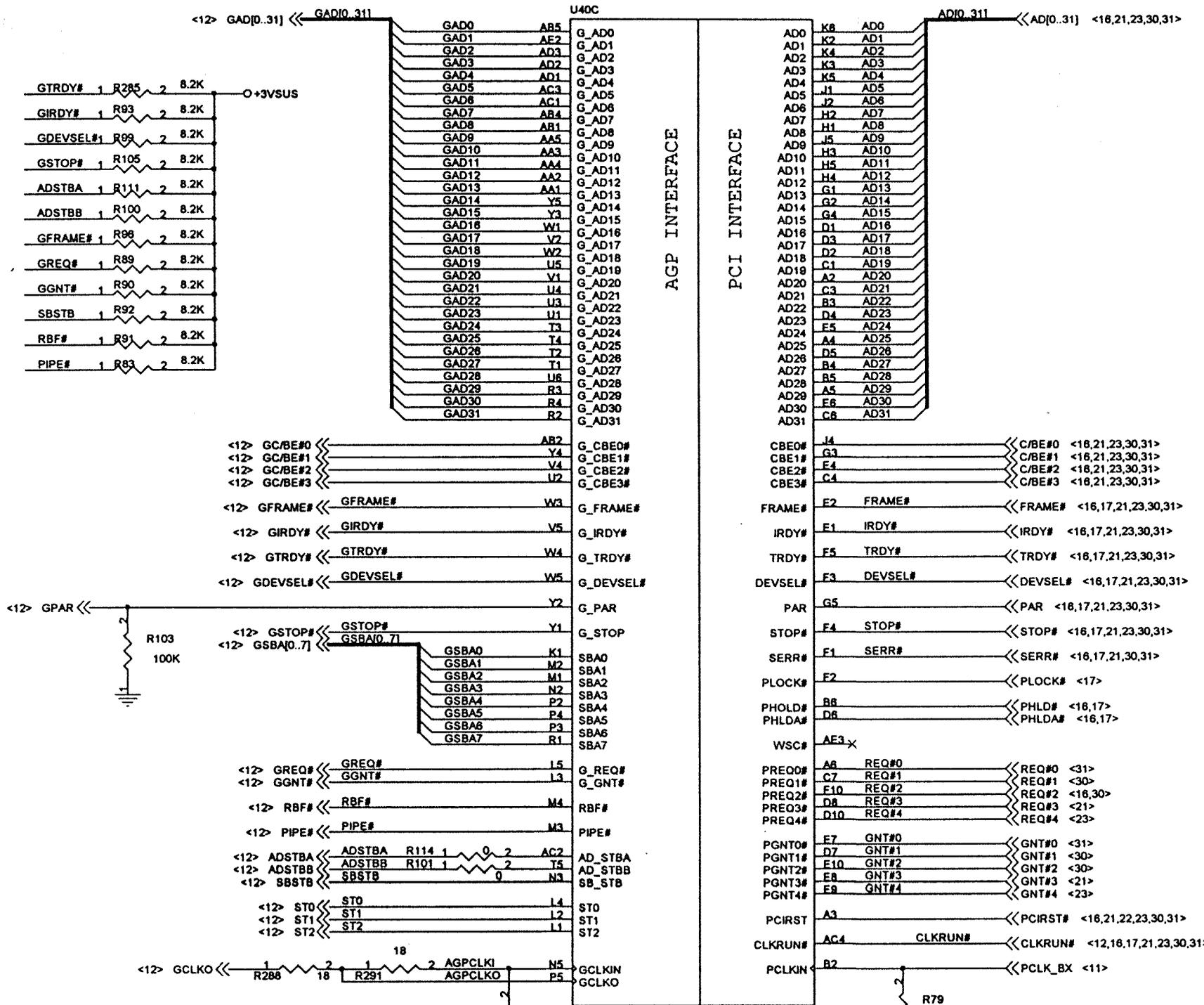




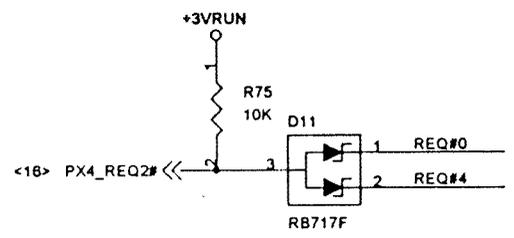
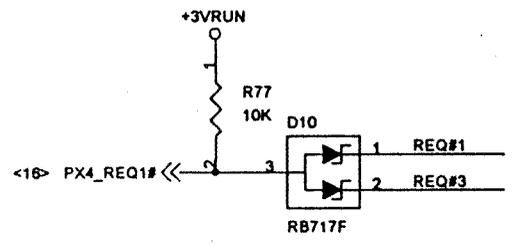


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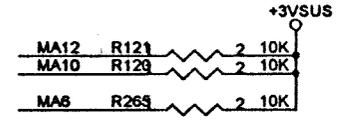
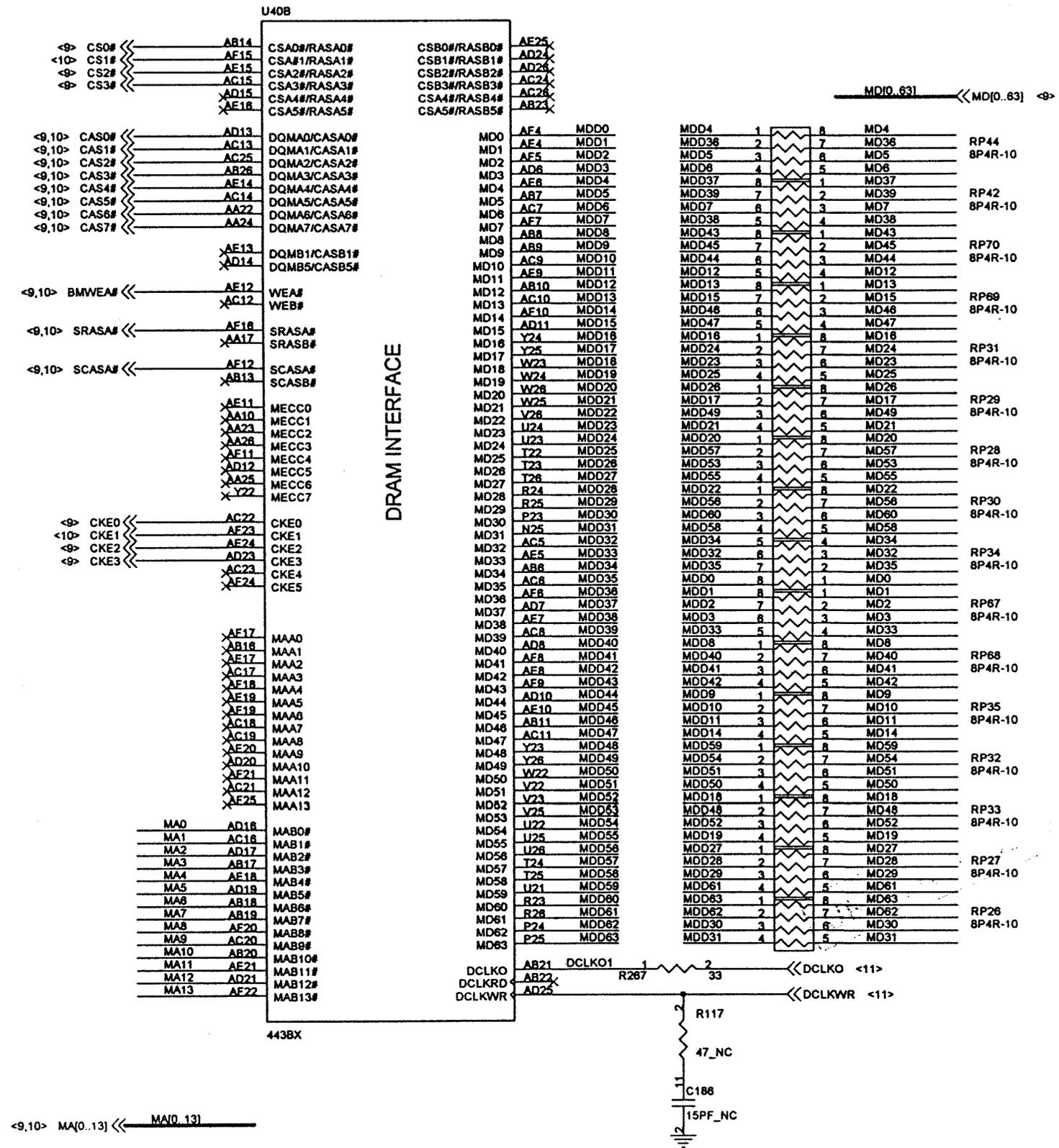
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PCI REQ ASSIGNMENT	
REQ#0	ULTRABASE
REQ#1	MINI PCI (MODEM)
REQ#2	MINI PCI (LAN)
REQ#3	PCMCIA CONTROLLER
REQ#4	PCI AUDIO



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Pin Name	Function	Low	High	Internal Resistor	Status Register
MAB12#	Host Frequency Select	68MHz	100MHz	Pull-down	NBXCFG[13]
MAB10#	Quick Start Select	Stop Clock Mode	Quick Start Mode	Pull-down	PMCR[3]
MAB6#	Host Bus Buffer Mode Select	Desktop GTL+	Mobile Low Power GTL+	Pull-down	none



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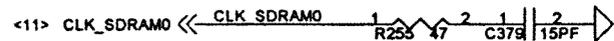
# SODIMM X 1

(H: 5.6mm)

Support 3 SDRAM CLOCK

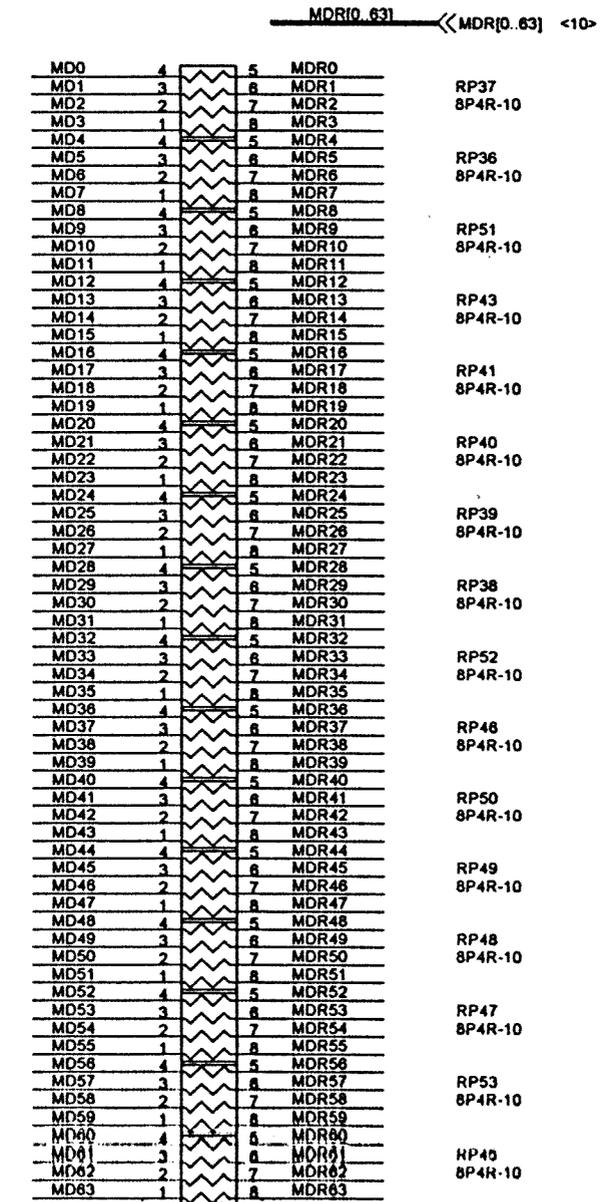
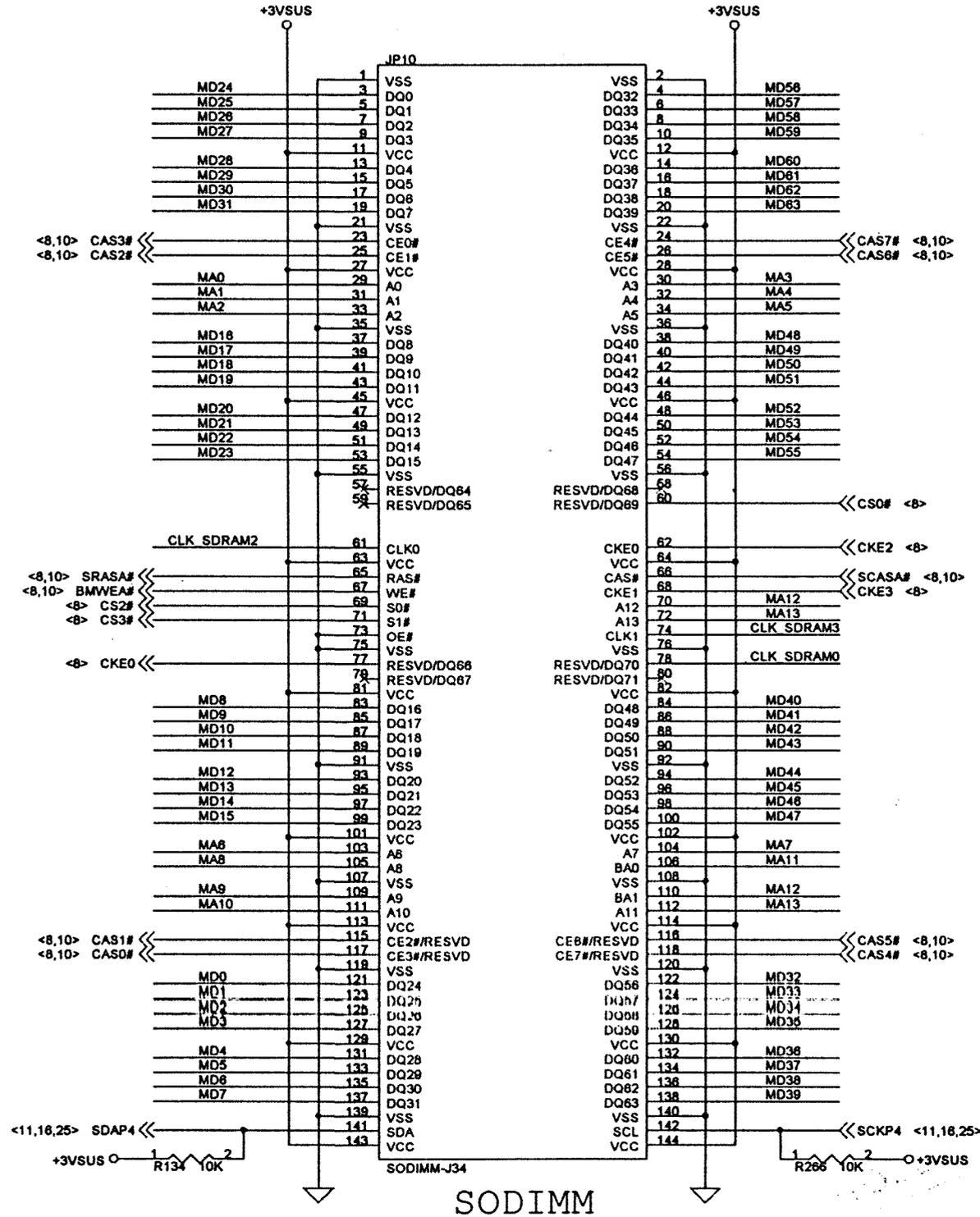
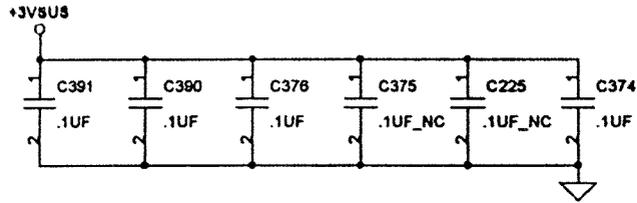
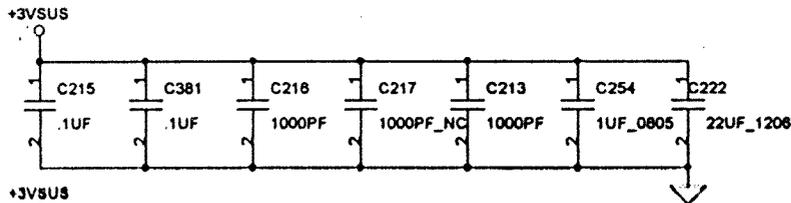
PIN 60, 77, 78 Difference

# BANK 2,3,0



<8,10> MA[0..13] << MA[0..13]

<8> MD[0..63] << MD[0..63]



SODIMM

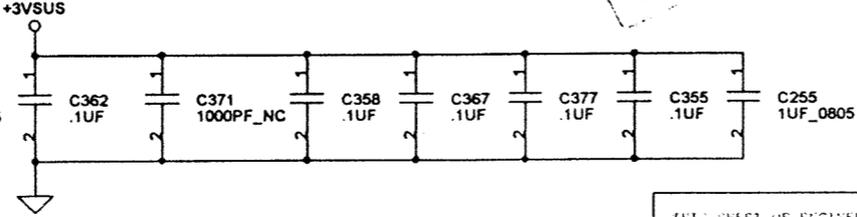
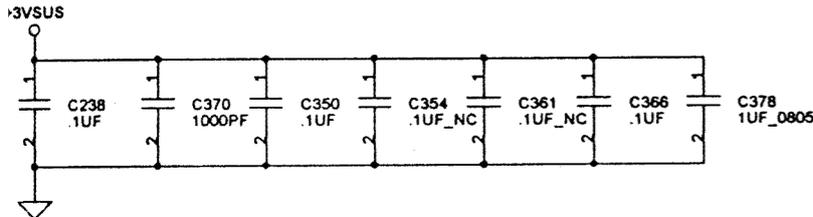
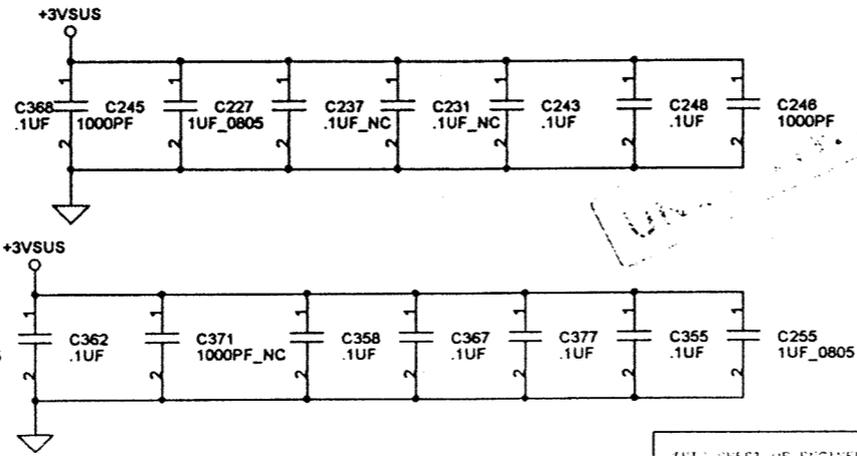
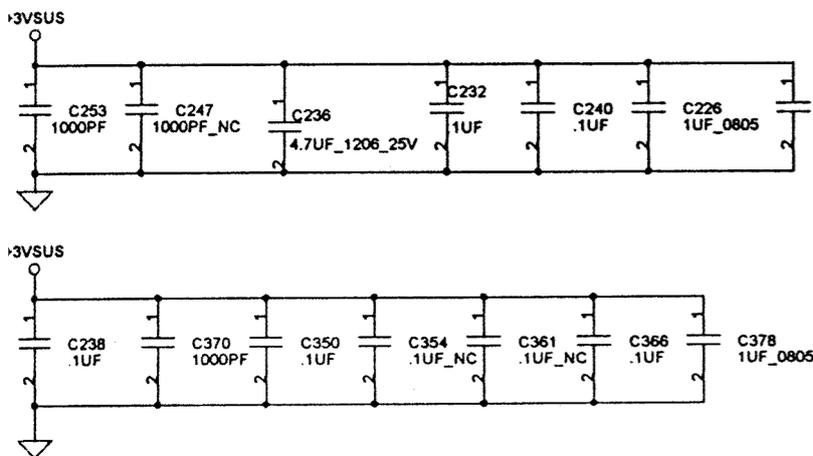
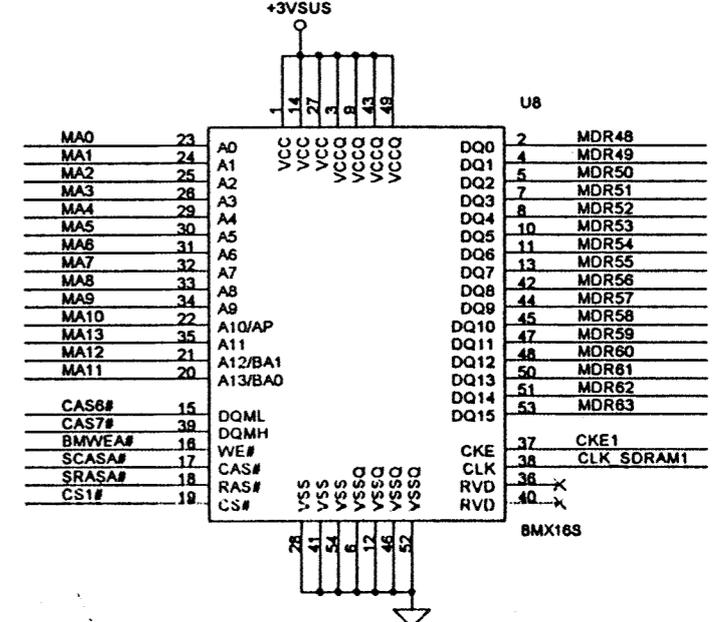
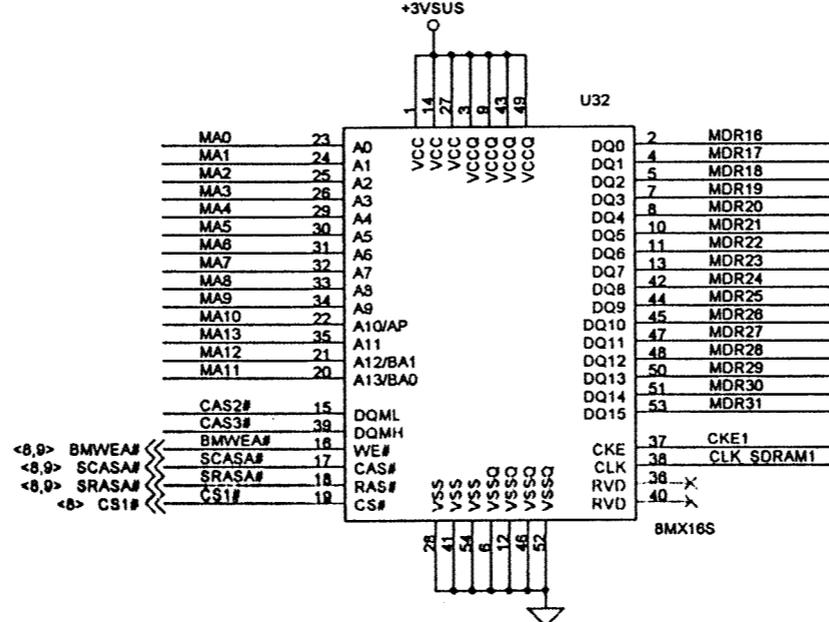
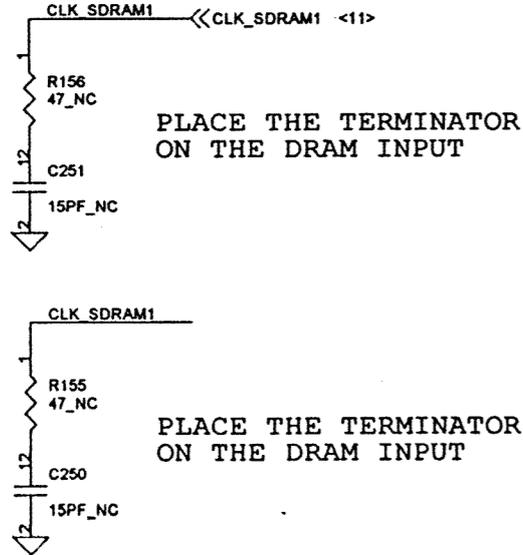
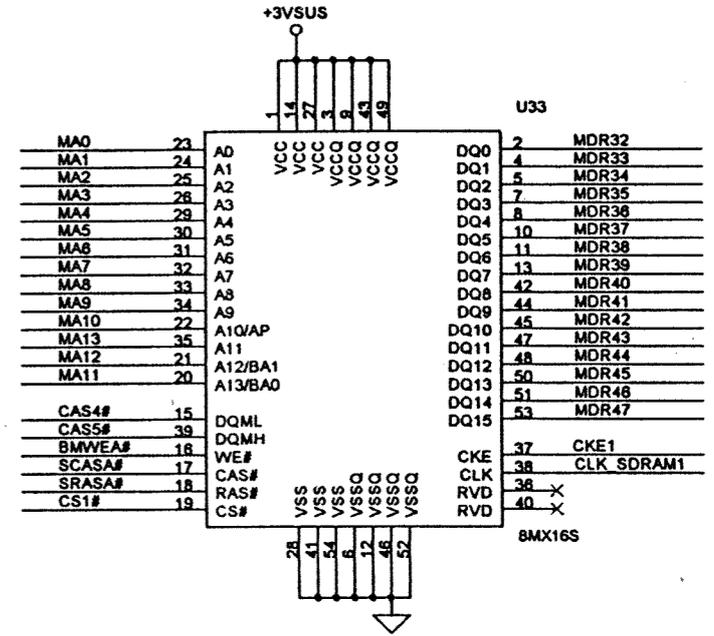
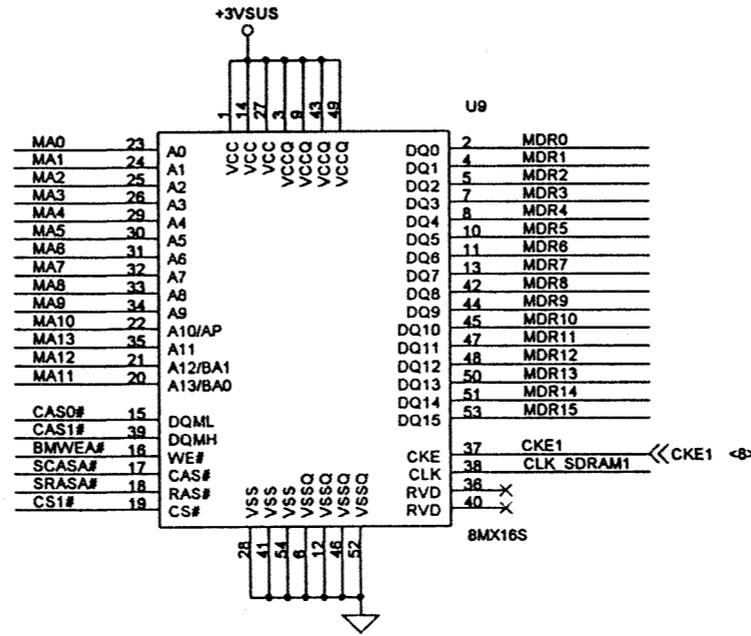
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# 32MB/64MB SDRAM

# BANK 1

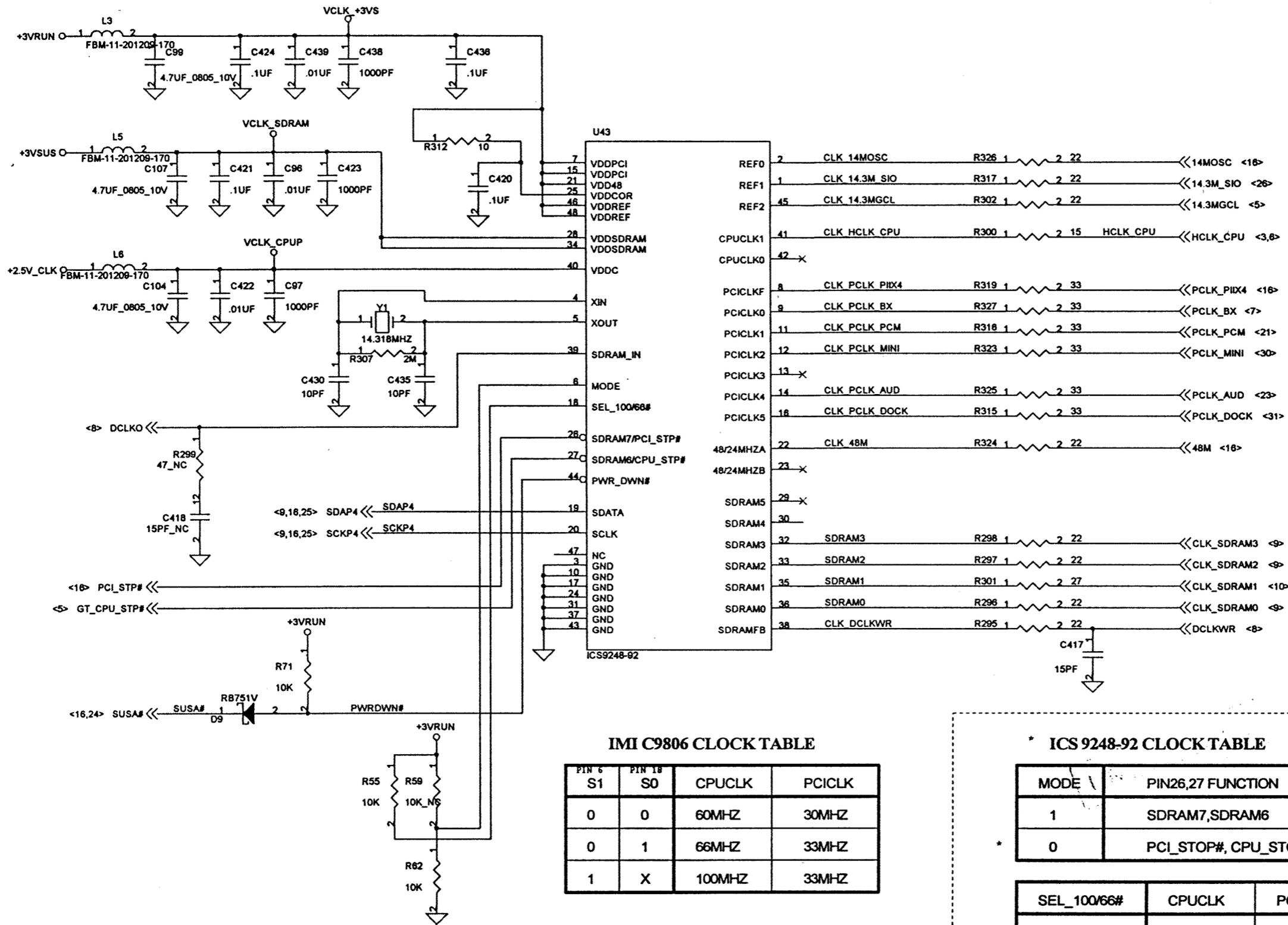
64Mbit 4Mx16 : Row: MA0-MA11  
 Column: MA0-MA7  
 Bank address: 2  
 128Mbit 8Mx16 : Row: MA0-MA11  
 Column: MA0-MA8  
 Bank address: 2



<8,9> MA[0..13] << MA[0..13]  
 <9> MDR[0..63] << MDR[0..63]  
 <8,9> CAS0# << CAS0#  
 <8,9> CAS1# << CAS1#  
 <8,9> CAS2# << CAS2#  
 <8,9> CAS3# << CAS3#  
 <8,9> CAS4# << CAS4#  
 <8,9> CAS5# << CAS5#  
 <8,9> CAS6# << CAS6#  
 <8,9> CAS7# << CAS7#

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# CLOCK GENERATOR & BUFFER



IMI C9806 CLOCK TABLE

PIN 6 S1	PIN 18 S0	CPUCCLK	PCICLK
0	0	60MHZ	30MHZ
0	1	66MHZ	33MHZ
1	X	100MHZ	33MHZ

ICS 9248-92 CLOCK TABLE

MODE	PIN26,27 FUNCTION
1	SDRAM7,SDRAM6
0	PCI_STOP#, CPU_STOP#

SEL_100/66#	CPUCCLK	PCICLK
0	66.6MHZ	33.3MHZ
1	100MHZ	33.3MHZ

N31B2

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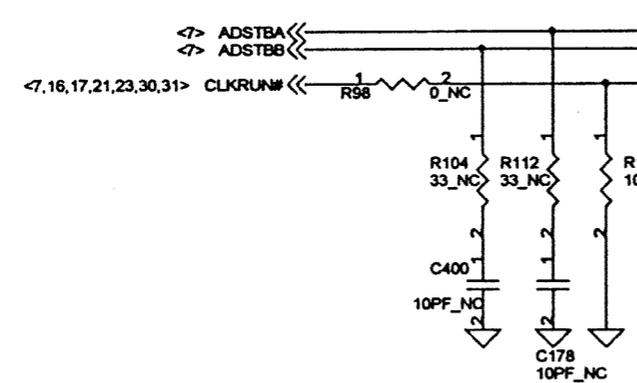
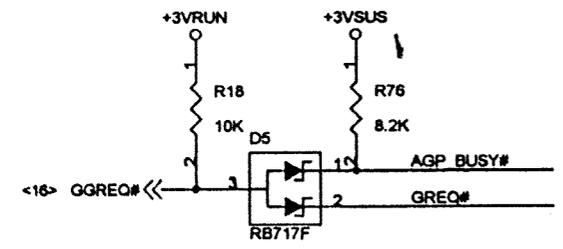
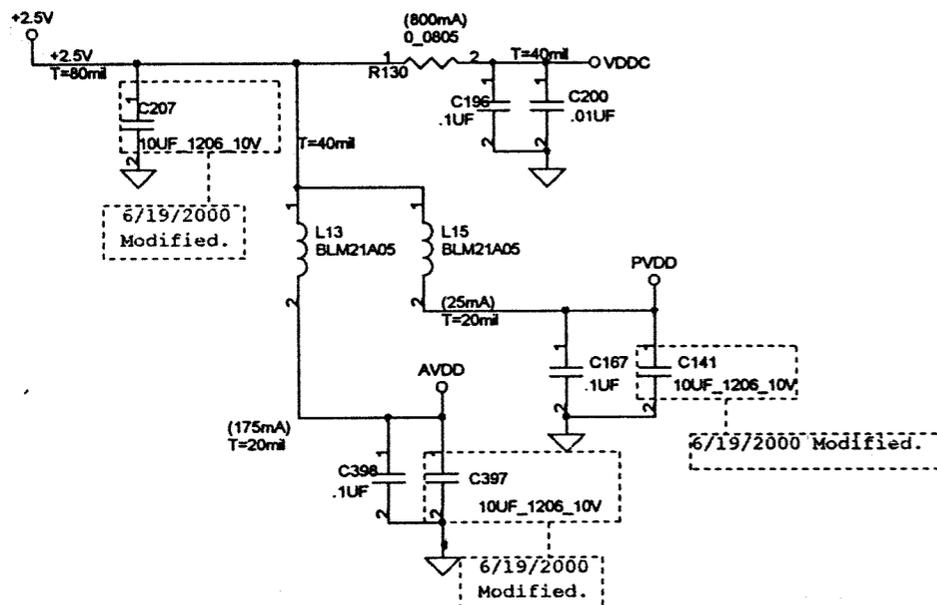
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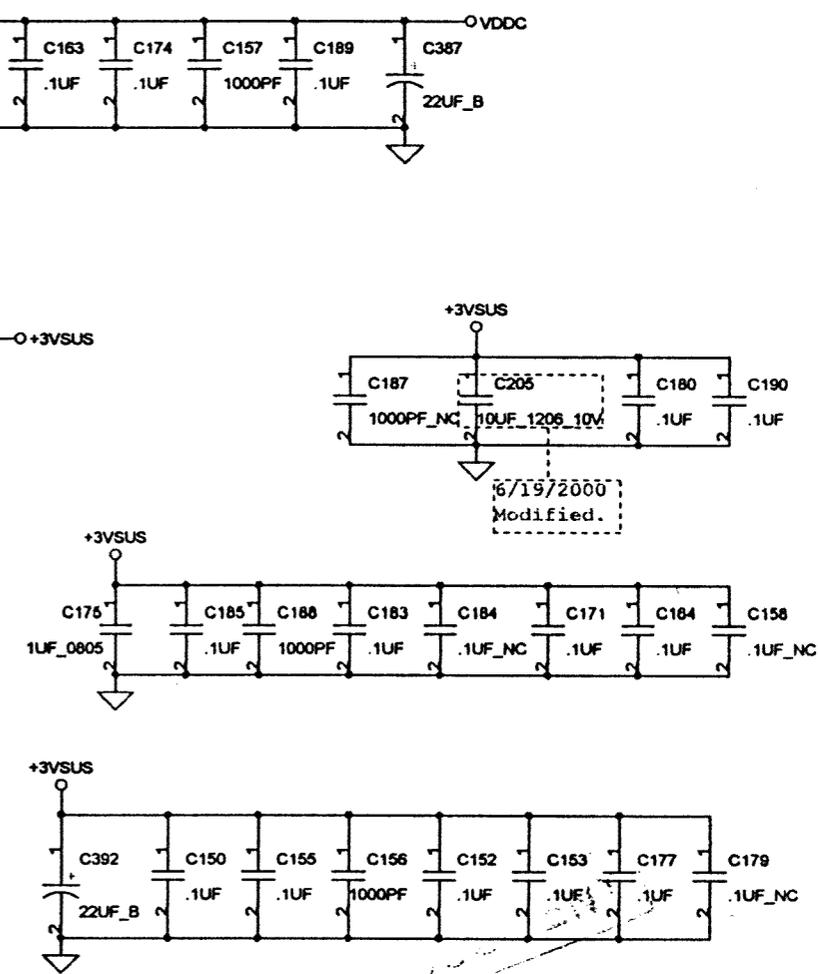
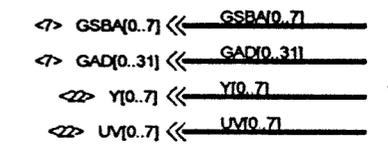
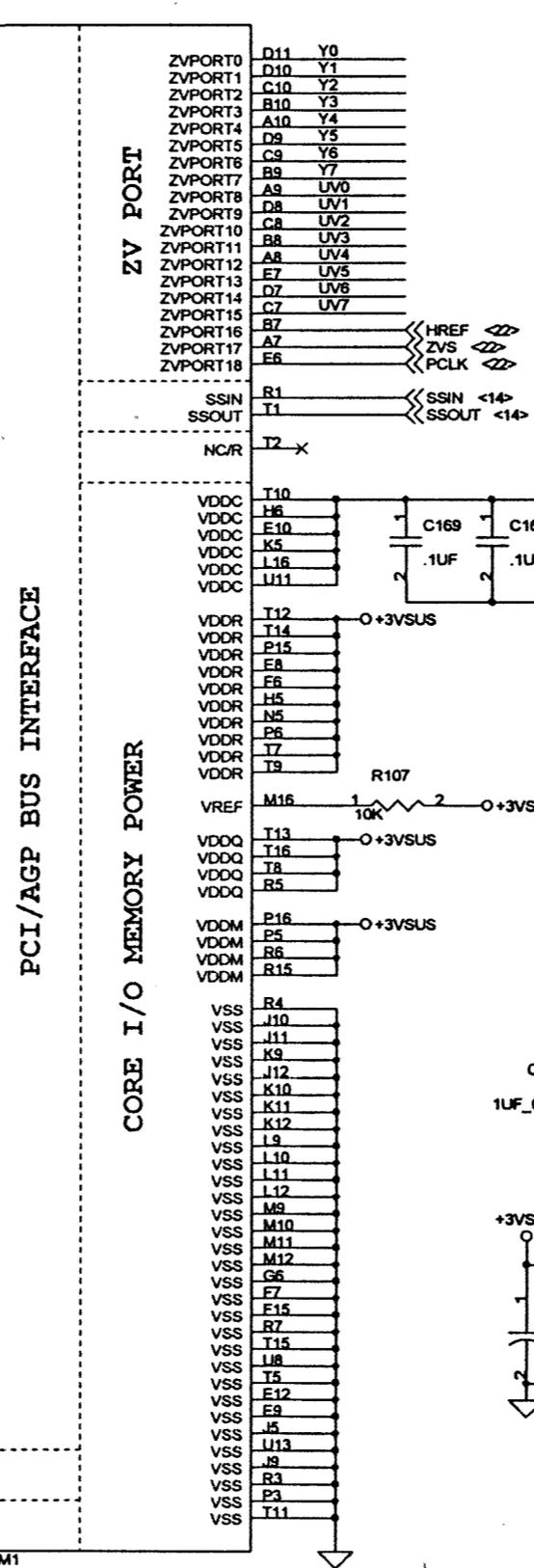
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U39A	
GAD0	B11
GAD1	A11
GAD2	C11
GAD3	D12
GAD4	AD3
GAD5	A12
GAD6	B12
GAD7	D13
GAD8	A13
GAD9	E14
GAD10	C14
GAD11	D14
GAD12	A14
GAD13	A18
GAD14	D15
GAD15	B14
GAD16	D18
GAD17	C19
GAD18	E17
GAD19	E18
GAD20	D20
GAD21	B20
GAD22	F18
GAD23	E19
GAD24	G18
GAD25	F19
GAD26	F20
GAD27	D17
GAD28	J20
GAD29	G16
GAD30	G20
GAD31	E16



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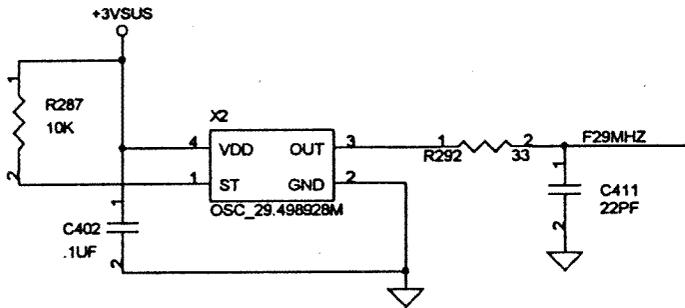
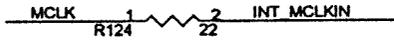
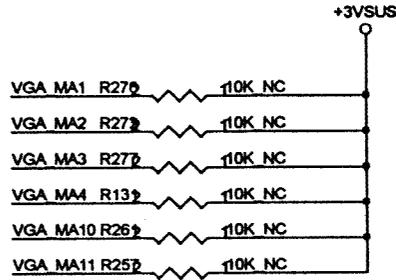
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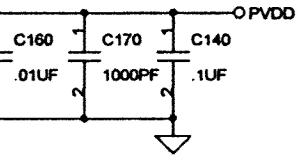
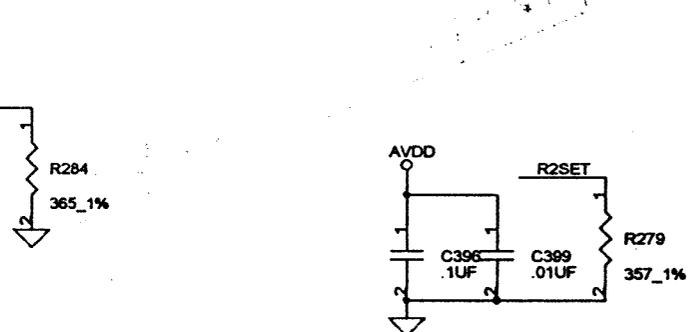
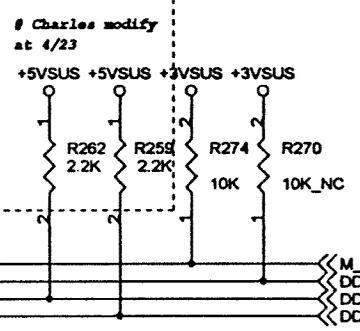
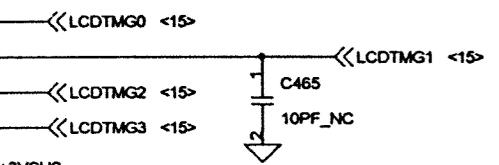
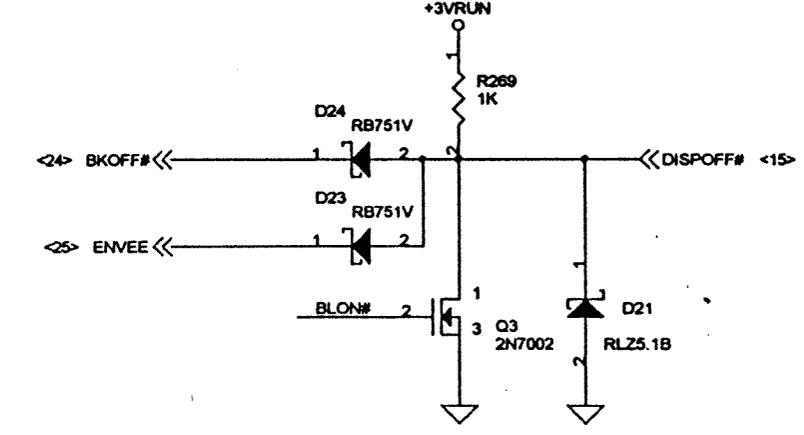
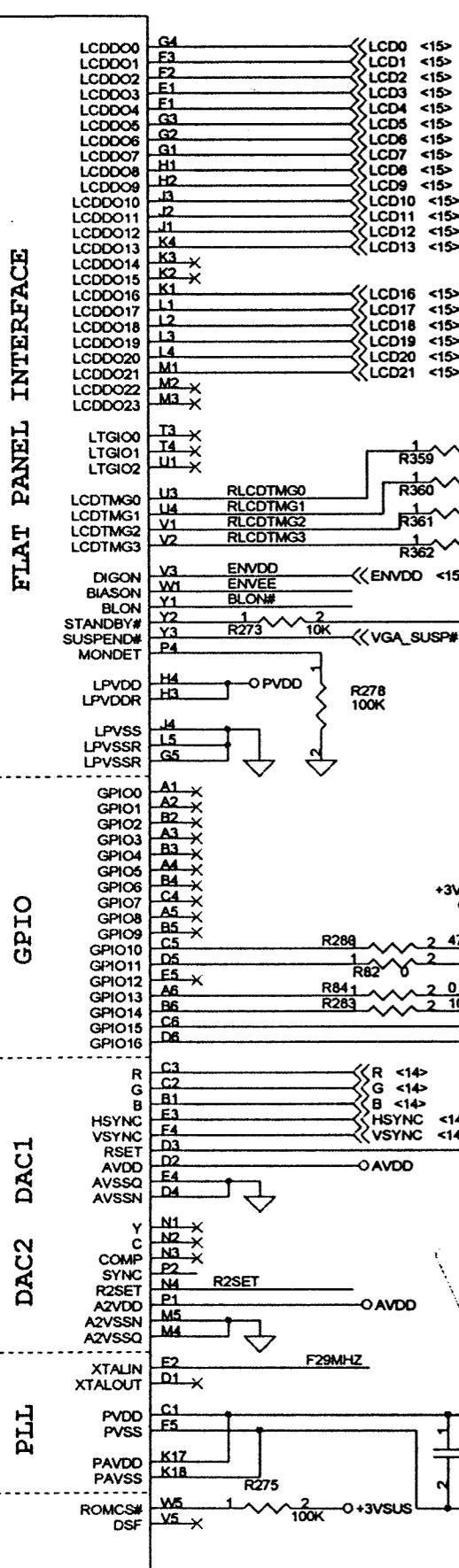
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MA2	MA1	AGP CLOCK SKEW ADJUSTMENT
DNI	DNI	INTERNAL VS EXTERNAL CLOCKS (DEFAULT)
MA4	MA3	AGP CLOCK SKEW ADJUSTMENT
DNI	DNI	BETWEEN X1 AND X2 CLOCKS (DEFAULT)
MA11	MA10	AGP PLL VCO GAIN
DNI	DNI	VCO GAIN ADJUSTMENT (DEFAULT)

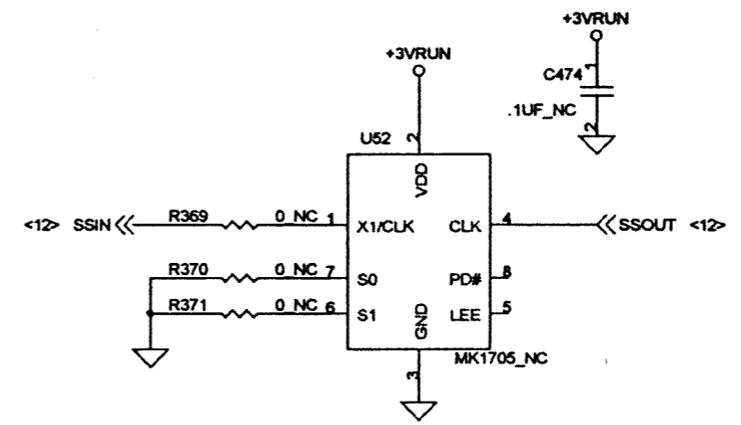
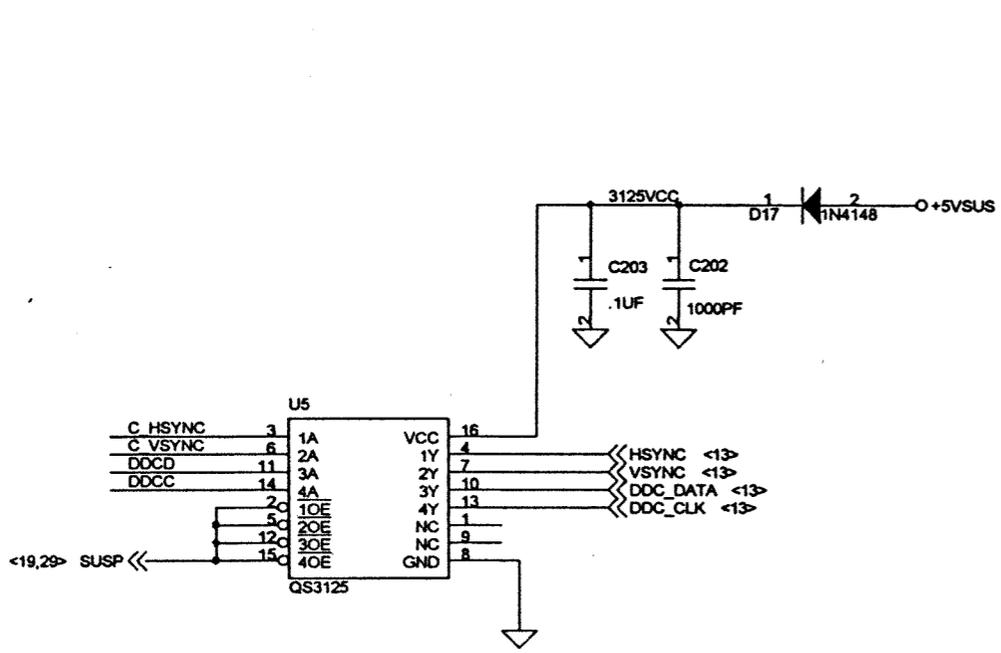


Y11	MD0	U398
U12	MD1	
V12	MD2	
W12	MD3	
Y12	MD4	
V13	MD5	
W13	MD6	
Y13	MD7	
U14	MD8	
V14	MD9	
W14	MD10	
Y14	MD11	
U15	MD12	
V15	MD13	
W15	MD14	
Y15	MD15	
U16	MD16	
V16	MD17	
W16	MD18	
Y16	MD19	
V17	MD20	
W17	MD21	
Y17	MD22	
W18	MD23	
Y18	MD24	
W19	MD25	
Y19	MD26	
W20	MD27	
V19	MD28	
V18	MD29	
V20	MD30	
L20	MD31	
U19	MD32	
U18	MD33	
U17	MD34	
U16	MD35	
T20	MD36	
T19	MD37	
T18	MD38	
T17	MD39	
R16	MD40	
R20	MD41	
R19	MD42	
R18	MD43	
R17	MD44	
P20	MD45	
P19	MD46	
P18	MD47	
P17	MD48	
N16	MD49	
N20	MD50	
N19	MD51	
N18	MD52	
N17	MD53	
M20	MD54	
M19	MD55	
M18	MD56	
M17	MD57	
L20	MD58	
L19	MD59	
L18	MD60	
L17	MD61	
K20	MD62	
K19	MD63	
T8	MA0	
Y7	MA1	
W7	MA2	
V7	MA3	
L7	MA4	
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V11	DQM#6	
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X Y4	CS1	

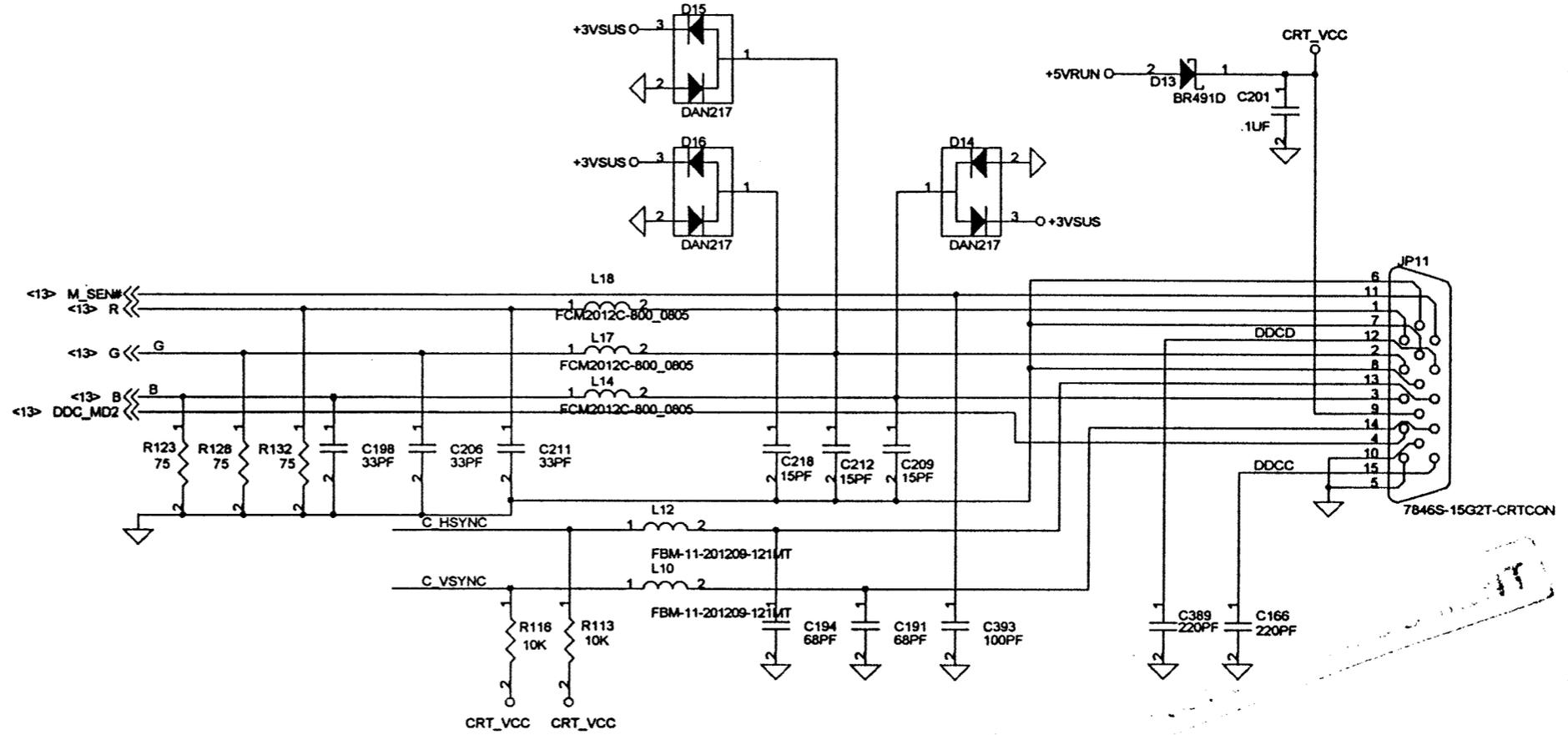


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Clock Modulator for EMI Reduction



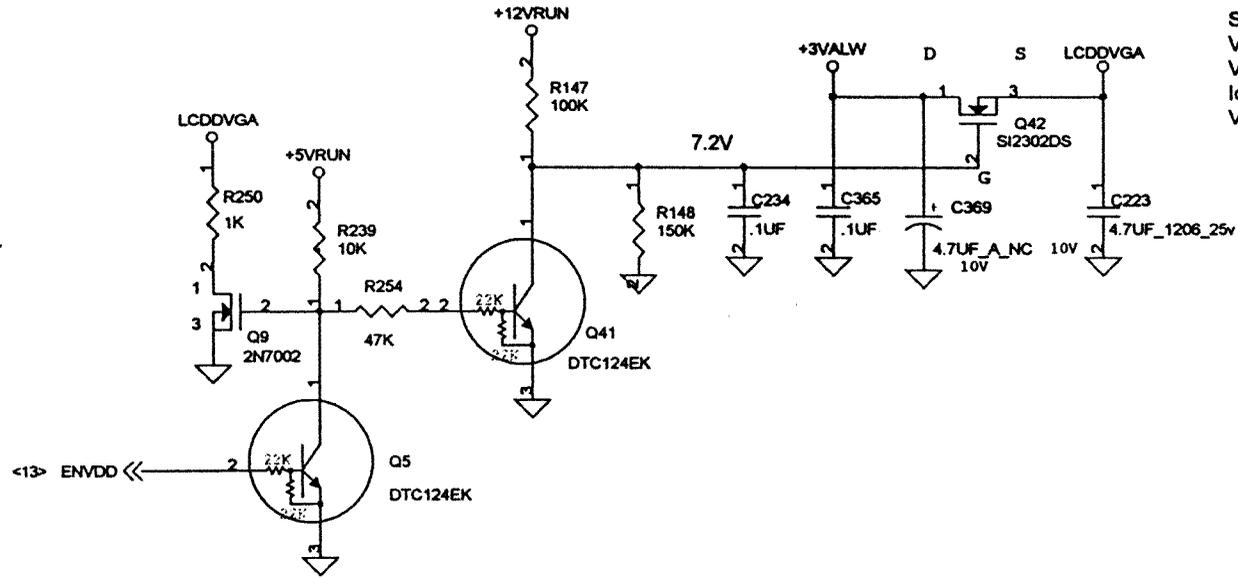
CRT CONNECTOR

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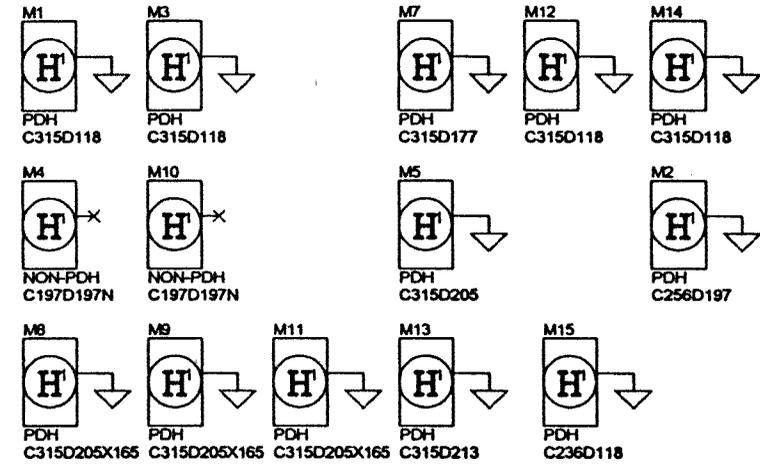
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Size: B	Document Number: 401130	Rev: 3E
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SI2301DS: P CHANNEL  
 VGS: -4.5V, RDS: 130mOHM  
 VGS: -2.5V, RDS: 190mOHM  
 Id(MAX): 2.3A  
 VGS(MAX): +8V

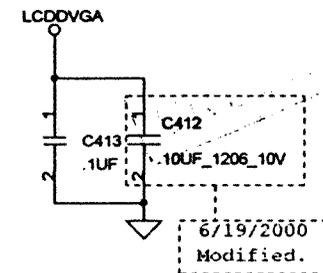
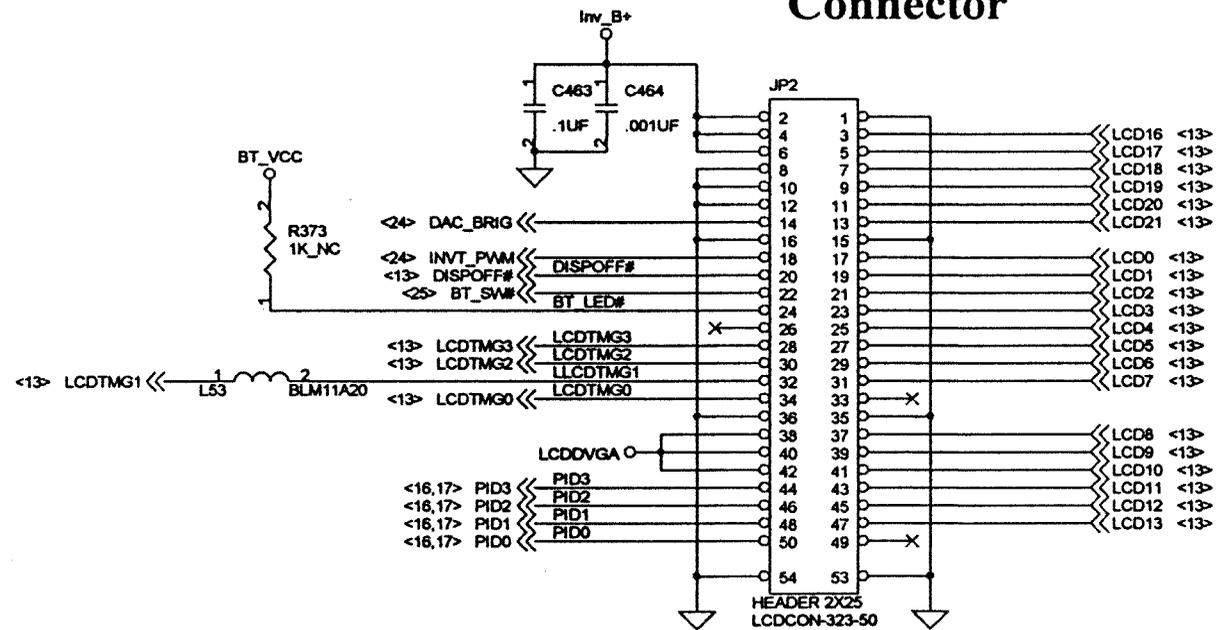
SI2302DS: N CHANNEL  
 VGS: 4.5V, RDS: 85mOHM  
 VGS: 2.5V, RDS: 115mOHM  
 Id(MAX): 2.8A  
 VGS(MAX): +8V



FOR LAYOUT SCROLLING, DELETE FROM BOM



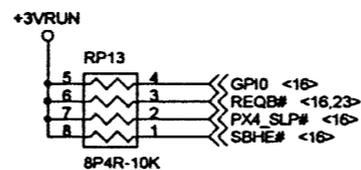
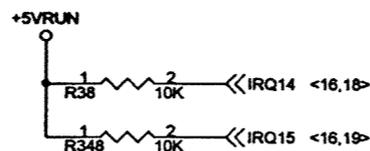
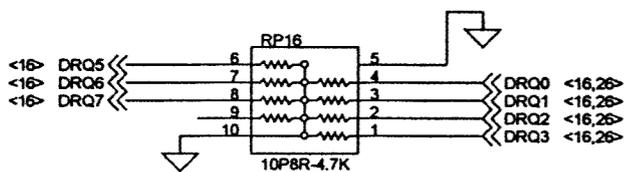
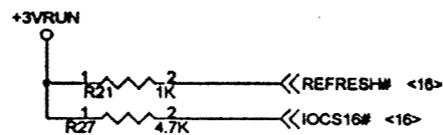
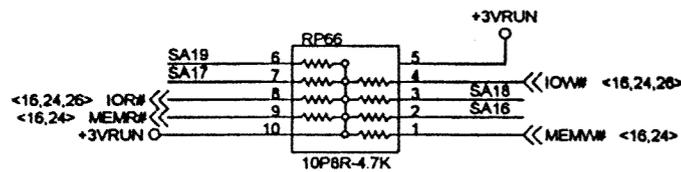
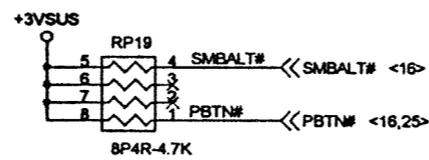
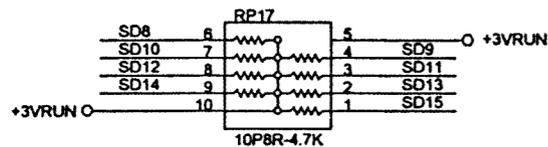
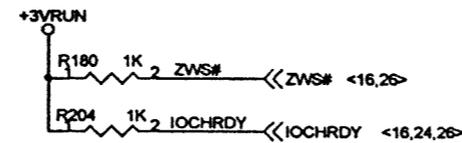
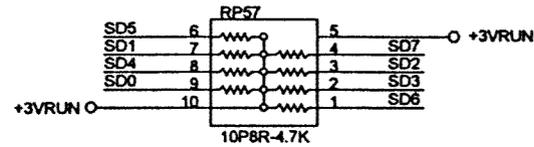
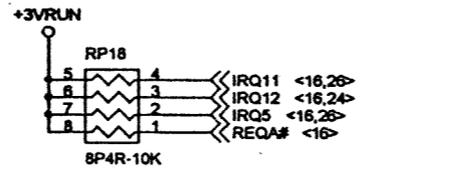
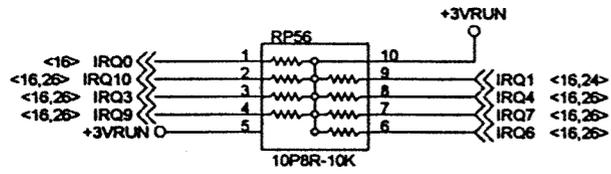
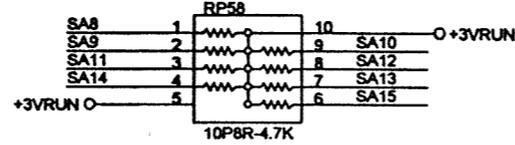
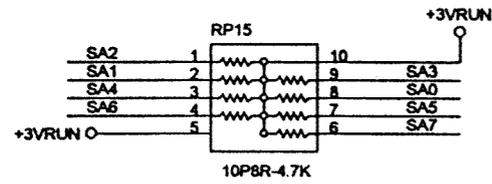
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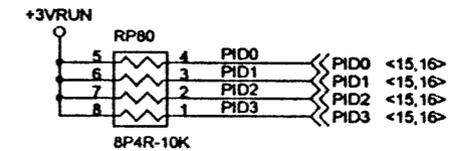
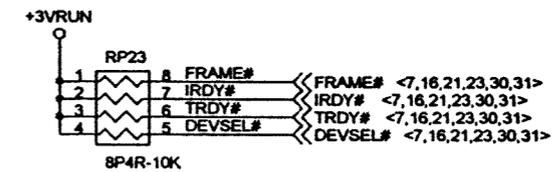
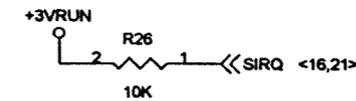
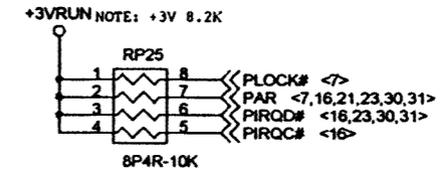
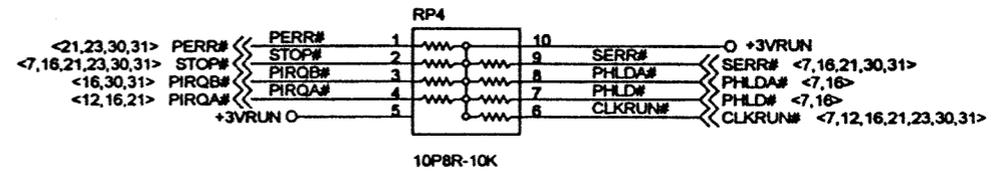
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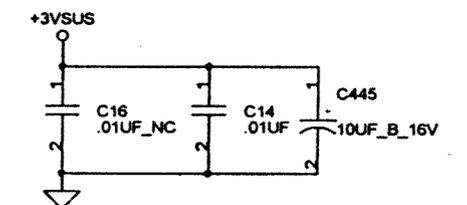
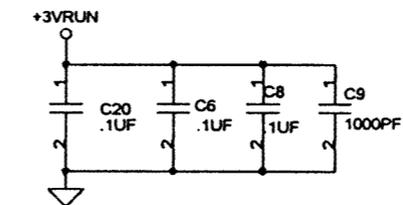
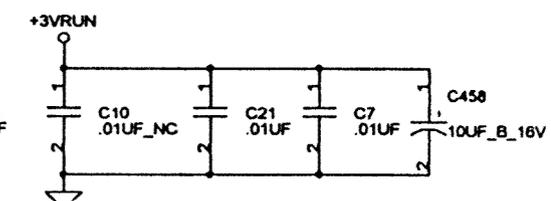
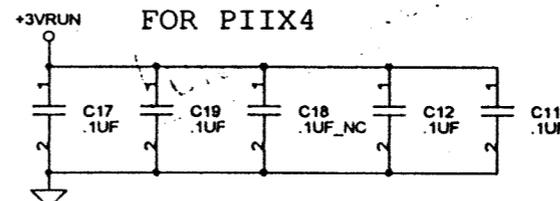
# ISA



# PCI



## FOR PIIX4

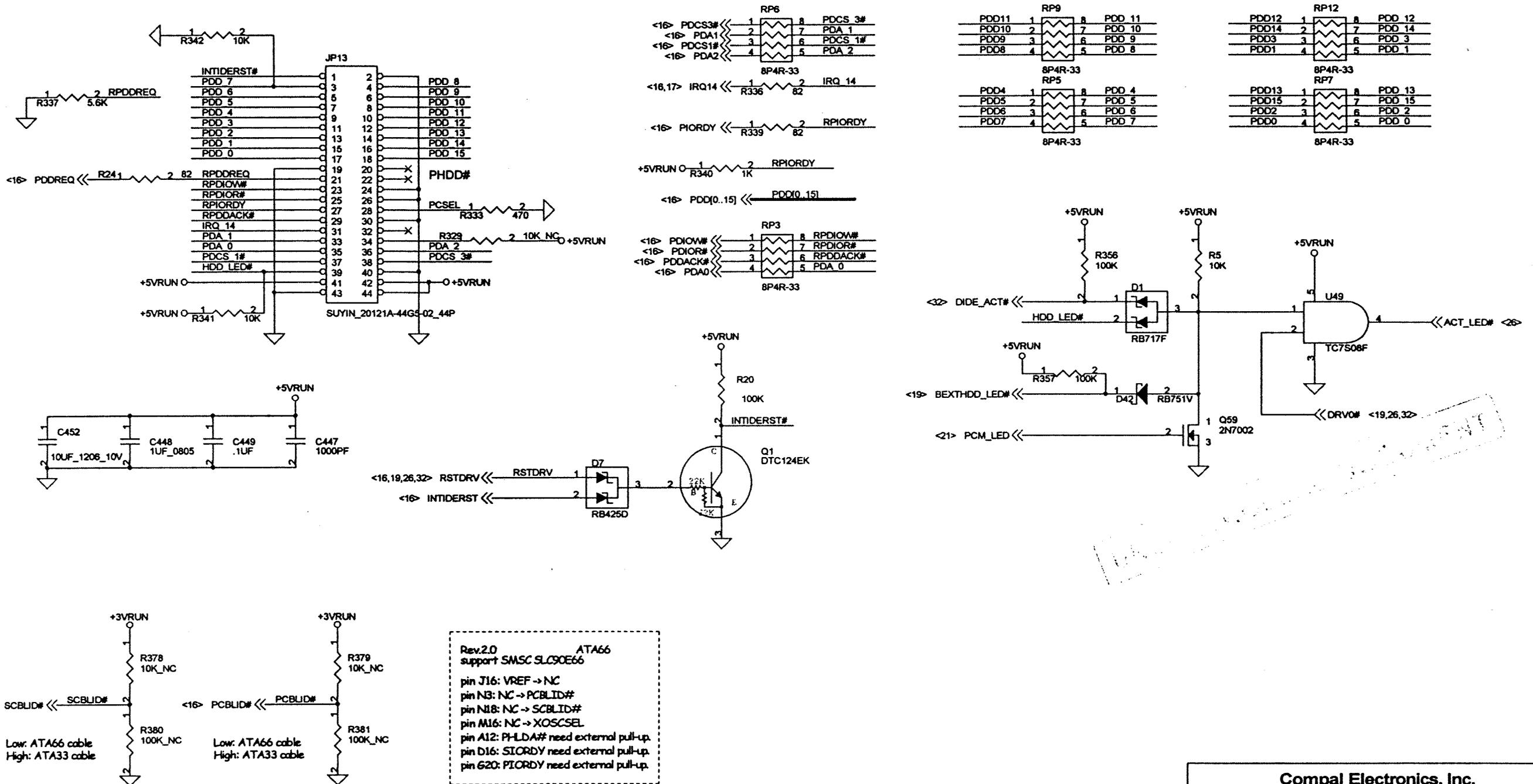


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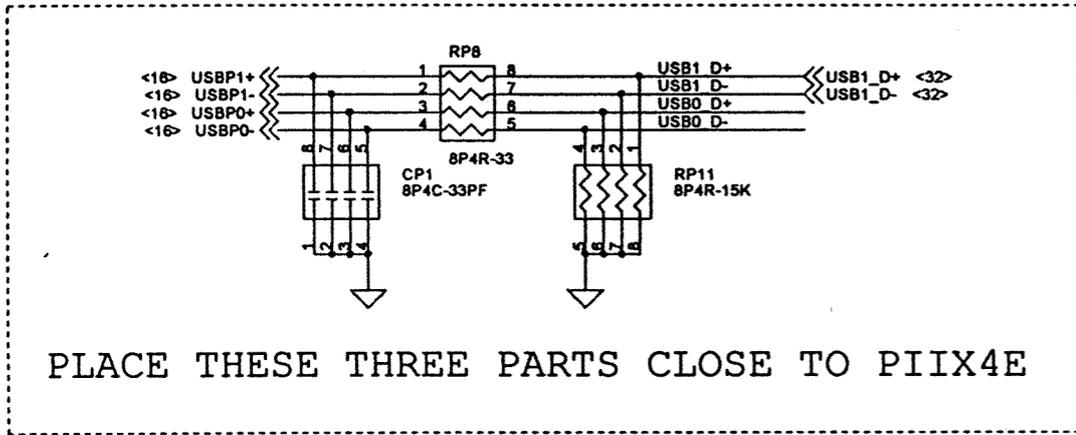
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SCHEMATIC, M/B LA-542		
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# IDE CONN.



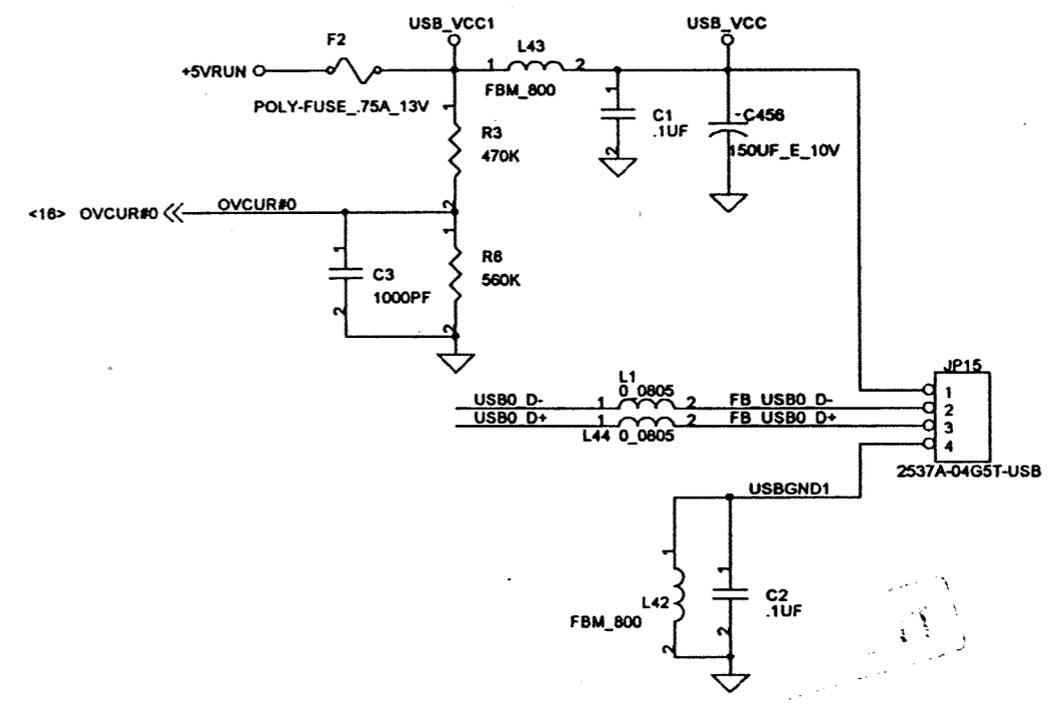
Rev.2.0 ATA66 support SMSC SLC90E66  
 pin J16: VREF -> NC  
 pin N3: NC -> PCBLID#  
 pin N18: NC -> SCBLID#  
 pin M16: NC -> XOSCSEL  
 pin A12: PHLDA# need external pull-up.  
 pin D16: SIORDY need external pull-up.  
 pin G20: PIORDY need external pull-up.



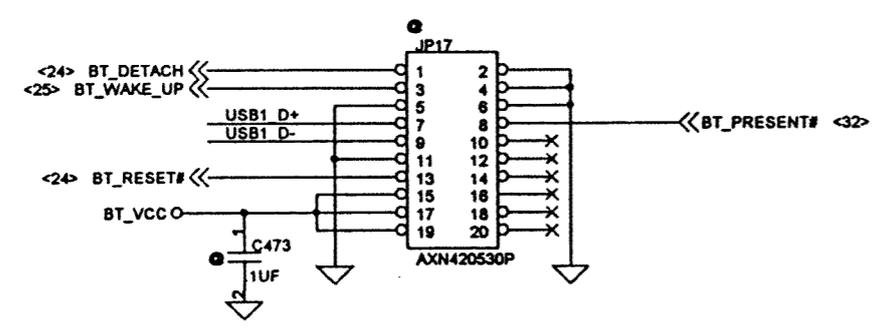
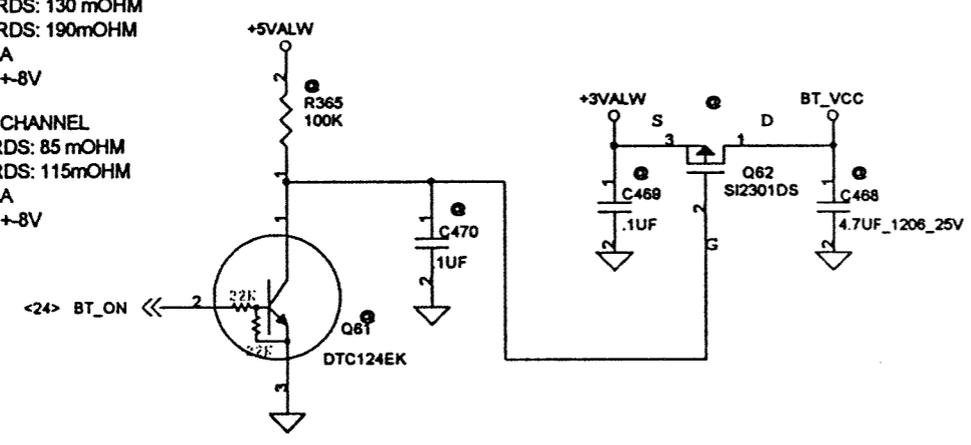


PLACE THESE THREE PARTS CLOSE TO PIIX4E

# USB CONNECTOR



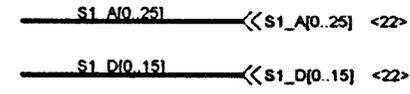
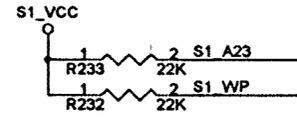
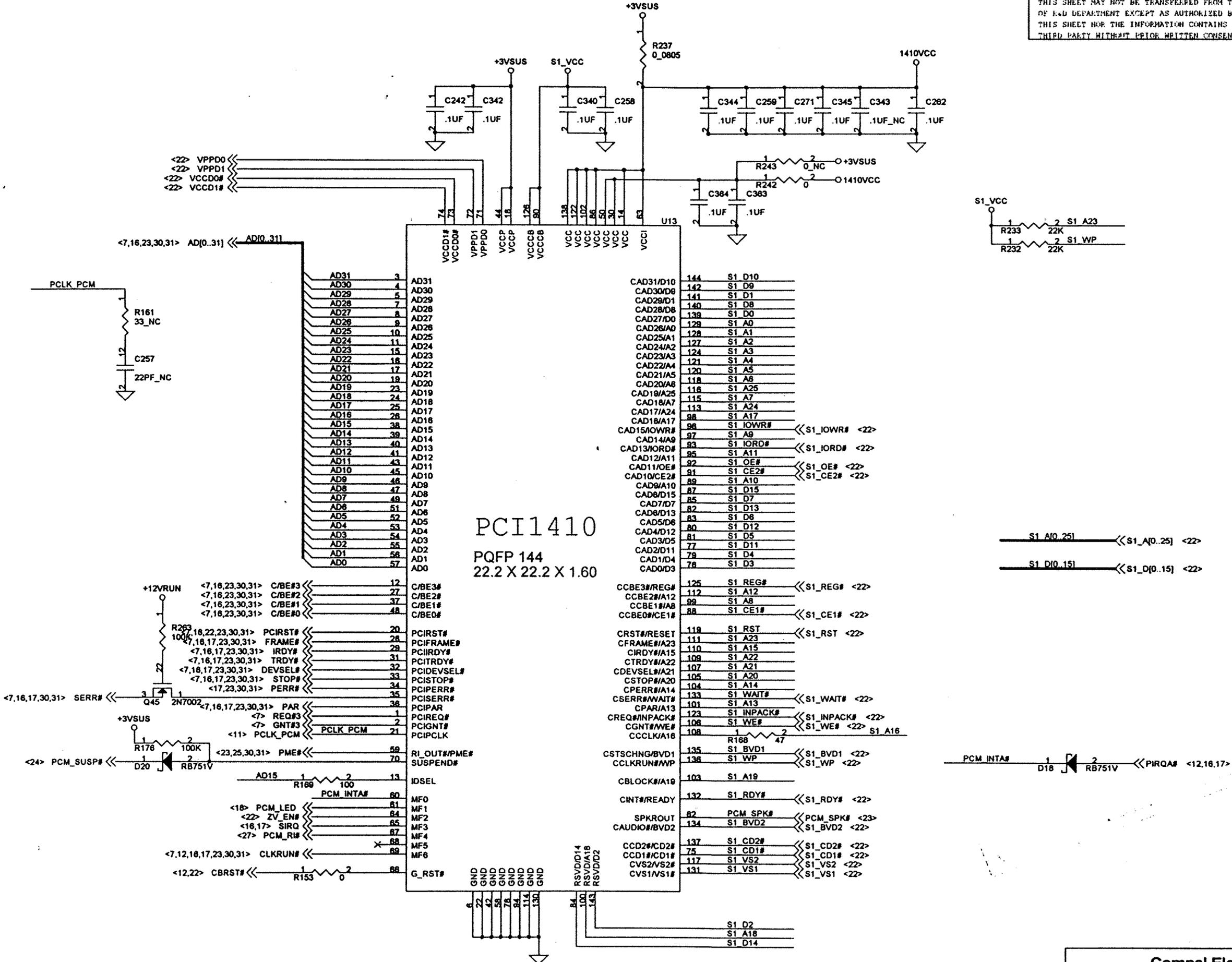
SI2301DS: P CHANNEL  
 VGS: -4.5V, RDS: 130 mOHM  
 VGS: -2.5V, RDS: 190mOHM  
 Id(MAX): 2.3A  
 VGS(MAX): +8V  
 SI2302DS: N CHANNEL  
 VGS: 4.5V, RDS: 85 mOHM  
 VGS: 2.5V, RDS: 115mOHM  
 Id(MAX): 2.8A  
 VGS(MAX): +8V

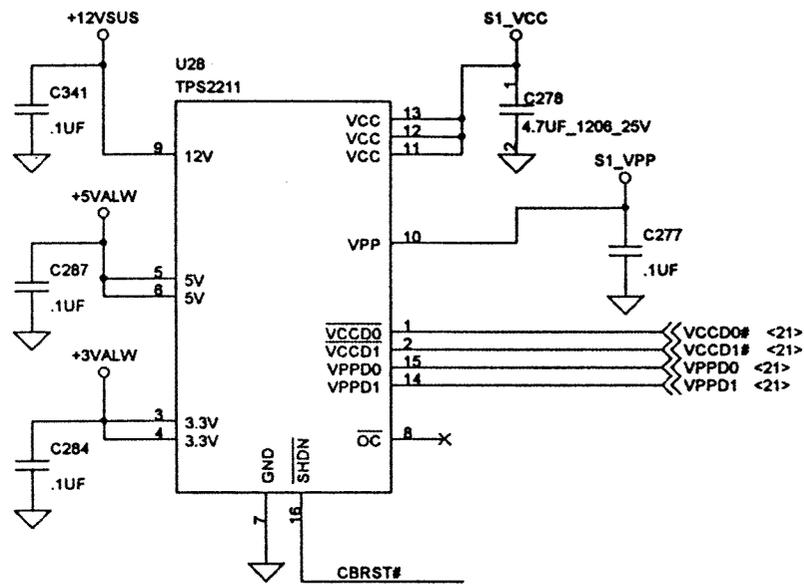


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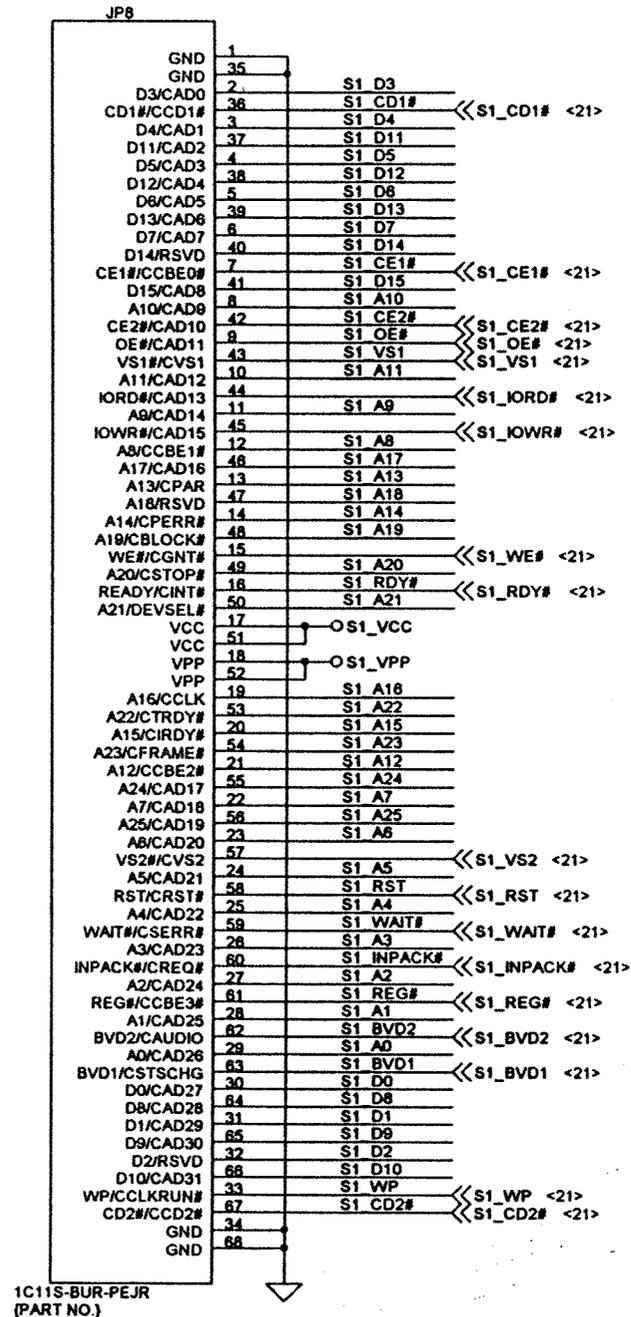
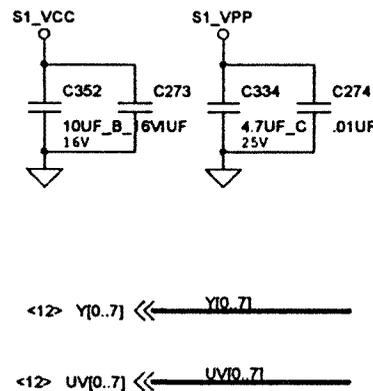
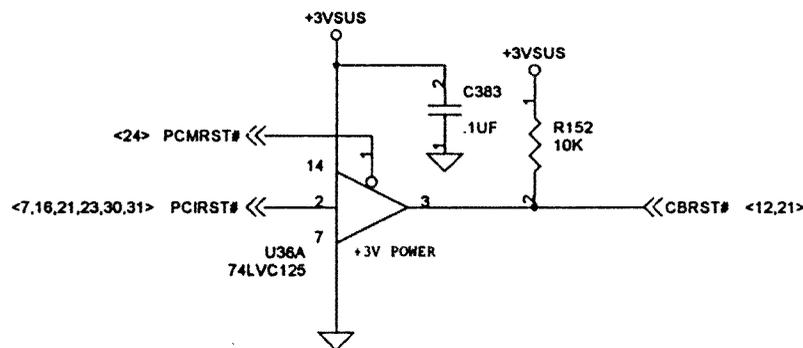
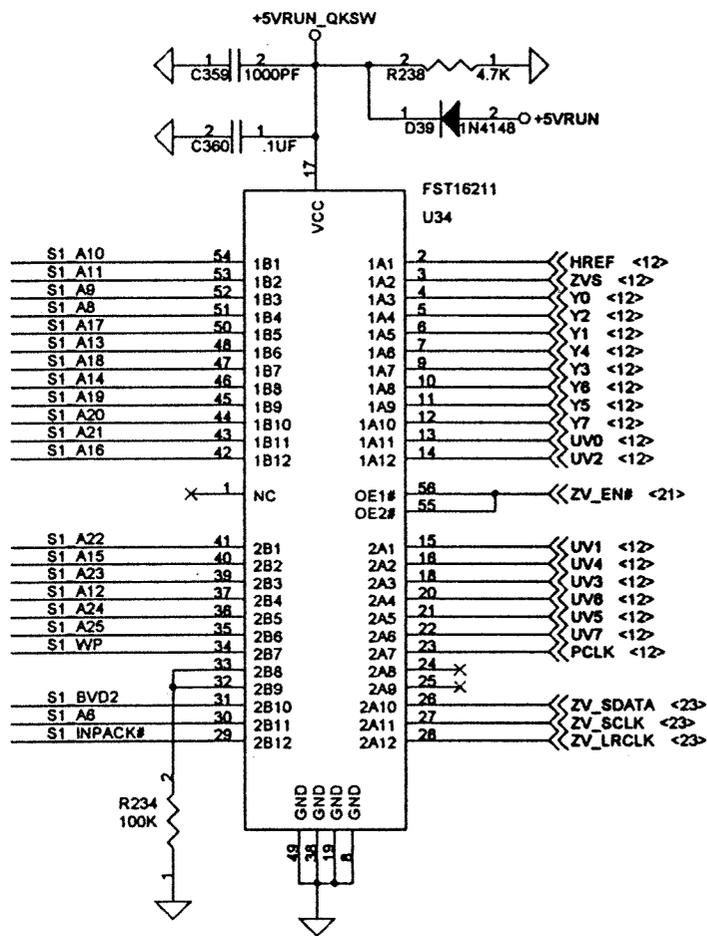
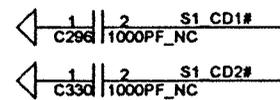
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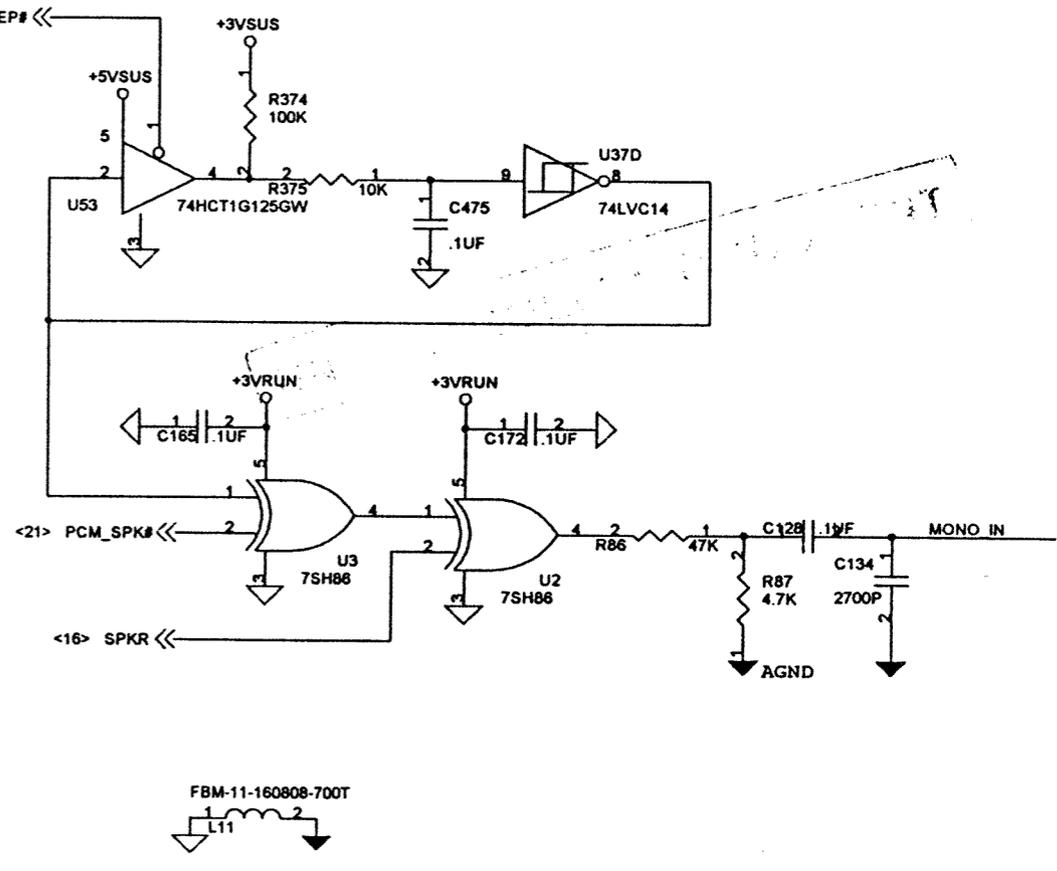
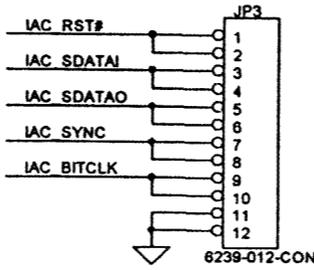
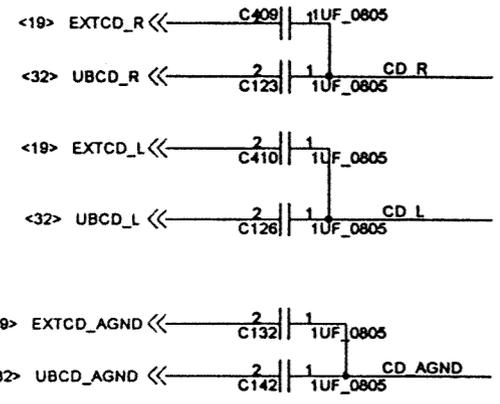
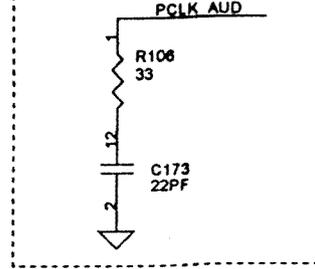
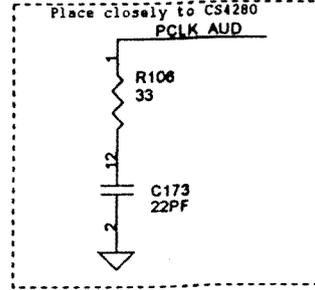
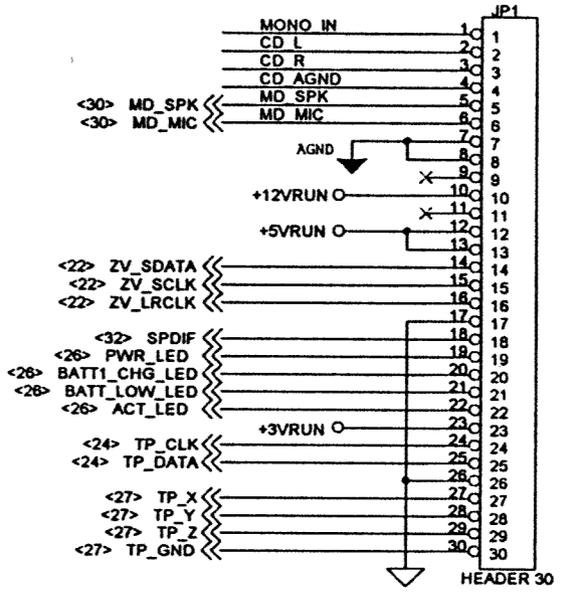
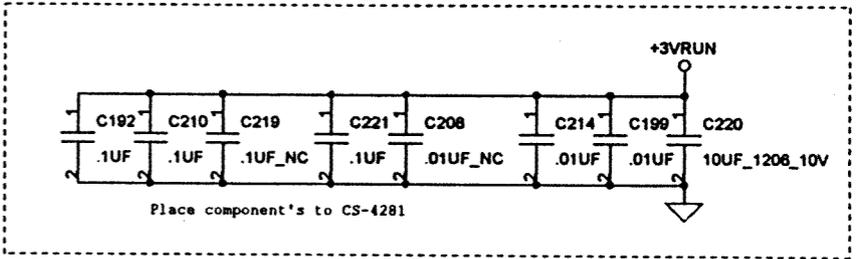
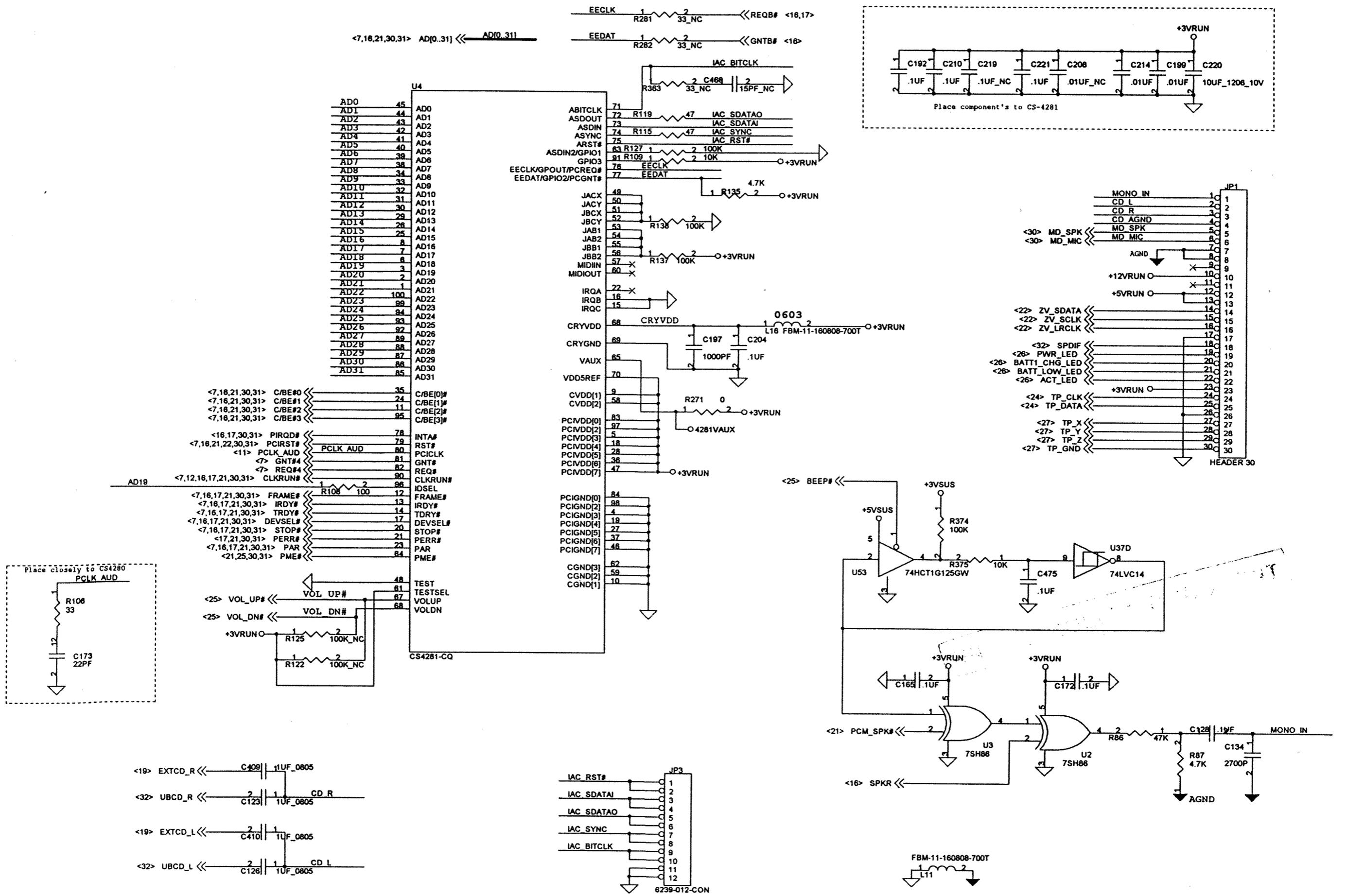
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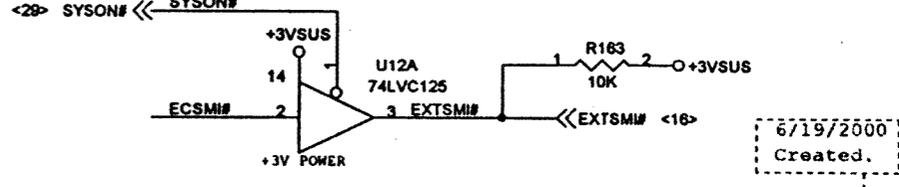
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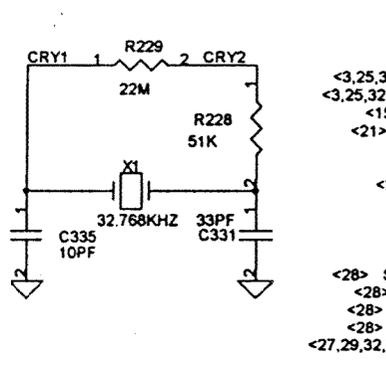
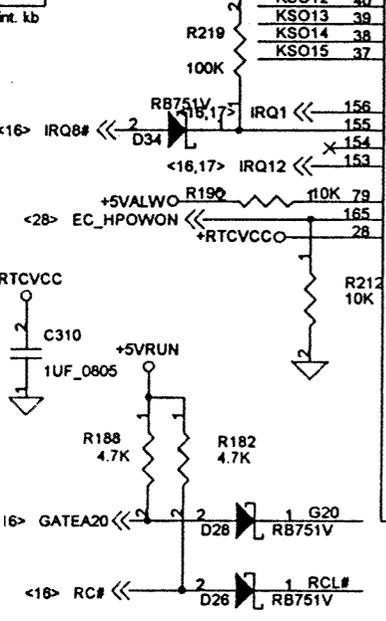
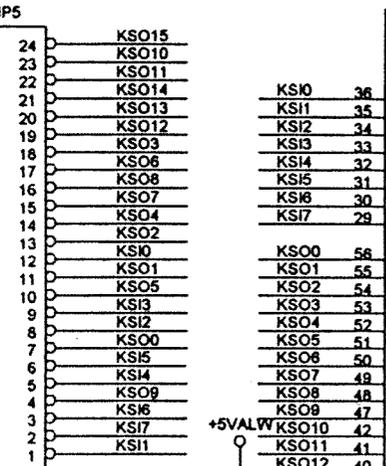
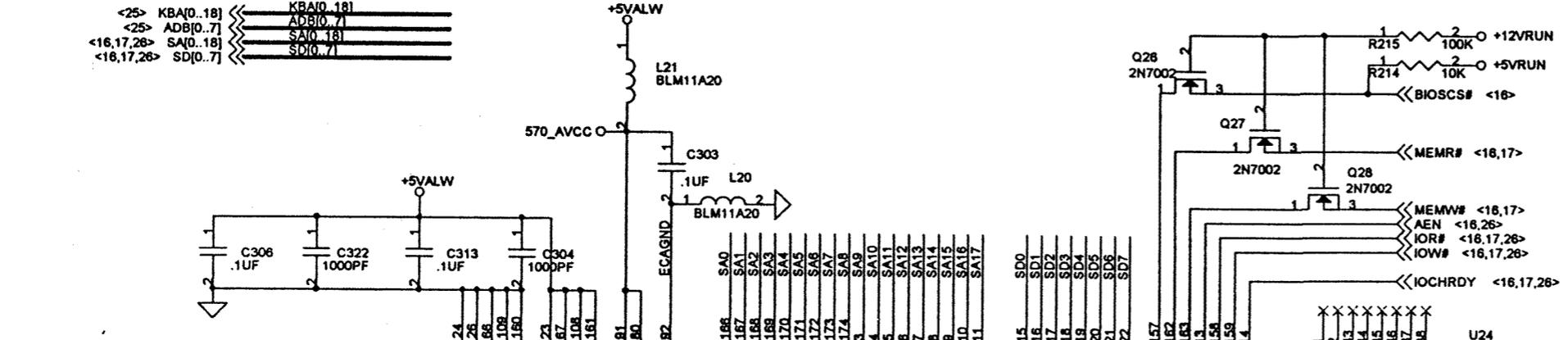
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6/19/2000 Created.



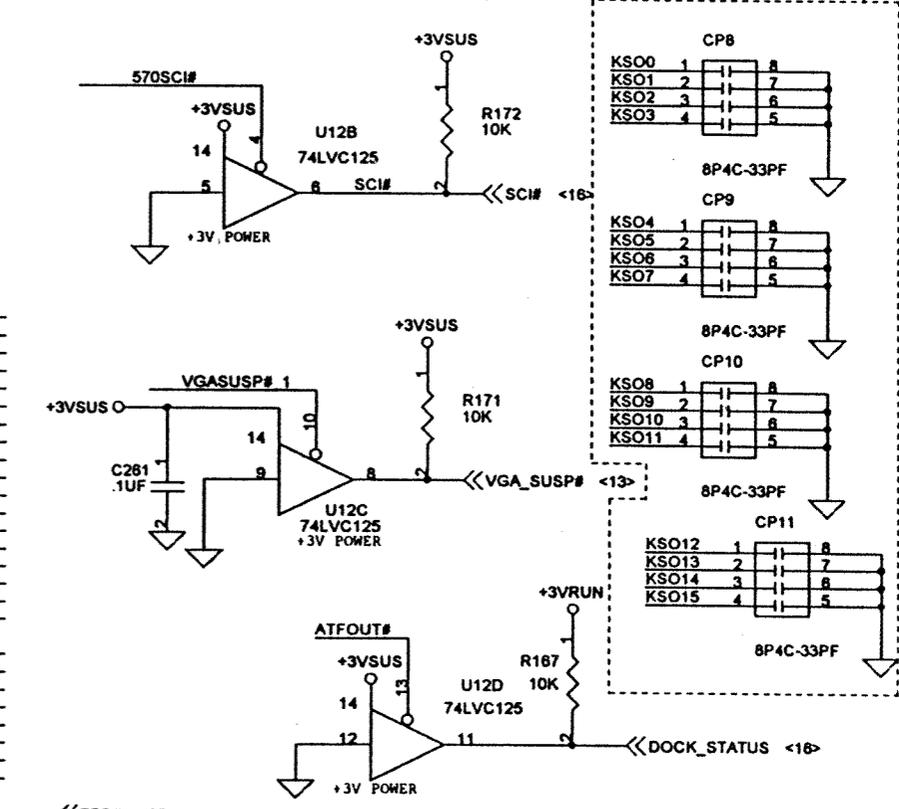
Environment	EMV0 (P104)	EMV1 (P103)	Mode (P105)	HRMS#
IRE	0	0	Reset host when shared memory access can not be completed	1
IRD	0	1	Extend access until completed	0
Development	1	0		

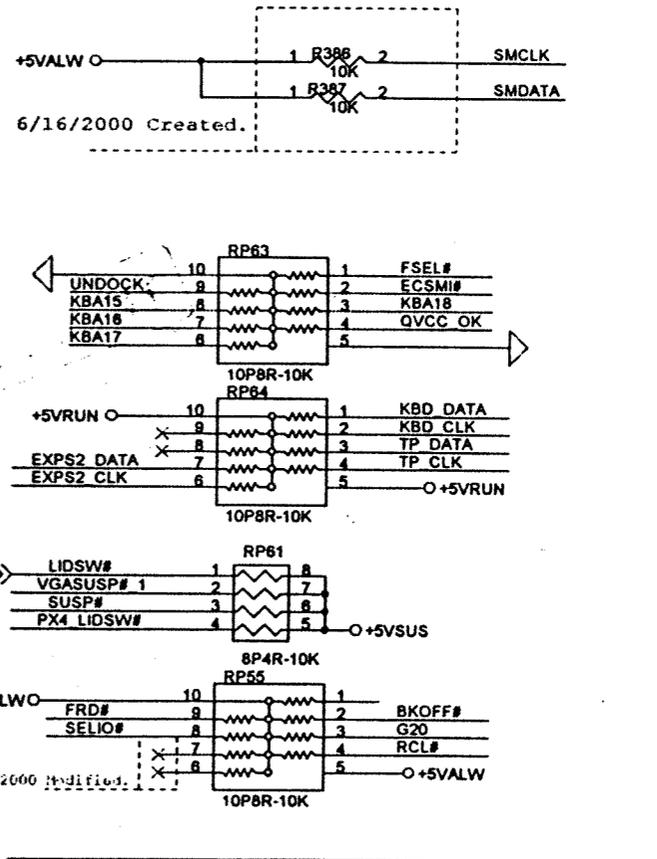
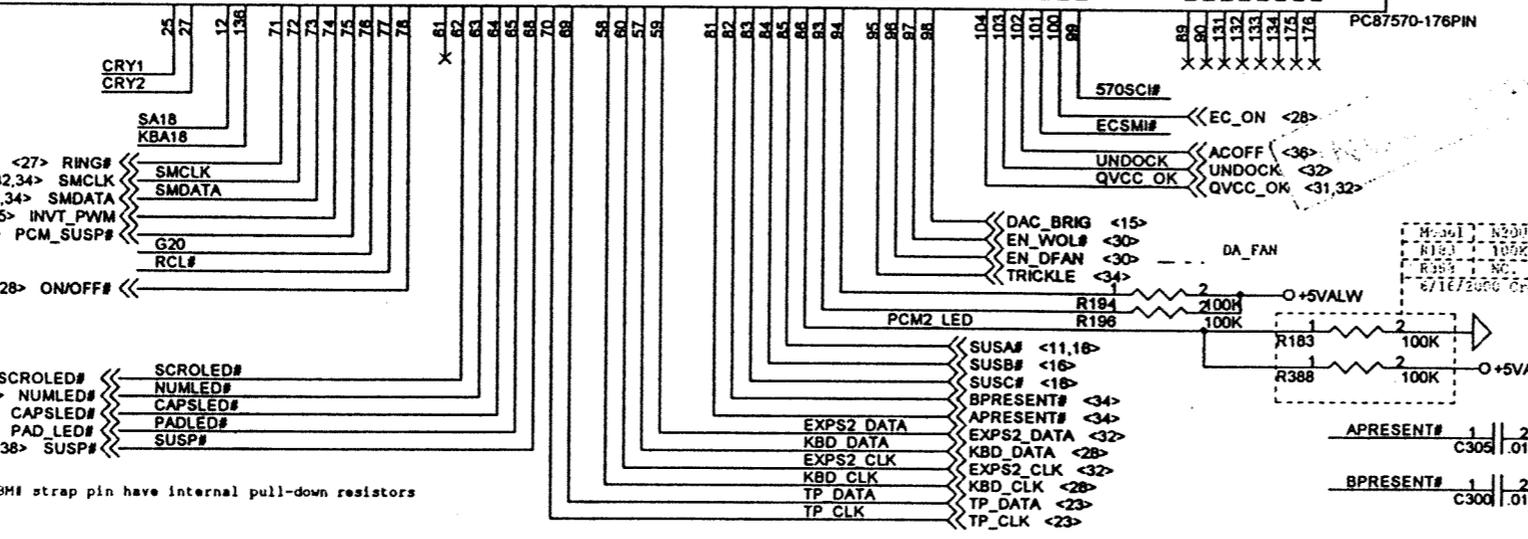
Mode	FXBUSEN# (P130)	FXBUSEN#
1	Non Shared Memories	1
0	Shared Memories	0

Mode	HDEN# (P111)	HDEN#	TRIS (TRI-STATE) (P102)
1	Device are enabled o reset	1	Normally
0	Devices are disabled on reset	0	TriState



6/16/2000 Created.



6/14/2000 Modified.

EMV0,1 TRIS# HRMS# HDEN# FXBUSEN# SHBM# strap pin have internal pull-down resistors

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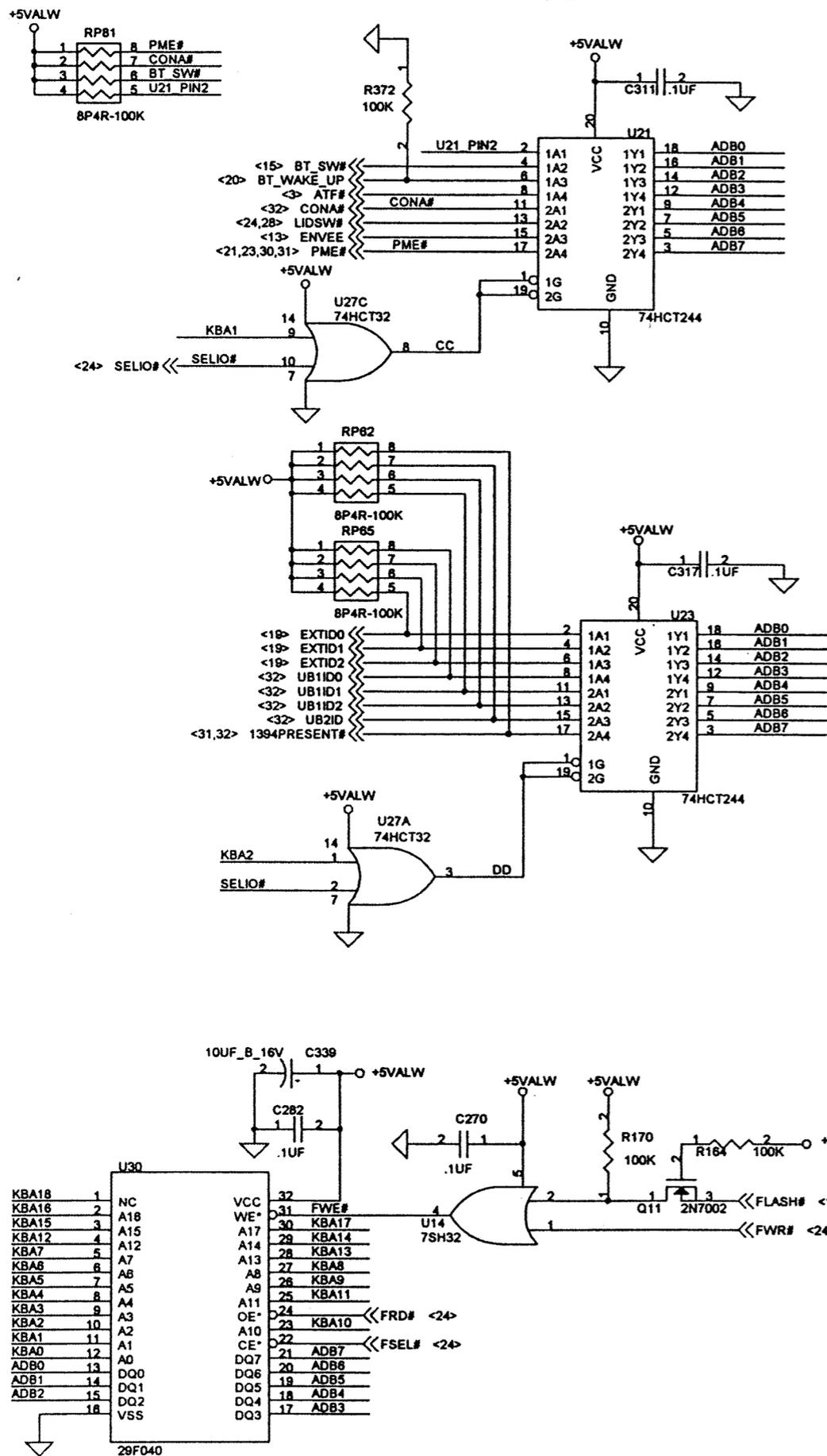
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Size: Document Number 401130

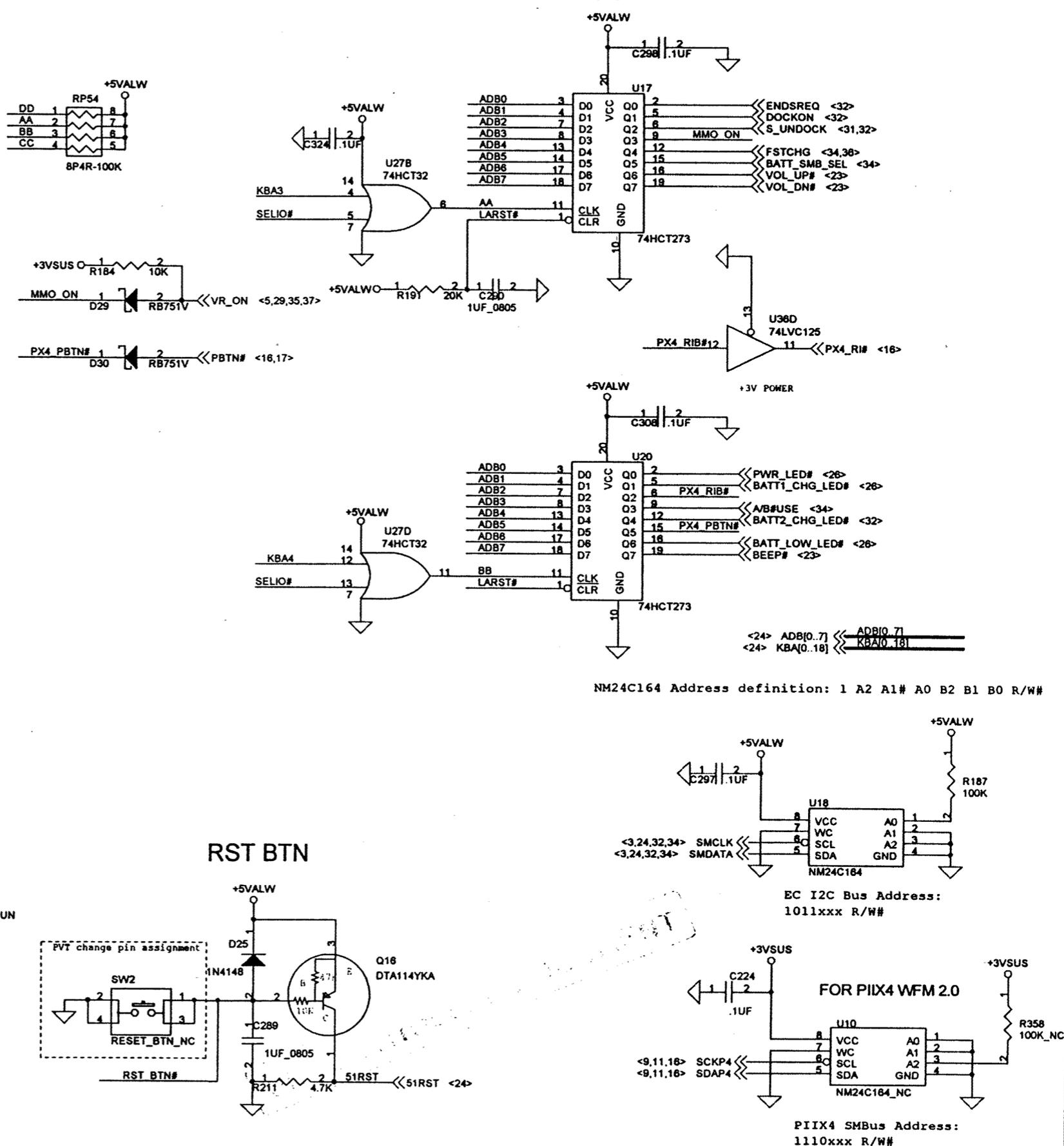
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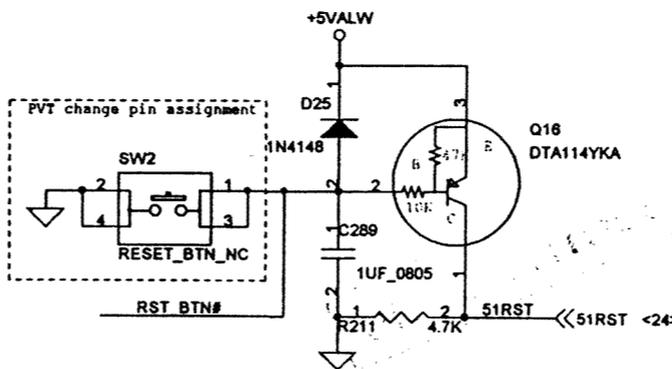
INPUT



OUTPUT



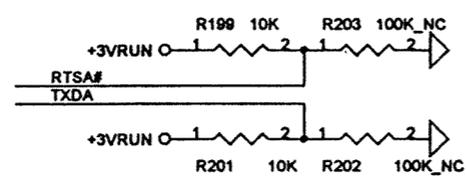
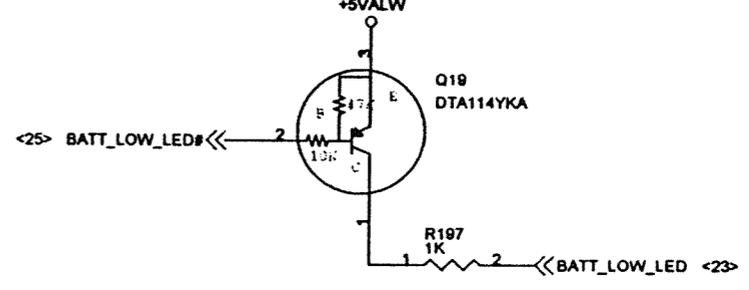
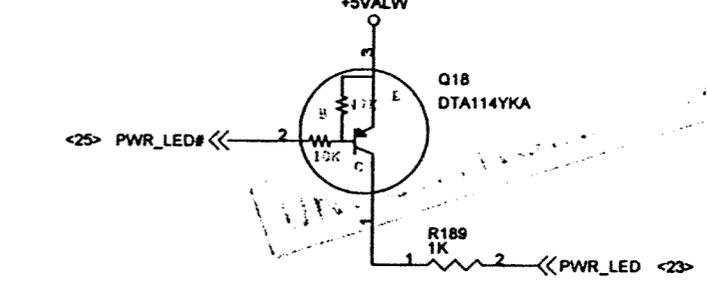
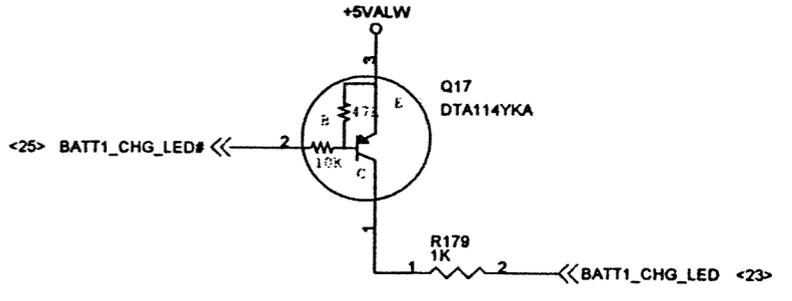
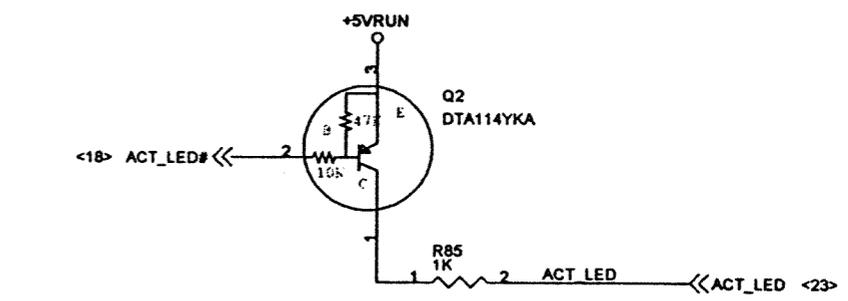
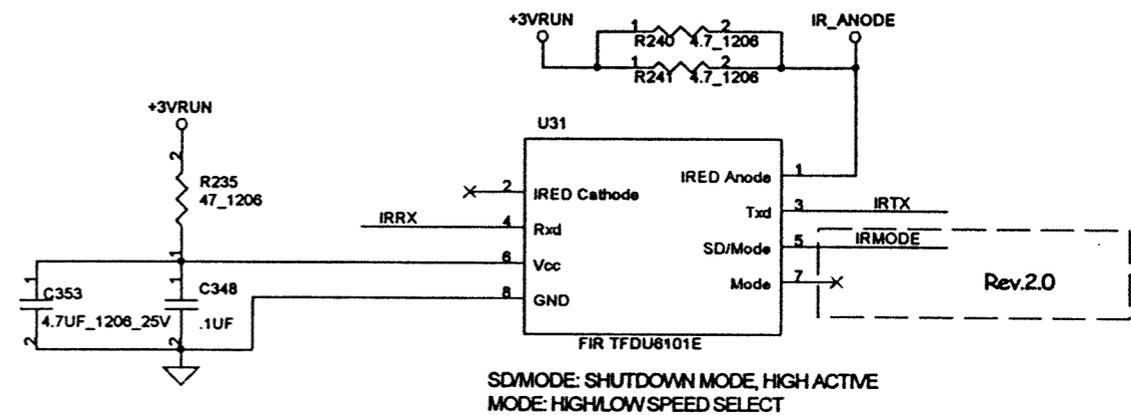
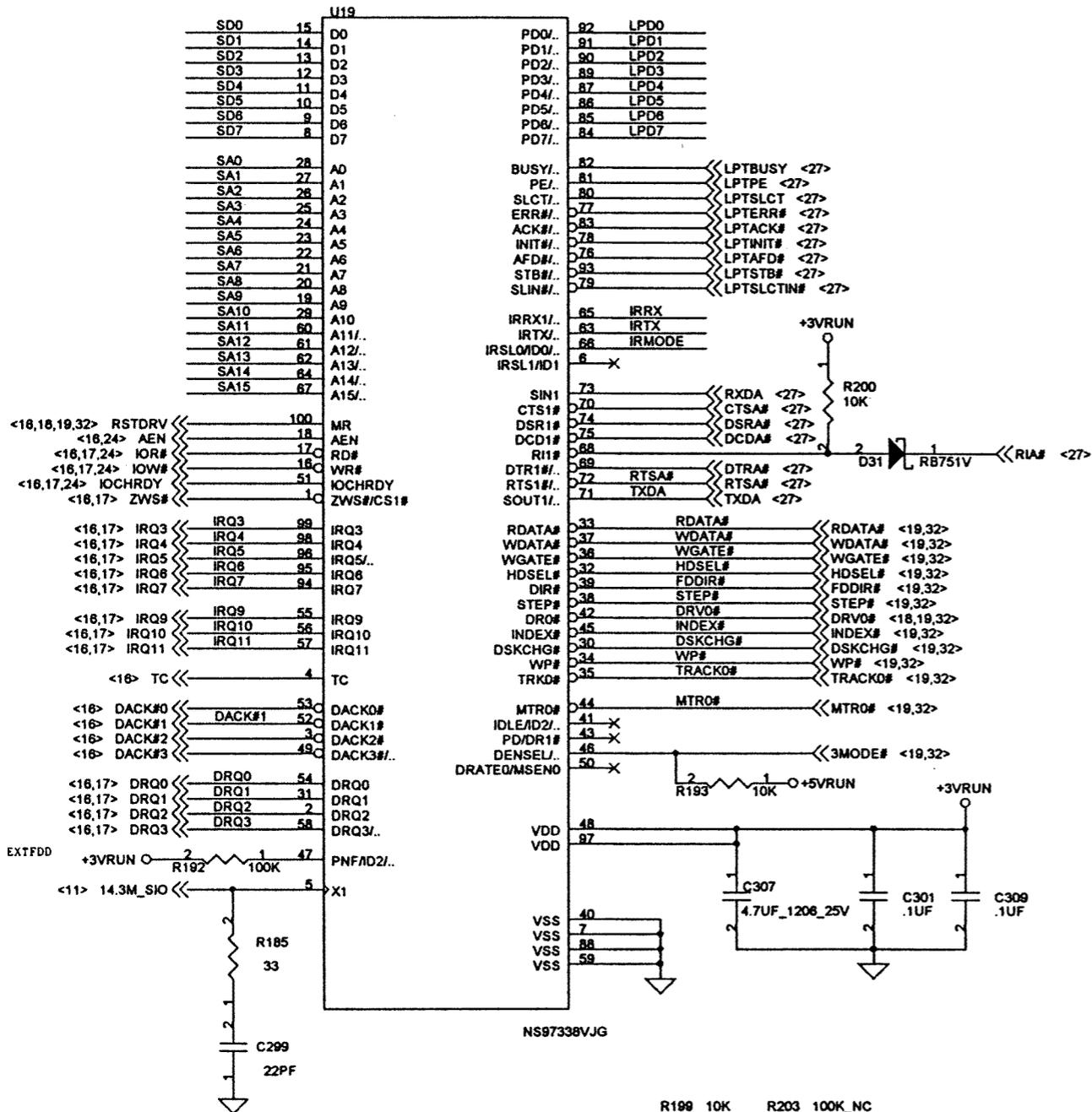
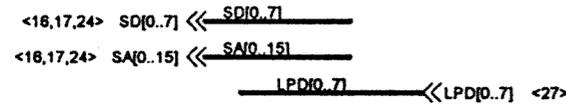
RST BTN



Compal Electronics, Inc.

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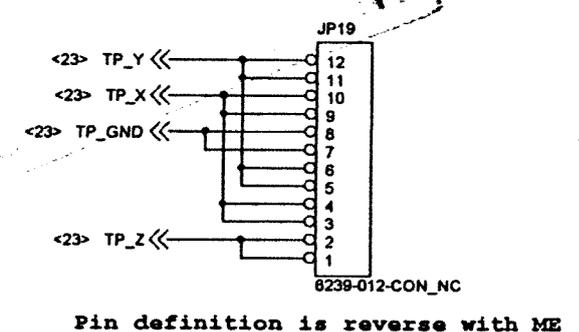
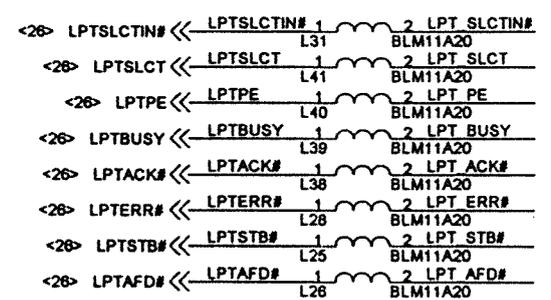
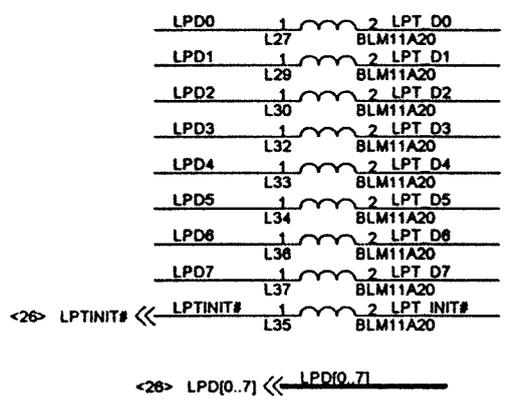
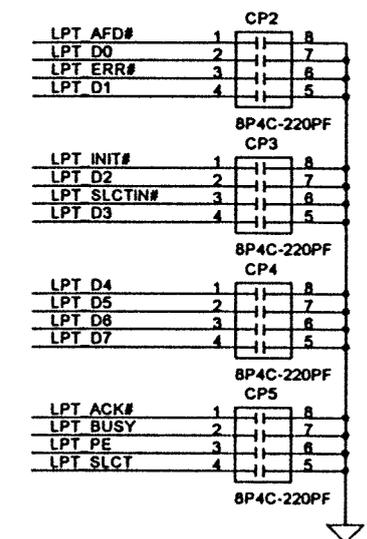
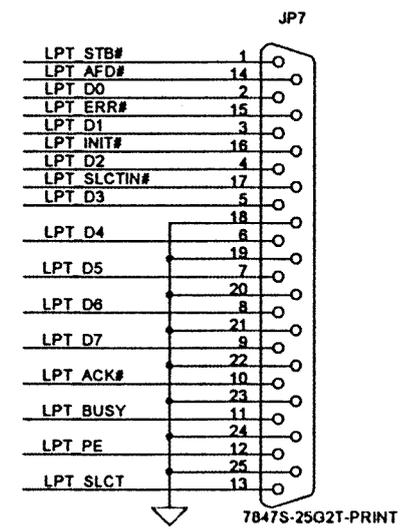
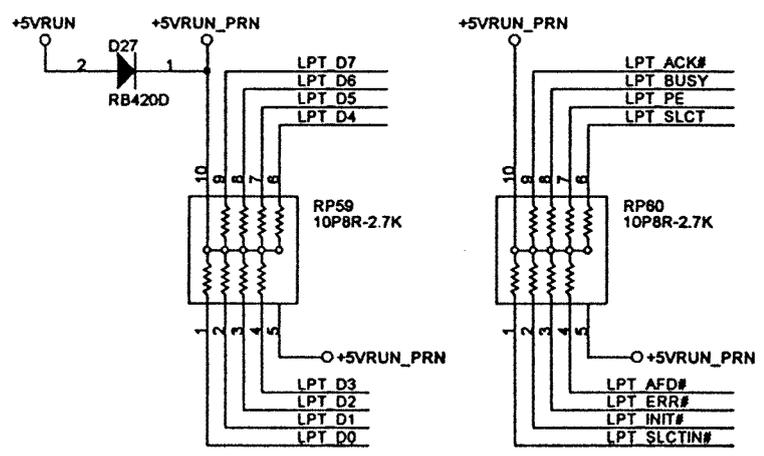
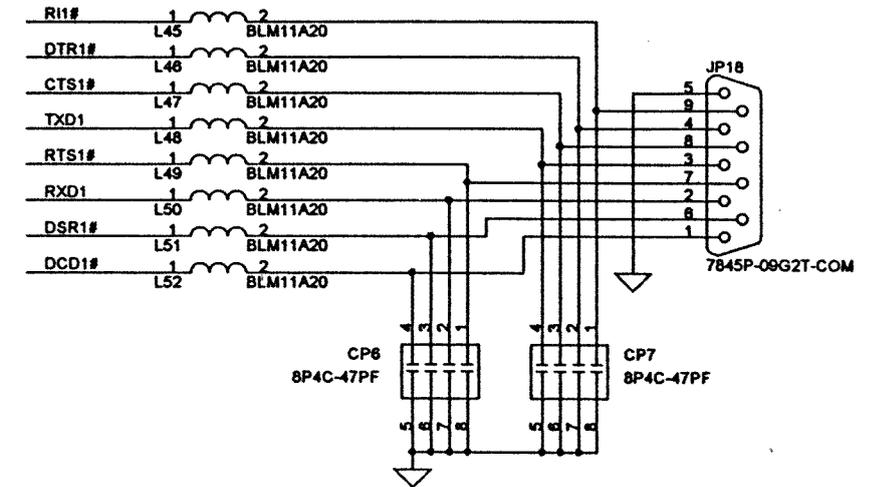
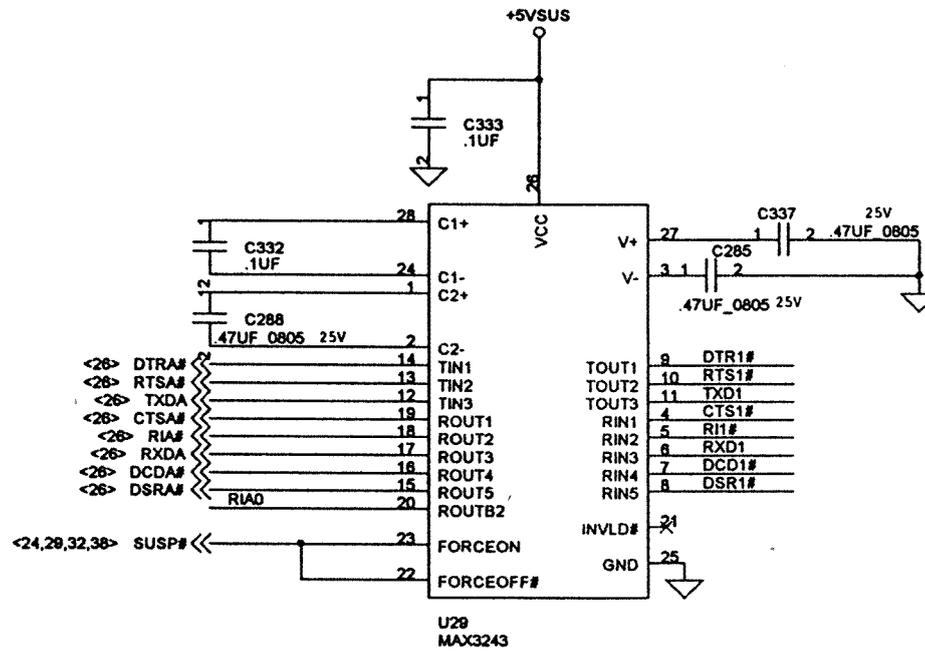
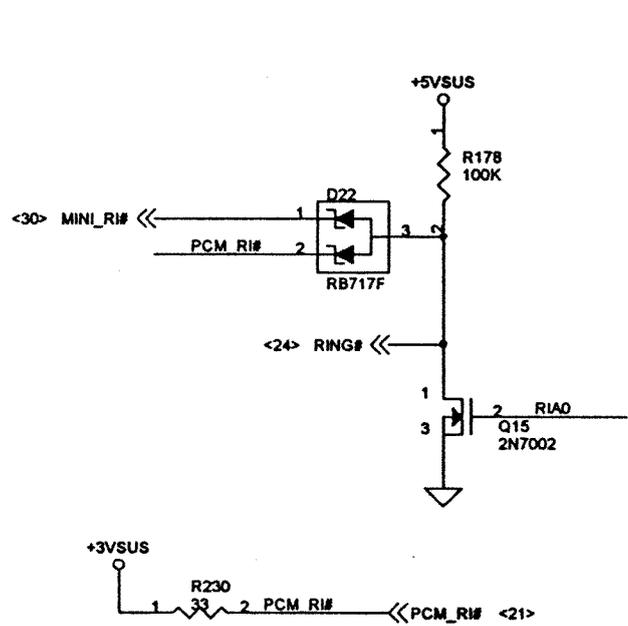
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# SERIAL/PARALLEL PORT

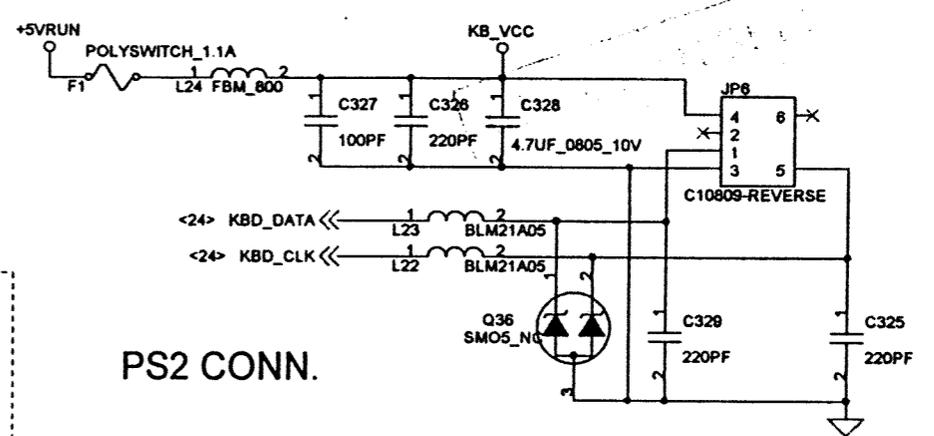
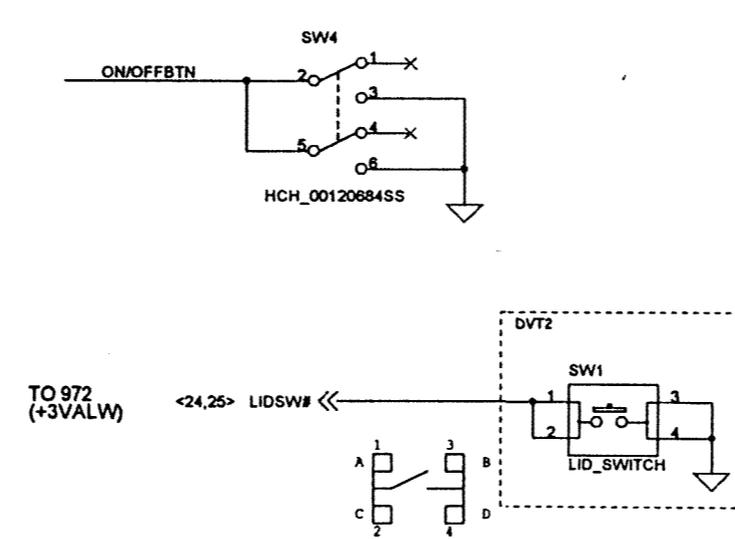
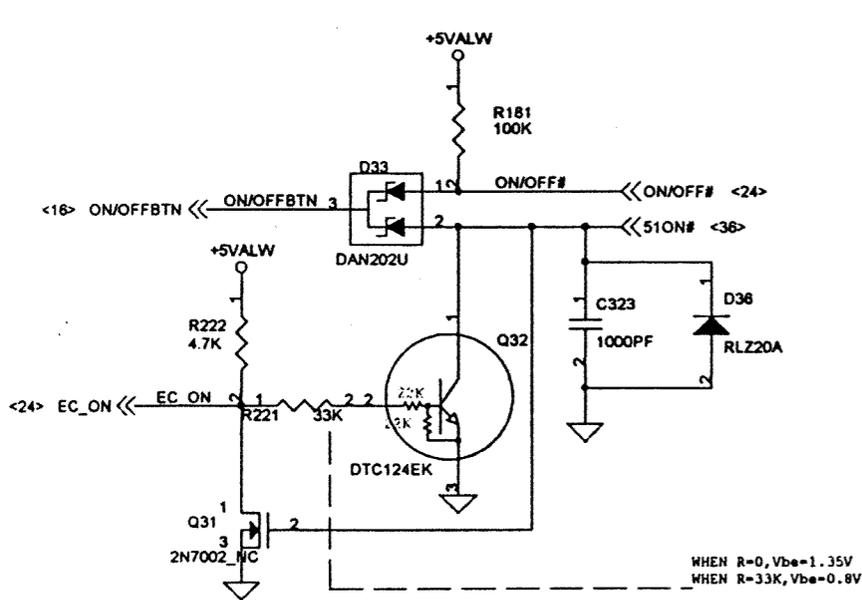
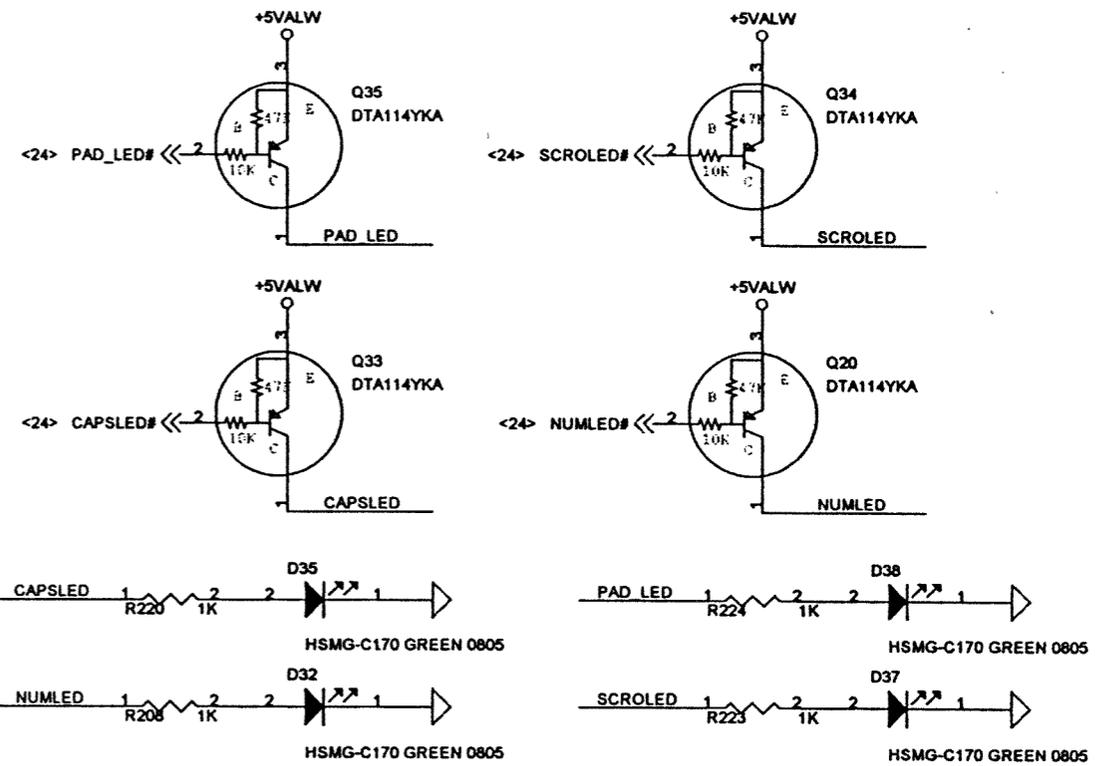
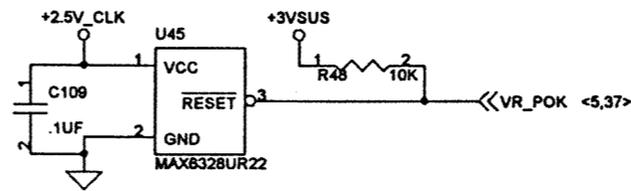
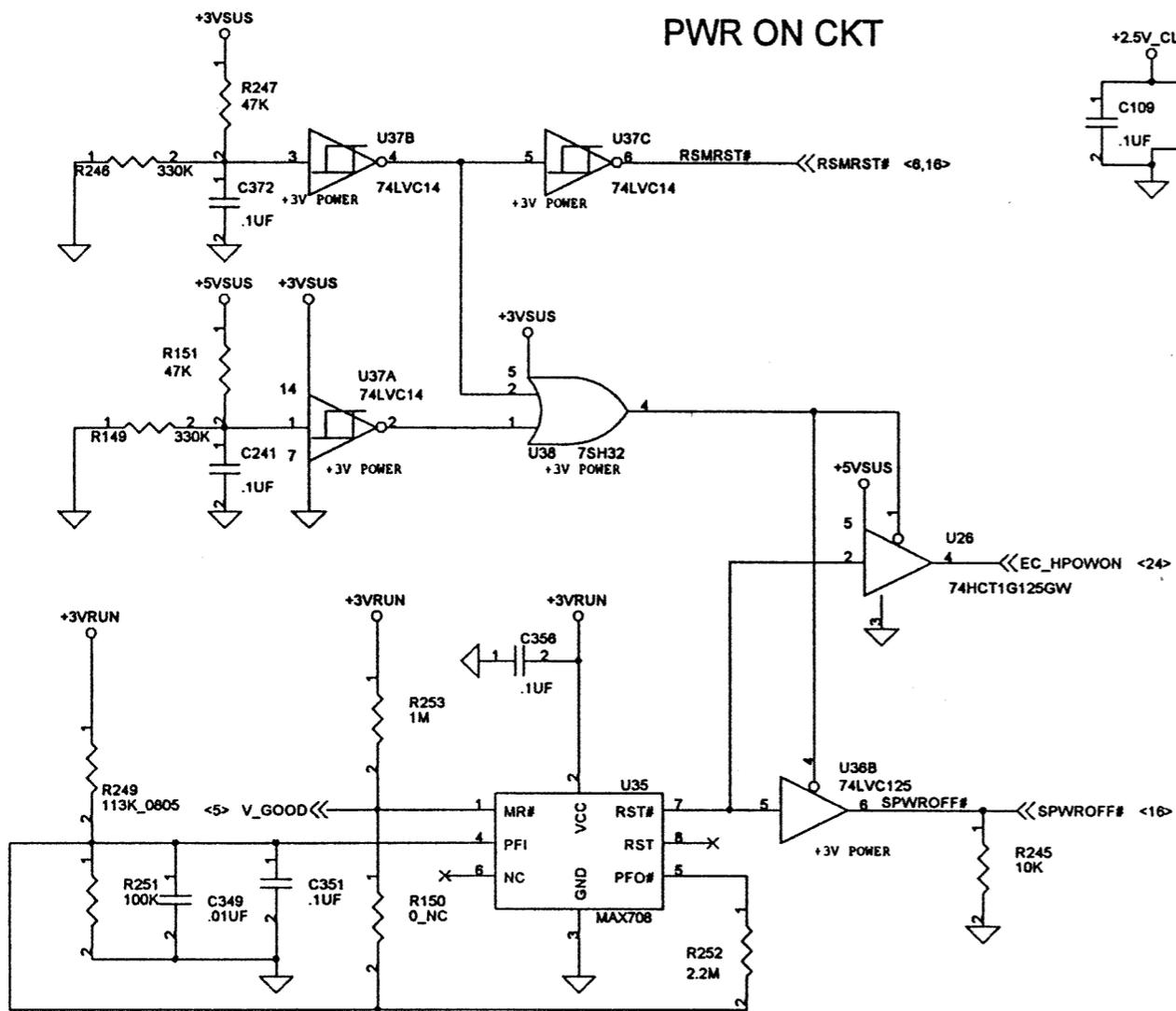


Pin definition is reverse with ME

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# PWR ON CKT

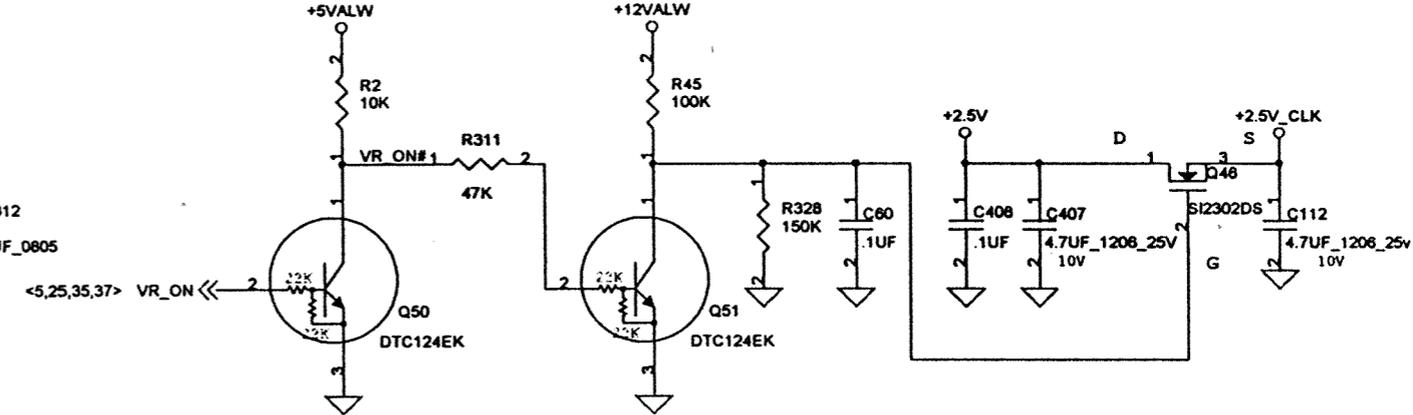
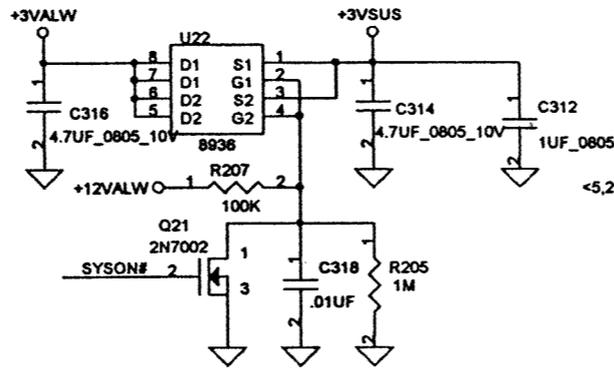
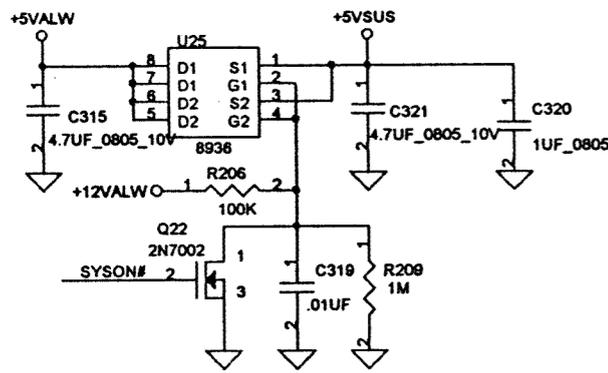
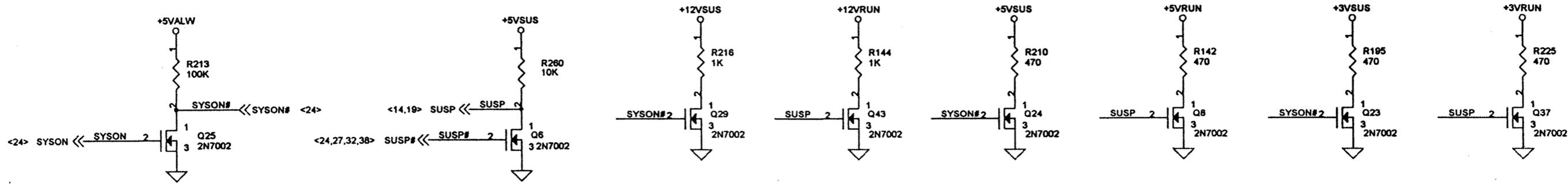


Change R214: 4.7k -> 22k, R215: 33k -> 22k, remove Q15.

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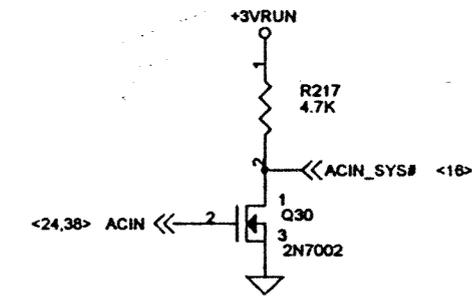
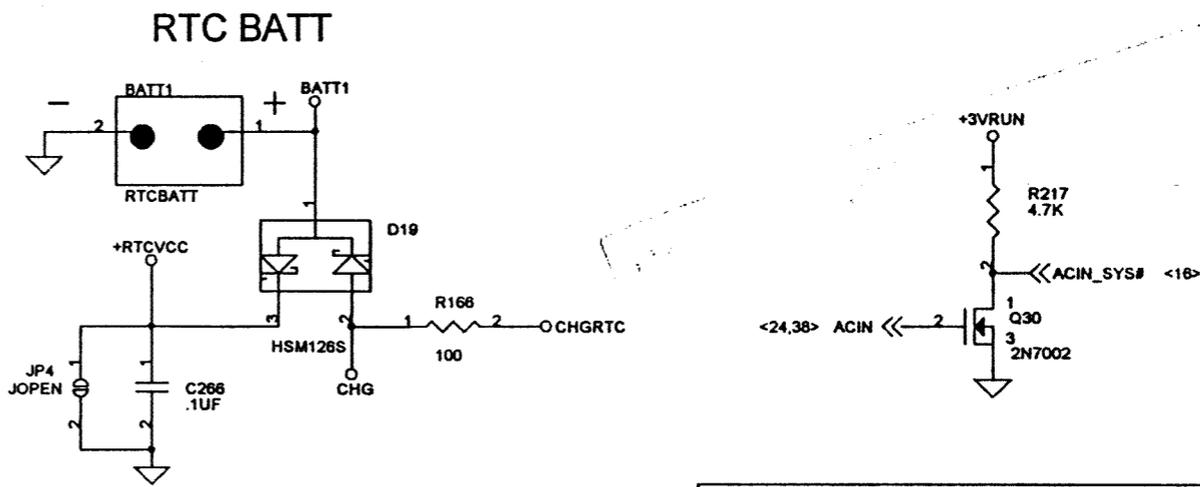
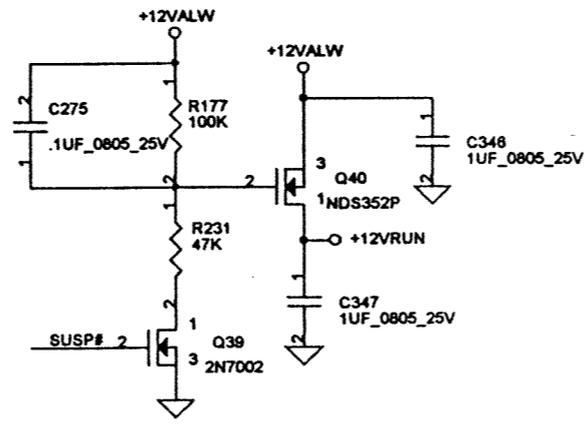
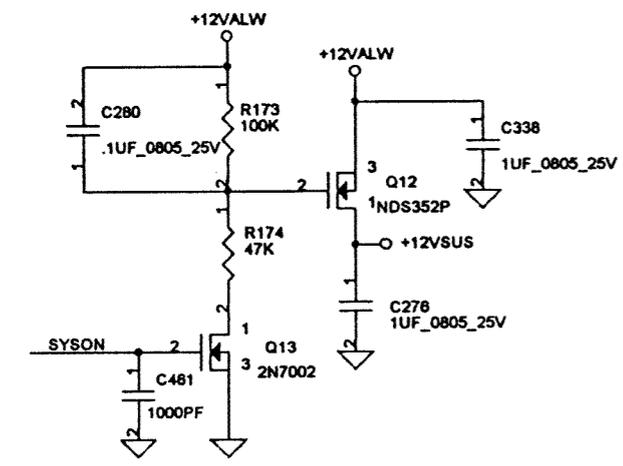
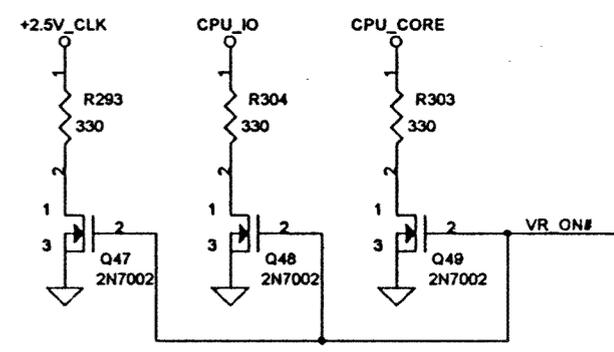
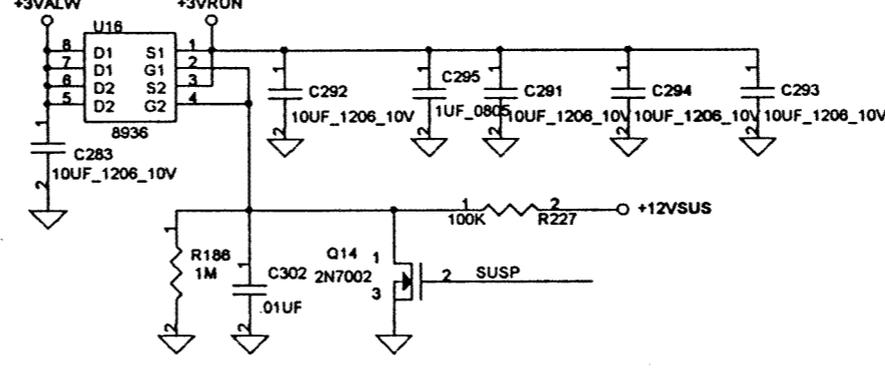
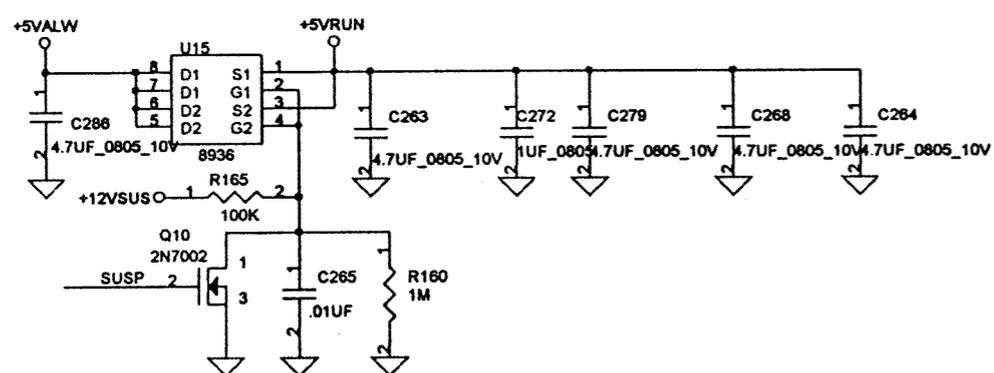
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N31B2



SI2301DS: P CHANNEL  
 VGS: -4.5V, RDS: 130 mOHM  
 VGS: -2.5V, RDS: 190mOHM  
 Id(MAX): 2.3A  
 VGS(MAX): +8V

SI2302DS: N CHANNEL  
 VGS: 4.5V, RDS: 85 mOHM  
 VGS: 2.5V, RDS: 115mOHM  
 Id(MAX): 2.8A  
 VGS(MAX): +8V

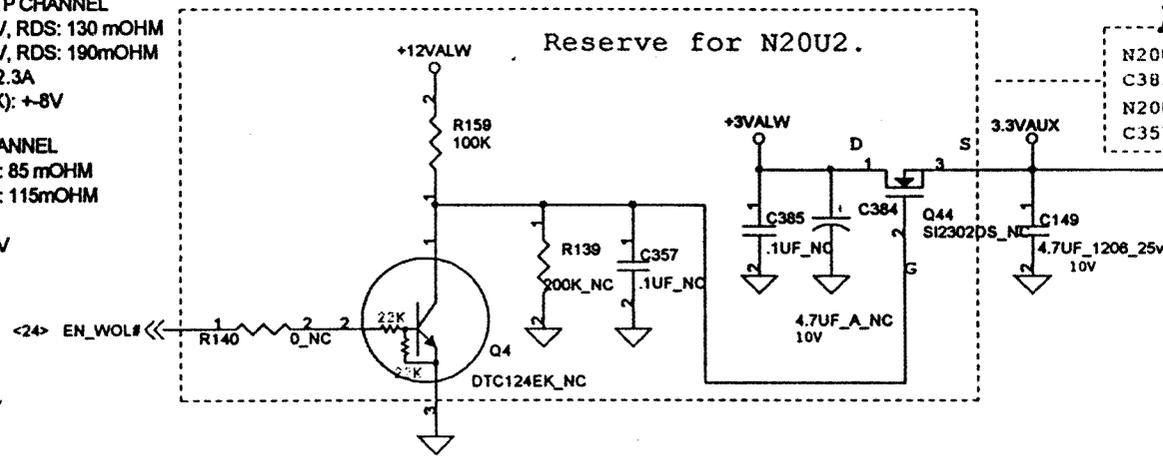


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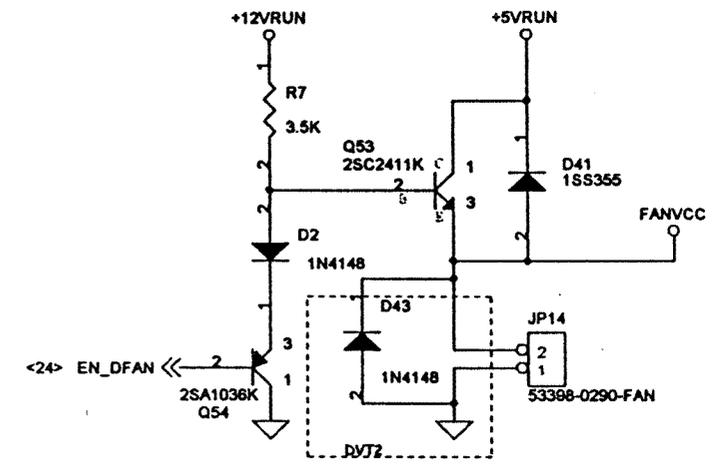
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 VGS: -4.5V, RDS: 130 mOHM  
 VGS: -2.5V, RDS: 190mOHM  
 Id(MAX): 2.3A  
 VGS(MAX): +8V

SI2302DS: N CHANNEL  
 VGS: 4.5V, RDS: 85 mOHM  
 VGS: 2.5V, RDS: 115mOHM  
 Id(MAX): 2.8A  
 VGS(MAX): +8V

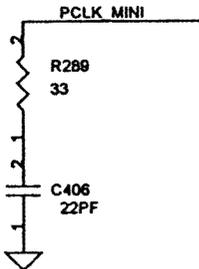
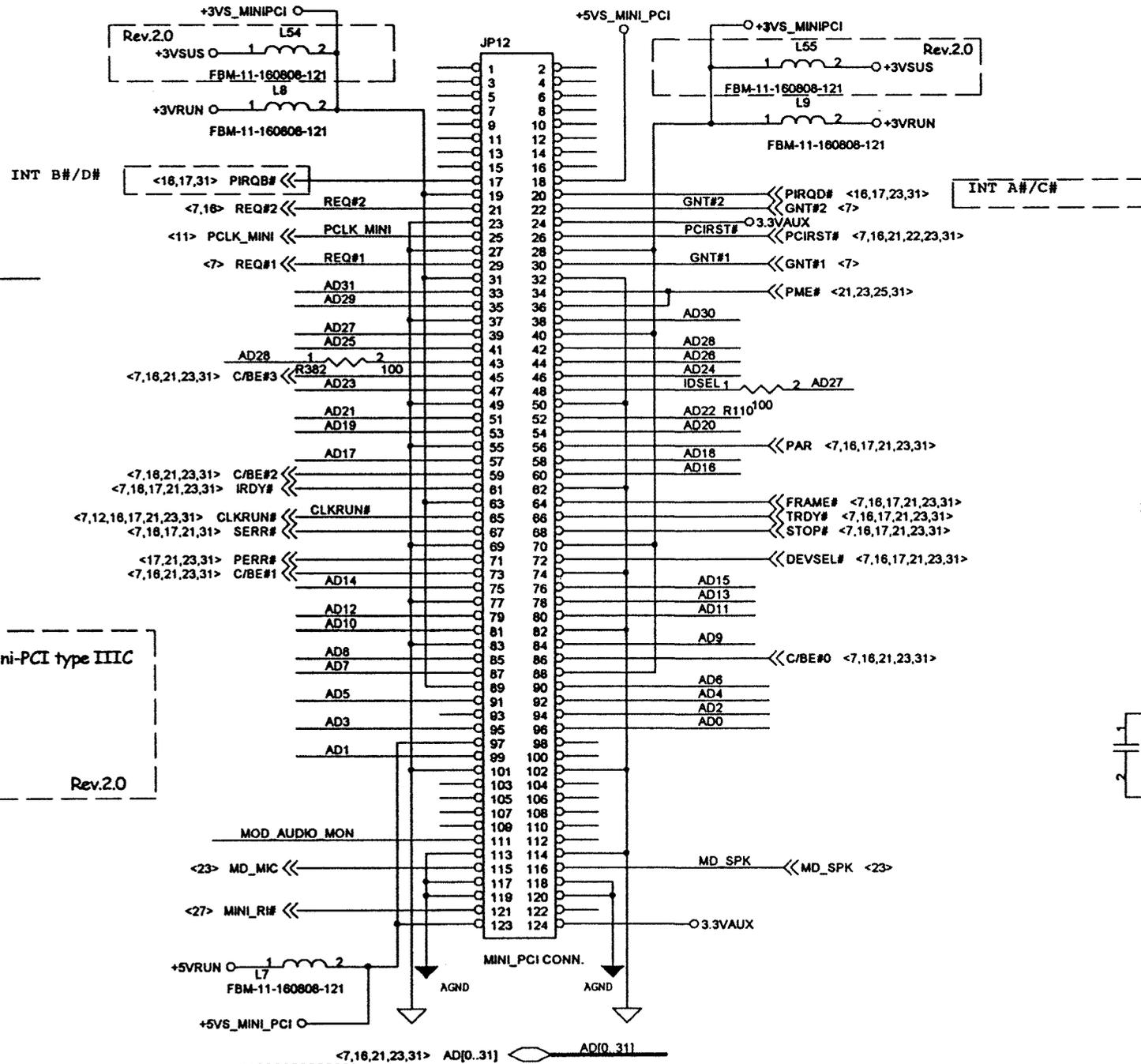


**MODEM CONN.**

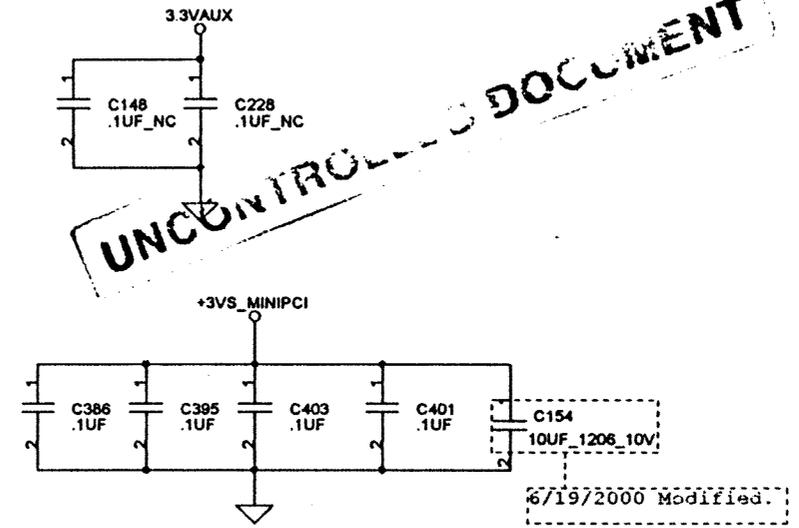
N20U: R389 0\_0805 NC. R140, R159, Q4, R139, C357, C385, C384, Q44 mount parts. C384 4.7UF\_A\_NC.  
 N20U2: R389 0\_0805. R140, R159, Q4, R139, C357, C385, C384, Q44 NC.  
 6/16/2000 Modified.



**FAN CONN.**



For Compal private Mini-PCI Combo card - Mini-PCI type IIIC  
 pin 21. LAN REQ# (use REQ#2)  
 pin 22. LAN GNT# (use GNT#2)  
 pin 36. LAN PME#  
 pin 43. LAN IDSEL (use AD28)  
 pin 121. MODEM RING#  
 Rev.2.0

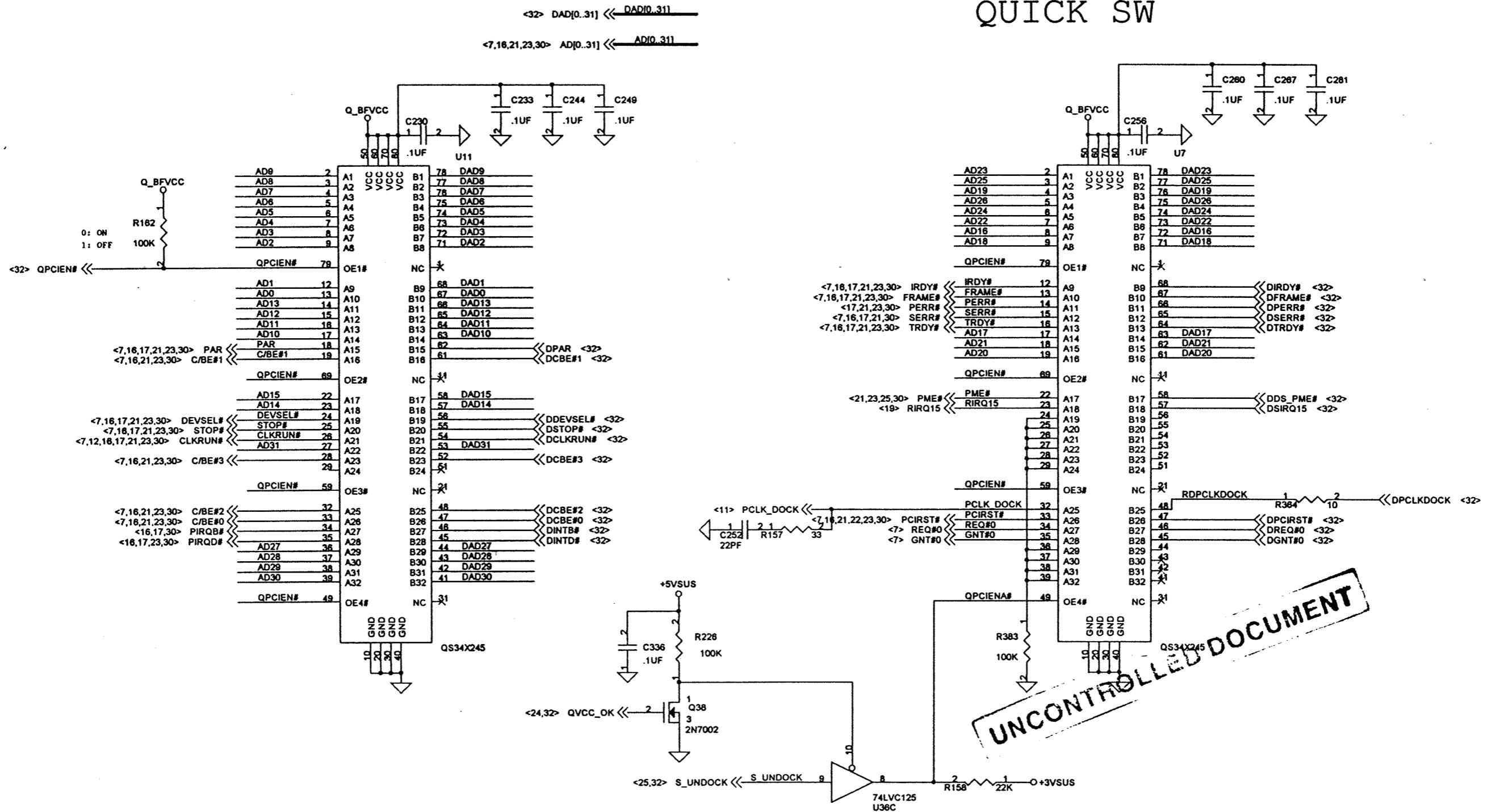


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# QUICK SW



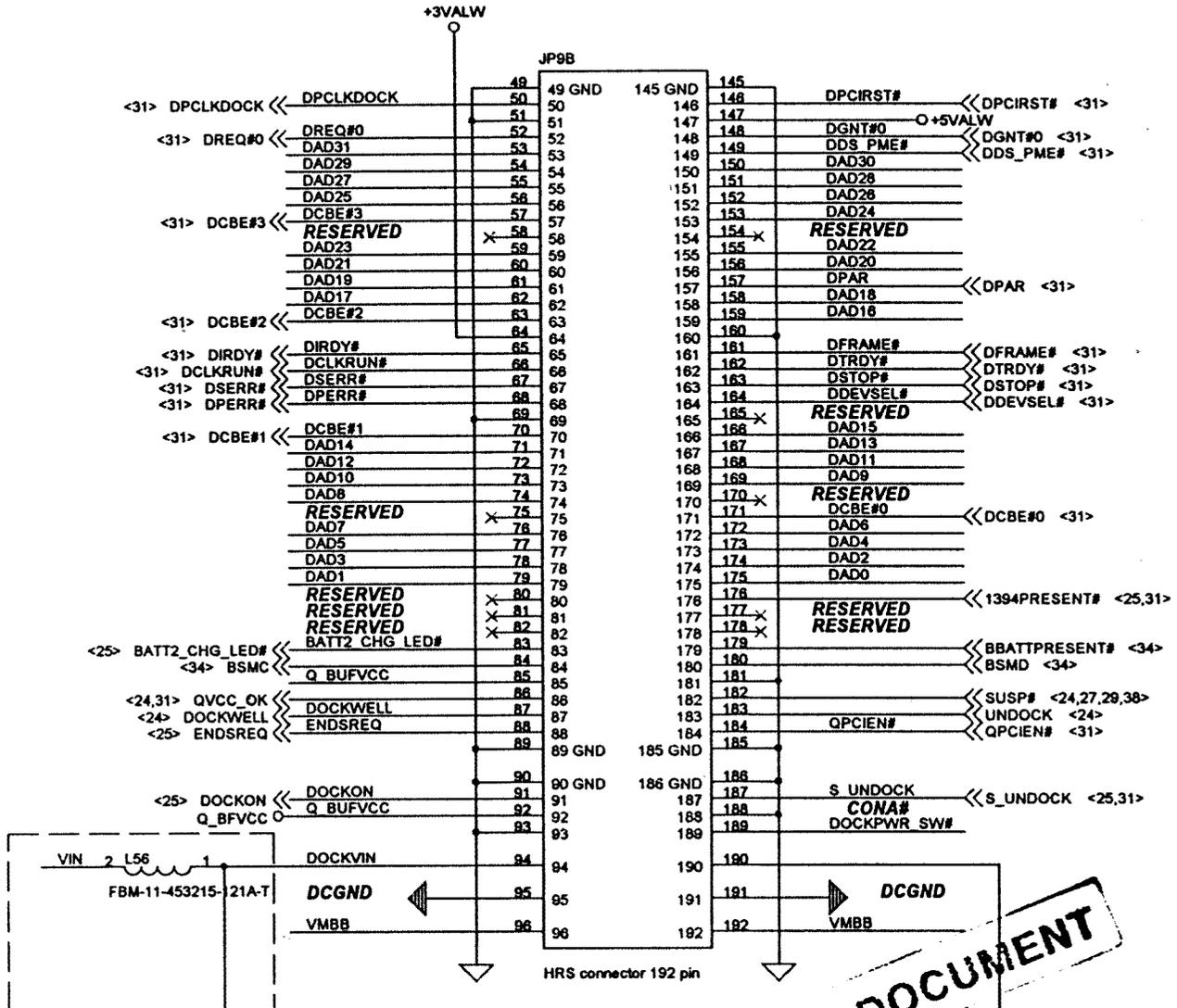
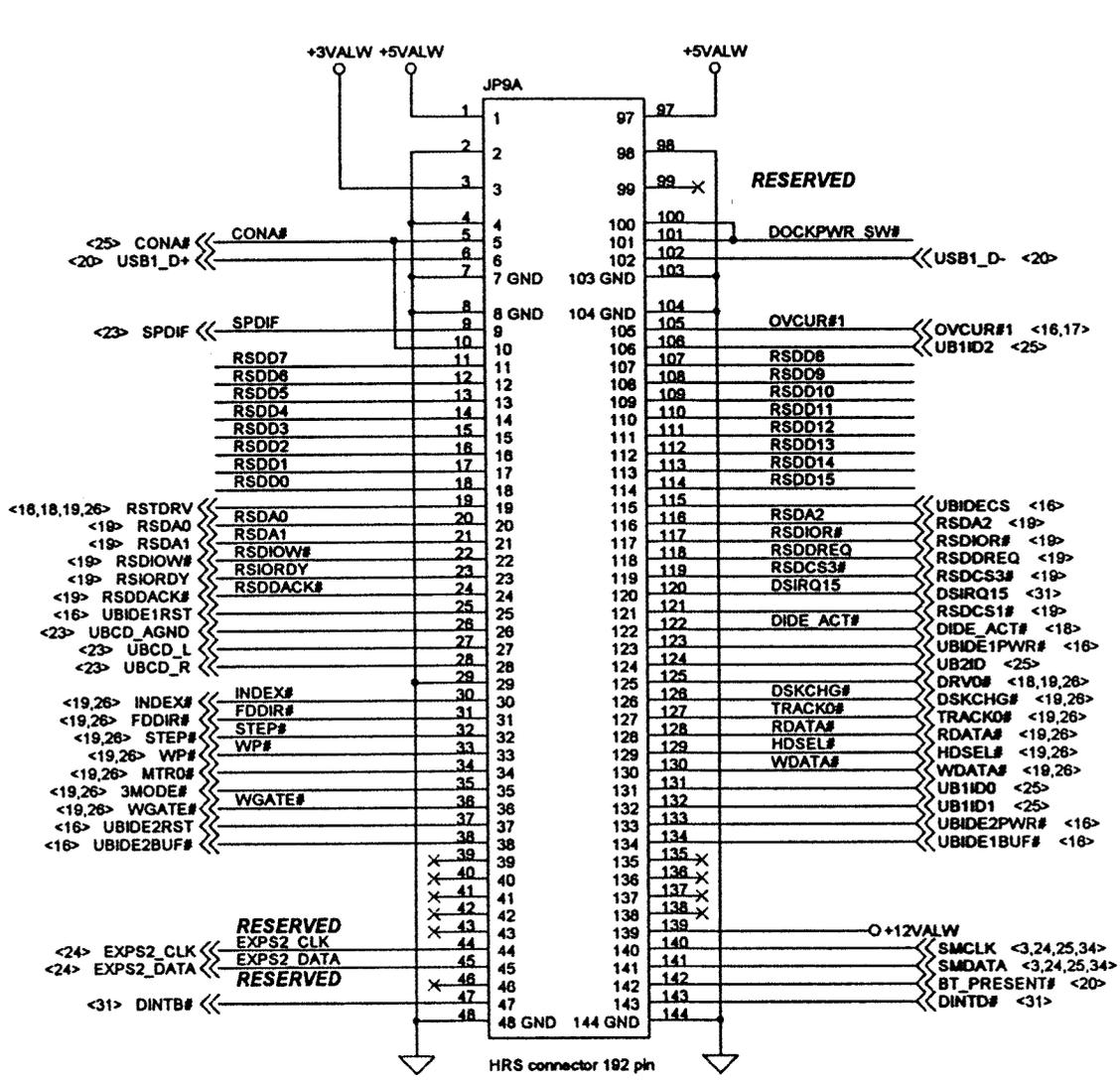
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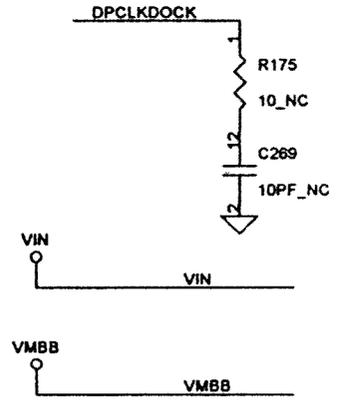
# DOCKING 192 PIN

\*NOTE 1: ONLY FOR PLUG TYPE CONNECTOR:  
 A. EFFECTIVE MATING OF CONTACT NO.5, 92, 101, 188, SHALL BE 0.6mm MIN.  
 B. EFFECTIVE MATING OF CONTACT NO.2, 4, 93, 95, 98, 100, 189, 191 SHALL BE 1.3mm MIN.  
 C. EFFECTIVE MATING OF OTHER CONTACT SHALL BE 0.8mm MIN.

\*NOTE 2: RECEIVE TYPE CONNECTOR FOR M/B. PLUG TYPE FOR ULTRA BAY USE.



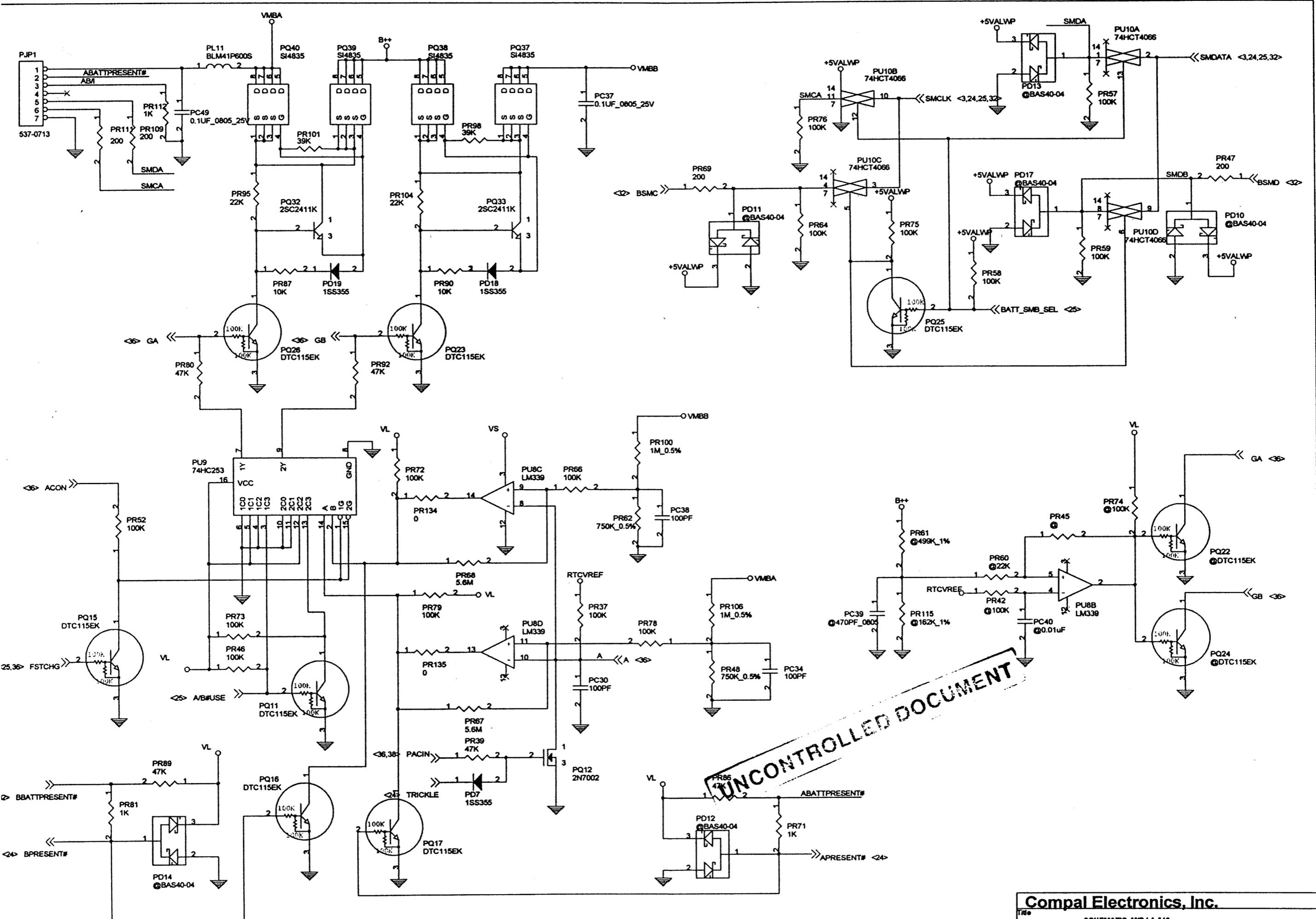
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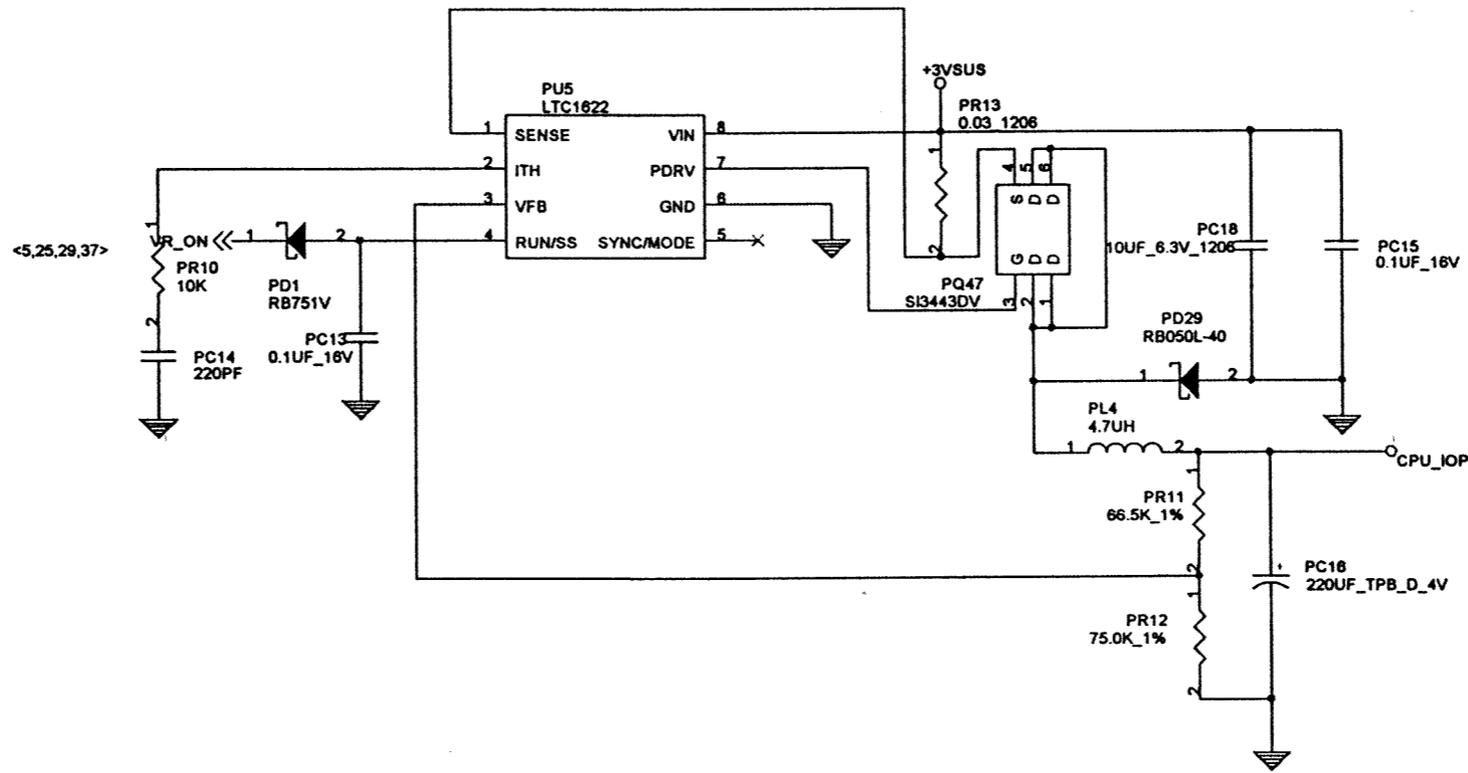


<31> DAD[0..31] << DAD[0..31]  
 <19> RSDD[0..15] << RSDD[0..15]

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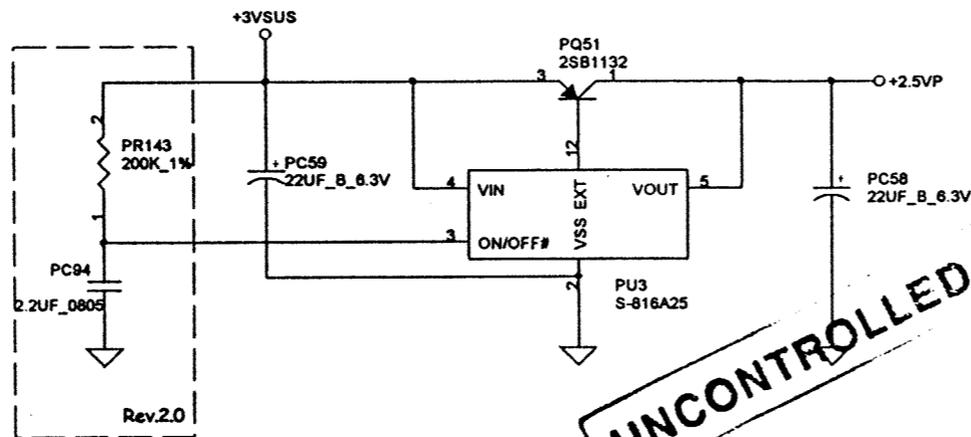




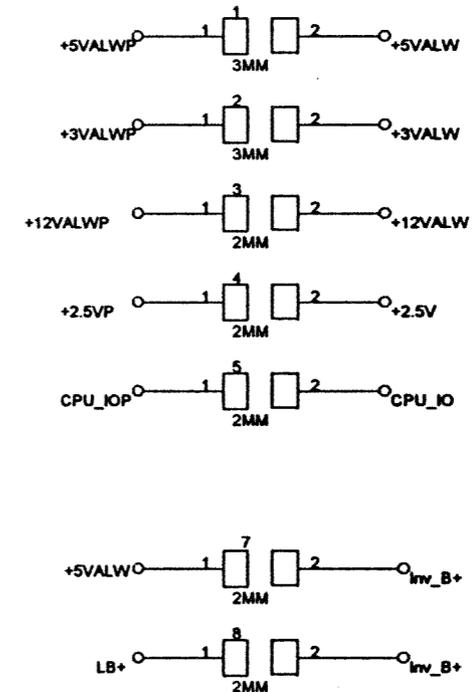
\*Note: +2.5V FOR VGA  
CPU\_IOP : +1.5V

For ATI suggestion: +3V and +2.5V power sequence

PR143: 200Kohm (SD014200305)  
PC94: 2.2uF (SE049225Z08)



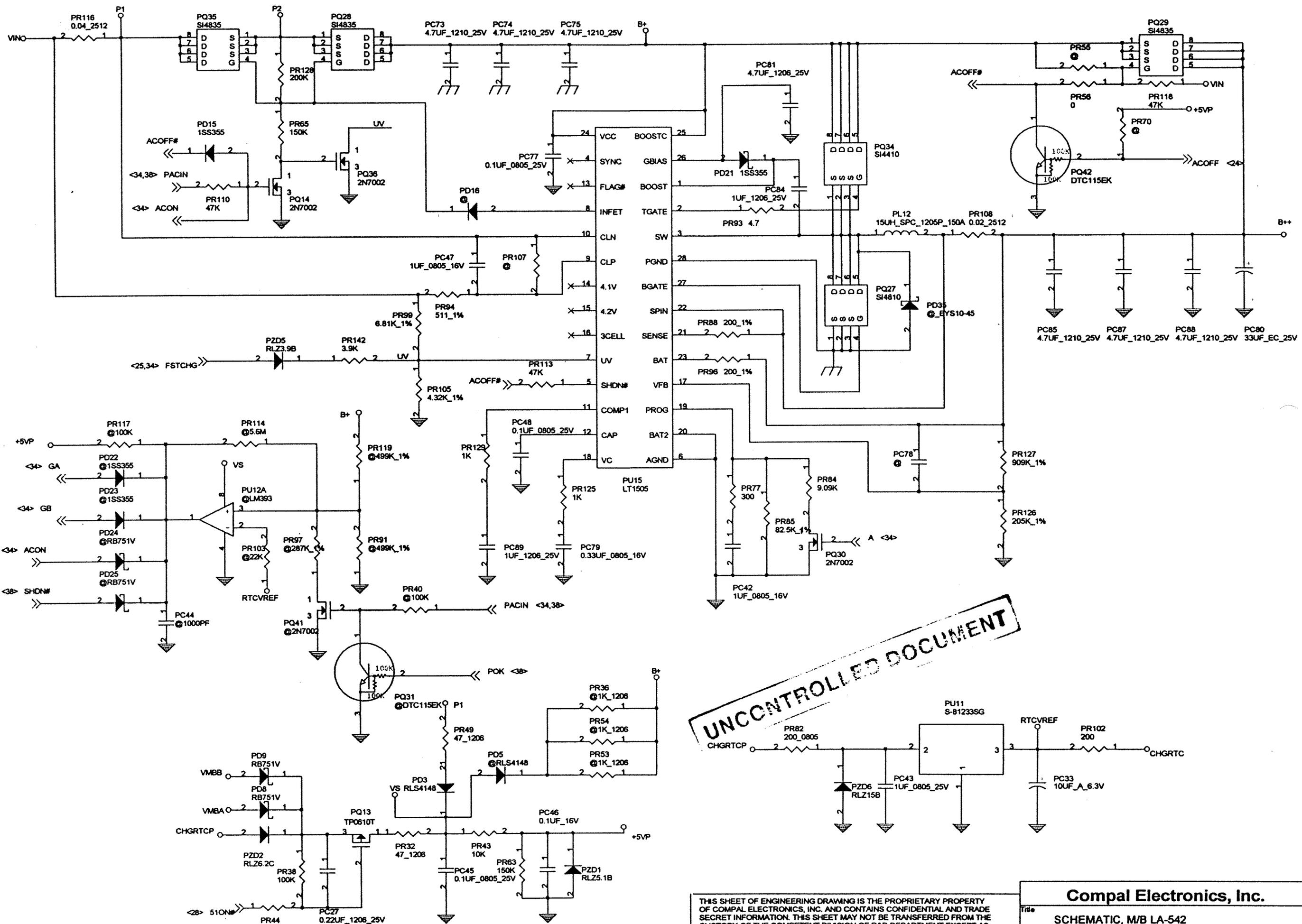
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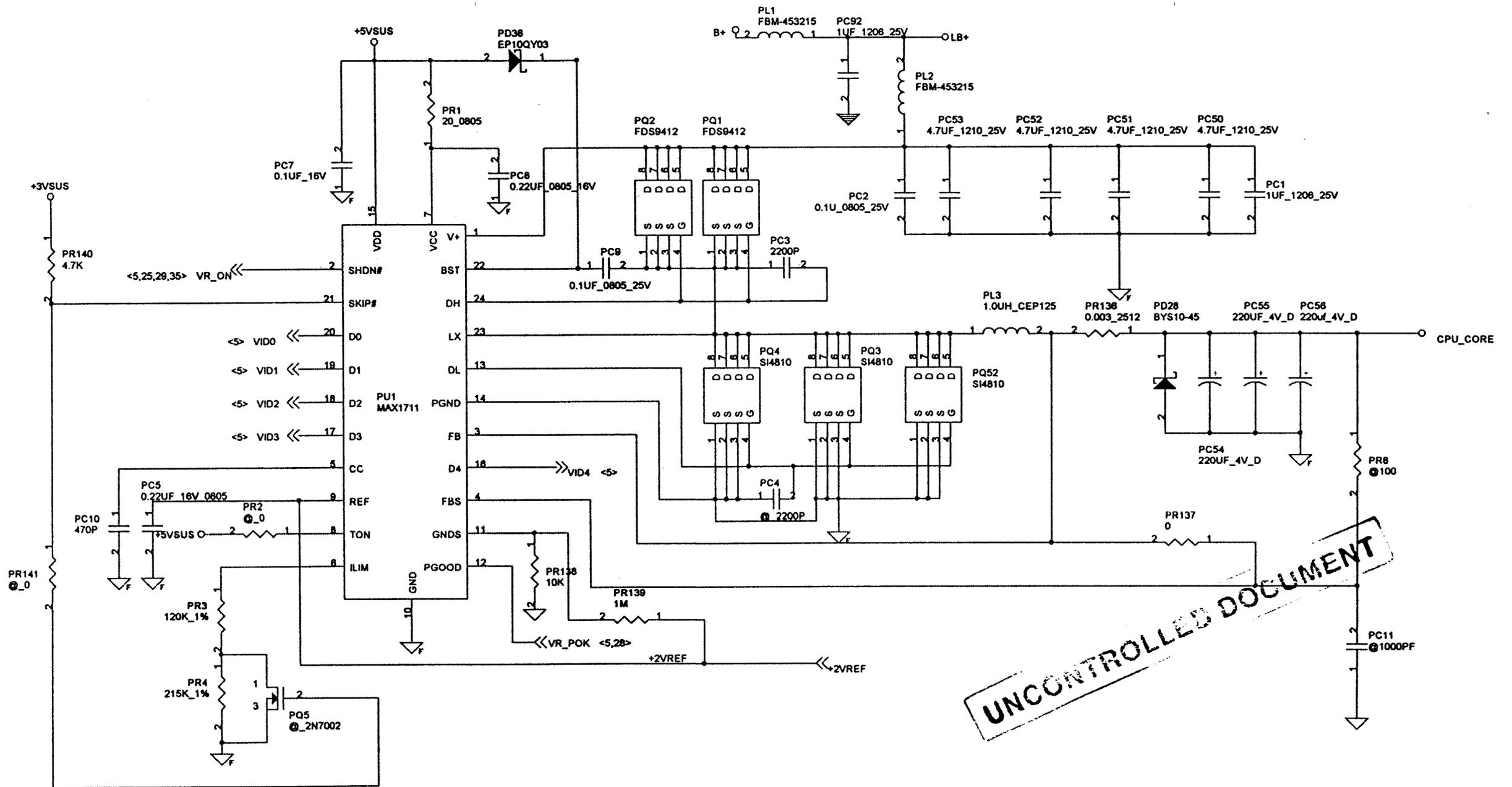


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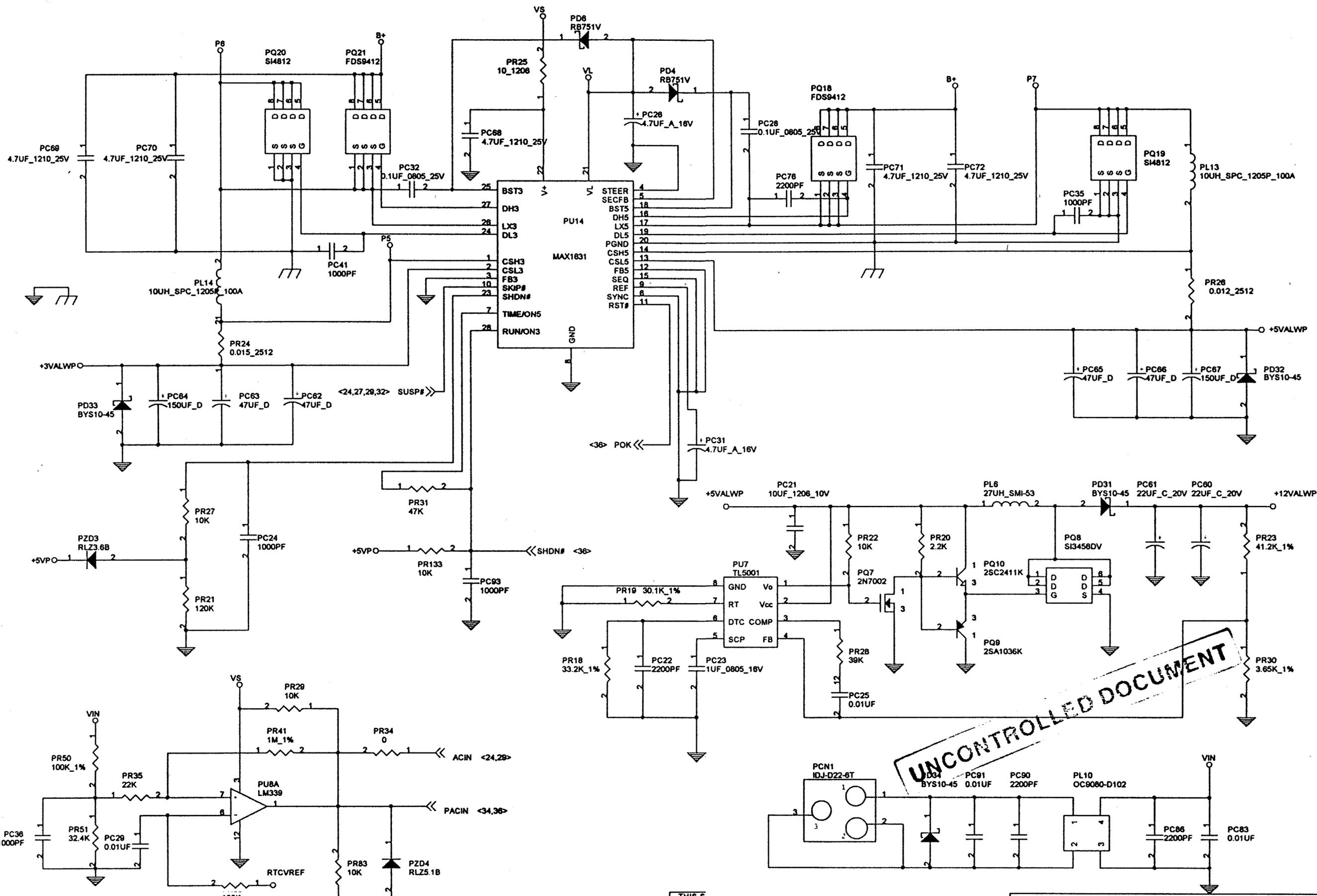
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