

# Compal confidential

## Schematics Document

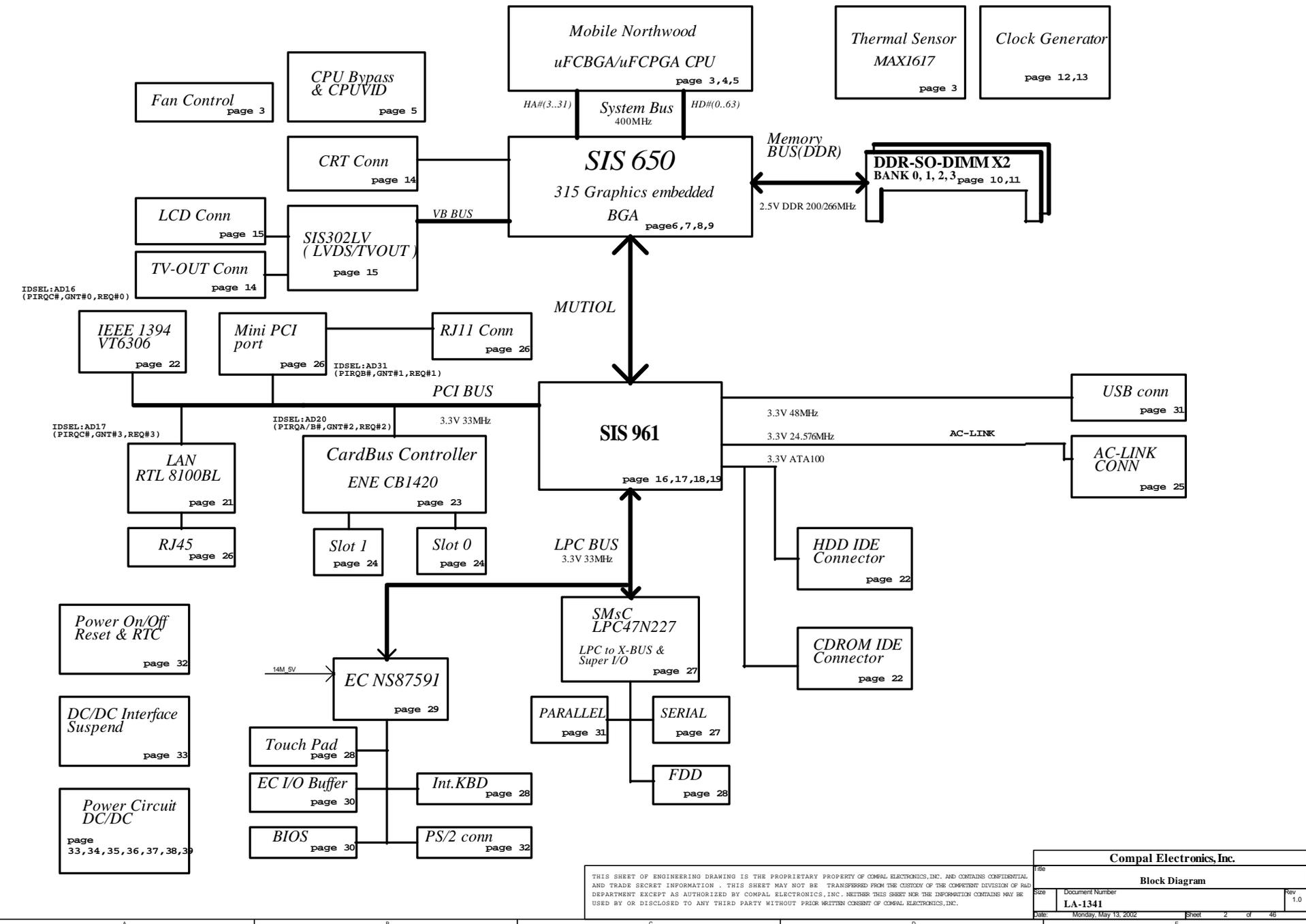
**Mobile P4 uFCBGA/uFCPGA with SIS 650/961 core logic chip**

**2002-05-03**

**REV:1.0**

<b>Compal Electronics, Inc.</b>			
Title			
<b>Cover Sheet</b>			
Size	Document Number	Rev	
	<b>LA-1341</b>	1.0	
Date:	Monday, May 13, 2002	Sheet	1 of 46

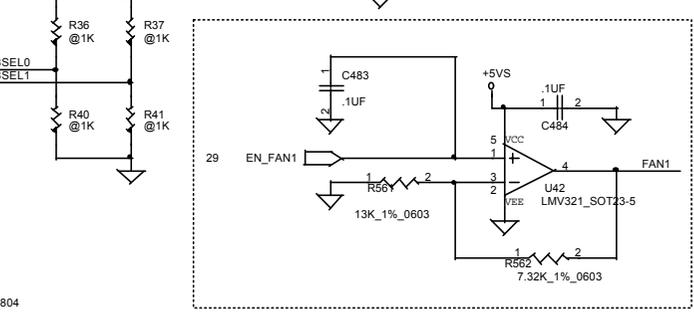
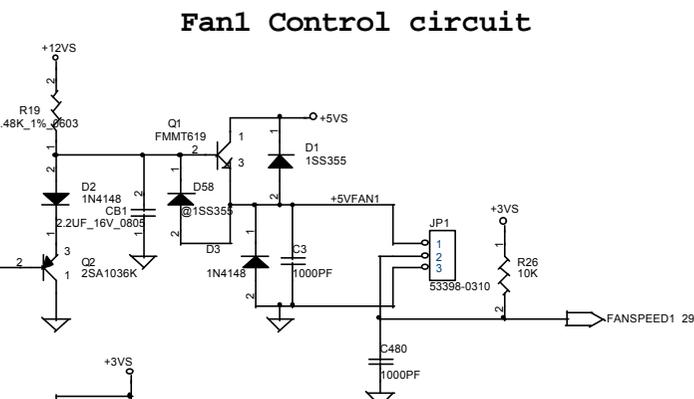
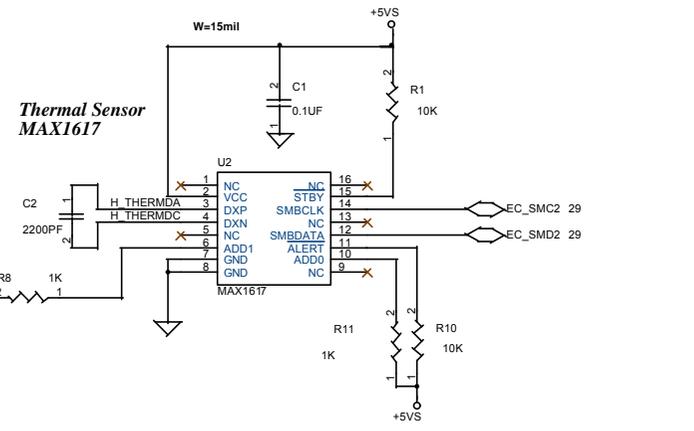
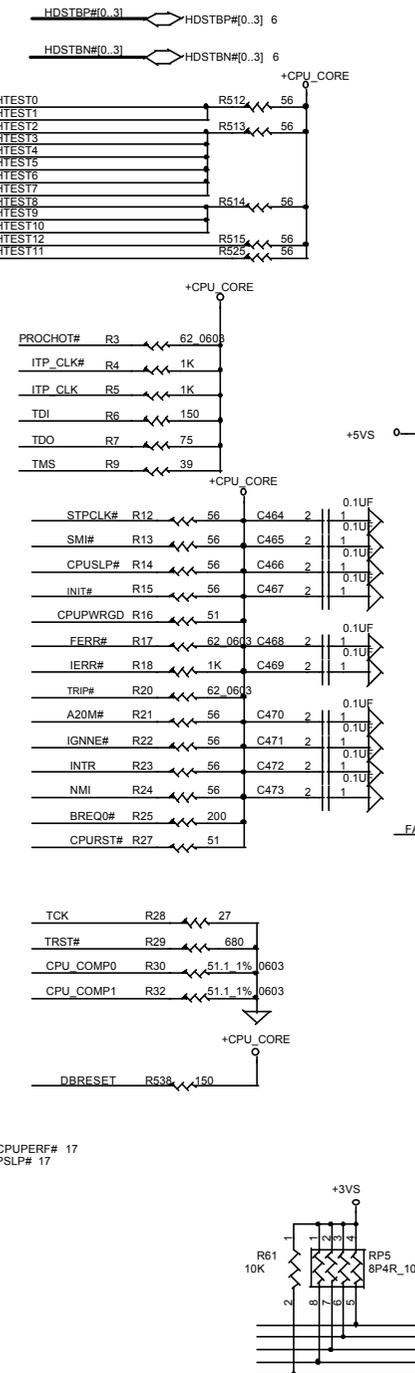
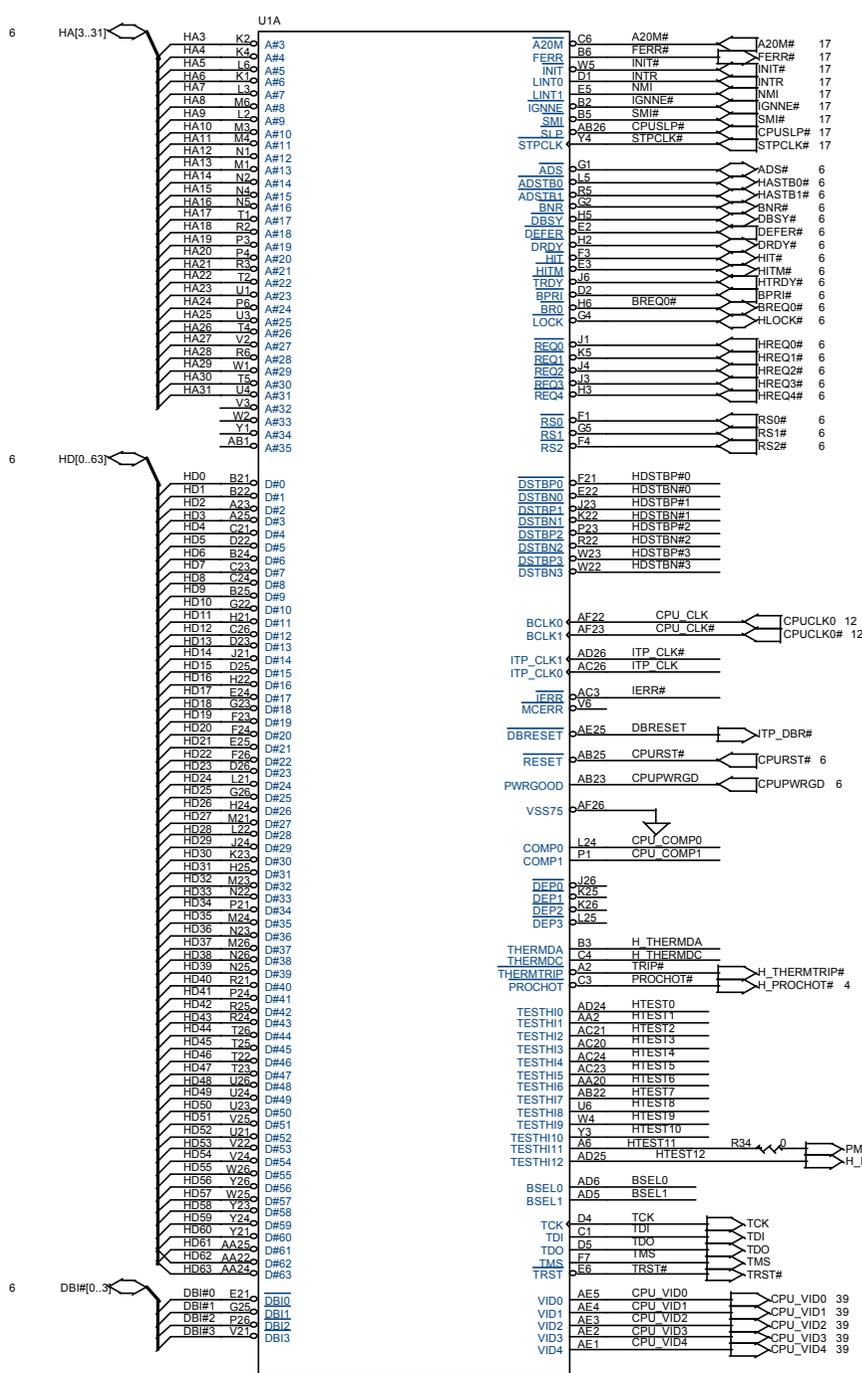
File Name : LA-1341



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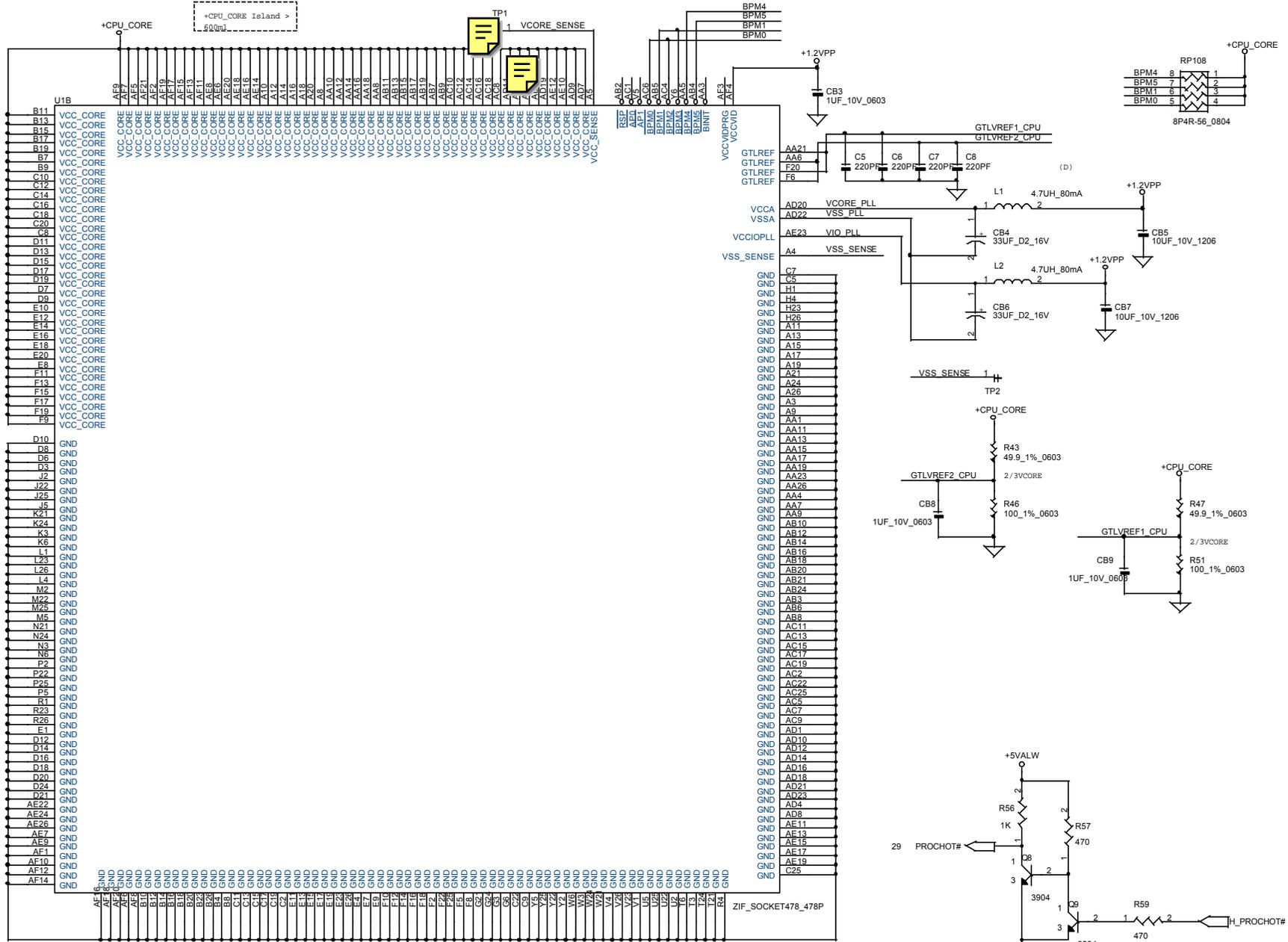
Compal Electronics, Inc.		
Block Diagram		
File	Document Number	Rev
	LA-1341	1.0
Date	Monday, May 13, 2002	
	Sheet	2 of 46

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<b>Compal Electronics, Inc.</b>			
Title: <b>MobilP4-Host I/2</b>			
Size: <b>LA-1341</b>	Document Number:	Rev: <b>1.0</b>	
Date: <b>Monday, May 13, 2002</b>	Sheet: <b>3</b>	of <b>46</b>	

ZIF\_SOCKET478\_478P



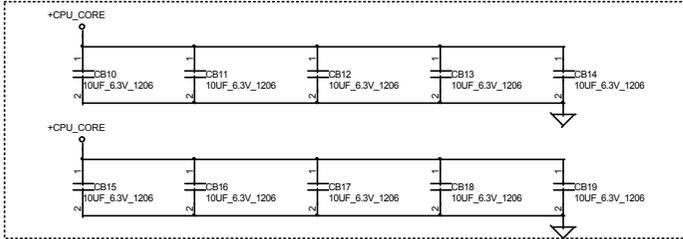
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<b>Compal Electronics, Inc.</b>		
Title	<b>Mobil P4 - Power &amp; Ground 22</b>	
Size	Document Number	Rev
	<b>LA-1341</b>	1.0
Date:	Monday, May 13, 2002	Sheet 4 of 46

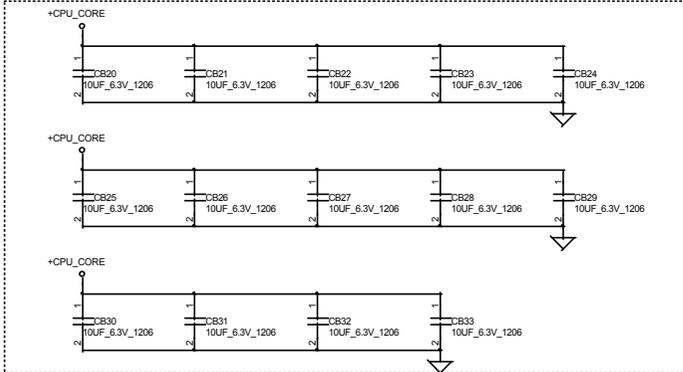
**Layout note :**

Place close to CPU. Use 2-3 vias per PAD.  
Place .22uF caps underneath balls on solder side.  
Place 10uF caps on the peripheral near balls.  
Use 2-3 vias per PAD.

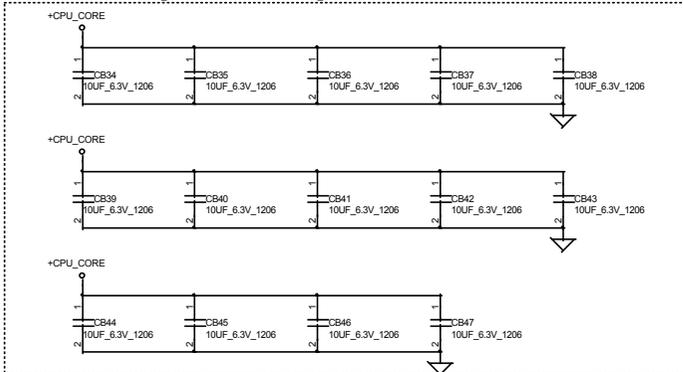
**Please place these cap in the socket cavity area**



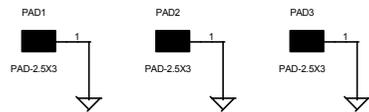
**Please place these cap on the socket north side**



**Please place these cap on the socket south side**

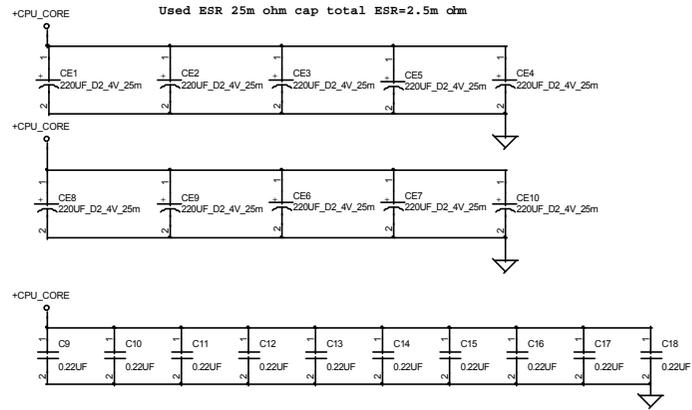


**EMI Clip PAD for CPU**



**Layout note :**

Place close to CPU power and ground pin as possible (<1inch)

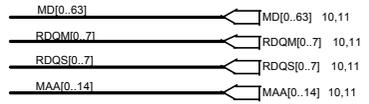


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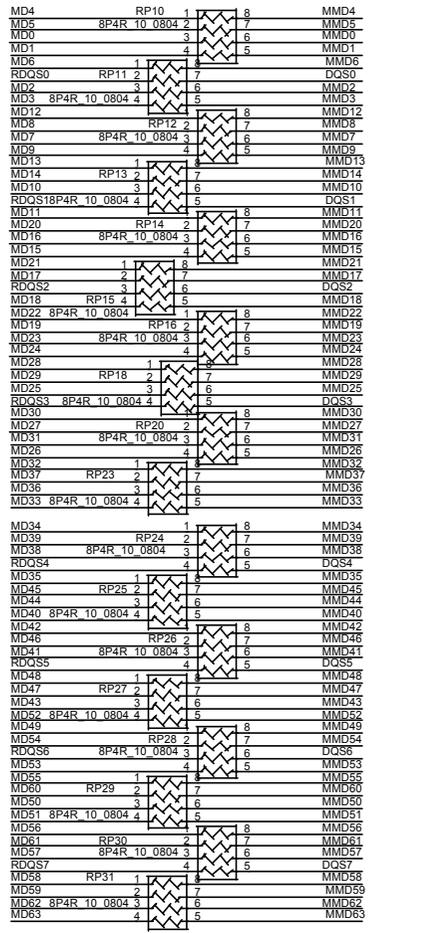
<b>Compal Electronics, Inc.</b>			
<b>CPU Bypass Cap.</b>			
File	Document Number	Size	Rev
	<b>LA-1341</b>		1.0
Date	Monday, May 13, 2002	Sheet	5 of 46



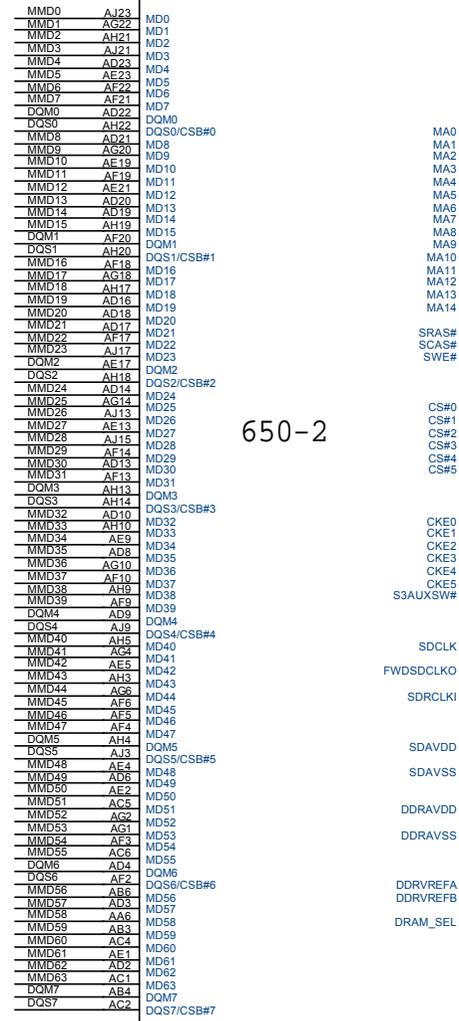
NOTE: This page is for pure DDR SDRAM PCB design



RP\* PLACE CLOSE TO DIMM

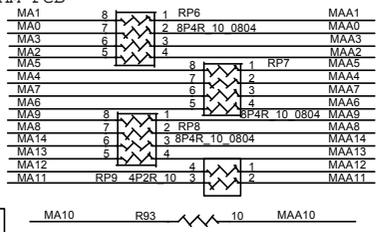
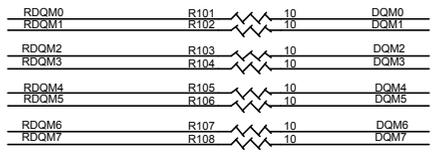


USB

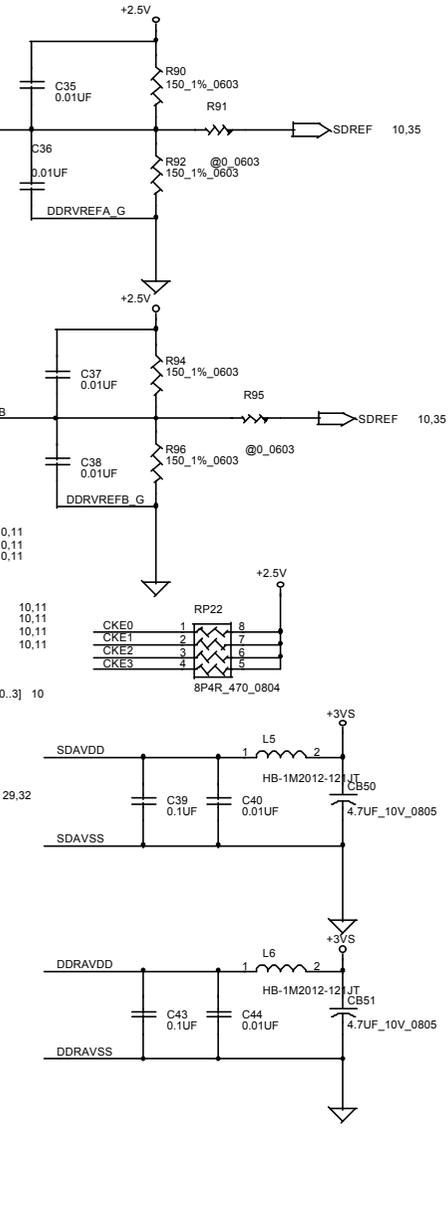
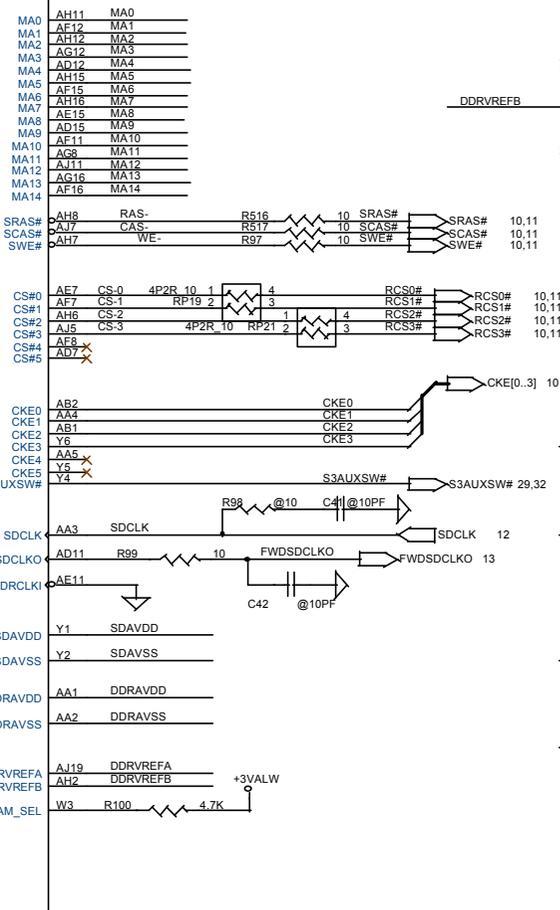


650-2

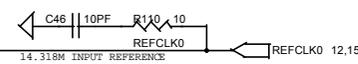
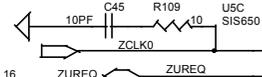
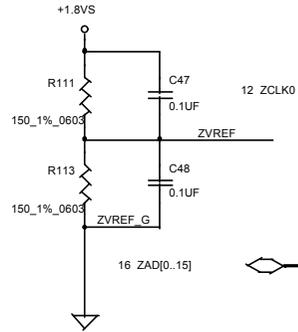
SIS650



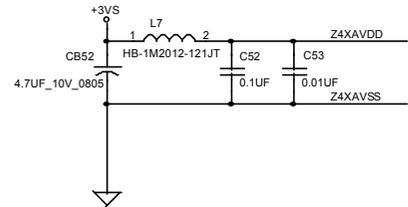
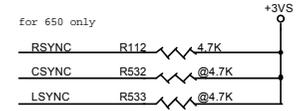
RP\* place close to DIMM1



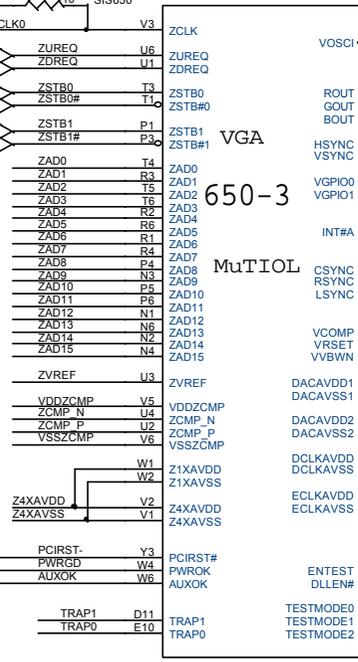
16 ZSTB[0..1] ZSTB[0..1]  
 16 ZSTB[0..1]# ZSTB[0..1]#



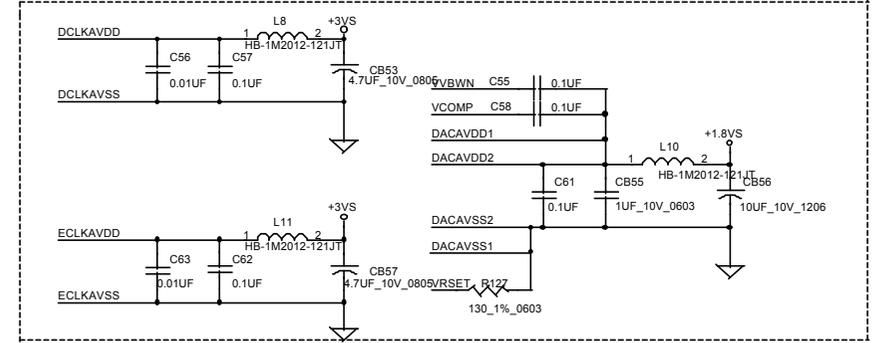
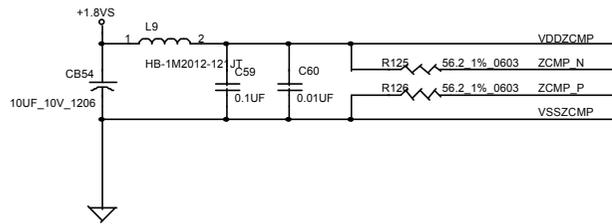
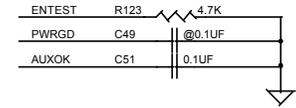
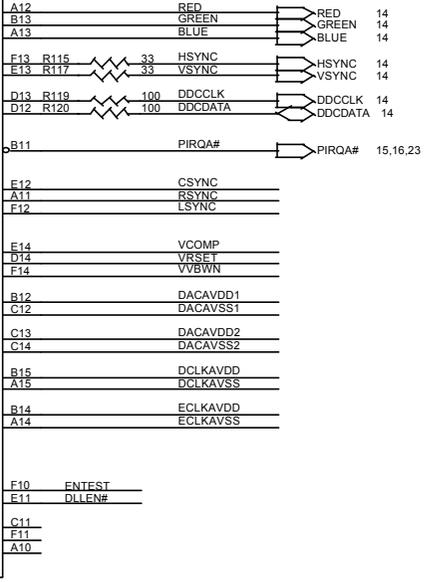
for 650 only



16,20,29 PCIRST-  
 17,32 PWRGD  
 17,29 RSM\_RST



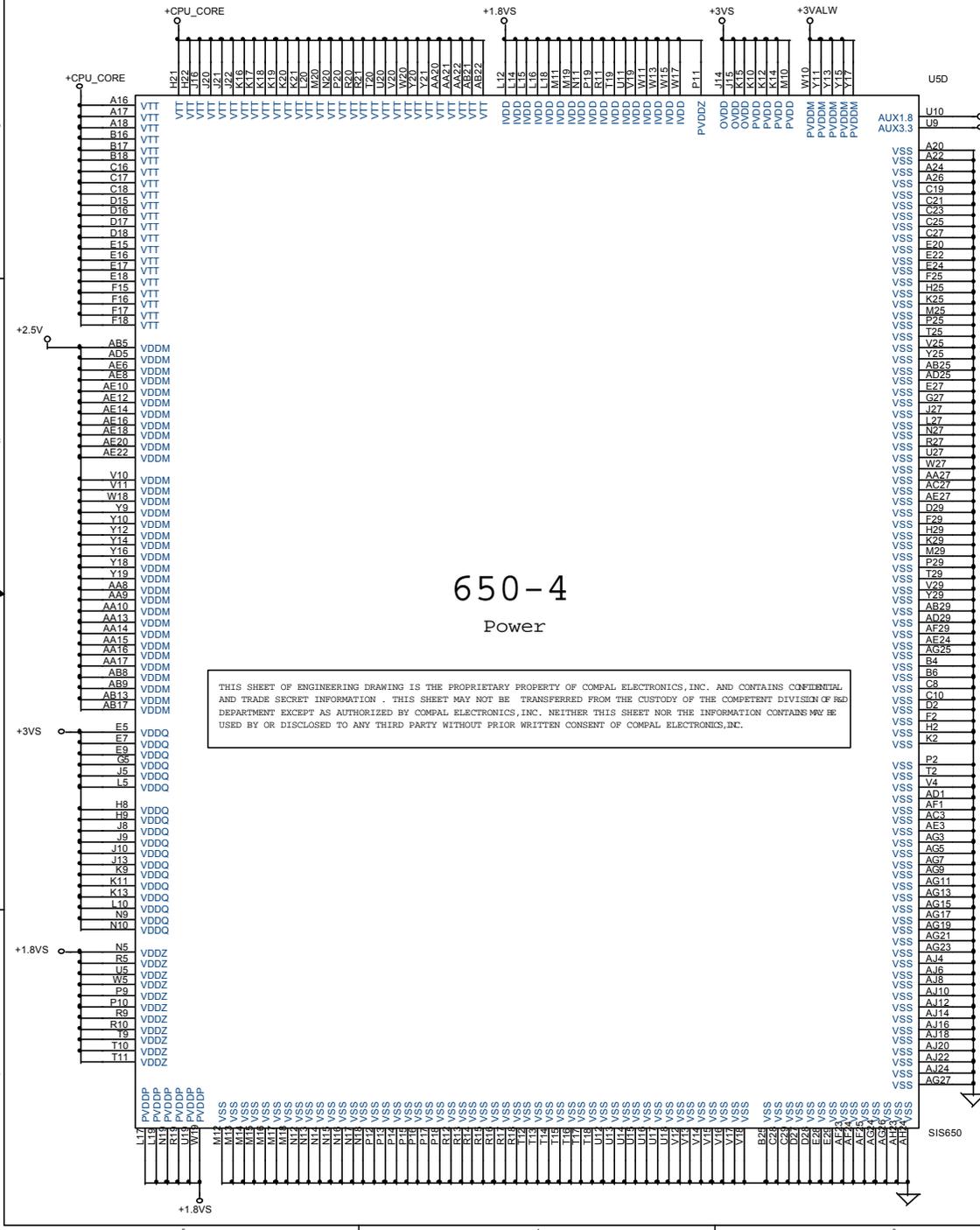
VGA  
 650-3  
 MuTIOL



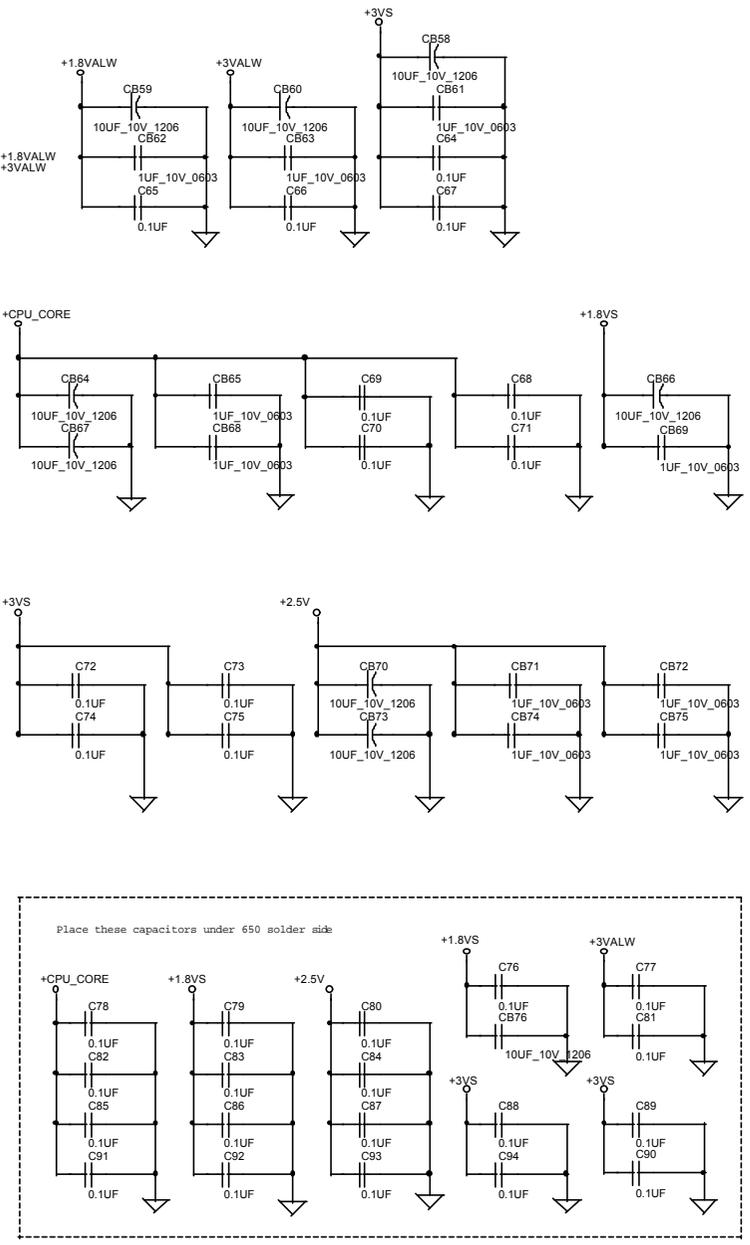
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<b>Compal Electronics, Inc.</b>		
File	<b>SIS650-3HyperZip</b>	
Size	Document Number	Rev
	<b>LA-134I</b>	1.0
Date:	Monday, May 13, 2002	Sheet 8 of 46

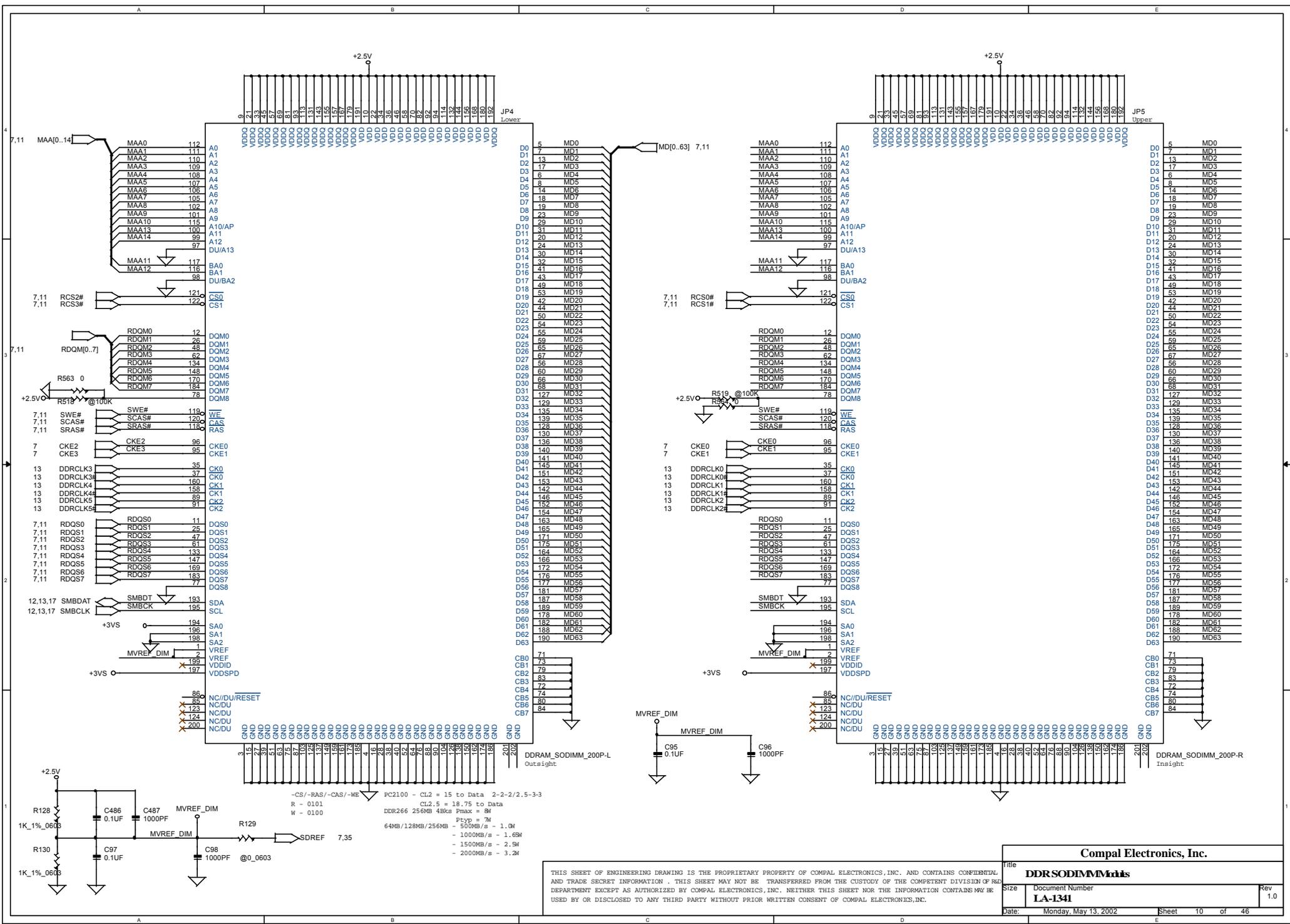
NOTE: This page is for pure DDR SDRAM PCB design:



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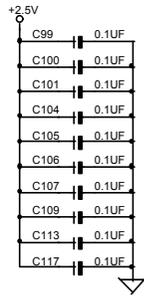
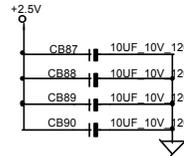
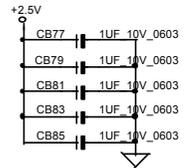
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Size	Document Number	Rev
	<b>LA-1341</b>	1.0
Date:	Monday, May 13, 2002	Sheet 9 of 46



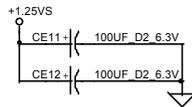
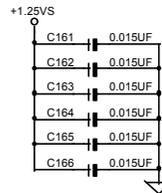
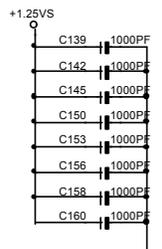
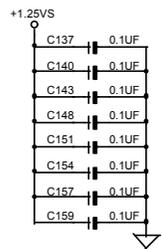
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<b>Compal Electronics, Inc.</b>		
File	<b>DDR SODIMM 128MB</b>	
Size	Document Number	Rev
	<b>LA-1341</b>	1.0
Date:	Monday, May 13, 2002	Sheet 10 of 46

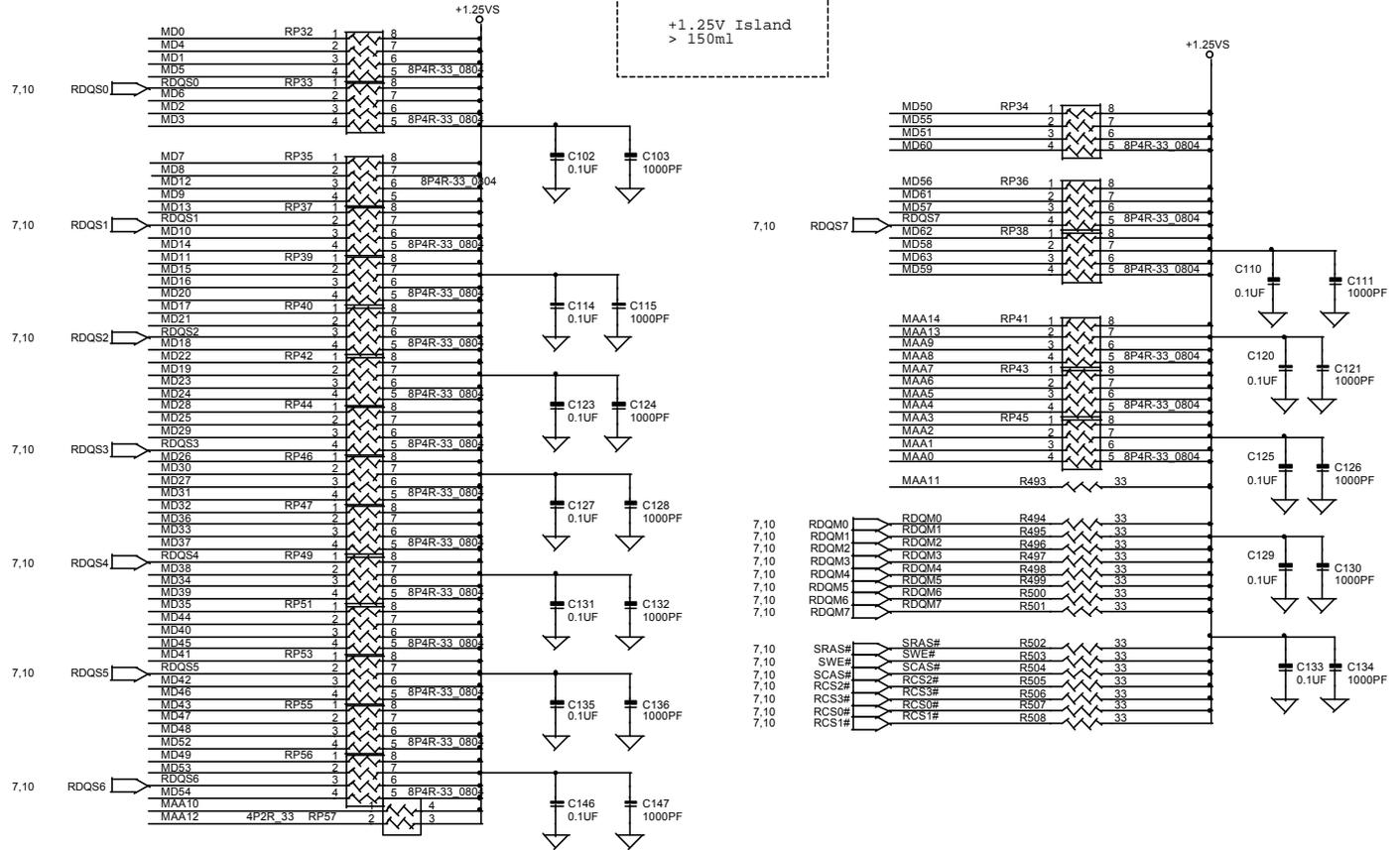
Decoupling capacitors  
(Place near DDR SODIMM)



Place these decoupling capacitors close to VTT\_MEM termination resistors.



Termination Network place closely to DIMM



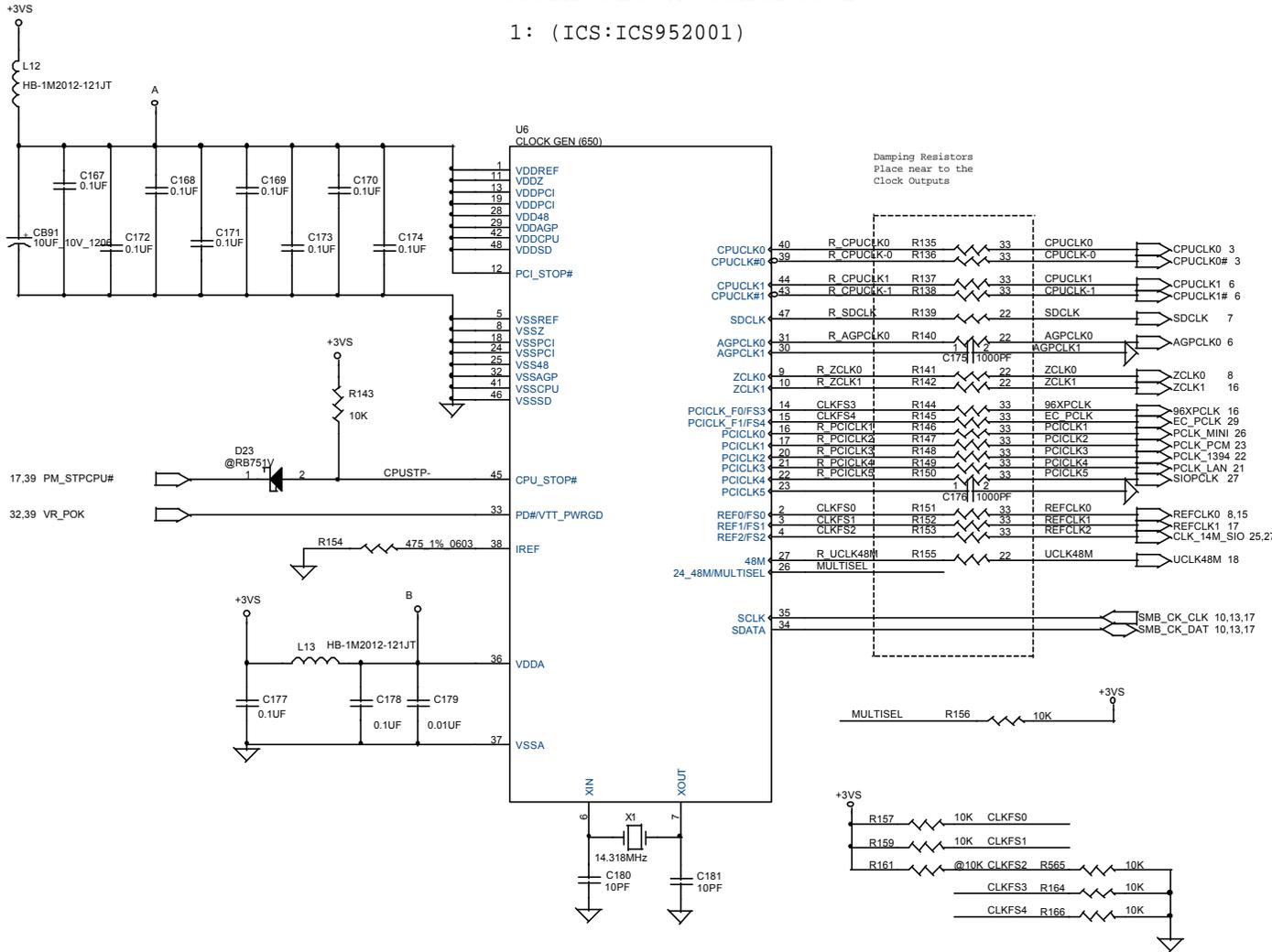
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Title			DDRS DRAM Terminations
Size	Document Number	Rev	
	LA-1341	1.0	
Date:	Monday, May 13, 2002	Sheet	11 of 46

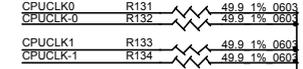
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# Main Clock Generator

1: (ICS:ICS952001)



Place near to the Clock Outputs



FS4	FS3	FS2	FS1	FS0	CPU	DDR	ZCLK	AGP	PCI
1	1	0	0	0	100.0	133.0	80.0	66.7	33.3
1	1	0	0	1	100.0	100.0	80.0	66.7	33.3
* 0	0	1	1	1	100.0	133.3	80.0	66.7	33.3

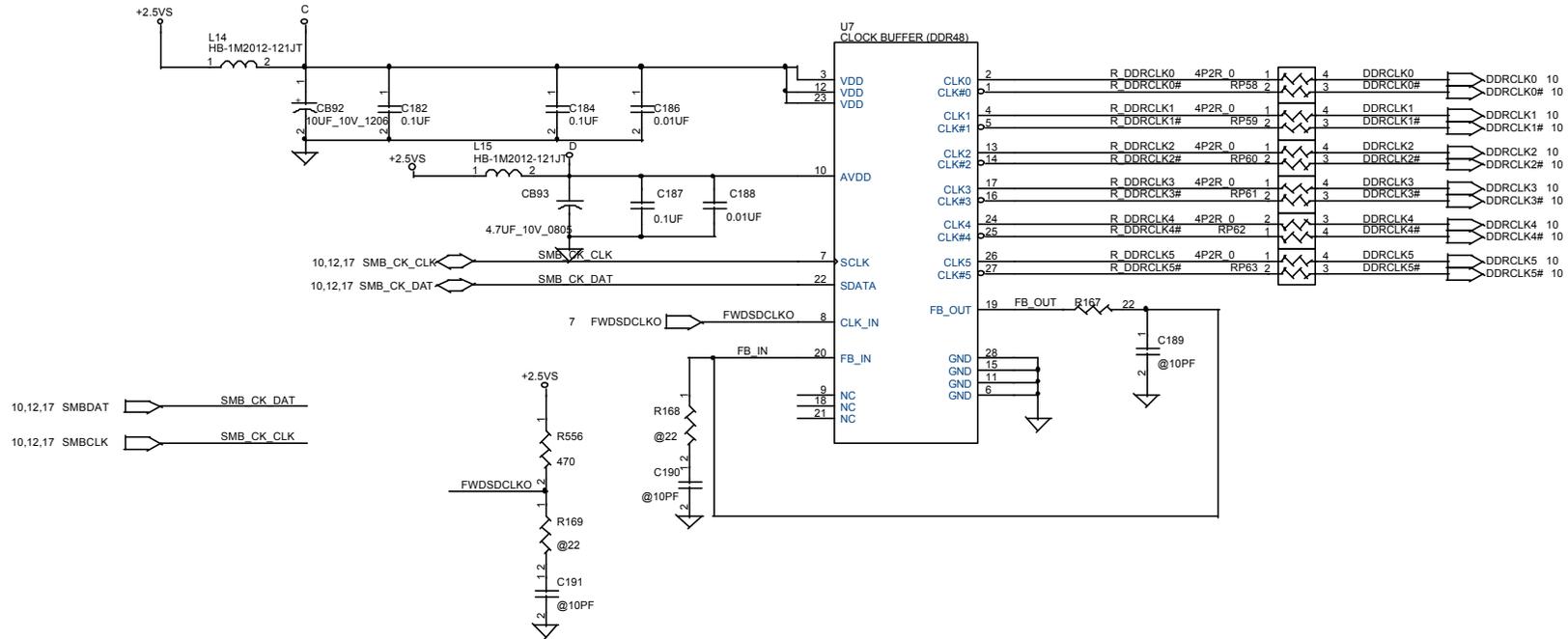
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Title		Clock Generator	
Size	Document Number	Rev	
	<b>LA-134I</b>	1.0	
Date:	Monday, May 13, 2002	Sheet	12 of 46

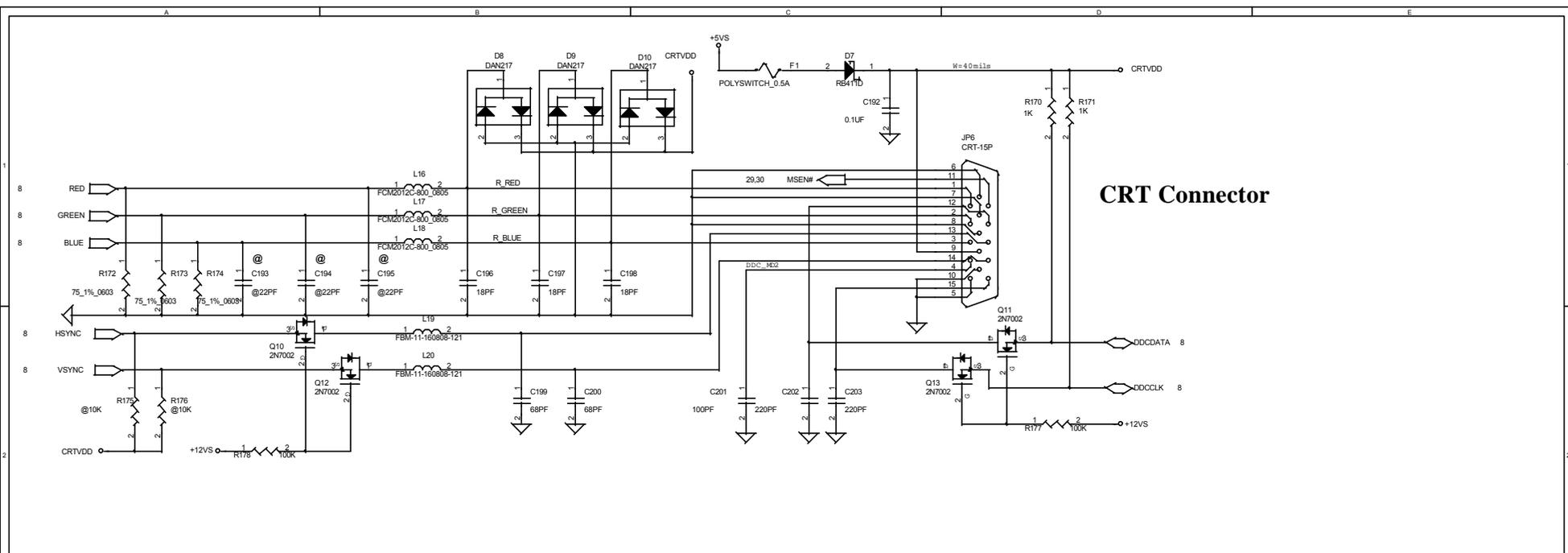
# Clock Buffer (DDR)

1: (ICS: ICS93722)

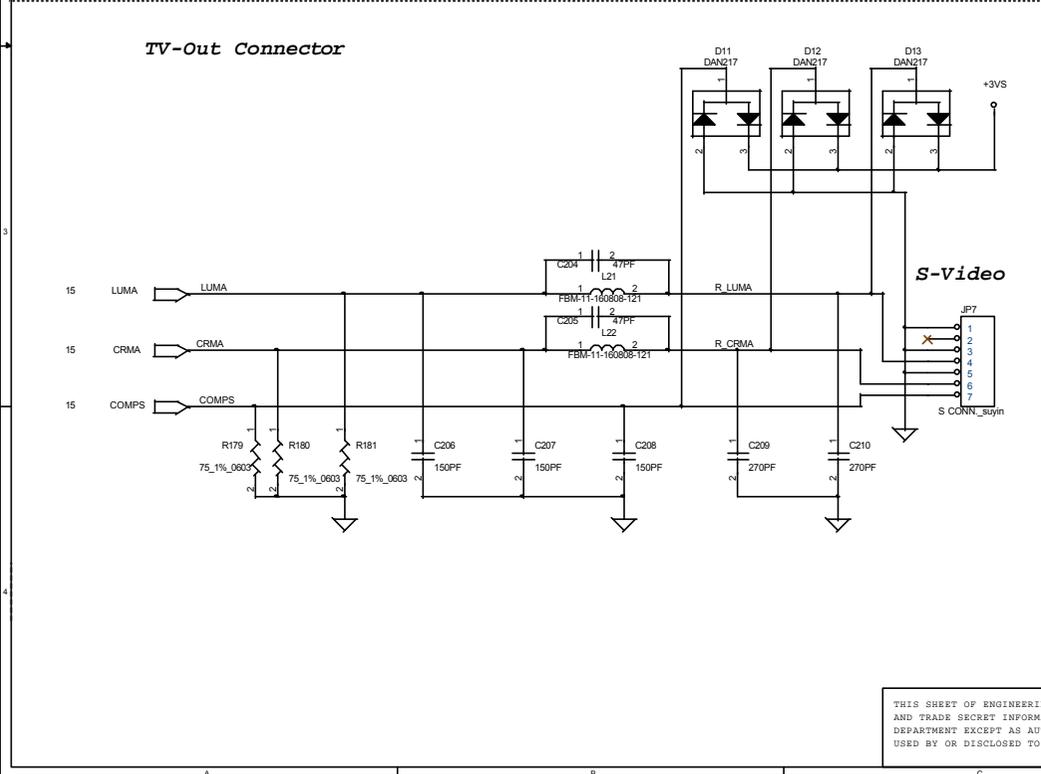


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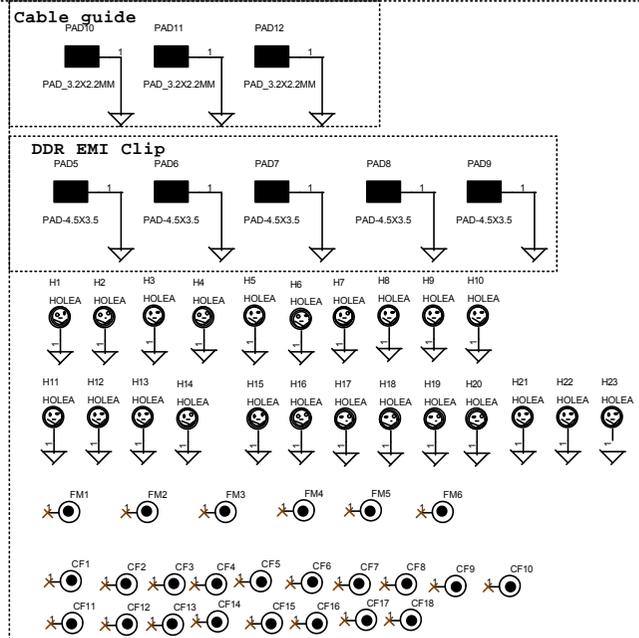
<b>Compal Electronics, Inc.</b>		
Title	<b>DDR Clock Buffer</b>	
Size	Document Number	Rev
	<b>LA-1341</b>	1.0
Date:	Monday, May 13, 2002	Sheet 13 of 46



**CRT Connector**

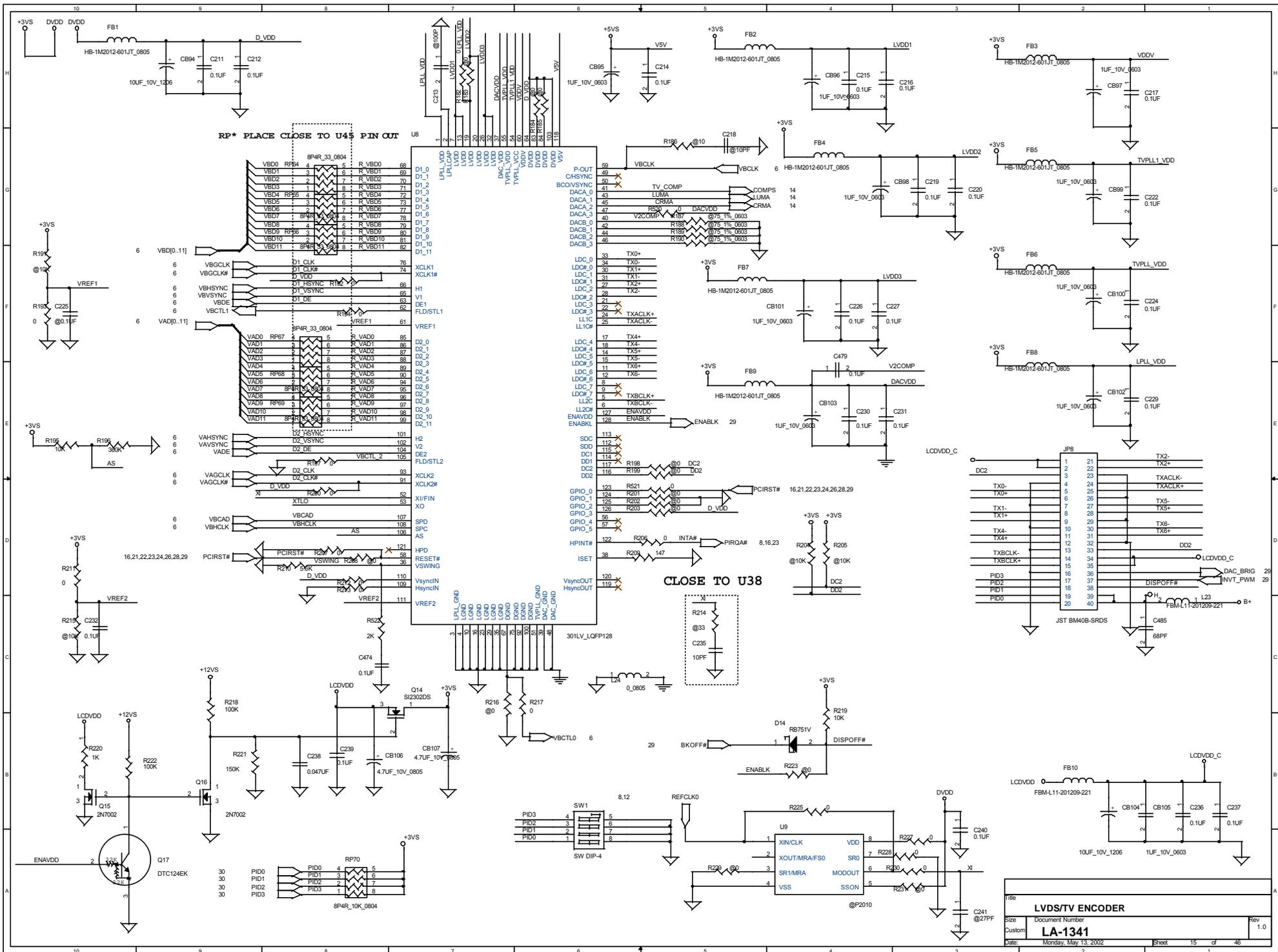


**TV-Out Connector**

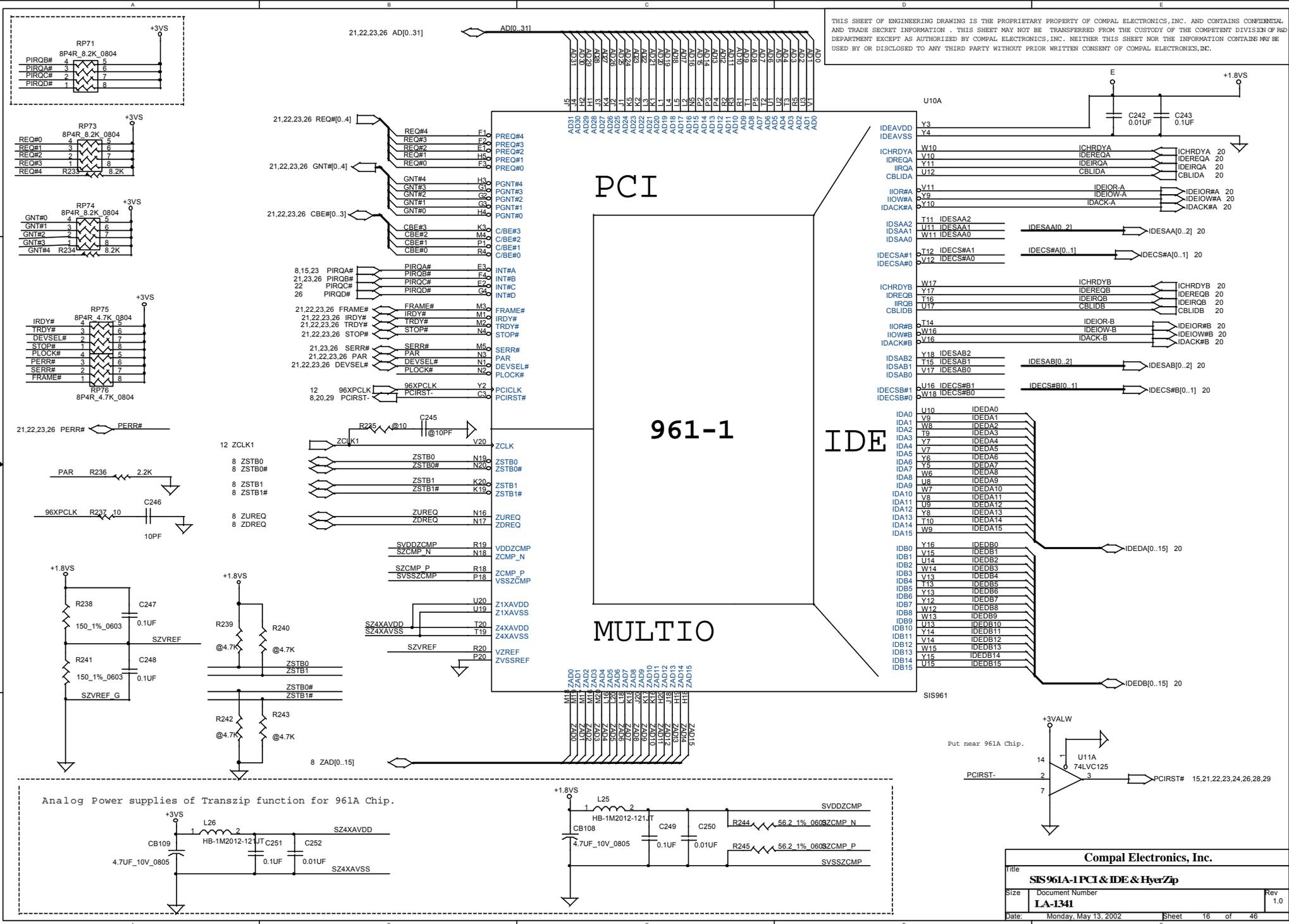


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<b>Compal Electronics, Inc.</b>		
<b>CRT &amp; TVout Connector</b>		
File	Document Number	Rev
	<b>LA-1341</b>	1.0
Date	Monday, May 13, 2002	Sheet 14 of 46

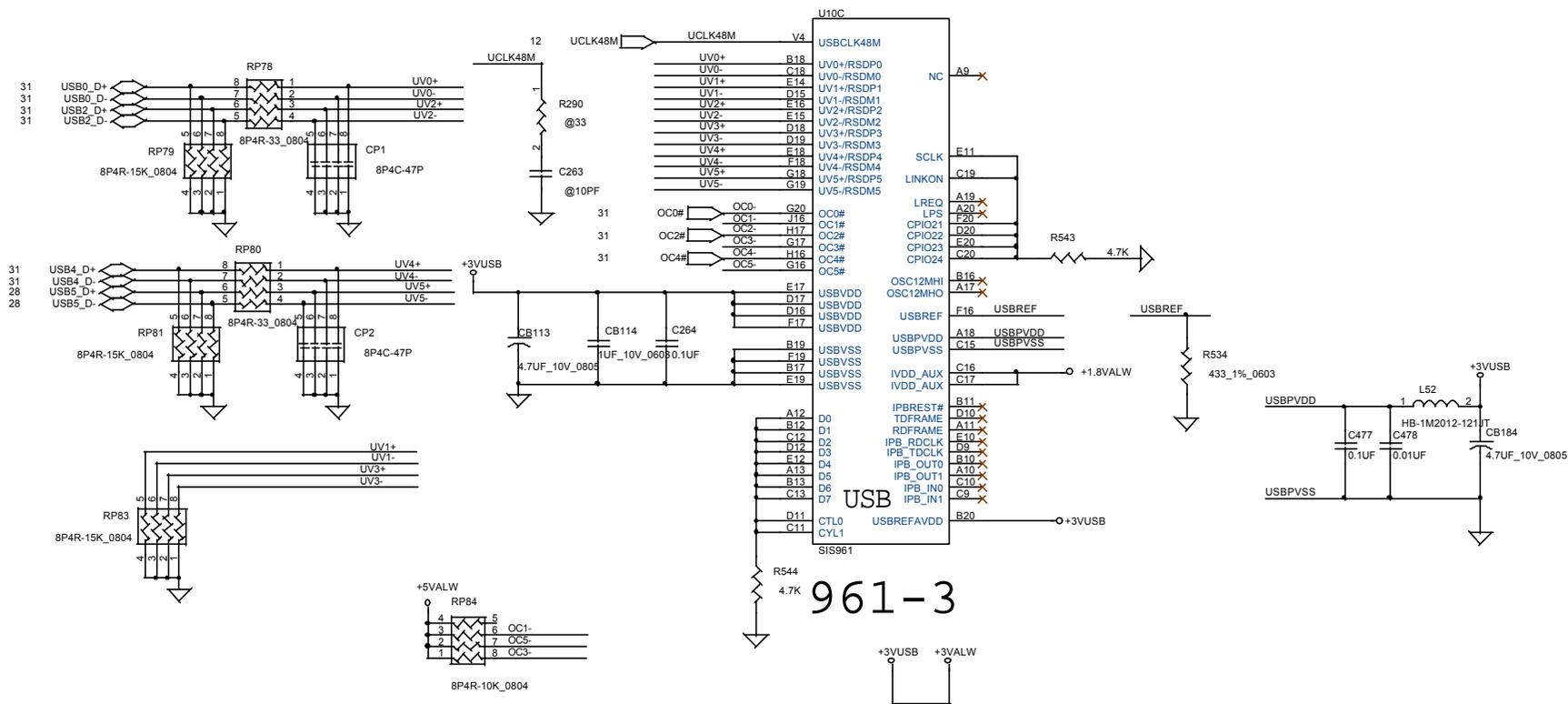


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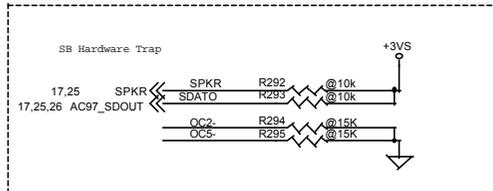


Compal Electronics, Inc.		
Title	SIS961A-1 PCI & IDE & HyperZip	
Size	Document Number	Rev
	LA-1341	1.0
Date:	Monday, May 13, 2002	Sheet 16 of 46





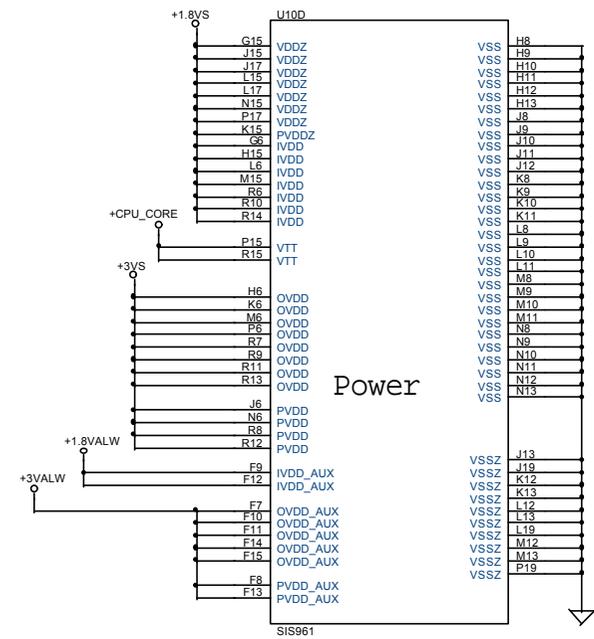
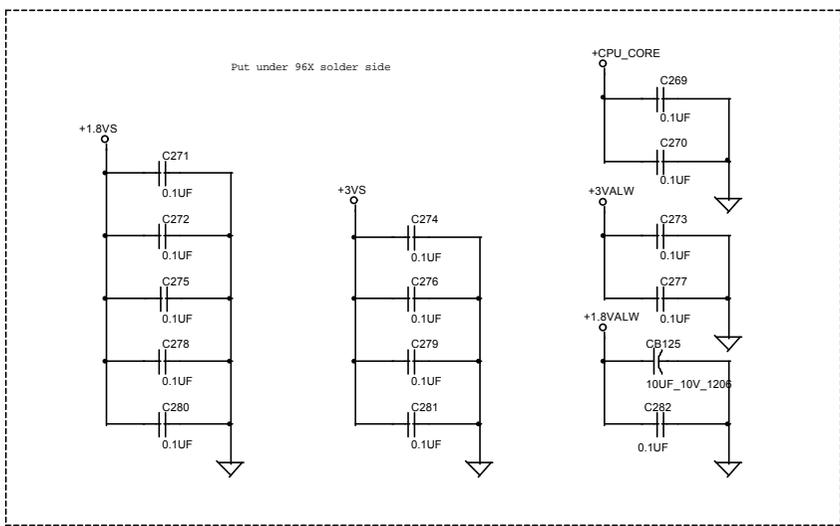
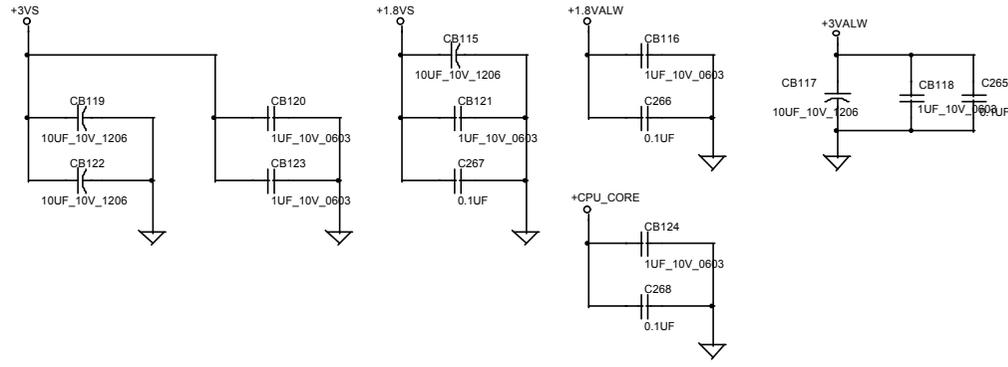
961-3



	0	1	Default
SPKR( LPC addr mapping)	disable	enable	0
SDATO( PCICLK PLL)	enable	disable	0
OC2-( SB debug mode)	enable	disable	1
OC5-( Trap mode)	Ext Ad	RMK	1

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<b>Compal Electronics, Inc.</b>		
Title	SIS961A-3USB	
Size	Document Number	Rev
	LA-1341	1.0
Date	Monday, May 13, 2002	Sheet 18 of 46

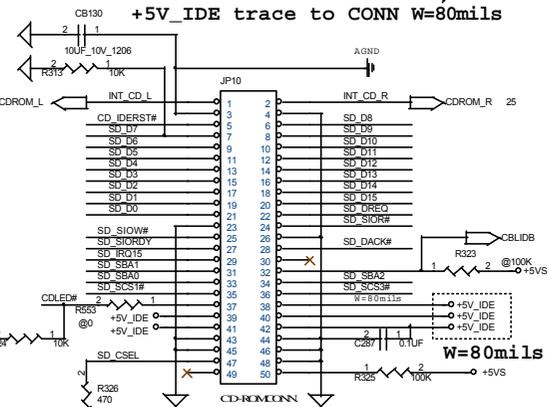
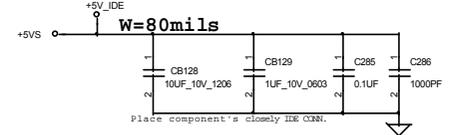
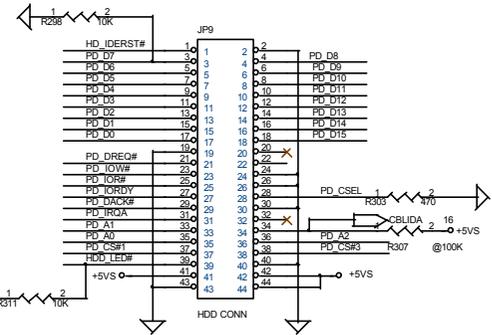
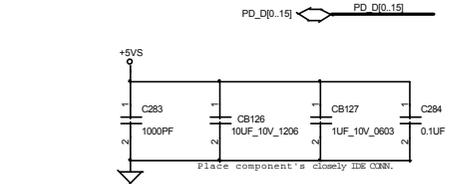
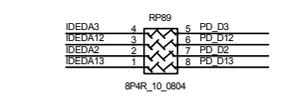
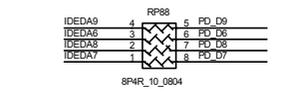
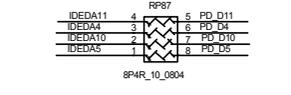
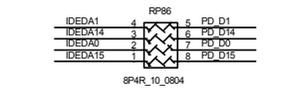
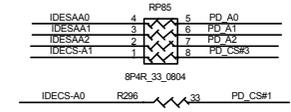
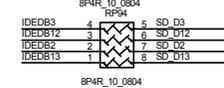
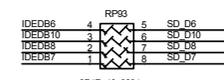
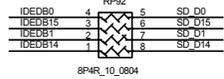
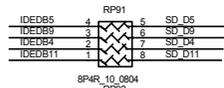
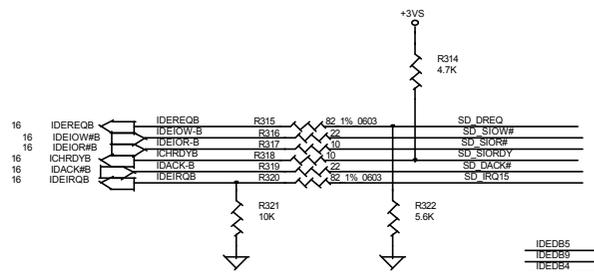
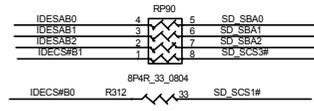
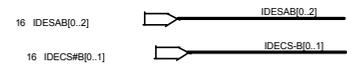
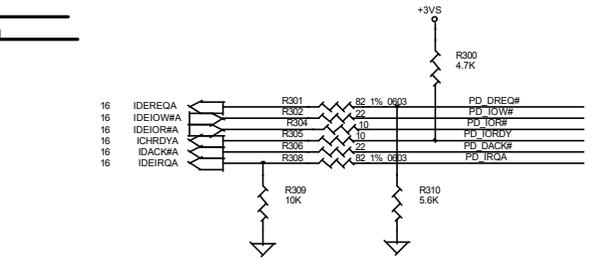
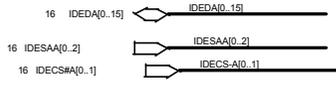
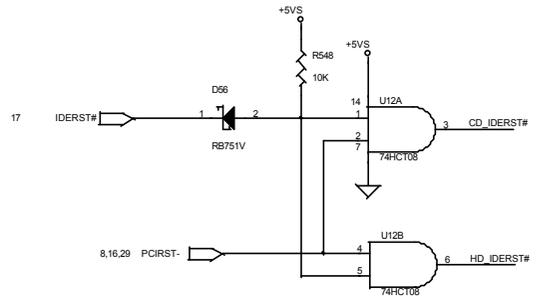


961-4

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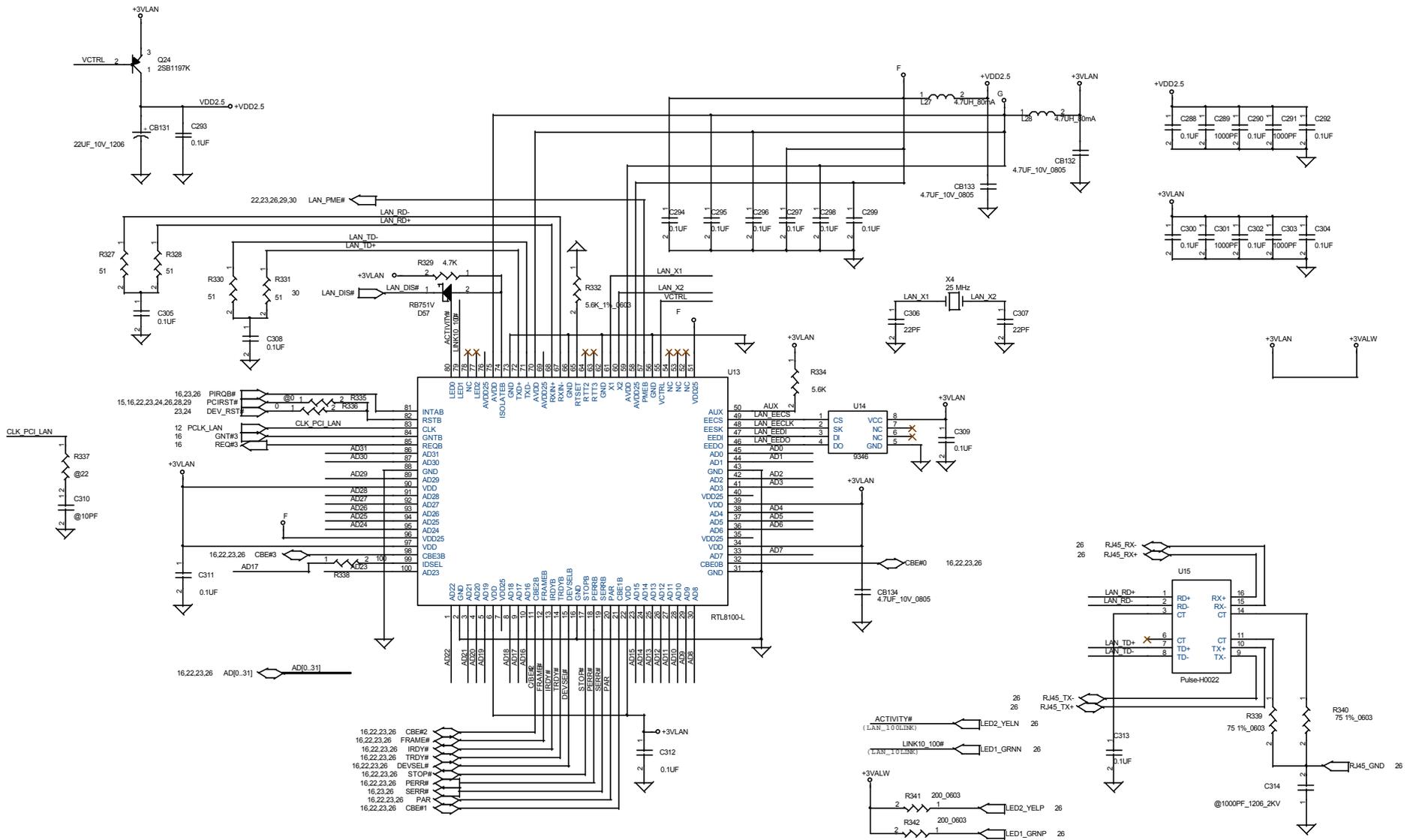
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Title	<b>SIS961A-4Power</b>	
Size	Document Number	Rev
	<b>LA-1341</b>	1.0
Date:	Monday, May 13, 2002	Sheet 19 of 46

# HDD/CD-ROM Module



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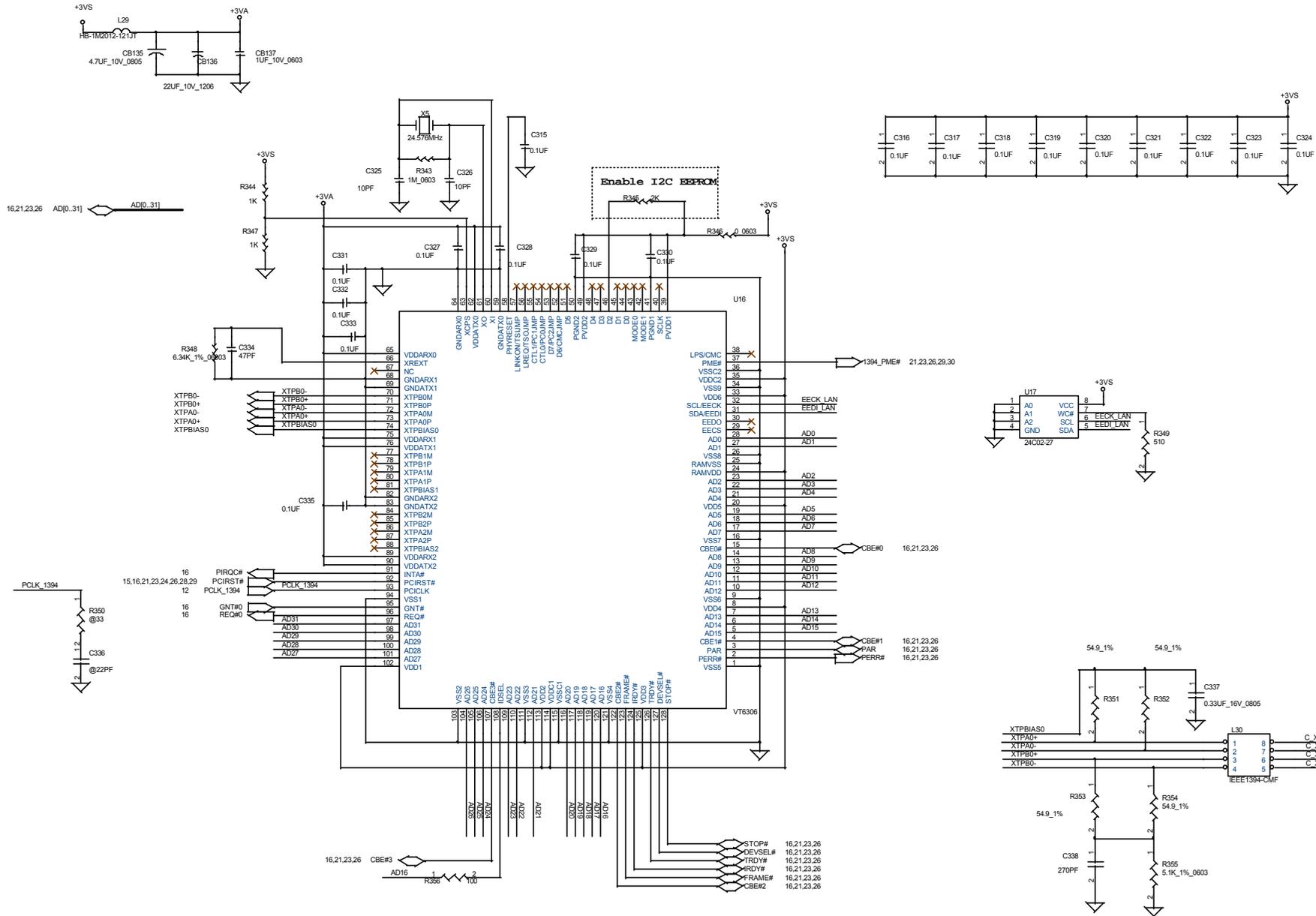
Compal Electronics, Inc.		
HDD & CDROM Connector		
Size	Document Number	Rev
LA-1341		1.0
Date	Monday, May 13, 2002	Sheet 20 of 46



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File	<b>LAN Controller</b>
Size	Document Number
	<b>LA-1341</b>
Date:	Monday, May 13, 2002
Sheet	21 of 46
Rev	1.0

# IEEE1394 Controller/PHY

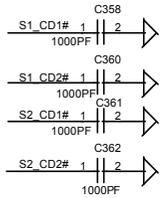
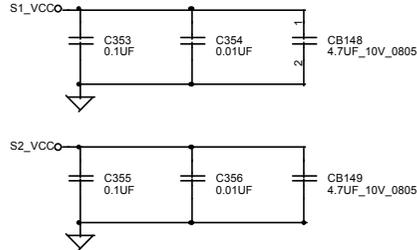
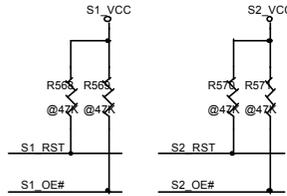
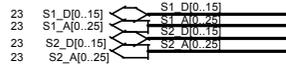
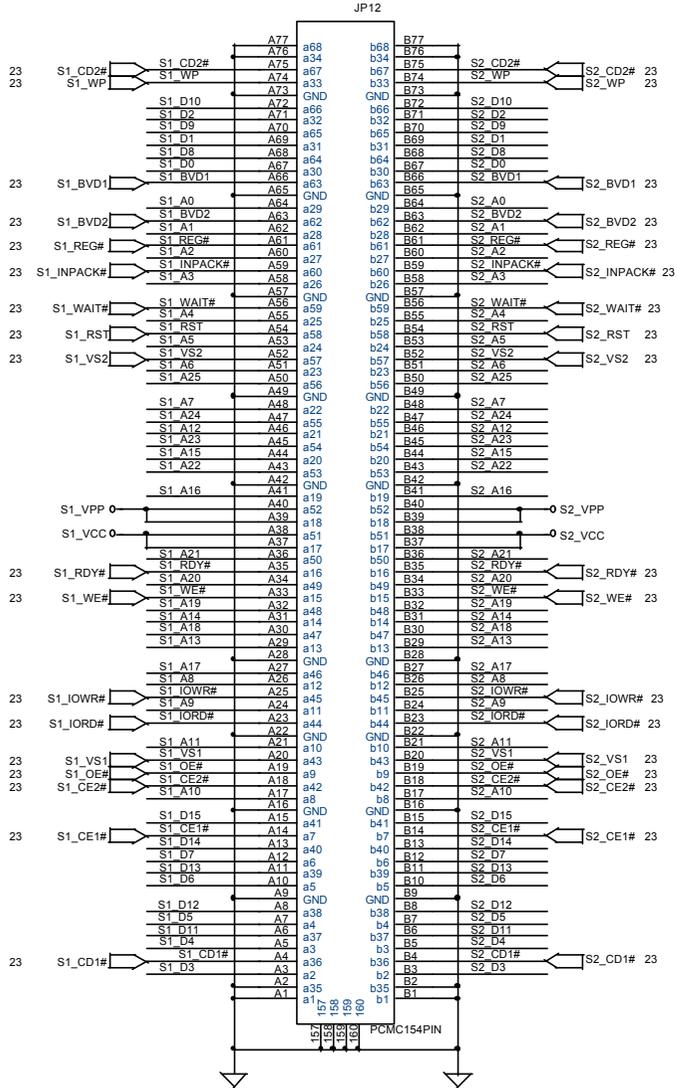


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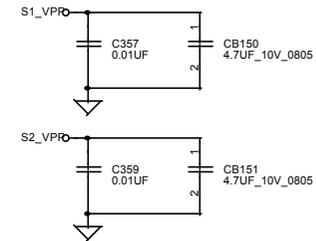
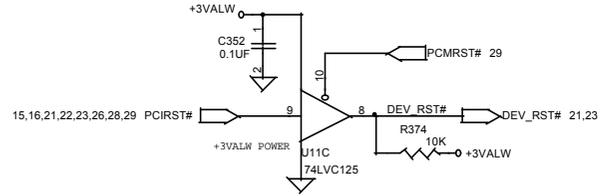
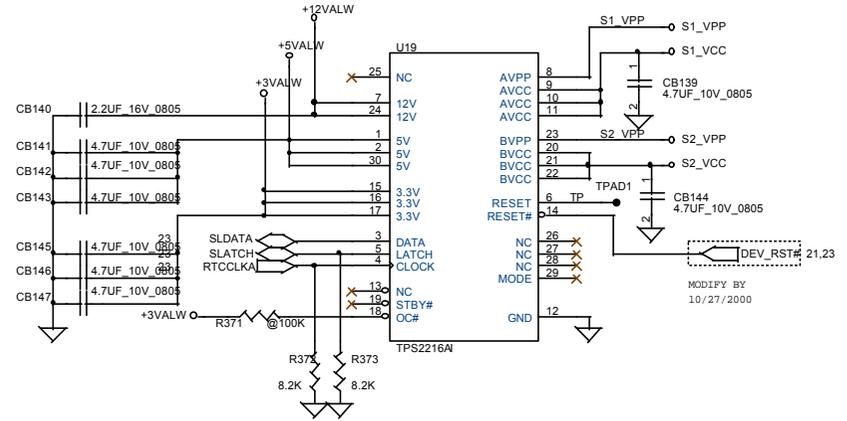
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<b>Compal Electronics, Inc.</b>	
<b>IEEE1394 Controller &amp; PHY</b>	
File	Rev
Size	Document Number
<b>LA-1341</b>	
Date	Monday, May 13, 2002
Sheet	22 of 46



# CARDBUS SOCKET

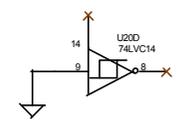
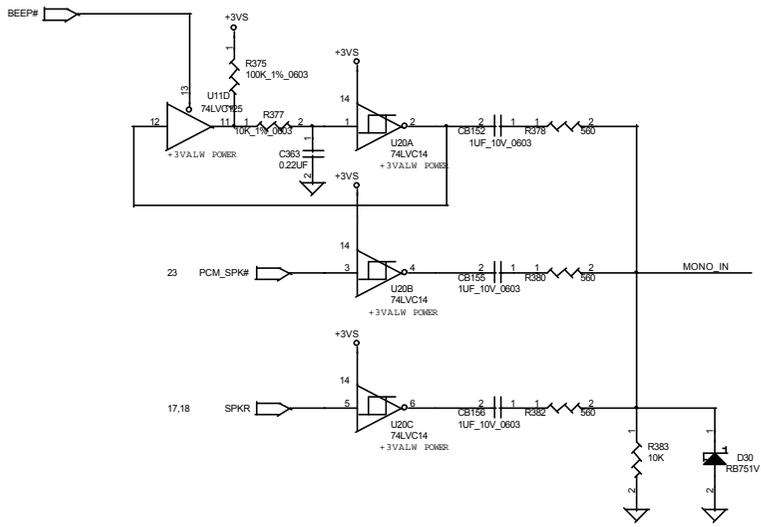


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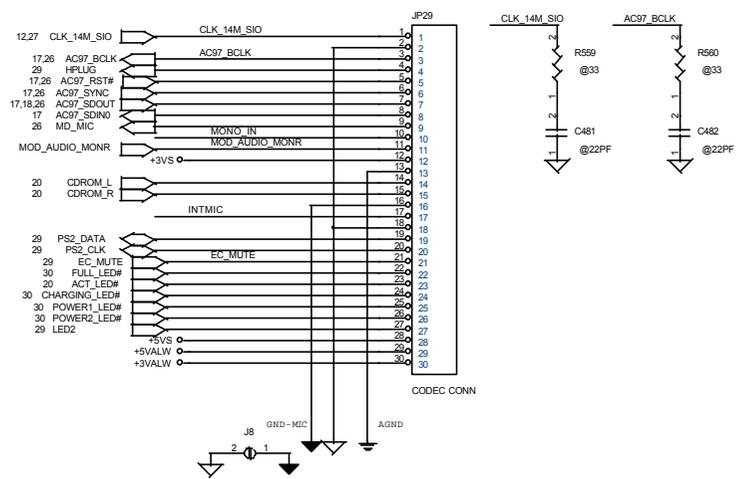
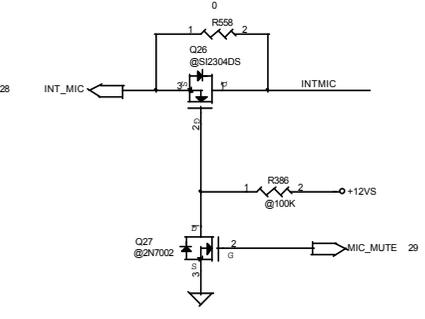
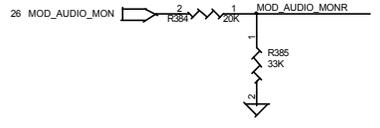


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Title <b>CARD BUS SOCKET</b>		
Size <b>B</b>	Document Number <b>LA-1341</b>	Rev <b>1.0</b>
Date: <b>Monday, May 13, 2002</b>	Sheet <b>24</b>	of <b>46</b>



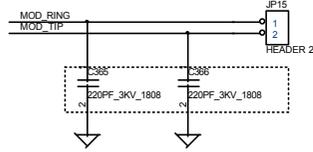
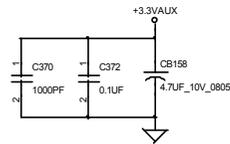
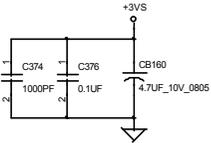
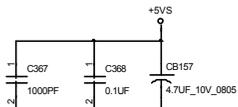
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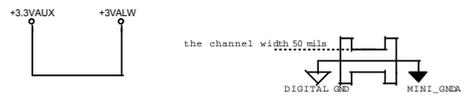
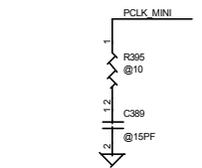
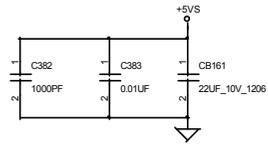
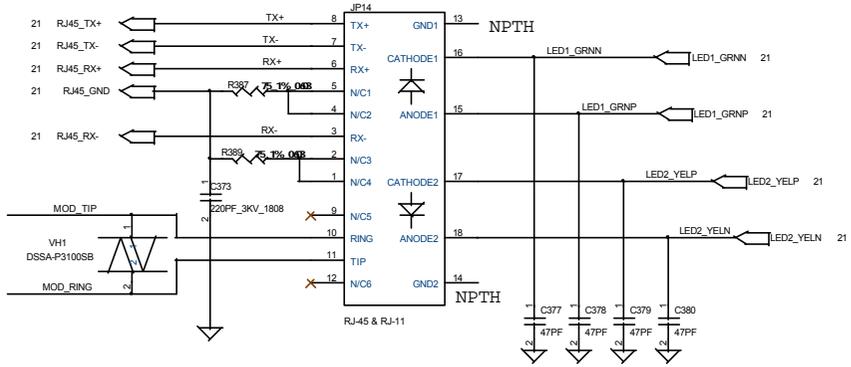
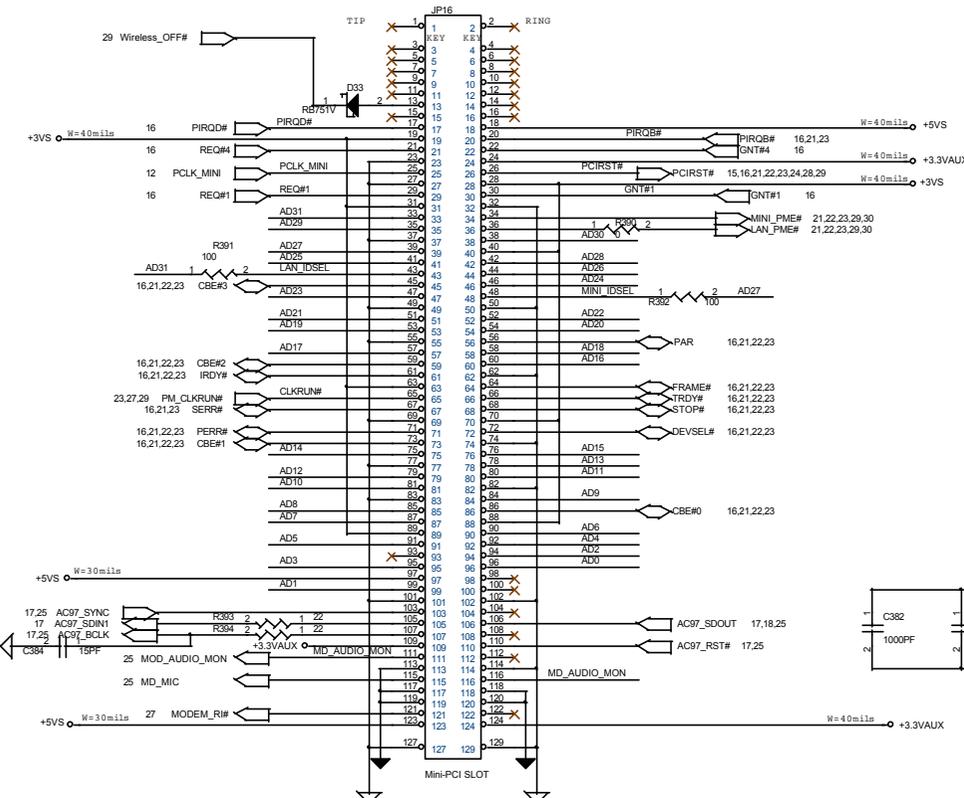
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Size	Document Number
	<b>LA-1341</b>
Date	Monday, May 13, 2002
Sheet	2 <sup>nd</sup> of 46
Rev	1.0

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# Mini-PCI Slot



AD[0..31] 16,21,22,23

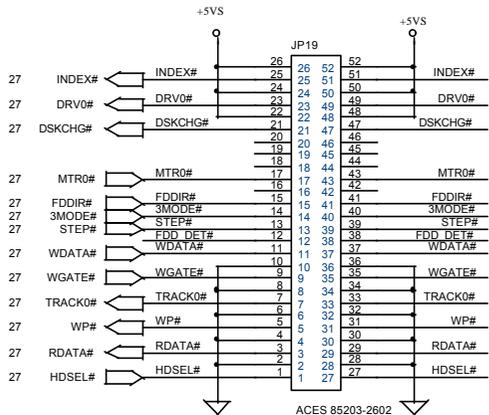


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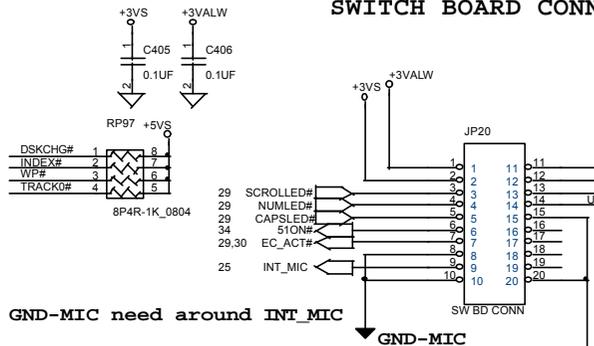
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File	Mini PCI Slot & SPR Docking
Size	Document Number
	<b>LA-1341</b>
Date	Monday, May 13, 2002
Sheet	26 of 46
Rev	1.0



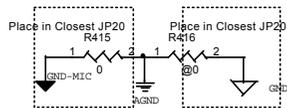
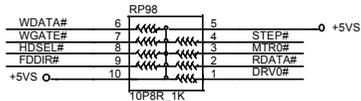
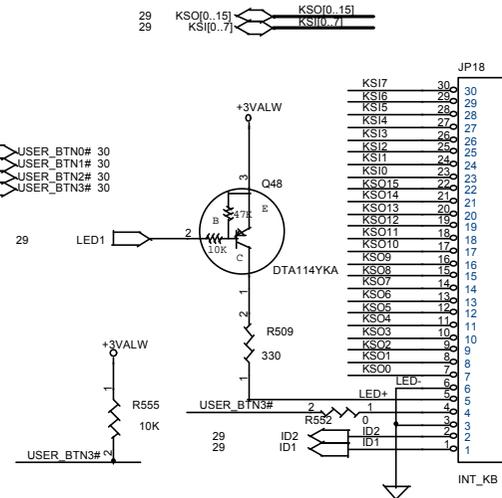
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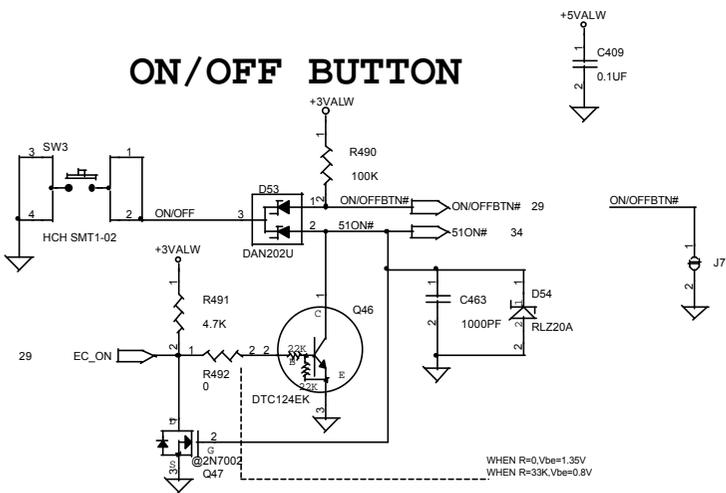
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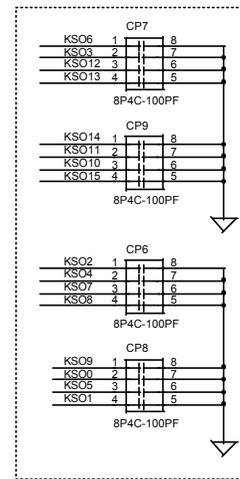
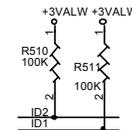
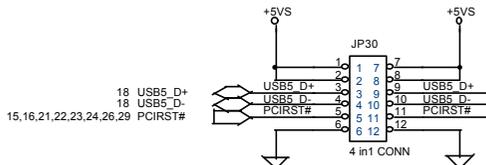
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# ON/OFF BUTTON

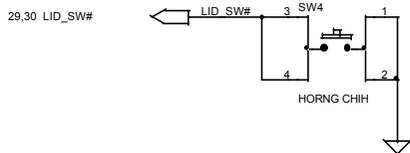


# 4 IN 1 CONN



NEED CLOSEST JP18 ADD BY EMI REQUEST

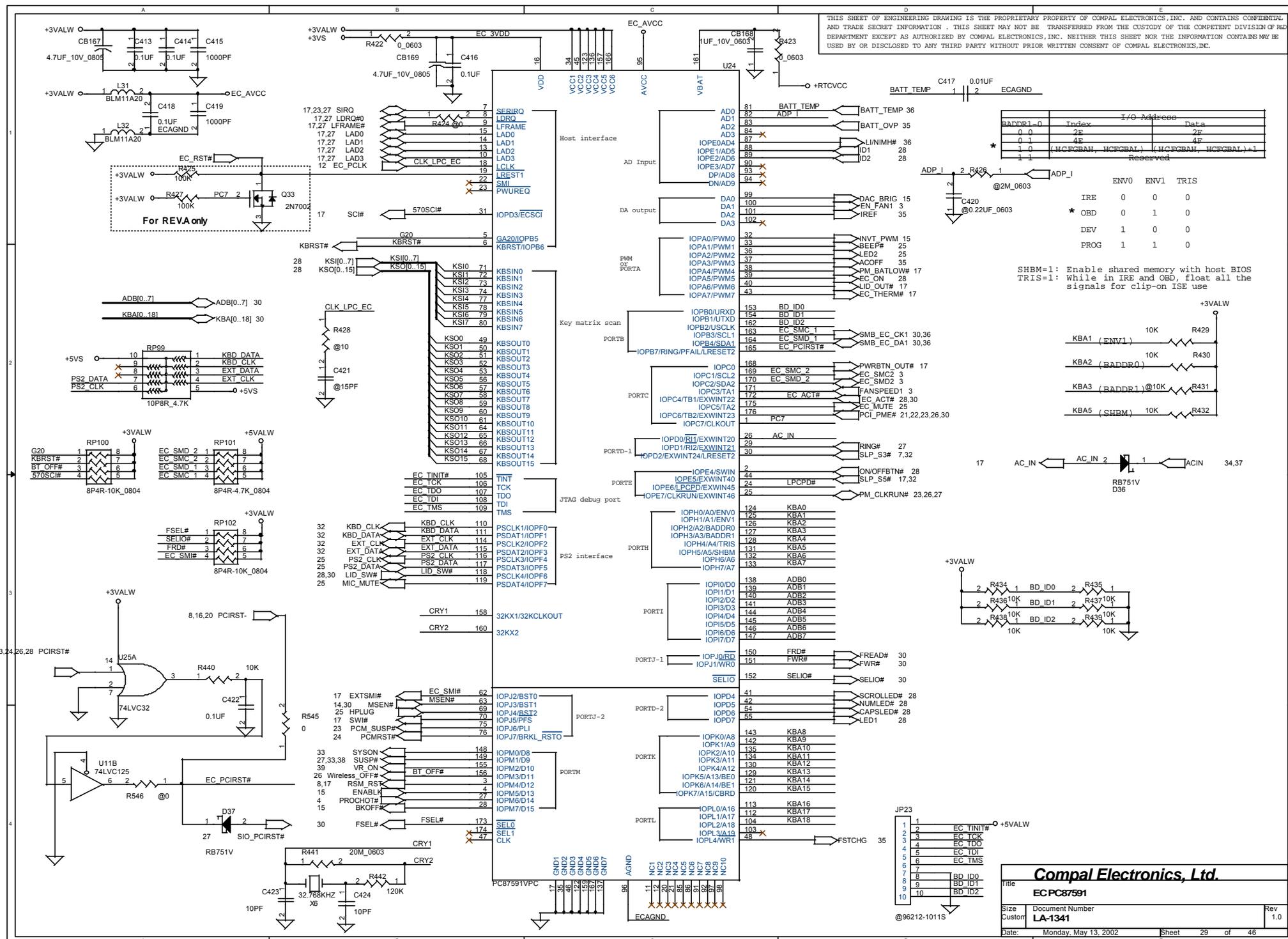
# LID SW



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<b>Compal Electronics, Inc.</b>		
Title	<b>System Connector</b>	
Size	Document Number	Rev
	<b>LA-1341</b>	1.0
Date	Monday, May 13, 2002	Sheet 28 of 46

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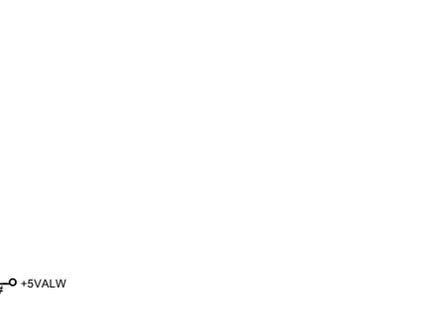
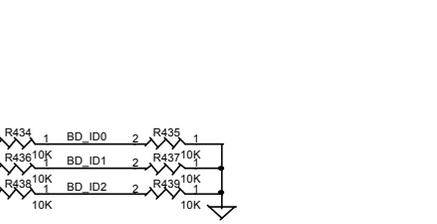
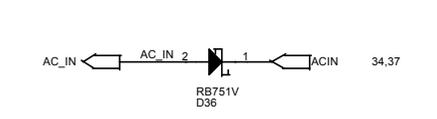
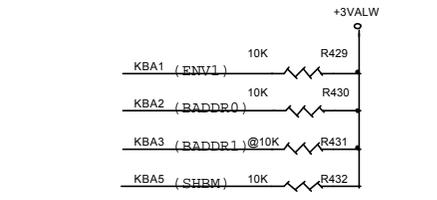


BADDR1-0	Index	I/O Address	Data
0 0	2F		2F
0 1	4F		4F
1 0	(HCP0BAH, HCP0BAL)	(HCP0BAH, HCP0BAL)+1	
1 1	Reserved		

ENVO	ENV1	TRIS
IRE	0	0
* OBD	0	1
DEV	1	0
PROG	1	1

SHBM=1: Enable shared memory with host BIOS  
 TRIS=1: While in IRE and OBD, float all the signals for clip-on ISE use



JP23	Pin	Signal
1	1	EC TINIT#
2	2	EC TCK
3	3	EC TDO
4	4	EC TDI
5	5	EC TMS
6	6	EC TMS
7	7	BD ID0
8	8	BD ID1
9	9	BD ID2
10	10	

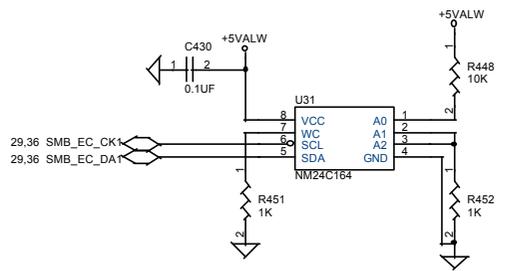
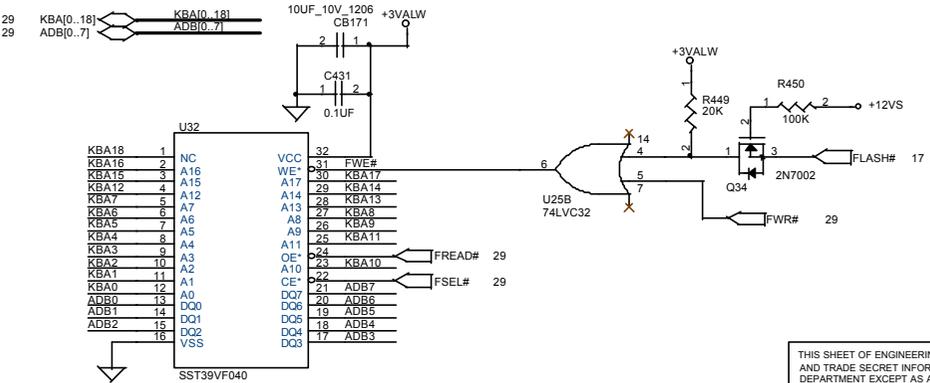
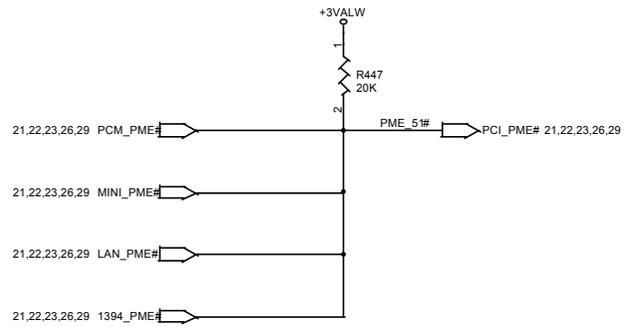
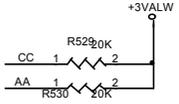
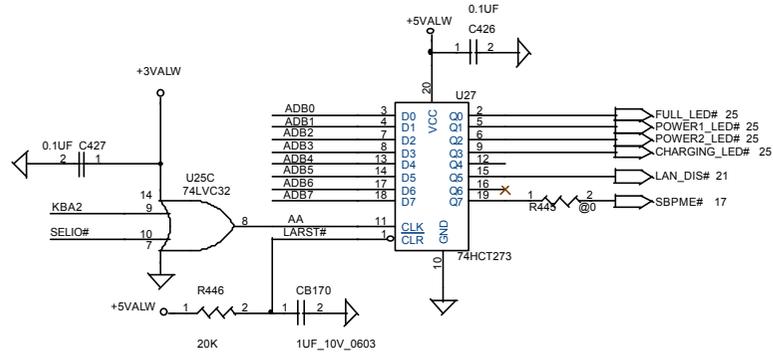
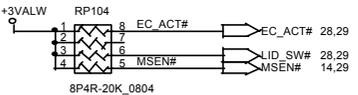
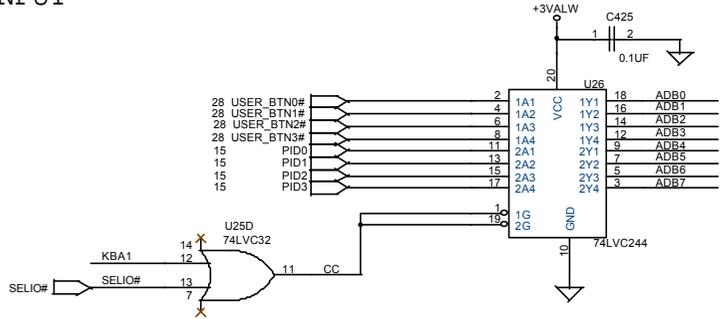
**Compal Electronics, Ltd.**

ECPC87591

Size: Document Number  
 Custom: LA-1341  
 Date: Monday, May 13, 2002  
 Sheet: 29 of 46  
 Rev: 1.0

INPUT

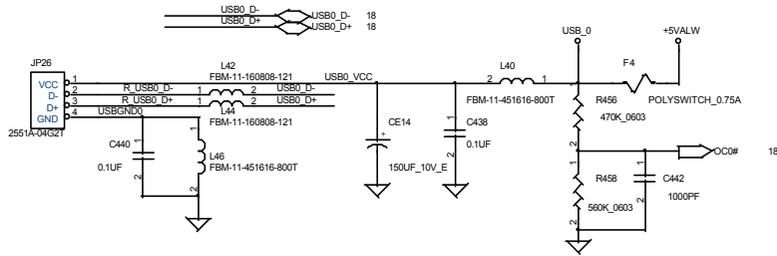
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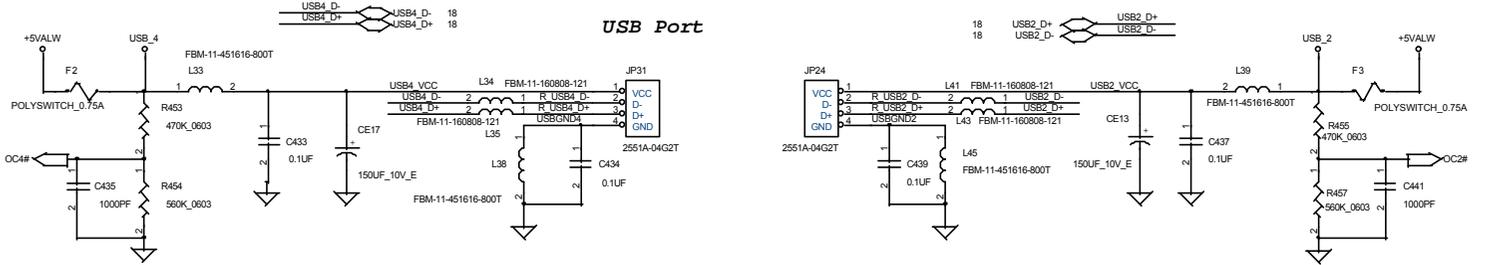
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<b>Compal Electronics, Inc.</b>		
Title	<b>BIOS &amp; EC I/O Port</b>	
Size	Document Number	Rev
	<b>LA-1341</b>	1.0
Date	Monday, May 13, 2002	Sheet 30 of 46

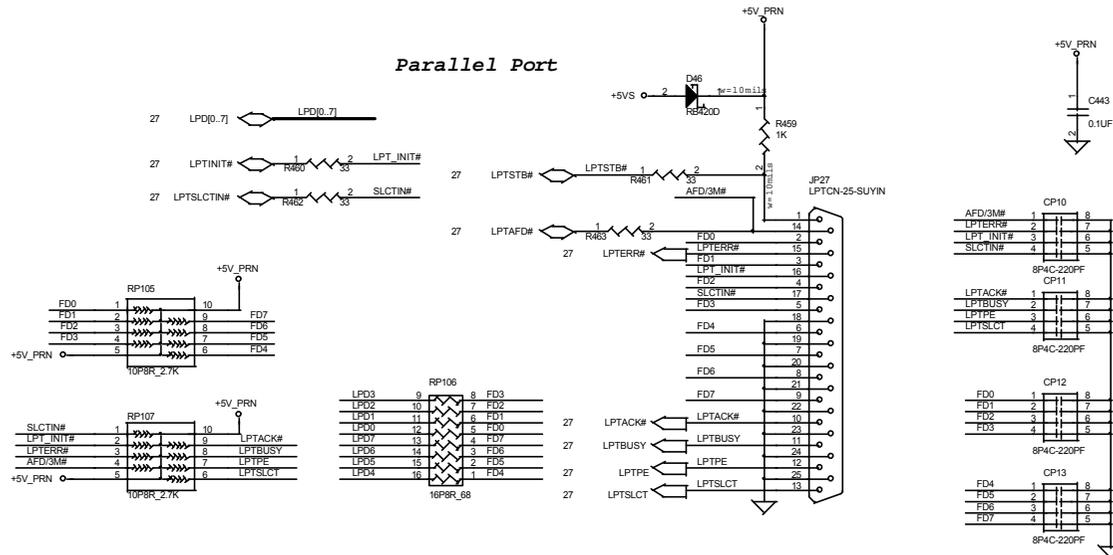
# Printer Port/USB



## USB Port



## Parallel Port

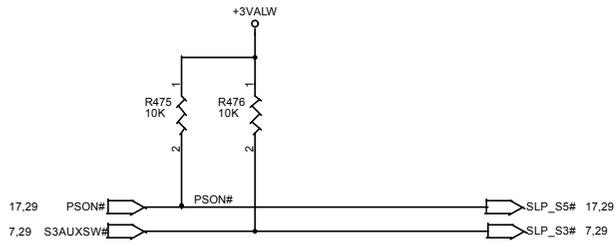
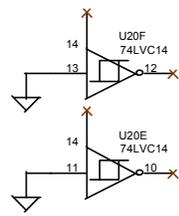
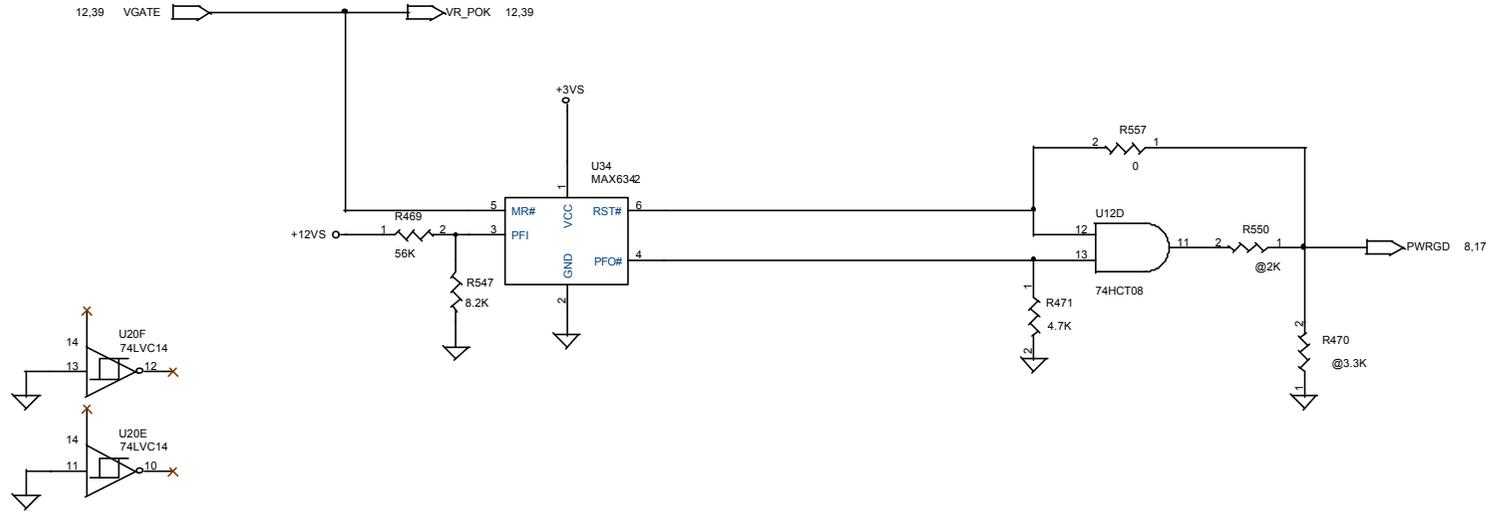


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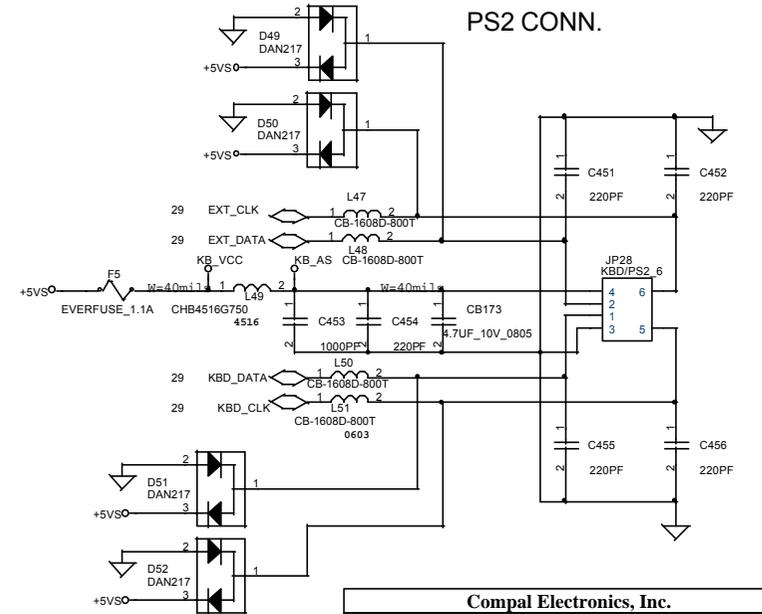
Printer & USB Port

File	Document Number	Rev
	LA-1341	1.0
Date	Monday, May 13, 2002	Sheet 31 of 46

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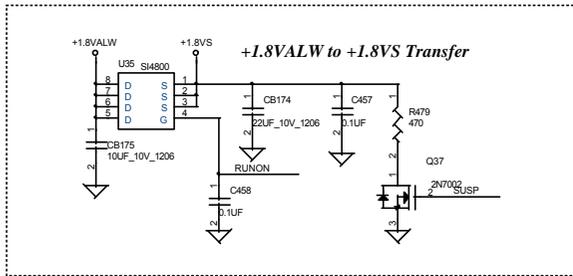
	S1	S3	S5
S3AUXSW#	1	0	1
PSON#	0	1	1
SLP_S3#	1	0	0
SLP_S5#	1	1	0



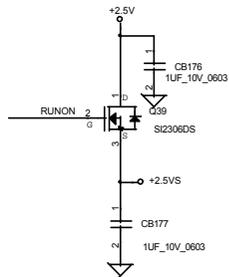
**Compal Electronics, Inc.**

Title <b>RESET &amp; PS2 Connector</b>		
Size	Document Number <b>LA-1341</b>	Rev 1.0
Date	Monday, May 13, 2002	Sheet 32 of 46

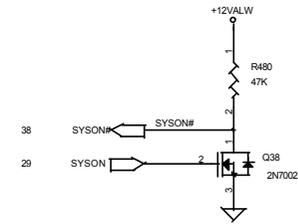
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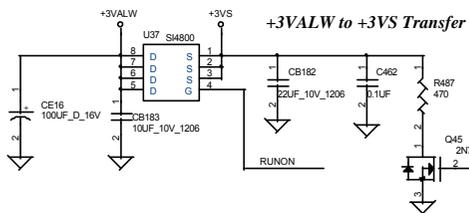
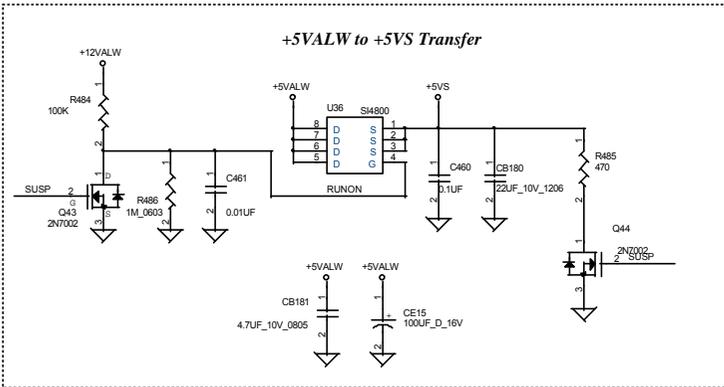
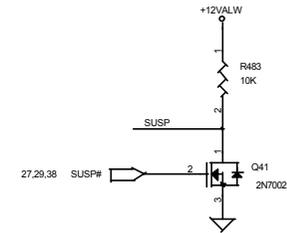
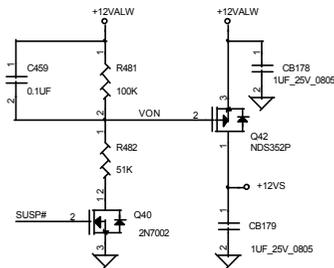
**+2.5V to +2.5VS Transfer**



**1.8VALW/+1.5VS Power direct provide**

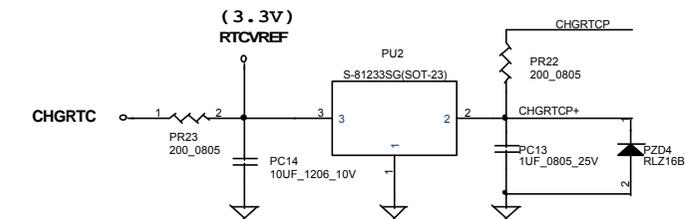
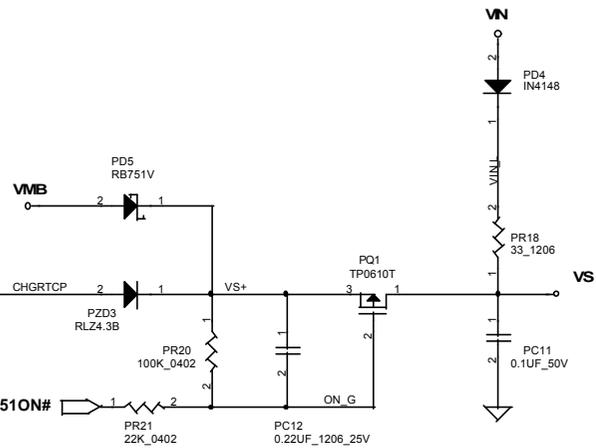
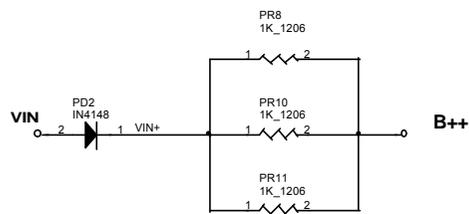
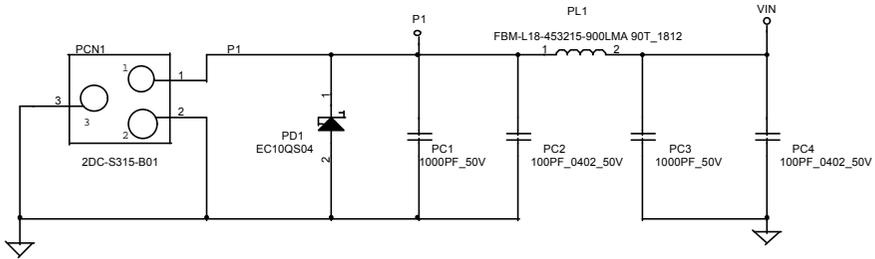


**+12VALW TO +12VS Transfer**

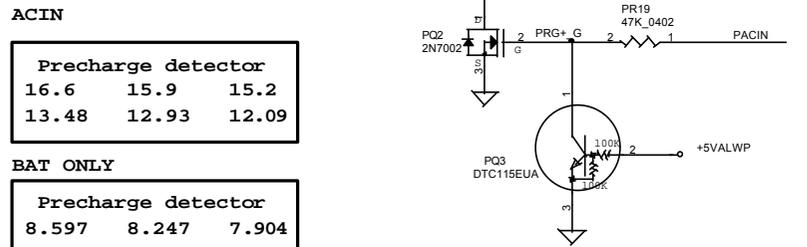
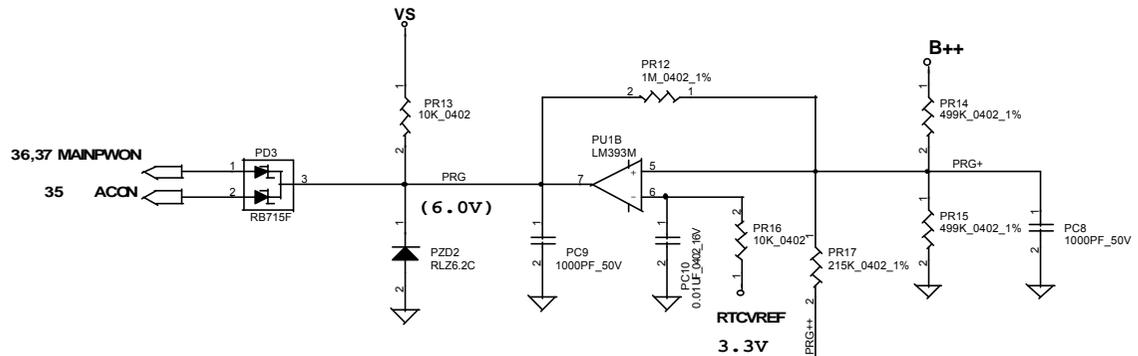
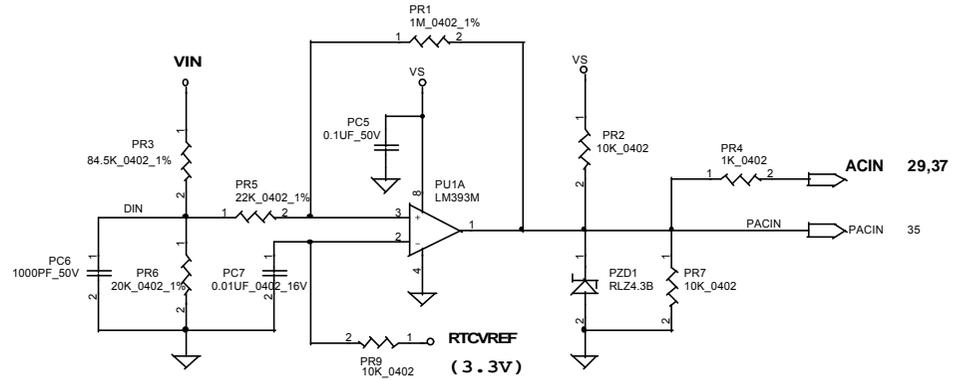


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<b>Compal Electronics, Inc.</b>		
File	<b>DC/DC Circuits</b>	
Size	Document Number	Rev
	<b>LA-1341</b>	1.0
Date:	Monday, May 13, 2002	Sheet 33 of 46

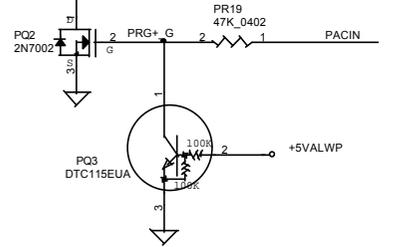


Vin Detector		
High	18.784	17.901
Low	17.877	16.195



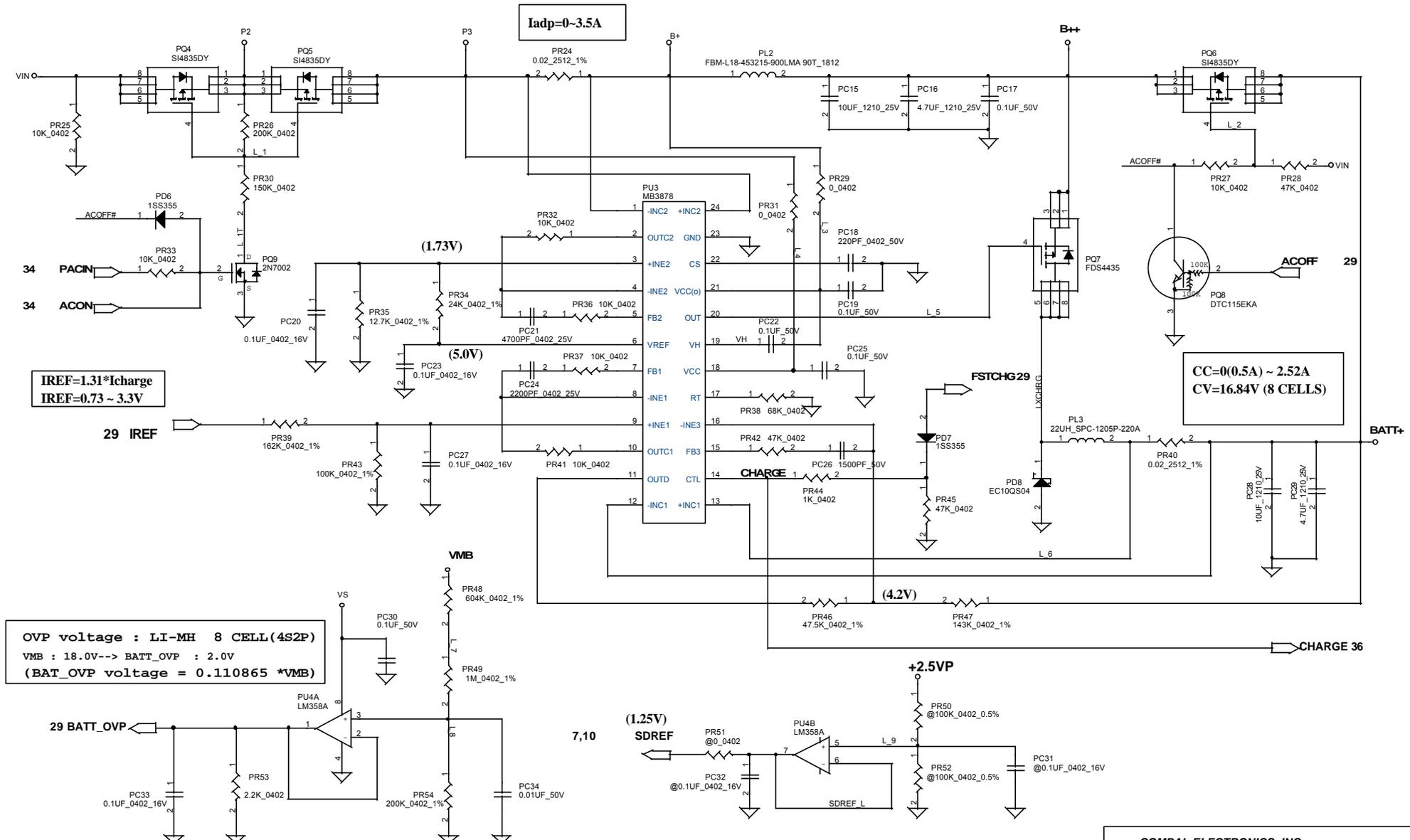
Precharge detector		
16.6	15.9	15.2
13.48	12.93	12.09

BAT ONLY		
8.597	8.247	7.904
6.310	6.101	5.683



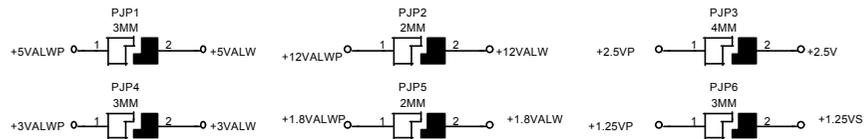
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COMPAL ELECTRONICS, INC		
Title <b>DCIN &amp; DETECTOR</b>		
Size B	Document Number <b>L A- 1341</b>	Rev <b>1.0</b>
Date: Monday, May 13, 2002	Sheet	34 of 46

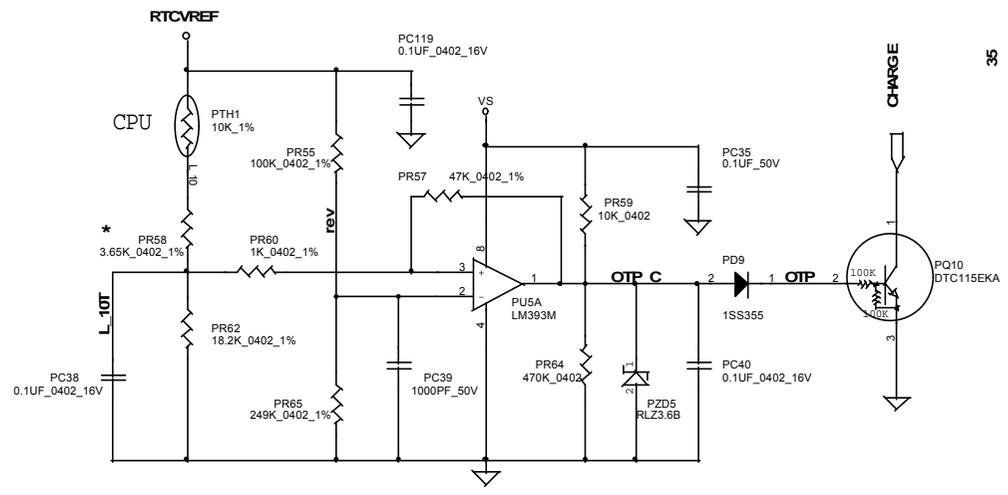
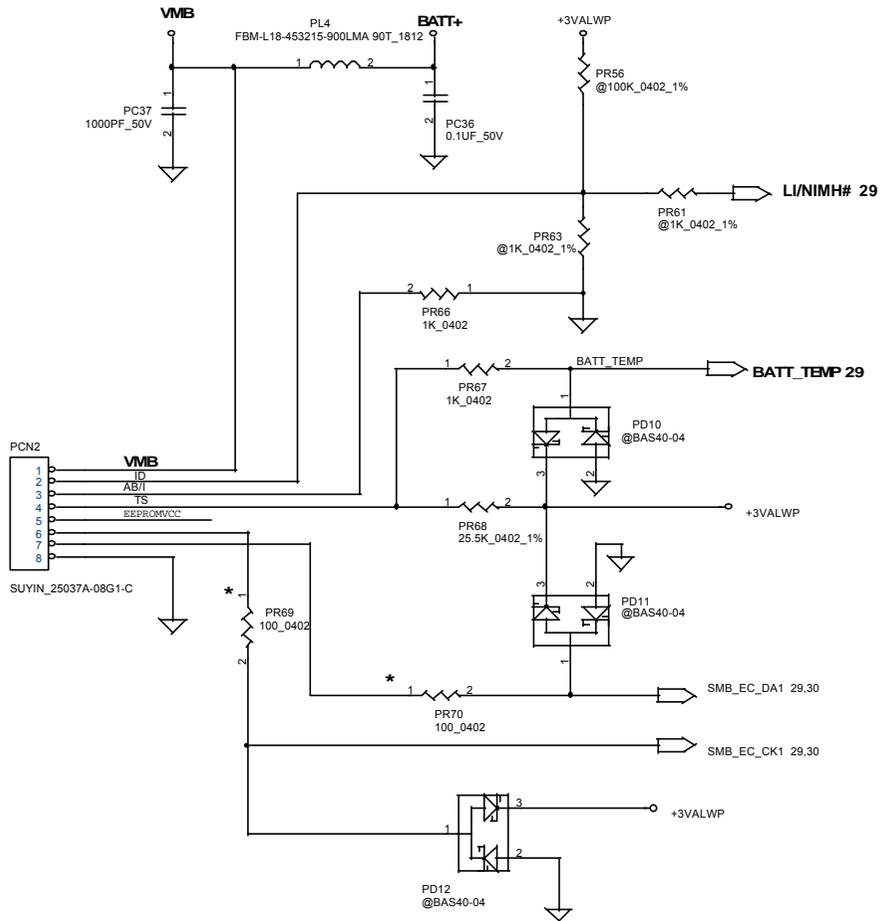


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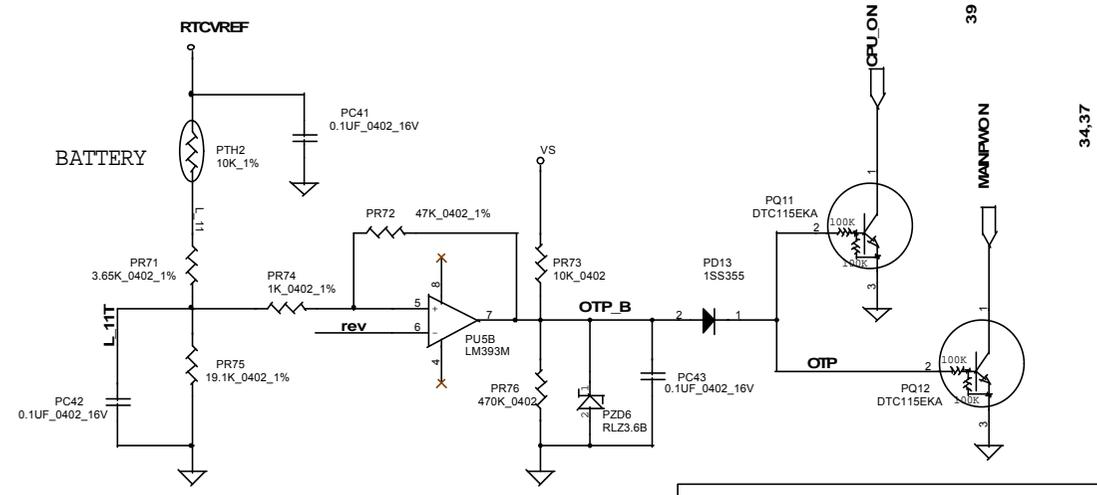
<b>COMPAL ELECTRONICS, INC</b>		
Title	<b>CHARGER</b>	
Size	Document Number	Rev
<b>B</b>	<b>LA - 1341</b>	<b>1.0</b>
Date:	Monday, May 13, 2002	Sheet 35 of 46



**PH1 under CPU bottom side :**  
 CPU thermal protection at 90(91) $\pm$ 3 degree C  
 Recovery at 50(51) $\pm$ 3 degree C

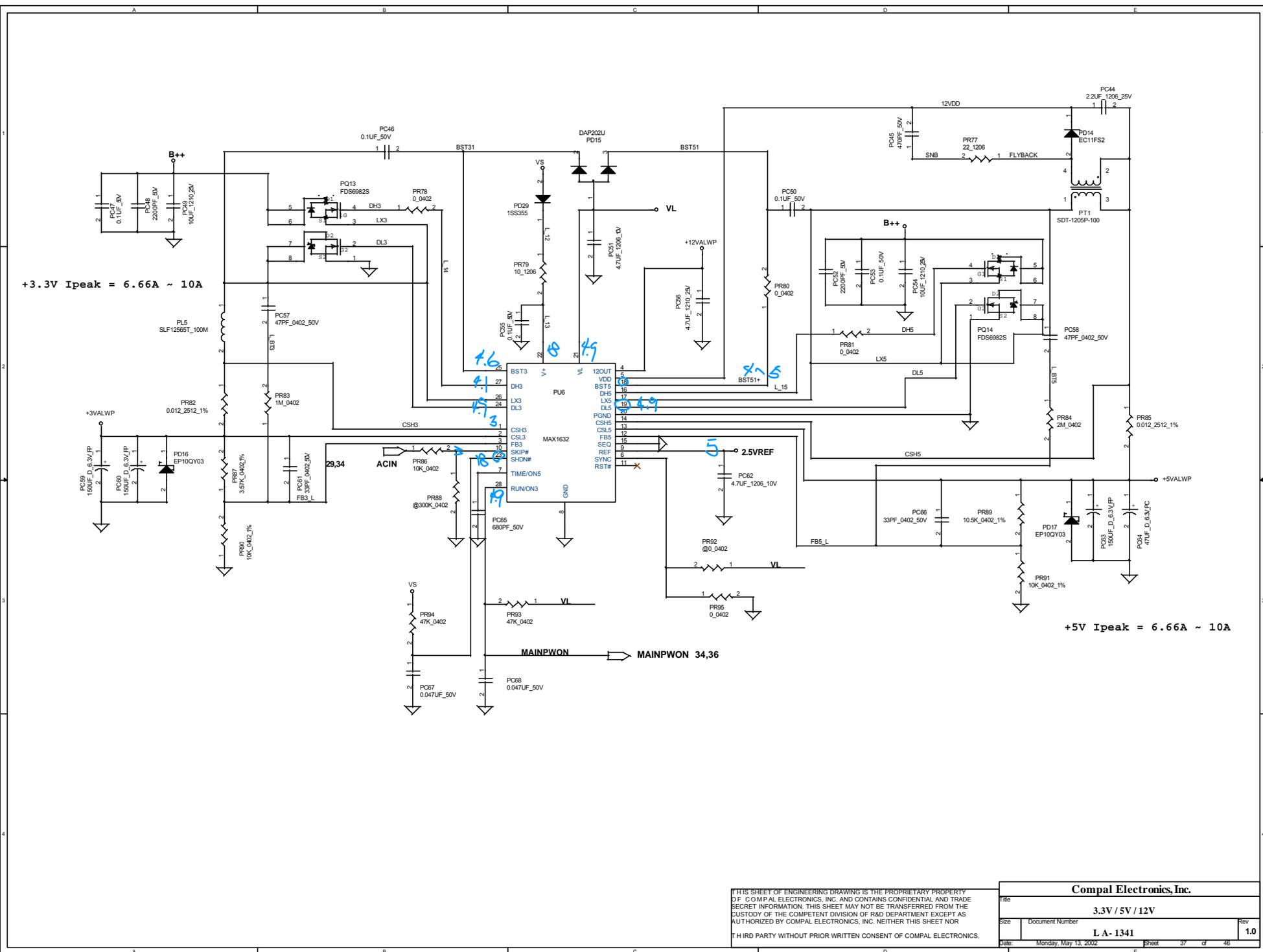


**PH2 near main Battery CONN :**  
 BAT. thermal protection at 85(86) $\pm$ 3 degree C  
 Recovery at 50(51) degree C



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<b>COMPAL ELECTRONICS, INC</b>		
Title		
<b>BATTERY CONN / OTP</b>		
Size	Document Number	Rev
<b>B</b>	<b>L A- 1341</b>	<b>1.0</b>
Date: Monday, May 13, 2002	Sheet	36 of 46

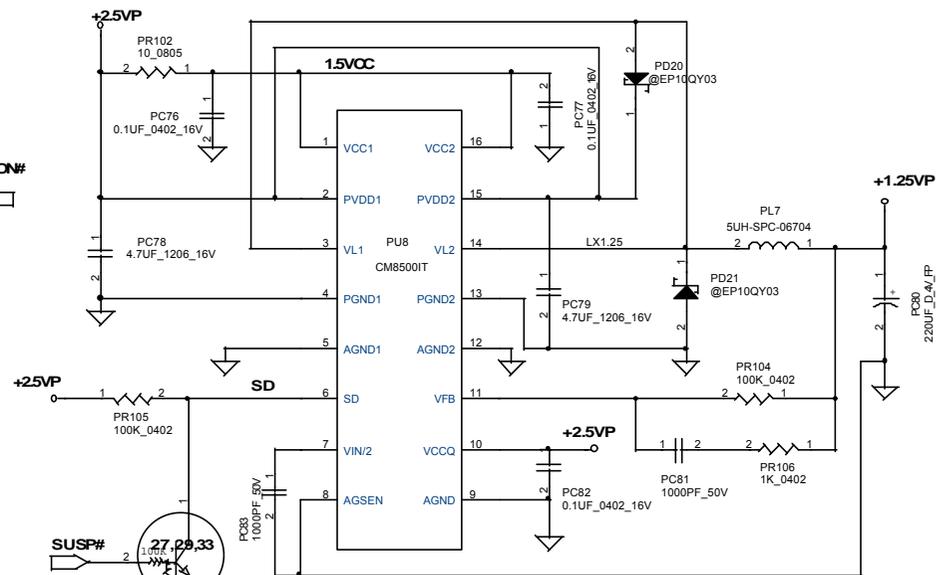
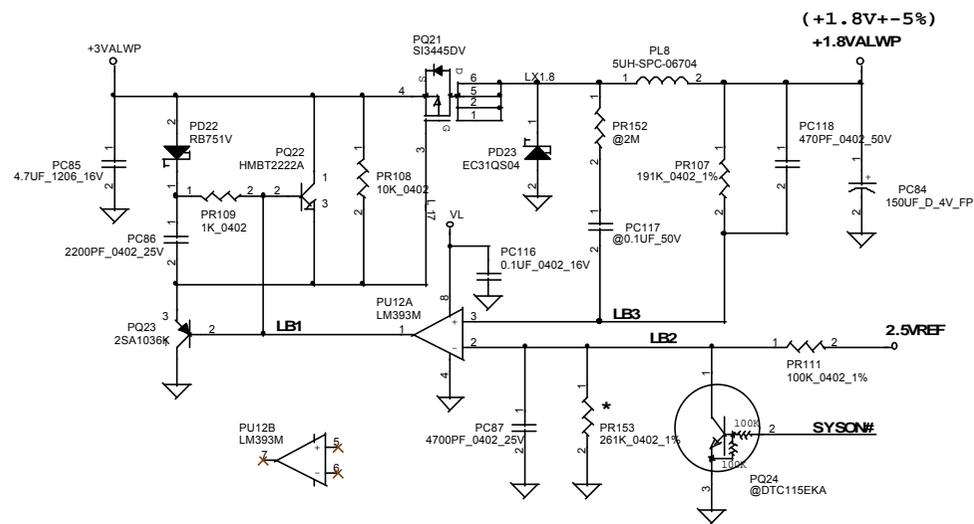
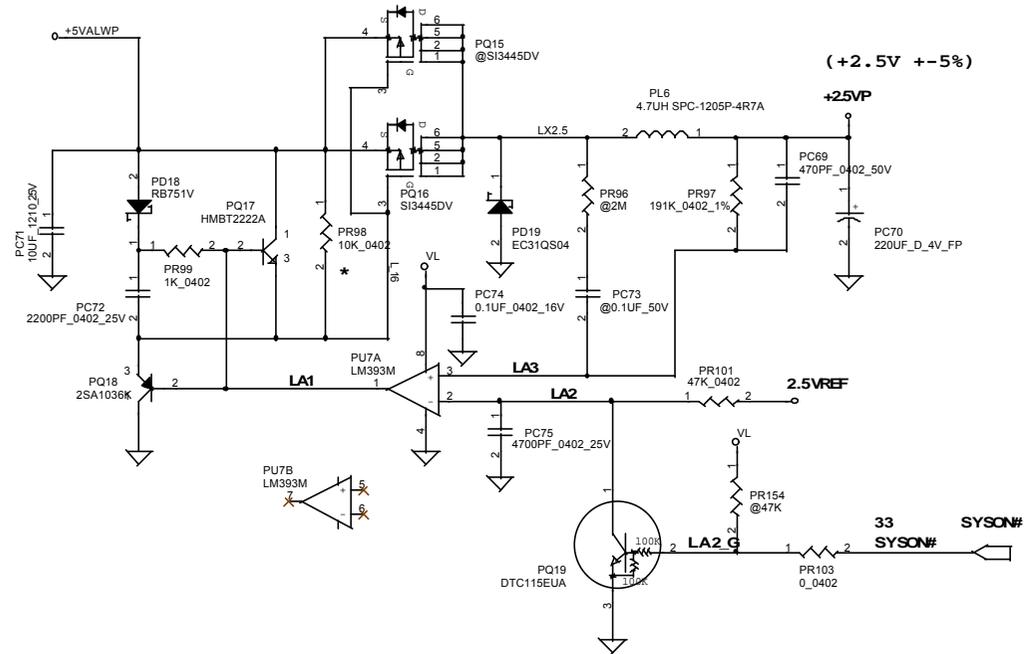


+3.3V Ipeak = 6.66A ~ 10A

+5V Ipeak = 6.66A ~ 10A

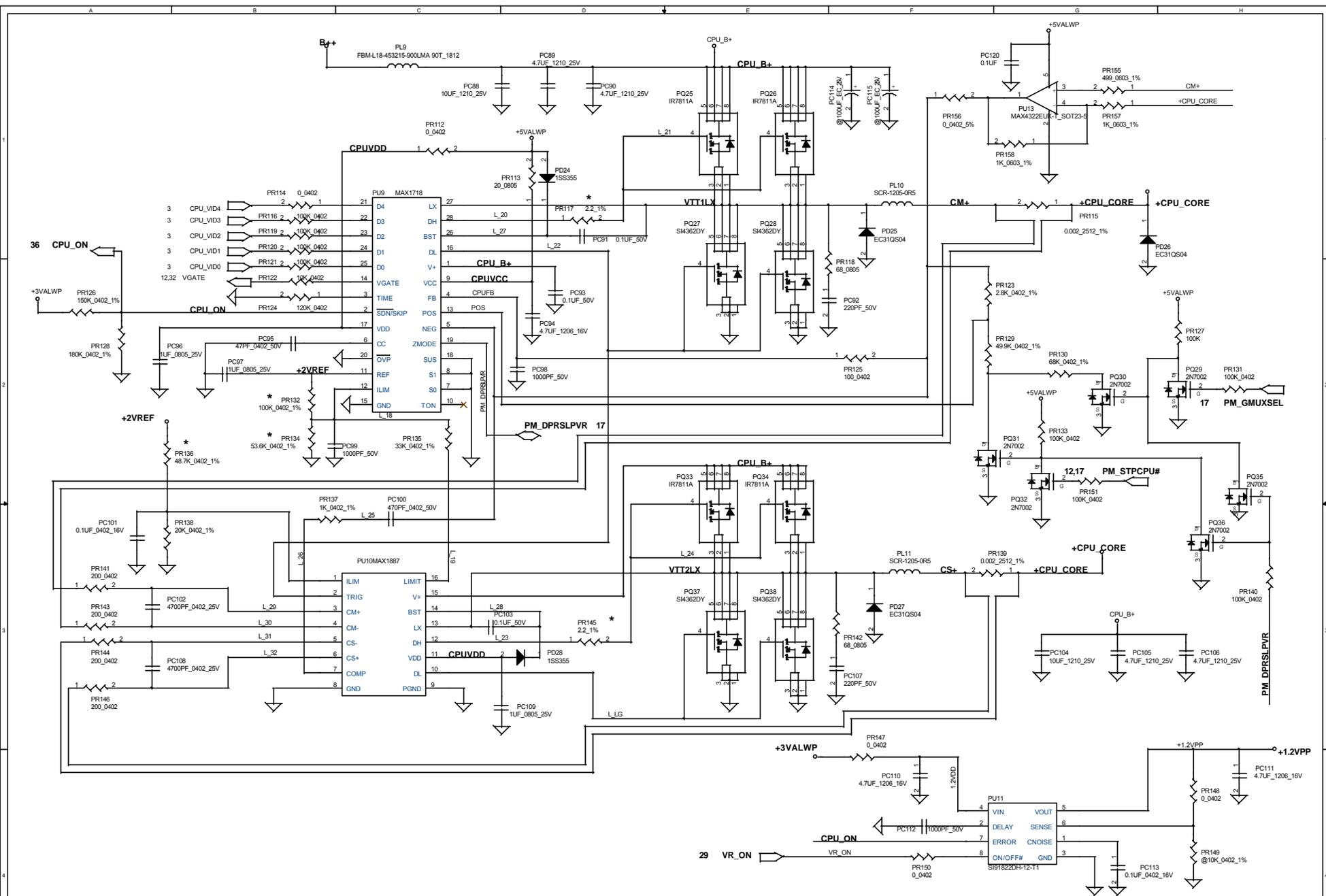
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<b>Compal Electronics, Inc.</b>		
3.3V / 5V / 12V		
Size	Document Number	Rev
	<b>L A - 1341</b>	<b>1.0</b>
Date	Monday, May 13, 2002	Sheet 3/ of 46



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<b>COMPAL ELECTRONICS, INC</b>	
Title <b>DDR /2.5V / 1.8V</b>	
Size <b>B</b>	Document Number <b>L A- 1341</b>
Date: Monday, May 13, 2002	Rev <b>1.0</b>
Sheet	38 of 46



	GMUXSEL	STPCPU#	DPRSLPVR	VCORE*	Offset	VCORE
PM	1	1	0	1.30V	0%	1.30V
PM D-S	1	0	0	1.239V	4.62%	1.239V
EM	0	1	0	1.20V	2.0%	1.176V
EM D-S	0	0	0	1.144V	4.62%	1.144V
Deeper	X	0	1	1.0V	0%	1.0V

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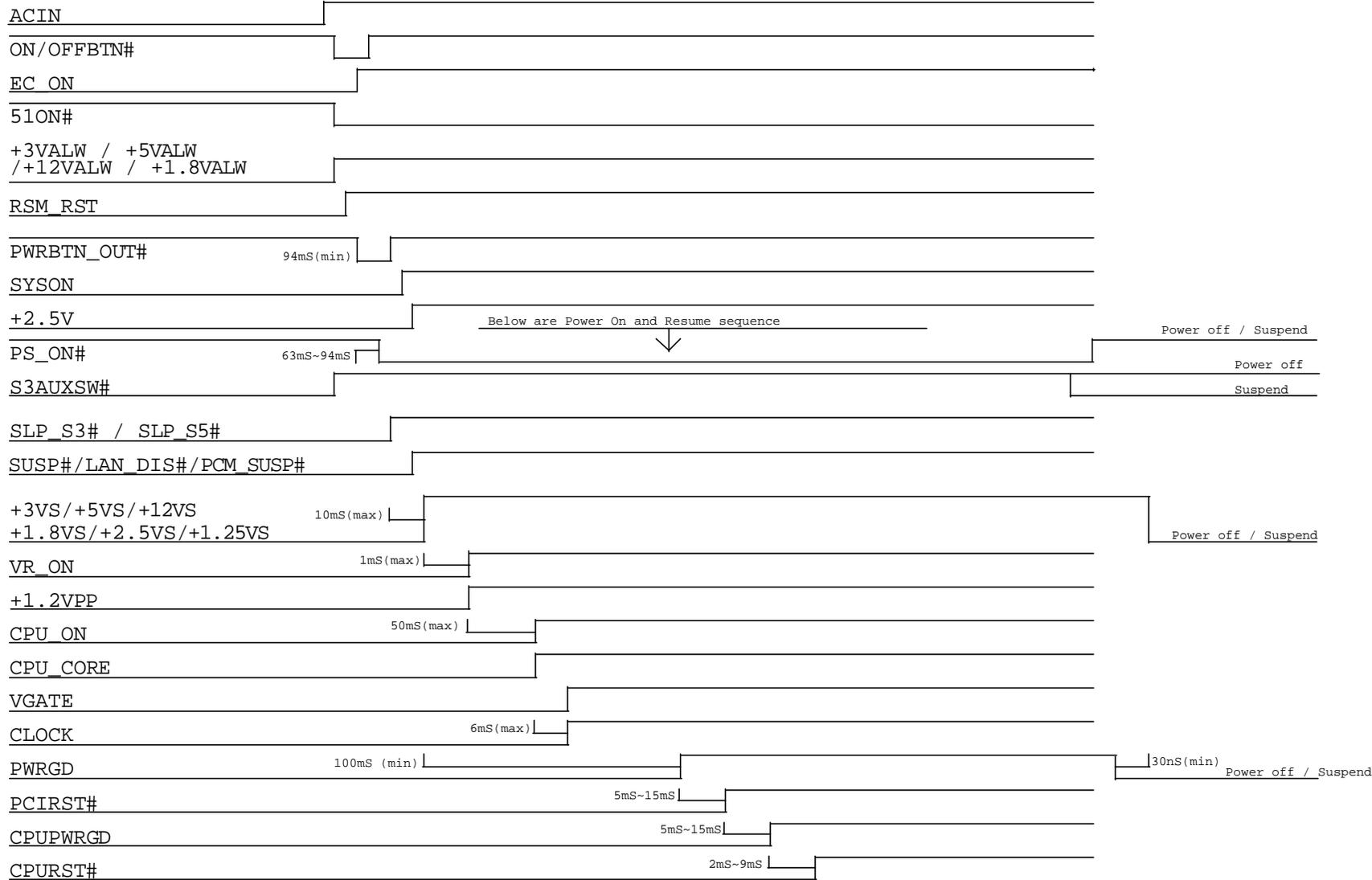
**COMPAL ELECTRONICS, INC**

**+CPU CORE**

File: \_\_\_\_\_  
 Size: \_\_\_\_\_ Document Number: \_\_\_\_\_  
 B: \_\_\_\_\_ L A-1341  
 Date: Monday, May 13, 2002 Sheet 39 of 46  
 Rev: **1.0**

# Power ON sequence

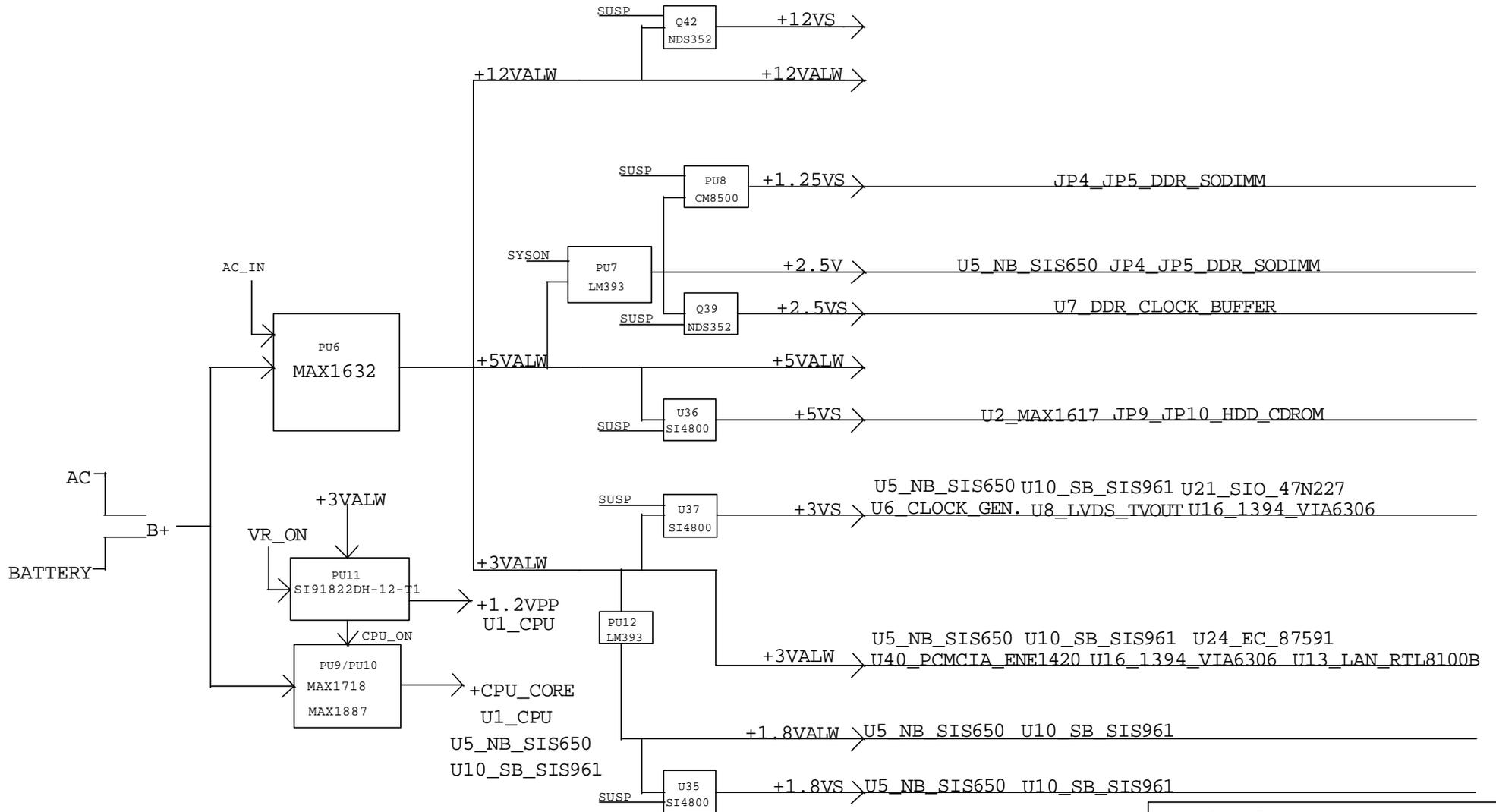
# Power Off sequence



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Compal Electronics, Inc.		
Title Power On Sequence Chart		
Size B	Document Number LA-1341	Rev 1.0
Date Monday, May 13, 2002	Sheet 40	of 46

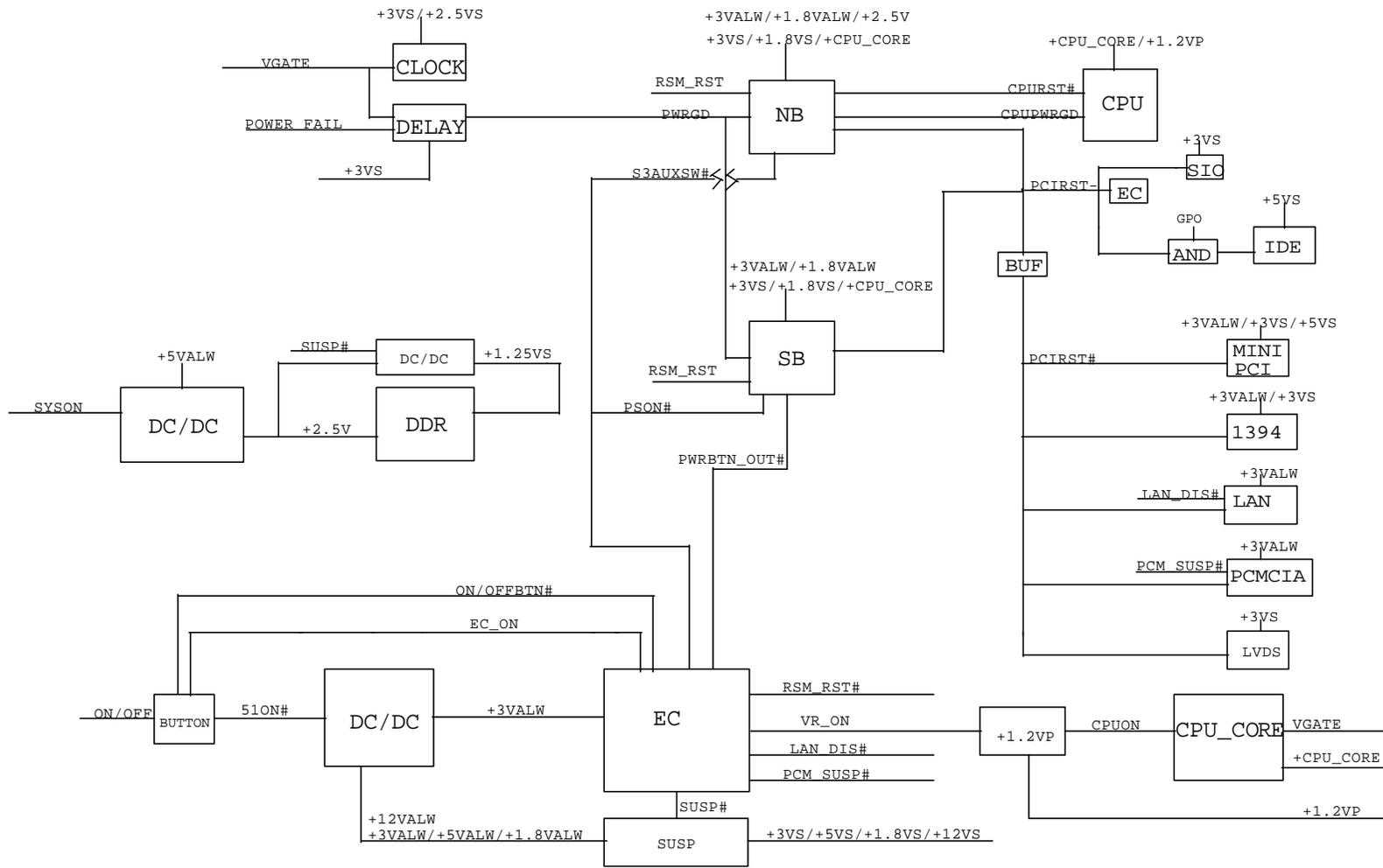
# POWER SOURCE BLOCK DIAGRAM



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Compal Electronics, Inc.		
Power Source Diagram		
File	Document Number	
Size B	LA-1341	Rev 1.0
Date	Monday, May 13, 2002	Sheet 41 of 46

# ACY25 RESET MAP DIAGRAM



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Compal Electronics, Inc.			
Reset Map Diagram			
Size B	Document Number LA-1341	Rev 1.0	
Date Monday, May 13, 2002	Sheet 42	of 46	

**Power PIR**

Item	Fixed Issue	Reason for change	Page	Modify item	MB_Ver.	Phase
1	NO	Improve CPU_CORE voltage regulator.	39		0.3	C test
2						
3						
4						
5						
6						
7						
8						
9						
10						
11						
12						
13						
14						
15						
16						
17						
18						

<b>Compal Electronics, Inc.</b>		
Title		
<b>Power PIR</b>		
Size A	Document Number <b>LA-1341</b>	Rev <b>1.0</b>
Date:	Monday, May 13, 2002	Sheet 43 of 46

UNIT	IDSEL	IRQ	GNT	REQ
1394 U16	AD16	PIRQC#	GNT#0	REQ#0
MINIPCI JP16	AD31	PIRQB#	GNT#1	REQ#1
LAN U13	AD17	PIRQB#	GNT#3	REQ#3
CARDBUS U40	AD20	PIRQA/B#	GNT#2	REQ#2

SMBUS from EC

EC\_SMD2,EC\_SMC2 : U2 (MAX1617) AD : 1001 110  
 SMB\_EC\_CK1,SMB\_EC\_DA1: U31( EEPROM ) , PCN2 (BATT CONN)

SMBUS from SIS961

SMBCLK , SMBDAT: JP5 , JP4 , CLK GEN ( U6 ) , CLK BUF( U7 ).

ACY25 A-TEST Modify

Change to 310LV : Add R64,R73,R76. Del R77,R78,Q49,Q50,R539

Add DPSP# : Add Q49 ,R551

DPRSLPVR : Change to pull Low =Del R536 Add R284 ; Add U41 ,R554.

AUXOK : Del CB112

IDERST# : Add D56 , R548

LAN : VDD2.5 add L27,C294,C297,C299

1394 : +3VA change to +3VS power , R351,R352,R353,R3354 change to 54.9\_1% , R355 change to 5.1K\_1% , C337 change to .33UF , C338 change to 270PF

KB : Add R552 to disconnect ON/OFF

PSO# : Connect to SLP\_S5# directly. Del U33

S3AUXSW# : Connect to SLP\_S3# directly

PWRGD : Add R550 transfer 5V to 3V

+2.5V : Q39 using SI2306 to transfer +2.5VS

H\_DPSP# : Add Q49 , R551 to connect with PM\_STPCPU#

Title		
(Title)		
Size B	Document Number (Doc)	Rev (RevCode)
Date	Friday, April 26, 2002	Sheet 44 of 46

CDLED# : Add R553 to disconnect with JP10

USER\_BTN3# : Add R552 to disconnect with JP18,R555 pull high to +3VALW

DDR termination : RP32~RP57 , R494~R508 change to 33 ohm

PWRGD : Del C42 , C256

SUSP# : R487 change to 75 ohm

FOR C TEST

LED1 : Q48 PIN3 CHANGE TO +3VALW

FWSDCLKO : Add pull high resistor R556

PWRGD : Add pass through resistor R557

CRTVDD : R170,R171 change from 2.2K to 1K

GPIO19,20 : Add pull high resistor R566,R567 , del R269

EC\_ON : Del Q47. R492 change to 0 ohm

EN\_FAN1 : Add U42 , C483 , C484 , R561 ,R562

CLKFS2 :Del R161 , Add R565

AUXOK : Del D18 , R254

For MP

+5VFAN1 : Add D58 for reserve

S1\_RST# ,S2\_OE# , S2\_RST# , S2\_OE# :Add R568,R569,R570,R571 for reserve

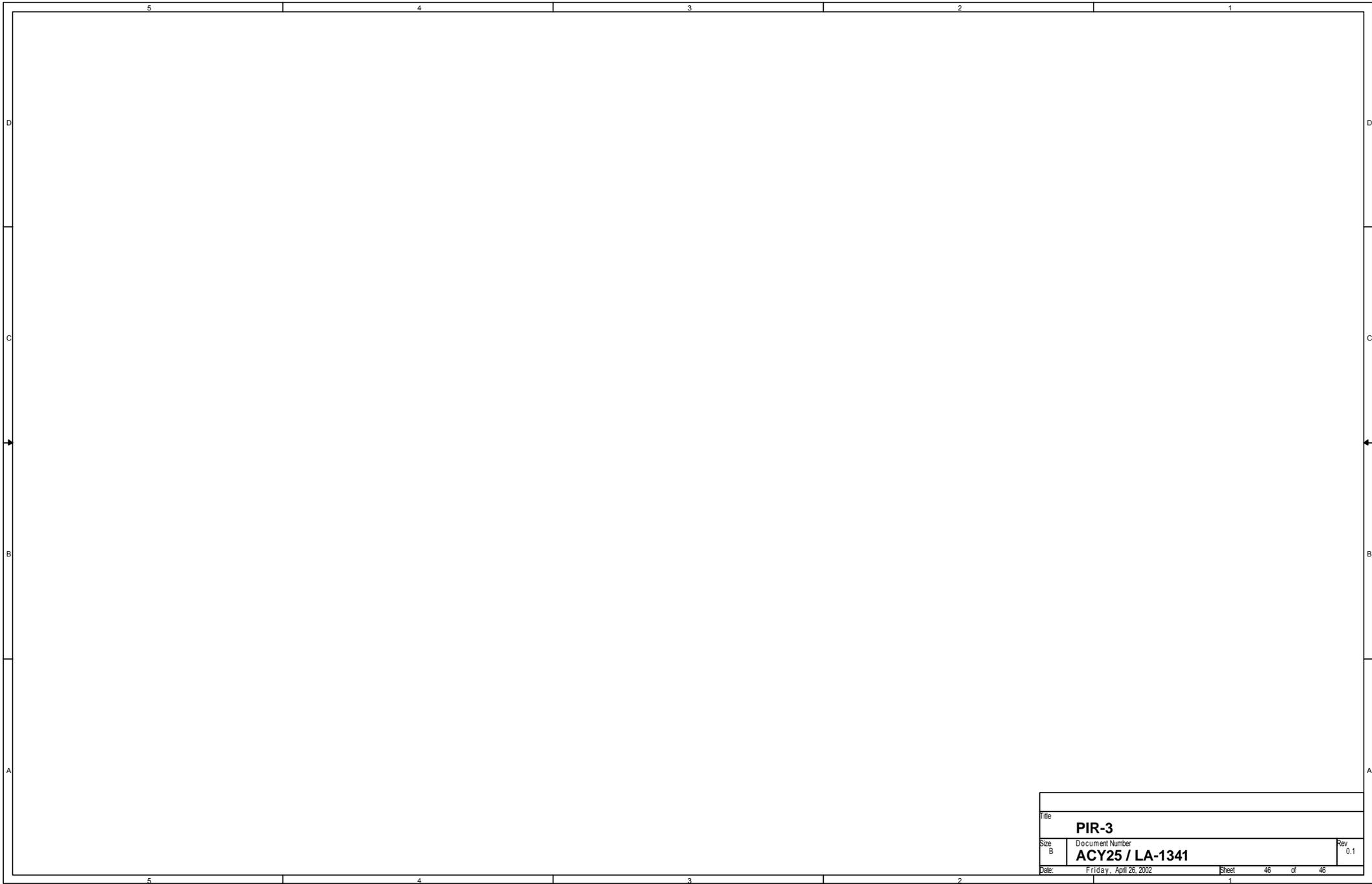
LAN\_DIS# : Del R333 , add D57 for reserve

MINI PCI : Change to REQ#4 & GNT#4

For MP 5/3

R248 change to 47K , R251 change to 15K

Title			
PIR-2			
Size	Document Number		Rev
B	ACY25 / LA-1341		0.1
Date	Friday, May 03, 2002	Sheet	45 of 46
		1	



Title			
<b>PIR-3</b>			
Size	Document Number	Rev.	
B	<b>ACY25 / LA-1341</b>	0.1	
Date:	Friday, April 26, 2002	Sheet	46 of 46