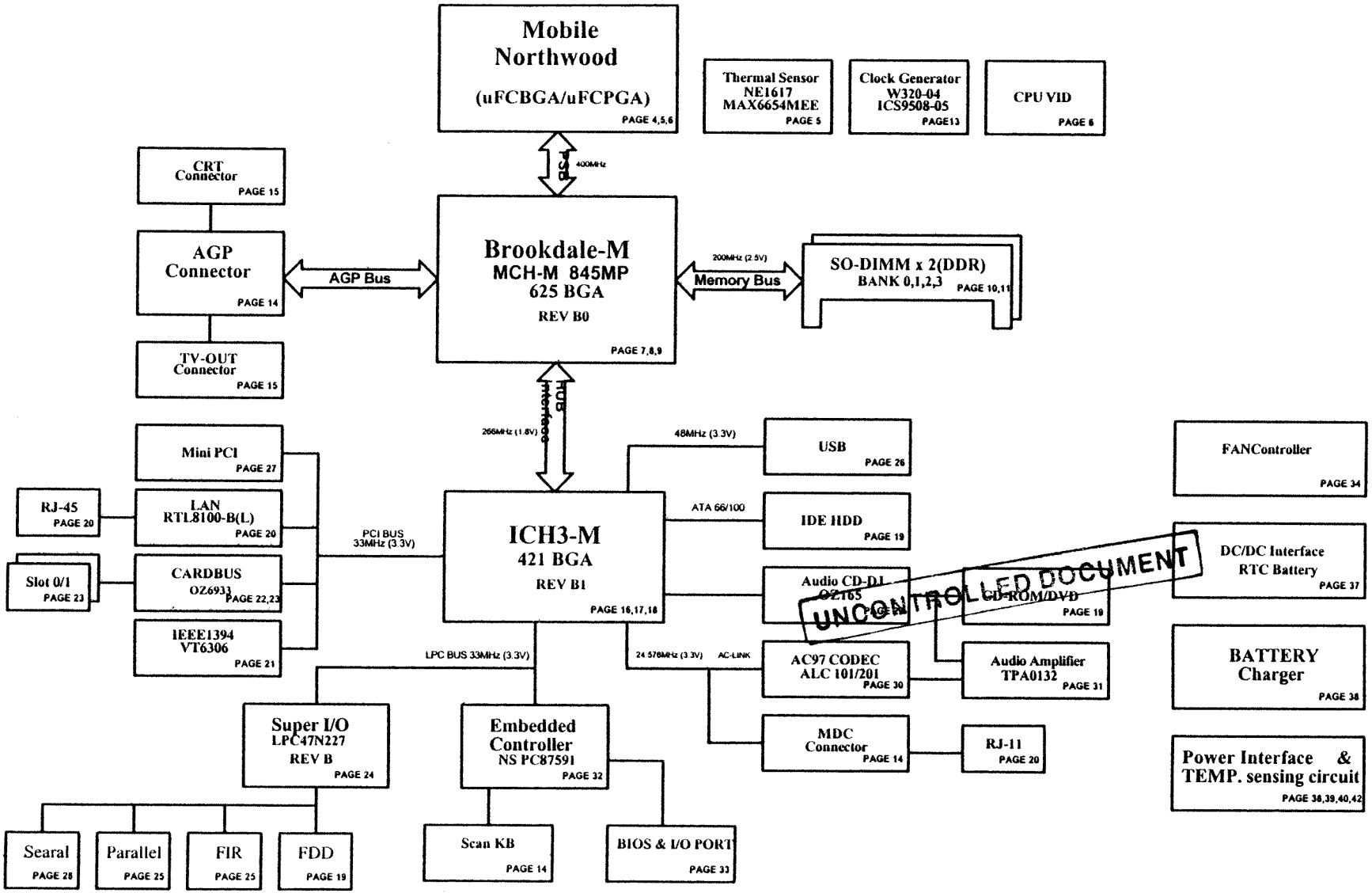
ACL10 LA-1331 BLOCK DIAGRAM



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
1.2VP	1.2VP switched power rail for CPU VID	ON	OFF	OFF
+1.25VS	1.25VS power rail	ON	OFF	OFF
+1.5VS	AGP 4X	ON	OFF	OFF
+1.8VALW	1.8V always power rail	ON	ON	ON*
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5V	2.5V power rail	ON	ON	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5V	5V power rail	ON	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
+12V	12V power rail	ON	ON	OFF
+12VS	12V switched power rail	ON	OFF	OFF
RTCVCC	RTC power	ON	ON	ON
+SDREF	+SDREF power	ON	ON	OFF

Note : "ON*" means that this power plane is "ON" only with AC power available, otherwise it is "OFF".

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
IEEE 1394	AD16	0	PIRQA
Mini-PCI	AD18	1/4	PIRQC/PIRQD
CardBus	AD20	2	PIRQA/PIRQB
LAN	AD17	3	PIRQB
SM	AD22	-	PIRQC/PIRQD

EC SM Bus1 address

Device	Address
Smart Battery	0001 011Xb
EEPROM(24C16/02) (24C04)	1010 000Xb 1011 000Xb

EC SM Bus2 address

Device	Address
MAX8654MEE	1001 110Xb
OZ165	1011 0100b (B4h)
Smart Battery	0001 011Xb
Docking	0011 011Xb
DOT Board	XXXX XXXXb

ICH3-M SM Bus address

Device	Address
Clock Generator W320-04 / ICS9508-05	1101 0000

DDR SODIMM SM Bus address

DDR SLOT	SA2	SA1	SA0
DDR SODIMM0 (REVERSE)	0	0	0
DDR SODIMM1 (NORMAL)	0	0	1

PIR

REV 0.1

Date	Page	Description
2001/12/29	7	Change R212,R214 & R213 to 8.2K ohm for Intel recommend.
2001/12/29	14	Stuff R361=22 Ohm and no-stuff R360 for Data-IN1 of MDC module.
2001/12/29	15	Change L26 & L29 to 0 Ohm for EMI issue.
2001/12/29	16	Change R39 power-plane to +3VALW for Resume-well Power-plane(+3VALW)
2001/12/29	17	DEL C73, C87, C371 for EMI issue.
2001/12/29	17	Change L37 power-plane to +1.8VS for Intel recommend.
2001/12/29	17	Change R279 power-plane to +3VS for Intel recommend.
2001/12/29	17	Change U29 pinV22,U18 & P14 power-plane to +CPU_CORE for Intel recommend.
2001/12/29	17	Change R284 power-plane to +3VALW for Intel recommend.
2001/12/29	18	Change "SMB_ALERT#" power-plane to +3VALW for "RESUME-WELL" power-plane(+3VLAW).
2001/12/29	18	Exchang D13,D14,D16,D17,D18 and R28,R34,R30,R29 to RP135,R466,R468 for cost-down.
2001/12/29	20	Add D43 for leakage.
2001/12/29	21	Exchang L42 to L52,L53, L54, L55 for ME limitation.
2001/12/29	27	Add D42 for leakage.
2001/12/29	31	Add R465 for PC99 Spec.
2001/12/29	34	Add C368, C369 for EMI solution.
2001/12/29	35	EC control "EC_RSMRST#". ->DEL R92, Stuff R48.
2001/12/29	35	Change R97 to 100K for "VGATE" of Max1718A issue.-> Change PR134= 0 Ohm.
2002/01/07	39	Change PR88 from 10k_1% to 10.5k_1% (increase 5valwp to 5.125v).
2002/01/07	40	Change PR81 from 2.15k_1% to 1.87k_1% (CPU thermal OTP from 83+-3C to 85+-3C).
2002/01/07	42	Add PR147, PR161 to 2.7_0805. for EMI requirement.
2002/01/07	42	Add PC120, PC121, PC122 to 1000pf. for ESD.
2002/01/07	42	Add PQ44 to 2N7002 for CPU SPEED STEP.
2002/01/07	42	Change PR130, PR152 from 0 to 2.2. for EMI requirement.
2002/01/07	42	Change PR143 from 53.6k_1% to 100k_1% for CPU OCP.
2002/01/07	42	Change PR145 from 100k_1% to 53.6k_1% for CPU OCP.
2002/01/07	42	Change PR148 from 30k_1% to 46.7k_1% for CPU OCP.
2002/01/07	42	Change PU12 VIN from +2.5VP to +3VALWP.

REV 0.2

Date	Page	Description
2002/01/11	40	Change PH1 and PH2 design by high active for AC-IN issue.

REV 0.3

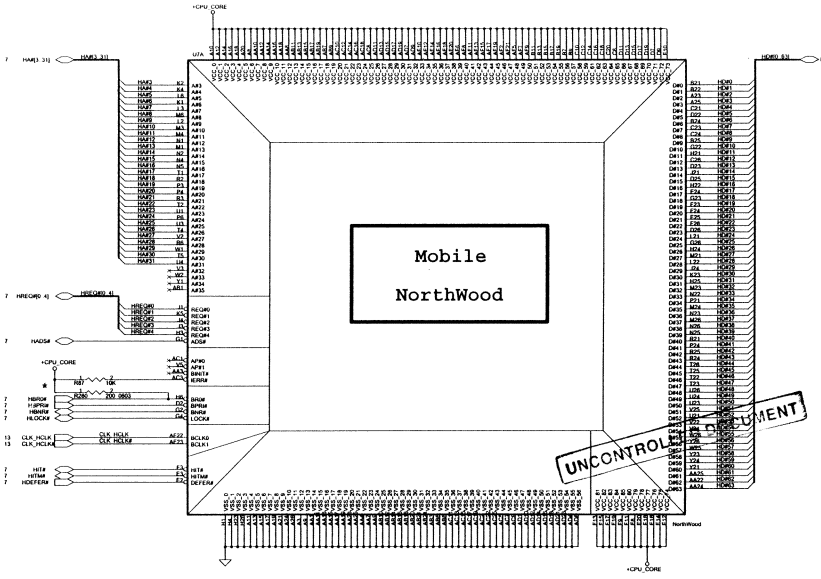
Date	Page	Description
None		

REV 1.0

Date	Page
None	

REV 2.0

Date	Page	
2002/04/10	20	GCR: (For LAN issue) <1>Isolation U18 pin5 for Realtek application notice. <2>Change R204 from 5.9K+-1% to 5.6K +-1%. <3>Change L23 from 4.7UH to 0 ohm.



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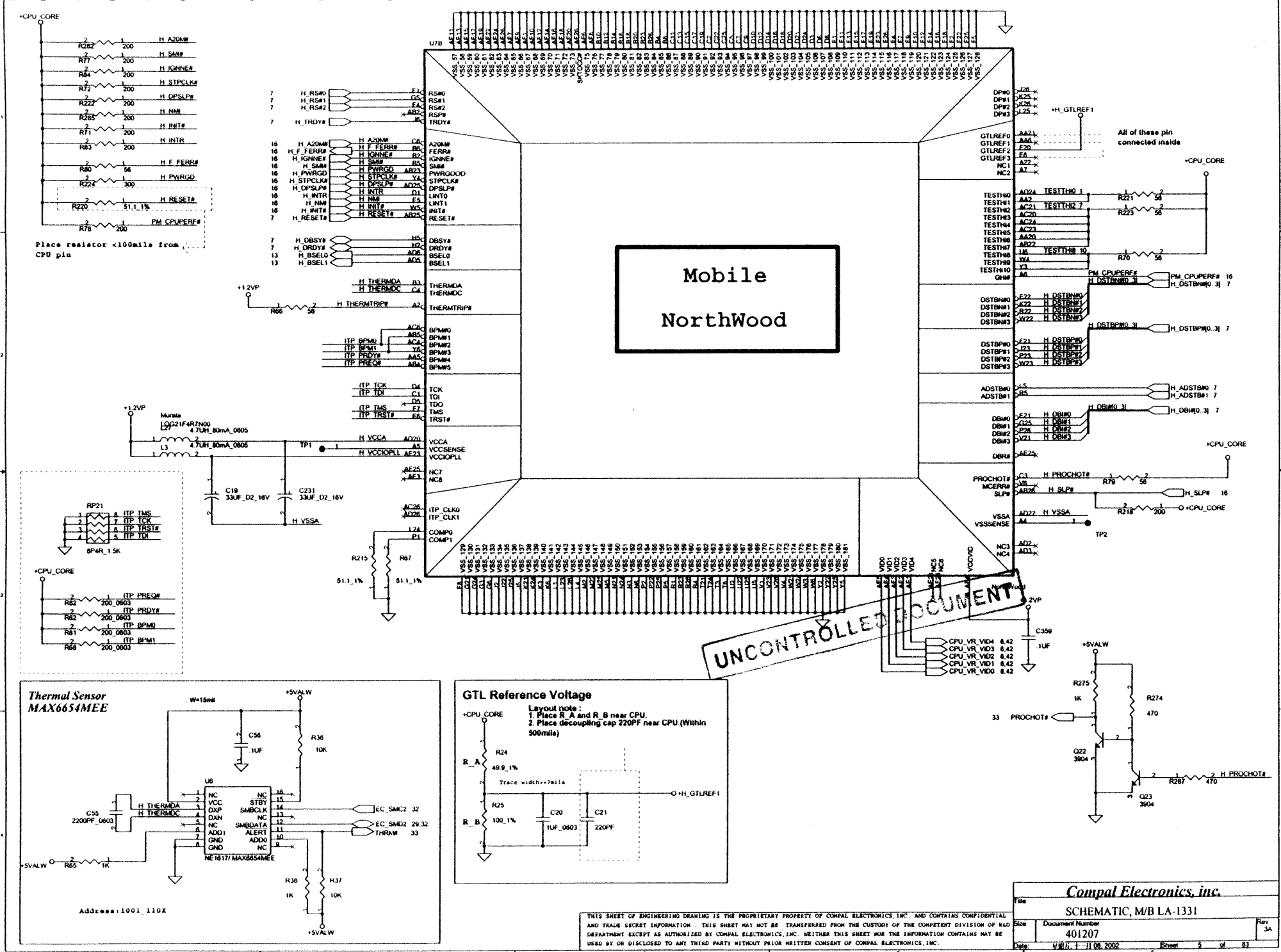
Mobile
NorthWood
U7B
All of these pin connected inside
Place resistor <100mils from CPU pin
UNCONTROLLED DOCUMENT
Thermal Sensor
MAX6654MEE
GTL Reference Voltage
Layout note :
1. Place R_A and R_B near CPU.
2. Place decoupling cap 220PF near CPU.(Within 500mils)
Address:1001_110X
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SCHEMATIC, M/B LA-1331
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401207
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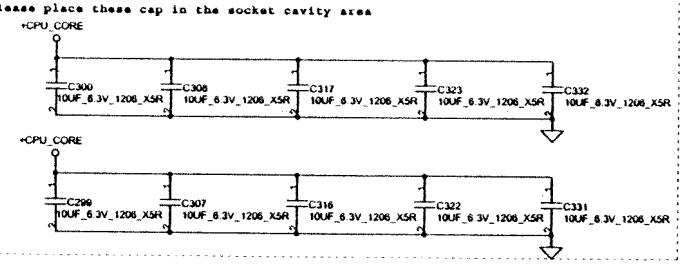
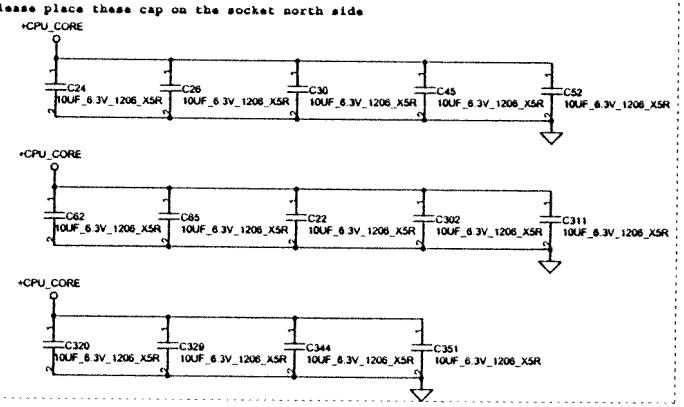
Layout note :

Place close to CPU, Use 2~3 vias per PAD.
Place .22uF caps underneath balls on solder side.
Place 10uF caps on the peripheral near balls.
Use 2~3 vias per PAD.

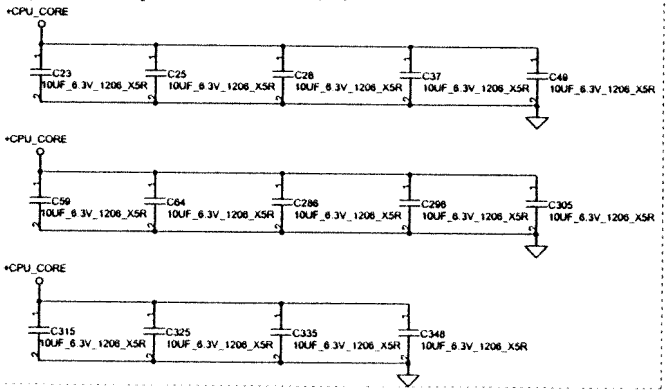
Please place these cap in the socket cavity area



Please place these cap on the socket north side



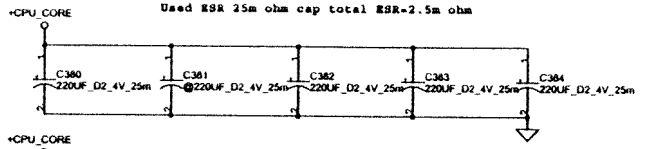
Please place these cap on the socket south side

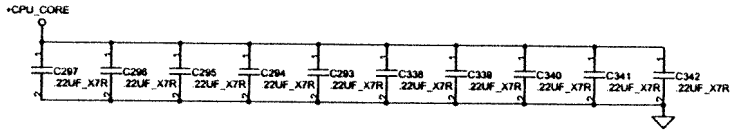


Layout note :

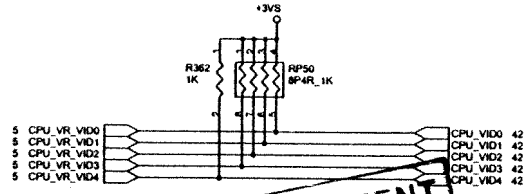
Place close to CPU power and ground pin as possible (<1inch)

Used ESR 25m ohm cap total ESR=2.5m ohm

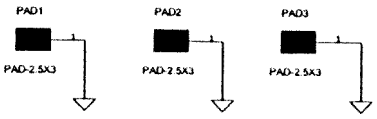




CPU Voltage ID



EMI Clip PAD for CPU



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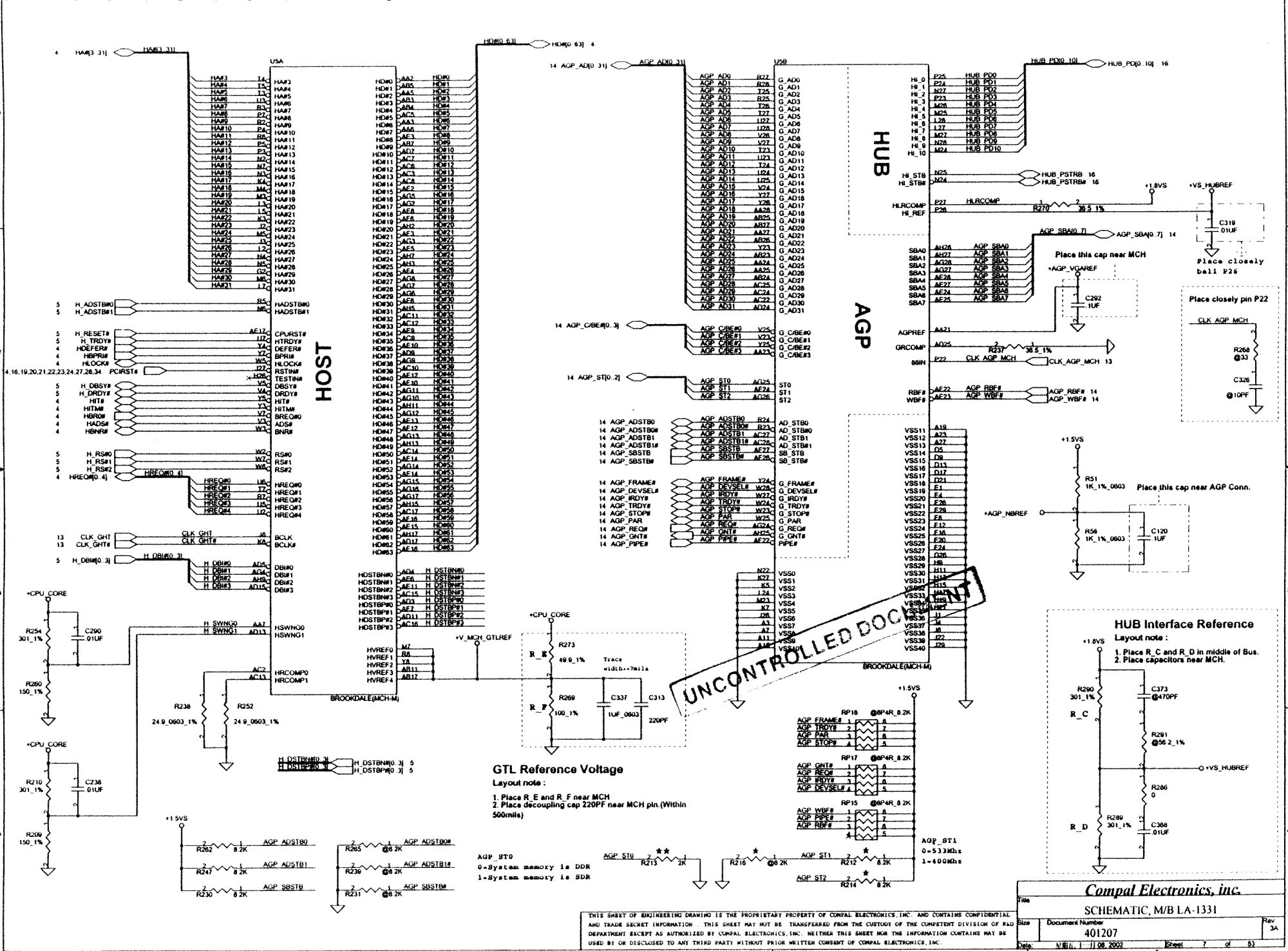
HOST
AGP
HUB
BROOKDALE(MCH-M)
GTL Reference Voltage
Layout note :
1. Place R_E and R_F near MCH
2. Place decoupling cap 220PF near MCH pin.(Within 500mils)
HUB Interface Reference
Layout note :
1. Place R_C and R_D in middle of Bus.
2. Place capacitors near MCH.
Place this cap near MCH
Place closely pin P22
Place this cap near AGP Conn.
Place closely ball P26
UNCONTROLLED DOCUMENT
AGP_ST0
0=System memory is DDR
1=System memory is SDR
AGP_ST1
0=533Mhz
1=400Mhz
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401207
Rev 3A
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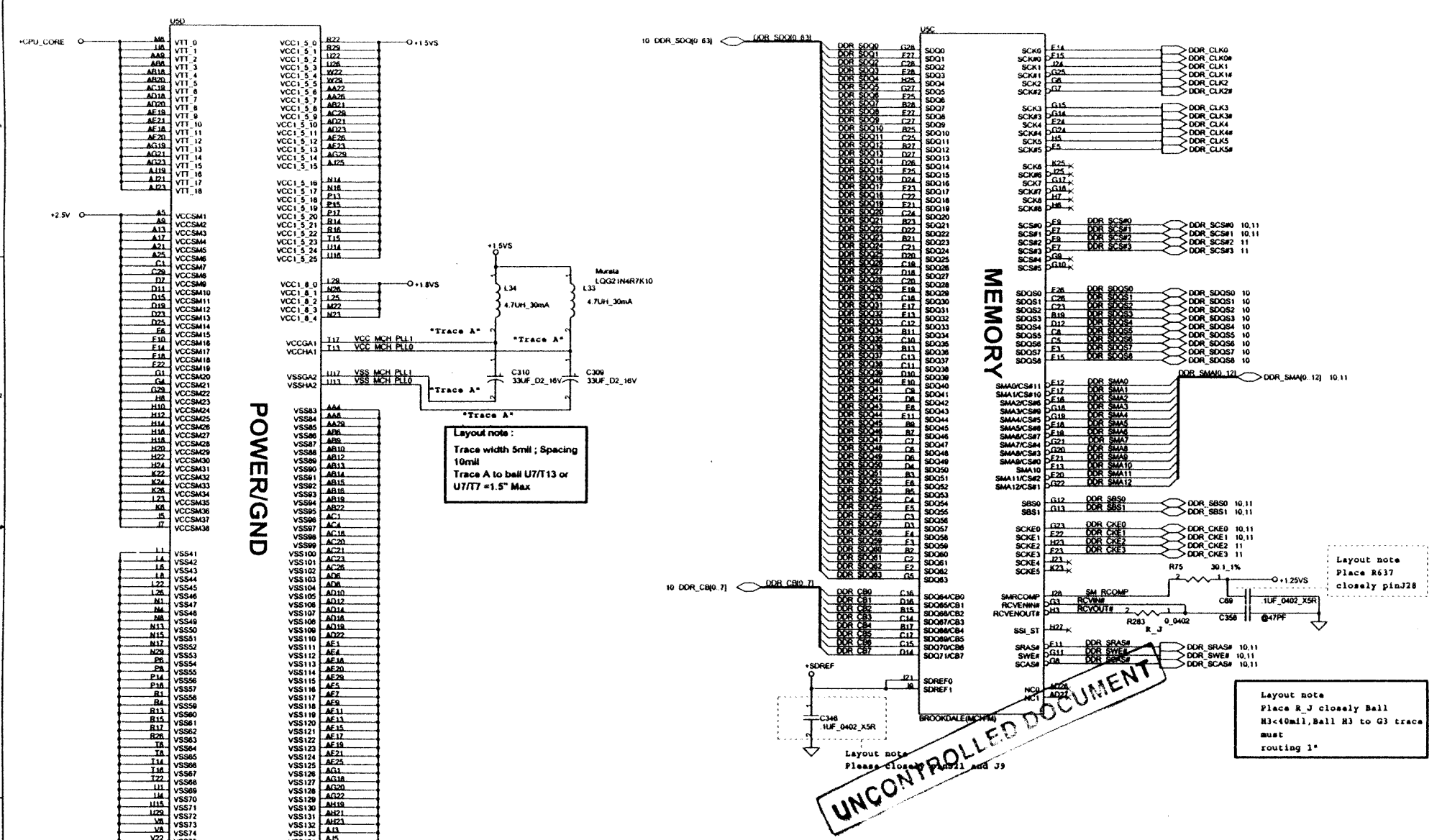

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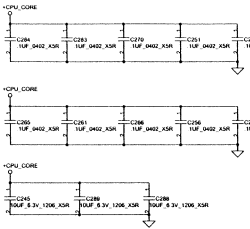
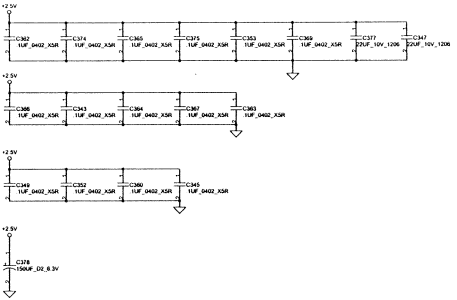
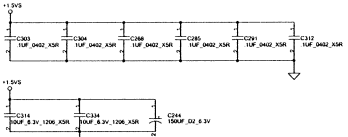
Layout note : Processor system bus
Distribute as close as possible to MCH Processor Quadrant.(between VTTFSB and VSS pin)



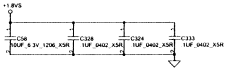
Layout note : DDR Memory interface
Distribute as close as possible to MCH Processor Quadrant (between VCCSM and VSS pin)



Layout note : AGP/CORE
Distribute as close as possible to MCH Processor Quadrant.(between VCCAGP/VCCCORE and VSS pin)



Layout note : Hub-Link
Distribute as close as possible to MCH Processor Quadrant.(between VCCHL and VSS pin)



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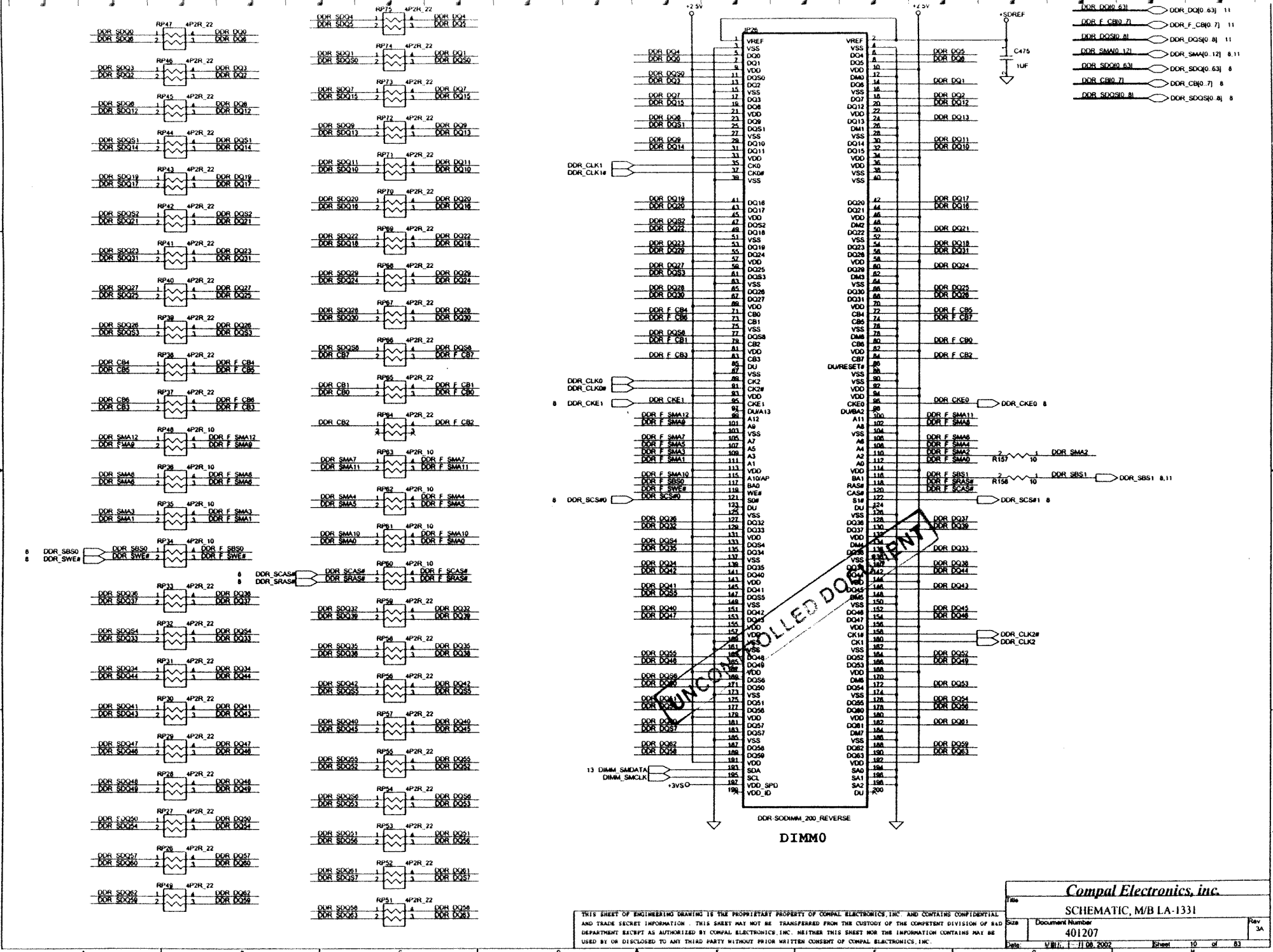

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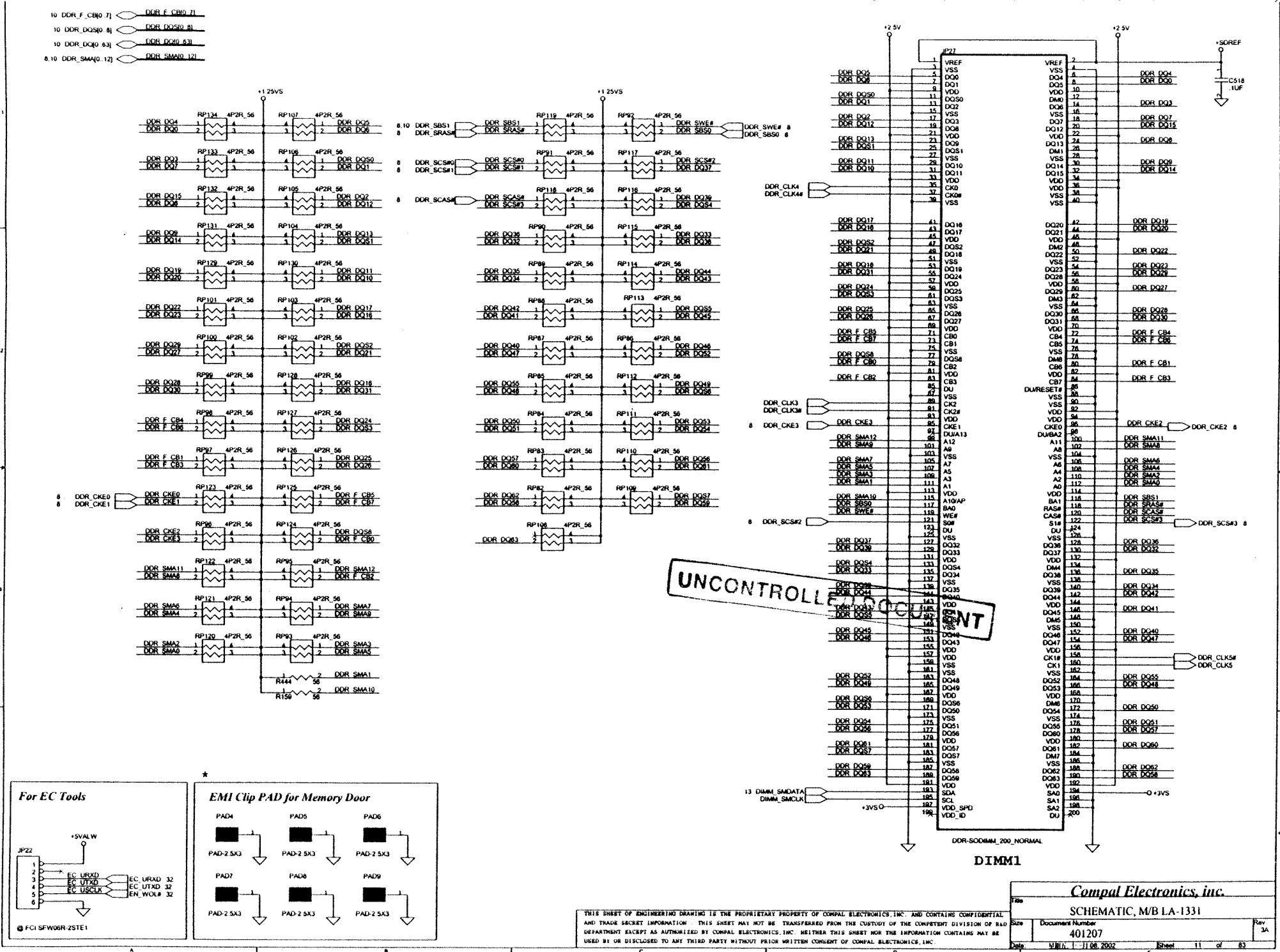
10 DDR_F_CB[0..7]
DDR_F_CB[0..7]
10 DDR_DQS[0..8]
DDR_DQS[0..8]
10 DDR_DQ[0..63]
DDR_DQ[0..63]
8,10 DDR_SMA[0..12]
DDR_SMA[0..12]
+1.25VS
+2.5V
+SOREF
C518
.1UF
JP27
DDR-SODIMM_200_NORMAL
DIMM1
UNCONTROLLED DOCUMENT
For EC Tools
+5VALW
JP22
EC_URXD
EC_UTXD
EC_USCLK
EC_URXD 32
EC_UTXD 32
EN_WOL# 32
FCI SFW06R-2STE1
EMI Clip PAD for Memory Door
PAD4
PAD5
PAD6
PAD7
PAD8
PAD9
PAD-2.5X3
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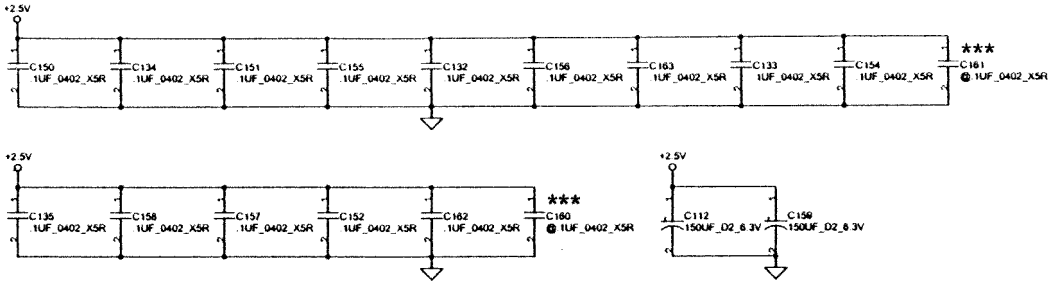
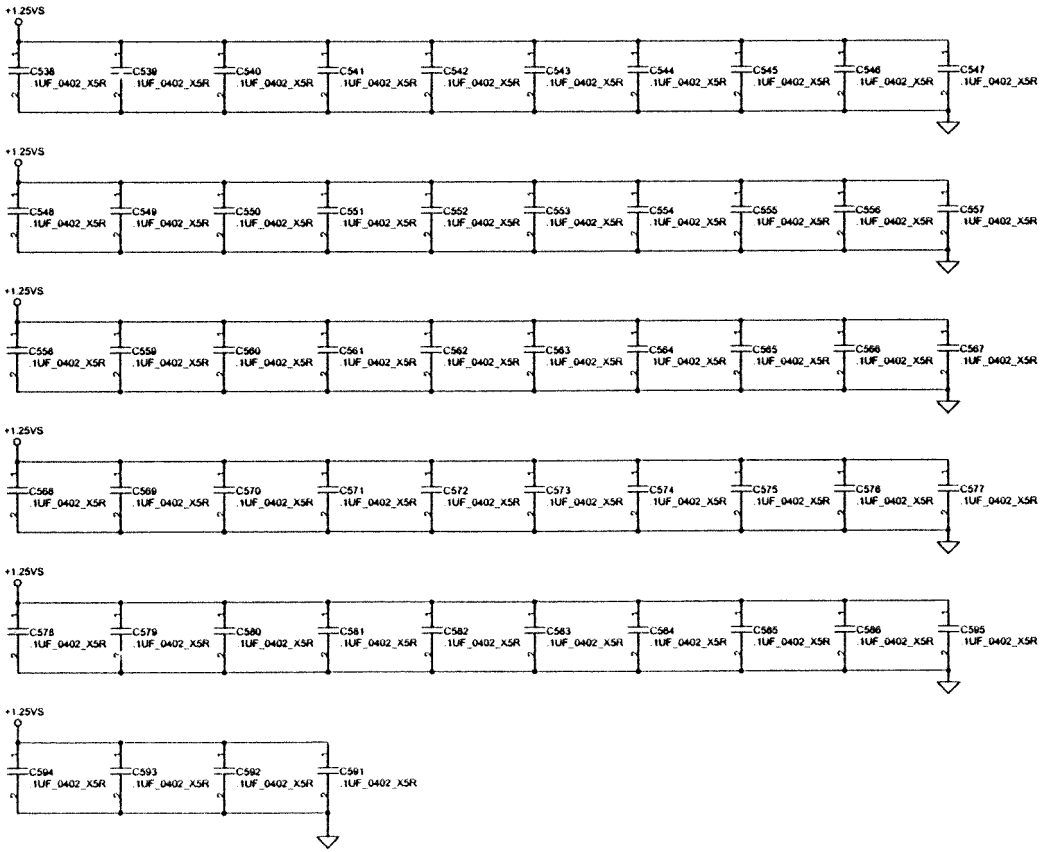
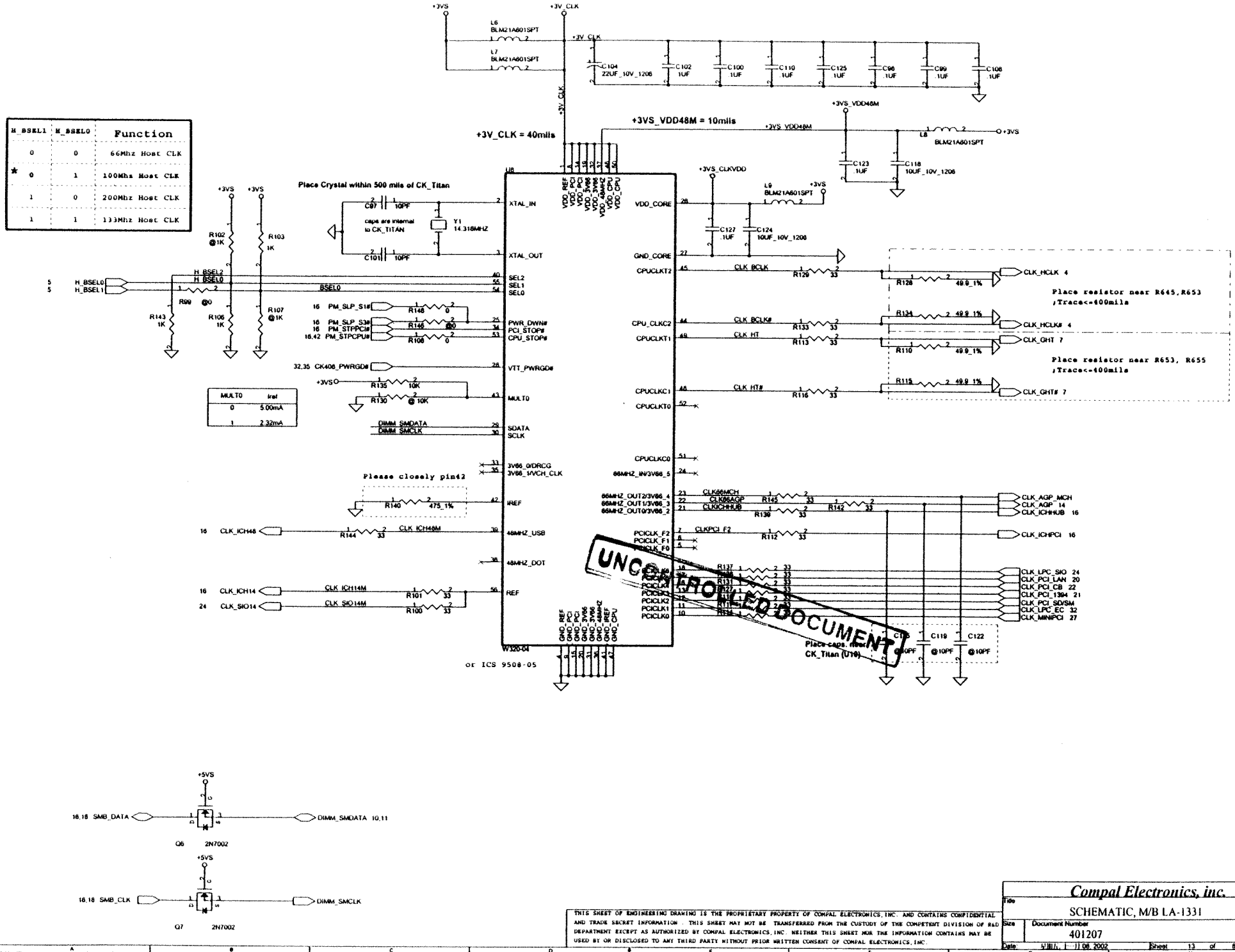
Layout note :
Distribute as close as possible to DDR-SODIMM.



Layout note :
Place one cap close to every 2 pull up resistors termination to +1.25V





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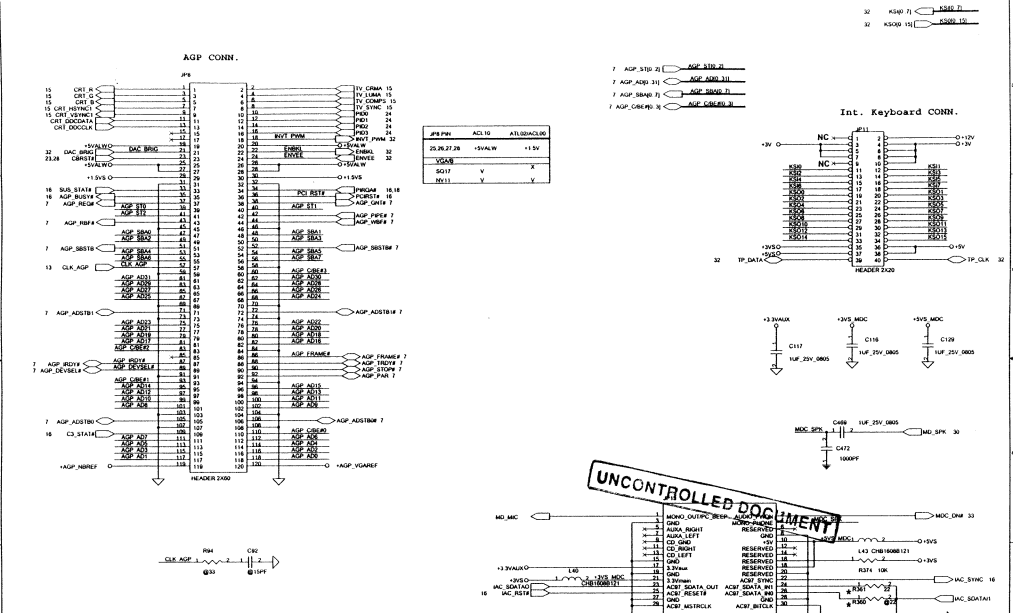
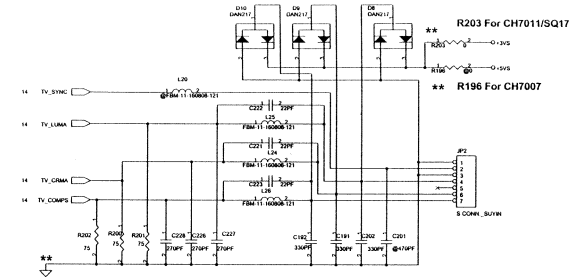
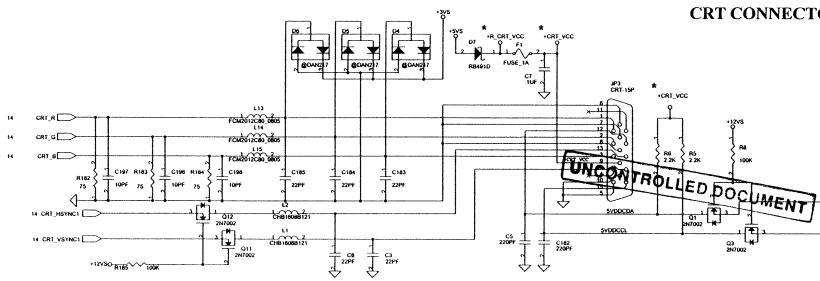


JP6 P/N	ACL10	ATL02/ACL00
25,26,27,28	+5VALW	+1.5V
VGA/B		
SG17	V	X
INV11	V	Y





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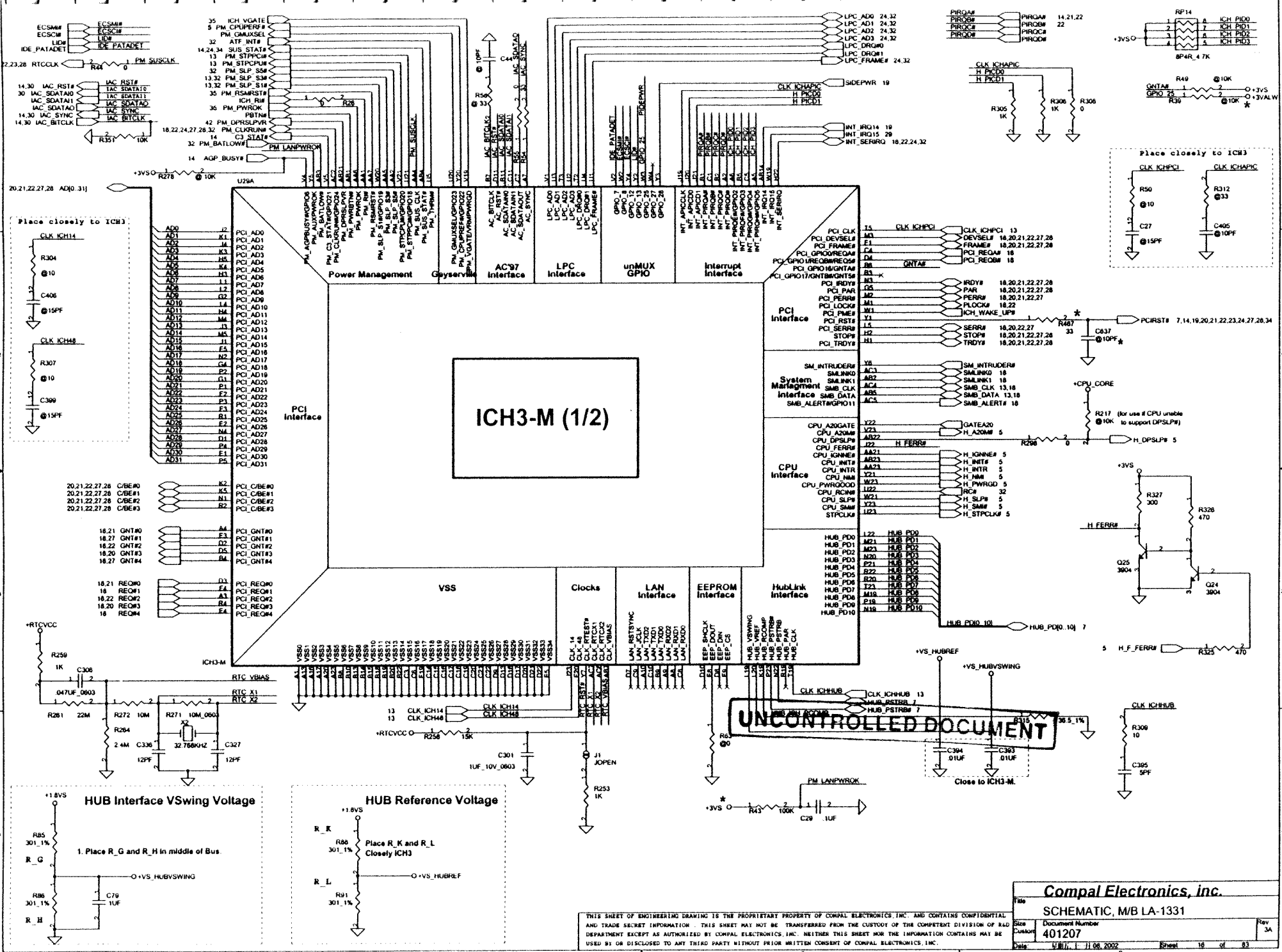

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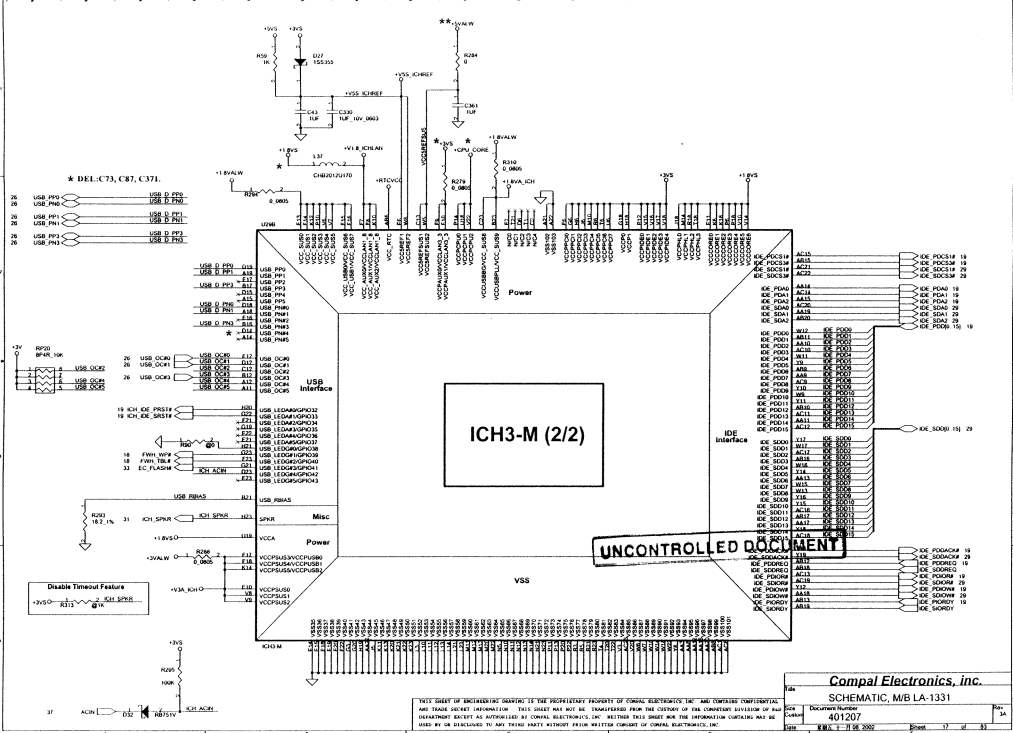

Compal Electronics, Inc.	
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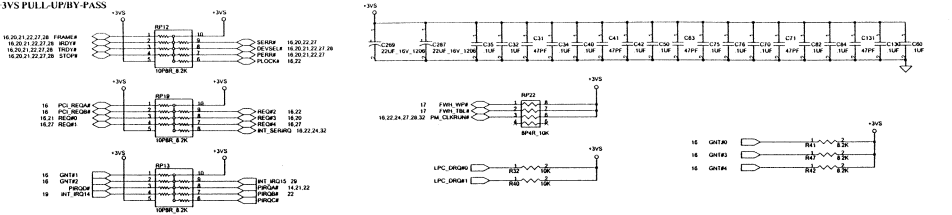
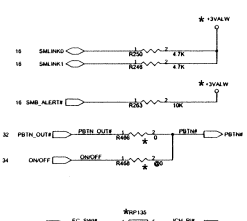
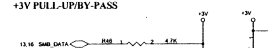
+3VS PULL-UP/BY-PASS

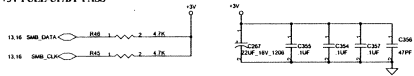


+3VALW PULL-UP

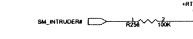




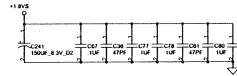
+3V PULL-UP/BY-PASS



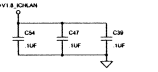
+RTCVCC PULL-UP



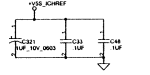
+1.8SV BY-PASS



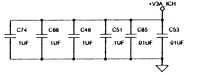
+V1.8S_ICHLAN BY-PASS



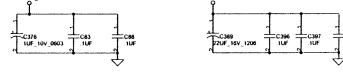
+V5S_ICHREF BY-PASS



+V3A_ICH BY-PASS



+V3A_ICH BY-PASS



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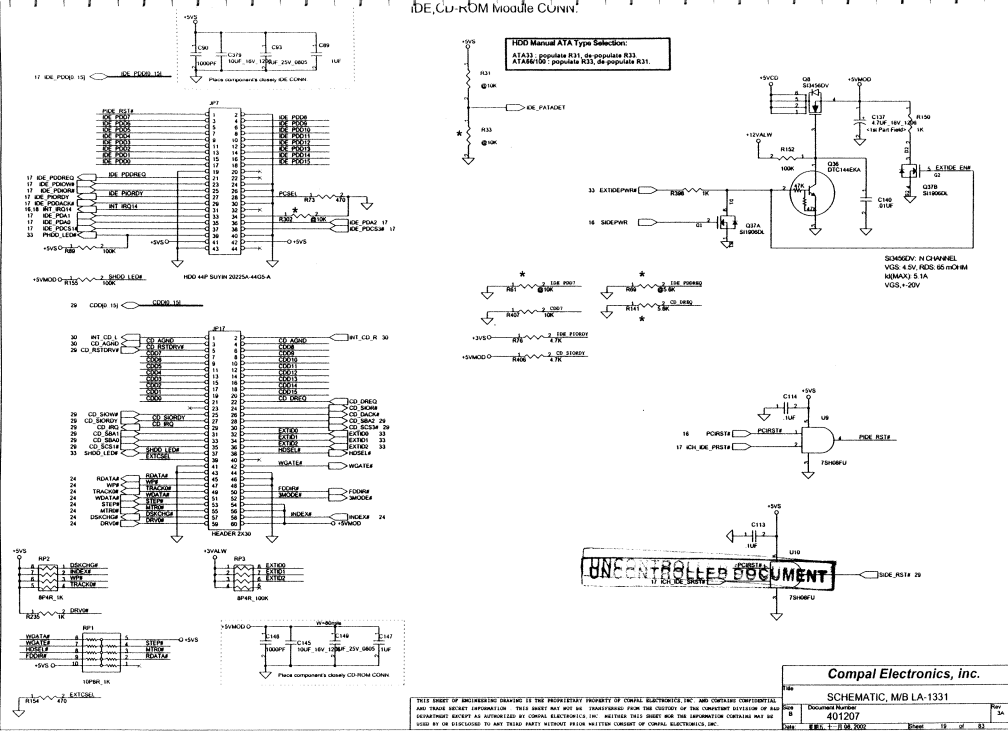

Compal Electronics, Inc.			
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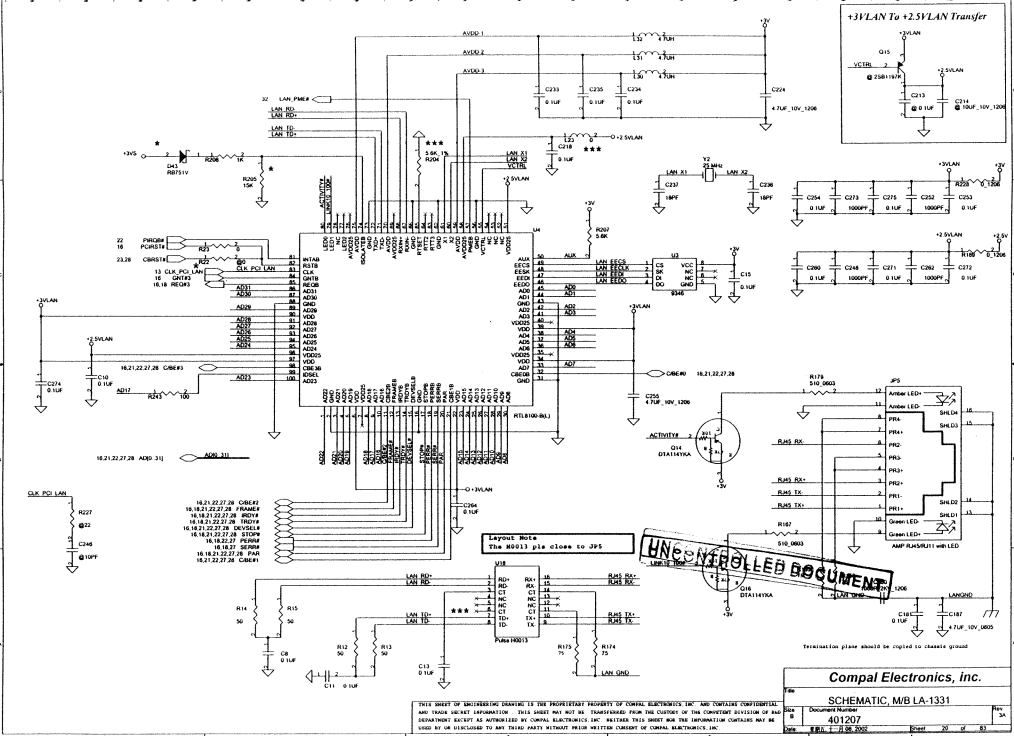
+3VLAN To +2.5VLAN Transfer
Layout Note
Place Q13 close to JP5
UNCONTROLLED DOCUMENT
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401207
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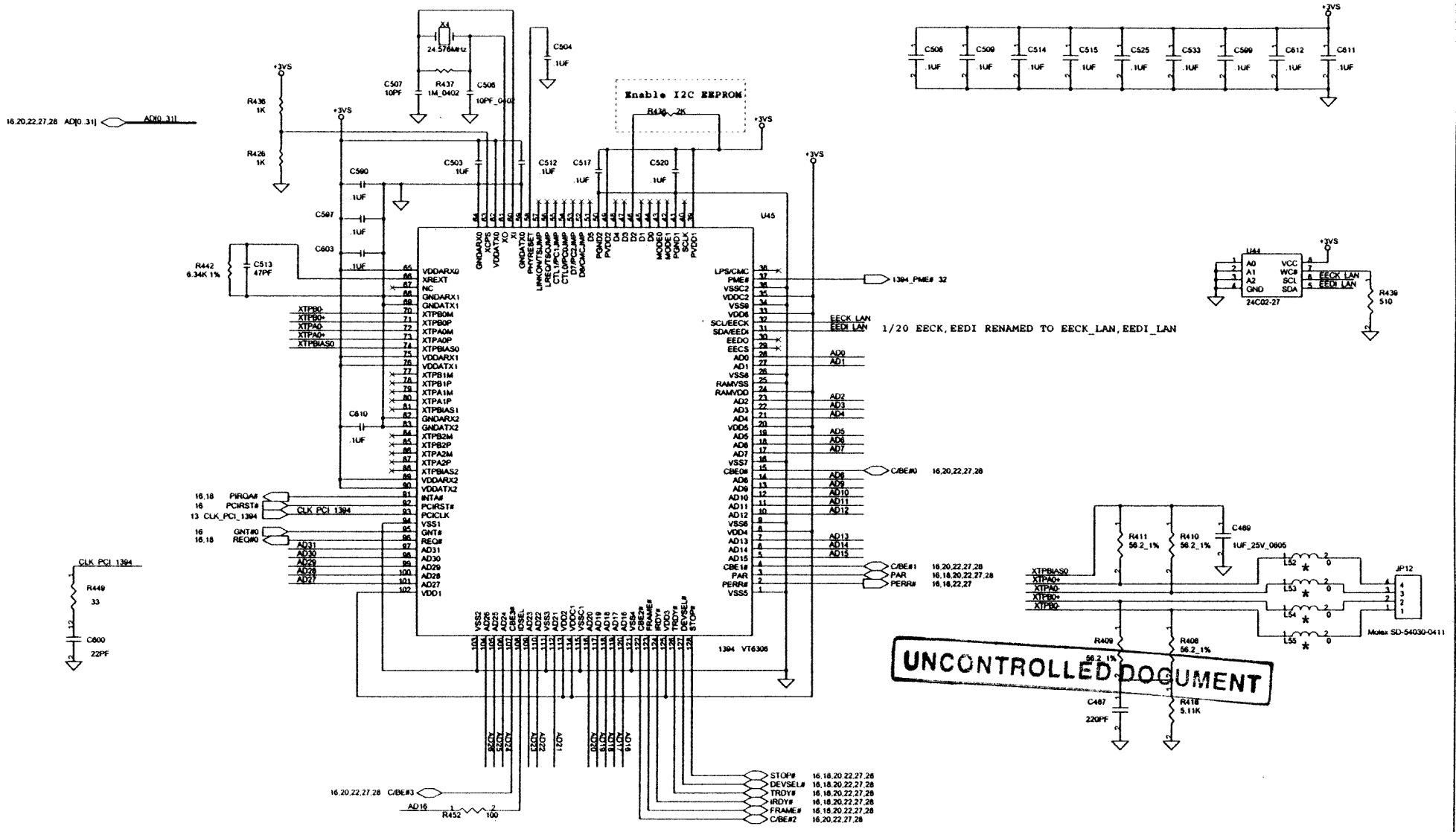
Pulse H0013
RTL8100-B(L)
ACTIVITY#
AMP RJ45/RJ11 with LED
Termination plane should be copied to chassis ground



@X3

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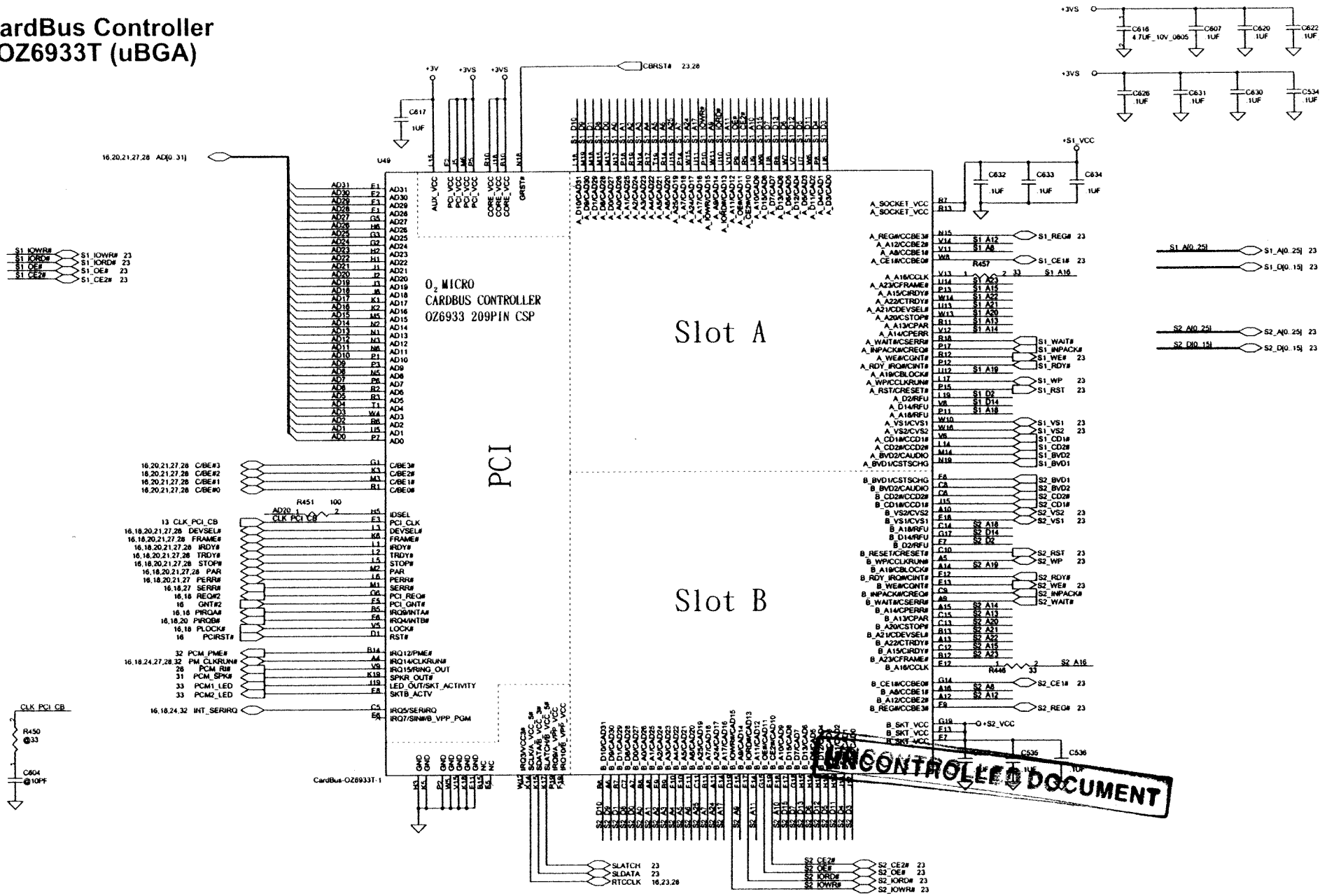
CardBus Controller
OZ6933T (uBGA)



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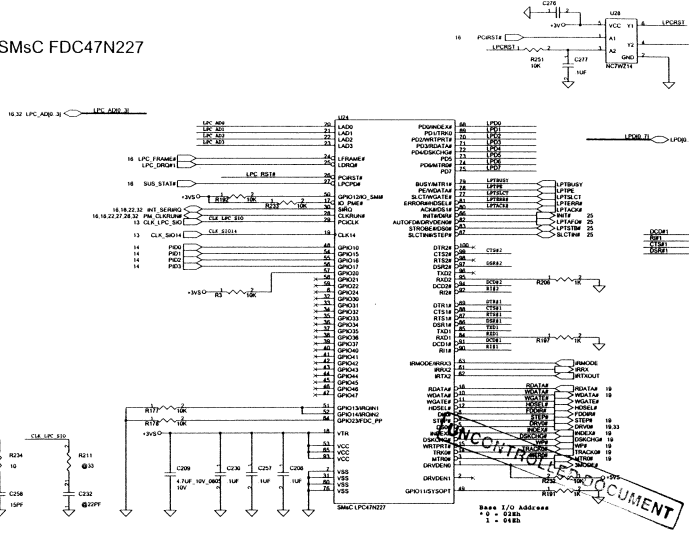
SUPER I/O SMsC FDC47N227



Compal Electronics, inc.

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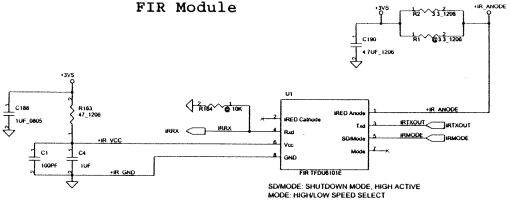
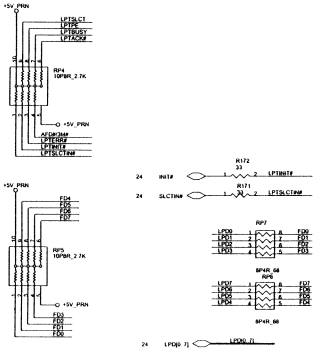
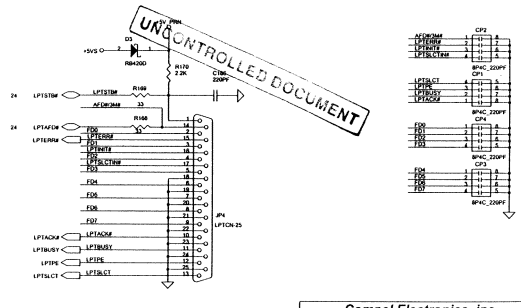
FIR Module



SD/MODE: SHUTDOWN MODE, HIGH ACTIVE
MODE: HIGH/LOW SPEED SELECT



PARALLEL PORT



Compal Electronics, inc.

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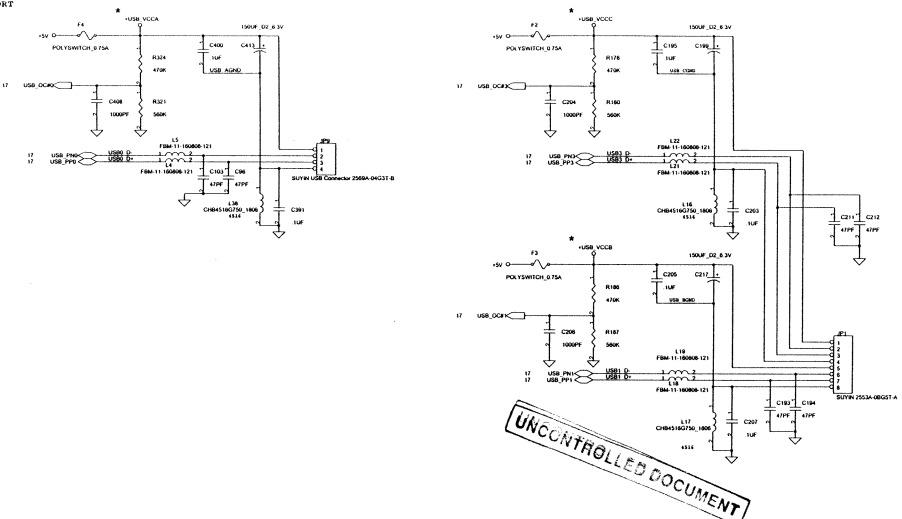
USB PORT



Compal Electronics, Inc.

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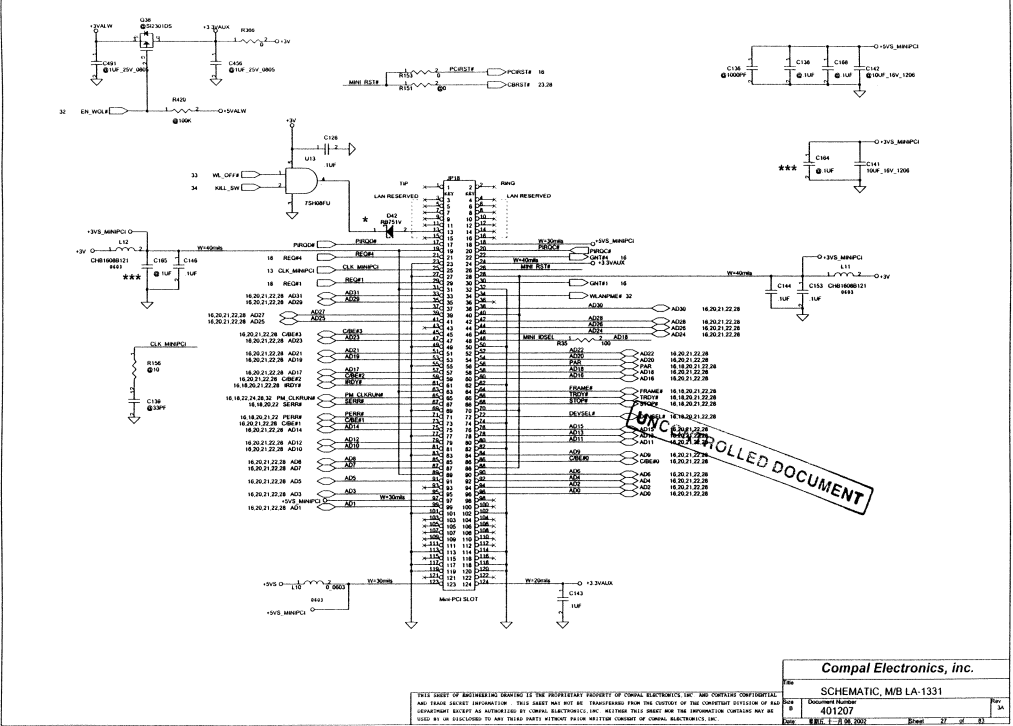

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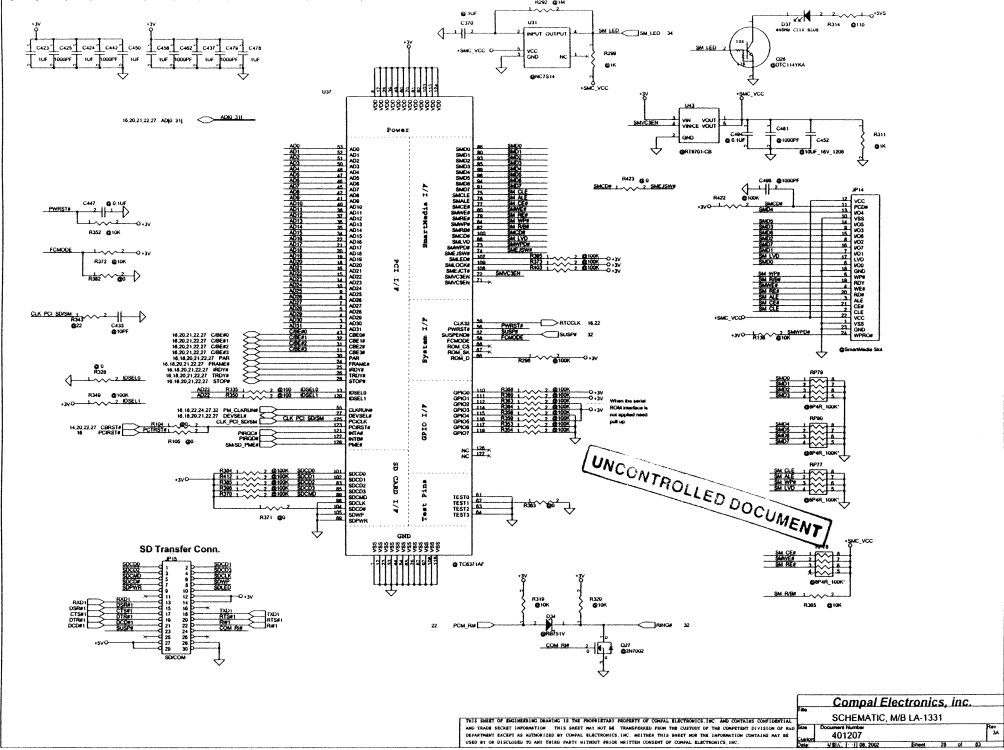
Powise
Intel Brookdale 1/7
A/D 1/4
System 2/7
GPIO 1/7
SD GPIO 1/7
Test Pins
U37
U31
U53
U52
U54
U55
U56
U57
U58
U59
U60
U61
U62
U63
U64
U65
U66
U67
U68
U69
U70
U71
U72
U73
U74
U75
U76
U77
U78
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U80
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U83
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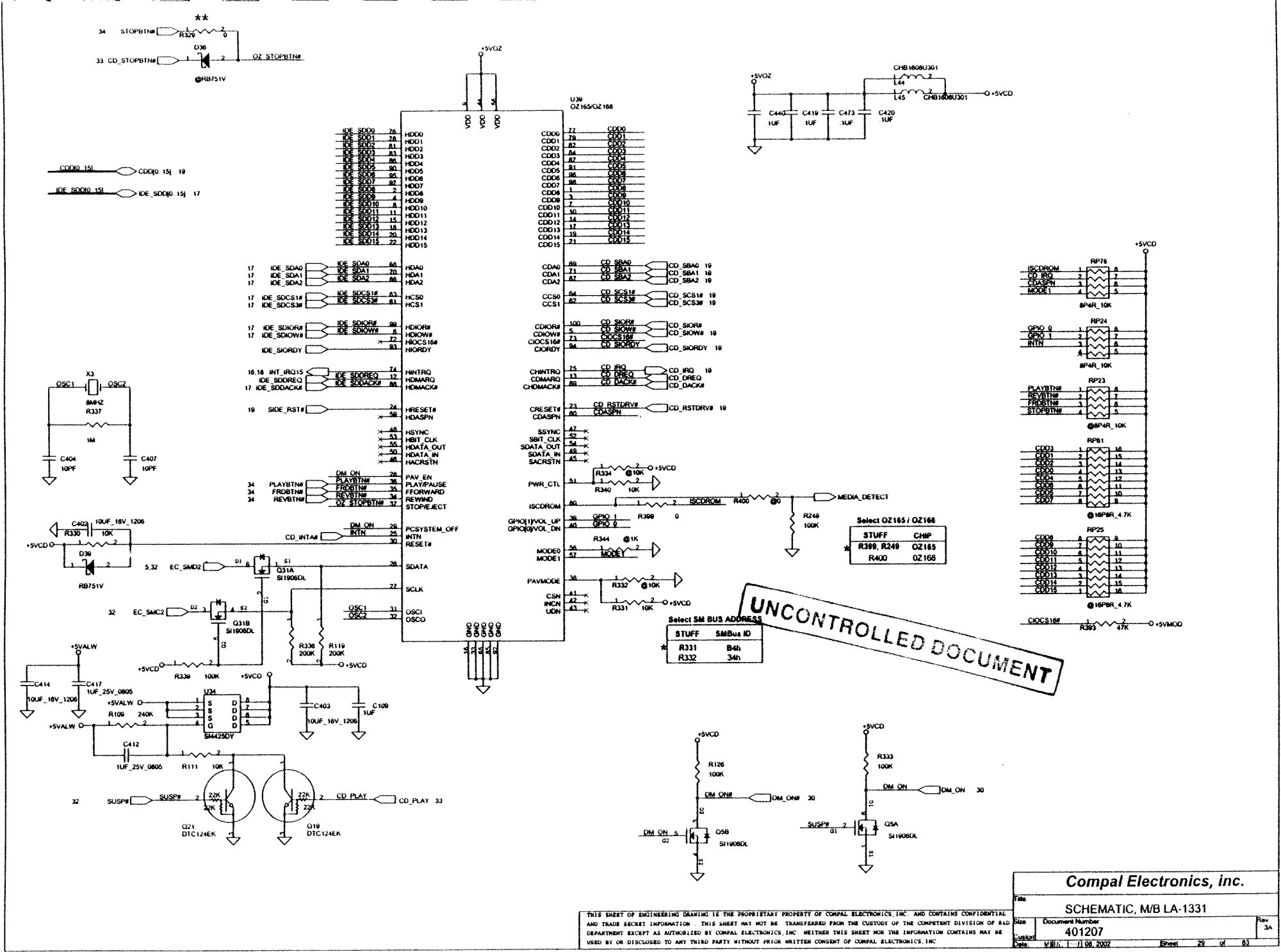
U89
U90
U91
U92
U93


STOPBTN#
CD_STOPBTN#
OZ_STOPBTN#
RB751V
+5VOZ
U39
OZ165/OZ166
CDD[0..15]
IDE_SDD[0..15]
HDD0
HDD1
HDD2
HDD3
HDD4
HDD5
HDD6
HDD7
HDD8
HDD9
HDD10
HDD11
HDD12
HDD13
HDD14
HDD15
IDE_SDA0
IDE_SDA1
IDE_SDA2
IDE_SDCS1#
IDE_SDCS3#
IDE_SDIOR#
IDE_SDIOW#
IDE_SIORDY
INT_IRQ15
IDE_SDDREQ
IDE_SDDACK#
SIDE_RST#
HSYNC
HBIT_CLK
HDATA_OUT
HDATA_IN
HACRSTN
PLAYBTN#
FRDBTN#
REVBTN#
OZ_STOPBTN#
PAV_EN
PLAY/PAUSE
FFORWARD
REWIND
STOP/EJECT
PCSYSTEM_OFF
CD_INTA#
INTN
RESET#
EC_SMD2
EC_SMC2
SDATA
SCLK
OSCI
OSCO
X3
8MHZ
R337
1M
C404
10PF
C407
10PF
C402
10UF_16V_1206
R330
10K
D39
RB751V
Q31A
SI1906DL
Q31B
SI1906DL
R336
200K
R119
200K
R339
100K
C414
10UF_16V_1206
C417
1UF_25V_0805
U34
SI4425DY
R109
240K
C412
1UF_25V_0805
R111
10K
C403
10UF_16V_1206
C109
1UF
SUSP#
Q21
DTC124EK
Q19
DTC124EK
CD_PLAY
CHB1608U301
C440
1UF
C419
1UF
C473
.1UF
C420
1UF
R334
@10K
R340
10K
PWR_CTL
ISCDROM
R400
@0
MEDIA_DETECT
R249
100K
GPIO[1]/VOL_UP
GPIO[0]/VOL_DN
GPIO_1
GPIO_0
R399
0
R344
@1K
MODE0
MODE1
PAVMODE
R332
@10K
R331
10K
CSN
INCN
UDN
Select OZ165 / OZ166
STUFF
CHIP
R399, R249
OZ165
R400
OZ168
Select SM BUS ADDRESS
STUFF
SMBus ID
R331
B4h
R332
34h
UNCONTROLLED DOCUMENT
R126
100K
DM_ON#
DM_ON
Q5B
SI1906DL
R333
100K
Q5A
SI1906DL
RP78
ISCDROM
CD_IRQ
CDASPN
MODE1
8P4R_10K
RP24
GPIO_0
GPIO_1
INTN
8P4R_10K
RP23
PLAYBTN#
REVBTN#
FRDBTN#
STOPBTN#
@8P4R_10K
RP81
CDD3
CDD1
CDD2
CDD0
CDD4
CDD6
CDD5
CDD7
@16P8R_4.7K
RP25
CDD8
CDD9
CDD10
CDD11
CDD12
CDD13
CDD14
CDD15
@16P8R_4.7K
CIOCS16#
R393
47K
+5VMOD
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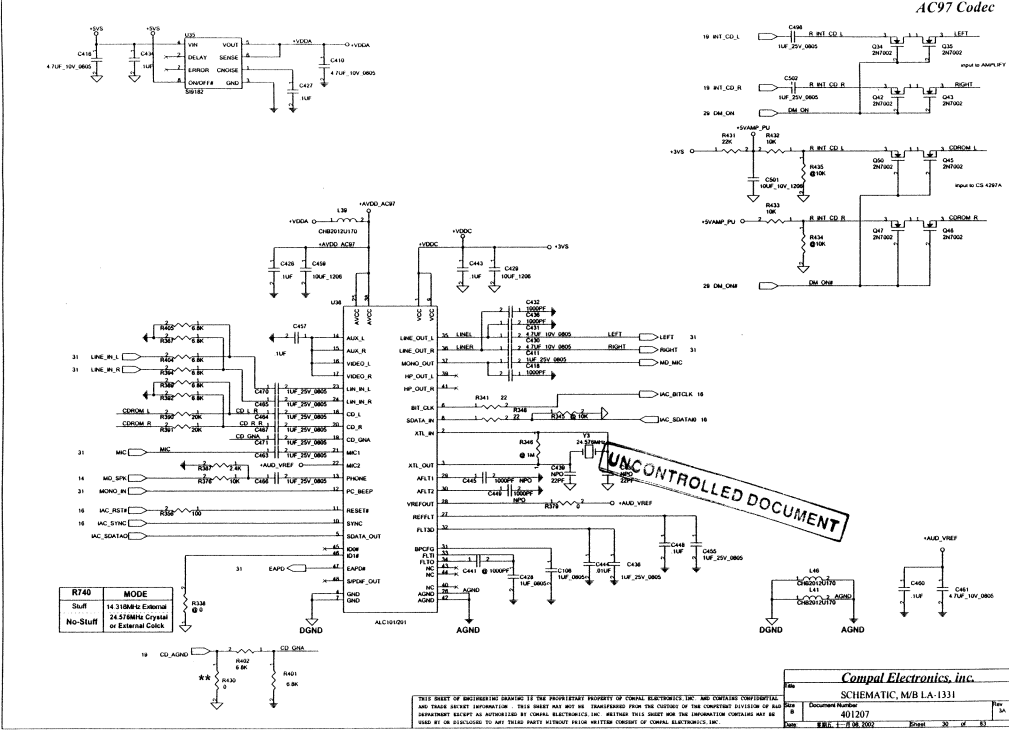

R740	MODE
Stuff	14.318MHz External
No-Stuff	24.576MHz Crystal or External Colck

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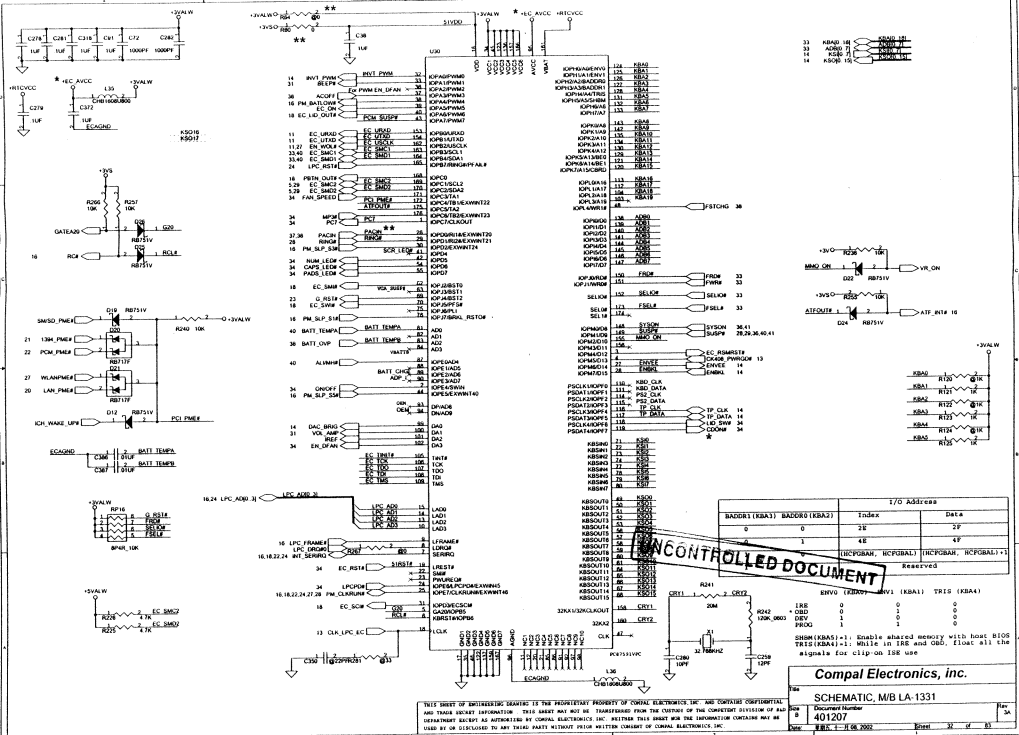
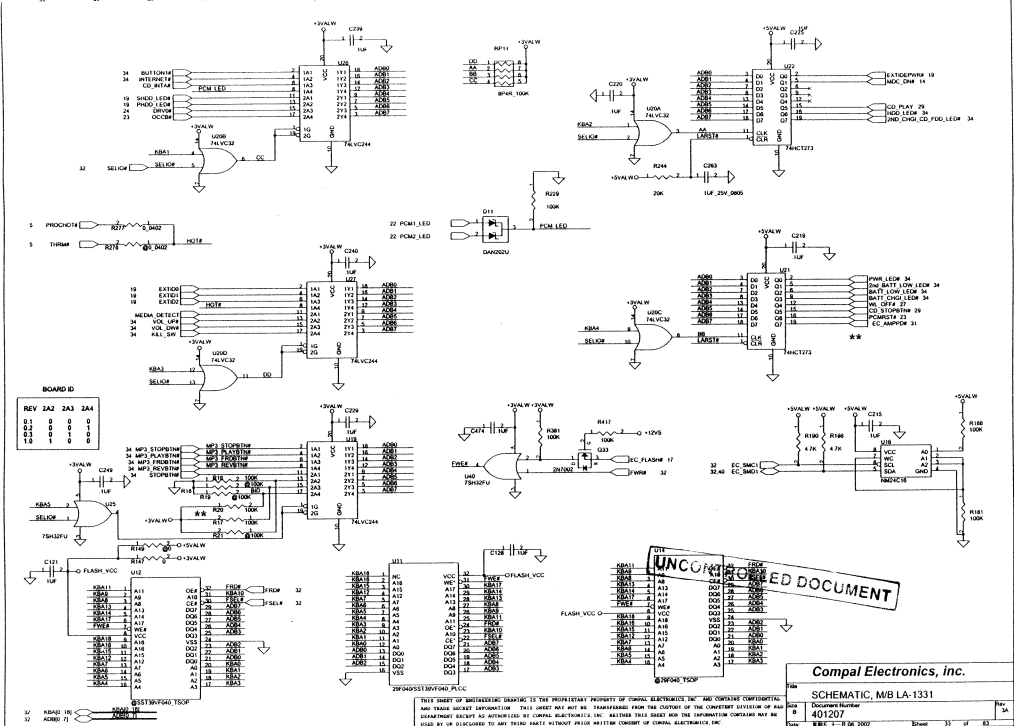

+3VALW
+3VSO
+RTCVCC
+EC_AVCC
+5VDU
+5V
U30
KSO16
KSO17
KBA0
KBA1
KBA2
KBA3
KBA4
KBA5
KBA6
KBA7
KSO0
KSO1
KSO2
KSO3
KSO4
KSO5
KSO6
KSO7
KSO8
KSO9
KSO10
KSO11
KSO12
KSO13
KSO14
KSO15
KBA0 16
KBA1 17
KBA2 18
KBA3 19
KBA4 20
KBA5 21
KBA6 22
KBA7 23
KSO0 14
KSO1 15
KSO2 16
KSO3 17
KSO4 18
KSO5 19
KSO6 20
KSO7 21
KSO8 22
KSO9 23
KSO10 24
KSO11 25
KSO12 26
KSO13 27
KSO14 28
KSO15 29
INVT_PWM
BEEP#
For PWM EN_LENOVO
ACOFF
PM_BATLOW#
EC_ON
EC_LID_OUT#
PCM_SUSP#
EC_URAD
EC_UTXD
EC_USCLK
EC_SMC1
EC_SMD1
LPC_RST#
PBTN_OUT#
EC_SMC2
EC_SMD2
FAN_SPEED
PCI_PME#
ATICUTE
MPCI#
PCT
PACIN
RINGIN
SCR_LED#
NUM_LED#
CAPS_LED#
PADS_LED#
EC_SMI#
VGA_SUSP#
G_RST#
EC_SWI#
IRQPL1
SLP_S1#_RSTOUT#
BATT_TEMP_A
BATT_TEMP_B
BATT_OVP
ALWHW#
BATT_CHG#
ADP_I
GNI/OFF
PM_SLP_S5#
DAC_BRIG
VOL_AMP
IREF
EN_DFAN
EC_TRST#
TCK
TDO
TDI
TMS
LPC_AD0..3
LPC_AD0
LPC_AD1
LPC_AD2
LPC_AD3
LFRAME#
LDRQ#
SERIRQ
EC_RST#
SUS1#
SWI#
PWUREQ#
LPCPD#
LPC_CLKRUN#
EC_SCI#
CLK_LPC_EC
KBRST#/KP56
KP_ROW0..7
KP_COL0..17
KBRST#
KP_COL0
KP_COL1
KP_COL2
KP_COL3
KP_COL4
KP_COL5
KP_COL6
KP_COL7
KP_COL8
KP_COL9
KP_COL10
KP_COL11
KP_COL12
KP_COL13
KP_COL14
KP_COL15
KP_COL16
KP_COL17
KP_ROW0
KP_ROW1
KP_ROW2
KP_ROW3
KP_ROW4
KP_ROW5
KP_ROW6
KP_ROW7
KP_ROW8
KP_ROW9
KP_ROW10
KP_ROW11
KP_ROW12
KP_ROW13
KP_ROW14
KP_ROW15
KP_ROW16
KP_ROW17
KP_ROW18
KP_ROW19
KP_ROW20
KP_ROW21
KP_ROW22
KP_ROW23
KP_ROW24
KP_ROW25
KP_ROW26
KP_ROW27
KP_ROW28
KP_ROW29
KP_ROW30
KP_ROW31
KP_ROW32
KP_ROW33
KP_ROW34
KP_ROW35
KP_ROW36
KP_ROW37
KP_ROW38
KP_ROW39
KP_ROW40
KP_ROW41
KP_ROW42
KP_ROW43
KP_ROW44
KP_ROW45
KP_ROW46
KP_ROW47
FSTCHG
FRDY
SELIO#
FSEL#
SYSON
SUSP#
MM0_ON
EC_RSMRST#
PCIRST_PWRGOK
ENVEE
ENBKL
KBD_CLK
KBD_DATA
PS2_CLK
PS2_DATA
TP_CLK
TP_DATA
LID_SW#
CIDN#
TP_CLK
TP_DATA
32KX1/32KCLKOUT
32KX2
CRY1
CRY2
X1
32.768KHZ
CLK
PCF8751VPC
EC_SMC2
EC_SMD2
EC_SMC1
EC_SMD1
GATEA20
RC#
RCLK
SMSO_PME#
1394_PME#
PCM_PME#
WLANHW#
LAN_PME#
ICH_WAKE_UP#
PCI_PME#
ECAGND
BATT TEMPA
BATT TEMPB
VR_ON
ATF_INT#
ATFOUT#
MM0 ON
FRDY
SELIO#
FSEL#
SYSON
SUSP#
MM0_ON
EC_RSMRST#
PCIRST_PWRGOK
ENVEE
ENBKL
KBD_CLK
KBD_DATA
PS2_CLK
PS2_DATA
TP_CLK
TP_DATA
LID_SW#
CIDN#
KBA0
KBA1
KBA2
KBA3
KBA4
KBA5
KBA6
KBA7
KBA0 16
KBA1 17
KBA2 18
KBA3 19
KBA4 20
KBA5 21
KBA6 22
KBA7 23
R136 1K
R137 1K
R122 1K
R123 1K
R124 1K
R125 1K
R240 10K
R241 20M
R242 120K_0603
R243 10K
R244 10K
R245 10K
R246 10K
R247 10K
R248 10K
R249 10K
R250 10K
R251 10K
R252 10K
R253 10K
R254 10K
R255 10K
R256 10K
R257 10K
R258 10K
R259 10K
R260 10K
R261 10K
R262 10K


BUTTON1#
INTERRUPT#
CD_INTA#
PCM LED
SHDD_LED#
PHDD_LED#
DRIVE#
OCCB#
SELIO#
KBA1
U20B
74LVC32
U20A
KBA2
U20C
KBA4
U20D
KBA3
U26
74LVC244
U27
74HCT273
U21
74HCT273
U22
74LVC244
U23
74LVC244
RP11
8P4R_100K
R244
20K
C263
1UF_25V_0805
R229
100K
D11
DAN202U
22 PCM1_LED
22 PCM2_LED
PCM LED
PROCHOT#
THRM#
R277
R278
H27#
EXTIDEPWR# 19
IDE_DIR# 34
CD_PLAY 29
HDD_LED# 34
2ND_CHGU_CD_FDD_LED# 34
PWR_LED# 34
2nd BATT_LOW_LED# 34
BATT_LOW_LED# 34
BATT_CHG_LED# 34
WL_OFF# 27
CD_STOP/BTN# 29
PCMCIA/TI# 23
EC_AMPON# 31
EXTIDE0
EXTIDE1
EXTIDE2
HGT#
MEDIA_DETECT
VOL_UP#
VOL_DWN#
KILL_SW
MP3_STOP/BTN#
MP3_PLAY/BTN#
MP3_FROM/TI#
MP3_REV/BTN#
STOP/BTN#
R18
R19
R20
R21
R149
R147
R148
U25
75H32FU
C249
C121
C229
C240
C219
C225
C226
C215
C274
C126
R381
100K
R417
100K
Q33
2N7002
PWE#
FWR#
EC_FLASH# 17
EC_SMC1
EC_SMD1
R190
4.7K
R188
100K
R181
100K
U18
NM24C16
BOARD ID
REV 2A2 2A3 2A4
0.1 0 0 0
0.2 0 0 1
0.3 0 1 0
1.0 1 0 0
U12
U11
U14
FLASH_VCC
FRD#
FSEL#
KBA10
29F040/SST39VF040_PLCC
SST39VF040_TSOP
29F040_TSOP
UNCONTROLLED DOCUMENT
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Rev 3A
Date: 2002-8-6
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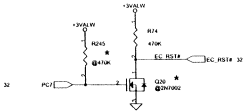
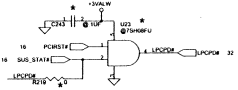
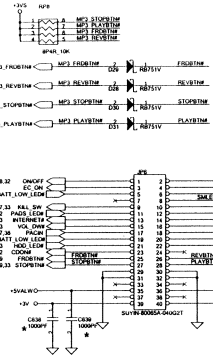




For PC87591 REV 0.A Only



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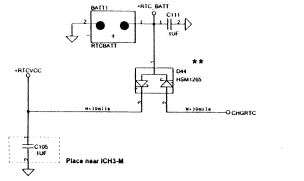
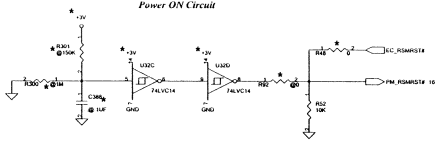
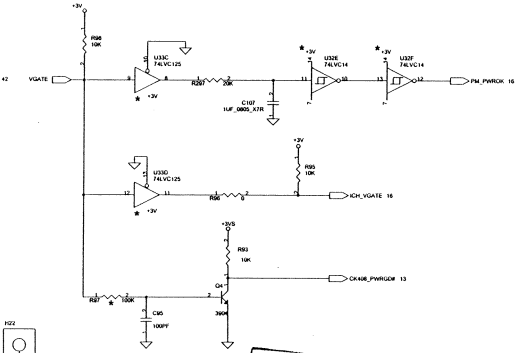
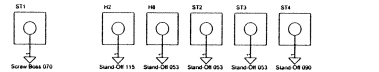
RTC Batt. Connector

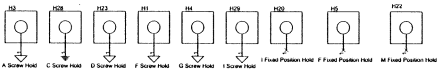


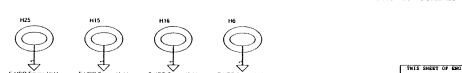
Power ON Circuit

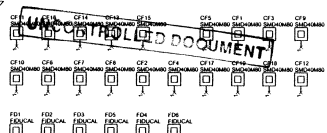












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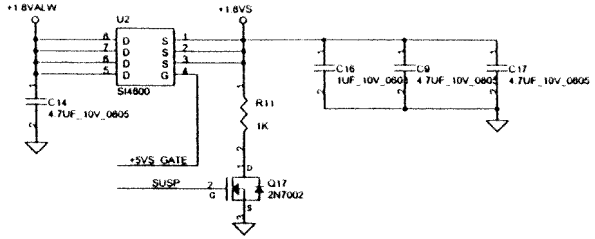
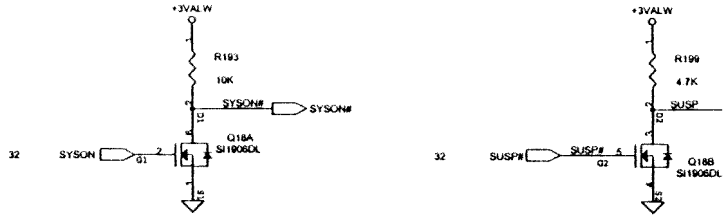
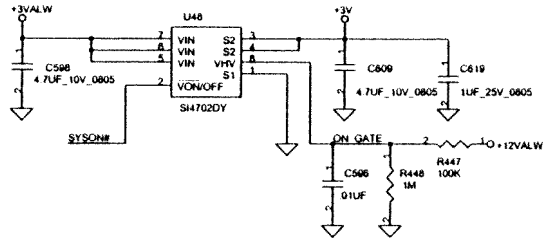
+1.8VALW To +1.8VS Transfer

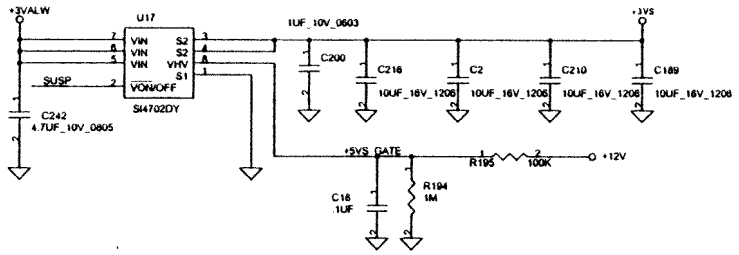




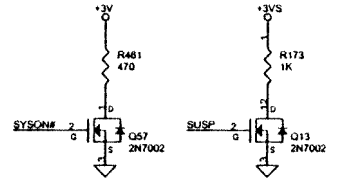
+3VALW To +3V Transfer



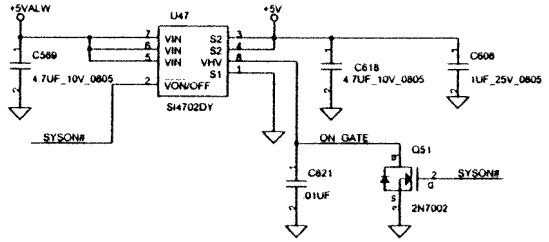
+3VALW To +3VS Transfer



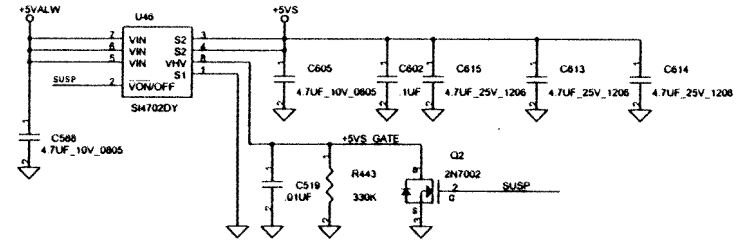
+3V & +3VS Discharge



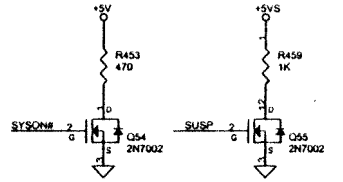
+5VALW To +5V Transfer



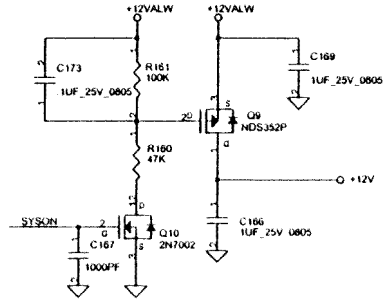
+5VALW To +5VS Transfer



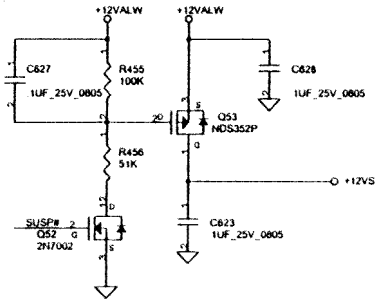
+5V & +5VS Discharge



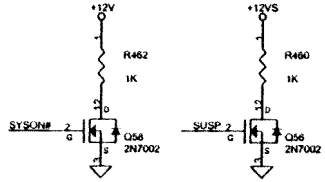
+12VALW To +12V Transfer



+12VALW To +12VS Transfer



+12V & +12VS Discharge



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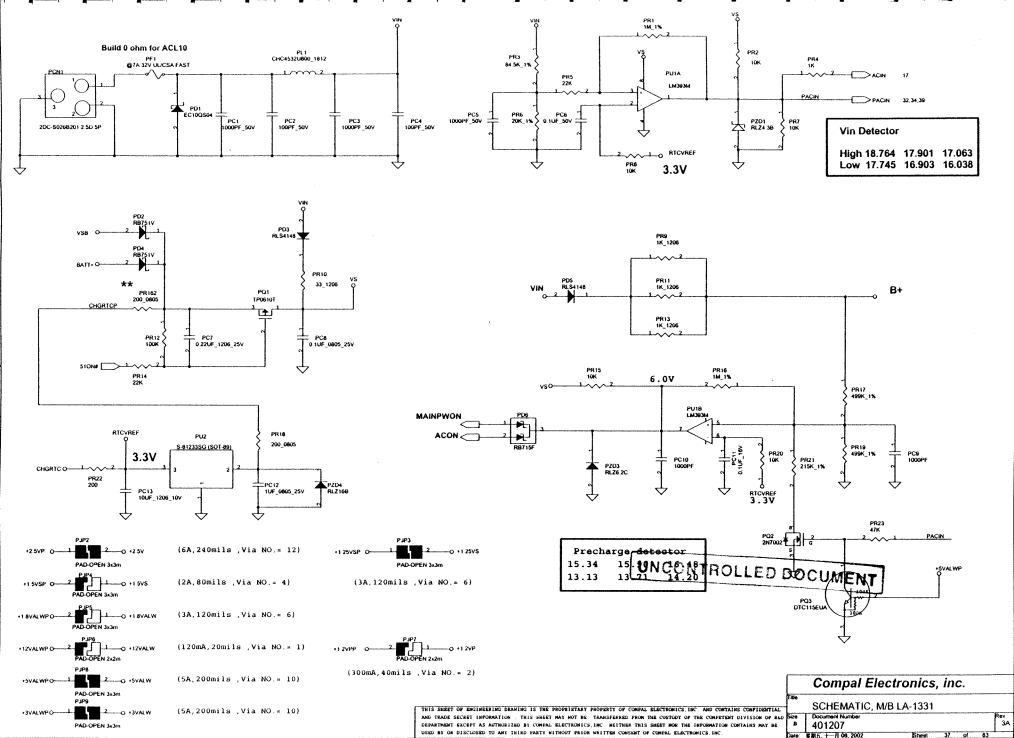

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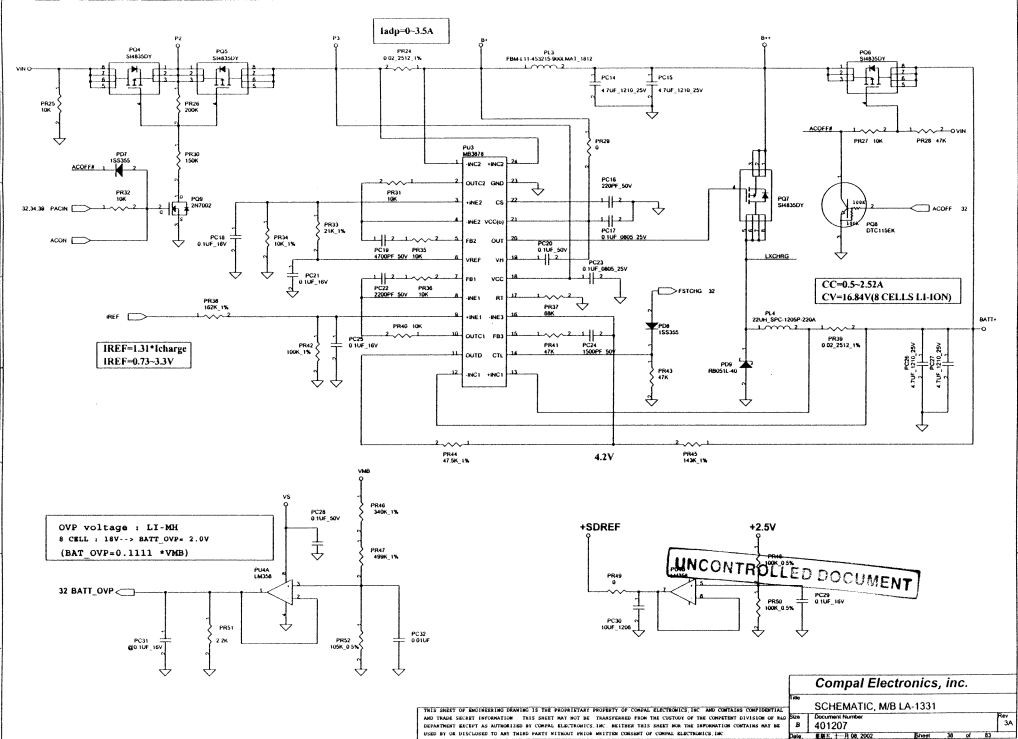

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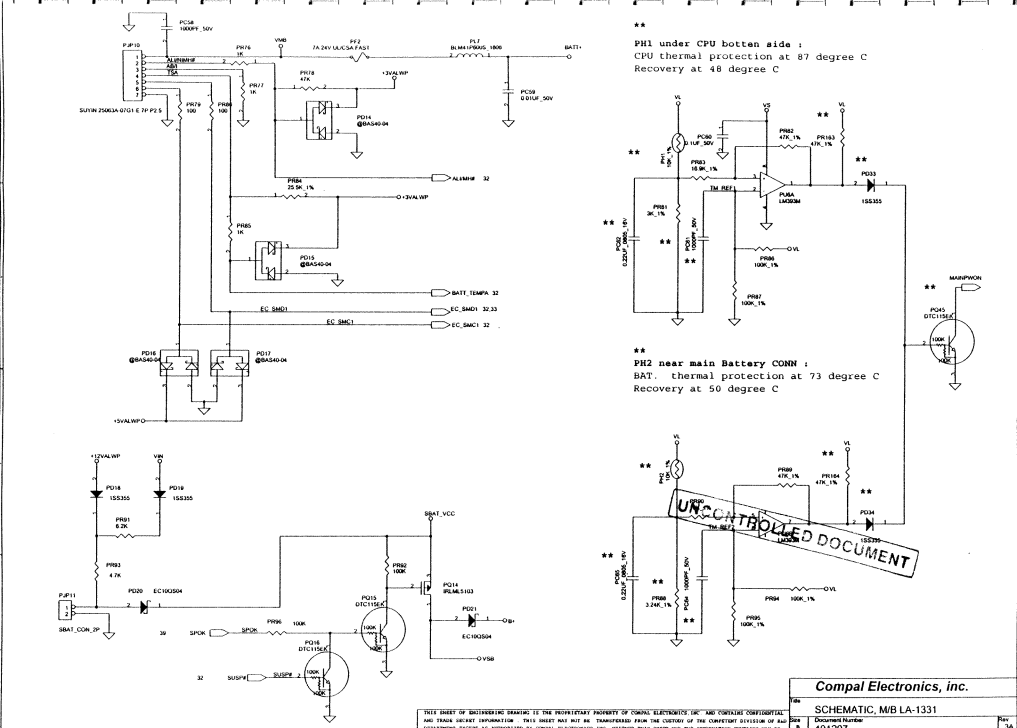
**
PH1 under CPU botten side :
CPU thermal protection at 87 degree C
Recovery at 48 degree C
**
PH2 near main Battery CONN :
BAT. thermal protection at 73 degree C
Recovery at 50 degree C
UNCONTROLLED DOCUMENT
PJP10
PJP11
PJP12
PJP13
PJP14
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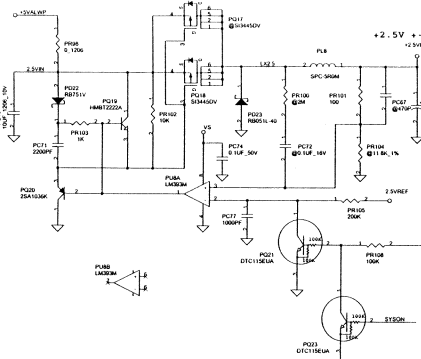
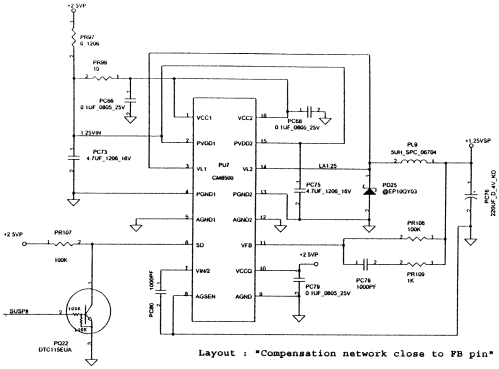
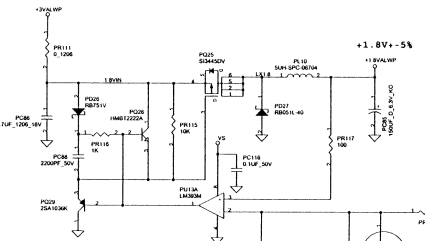
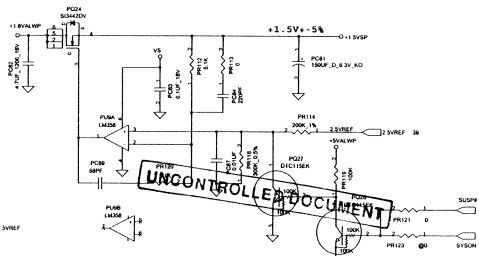




Layout : "Compensation network close to FB pin"





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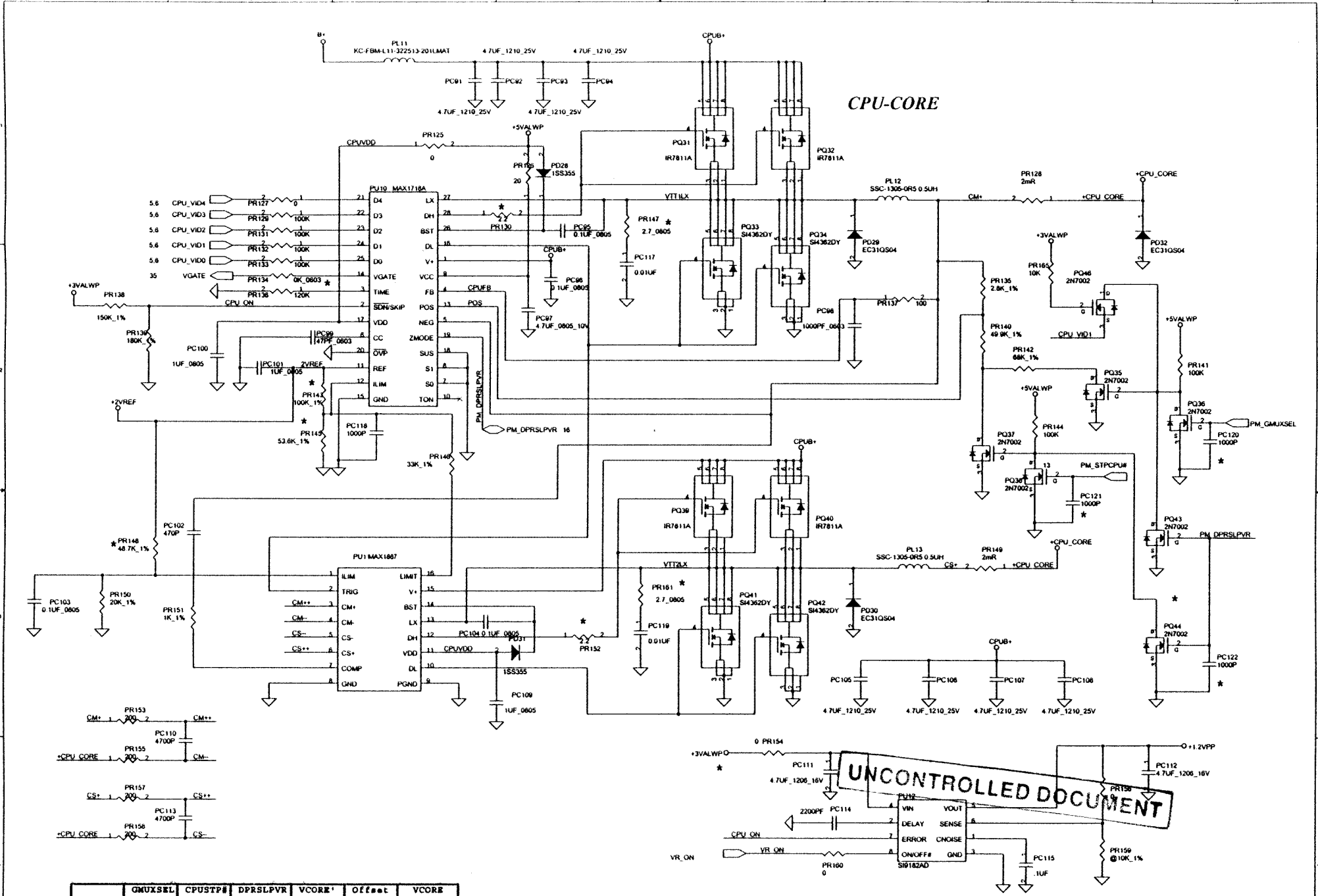

	GMUXSEL	CPUSTP#	DPRSLPVR	VCORE'	Offset	VCORE
PM	1	1	0	1.30V	0%	1.30V
PM D-S	1	0	0		4.62%	1.239V
BM	0	1	0	1.20V	2.0%	1.176V
BM D-S	0	0	0		4.62%	1.144V
Deeper	X	0	1	1.0V	0%	1.0V

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