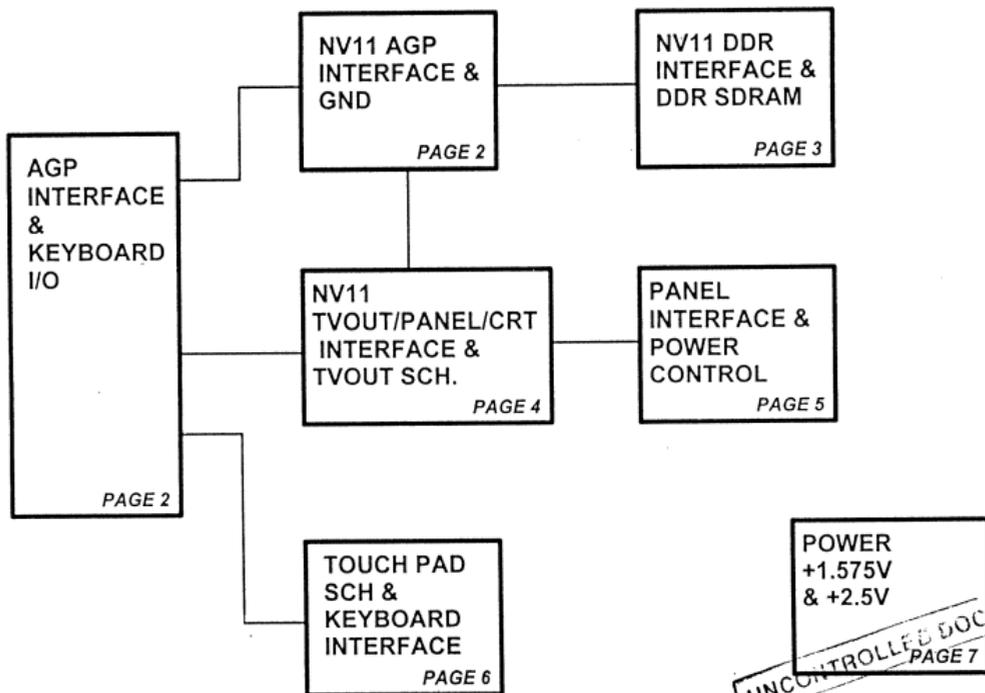


# COMPAL CONFIDENTIAL

MODEL NAME : 888M3/CL00 VGA BOARD



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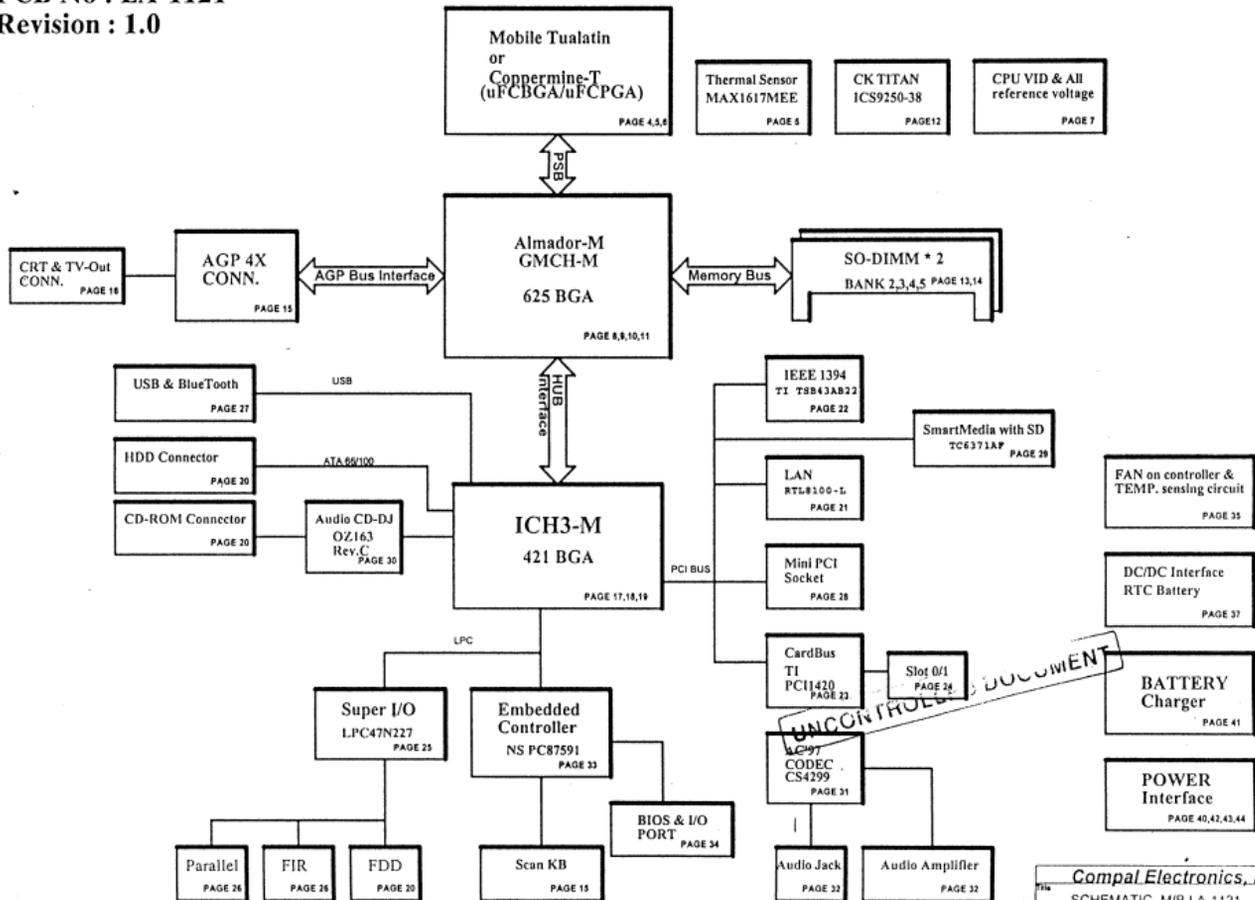
Compal Electronics, Inc.	
SCHEMATIC, VGA/B LS-1126	
Document Number	405527
Date	Thursday, September 04, 2003
Sheet	1 of 1

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Model Name : 888M3  
 PCB No : LA-1121  
 Revision : 1.0

# BLOCK DIAGRAM

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## Voltage Rails

Power Plane	Description	S4	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+VCC_H_CORE	Core voltage for CPU	ON	OFF	OFF
+VTT	1.2V switched power rail for CPU AGTL Bus	ON	OFF	OFF
+1.5V	1.5V power rail	ON	ON	OFF
+1.5VS	AGP 4X	ON	OFF	OFF
+1.8V	1.8V power rail	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5V	2.5V power rail	ON	ON	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5V	5V power rail	ON	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
+12VS	12V switched power rail	ON	OFF	OFF
RTCVC	RTC power	ON	ON	ON

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

## External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
AGP 4X CONN.			PIRQA
IEEE 1394	AD16	0	PIRQA/PIROB
CardBus	AD20	2	PIRQA/PIROB
LAN	AD17	3	PIROB
Mini-PCI	AD18	14	PIROC/PIROD
SD/SIM	AD22		PIROC/PIROD

## EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
EEPROM(24C1602)	1010 000X b
(H4GH)	1011 000Xb

## EC SM Bus2 address

Device	Address
MAX1617MEE	1001 110X b
OZ163	0011 0100 b
Smart Battery	0001 011X b
Docking	0011 011X b
DOT Board	XXXX XXXXb

## ICH3-M SM Bus address

Device	Address
Clock Generator (IC5623R-50)	1101 0000
SDRAM Select (74HC4052)	1010 0000
CPU Voltage VID select (F3365)	0110 111Xb

## PIR

REV 0.2		
Date	Page	Description
5/8	29	Modification includes SM-S0 function
5/8	32	Modification audio volume control function
5/8	42	ADD system thermal protection
5/14	33	DEL R244_Add D44
REV 0.3		
Date	Page	Description
5/23	5	U8 Vcc plane modify to +5VALW
6/23	18	DEL R90,R99,R261
5/23	32	R448 change gnd to +5VCC, R476 change +5VCC to gnd.
6/23	37	U2 link to U20.8
5/23	30	Add R516.
5/23	6	U8 AF18 add R517 link to +1.5VS
5/23	25	Modify LPC_RSTA timing. Add U56,D45,R518.
5/31	27	JP15.8 connector to U29.57
5/31	25	ADD R520. Add net name BT_DET4 to U29.57
5/31	34	Modify net name ANT_SW to W6_OFFA, ADD R221
5/31	28	Modify net name RPOFFB to W6_OFFB
5/31	35	DEL R19
REV 0.4		
Date	Page	Description
7/2	16	Del L23,R14,R12,R10,R8,R6
7/2	27	ADD C726,C721,C722,C723,C724,C725
7/2	29	IDSEL0 change to PCI_AD28, INTAWNT0# change to PIRQCAPROD0
7/10	24	Add U56,U59,R531,R532,R533,R534,C18,C718
7/17	29	Del S0 function
7/18	28	Change IDSEL to PCI_AD22
7/23	21	DEL C13
REV 0.5		
Date	Page	Description
8/13	13	Add R544 reserve for aux_gstiff and s10_appd
8/13	28	Add R545 pull-up signal SM_LED to SMC_VCC_ASH0 in U82,C726,R496
8/13	35	Change R543 pull-up term SMC_VCC to +5VS
8/13	29	Add R546,R547 signal PCHSTA,CBRST#
8/13	37	Del U2,G4,R230
8/16	10	Add Signal TV_out_DDC2CLK,TV_out_DDC2DATA,VIDK_DDCCLK,VIDK_DDC2FA,AGP_DDCCLK,AGP_DDC2DATA
8/16	10	Add R551,R552 DEL R225,R226
8/16	15	Add R936,R939
8/16	16	Add R553,R554,R555
8/17	34	Del R26, Add R557, R558
8/17	20	Add R556
REV 1.0		
Date	Page	Description
8/31	5	06 RESERVE
REV 1.A		
Date	Page	Description
9/6	12	06 Cr1ption

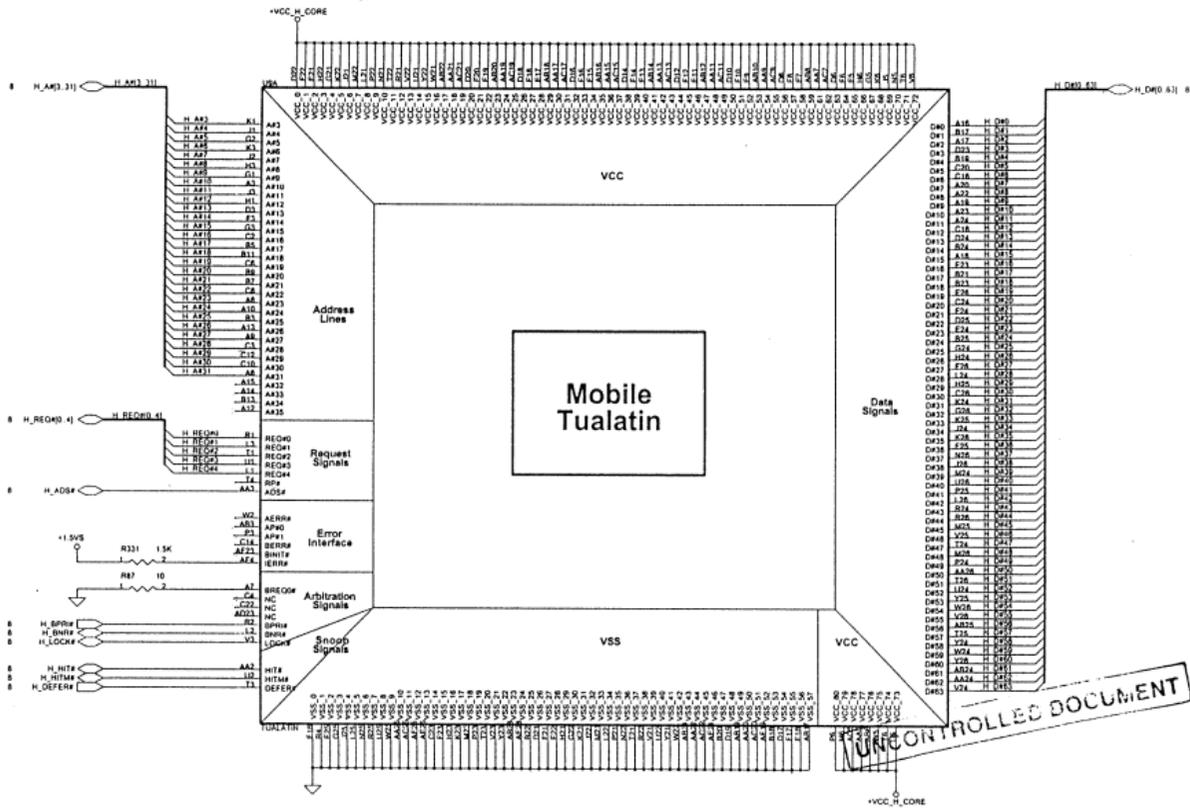
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401191 (FOR ATL02 / ACL00)

Rev. C

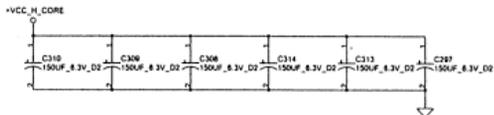
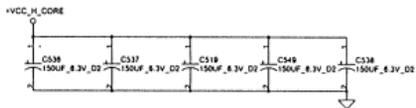
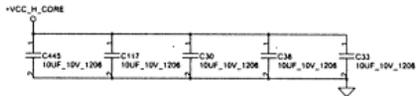
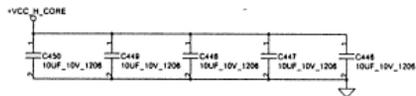
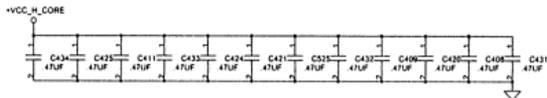
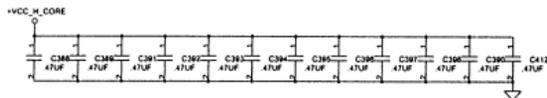


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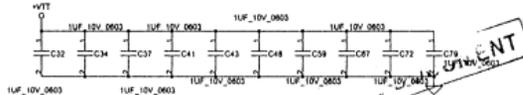
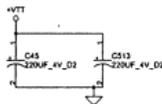
**Layout note :**

Place close to CPU, Use 2-3 vias per PAD.  
 Place .47uF caps underneath balls on solder side.  
 Place 10uF caps on the peripheral near balls.  
 Use 2-3 vias per PAD.



**Layout note :**

Place close to CPU,  
 Use 2 vias per PAD.



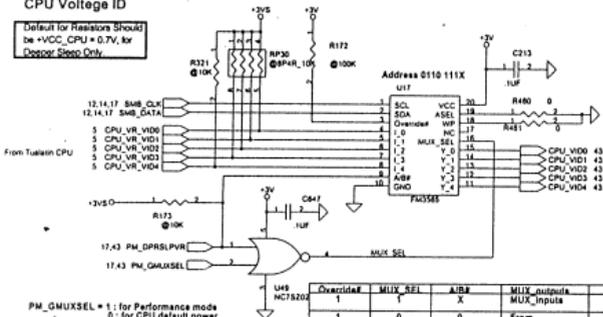
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File	SCHEMATIC, M/B LA-1121
Rev	0000000000
Dist	401191 (FOR ATL02 / ACL00)
Date	8.11.2001
Page	3 of 37

### CPU Voltage ID

Default for Resistor should be +VCC, CPU = 0.7V, for Deeper Sleep Only.



PM\_GMUXSEL = 1: for Performance mode  
0: for CPU default power

PM\_DPRSLPVR = 1: for Deeper Sleep mode  
0: for Performance mode

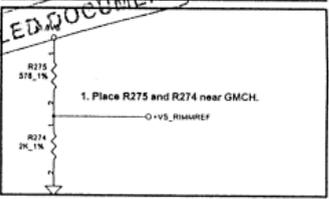
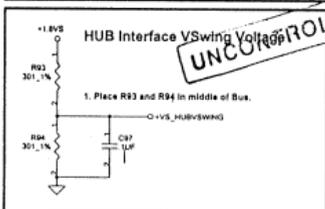
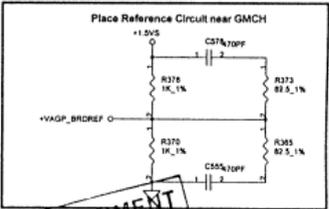
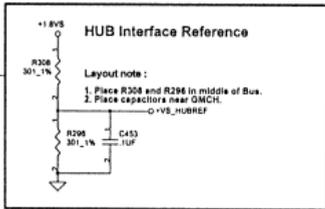
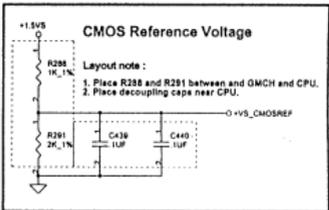
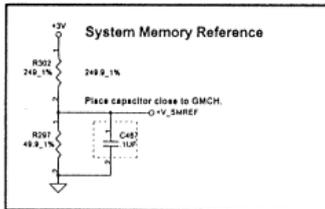
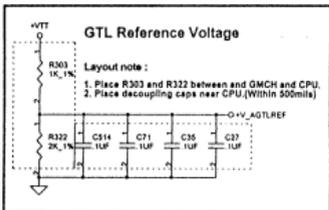
Descriptor	MUX_SEL	ADB	MUX_output	MUX_input	Mode
1	0	0	From Non-volatile register(SOPRB)	Battery	Performance
1	0	1	From Non-volatile register(SOPRA)	Battery	

### Tualatin

```

04 03 02 01 00 CPU_Core(V) B6(before #P)
0 0 1 0 1 1.35V (Performance)
0 1 1 0 0 1.35V (Battery)
1 0 1 0 1 1.85V (Deeper Sleep)

04 03 02 01 00 CPU_Core(V) D61 (#P)
0 0 1 0 1 1.35V (Performance)
0 1 1 0 0 1.35V (Battery)
1 0 1 0 1 1.85V (Deeper Sleep)
    
```

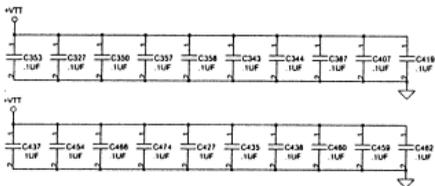




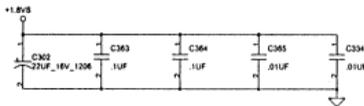




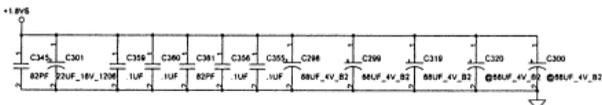
**Layout note:**  
Distribute as close as possible to GMCH Processor Quadrant.



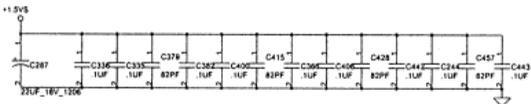
**Layout note:**  
Distribute as close as possible to VCCPCMOS\_LM.



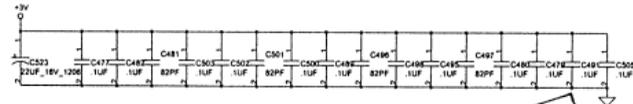
**Layout note:**  
Distribute as close as possible to GMCH Local Memory Quadrant.



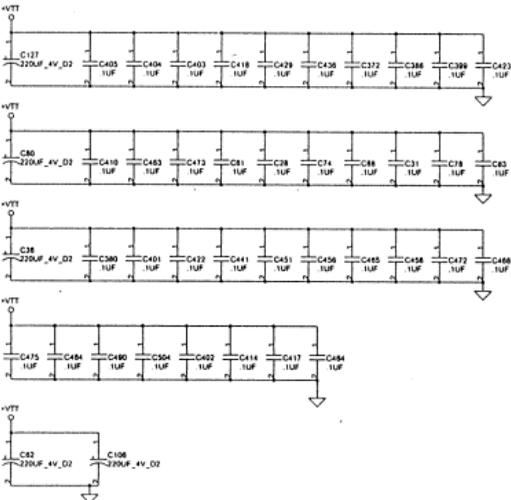
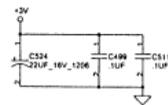
**Layout note:**  
Distribute as close as possible to GMCH AGP/DVD Quadrant.



**Layout note:**  
Distribute as close as possible to GMCH System Memory Quadrant.



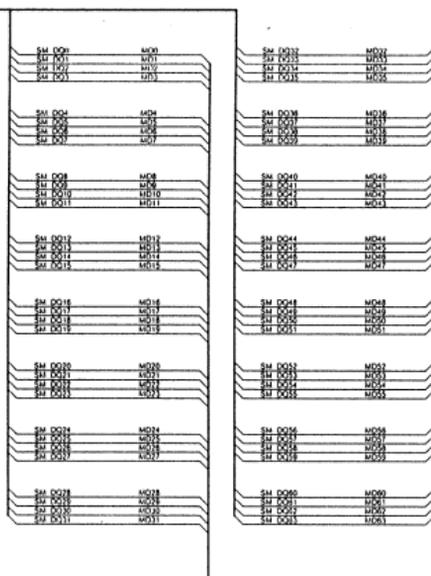
**Layout note:**  
Distribute as close as possible to IO Quadrant.



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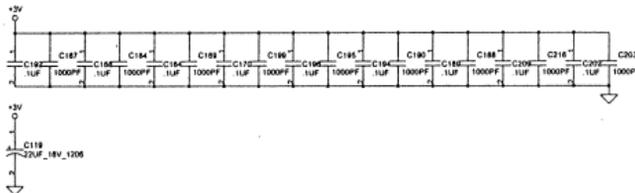
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MQ0\_83, 8,14

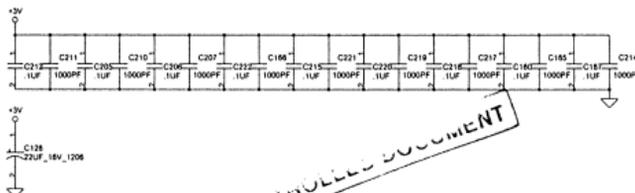
Layout note :

One .1uF cap per power pin.  
Place each cap close to SODIMM(DIMM 0) pin.

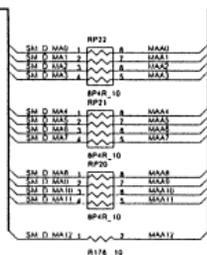


Layout note :

One .1uF cap per power pin.  
Place each cap close to SODIMM(DIMM 1) pin.



9 SM\_D\_MAR\_12



R176 10

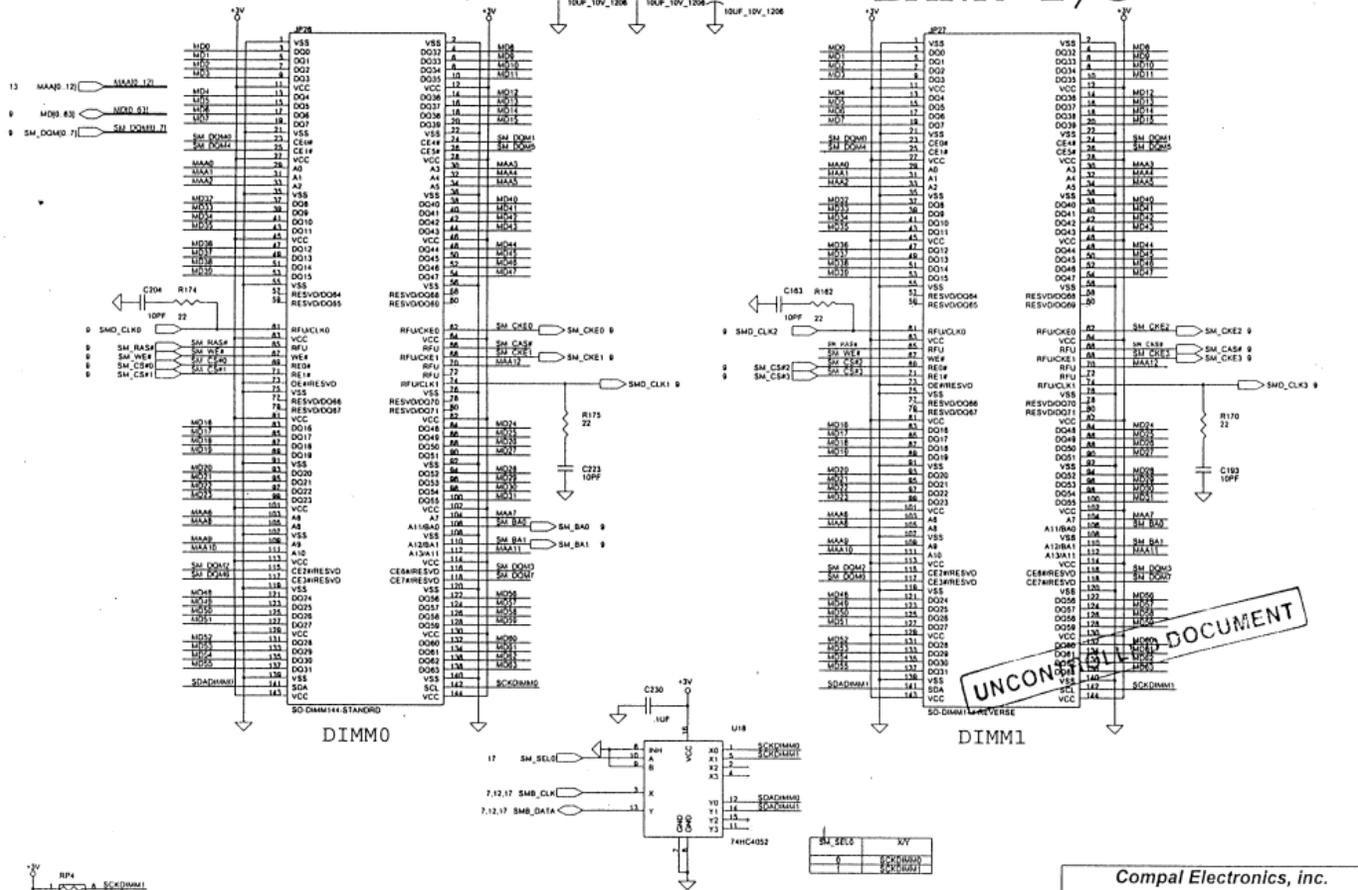
MAAR\_12 14

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SO-DIMM 144 PINS  
RAM MODULE CONN.

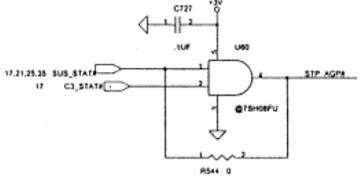
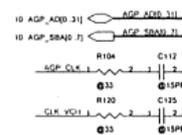
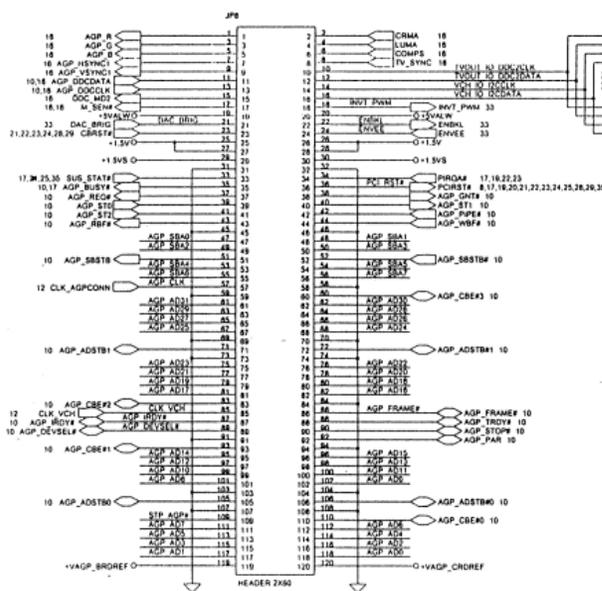
BANK 0/1

BANK 2/3

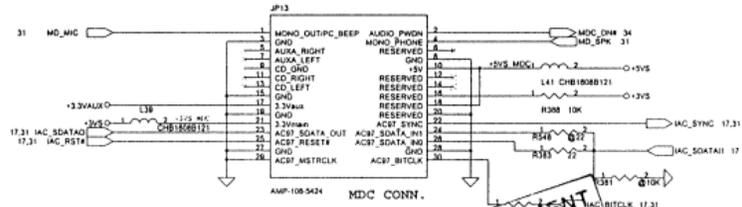
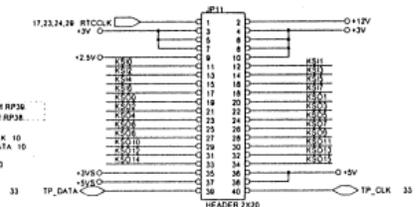


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AGP CONN.



33 K500 71 K500 13 Int. Keyboard CONN.



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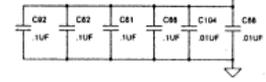
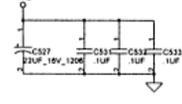
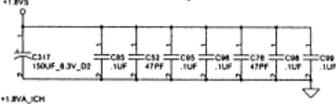
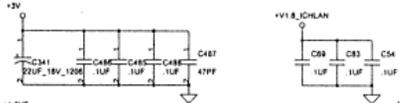
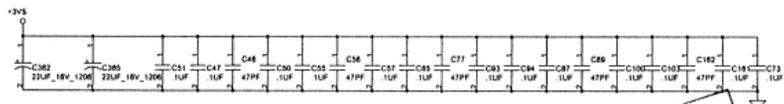
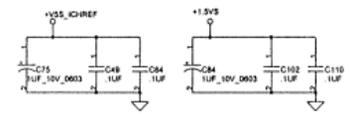
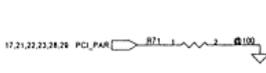
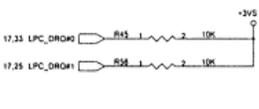
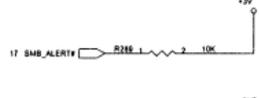
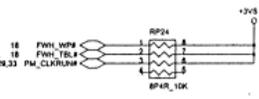
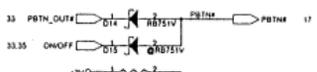
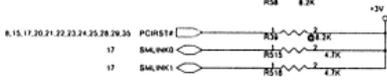
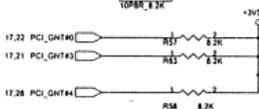
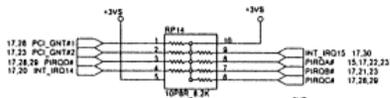
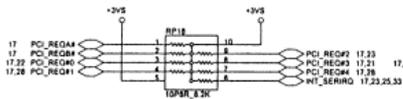
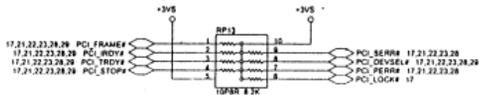
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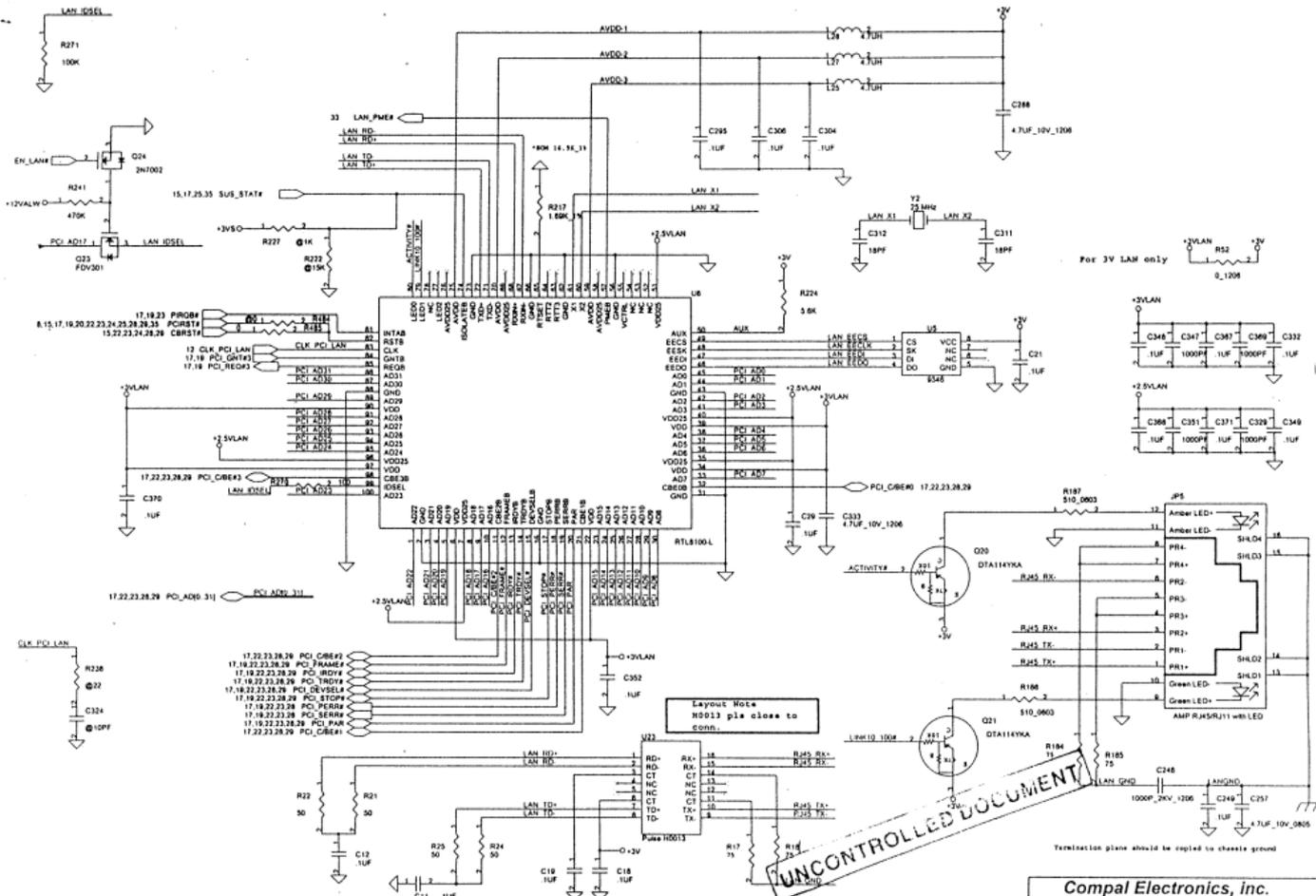




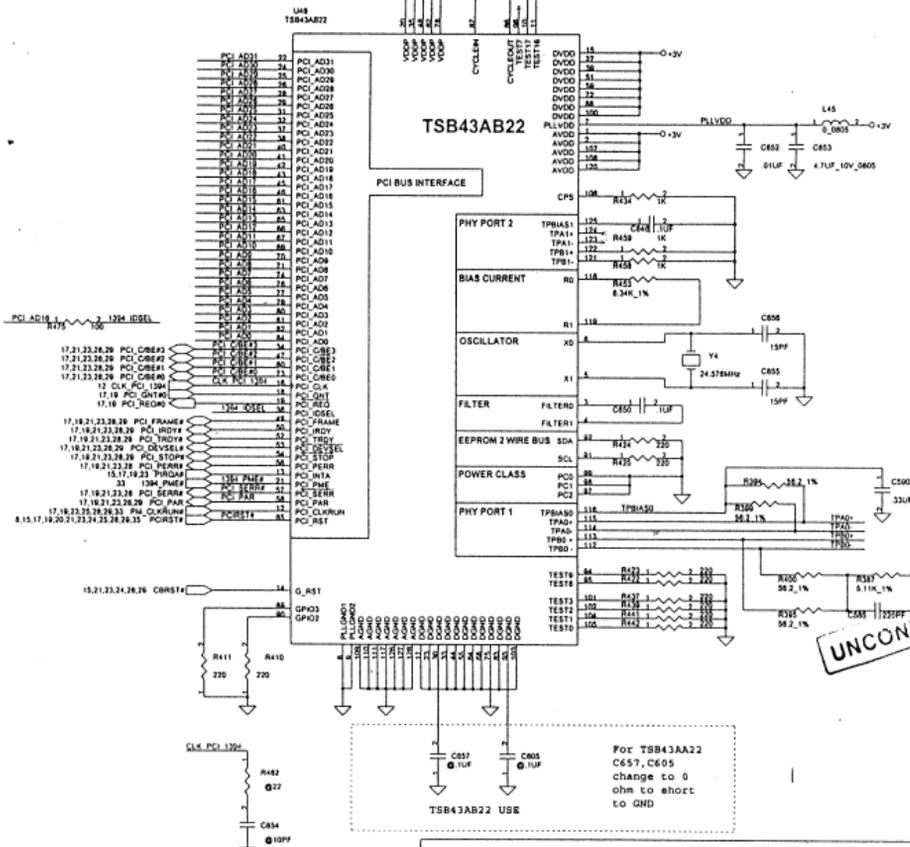
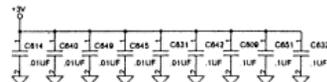


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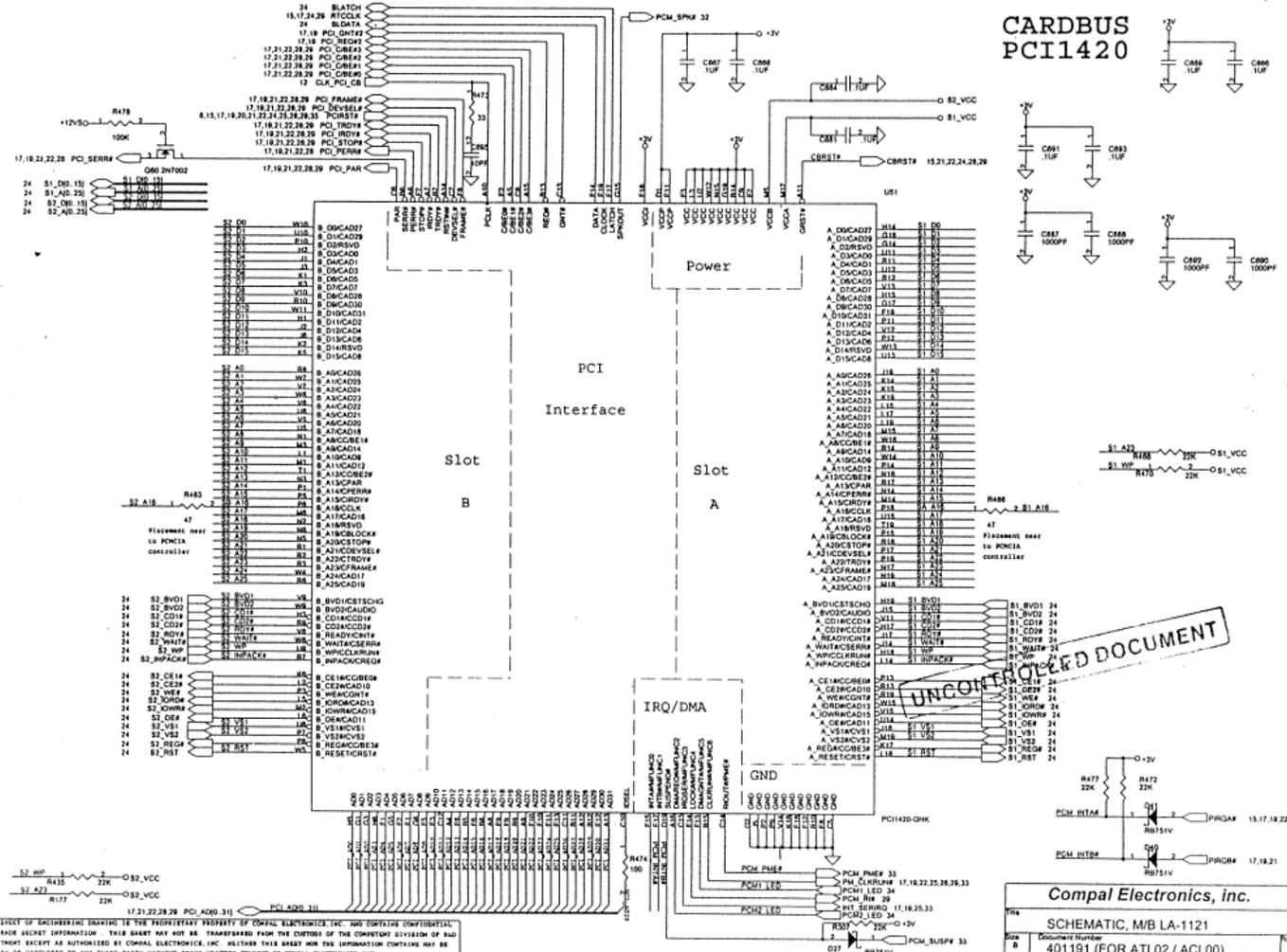
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# CARBUS PCI1420



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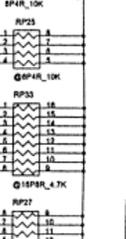
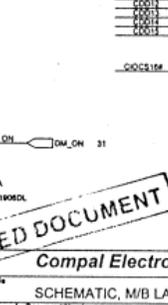
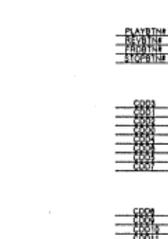
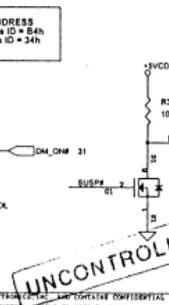
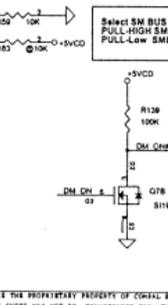
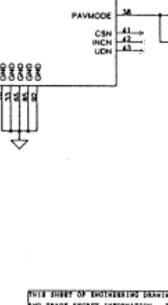
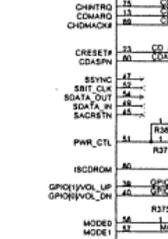
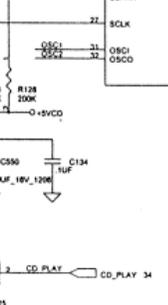
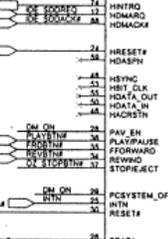
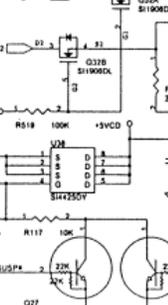
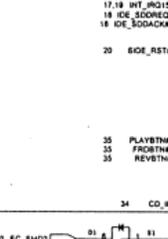
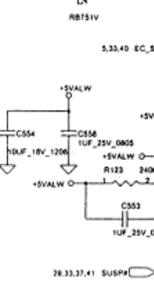
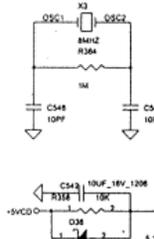
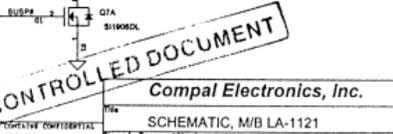
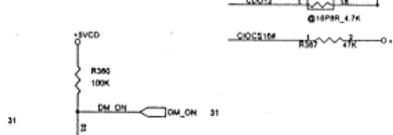
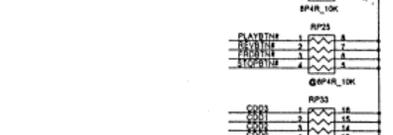
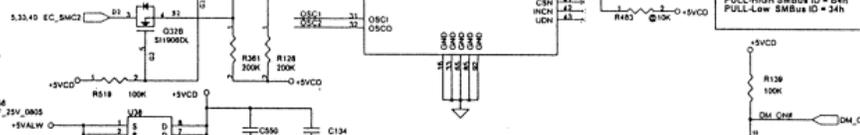
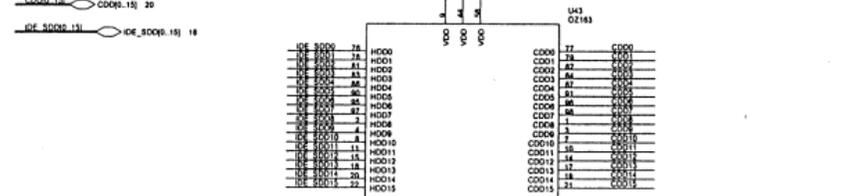
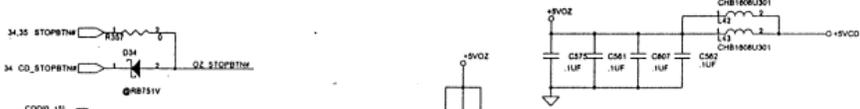








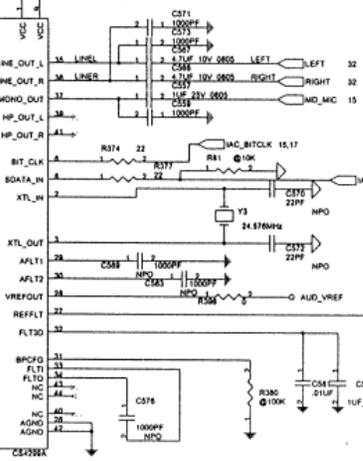
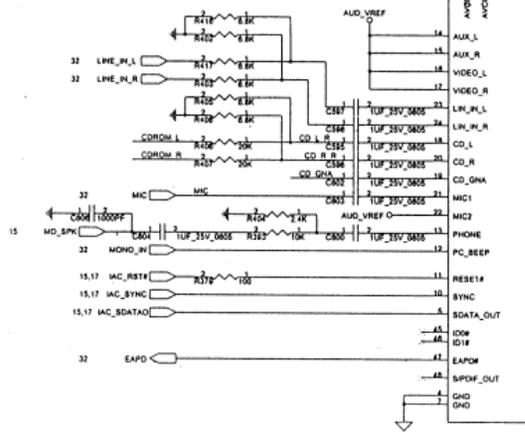
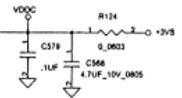
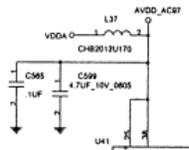
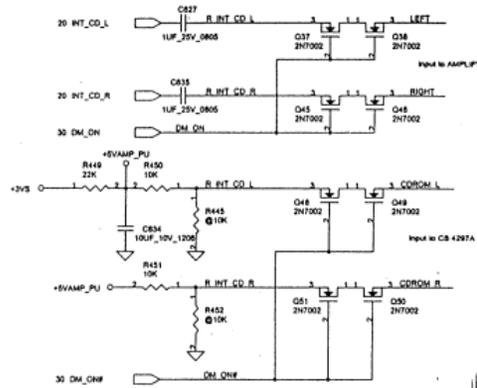
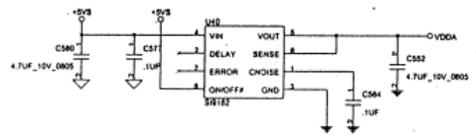




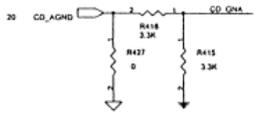
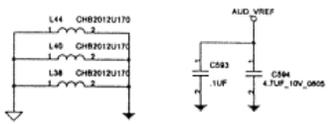
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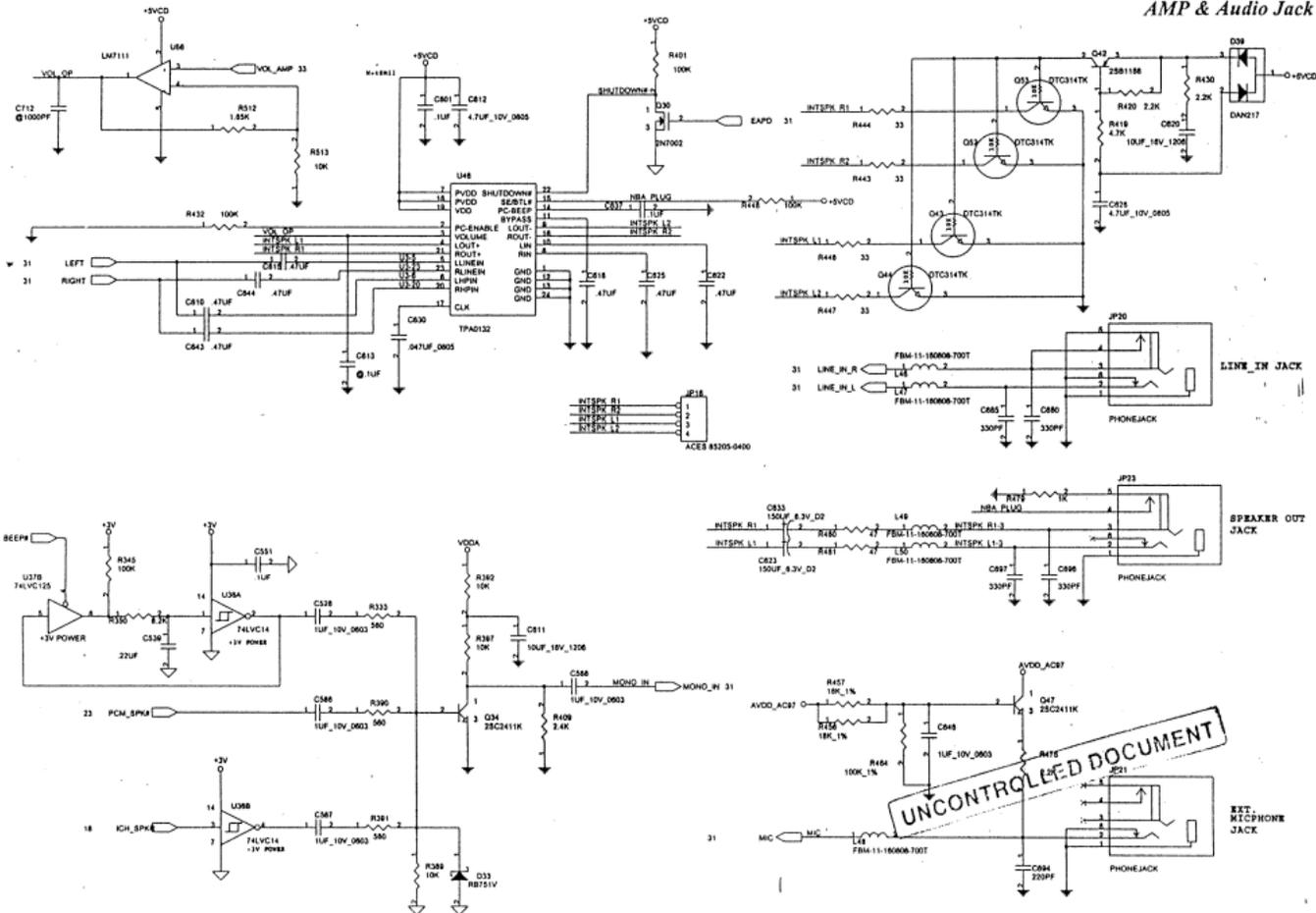
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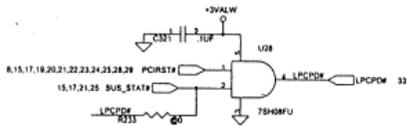
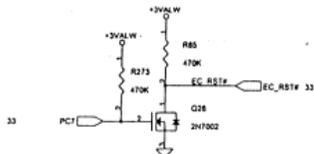
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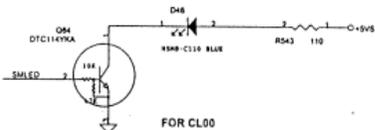
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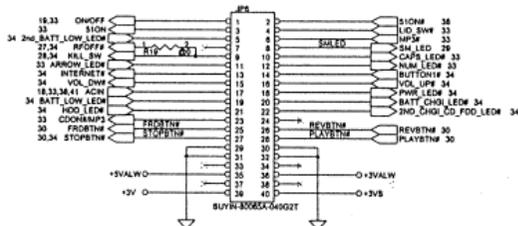
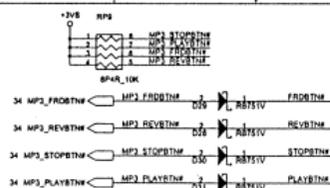




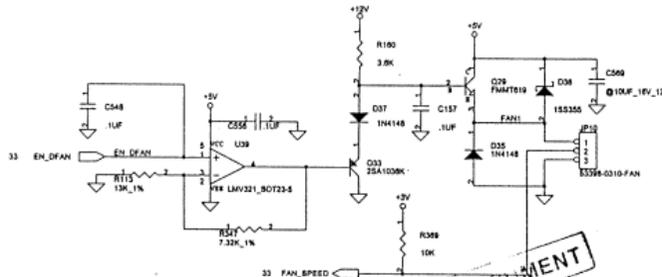
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FOR CL00



FAN CONN.



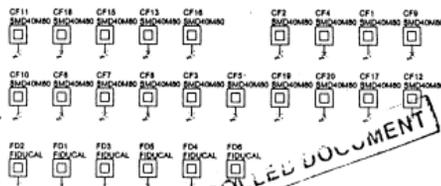
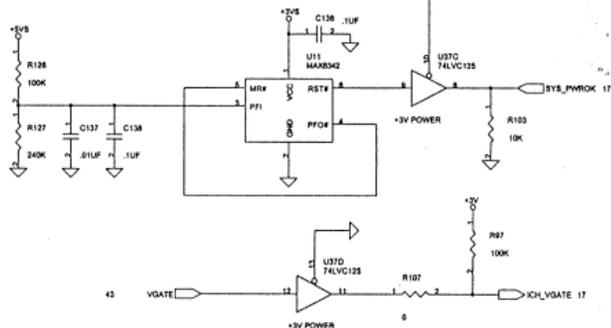
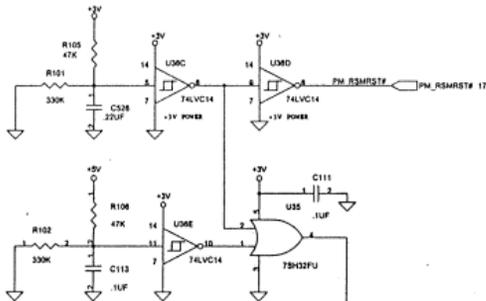
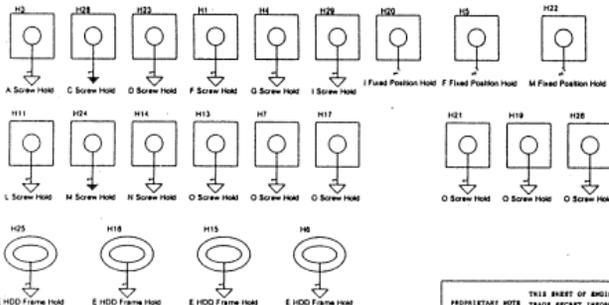
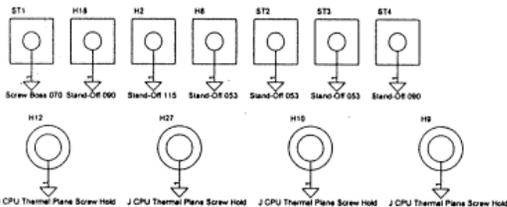
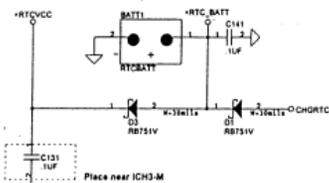
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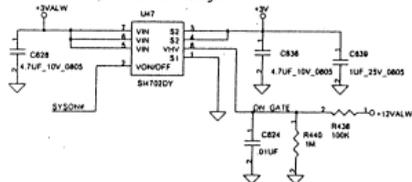
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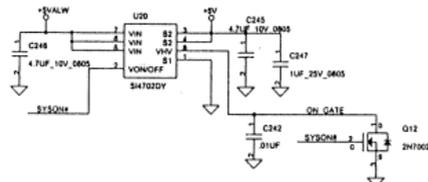


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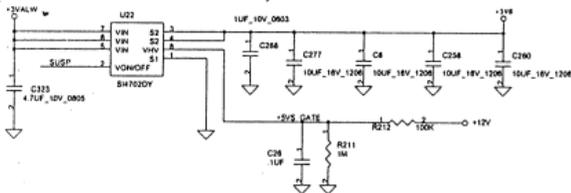
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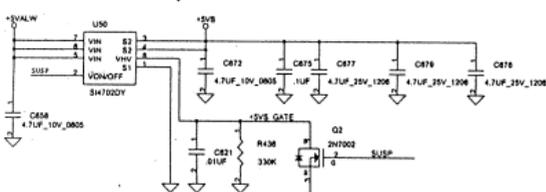
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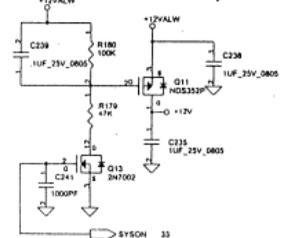
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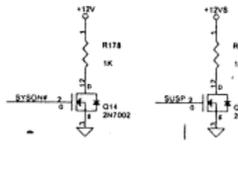
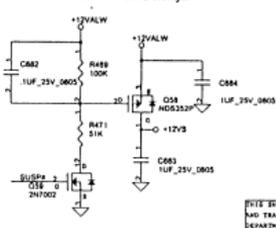
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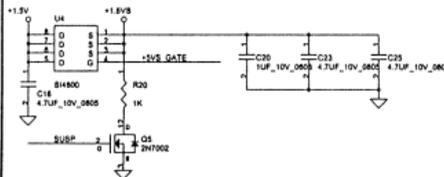
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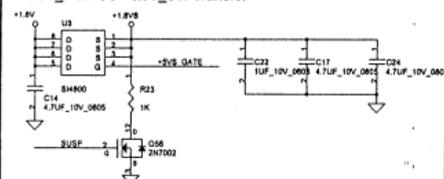
### +12VALW To +12VS Transfer



### +1.5V TO +1.5V\_SW Transfer



### +1.8V\_ALW TO +1.8V\_SW Transfer

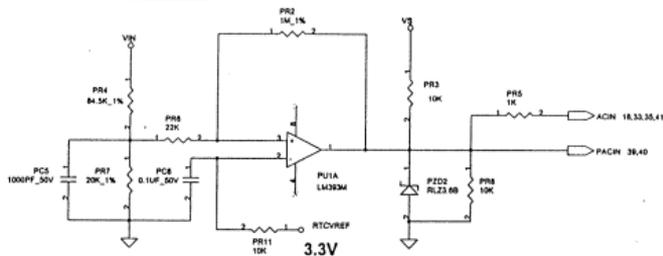
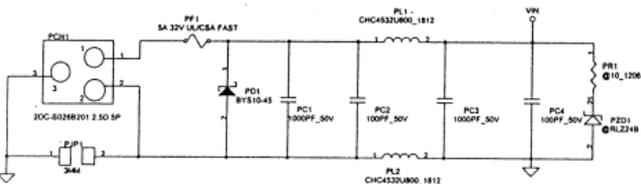


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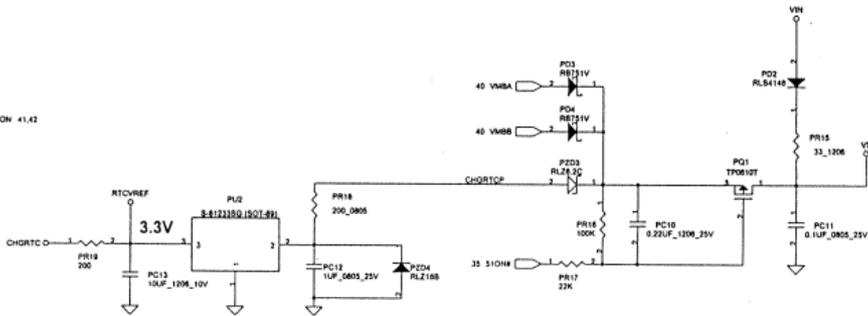
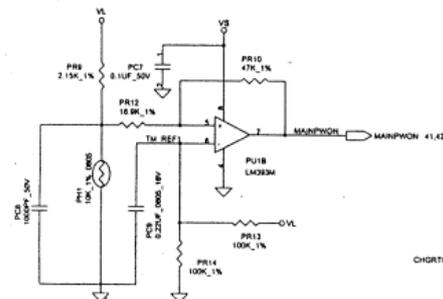
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### Vin Detector

High 18.764 17.901 17.063  
Low 17.745 16.903 16.038



PH1 under CPU bottom side ;  
CPU thermal protection at 81(82) degree C  
Recovery at 50(51) degree C



+12VALWP → PJP2 → +12VALW (120mA, 20mils, Via NO. = 1)  
JOPEM=12V

+5VALWP → PJP3 → +5VALW (5A, 200mils, Via NO. = 10)  
PAD-OPEN 4x4x4

+2VALWP → PJP4 → +2VALW (5A, 200mils, Via NO. = 10)  
PAD-OPEN 4x4x4

+1.5VP → PJP5 → +1.5V (1.5A, 60mils, Via NO. = 3)  
3MANGPU\_JD

+1.8VP → PJP6 → +1.8V (3A, 120mils, Via NO. = 6)  
3MANGCPU\_JD

+VTP → PJP7 → +VTT (16A, 240mils, Via NO. = 12)  
PAD-OPEN 4x4x4

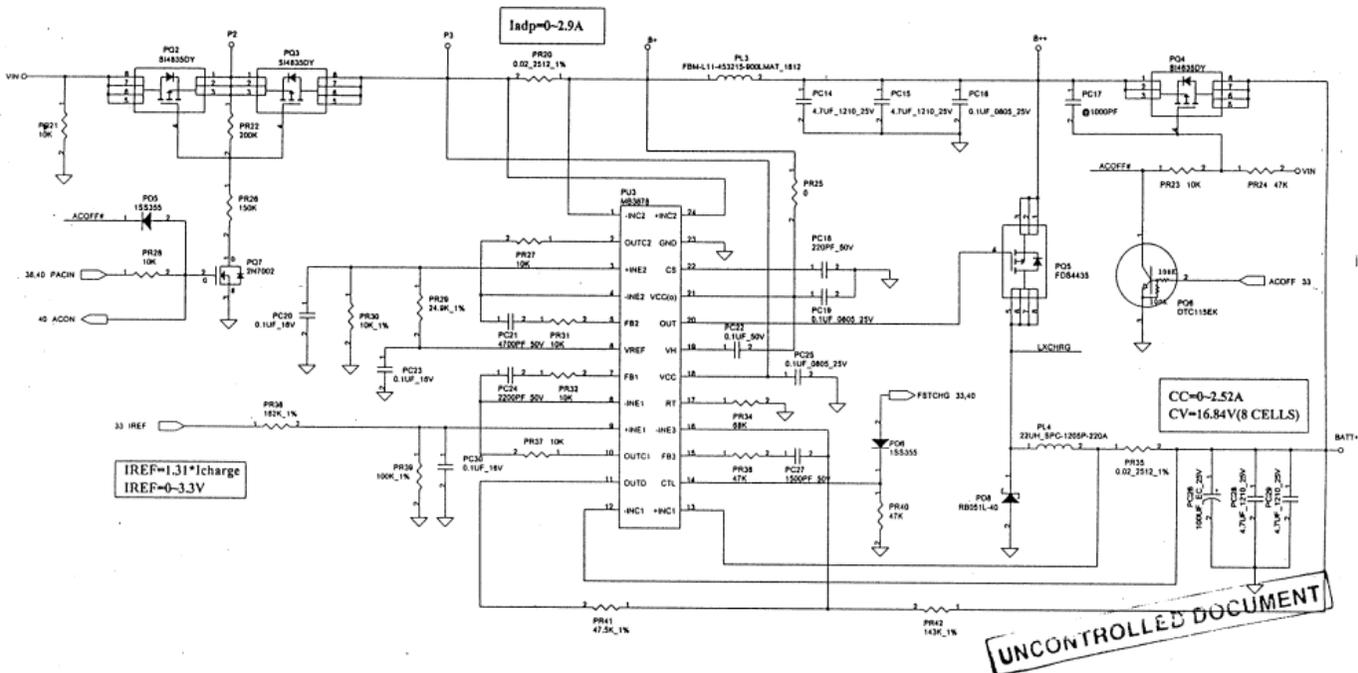
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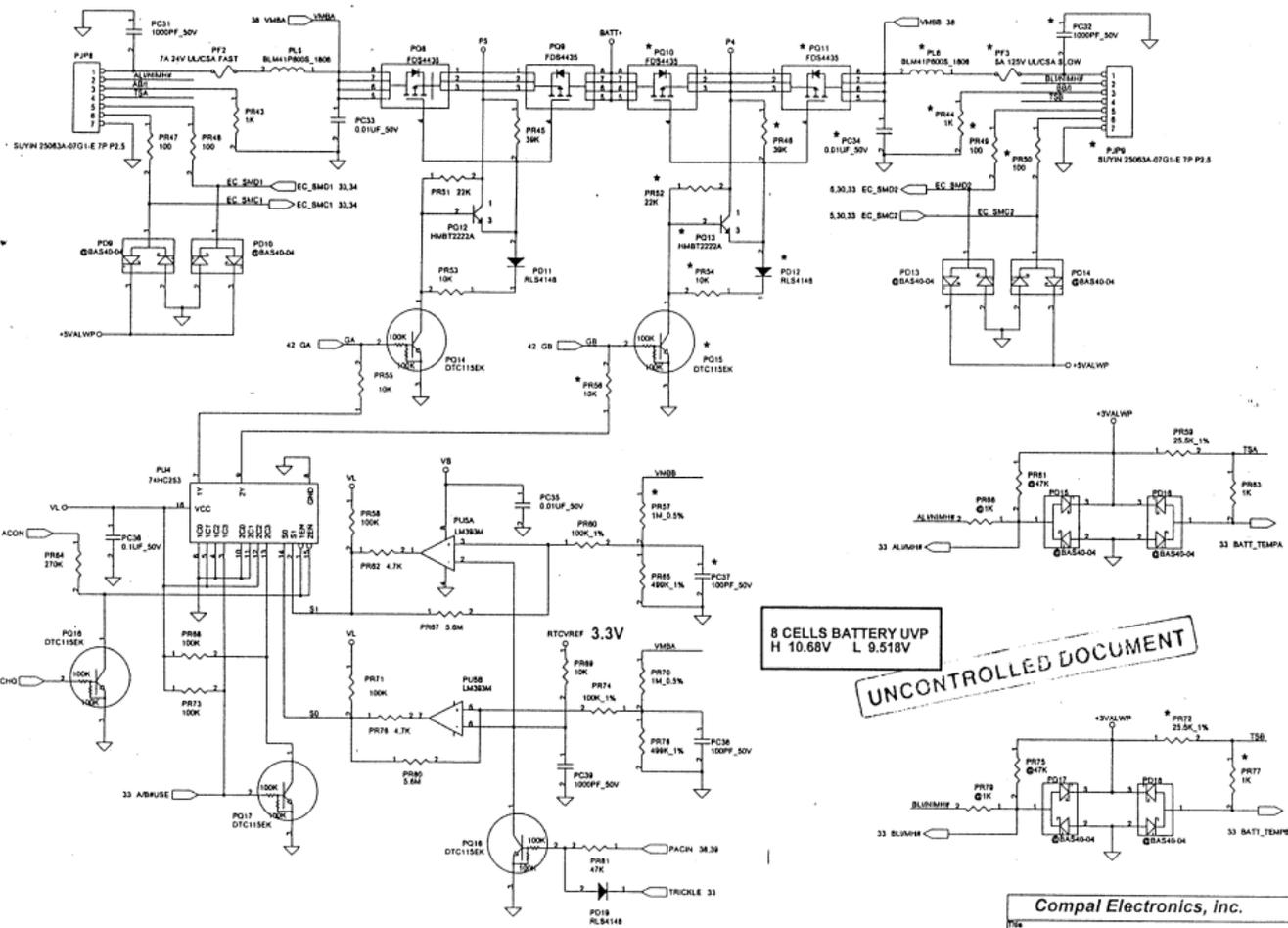
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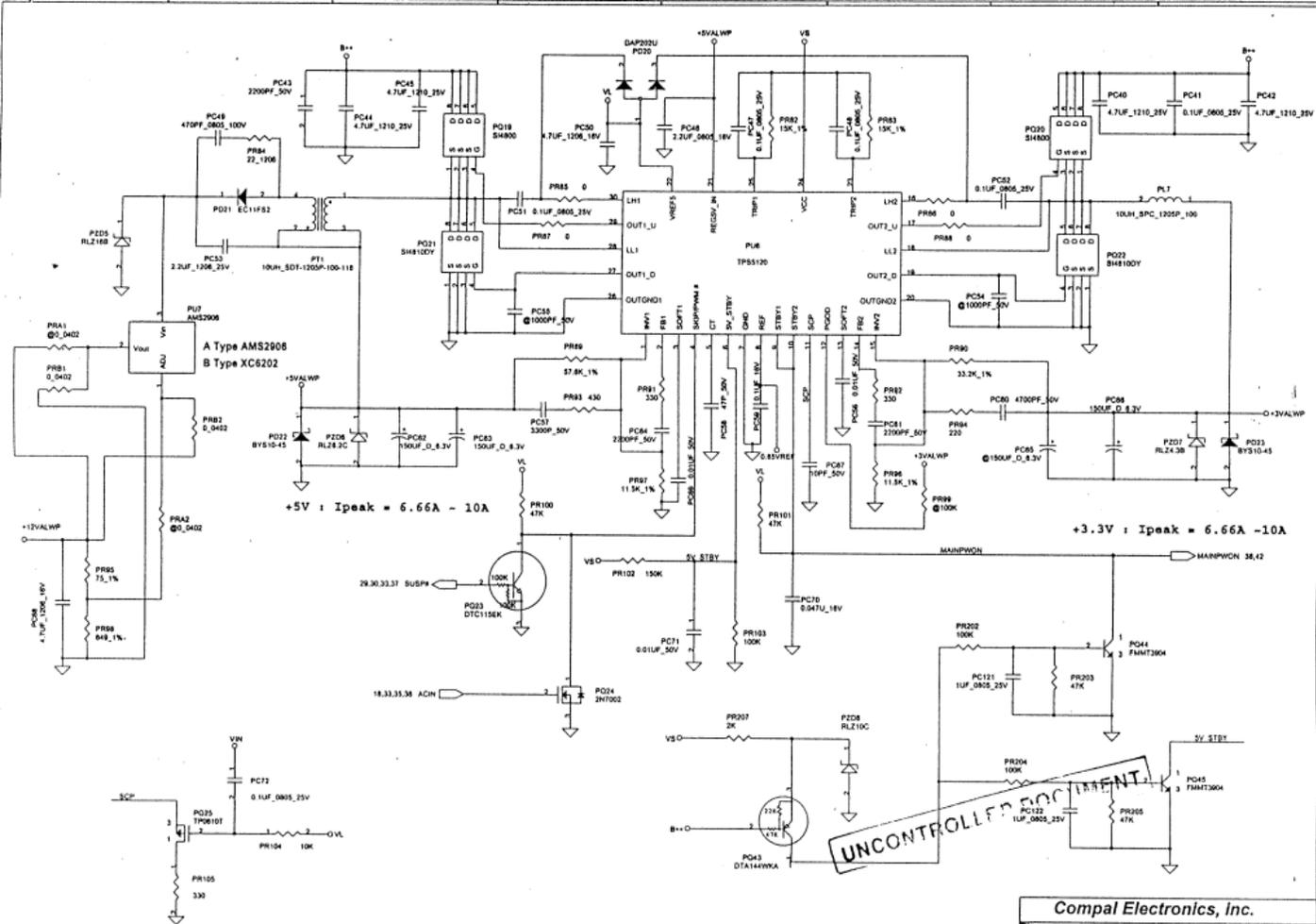
8 CELLS BATTERY UVP  
H 10.68V L 9.518V

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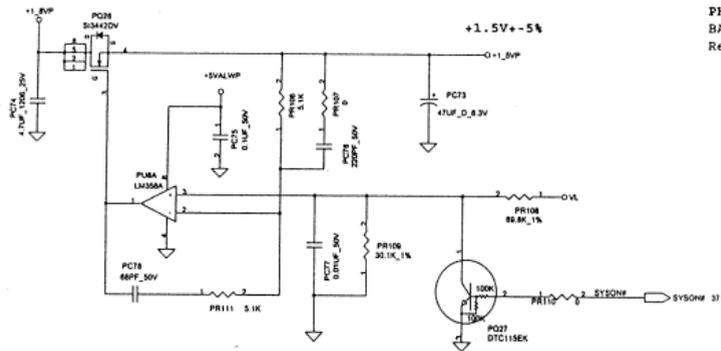
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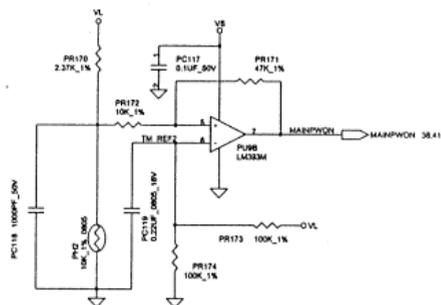
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Rev	1
Page	10

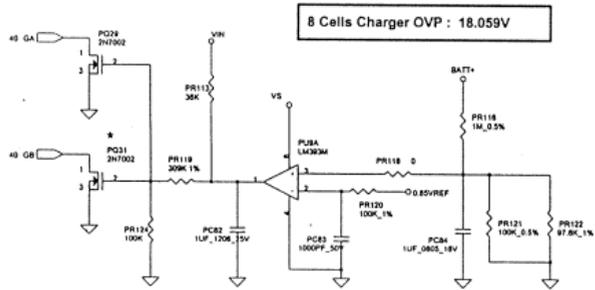
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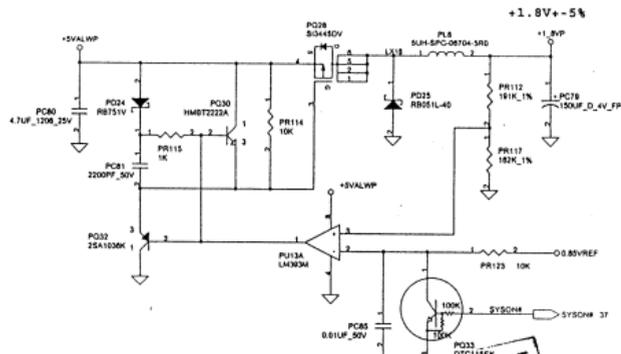
PH2 near main Battery CONN :  
 BAT. thermal protection at 73(74) degree C  
 Recovery at 50(51) degree C



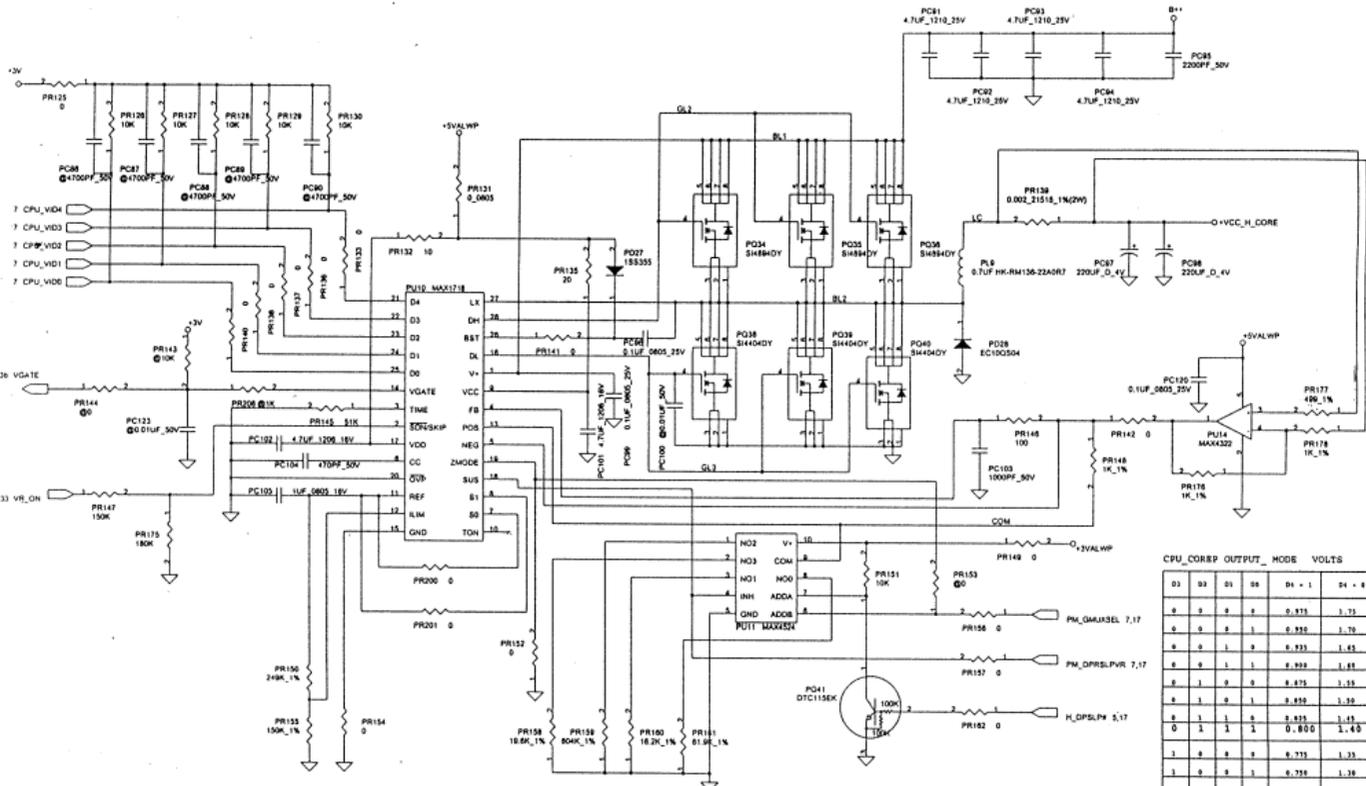
The \* Is DEL Item only for ACL00



8 Cells Charger OVP : 18.05V



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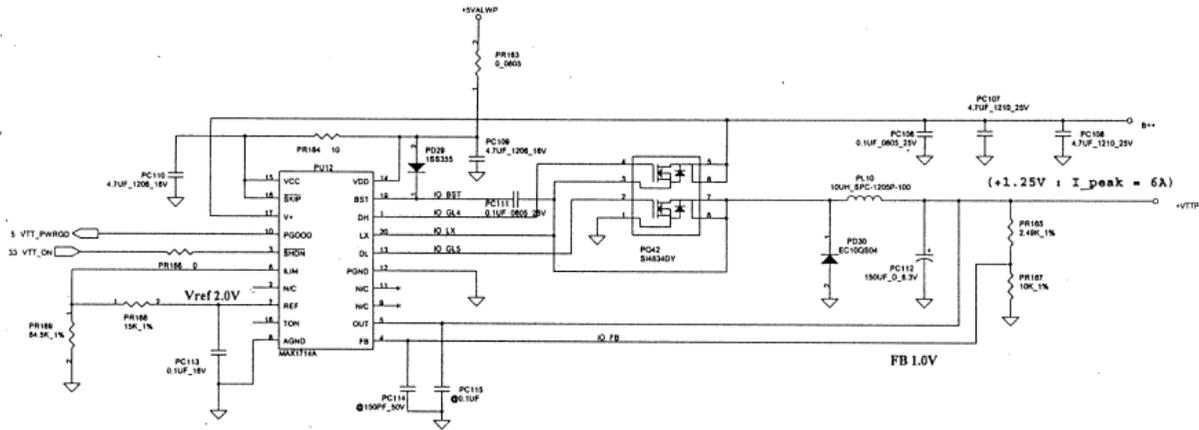
CPU\_CORSP OUTPUT MODE VOLTS

D3	D2	D1	D0	D1 - 1	D4 - 4
0	0	0	0	0.815	1.15
0	0	0	1	0.850	1.10
0	0	1	0	0.835	1.05
0	0	1	1	0.820	1.00
0	1	0	0	0.875	1.10
0	1	0	1	0.890	1.10
0	1	1	0	0.815	1.05
0	1	1	1	0.800	1.00
1	0	0	0	0.715	1.15
1	0	0	1	0.750	1.10
1	0	1	0	0.735	1.15
1	0	1	1	0.700	1.10
1	1	0	0	0.675	1.15
1	1	0	1	0.650	1.10
1	1	1	0	0.635	1.00
1	1	1	1	0.600	1.00

CPU CONTROL MODE

MODE	OFFSET	POSITION	V <sub>DD</sub> VAL	200A	200B
DEEPER SLEEP	0.0V	10K	0.800	0	0
PERFORMANCE SLEEP	0.1V	10K	0.800	0	0
BATTERY SLEEP	0.2V	10K	0.800	0	0
PERFORMANCE WAKE	1.8V	50K	1.75	0	0

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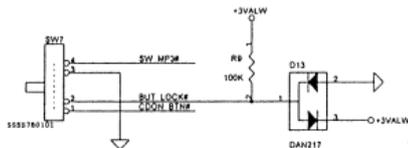
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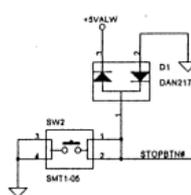
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PCB REV: **1.0**

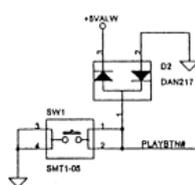
For MP3 / BUTTON LOCK / CD-PLAY



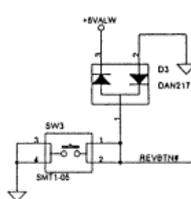
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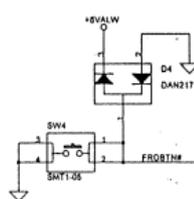
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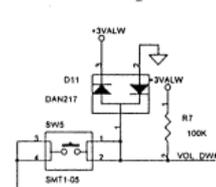
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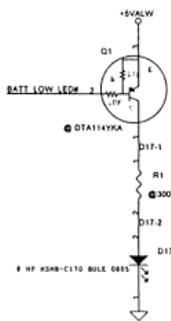
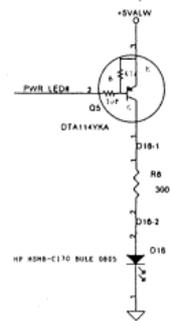
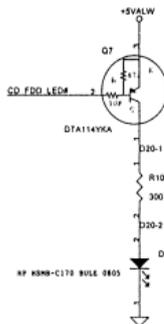
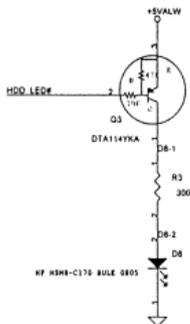
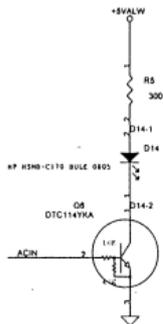
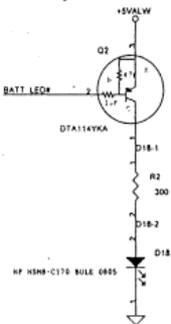
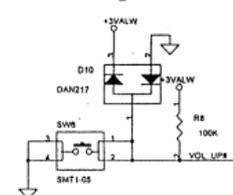
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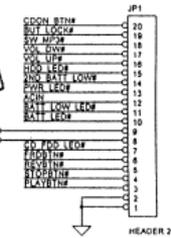
For VOL\_DWN



For VOL\_UP#



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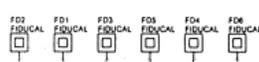
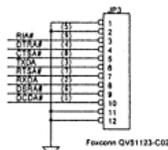
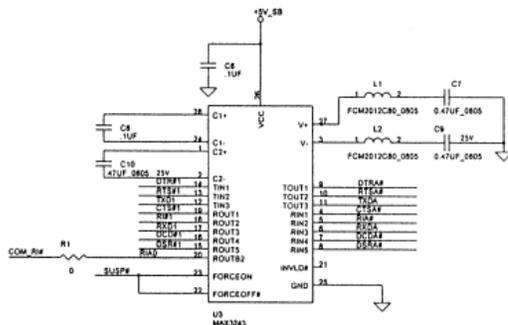
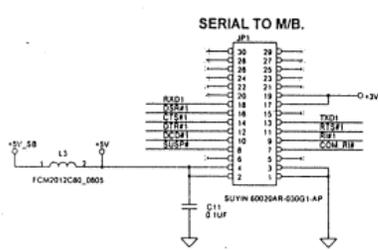
# COMPAL CONFIDENTIAL

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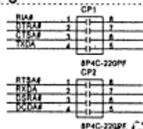
PCB NAME: **LS-1124 SERIAL BOARD**

PCB REV: **1.0**

## SERIAL PORT



Closed JP3

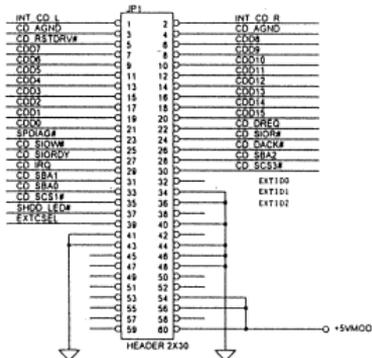


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# COMPAL CONFIDENTIAL

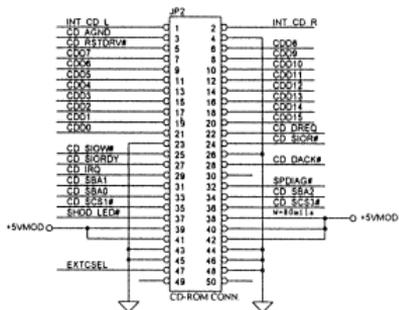
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 PCB REV: 1.0  
 COMPAL P/N:  
 TOSHBA P/N:  
 REWORK REV:

A1B Connector



CD ROM ID: 001

DVD Connector



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Compal Electronics, Inc.  
 SCHEMATIC, DVD/B LS-1085

U1A

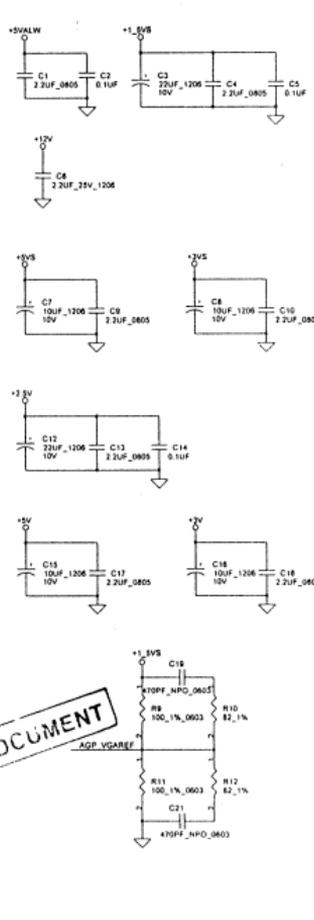
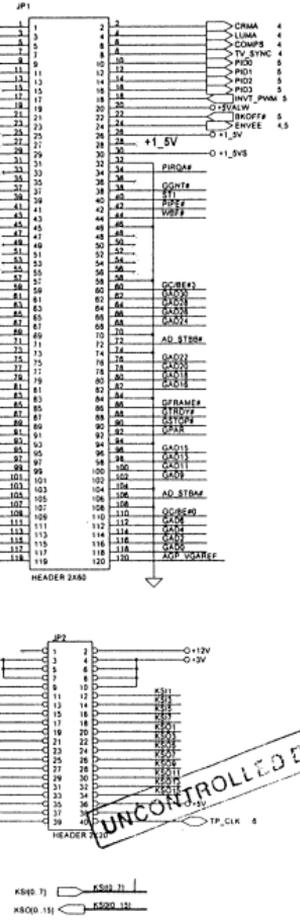
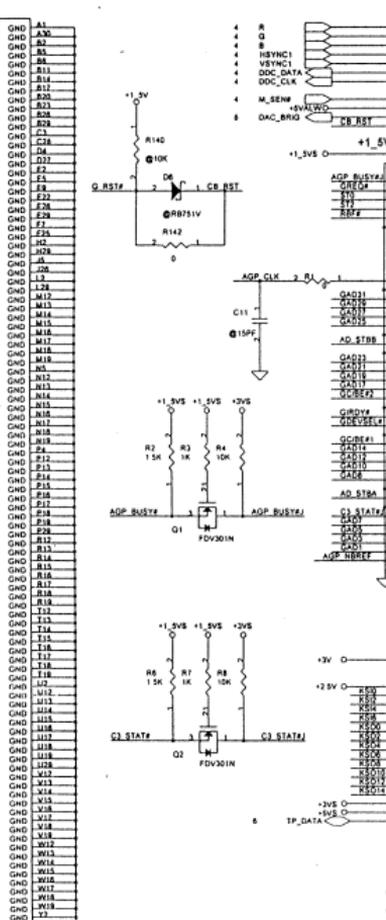
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HOST INTERFACE

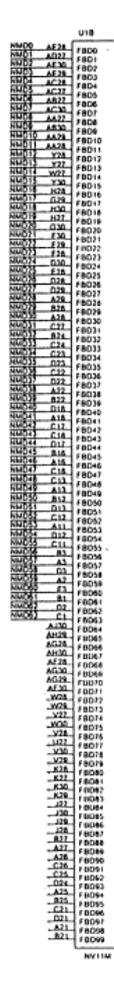
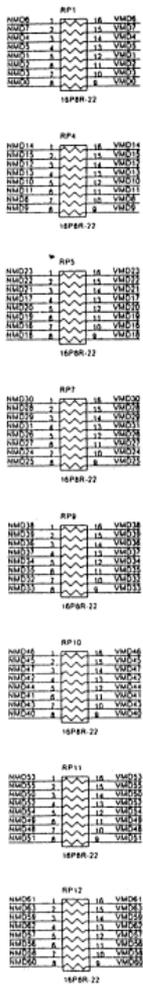
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PCI/AGP INTERFACE

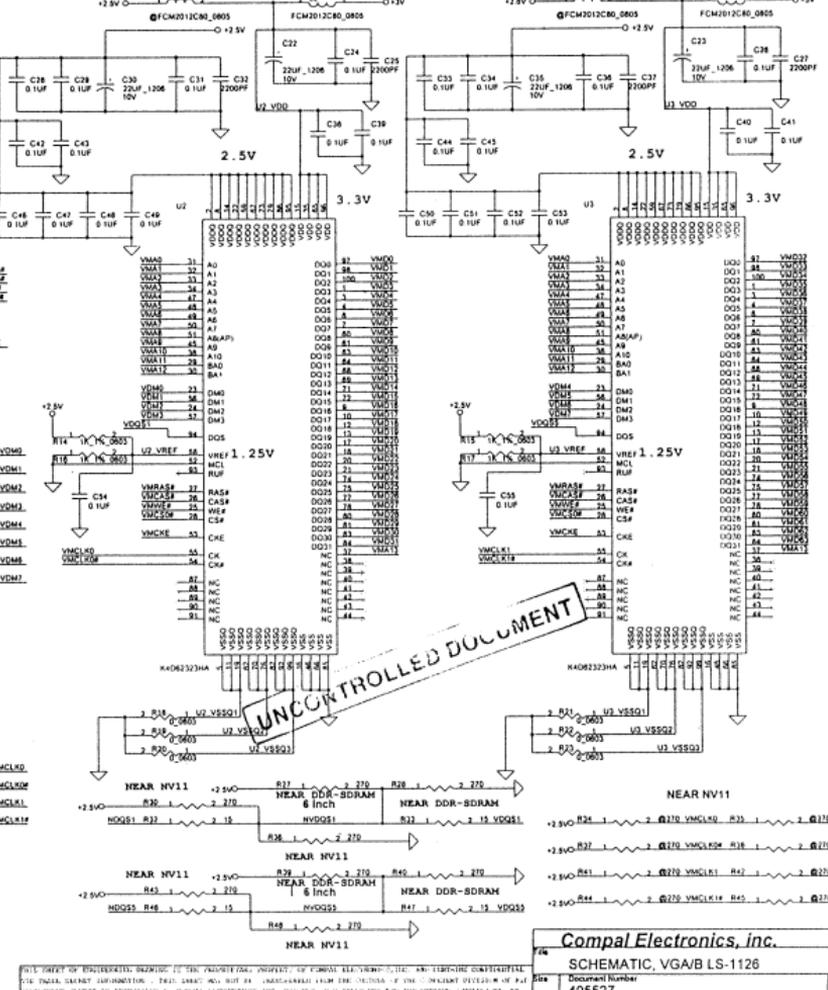
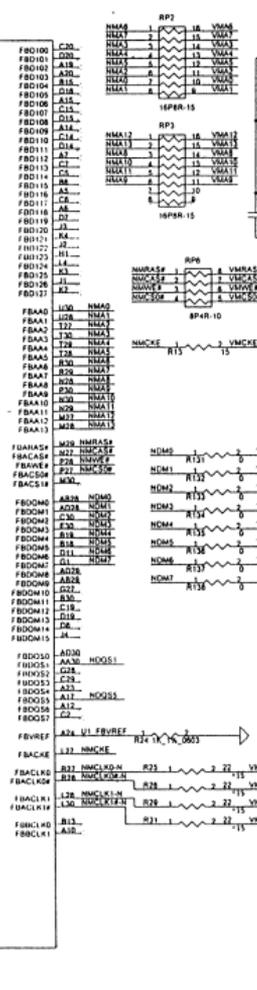
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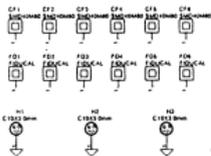
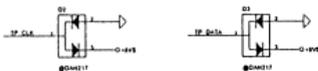
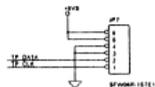
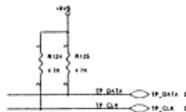
SDRAM/GRAM FRAMEBUFFER INTERFACE



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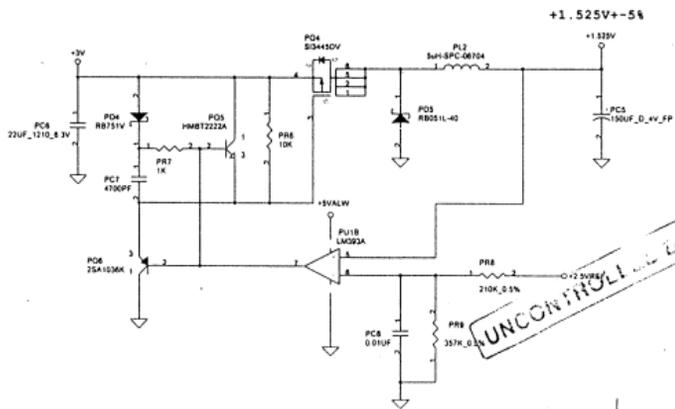
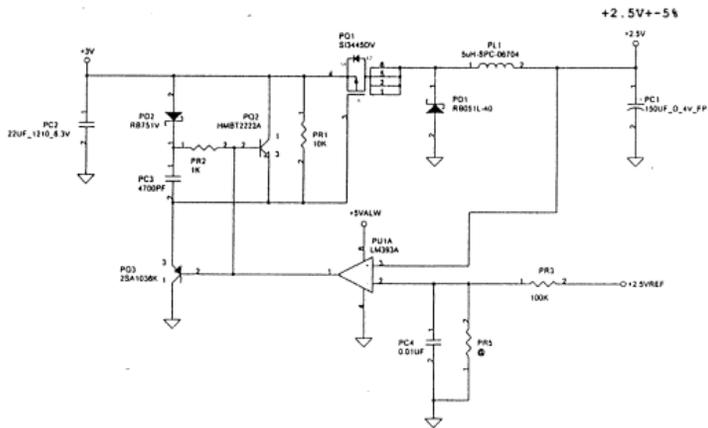






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Compal Electronics, Inc.

Schematic Number VG/A/B LS-1126

Revision Number 405527

Rev. 1A

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